Down-Converter Gilbert-Cell Mixer for WiMax Applications using 0.15µm GaAs HEMT Technology

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Abstract

The Worldwide Interoperability for Microwave Access, or WiMax, is a wireless communication technique based on IEEE 802.16 standards. Its advantage of sending high-data rates over long distances, while using a single base station to cover a large area, has made this technique a flexible and reliable solution for public wireless networks. WiMax has two main types of networks: *Fixed* and *Mobile*.

The most popular transceiver used in WiMax applications is the "Direct-Conversion Architecture" due to its high level of integration and less component requirements, which leads to reduced power dissipation.

In Direct Conversion Architecture, the mixer is a key block in the transceiver chain. Depending on design specifications and constraints, different types of mixers may be considered. However, the most appropriate *down converter* mixer for WiMax applications is the Gilbert-cell mixer. This thesis will then explore the design of a *down converter* Gilbert-Cell Mixer within the realm of Fixed WiMax technology. This design was achieved in the commercial circuit simulator Advanced Design System (ADS) using the 0.15mm InGaAs pHEMT technology process provided by Win Semiconductor Crop.

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I dedicate this thesis to my daughter, Mays

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List of Acronyms

Acronym	Definition
WiMax	Worldwide Interoperability for Microwave Access
BWA	Broad Band Access
MIMO	Multiple-Input Multiple-Output
OFDM	Orthogonal Frequency Division Multiplexing
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
ADC	Analog-Digital Converter
DAC	Digital-Analog Converter
IF	Intermediate Frequency
BB	Base Band
Tx	Transmitter
Rx	Receiver
LNA	Low Noise Amplifier
SNR	Signal to Noise Ratio
ADS	Advanced Design System
DC	Direct current
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IMD	Intermodulation Distortion
RF	Radio Frequency
HB	Harmonic Balance
SSB	Single Side Band
DSB	Double Side Band

List of Variables

Variables	Definition
Grx	Receiver Antenna Gain
Gtx	Transmitter Antenna Gain
NF	Noise Figure
F	Noise Factor
P1dB	Output Power at 1 dB compression
G	Gain
IIP3	Third Order Input Intercept Point
IMD3	Third Order Intermodulation Distortion
OIP3	Third Order Output Intercept Point
Gm	Transconductance
Ft	Transition Frequency
Fmax	Maximum Frequency

Chapter 1. Introduction

1.1. Motivation

The ever-higher demand for high speed and data rates as well as more secure communication links makes the WiMax technology an essential topic to discover. In addition, WiMax can cover long distance areas with fewer base stations compared to other wireless technologies, thus involving lower costs in maintenance, operation, and management. WiMax technologies theoretically can deliver 70Mb/s over long distance of 30 miles. There are two categories of WiMax: *Fixed* and *Mobile.* Each type has its own advantages and services. Typically, a fixed WiMax station can cover up to 5 miles, thus providing last-miles access to people living in rural areas to keep them in touch through telephony/internet services. On the other side, mobile WiMax systems can cover up to 2 miles. They are mainly devoted to people who use laptops and smartphones to access Internet services as well as mobile telephony systems such as Voice over IP (VoIP). In this work, the Fixed WiMax was retained because of its larger coverage, a key issue in Canada.

In WiMax technologies, the most popular RF transceiver used is the “Direct-Conversion Architecture.” Direct Conversion Architecture is dominant over other configurations due to its high level of integration and less component requirements, which leads to reduced power dissipation.

In a WiMax receiver, the down converter mixer is one of the most important elements to consider. However, due to its design complexity, few of papers have been published in this topic. Depending on the desired performance, various parameter objectives

should be targeted while designing a mixer, such as high conversion gain, 1dB compression point (P-1dB), port-to-port isolation, input second-order intercept point (IIP2) and input third-order intercept point (IIP3) as well as low noise figure (NF) and voltage supply. In practice, these parameters cannot be achieved simultaneously; improvements in certain aspects of the circuit performance lead to a degradation in others. So, based on the design constraints and standard specifications, different mixer types and topologies can be considered. The transistor mixer is selected in our design due to its advantages of providing conversion gain and low LO power compared to diode mixer. In the transistor mixer, the most appropriate *down converter* mixer for WiMax applications is the Gilbert-cell mixer. The Gilbert-cell mixer has advantages when compared to other mixers, such as single, dual-gate, and single balanced mixers due to inherent ports isolation, acceptable gain, moderate linearity, and cancel the even harmonics distortion.

In this thesis, different mechanisms discussed to develop the Gilbert cell mixer performance including folded mixer, current reuse mixer and current bleeding mixer. Mainly, the current bleeding or charge-injection technique is utilized to improve the Gilbert cell performance including the conversion gain and noise figure. Using this technique presents good result compared with other work that published in this field. The Gallium Arsenide (GaAs) semiconductor shows low noise figure, high transconductance (g_m) and high cut-off frequency (f_t). The transistor is sized based on the low noise figure and low power dissipation. The Gilbert cell mixer exhibits a conversion gain of 5.1 dB, an IIP2 of 36 dBm, an IIP3 of 1 dBm, as well as a noise figure for both single side band and double side band of 11.4 and 8.4 dB, respectively.

The design of the *down-converter* mixer including schematic, layout and co-simulation was achieved in the commercial circuit simulator from Agilent Technologies, i.e., the Advanced Design System (ADS) simulator. This mixer design is simulated using the 0.15mm InGaAs pHEMT technology process provided by Win Semiconductor Crop.

1.2. Thesis Contributions

In this thesis, the WiMax technology was investigated and a down-converted Gilbert-cell mixer designed and its layout generated. The simulated results of this Gilbert-cell mixer show that this device meets the WiMax standards and thus, can be successfully compatible with existing designs (even if relatively few papers have been published in this topic due to the complexity of the design).

1.3. Thesis Overview

This thesis is divided into five chapters. After an introductory Chapter, Chapter 2 presents an overview of WiMax systems as well as different receiver architectures and WiMax requirements. Also, the link budget for a WiMax receiver system is calculated.

In the third chapter, the basic mixing process is described including mixer definition and characterizations. In addition, different mixer topologies are presented and discussed.

Chapter 4 provides the design, implementation and results for the down-converter Gilbert cell mixer using the 0.15 GaAs HEMT technology. The circuit schematic and layout are designed in the Advanced Design System (ADS) simulator. In addition, the simulation results for conversion gain, noise figure and linearity are shown and successfully compared with other works.

Chapter 5 summarizes the thesis, clarifies the major contributions and points to potential future works.

Chapter 2. WiMax Overview

2.1. WiMax Principle

In 1998, the Institute of Electrical and Electronics Engineers (IEEE) organization initiated a standard called 802.16 to develop wireless metropolitan area networks, or MAN, for broadband wireless access (BWA). This standard was designed to operate on the line-of-sight at 11-66 GHz for high-speed data where optic fibers are prohibited. Later, this standard was improved to include non-line-of-sights, at licensed and unlicensed frequencies from 2 to 11 GHz. The last modifications were labeled IEEE 802.16-2004 for fixed wireless and IEEE 802.16-2005 for mobile wireless. Worldwide Interoperability for Microwave Access, or WiMax, is a wireless telecommunication technique based on the IEEE 802.16 standard, which provides high data over long distances. WiMax can theoretically deliver data up to 70 Mb/s over a coverage area of 50 km by using smart antennas such as Multi Input Multi Output (MIMO) technique. The standard spectrum of WiMax is allocated at 2.3 GHz, 2.5 GHz, 3.3 GHz, 3.5 GHz, and 5.8 GHz frequency bands as depicted in Figure 1 [1][2]. In addition, the channel bandwidth varies from 1.25 MHz to 20 MHz. In order to enhance the multipath performance, orthogonal frequency division multiplexing (OFDM) is utilized along with different types of modulations, such as BPSK, QPSK, 16QAM and 64QAM [1][3][4][5].

WiMax users can utilize many services in point-to-point and point-to-multipoint deployments such as Voice Over IP (VOIP), Internet Protocol Television (IPTV), video conferencing, multiplayer interactive gaming, web browsing and wireless backhaul for Wi-

Fi hotspots. For fixed wireless WiMax, there are many advantages over other wireless systems like Wi-Fi: WiMax can transfer and handle up to 70Mb/s for long distances, while the Wi-Fi system can cover around 100 feet [2]. This main advantage sheds light on other important aspects: the number of base stations needed in such areas is fewer compared to other technologies, and the maintenance, operation, and management can lead to lower costs. In addition, the high demands for increased data and speed rates have made the Wi-Max a significant topic of discussion [4] [5]. Figure 2 shows how WiMax works in different modes [5]. The first mode is line-of-sight backhaul, which operates from 11 to 66 GHz, while the second mode is non-line-of-sight transmission, which operates at lower frequencies (2 to 11 GHz). This mode utilizes point-to-multipoint deployment as depicted in Figure 2.

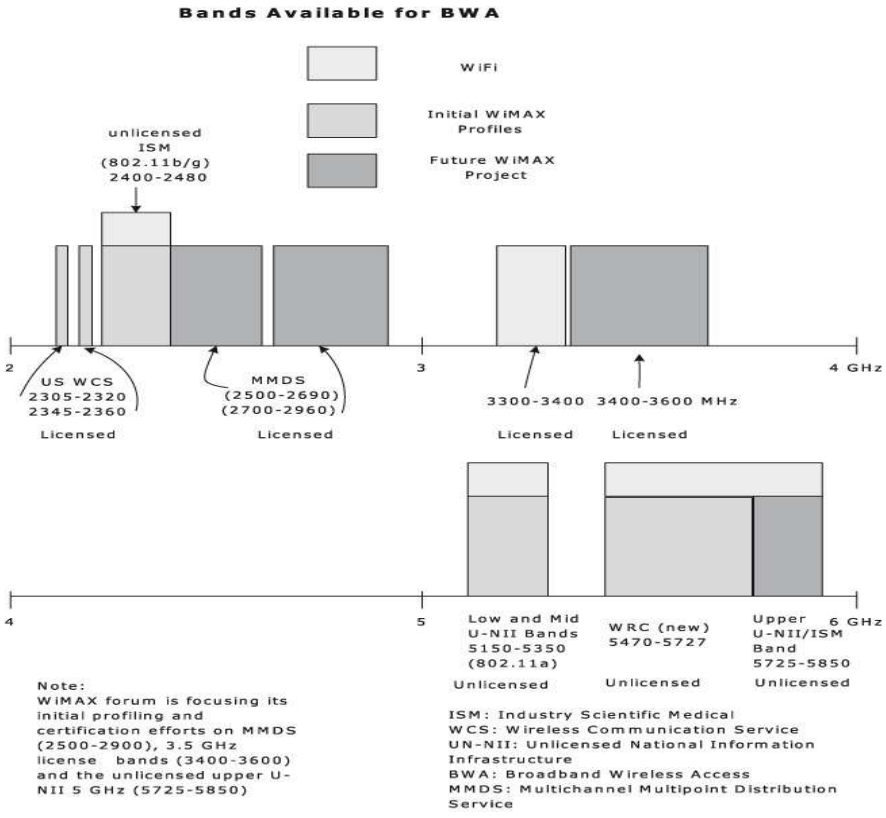


Figure 1 WiMax Spectrum [2]

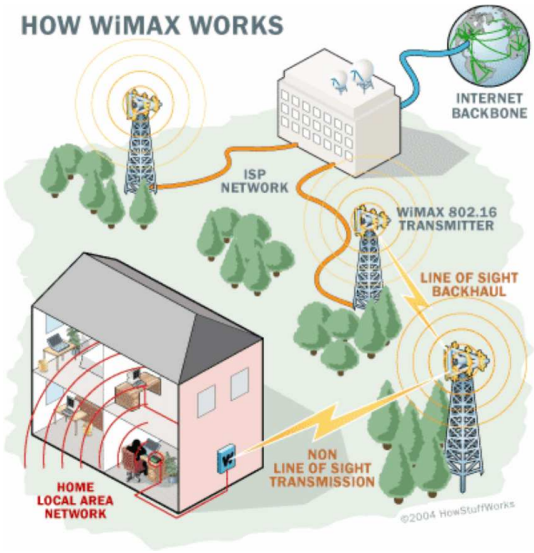


Figure 2 Different Modes of WiMax [5]

2.2. WiMax Receiver Architecture

The widely accepted definition of an RF transceiver is where the receiver starts from the antenna to the *analog-to-digital converter* (ADC), and an RF transmitter acts in the opposite way, moving from a *digital-to-analog converter* (DAC) to a transmitter antenna. The RF receiver (Rx) and transmitter (Tx) are also defined by the intermediate frequency (IF) and analog baseband (BB) circuitry. There are many blocks used in RF transceivers, including frequency filters, amplifiers, down-up converter mixers, modulator/demodulators, oscillators, synthesizers, signal coupler/divider/combiner/attenuators, switches, etc. An RF transceiver usually utilizes most of these blocks, but never all of them. The most popular architectures used in RF transceivers in wireless communication systems are *Superheterodyne architecture* and *direct conversion architecture.*

2.2.1 Superheterodyne Architecture

This configuration is widely used in wireless communications. It uses two stages for conversion. First, it down-converts the RF signal to an intermediate frequency (IF) signal by mixing the RF with a local oscillator (LO). Then, it transfers the IF signal to baseband by mixing the IF signal with another LO or voltage controlled oscillator (VCO). It has advantages, such as control for receiver gain, noise figure, better performance, and it is robust. On the other hand, it has some drawbacks, including a larger circuit that leads to more complexity for circuit designers, and high power consumption. Also, there is an unwanted image signal that needs adequate image filtering (SAW) to prevent interferences before the mixing stage [6] [7].

In Figure 3, the upper part represents the receiver blocks and the bottom section refers to the transmitter blocks. As shown in this figure, the duplexer and the LO operate at the same band for Tx and Rx. There are also two band-pass filters that are mainly used as pre-selection filters, as well as to reduce the leaking power at the receiver end. Also, on the transmitter side, the band-pass filter is used to suppress the noise of the transmission band. The main advantage of the duplexer is that it reduces the transceiver current and cost.

The Superheterodyne receiver is divided into three parts: RF, IF, and BB. The RF section usually contains the duplexer as band-pass filter pre-selection, a low noise amplifier (LNA), a RF band-pass filter (BPF), a RF amplifier, which acts as pre-amplifier for the mixer, and a RF-to-IF down-converter (mixer). The LNA is necessary to obtain better receiver sensitivity while its gain can control the receiver dynamic gain. The BPF is a SAW filter, which can suppress leakage and other interferences. The pre-amplifier injects sufficient gain for the rest of the receiver. Therefore, the noise figure of the mixer and the next

stages will have minor effects on the overall receiver noise and sensitivity. The down-converter is utilized for frequency translation from RF to IF frequency. The next block after the mixer is the IF amplifier followed by the IF SAW, used to prevent unwanted signals and for high channel selection filtering. The I/Q demodulator contains the second frequency down-converter that converts the signal from IF to BB. The demodulator has two In-phase/Quadrature (I/Q) mixers. A low-pass filter (LPF) is located after the BB mixer to prevent unwanted signals and other interferences, and followed by a BB amplifier. The last block in this architecture is the ADC, which converts the amplified analog signal to a digital one for more processing in digital band. On the transmitter side, it works almost in the same manner [6].

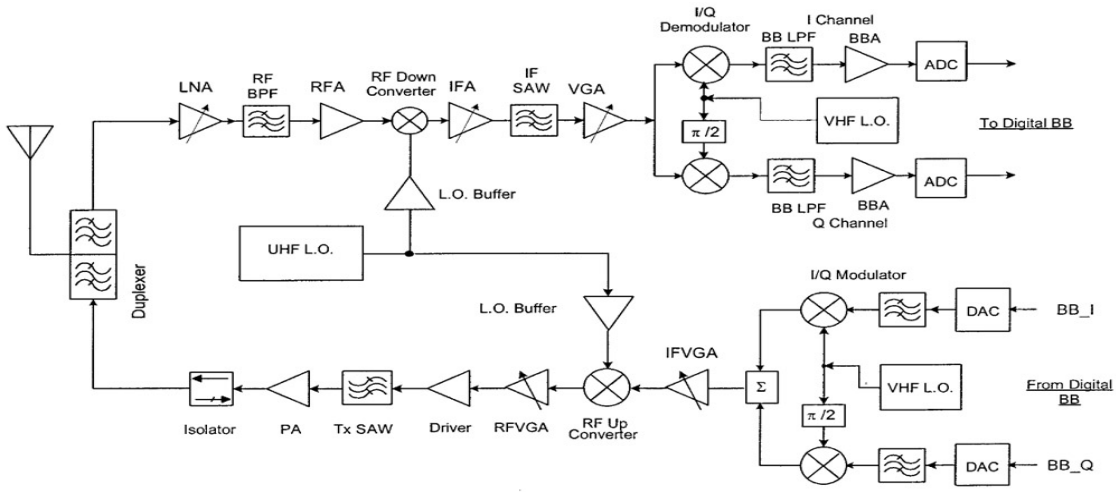


Figure 3 Block Diagram of Super-heterodyne Transceiver [6]

2.2.2 Direct Conversion Architecture

The direct conversion is the process of conversion of the RF signal directly to the BB signal with zero intermediate. Therefore, it is also called zero IF architecture. In addition, this receiver is referred to as homodyne because the LO frequency is equal or close to

the receiver input signal frequency. The direct conversion has many aspects that makes it very appealing. First, the receiver has no IF stage; therefore, it can reduce size and cost, and can save the transceiver power by removing the IF passive filter (SAW filter). Also, there is no image issue in this configuration. The active low-pass filter can be used to implement the filtering of channel for the direct-conversion in analog baseband as this type of active filter can be considered as changeable. Thus, it is easy to design the receiver working in multimode band.

As shown in Figure 4, the direct conversion transceiver has usually two stages, the RF and the BB. The receiver and transmitter have different oscillators because they are working in different frequency bands. In order to prevent power leakage and other interferences, a band-pass filter has been included in the duplexer. The LNA amplifies the income receiver signal selected by the BPF. In direct conversion, the RF filter should be stronger than the filter in Superheterodyne receiver in order to overcome the self-mixing issue and reduce the second order distortion requirements in the next stage, called the down-converter mixer stage. The filtered signal converts the signal to I and Q signals via a 90^{o} quadrature demodulator. The quadrature mixing reduces the phase mismatch between the LO and the incoming signal. Most of the receiver's gain (around 75%) is obtained by the baseband stage operating at high gain mode. Therefore, it has the advantage of saving power. The gain in the RF stage is classified as power gain, while in the BB stage it is categorized as voltage gain. The signal amplified and filtered is converted to digital for further process[6] [8].

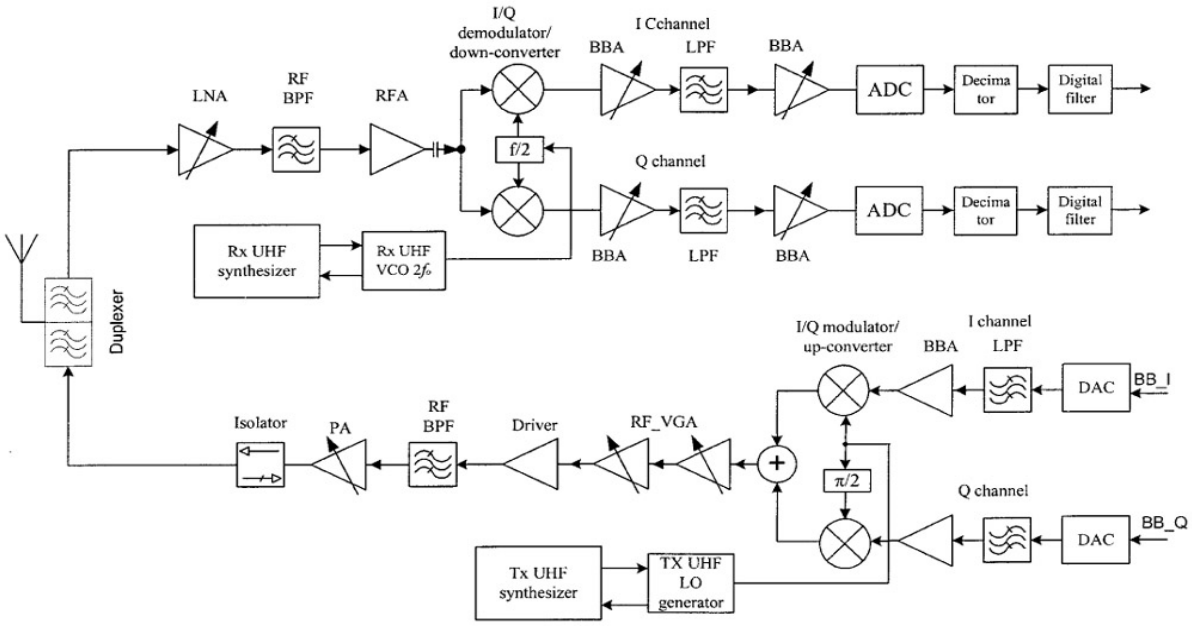


Figure 4 Block diagram of Direct-conversion Transceiver [6]

Superheterodyne architecture has a superior performance compared to others. Noteworthy, the *direct conversion* or *homodyne* configuration has become a preferred architecture for wireless systems, because it cancels the image (assuming perfect quadrature) and eliminates some blocks (like filters) that lead to savings in size, cost, and power dissipation [6]. —Table 1 shows the comparison of heterodyne vs. direct conversion architectures in terms of most important parameters to consider during design.

Compared to other configurations, direct-conversion receiver architecture is indeed widely used in WiMax [1][3][9][10][11]. This has dominated other configurations mainly because of its high level of integration.

However, it has still challenges to overcome. First, DC offset and noise flicker occur as a result of converting directly to DC. Also, the LO, RF, and LNA ports are not well isolated, thus possibly causing leakage at the ports [6][9] .

Nevertheless, the advantages outweigh the disadvantages, making direct conversion easier to handle when trying to meet technical specifications.

Table 1 Design Parameters to Consider for Different Receiver Architectures.

Description	Heterodyne configuration	Direct Conversion configuration
Linearity	IIP3	IIP3, IIP2
Noise figure	SSB	DSB
Power dissipation	High	Low
Image	Need Filter	NO Image
Complexity	More	Less
Level of integration	Low	High
DC offset	No DC offset	Need to care the DC offset
Size & cost	Large & expensive	Small & inexpensive

2.3. WiMax Requirements and Link Budget

Receiver requirements are defined and set up by the IEEE 802.16 standard and the Wireless Metropolitan Area Network (Wireless MAN™) standard [1][13][14][15]. These standards specify the frequency operation, the channel bandwidth, the type of modulation, the signal-to noise ratio (SNR, Table 2), the receiver noise figure, and other technical parameters). As reported in Table 3 for the 64-QAM modulation, different operating frequencies and channel bandwidth are allocated for WiMax. In this work, the 3.5 GHz frequency band and the 7 MHz channel bandwidth have been selected based on the data provided by

the IEEE 802.16-2004 standard [1][3][9][11][13]. For more generality, the receiver and transmitter antennas are different (different gain).

Table 2 WiMax Receiver SNR [14]

Modulation	Code rating	Receiver SNR [dB]
BPSK	1/2	6.4
QPSK	1/2	9.4
	3/4	11.2
16-QAM	1/2	16.4
	3/4	18.2
64-QAM	2/3	22.7
	3/4	24.4

Table 3 WiMax Specifications for the 64-QAM Modulation

Item	Value
Operation Frequency	2-6 GHz
Channel Bandwidth (BW)	6, **7**, 12, 14 MHz
Modulation	64-QAM
Signal to Noise Ratio (SNR)	24.4 dB
Max. Distance between Rx and Tx	3.5 km
Transmitter maximum Power (P_{TX})	29.5 dBm
Transmitter antenna Gain (G_{TX})	0 dBi
Receiver antenna Gain (G_{RX})	11 dBi
Receiver maximum input	-30 dB
Receiver maximum Noise figure	5 dB

2.3.1 Receiver Link Budget Calculation:

Studying and calculating the link budget for the receiver is crucial to understand and measure its performance requirements. In addition, it is also crucial in determining the capability of each block in the front-end receiver. As discussed, the most common front-end receiver used in WiMax is the direct-conversion architecture (Figure 5) [1].

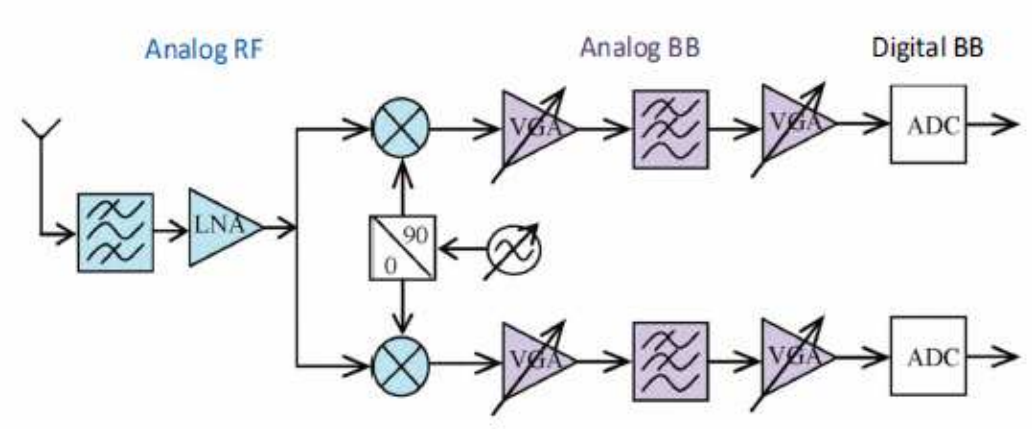


Figure 5 WiMax Direct-conversion Architecture [1]

In this section, the receiver specifications are calculated for the major blocks in the direct-conversion architecture.

2.3.2 Receiver Sensitivity:

The sensitivity of the receiver is a very important parameter that determines the minimum desired signal strength (MDS), or the weakest signal to get the bit error rate needed for the receiver. It is measured by the total noise figure of the receiver (nt). The receiver sensitivity can be expressed as [16].

$$\boldsymbol{Sensitivity = Rss = NF + SNR + nt} \quad (2.1)$$

and

$$\boldsymbol{Rss = 5 + 24.4 + KTB}$$

where

$$\boldsymbol{nt = KTB = -174 + 10\,log(BW)}$$

$$\boldsymbol{Rss = 5 + 24.4 + (-174) + 10\,log(BW) = -76.1\ dBm}$$

In the above equations, NF is the noise figure, set to 5 dB [6][13][16][17]. The main parameters that characterize a direct conversion receiver are the gain, noise figure, linearity and P1-dB compression point. Because the WiMax receiver architecture can include several stages (Duplexer, LNA, Mixer, filter …, Figure 5), the above parameters need to be specified for each of these blocks based on the WiMax receiver requirements. First, the WiMax duplexer, taken from Network International Corporation (NIC), exhibits a 1.5 dB max insertion loss [18]. Then, according to the WiMax specifications, the gain and noise figure of the low noise amplifier were selected as 14 dB and 2 dB at 3.5 GHz, respectively [19][20]. Therefore, the parameters related to linearity and noise figure can be deduced through the following steps.

2.3.3 Low Noise Amplifier and Mixer Specifications

A- LNA:

To obtain the linearity and maximum power signal requirements for the LNA, a maximum power signal has to be set. Therefore, an acceptable interference distance *d* for mesh architecture in WiMax standard has to be stated. Based on the IEEE 802.16 standard for fixed broadband wireless access operating at f = 3.5 GHz [13], d = 100m.

Thus, the corresponding free space path loss (FPLS) is

$$\boldsymbol{FSPL = 10\, log_{10}\left(\frac{4\times\pi\times d\times f}{c}\right)^2 = 83.3\ dB} \qquad (2.2)$$

with *c* the light speed ($3x10^8$m/s). Therefore, the maximum received power between two antennas that spread over a distance *d* and operating at a specific frequency *f* can be calculated using the Friis transmission equation [21][22], the receiver being considered as a cascaded system (Figure 6).

$$\boldsymbol{Pi = P_{TX} + G_{RX} - FSPL + G_{TX} + G_{Dublexer}} \qquad (2.3)$$

$$\boldsymbol{= 29.5 + 11 - 83.3 + 0 - 1.5 = -44.3\ dBm}$$

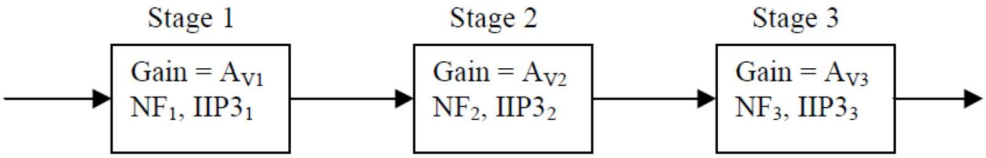


Figure 6 Receiver System with Three Cascade Stages [17]

The LNA linearity parameters, i.e., the third order input/output intercept points (IIP_3 *and* OIP_3) as well as the gain compression point (P_1_dB) can be obtained through the following equations [6][16]. These parameters are summarized in Table 4.

$$\boldsymbol{IIP_{3\ LNA} = \frac{3\times Pi - IMD_3}{2}} \qquad (2.4)$$

$$\boldsymbol{= \frac{3\times(-44.3) - (-76.1 - 29.4)}{2} = -13.7\ dBm}$$

then,

$$\boldsymbol{OIP_{3\,LNA} = IIP_{3\,LNA} + LNA\ Gain} \qquad (2.5)$$

$$\boldsymbol{OIP_{3\,LNA} = -13.7 + 14 = 0.3\ dB}$$

$$\boldsymbol{P_1dB_{LNA} = OIP_{3\,LNA} - 10\ dB = -9.7\ dBm} \qquad \textbf{for one tone} \qquad (2.6)$$

$$\boldsymbol{P_1dB_{LNA} = OIP_{3\,LNA} - 15dB = -14.7\ dBm} \qquad \textbf{for two tones}$$

Table 4 LNA Specifications

Description	**Value**
Gain	14 dB
NF	2 dB
IIP3	-13.7 dBm
OPI3	0.3 dBm
P1_dB (one tone)	-9.7 dBm
P1_dB (two tones)	-14.7 dBm

B- BB Mixer:

First of all, the mixer input has to be set up. Therefore, due to the duplexer loss and LNA gain, the mixer input is going to be between -20 to -15dBm. In addition, by considering cascade blocks, mixer parameters can be determined [6][16]. In the Direct Conversion Configuration (DRC), the spectrum is centered close to zero. *DC* components generated by second order will directly impact the system performance of direct conversion receivers[6]. Therefore, the second order (IP2) must be carefully investigated during design.

In our application, the gain and the noise figure of the BB mixer was set up to 5 dB and 11 dB, respectively [23][24]. Hence, the IIP3, OIP3, P1-dB, IIP2 and OIP2 can be obtained as

$$\boldsymbol{IIP_{3\,Mixer} = OIP_{3LNA} = +0.3\ dBm}$$

$$\boldsymbol{OIP_{3\,Mixer} = IIP_{3\,Mixer} + Gain_{Mixer} = 0.3 + 5 = +5.3\ dBm}$$

$$\boldsymbol{P_1dB_{Mixer} = OIP_{3\,Mixer} - 10\ dB = -4.7\ dBm}$$ for one tone

$$\boldsymbol{P_1dB_{Mixer} = OIP_{3\,Mixer} - 15\ dB = -9.7\ dBm}$$ for two tone

$$\boldsymbol{IIP_2 = 2 \times Pi - IMD_2}$$

$$\boldsymbol{= 2 \times (-30.3) - (-63.6 - 29.5) = 32.4\ dBm}$$

$$\boldsymbol{OIP_2 = IIP_2 + Gain = 33.4 + 5 = 38.4\ dBm}$$

The total noise for the system is 5 dB [13]. Based on the Friis transmission equation [26] given for *n* stages as

$$\boldsymbol{F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}} \qquad (2.8)$$

with

F_T = overall system noise factor

F_k = noise factor of the k^{th} stage

G_k = power gain of the k^{th} stage

We have

$$\boldsymbol{NF_{LNA\ input} = NF_{system} - Duplexer\ instersion\ loss} \quad (2.9)$$

$$\boldsymbol{NF_{LNA\ input} = 5 - 1.5 = 3.5\ dB}$$

Knowing that the noise factor *F* is related to the noise figure *NF* as [16]

$$\boldsymbol{NF = 10\log(F)\ dB} \qquad (2.10)$$

$$\boldsymbol{F = 10^{NF/10}} \qquad (2.11)$$

the noise factor F_{rest} at the mixer input can be expressed as

$$\boldsymbol{F_{inputLNA} = 10^{0.1*3.5} = 2.23 \quad and \quad F_{LNA} = 10^{0.1*2} = 1.58}$$

$$\boldsymbol{F_{G\ LNA} = 10^{0.1*14} = 25.1}$$

$$\boldsymbol{F_{input\ LNA} = F_{LNA} + \frac{F_{rest} - 1}{F_{G\ LNA}}}$$

$$\boldsymbol{F_{rest} = \left(F_{input\ LNA} - F_{LNA}\right) * F_{G\ LNA} + 1 = 17.3}$$

Hence, by converting F_{rest} to dB, the equivalent noise figure at the mixer input is equal to

$$\boldsymbol{NF_{rest} = 10\ log\ (17.3) = 12.4\ dB}$$

For clarity, the main parameters for the BB mixer are reported in Table 5.

Table 5 Mixer Specifications

Parameters	Value
RF Frequency	3.493 - 3.507 GHz
LO Frequency	3.5 GHz
IF Frequency	7 MHz
Minimum Gain dB	5 dB
Maximum Noise Figure	11 dB
Minimum IIP3	0.3 dBm
Minimum OPI3	5.3 dBm
Minimum P1_dB (one tone)	-4.7 dBm
Minimum P1_dB (two tone)	-9.7 dBm
Minimum IIP2	32.4 dBm
Minimum OIP2	38.4 dBm

2.4. Conclusion

In RF transceivers, a variety of architectures can be utilized. Each of them has its own advantages/disadvantages depending on the frequency range and application. In Wi-Max, the direct-conversion shows better performance over other configurations, including a high level of integration and the use of less blocks that result in lower cost and less power dissipation. Based on that, a link budget was calculated to deduce the desired specifications for the down-converter mixer to be designed (Table 6).

Table 6 Receiver System: Specifications

Description	**Antenna**	**Duplexer**	**LNA**	**Mixer**
Gain (dB)	11 dBi	-1.5	14 dB	5 dB
NF (dB)	N/A	-1.5	2 dB	11 dB
IIP3 (dBm)	N/A	N/A	-13.7 dBm	0.3 dBm
OPI3 (dBm)	N/A	N/A	0.3 dBm	5.3 dBm
P1_dB (one tone) (dBm)	N/A	N/A	-9.7 dBm	-4.7 dBm
P1_dB (two tones) (dBm)	N/A	N/A	-14.7 dBm	-9.7 dBm
IIP2 (dBm)	N/A	N/A	N/A	32.4 dBm

Chapter 3. Basics of Mixers

3.1. Mixer Principle

Mixers are essential building blocks for RF communication systems. These three port devices use nonlinear components to convert a signal to a higher or lower frequency by combining the input RF frequency with a local oscillator (LO) frequency as

$$(A_{RF}cos\omega_{RF}t).(A_{LO}cos\omega_{LO}t) = \frac{A_{RF}.A_{LO}}{2}\left[\cos(\omega_{RF}-\omega_{LO})\,t + \cos(\omega_{RF}+\omega_{LO})\,t\right] \quad (3.1)$$

Note that in the above equation, $\omega_{RF} - \omega_{LO}$ can be positive or negative, depending on the values of the respective RF and LO frequencies. As seen in the above equation, there are two types of mixers, up and down depending on the value of the output frequency, usually called intermediate frequency (IF). When the RF frequency is lower than the output frequency, it is called up-converter and the component $(\omega_{RF} - \omega_{LO})$ is filtered out. However, when the RF frequency is larger than the output frequency, it is called down-converter and the component $(\omega_{RF} + \omega_{LO})$ is filtered out [25][26][27]. Figure 7 illustrates the concept of mixer operation for up and down converters $f_{Rf} + f_{Lo}$ and $f_{Rf} - f_{Lo_{,,}}$ respectively [26].

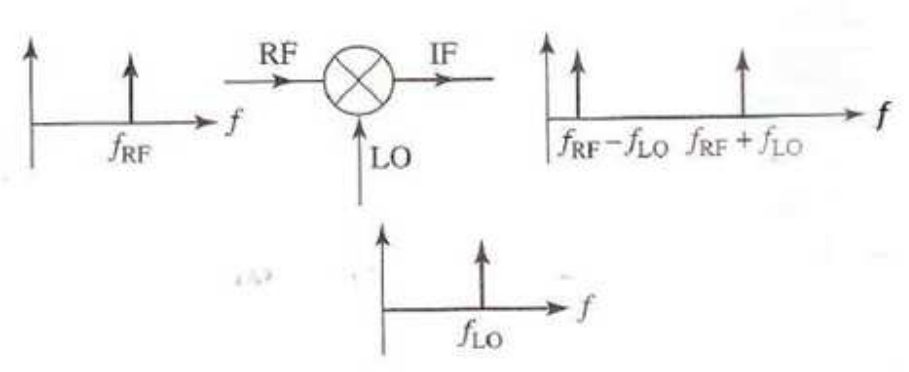


Figure 7 Basic Operation of Mixing [26]

After the mixing occurs, the output has both up-converted and down-converted frequencies. The up-converted deals with the transmitter, while the down-converted relates to the receiver side. In general, the mixer is specified in terms of signal as follows:

- Lower sideband, or LSB $(\omega_{RF} - \omega_{LO})$
- Upper sideband, or USB $(\omega_{RF} + \omega_{LO})$.
- Double sideband, or DSB $(\omega_{RF} + \omega_{LO}, \omega_{RF} - \omega_{LO})$

There is an issue for the image frequency that results from the second harmonic of the local oscillator as

$$2\omega_{LO} - \omega_{RF} = \omega_{LO} + (\omega_{LO} - \omega_{RF}) = \omega_{LO} - \omega_{IF} = \omega_{IM}$$

To prevent these unwanted signals to appear at the output, an image rejection filter needs to be in the front of the mixer to suppress this effect [27].

3.2. Mixer characterizations

Mixer design raises some issues that should be considered in case of mixer performance assessment. There are trade-offs to achieving a certain value of parameters. These parameters vary from application to application. Therefore, what follows can be characterized as the most significant parameters of mixer types.

3.2.1 Conversion Gain

The mixer conversion ratio is the ratio between output and input powers [15]

$$\boldsymbol{Power\ Conversion\ Gain} = \frac{\boldsymbol{IF\ power\ delivered\ to\ the\ load}}{\boldsymbol{Available\ power\ from\ the\ source}} = \frac{\boldsymbol{P_{out}}}{\boldsymbol{P_{in}}} \quad (3.2)$$

$$\boldsymbol{Power\ Conversion\ Gain\ (dB)} = \boldsymbol{10log}\ \frac{\boldsymbol{P_{out}}}{\boldsymbol{P_{in}}} \quad (3.3)$$

$$\boldsymbol{Voltage\ Conversion\ Gain\ (dB)} = \boldsymbol{20\ log}\ \frac{\boldsymbol{V_{out}}}{\boldsymbol{V_{in}}} \quad (3.4)$$

For diode mixers, this ratio is less than unity, and therefore is called conversion loss. While for a transistor mixer, this quantity is called conversion gain since it is usually higher than unity [27].

3.2.2 Linearity

The linearity of the mixer can be quantified by the 1dB compression point, the input third-order intercept point (IIP3) and the input second-order intercept point (IIP2). As seen in Figure 8 [5], when the fundamental power is equal to the 3rd order intermodulation (IM) distortion, it is called IIP3.

Also, when the fundamental power is equal to the 2rd order intermodulation (IM) distortion, it is called IIP2. In addition, when the fundamental gain starts to differ from the original or ideal signal by 1dB, this phenomenon is called 1dB compression point [17] [25].

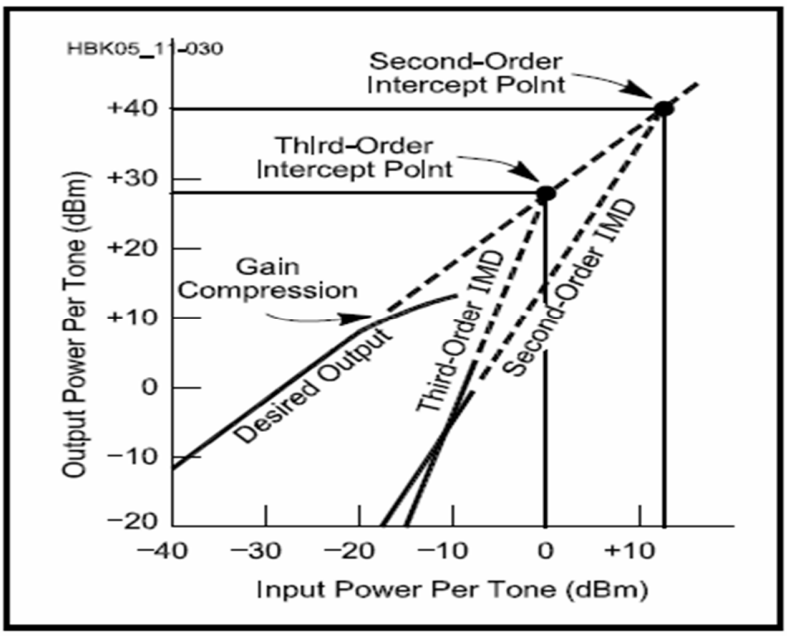


Figure 8 IIP2, IIP3 and P1-dB Compression Points [28]

3.2.3 Noise Figure

Noise factor *F* is defined as the ratio of signal to noise (SNR) at the input port to the SNR at the output port, while the noise figure *NF* is defined as the noise factor in dB, as expressed below

$$\boldsymbol{F = \frac{(SNR_{IN})}{(SNR_{out})}} \quad \textbf{(3.5)}$$

$$\boldsymbol{NF = 10\,Log\,\frac{(SNR_{out})}{(SNR_{IN})}} \quad (3.6)$$

There are two categories of noise figures that can be applied to mixers: single side band (SSB) and double side band (DSB). When the input signal exists in one sideband of the input, the SSB noise figure is considered to assess the mixer performance. On the other hand, when the input signal exists in both sidebands, the input signal and the image, the DSB noise figure is considered to measure the mixer performance.

Indeed, SSB is utilized for heterodyne architecture, whereas DSB is used in direct conversion configuration [17][29].

3.2.4 Isolation

Mixer isolation is a very essential parameter for the overall transceiver performance. A good isolation between LO, RF, and IF ports is crucial because any leakage from any port will degrade the overall transceiver performance [5].

3.3. Mixer configuration

In this section, the diversity of mixer topologies is described and divided into subsections; diode mixer and transistor mixer.

3.3.1 Diode Mixer

In the past, mixers were mainly diode mixers (Figure 9). The most popular diode used as a mixing device is the Schottky-barrier diode. Diode mixers have their own advantages, including low cost and broadband, that provide reasonable performance in term of distortion, conversion loss, and LO noise [31][32]. On the other hand, diode mixers need high LO drive level, which is a disadvantage [30]. In fact, diode mixers are not used in

receivers due to conversion loss that lead to increase the noise figure as illustrated in equation 2.8. There are three main configurations of diode mixers based on the number of diodes and their characteristics as described in Table 7 [33]:

- ✓ Single ended mixer (one diode).
- ✓ Single balanced mixer (two diodes).
- ✓ Double balanced mixer (four diodes).

Note that a double balanced configuration (also called triple balanced) exists but it is much less used due to the large number of diodes it requires (8 diodes).

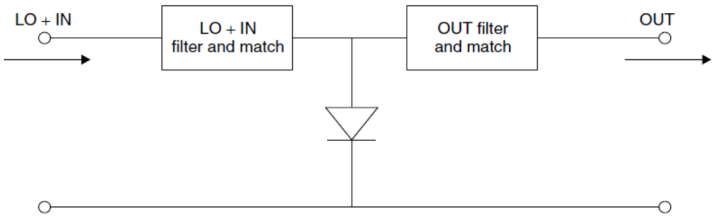


Figure 9 The General Structure of Diode Mixer [31]

Table 7 Summary for Diode Mixer

Configuration	Advantages	Disadvantages
Single Diode	• Low LO power level compared to balanced mixers	• Poor linearity
Single Balanced	• Provide either LO or RF Rejection (20-30 dB) at the IF output. • Suppression of Amplitude Modulated (AM) LO noise. • Better linearity of single diode.	• Require a high LO drive level
Double Balanced	• Both LO and RF are balanced, providing both good LO and RF rejection at the IF output • All ports of the mixer are inherently isolated from each other • Increased linearity compared to single balanced	• Require two baluns • Relatively high noise figure, about the same as conversion loss • Diodes need to be well "matched"
Double Double Balanced (or triple balanced)	• Increased linearity compared to double balanced	• Increased complexity and cost (3 baluns and 8 "matched" diodes are required) • Higher level of LO drive must be provided.

3.3.2 Transistor Mixer

Transistor, such as MESFETs, HEMTs, HBTs, or BJTs, provide mixing gain. Although diode mixers have their own advantages, transistor mixers are superior in different aspects and specific applications, such as for wireless systems. For instance, compared to diodes, transistors mixers can work with less LO power consumption.

Also, transistor mixers can provide conversion gain instead of conversion loss [35]. Single FET mixers can achieve gain but their isolation is poor. Dual-gate mixers have inherent isolation between LO and RF ports because the signal is applied to different gates. Balanced FET mixers exhibit good RF-LO isolation and LO noise rejection and are a good solution to prevent spurious responses.

Diode mixers designers try to reduce conversion loss. Consequently, the noise can be reduced accordingly. On the contrary, FET mixers can easily achieve high gain but this could affect other parameters such as linearity and noise figure. In fact, transistor mixers are usually designed to achieve low noise figure with moderate conversion gain [32]. In the following section, different configurations of transistor mixers will be discussed.

3.4. Different Topologies of Transistor Mixers

3.4.1 Single FET Mixer

There are different types of single FET mixers depending on where the LO signal is fed:

- Gate Mixer:

In FET-gate mixers, the main nonlinear element is the transconductance.

The input signal is connected to the gate FET with constant voltage drain, while the output signal is applied to the drain. As shown in Figure 10, the intrinsic isolation between the LO port and the IN (input) port is weak while the OUT port is isolated from IN and LO port (due to little reverse gain of the transistor) [31].

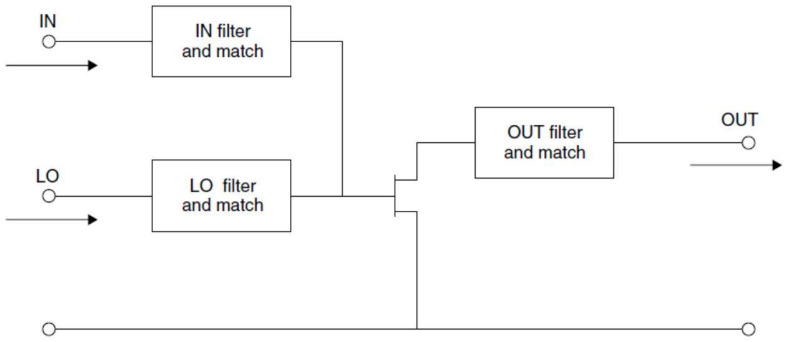


Figure 10 FET-Gate Mixer Configuration [31]

- Drain Mixer:

In FET-drain mixers, the input signal is applied at the FET gate while the output signal is connected to the drain terminal. The transistor nonlinear parameters that are modulated by the signal are the transconductance and the conductance with constant gate voltage (Figure 11).

The problem of the drain mixer is similar to the gate mixer: the isolation between the ports is an important issue to consider. The isolation between LO and OUT ports are very weak; however, the IN port is isolated from OUT and LO ports, due to the little reverse gain of the FET [31]

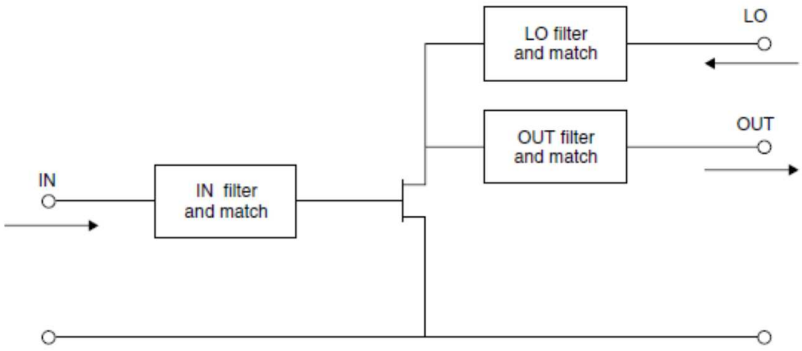


Figure 11 FET-Drain Mixer Configuration [31]

- Source Mixer:

In a source mixer, the main nonlinear parameters modulated by the LO signal are the transconductance and the output conductance. The drain and gate voltage are constant (Figure 12). The source mixer has the same isolation issue as the gate and drain mixers.

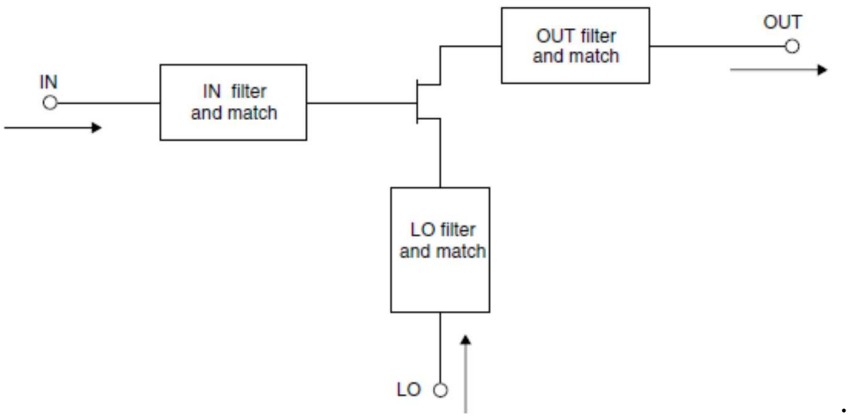


Figure 12 FET-source Mixer Configuration [31]

- Resistive Mixer:

In resistive mixers, the main nonlinear parameter is the channel conductance. The voltage bias at the drain is zero.

Therefore, it is called resistive mixer, which leads to no gain provided. As seen in Figure 13, the output signal is at the drain, while the input signal is taken from the drain and the LO signal applied at the gate.

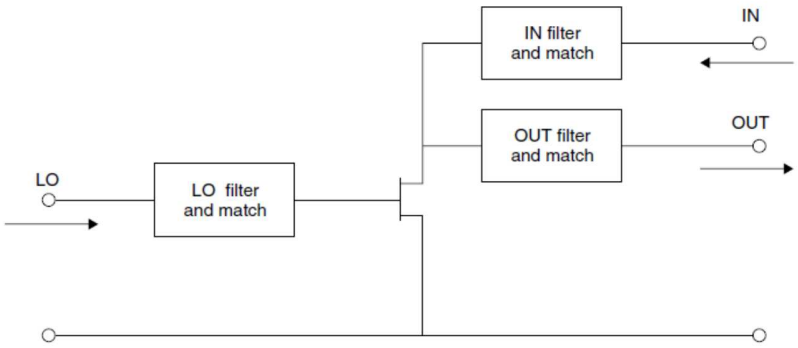


Figure 13 Channel Mixer (Resistive Mixer) Configuration [31]

The isolation between the LO and both IN and OUT ports is quite good. However, the channel mixers do not provide gain because of the zero bias at the drain. In addition, the resistive mixer has poor isolation between the IN and OUT ports [31].

As stated in [32], “the advantages of resistive mixer are low distortion, low 1/f noise, and no shot noise; the conversion loss of such mixers is comparable to diode mixers, around 6 dB.” Therefore, the resistive mixer may be suitable for low-intermodulation applications.

3.4.2 Dual-gate Mixer

The main advantage of dual-gate mixers over single gate mixers is the good isolation between the LO and RF ports, due to the low gate capacitance. Therefore, the dual-gate FET mixer is a better choice in applications where balanced mixers cannot be used.

In addition, it is preferable to use dual-gate devices in integrated circuits, in case where filters or similar devices cannot be used or cannot provide good isolation.

However, even if dual-gate mixers provide gain and good isolation, their noise figure is worse than single FET mixers. Also, their use is still limited due to the complexity of modeling/characterizing the active device. As shown in Figure 14, the dual-gate mixer contains two single-gate transistors, FET1 and FET2. The input signal is connected to the gate of FET1, while the LO signal is connected with the gate of FET2.

As stated in [32] "A dual-gate mixer is a transconductance mixer. Therefore, the mixing should occur by variation of the transconductance between V_{gs1} and I_d. The transconductance variation must come from varying the drain voltage of FET1".

In order to get mixing in dual-gate mixer, the FET1 should operate in linear region, while the FET2 must operate in saturation mode. Indeed, mixing is occurring in FET1 with low g_m and R_{ds} varying in time [32].

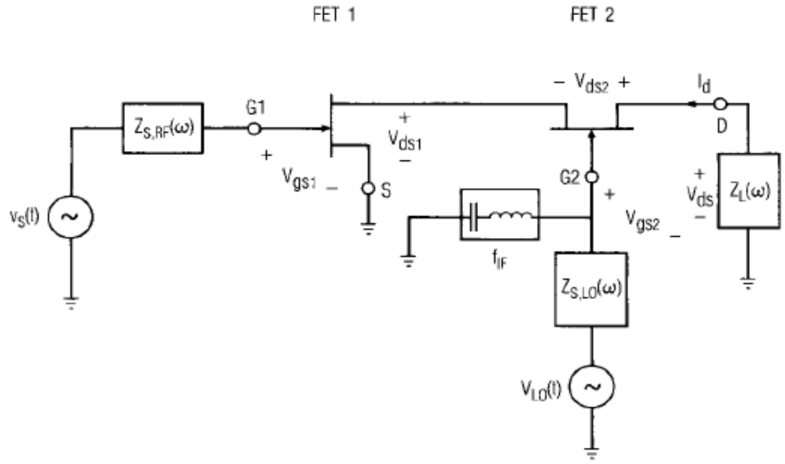


Figure 14 Circuit of the Dual-Gate FET Mixer [32]

3.4.3 Balanced Mixers

A. Single Balanced Mixer

The important advantages of single balanced transistor mixers are, as in [32], “LO isolation, spurious-response rejection and LO noise rejection.” A single balanced mixer consists of a set of two transistors combined through 90^{o} or 180^{o} 3-dB baluns. The use of such hybrids at the LO and IF ports, implies a relatively complex topology.

As shown in Figure 15.a, the mixer needs a balun at the LO port to apply the LO signal to the two FETs working as switches. A third transistor is used to amplify the RF signal. The advantage of this figure is that no LO voltage is applied to the RF FET drain because the point “A” is virtually grounded. In Figure 15.b, a second structure for single balanced mixer is displayed. It is similar to the previous one although it does not have a balun at the LO input. This will give a simpler topology but at the cost of a lower conversion gain (the “A” point is no longer virtually grounded. Hence, there is an LO voltage applied to the RF FET drain, causing degradation in the mixer gain). So this second configuration is exploited only if a balun cannot be used [32].

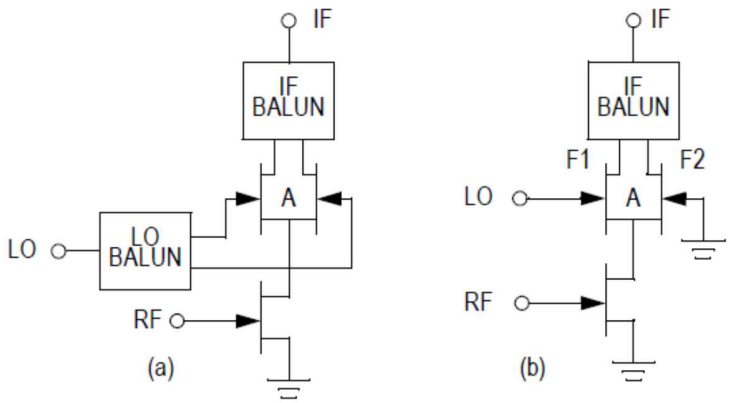


Figure 15 Two single balanced FET mixers: (a) conventional and (b) configured [32]

B. Double Balanced Mixer

Even if double balanced FET mixers are similar to single balanced mixers, they are broadband with good port isolation and rejection of LO AM noise. Also, they prevent all spurious responses of the even harmonics of LO and RF frequencies. The issues in double balanced mixers are the power consumption and the use of baluns at each port; however, small active baluns can be used instead of distributed elements (e.g., transmission line couplers). Also, using more transistors increases the circuit complexity while reducing linearity and symmetry. Figure 16 shows the two stages of a double balanced FET mixer: the switch stage (LO) and the amplifier stage (RF). The upper transistors are considered as switch stages and should operate in the linear region. On the other hand, the lower transistors are defined as amplification stages and operate in the saturation region. Using a current source can provide more balance to the circuit, but the power consumption will increase [32]. A well-known configuration of the double balanced FET mixer is the Gilbert-cell mixer [34] that will be discussed more details in Chapter 4. Table 8 compares the performance of the above mixers [17][35].

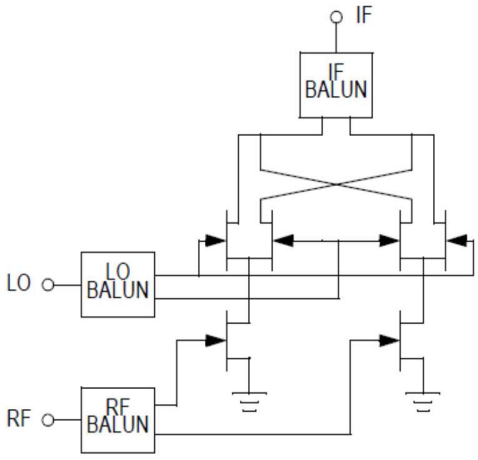


Figure 16 Double Balanced FET Mixer [32]

Table 8 Performance Comparison of Different Types of Mixers

Evaluated Parameters	Diode Mixer	Single FET Mixer	Single Balanced Mixer	Gilbert Cell Mixer
Gain	Low	Moderate	Moderate	High
Linearity	High	Low	Low	Low
Noise Figure	High	Low	Low	Low
LO-RF feed through	High	High	Moderate	Low
Voltage	Low	Moderate	Moderate	High
Power consumption	Low	Low	Medium	High
LO power	High	Much Lower	Lower	Low

3.5. Discussions and conclusion

Two active components can be used in mixing: diode and transistor. Diode mixers have high linearity but with high LO power and conversion loss. On the other hand, the main advantages of transistor mixers are conversion gain and low LO power requirement [36]. Therefore, the transistor mixer will be selected for WiMax applications.

From the well-known transistor mixer topologies, the single FET mixer can provide gain but raises issues with ports isolation. This can be addressed in dual-gate FETs, but with moderate gain and higher noise figure.

The single balanced mixer exhibits good conversion gain, LO isolation, and spurious response rejection. However, it has a problem with RF feed through, while double balanced mixer provides superior advantages, including inherent isolation between the RF/LO, RF/IF, and LO/IF ports.

It can provide acceptable gain, moderate linearity, and cancel the even harmonics distortion, thus improving the IIP2, but at the expense of circuit complexity [23][24][38].

As reported in Table 8, because of the above advantages over other types of mixers, the Gilbert cell has been chosen for WiMax application.

Chapter 4. Gilbert Cell Mixer: Design, Implementation, and Results

In this chapter, a Gilbert cell mixer design in Gallium Arsenide (GaAs) transistor technology will be provided in details including the design specifications for WiMax application. Thus, different improvement techniques for conventional Gilbert-cell mixers will be reviewed. Then, the design simulation procedure will be discussed for current bleeding technique. The last part in this chapter will focus on the mixer layout design and optimization.

4.1. Design Specifications for WiMax

The foremost step in designing a down converter mixer is to determine the receiver requirements. Since the objective of this thesis is to design a Gilbert cell mixer for WiMax application, the system requirements will be based on the IEEE 802.16 standard. Based on the receiver requirements and link budget for WiMax discussed in section 2.3 and summarized in Table 9, the receiver sensitivity is -76.1dBm and modulated with 64-QAM. The RF center frequency is centered around 3.5GHz. After the LNA, the RF signal is converted through I/Q down converters to 7 MHz using a local oscillator (LO) centered at 3.5 GHz. Then the signal passes through other stages for more process. The mixer specifications are reported in Table 10.

Table 9 WiMax Requirements

Item	Value
Operating Frequency	2-6 GHz
Channel Bandwidth (BW)	6, 7, 12, 14 MHz
Modulation	64-QAM
Signal to Noise Ratio (SNR)	24.4 dB
Maximum distance between Rx and Tx	3.5 km
Transmitter maximum power	29.5 dBm
Transmitter antenna gain (GTx)	0 dBi
Receiver antenna gain (GRx)	11 dBi
Receiver maximum input	-30 dB
Receiver maximum Noise figure	5 dB

Table 10 Mixer Specifications

Description	Value
RF Frequency	3.493 - 3.507 GHz
LO Frequency	3.5 GHz
IF Frequency	7 MHz
Minimum Gain dB	5 dB
Maximum Noise Figure	11 dB
Minimum IIP3	0.3 dBm
Minimum OPI3	5.3 dBm
Minimum P1dB (one tone)	-4.7 dBm
Minimum P1dB (two tones)	-9.7 dBm
Minimum IIP2	32.4 dBm
Minimum OIP2	38.4 dBm

4.2. Semiconductor Technology Selection

To implement a Gilbert-cell mixer, different types of transistors can be potentially used such as Si CMOS, Si BJTs, GaAs MESFETs, GaAs and GaN HEMTs, or GaAs HBTs [39][40]. However, for our application, because of their better noise performance, higher transconductance (g_m), higher cut-off frequency (f_t), as well as excellent level of integration [41], HEMT devices have been retained.

Over existing HEMTs, Gallium Arsenide (GaAs) pseudomorphic HEMTs (pHEMTs) can exhibit very low noise and excellent aptitudes to operate at high frequencies with a cut-off frequency higher than 100 GHz [41]. Also, it has high breakdown voltage and direct band gap [42]. As stated in [43] "GaAs offers a good balance of properties for a wide range of RF applications such as wireless application including Wi-Fi, Bluetooth and WiMax".

In this work, we used the 0.15µm GaAs pHEMT technology process provided by "Win Semiconductor Crop. (WSC)" [44]. All the components are taken from the WSC design kit including transistors, capacitors, and resistors.

4.3. Down-Converter Gilbert Cell Mixer

In this subsection, the basic operation of the Gilbert-cell is detailed. In addition, different optimization improvement techniques are presented including current bleeding, current reuse, and folded mixer.

4.3.1 Basic Operation of Conventional Gilbert Cell Mixer

The Gilbert cell mixer is a double balanced mixer widely utilized in widespread circuits [25]. Its basic structure is illustrated in Figure 17 [37] where two single balanced topologies are combined together to create a double balanced structure. The Gilbert-cell mixer is a differential topology at each of its three ports (LO, RF, and IF). This feature leads to an inherent isolation between the RF/LO, RF/IF and LO/IF ports and prevent LO feed through. In addition, it can exhibit acceptable conversion gain and provide moderate linearity. Furthermore, it can cancel the even harmonics distortion, albeit at the expense of circuit complexity [36][37].

The operation of a Gilbert-cell mixer could be divided into three stages as seen in Figure 17 [37]: the RF stage (input stage), the LO stage (switching stage), and the IF stage (output stage).

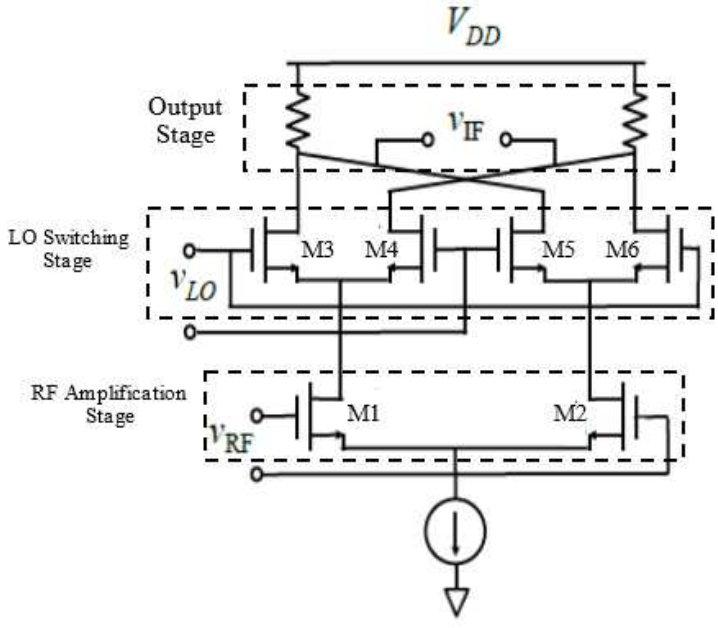


Figure 17 Conventional Gilbert-Cell Mixer [16]

The input stage consists of two differential transistors (M1 and M2, operating at saturation region). It amplifies and converts the input voltage to an output current. The switching stage (transistors M3 to M6, working near the pinch-off range) is in charge of multiplication of the RF incoming signal, making the current out of phase [37][45][46].

Gilbert-cell mixer demonstrated high port isolation, excellent gain, and cancellation of all even harmonics; however, it requires staking more transistors leading to more bias supply and power dissipation [47][48]. In addition, the noise figure is going to be increased [48]. Also, the linearity could be degraded. Therefore, there are some techniques to improve the conventional Gilbert cell mixer performance.

4.3.2 Gilbert-Cell Mixer Improvement Techniques

To address the issues of power consumption and relatively high noise figure, different configurations have been proposed to improve the basic Gilbert cell performance.

A. Folded Gilbert cell mixer

The main idea for folded mixer is to reduce the voltage supply and improve the conversion gain and noise figure. This concept can be achieved by separating the RF stage from the LO stage in terms of voltage supply, as depicted in Figure 18. Indeed, the key of this technique is reducing the voltage supply but at the expense of larger chip size by adding additional components [47][48]. The folded mixer utilizes both N-channel and P-channel devices; however, the P-channel ones limit the frequency operation [36].

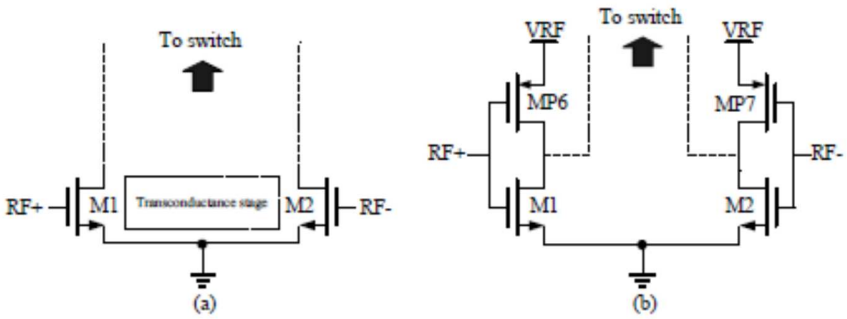
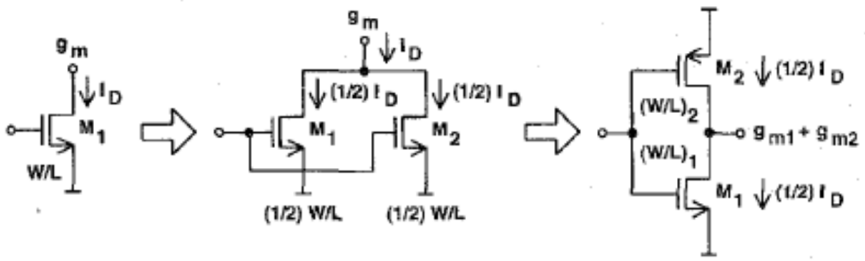


Figure 18 Folded Mixer [48]

B. Gilbert-cell Mixer with Current Reuse

The key advantage of using a current reuse technique is to have low current in order to reduce the circuit power consumption. Figure 19 (a) presents a single N-channel transistor with a transconductance g_m and a drain current I_D while in Figure 19 (b) there are two N-channel transistors. Each transistor has ½ g_m and ½ I_D which the same operation as Figure 19 (a). In Figure 19 (c), the M2 is replaced by a P-channel transistor and the total transconductance is almost double (g_{m1}+ g_{m2}) while the current is reduced by half. The main problem of this technique is that, using P-channel with a more limited frequency operation, could be increase some parameters like noise figure [49].



(a) (b) (c)

Figure 19 Current-reuse Technique [49]

C. Current Bleeding or Charge-injection Technique

As mentioned above, the conventional Gilbert cell has two stages namely, the switching stage (M3-M6) and the amplification stage (M1 and M2). The principle of charge injection is to increase the current in the amplification without affecting the current of the LO stage and make sure the RF transistors are operating at saturation region with enough current. This can be achieved by adding two resistances to the RF stage to improve the conversion gain as in Figure 20. This mechanism reduces the current in the LO stage thus, the voltage in the load resisters can be decreased as well [47][48][50].

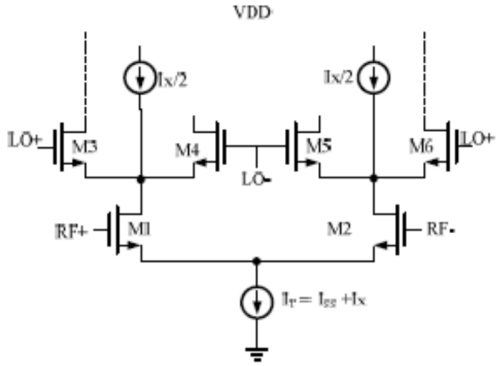


Figure 20 Charge-injection Technique [48]

To conclude, there are varieties of mechanisms to improve the conventional Gilbert-cell mixer. The folded mixer allows decreasing the voltage dependency by making separate voltage supplies for the LO stage and the RF stage. In addition, the current reuse technique could be utilized to reduce the power consumption by providing lower current. On the other hand, in both previous techniques, the need for P-channel devices limits the frequency operation. The current bleeding technique reduces the voltage in the LO and RF stages and increases the conversion gain by injecting current in the RF stage. In addition, the design kit provided by WSC can be used only for N-channel transistors.

Therefore, the current bleeding technique has been retained for our down-converter Gilbert-cell mixer design.

4.4. Current Bleeding Technique for Gilbert-cell Mixer

In this section, the current bleeding or charge-inject technique is going to be discussed in details including the circuit operation, design and implementation.

4.4.1 Operation of Current Bleeding Technique for Gilbert-Cell Mixer

The schematic of the Gilbert-cell mixer by using charge injection or current bleeding technique is shown in Figure 21. The RF signal is applied to the gate of the differential transistors (M1 and M2). Such configuration produces relatively constant gain, cancels the even harmonics, and converts the M1 and M2 RF input signal voltage to output current.

The LO signal is applied to M3-M6. These transistors operate near pinch-off region in order to accomplish the multiplication of the RF amplified signal with the LO signal. A current mirror stage (M9 and M10) provides the required current for the circuit. Figure 22 shows the current mirror configuration used in the Gilbert-cell mixer design [51]. The total current of this configuration relies on the input current and R8 (independent supply). Adding R8 reduces the dependency on the input current [51]. Finally, two source follower buffers (M7 and M8) are added to match the IF+/IF- output with baluns.

In order to get high conversion gain, the RF transistors should be larger than the LO transistors. On the other side, large size transistors increase DC and LO power consumption.

Therefore, the current bleeding (R_1 and R_2) was added to M1 and M2 to enhance the conversion gain by increasing the current in the RF stage. This current should be enough

to operate M1 and M2 in the saturation region while reducing the current in the LO stage; therefore, the voltage is dropped in the load resistors R_6 and R_7 [32][45][46][50].

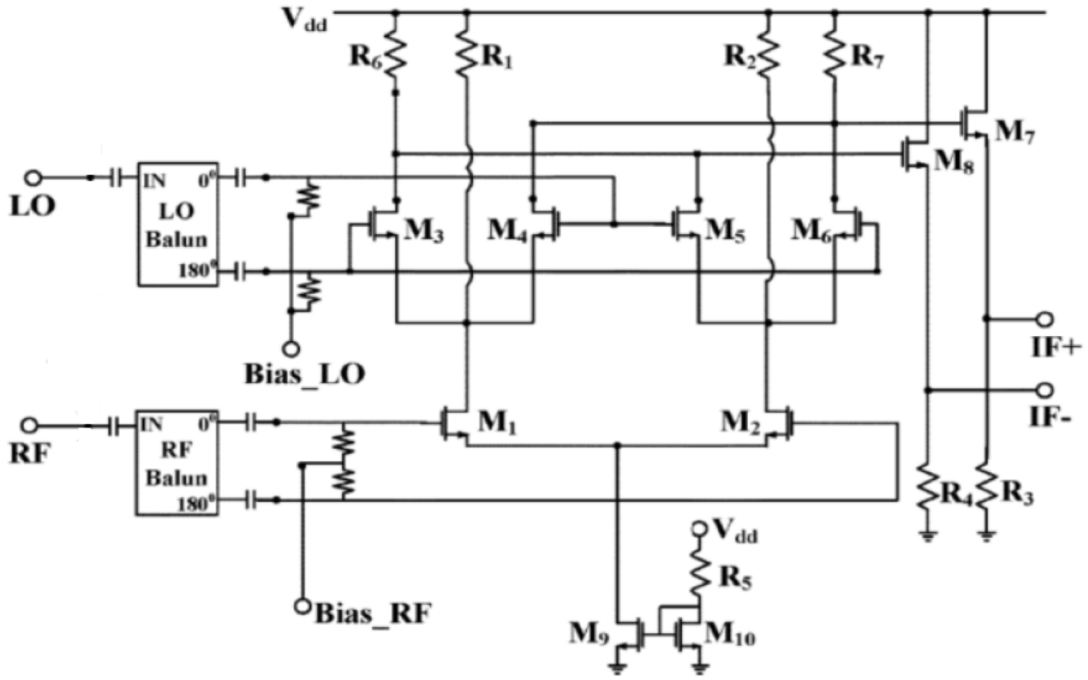


Figure 21 Schematic of Fully Integrated Gilbert-cell Mixer [45]

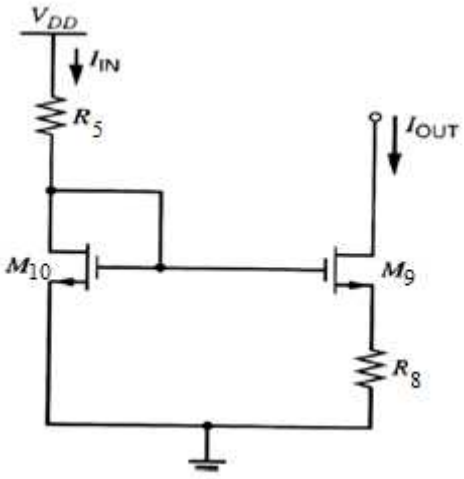


Figure 22 Current Mirror Configuration (independent supply) [51]

4.5. Device Sizing

The next step in mixer design is selecting the suitable size of the transistors. In fact, there are trade-offs in terms of noise figure, conversion gain, maximum frequency (f_{max}), and power consumption for specific transistor dimensions. Most of these parameters are relied on the transistor size [52]. Note that in our work, we were limited by the WCS transistor design kit availabilities (for instance, the available gate widths are limited to 25, 50 and 100 µm, while the number of fingers should be even and not exceed 8). Therefore, preliminary simulations run in the commercial circuit simulator Agilent ADS indicated that the retained GaAs HEMT exhibits a minimum noise figure for a current density around 0.15 mA/µm as reported for different semiconductors in [53]. As seen in Figure 23, lowest minimum noise figure around 0.17 dB was achieved for 2 fingers and 25µm gate-width (2×25µm) and 8 fingers and 25µm gate width µm (8×25µm). However, these two transistor behaviours are different in terms of power consumption, as showed in Figure 24.

Note that the maximum frequency (f_{max}) is around 95 GHz while the WiMax technology operates in the range of 5 GHz. Therefore, the smallest size transistor available in the design kit, i.e., 2×25 µm, is chosen based on minimum noise figure, power consumption and maximum frequency (f_{max}). Moreover, the small transistor size provides the ability to apply the current bleeding or charge injection technique in order to reduce the circuit voltage and increase the conversion gain.

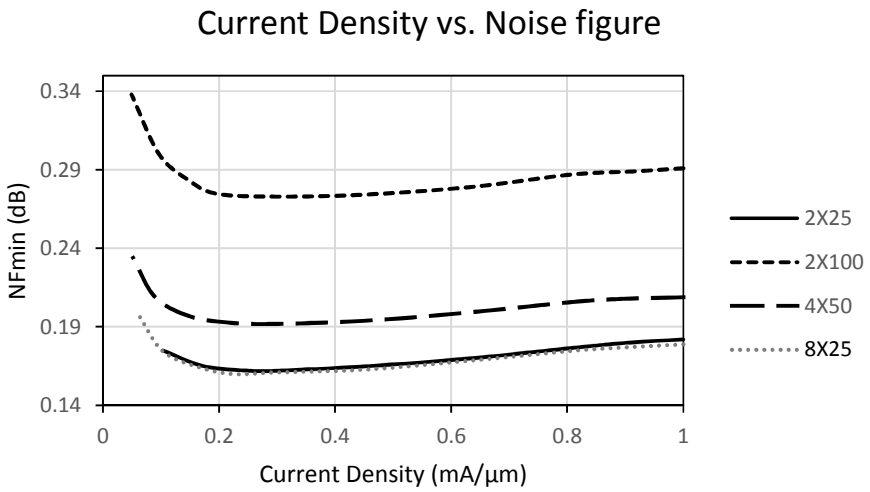


Figure 23 Minimum Noise Figure vs. Transistor Size

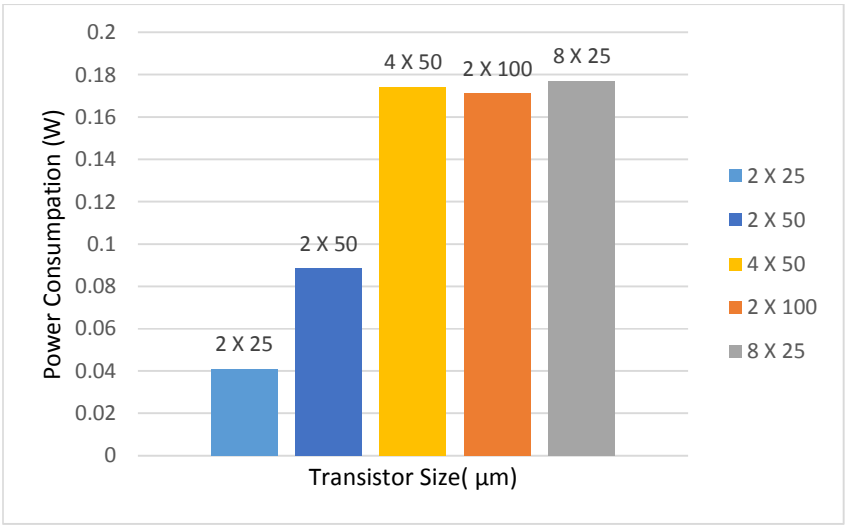


Figure 24 Power Consumption vs. Transistor Size

4.6. DC analysis

In this section the DC analysis for the 2×25 µm transistor is discussed. The main purpose is to choose the suitable transistor bias settings [54] to ensure that the amplification

stage will be operating in saturation region while the switching stage would function near pinch-off region.

For the amplification transistors M1 and M2, the drain current (I_{DS}) should be sufficient to saturate the transistors, i.e., $V_{DS} > V_{dsat}$ with V_{dsat} the point where the drain reaches saturation, and V_{DS} the drain-to-source voltage [54]. As shown in Figure 25, the highest transistor transconductance g_m occurs when the value of gate-to-source voltage (V_{GS}) is between -0.25V and 0V [54]. On the contrary, for the switching stage, the transistors M3 to M6 should operate near pinch off region.

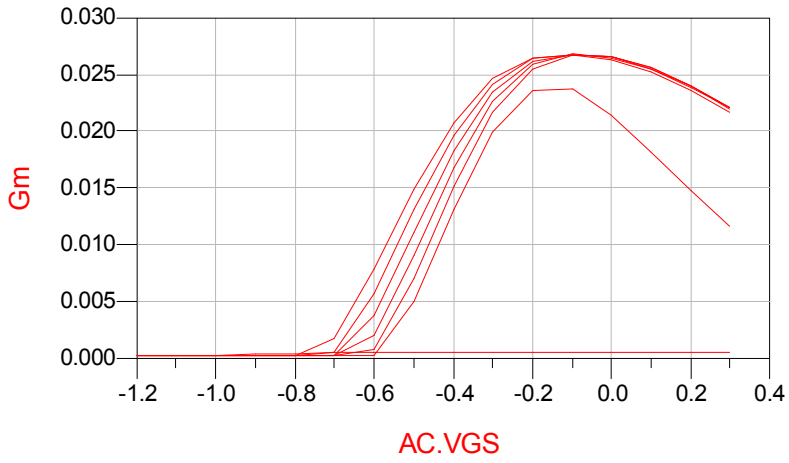


Figure 25 The Transconductance vs. Gate-to-Source Voltage

The following step is to simulate the transistors and determine the bias voltage and current for each transistor. For transistors M1 and M2, Figure 26 shows that they should be biased at V_{DS} =1.3V and V_{GS} =-0.25V to provide high g_m. The corresponding drain current is 6 mA. While for the switching stage, Figure 27 shows a bias point of V_{DS} =0.2V and V_{GS} =-0.3V with a drain current of 2 mA, leading to a current of 12 mA traveling through M9 transistor (Figure 28). Finally, the simulation of M10 transistor is presented

in Figure 29. It should operate in saturation region; beside, the gate voltage (V_G) should be equal to the drain voltage (V_D) (Figure 22).

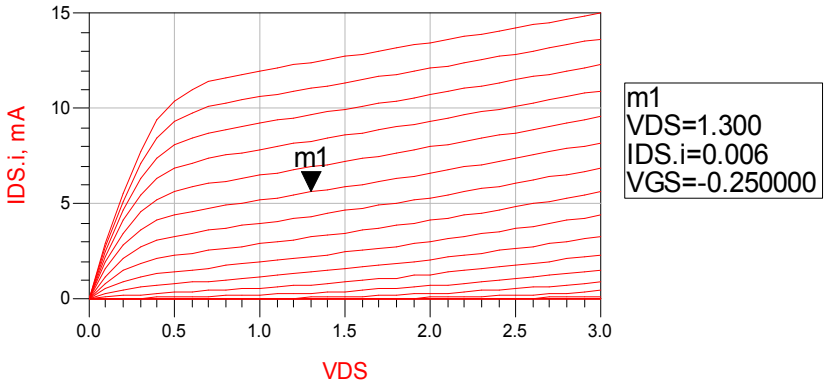


Figure 26 Bias Point for Amplification Transistors (M1 and M2)

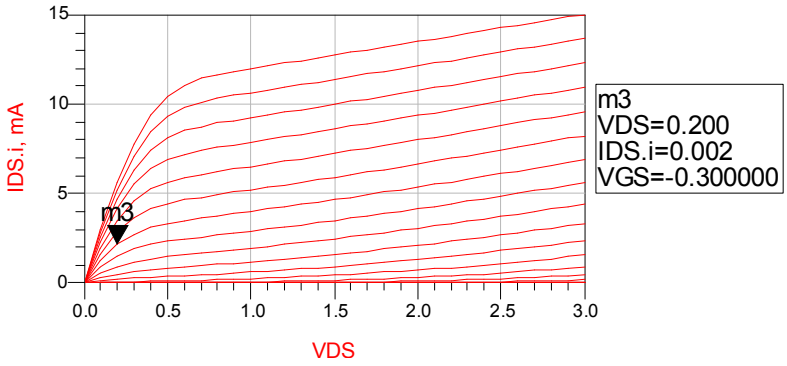


Figure 27 Bias Point for Quad Switching Transistors (M3-M6)

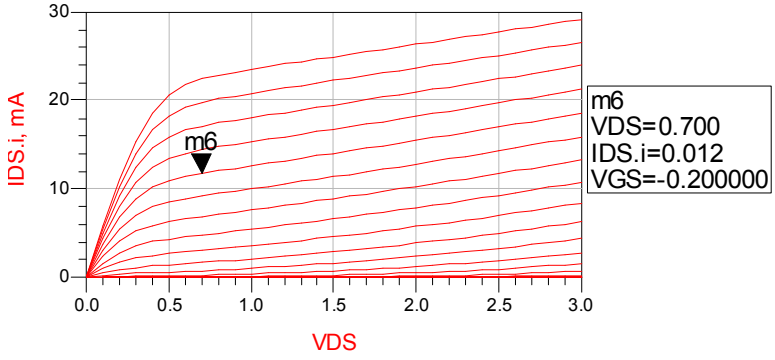


Figure 28 Bias point for Total Current Transistor (M9)

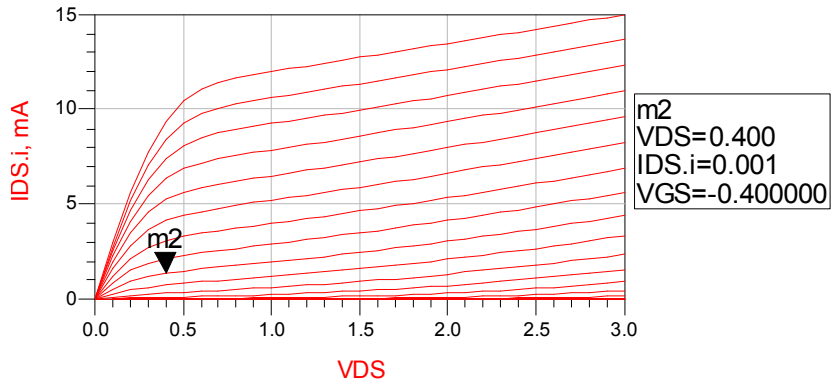


Figure 29 Bias point showing $V_{GS} = V_{DS}$ for the Current Mirror (M10)

The operating point for each transistor has been set up. The subsequent step is to determine the value of resistors R_1, R_2, R_5, R_6 and R_7. By applying Kirchhoff's Voltage Law (KVL) to the circuit shown in Figure 21 (with $V_{DD} = 3.3V$), we have:

$$\boldsymbol{V_{DD} = IR_1 1 + V_{DS\,M1} + V_{DS\,M9}} \quad (4.1)$$

$$\boldsymbol{R_1 = \frac{V_{DD} - V_{DS\,M1} + V_{DS\,M9}}{I}}$$

$$\boldsymbol{= \frac{3.3 - 1.3 - 0.7}{2\ mA} = 650\ \Omega}$$

Because the Gilbert cell mixer is symmetric,

$$\boldsymbol{R_1 = R_2 \text{ and } R_6 = R_7.}$$

Thus,

$$\boldsymbol{R_6 = R_7 = 275\ \Omega.}$$

The resistor R_5 can be obtained using the following equation

$$\boldsymbol{I_{D\,M10} = \frac{V_{DD} - V_{GS\,M10}}{R_5}} \qquad (4.2)$$

Referring to the current mirror circuit, V_G = V_D = 0.4 V. Therefore, the current through M10 was set to 1 mA to equalize V_G and V_D.

Then,

$$\boldsymbol{R_5 = \frac{V_{DD} - V_{GS\,M10}}{I_{D\,M10}}} \qquad (4.3)$$

$$\boldsymbol{R_5 = \frac{3.3 - 0.4}{1\ mA} = 2900\ \Omega}$$

To conclude, the transistors have been sized as 2×25 µm. Then, the bias points have been fully selected for each transistor including amplification stage, switching stage and current source stage. In addition, the resistors values have been calculated to get the desired performance operation. Table 11 summarizes the size of the transistor used in the gilbert cell mixer shown in Figure 31.

4.7. Harmonics Balance Analysis

Once the DC analysis completed, the following step is going to run the large signal analysis or harmonic balance (HB) analysis of the Gilbert-cell mixer circuit depicted in Figure 21. Furthermore, the simulator was set up for input signal frequency from 3.493

to 3.507 GHz and LO signal frequency of 3.5 GHz in order to get the IF output frequency of 7 MHz. Because of differential configurations, RF and LO inputs and IF output are converted to single ended by using ideal transformers.

Figure 30 shows the basic set up for the down-converter Gilbert-cell mixer including the HB analysis, differential mixer and transformers while Figure 31 shows its schematic implemented in ADS. The essential parameters for down converter Gilbert cell mixer are going to be simulated including conversion gain, linearity, and noise figure.

4.8. Harmonics Balanced Results for Gilbert Cell Schematic

In this section, the schematic results are reported including conversion gain, noise figure, IIP3, OIP3 and P1-dB compression point. Note that in this section, ideal transmission lines have been utilized.

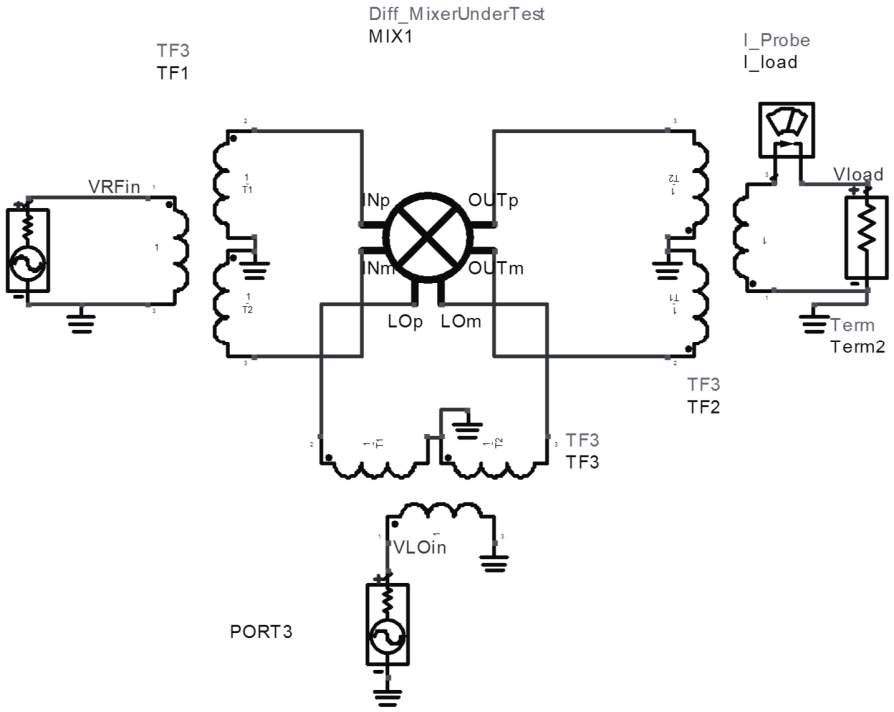


Figure 30 ADS Set Up for Gilbert Cell Mixer

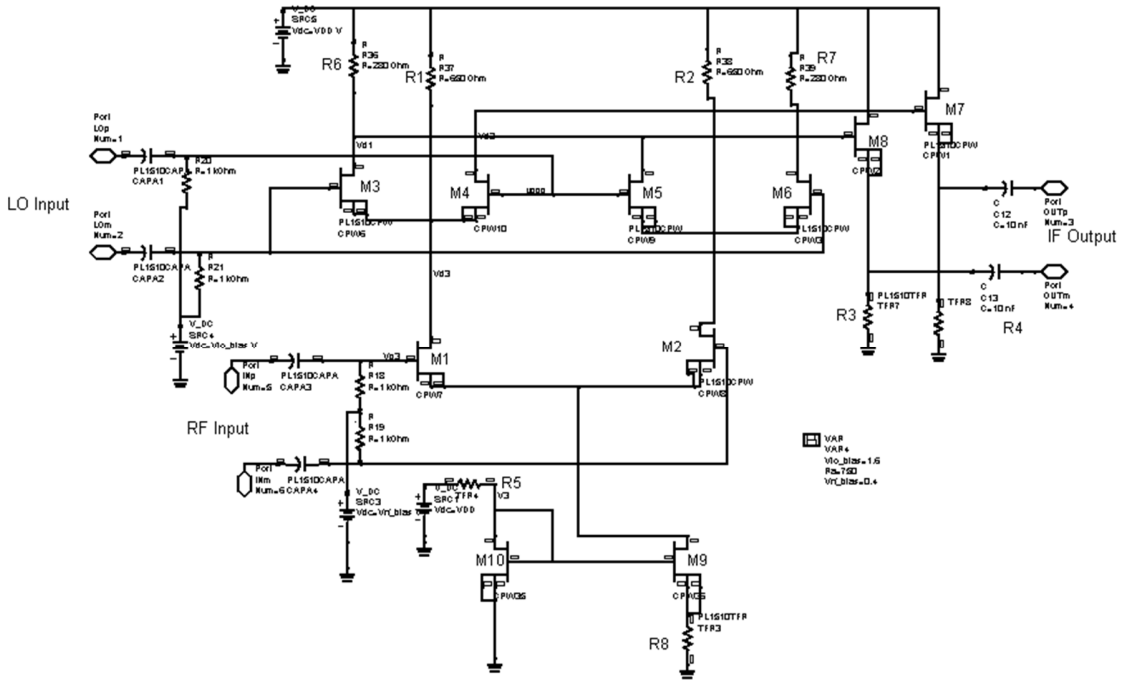


Figure 31 ADS View for Gilbert-cell Mixer Schematic

Table 11 Transistor size for the designed Gilbert cell mixer

Description	Function	Size
Transistors(M1 and M2)	Amplification Stage	2×25µm
Transistors(M3, M4, M5 and M6)	Switching Stage	2×25µm
Transistors (M7 and M8)	Source follower	4×100µm
Transistor (M9)	Current Source	2×50µm
Transistor (M10)	Current source	2×25µm

4.8.1 Conversion Gain

The same set up used in Figure 30 and Figure 31 is used to simulate the Gilbert cell mixer conversion gain.

Different elements affect the conversion gain such as LO power level, impedance matching and device width. There are indeed tread-offs between these factors but the main parameter to be considered is the LO power level. In fact, this value has to be chosen carefully to get the optimum value for gain, compression point, and noise figure [54].

As seen in Figure 32, the optimum LO power of -3 dBm allows reaching the highest conversion gain value, i.e., 7.3 dB.

However, as displayed in Figure 33, the above LO power gives a relatively high single side band noise figure of around 10 dB. Therefore, as compromise, we selected a LO power of 0 dBm, corresponding to a conversion gain of about 6 dB and a noise figure of 9.3 dB for single side band and 6 dB for double side band, which are still acceptable values according to mixer requirements (Table 9).

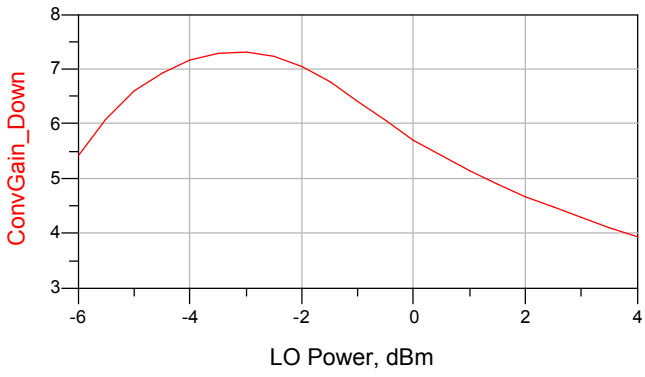


Figure 32 Conversion Gain vs. LO Power Level

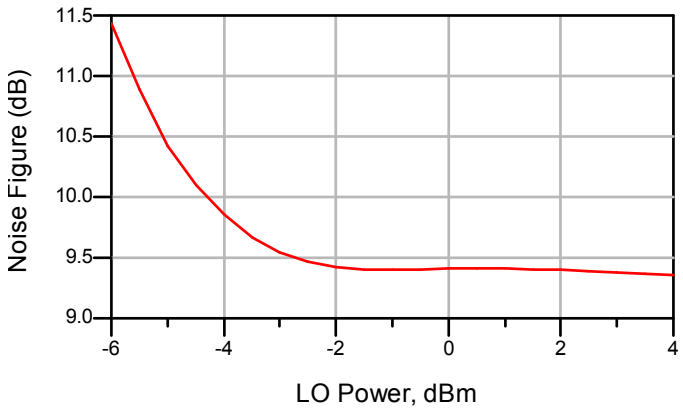


Figure 33 Noise Figure vs. LO Power Level

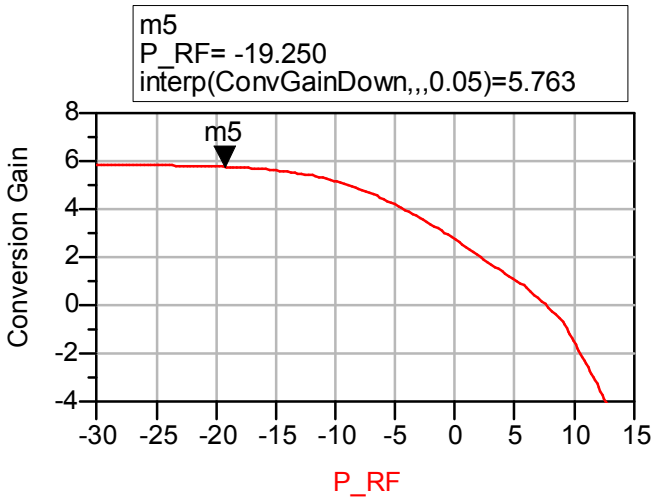
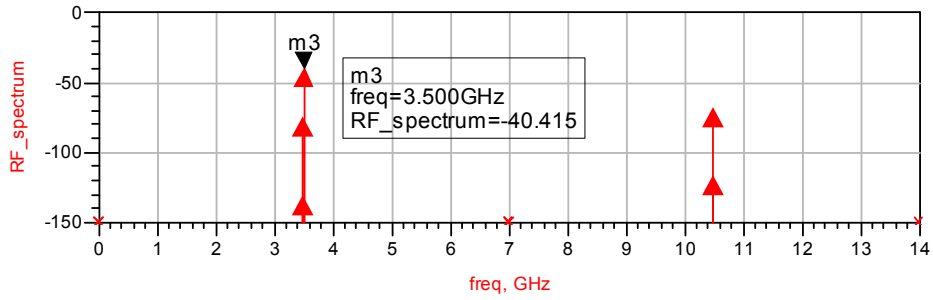
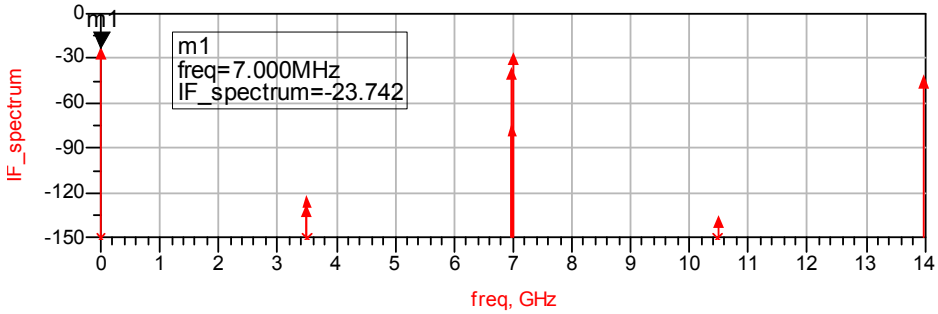


Figure 34 Conversion Gain vs. RF Power

Based on the WiMax receiver budget link discussed in Chapter 2, the RF input power for Gilbert cell mixer has been set in the range -20 dBm to -15 dBm, leading to a conversion of gain of about 6 dB (Figure 34). The input/output power spectrums are presented in Figure 35.



(a)



(b)

Figure 35 (a) RF Spectrum, (b) IF spectrum

To conclude, to reach a conversion gain of around 6 dB, the LO power should be set at 0 dBm and the RF power around -20 dBm.

4.8.2 Linearity

As mentioned in section 3.2.2, the system linearity could be evaluated through the 1dB compression point and the input third-order intercept point (IIP3). Therefore, a two-tone analysis was performed with the two RF frequencies f_1 = RF+Fspacing/2 and f_2 = RF-Fspacing/2, with Fspacing = 20 kHz (i.e., 3500.010 MHz and 3499.990 MHz, for a center RF frequency of 3500MHz). The third-order products at $2f_1$-f_2 and $2f_2$-f_1 correspond to 3500.03 MHz and 3499.97 MHz, respectively. As result, the undesired output signals will take place around 7.010 MHz and 6.990MHz, as shown in Figure 36.

Figure 37 shows an IIP3 of 1 dBm while the IIP2 was found to be 39 dBm. In this figure, the curves in dash lines are the real signal power while the sold lines represent the ideal behavior of the first and the 3rd order terms. At low input power values, these curves overlap whereas, when the input power continues to increase, the curves of the real signal power depart from their ideal behavior, showing compression. The point X at the intersection of the two solid lines of ideal behavior indicates the IIP3. Figure 38 shows a 1-dB compression point of -8 dBm.

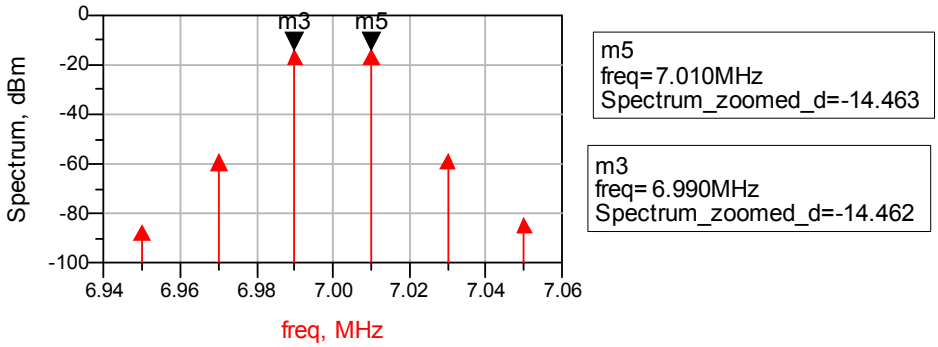


Figure 36 Two-Tone Output Product

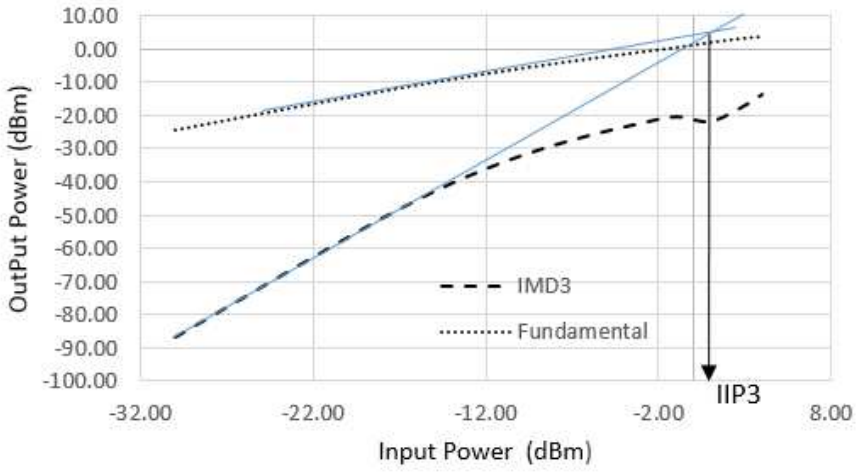


Figure 37 IIP3 Simulation

As for the Figure 38, the two curves show the ideal and the real fundamental signals. When the input is low, both the ideal and the fundamental are linear but at some point the fundamentals compress. When the difference between the two curves is 1 dBm, there we have the 1-dB compression point.

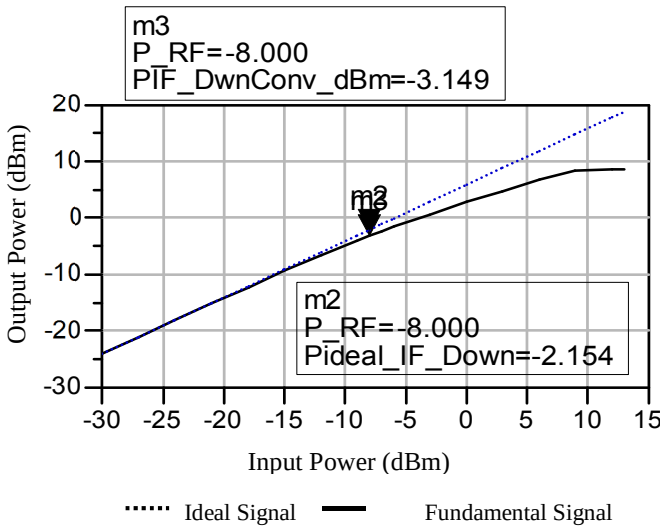


Figure 38 P1-dB Compression Point

4.8.3 Noise Figure

With a LO power level of 0 dBm, we obtained a SSB noise figure of 9.3 dB (Figure 39) and a DSB noise figure of 6 dB (Figure 40). This value is in agreement with the WiMax standards [16].

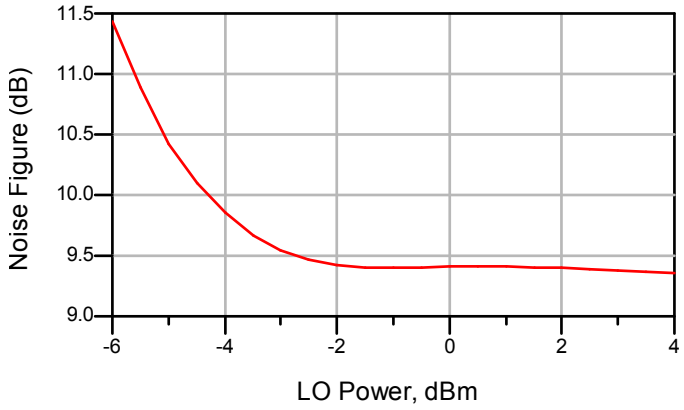


Figure 39 SSB Noise Figure

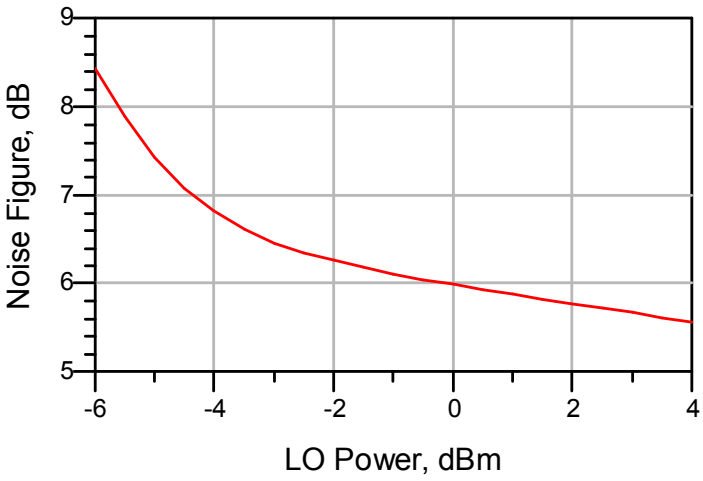


Figure 40 DSB Noise Figure

4.9. Co-simulation and Layout

4.9.1 Transmission Line:

Different transmission line widths were considered to get the 50Ω characteristic impedance. As seen in Figure 41, the most suitable transmission line width that can provides 50Ω characteristic impedance is around 70µm.

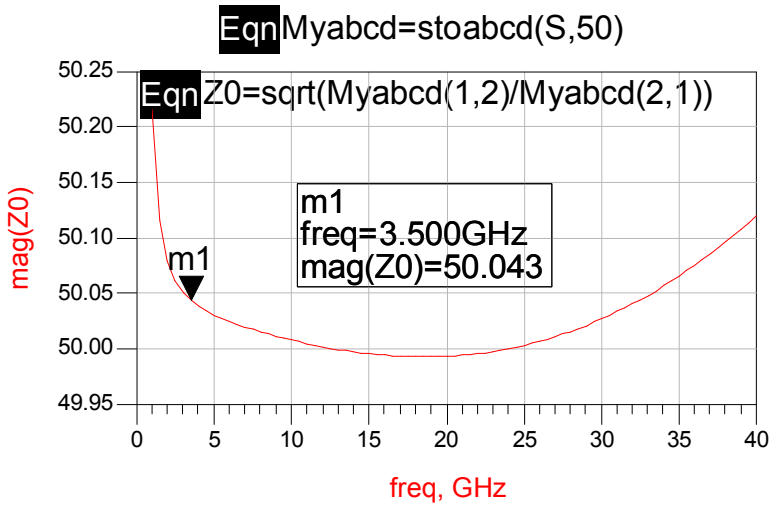


Figure 41 Characteristic impedance for 70 µm width

4.9.2 Layout Design

In the process of generating layout, note that the passive components used in this design are already built-in and taken from the design kit provided by "Win Semiconductor Crop."

The first stage to be implemented is the LO stage (Figure 42) and its co-simulation setup is shown in Figure 43. Using the same approach, all stages were implemented one by one in the layout and co-simulated to compare their performance with the equivalent schematic results. This technique is time consuming but it assures a good control on the layout generation in terms of performance degradation minimization while switching from schematic to layout. The layout ground is consider to be ideal. The full Gilbert-cell mixer layout is displayed in Figure 44 while the full co-simulation is displayed in Figure 45.

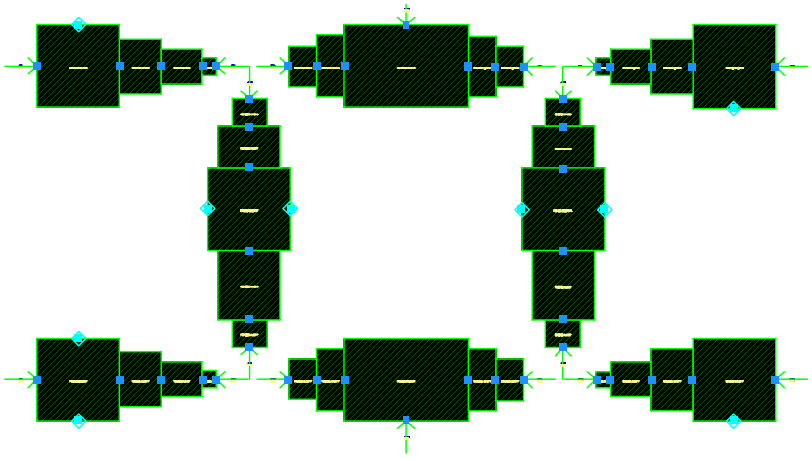


Figure 42 Layout of the LO Stage

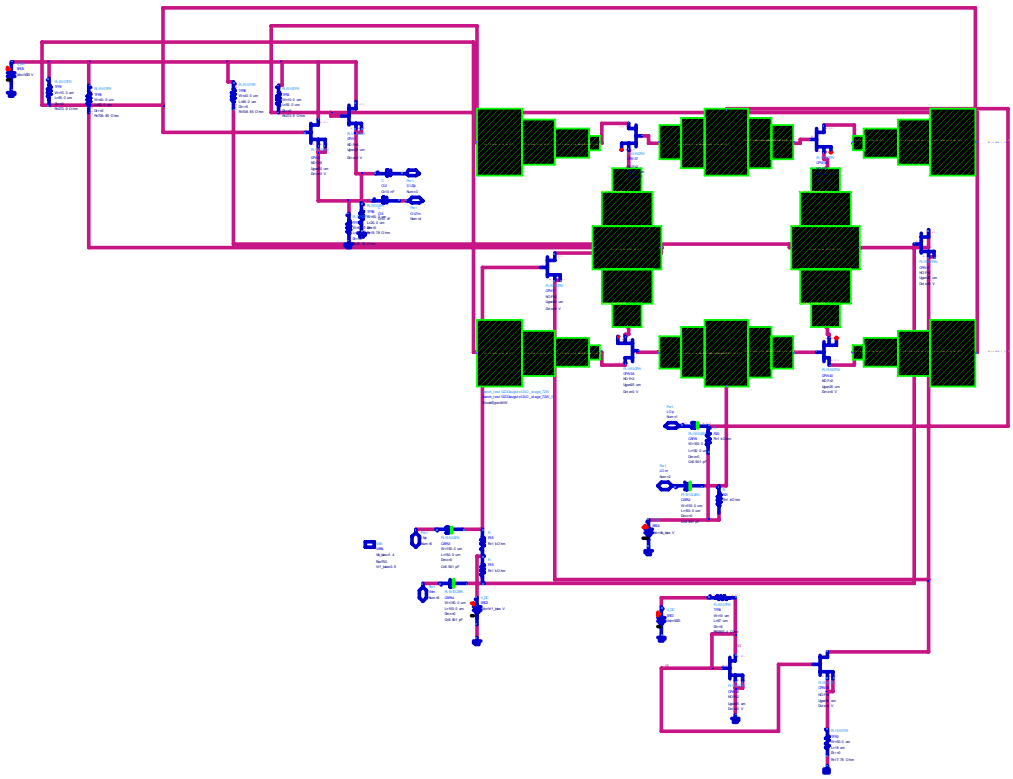


Figure 43 Co-simulation for LO Stage

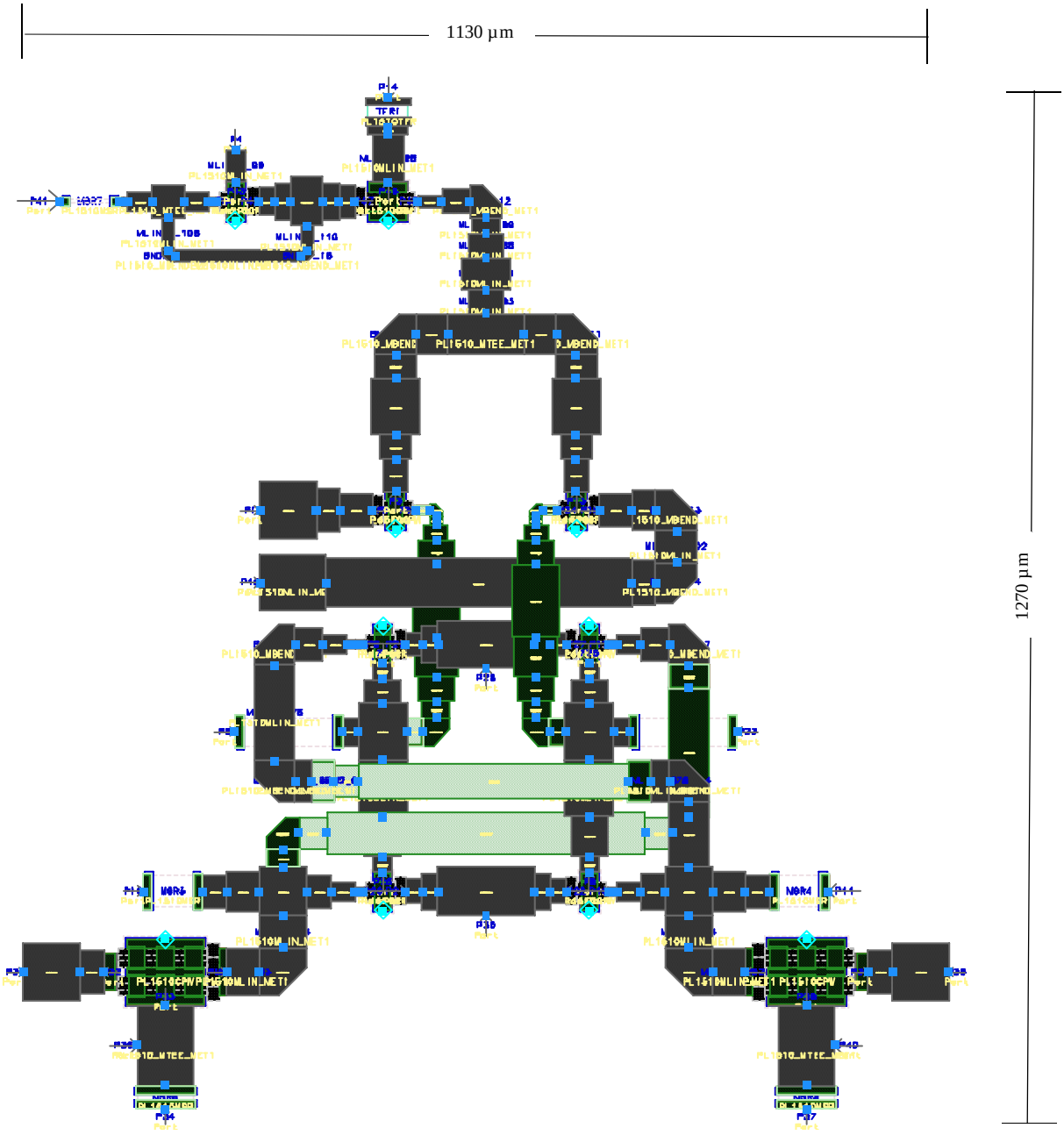


Figure 44 Gilbert Cell Mixer Full Layout

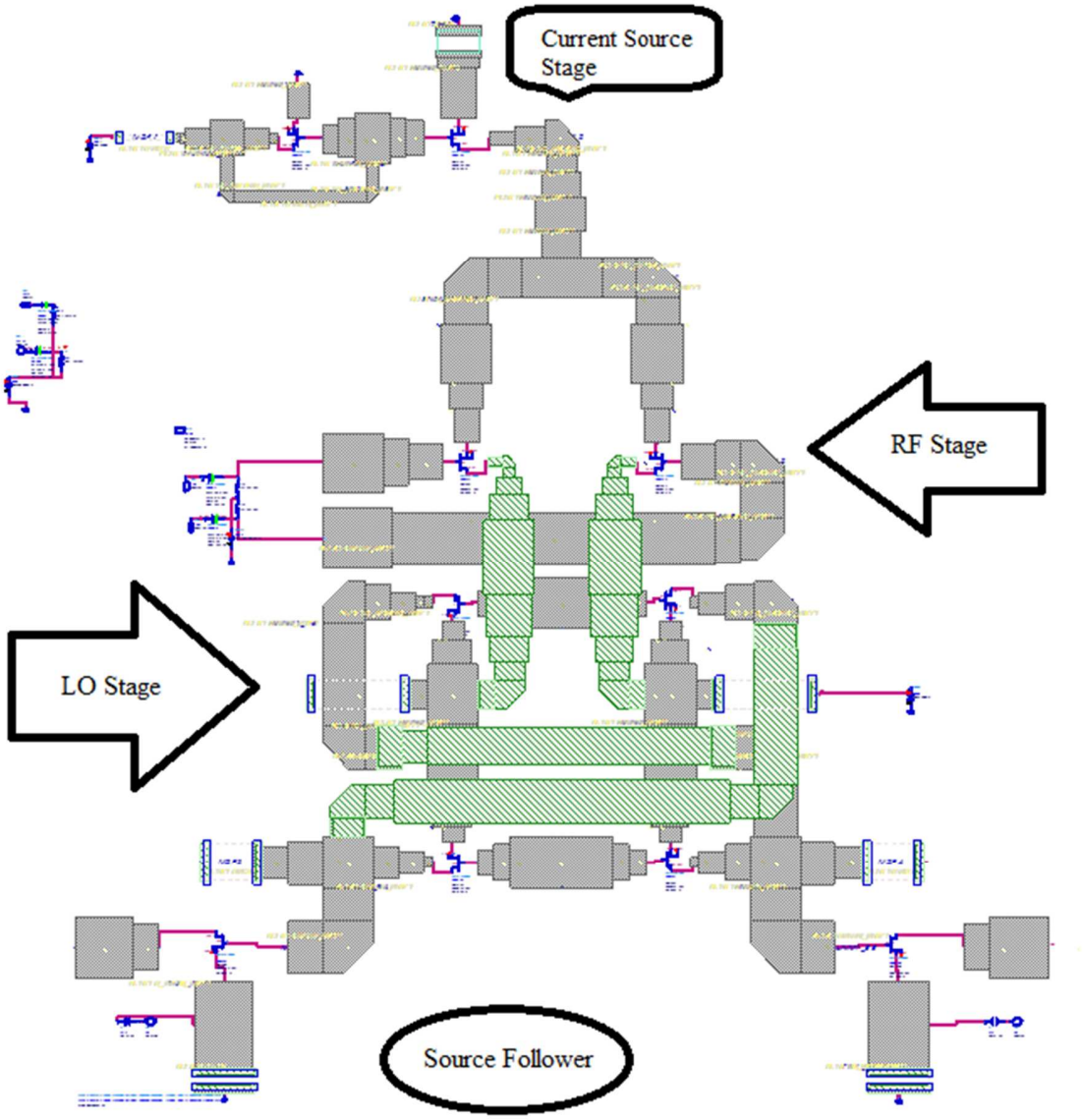


Figure 45 Full Co-simulation Schematic for Gilbert Cell Mixer

4.9.3 Co-simulation Results

The following subsection shows the co-simulation results of the conversion gain, linearity and noise figure for the designed down-converter Gilbert cell mixer.

❖ Conversion Gain

Figure 46 displays the conversion gain while sweeping the LO power. For the selected LO power of 0 dBm, the conversion gain from co-simulation is found equal to 5.1 dB.

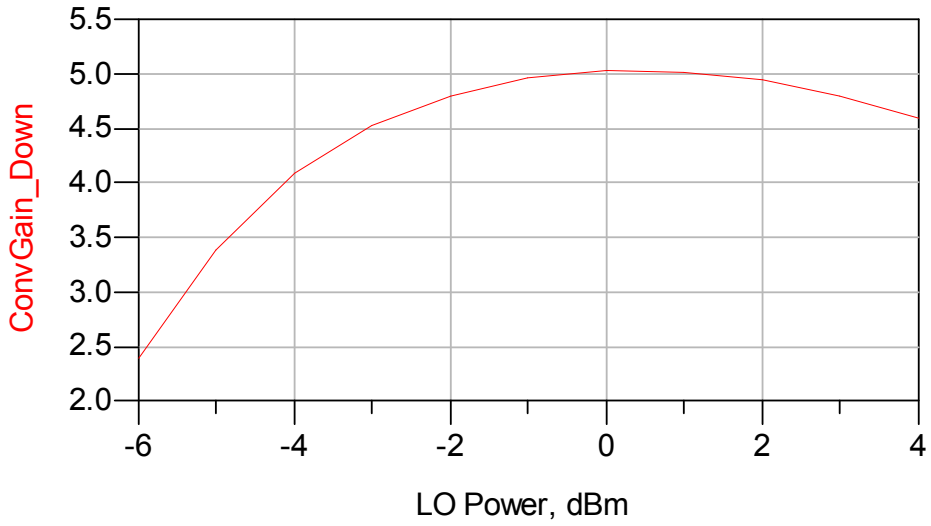


Figure 46 Co-simulation: Conversion Gain vs. LO Power Level

❖ Linearity

Linearity can be evaluated by IIP3, IIP2 and P1-dB compression points. Figure 47 shows the co-simulation results for both IIP3 and IIP2. The co-simulation achieved an IIP3 of about 1.5 dBm and an IIP2 of 36 dBm. The co-simulation result for a P1-dB compression point is -8dBm.

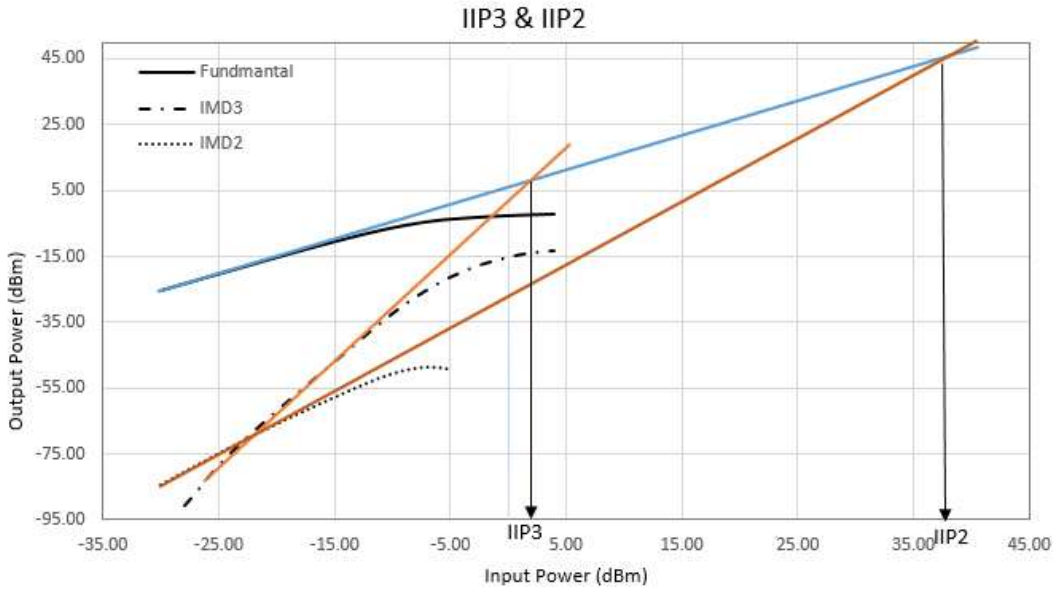


Figure 47 Co-simulation Results for IIP3 and IIP2

❖ Noise Figure

A SSB noise figure of 11.6 dB was achieved for 0dBm LO power (Figure 48). As for the DSB noise figure, it attained 8.4 dB at 0 dBm (Figure 49).

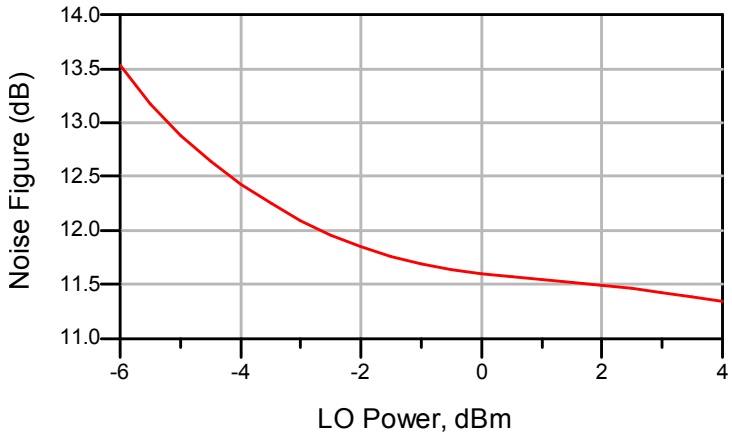


Figure 48 Co-simulation: SSB Noise Figure

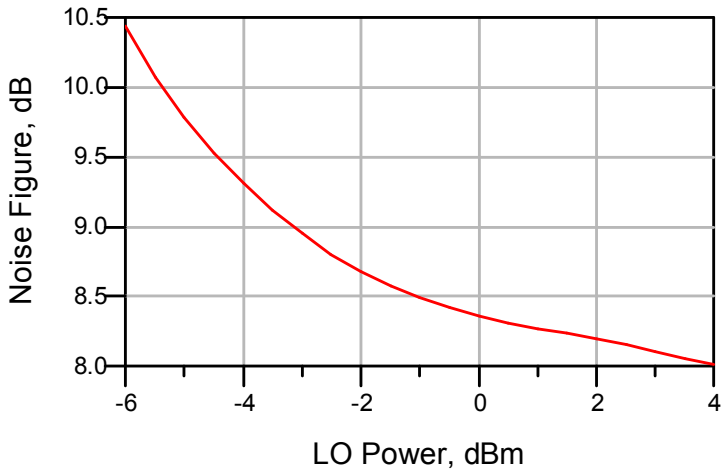


Figure 49 Co-simulation: DSB Noise Figure

4.10. Coupler or Baluns

In RF transceivers, most mixers are designed as differential circuits. Therefore, to supply differential RF signals from a single-ended RF signal, a coupler or balun is required. Baluns can be categorized as active baluns or passive baluns [56]. Passive baluns include power dividers, branch line couplers (90°) and rate-race couplers (180°). In this thesis, the rate-race coupler was retained because the circuit that has been designed requires a 180° phase shift between signals. Figure 50 demonstrates different type of rate-race power divider where the input, output and isolated ports allocated as clarified in Table 12. Figure 51 presents the Rate-Race coupler configuration including the transmission line impedance and wavelength that should be designed.

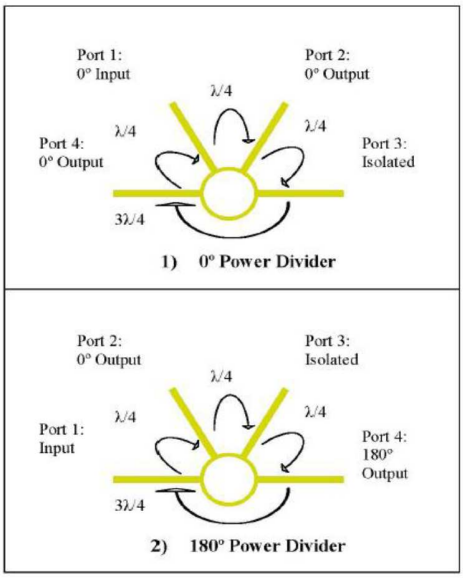


Figure 50 Power Divider Circuits Configurations [58]

Table 12 Rate-Race Ports Situations

Input Port	Output Ports	Isolated Port	Phase difference between output ports
1	2,4	3	180
2	1,3	4	0
3	2,4	2	0
4	1,3	1	180

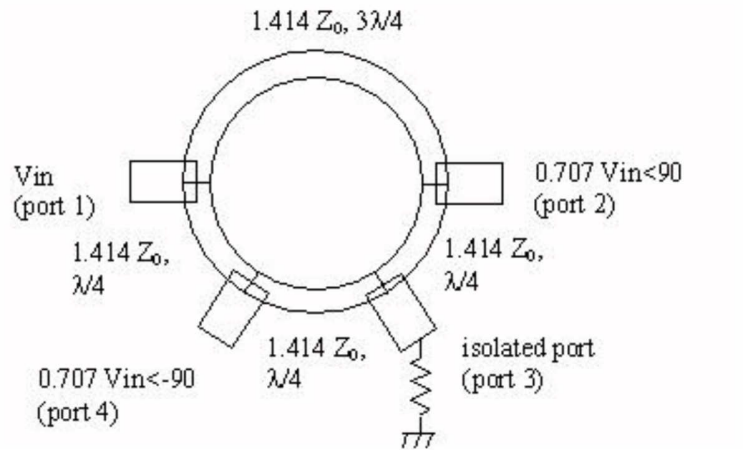


Figure 51 Rate-Race Coupler configuration [59]

In the Rate-Race coupler design, the width, length and radius of the transmission line displayed in Figure 51 have been calculated using the LinCalc tool from ADS. The results of this calculation are 27 µm of width, 7000 µm of length and 7400µm of radius. By looking for these results, the length and the radius are too large. Hence, the layout size is going to be large and impossible to fabricate.

The coupler layout size is illustrated in Figure 52. Using passive balun has advantage such as no dc power consuming. On the other hand, using inductors and micostrip line makes the design more lossy and hard to fabricate due to its size and cost [60]. Therefore, we looked for another option to apply instead of using passive coupler. Active baluns are a good alternative for WiMax application as reported in [56].

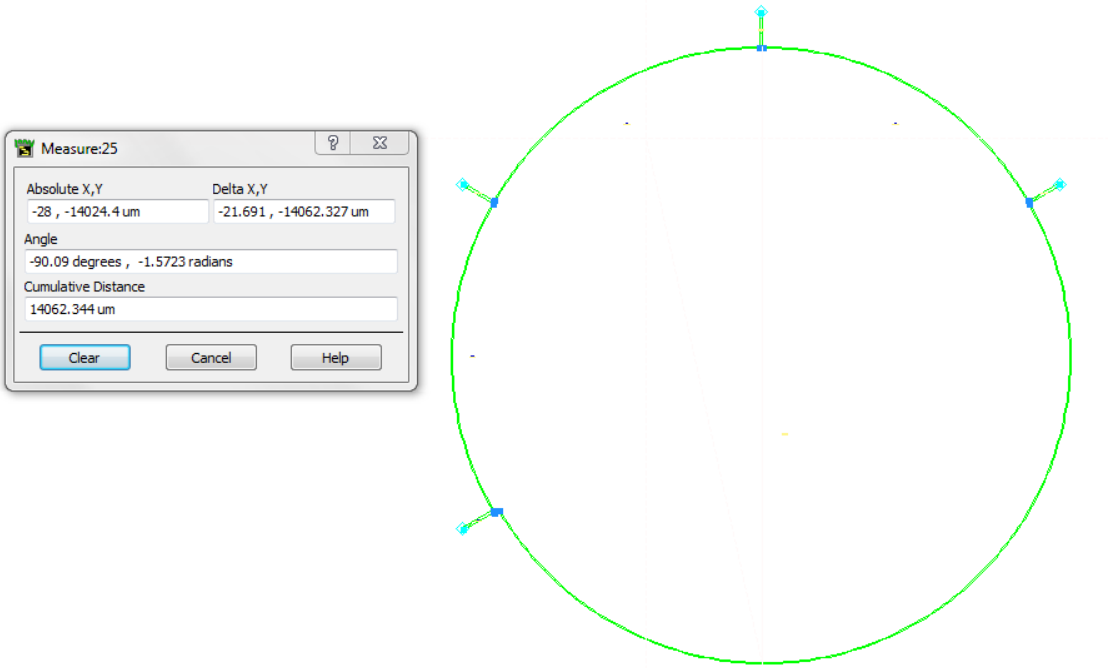


Figure 52 Rate-Race Coupler Size

4.10.1 Active Balun

Active baluns use active components such as transistors to convert the single-ended signal to differential ones and vice versa. Active baluns could be allocated in two ways such as in the front of LNA block as illustrated in Figure 53 or between the LNA and the mixer as seen in Figure 54. However, since active baluns usually exhibit high noise figure, the second configuration is the most widely used to implement these baluns as illustrated in Figure 54.

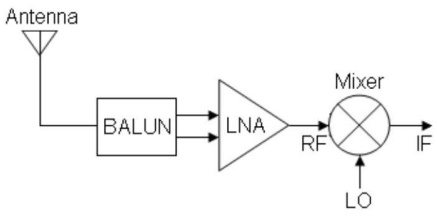


Figure 53 Active balun connected to LNA [56]

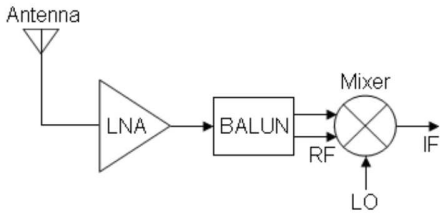


Figure 54 Active balun as intermediate block between LNA and Mixer [56]

In practical design, there are varieties of circuit configurations to implement active baluns with gain like the common-gate/source configuration illustrated in Figure 55 (a) or the differential configuration shown in Figure 55 (b). Figure 56 shows the simplest topology of active balun with a single transistor, which gain is less than unity [56]. The main concept of these topologies is to achieve phase difference of 180° between the two output nodes (RFout1 and RFout2) [56]. In fact, the main complexity to design active baluns is to achieve balanced gain between the two phases shifted ports.

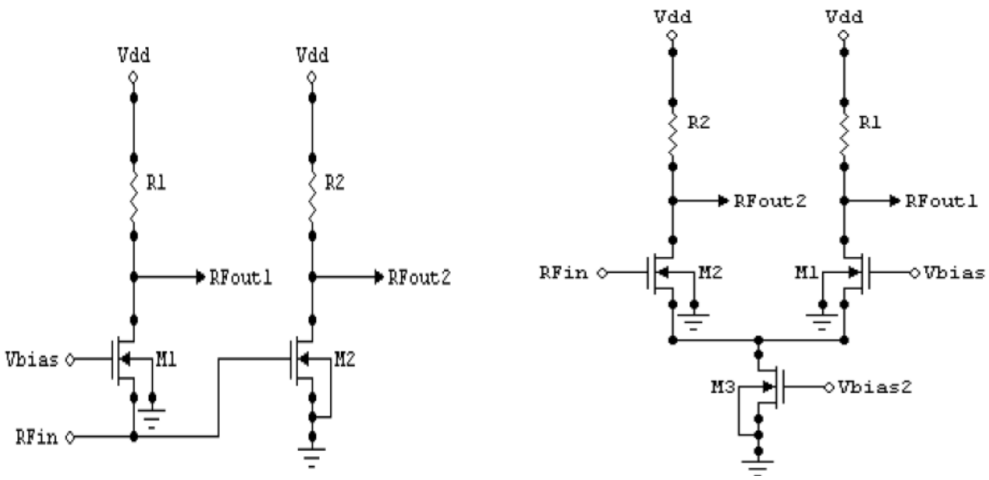


Figure 55 Active baluns circuits (a) Common-gate with common source (b) Differential [56]

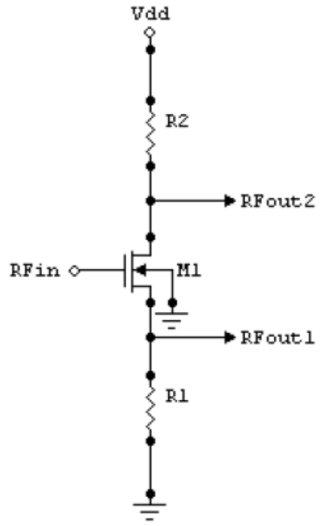


Figure 56 Common source/drain active balun circuit [56]

Using active baluns can provide gain and consume less chip area which is very important in our design; however, it is more complex to implement. Therefore, the design of active baluns is left as future work.

4.11. Discussion

To conclude this Chapter, a GaAs pHEMT transistor was first selected and its size optimized for optimum trade-off between gain, noise figure and power consumption, while meeting design requirements. With a transistor width of 25×2 µm, a DC simulation was performed and a DC analysis applied to determine the proper bias points for the circuits. Then, basic operation of Gilbert cell mixer was explained and improvement techniques introduced. The current bleeding or charge injection technique was retained to optimize the Gilbert cell performance. Next, the full schematic of the down converter Gilbert cell mixer was simulated and the results discussed.

Finally, a layout was generated, a co-simulation performed, and the obtained results successfully compared to those obtained by the schematic.

In Table 13, a comparison was made between the co-simulation results and those obtained by the schematic including conversion gain, noise figure, IIP3 and IIP2. Figure 57, Figure 58 and Figure 59 show the mixer results in terms of conversion gain and noise figure for both schematic and co-simulation. Also, the conversion gain and noise figure were simulated over the RF frequency as seen in Figure 60 and Figure 61. Finally, Table 14 shows the comparison of our designed Gilbert cell mixer performance with published works.

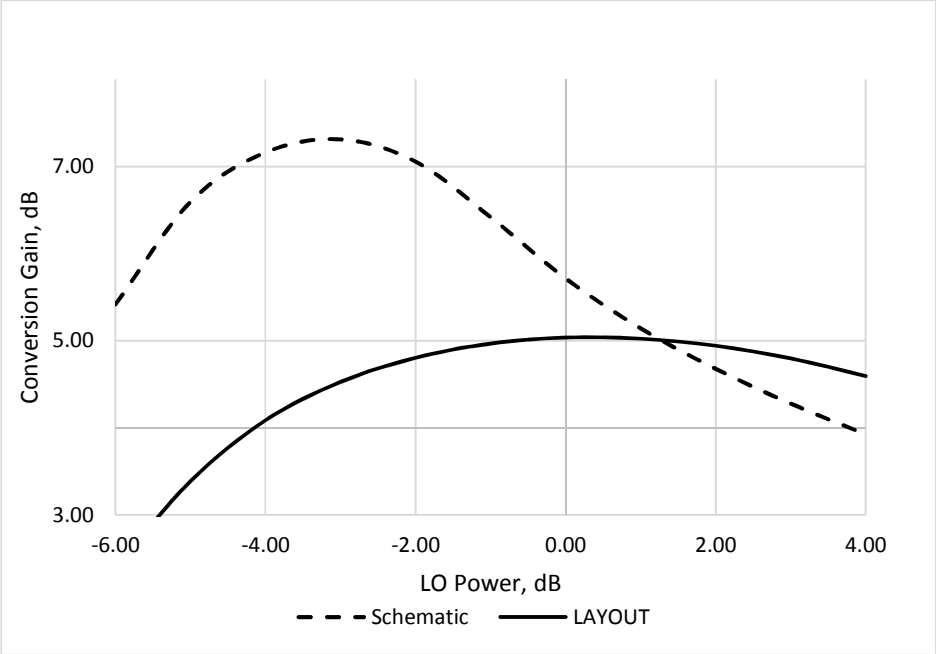


Figure 57 Conversion Gain Comparison

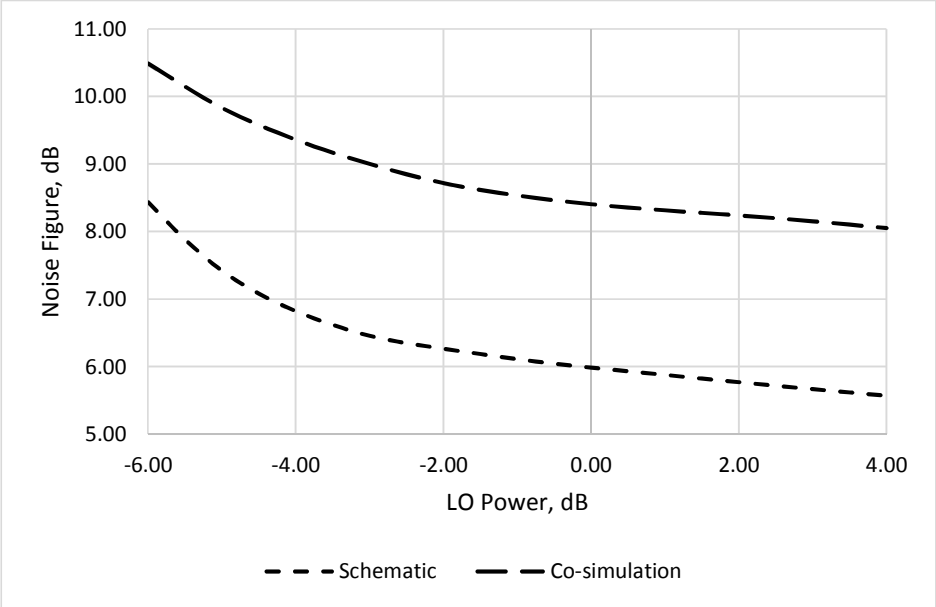


Figure 58 DSB Noise Figure Comparison

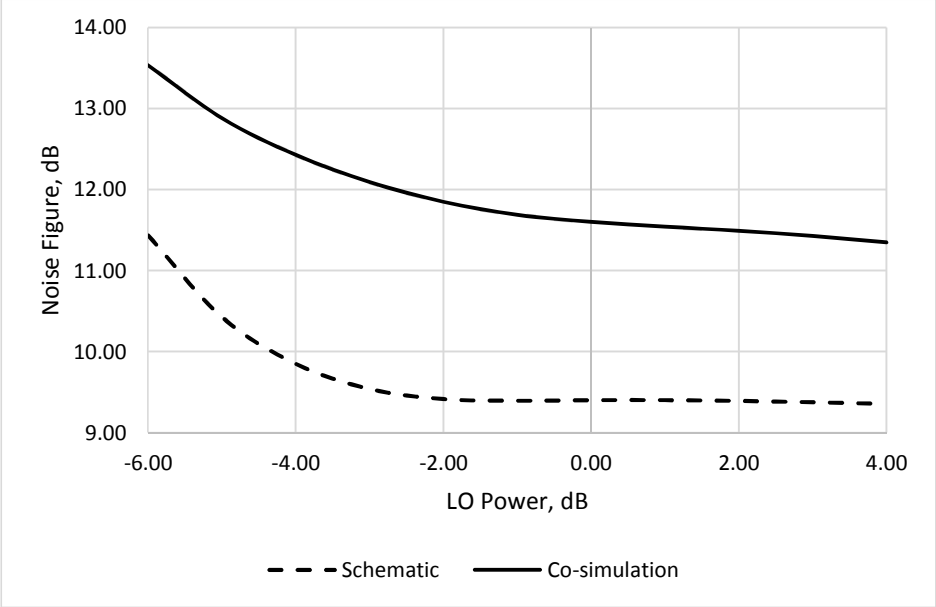


Figure 59 SSB Noise Figure Comparison

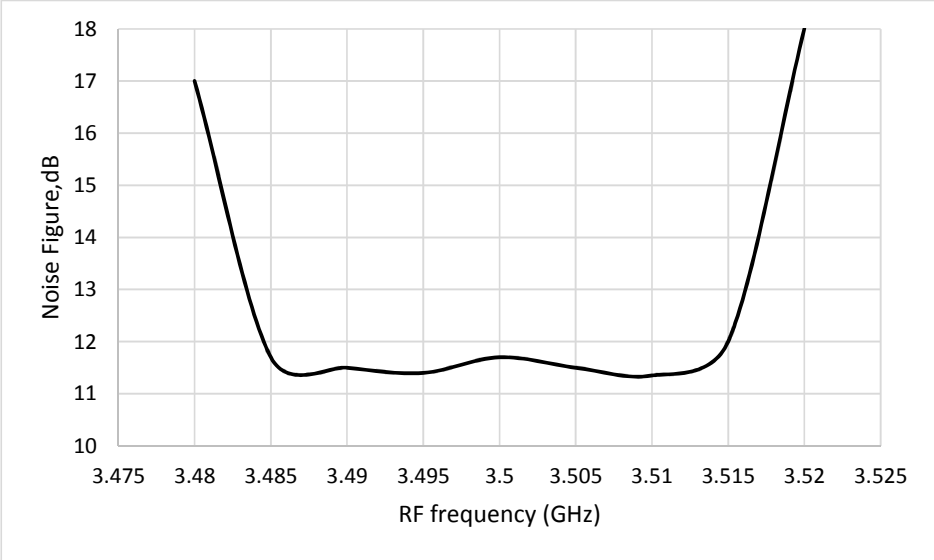


Figure 60 Co-simulation: noise figure vs. RF frequency

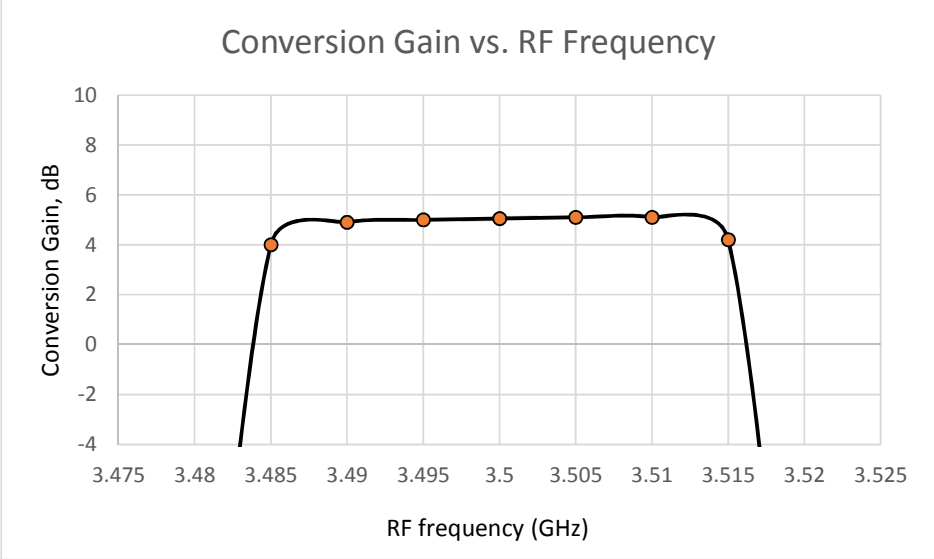


Figure 61 Co-simulation: conversion gain vs. RF frequency

Table 13 Gilbert Cell Mixer Results Comparison

	Schematic	**Co-simulation**	**Design Specifications**
Conversion Gain	5.7 dB	5.1 dB	Minimum 5 dB
Noise Figure (SSB)	9.3 dB	11.6 dB	Maximum 11 dB
Noise Figure (DSB)	6 dB	8.4 dB	Maximum 8 dB
IIP3	1 dBm	1.5 dBm	Minimum 0.3 dBm
OIP3	6.7 dB	6.6 dBm	Minimum 5.3 dBm
P1-dB Compression	-8 dBm	-8 dBm	-9.7 dBm
IIP2	39 dBm	36 dBm	32.4 dBm

As seen in the above table, there are slight differences between the design specifications constraints and the obtained results. In terms of conversion gain, the result that achieved in both schematic and co-simulation is better than the design specifications. This implies higher noise figure. So if the schematic noise figure for both SSB and DSB met the specifications, the co-simulation noise figures are slightly higher than the design specifications, mainly due to transmission line losses and parasitic coupling in layout.

Table 14 Mixer Performance Compared with Published Works

Ref	Technology	Topology	RF freq. (GHz)	IF freq. (MHz)	PLO (dBm)	P-1dB (dBm)	Gc (dB)	IIP3 (dBm)	IIP2 (dBm)	NF (SSB)	Pdiss (mW)
[23]	0.15 µm In-GaAs pHEMT	Gilbert-Cell	2.6		0	-6	6	-0.1	41	11 (DSB)	30
[38]	0.18 µm CMOS	Gilbert-Cell	2.4	10	-6	-9.8	0.44	10	N/A	11.4	5
[61]	0.18µm RF CMOS	LNFM based Gilbert**	3.5	20	-20*	-21	10.96	-11	N/A	6.5	10
[12]	0.18µm RF CMOS	Gilbert-Cell cancelation	2-11	20	0	N/A	21	5	N/A	22	12
Specs	0.15µm GaAs pHEMT	Gilbert-Cell	3.5	7	0	-4.7	5	0.3	32.4	11	39.6
Co-simulation	0.15µm GaAs pHEMT	Gilbert-Cell	3.5	7	0	-8	5.1	1.5	36	11.6	39.6
Schematic	0.15µm GaAs pHEMT	Gilbert-Cell	3.5	7	0	-8	5.7	1	39	9.3	39.6

*RF Power
**Low Noise Figure Mixer

Chapter 5. Conclusions

5.1. Summary

In thesis, the design of down converter Gilbert cell mixer for WiMax application was explored. This implementation was performed using the 0.15µm GaAs pHEMT technology process provided by "Win Semiconductor Crop. (WSC)". In WiMax, direct conversion architecture exhibits better performance compared to other configurations. It has high level of integration and less blocks, thus saves cost and power. From the WiMax requirements, taken from the IEEE 802.16 standard, a link budget for the down converter mixer was calculated including main design parameters.

Then, different mixer topologies were discussed and the Gilbert cell mixer was retained due to its better performance in terms of LO/RF/IF ports isolation, suitable gain, adequate linearity and even harmonics cancelation compared to other mixer types including single, dual-gate, and single balanced transistor mixers.

The Gilbert cell mixer design was implemented using GaAs HEMT semiconductors due their advantages of high noise performance, high transconductance (g_m) and high cut-off frequency (f_t). To further improve the performance of the designed Gilbert cell, different configurations were proposed such as the folded mixer, current reuse mixer, and current bleeding mixer. The current bleeding or charge injection technique was utilized because it reduces the voltage in the LO and RF stages while increasing the conversion gain in the RF stage by injecting more current.

The selected transistor was sized based on low noise figure and low power consumption. Also, the DC analysis was performed in order to specify the bias point for different design stages. Furthermore, a harmonic balance simulation was achieved to determine the main parameters of the Gilbert cell mixer including conversion gain, IIP3, OIP3, P1-dB, IIP2 and NF. The full Gilbert cell schematic was implemented and its design parameters successfully compared to the co-simulation results.

Finally, due to the mixer differential configuration, RF and LO inputs and IF output should be converted to single ended by using real couplers/baluns. Using a passive coupler, like a Rate-Race coupler, was an option due to its advantage of no dc power consuming; however, a problem has been faced in terms of large size. Therefore, we had to look for other options to use it as an alternative design. We found that active baluns can be the proper selection for WiMax application because they show advantages of small size while generating gain, but at the expense of more design complexity. Hence, the active balun design was left as future work.

5.2. Future Work

The down converter Gilbert cell mixer was designed for WiMax technologies to work at 3.5 GHz. The design presents good performance and is compatible with other existing designs. The Gilbert cell mixer achieves 5.1 dB of conversion gain, 1.5 dBm of IIP3, 36 dBm of IIP2 and 11.6 and 8.4 of single side band (SSB) and double side band (DSB) noise figure, respectively.

The following recommendations can be considered to further expand the direction of research:

- Inductive resonator could be utilized to reduce noise figure and improve conversion gain of Gilbert cell mixer as reported in [62].
- Due to large size and high cost in designing passive hybrids, active baluns need to be designed and implemented at RF, LO and IF ports. Matching networks could be required once the active baluns will be connected at the ports.
- The present work could be extended to mobile systems, which will require redefining specifications to be met. One of the major design objectives will involve dc power minimization.
- Designing a device which can operate with different applications, i.e., a multi-band multi-mode mixer.

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