Design Approach for Thermal Performance Enhancements of a Pico-Cell Base-station Power Amplifier in Gallium Nitride HFET Technology

By

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Abstract

As newer and more powerful technologies emerge in the market, the desire for compactness and aesthetics drive designers to aggressive new heights. The trend of technology is quite simply to deliver high-speed designs that pack more power while seeing reduction in form factor for ease of use at the consumer level. This presents new challenges with reliability, cost, and ultimately what the consumer strives for: performance. It is inevitable for a small compact size device, such as a smartphone or wireless repeater, to face heating issues when packing large amounts of power.

The goal of this thesis is to characterize an in-market device's thermal behavior and RF performance, and present an alternative design approach that helps improve thermal performance. This solution must not increase the design space or form factor excessively. The proposal utilizes an off-the-shelf solution and predicts performance improvements and degradation as a function of thermal performance. Electro-thermal simulators are used extensively to gauge the behavior and flow of heat within a gallium nitride device, and used as a baseline for comparison. Two modified approaches are presented and declared to be more efficient and reliable than the baseline.

The design approaches comply with the industry standards of minimizing size and show a clear improvement in thermal behavior that can be utilized for any single device approach. The research is focused under similar power and biasing conditions so that designers can effectively implement a simple plug and play approach whenever the device under test is at risk of violating temperature limits and/or if performance degradation is observed under a variety of operating conditions.

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List of Acronyms and Abbreviations

AlGaN	Aluminum Gallium Nitride
ET	Envelope Tracking
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HBT	Hetero-Junction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HFET	Hetero-Junction Field Effect Transistor
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LED	Light Emitting Diode
LTE	Long Term Evolution
MESFET	Metal-semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
MPR	Maximum Power Reduction
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PCB	Printed Circuit Board
PA	Power Amplifier
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
Si	Silicon
SiC	Silicon Carbide
UE	User Equipment

Chapter 1 - Introduction

As technology continues to evolve, one of the most striking consistencies with the enhancement of technology is the need to pack higher power into smaller form factors. Clear evidence of this is the common smartphone that continues to challenge its' industry by packing in more computing power than ever and introducing more compact form factors in competition for consumer satisfaction. The most obvious concern is on how the system uses all this power in such a restricted design area and maintains thermal integrity for proper functionality and safety. High-tech industry is key in driving innovation on power and thermal integrity. A device such as a smartphone will pack several antennas along with power amplifiers to satisfy wireless radio conformance and reliability, and with faster broadband speeds and data rates accompanied with 4G LTE standards, introduces more overall power to the system in a decreasing form factor. Designers then need to focus on technologies and methods to improve efficiency and characterize thermal properties.

The challenges faced today can be broken down to constraints with electronic packaging (since the demand is for chips to reduce in size) and thermal designs that take into account such constraints of packaging. More and more devices can be added to chips and the rate of device density growth is not met with advancement in low power semiconductor technologies. Heat removal or sinking technologies have also been slow to catch up [1]–[3]. In essence, most electronic equipment failure is related to temperature. It's only natural as device speed and density increase, power dissipation follows suit. Heat spreaders and sinks can be added to help prevent this lost power from affecting the rest of the system, however more focus is now being placed on optimized chip design for thermal performance.

Thus, the focus becomes on understanding thermal principles and characterizing its' relation to device performance. A radio frequency (RF) power amplifier (PA) in particular packs lots of power in a constrained packaging and requires little to no degradation to the amplified signals. Most 4G technologies require the use of pico-cell base-stations to extend coverage of networks

in smaller areas where outdoor signals do not reach well. Pico-cell base stations cover smaller areas that require wireless coverage, such as office buildings and aircrafts. LTE signals, which offer some of the highest speeds, are the most prominent networks requiring added network capacity and thus require the use of pico-cells. Access points and wireless repeaters readily amplify targeted signals with the use of RF PAs and with high-speed wireless technologies such as LTE in demand; therefore, an obvious focus is placed on RF PAs and thermal performance. A pico-cell also is in its simplest form an amplifier that consumes large amount of power, and thus is chosen as the usage case for this thesis.

1.1 RF Power Amplifier Challenges

RF PAs, be it in smartphones or pico-cells, face challenges on minimizing size and maintaining linearity and efficiency. An RF amplifier needs to satisfy power delivery at high frequencies, but based on design often faces challenges with linearity and efficiencies. Class-A amplifier for instance offers better linearity but worse efficiency due to conduction of an entire cycle which increases power consumption and as well as quiescent current. Class-B only conducts for half the cycle so it isn't ON the entire period and is allowed to be more efficient, but less linear creating large amounts of distortion [4]. Ideally, a designer will need to use balanced tradeoffs between the two to ensure proper performance of the PA.

Among key targets of a microwave amplifier are gain and power delivery specifications. Efficiency is one of the key parameters that achieves these requirements and also relates to the thermal performance of the device. The more efficient the device, the less power is lost and converted to heat. Thus, it can also be argued that thermal properties of an RF PA affect overall power delivery and gain, not just reliability of device. Designers not only need to design with RF principles in mind but also need to now focus on analog principles surrounding thermal behavior of a device.

1.2 Design Space Challenge

Several techniques exist to improve efficiency of an amplifier, such as impedance matching, load-pull analysis, biasing points, pre-distortion, etc. Device geometry is another factor that can improve efficiency when there is plenty of design space or real estate to use to minimize losses; however with evolving technologies this is not a feasible option as it opposes demand of minimizing form factors. Pico-cell base stations are required to use minimal area while transferring large amounts of power as efficiently and linearly as possible. It is here where new wideband semiconductors such as Gallium Nitride (GaN) hetero-junction field effect transistor (HFET) present form factor benefits. GaN technology and chemistry allows for larger power densities of 30W/mm, thus allowing the ability for transistor sizing to be smaller and packing larger amounts of power [5, 6]. GaN devices can operate at higher frequencies and transmit higher power than common technologies such as gallium arsenide (GaAs), silicon carbide (SiC), and silicon (Si). The technology also offers lower parasitic losses, which allow GaN to be a more efficient option. GaN is a fairly new technology that is being implemented today in the market and is an apt solution to overcome tight space constraints for high-powered devices.

1.3 Research Goals

It is abundantly clear to designers the importance of mitigating thermal deficiencies of RF devices for performance and safety. Cell phones and pico-cells will always pack large amounts of power in small compact areas, which will present challenges for designers.

The focus of this thesis is to characterize and enhance the thermal performance of an in-market RF amplifier suitable for a 4G Pico-cell base station. To meet this goal, the market design will be recreated in Agilent ADS for simulating true performance of the amplifier, and then analyzed and characterized for thermal behavior. The thesis will focus on high-powered devices such as a GaN high electron mobility transistor (HEMT) to transmit an LTE signal, and correlate RF and Thermal performance of the PA. After recreating the design and performance, further thermal

analysis will be performed on a similar device for the purposes of presenting design techniques that improve overall performance of the device, with the focus being on thermal performance of RF power.

1.4 Thesis Contribution

An in-market GaN design is characterized for its RF performance over temperature. The thermal effects taking place due to the junction or channel temperature will showcase the steady degradation expected within the FET model's performance for gain, power delivery, and efficiency. After the characterization of the circuit, further research is performed at the device level with regards to temperature. A thermal solver is utilized to model and predict heat and power dissipation on a GaN FET. A multi-cell solution in a parallel architecture is then presented to improve the original in-market circuit by showing improvements in temperature at the gate and the resulting RF performance. The solution focuses on the characterization and distribution of temperature over the proximity between the cells. All contributions are simulation based.

1.5 Thesis Organization

The content of this thesis is divided into six chapters. Chapter 1 presents an introduction on the thesis topic and presents motivations and research goals.

Chapter 2 provides a design background that is essential for thermal analysis. It is these principles that make up the basics for a PA design, and the parameters that are deemed most crucial to thermal performance are discussed.

Chapter 3 presents information on a variety of semiconductor technologies that are available in the market today. It compares characteristics of these technologies and provides more details on the most recommended technology for thermal performance. IT concludes the need for

focus on such technology and discusses the model chosen to perform research with for this thesis. Preliminary simulation data is also shared in this chapter.

Chapter 4 shares detailed analysis on the recreating of an evaluation board. This details the system under which the research is performed and presents data to validate the simulation results versus datasheet results for accuracy. Schematic level thermal analysis is performed with the model and the results and correlations between RF performance and temperature are presented.

Chapter 5 presents improvements to the design in chapter 4 and achieves this by analyzing a GaN FET in a similar environment as the model under test in chapter 4. The in-depth analysis is done with load-pull simulations and an electro-thermal simulators, providing one of the more unique analyses ever performed with on a GaN device. This chapter ultimately presents different design approaches that improve thermal performance and can be applied to most designs in the market today.

Finally, chapter 6 summarizes the contents of this thesis and provides ideas for future research on the topics discussed in this thesis.

Chapter 2 - Design Background for Thermal Analysis

A significant portion of a wireless base station power budget is consumed by the transmitting RF PA. Since the PA can account for more than half of the base-station or pico-cell's power usage, PAs have been the focus of efforts to improve power-added efficiency (PAE). The PAE is a measure of how well a PA can convert DC power into RF/microwave power [7, 8]. PAE is dependent on the overall gain of the device, and can vary based on the class of PA being used and configured. This section will explain the different classes of PA design and the importance of PAE optimization for thermal performance.

2.1 Classes of Operation

Power amplifier circuits are classified for different methods of operation based on the application. The classes that define the output stages of a PA are A, B, AB, C, D, E, and F. Each class varies in its conduction angle during which it passes current through the transistor and can be set with a biasing point. For instance, if the conduction angle is chosen at 360 degrees (Class A), the device would always be ON and very linear but not very efficient; similarly a half cycle has a conduction angle of 180 degrees (Class B) and the device would only operate for half the cycle allowing for higher efficiency but not much in terms of linearity. This angle, and thus biasing point, affects just how power efficient and linear the PA can be. Class-AB is by far the preferred choice for designers as it offers a compromise between both linearity and efficiency [4]. See Figure 1 for DC-IV plots for different classes of operation and ideal bias points.

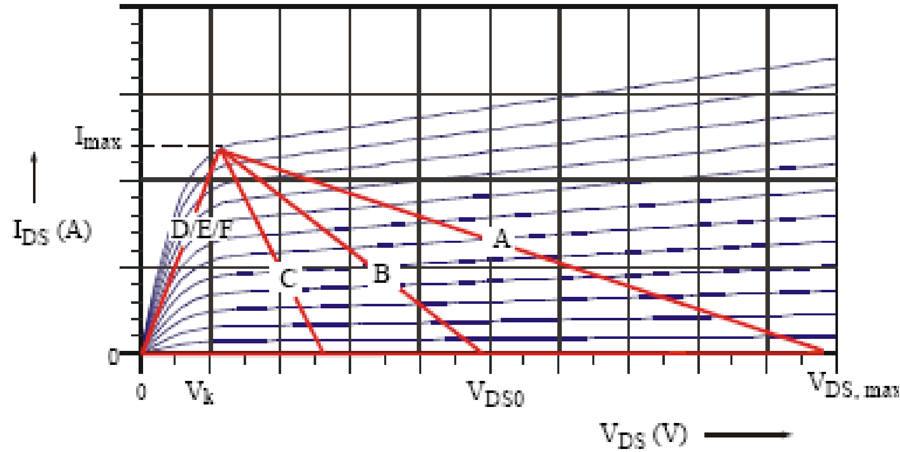

Figure 1: Load lines for different classes of PA operation [4]

This chapter will analyze these four classes of power amplifier operations and their various characteristics.

2.1.1 Class-A

This class of amplifiers is defined as a PA that is biased so that the current flows all the time and the input signal drive level is kept small enough to avoid driving the transistor into cutoff. As mentioned earlier, this is another way of saying that the conduction angle of the transistor is 360 degrees, meaning the transistor conducts for the full-cycle of the input signal. This allows Class-A to be the most linear class of amplifiers. In terms of linearity, this means the output signal resembles the input signal very closely. The DC input power is constant and the theoretical maximum efficiency of a Class-A amplifier is ~ 50%. The DC power consumption can be calculated as in Equation 2.1 [4].

$$P_{DC} = \frac{(V_{DD})^2}{R} = V_{DD} \times I_{DQ} \tag{2.1}$$

where V_{DD} is the drain voltage and I_{DQ} is the quiescent current at roughly half of the maximum current. See Figure 2 for the amplifier's bias point and conduction cycle.

A drawback to being ON at all times is the higher quiescent current. This degrades efficiency as the conduction cycle always continues and inherently requiring more DC power. The transistor on-resistance and presence of load reactance also affects the efficiency degradation. Conversely, the absence of harmonics allows Class-A amplifiers to be used at frequencies close to the maximum capabilities of the transistor. Therefore, when accounting for their lower efficiencies, Class-A amplifiers are ideal for applications requiring low power, high linearity, high gain, broadband or high-frequency operations [4]. See Figure 3 for the transfer cycle of Class-A amplifiers.

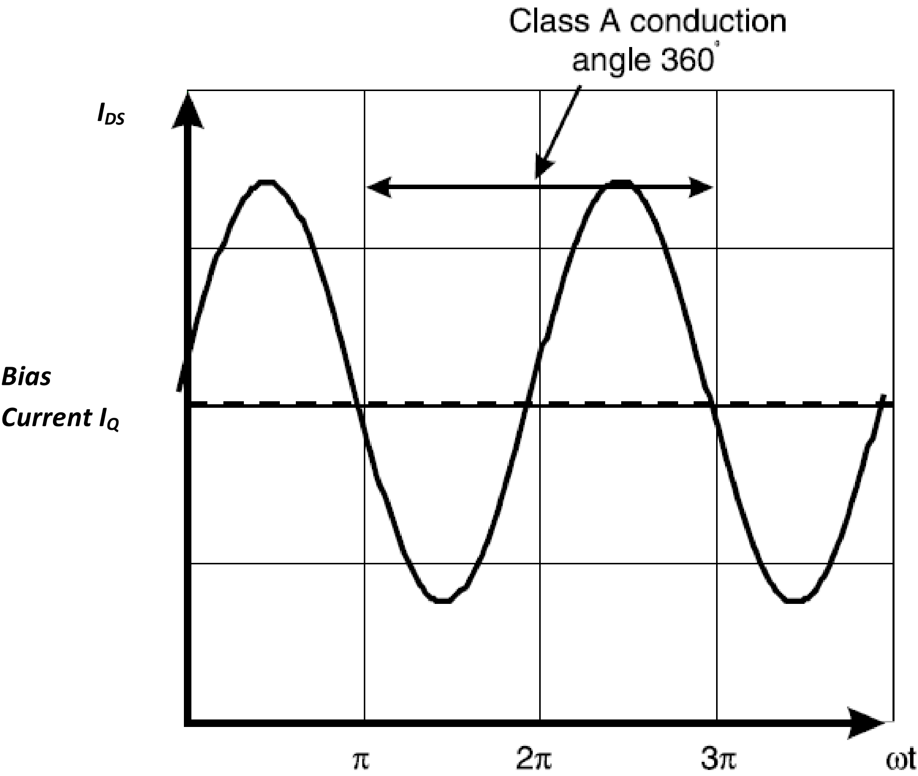

Figure 2: DC Bias point and conduction cycle of Class-A amplifier [4]

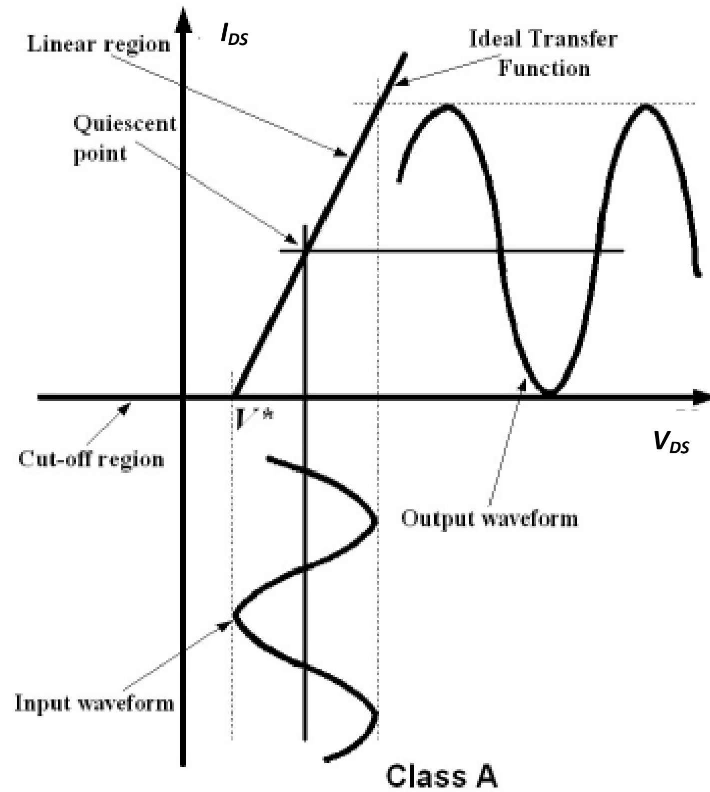

Figure 3: Transfer characteristics of Class-A amplifier [4]

2.1.2 Class-B

This type of amplifier conducts with an angle of 180 degrees, or simply put, it conducts half the time either on the positive or negative half cycle of the input signal. The quiescent current is nearly zero due to the biasing point being near the cut-off voltage of the transistor. Due to this operation, this class type is much more efficient but produces more distortion in the output [4,7].

Class-B has a theoretical maximum efficiency of ~ 78.5% since the amplifying element is switched off for half the cycle, thus dissipating less power. The tradeoff as mentioned before is linearity as this amplifier will produce quite a bit of harmonic distortion that will require

filtering at the output. The DC power consumption can be calculated as shown in Equation 2.2, where I_{AC} is the maximum AC output current [4].

$$P_{DC} = 2 \times \frac{(V_{DD} \times I_{AC})}{\pi} \tag{2.2}$$

Since the amplifier only conducts for half the cycle of the input signal when using a single transistor, it requires some resonant circuit in the output network to produce the remaining half of the signal. A common approach instead is to implement a push-pull configuration where two transistors are used for each cycle of the input signal to produce the entire signal at the output. This parallel configuration does not offer better efficiency than a single transistor approach, but it does allow for more power to be output. See Figure 4 for Class-B biasing and operation. [4]

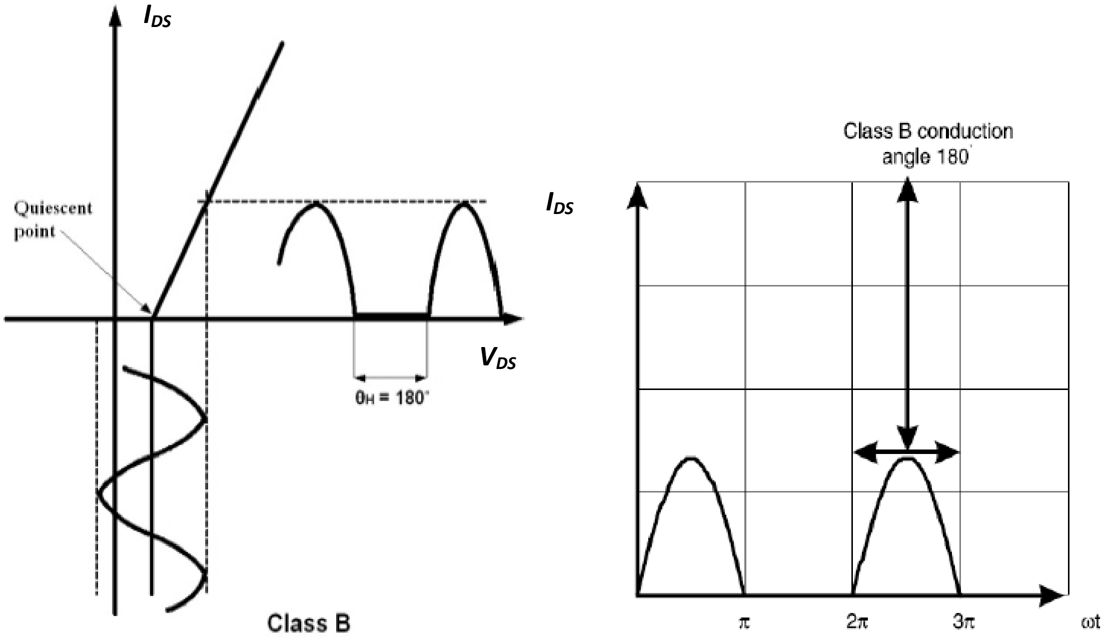

Figure 4: Biasing current and conduction angle for Class-B amplifiers [4]

2.1.3 Class-AB

This type of amplifier offers a true compromise between linearity and efficiency by utilizing key techniques from both aforementioned classes of amplifiers. The devices are biased so that they're not completely off when not in use. This strikes a balance between both class-A and B types, and can be seen in its' operation [4, 6, 7].

The transistor is biased to a quiescent point set between cutoff and Class-A bias point, approximately 10-15% of the drain current. True to its description, the conduction angle is between 180 and 360 degrees which helps improve linearity; it also offers an efficiency anywhere between the 50% and 78.5% offered by Class-A and Class-B respectively. See Figure 5 for biasing and operating points of a Class-AB amplifier [4].

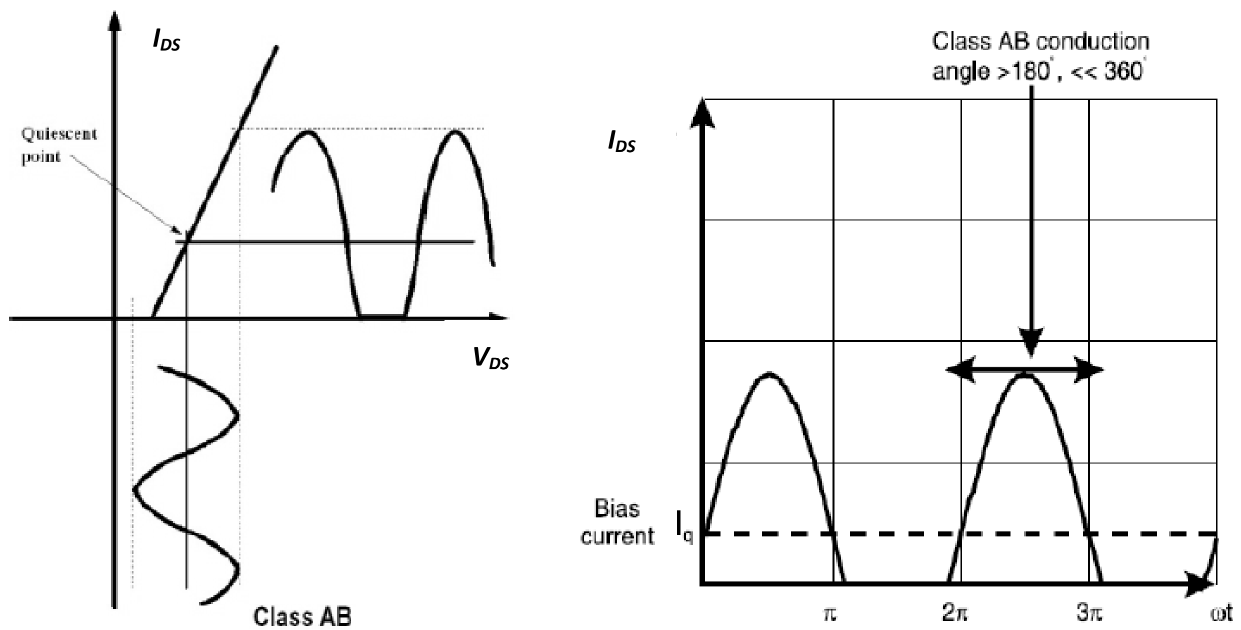

Figure 5: Class-AB biasing point and operation [4]

2.1.4 Class-C

The amplifier classes discussed earlier have shown a strong correlation of the conduction cycle to both linearity and efficiency. An option to achieve a maximum theoretical efficiency of approximately 85% is available with the use of a Class-C amplifier, which conducts at an angle significantly less than 180 degrees [4, 7]. However, this offers the poorest linearity of all the amplifier types and thus is not often used in higher RF and microwave frequency applications. See Figure 6 for biasing and operation of Class-C amplifiers [4].

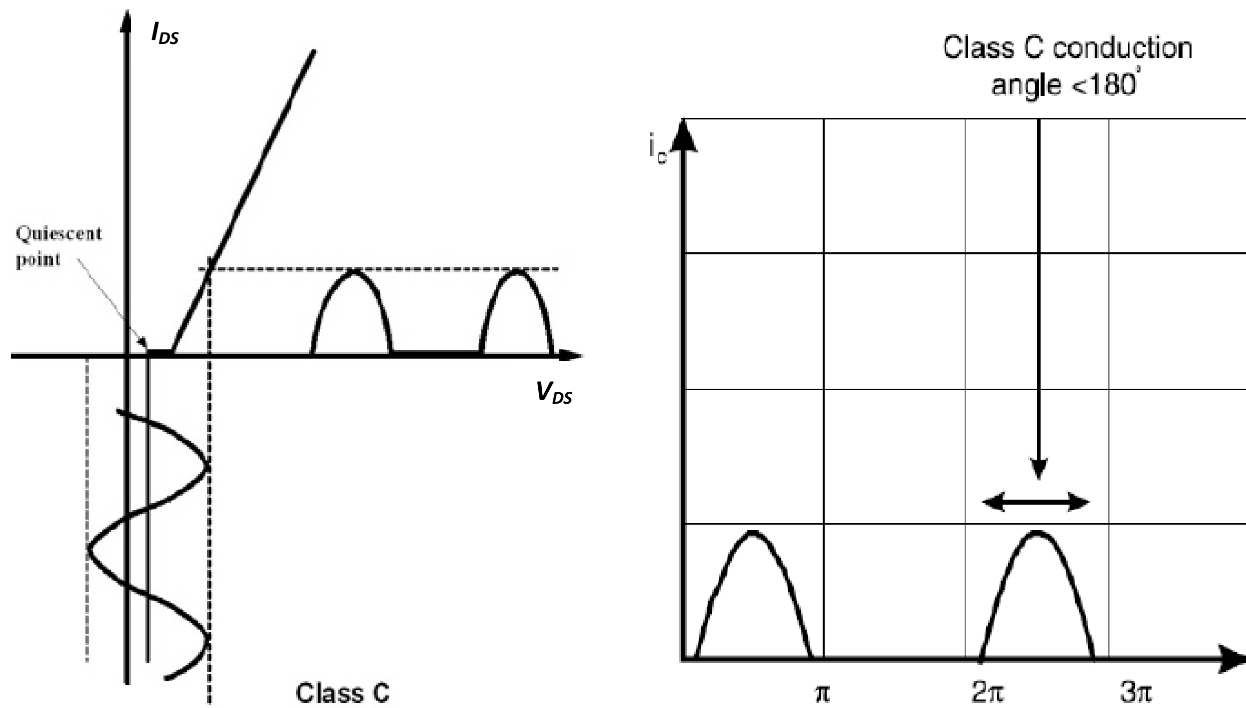

Figure 6: Class-C operation and biasing point [4]

2.1.5 Additional Classes

Additional power amplifier classes exist that are specifically focused for high-efficiency performance. These include Class-D, E, F, G, H power amplifiers. A stark contrast in techniques is seen with these classes as opposed to the biasing and operating cycles seen with the amplifiers covered earlier. For example, Class-D and E amplifiers use switching circuitry to improve efficiency, and Class-F uses harmonic resonators in its output stage to achieve higher efficiency [6,7]. However, these techniques are focused solely on narrowband-tuned amplifiers that do not require linear operation and therefore are used in more focuses applications such as audio and power supplies [4].

2.2 Efficiency

Efficiency is defined as a device's ability to convert energy from one source to another, typically from an input to an output. For an RF power amplifier, the measure of efficiency is based on the device's ability to convert DC power into RF power. The energy that isn't converted between DC and RF is dissipated and released as heat. As a result, lower efficient devices dissipate more heat and produce less RF power that will affect device performance. The released heat can also adversely affect the system that can result in catastrophic failures. Efficiency, therefore, becomes a key design parameter for high-power devices. The maximum efficiency of a microwave device is a function of frequency, temperature, input drive level, load impedance, bias point (as covered in amplifier classes), device geometry, and intrinsic device characteristics [8].

2.2.1 Drain Efficiency

Drain efficiency is the measure of how much DC power is converted to RF power. The DC power is supplied through the drain or collector of the device under test. See Equation 2.3 for details on how to calculate this parameter. While a valuable piece of information, this calculation does not take into account the real input RF power going into the device and thus not accounting for the gain seen by the device. Hence, it is typically not treated as a true benchmark evaluation for the device under test [8].

$$\eta_{drain} = \frac{P_{RFOUT}}{P_{DC}} = \frac{P_{RFOUT}}{V_{DC} \times I_{DC}} \quad (2.3)$$

2.2.2 Power Added Efficiency (PAE)

What drain efficiency lacks in its' calculation is made up for by the PAE measurement. The PAE takes into account the input power to the device and effectively accounts for the device's gain in the calculation. This is the most accepted figure of merit when comparing single amplifiers. It also offers a theoretical measure of linearity for the device under test where an amplifier with linear gain will have the same PAE and drain efficiency. Typically, as can be seen by the calculation in Equation 2.4, the PAE will always be less than the drain efficiency unless the gain is very high. This is why drain efficiency is often used in datasheets to overvalue the device's efficiency, but PAE is a true comparison while accounting for the entire system's power [6, 8].

$$\eta_{power-aided} = P.A.E = \frac{P_{RFOUT} - P_{RFIN}}{P_{DC}} = \frac{P_{RFOUT} - P_{RFIN}}{V_{DC} \times I_{DC}} \quad (2.4)$$

2.2.3 Total Efficiency

The overall efficiency of a device under test gives the complete picture of the ratio of output power to all input power (DC and RF). This is reflected in Equation 2.5. When referring to the electrical efficiency of a device, this calculation offers the truest measure of total electrical output power divided by the total electrical input power, or power consumed. However, the PAE is still a preferred measure for RF power amplifiers as it is specific to the input drive of the amplifier [8].

$$\eta_{total} = \frac{P_{RFOUT}}{P_{DC} + P_{RFIN}} = \frac{P_{RFOUT}}{V_{DC} \times I_{DC} + P_{RFIN}} \tag{2.5}$$

2.2.4 Techniques for Efficiency Enhancements

With a direct correlation to thermal performance, designers require optimization to save on overall power consumption. High data rate RF signals, such as LTE, use complicated modulation schemes and impose tough requirements on the PA's linearity, power, and size due to the high-power application usage. Several techniques have been presented and utilized over the years to improve efficiency of RF amplifiers [7, 10, 11].

Amplifiers can operate in compression to theoretically achieve higher efficiency; however this is impractical as the amplifier will not run in compression all the time and does not take care of signals with high peak to average power ratio (PAPR). DC tracking is another technique where the PA voltage is adjusted in line with the modulation level; however this technique doesn't address instantaneous spikes [10]. Quite clearly, a technique is desired to account for signals with high PAPR.

Envelope Tracking (ET) is an approach to power amplifier design in which the applied voltage from a supply is continuously adjusted to ensure the amplifier is operating at peak efficiency for the power required. Essentially, the PA supply voltage tracks the RF envelope and adjusts the

supply voltage accordingly to produce optimum efficiency. This allows the PA to operate without compression and in a linear mode. This technique is highly useful for high data rate waveforms such as 4G LTE that incorporate an amplitude component in addition to phase elements and require a high peak to average ratio of RF power. Figure 7 and Figure 8 illustrate the margins in unnecessary dissipated power versus required envelope power [10].

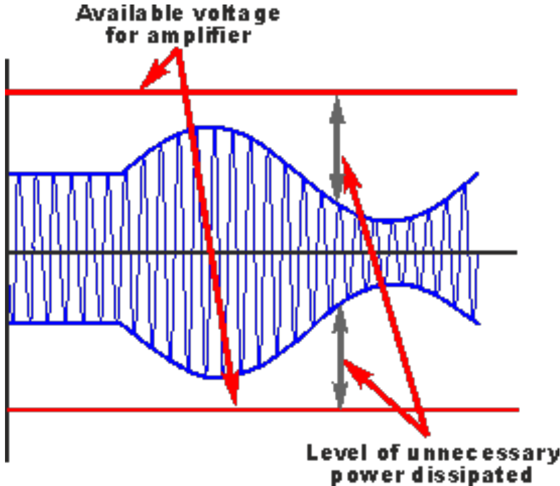

Figure 7: High level of power dissipation at full rail voltage [10]

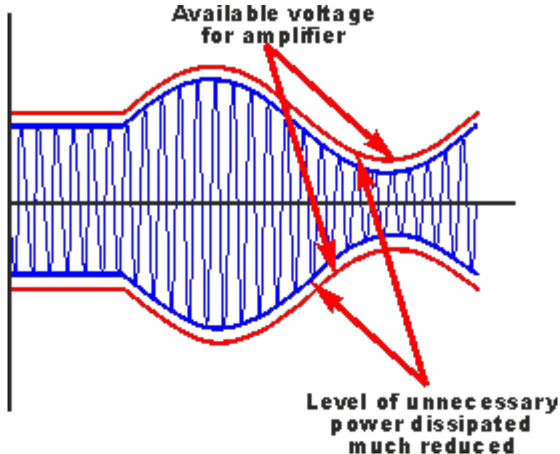

Figure 8: Envelope tracking allows for no unnecessary dissipation of power [10]

Typical RF PA design topology uses a single device, but many configurations and multi-stage designs use multiple devices that can help improve efficiency. Doherty amplifier is one such design. The configuration for a Doherty amplifier requires two elements: a main amplifier and a peaking amplifier, which are biased typically as Class-AB and Class-C, respectively. The peaking amplifier is biased off for the most part, only coming into operation for peak power levels. However, requires the use of hybrid couplers at the input as well as quarter wavelength transformer at the output to align the signals [10]. See Figure 9 for the Doherty amplifier block diagram, which shows the use of transmission lines of a quarter wavelength.

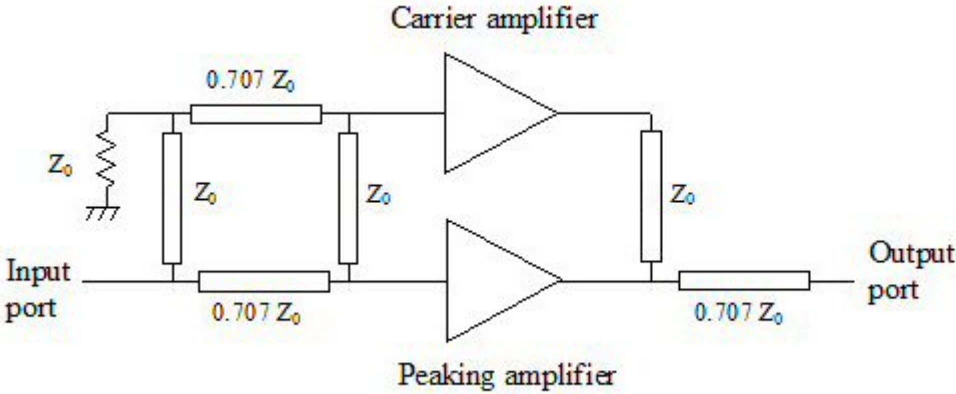

Figure 9: Doherty amplifier topology [10]

Designers can utilize design algorithms and topologies to improve efficiency and, therefore, thermal performance of an amplifier. However, there are still several factors that can be used to improve the thermal performance at the device level, and subsequently improve the overall performance of the PA before using a topology or design change.

2.3 Thermal Concepts

Thermal management is critical for linear RF operation as well as device reliability. Many PAs implement high back-off power from saturation point as a strategy for thermal management [12]. Performing at such high power result in more DC power dissipation and heat generation. As mentioned, package selection and sizing affect thermal performance. This section explains what factors in a package affect heat flow and overall thermal performance of a device.

2.3.1 Fourier's Law

The law of heat conduction states that the time rate of heat transfer through a material is proportional to the area of heat flow and the negative gradient in the temperature. Fourier's law can be represented in a differential and integral form. These forms are further correlated to Ohm's law to create an electrical analogue of Fourier's law. This law helps derive a relationship for an absolute thermal resistance across the length of a material [13]:

$$R_\theta = \frac{L}{A \times k} \tag{2.6}$$

Where R_θ is the absolute thermal resistance across the length of the material (K/W), L is the length of the material (m), k is the thermal conductivity of the material (W/(K·m)), and A is the cross-sectional area.

2.3.2 Thermal Resistance

Thermal resistance is one of the main heat properties that define thermal performance of a device. It is a measurement of temperature difference by which an object or material resist heat-flow (measured as heat per time unit). The units of measure are kelvins or degrees Celsius per watt (K/W or °C/W). Quite simply put, the thermal resistance can be expressed as

proportional to the temperature difference (ΔT) and given heat flow (Q), expressed in Equation 2.7 [13]. Manufacturers typically provide the thermal resistance based on the device's dimensions and material's thermal conductivity, as explained in the previous section.

$$\Delta T = Q \times R_{\theta} \tag{2.7}$$

The heat flow can be modeled as a direct analogy to an electrical circuit where the heat flow is represented as the current and temperatures as voltages. This relationship can be understood as a direct representation of Ohm's law. Figure **10** helps to show this relationship as a circuit, with 'Q' as the main power dissipated in the device (can be treated as a current source) [13].

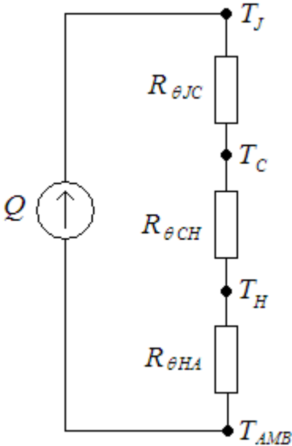

Figure 10: Equivalent thermal circuit for a device with heat sink from junction to ambient [13]

The figure shows a series circuit that is representing the several layers of a device such as a transistor. One of the most common parameters in a datasheet for devices is the absolute thermal resistance from junction to case, typically denoted as $R_{\theta JC}$. Maximum temperature, at which the device can function properly, along with the maximum allowable temperature of the semiconductor junction are also listed.

Designers need to consider how the heat from a device, such as a transistor, flows and escapes into the environment. This can be by convection into the air or conduction through the printed circuit board [3, 13, 14]. In the example in Figure **10**, the heat is shown to flow from the device's junction to the case, to a heat sink, and then released to the ambient environment. Each medium through which the heat flows can be represented with a thermal resistance between each stage of the flow and can be used to predict temperature drop across the flow. A simple ohm's law calculation as seen in Equation 2.8 can be used to predict the maximum power dissipation through as many required layers of heat conducting mediums [13]:

$$Q_{MAX} = \frac{T_{JMAX} - T_{AMB}}{R_{\theta JC} + \cdots + R_{\theta HA}} \tag{2.8}$$

where T_{JMAX} is the maximum junction temperature allowed, T_{AMB} is the maximum ambient temperature for proper operation, and $R_{\theta JC}$ is the junction to case resistance provided typically by the manufacturer. Equation 2.8 assumes a heat sink is present ($R_{\theta HA}$) for heat to escape into the surrounding air, but any heat conducting medium can be replaced as the last stage of thermal resistance before the heat escapes, and any number of layers can be added to properly represent the overall thermal resistance [13-17]. The junction temperature in an IC-device can be seen in Figure 11 and the number of layers for the heat, denoted as Q, to pass through from board to solder balls, and onto junction and case [1].

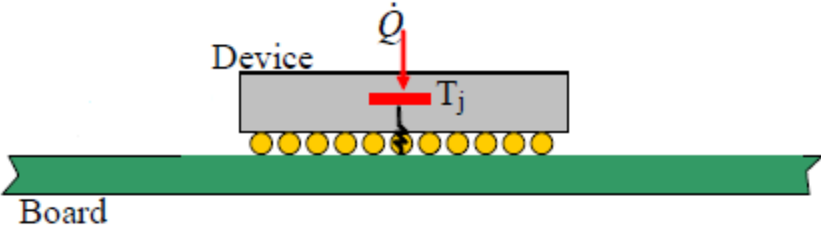

Figure 11: Junction temperature and heat dissipation in a ball grid array (BGA) package [1]

2.3.3 Thermal Conduction

Thermal conduction is important because the surface area is required to eventually dissipate the heat, which can only be spread out through proper conduction over the surface area. Technology is migrating towards smaller packages, but with smaller footprint comes the same power dissipation. This requires a better PCB conduction design for a given temperature rise [14].

Heat exchange occurs mainly via conduction or convection. All methods to determine thermal conductivity involve either the direct measurement of heat that passes through a sample or comparison of the amounts of heat flowing through a sample of known thermal conductivity. For static and steady state methods to determine thermal conductivity requires the knowledge of temperature, which can be measured experimentally with the use of thermocouples. These measurements are typically made after achieving thermal equilibrium. Heat flux can be measured with a heat flow meter or by determining the power dissipated. The thermal conductivity can then be deduced using Fourier's law [13]:

$$k = \frac{Q \times L}{\Delta T \times A} \tag{2.9}$$

where k is the thermal conductivity, Q is the heat flow for a sample area of A, L is the length of the conduction path, and ΔT is the temperature change through the sample [13]. Dynamic methods use thermal gradients observed as a function of time, but this measurement is more suited for thermal diffusivity as opposed to the measurement of conductivity.

Thermal conductivities for variety of materials are widely known today. In particular interest is the ability for heat to flow in surface mount packages. A power transistor, for example, will sit on top of a dielectric substrate, which sits on top of a metal ground. This metal sheet is the main electrical and thermal ground. From here out, the designer has an option to connect the

ground to a heat sink with large surface areas to absorb heat. Common material thermal conductivities are listed in Table 1 [15-17].

Table 1: List of thermal conductivities in common material substrates

Material	Thermal Conductivity (W/cm·K)
Copper	4.01
Silicon	1.49
Gallium Arsenide (GaAs)	0.55
Gallium Nitride (GaN)	2.30
Alumina	0.30
Silver	4.29
Gold	3.18
FR-4	0.0081

2.3.4 Heat Transfer in a FET Device

As the previous section explained, the thermal conduction properties of a material are affected by size and design as shown in Equation 2.9. In monolithic microwave integrated circuit (MMIC) design, the main cause for heat problems can be the amplifying FET or HEMT device. The reliability and power performance of a device depends critically on the operating channel temperature [19]. Figure 12 shows a multi cell GaN device FET device and the regions of interest for heat transfer, where the gate dimensions are L_G X W_G, gate-to-gate spacing is S, and substrate thickness is t_N. The main heat source can be assumed to be at the gate, denoted as G. It is under the gate where the main power will be dissipated, generating a constant heat flux. This will directly lead into GaN buffer layer and any other substrates that follow. Thus, the correlation for a GaN HEMT device to Figure **10** would be the summation of thermal resistances from the bottom substrate all the way to the surface. That is, $\theta_{TOTAL} = \theta_{GaN} + \theta_{Substrate}$ from the regions shown in Figure 12. Gallium Nitride technology will be discussed more in Chapter 3; as well, [18, 19] present an

effective closed form method to calculate thermal resistances in the corresponding regions of a GaN HEMT.

Figure 12: An example of a FET HEMT stackup and dimensions of interest [18, 19]

2.4 Conclusion

A designer needs to consider class of operation and account for several parameters when designing a PA for a particular application that is optimized for both RF and thermal performance. However, when it comes to both thermal and RF performance, biasing techniques are not enough [19]. The previous section exhibited the importance of material characteristics when designing for thermal, but it is equally important for high-frequency applications. The next chapter will introduce common materials in the market and introduce a chosen device model, which will serve as the basis of the design of a power amplifier in this thesis.

Chapter 3 - Semiconductor Technology and Device Model

3.1 Technology Selection

RF power devices are available in a wide variety of semiconductor technologies for use in high-efficiency amplifier designs. The devices must meet a strict set of performance requirement for output power and linearity. In addition, system manufacturers also require their own requirements for PAE, supply voltage, ruggedness, physical size, reliability, and cost [3, 9, 12]. All of these performance parameters are considered when selecting a technology for an RF power amplifier. It has already been explained in Chapter 2 how design configurations can affect the linearity, efficiency, and thermal characteristics of an RF PA.

Cellular infrastructure base stations are the largest market for high power RF semiconductor devices, specifically RF PAs. These devices can deliver hundreds of watts of power from just tens of volts of supply. Some of the most common semiconductor technologies used for these RF PA designs includes Si LDMOS FET, Si BJT, GaN HFET, GaAs MESFET, GaAs HEMT, and GaAs HBT. Si LDMOS FETs are considered to be the most widely used technology for base station applications due to their cost effectiveness, however this technology also struggles to meet required performance above 2 GHz, and requires a larger die size when compared to other technologies due to its' low power density [17].

In recent years, high power GaAs MESFETS and pHEMTs have shown to have superior performance compared to Si LDMOS devices at higher frequencies. Wide bandgap semiconductors such as SiC and GaN have also emerged for high power RF applications. These technologies offer improvements with their unique material properties, and can be seen listed in Table 2 [17]. High electric breakdown fields, drift velocity, and thermal conductivity (seen in Table 2) show distinct advantages for SiC and GaN for high power considerations. The breakdown fields themselves (being 5-6 times more than the competition) allow both SiC and GaN to be the preferred choice for high power RF applications over GaAs and Si [17, 21].

Table 2: Material Properties of Microwave Semiconductors [21]

Material	Mobility, μ (cm^2/V-sec)	Dielectric Constant, ε	Bandgap, Eg (eV)	Break down field, Eb (10^6V/cm)	Tmax (°C)
Si	1300	11.9	1.12	0.3	300
GaAs	5000	12.5	1.42	0.4	300
4H-SiC	260	10	3.2	3.5	600
GaN	1500	9	3.4	2	700

As Table 1 indicates, SiC has an advantage over GaN with its' higher thermal conductivity. However GaN offers more versatility in its' material system, such as having superior current handling capability compared to SiC devices [20, 21]. The next section will help explain the characteristics of a GaN device that make the technology so appealing in RF PA design.

3.1.1 Gallium Nitride Device

GaN based devices are defined as the state-of-the art technology for high power performance that have the potential to replace GaAs based transistors. The GaN material system has become the basis of advanced, microwave-power-device technology for numerous reasons, mostly attributed to its material properties. Table 2 lists semiconductor technologies and the key material properties that influence amplifier performance. GaN offers improvements in electron mobility that allows the technology to be suitable for high-speed devices that operate at higher frequencies. The high-breakdown field, which is ten times larger than that of GaAs, allows GaN devices to withstand large drain voltages [15, 17, 21]. This leads to high output impedance per watt of RF power, resulting in easier matching and lower loss matching circuits. The high sheet charge leads to large current densities, allowing the transistor area to be reduced. GaN also possesses a high-saturated drift velocity that leads to high saturation

current and power densities, another very important figure of merit for high power devices [17, 21]. The higher the power density, the smaller the die size and the easier the input and output circuit matches can be realized. The wide bandgap devices, SiC and GaN, have the highest power densities at 1.7 W/mm and 4.5W/mm, respectively [17]. Conventional GaAs FETs have power densities around 0.4W/mm. This property makes GaN further attractive in the high-power/frequency small-package size applications such as pico-cell base-stations.

GaN also offers a larger band-gap compared to Si and GaAs. This higher energy gap, which is more than double than the semiconductors listed in Table 2, determines the upper temperature limit of device operation, meaning GaN can withstand higher ambient and channel temperatures. In addition, this material system is capable of supporting hetero-structure device technologies with a high two-dimensional electron gas carrier density and mobility. Hence, GaN is commonly used in devices like the High-electron-mobility-transistor (HEMT), which incorporates a junction between two materials with different bandgaps. GaN can be grown on a number of different substrates, such as Si, SiC, and Sapphire. Typical AlGaN devices grown on GaN have shown to have superior current handling capabilities [17, 21]. However, since SiC has a higher thermal conductivity than GaN, it is often the most preferred choice as a substrate to fabricate a GaN device onto. This resulting hetero-structure offers high reliability and performance at large power levels, and proves to be quite efficient in design space and thermal dissipation. However, it is not the most practical choice as both SiC and GaN are very costly, and thus it is more common to grow a GaN device on a Si or sapphire substrate [17].

In summary, GaN offers a rugged and reliable technology capable of high-voltage and high-temperature operation, which opens up many commercial and industrial opportunities for the technology.

3.1.2 Trapping Effects in GaN

GaN FETS have demonstrated impressive microwave performance, with AlGaN/GaN HEMTs exhibiting 9.8 W/mm power densities at 8 GHz [17, 21]. Despite the state of the art microwave performance, it is widely acknowledged that significant development work still remains for wide bandgap technologies such as GaN and SiC. An area of particular concern is trapping effects seen on microwave power performance, which can be described as the trapping of electrons on various layers and surfaces of an active channel. This is a phenomena created when a device sees a high electric field between the gate and drain in the OFF state, temporarily trapping electrons [22-26]. When the device is ON, the detrapping of these electrons is not fast enough to allow for the proper flow of conduction for an AC signal [26]. As a result, the power delivery and performance of the devices is affected due to the drain current being restricted by the 'trapped' electrons. A variety of trapping effects have been observed, including transconductance frequency dispersion, current collapse at the drain, and gate and drain lag transients. Trapping effects in GaN FETs are covered in more detail in [22]. This phenomena isn't exclusive to GaN only, as it has been observed on both GaAs and SiC devices. As a maturing technology, trapping effects on GaN have yet to be fully understood, but techniques used with GaAs to limit these effects can also be applied to GaN, such as improvements in gate lag and passivation by annealing at high temperatures of the surface traps [26]. The results of trapping effects however beg the question of whether or not a proper thermal design of a device would help limit the effects of trapping effects or if there is any correlation between the two, since both can lead to similar performance deficiencies like current collapse.

Despite this phenomenon, GaN can still delivers exceptional performance for high-power MMIC thanks to its material properties. It has the ability to operate up to a theoretical maximum frequency of 155 GHz and at elevated temperatures of 700°C with SiC as the substrate [22, 24]. Design improvements can help limit the overall effects of surface and buffer trapping.

3.1.3 GaN Foundry Process

To help explore the makeup of a GaN device, this thesis will consider an example GaN HFET technology foundry process provided by the Canadian Photonics Fabrication Centre (CPFC) of the National Research Council (NRC), grown on insulating SiC wafers. A cross-section can be seen of the epitaxial layers and metal contacts in Figure 13.

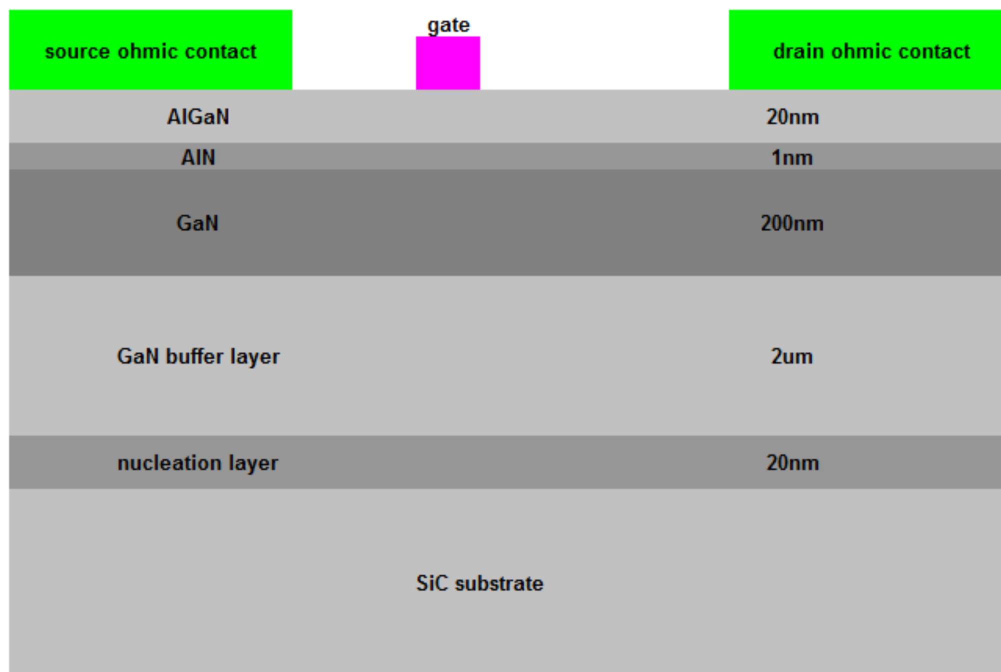

Figure 13: Schematic cross section of GaN HFET with epitaxial structures and metal contacts [27]

The foundry process is made up of nine mask layers, and is listed in detail in [27]. One interesting note is the use of 1um gold for the interconnect layers which, according to Table 1, has a fairly high thermal conductivity of 3.18 W/cm-K. Due to the high thermal conductivities of the substrates, there is little concern of self-heating effects within the interconnect layers. Current density of 6 mA/um of width is also listed for the interconnect layers [27]. Despite such careful thermal design considerations, the foundry does not provide a thermal model within its

simulation component and thus cannot consider the impact of temperature on device performance.

Therefore, for the purposes of this project, the NRC GaN foundry is not used in the design of a GaN HEMT power amplifier. Instead, an in-market design is considered using a CREE GaN HEMT and is explained in section 3.2.

3.1.4 Conclusion

Gallium Nitride is a growing wideband gap device technology that exhibits great advantages over existing material solutions such as GaAs and Si LDMOS, especially in the design for high power RF PA design. GaN addresses drawbacks of both GaAs and Si LDMOS, being able to deliver higher power and operate at higher frequencies, respectively. This is due to the material properties such as the high breakdown voltage and high power densities, as well as higher temperature thresholds. Due to the superior tolerance of temperature and higher frequency performance, GaN is a more suitable technology than SiC for high-powered RF PAs used in base station operation [17, 20, 21].

3.2 Transistor Model Evaluation of In-market GaN PA

To conduct a study on thermal performance of an RF PA, it was important to choose a foundry and design capable of handling high power delivery in order to test the limits of thermal stress in a small form factor. A device needs to be chosen to meet performance requirements and reliability goals. Considering a pico-cell base-station, requirements include high-gain and high frequency operation for effective power delivery. The device chosen must meet these criteria from package level, and then be optimized with effective component selection and line matching to meet the requirements of signal integrity. The design has to undergo several stages, beginning with schematics to layout for effective simulation data before it can be fabricated. For the purposes of this thesis, an existing package has been chosen to perform thermal analysis on.

One of the market leaders in the advancement and evolution of the GaN technology is CREE semiconductor solutions. They specialize in GaN infused products such as LEDs and RF PAs. Their packaged PAs for market can be used for very high power applications, such as radar and base stations [21]. Due to CREE's reliability and performance with large signal applications, this thesis will be utilizing their simulation model for CREE's CGH25120F model PA. Furthermore, CREE's simulation model accounts for thermal considerations, and was a big factor in choosing this PA for analysis in Agilent ADS. The CGH25120F package size measures 9.91 mm x 15.37 mm, however the transistor size is left unspecified [28]. The simulations will be performed using Agilent ADS and Agilent Momentum for layout. A schematic will be constructed to recreate CREE's evaluation board of a single stage class-AB PA using the CGH25120F transistor, followed by a layout design that is recreated to mimic the evaluation board performance.

3.2.1 Requirements

In order to recreate the performance of an in-market HEMT, the RF performance requirements needed to be defined. The requirements are derived directly from the CGH25120F datasheet and fit the scope of this thesis case study on high-powered applications for an LTE pico-cell base-station. The device will be operating at a frequency of 2.5 GHz and will effectively deliver a gain of 13.1 dB at room temperature of 25°C. The device shall deliver up to 20W of power and maintain a minimum efficiency of 30% [28].

3.2.2 DC Analysis

To characterize the performance of a market GaN HEMT device, the first step is to analyze the DC performance of the RF PA that is to be designed. As discussed in earlier topics, one of the key factors that determine an RF PA's performance and class is the biasing point. Since the goal here is to recreate the CGH25120F evaluation board, it is important to recognize the DC operating points and quiescent current specified in the device's datasheet. According to the datasheet, the operating point for the measured RF performance parameters such as gain and PAE are done at a drain voltage of 28V and a quiescent drain current of 0.5A [28]. Since the evaluation board is designed for a Class-AB bias, we can assume our bias point is required to be at or near 0.5A. The transfer characteristics for VDS=28V are shown in Figure 14, which is a plot of the gate voltages and subsequent drain current and operation. Three distinct regions should be noted in Figure 14: cutoff, linear, and saturation. It can be seen that the device is in cut-off mode when the voltage is less than -3.5V, corresponding to no DC current. The device enters linear mode of operation near -3.25V and continues until it saturates at a current of approximately 23A at a gate voltage of 0.8V. The appropriate quiescent current for our class of operation is approximately 500 mA, and thus it can be seen using the plot in Figure 14 that this current is achieved at a gate voltage of -3V.

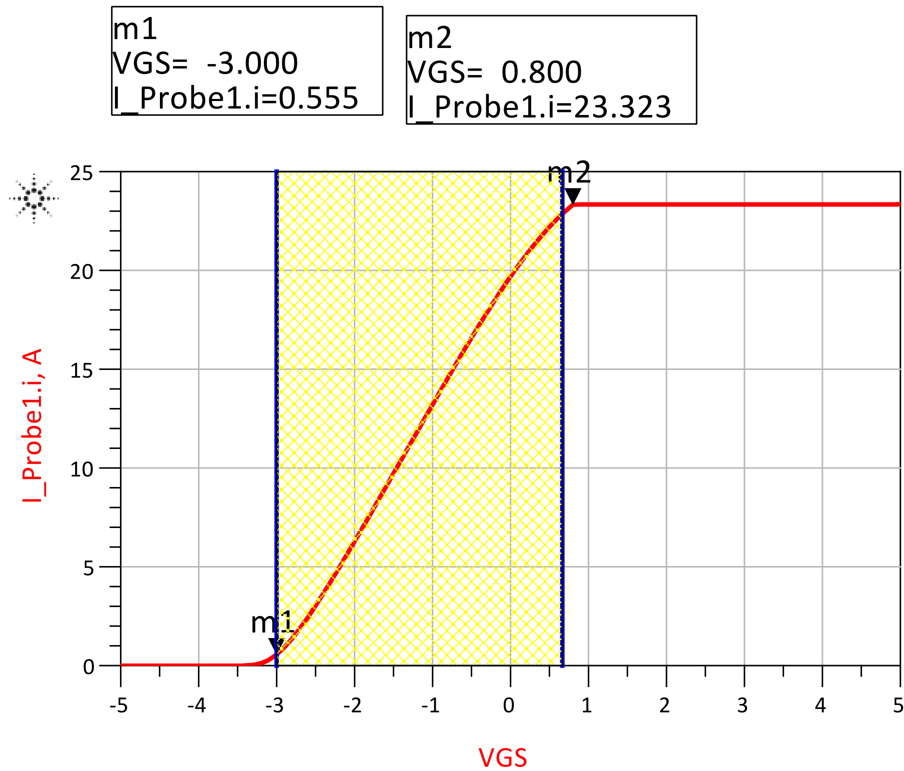

Figure 14: Transfer Characteristics of CGH25120F at DC

The full DC I-V curves can be seen in Figure 15 along with the biasing point. For operation of a Class-AB amplifier, the bias point is chosen to be typically between 10%-15% of the max drain current, which complies with the operating points of the gate-to-source voltages listed in the datasheet. The plot clearly shows the vast range of operating currents as a function of drain and gate voltages. Since the evaluation board has no heat sink on top of the case, it can be seen according to Figure **10** that the case temperature matches the ambient temperature. Hence, to match the evaluation board, the DC analysis was performed at a case or room temperature of 25°C.

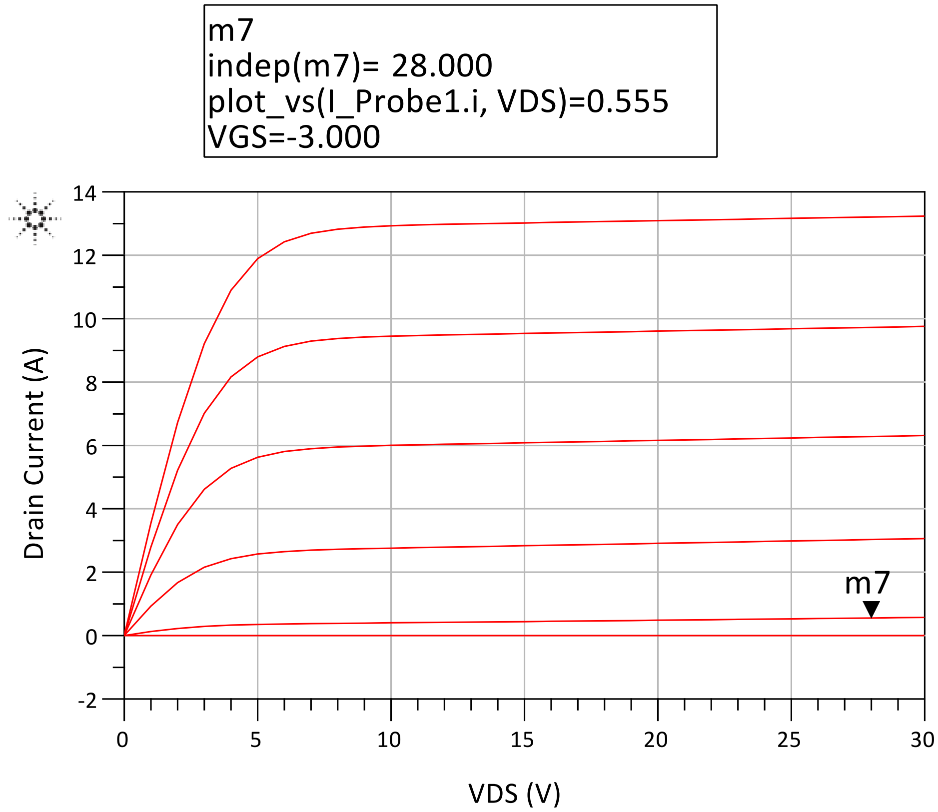

Figure 15: Drain Bias as a function of drain voltage

Due to the nature of this thesis, it was also prudent to perform DC analysis over temperature settings. The case operating temperatures listed for the CGH25120F HEMT are between -40°C and 150°C. The I-V curves under operating bias conditions for Class-AB operation (VGS = -3V) can be seen in Figure 16. Under DC conditions, we can see the trend of reduced drain current as temperature rises. When biased at a drain voltage of 28V, the direct correlation between drain current and case temperature can be seen as an indicator of device performance degradation.

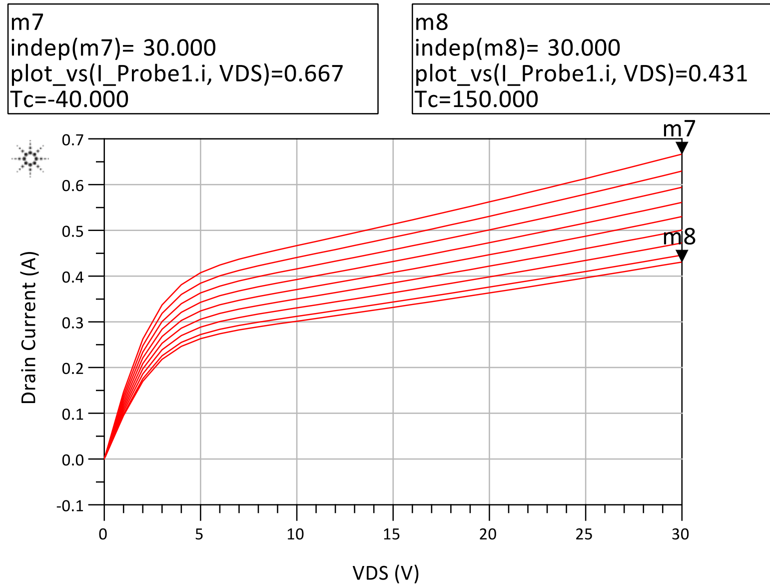

Figure 16: Drain current across case operating temperature and drain voltages

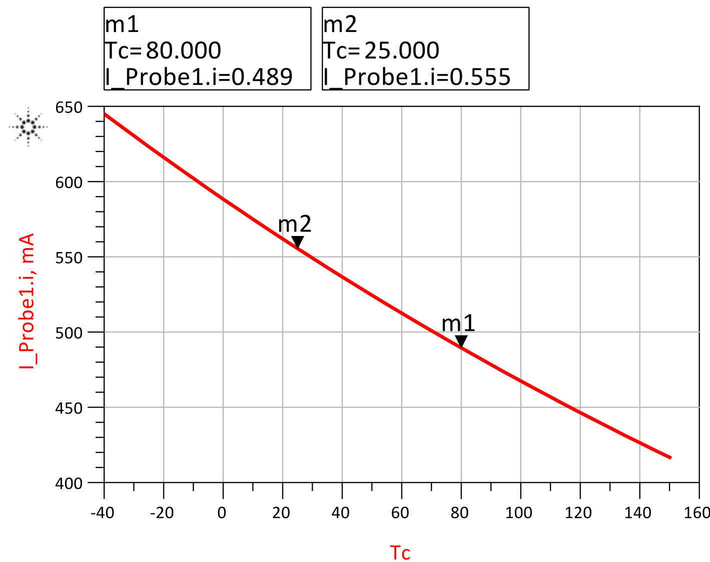

Figure 17: Drain current as a function of case temperature under bias conditions

The CGH25120F model shows a reduced drain current capability as ambient temperature rises, which would indicate less power delivery at higher temperatures. The linear and saturation regions again experience a dip in current. The behaviour in current change is similar across all temperature variations when the gate voltage is swept, however the characteristic regions remain the same; saturation point seems to still be near a gate voltage of 0.8V, and the current enters a linear region near -3.25V of bias at the gate, similar to Figure 14. Despite these

similarities, it can be seen that the model isn't linear for current degradation across temperature.

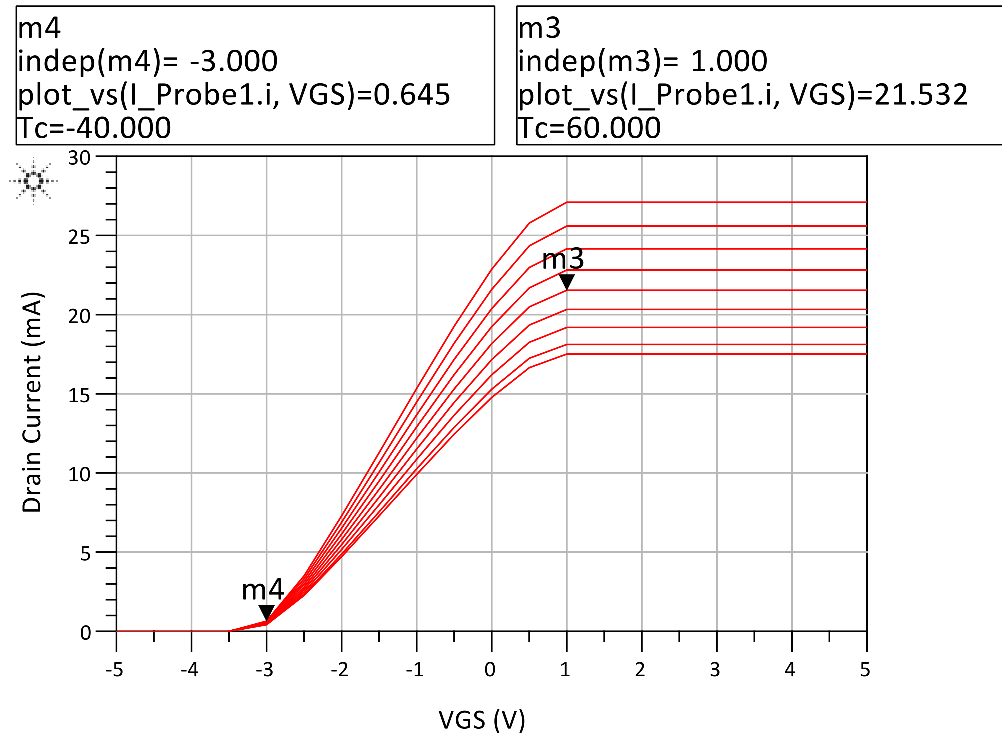

Figure 18: Transfer characteristics over operating case temperatures

3.2.3 Evaluation Board Reconstruction and Impedance matching

The next step in re-creating CREE's design was to begin constructing the schematics and matching networks as designed on the CGH25120F evaluation board. The goal was to match the routing and the source and load impedances to create a direct correlation between the evaluation board and simulations in ADS and ADS momentum. Furthermore, load-pull simulations were performed on the GaN HEMT to assess optimum performance metrics for impedance matching; contours will be presented for impedances that produce maximum PAE and power delivery for the CREE HEMT.

The substrate properties used in the simulations match the specifications of Rogers 4350B, which is the material used by CREE to build the evaluation board on [28]. These properties can be seen in Table 3.

Table 3: Substrate Properties of Rogers4350B

Height	20 mil
Loss Tangent	0.004
Dielectric Constant, ε_R	3.66
Conductor Thickness	1.4 mil
Dielectric Loss Tangent	0.004

The ADS schematic includes the input and output-matching networks of CGH25120F evaluation board, including the drain and gate bias circuitry. A momentum layout is also created to show the true effects of metallic trace routing, as well as the input and output matching networks.

The schematics and layout for the evaluation board presented in the CGH25120F datasheet can be seen in Figure 19 and Figure 20. The re-construction of this schematic in ADS is performed in two parts for proper impedance matching, beginning with the input and then the output. As opposed to simulating ideal connections, transmission line models of the Rogers 4350B substrate were utilized for interconnections between the signals to create a more realistic model that can be compared to the evaluation board measurements for impedance. Furthermore, this helps create a very simple transition into layout of the design for momentum simulations. The ADS schematics can be seen in Figure 21.

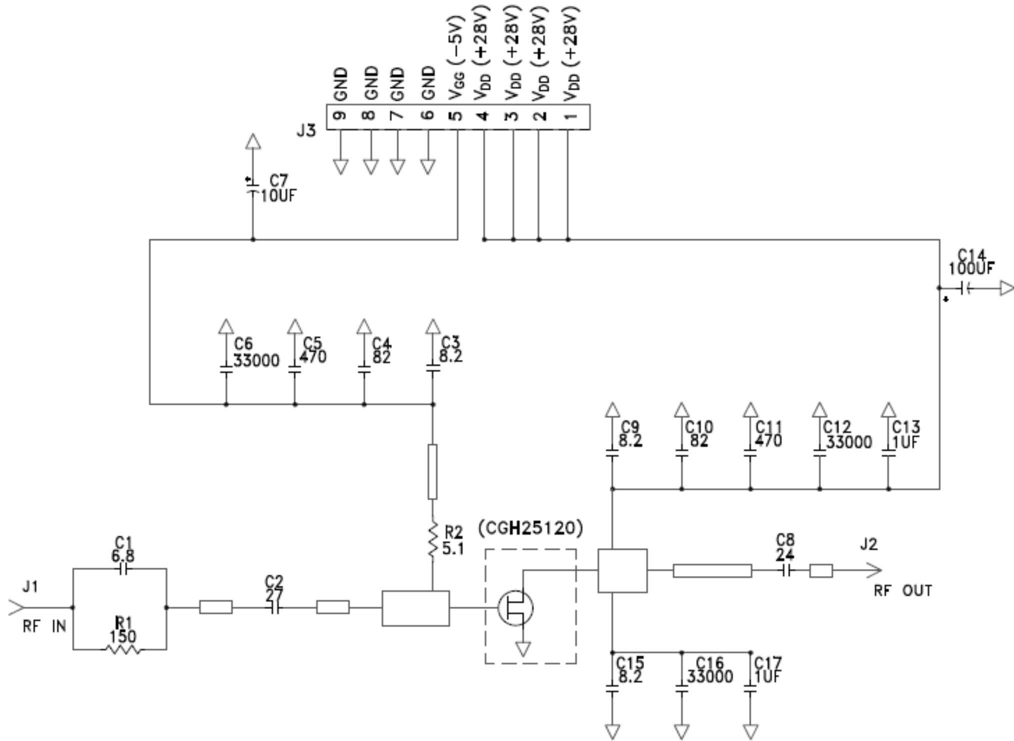

Figure 19: CREE's schematic block for the CGH25120F evaluation board [28]

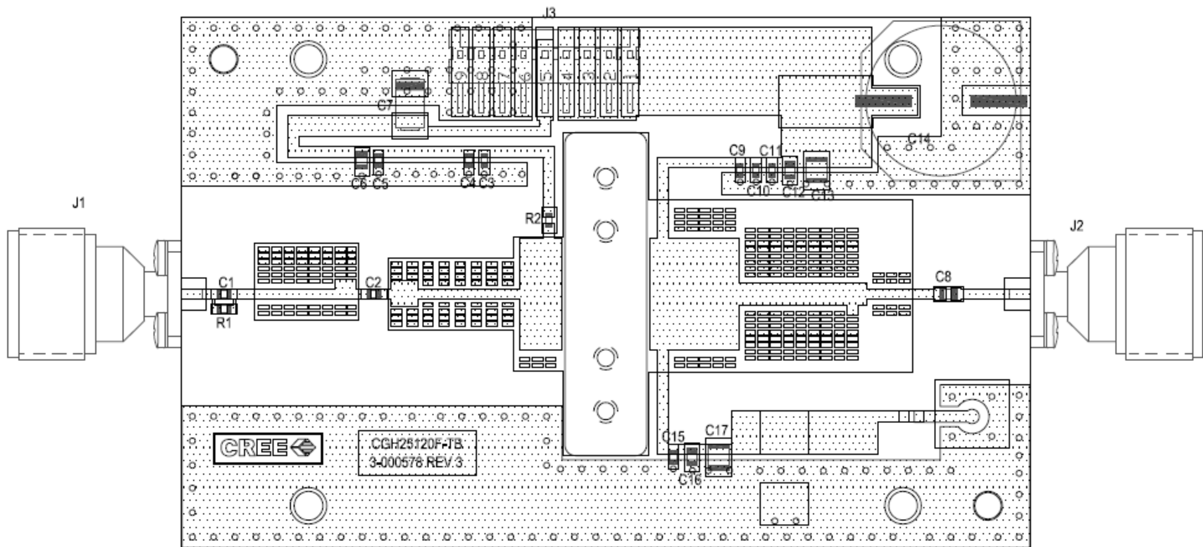

Figure 20: Layout and placement of CGH25120F evaluation board [28]

P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(Pavs)
Freq=2.5 GHz

P_Probe
P_Probe1

MLIN
TL1
Subst="MSub1"
W=42 mil
L=145 mil

MTEE_ADS
Tee1
Subst="MSub1"
W1=42 mil
W2=42 mil
W3=10 mil

MLIN
TL3
Subst="MSub1"
W=42.5 mil
L=40 mil

MLIN
TL2
Subst="MSub1"
W=10 mil
L=30 mil

HarmonicBalance
HB1
Freq[1]=2.5 GHz
Order[1]=1

HARMONIC BALANCE

MLIN
TL4
Subst="MSub1"
W=42 mil
L=32.5 mil

S_Param
SP1
Start=0.001 GHz
Stop=3 GHz
Step=0.01 GHz

S-PARAMETERS

R
R1
R=150 Ohm

SRLC
SRLC1
R=0.13 Ohm
L=0.16 nH
C=6.8 pF

MSub

MSUB
MSub1
H=20 mil
Er=3.66
Mur=1
Cond=1.0E+50
Hu=3.9e+034 mil
T=0 mil
TanD=0.004
Rough=0 mil
Bbase=
Dpeaks=

MLIN
TL5
Subst="MSub1"
W=42 mil
L=32.5 mil

MTEE_ADS
Tee2
Subst="MSub1"
W1=42 mil
W2=42 mil
W3=10 mil

MLIN
TL6
Subst="MSub1"
W=42.5 mil
L=40 mil

MLIN
TL7
Subst="MSub1"
W=10 mil
L=30 mil

VAR
VAR1
Pavs=39
tempC=-20

MCORN
Corn2
Subst="MSub1"
W=50 mil

MLIN
TL28
Subst="MSub1"
W=50 mil
L=47 mil

MCORN
Corn3
Subst="MSub1"
W=50 mil

MLIN
TL8
Subst="MSub1"
W=42 mil
L=462 mil

MLIN
TL27
Subst="MSub1"
W=50 mil
L=262 mil

MLIN
TL29
Subst="MSub1"
W=50 mil
L=441 mil

MTEE_ADS
Tee3
Subst="MSub1"
W1=42 mil
W2=42 mil
W3=100 mil

MLOC
TL9
Subst="MSub1"
W=100 mil
L=50 mil

MTEE_ADS
Tee8
Subst="MSub1"
W1=50 mil
W2=50 mil
W3=50.0 mil

MTEE_ADS
Tee9
Subst="MSub1"
W1=50 mil
W2=50 mil
W3=167 mil

MLIN
TL30
Subst="MSub1"
W=167 mil
L=110 mil

C
C3
C=10 uF

MLIN
TL10
Subst="MSub1"
W=42 mil
L=70 mil

C
C2
C=33 nF

MLIN
TL26
Subst="MSub1"
W=50 mil
L=10 mil

MLIN
TL25
Subst="MSub1"
W=50 mil
L=18 mil

SRLC
SRLC2
R=0.135 Ohm
L=0.14 nH
C=27 pF

MLIN
TL31
Subst="MSub1"
W=50 mil
L=10 mil

MTEE_ADS
Tee7
Subst="MSub1"
W1=50 mil
W2=50 mil
W3=50.0 mil

MLIN
TL11
Subst="MSub1"
W=42.5 mil
L=69 mil

C
C1
C=470 pF

MLIN
TL24
Subst="MSub1"
W=50 mil
L=10 mil

V_DC
SRC1
Vdc=-3.5 V [-t]

I_Probe
I_Probe1

MLIN
TL23
Subst="MSub1"
W=50 mil
L=37.5 mil

MCROSO
Cros1
Subst="MSub1"
W1=42.5 mil
W2=125 mil
W3=42.5 mil
W4=125 mil

MLOC
TL13
Subst="MSub1"
W=125 mil
L=40 mil

MLOC
TL12
Subst="MSub1"
W=125 mil
L=39.2 mil

MTEE_ADS
Tee6
Subst="MSub1"
W1=50 mil
W2=50 mil
W3=50.0 mil

SRLC
SRLC4
R=0.119 Ohm
L=0.12 nH
C=82 pF

MLIN
TL22
Subst="MSub1"
W=50 mil
L=10 mil

MLIN
TL14
Subst="MSub1"
W=42.5 mil
L=480 mil

MLIN
TL21
Subst="MSub1"
W=50 mil
L=24 mil

MSTEP
Step1
Subst="MSub1"
W1=42.5 mil
W2=530 mil

MTEE_ADS
Tee5
Subst="MSub1"
W1=50 mil
W2=50 mil
W3=50.0 mil

SRLC
SRLC3
R=0.127 Ohm
L=0.15 nH
C=8.2 pF

MLIN
TL20
Subst="MSub1"
W=50 mil
L=10 mil

MLIN
TL15
Subst="MSub1"
W=530 mil
L=113 mil

MLIN
TL19
Subst="MSub1"
W=50 mil
L=255 mil

MTEE_ADS
Tee4
Subst="MSub1"
W1=530 mil
W2=530 mil
W3=50 mil

MLIN
TL17
Subst="MSub1"
W=50 mil
L=70 mil

R
R2
R=5.1 Ohm

MLIN
TL18
Subst="MSub1"
W=50 mil
L=282 mil

MCORN
Corn1
Subst="MSub1"
W=50 mil

MLIN
TL16
Subst="MSub1"
W=530 mil
L=37 mil

CGH25120F_r6_CGH25_r6
X1
tcase=tempC
crth=1.5

Figure 21: Schematics split into input and output sections matching the datasheet parts and routing

With these transmission line models, an accurate and consistent layout can be constructed for the metal traces seen at the surface layer for the evaluation board. Once again, the layout was performed in two distinct parts: input and output. The Rogers 4350B duroid substrate stack-up can be seen in Figure 22.

As referenced in Table 3, the dielectric substrate thickness is at 20 mil. A copper conductor of 0.7 mil thickness is used for the metal tracks, and a via conductor is added to ground signals to a perfect conductor sheet placed at the bottom layer. No vias are utilized in the layout of the copper traces.

The metal tracks were etched to match the routing of the evaluation board in Figure 20 to mimic the design as close as possible. No passive components were placed in the layout as only the metallic tracks were simulated in momentum, instead replaced with ports for the placement of such components. The HEMT model itself does not provide a layout component. Finally, the layout was simulated in momentum and then used in co-simulations with the input signal and passive components for a final accurate evaluation of the impedance, RF power delivery, and thermal performance. The layout of the metal tracks can be seen in Figure 24 and Figure 24 for the input and output sections. The correlation in shape and size can be seen when compared to Figure 20.

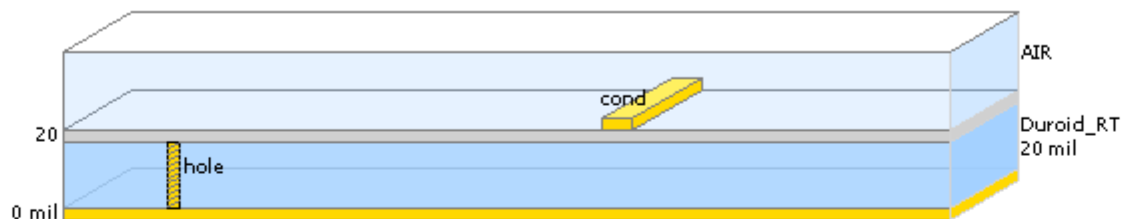

Figure 22: Substrate stack-up for the Rogers 4350B duroid material used in the evaluation board

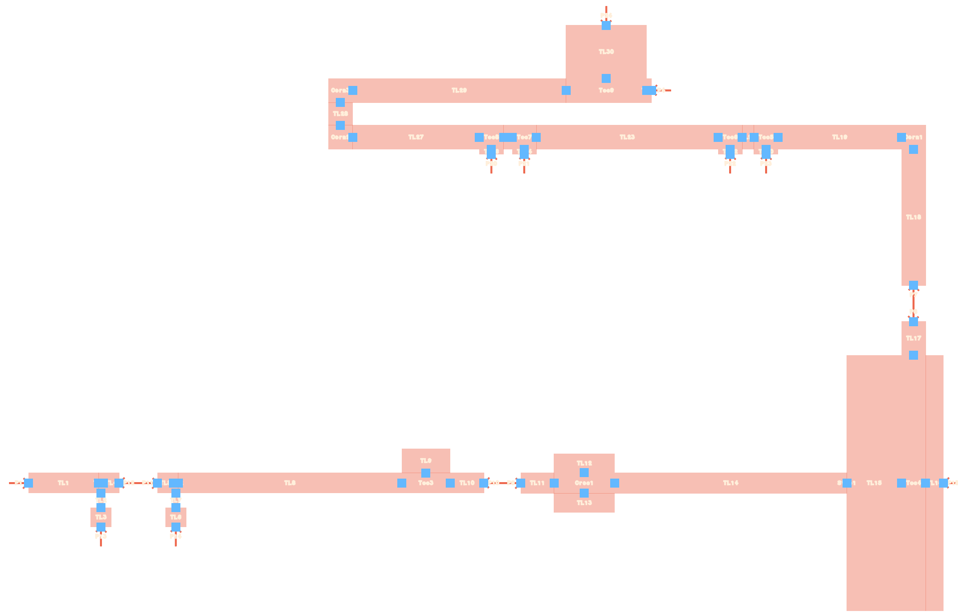

Figure 23: Layout of copper routing on the input side of CGH25120F evaluation board

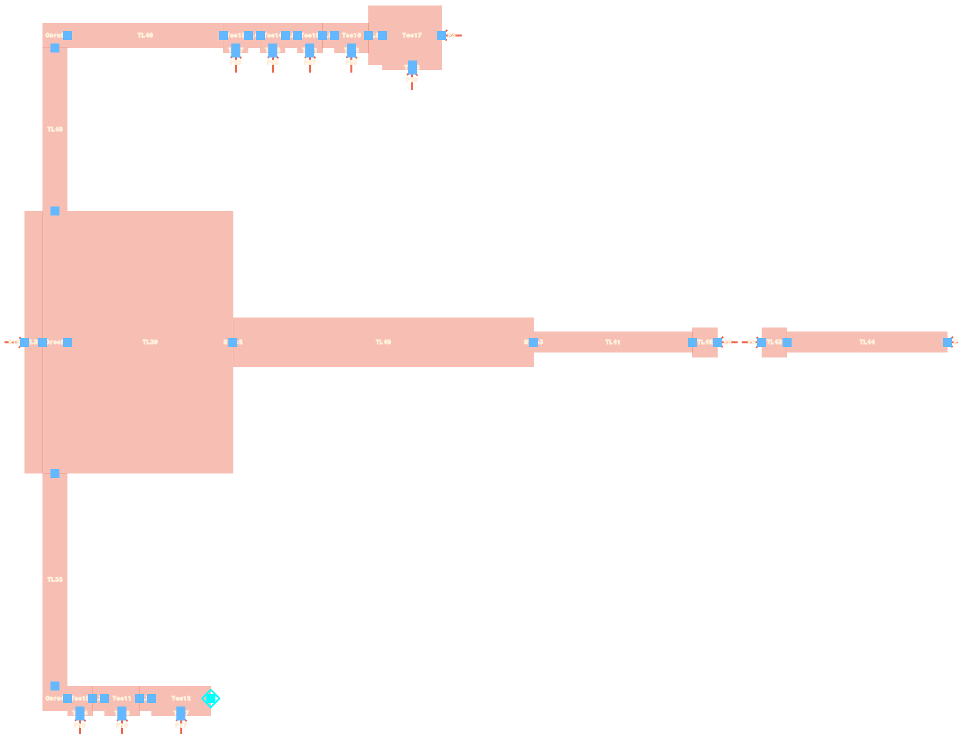

Figure 24: Layout of copper routing on the input side of CGH25120F evaluation board

Simulations for both the impedance seen by the gate (Z-source) and the drain (Z-load) were performed in ADS and momentum. The results are compared to the datasheet measurements, which were extracted from the evaluation circuit and not pulled from source and load-pull data from the transistor [28].

Table 4: Source and load impedance comparison between measurement and simulation [28]

Impedance Measurement	Datasheet Measurement @ 2.5 GHz	Agilent ADS Pre-layout Simulation @ 2.5 GHz	Agilent Momentum Post-Layout Simulation @ 2.5 GHz
Z-source	5.37 – j11.08	4.94 – j12.34	5.11 – j12.58
Z-load	4.31 – j1.33	4.95 – j1.47	4.11 – j2.97

As can be seen in Table 4, the simulated impedance seen at both the drain and gate are very close to the measured values listed in the CREE datasheet. Though both simulations offer fairly accurate representations of the evaluation board, the momentum simulation is preferred as it presents a more realistic model of the evaluation board copper as opposed to the ideal conditions in ADS. The overall resistive path in momentum is matched more accurately to the board level measurement, which will directly affect the power delivery and heat dissipation. Some of the differences can be accounted for differences in copper weight and dimensions, and the effects of parasitic losses on the lumped component models used. Most importantly, it can be concluded that the momentum simulation and layout design offers an accurate representation for simulation of the CGH25120F evaluation board. Therefore, for further assessment of the CGH25120F large signal model, the evaluation will be carried as a co-simulation with momentum structures and passive components.

3.2.4 Load-pull Analysis

Before performing co-simulation of the full amplifier circuit, a single tone load-pull analysis was performed to predict the most optimized conditions of operation for the large signal model. The analysis was performed to predict the optimum impedance of the device at different case temperatures, and the corresponding maximum DC power, power delivery, and input impedance was recorded. Load-pull simulations are performed on Agilent ADS and show the performance of the large signal model under different load conditions using harmonic balance analysis. The available power is optimized to provide a maximum constant power delivery, utilizing the biasing voltages chosen in our DC analysis (VDS = 28V, VGS = -3V) to achieve a quiescent drain current of ~ 500 mA (Class-AB operation). The load-pull simulations are performed at the chosen frequency of operation, 2.5GHz, to maintain consistency. Limits for power delivery were identified in the simulation to achieve a gain of 12-13 dB as per the CREE datasheet [28]. The fundamental source impedance was kept the same as the momentum simulation result of 5.11 – j12.58.

As this thesis is more concerned with thermal analysis, the maximum achievable PAE is recorded, along with the conditions that achieve this performance. The PAE contours are presented in Figure 25 for a temperature of 25°C, i.e. normal operating condition. The center of the smith chart is adjusted to show the load marking for maximum PAE. Figure 26 shows the I-V curves and lists the optimum load impedance, along with the gain and delivered power for the same simulation. When sweeping over to the load impedance listed in the datasheet, the achievable PAE is listed as 37%, which is close to the 32% specified by CREE [28]. This would indicate a compromise in design for more linearity, as has been explored in Chapter 2. When compared to the momentum simulation results, the achievable PAE is about 34%, which once again is close to the specifications. The maximum achievable PAE is listed as results for a temperature sweep are recorded in Table 5.

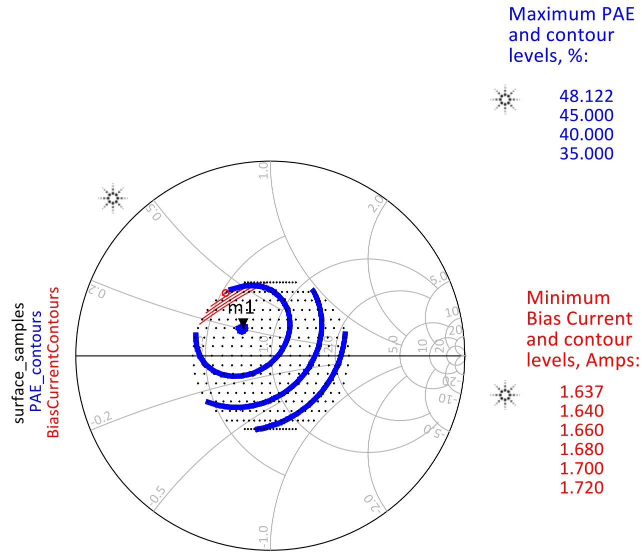

Figure 25: PAE and Bias Current load-pull simulation contours across different loads

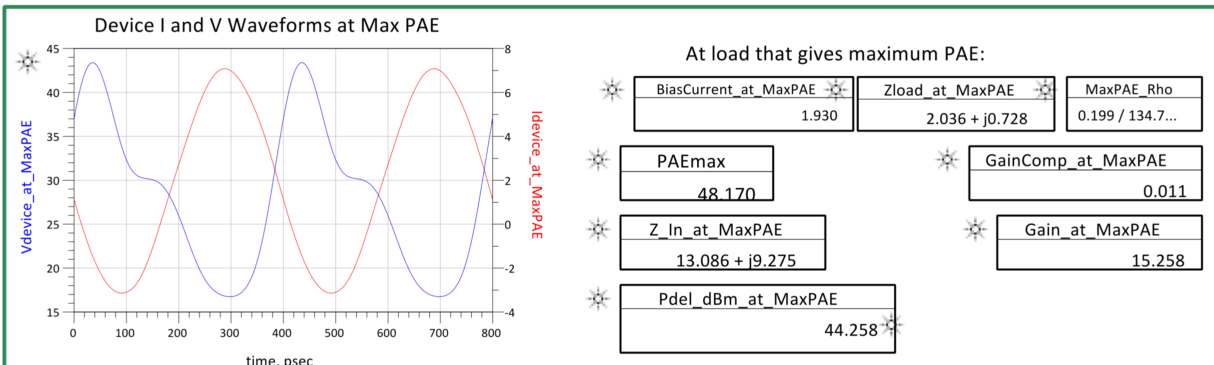

Figure 26: Device performance at optimal load for PAE

Table 5: Load-pull device performance across different temperatures

Temperature	Optimal impedance (Z_{OPT})	Input impedance (Z_{IN})	Maximum PAE at load (%)	Gain at load (dB)	Power Delivered (dBm)	DC Power (W)	Bias Current (A)
-40°C	2.055 + j0.527	12.826 + j9.338	48.201	15.707	44.707	60.03	2.144
0°C	2.055 + j0.527	13.179 + j9.531	48.176	15.505	44.505	57.28	2.046
25°C	2.036 + j0.728	13.086 + j9.275	48.170	15.258	44.258	54.04	1.930
85°C	1.841 + j0.872	13.537 + j8.967	48.076	14.750	43.750	48.05	1.716
150°C	1.687 + j1.008	13.962 + j8.760	47.904	14.217	43.217	42.53	1.519

As temperature varies, it is no surprise the bias current decreases, based on the previously performed DC analysis. Along with this, the gain, power delivery, and efficiency all decrease when targeting the best possible PAE. However, the optimal impedance is also changing with the variable temperature. This raises the question as to whether it is really the surrounding temperature affecting performance or if it is due to potential mismatches in impedance seen by varying temperature. If the optimal impedance is fixed at Z_{OPT} = 2.036 + j0.728, corresponding to a normal case temperature of 25°C from the table above, we still see performance degradation as temperature is increased. These results are listed across the same operating temperatures in Table 6. It offers further proof that the reduction in power delivery and gain has more to do with the effects from the operating temperature than impedance mismatch. Since the load-pull is performed under the same input power and biasing conditions, the case temperature is the lone variable in these simulations that affect the self-heating behaviour of the device.

Table 6: Load-pull data with fixed optimal impedance further depicting the temperature effects independent of impedance

Z_{OPT} = 2.036 + j0.728			
Temperature	**Maximum PAE at load (%)**	**Gain at load (dB)**	**Power Delivered (dBm)**
-40°C	48.003	15.573	44.573
0°C	48.164	15.384	44.384
25°C	48.170	15.258	44.258
85°C	47.872	14.926	43.926
150°C	47.068	14.518	43.518

With this analysis, it can be concluded that the CGH25120F HEMT can be optimally designed for a much better theoretical PAE and power delivery if desired. The next section will examine the co-simulation of the RF PA design with the momentum layout components in place and the results for performance versus temperature will be presented.

Chapter 4 - RF PA Performance

With the transistor model evaluation completed, the model can now be evaluated for its' RF performance and characterized over temperature. The power amplifier circuit is constructed as per the reference [28] and uses the momentum layout components from Figure 24 for both the input matching and output matching circuits as part of a co-simulation, which is a simulation incorporating layout characteristics from momentum at schematic level. The circuit can be seen below in Figure 27. The simulations are run with the input power being swept from 24 dBm to 39 dBm at an operating frequency of 2.5 GHz.

4.1 CGH25120F performance across power levels

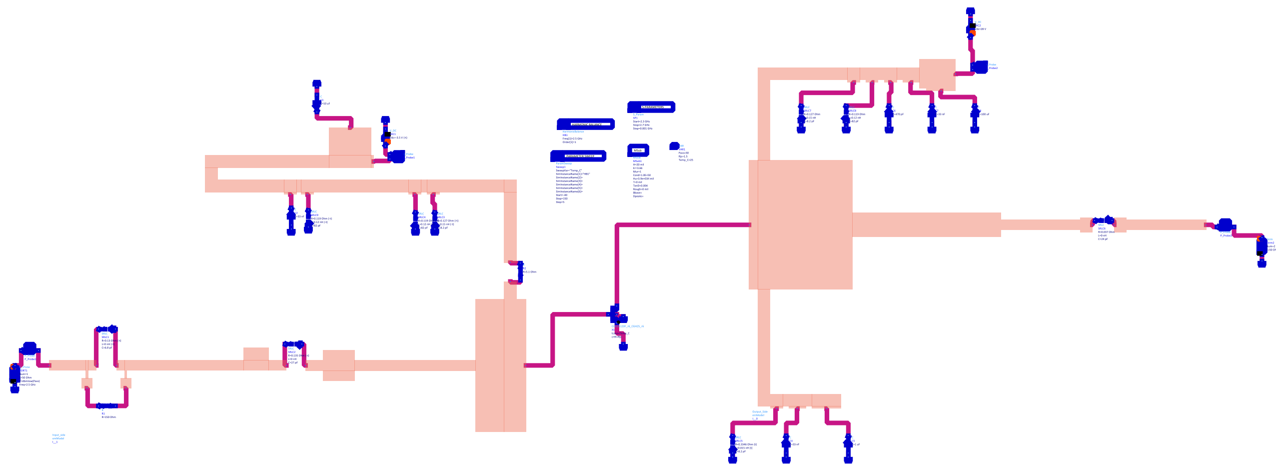

Figure 27: Co-simulation circuit for the CGH25120F RF PA model

The CREE datasheet has specifications based on an output power of 43 dBm [28]. This operating point is found to be approximately an input power of 29 dBm, based on the simulation results in Figure 28. The gain can also be seen in Figure 29 to be over 14.45 dB, which would indicate a better performance than the typical 13.1 dB gain that is specified at a frequency of 2.5 GHz. However, the linear gain of the amplifier for the bias conditions is actually measured near 15.5 dB with 32% drain efficiency. A summary of these results can be seen in Table 7. The slight discrepancies in measurement and simulated data can be attributed

to possible differences in measurement points. As a realistic representation of the amplifier performance, the simulation uses probe points before and after the momentum traces for a true measure of input and output power. For the scope of this thesis, this discrepancy will be ignored as the gain and efficiency is measured very closely for thermal analysis.

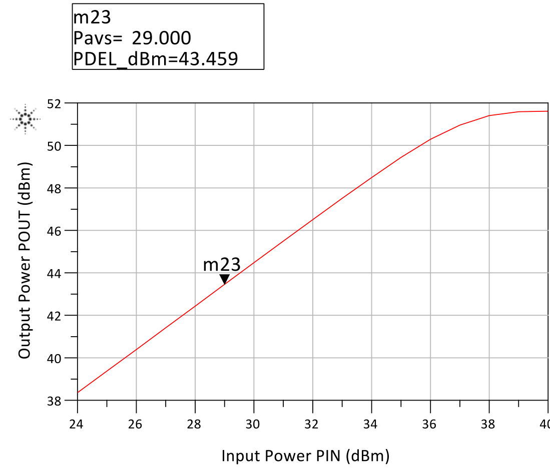

Figure 28: Power delivery performance as function of input power

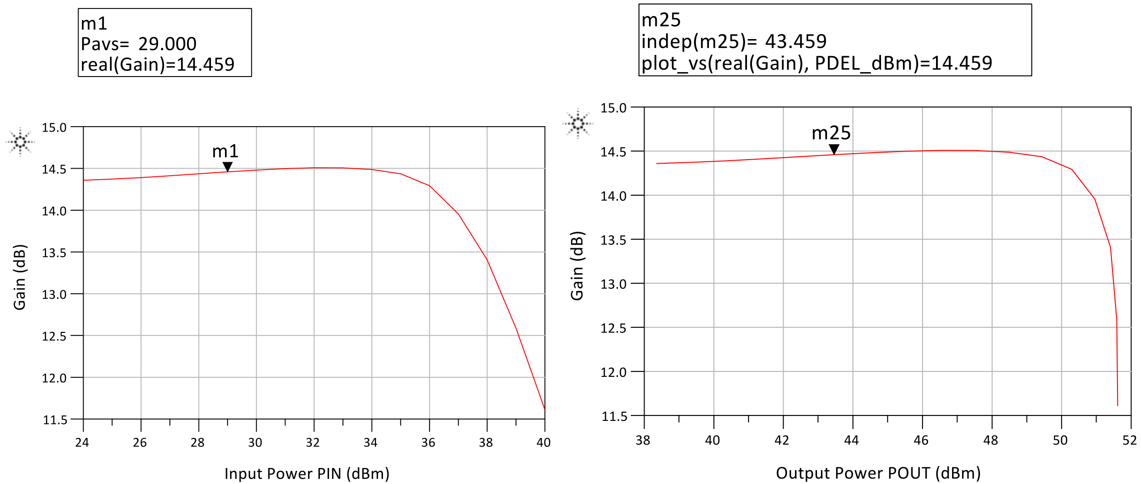

Figure 29: Gain performance as a function of input and output power

4.1.1 Efficiency performance

The PAE, seen in Figure 30, is calculated using equation 2.4 from chapter 2. Since the datasheet specifies 32% drain efficiency at these operating conditions, it further proves the manufacturer's preference to list the higher drain efficiency as opposed to the PAE, which subsequently measures at 31.96% according to the simulation. The drain efficiency in the simulation measures at 32.99%, which is very close to CREE specifications.

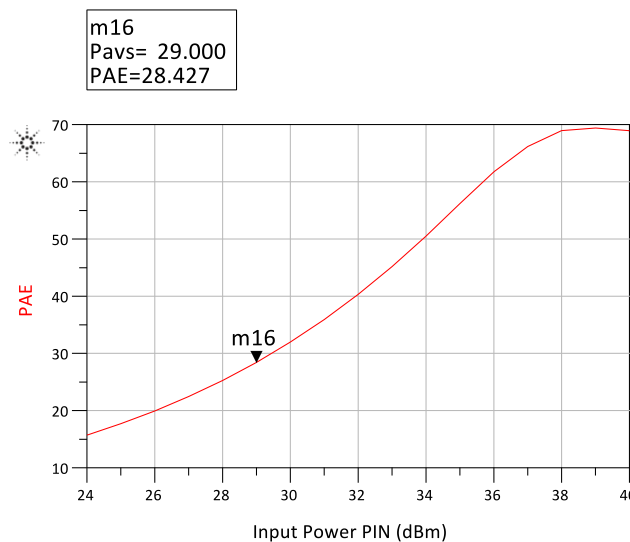

Figure 30: Power added efficiency of the CGH25120F HEMT model

This efficiency would indicate a calculated 54 watts of power being dissipated at this operating point. At 54 watts, the board needs to be designed to be able to dissipate this safely into the air instead of trapping it within the components and catastrophically damaging the components and PCB, not to mention the degradation in performance. Once again, this simulation is very accurate as the dissipated power in the datasheet is 56W. Therefore, the co-simulation represents a very accurate measurement representation of the evaluation board and further validates the CGH25120F model for ADS. For the purposes of this thesis, noise figure analysis was ignored.

Table 7: Comparison of key design specifications between datasheet and co-simulation

Typical Performance at T_C = 25, Frequency = 2.5 GHz					
Measurement Data Set	**Linear Gain (dB)**	**Drain Efficiency (%)**	**Power Delivered (dBm)**	**Power Dissipation (W)**	**Saturated Power (dBm)**
Datasheet	15.50	32.00	43.00	56	51.40
Simulation	15.04	32.99	43.46	54	51.58

The power delivery of the device begins to significantly suffer at an input power near 40 dBm, seeing a drastic drop-off in gain and reduction in PAE rate as the power delivered levels off near a saturated point of 51.5 dBm. This matches the measured data in [28], but lays some credence into what may be causing the drop off in performance, which could be related to the saturated power of 144 W seen in the simulations and effects of the thermal performance limits of the device at such high power levels. True to RF principles, the PAE is at a maximum of 68% near the saturated power of 51.5 dBm [4, 6, 8]. The PAE percentage also validates the theoretical achievable efficiency in class-AB operation, which entails a maximum between 50% - 78%.

4.1.2 Maximum Power model calculations

The back-off in power would indicate the PA's tradeoff for linearity. The maximum linear power is a key specification for the linearity of a PA. It can be extracted using equation 4.1 by counting the path loss budget and maximum power reduction (MPR), which is used to address PAPR variation [9]. P_{MAX_PAM} represents the maximum linear output power for the power amplifier module, and P_{MAX_UE} is the maximum power allowed by the user equipment (UE) transmitter power class, and P_{LOSS} is the path loss budget of the propagation area. The propagation path loss model would make up estimated losses in the environment and distance of the maximum cellular range. The MPR and path loss are dependent on modulation schemes, but the latter can also be extracted with the simulation data from ADS and momentum. A modulation scheme of quadrature phase shift keying (QPSK) lists a maximum MPR of 1 dB,

while a modulation scheme of 16-bit quadrature amplitude modulation (16-QAM) lists a maximum MPR of 2 dB [9]. Based on measurement and simulation data, the P_{MAX_PAM} can be concluded to be near 51.5 dBm. The P_{MAX_UE} for LTE can be assumed to be a class-3 transmit power class, which is 23 dBm across all frequency bands [29]. Assuming a 16-bit modulation scheme is utilized, the maximum path loss can be calculated with a UE power range between 0-23 dBm.

$$P_{MAX_PAM} = P_{MAX_UE} - MPR + P_{Loss} \tag{4.1}$$

Based on equation 4.1, and the simulated maximum power delivered, the propagation P_{LOSS} is allowed to be between in a range of approximately 30 dB and 53.5 dB to account for all levels of transmit power, which would indicate a very transmit area for the LTE signal. Models, such as the Okumura-Hata, are widely available to calculate path loss in indoor urban areas (where pico-cell repeaters may be used) based on area and distance, among other parameters. Refer to the appendix for the Okumura-Hata model path loss curves to estimate loss across frequency for the limits discussed in this section [30].

The next section shows conducted studies of the co-simulation data across different operating case temperatures and shares key performance parameters for evaluating the thermal limits at the operating point chosen in this section (i.e. P_{IN} = 29 dBm, Frequency = 2.5 GHz).

4.2 CGH25120F thermal related performance

The reliability and power performance of a GaN device depends critically on the operating channel temperature [18]. CREE has developed a systematic approach to thermal modeling and measurement of their CGH25120F large signal model. Since GaN has a high power density, the application of this approach to the prediction of operating channel temperature is essential to evaluating robustness and reliability. CREE has allowed designers to enter thermal resistance values that are imported into the self-heating large signal model so channel temperatures and

resulting effects on RF performance can be determined in the design phase [20]. Sweeps of operating temperature and thermal resistance are characterized for the CGH25120F transistor.

Chapter two describes several relevant thermal concepts, including calculations on thermal resistance and its' dependencies on a variety of parameters. It's worth repeating the relationship between temperature, dissipated power, and thermal resistance as that with ohm's law. The thermal resistance can equivalently be calculated by re-arranging equation 2.7, to produce equation 4.2, where θ_{JC} is the thermal resistance between junction and case, while T_J and T_C are the junction and case temperatures of the package, respectively [13, 18]. The dissipated power is once again treated as the constant flow of energy across the channel and case.

$$\theta_{JC} = \frac{T_J - T_C}{Dissipated\ Power} \tag{4.2}$$

4.2.1 Effects of temperature on CGH25120F evaluation board performance

The co-simulation results across temperature are shown in Figure 31. The CGH25120F model was swept across operating case temperatures of -40°C to 150°C, which corresponds to the CREE HEMT's ratings. Across these temperatures, the simulation shows a clear reduction in PAE and the subsequent reduction in power delivery. Closer inspection on gain and DC power, seen in Figure 32, shows a linear degradation of the RF performance of the device. This would indicate a linear performance metric of the CREE HEMT model in the specified temperature range.

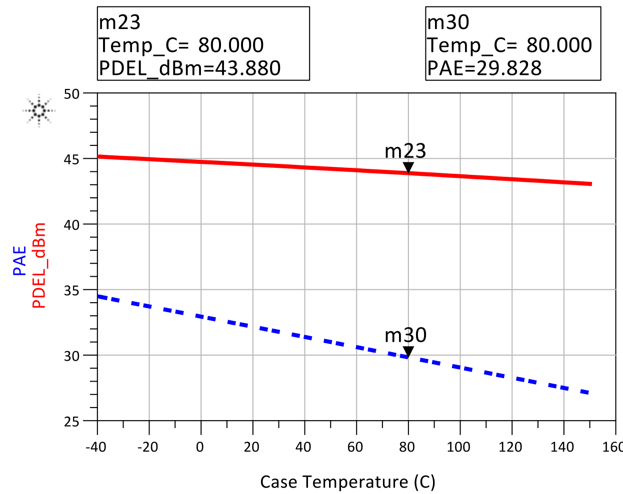

Figure 31: RF performance of PAE and Output power across ambient temperature

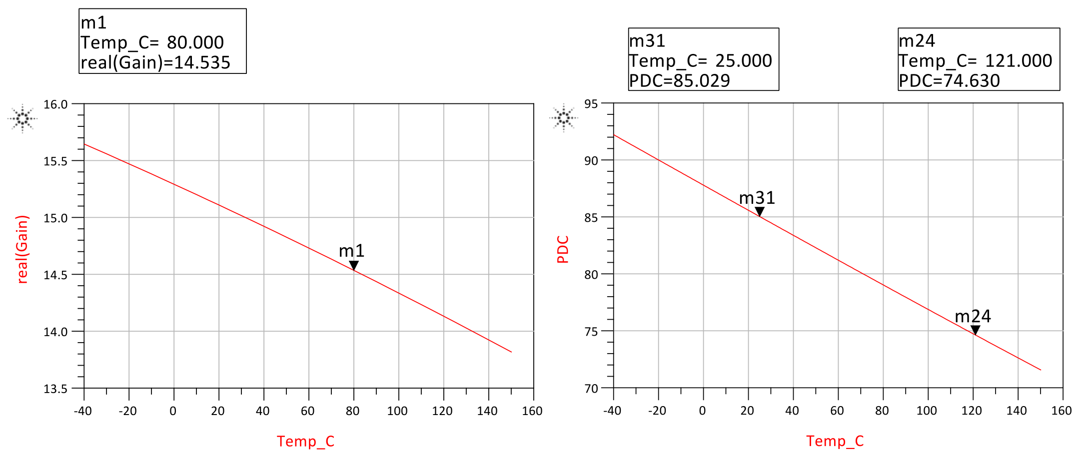

Figure 32: Linear decline in gain and DC power across temperature

The linearity of the RF performance degradation can be scaled all the way down to the junction temperature. Using equation 4.2 and the simulation results, the junction temperature can be calculated as a function of the dissipated power and constant thermal resistance. As can be seen in Figure 33, the junction temperature rises at a constant rate, reaching a maximum value of 228°C at the edge of the operation range, which coincides very closely to the maximum junction temperature specification of the CGH25120F module (T_{Jmax} = 225°C). The linear behaviour is a result of the RF performance reduction. Therefore, it can be deduced that the CGH25120F model displays a linear behaviour in RF performance degradation as operating temperature rises.

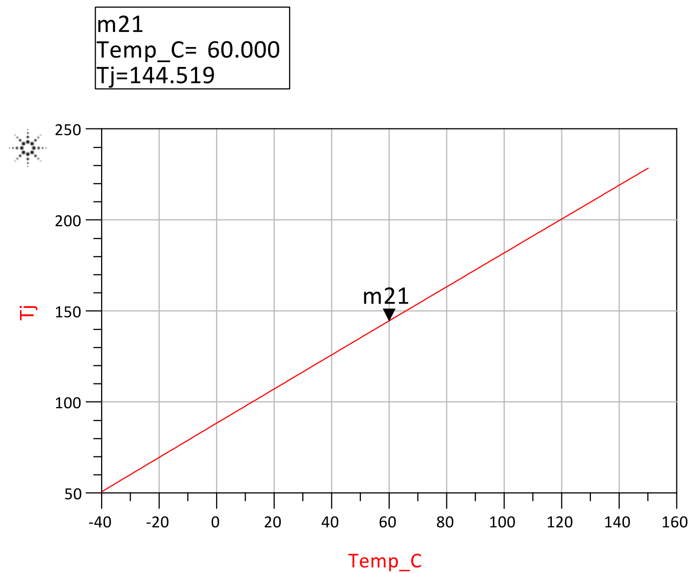

Figure 33: Junction or channel temperature rise at thermal resistance of 1.5 °C/W

The results, however, seem to be too ideal when considering the basic foundation for thermal resistance calculation, seen in equations 2.8 and 4.2. For the calculations derived from the simulation results, a thermal resistance is being assumed based on a datasheet and as such allowing for a very simple calculation of theoretical junction temperatures. Furthermore, these simulations are being performed at a very specific operating point, with no variation in input power which was done in order to fulfill the thorough evaluation of the CGH25120F evaluation board at the specification level; i.e. recreating the datasheet test case scenario.

4.2.2 Temperature related performance across input power

The CGH25120F model's thermal engine is analyzed across varying power levels in this section. Previous sections have covered a single operating point to keep consistency with the CREE datasheet, however for full analysis, it was important to sweep various input power levels to observe if the model's thermal parameter influenced results more. As established in the previous section, the RF performance begins linearly degrading across higher temperatures, indicating a strong influence of operating case temperatures on the DC and RF operation of the

device. Efficiency, gain, and power delivery all reduce while junction temperature rises as temperature increases. A peculiar trend is however noticed with the power dissipation, as it decreases while ambient temperature increases, despite the efficiency decreasing. This can be explained due to the decrease in DC power as temperature rises, as seen in equation 4.3, where P_{DISS} is the dissipated power as a function of the PAE and DC power (P_{DC}).

$$P_{DISS} = \left(1 - \frac{PAE}{100}\right) \times P_{DC} \tag{4.3}$$

This calculation effectively takes into account the gain of the device and calculates the left over power, i.e. heat, for the device to dissipate. When input power is varied, the CGH25120F model exhibits a more detailed and unique behavior. The dissipated power in Figure 34 illustrates a change in behavior near an input power of 35.5 dBm. This operating point is still in the linear operating region of the device, at which point we see the effects of case temperature more prominently in the results. The higher operating temperatures begin to show more dissipated power and continue as such past the saturation point of the device. This also coincides with the turning point in the device's gain, seen in Figure 29. Therefore, the cause for concern comes at the point of saturation, where it can be seen that the dissipated power is increasing despite the gain reducing.

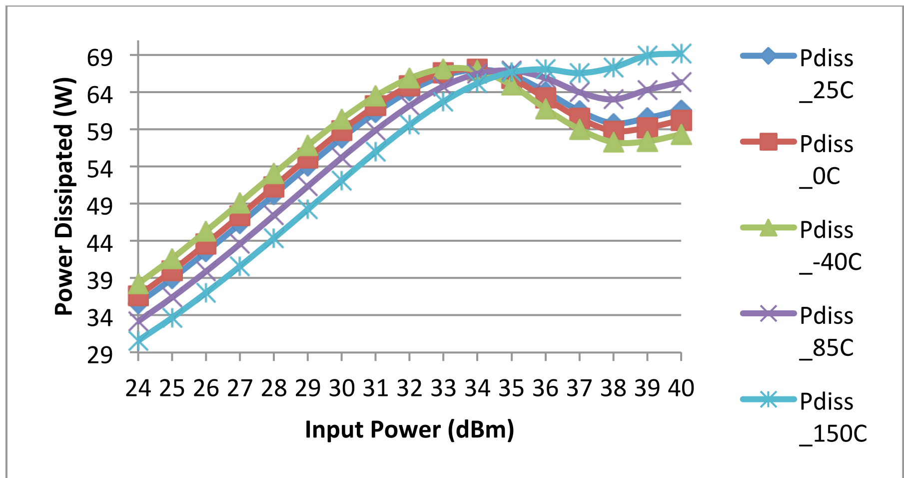

Figure 34: Power dissipated in watts over different input power (dBm)

The junction temperature is also shown to increase with temperature, as expected. It can be seen from Figure 35 that at the same input power level of 35.5 dBm, only the junction temperature at 150°C ambient is consistent, which may indicate susceptibility to thermal runaway. This justifies the limits set by the manufacturer on case temperature and clearly showcases severe degradation when the junction temperature exceeds 200°C. For PAE and gain information, please refer to the appendix.

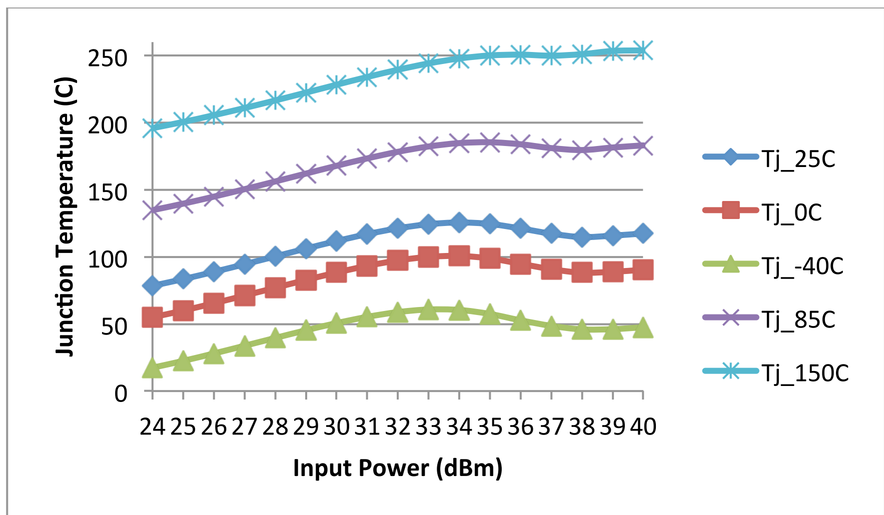

Figure 35: Junction temperatures across different input operating points

4.3 Heat Flux Analysis on Momentum Structures

In reality, thermal resistance is composed of many complex heat transfer mechanisms through a module [20]. As chapter 2 explained, these resistance values depend on material that influence the thermal conductivity and power density. Designers can model the power dissipation in the design path by modeling the heat flux, which is the heat transfer rate per unit area. This helps identify potential heat spots and current bottlenecks based purely on geometry and layout. For the CREE evaluation board, the effects of the long metal traces cannot be ignored. Main RF and DC power will propagate through these micro-strip traces and can add to the loss of power. Proximity of the traces to the main transistor will also highlight the flow of power into the device; a bottleneck path into the device may further heat the transistor, affecting the ambient case temperature. Before evaluating the device's thermal behavior, a simulation for current density and heat flux was performed on the momentum structures, representing the copper traces of the evaluation board. The simulations were performed in SONNET. The output momentum structure current density and heat flux are presented in Figure 36 and Figure 37, respectively. The simulations are performed with unity voltage at the input to help understand the distribution at a smaller scale. It is observed that the output signal enters the delivery path with ample copper area allowing for better distribution of power. As expected, a bottle neck series path near the output port shows a much higher current density and heat flux [30-32]. Furthermore, the operation at such high frequencies indicates a possible effect of skin effect as the current density increases in the conductor region at the surface [19]. The heat flux along the same path confirms the effect of the higher current density resulting in more power dissipation. The tight path also means higher resistance, and with the high current density will result in more heat [30]. When applying the drain bias voltage, the simulation shows the heat flux can reach a maximum value near 798 Watts/mm^2 in very tight traces. It is plausible that traces can begin to melt at these points. To reduce the heat flux and current density would simply mean to widen the traces. Though this is just an evaluation board, it highlights the importance even more for proper

routing as the industry trends towards tighter form factors. Standards such as the IPC-2152 [32] provide a good guideline for current carrying capacity in PCB design.

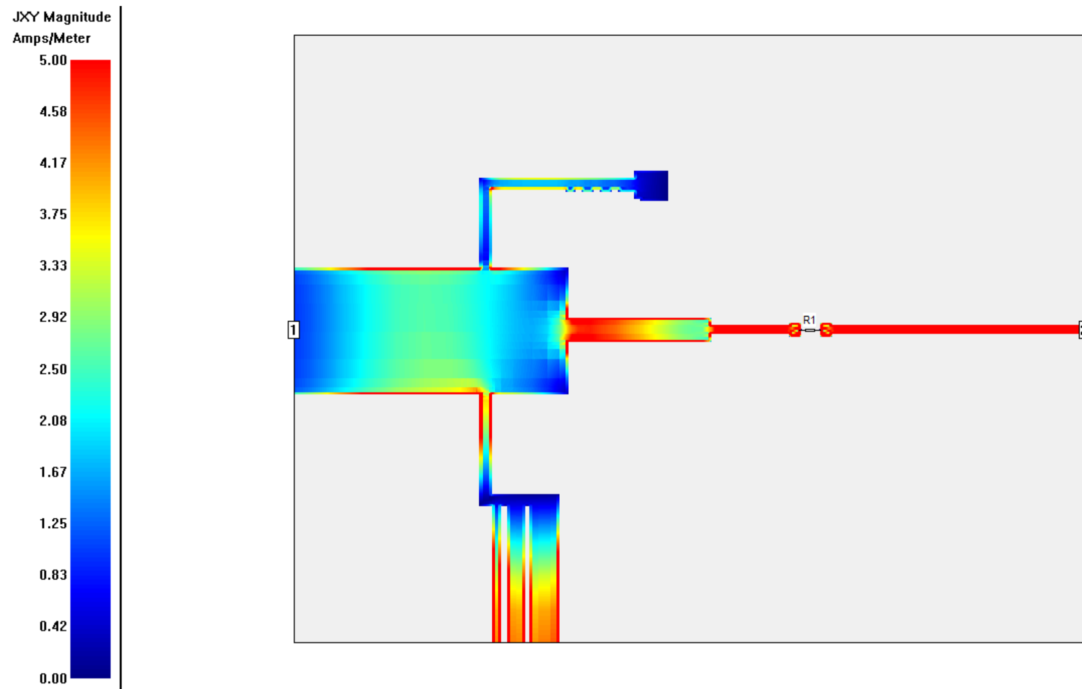

Figure 36: Current Density of the output power delivery path

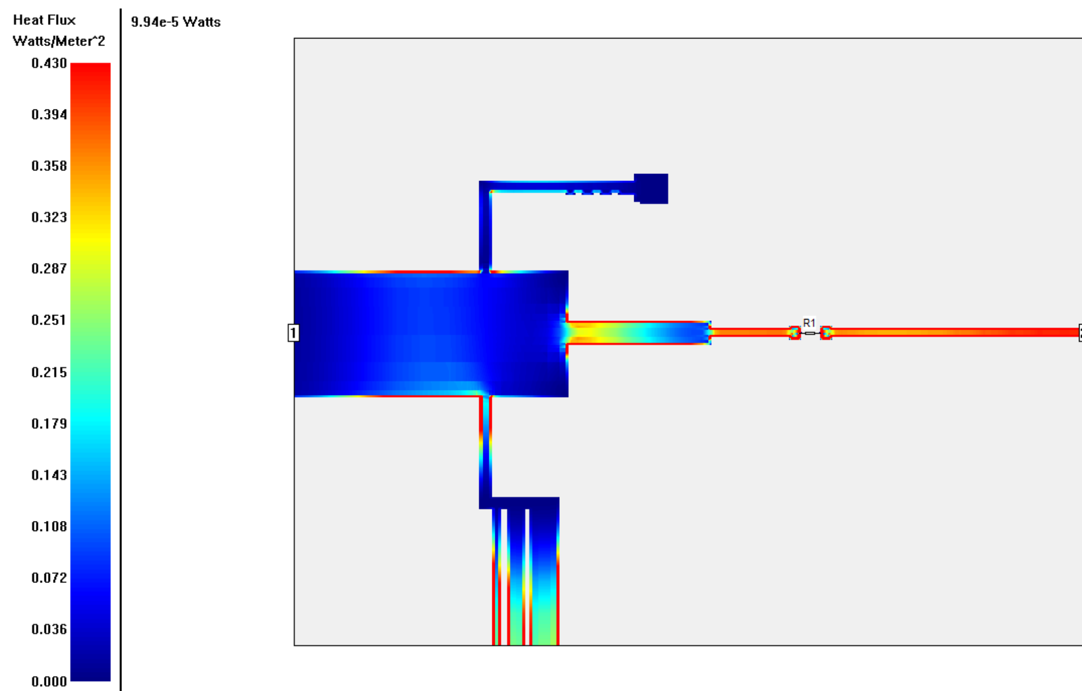

Figure 37: Heat Flux of the output power delivery path

4.4 Conclusion

After successfully recreating the CREE evaluation board, the thermal related effects on RF performance could clearly be seen in the CGH25120F model. The degradation is correlated to the junction temperature of the device and begs the question to how the design can be improved further to prevent heating at the junction. Figure 38 shows this relationship between degradation and junction temperature. Chapter two discussed some efficiency enhancing techniques that can improve the power dissipation and efficiency allowing for lower rise in junction temperature. At the device level however, material properties and stackup play a key role in the thermal performance and heat distribution. After all, the regions within the HEMT stackup makeup the total thermal resistance the device sees. Many studies have been performed to predict thermal resistance in each layer of a HEMT device as seen in [18, 19]. The geometry and spacing can also influence the thermal effects as shown in the SONNET simulations for heat flux and current density. The next chapter focuses more on the physical layout and dimensions and offers an improvement in design of a GaN HEMT PA, focusing on the temperatures seen at the device and the corresponding RF performance.

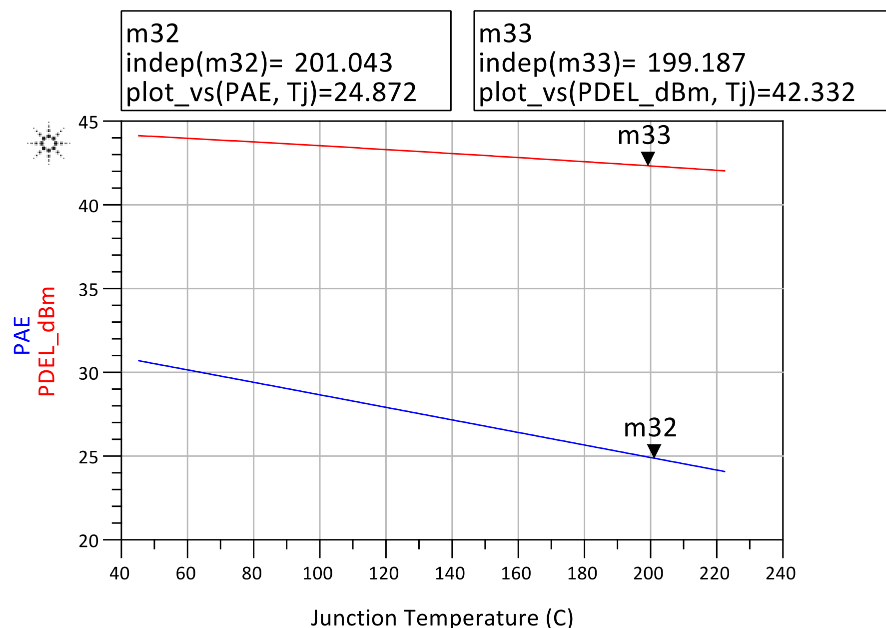

Figure 38: Efficiency and power delivery degradation as a function of junction temperature

Chapter 5 – Improvements at device level for thermal optimization

GaN FETs are considered as great candidates for high power microwave systems due to their material properties such as high-breakdown voltage and high saturation current. As a result, power dissipated in GaN FETs can reach very high values and lead to substantial self-heating of the device [33]. In the analysis of a GaN device, such as the CGH25120F in Chapter 4, it is abundantly clear that power dissipation will occur and affect RF performance.

The dissipated power is let off as heat and ideally needs to flow out of the chip into the environment. However, the ever-shrinking chip size causes the heat to concentrate within a small area that leads to higher power density [33-35]. This causes the device to heat up and can possibly exceed the maximum allowable temperature, especially in high-powered applications. Thus, the goal of every designer is to minimize potential self-heating effects and distribute the heat evenly without compromising on performance and form factor [3, 35-40]. We have already discussed how material properties play heavily into these decisions and that the GaN technology is the top candidate in the market for optimal RF and thermal performance trade-offs. The analysis of the CGH25120F however also shows potential for exceeding specification on temperature at higher power levels.

This chapter will analyze a single RF PA device in the CREE evaluation board circuit and how the heat is distributed within the cells and substrate, and present an accurate depiction of channel temperature using an electro-thermal simulator. A modified design with multiple stages in parallel is also presented that offers improvements on thermal and RF performance under the same bias conditions. For the simulations, the CGH25120F model is not utilized, as the vendor was unable to provide compatible models for the electro-thermal simulator. Instead, a non-linear design kit model from ADS is used with GaN characteristics and can effectively be used to detail the effects of device sizing and geometry.

5.1 Single FET Analysis

Most market devices today can effectively use a single cell as an RF PA. Such is the case with the CGH25120F design presented in Chapter 4. To create a baseline of the effects on a singular device, a single stage FET from the non-linear Agilent demo-kit is inserted as a replacement in the CGH25120F evaluation board circuitry. This way, it mimics the same routing and impedance matching with passives, however since it is a different FET than the CREE model, the DC biasing and load-pull analysis is different. The biasing shows a much lower DC power indicating the inability of the device for higher-powered applications. The non-linear design kit used allows for a maximum of 8 fingers and gate width of 300 um. Therefore, the maximum gate size allowed for this design is 2400 um. The device can be seen in Figure 39, with the maximum number of fingers along with bond vias to ground. The FET utilizes the specified GaN substrate dielectric constant and substrate thickness, denoted as 'H', as seen in the GaN foundry (i.e. H = 10 mils, $\varepsilon_R = 9.5$) [27]. The thermal resistance is also kept consistent with the CGH25120F model at θ_{JC} = 1.5 °C/W.

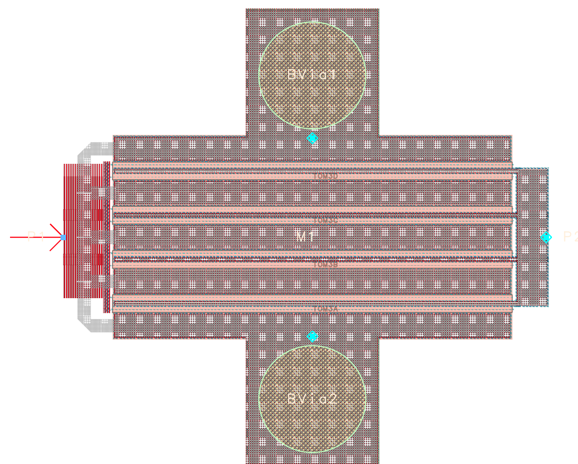

Figure 39: Non-linear medium power FET layout

The DC biasing of the device is kept consistent with that of CGH25120F, where the voltages are biased to produce a quiescent current of ~ 500 mA.

5.1.1 Load-pull vs Electro-thermal Analysis

Load-pull analysis of the device reveals maximum theoretical efficiency, power delivery, and gain are significantly lower than that of the CREE model (as seen in Table 5). The load-pull data for maximum achievable efficiency can be seen listed in Table 8. Temperature is assumed to be at a normal room environment for industry standards to place more emphasis on the self-heating effects of the device. Based on this data, the electro-thermal simulations will focus on a lower power scale than those seen in Chapter 4 for the CGH25120F model.

Table 8: Load-pull on single FET structure showing lower capabilities than the CGH25120F model

Temperature	Optimal impedance (Z_{OPT})	Input impedance (Z_{IN})	Maximum PAE at load (%)	Gain at load (dB)	Power Delivered
25°C	2.75 + j0.651	5.392 – j2.631	14.215	5.790	34.79

Since there is no temperature parameter in the model to perform load-pull analysis with, a load-pull of the entire circuit is performed for output power, gain, and PAE. The results were then compared to an electro-thermal simulation of the same circuit varied across input power. Compression was seen in the electro thermal results for PAE and output power. The PAE percentage point data is seen in Figure 40, where LP_PAE is the load-pull measured PAE, ET_PAE is the electro-thermal measured PAE. The compression is measured as the difference between the electro-thermal simulation results from the load-pull results.

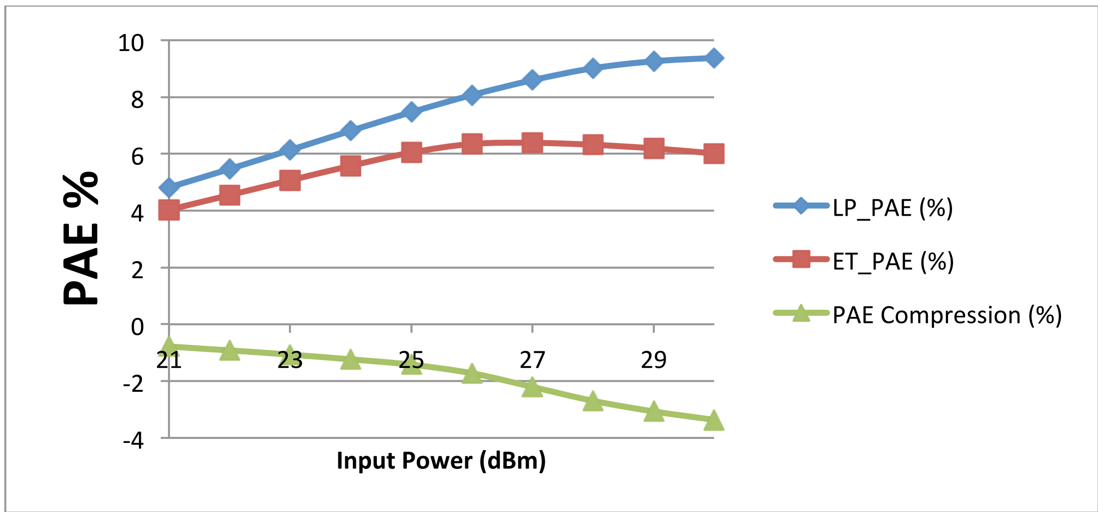

Figure 40: Load-pull and electro thermal comparison along with PAE compression

It's clear to see from the PAE compression points that thermal effects negatively impact the efficiency of the circuit despite no changes to impedance structure. Thermal effects affect power delivery similarly, where the compression goes below -2 dB at higher power, and thus, higher temperature. The 1-dB compression point occurs at an input power of 21 dBm and can be seen in Figure 41.

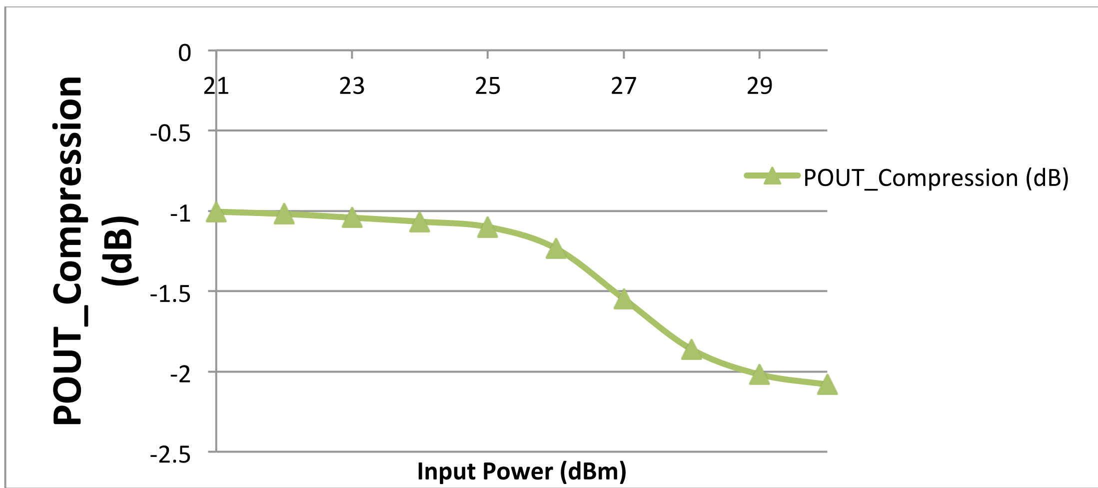

Figure 41: Output power compression seen between load-pull and electro-thermal simulations

The gain also sees a reduction with the electro-thermal simulation, with the 1-dB compression point seen at 21 dBm of input power. The compression is expected and proves the independent effects of thermal from impedance. The compression curve can be seen in Figure 42.

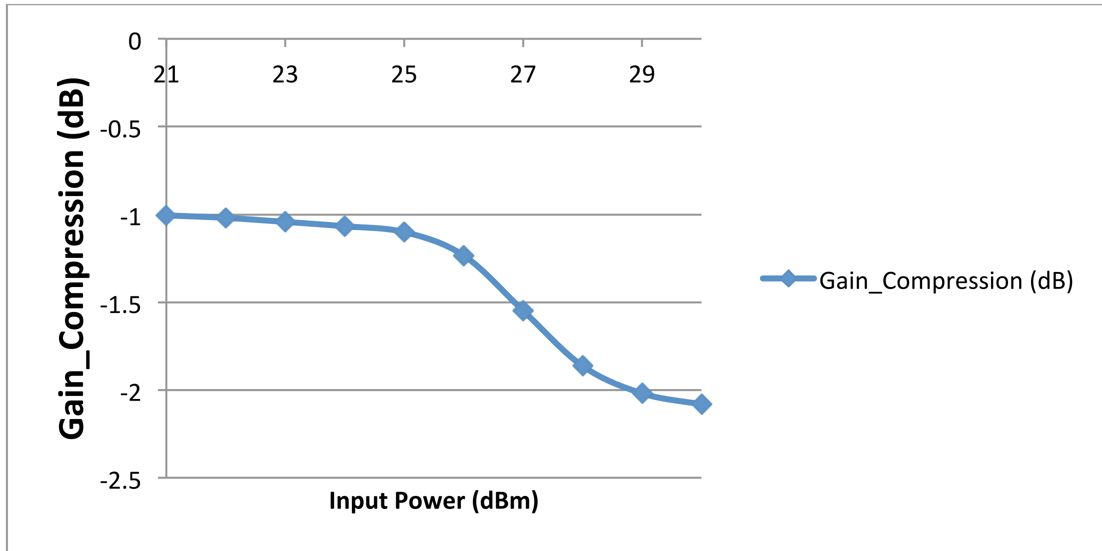

Figure 42: Gain difference of electro-thermal simulation versus load-pull data

5.1.2 Thermal Profile

The thermal profile at P_{IN} = 27 dBm can be seen in Figure 44 for the 2400 um single FET device. Consistent with the assumptions made in [18, 19], we see the fingers in the middle of the device have the highest temperature and heat dissipation. The spectrum shows temperatures potentially measuring greater than 225°C for the heat sources near the center. The power dissipated in the device is approximately 5.6 Watts for an average channel temperature of 193°C, delivering 1.6 Watts of power at the output after losses. Though it is able to produce a gain of more than 8 dB, the PAE is measured quite low at only 8.1% as seen in Figure 43. This is a stark contrast to our initial simulation results seen in Figure 29, but this is expected since the devices under test are different.

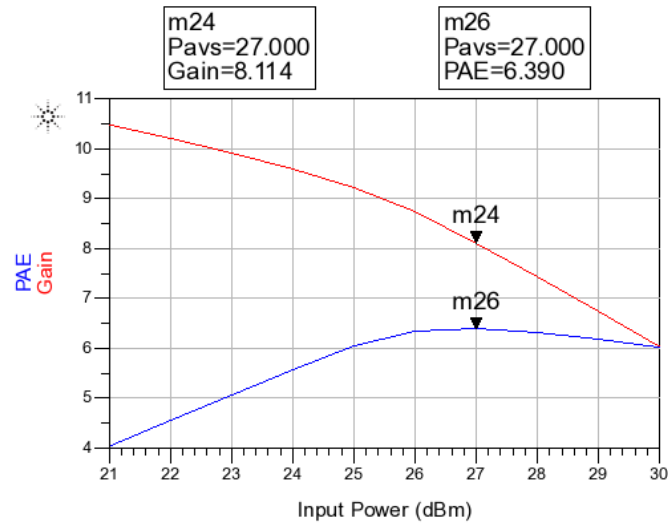

Figure 43: Efficiency and gain suffering as input power is increased, thereby increasing power at the device

The surface plot and contour curves in Figure 45 show an even distribution of power across the 4 channel sources, and the heat contours describe the heat spreading area about the device. The heat flux seen in Figure 46 shows a more detailed view of the flow of heat within the device and helps explain why the fingers near the center heat up more than the outer gates. The heat is also predominantly rising up. This behavior is fascinating to note as it gives a very detailed perspective on the behavior of a GaN device and what the roots are of self-heating effects. Since we can see heat moving within the channels, it is plausible to predict, based on the heat flux data, that temperature rise in junction or channel can be reduced if the gate-to-gate spacing is increased.

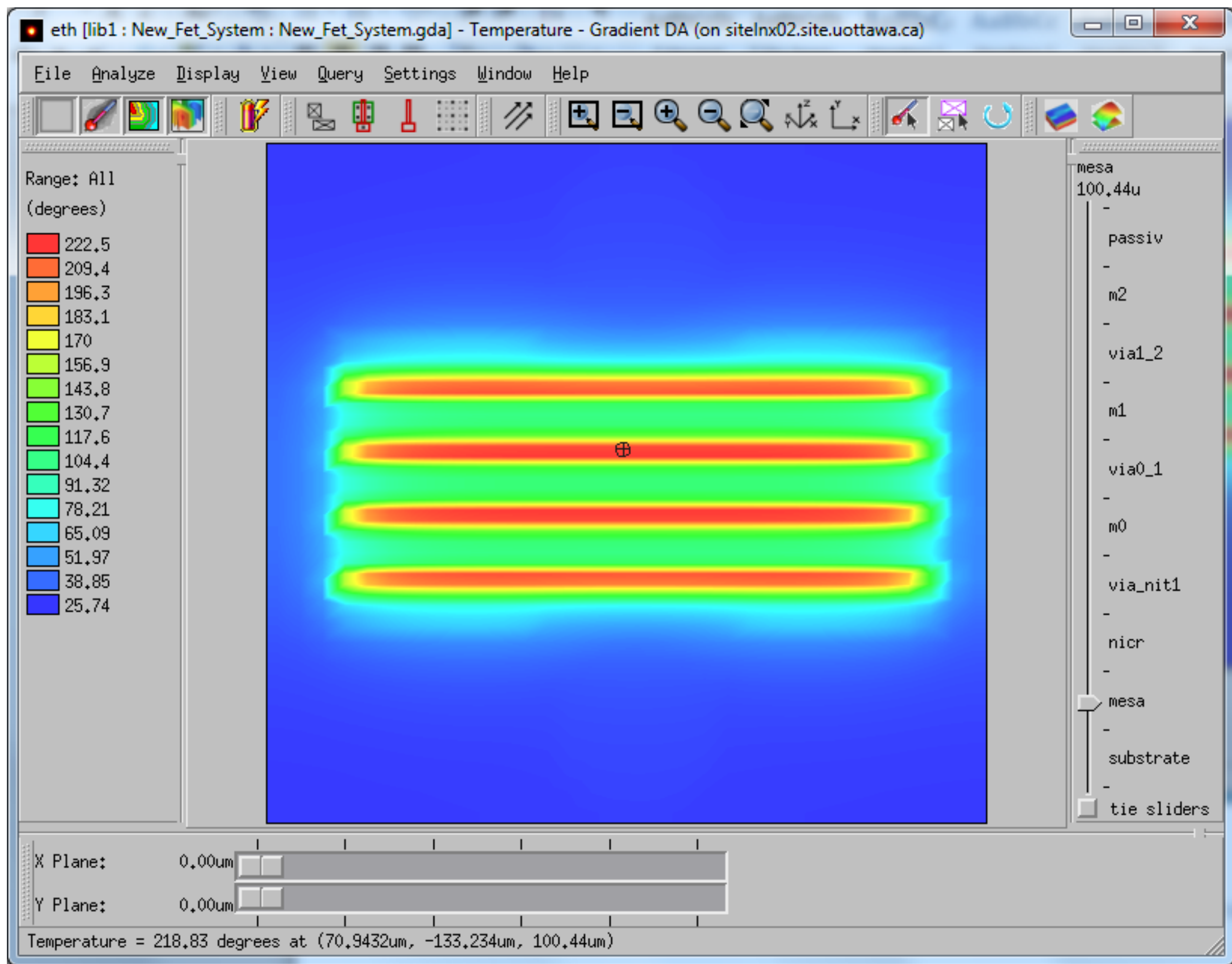

Figure 44: Thermal profile of temperature in the single FET device at P_{IN} = 27 dBm

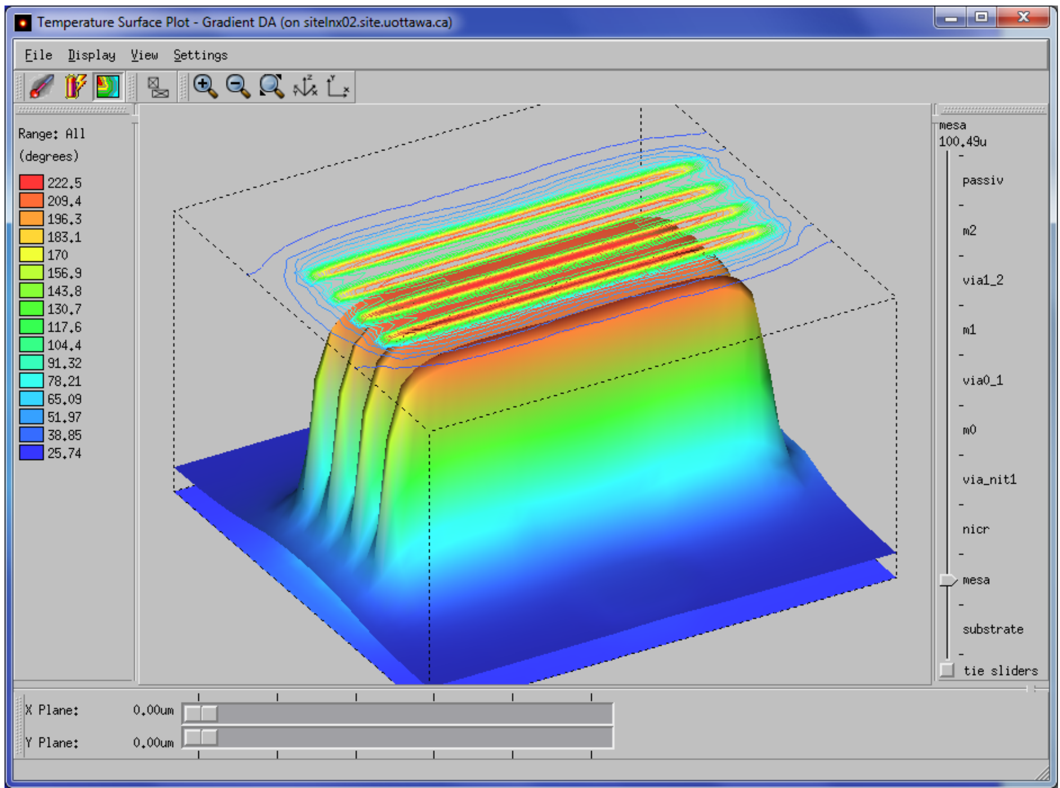

Figure 45: Surface plots and contour curves show a relatively even distribution across the channels

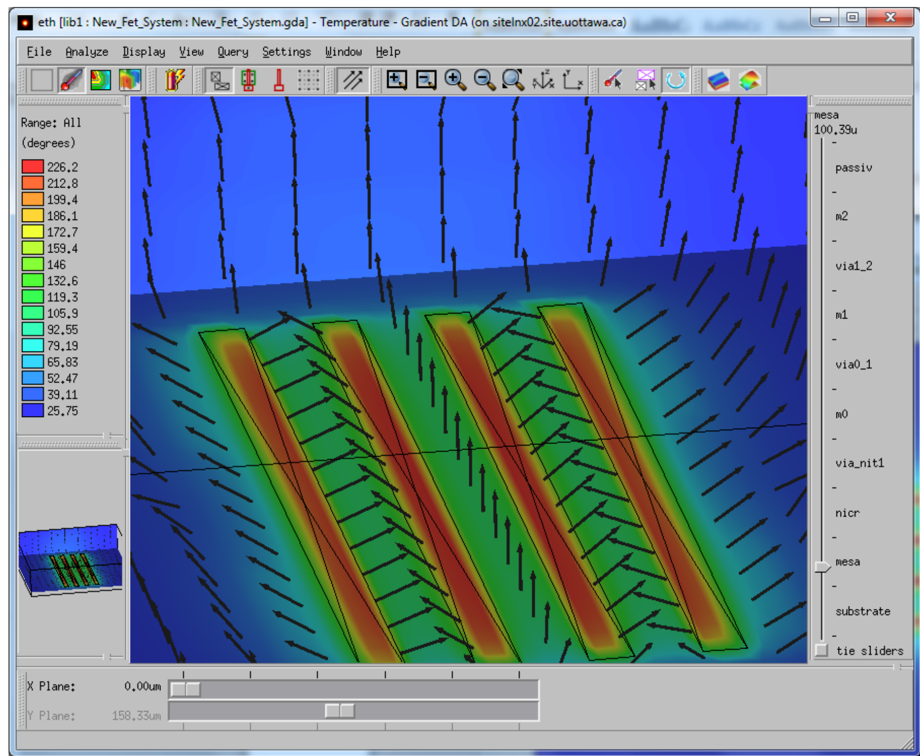

Figure 46: Heat flux representing the contour curves near the power sources

According to the study performed by Darwish et al in [18,19], there is a strong correlation between thermal resistance and gate spacing. The relationship would indicate a decline in thermal resistance as spacing is increased, a good indicator of improved heat flow. This concept will be explored in the next section.

5.2 Dual FET Analysis

The dual FET solution is a proposal where the gates are effectively spaced out by way of using two separate FETs. The devices are sized with 4 fingers and a gate width of 300 um. The total area sums up to be the equivalent of the single cell approach seen in section 5.1 (i.e. 1200um X 2 = 2400 um), and be seen in Figure 47. The FETs share a bond via in between to minimize solution size and serves as the added spacing between the gates measuring 100um in width. The design includes a 2-way splitter that feeds into the dual FET system and combiner at the output. The bias circuitry is kept consistent with the baseline design to create a more direct comparison of operating points. The thermal profile over a power sweep can be seen in Figure 48, where a fairly even distribution of power is seen between the two devices. Both devices dissipate about 2.6 Watts each.

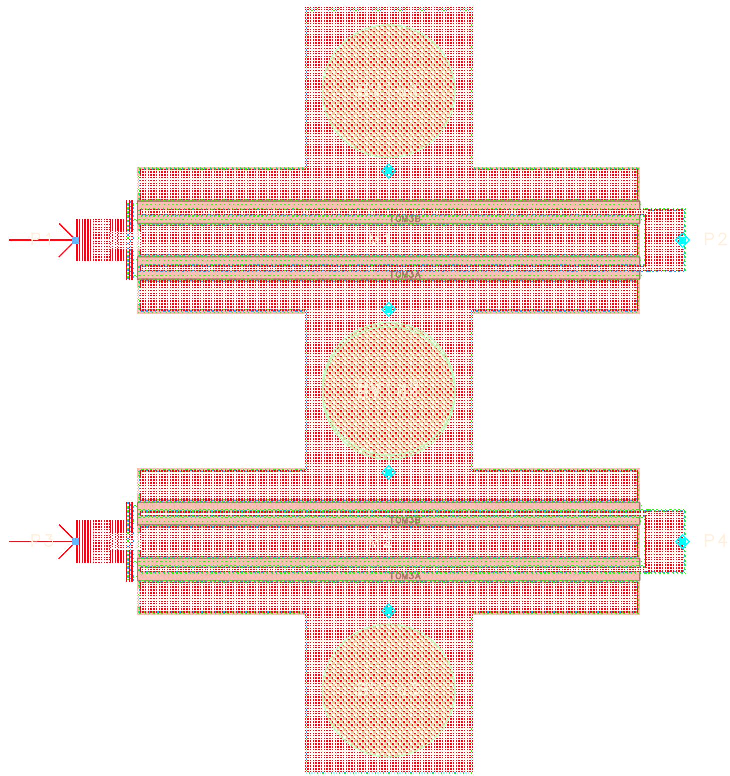

Figure 47: Dual FET Layout solution with 100um spacing

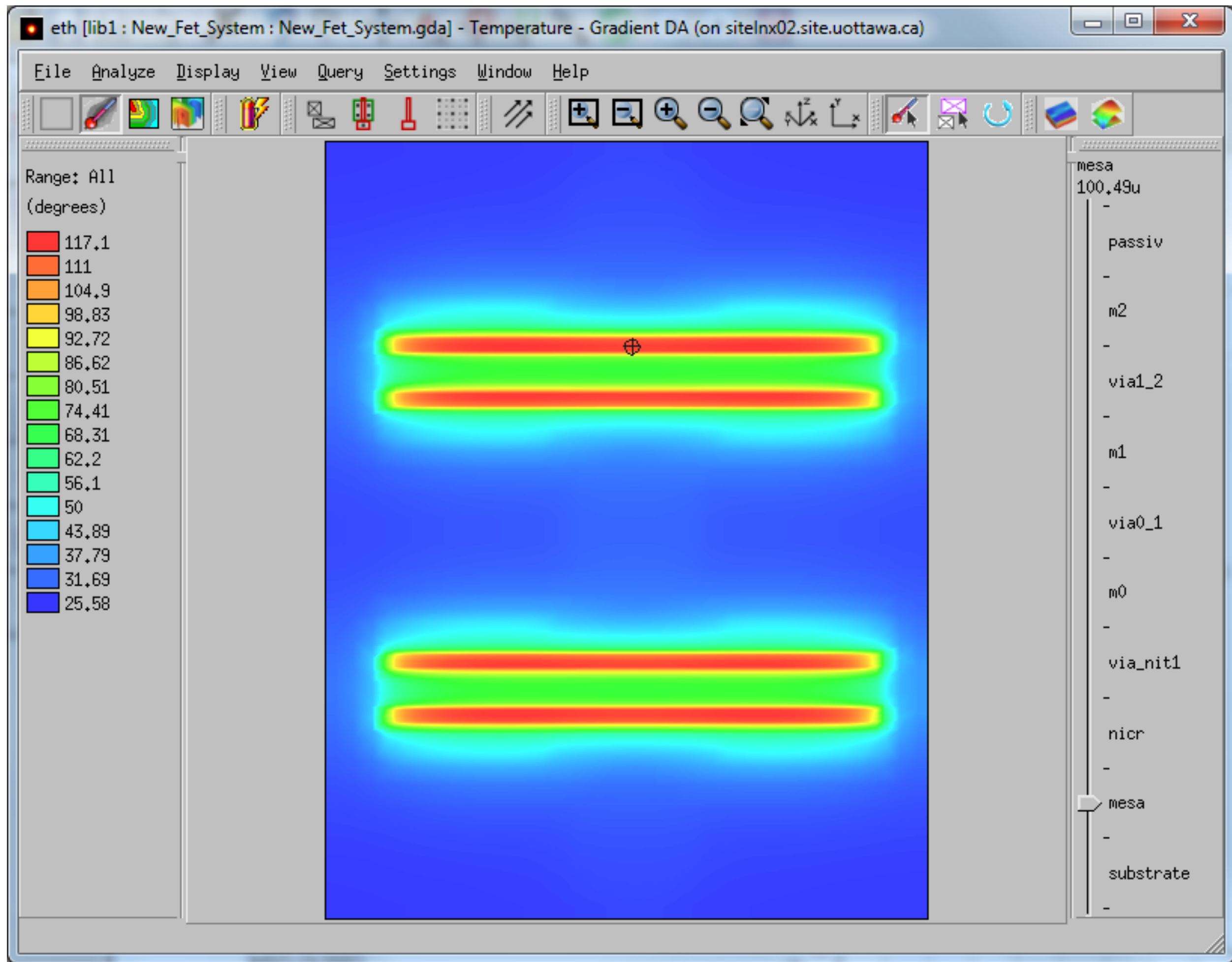

Figure 48: Thermal profile for the dual FET solution

The temperature seen at a single device is much lower at the same power level, seeing an improvement of 100°C in temperature. This in turn shows a great improvement in RF performance as well. The PAE improved to 24.68%, which is quite an achievement from the single FET solution. Subsequently, the gain and power delivery come in at over 13 dB and 35 dBm, respectively. The contours on the surface plot show a wider power distribution and heat flow path, seen in Figure 49. The heat flux when analyzed a little closer also shows the flow going towards the outer parts, choosing a path of least resistance to dissipate in. This results in the outer gates being slightly warmer in temperature as opposed to the middle gates, seen in Figure 50.

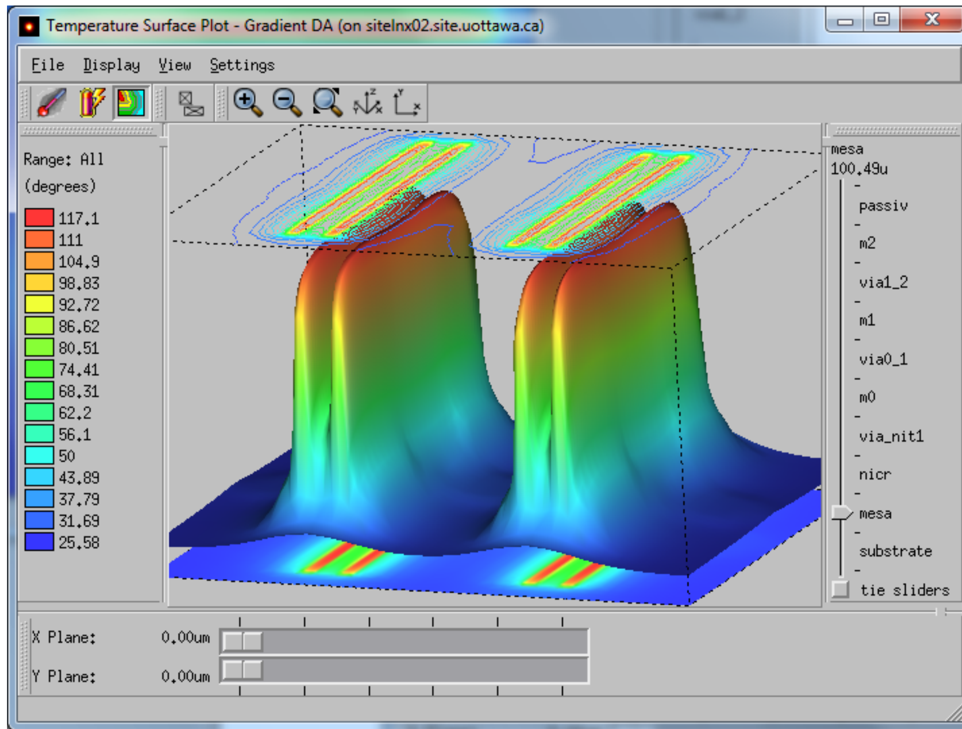

Figure 49: Surface plot and contour lines for the dual FET solution

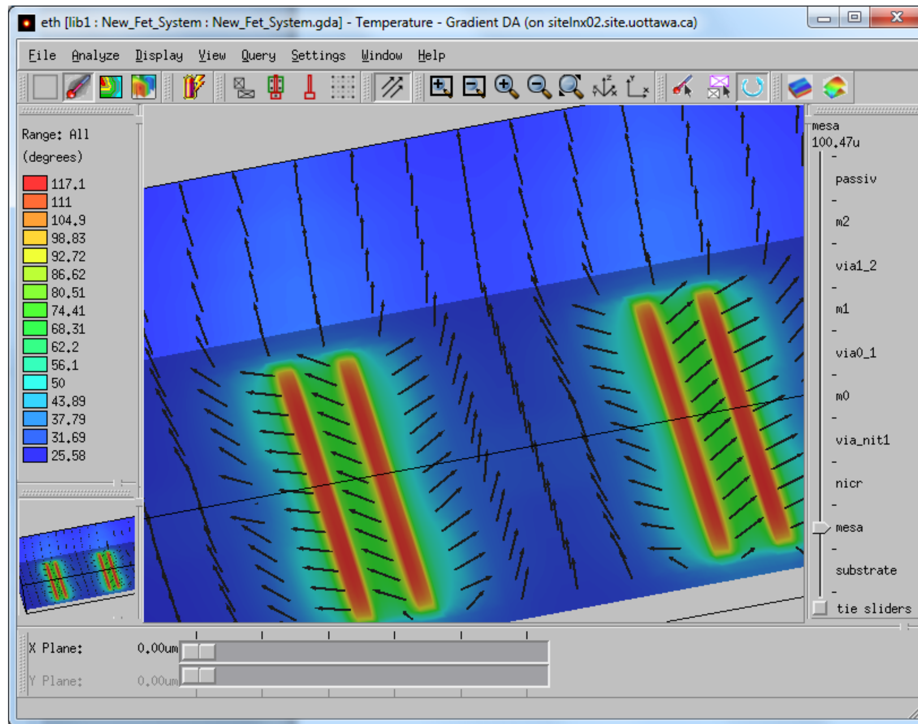

Figure 50: Heat flux moving away from the center, indicating the cooler part of the device being near the middle

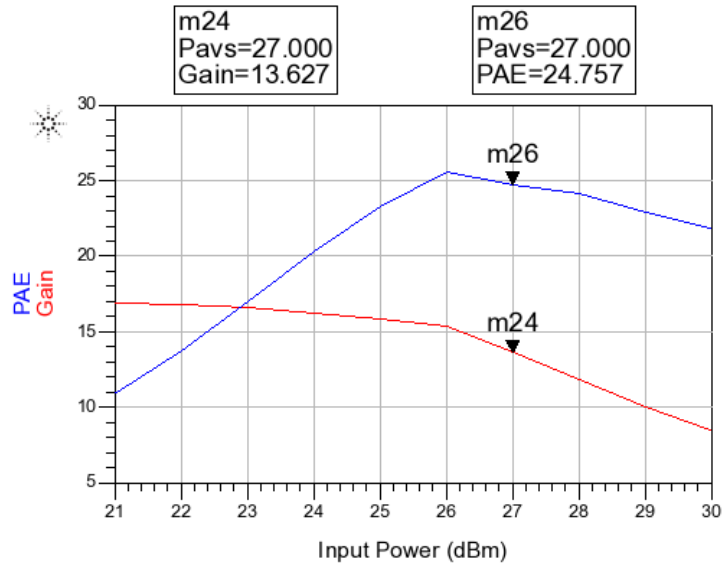

Figure 51: Drastic Improvement in PAE and Gain seen with Dual FET design

The gain and PAE performance of this design over input power can be seen in Figure 51 and shows drastic improvements when compared with Figure 43. The results of spacing out the gates are already paying dividends to the thermal reliability as no temperature is seen above 142°C across any power level, and RF performance is not compromised at all. To really see how much more we can optimize the design, a third design is constructed with an increased number of devices.

5.3 Quad FET Analysis

Similar to the dual FET solution, the quad FET proposal consists of four FETS operating in parallel with a bond via inserted in between for spacing as well as thermal relief. The FETS consist of 2 fingers and gate width of 300 um, keeping consistent with the initial device area. To effectively split the signals, multiple 2-way splitters are required to effectively feed the RF signal and biasing into the 4 separate FETs. The use of so many splitters does however introduce more insertion losses into the system that can affect the RF performance, namely transducer gain. The layout can be seen in Figure 52. Note the increase in design area due to the shared 100 um-wide bond vias between the FETs.

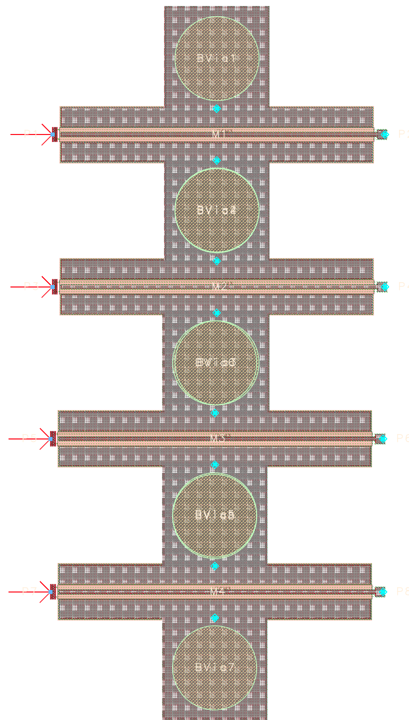

Figure 52: Layout of the quad FET solution with 100um spacing between devices

The temperature profile over a power sweep reveals a more uneven distribution of power when compared to the modified design in section 5.2. The simulations yield lower temperature values at the gates, however the output power and PAE are all worse than the dual FET configuration. One reason could be the amount of power lost due to insertion losses from the splitter and combiner circuits, along with the addition of more FETS. Some more reasons could be due to the potential unbalance of current. The current in parallel FETs can be unbalanced due to a variety of reasons. These reasons include gate driver mismatch, which may be due gate loop inductance and capacitance mismatch [41], which primarily has to do with layout.

The thermal profile and contour curves at an input power of 27 dBm can be seen in Figure 53 and Figure 54, respectively, where heat distribution was most uniform.

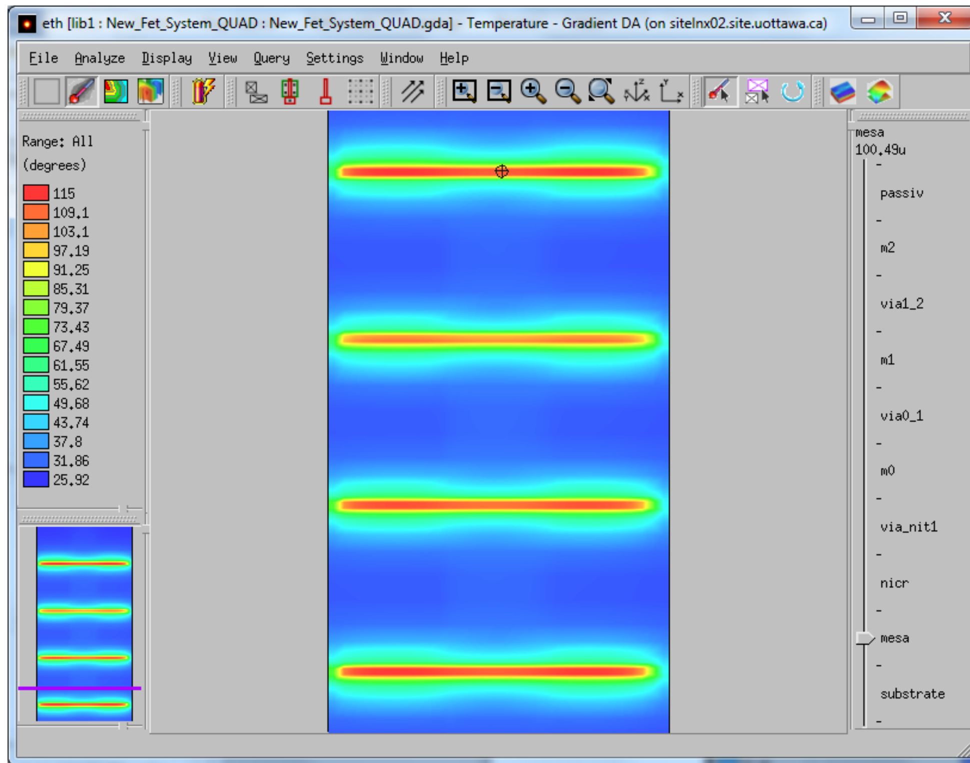

Figure 53: Thermal profile of the quad FET structure yields lower temperatures yet worse RF performance

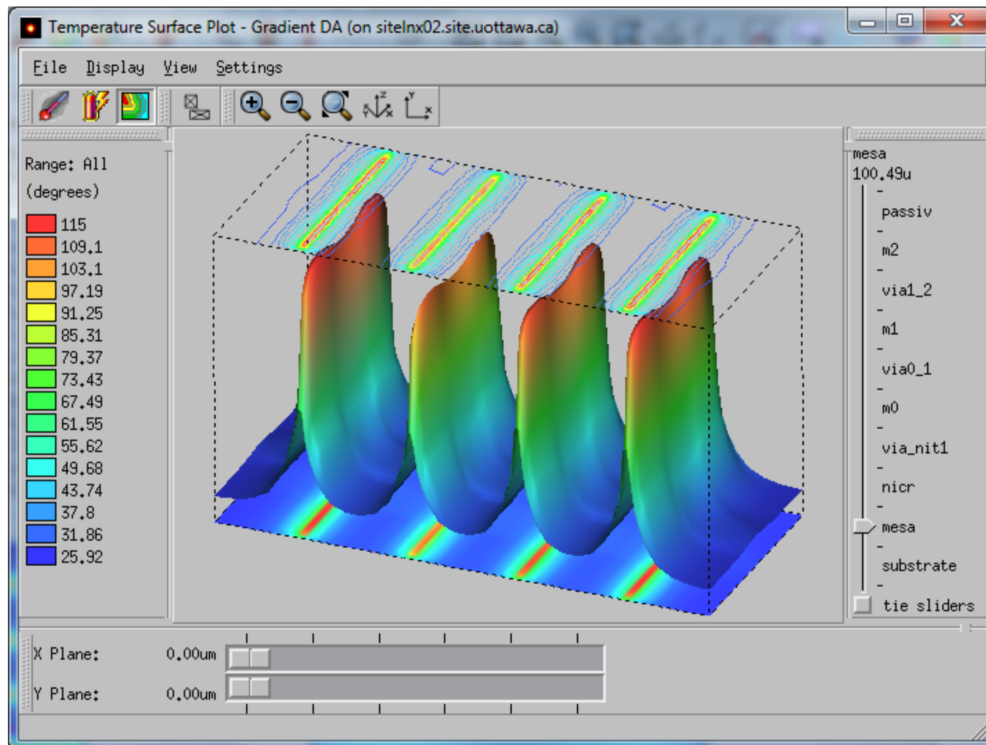

Figure 54: Surface plots and contour curves for an uneven distribution of heat

Another major factor scales back to concerns from the insertion of multiple divider and combiner circuits. The use of splitters results in DC loss, which primarily affects the biasing of the device. Power delivery is affected, as the devices are not biased as intended from the power supply settings, meaning less DC power is consumed affecting the biased current. When pre-distorting or compensating for this loss, an improved distribution was seen across all power levels. Figure 55 shows the initial uneven distribution when the input power is swept under the same bias conditions as of the previous two approaches, and compared against an over-compensated biasing. The improved distribution sheds focus on the DC biasing and the effect it has over RF power distribution. If a quad FET approach is used, it is recommended to perform separate DC biasing to account of the losses and parallel configuration. However, for the purpose of this thesis, the analysis is focused to a single biasing operating point and therefore will focus solely on the results achieved with the initial test case. Please refer to the appendix on thermal profiles of uneven heat distribution seen in both dual and quad FET architecture.

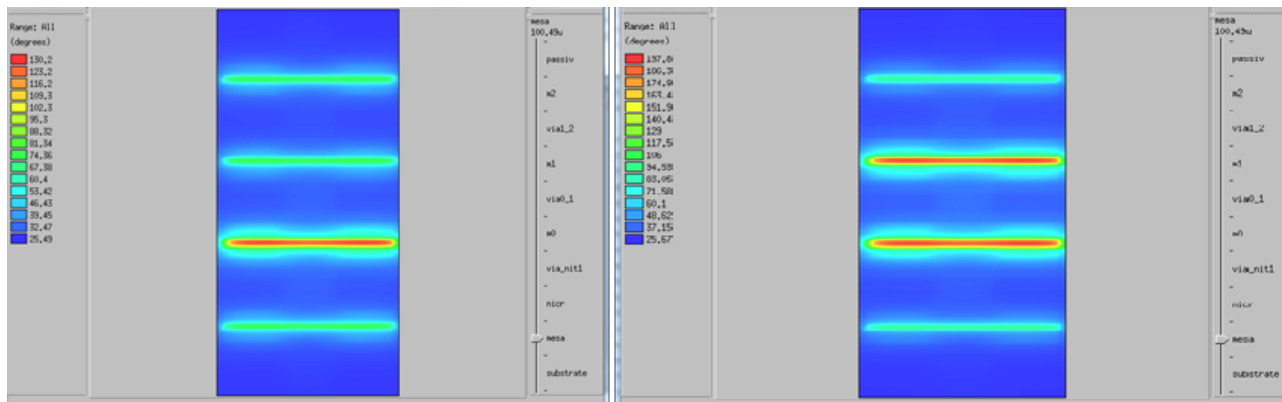

Figure 55: Initial bias versus compensated bias shows improved distribution and power delivery but higher temperatures

5.4 Discussion

A comparison of performance for all three designs details clear picture. From a temperature perspective, and protecting against maximum junction temperatures, Figure 56 illustrates the vast improvement in gate temperatures across all three approaches. The conventional single device approach shows temperatures more than 70°C warmer at higher power levels. Increasing the number of FETs shows lower temperatures across most of the input power levels, however the quad FET solution shows higher temperatures than the dual FET solution at 28 dBm of input power. This is a good indicator that the quad FET solution isn't the optimal solution for RF power, but still the preferred solution than the single FET approach.

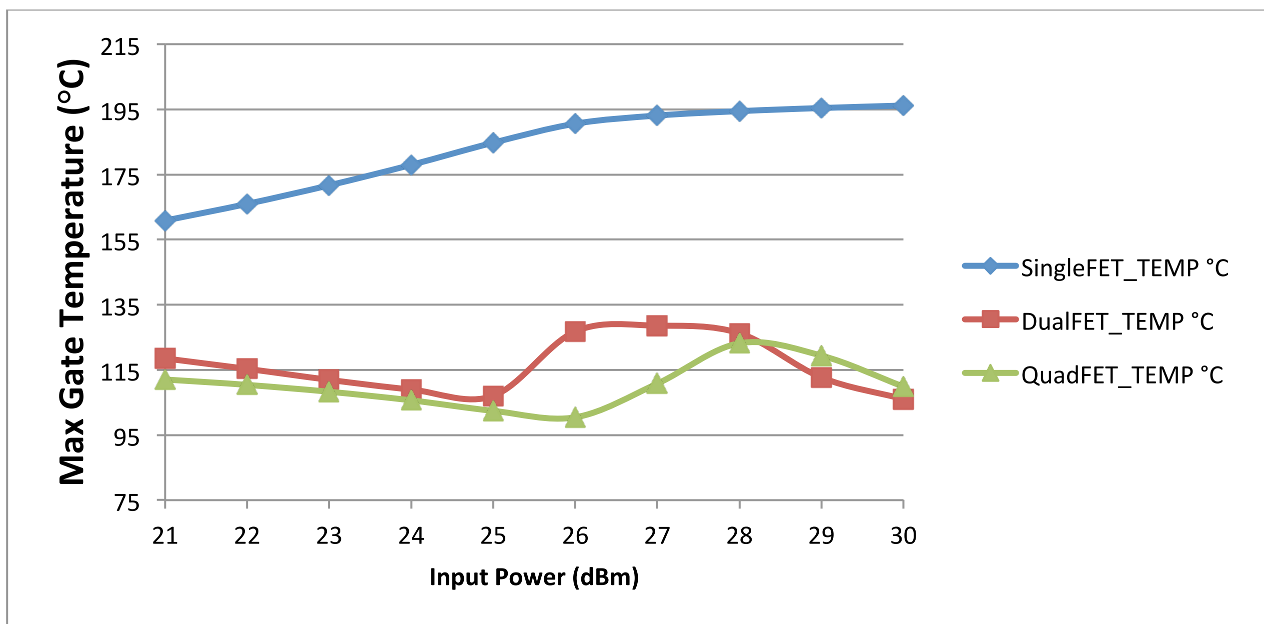

Figure 56: Gate temperature comparison for all three designs is a clear indicator of the improvements seen in a multi-device approach

The correlation between temperature and power dissipation is also realized when observing Figure 57, where it is apparent that the temperature reduction seen in Figure 56 is due to the reductions seen in dissipated power. This further validates the temperature improvements of a multi-device approach.

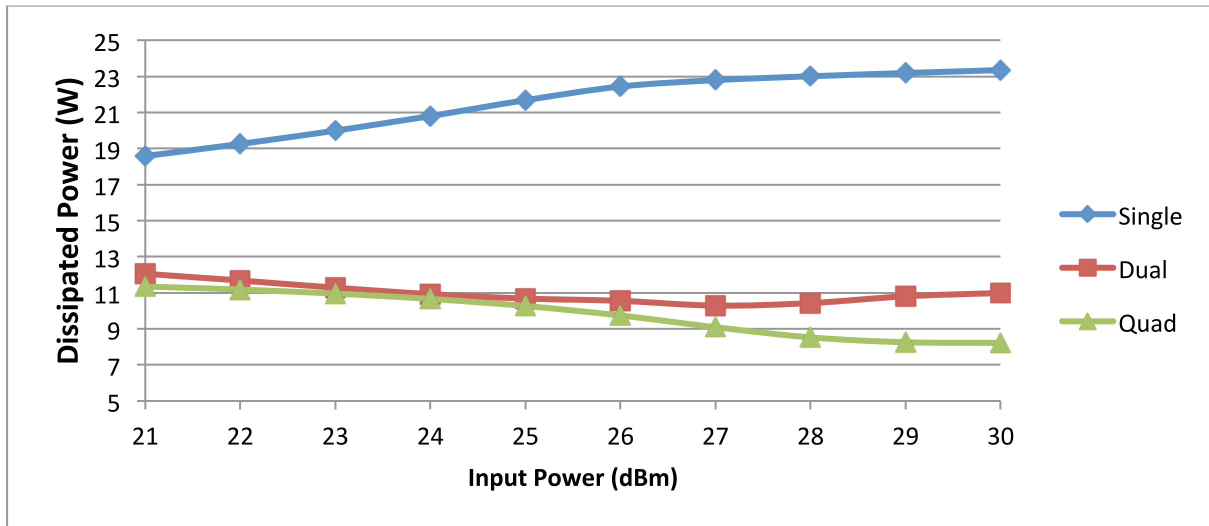

Figure 57: Power dissipation seen in a single and multiple FET design approach.

The power delivery and PAE show major improvements using the multi-device approach. This can be seen in Figure 58. Both the dual and quad FET approaches deliver a higher saturated power and considerably higher efficiency at the same bias point. However, at lower power levels, the quad FET approach doesn't deliver as much as the single FET approach, which can be purely attributed to the lack of optimal DC power. The dual FET approach comes out as the clear winner under these conditions, as the efficiency and power delivery are much better than that of the single and quad FET approach. Furthermore, the dual FET approach also results in minimal increase to design area by virtue of the spacing between the two devices. This is an excellent trade-off for increased output power, gain, and efficiency that is extremely valuable for small form factor designs. A device, such as the CGH25120F amplifier, can see drastic improvements under the same settings if it utilizes the dual FET approach presented in this thesis. If we look simply at the single FET approach, we can see the dependence on temperature and the impact seen on gain, efficiency, and power dissipation, seen in Figure 59. This compares well with the effects seen from the junction temperature in the CGH25120F model. Therefore, the thermal analysis performed in this chapter can be used to predict degradation and improvements in temperature and the ensuing RF performance. This concludes the thermal analysis on the CGH25120F amplifier and the generic GaN amplifier.

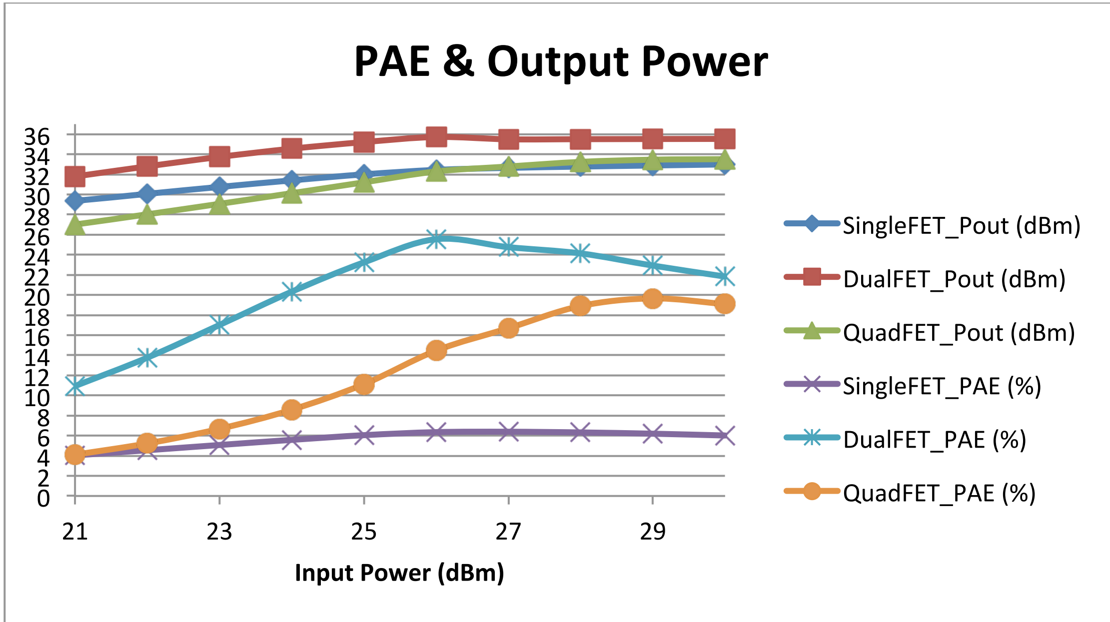

Figure 58: Summary of efficiency and power delivery across all three FET design approaches

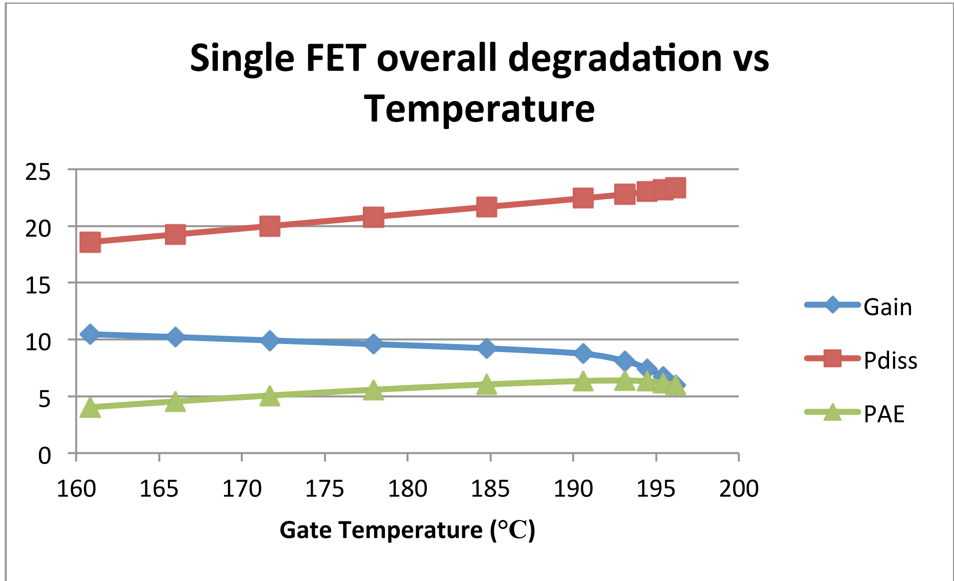

Figure 59: Degradation in the single FET approach across gate temperature

5.5 Conclusion

After analyzing three distinct designs, it's clear to see what steps designers can take in order to improve thermal performance of a power-amplifying device. Proximity of conducting gates result in self-heating, and affect the RF performance of the device. To protect the device against reliability concerns and performance degradation at such high power levels, it is recommended to use a parallel multi-device approach to effectively split the signal and current consumption, thus leading to improved heat flow.

Chapter 6 – Conclusion and Future Work

6.1 Summary

The research in this thesis has characterized the thermal performance of an in-market GaN device and presented the correlation of temperature and RF performance. The underlying focus is on the importance of thermal performance of a device due to the aggressive demands of the market to reduce package size.

Though technologies today, such as GaN, have improved to help designers to help alleviate effects of high power compacted in a small design area, it is crucial to recognize the trends and present a design approach that can be as simple as a plug and play approach [3, 14, 36, 40]. The thesis concludes that a GaN FET can operate more efficiently, delivering higher power, and reduce device temperature significantly if it is designed with multiple devices in a parallel structure. The use of two FETs in parallel produced the best results in RF performance and improved thermal performance by more than 70°C at the gate than the conventional approach, vindicating the spacing between the devices operating in parallel. This approach yields an improvement in PAE by more than 20% points, while improving gain by more than 3 dB.

The analysis presented looks at thermal effects and performance degradation of an in-market amplifier for a pico-cell base-station application, and presents an approach meant to improve the in-market solution. To achieve this, the model's evaluation board circuit was accurately reconstructed for schematic and layout level simulations. A background on RF principles, such as biasing classes, and thermal concepts was presented to understand the impact design decisions play at high and low levels of a device's performance. For thermal integrity and RF power amplifier linearity, a class-AB amplifier is deemed most suitable and subsequently implemented in the analysis of the amplifiers presented in this thesis. The analysis concludes that the effects at device level of temperature impact the RF power and reliability of the device.

A more detailed thermal analysis was presented on a GaN FET that is biased at a similar class-AB point as the CGH25120F model. The in-depth thermal analysis of a GaN device has been

considered to be cutting edge and trend-setting as it gives designers the potential to understand internal thermal effects their design has on a DUT. Thermal studies are heavily driven by market requirements; as such, researchers have just scratched the surface of thermal analysis and impact on electrical devices.

A parallel architecture was presented as an improved solution that designers can potentially use to replace a single FET design approach, without altering the layout of the PCB or the biasing, save for the placement of the additional FET. The approach contends that the multiple devices used are sized appropriately to match the original sizing of the sole transistor. This allows for minimal impact to the design space, in accordance with stringent form factor requirements. Though the electro-thermal analysis of the original CGH25120F model would have offered a more direct comparison of performance, we can predict the internal degradation and output performance effectively with the approaches presented in this thesis. The approaches and analysis presented in this thesis satisfy the requirements of thermal relief in small form factors without compromising device performance.

6.2 Conclusion

The dual GaN FET design presented in this thesis has demonstrated the feasibility to achieve higher efficiency, gain, and power delivery than a standard one-cell device by virtue of improvement in thermal performance at gate level. It presents evidence that suggest and validate the notion of gate separation improving temperature performance, thus optimizing the design without affecting the design space or form factor. Furthermore, it proves the solution to be an extremely simple substitute that does not need modification to impedance matching or bias circuitry. The most significant contribution is the characterization of thermal behavior on an emerging technology like GaN, and the design approach to offer improvements in reliability and RF performance.

6.3 Future Work

As mentioned, researchers are only scratching the surface on the thermal impacts, and effects of temperature on a variety of market technologies. With ground breaking tools available, it is important to go even further into the distribution of heat and power in a parallel architecture. Some recommendations include the following:

- Analyze the different input power levels and the cause of uneven distribution, as mentioned in analysis of the quad FET approach. This approach can be further optimized with such research.
- Efficiency enhancement techniques exist in the market today, and the thermal impact of these techniques should also be characterized at device level.
- Further research to understand phenomena such as trapping effects should be carried out, as there isn't too much conclusive evidence to suggest the effects of temperature on trapping effects, and vice versa.
- With regards to the CGH25120F, it would be valuable to analyze the evaluation board under a thermal camera to locate heat spots and identify potential areas for further analysis, and then to compare with the electro-thermal simulations.
- A parallel FET architecture should also be analyzed under a thermal camera to further correlate the impact of thermal relief on the surrounding system.
- Analyze a Doherty amplifier for thermal performance and compare with the dual FET approach presented in this thesis.

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Appendix

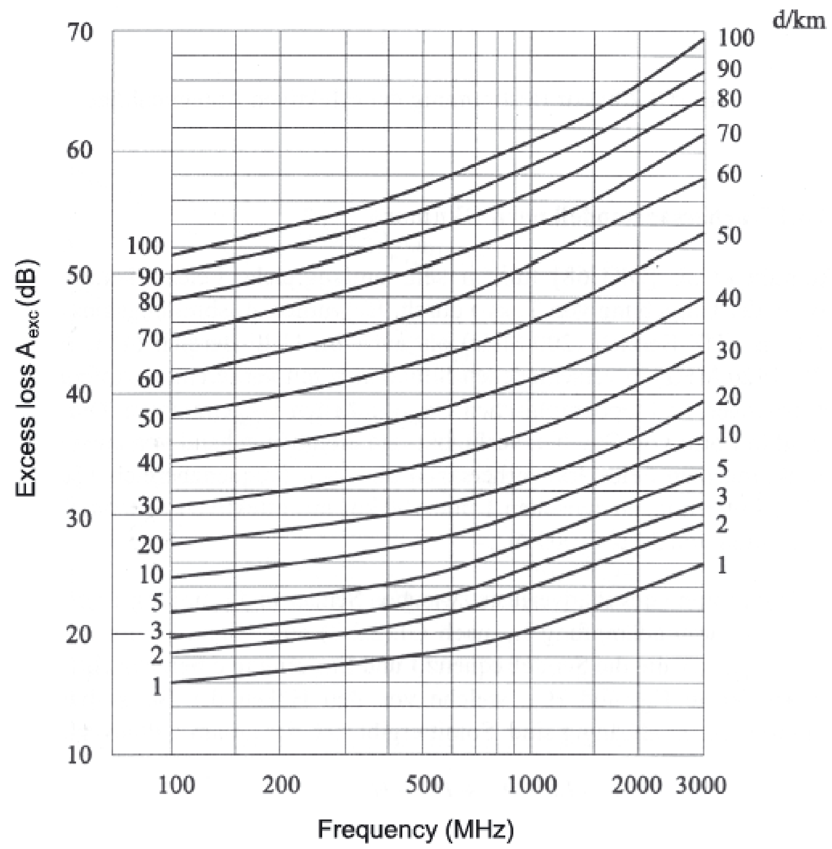

Figure 60: Okumara-Hata Path Loss Curves

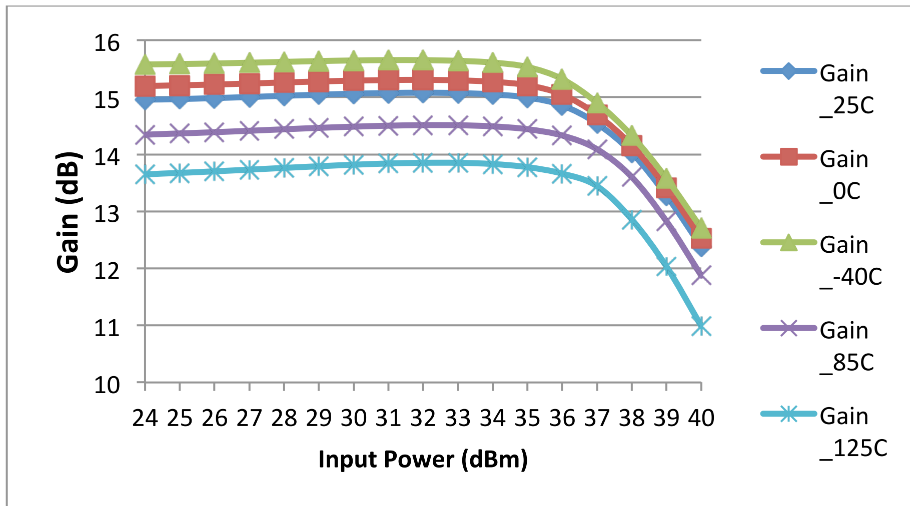

Figure 61: Gain over temperature and input power

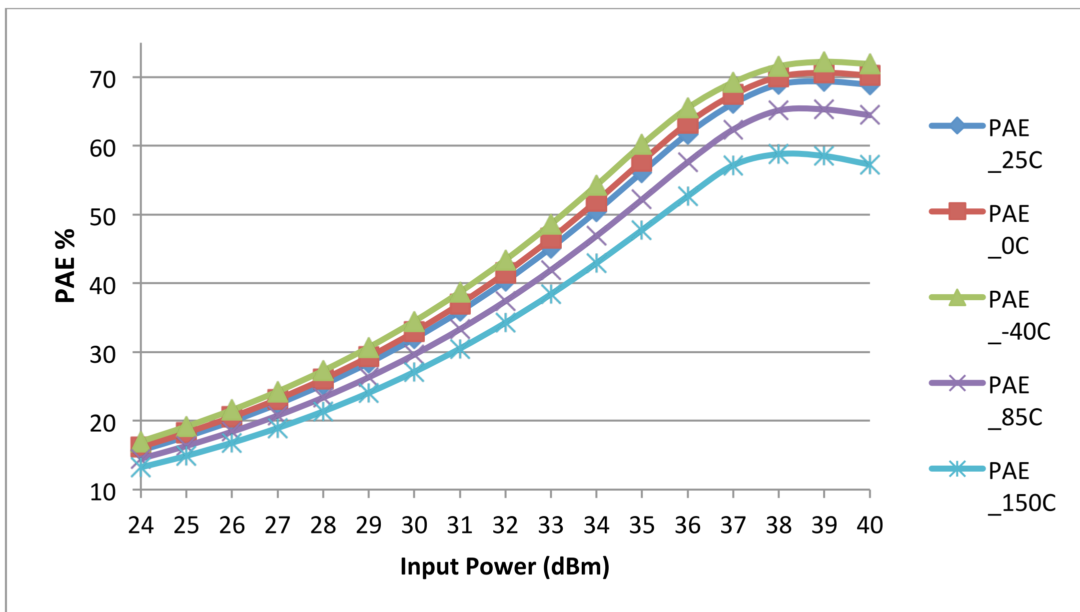

Figure 62: PAE over temperature and input power

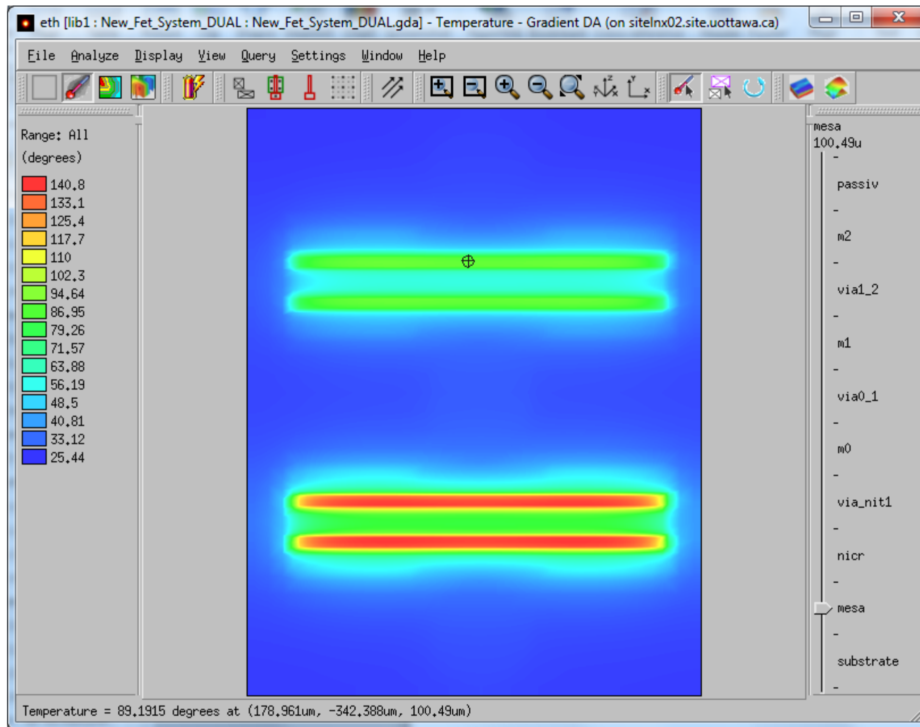

Figure 63: Thermal profile at a single operating point, showing uneven distribution of heat in a dual FET configuration

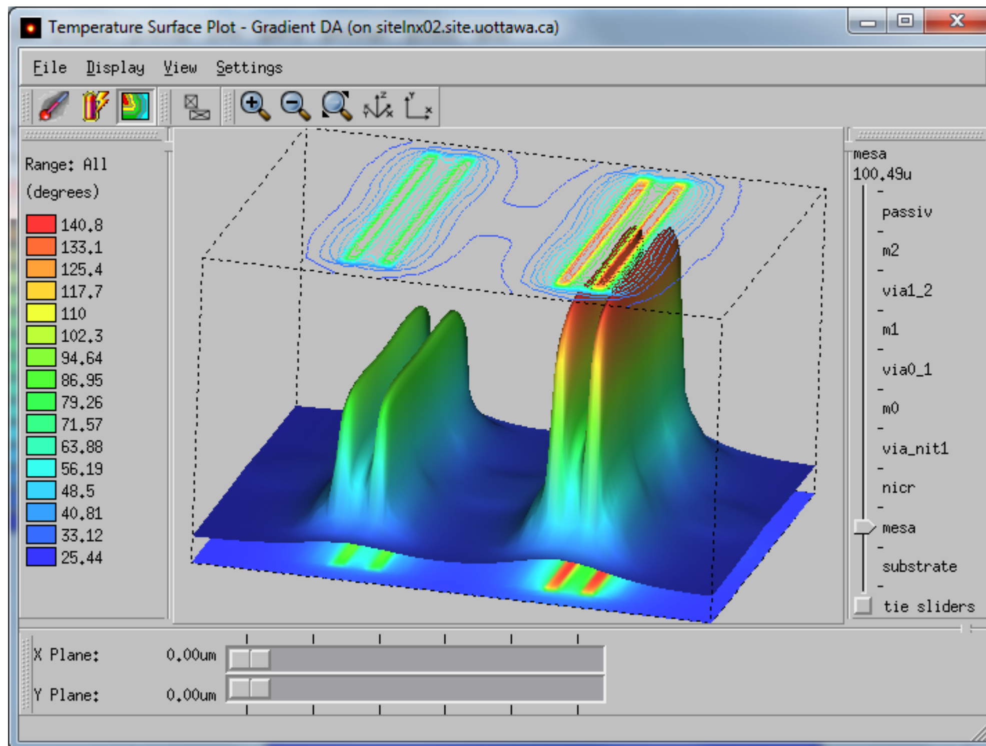

Figure 64: Contour curves of an uneven distribution in a duel FET design

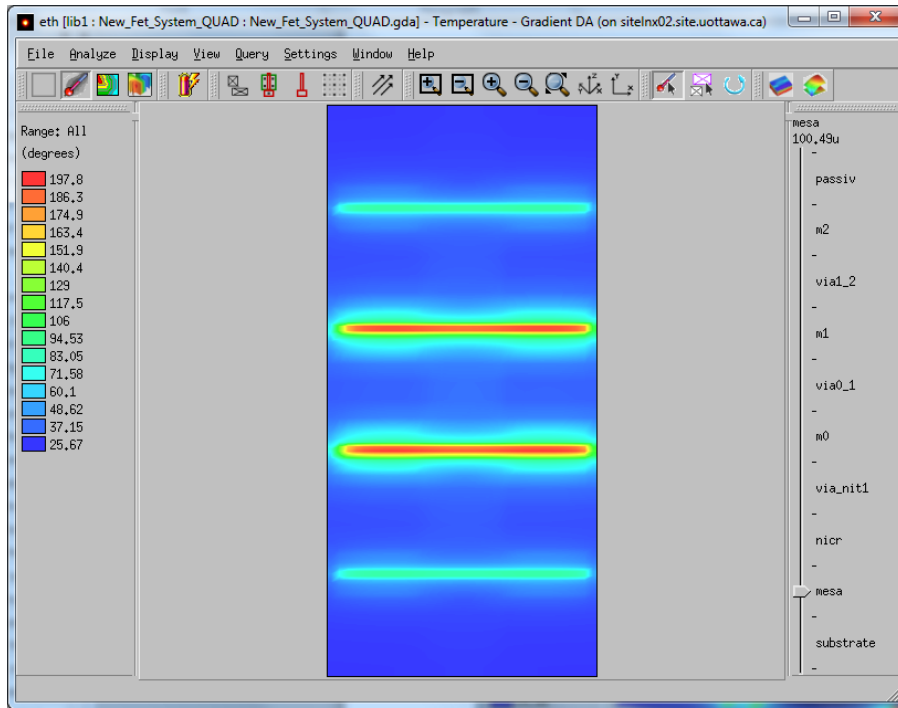

Figure 65: Improvement in distribution of heat and power after biasing is adjusted

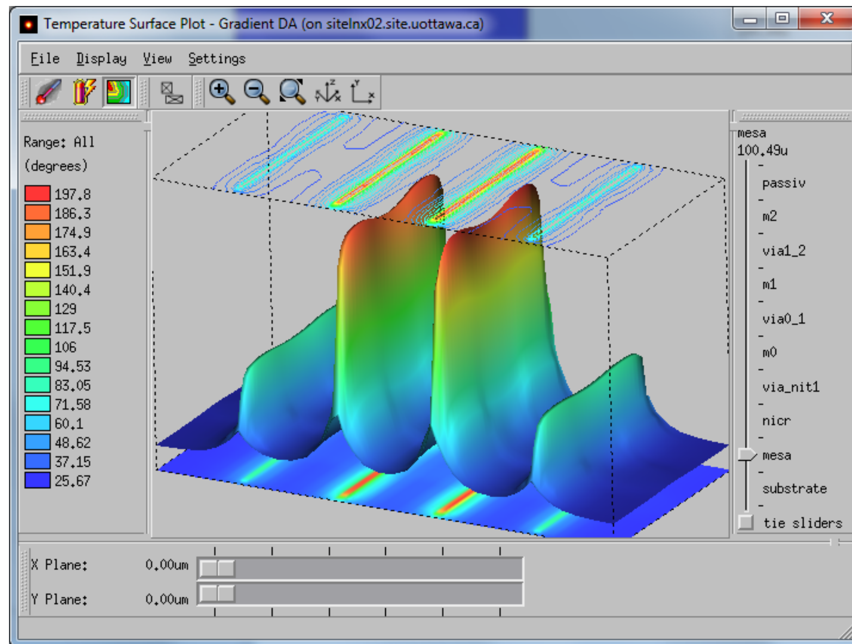

Figure 66: Contour curves further illustrate the improvement in biasing