A Non-Quadrature Vector Modulator Approach for Wideband Phased Array Systems

by

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Declaration of Authorship

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Abstract

Phased array systems are widely used in wireless/satellite communication, as well as radar systems, to improve data rate, Signal-to-Interference Ratio (SIR), and Signal-to-Noise Ratio (SNR), thereby enhancing the system's Quality of Service (QoS). RF phase shifters are essential to the operation of phased array systems. The production of phase array components, including antennas, is relatively cost-effective thanks to the advancement of printing manufacturing technology. However, the design of cost-effective RF phase shifters remains challenging in implementing phased array beamformers. Additionally, new-generation telecommunication and radar systems often require stringent phase shifter performance metrics, such as phase resolution and bandwidth, to perform fine beam scanning, which helps increase pointing accuracy. Meanwhile, practical phase shifters display limited performance. On the one hand, On-chip passive phase shifters offer low power consumption and high linearity, but suffer from low resolution, large chip area, and high insertion loss. On the other hand, active phase shifters like vector modulators present relatively high gain at the expense of poor linearity, high power consumption, and relatively low resolution. To attain decent performance in phase precision, commercial phase shifters typically use the GaAs or GaN technology to achieve a 360º digital phase shift, which is costly. Additionally, most phase shifters have a fractional bandwidth below 25 %. This dissertation presents a comparative study and classification of state-of-the-art phase shifter designs and investigates the noise and linearity of vector modulator phase shifters. Then, a novel vector modulator phase shifter approach is proposed for the first time to address the phase resolution limitation, high power consumption and narrow bandwidth issues of state-of-the-art phase shifters.

The proposed vector modulator is based on the generation and subtraction of two unbalanced non-quadrature vectors to produce a 360º analog phase range. A PCB prototype designed at 5 GHz center frequency generates more than 360º continuous phase range with a fractional bandwidth greater than 50%. Moreover, an RF module, comprising input and output Single-Pole Double-Throw (SPDT) switches and the proposed vector modulator with amplification, was designed and laid out in the 130 nm BiCMOS technology for phased array transceiver applications. From the results, the 2.66 mm^2 RF module exhibits a respective maximum gain and minimum isolation of 3.3 dB and 49.8 dB from 6.4 GHz to 13 GHz. In addition, an input 1-dB compression power and third-order intercept point (IP3) of 3.78 dBm and 9.1 dBm, respectively, were obtained at the center frequency. Furthermore, the novel X-band non-quadrature

vector modulator generates a phase range of more than 360º with a 68% fractional bandwidth, while consuming 18.9 mW of DC power and occupying an area of 1.6 mm^2.

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List of Acronyms

AC	Alternative Current
ADC	Analog-to-Digital Converter
ADS	Advanced Design System
AF	Array Factor
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
BJT	Bipolar Junction Transistor
BM	Biphase Modulator
BST	Barium Strontium Titanate
BW	Bandwidth
CMOS	Complementary Metal-Oxide Semiconductor
CPW	Coplanar Waveguide
CS	Common-Source
DAC	Digital-to-Analog Converter
DC	Direct Current
DMTL	Distributed Micro-Electromechanical Systems Transmission Line
DPDT	Double-Pole Double Throw
DSP	Digital Signal Processing
EM	Electromagnetic
ESD	Electrostatic Discharge
FBW	Fractional Bandwidth
FET	Field-Effect Transistor
FM	Ferromagnetic
GGW	Groove Gap Waveguide
GW	Gap Waveguide

HLPPS	High/Low Pass Phase Shifter
HP	Half-Power Beamwidth
HPF	High Pass Filter
HTS	High-Throughput Satellite
IC	Integrated Circuit
IF	Intermediate Frequency
IL	Insertion Loss
IM	Intermodulation
IM3	Third-Order Intermodulation Product
IIP3	Input Third-order Intercept Point
IP3	Third-order Intercept Point
IQ	In-Phase-Quadrature
L-C	Inductor-Capacitor
LC	Liquid Crystal
LLPS	Loaded-Line Phase Shifter
LM	Liquid Metal
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LTLPS	Loaded-Transmission Line Phase Shifter
MAM	Metal-Air-Metal
MEMS	Micro-Electromechanical System
MIM	Metal-Insulator-Metal
MIMO	Multiple-Input Multiple-Output
MMIC	Monolithic Microwave Integrated Circuit
MN	Matching Network

MOM	Metal-Oxide-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPAR	Multi-Purpose Phased Array Radar
NF	Noise Figure
NMOS	N Metal-Oxide-Semiconductor
NQ	Non-Quadrature
NQVSPS	Non-Quadrature Vector-Sum Phase Shifter
PA	Power Amplifier
PAR	Phased Array Radar
PAS	Phased Array System
PCB	Printed Circuit Board
PIVA	Phase-Invertible Variable Attenuator
PMOS	P Metal-Oxide-Semiconductor
PN	Phase Noise
PPF	Polyphase Filter
PSN	Phase Shifter Network
Q-factor	Quality factor
QAF	Quadrature All-Pass Filter
QAM	Quadrature Amplitude Modulation
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
R-C	Resistor-Capacitor
R-L-C	Resistor-Capacitor-Inductor
REV	Rotating-Element Electric Field Vector
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit

RGW	Ridge Gap Waveguide
RMS	Root Mean Square
RTPS	Reflective-Type Phase Shifter
RTTLPS	Reflective-Type Transmission Line Phase Shifter
Rx	Receive
SAR	Synthetic Aperture Radar
SATCOM	Satellite Communications
SFPS	Switched-Filters Phase Shifter
SIR	Signal-to-Interference Ratio
SIW	Substrate-Integrated Waveguide
SLPS	Switched-Line Phase Shifter
SNR	Signal-to-Noise Ratio
SOI	System-on-Insulator
SOTM	Satellite-on-the-Move
SPDT	Single-Pole Double-Throw
STPS	Switched-Type Phase Shifter
TL	Transmission Line
TSMC	Taiwan Semiconductor Manufacturing Company
Tx	Transmit
UWB	Ultra-Wideband
VGA	Variable-Gain Amplifier
VNA	Vector Network Analyzer
VSPS	Vector-Sum Phase Shifter
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network

List of Symbols

A_O	Amplitude of output signal
A_{IIP3}	Voltage peak of third-order intercept point
$A_{in,1dB}$	Input voltage peak 1-dB compression point
A_{nI}	Noise amplitude of I-signal
A_{nQ}	Noise amplitude of Q-signal
$A_{out,noisy}$	Noise amplitude of output signal
dBV	Decibel-Volt
F_I	Noise factor of I-branch
F_Q	Noise factor of Q-branch
G_V	Voltage gain of system
G_{VI}	Voltage gain of I-branch
G_{VQ}	Voltage gain of Q-branch
GaAs	Gallium Arsenide
GaN	Gallium Nitride
I_D	Drain current
IIP3	Input third-order intercept point
J_{RMS}	Root mean square jitter
NF	Noise Figure
OIP3	Output third-order intercept point
P_{1dB}	1-dB compression point
R_{in}	Input resistance
R_{ON}	ON resistance
R_L	Load resistance
R_S	Source resistance

$\boldsymbol{SiGe}$	Silicon-Germanium
$\boldsymbol{V_{Ctrl}}$	Control voltage
$\boldsymbol{V_{DD}}$	Drain supply voltage
$\boldsymbol{V_{DS}}$	Drain-source voltage
$\boldsymbol{V_G}$	Gate voltage
$\boldsymbol{V_{GS}}$	Gate-source voltage
$\boldsymbol{V_L}$	Load voltage
$\boldsymbol{\overline{V_n^2}}$	Total noise voltage squared
$\boldsymbol{\overline{V_{nI}^2}}$	Noise voltage squared of the I-branch
$\boldsymbol{\overline{V_{nQ}^2}}$	Noise voltage squared of the Q-branch
$\boldsymbol{V_{OV}}$	Overdrive voltage
$\boldsymbol{V_{TH}}$	Threshold voltage
$\boldsymbol{Z_L}$	Load impedance
$\boldsymbol{Z_T}$	Tail impedance
$\boldsymbol{\varepsilon_G}$	Gain error
$\boldsymbol{\varepsilon_\varphi}$	Phase error
$\boldsymbol{\varphi}$	Phase shift
$\boldsymbol{\varphi_O}$	Output phase
$\boldsymbol{\varphi_{ref}}$	Reference phase shift
$\boldsymbol{\varphi_{resol}}$	Phase resolution

Chapter 1

Introduction

1.1 Background and Motivations

Antenna array systems have been widely used since 1926, with the introduction of the Yagi-Uda antenna [1], followed by other constant-phase mechanically-steered array systems. Phased array systems were first introduced during World War II with mechanical phase shifters. The invention of ferrite phase shifters in the 1950s allowed the application of antenna array systems in electronic scanning. From the 1960s onward, phased array systems became more compact and relatively cost-effective thanks to advancements in the development and manufacturing of both antenna array elements and solid-state phase shifters. The recent introduction of active array systems permits simultaneous use of transmit and receive branches with phase and gain adjustment, which is referred to as phased array transceivers. In this regard, phased array systems find their applications from radio communications, aircraft, and weather monitoring like the one in Figure 1.1, which is a Multi-function Phased Array Radar (MPAR) for aircraft tracking, weather monitoring, and wind profiling [2].

1.1.1. Operating Principles of Antenna Array Systems

The operating principle of a typical Transmit (Tx) or Receive (Rx) Phased Array System (PAS) is depicted in Figure 1.2. The radiation pattern of the N-element antenna array is customized for scanning in space and achieving optimum directivity through phase and amplitude variations, or tapering of individual antenna elements. Assuming N identical antenna elements, the array model is composed of two distinct parameters: the element pattern, which is the pattern of a single antenna, and the Array Factor (AF), which corresponds to the pattern of the array system with the antenna replaced by isotropic elements. Therefore, the total pattern is the product of the element pattern with the array factor. Here, we are mostly interested in the array factor and its effect on the total pattern, as it helps indicate the optimum angle for maximum signal transmission or reception. For a uniform excitation, the current of the n^{th} antenna element can be written in phasor format as [3]:

$$I_n = A_n e^{j\Psi(n)} \tag{1-1}$$

Figure 1.1: Phased array radar for aircraft and weather monitoring [2]

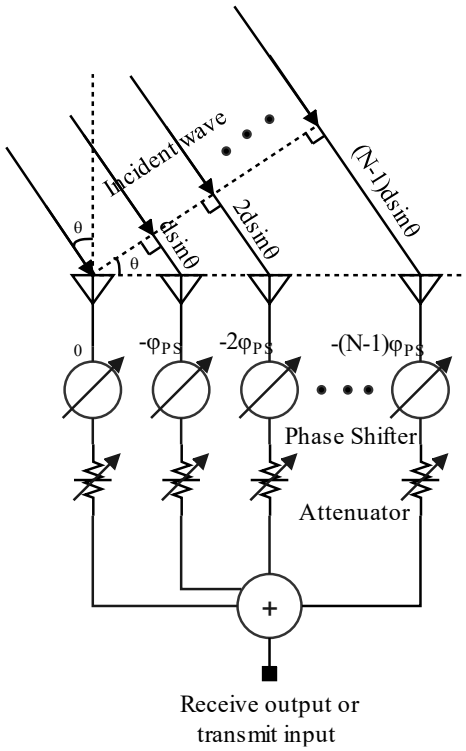


Figure 1.2: Phased-array system with N antenna elements.

Here, Ψ(n) is the total excitation current phase of the n^{th} antenna. It is composed of the phase produced by the blocks preceding the phase shifter, such as the attenuator and the power divider, and the phase shift provided by the phase shifter. Ideally, the phase produced by the attenuator and the splitter must be constant on all branches of the array at all phase shift conditions, to avoid any error. For simplicity, we can assume that the total phase shift of the blocks preceding the phase shifter is zero on all

branches. In this case, Ψ(n) is the phase produced by the phase shifter on the nth antenna element. By providing a tapering of the excitation current through phase shifters, Ψ(n) can be written as:

$$\Psi(n) = (n-1)\varphi_{PS} \tag{1-2}$$

where φ_{PS} is a constant phase shift between two adjacent antenna elements.

If a wave is incident on the antenna array at an angle θ with respect to the plane normal to the antenna surface, as seen in Figure 1.2, each individual antenna receives the signal at a different phase or time delay. The phase of the incident wave on the nth antenna is a function of the distance separating consecutive antennas, d, and the signal wavelength λ. It can be written as:

$$\varphi_{space}(n) = -(n-1)\frac{2\pi}{\lambda} d \sin\theta \tag{1-3}$$

Hence, the current of the nth antenna element after an incident wave at the receiver mode becomes:

$$I'_n = A_n e^{j\left[-(n-1)\frac{2\pi}{\lambda} d \sin\theta + \Psi(n)\right]} = A_n e^{j(n-1)\left[-\frac{2\pi}{\lambda} d \sin\theta + \varphi_{PS}\right]} \tag{1-4}$$

With no amplitude tapering of the current, $A_n = A_0$. Using the current expression in (1-4), the array factor of the N-element system is therefore found as [3]:

$$AF = A_0 \sum_{n=1}^{N} e^{j(n-1)\left[-\frac{2\pi}{\lambda} d \sin\theta + \varphi_{PS}\right]} = A_0 \frac{\sin\left[(N/2)\left(-\frac{2\pi}{\lambda} d \sin\theta + \varphi_{PS}\right)\right]}{\sin\left[(1/2)\left(-\frac{2\pi}{\lambda} d \sin\theta + \varphi_{PS}\right)\right]} \tag{1-5}$$

By setting $\varphi_{PS} = \frac{2\pi}{\lambda} d \sin\theta$, the AF is maximized as $AF_{max} = NA_0$. Therefore, the signals are added constructively at the incident angle θ and rejected at other directions for the receive mode. The same concept applies at the transmit mode, where the transmitted signal is maximized in amplitude when $\varphi_{PS} = \frac{2\pi}{\lambda} d \sin\theta$. In other words, the phased array beamformer performs a spatial signal combining in order to compensate for the time difference of the departure from (or the arrival at) the antennas. The AF equation in (1-5) can be normalized as:

$$f = \frac{AF}{AF_{max}} = \frac{1}{N} \frac{\sin\left[(N/2)\left(-\frac{2\pi}{\lambda} d \sin\theta + \varphi_{PS}\right)\right]}{\sin\left[(1/2)\left(-\frac{2\pi}{\lambda} d \sin\theta + \varphi_{PS}\right)\right]} \tag{1-6}$$

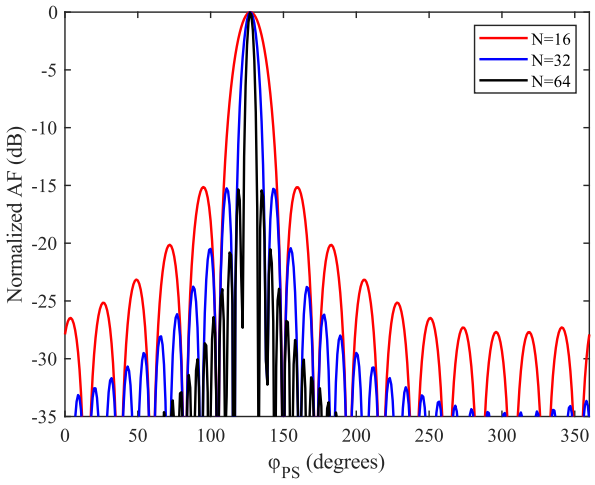


Figure 1.3: Plot of normalized AF with respect to the phase of the phase shifter of an N-element (N=16, 32 and 64) array system for an incident wave at $\theta = 45°$.
The maximum directivity occurs at $\varphi_{PS} = \frac{2\pi}{\lambda} d \sin\theta = 127.279°$

Figure 1.3 displays the plots of the normalized AF in dB with respect to the phase difference between two consecutive phase shifters (φ_{PS}) for N = 16, 32, and 64. The array element separation distance is set to d=λ/2, and the angle of incidence of the incoming or outgoing wave is assumed to be θ = 45°. We can clearly observe that the AF is maximized at $\varphi_{PS} = \frac{2\pi}{\lambda} d \sin\theta = 127.279°$. Additionally, the half-power beamwidths (HP) for near broadside and end-fire of a uniformly excited linear antenna array are respectively expressed as [3]:

$$HP_{broadside} \approx 0.886 \frac{\lambda}{Nd} \csc\theta_0 \tag{1-7}$$

$$HP_{endfire} \approx 2\sqrt{0.886 \frac{\lambda}{Nd}} \tag{1-8}$$

where θ_0 and d are, respectively, the pointing angle of the main beam and the distance between consecutive array elements. From (1.7) and (1.8), the beamwidth of the array elements becomes narrower as N increases, allowing better out-of-beam signal rejection. However, larger array systems consume more power and occupy more area. Meanwhile, the sidelobes may be reduced by using amplitude tapering [3] with the help of attenuators or Variable-Gain Amplifiers (VGAs).

Moreover, the noise generated by the receive channels is incoherently added, whereas the antenna gain increases substantially, resulting in a Signal-to-Noise Ratio (SNR) improvement by N, and therefore improving the overall channel capacity [4]. The spatial coherent combining of the transmit channels' signals leads to an overall power efficiency improvement at the transmitter side.

1.1.2. Applications of Phased Array Systems

One of the primary benefits of using phased array antennas for wireless data transmission and reception is the increase in speed. By carefully controlling the phase of the signals emitted by each element in the array, it is possible to create a beam of electromagnetic energy that can be steered with great precision. This allows for much higher data rates than would be possible with a traditional omnidirectional antenna, as the focus of the beam can be directed very precisely at a specific target. In addition, phased array antennas can also be used to null out interfering signals. It is possible to cancel out unwanted signals through phase shifters in an array system, such as those from nearby cell towers or other sources of interference. This allows for much higher data rates and improved Quality of Service (QoS). Phased array systems have a wide range of applications for both military and civilian purposes. The most prominent applications include Satellite Communications (SATCOM), wireless data communications, and radar systems.

1.1.2.1 Satellite Communications

There is currently active research for developing high data throughput and low-latency broadband satellite communication systems. Broadcasting satellite systems, whereby programs are transmitted simultaneously to multiple terrestrial stations, are becoming obsolete with the development of High-Throughput Satellite (HTS) systems [5]. Providing broadband connectivity services in remote areas is currently one of the main targets of these satellite systems. Starlink is an internet network that provides such a service [6]. Other applications of HTS systems include providing broadband services for commercial cruises and military applications. Low-cost phase-array systems are crucial for the development of HTS systems [7]. Phased-array beamformers allow the ground-based Satellite-On-The-Move (SOTM) systems to point their beam to the stationary or non-stationary satellites.

1.1.2.2 Wireless Communications

As stated before, the use of phased array systems in data communication allows higher signal transmission area coverage and interference cancellation. The Wireless Wide Area Network (WWAN) and the Wireless Local Area Network (WLAN) communications systems exploit these advantages in their smart base stations. The fourth Generation (4G) cellular network smartphones incorporate a linear phased array to provide more efficient voice and data communication. However, their band shortage caused the deployment of the fifth-Generation (5G) communication systems, which use higher frequency bands (e.g., 27.5-28.35 GHz) and massive Multiple-Input-Multiple-Output (MIMO) schemes to increase the signal

data rate 1000 times faster than the 4G networks. In this regard, a minimum of 6 antenna elements are integrated in the 5G mobile terminal in order to provide better signal diversity and multiplexing gain [8]. To achieve the high data transmission speed and channel capacity requirements of the 5G, low-cost phased array systems are needed to move from the 4G MIMO [9] effectively.

1.1.2.3 Radar Systems

Phased Array Radars (PARs) are used for object detection, identification, and localization alongside other methods, including mechanical tracking and electromagnetic fence [10]. They can perform multi-object search, tracking, acquisition, identification, guiding, and control, simultaneously from various heights and directions. This is done through the control and regulation of the main lobe of the beam formed by the antenna elements while suppressing the side lobes. The quick scanning capability of these radars allows for a fast response. Moreover, the ability of the radar to operate with reasonable performance in the event of the damage of one or more array elements makes them reliable. In this regard, phased-array radars find their application in defence, space surveillance, and search & rescue.

Moreover, phased-array radars are applied in geoscience and astronomy with the use of Synthetic Aperture Radars (SARs). Modern SARs employ phased array antenna systems to scan parts of the earth and, therefore, produce images electronically. SAR radars send an electromagnetic (EM) wave with a certain energy to an object, capturing and processing the energy of the reflected wave (echo) to produce a picture of the object similar to optical imaging. Unlike optical imaging systems, SAR radars can operate in any weather conditions or at any time of the day. Phased array SAR radars produced higher resolution images than single-antenna SAR radars [11]. In addition, single-antenna airborne SARs can not detect moving objects like cars, as they will be suppressed during the clutter removal process in the signal processing. Therefore, a multichannel phased array antenna system pointing toward the object must detect moving objects.

Furthermore, there has been growing interest in phased array radars for weather surveillance and air traffic monitoring for the past decades. Aviation is one important area where weather surveillance continuously updates pilots and air traffic agents on severe weather conditions such as tornadoes. Traditional weather control radars perform mechanical 3-dimensional (3D) steering to provide updates on the weather. Nevertheless, mechanical 3D scanning proves to be relatively slow. For instance, the WSR-88D, a weather surveillance system developed in the USA, requires five minutes to complete a full 360˚ mechanical scanning [12]. This scanning time is slow for continuous updates on weather phenomena such as tornadoes. PARs, on the other hand, can perform full electronic scanning in less than one minute.

Besides, aviation radars typically use thousands of radars to monitor air traffic and weather conditions independently. MPARs are currently being developed to monitor both the weather and aircraft, thus providing a cost-effective solution to the radar systems for aviation control.

1.1.3. Motivations

Due to their numerous applications and distinct advantages, such as higher SNR/SIR and faster scanning speed compared to mechanically-steered systems, phased array antenna systems continue to be critical for current and future generations of wireless systems, such as the 5G systems and beyond. Meanwhile, RF phase shifters are essential to the functioning of phased array systems. As described in Section 1.1.1, phase shifters are used to maximize the signal transmission or reception gain in a specific scanning angle while rejecting the signals at other angles. Early phase shifters used mechanical and ferromagnetic/magnetic tuning mechanisms for beam steering purposes [13], [14]. Nevertheless, these phase shifters had relatively lower scanning speeds and, more importantly, were bulky and often required the exertion of a high voltage for phase tuning. Most recent phase shifter designs use the semiconductor [15], MEMS [16], Liquid Crystal (LC) [17] and Liquid Metal (LM) [18] technologies to achieve decent phase shifting performance with reduced size and power consumption. However, MEMS devices inherently face reliability issues due to their brittleness and temperature effects [16], while the LC and LM technologies are relatively new in phase shifter design applications. Therefore, even if they offer promising advantages in terms of high-frequency capability, more profound research is needed for the miniaturization of the relatively large LC devices and to address the containment issues of the LM material at high frequencies [17], [19]. Besides, it is challenging to integrate the LC and LM devices into the semiconductor technology, which offers the batch production advantage. In this regard, electronic phase shifters using semiconductor technologies remain the most preferred in antenna array applications. As electronic circuits are moving towards higher operating frequencies to fulfill the bandwidth demand of billions of connected devices, the electronic phase shifter must be able to provide acceptable performance at these frequencies. The vast majority of commercial electronic phase shifters operating at X-band and above employ III-V semiconductors such as GaN, which are costly. Meanwhile, the cost-effective silicon technology presents higher loss generation as its main disadvantage. Active phase shifters such as the vector modulators, offer relatively higher gain and smaller size at high frequencies compared to their passive counterparts, such as the switched and reflective types, rendering them increasingly attractive for mm-wave frequency applications. In contrast, state-of-the-art vector modulators exhibit limited phase resolutions and relatively higher power consumption. In this regard, this dissertation aims to provide an alternative approach to designing a vector modulator phase shifter with high phase resolution and low loss

using cost-effective technologies such as the CMOS process. In addition, the linearity and noise aspects of vector modulators are mostly uncovered in the literature. The presence of nonlinear blocks, such as the Variable-Gain Amplifier (VGA), can affect the overall performance of the modulator in terms of phase precision and signal fidelity. Similarly, the effect of noisy constituent blocks of the modulator may undermine the ability of a phased array receiver to recover the captured signals. Since vector modulators are becoming increasingly popular for mm-wave antenna array systems, this work aims to provide a generalized study on the effects of noisy and nonlinear building blocks of a vector modulator in an effort to cover the research gap in this area.

1.2 Thesis Contributions

The cost of a phased array transmitter/receiver is mainly dictated by that of the Phase Shifter Network (PSN), which counts for about 50 % of the total cost [20]. This thesis emphasizes a novel approach to designing vector modulators for low-cost phase shifter solutions. The proposed method aims to reduce the power and area consumption of electronic phase shifters while providing a continuous 360˚ phase range in the CMOS process. To this end, the following contributions were achieved:

- A novel vector modulator based on non-quadrature vector operations was proposed. Referred to as Non-Quadrature Vector-Sum Phase Shifter (NQVSPS), the novelty in the designed vector modulator lies in generating and synthesizing two non-differential signals with a phase difference of less than 90˚, thereby reducing the chip area and DC power consumption of the phase shifter. Traditional Vector-Sum Phase Shifters (VSPSs) employ balanced quadrature vector operations to perform phase shifting, which is less power- and area-effective compared to the proposed NQVSPS.
- A novel approach to suppressing phase gaps, which limit the resolution of vector-sum phase shifters, was proposed to achieve analog phase shifting.
- A thorough study of the effects of nonlinear and noisy blocks in vector modulators, which has not been covered in the literature.
- A novel phase variation reduction technique was proposed for overall bandwidth improvement. The novelty consists of using the slow-wave properties of open- and shorted-stubs in transmission line phase-shifting structures for phase compensation.
- A novel wideband microstrip-based analog subtractor with low amplitude and phase variation was designed and implemented. The novelty emanates from the use of T-stubs to generate slow-wave transmission effects.

- A new RF wideband active balun was designed as part of the vector synthesizer to boost the system gain. The novelty of the proposed balun is based on current subtraction with inductive degeneration for phase compensation.
- Wideband Single-Pole Double-Throw (SPDT) and Double-Pole Double-Throw (DPDT) with improved isolation were implemented. The isolation was improved by a synchronized switching circuit.

1.3 Thesis Outline

After the introductory chapter, this thesis is organized as follows:

Chapter 2 provides the principle of operation and a review of different types of RF phase shifters, along with a detailed and comparative study of the conventional phase shifters. This gives the reader an insight into the issues associated with conventional phase shifters and how some of these issues were addressed in the literature.

Chapter 3 presents a detailed study of the linearity and noise of vector modulators. The effects of nonlinear and noisy modulator building blocks are investigated with the support of simulation results.

Chapter 4 discusses the design of the proposed non-quadrature vector-sum phase shifter. Its working principle is described along with the reasoning behind the potential improvement factors. The design and measurement results of a PCB prototype are described in detail. The obtained results of the fabricated prototype are compared with the state-of-the-art relevant works.

Chapter 5 covers the design of an X-band RF module composed of the NQVSP and SPDT switches in the 130 nm CMOS Process. The design procedure of the module's constituent blocks is provided with the help of simulation results. The results of the proposed phase shifter are drawn and compared to state-of-the-art similar work. Lastly, the results of the overall system are summarized and commented.

Finally, Chapter 6 draws conclusions on the different studies performed in this thesis and discusses projected future work on the proposed vector modulator.

1.4 Publications

1. M. Kebe, M. C. E. Yagoub, and R. E. Amaya, "A Wideband Analog Vector Modulator Phase Shifter Based on Non-Quadrature Vector Operation," *Electronics*, vol. 14, no. 5, p. 997, 2025.

2. M. Kebe, M. C. E. Yagoub and R. E. Amaya, “A Survey of Phase Shifters for Microwave Phased Array Systems”, *Int. J. Circuit Theory Appl.*, Oct. 2024.
3. M. Kebe, R. E. Amaya, and M. C. E. Yagoub, “A 2.2-3 GHz Non-Quadrature Vector-Sum Phase Shifter with Low-Phase Error and Based on Coarse-Fine Tuning”, *Microw. Opt. Technol. Lett. vol.* 67, no. 1, Jan. 2025.
4. M. Kebe, S. Abdullah, R. E. Amaya, and M. C. E. Yagoub, “Architecture and Design of a New Non-Quadrature Vector-Sum Microwave Phase Shifter at 10 GHz With Maximum Residual Phase Error of 1.80°”, in *2023 Int. Conf. Elect., Comput. Communication Eng. (ECCE)*, Chittagong, Bangladesh, Feb. 23–25, 2023. IEEE, 2023.

Chapter 2

An Overview of Phased Array Transceivers and RF Phase Shifters

2.1 Introduction

2.1.1 Phased Array Transceiver Configurations

A phased array transmitter/receiver has three different signal paths based on the frequency level: the Radio Frequency (RF) signal, the Local Oscillator (LO) signal, and the Intermediate Frequency (IF) signal. The delay compensation can be performed on the RF, LO, or IF path. Therefore, the phased array system can be based on RF, LO, or IF phase shifting, as seen in Figure 2.1. Figure 2.1(a) represents a phased array receiver with RF phase shifting. In this configuration, the phase shifters are placed along the RF signal paths before the Low-Noise Amplifier (LNA) and antenna. Thus, the spatial delays of the signals are corrected in the RF domain. The RF phase shift architecture is the most popular in the phased array system design for a few reasons [21]. One advantage of the RF phase shifting is its high Signal-to-Interference-Ratio (SIR). The RF phase shift receiver has the ability to eradicate any interference that does not fall in the receiver beam angle before demodulation, therefore alleviating the linearity and dynamic range requirements of the down-conversion mixer. In addition, the RF phase shift architecture does not require an LO distribution network, unlike its LO and IF architecture counterparts. The LO distribution network augments the complexity of the system as the number of array elements increases. On the other hand, the LO and IF phase shift architectures do not require phase shifters in the RF domain, as seen in Figures 2.1(b) and (c), respectively. The RF phase shifters often exhibit high non-linearity and generate high loss and noise. Therefore, the LO and IF phase shift architectures typically exhibit better linearity and noise figures than the RF phase shift architecture [21]. Aversely, the need for an LO distribution network, along with the need to cancel the interference after demodulation, makes the IF and LO architectures more complex with increased dynamic range. In addition, the size of the phase shifter in the IF phase shift architecture is relatively larger due to its lower frequency. Moreover, phase shifting may be performed during the Digital Signal Processing (DSP) in a phased array system. This type of system is called the digital baseband phase shift architecture and is conceptualized in Figure 2.1(d). The main advantage of this architecture is the ability to process a wide variety of signals, including modulated

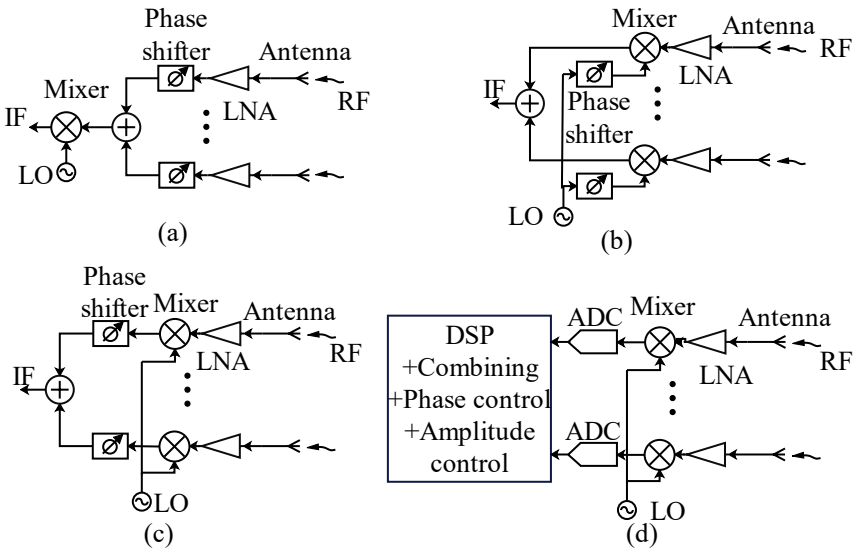


Figure 2.1: Architectures of phased array receiver systems: (a) RF phase shift, (b) LO phase shift, (c) IF phase shift, and (d) baseband phase shift.

signals. Similar to the LO and IF phase shift architectures, it requires highly linear and wide dynamic range down conversion mixers to accommodate the interferences. In addition, the dynamic range of the Analog-to-Digital Converter (ADC) must also be high, along with the large processing power of the digital processor, rendering this architecture unattractive [21]. The remaining sections will be focused on the RF phase shift architecture, as it remains the most popular due to previously stated advantages.

An RF phase shift phased array transmitter/receiver system can be divided into two main parts, namely the antenna array and the beamformer circuitry. An antenna array typically consists of several antenna elements separated by a fixed distance to maximize the directivity of the overall beam. The design and production of antenna arrays are relatively cost-effective thanks to techniques such as additive manufacturing [22]. On the other hand, the beamformer circuit is generally composed of a phase shifter, a gain tuning unit, which can be either an attenuator or a VGA, a power splitter/combiner and Single-Pole Double-Throw (SPDT) switches, as seen in Figure 1.2. The gain tuning unit is used to taper the signal amplitude in order to reduce the side lobe levels as well as to compensate for the gain imbalance resulting from phase shifting. The power splitter/combiner splits the signal power into multiple branches at the transmitter path and combines the signals from individual elements at the receiver path. The SPDT switches are used to switch between the receiver and transmitter paths. Many modern phase array systems incorporate transmit and receive paths on the same module. This is referred to as the phased array transceiver and can share one or more building blocks between the transmit and receive paths. In this regard, three RF phase shift transceiver configurations exist in the literature, as seen in Figure 2.2 [22]. In the configuration of Figure 2.2(a), only the antenna is shared by the Tx and Rx paths. It provides high

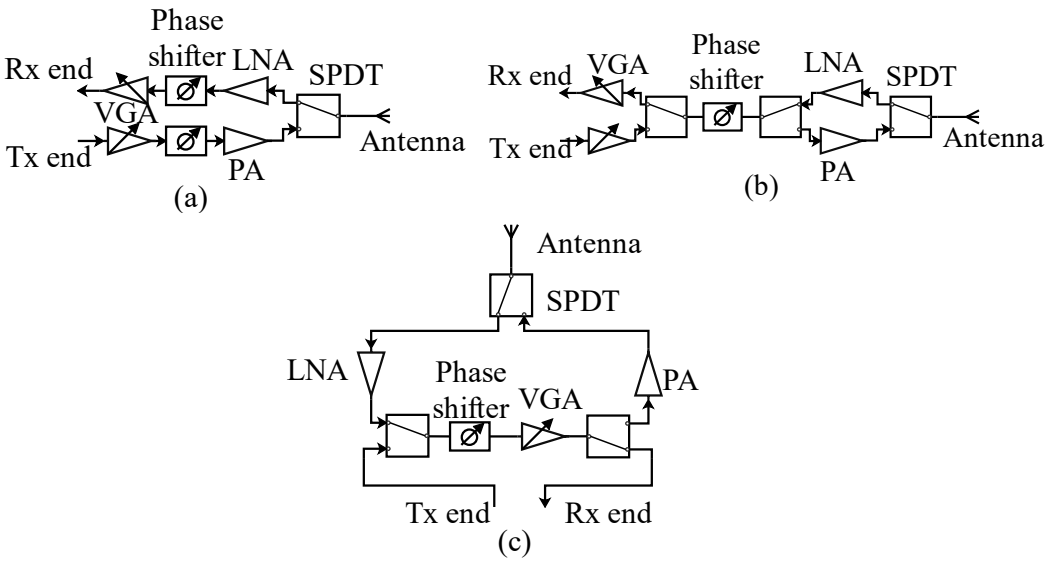


Figure 2.2: Configurations of phased array transceivers: (a) shared antenna, (b) shared antenna and phase shifter, and (c) shared antenna, phase shifter and VGA.

Tx/Rx gain and better control of the paths. In contrast, the power and area consumption are high. The configuration in Figure 2.2(b) is less area-consuming since the phase shifter is common to the two paths besides the antenna. Nevertheless, the SPDT switches must have high isolation to avoid coupling between the Tx and Rx and, hence, maintain system stability. Moreover, the system provides relatively less Tx/Rx gain as the SPDT switches generate a loss, especially at Ka-band and beyond. The block diagram in Figure 2.2(c) may be adopted to minimize power and area consumption, where the two paths share the phase shifter and VGA. This configuration is also suitable for the non-reciprocal phase shifters, such as the most active ones [21]. Even though the RF phase shift configurations remain the most frequent ones in the phased array system design, their performance and cost are mainly dictated by those of the phase shifter, which must have high linearity, low noise, high resolution, and low loss.

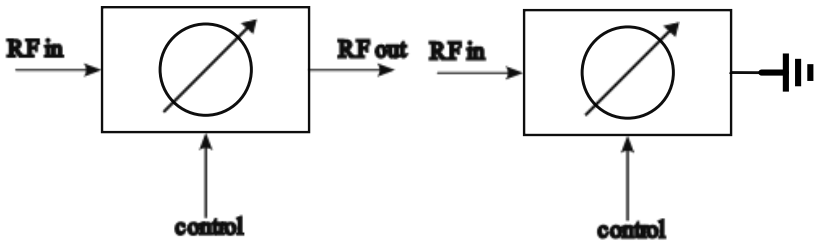
2.1.2 Principles of Phase Shifters

An RF phase shifter is an essential building block of a PAS, used to change the transmission phase of an input signal via a control element. This may be achieved through active or passive means. Hence, there exist passive and active phase shifters. Besides PASs, phase shifters are used in various applications, including electronic testing equipment such as signal generators [23], linearization of amplifiers [24], and image rejection receivers [25]. The primary purpose of a phase shifter is to change the phase of an incoming signal without modifying other parameters, such as gain and frequency.

In this regard, the scattering matrix of an ideal reciprocal phase shifter with φ phase shift is given as:

$$S = \begin{bmatrix} 0 & e^{j\varphi} \\ e^{j\varphi} & 0 \end{bmatrix} \tag{2-1}$$

The RF phase shifter is mostly used in transmission mode, implying a two-port network, as seen in Figure 2.3(a). It can also be used in reflection mode or as a one-port device (Figure 2.3(b)), where the ideal S-parameter is $S = S_{11} = e^{j\varphi}$.



(a) (b)

Figure 2.3: Phase shifters: (a) Transmission mode and (b) reflection mode

Even though ideal phase shifters only change the phase of the signal, practical RF phase shifters suffer from performance degradation. Several parameters determine the performance of an RF phase shifter, including the frequency capability/bandwidth, insertion loss, return loss, linearity, power handling, phase range/resolution, phase error, chip area, and power consumption [26].

a) **Frequency capability and bandwidth**: RF phase shifters are desired to operate at a center frequency (f_0) with a bandwidth $BW = f_H - f_L$, where f_H and f_L are the upper and lower cutoff frequencies, respectively. The bandwidth is often referred to as the 3-dB bandwidth. However, the bandwidth of practical RF phase shifters may refer to the range of frequencies where the reflection coefficients (S_{11}, S_{22}) are below -10 dB. The term fractional bandwidth, which is the percentage of the bandwidth with respect to the center frequency, is sometimes used as $FBW = \frac{f_0}{BW} \times 100$. It is often desired that the phase shifter operate at high frequencies with a large bandwidth. However, the design of high-frequency and large-bandwidth phase shifters is challenging due to the degradation in the quality factor and performance of passive and active elements at upper gigahertz frequencies.

b) Insertion loss: The insertion loss is the energy loss of the transmission mode RF phase shifter as the signal travels from the input to the output and is equivalent to the negative of S_{21} in decibels (dB): $IL = -20\log|S_{21}|$. The term gain is sometimes used in place of insertion loss and refers to the ratio of the amplitude of the output wave to that of the input wave. The isolation and insertion loss are equal for reciprocal devices, which are made of passive elements. Phase shifters are often required to achieve low insertion loss or high gain over the range of frequencies of interest. The variation of the gain over all phase states is termed the gain imbalance and must be as low as possible. Passive phase shifters produce more insertion loss than their active counterparts. Furthermore, the insertion loss of an RF phase shifter typically increases with frequency.

c) Return loss: The return loss measures the energy loss due to the reflection of an incoming signal at the input or output of the device. The input return loss is measured by S_{11} ($RL_{in} = -20\log|S_{11}|$), whereas the output return loss is measured by S_{22} in dB ($RL_{out} = -20\log|S_{22}|$). The term reflection coefficient (S_{11} or S_{22}) is often used to indicate the energy reflected from the phase shifter's input or output. RF phase shifters must maintain good input and output matching to ensure the maximum energy transfer.

d) Linearity: Linearity is an important parameter in the design of RF phase shifters. It is desired that the change in the output power level be constant with respect to the input power to avoid intermodulation effects and, thus, difficulties in signal demodulation at the receiver side. Like the amplifier, the linearity of an RF phase shifter is usually measured by its third-order intercept point (IP3). The IP3 is the intersection between the ideal linear response of the fundamental signal and its third-order intermodulation (IM) product and is found using a two-tone measurement. It can be given in input (IIP3) or output (OIP3). Passive phase shifters are naturally more linear than their active counterparts, which contain active devices that are inherently nonlinear [27].

e) Power handling: The RF phase shifters are often required to operate with high power without significant performance alteration. The power handling of an RF phase shifter is determined by its maximum output power and is measured by its one-dB compression point (P_{1dB}). Like an amplifier, the 1-dB compression point of a phase shifter refers to the point where its actual output power is 1 dB less than its ideal linear output power and can be given in input (IP_{1dB}) or output (OP_{1dB}). Passive phase shifters possess better power handling capability compared to active phase shifters.

f) Phase range and resolution: The phase range constitutes the phase difference between the maximum obtainable phase shift (φ_{max}) and the reference phase (φ_{ref}) as given by (2-2) [28].

$$\varphi_{range} = \varphi_{max} - \varphi_{ref} \tag{2-2}$$

The phase state may be normalized by subtracting the reference value from the actual phase shift (φ).

$$\Phi = \varphi - \varphi_{ref} \tag{2-3}$$

In this regard, the reference value of the phase shifter becomes 0˚, and the maximum normalized phase shift corresponds to the phase range ($\varphi_{range} = \Phi_{max}$). The resolution of a phase shifter is the minimum phase shift value between two consecutive phase states. The resolution is a useful parameter, particularly for phase shifters with digital phase control or digital phase shifters. It is dependent on the number of bits *N* of the bit control or DAC and expressed as [28]:

$$\varphi_{resol} = \frac{\Phi_{max}}{2^N} \tag{2-4}$$

For a 2-bit phase shifter with a phase range $\Phi_{max} = 360°$, the resolution is $\varphi_{resol} = 90°$ and the possible phase states are $\Phi_1 = 90°$, $\Phi_2 = 180°$, $\Phi_3 = 270°$, and $\Phi_4 = 360°$. The resolution is usually given as the number of control bits. Most practical digital phase shifters have a phase range of 360˚ and a resolution as high as 8 bits [29]. While digital phase shifters have limited resolution, analog phase shifters have a resolution dependent on the continuous analog control voltage [20].

g) Phase and amplitude error: The phase error of an RF phase shifter indicates the discrepancy between the desired phase shift and the measured actual phase shift. It is expressed as [30]:

$$\varepsilon_{\varphi} = \Phi - \Phi_0 \tag{2-5}$$

where Φ and Φ_0 are the measured and targeted phase states, respectively. The Root Mean Square (RMS) phase error is often used to evaluate the accuracy of the phase shifter. It is obtained by taking the RMS of the actual phase errors at all possible phase shifts. For an *N*-bit phase shifter, the total number of possible phase shifts is $M = 2^N$.

The RMS phase error is formulated as [30]:

$$\varepsilon_{\varphi,RMS} = \sqrt{\frac{1}{M}\sum_{n=1}^{M}\left(\Phi_n - \Phi_{0,n}\right)^2} \quad (2\text{-}6)$$

where Φ_n and $\Phi_{0,n}$ are the nth actual and target possible phase shifts, respectively. The RMS phase error is particularly important for digital phase shifters and is desired to be as low as possible [30].

The notion of amplitude or gain error is analogous to phase error and indicates the mismatch between the theoretical expected amplitude or gain and the measured/actual amplitude or gain of the phase shifter in decibels for a particular phase state. Nevertheless, passive and active phase shifters exhibit gain errors of less than 3 dB in general and do not present issues of greater significance for PASs [26]. Besides, the amplitude errors can be rectified by a VGA or an attenuator, which follows the phase shifter in the phased array system.

h) Chip area: the size of the phase shifter is an important parameter that must be kept small. RF phase shifters are often enormous in size since they generally employ inductors, which occupy large areas. For passive phase shifters, the area consumption is mostly dependent on the resolution/phase range, the frequency, and the process technology. Higher phase resolution and lower operating frequencies exhibit larger areas. Active phase shifters, on the other hand, tend to occupy relatively less areas compared to their passive counterparts since they rely on active blocks like amplifiers and area-effective blocks like attenuators for phase tuning.

i) Power consumption: It is desired for phase shifters to exhibit little to no DC power consumption, like any other RF module. Nevertheless, many active phase shifters use VGAs to perform phase tuning, therefore producing a decent amount of DC power consumption. Moreover, some phase shifters require amplification to improve the signal power and quality. As a result, the DC power consumption increases. Conversely, digital phase shifters typically consume negligible DC power.

There are many ways to classify RF phase shifters [25]. Based on the phase tuning mechanism, there exist mechanical, ferromagnetic/magnetic, micro-electromechanical systems (MEMS), and electronic phase shifters. RF phase shifters are categorized as passive and active based on the building blocks or elements. Moreover, phase shifters can be either digital or analog, depending upon the control voltage, albeit this generally refers to electronic phase shifters [25]-[26]. The next section describes the types of phase shifters based on their tuning mechanism.

2.2 Mechanical Phase Shifters

A mechanical or mechanically-tuned phase shifter is essentially a transmission line with a knob to manually change its electrical length and, thus, the phase of the input signal. Early RF phase shifters were based on mechanical tuning mechanisms. Phase shifters utilizing the variation of the electrical properties of coaxial lines have been widely studied since the 1960s [13], [31]-[33]. Two coaxial phase shifters were designed for the UHF to C bands in [13]. The first one is based on a helix formed by a coaxial line with an outer conductor shield, as shown in Figure 2.4(a). A movable dielectric slug is plunged into the helix. By changing the depth of the slug into the helix with a displacement x, a phase shift is produced between the two ends of the coaxial cable. As a result, a phase shift of 360˚ is obtainable for a slug displacement of about 1.4 inches (35.56 mm) at the C band. The second phase shifter is constructed using a coax-based 3-dB coupler terminated by grounded lines with variable length. By changing the length of the terminated coaxial line by a quarter wavelength, a total phase shift of 360˚ is obtainable. Illustrated in Figure 2.4(b), this configuration constitutes one of the first reflective-type phase shifters based on mechanical tuning [13]. Moreover, a stretchable coaxial-based phase shifter structure was recently developed from 1 to 4 GHz in [33]. The phase shifter is a cylindrical structure composed of a liquid inner conductor and a liquid metal shield encased in and insulated by a stretchable polymer, as seen in Figure 2.4(c). The results show a 194˚total phase shift for a 62% stretch of the structure while keeping the input reflection coefficient below -10 dB.

Mechanical phase shifters using microstrip lines have also been proposed [34], [35]. In [34], a trombone beamformer based on a mechanical microstrip phase shifter has been proposed, as seen in Figure 2.4(d). Phase shifting or delay generation is performed by sliding a movable superstrate on top of a fixed substrate, where the microstrip lines make physical contact for continuous signal flow. A phase shift of ±80˚ is obtainable for a translation distance of x = ±10 mm at 2.4 GHz. In [35], a reconfigurable microstrip phase shifter is discussed. Based on displacing the ground plane, which encompasses a stretchable membrane structure, it uses a single membrane with a 10.4 mm diameter to achieve a total phase shift of -55.5˚ at 14.25 GHz. Despite its high-power handling capability, this phase shifter design requires high voltages applied to the membrane in order to produce wider phase shifts.

Slotted waveguides are also used to design mechanical phase shifters [36]-[37]. Two X-band phase shifter designs based on slotted waveguides have been proposed in [36]. The first comprises two metal fin

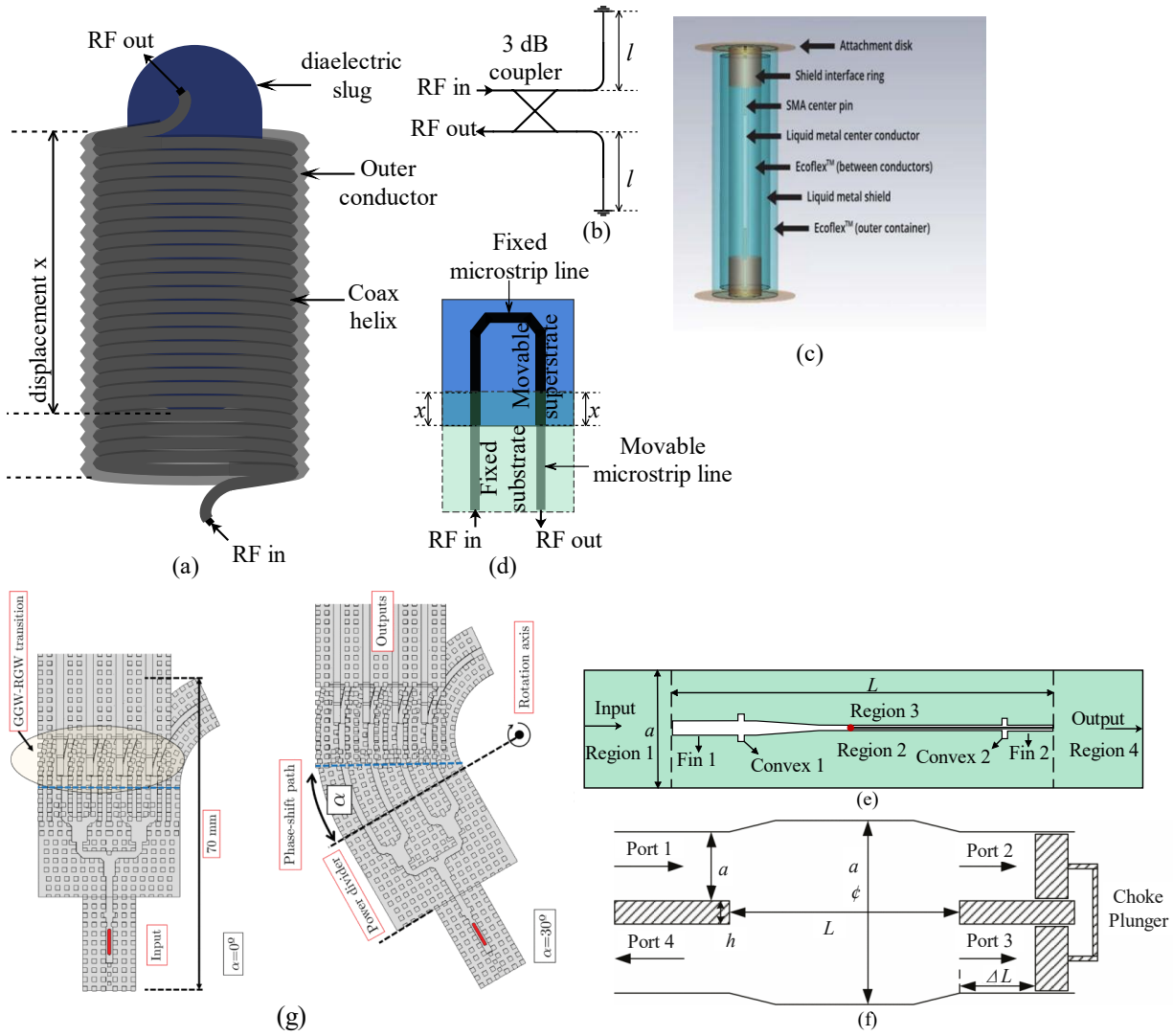


Figure 2.4: Mechanical phase shifters: (a) helix coaxial structure, (b) 3-dB coaxial coupler structure, (c) stretchable coaxial structure [33], (d) trombone movable microstrip line structure, (e), (f) slotted waveguide structures [36], (g) gap waveguide structure [38].

structures, one fixed and the other mobile, embedded in a slotted waveguide and forming four different regions, as seen in Figure 2.4(e). When a TE_{10} mode wave is transmitted to Region 1, it will be split into Regions 2 and 3 and then combined in Region 4. The phase shift is accomplished by changing the transmission length L of Regions 2 and 3. The convex structures improve wave transmissivity. The other design is based on the side-slot waveguide structure in Figure 2.4(f). The structure has four ports, where a movable choke plunger is placed at ports 2 and 3. Similar to the reflective-type phase shifter, a wave sent through port 1 propagates in the region of narrow side slots and splits into two, each directed towards ports 2 and 3. The waves at ports 2 and 3 are then reflected from the plunger and combined at port 4, the output port. By sliding the choke plunger by a distance ΔL, the transmission length of the split waves is changed, and so is the phase of the output wave. Moreover, a slotted waveguide phase shifter was

implemented in [37] by mechanically changing the length of the short stub of the left-handed waveguide. The total phase shift produced by the structure is -50˚ for a stub length difference of 3 mm.

Lastly, the gap waveguide (GW) technology has gained popularity in PASs in recent years [38]-[40]. It typically enables mechanical phase shifting through power splitting, as illustrated in Figure 2.4(g). A 1:N power divider was designed using the groove gap waveguide (GGW) on an upper fixed block. The output lines of the power divider are located on a rotatable lower block and designed using a ridge gap waveguide (RGW). The signals are transmitted from the lower to the upper lines using a slot. By rotating the lower lid by an angle α, the lengths of the lines increase, therefore increasing the output phases with respect to the input. Moreover, the physical lengths of the output lines are unequal due to the circular nature of the fixed block. Thus, a constant phase shift is created between the output ports [38]. The reported mechanical phase shifters offer high phase precision, low overall cost, high-power handling, and high mechanical strength since they often use rigid materials such as copper. Moreover, microstrip and waveguide phase shifters can operate in a relatively wide range of temperatures due to their constituent materials. However, their applications are mostly limited to instrumentation due to their bulky size and the difficulty of implementing a proper automated phase control system, lowering their speed.

2.3 Magnetic and Ferromagnetic Phase Shifters

Magnetic/ferromagnetic (or ferroelectric) phase shifters are based on varying the dielectric properties of a ferromagnetic material inserted in the structure of a transmission line. The earliest magnetic phase shifters were built with waveguide lines in general. The most basic waveguide magnetic phase shifter is made by centrally inserting a ferromagnetic rod (ferrod) inside a waveguide structure, as seen in Figure 2.5(a) [14]. A dielectric foam supports the ferrod and bears a dielectric material (e.g., stycast) at the two ends for impedance matching. A solenoid wrapped on the outer surface of the waveguide is used to apply a magnetic field to the ferrod through voltage bias. By changing the magnetic flux inside the rod, the dielectric material's permittivity changes, therefore, varying the phase velocity of the wave travelling on the ferrod. In [14], several experiments were conducted with magnetic phase shifters using rectangular waveguides and a ferrite rod of diameter equal to 0.27 inches (6.858 mm). The signal wavelength is 3 cm. It was observed that a 360˚ total phase shift is obtainable using a ferrod with at least 2.5 inches (63.5 mm) length for an applied field below 60 Oesterds (4.77 kA/V). As the phase shift is related to the length of the ferrite rod, a digital or latching phase shifter may be designed by using several cascaded ferrods with different latching switches centrally positioned in the waveguide [41].

Strip line technology was also used to implement magnetic phase shifters. The typical strip line-based magnetic phase shifter is composed of a center conductor placed within a ferrite or garnet dielectric loading medium, as shown in Figure 2.5(b). A magnetic field is applied to the dielectric material through the center conductor and the magnetic material, changing the phase of the signal on the conductor. Similar to the waveguide magnetic phase shifter, the phase change is proportional to the size of the ferrite. In [42], the authors designed a 4-bit phase shifter using the strip line in the C-band. Cascaded garnet toroids were used as phase shift elements with lengths adjusted to provide 22.5˚, 45˚, 90˚, and 180˚ phase shifts. The experimental results showed a phase deviation of ±3 % with an insertion loss of less than 0.9 dB over the band.

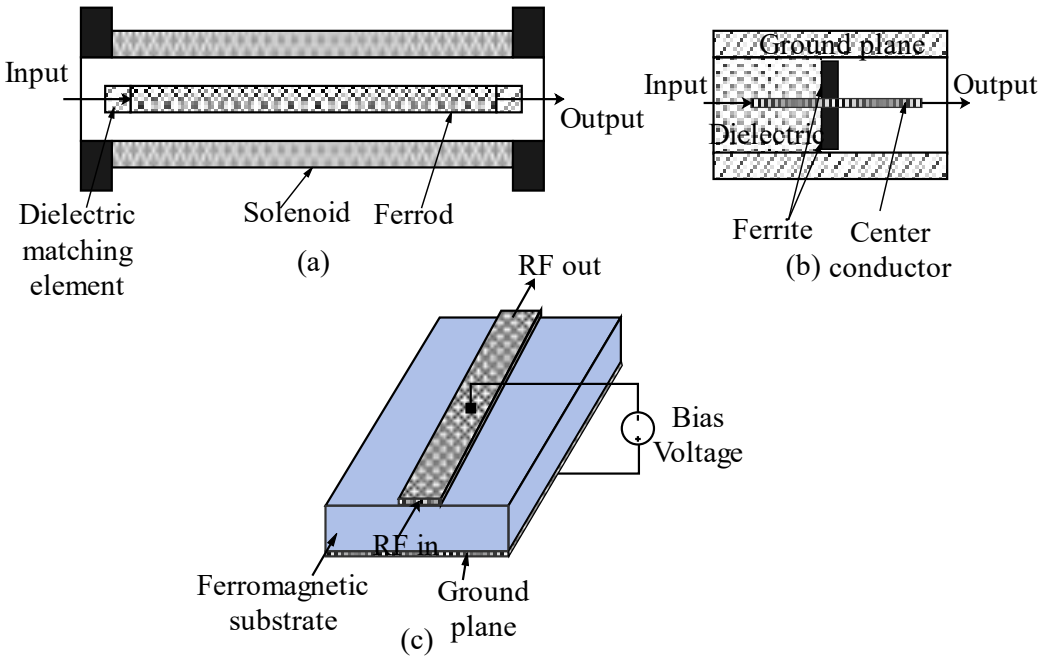


Figure 2.5: Magnetic/Ferromagnetic phase shifters: (a) rectangular waveguide structure, (b) Strip line structure and (c) microstrip line with ferromagnetic substrate.

Most recent ferromagnetic phase shifters employ microstrip lines or substrate-integrated waveguides (SIWs) with ferromagnetic substrates such as the Barium Strontium Titanate (BST) [43]-[45]. The basic operating principle of microstrip phase shifters with a ferromagnetic substrate is represented in Figure 5(c). By applying a high voltage to the substrate (e.g., 270 V), the permittivity of the ferromagnetic material changes. Any change in the dielectric constant of the substrate results in an alteration of the electrical length of the wave on the microstrip line. This principle was used in [43] to design a phase shifter with a 165˚ tuning range at 2.4 GHz. Furthermore, a 2×3 element phased array using a SIW phase shifter was proposed in [44]. It encompasses a ferrite-loaded substrate, which modifies the phase velocity

of the structure when subjected to magnetization through external coils. The fabricated array system achieved a total phase shift of ±19˚ at 13.2 GHz using embedded biasing windings. It can be observed from [14], [41]-[45] that magnetic and ferromagnetic phase shifters provide high phase accuracy with continuous or digital tunability. Nevertheless, their relatively large size and the need to apply large electromagnetic stimulating voltages render them unattractive for integrated and compact designs.

Despite their incompatibility with semiconductor technologies, magnetic/ferromagnetic and mechanical phase shifters suffer from low speed and difficulty in implementing proper control circuits [13], [14], [31]-[45]. For these reasons, most recent research on phase shifters for antenna array system applications has been directed towards electronic-based solutions, which offer lower power and area consumption.

2.4 Electronic Phase Shifters

Electronic phase shifters are among the most popular due to their compact size and compatibility with the CMOS process. The phase shift is fulfilled by applying a DC control voltage signal, which may be discrete or continuous. Thus, there exist digital and analog electronic phase shifters. Moreover, RF phase shifters may be classified as passive or active depending on their building circuit elements. In terms of architecture, electronic phase shifters are categorized as Switched-Type Phase Shifters (STPS) [46]-[55], Reflective-Type Phase Shifters (RTPS) [56]-[72], Loaded-Line Phase Shifters (LLPS) [73]-[76], and Vector-Sum Phase Shifters (VSPS) [77]-[88].

2.4.1 Switched-Type Phase Shifters

The STPS is widely used in phased array applications. The simplest STPS is essentially based on switching between two different phase or delay paths. The switch is typically an SPDT controlled by a digital voltage signal. The STPS is, therefore, inherently digital. The delay paths may be implemented using transmission lines (switched-line phase shifter) or lumped-element filters (high/low pass phase shifter).

The Switched-Line Phase Shifter (SLPS) or Switched-Transmission Line Phase Shifter (STLPS) is composed of two transmission lines with different lengths, as represented in Figure 2.6(a).

The effective phase shift of an SLPS is determined by the difference between line lengths and the signal wavelength as formulated below [46]:

$$\Delta\varphi = \frac{2\pi(l_2 - l_1)}{\lambda} \tag{2-7}$$

where l_2 and l_1 are the respective lengths of the longer and shorter line. The wavelength, $\lambda = \frac{c}{f\sqrt{\varepsilon_{eff}}}$ is dependent on the speed of light *c*, the frequency *f* and the effective permittivity of the medium ε_{eff}. The SPDT employed in the design of SLPSs must have relatively high isolation between ports to improve signal transmissivity. Furthermore, it is recommended to avoid implementing half-wavelength lines to avoid return loss deterioration. In this regard, to design a 180˚ phase shifter, the Schiffman topology may be used, where $l_2 = 3\lambda/4$ and $l_1 = \lambda/4$ [47]. SLPSs are robust and stable against temperature variations because the phase shift mostly depends on the transmission line size [48]. Thus, the thermal performance of the phase shifter is dependent on the switching element, which is typically made of silicon diodes and can withstand up to 175˚C [49]. Besides, they offer wider bandwidth compared to the STPSs implemented with lumped elements. However, they occupy large areas at low frequencies as the electrical length of the line is inversely proportional to the frequency [46].

Moreover, the delay blocks may be built using lumped element filters. The most common STPS based on lumped elements is the High/Low Pass Phase Shifter (HLPPS) or Switched-Filter Phase Shifter (SFPS). The operating principle of an HLPPS consists of switching between a High Pass Filter (HPF) and a Low Pass Filter (LPF), which generate different delays, as illustrated in Figure 2.6(b). The LPF and HPF can be either tee (T) or pi (π) configurations, as shown in Figure 2.6(c). For an LPF, Z_{2t}, Z_{3t} and Z_{1p} are inductive, whereas Z_{1t}, Z_{2p} and Z_{3p} are capacitive. The reverse scenario holds for an HPF. If the tee or pi network is symmetric (i.e., Z_{2t}= Z_{3t} and Z_{2p}= Z_{3p}), they can be analogized to a transmission with characteristic impedance Z_0 and electrical length βl = φ, where β and l are the phase constant and the length of the line, respectively.

By equating the transmission (ABCD) matrices of the tee and pi networks to that of the transmission line as provided in [46], the phases of the tee and pi networks are expressed as follows:

$$\varphi_t = \cos^{-1}\left(1 + \frac{Z_{2t}}{Z_{1t}}\right) \tag{2-8}$$

$$\varphi_p = \cos^{-1}\left(1 + \frac{Z_{1p}}{Z_{2p}}\right) \tag{2-9}$$

And their respective characteristic impedances are given as:

$$Z_{0t} = |jZ_{1t} \sin \varphi_t| \tag{2-10}$$

$$Z_{0p} = \left| \frac{Z_{1p}}{j \sin \varphi_p} \right| \tag{2-11}$$

where φ_t and φ_p are the phases produced by the T and π networks, respectively, while Z_{0t} and Z_{0p} are their respective equivalent characteristic impedances. The total phase shift generated by an HLPPS is equivalent to the difference between the phases of the LPF and the HPF. In practice, most of the phase shift is produced by the LPF since the low-pass network exhibits a better gain-frequency response compared to the high-pass network. In addition, the switches may be repositioned through the filter structure to obtain a simpler configuration. One such design is the switched π-network shown in Figure 2.6(d) [54]. The network may be a high- or low-pass, albeit the latter is frequently used. The ON and OFF states of the switches produce delays, the difference of which determines the total phase shift. This configuration is more area-effective and exhibits lower insertion loss. SFPSs are preferred for low-frequency applications as they occupy smaller areas compared to their switched-line counterparts.

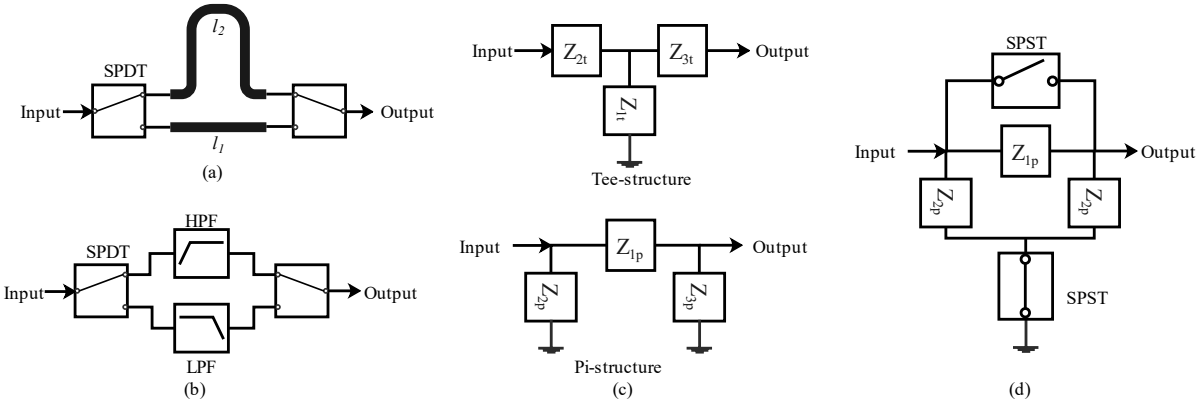


Figure 2.6: (a) SLPS, (b) SFPS, (c) T- and π- filter networks and (d) Simplified SFPS.

However, as they present different parasitic resistances and capacitances, their design is relatively more difficult due to the limited quality factor (Q-factor) of on-chip inductors in addition to their high loss and bandwidth limitation [53]-[55].

Furthermore, broad phase ranges may be obtained by cascading two or more simple STPSs. The number of bits of the phase shifter is equivalent to the number of stages. Typically, the individual phase stages of an N-bit phase shifter with a 360˚ phase range are $360^\circ/2^{N-0}$, $360^\circ/2^{N-1}$… $360^\circ/2^1$. For instance, a

4-bit STPS will have 22.5˚, 45˚, 90˚ and 180˚ individual phase stages. Consequently, the resolution is proportional to the number of bits and the chip area.

STPSs have been extensively explored in the literature, the switched-filter type being the most common design. The SLPSs are often implemented on PCB for frequencies below X-band [50], using RF MEMS switches [51] and coplanar waveguides in System-On-Insulator (SOI) technologies in mm-wave frequencies [52]. On the other hand, many switched-filters phase shifters are implemented in the CMOS technology [53]-[55]. STPSs present several advantages, including low power consumption, high linearity, and relatively high-power capability since they do not employ active devices in their primary circuits. However, the main issues associated with the reported STPSs are high insertion loss, poor switching performance, large chip area, and low phase resolution [46]-[55]. STPSs are built using passive elements such as inductors, which generate high losses at high frequencies and occupy large areas. Moreover, the performance factors of the MOSFET switches, such as the insertion loss and isolation, degrade as the frequency increases. In this regard, techniques involving floating the bulk of transistors were used in [55] to improve the overall insertion loss of the phase shifter. Furthermore, as the number of bits determines the number of building stages in an STPS, higher resolution results in larger chip areas. Consequently, the reflective-type phase shifter is often explored in the literature as an alternative to the switched-type since it provides continuous phase tuning.

2.4.2 Reflective-Type Phase Shifters

The reflective-type phase shifter is widely used in diverse applications, including PASs, to provide precise phase shifts with fine resolution. Unlike the STPS, the RTPS has the ability to provide continuous phase tuning and is, therefore, an analog phase shifter, even though the phase states may be digitized using a DAC. A typical RTPS is composed of a hybrid coupler or circulator and a variable reflective load, as depicted in Figure 2.7. The variable load is ideally purely reactive and may be built using a varactor, a pin diode, or a combination of varactors and inductors [56]. The phase shifters implemented with circulators are cost-effective and less lossy. Nevertheless, passive circulators are often made with magnetic materials, rendering them bulky and difficult to integrate with semiconductor processes. The

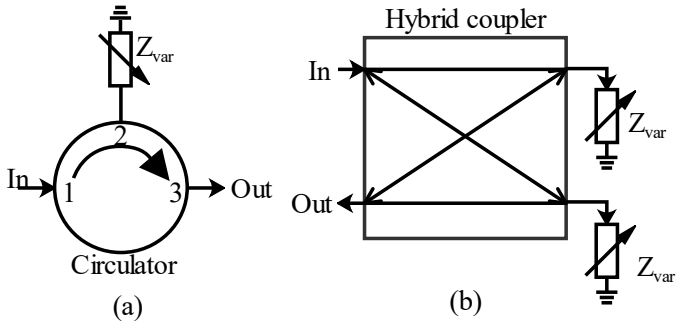


Figure 2.7: RTPS based on (a) circulator and (b) hybrid coupler.

circulator-based phase shifter is represented in Figure 2.7(a) and comprises 3 (or 4) ports. The reflective load is connected to Port 2, whereas the input and output ports are Port 1 and Port 3, respectively. A signal transmitted from the input is reflected at the variable load. The reflected signal, in turn, is delivered to the output at Port 3 while no signal flows back to Port 1. The amplitude and phase of the output signal are thereby proportional to the reflection coefficient of the signal from Port 2, which is expressed as:

$$\Gamma_{load} = \frac{jX_{load}-R_0}{jX_{load}+R_0} = 1e^{j\left[180°-2\tan^{-1}\left(X_{load}/R_0\right)\right]} \tag{2-12}$$

where X_{load} and R_0 are the reactance of the variable load and the characteristic resistance of the network, respectively. As seen from (2-12), the phase of the output signal can be tuned by changing X_{load}. On the other hand, the coupler-based phase shifter is commonly constructed using a 3-dB hybrid coupler and identical reflective loads connected at the thru and coupling ports, as seen in Figure 8(b). It is more popular than its circulator-based counterpart as the coupler is easier to design and may be implemented using transmission lines or lumped elements. The coupler may have a 90˚ or 180˚ phase difference between its outputs. In this regard, the branch-line, Lange, and directional couplers are commonly used to implement the RTPS [57]-[63]. The working principle of the coupler-based RTPS is similar to that of the circulator-based phase shifter. A signal inserted at the input port gets reflected from the variable reactive loads ($Z_{var} = jX_{load}$) at the thru and coupling ports with the reflection coefficient Γ_{load} formulated in (2-12) with phase $\varphi_{load} = 180° - 2\tan^{-1}\left(X_{load}/R_0\right)$. The individual signal reflected from the thru and coupling ports will be transferred to the input and isolation ports. The phases of the reflected signal from the thru and coupling ports following the complete trajectory have a 180˚ difference at the input port and are the same at the isolation port. Therefore, the reflected waves will be subtracted at the input and added at the isolation port, which is the output of the phase shifter.

The phase range of an RTPS is given as [56]:

$$\varphi_{range} = 2\left[\tan^{-1}\left(\frac{X_{load,max}}{R_0}\right) - \tan^{-1}\left(\frac{X_{load,min}}{R_0}\right)\right] \quad (2\text{-}13)$$

where $X_{load,max}$ and $X_{load,min}$ are the maximum and minimum values of the load reflective reactance, respectively.

As demonstrated in (2-13), the theoretical phase range of the ideal RTPS is below 180˚ if the load is purely reactive. Additionally, diodes have a limited tuning capacitance range. As a result, RTPSs have narrow phase ranges. The phase range can be increased using a combination of varactors and inductors as the reflective load [56], despite parallel L-C loads having a wider phase range than their series counterparts [57]. Another technique used to achieve a 360˚ total phase shift is the cascading of two quadrature couplers and using π-type LC variable loads as demonstrated in [58] and [59]. Alternatively, multi-resonating variable loads may be used to obtain wide phase ranges. In [60], a single quadrature coupler is used in conjunction with a transformer-based multi-resonating variable load to achieve 360˚ total phase shift at millimeter-wave frequencies. Recent publications use multi-resonating transmission lines as the reflective load to achieve 360˚ phase shift [61]-[63]. Note that the phase shifter utilizing a distributed transmission line as a reflective load is called the reflective-type transmission line phase shifter (RTTLPS).

Moreover, from (2-12), all the signals reflected from the variable load will appear at the output if the coupler and load do not generate any loss. Nevertheless, the coupler and the reflective load are generally built using either transmission lines or lumped elements, which have a limited Q-factor, leading to the gain degradation of the phase shifter. Besides, as the varactor presents limited reverse bias resistance, there is often significant gain variation for different phase states. One solution addressing the gain imbalance and low insertion loss is the use of two couplers, each providing a 180˚ phase shift [58], [59]. This reduces the gain variation of the phase shifter to only half, but with an increased chip area. Another loss reduction method is the implementation of active reflective loads with R-C feedback, as described in [64]. Next, a reflective amplifier and a tunable load are used in [65] to implement a sub-millimeter-wave phase shifter with 10.2 dB gain and 0.7 dB gain variation over a 180˚ phase range. Lastly, it has been proven in [66] that using diagonally configured coupled lines improves the insertion loss of the RTPS.

Furthermore, RTPSs have limited bandwidth, which is mostly dependent on the coupler. RTPS designs with 3-dB quadrature couplers often present larger bandwidths than the 180˚ hybrid coupler

designs, but at the cost of larger chip areas [58]-[63]. The typical fractional bandwidth of passive RTPSs is at most 21% [59]-[63]. Several bandwidth improvement techniques have been employed in the literature, including the use of reflective coupled lines in the hybrid coupler [67] or the reflective load [68] structure, as well as the use of planar magic-T quadrature couplers [69].

Moreover, RTPSs occupy large chip areas due to their passive nature. Nevertheless, phase shifters implemented with directional couplers [70], reflective amplifiers [65], and active circulators [71] offer smaller chip areas. The bandwidth and insertion loss improvements generally trade off with chip area performance. Yet, it has been proven in [72] that coupled lines with a length shorter than a quarter-wave may be used to design an RTPS by selecting optimum values of the odd and even impedances. The resulting phase shifter provides 36% fractional bandwidth with an area equal to $\lambda^2/56$, which corresponds to one of the smallest chip areas produced by a passive phase shifter.

2.4.3 Loaded Transmission Line Phase Shifters

Loaded-Line Phase Shifters (LLPSs) are mostly employed in wireless communications to perform phase shifts typically below 180˚ [73]-[75]. Basic LLPS comprises a transmission line section and shunt or series variable reactance, as shown in Figure 2.8(a) and Figure 2.8(b), respectively. The variable reactance may be capacitive or inductive. Additionally, it may be tuned continuously or discretely. Hence, the LLPS may be analog or digital. The transmission lines in Figures 2.6 (a) and 2.6(b) can be modelled as π and T L-C networks, respectively, as seen in Figures 2.8(c) and 2.8(d). The impedance values from the π- and T-transformations of a line with characteristic impedance Z_0 and electrical length βl are

$$Z_{TL,1p} = jZ_0 \sin \beta l \tag{3-14}$$

$$Z_{TL,2p} = j\frac{Z_0 \sin \beta l}{\cos \beta l - 1} \tag{3-15}$$

$$Z_{TL,1t} = j\frac{(\sin \beta l)(\cos \beta l - 1)}{Z_0} \tag{3-16}$$

$$Z_{TL,2t} = j\frac{\sin \beta l}{Z_0} \tag{3-17}$$

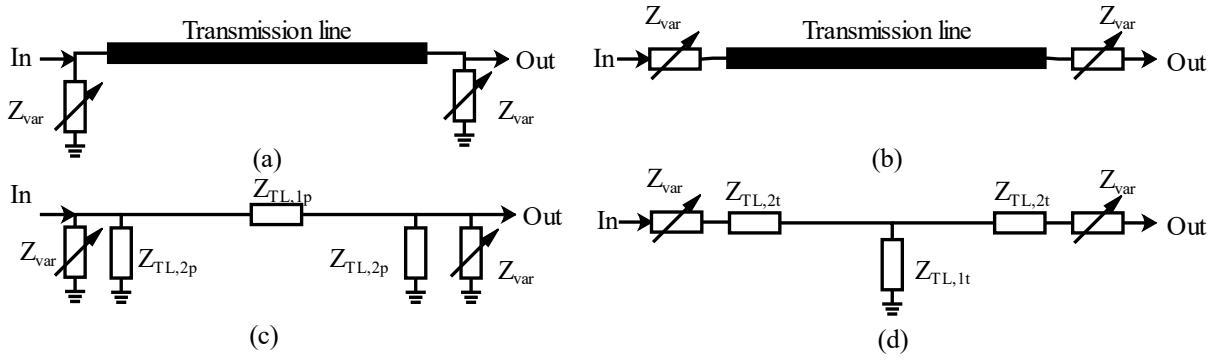


Figure 2.8: LLPS: (a) Shunt-configured and (b) series-configured variable reactance. Transmission lines modelled as (c) π- and (d) T- impedance networks, respectively.

The transmission phase and characteristic impedance of the LLPS with shunt and series variable impedances are found using (2-8) through (2-17) as:

$$\varphi_{shunt} = \cos^{-1}\left(1 + \frac{Z_{TL,1p}\left(Z_{TL,2p}+Z_{var}\right)}{Z_{TL,2p}Z_{var}}\right) \tag{2-18}$$

$$\varphi_{series} = \cos^{-1}\left(1 + \frac{Z_{var}+Z_{TL,2t}}{Z_{TL,1t}}\right) \tag{2-19}$$

$$Z_{0,shunt} = \frac{Z_{TL,1p}}{j\sin\varphi_{shunt}} \tag{2-20}$$

$$Z_{0,series} = jZ_{TL,1t}\sin\varphi_{series} \tag{2-21}$$

As seen from (2-18) through (2-21), the output phases are functions of the tuning-loaded impedance Zvar, albeit the phase range is limited by other parameters. Moreover, as the phases change, the equivalent characteristic impedances of the phase shifters are altered, as demonstrated by (2-20) and (2-21). Consequently, the LLPSs typically suffer from input and output mismatches during the phase tuning.

The main drawbacks of LLPSs are the poor return loss over the entire phase states and the limited phase range [73]-[75]. The phase range of an LLPS is imposed mainly by the variable load, which is generally a varactor, as the transmission line length is generally fixed at a quarter-wavelength. An LLPS with only varactor loads provides a maximum theoretical phase shift of only 90˚. The phase range is much lower in practice due to the limited varactor tuning range [73]. The tuning range of a varactor-loaded LLPS may be improved by cascading several sections as in [73], where a 70˚ phase shift was obtained by

cascading three identical cells. This is sometimes referred to as the distributed transmission line phase shifter. However, its poor return loss at high tuning capacitance narrows the bandwidth. To improve the return loss and phase range, an artificial transmission line composed of a varactor-tuned transformer and varactor loads was used in [74] to design a phase shifter with a total phase range of 133˚ at mm-wave frequencies. Digital tuning may be employed to achieve 360˚ phase shift as in [75], where microstrip slot line structures with open/short stub loads have been used to design a 5-bit phase shifter with improved matching at all phase states. Moreover, the frequency range of transmission lines is limited by their Bragg frequency, which depends on their equivalent inductance and capacitance values [76]. As a result, the frequency of operation and the phase range of a distributed LLPS are cut off by its Bragg frequency, which reduces as the total line length increases.

Passive phase shifters present several disadvantages, such as high insertion loss, large area, and narrow bandwidth, generally limiting their applications to Ku-band and below [67]. Active phase shifters, on the other hand, address these issues, providing higher gain and smaller chip area.

2.4.4 Vector-Sum Phase Shifters

Vector modulators are the most common active phase shifters, with applications often targeting mm-wave frequencies. Represented in Figure 2.9(a), a basic VSPS is composed of a vector generation unit, a gain-tuning unit and a vector summation/subtraction unit. An input RF signal is divided into two signals with a phase difference of 90˚, which are subjected to gain tuning before being added to provide the output signal. The change in the gain of one signal path with respect to the other results in the phase shift of the output signal with respect to the input. The output signal of an ideal VSPS is given as:

$$V_{out} = \left(A_1 e^{j0} + A_2 e^{j\frac{\pi}{2}}\right) V_{in} = \left(\sqrt{{A_1}^2 + {A_2}^2}\, e^{j \tan^{-1}\left(\frac{A_2}{A_1}\right)}\right) V_{in} \tag{2-22}$$

where A_1 and A_2 are the tuning gains of the in-phase and quadrature signals generated, respectively, and V_{in} is the input RF signal. From the above equation, one can observe that both the phase and gain of the output signal are dependent on the tuning gains A_1 and A_2. Meanwhile, the maximum theoretical phase range of a basic vector modulator is 90˚. To obtain a 360˚ total phase shift, a 4-quadrant operation of the VSPS is required. This is often achieved through the generation of differential I/Q vector signals, as seen in Figure 2.9(b) [77]-[82].

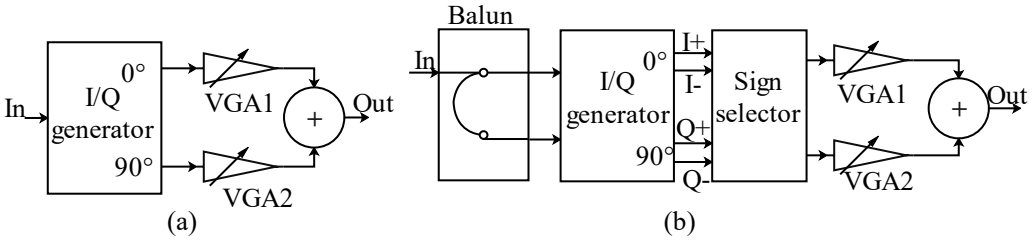


Figure 2.9: VSPS: (a) basic block diagram (b) block diagram for obtaining 360º phase range.

Differential quadrature signals may be generated through Polyphase Filters (PPFs) [77]. However, passive PPFs suffer from high insertion loss at high frequencies. Active PPFs may be used to improve the system gain [78] but at the cost of poor linearity, power handling, and DC power consumption. Moreover, Quadrature All-Pass Filters (QAFs) are often used to generate differential quadrature signals [79]-[81]. Since the QAFs suffer from capacitive loading from the succeeding stages, techniques such as inductive loading [80], [81] and the use of series resistance [79], [82] are employed to boost the phase and amplitude mismatch of the phase shifter. The generation of differential I/Q vectors by PPFs and QAFs is area-consuming as a balun at the input is required to produce a balanced input signal. Additionally, to access the four quadrants, sign selectors are used, which are often differential or single-ended amplifiers and switching networks. Consequently, the power overhead is increased.

Zero-π amplifiers have been used in [83] to design a vector modulator with reduced power consumption, but the chip area remains relatively large. Attenuator tuning may be used to reduce power consumption [84]-[86]. Biphase modulators (BMs), phase-invertible variable attenuators (PIVAs), and an X-type attenuator were used, respectively, in [84], [85], and [86], to implement two-branched active phase shifters with reduced area and power consumption. Nevertheless, these techniques require using baluns or couplers alongside attenuators to achieve phase inversion, limiting the area reduction. In addition, the insertion loss of attenuator-tuned phase shifters tends to be high [84]. Furthermore, for a VSPS to achieve 360˚ continuous phase shifting, the theoretical gain tuning range must be infinity, which is impractical. As a result, each quadrant practically provides a phase range of less than 90˚, leaving "phase gaps" during the device operation. These phase gaps limit the tuning range and resolution of vector modulators, which generally operate as digital phase shifters. A fine scaling resistive network was employed in [15] to increase the phase resolution. Nevertheless, 360˚ fine-tuning is not feasible with this method. An analog vector modulator was designed in [87] between 1.05 and 1.3 GHz with the help of a passive reconfigurable filter. In spite of not generating a full 360˚ phase range, the implemented phase shifter appears to be bulky, limiting its application to low frequencies. Consequently, it is challenging to implement analog phase shifters with small chip areas. In this respect, a non-quadrature vector modulator

solution was proposed in [88] to produce a power and area-efficient phase shifter with continuous phase shifting. It was proven that the phase range produced by a non-quadrature vector modulator is greater than that of its quadrature counterpart, allowing the operation of only two vectors to produce a 360˚ phase range and, hence, reducing both the power and area consumption.

Table 2.1 summarizes the performance of the diverse electronic phase shifters. The passive phase shifters, mainly the STPS, the RTPS and LLPS, exhibit higher linearity, can handle high power, and consume less power than their active counterparts. In contrast, the VSPSs offer relatively wider bandwidth, higher gain, and smaller chip area than the passive phase shifters. Meanwhile, most passive and active electronic phase shifters can be controlled to provide either continuous or discrete resolution, except for the STPS, which is inherently a digital phase shifter. To achieve decent performance in terms of power capability, bandwidth, insertion loss, and chip area, much recent research is targeting the MEMS solution.

Table 2.1: Comparison of electronic phase shifters

Performance	**STPS**	**RTPS**	**LLPS**	**VSPS**
Bandwidth	Narrow	Narrow	Narrow	Wide
Passive/Active	Passive	Passive	Passive	Active
Phase control	Digital	Analog/Digital	Analog/Digital	Analog/Digital
Power consumption	Low	Low	Low	High
Chip area	Large	Large	Large	Small
Linearity	High	High	High	Limited
Output power	High	High	High	Low to medium
Insertion loss	High	High	High	Low
Return loss	Medium	High	Low	High

2.5 Micro-Electromechanical System Phase Shifters

RF MEMS have been employed in the design of phase shifters thanks to the advancement of the MEMS switches in the Monolithic Microwave Integrated Circuit (MMIC) technology. The RF MEMS phase shifters are more linear and less lossy than their electronic counterparts [16], [89]-[99]. Additionally, they are compatible with the CMOS process, unlike the mechanical and ferromagnetic phase shifters. PASs integrating MEMS phase shifters are more cost-effective since they offer higher

system gain, which eliminates the need for extra amplification stages, in addition to lower production cost, as the MEMS switches can be fabricated with the antennas [16]. RF MEMS phase shifters incorporate the MEMS switches into delay structures to produce different phase states. Therefore, they are generally digital, albeit the switch may be tuned to provide continuous states. Similar to electronic phase shifters, RF MEMS phase shifters can be switched-type, reflective-type, or distributed transmission line type.

The switched-type MEMS phase shifter employs MEMS SPDTs to switch between two or more delay lines. The delay lines may be MEMS transmission lines or low/high pass filters. The simplest 1-bit STPS is represented in Figures 2.6(a), (b), and (d). Multibit structures may be obtained by adding more delay lines to the 1-bit structure or cascading several 1-bit units. Conventionally, the number of switches used in an N-bit cascaded STPS is double the number of bits (2N), and the number of DC contacts is quadruple the number of bits (4N). Therefore, the insertion loss and chip area exhibited by typical MEMS-cascaded STPS with at least 5-bit control tend to be poor. Nevertheless, using multiple delay blocks along with Single-Pole, Multiple-Throw (SPMT) switching results in lower insertion loss and smaller area compared to the cascading method [16]. Alternatively, loss and area improvements may be achieved by combining cascading and multi-delay line methods, as in [89].

Switched-line MEMS phase shifters are more popular than their low/high pass switched filter counterparts, albeit many early reported MEMS phase shifters were switched-filter type [90]. This is due to the lower Q-factors of micromachined low/high pass filters.

The reflective-type MEMS phase shifter constitutes a hybrid coupler with its thru and coupled ports terminated by a reflective load, like the electronic RTPS. In the operating principle of the RTPS described above, the reflective load is ideally reactive. Here, the reflective load is a MEMS switching network of series or shunt delay lines, as illustrated in Figure 2.10(a). Therefore, the MEMS RTPS is typically digital, although the switches may be controlled continuously. The shunt delay switching provides better ON-state return loss [16]. The number of bits of the phase shifter is proportional to the number of shunt or series delay lines. The MEMS switches often introduce additional delays during the ON states. This creates phase errors in MEMS RTPSs that become significant at mm-wave frequencies [89]. Analog phase shifting is sometimes used to bypass the ON state switching error, as in [92], where an LC equivalent network with actuator-based varactors was designed as the reflective load of a mm-wave phase shifter. Besides, the tuning range of the RTPS may be improved by using reconfigurable quadrature couplers along with variable reflective loads [93].

Loaded transmission lines have been actively used in MEMS phase shifter implementations. Similar to the electronic LLPS described earlier, the variable load is usually capacitive and may be digitally or continuously tuned. Nevertheless, most recent MEMS LLPSs are analog, thanks to the development of MEMS varactors [94]. Moreover, the transmission line may be periodically loaded with

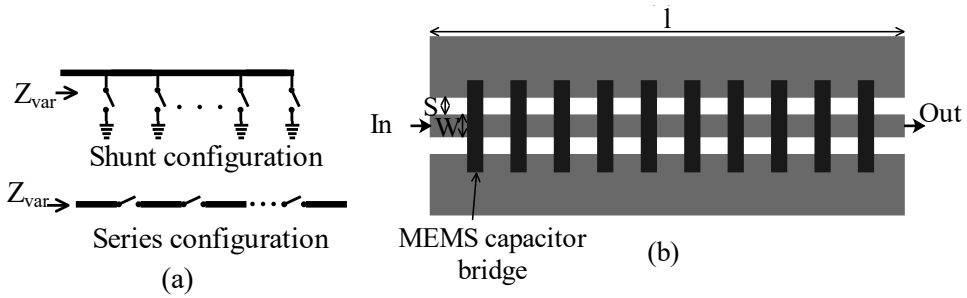


Figure 2.10: (a) Reflective load configurations for MEMS RTPS (b) DMTL phase shifter [16].

identical reactive loads forming a multi-section phase shifter, i.e., the distributed MEMS transmission line (DMTL) phase shifter, which offers a wider phase range than the single-section loaded line. A typical DMTL phase shifter is formed by a Coplanar Waveguide (CPW) crossed over by multiple MEMS capacitor bridges, as illustrated in Figure 2.10(b). The MEMS variable-capacitor may be of type Metal-Air-Metal (MAM) or Metal-Insulator-Metal (MIM), despite the former type offering better tunability and being easier to fabricate compared to the latter [16], [95]. Note that the MEMS LLPS suffers from low return loss like its electronic counterpart. The matching and phase range of the phase shifter are determined by the capacitance ratio between the tuning load capacitance and the input capacitance of the line. The higher the capacitance ratio, the higher the phase range and the poorer the matching, hence creating a trade-off between the phase range and the return loss exhibited by the phase shifter [16]. Several return loss improvements have been discussed in the literature while maintaining reasonable phase shifts. In [96], a liquid crystal-filled varactor was used as a variable load with a dielectric tuning mechanism alongside a CPW line to realize a phase shifter with a 92˚ phase range and 19 dB return loss at 76 GHz. The use of digital CMOS MIM and MEMS capacitors allows for higher-Q variable load and results in low insertion loss and high return loss [97]. A technique involving interlaced bits was used in [98] to improve the return loss and phase deviations compared to the cascaded bits. Moreover, as the total phase shift of a DMTL phase shifter increases, the total length of the line increases, therefore producing more insertion loss. This insertion loss may be improved by using a CPW line with an MAM varactor on a glass substrate [99]. In [100], a silicon slab with hexagonal patterns was inserted in a CPW to produce a total phase shift, insertion loss, and return loss of 145˚, 1.8 dB, and 18 dB, respectively, at 550 GHz. Like the electronic LLPS, the DMTL phase shifter suffers from the effect of the Bragg frequency, which limits its high-frequency operation and phase range.

Even though MEMS phase shifters outperform electronic phase shifters in terms of insertion loss, return loss, linearity, and bandwidth, they suffer from reliability issues mainly due to temperature effects on the MEMS switches [90], [92], limiting their application for mm-wave phased array systems. One potential solution is the emerging Liquid Crystal (LC) tunable device technology, which displayed excellent reliability and high phase precision at mm-wave frequencies.

2.6 Liquid Crystal and Liquid Metal Phase Shifters

The Liquid Crystal technology is emerging as a potential alternative to the electronically-tuned phase shifters due to its high performance at mm-wave frequencies [101]. The basic operating principle of an LC phase shifter is described in Figure 11(a) and is similar to that of an FM phase shifter [102]. The LC device is essentially based on the MIM structure, where the LC, a dielectric material, is sandwiched between two metal electrodes. The nematic LCs such as K12 and E7 are often used due to the diverse orientations of their anisotropic molecules [103]. Under no electric field, the LC molecules are oriented parallel to the electrodes, as seen in Figure 2.11(a) left. By applying an electric field through a voltage (DC or AC), the orientation of the molecules becomes perpendicular to the electrodes (or parallel to the electric field), as pictured in Figure 2.11(a), right. The change in the LC molecules' orientation results in a change in the permittivity of the LC dielectric material, which may be tuned continuously, depending on the magnitude and frequency of the applied voltage. Since the phase velocity of a planar transmission line is proportional to the dielectric constant of the substrate, a variation in the latter causes a phase shift of the transmission line. The maximum phase shift of a microstrip line is therefore written as [101]:

$$\Delta\varphi_{max} = 2\pi l(f/c)\Delta n = 2\pi l(f/c)\left(\sqrt{\varepsilon_{\parallel}} - \sqrt{\varepsilon_{\perp}}\right) \tag{2-23}$$

where $\varepsilon_{\parallel}$ and $\varepsilon_{\perp}$ are the maximum and minimum reflection coefficients of the LC, respectively, l the physical length of the line, c the speed of light, and $\Delta n = \sqrt{\varepsilon_{\parallel}} - \sqrt{\varepsilon_{\perp}}$ the maximum difference in the refractive index. $\varepsilon_{\parallel}$ is found under the maximum bias condition, where the LC molecules are oriented parallel to the applied electric field, whereas $\varepsilon_{\perp}$ occurs when no electric field is applied. This concept was first utilized in [104] to design a waveguide and microstrip phase shifter [105] at microwave frequencies. Early LC phase shifters were bulky and required the exertion of a high voltage (> 10 V) for phase tuning. Thanks to the advancement of material technology, recent LC phase shifters require only a few volts to change the device's permittivity with negligible power consumption. Besides, the LC phase shifters may be implemented using different types of transmission lines. In [106], a meander microstrip line and an RTPS with LCs were designed to provide respective total phase shifts of 243º and 170º at mm-wave frequencies. The implemented designs are described in Figure 2.11(b). Moreover, Figure 2.11(c) depicts

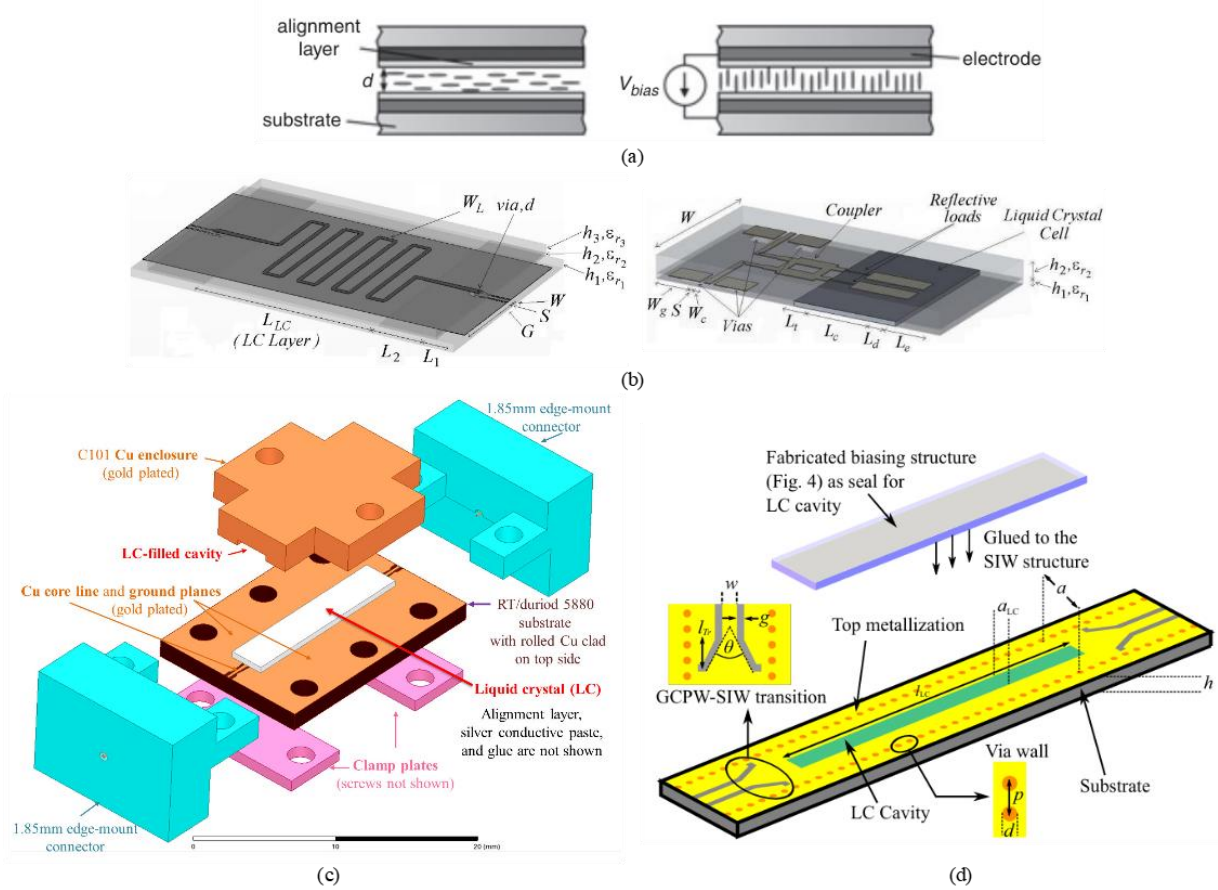


Figure 2.11: (a) Operating principle of LC devices: Crystal molecule alignment with (Right) and without (Left) applied electric field [102]. (b) LC meander microstrip line (Left) and reflective-type phase shifters [101]. (c) Exploded graphic view of an CPW LC phase shifter [17]. (d) Description of an SIW LC phase shifter [107].

the exploded view of a CPW broadband mm-wave phase shifter [17], which exhibits over 170˚ phase shift at 66 GHz for an applied voltage of 10 V. Furthermore, a proof-of-concept LC-based SIW phase shifter was designed in [107]. Shown in Figure 2.11(d), the realized phase shifter provided more than 80˚ differential phase shift at 20 GHz.

The gap waveguide technology was also used to implement LC phase shifters as in [108], where a phase shifter was designed to obtain a 387˚ phase range with an insertion loss ranging from 3.5 dB to 5.5 dB at 20 GHz. Lastly, the coaxial cable filled with LC was proven suitable for sub-millimeter-wave phase shifter applications [109], although a real-world implementation is lacking in the literature.

The reported LC-based phase shifters generally display high-frequency capability and low insertion loss with high reliability. However, their difficulty integrating with semiconductor technologies and their relatively larger size impede their broad application vis-à-vis the electronic phase shifters. As the LC tunable device is a relatively new technology, there is room for performance improvement of these phase

shifters to enable their potential use in 5G communication systems and beyond. Figure 2.12 illustrates a corporate chart classification of the existing phase shifter types implemented for antenna array systems.

Another emerging technology in phase shifter applications is the liquid metal (LM) device [110]-[113]. Most applications of LM devices in electronics and microfluidics use Gallium (Ga) based LM materials, which are nontoxic, unlike mercury [110]. The LM via is typically incorporated in an SIW substrate to generate a high-pass filtering effect, generating a phase shift [111]-[113]. The LM phase shifters rely on the activation of one or several individual LM vias to produce wide phase ranges.

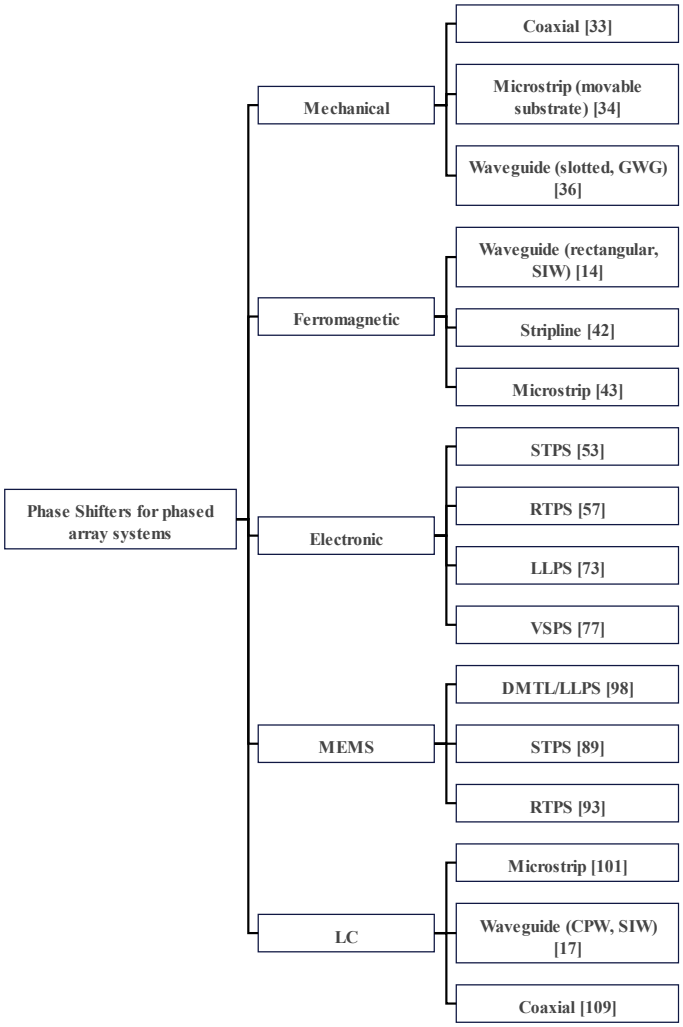


Figure 2.12: Classification chart of phase shifter for antenna array systems.

Therefore, they are generally digital. The reported LM phase shifters exhibit wider bandwidth, lower insertion loss and phase errors for X-band frequencies and below compared to their electronic counterparts. Nevertheless, this relatively new technology requires more profound research, especially at mm-wave frequencies, where LMs face challenges of proper actuation and containment [110].

A quantitative comparison of selected phase shifters from each type is provided in Table 2.2. While the mechanical and FM phase shifters proposed respectively in [38] and [45] provide continuous tuning, their phase ranges are limited due to their low phase shift per size. Additionally, the biasing of the FM requires a power consumption of 4.8 W, which is impractically high for phased array systems applications with dozens of elements. In contrast, the electronic and MEMS phase shifters described in [80] and [95] exhibit wide phase ranges with low power consumption. It is worth noting that the electronic phase shifter is digital with a 5.625˚ phase step, though it offers a 360˚ phase range. The LC phase shifter [108], on the other hand, provides more than 360˚ continuous phase tuning with little power consumption but has a volumetric size of 7424 mm^3, which is relatively large.

Table 2.2: Comparison of a few state-of-the-art phase shifters.

Reference	**[38]**	**[45]**	**[80]**	**[95]**	**[108]**
Type	Mechanical-GWG	Ferromagnetic-SIW	Electronic-VSPS	MEMS-DMTL	LC-GWG
Frequency (GHz)	29.5–30.5	11.5–13.5	15–38	15	25
Phase range/ resolution (˚/bit)	25/ continuous	153**/ continuous	360/6	165/3	387/ continuous
RMS phase error (˚)	-	-	2-3.5	-	-
Insertion loss	~0*	2.3	1.7–4.7	1.5	3.5–5.5
Power consumption (mW)	0	4800	19.2	0	3.618*
Size	-	85 mm^3	0.16 mm^2	30	7424 mm^3

*Data estimated; **Phase range under non-reciprocal bias.

Table 2.3 summarizes the generalized performance comparison of different phase shifter types in terms of tuning mechanism.

We can observe that the mechanical and ferromagnetic phase shifters are less attractive in most applications due to their limited frequency of operation, lower phase control speed, and poorer integration capability with semiconductor technologies.

Additionally, their bulky nature in general, lack of batch production technique, and costly fabrication process/material render them less attractive than their electronic and micromachined counterparts. In this regard, most modern phase array systems employ electronic and MEMS phase

shifters, even though they are relatively less precise. As the MEMS phase shifters suffer from temperature-related reliability issues and the brittleness of micromachined structures, electronic phase shifters remain the natural choice for low and medium-power applications. Moreover, even though the LC phase shifters offer good alternatives to their MEMS and electronic counterparts, especially at mm-wave frequencies, more research, particularly in the direction of miniaturization, is needed to make them suitable candidates for 5G wireless systems.

Table 2.3: Comparison of phase shifters classified based on their tunning method.

Performance	Mechanical	Ferromagnetic/ magnetic	Electronic	MEMS	LC
Operating frequency	Up to Ka-band	Below Ka-band	Beyond mm-wave	Beyond mm-wave	Beyond mm-wave
Bandwidth	Narrow	Narrow	Medium	Wide	Wide
Power consumption	Low	Low	Low/High	Low	Low
Power handling capability	High	High	Low/Medium	Medium	High
Phase precision	High	High	Medium	Medium	High
Speed	Low	Low	High	High	Low
Integration capability	Poor	Poor	Excellent	Good	Poor
Overall cost (material, production)	Low/Medium	Medium	High	Medium	Low
Main limitations	Bulky; physical phase adjustment; batch production not possible	Bulky; High voltage required; costly production	Relatively limited resolution/phase precision; gain/linearity trade-offs	Less reliable	Limited miniaturization

2.7 Calibration Methods of Phase Shifters for Antenna Array Systems

An antenna array with RF phase shifting contains a Phase Shifter Network (PSN), which typically encompasses phase shifter blocks along with DC feeding and a phase/gain control network. The phase shifter accessories, such as the control circuits, often present additional phase and gain errors, especially at high frequencies. In addition, phase deviations occur when the PSN is interconnected with blocks such as Low-Noise Amplifiers (LNAs), Power Amplifiers (PAs), and antennas in a receive or transmit chain. As a result, phase calibrations are always required for phase array antenna system operation. Most

Antenna array systems operate based on presumed fixed phase states, typically after accounting for the additional phase brought by the PSN's adjacent blocks [114]. Nevertheless, factors such as temperature, aging of the PSN, and adjacent blocks may cause additional phase drifts over time and, therefore, lower the performance of the array system. For that reason, it is recommended to incorporate a phase measurement and calibration mechanism into the system to readjust the phase errors periodically. The calibration methods used in phased array systems may be either amplitude-based or complex signal-based [114]. The most popular amplitude-based calibration method is the Rotating Element Electric Field Vector (REV) [115]-[117]. In the REV method, signal amplitudes (or powers) are measured by changing the phases of individual phase shifters in an array system to obtain their optimum phase states. The REV technique originally required the phase adjustment of each element. However, several advancements were made to the REV to reduce the number of measurements, including the use of a simple classification algorithm along with curve fitting and sinusoidal regression [116], as well as the maximum likelihood algorithm [117]. The REV calibration process is typically done over-the-air, meaning the signal power from the array element is measured in the far-field, therefore requiring a laboratory environment. On the other hand, the complex-based method involves the measurement of both the amplitude and phase of the array elements in order to adjust their phase states [118]-[121]. The phase and amplitude measurements are usually done through the injection of an oscillator signal to the phase-shifting element and I/Q demodulation of the output signal. Like the amplitude-based method, the complex signal-based method commonly requires element-by-element measurement and calibration, albeit improvement methods may be employed to render the calibration process faster [121]. Unlike its amplitude-based counterpart, the complex signal calibration circuit may be integrated into the PSN [118], [120] and, therefore, not require a laboratory environment. Moreover, the phase adjustment method of the PSN depends on the type of phase shifter used. For VSPSs, the phase correction may be done by changing the gains of the VGA through analog or digital means [120]. Multiple vector generators may also be used to correct the phase error in a vector modulator [122]. For passive phase shifters, the loaded-line phase trimmers may be used [123].

2.8 Conclusion

In this chapter, different phased array configurations were discussed with RF phased array systems offering a unique advantage of high SNR/SIR. Next, the working principle of a phase shifter has been described along with the metrics used to evaluate its performance. Then, a comparative study of the types of phase shifters based on their tuning mechanisms was performed. These types include mechanical, magnetic/ferromagnetic, MEMS, electronic and liquid crystal/metal phase shifters. The electronic phase

shifters appear to be the most popular type due to several advantages, including their compactness, integration capability with semiconductor technologies and high frequency operation capability. The passive electronic phase shifters are more linear and offer higher output power than the active phase shifters. Nevertheless, vector modulators outperform their passive counterparts in terms of chip area and gain. Even though quadrature vector modulators are preferred for high-frequency operations, the generation and synthesis of balanced quadrature signals proved to be relatively area- and power-consuming. Moreover, their resolution is limited by the presence of uncovered phase ranges between tuning quadrants. Finally, the calibration methods of phased shifters used in antenna array systems have been introduced. The next chapter covers the general study of linearity and noise of active phase shifters.

Chapter 3

Linearity and Noise Analysis of Vector Modulators

3.1 Introduction

Vector-sum phase shifters employ active blocks such as VGAs and sometimes active quadrature signal generators and adders to perform phase tuning. The nonlinear behaviour of these blocks results in limited linearity presented by the overall system. Additionally, all the building blocks of the vector modulator practically generate low- or high-frequency noise and, therefore, limit the sensitivity of the overall system. Since the linearity and noise analysis of phase shifters, in general, are almost entirely uncovered in the literature, this chapter is dedicated to addressing this research gap by providing a detailed analysis of the effects of nonlinear and noisy blocks on the overall system performance.

3.2 Linearity Analysis of Quadrature Vector Modulators

3.2.1 Gain Compression

Consider the simple vector modulator in Figure 2.9(a) composed of an I/Q generator, VGAs, and an analog/vector adder. The quadrature generator is generally a balun/transformer and a PPF or QAF and, therefore, a passive block. Similarly, the vector adder may be implemented using a transformer [82] or a Wilkinson power combiner [85], [87], which are also passive blocks. Since passive blocks are inherently linear, the overall nonlinearity of the system emanates from the gain-tuning block (e.g., VGA). First, let us assume the two VGAs (VGA1 and VGA2) to be the only non-linear blocks. The third-order approximation of VGA1 output signal can be expressed as [124]:

$$y_{VGA1}(t) \approx \alpha_{11}x(t) + \alpha_{21}x^2(t) + \alpha_{31}x^3(t) \tag{3-1}$$

where α_{11}, α_{21}, and α_{31} are the small signal gain, the second- and third-order coefficients of VGA1, respectively. The time domain output equation of VGA2 is similar to that of VGA1 in (3-1), with α_{12}, α_{22}, and α_{32} its respective linear gain, second, and third-order coefficients. An input signal $x(t) = A\cos(\omega_0 t)$ to the phase shifter is equally split into $x_I(t) = \frac{1}{\sqrt{2}}A\cos(\omega_0 t)$ and $x_Q(t) = \frac{1}{\sqrt{2}}A\cos(\omega_0 t + 90°)$, which pass respectively by VGA1 and VGA2 before being combined to provide the output signal. Assuming that the vector generator and summer are lossless, and the only gain change experienced by the input signal is through the VGAs, the output amplitudes of the VGAs as well as the modulator are provided in Table 3.1

for different harmonics. It can be observed that the phase shift and amplitude of the fundamental frequency are given respectively as:

$$\varphi_O = \tan^{-1}\left(\frac{A_{12}}{A_{11}}\right) \tag{3-2}$$

$$A_O = \sqrt{{A_{11}}^2 + {A_{12}}^2} \tag{3-3}$$

where $A_{11} = \frac{\alpha_{11}A}{\sqrt{2}} + \frac{3\alpha_{31}A^3}{8\sqrt{2}}$ and $A_{12} = \frac{\alpha_{12}A}{\sqrt{2}} + \frac{3\alpha_{32}A^3}{8\sqrt{2}}$. Therefore, the fundamental frequency is composed of the first and third nonlinear coefficients of VGA1 (α_{11}, α_{31}) and VGA2 (α_{12}, α_{32}). Moreover, the DC and second-order harmonic components are composed of the second-order nonlinear coefficients of the VGAs. In addition, it is worth noting that the second-order harmonic of the system output is found by subtracting the second-order harmonic component of VGA2 from that of VGA1, resulting in a reduced second-order component at the output compared to individual VGA outputs. Like the fundamental frequency, the third-order harmonic will experience a phase shift $\varphi'_O = -\tan^{-1}\left(\frac{\alpha_{32}}{\alpha_{31}}\right)$, which depends on the third non-linear coefficients of the VGAs. Likewise, its amplitude also depends on α_{31} and α_{32}. Here, the fundamental and third-order harmonic components are of particular interest as they define the harmonic distortion of the system. The gain of the vector modulator is given as:

$$G_V = \frac{A_O}{A} = \frac{1}{\sqrt{2}}\sqrt{\left(\alpha_{11} + \frac{3\alpha_{31}A^2}{8}\right)^2 + \left(\alpha_{12} + \frac{3\alpha_{32}A^2}{8}\right)^2} \tag{3-4}$$

As the nonlinear coefficients of the VGAs are changed during phase tuning, the amplitude of the fundamental gain G_V of the modulator is changed as demonstrated by (3-4). Consequently, each phase state of the modulator exhibits a different nonlinear behaviour. If the first and third nonlinear coefficients are of opposite signs, the gain is compressive; otherwise, it is expansive. Since solid-state devices are compressive in nature, we shall consider α_{11}(or α_{12}) and α_{31}(or α_{32}) to be of opposite signs. The one-dB (1-dB) compression point is defined as the input or output voltage or power point where the ideal linear gain of the amplifier in decibels exceeds its actual compressed gain by 1 dB.

Table 3.1: Harmonic components of a vector modulator.

Harmonics		VGA1 output	VGA2 output	System output
DC		$\frac{\alpha_{21}A^2}{4}$	$\frac{\alpha_{22}A^2}{4}$	$\frac{\alpha_{21}A^2}{4}+\frac{\alpha_{22}A^2}{4}$
Fundamental	$\omega_0 t$	$A_{11}=\frac{\alpha_{11}A}{\sqrt{2}}+\frac{3\alpha_{31}A^3}{8\sqrt{2}}$	-	-
	$\omega_0 t+90°$	-	$A_{12}=\frac{\alpha_{12}A}{\sqrt{2}}+\frac{3\alpha_{32}A^3}{8\sqrt{2}}$	-
	$\omega_0 t+\varphi_O$	-	-	$\sqrt{{A_{11}}^2+{A_{12}}^2}$
2nd Harmonics	$2\omega_0 t$	$\frac{\alpha_{21}A^2}{4}$	-	$\frac{\alpha_{21}A^2}{2}-\frac{\alpha_{22}A^2}{2}$
	$2(\omega_0 t+90°)$	-	$\frac{\alpha_{22}A^2}{4}$	-
3rd Harmonics	$3\omega_0 t$	$A_{31}=\frac{\alpha_{31}A^3}{8\sqrt{2}}$	-	-
	$3(\omega_0 t+90°)$	-	$A_{32}=\frac{\alpha_{32}A^3}{8\sqrt{2}}$	-
	$3\omega_0 t+\varphi_O{}'$	-	-	$\sqrt{{A_{31}}^2+{A_{32}}^2}$

The ideal system linear gain is found when $\alpha_{31}=\alpha_{32}=0$. The resulting expression is:

$$G_{V,linear}=\frac{1}{\sqrt{2}}\sqrt{(\alpha_{11})^2+(\alpha_{12})^2} \tag{3-5}$$

Therefore, the 1-dB input compression point is found by solving the following equation:

$$20\log\left|G_{V,linear}\right|=20\log\left|G_V\left(A=A_{in,1dB}\right)\right|+1 \tag{3-6}$$

where $A_{in,1dB}$ is the 1-dB input compression voltage peak. From (3-4) through (3-6), the general expression of $A_{in,1dB}$ is formulated as:

$$A_{in,1dB}=\sqrt{\frac{-0.945(\alpha_{11}\alpha_{31}+\alpha_{12}\alpha_{32})+\sqrt{0.893(\alpha_{11}\alpha_{31}+\alpha_{12}\alpha_{32})^2-0.185({\alpha_{11}}^2+{\alpha_{12}}^2)({\alpha_{31}}^2+{\alpha_{32}}^2)}}{0.356({\alpha_{31}}^2+{\alpha_{32}}^2)}} \tag{3-7}$$

It appears from (3-7) that $A_{in,1dB}$ ranges from a minimum to a maximum value depending on the nonlinear coefficients of the VGAs. The minimum $A_{in,1dB}$ occurs when the output gain G_V is maximal and corresponds to the worst-case nonlinearity of the VGAs and, therefore, of the modulator. This is because stronger nonlinear behaviour occurs when the gain of the amplifier is larger [125] since its third nonlinear coefficient is proportional to its transconductance parameters, which are proportional to its gain. Additionally, the input 1-dB compression point of a VGA is somewhat linearly related to its gain for gain values above 0 dB [125]-[127], which are reasonable values for phase shifter applications. This implies the output 1-dB compression point and the maximum output power remain almost unchanged when the VGA bias current exceeds a threshold value. Meanwhile, G_V is maximal when α_{11}, α_{31}, α_{12} and α_{32} are all maximum. For simplicity, it is assumed that the VGAs are identical, implying their maximum nonlinear coefficients are equal: $\alpha_{11,max} = \alpha_{12,max} = \alpha_{1,max}$ and $\alpha_{31,max} = \alpha_{32,max} = \alpha_{3,max}$. Using these conditions in (3-4) and (3-7), the maximum gain and the corresponding $A_{in,1dB}$ of the system are therefore respectively expressed as:

$$G_{V,max} = \frac{A_{O,max}}{A} = \alpha_{1,max} + \frac{3}{8}\alpha_{3,max}A^2 \tag{3-8}$$

$$A_{in,1dB}^{min} = \sqrt{0.29\left|\frac{\alpha_{1,max}}{\alpha_{3,max}}\right|} \tag{3-9}$$

It can be inferred from (3-9) that the minimum input 1-dB compression point of a modulator phase shifter is dependent on the nonlinear coefficients of the VGAs at the maximum gain state. Moreover, the input 1-dB compression point of a single-ended amplifier is demonstrated in [124] to be $\sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$, where α_1 and α_3 are the first and third non-linear coefficients of the amplifier, respectively. Consequently, the minimum input 1-dB compression point is $\sqrt{2}$ times that of a single VGA at the maximum gain state. On the other hand, the maximum $A_{in,1dB}$ of the system occurs when the gains of the VGAs are minimum, implying $\alpha_{11,min} = \alpha_{12,min} = \alpha_{1,min}$ and $\alpha_{31,min} = \alpha_{32,min} = \alpha_{3,min}$.To this end, the maximum $A_{in,1dB}$ of the system is $\sqrt{2}$ times larger than the input 1-dB compression point of the VGAs at the minimum gain state and is expressed as:

$$A_{in,1dB}^{max} = \sqrt{0.29\left|\frac{\alpha_{1,min}}{\alpha_{3,min}}\right|} \tag{3-10}$$

The above nonlinearity study assumes all the building blocks of the modulator in Figure 2.7(a) are ideal and the only gain change experienced by the I and Q signals is through the VGAs. Next, we shall

examine the case where the I and Q branches experience different losses. The most common losses appear during the quadrature signal generation and addition, which are often performed by passive blocks. Moreover, loss and mismatch of the I and Q branches may occur during the layout design, undermining the expected output signal. Let L_1 and L_2 be the losses experienced by the I and Q branches, respectively. Assuming the VGAs are matched, and the losses are generated before the VGAs (e.g. the quadrature generator), the maximum system gain is determined by replacing A in the expressions of A_{11} and A_{12} from Table 3.1 by $L_1 A$ and $L_2 A$, respectively and using the maximum values for the nonlinear coefficients. The resulting gain is therefore found as:

$$G_{VL,max} = \frac{1}{\sqrt{2}}\sqrt{\left(\alpha_{1,max}L_1 + \frac{3\alpha_{3,max}{L_1}^3 A^2}{8}\right)^2 + \left(\alpha_{1,max}L_2 + \frac{3\alpha_{3,max}{L_2}^3 A^2}{8}\right)^2} \tag{3-11}$$

It can be inferred from (3-11) that the first and third nonlinear coefficients of VGA1 (or VGA2) are reduced by a factor of L_1 (or L_2) and ${L_1}^3$ (or ${L_2}^3$), respectively. Thus, the minimum $A_{in,1dB}$ is calculated by taking $\alpha_{11} = \alpha_{1,max}L_1$, $\alpha_{12} = \alpha_{1,max}L_2$, $\alpha_{31} = \alpha_{3,max}{L_1}^3$ and $\alpha_{32} = \alpha_{3,max}{L_2}^3$ in the general expression in (3-7). The resulting expression is:

$$A_{inL,1dB}^{min} = \sqrt{\frac{0.945\left({L_1}^4+{L_2}^4\right)-\sqrt{0.893\left({L_1}^4+{L_2}^4\right)^2-0.185\left({L_1}^2+{L_2}^2\right)\left({L_1}^6+{L_2}^6\right)}}{0.356\left({L_1}^6+{L_2}^6\right)}\left|\frac{\alpha_{1,max}}{\alpha_{3,max}}\right|} = K_L A_{in,1dB}^{max} \tag{3-12}$$

Consequently, the minimum $A_{in,1dB}$ is proportional to the minimum 1-dB input compression point of the lossless system and a function K_L which only depends on the loss factors L_1 and L_2. This function decreases as the value of L_1 and/or L_2 increases. For the lossless case ($L_1 = L_2 = 1$), the value of the function is predictably 1. As the branch losses increase, the minimum $A_{in,1dB}$ monotonically increases from the ideal lossless case. For instance, if $L_1 = L_2 = 0.1$, the corresponding input 1-dB compression point is $10A_{in,1dB}^{max}$, or 10 times that of the lossless case. Nevertheless, the output power is also reduced by almost the same factor. Therefore, the pre-VGA losses extend the system compression point. If the branch losses appear after the VGAs (e.g., the vector adder), the amplitudes of A_{11} and A_{12} will be respectively multiplied by the branch losses L_1 and L_2 before the vector synthesis. Thus, the maximum lossy system gain for matched VGAs becomes:

$$G_{VL,max} = \sqrt{\frac{{L_1}^2+{L_2}^2}{2}}\left(\alpha_{1,max} + \frac{3\alpha_{3,max}A^2}{8}\right) \tag{3-13}$$

Furthermore, the minimum input 1-dB compression point is found by using the non-linear coefficients $\alpha_{11} = \alpha_{1,max}L_1$, $\alpha_{12} = \alpha_{1,max}L_2$, $\alpha_{31} = \alpha_{3,max}L_1$ and $\alpha_{32} = \alpha_{3,max}L_2$ in (3-7). The corresponding minimum $A_{in,1dB}$ is the same as the lossless case in (3-9), whereas the output power will have a factor of $\frac{{L_1}^2+{L_2}^2}{2}$. Therefore, branch losses appearing after the VGAs do not affect the input 1-dB compression point. Consequently, the pre-VGA branch losses present better linearity performance compared to their post-VGA counterparts. In both cases, the branch losses reduce the system gain.

To validate the above theory, a simple vector modulator schematic was set up in the Keysight ADS environment, as seen in Figure 3.1. The schematic is composed of a quadrature generator (HYB1) followed by attenuators (ATTEN1, ATTEN2, ATTEN3 and ATTEN4), VGAs (X1 and X2), and a power combiner (PWR1). The VGAs are identical and modelled as third-order non-linear Verilog-AMS blocks. The model is based on a fixed maximum output power, and therefore, a fixed output 1-dB compression point, which is taken at 10 V_P. The nonlinear modulator is simulated with no branch loss, with pre-VGAs and post-VGAs branch losses, where $L_1 = 0.6$ or 4.44 dB and $L_2 = 0.9$ or 0.92 dB. Figure 3.2(a) represents the gain-versus-input voltage plot of the vector modulator and a standalone VGA for three different VGA gain states: 0 dB, 6.8 dB, and 10 dB. In this regard, the linear gain of VGA2 is maintained at the maximum state of 10 dB while that of VGA1 is stepped between 0 and 10 dB. It can be observed that the minimum input 1-dB compression point of the modulator is found when the linear gains of the VGAs are maximal and equal to 5.01 V_P. Additionally, the 1-dB compression point of the VGA occurs at 3.54 V_P, which is about $\sqrt{2}$ times less than that of the modulator. Figure 3.2(b) illustrates the gain plot with respect to the input voltage of the modulator system with pre-VGAs and post-VGAs losses. The gain of VGA1 is stepped from a minimum of 0 dB to a maximum of 10 dB, whereas that of VGA2 is fixed at 10 dB. Similar to the lossless system, the minimum $A_{in,1dB}$ of the pre-VGAs and post-VGAs lossy modulators occur when the VGA gains are maximum and are equal to 6.17 V_P and 5.03 V_P, respectively. The minimum $A_{in,1dB}$ of the modulator with post-VGAs branch losses are equal to that of the lossless system as previously stated. Moreover, the loss factor K_L of the pre-VGAs lossy system in (3-12) can be theoretically computed as 1.23. The simulated minimum $A_{in,1dB}$ of the corresponding lossy modulator is less than that of the lossless system by about the same factor. Finally, the modulator with pre-VGAs branch losses appears more linear than the one with post-VGA branch losses.

3.2.2 Gain and Phase Errors Caused by Harmonic Distortion

Gain compressions in vector modulators cause a deviation of the fundamental gain from its linear expected value and, therefore, create gain errors. The gain error (in dB) due to nonlinearities is obtained

by subtracting the linear gain in (3-5) (in dB) from the actual nonlinear gain (in dB) in (3-4) [128] as

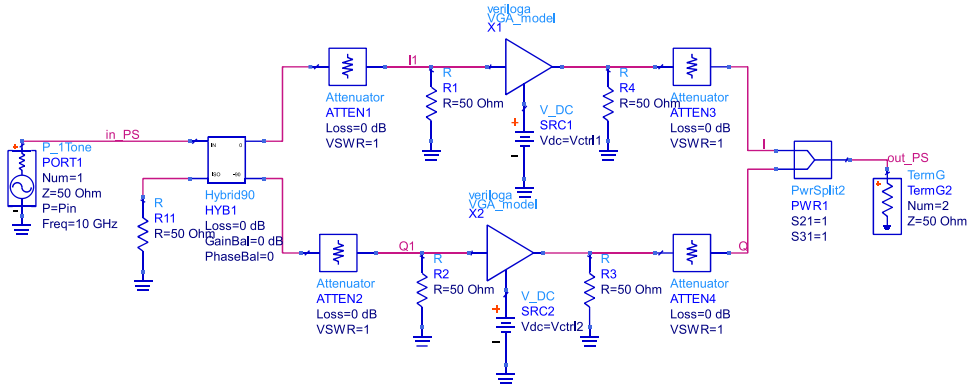


Figure 3.1: Schematic setup for block diagram simulation of a non-linear quadrature vector modulator.

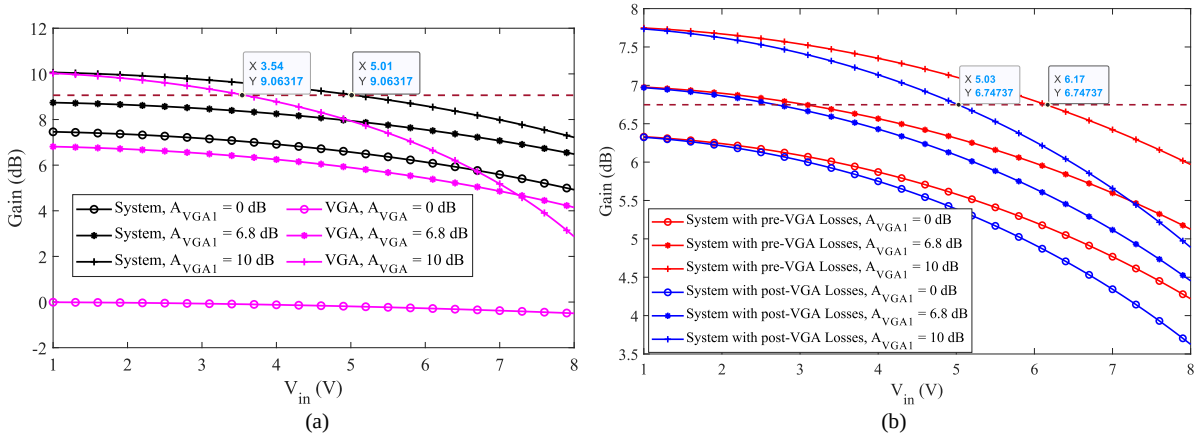


Figure 3.2: Plots of gain versus input voltage for (a) the nonlinear lossless modulator and the VGA and (b) the nonlinear lossy modulator.

follows:

$$\varepsilon_G = 20\log|G_V| - 20\log|G_{V,linear}| = 10\log\left|\frac{\left(\alpha_{11}+\frac{3\alpha_{31}A^2}{8}\right)^2+\left(\alpha_{12}+\frac{3\alpha_{32}A^2}{8}\right)^2}{(\alpha_{11})^2+(\alpha_{12})^2}\right| \quad (3\text{-}14)$$

It is obvious from (3-14) that the larger the amplitude of the input signal *A*, the larger the gain error. However, the effect of the VGA gains on the error is not straightforward. To analyze the behaviour of the gain error with respect to the VGAs' gains, it is important to understand the tuning mechanism of the modulator. To ensure minimum tuning gain imbalance and maximum average insertion loss, each tuning quadrant of a vector modulator requires one VGA to be fixed at the maximum gain state, while the other spans between the minimum and maximum gain states, as will be later described in Chapter 4. Let us assume VGA1 is fixed at the maximum gain state (e.g. $\alpha_{11} = \alpha_{1,max}$ and $\alpha_{31} = \alpha_{3,max}$) and the gain of VGA2 is varied between the minimum and the maximum gain states within the first quadrant.

The gain error in (3-14) will therefore become:

$$\varepsilon_G = 10\log\left|\frac{\left(\alpha_{1,max}+\frac{3\alpha_{3,max}A^2}{8}\right)^2+\left(\alpha_{12}+\frac{3\alpha_{32}A^2}{8}\right)^2}{(\alpha_{1,max})^2+(\alpha_{12})^2}\right| \tag{3-15}$$

For a tuning range smaller than the 1-dB input compression point, the maximum gain error occurs when $\alpha_{12} = \alpha_{1,max}$ and $\alpha_{13} = \alpha_{3,max}$. The maximum gain error for a lossless system is thus expressed as:

$$\varepsilon_{G,max} = 20\log\left|1-0.109\frac{A^2}{{A_{in,1dB}^{min}}^2}\right| \tag{3-16}$$

For a lossy system where the branch losses precede the VGAs, the maximum gain error can be obtained by using the lossy gain expression in (3-11). Knowing that the maximum linear gain for a lossless system is $\alpha_{1,max}$, the error becomes:

$$\varepsilon_{GL,max} = 10\log\left|\frac{1}{2}\left[{L_1}^2\left(1-0.109{L_1}^2\frac{A^2}{{A_{in,1dB}^{min}}^2}\right)^2+{L_2}^2\left(1-0.109{L_2}^2\frac{A^2}{{A_{in,1dB}^{min}}^2}\right)^2\right]\right| \tag{3-17}$$

From (3-17), the maximum gain error increases as the pre-VGA losses increase. In contrast, as L_1 and L_2 approach 0, the non-linear terms in the expression reduce. Consequently, the gain error generated by the nonlinearity of the system is reduced. However, the overall increase in the gain error is due to the gain mismatch caused by the losses L_1 and L_2. If the branch losses appear after the VGAs, the maximum gain error is calculated by using (3-13) and the maximum linear gain $\alpha_{1,max}$ as:

$$\varepsilon_{GL,max} = 20\log\left|\sqrt{\frac{{L_1}^2+{L_2}^2}{2}}\left(1+\frac{3}{8}A^2\left|\frac{\alpha_{3,max}}{\alpha_{1,max}}\right|\right)\right| = \varepsilon_{G,max}+10\log\left[\frac{1}{2}\left({L_1}^2+{L_2}^2\right)\right] \tag{3-18}$$

From (3-18), it appears that the gain error emanating from post-VGA branch losses is equivalent to the sum of the nonlinear lossless gain error and the errors caused by the branch loss-induced gain mismatch. This indicates that the post-VGA branch losses do not affect the non-linear gain error. In this regard, a non-linear modulator with pre-VGA branch losses outperforms its post-VGA counterpart in terms of gain error.

Similar to the gain error, the phase error measures the discrepancy between the expected phase state and the actual phase of the modulator. The phase shift generated by a lossless vector modulator with a

third-order nonlinear approximation is given in (3-2). The ideal phase shift is obtained by setting the third nonlinearity coefficients to 0 ($\alpha_{31} = \alpha_{32} = 0$), and the result is found as:

$$\varphi_{O,linear} = \tan^{-1}\left(\frac{\alpha_{12}}{\alpha_{11}}\right) \tag{3-19}$$

As a result, the general expression for the phase error is given as:

$$\varepsilon_{\varphi} = \varphi_O - \varphi_{O,linear} = \tan^{-1}\left(\frac{\alpha_{12}+0.375A^2\alpha_{32}}{\alpha_{11}+0.375A^2\alpha_{31}}\right) - \tan^{-1}\left(\frac{\alpha_{12}}{\alpha_{11}}\right) \tag{3-20}$$

The general phase error expression in (3-20) demonstrates that the error augments as the input amplitude increases. For the first tuning quadrant, $\alpha_{11} = \alpha_{1,max}$ and $\alpha_{31} = \alpha_{3,max}$, while α_{12} and α_{32} are tuned. When $\alpha_{12} = \alpha_{1,max}$ and $\alpha_{32} = \alpha_{3,max}$, the nonlinear phase error is null. As α_{12} and α_{32} decrease and diverge from their respective maximum values, ε_{φ} becomes larger and eventually peaks within the gain tuning range. If $\alpha_{1,min} > 1$ or 0 dB, the maximum phase error is generated at approximately the minimum gain tuning state of VGA2. Likewise, in the second quadrant, where VGA2 is fixed at the maximum gain state and VGA1 is tuned, the phase error is maximal for $\alpha_{11} \approx \alpha_{1,min}$ and $\alpha_{31} \approx \alpha_{3,min}$ if $\alpha_{1,min} > 1$. The maximum phase errors for the two quadrants are therefore respectively represented as:

$$\varepsilon^1_{\varphi,max} \approx \tan^{-1}\left(\frac{\alpha_{1,min}+0.375A^2\alpha_{3,min}}{\alpha_{1,max}+0.375A^2\alpha_{3,max}}\right) - \tan^{-1}\left(\frac{\alpha_{1,min}}{\alpha_{1,max}}\right) \tag{3-21}$$

$$\varepsilon^2_{\varphi,max} \approx \tan^{-1}\left(\frac{\alpha_{1,max}+0.375A^2\alpha_{3,max}}{\alpha_{1,min}+0.375A^2\alpha_{3,min}}\right) - \tan^{-1}\left(\frac{\alpha_{1,max}}{\alpha_{1,min}}\right) \tag{3-22}$$

It can be concluded from (3-21) and (3-22) that the maximum phase errors due to nonlinearities in each tuning quadrant arise when the gain of one VGA is minimum while that of the other is maximum or vice-versa. In addition, using the trigonometric identity $\tan^{-1}(a) = \pi/2 - \tan^{-1}(1/a)$, $\varepsilon^1_{\varphi,max} = -\varepsilon^2_{\varphi,max}$. If there exist pre-VGA losses in the generated vector branches, the phase errors can be determined by taking $\alpha_{11} = L_1\alpha_{1,max}$, $\alpha_{31} = {L_1}^3\alpha_{3,max}$, $\alpha_{12} = L_2\alpha_{1,min}$ and $\alpha_{32} = {L_2}^3\alpha_{3,min}$ in the first inverse tangent ($\tan^{-1}$) term for the first quadrant. These values become $\alpha_{11} = L_1\alpha_{1,min}$, $\alpha_{31} = {L_1}^3\alpha_{3,min}$, $\alpha_{12} = L_2\alpha_{1,max}$ and $\alpha_{32} = {L_2}^3\alpha_{3,max}$ for the second tuning quadrant.

The resulting maximum phase errors are formulated as:

$$\varepsilon_{\varphi L,max}^{1} \approx \tan^{-1}\left(\frac{L_1}{L_2}\frac{\alpha_{1,min}+0.375{L_1}^2A^2\alpha_{3,min}}{\alpha_{1,max}+0.375{L_2}^2A^2\alpha_{3,max}}\right) - \tan^{-1}\left(\frac{\alpha_{1,min}}{\alpha_{1,max}}\right) \tag{3-23}$$

$$\varepsilon_{\varphi L,max}^{2} \approx \tan^{-1}\left(\frac{L_1}{L_2}\frac{\alpha_{1,max}+0.375{L_1}^2A^2\alpha_{3,max}}{\alpha_{1,min}+0.375{L_2}^2A^2\alpha_{3,min}}\right) - \tan^{-1}\left(\frac{\alpha_{1,max}}{\alpha_{1,min}}\right) \tag{3-24}$$

As seen from the above expressions, the terms with the third nonlinear coefficients dissipate as L_1 and L_2 approach 0. This implies that the phase errors due to nonlinearities of the VGAs are reduced by the pre-VGA branch losses. In contrast, the phase errors due to the branch mismatch persist and are proportional to L_1/L_2. In the case of post-VGA branch losses, the third nonlinear coefficients will be multiplied by L_1 or L_2 instead of ${L_1}^3$ or ${L_2}^3$. The obtained maximal phase errors for the first and second quadrants are therefore represented as:

$$\varepsilon_{\varphi L,max}^{1} = \tan^{-1}\left(\frac{L_1}{L_2}\frac{\alpha_{1,min}+0.375A^2\alpha_{3,min}}{\alpha_{1,max}+0.375A^2\alpha_{3,max}}\right) - \tan^{-1}\left(\frac{\alpha_{1,min}}{\alpha_{1,max}}\right) \tag{3-25}$$

$$\varepsilon_{\varphi L,max}^{2} = \tan^{-1}\left(\frac{L_1}{L_2}\frac{\alpha_{1,max}+0.375A^2\alpha_{3,max}}{\alpha_{1,min}+0.375A^2\alpha_{3,min}}\right) - \tan^{-1}\left(\frac{\alpha_{1,max}}{\alpha_{1,min}}\right) \tag{3-26}$$

The expressions (3-25) and (3-26) demonstrate that the post-VGA losses affect the nonlinear phase errors by a factor of L_1/L_2, which indicates the mismatch of the branches. Predictably, the pre-VGA nonlinear phase errors are smaller than their post-VGA counterparts. Meanwhile, it is worth noting that the phase and gain errors of a vector modulator caused by nonlinearities have more or less opposite characteristics within each tuning quadrant: When one increases, the other decreases, creating somehow a trade-off between the phase and gain errors.

The schematic setup in Figure 3.1 was used to simulate the gain and phase errors of the nonlinear lossless and lossy vector modulators. For the lossy systems, the branch losses have been maintained as $L_1 = 4.44$ dB and $L_2 = 0.92$ dB. The gain and phase plots with respect to the VGA gain of the nonlinear lossless system, as well as the system with linear VGAs, are provided in Figure 3.3(a) and Figure 3.3(b), respectively, for different input signals. For smaller input voltages (e.g. V_{in} = 4 V_P), both the gain and the phase of the nonlinear system are closer to those of its linear counterpart. As the input voltage increases beyond the minimum $A_{in,1dB}$, previously found at 5.01 V_P, the phase and gain curves become more and more distant from their linear system counterparts. This consequently creates larger errors as can be observed from Figure 3.4(a) and Figure 3.4(b), which depict respectively the gain and phase errors of

lossless and lossy nonlinear systems. It is clear from Figure 3.4(a) that higher input voltages and losses negatively affect the gain error of the quadrature modulator. In addition, the worst-case gain errors are obtained when both VGA gains are maximum, and the pre-VGA lossy system outperforms its post-VGA counterparts in terms of gain error. On the other hand, while the post-VGA branch losses destructively

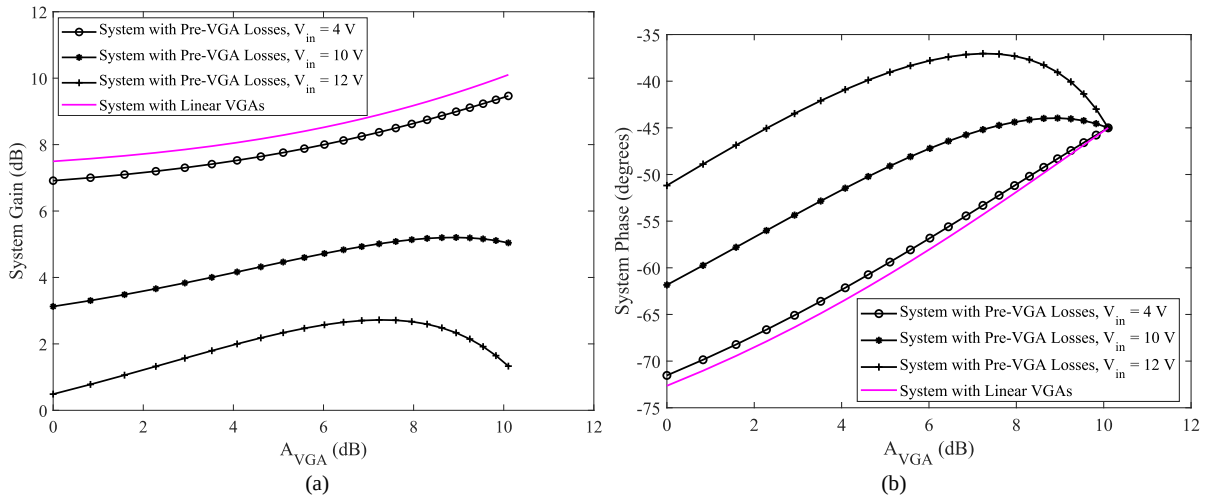


Figure 3.3: Plots of the lossless nonlinear and linear modulator (a) gain and (b) phase versus VGA gain.

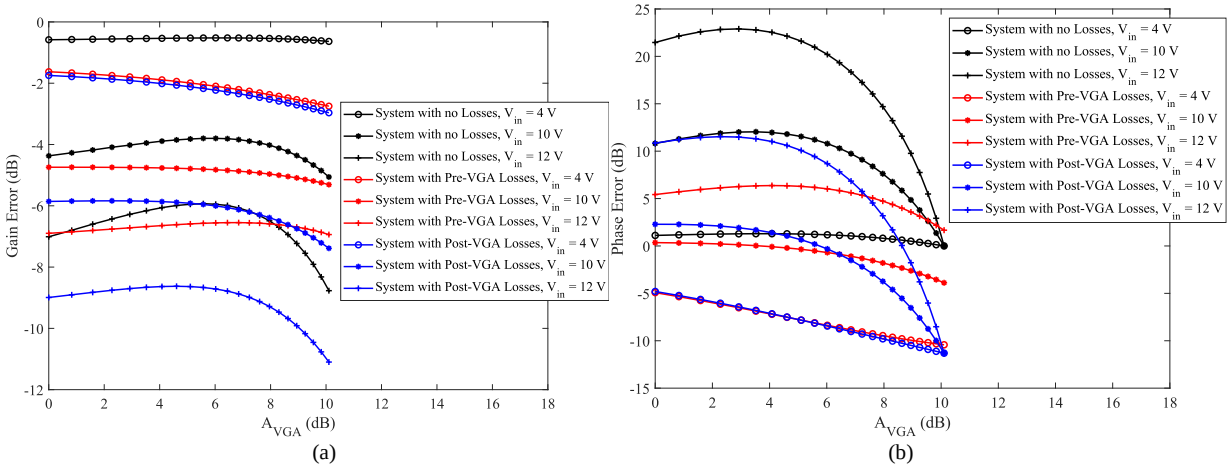


Figure 3.4: (a) Gain and (b) phase error plots of the nonlinear lossless and lossy modulators with respect to VGA gain.

affect the phase error of the non-linear system, the influence of the pre-VGA losses on the modulator is somewhat complex. For lower input Voltages (e.g. voltages below the minimum input 1-dB compression point), the branch losses increase the system phase error, which is negative.

As the input voltage increases, the phase error converges to positive values passing through the 0˚ line. Therefore, pre-VGA branch attenuations can be used to correct the phase errors caused by the

nonlinear characteristics of the VGAs, but at the cost of reduced system gain. Meanwhile, the maximum phase error in each tuning case appears at the minimum tuning VGA gain or close by.

3.2.3 Interferer Effects

RF phase shifters are typically desired to operate at a single carrier frequency. Nevertheless, one or more undesired signals at the receiver bandwidth may be captured by the antennas and subsequently processed by the phase shifter along the receiver chain. These unwanted signals are called interferers and may affect both the phase and the amplitude of vector modulators.

Let us first consider one interferer signal $x_1(t) = A_1 \cos(\omega_{01} t)$ is inputted to the modulator with nonlinear VGAs along with the desired signal $x(t) = A \cos(\omega_0 t)$. Assuming the VGAs can be modelled in a third-order nonlinear approximation represented in (3-1), the amplitudes and phases of the fundamental output frequency of the desired signal (ω_0) are given in Table 3.2 for the VGAs and the system. As seen from Table 3.2, the gain and phase of the modulator's desired frequency component are dependent on the square of the amplitude of the interferer component. Therefore, the interferer causes a nonlinear effect on the vector modulator. To evaluate the effect of the interferer signal, let us assume the modulator operates at its linear input range for all phase states (i.e. $A < A_{in,1dB}^{min}$). The effect of the interferer becomes prominent when $A_1 \gg A$. In this case, the nonlinear terms of the VGAs' amplitudes as well as the amplitude of the modulator depend only on the interferer's amplitude and the third nonlinear coefficients. The nonlinearity caused by the interferer induces not only gain compression but also gain and phase errors of the modulator. The maximum gain and phase errors of a lossless vector modulator with an input interferer are, respectively found as:

$$\varepsilon_{G,int}^{max} = 20 \log \left| 1 - 0.218 \frac{{A_1}^2}{{A_{in,1dB}^{min}}^2} \right| \tag{3-27}$$

$$\varepsilon_{\varphi,int}^{max} \approx \tan^{-1}\left(\frac{\alpha_{1,min} + 0.75{A_1}^2 \alpha_{3,min}}{\alpha_{1,max} + 0.75{A_1}^2 \alpha_{3,max}}\right) - \tan^{-1}\left(\frac{\alpha_{1,min}}{\alpha_{1,max}}\right) \tag{3-28}$$

It is worth mentioning that the maximum phase error expressed in (3-28) is approximate and assumes that the minimum gain of the VGAs is over 0 dB. Moreover, it can be observed that the gain and phase errors generated by an interferer are analogous to those due to the nonlinear characteristics of the VGAs, as proven in (3-16) and (3-21). For sufficiently large values of A_1, the VGA gain may be desensitized and nullified if it is compressive ($\alpha_1 \alpha_3 < 0$) and thus, the interferer becomes a blocker. The

minimum amplitude of the interferer required to block the VGA's signal can be found when it is at its minimum gain state ($\alpha_{11} = \alpha_{12} = \alpha_{1,min}$ and $\alpha_{31} = \alpha_{32} = \alpha_{3,min}$) and by equating A_{11} to 0, leading to:

$$A_{block,VGA}^{min} = \sqrt{\frac{4}{3}\left|\frac{\alpha_{1,min}}{\alpha_{3,min}}\right|} \tag{3-27}$$

Table 3.2: Amplitude and phase of the desired frequency of a nonlinear modulator with a single interferer.

	Amplitude	**Phase (rad)**
VGA1	$A_{11} = \frac{A}{\sqrt{2}}\left[\alpha_{11} + \frac{3\alpha_{31}}{4}\left(A^2/2 + {A_1}^2\right)\right]$	0
VGA2	$A_{12} = \frac{A}{\sqrt{2}}\left[\alpha_{12} + \frac{3\alpha_{32}}{4}\left(A^2/2 + {A_1}^2\right)\right]$	$\pi/2$
System	$\sqrt{{A_{11}}^2 + {A_{12}}^2}$	$\tan^{-1}\left(\frac{A_{12}}{A_{11}}\right)$

This quantity also corresponds to the minimum third-order intercept point of the individual VGA, which is essentially a point where the amplitude of a third-order intermodulation product intersects that of the fundamental in the case of two interferers inputted to an amplifier. Despite significantly reducing the system gain, the complete desensitization of only one VGA does not entirely nullify the vector modulator signal. To completely block the modulator signal, both vector branches must be identical, and the VGAs must maintain the same gain state. In this regard, the system blocking occurs only when both VGAs hold their maximum values in a typical phase-tuning quadrant. As a result, the blocking signal of the modulator is formulated as:

$$A_{block} = \sqrt{\frac{4}{3}\left|\frac{\alpha_{1,max}}{\alpha_{3,max}}\right|} \tag{3-28}$$

Even though each gain state of the VGA has its corresponding blocking signal, which leads to a crucial decrease in the system gain, the complete desensitization of the modulator only occurs when the amplitude of the interferer equals A_{block}, which also corresponds to the blocking signal of the VGA at its maximum gain state. It is worth noting that A_{block} is 2.14 times larger than the minimum 1-dB compression point or 6.63 dBV larger than the input 1-dB compression point. By suppressing the amplitude of the vector modulator, the blocker signal causes serious gain and phase errors.

Let us now assume there exist losses on the modulator branches. By maintaining the assumption that the vector modulator is operating in the linear region and the interferer signal is relatively much larger than the input desired signal, the nonlinear terms of the modulator are independent of A but dependent on A_1. In this regard, the pre-VGA and post-VGA branch losses exhibit identical behaviours as for the nonlinear modulator without an interferer studied in the previous sections. Therefore, the respective maximum gain and phase errors may be found by simply replacing A^2 by $2{A_1}^2$ in (3-17), (3-18), (3-23) and (3-24). On the other hand, a complete blocking occurs only if $L_1 = L_2$. For $L_1 = L_2$, the blocking for a post-VGA lossy modulator is found by multiplying A_{11} by L_1 and equating the result to 0. The result found is the same as in (3-27). Nevertheless, the blocking signal in a modulator with pre-VGA branch losses may be found by replacing A_1 by $L_1 A_1$ in the expression of the minimum A_{11} from Table 3.2 and setting the resulting expression to 0. The resulting blocking input signal is:

$$A_{block,L} = \frac{1}{L_1}\sqrt{\frac{4}{3}\left|\frac{\alpha_{1,max}}{\alpha_{3,max}}\right|} = \frac{A_{block}}{L_1} \tag{3-29}$$

Clearly from (3-29), the minimum interference signal required to block a modulator with pre-VGA loss is increased by a factor of $1/L_1$ compared to its post-VGA lossy and lossless counterparts.

Next, we shall consider the effect of two different interferers $x_1(t) = A_1\cos(\omega_{01}t)$ and $x_2(t) = A_2\cos(\omega_{02}t)$ on the system. In this case, the total input signal is the sum of the desired signal $x(t) = A\cos(\omega_0 t)$ and the two interferers. Assuming the VGAs can be modelled as third-order nonlinear blocks, the system output produces harmonic components, but also intermodulation (IM) products that can potentially affect the fundamental desired signal. In particular, the third-order IM products are the closest to the fundamental signal and therefore may fall in the desired band. Table 3.3 provides the amplitudes of the fundamental and third-order IM products of the VGAs and the system. It can be observed from the table that the interferers cause gain compression as their magnitudes A_1 and A_2 appear in the amplitude expression of the fundamental frequency. Consequently, gain and phase errors are generated, likewise the single interferer case studied before. In addition, if $A_1 + A_2$ is large enough, the VGAs and the system output signal may eventually be blocked. For $A_1 = A_2$, the minimum signal required to nullify the system gain corresponds to half of the blocking signal amplitude expressed in (3-27). Despite the effect of gain compression, the interferers generate third-order IM products such as $2\omega_{01} - \omega_{02}$ and $2\omega_{02} - \omega_{01}$ that fall near the fundamental desired signal and potentially corrupt it. In this regard, the third-order intercept point (IP3) may be used to evaluate the linearity of the vector modulator, as for the amplifier. To determine the input IP3 (IIP3) of the modulator, its linear gain expressed in (3-5) is equated to its third-order IM gain.

Assuming $A_1 = A_2 = A$, the general expression of the IIP3 is found as:

$$A_{IIP3} = \sqrt{\frac{8}{3}\sqrt{\frac{{\alpha_{11}}^2+{\alpha_{12}}^2}{{\alpha_{31}}^2+{\alpha_{32}}^2}}} \tag{3-30}$$

Table 3.3: Amplitudes of desired frequency and third order IM products of a nonlinear modulator with two interferers.

	$\boldsymbol{\omega_0}$	$\boldsymbol{2\omega_{01} \pm \omega_{02}}$	$\boldsymbol{2\omega_{02} \pm \omega_{01}}$
VGA1	$A_{11} = \frac{A}{\sqrt{2}}\left[\alpha_{11} + \frac{3\alpha_{31}}{4}\left(A^2/2 + {A_1}^2 + {A_2}^2\right)\right]$	$\frac{3\alpha_{31}}{8\sqrt{2}}{A_1}^2 A_2$	$\frac{3\alpha_{31}}{8\sqrt{2}}{A_2}^2 A_1$
VGA2	$A_{12} = \frac{A}{\sqrt{2}}\left[\alpha_{12} + \frac{3\alpha_{32}}{4}\left(A^2/2 + {A_1}^2 + {A_2}^2\right)\right]$	$\frac{3\alpha_{32}}{8\sqrt{2}}{A_1}^2 A_2$	$\frac{3\alpha_{32}}{8\sqrt{2}}{A_2}^2 A_1$
System	$\sqrt{{A_{11}}^2 + {A_{12}}^2}$	$\frac{3}{8\sqrt{2}}{A_1}^2 A_2\sqrt{{\alpha_{31}}^2 + {\alpha_{32}}^2}$	$\frac{3}{8\sqrt{2}}{A_2}^2 A_1\sqrt{{\alpha_{31}}^2 + {\alpha_{32}}^2}$

Provided that a typical tuning is performed by holding one VGA at its maximum gain state while varying the gain of the other, the minimum input IP3 is found when all VGAs attain their maximum gain values (i.e. $\alpha_{11} = \alpha_{12} = \alpha_{1,max}$ and $\alpha_{31} = \alpha_{32} = \alpha_{3,max}$). Therefore, (3-30) becomes:

$$A_{IIP3}^{min} = \sqrt{\frac{8}{3}\frac{\alpha_{1,max}}{\alpha_{3,max}}} \tag{3-31}$$

The minimum IIP3 of the modulator expressed in (3-31) corresponds to $\sqrt{2}$ times that of the individual VGA or the minimum blocking signal for a single inference. Moreover, the ratio of the minimum IIP3 to the minimum $A_{in,1dB}$ is 3.03 or 9.6 dB. Therefore, the minimum input IP3 of a Vector modulator with nonlinear VGAs lies 9.6 dBV beyond its minimum input 1-dB compression point, similar to a nonlinear amplifier [124]. In the presence of post-VGA losses, both the linear and nonlinear terms of the VGAs' outputs are multiplied by the same loss factors (L_1 or L_2). Thus, the input IP3 of a post-VGA lossy modulator remains the same as its lossless counterpart in (3-31). In contrast, if the losses appear

before the VGAs, the interferers experience branch losses before being subjected to the nonlinear characteristics of the VGAs. Consequently, the minimum IIP3 of a vector modulator phase shifter with pre-VGA losses can be found by setting $\alpha_{11} = L_1\alpha_{1,max}$, $\alpha_{12} = L_2\alpha_{1,max}$, $\alpha_{31} = {L_1}^3\alpha_{3,max}$ and $\alpha_{32} = {L_2}^3\alpha_{3,max}$ in (3-31).

Assuming that $L_1 \leq L_2$, the minimum input IP3 for all phase quadrants is:

$$A_{IIP3,L}^{min} = \sqrt{\frac{8}{3}\frac{\alpha_{1,max}}{\alpha_{3,max}}\sqrt{\frac{{L_1}^2+{L_2}^2}{{L_1}^6+{L_2}^6}}} = A_{IIP3}^{min}\sqrt{\sqrt{\frac{{L_1}^2+{L_2}^2}{{L_1}^6+{L_2}^6}}} \tag{3-32}$$

The minimum IIP3 in (3-32) demonstrates that the pre-VGA losses augment the linear range of the nonlinear modulator. As for the gain compression studied in the previous sections, pre-VGA losses exhibit better performance in terms of the overall linearity of the vector modulator.

The setup in Figure 3.1 was used to perform a nonlinearity simulation with input interferers. The VGAs are modelled as third-order nonlinear blocks with an output 1-dB compression point at 10 V and a linear gain range from 0 dB to 10 dB, as before. First, the output-input voltage characteristics of the modulator were retrieved with an input desired signal of 1 V_P, which is within the linear input range of the system, and a single interferer. The input desired and interferer frequencies are 10 GHz and 11 GHz, respectively. The magnitude of the interferer spans from 1 V_P to 20 V_p.

Figure 3.5(a) illustrates the output peak voltage with respect to the input interferer peak voltage at three different VGA gain states: 0 dB, 6 dB and 10 dB. It can be observed from the figure that the output voltage decreases with the interferer input voltage before reaching a minimum value. After reaching the minimum value, the output voltage increases with increasing input interferer voltage, implying the complete desensitization of the system. In addition, the output goes to zero when the VGA gain is maximal, and the input interferer voltage is 10. 63 V_P. This corresponds to the input-blocking signal. The previously found minimum 1-dB compression point is 5.01 V, which is about 2.12 times less than the blocking signal, and, hence, validating the theoretical estimation. Moreover, Figure 3.5(b) represents the output voltage versus the interferer voltage at the maximum VGA gains for the lossless, pre-VGA lossy and post-VGA lossy systems with a loss factor of $L_1 = L_2 = 0.6$ (or 4.4 dB). It can be seen that the blocking occurs at an interferer signal of 10.63 V_P for both the lossless and post-VGA lossy systems. On the other hand, the blocking occurs at an interferer input signal of 17.72 V_P for the pre-VGA lossy system. Given that the $A_{block} = 10.63\ V_P$ for the lossless system, the blocking signal for the lossy system can be estimated from (3-29) as 17.72 V_P, validating the simulated result. Next, the simulations were performed

with two input interferers with equal amplitudes. The interferer frequencies are 9 GHz and 11 GHz, producing relevant third-order IM products (IM3) at 7 GHz and 13 GHz. Fig. 3.6(a) depicts the output voltage versus the interferer input voltage of the fundamental frequency as well as the IM3 in decibels for the lossless modulator. The figure shows that the minimum input IP3 is found at 23.58 dBV when the VGA gain is maximal. This value is about 9.58 dBV greater than the minimum $A_{in,1dB}$, which is $20\log(5.01) = 14\ dBV$.

Hence, the theoretical and simulation minimum IIP3 values of the modulator are approximately equal. Moreover, the minimum IIP3 of lossy systems with $L_1 = 0.6$ and $L_2 = 0.9$ are generated in Fig. 3.6(b). The found minimum IIP3 of the post-VGA lossy system is equivalent to that of the lossless system. Meanwhile, the minimum IIP3 of the pre-VGA lossy system is found at 25.1 dBV. This value converges with the theoretical one in (3-32), which is 25.11 dBV.

The study of the nonlinearity in the above sections is based on the third-order nonlinear approximation of the VGA, which generally holds for the quadrature approximation of the MOSFET drain current (I_D) with respect to its gate-source voltage (V_{GS}).

For instance, the first and third non-linear coefficients of a differential pair can be determined using the Taylor series approximation as [125], [129]:

$$\alpha_1 = 0.5 g_{m1} \tag{3-33}$$

$$\alpha_3 = -\frac{1}{16}\frac{{K_1}^2}{g_{m1}} \tag{3-34}$$

where g_{m1} and K_1 are the transconductance and the transconductance constant of the input transistor, respectively. Changing the gain of the amplifier involves changing both α_1 and α_3. Nevertheless, the

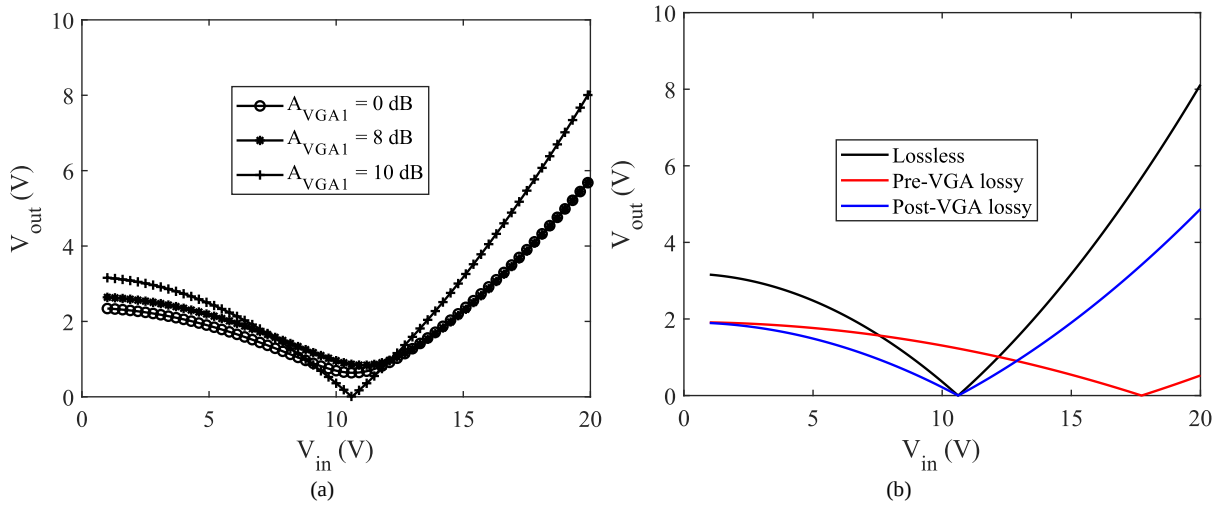


Figure 3.5: Plot of output voltage versus single interferer input voltage for (a) the lossless modulator with different VGA gain states and (b) lossless and lossy modulator with the VGA gain at 10 dB.

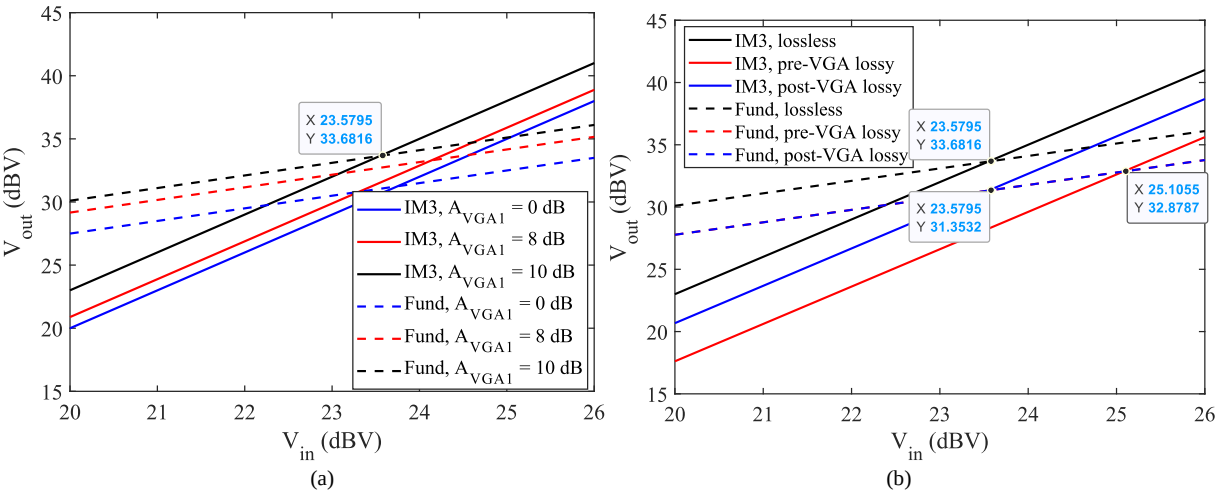


Figure 3.6: Plot of IP3 of (a) the lossless modulator with different VGA gain states and (b) the lossless and lossy modulators with the VGA gain at 10 dB.

overall change in the non-linear coefficients results in a monotonic gain increase for input signals less than the 1-dB compression point of the amplifier. On the other hand, the deep sub-micron technology does not necessarily obey the square-law relation of the I_D-V_{GS} curve in the saturation region. Instead, I_D is expressed in function of V_{GS} to the order of a constant α as follows [130]:

$$I_{D,SAT} = B\frac{W}{L_{eff}}(V_{GS} - V_{TH})^{\alpha}(1 + \lambda V_{DS}) \tag{3-35}$$

where V_{DS}, V_{TH}, B, λ, W, and L_{eff} are the drain-source voltage, the threshold voltage, the transconductance parameter, the channel length modulation, the width, and the effective length of the MOSFET, respectively. The carrier velocity saturation index α may take any value between 1 and 2.

Therefore, $I_{D,SAT}$ may be often more accurately approximated using Taylor's series with an order greater than 3. This implies that higher-odd nonlinear coefficients may contribute to the gain compression and affect the interference effects on the linearity of the system, as well as amplify the gain and phase errors of the vector modulator.

3.3 Noise Analysis of Quadrature Vector Modulators

Noise in electronic circuit design is generally defined as any unwanted signal randomly affecting the desired one. The noise can be from external or internal sources. The external noise may be caused by natural events such as lightning discharges, in which case it is called atmospheric noise. It may also be due to intermodulation or cross-modulation effects of interferers as described in the previous section. In contrast, the internal noise is caused by the noisy building components of the circuit, such as resistors and transistors. There exist many internal noise types, including thermal noise, flicker or 1/f noise, shot noise, bursting or popcorn noise… Nevertheless, the most common and significant noises generated by electronic circuits are the thermal, flicker, and shot noises [124].

The shot is the random crossing of electrons or holes of a p-n junction through the application of a DC power [131]. Therefore, the shot noise only concerns diodes and bipolar junction transistors (BJTs). The shot noise power per Hz of a device is constant. Thus, it is a "white noise". Meanwhile, most modern solid-state circuits use field-effect transistors (FETs) instead of BJTs due to their better power, area and switching performances. In this regard, this section will focus on the MOSFET-based phase shifters and thus the shot noise is irrelevant to this noise study. Moreover, the 1/f noise is a frequency-dependent noise in transistors and resistors that is dominant at low frequencies. It is referred to as flicker noise for transistors and excess noise for resistors. The 1/f noise dominates the overall noise of the device for frequencies less than the corner frequency, beyond which the thermal noise (or white noise in general) prevails. Typically, the corner frequency of MOSFETs is in the megahertz range [132], though that of deep sub-micron devices can reach the lower gigahertz frequency range. As a result, the flicker noise is mostly irrelevant for active phase shifters, which generally operate in the upper gigahertz frequencies. However, for modulators using injection-locked quadrature generators, the 1/f noise becomes important as the lower frequency noise is translated into phase noise [133]. Consequently, the generated I and Q signals will have phase noise. If the phase noises of the I and Q signals are $\varphi_{NI}(t)$ and $\varphi_{NQ}(t)$, respectively, the signals may be respectively represented as $x_I(t) = \frac{A}{\sqrt{2}}\cos[\omega_0 t + \varphi_{NI}(t)]$ and $x_Q(t) = \frac{A}{\sqrt{2}}\cos\left[\omega_0 t + \pi/2 + \varphi_{NQ}(t)\right]$. Assuming the rest of the system is lossless, noiseless and linear, the gain and phase of the modulator can be respectively formulated as:

$$G_V = \frac{1}{\sqrt{2}}\sqrt{\left[\alpha_{11}\cos\varphi_{NI}(t) - \alpha_{12}\sin\varphi_{NQ}(t)\right]^2 + \left[\alpha_{11}\sin\varphi_{NI}(t) + \alpha_{12}\cos\varphi_{NQ}(t)\right]^2} \quad (3\text{-}36)$$

$$\varphi_O = \tan^{-1}\left[\frac{\alpha_{11}\sin\varphi_{NI}(t)+\alpha_{12}\cos\varphi_{NQ}(t)}{\alpha_{11}\cos\varphi_{NI}(t)-\alpha_{12}\sin\varphi_{NQ}(t)}\right] \quad (3\text{-}37)$$

where α_{11} and α_{12} are the linear gains of VGA1 and VGA2, respectively. From (3-36) and (3-37), it can be observed that both the gain (or amplitude) and the phase of the vector modulator are modulated by the phase noises of the I and Q signals. These undesired modulations result in random time domain amplitude and phase fluctuations of the output signal, called "jitter". Therefore, a jitter in the vector generator induces a jitter in the modulator output. Since the noise phenomenon is random, it is best represented by its power per bandwidth. Assuming the phase noise power of an I/Q generator is *PN* (in dBc/Hz), its jitter (in radians) can be expressed as follows [134]:

$$J_{RMS} = \sqrt{2 \times \sum \int_{f_1}^{f_2} 10^{PN(f)/10} df} \quad (3\text{-}38)$$

where f_1 and f_2 are the lower and upper frequency offsets, $PN(f)$ the phase noise function between f_1 and f_2, and J_{RMS} the RMS phase jitter in radians. With the RMS jitters of the I and Q signals noted as $J_{RMS,I}$ and $J_{RMS,Q}$, respectively, an estimate of the phase and amplitude errors can be done by using these values in place of the time domain phase noises in (3-36) and (3-37). Due to its arbitrary nature, the amplitude of the time domain noise is indeterministic. This implies that every tuning state of the VGA displays different time domain noise signals. In addition, the square of the flicker noise voltage is proportional to the dimension of the transistor, the process parameters and the inverse of the frequency [135]. Since the tuning of the VGAs does not typically involve any of these parameters related to the vector generator and for small gain tuning ranges, the phase noise power remains more or less constant for any given VGA gain state and the RMS jitter of the I signal is approximately equal to that of the Q signal ($J_{RMS,I} \approx J_{RMS,Q} = J_{RMS}$). It follows that the average gain and phase errors produced by a vector modulator with I and Q signals containing phase noises can be estimated as:

$$\varepsilon_G = 10\log\left[\frac{(\alpha_{11}\cos J_{RMS}-\alpha_{12}\sin J_{RMS})^2+(\alpha_{11}\sin J_{RMS}+\alpha_{12}\cos J_{RMS})^2}{{\alpha_{11}}^2+{\alpha_{12}}^2}\right] = 0\ dB \quad (3\text{-}39)$$

$$\varepsilon_\varphi = \tan^{-1}\left[\frac{\alpha_{11}\sin J_{RMS}+\alpha_{12}\cos J_{RMS}}{\alpha_{11}\cos J_{RMS}-\alpha_{12}\sin J_{RMS}}\right] - \tan^{-1}\left[\frac{\alpha_{12}}{\alpha_{11}}\right] = J_{RMS} \quad (3\text{-}40)$$

It can be observed from (3-39) that the gain error produced by the modulator with a fixed noise power is zero. It is worth noting that these errors (gain and phase) do not correspond to those of the

transient fluctuations, which depend on the time domain values of the phase noise. It is rather based on the predicted average value of the phase noise. Meanwhile, the phase error produced by the modulator is equivalent to the phase jitter of the vector generator. This is equivalent to the phase ambiguity in real time. Predictably, the presence of a jitter in the I and Q signals leads to the creation of a jitter at the modulator output. For instance, if the phase noise of the signal generator is -80 dBc/Hz @ 10 kHz and -110 dBc/Hz @ 1 MHz, the corresponding theoretical phase jitter of the generator and modulator is about 1˚. Expressions (3-39) and (3-40) assume that the phase noise of the I/Q generator does not change significantly with the net branch gains. In the Leeson phase noise model, the signal power of an oscillator is inversely proportional to its phase noise [136]. It is worth noting that the I- and Q-generated signals share the same input signal. In addition, since they share the same bias current, they are correlated and thus the phase noise of the output signal does not deviate from that of the vector generator as demonstrated in (3-40). While the presence of phase noise in the vector modulator may cause potential phase ambiguity, it does not practically induce any substantial phase and gain errors at the output of the modulator. Conversely, a phase noise created by the phase shifter leads to a phenomenon called "spectral regrowth" in a phased array receiver, which leads to power leakage to adjacent frequency channels, similar to a local oscillator with phase noise [135]. A severe spectral regrowth may cause the corruption of adjacent frequency bands. Lastly, the thermal noise is caused by the random motion of electrons due to temperature. The thermal noise is mainly a characteristic of resistors and transistors. Since it is white, it is present at low frequencies as well as at high frequencies [124]. In this regard, a thermal noise present in the I/Q generator may be translated into phase noise that subsequently modulates both the amplitude and the phase of the vector modulator output, similar to the 1/f noise. Nevertheless, as stated before, the 1/f noise predominates at a lower frequency and therefore contributes the most to the phase noise of the vector generator. Moreover, the presence of high-frequency noise in blocks such as VGAs and the vector combiner may also lead to an instantaneous amplitude and phase modulation of the modulator's output signal since it will contain a noise signal.

To analyze the effect of high-frequency noise on the amplitude and phase of the modulator, let us assume the RMS noise amplitude of the I and Q signal branches are A_{nI} and A_{nQ}, respectively. The worst-case scenario occurs when the branch noise signals are in phase with their respective vector branches. In this case, the magnitude and phase of a vector modulator with noisy vector signals are respectively expressed as:

$$A_{out,noisy} = \sqrt{(A_I + A_{nI})^2 + \left(A_Q + A_{nQ}\right)^2} \tag{3-41}$$

and

$$\varphi_{out,noisy} = \tan^{-1}\left(\frac{A_Q + A_{nQ}}{A_I + A_{nI}}\right) \tag{3-42}$$

Where A_I and A_Q are the amplitudes of the I and Q desired signals, respectively. Both the noise and desired signals in (3-41) and (3-42) account for the VGA amplifications and branch losses and the branch noises are uncorrelated. Let $\frac{{A_I}^2}{{A_{nI}}^2} = SNR_I$ and $\frac{{A_Q}^2}{{A_{nQ}}^2} = SNR_Q$. The SNR varies with the gain, which is mostly dictated by the VGAs. Since the noise factor of an amplifier is inversely correlated with its gain [124], the worst branch SNRs occur when both VGAs hold their minimum gain states. If the vector branches have a matched loss, their SNRs are also matched, and thus, the worst-case amplitude and phase errors of the modulator can be estimated as:

$$\varepsilon_A = 10\log\left[\frac{(A_I + A_{nI})^2 + (A_Q + A_{nQ})^2}{(A_I)^2 + (A_Q)^2}\right] = 20\log\left(1 + 1/\sqrt{SNR_{b,min}}\right) \tag{3-43}$$

$$\varepsilon_\varphi = \tan^{-1}\left[\frac{A_Q + A_{nQ}}{A_I + A_{nI}}\right] - \tan^{-1}\left[\frac{A_Q}{A_I}\right] = 0 \tag{3-44}$$

where $SNR_{b,min}$ is the minimum SNR of the I and Q branches. It can be implied from (3-44) that the phase error is negligible even at the worst branch noise case. Moreover, the magnitude error of the modulator decreases with increasing branch SNR as demonstrated in (3-43). For a minimum branch SNR of 10 dB (10), an average magnitude error of only 2.4 dB is produced. Consequently, the high-frequency thermal noise does not induce significant gain and phase modulations of the active phase shifter, as an SNR of at least 20 dB is required to demodulate constellations like the Quadrature Phase Shift Keying (QPSK) and the 64-symbols Quadrature Amplitude Modulation (64-QAM) [137]. Besides, phased array receivers can easily attain SNRs in the order of 30 dB [138]. Nevertheless, the presence of thermal noise in the modulator leverages its noise factor, which in turn affects the overall sensitivity of the phased array system. The different thermal noise sources are independent of each other and the input signal. As a result, the noise at the end of each modulator branch is uncorrelated. Uncorrelated noise sources in a system are added in power to obtain the total noise power [139]. In this regard, the total output noise power of the modulator can therefore be expressed as:

$$\overline{{V_n}^2} = \overline{{V_{nI}}^2} + \overline{{V_{nQ}}^2} \tag{3-45}$$

where $\overline{V_{nI}{}^2}$ and $\overline{V_{nQ}{}^2}$ are the total squared noise voltages of the I and Q branches, respectively. Assuming the source resistance is denoted by R_S, its thermal noise is $\overline{V_{nS}{}^2} = 4KTR_S$, with K and T the Boltzmann constant and the temperature in Kelvin, respectively. Since the noise factor of a system is found by dividing its total output noise power (including the source contribution) by that of the source at the output, the noise factor of the modulator can be formulated using (3-45) as:

$$F = 1 + \frac{\overline{V_n{}^2}}{G_V{}^2 \overline{V_{nS}{}^2}} = \frac{G_{VI}{}^2}{G_V{}^2} F_I + \frac{G_{VQ}{}^2}{G_V{}^2} F_Q \tag{3-46}$$

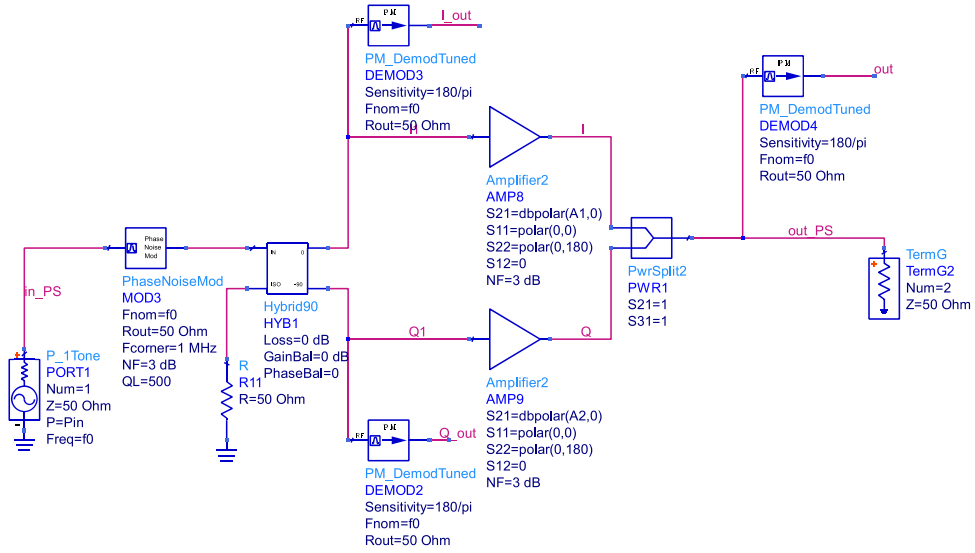
where G_{VI}, G_{VQ} are the respective net gains of the I and Q branches, including the VGAs' gains and the branch losses, and G_V the gain of the modulator system. F_I and F_Q represent the noise factors of the I and Q branches, respectively. We can observe from (3-46) that the total noise factor of a vector modulator corresponds to the sum of the products of individual branch noise factors and their respective power ratios. As noted before, the noise factor of a VGA is maximized when its gain is minimal. Nevertheless, the noise figure disparity of a VGA is relatively insignificant with respect to its gain change for gain values above 0 dB [140], [141]. Accordingly, the product of the branch noise factor and power ratio tends to increase with increasing VGA gain. Consequently, the noise factor of the modulator reaches its peak when the VGA gains are maximum. Moreover, given that $G_V{}^2 = \frac{1}{2}\left(G_{VI}{}^2 + G_{VQ}{}^2\right)$, if $F_I = F_Q$, the noise factor of the modulator equals twice that of the individual branch ($F = 2F_I = 2F_Q = 2F_b$). Therefore, the noise figure of the system becomes:

$$NF = NF_b + 3dB \tag{3-47}$$

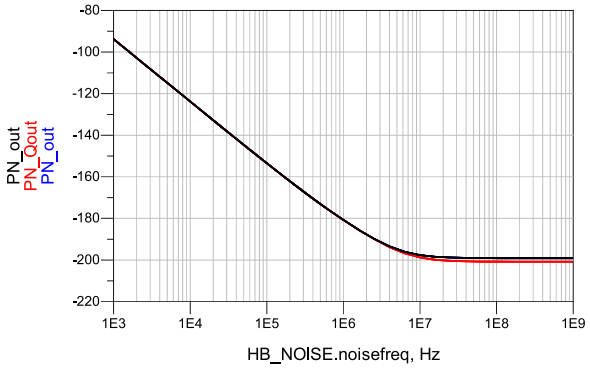
where $NF_b = NF_I = NF_Q$ is the noise figure of the individual signal branch. It can be concluded from (3-47) that the minimum possible noise figure of a quadrature modulator is 3 dB. In reality, the noise figures of the I and Q branches are more than 0 dB since the branches are often lossy and contain VGAs, which typically have noise figures above 1 dB. Besides, the vector adders are sometimes built with active elements, further exacerbating the overall noise figures of vector modulators [15]. Furthermore, it is known that the noise figure of a passive block is equal to its loss (in dB) [142]. This can be proven by modelling the passive block as a resistor connected in series with the source port. According to Friis' equation, the total noise factor of a cascaded element is divided by the gains of its preceding elements at the output within the same bandwidth [124], [143]. From that theory, losses present before the VGAs contribute more to the overall noise factor than their post-VGA counterparts. Hence, there is a trade-off between noise and linearity if the tuning element is composed of a variable attenuator and a fixed-gain

amplifier. For instance, if the attenuator is placed before the amplifier on the branch, the system linearity performance improves, whereas its noise performance degrades. In case the tuning block is built with attenuators only, the noise figures of individual branches correspond to their respective total losses. As a result, the modulator acts as a passive component with a noise figure approximately equal to its total attenuation in dB. In consequence, it is recommended to keep the modulator system gain above 0 dB to avoid noise performance deterioration.

Two simple simulations were performed to support the above theory on the modulator phase shifter noise behaviour. The first one concerns the phase noise induction in the vector generator. Depicted in Figure 3.7(a), the I/Q generator is modelled using a phase noise modulator called “PhaseNoiseMod” and a quadrature coupler in the Keysight ADS schematic environment. The phase noise modulator is based on the Leeson model, and the corner frequency is set to 1 MHz. The other parameters, such as the loaded Q of the resonator (QL) and the broadband noise figure (NF), can be adjusted to obtain the desired phase



(a)

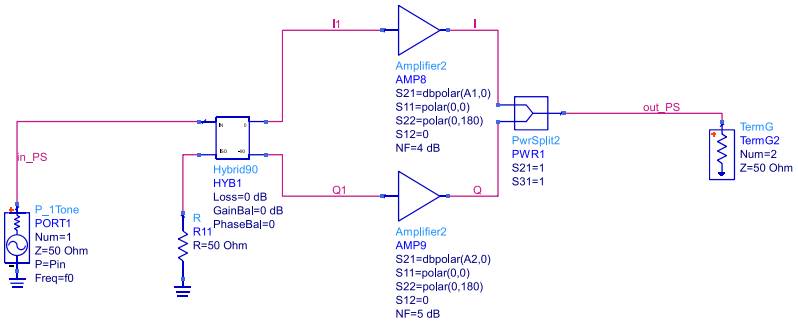


(b)

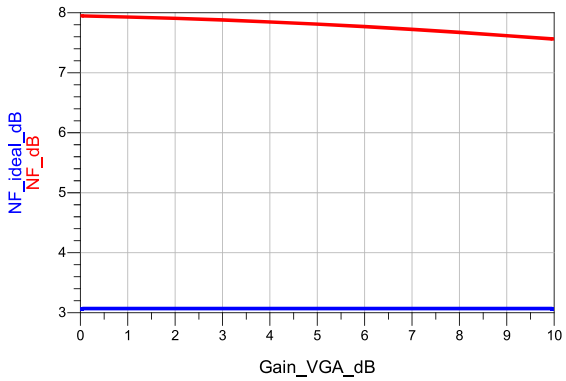
Figure 3.7: Effect of vector generator with phase noise: (a) schematic setup and (b) results displaying phase noise of the I/Q signals and the output signal.

noise at different noise frequencies. In this regard, by setting QL = 300 and NF = 3 dB, phase noise of -95 dBc/Hz and -180 dBc/Hz are obtained at 1 kHz and 1 MHz, respectively. The tuning gain of the VGA is swept from 0 dB to 10 dB. Figure 3.7(b) represents the phase noise simulation results. It can be observed that the output phase noise remains almost unchanged from the generated I and Q phase noises, which are identical for a 10 dB gain range, as predicted by the previously stated theory.

The second simulation setup pertains to the noise figure simulation of a modulator with unmatched branch noises. The setup is depicted in Figure 3.8(a). The tuning block is composed of two VGAs with noise figures of 4 dB and 5 dB. It is assumed that these noise figures remain constant as the gain is swept from 0 dB to 10 dB, which is a reasonable assumption as previously argued. In the ideal scenario, the NF of the VGAs is 0. Figure 3.8(b) illustrates the NF simulation results of the ideal noiseless modulator and the modulator with VGA NFs of 4 dB and 5 dB. The noiseless modulator exhibits an NF of 3 dB, whereas that of the system with noisy branches varies between 7.56 dB and 7.95 dB for a 10 dB tuning range. The minimum and maximum NFs occur at the maximum and minimum VGA gain states, respectively, and thus, verify the noise factor expression in (3-46).



(a)



(b)

Figure 3.8: Noise figure of a vector modulator: (a) Schematic setup and (b) NF plots of a noiseless system (blue) and a system with 5 dB and 4 dB branch noises (red).

3.4 Conclusion

In this chapter, the effects of nonlinear and noisy blocks on the performance of vector-sum phase shifters were discussed. The presence of nonlinear blocks such as the VGAs causes gain compression, which limits the maximum output power and creates gain and phase errors at the output of the modulator. The worst gain compression and gain error cases are observed when the VGAs are at their maximum gain states, whereas the phase error tends to be higher at lower tuning gains. To ensure reasonable phase error (e.g., lower than 2˚), the modulator must operate within input signals below $\sqrt{2}$ times the input 1-dB compression point of the VGAs. In addition, the branch losses present before the VGAs tend to exhibit better linear performance compared to their post-VGA branch losses counterparts. Moreover, the presence of one or more undesired signals at the input of a vector modulator may lead to nonlinear effects such as desensitization or partial/complete blocking of the desired signal. Similar to the gain compression, the worst intermodulation effect occurs at maximum VGAs' gain states. As for the noise, two different scenarios were investigated. First, the creation of phase noise in the vector generator due to the 1/f noise of active and passive elements leads to the presence of similar phase noise at the modulator output, which in turn may lead to phase ambiguity and spectral regrowth in a phased array receiver. Second, the presence of high-frequency noise may alter the noise figure of the modulator and, hence, reduce the overall sensitivity of the phased array system. The noise figure of a modulator lies at least 3 dB beyond that of the individual branch (e.g., VGAs). An attenuator-tuned modulator possesses a significantly higher noise figure than a VGA-tuned modulator, as the noise performance may be optimized by maintaining the system gain above 0 dB. In the next chapter, the theory and experimental validation of a novel vector modulator is studied.

Chapter 4

Proposed Non-Quadrature Vector-Sum Phase Shifter

4.1 Introduction

The high gain and compactness of VSPSs make them preferable for mm-wave applications. As illustrated by Figure 2.9(b), the production of a 360˚ phase shift by the conventional VSPS necessitates the generation of differential quadrature signals. As stated in section 2.4.4, the generation of differential quadrature signals with matched amplitude is challenging and area-consuming. In addition, most reported vector modulators are digital as each quadrant generates a phase range of less than 90˚. In this chapter, a new type of vector modulator is introduced. First, the system functional block diagram of the proposed phase shifter is described along with its working principle, with the help of simulation results. Next, a proof-of-concept PCB prototype is designed using the combination of microstrip transmission lines and discrete components. The building modules of the phase shifter are described with simulation results. Finally, the experimental results of the prototype are presented and compared with relevant state-of-the-art works.

4.2 System Level Analysis

4.2.1 General System Description

The block diagram of the proposed Non-Quadrature Vector-Sum Phase Shifter (NQVSPS) is illustrated in Figure 4.1. First, two RF signals (vectors) are generated with a phase difference of $\Delta\varphi < 90°$. Non-quadrature (NQ) vector generation can be achieved using a power splitter and a delay/phase generation of one signal path with respect to the other, which is done by Phase block 1. A path selector decides the signal direction of the two generated vectors through digital control. It may be implemented using a Double-Pole, Double-Throw (DPDT) or two Single-Pole, Double-Throw (SPDT) switches. Next, variable attenuators or VGAs are used to vary the gain of one signal path with respect to the other before the subtraction of the two vectors. The path selector, gain tuning block, and subtractor constitute the vector synthesizer. The subtractor may be realized using a passive or active balun. The use of variable

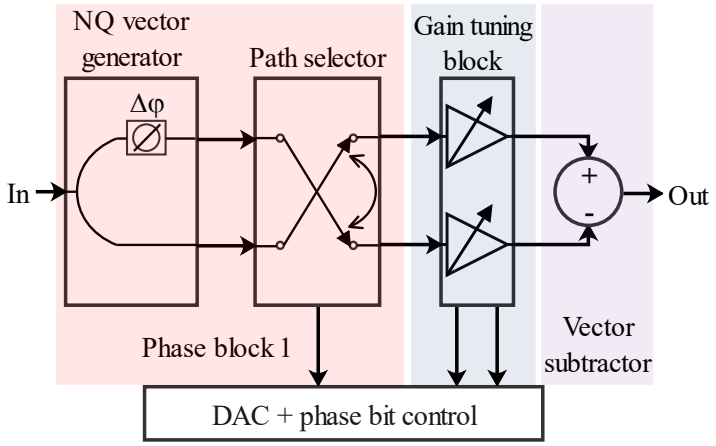


Figure 4.1: Block diagram of the proposed NQVSPS.

attenuators as analog phase tuning blocks offers the advantage of higher linearity and lower power consumption but at the cost of lower system gain.

The output voltage of the system in Figure 3.1 is expressed as:

$$V_{out} = A_0\left(A_2 e^{j(\varphi_2+\varphi_0)} - A_1 e^{j(\varphi_1+\varphi_0)}\right) V_{in} \tag{4-1}$$

with V_{in} the input RF voltage. A_1 and A_2 are the gain/attenuation of the gain tuning stage for the lower and upper paths, respectively. A_0 is the effective gain contribution from all other blocks except the gain tuning block. φ_1 and φ_2 are the phases generated by the phase block and introduced to the lower and upper paths, respectively. φ_0 is the effective phase generated by all other blocks apart from the phase block.

From (4-1), the phase and amplitude of the output signal are respectively given as:

$$\varphi_{out} = \begin{cases} \varphi_{in} + \tan^{-1}\left(\frac{Y}{X}\right), for\ X \geq 0 \\ 180 + \varphi_{in} + \tan^{-1}\left(\frac{Y}{X}\right), for\ X < 0 \end{cases} \tag{4-2}$$

$$A_{out} = |V_{in}|\sqrt{X^2 + Y^2} \tag{4-3}$$

where

$$X = A_2 \cos(\varphi_2 + \varphi_0) - A_1 \cos(\varphi_1 + \varphi_0) \tag{4-4}$$

$$Y = A_2 \sin(\varphi_2 + \varphi_0) - A_1 \sin(\varphi_1 + \varphi_0) \tag{4-5}$$

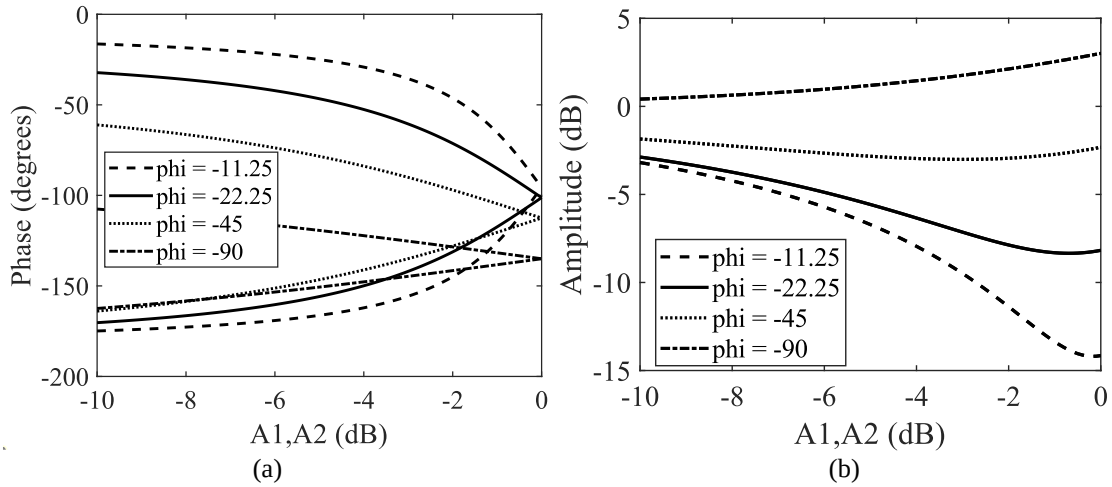


Figure 4.2: Plots of (a) φ_{out} and (b) A_{out} for different φ_1 steps.

As seen from (4-2), (4-4), and (4-5), the output phase φ_{out} is a function of the gains A_1 and A_2 of the gain tuning block. Hence, the phase tuning can be executed by tuning A_1 or A_2. Moreover, it is intended to inspect the behaviour of φ_{out} with respect to φ_1 or φ_2. For this aim, let us assume $\varphi_2 = \varphi_0 = \varphi_{in} = 0°$ and investigate the behaviour of φ_{out} with respect to the attenuations A_1 and A_2. One will be kept fixed and maximum (0 dB), and the other swept between -10 and 0 dB. By stepping the value of φ_1 between -11.25˚ and 90˚, the graph in Figure 4.2(a) is obtained. It can be observed that as the value of φ_1 decreases, wider total phase shifts are obtained. This is proven to be general for the vector phase difference $\Delta\varphi = \varphi_2 - \varphi_1$. In other words, larger phase tuning ranges are obtained for smaller $\Delta\varphi$ values. This is crucial for the proposed design as the phase difference is proportional to the size of the vector generator. In this regard, the phase range and area performance for $\Delta\varphi < 90°$ is better than that of the traditional quadrature architecture. The value of φ_0, which is common for the two signal paths, only changes the starting and the ending phases, keeping the phase range unchanged. Furthermore, by interchanging the path of φ_1 and φ_2, using the delay/phase path selector, the output signal becomes inverted. As a result, the corresponding output phase becomes that in (4-2) added to 180˚. Thus, similar phase ranges as in Figure 4.2 (a), expanding on the positive angle quadrant, are obtained. Moreover, the amplitude range increases as the value of φ_1 decreases as represented in Figure 4.2(b). Therefore, a stronger gain imbalance is created with a smaller vector differential phase $\Delta\varphi$.

4.2.2 Obtaining 360˚ Phase Range

To evaluate the phase range of the NQVSPS, one may refer to (4-2), (4-4), and (4-5). To this end, it can be assumed that $\varphi_0 = \varphi_1 = \varphi_{in} = 0°$, such that $\Delta\varphi = \varphi_2$. Assuming A_1 and A_2 are varied between

their maximum (A_{max}) and minimum (A_{min}) values, the extreme phase shifts occur when A_1 and A_2 take the values A_{max} and A_{min}, respectively and vice-versa, as given below:

$$\varphi_{out,min} = \tan^{-1}\left(\frac{\sin(\Delta\varphi)}{\cos(\Delta\varphi) - {A_{min}}/{A_{max}}}\right) \tag{4-6}$$

$$\varphi_{out,max} = 180° - \tan^{-1}\left(\frac{\sin(\Delta\varphi)}{{A_{max}}/{A_{min}} - \cos(\Delta\varphi)}\right) \tag{4-7}$$

Therefore, the phase range for the two quadrants can be expressed as:

$$\varphi_{range} = 2\left(\varphi_{out,max} - \varphi_{out,min}\right) \tag{4-8}$$

For ${A_{max}}/{A_{min}} \gg \cos(\Delta\varphi)$, $\varphi_{out,min} \approx \Delta\varphi$ and $\varphi_{out,max} \approx 180°$. The phase range becomes $\varphi_{range,max} \approx 360° - 2\Delta\varphi$, which corresponds to the maximum phase range obtainable for a vector differential phase $\Delta\varphi$. Clearly, the phase range of the phase shifter in Figure 4.1 is limited. In order to achieve a 360˚ phase range using this design, the gain tuning block must have an infinity attenuation (or gain) range (${A_{max}}/{A_{min}} \to \infty$) and $\Delta\varphi$ must approach 0˚. This is impractical as most attenuators (or VGAs) do not go beyond a 30 dB tuning range. Consequently, a phase gap is created between the two phase quadrants, limiting the phase tuning range or the phase resolution. The phase gap can be formulated as:

$$\varphi_{gap} = 360° - \varphi_{range} = 360° - 2\left(\varphi_{out,max} - \varphi_{out,min}\right) \tag{4-9}$$

For infinity gain tuning, $\varphi_{gap,min} = 2\Delta\varphi$. This is the ideal phase-step resolution of the NQVSPS. As a result, the DAC bit number $N < \log_2\left(\frac{360}{\varphi_{gap(°)}}\right)$. For instance, the required bit number for an NQVSPS with $\Delta\varphi = 22.5°$ is less than 3 to cover the 360˚ phase range.

Furthermore, one can examine the effect of the tuning range on the gain of the output signal. To do so, the previous assumptions are held: $\varphi_0 = \varphi_1 = \varphi_{in} = 0°$ and $\varphi_2 = \Delta\varphi$. Using (4-3), (4-4), and (4-5) and taking $|V_{in}| = 1$ for simplicity, the amplitude of the output signal can be written as:

$$A_{out} = \sqrt{{A_2}^2 + {A_1}^2 - 2A_2A_1\cos\Delta\varphi} \tag{4-10}$$

To obtain the minimum and maximum gains from the phase shifter, one may fix one of the attenuators' (or VGAs') gain at the maximum and sweep the gain of the other attenuator for phase tuning. In this regard, let $A_1 = A_{max}$ and A_2 be variable. The extreme values depend on both $\Delta\varphi$ and the tuning range $\frac{A_{min}}{A_{max}}$. Nevertheless, for low $\Delta\varphi$ (below 45º) and sufficiently high tuning range (e.g., 10 dB), the maximum gain can be found from (4-10) when $A_2 = A_{min}$ as:

$$A_{out,max} = A_{max}\sqrt{1 + \left(\frac{A_{min}}{A_{max}}\right)^2 - 2\frac{A_{min}}{A_{max}}\cos\Delta\varphi} \tag{4-11}$$

The other extreme gain is obtained by taking the derivative of A_{out} in (4-10) with respect to A_2 and setting it to 0. The corresponding value of A_2 is $A_{max}\cos(\Delta\varphi)$, which results in the minimum tuning gain as:

$$A_{out,min} = A_{max}\sin|\Delta\varphi| \tag{4-12}$$

It is worth noting that another critical point occurs $A_2 = A_{max}$, leading to $A_{out} = 2A_{max}\sin\left|\frac{\Delta\varphi}{2}\right|$. This is the maximum amplitude value for $|\Delta\varphi| \geq 60°$ or $\cos\Delta\varphi \leq 0.5$, whereas the minimum amplitude value corresponds to $A_{out,max}$ in (4-11). For $|\Delta\varphi| < 60°$, the fractional gain range is found from (4-11) and (4-12), as:

$$A_{out,range} = \frac{A_{out,max}}{A_{out,min}} = \frac{\sqrt{1+\left(\frac{A_{min}}{A_{max}}\right)^2 - 2\frac{A_{min}}{A_{max}}\cos\Delta\varphi}}{\sin|\Delta\varphi|} \tag{4-13}$$

From (4-13), for an attenuator tuning range of $A_{range} = \frac{A_{max}}{A_{min}} = 10 \equiv 20dB$ and $\Delta\varphi = 22.5°$, the tuning gain imbalance is about 7.5 dB. The gain imbalance does not change significantly with the attenuator tuning range for the chosen tuning method, as its maximum value is $1/\sin|\Delta\varphi|$. Nevertheless, this value is significant for real-world applications in phased array systems. Moreover, the gain imbalance worsens as the vector differential phase $\Delta\varphi$ reduces, creating a tradeoff with the phase range. Thus, a gain control mechanism must be incorporated into the system to reduce the imbalance. This adds more complexity to the design and potentially increases the overall DC power consumption.

For the aforementioned phase range and gain imbalance tradeoff challenges, a different approach must be adopted to cover a continuous 360˚ phase shift with low gain imbalance. Figure 4.3 shows the proposed 360˚ non-quadrature VSPS. A second phase block switched by two SPDT switches is added at

the input of the structure in Figure 4.2. The required vector differential phase produced by the second phase block is a function of the phase gap produced by the general structure in Figure 4.1. Consequently, the second phase gap must generate a differential phase only slightly above $2\Delta\varphi$ to ensure a continuous 360˚ phase tuning. The introduction of a second delay block alleviates the phase and gain ranges

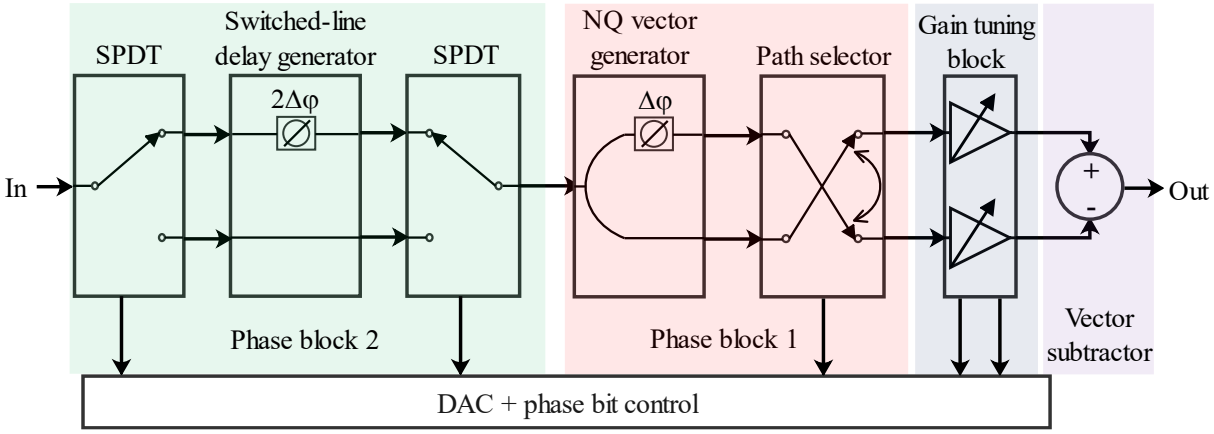


Figure 4.3: Block diagram of the proposed 360˚ continuous NQVSPS.

requirement on the non-quadrature phase shifter. For instance, by selecting a phase difference of 90˚ for the second phase block, each quadrant is required to produce only 90˚ maximum phase shift. As a result, the attenuation (or gain) range of the gain tuning block is reduced. Similarly, the output gain imbalance is improved. For $\Delta\varphi = 22.5°$, the required attenuator gain range is less than 5 dB, implying a maximum output gain imbalance of no more than 2 dB. Hence, the power consumption of the gain tuning block is reduced as well as the design complexity. The resulting phase shifter is, therefore, able to accomplish a 360˚ phase shift based on a coarse-fine tuning mechanism. The coarse tuning is effected by the two one-bit phase blocks, whereas the fine-tuning is fulfilled by the gain tuning block, which can be controlled by a DAC, which determines the resolution of the phase shifter. By using a 6-bit DAC, a phase resolution of $90°/(2^6) \approx 1.4°$ is feasible.

4.2.3 Linearity and Noise Analysis of Non-Quadrature Vector Modulators

If the tuning block of an NQVSPS is nonlinear (e.g., VGAs), high input power signals result in gain compression and phase error of the system. Assume $x(t) = A\cos(\omega_0 t)$ is the input signal of a non-quadrature vector modulator. The lossless-generated vectors $x_1(t) = \frac{1}{\sqrt{2}}A\cos(\omega_0 t)$ and $x_2(t) = \frac{1}{\sqrt{2}}A\cos(\omega_0 t + \Delta\varphi)$ are subjected to gain tuning by VGA1 and VGA2, respectively. If the VGAs are approximated by third-order nonlinear models, the amplitude of the fundamental output signal can be

expressed as:

$$A_O = \sqrt{{A_{11}}^2 + {A_{12}}^2 - 2A_{11}A_{12}\cos\Delta\varphi} \tag{4-14}$$

And its phase is given as:

$$\varphi_O = \tan^{-1}\left(\frac{-A_{12}\sin\Delta\varphi}{A_{11}-A_{12}\cos\Delta\varphi}\right) \tag{4-15}$$

where $A_{11} = \frac{A}{\sqrt{2}}\left(\alpha_{11} + \frac{1}{8}\alpha_{31}A^2\right)$ and $A_{12} = \frac{A}{\sqrt{2}}\left(\alpha_{12} + \frac{1}{8}\alpha_{32}A^2\right)$. α_{11} and α_{12} are the first nonlinear coefficients, whereas α_{31} and α_{32} are the third nonlinear coefficients of VGA1 and VGA2, respectively. Similar to the quadrature modulator, the worst nonlinearity case occurs when the VGAs hold their maximum gain state, leading to the minimum input 1-dB compression point and the maximum gain error.

Using the method described in Chapter 3, the minimum 1-dB compression point and the maximum nonlinear gain error can be computed and found to be equal to those of the quadrature modulator in (3-9) and (3-16), respectively. Nevertheless, the general expression of the phase error contains the vector differential phase, as formulated below:

$$\varepsilon_\varphi = \tan^{-1}\left(\frac{-\left(\alpha_{12}+\frac{1}{8}\alpha_{32}A^2\right)\sin\Delta\varphi}{\alpha_{11}+\frac{1}{8}\alpha_{31}A^2-\left(\alpha_{12}+\frac{1}{8}\alpha_{32}A^2\right)\cos\Delta\varphi}\right) - \tan^{-1}\left(\frac{-\alpha_{12}\sin\Delta\varphi}{\alpha_{11}-\alpha_{12}\cos\Delta\varphi}\right) \tag{4-16}$$

It can be observed from (4-16) that the error decreases as $\Delta\varphi$ approaches 0. Consequently, an NQVSPS exhibits better phase errors due to nonlinearity effects than its quadrature counterpart.

Moreover, the presence of one or more interferer signals may cause partial or complete desensitization of the non-quadrature modulator. The minimum IP3 of the NQVSPS can be calculated using the same method in Chapter 3, leading to:

$$A_{IIP3}^{min} = \sqrt{\frac{8}{3}\left|\frac{\alpha_{1,max}}{\alpha_{3,max}}\right|\left|\frac{\sin(\Delta\varphi/2)}{\sin(3\Delta\varphi/2)}\right|} \tag{4-17}$$

From (4-17), the minimum input IP3 of the non-quadrature modulator decreases with decreasing $\Delta\varphi$. In this regard, the quadrature modulator is more performant in terms of interferer-related nonlinearity.

On the other hand, the NQVSPSs present analogous internal noise characteristics as the quadrature

VSPSs. The presence of phase noise in the vector generator leads to the creation of amplitude and phase jitter at the output of the modulator. It is worth noting, however, that the generation of oblique vectors is more practically done through passive means and thus does not exhibit significant phase noise levels. Moreover, the high-frequency noises of individual blocks, such as the VGAs, cause degradation of the system noise factor, which is identical to (3-46) since the noise powers of the vectors are added at the output, regardless of their phases.

4.3 Implementation of the NQVSPS

A Printed Circuit Board (PCB) prototype based on the structure in Figure 4.3 is described in this section. The general design target parameters are provided in Table 4.1.

Table 4.1: Target design parameters of the proof-of-concept proposed vector modulator.

Parameter	**Center frequency (GHz)**	**FBW (%)**	**$\Delta\varphi$ (˚)**	**Gain (dB)**	**Phase range/resolution (˚/bit)**	**Gain imbalance (dB)**
Value	5	>25	45	>0	360/continuous	<4

The substrate used is the RT/Duroid 5880 with thickness h = 0.252 mm, dielectric constant $\epsilon_r = 2.2$, and loss tangent $\tan\delta = 0.0019$.

4.3.1 Phase Block 1 and Path Selector 1

The structure of Phase Block 1 is illustrated in Figure 4.4 along with its path selector. It is essentially a microstrip Wilkinson power divider with phase bandwidth improvement. A phase difference of $\Delta\varphi = 45°$ is created between the outputs by elongating one output line with respect to the other. From (2-2), the phase difference between 2 transmission lines can be expressed as a function of the frequency, the line dimensions and the substrate parameters. Given that the phase velocity of the chosen substrate is $v_p = \frac{c}{\sqrt{\varepsilon_{eff}}} = 0.22$ Gm/s, the phase shift in degrees is represented as:

$$\Delta\varphi = 1636.36 \times \Delta l \times f \tag{4-18}$$

where $\Delta l = l_2 - l_1$ is the physical length difference between the two lines and f the frequency in GHz. To obtain a phase difference of 45˚ at 5 GHz, the length difference of the lines must be maintained at $\Delta l = 5.5$ mm. With Δl fixed at 5.5 mm, the phase slope is 9˚/GHz, implying a rapid phase change with respect to frequency, reducing the frequency range over which a 360˚ continuous tuning is obtained. To improve the

phase bandwidth, i.e. the frequency range over which the phase is equal (or close) to a constant desired value, a $\lambda/2$ open stub may be used in the shorter line to provide a slow-wave effect at frequencies adjacent to the center frequency. As demonstrated in [144], the insertion loss of an open-stub T-resonator can be expressed as a function of the characteristic impedances and electrical lengths of the resonator. The

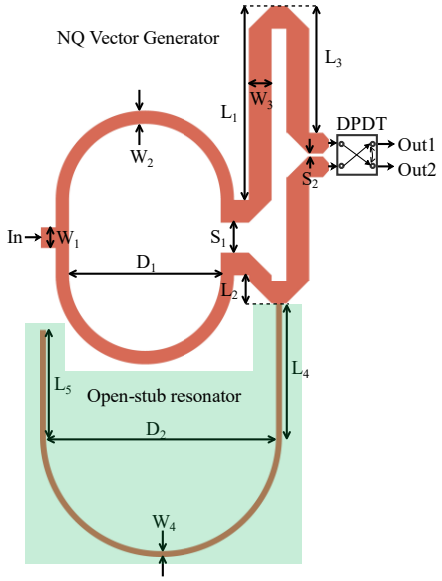


Figure 4.4: Description of the NQ vector generator and Path Selector 2.

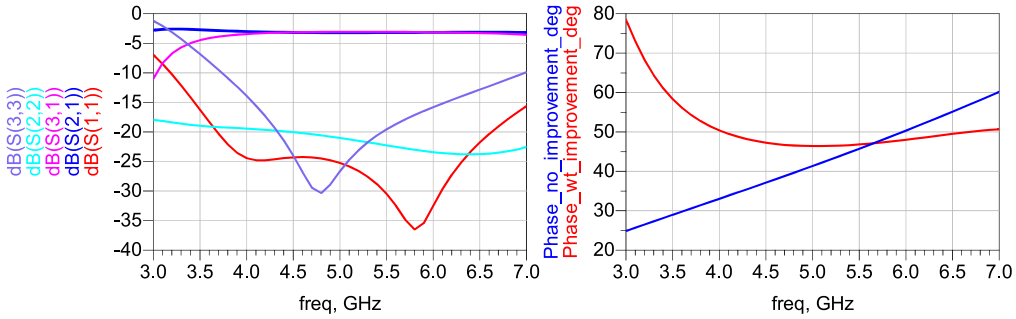
length of the stub is fixed at $\lambda_0/2$, such that the impedance through the tail of the resonator is infinity (or very high) at the center frequency f_0. In consequence, all the signal flows from the input to the output at f_0.

As we move from the center frequency towards lower or higher frequencies, the input impedance of the open stub gradually decreases, allowing one part of the input signal to flow through the tail, get reflected, and partially flow back to the input and the output, whereas the other part flows directly to the output. The partial round-trip of the signal through the tail of the resonator creates an effective resonator insertion phase close to 180° for frequencies near the center frequency. By incorporating an open-stub T resonator into the shorter line, the phase slope of $\Delta\varphi$ is decreased as we move away from f_0. Nevertheless, for frequencies far from f_0, the return loss becomes more significant, thus limiting the frequency bandwidth of the structure. The characteristic impedance of the open stub line controls the frequency and phase bandwidth in opposite directions. Smaller line impedances result in a narrower frequency bandwidth and wider phase bandwidth. Nevertheless, an optimum impedance value may be obtained by tuning the width of the resonator tail. In this regard, the proposed vector generator uses the open stub resonator for phase bandwidth improvement.

The dimensions of the proposed non-quadrature (NQ) vector generator described in Figure 4.4 are summarized in Table 4.2. The green shaded section of the structure indicates the open-end T-resonator. Since f_0 = 5 GHz and using the RT/Duroid 5880, with the aforementioned parameters, the line widths for $Z_0 = 50\ \Omega$ and $\sqrt{2}Z_0 = 70.7\ \Omega$ constituting the Wilkinson splitter are optimized along with the $\lambda_0/4$ and $\lambda_0/2$ lengths of the splitter branches and the tail of the T-resonators, respectively, in the ADS Momentum electromagnetic simulation environment. The proposed vector generator achieved insertion and return losses below 3.43 and 13 dB between 4 GHz and 6.5 GHz, respectively as illustrated in Figure 4.5(a). This corresponds to a total loss of about 0.42 dB. Moreover, the output phase difference of the proposed wide

Table 4.2: Dimensions of the microstrip line-based NQ vector generator.

Parameter	**W_1**	**W_2**	**W_3**	**W_4**	**L_1**	**L_2**	**L_3**
Value (mm)	0.70	0.45	0.77	0.20	6.57	0.97	4.30
Parameter	**L_4**	**L_5**	**D_1**	**D_2**	**S_1**	**S_2**	
Value (mm)	4.5	3.6	5.15	7.80	1.02	0.10	



(a) (b)

Figure 4.5: (a) Plots of the insertion and return losses of the NQ generator, (b) plots of generated phases for the vector generator with (red) and without (blue) the open stub.

phase bandwidth NQ generator is plotted in Figure 4.5(b) along with the generator without any phase improvement. Total phase variations of 4˚ and 22˚ between 4 GHz and 6.5 GHz for the generators with and without the open-stub T-resonator are found, respectively. Thus, a phase variation reduction of 81.8% is achieved.

To implement the isolation of the vector generator for proper input and output matching, a 100 Ω commercial RF resistor is selected [145]. Moreover, Path Selector 1 is implemented using a commercial

DPDT (BGSX22G6U10 from Infineon), with a maximum insertion loss of 0.95 dB, a minimum isolation of 19 dB, and a minimum return loss of 12 dB from 4 GHz to 6 GHz [146].

4.3.2 Phase Block 2 and Path Selector 2

Phase Block 2 is essentially a single-stage SLPS made of microstrip lines with phase bandwidth improvement, as seen in Figure 4.6. The targeted output phase difference is $2\Delta\varphi = 90°$. This leads to a reduced gain imbalance and an identical phase tuning range in each quadrant. From (4-17), the resulting length difference between the two lines is $\Delta l = 11$ mm and a phase slope of 18˚/GHz. With this rapid phase variation, a phase bandwidth amelioration technique is required to widen the overall bandwidth of the modulator. Two shorted-stub T-resonators separated by a quarter-wavelength line are added at the ends of the shorter line to provide a slow-wave effect, similar to the open stub resonator previously discussed.

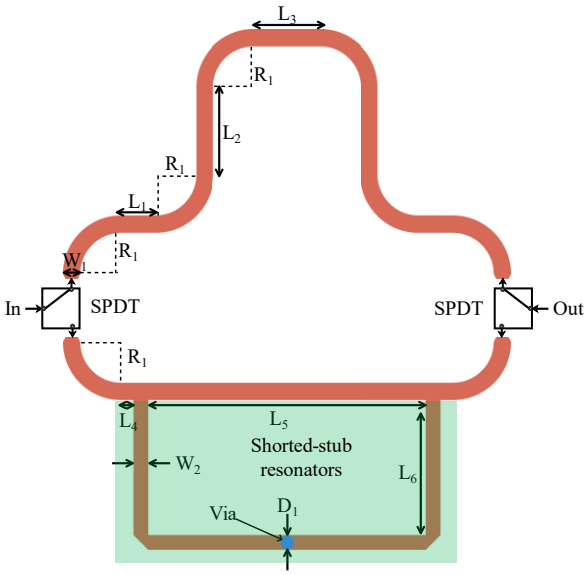


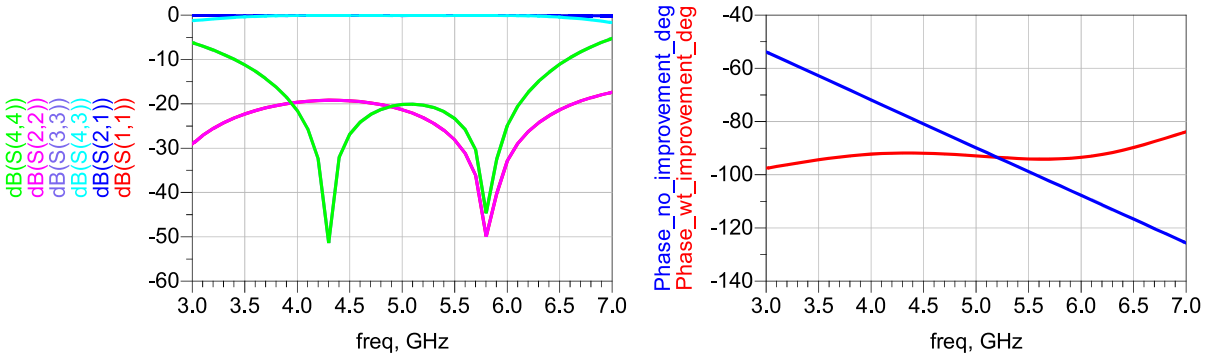
Figure 4.6: Structure of the proposed wideband switched-line delay block.

Each stub has a length of $\lambda_0/4$, generating a total delay of approximately 180˚ at frequencies adjacent to the center frequency, f_0. Like their half-wavelength open-stub counterpart, the quarter-wavelength shorted stub resonators act as bandpass filter delay generators [144]. The optimum line dimensions of the proposed wideband switched lines phase block are provided in Table 4.3. The shorted stub T-resonators' section is shaded in green. The ADS Momentum simulation results are represented in Figures 4.7(a) and 4.7(b). A maximum insertion loss and minimum return loss of 0.43 dB and 11.1 dB are obtained between 3.5 GHz and 6.5 GHz, respectively, as shown in Figure 4.7(a). Furthermore, the output phase difference of the vector modulator with and without bandwidth improvement is depicted in Figure 4.7(b). A total phase variation of only 4.6˚ is obtained for the proposed wideband switched-line delay block, whereas that of the

structure with no improvement mechanism is 51.1˚ for the same bandwidth. This corresponds to a phase variation improvement of 91%.

Table 4.3: Dimensions of the microstrip switched-lined phase block.

Parameter	**W_1**	**W_2**	**L_1**	**L_2**	**L_3**	**L_4**	**L_5**
Value (mm)	0.70	0.60	1.4	3.57	2.70	0.50	11.30
Parameter	**L_6**	**R_1**	**D_1**				
Value (mm)	5.60	1.65	0.25				



(a) (b)

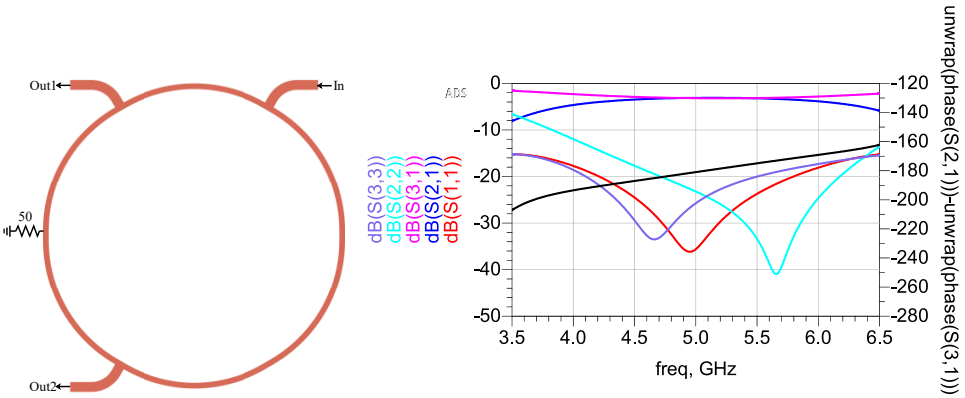
Figure 4.7: Simulation results: (a) insertion and return losses of the switched-line phase block with phase bandwidth improvement, (b) Output phase difference of the phase block with (red) and without (blue) the T-resonator improvement technique.

Meanwhile, Path selector 2 is realized using two SPDT switches. The discrete component switches are commercial (F2976NEGK8 from Renesas) and exhibit a maximum insertion loss of 0.43 dB, a minimum isolation of 40 dB, and a typical return loss below 20 dB from 4 GHz to 6 GHz [147].

4.3.3 Vector Subtractor

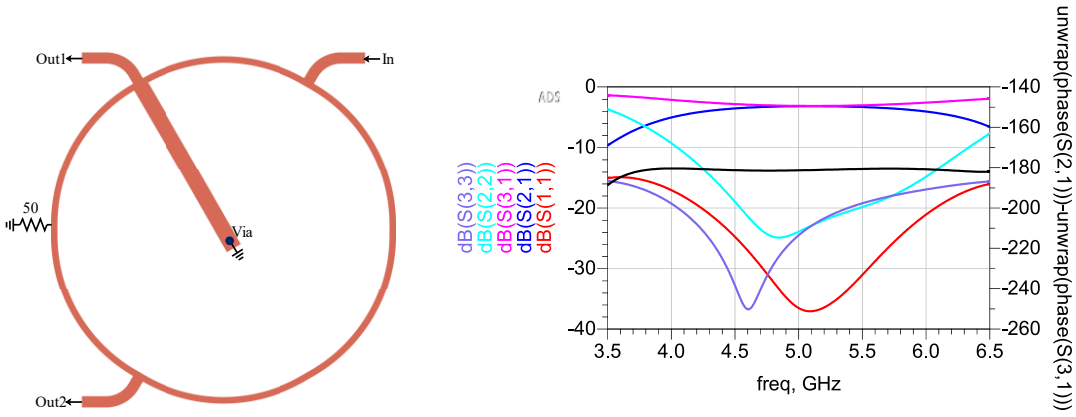
After the generation of the NQ vectors, a synthesizer is required to generate the single-ended output signal. As previously discussed, a vector subtractor is needed as an operator to obtain a wider phase tuning range. One way of subtracting analog vectors is through the 180˚ hybrid coupler, which has a coupling

factor of 3 dB. An example of such a coupler is the conventional microstrip rat-race coupler as represented in Figure 4.8(a). The simulation results of a microstrip rat-race balun designed at 5 GHz center frequency using the laminate described earlier in this section are provided in Figure 4.8(b). One may observe from the figure that the phase difference between the output ports is about 180˚ at the center frequency. This phase difference changes at a rate of 12˚/GHz as we move away from the center frequency between 4 GHz and 6GHz, reducing the phase bandwidth of the balun and, thus, the frequency bandwidth of the phase shifter. To reduce the phase slope of the balun, a shorted T-resonator may be employed at the output port closest to the input as seen in Figure 4.9 (a). This generates a slow-wave effect at frequencies adjacent to the center



(a) (b)

Figure 4.8: Conventional microstrip rat-race coupler: (a) layout, (b) Simulation results of insertion loss, return loss and output phase difference.



(a) (b)

Figure 4.9: Rat-race coupler with phase bandwidth improvement: (a) layout, (b) Simulation results of insertion loss, return loss and output phase difference.

frequency. A tail characteristic impedance of the resonator slightly below 50 Ω is sufficient to obtain a flattened phase response of the balun, as seen in Figure 4.9(b), which illustrates the simulation results of the improved balun. Although the bandwidth of the conventional rat-race balun can be improved using a T-resonator with acceptable return loss, the insertion loss mismatch between the outputs becomes more

significant as we move away from the center frequency. This mismatch results in phase and gain errors at the output if the phase shifter is digitally tuned. Furthermore, it leads to an increase in the gain imbalance of the phase shifter. For these reasons, an analog subtractor with balanced insertion loss was proposed in this work, as illustrated in Figure 4.10(a), which represents its conceptual schematic. The subtractor uses T-resonators in conjunction with a balance-to-unbalance transformation to subtract two analog input signals. With a resistive isolation midway between the differential ports, the proposed subtractor may be used as a signal subtractor, where the inputs are ports 2 and 3, and the output is port 1, as well as a single-to-differential converter, where the input is port 1, and the differential outputs are ports 2 and 3. The subtractor's even and odd mode half-circuits are represented in Figure 4.10(b) and 10(c), respectively. In the even mode operation, two signals of the same amplitude and phase are input at ports 2 and 3 of the subtractor. The input impedance $Z_{in,even}$ seen at port 2 of the half-circuit, is equal to Z_0, which corresponds

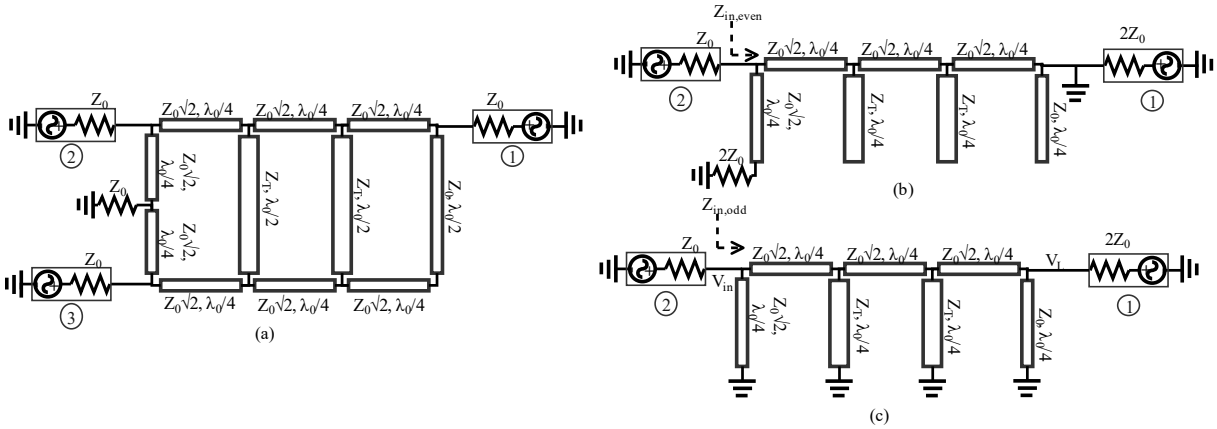


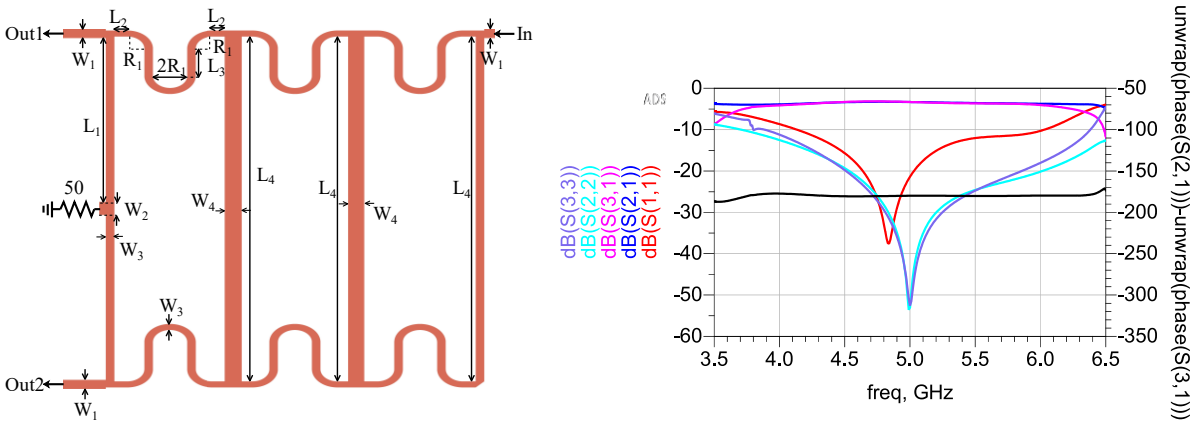
Figure 4.10: Proposed analog subtractor: (a) Conceptual schematic, (b) even-mode half-circuit and (c) odd-mode half-circuit.

to the port impedance at the center frequency f_0, whereas the signal flowing from port 2 is grounded by the quarter-wave open-stubs. This implies that no signal is transmitted to the output while the matching is maintained during the common-mode operation. Moreover, the odd or differential mode half-circuit is obtained when the signals of ports 2 and 3 are of the same amplitude with a 180˚ phase difference. In this case, the grounded quarter-wave stubs exhibit very high impedances, allowing the signal to follow the $3\lambda_0/4$-length straight path from the input to the output. As a result, the input impedance $Z_{in,odd}$ seen at port 2 is maintained at Z_0, and the insertion loss is given as $S_{21} = \frac{V_L}{V_{in}} = \frac{\sqrt{2}}{2} e^{-j3\pi/2}$ at the center frequency. As the frequency of operation moves from f_0, more signals start to flow in the two center stubs, especially following the path from port 1 to port 2, since it offers the shortest path to the stubs. Consequently, the signal delay from port 1 to port 2 and port 1 to port 3 are compensated, and the phase difference between the output ports is maintained at 180˚. Moreover, since the signal flowing in each path follows more or less

the same path, including the center stubs, the insertion losses from port 1 to port 2 and from port 1 to port 3 are matched for a relatively wider range of frequencies compared to the conventional rat-race balun. The characteristic impedance Z_T of the two middle stubs can be tuned to obtain the desired phase bandwidth or phase flatness by compromising the matching bandwidth of the input port. The proposed analog subtractor was designed and simulated using the Keysight ADS Momentum for a center frequency of 5 GHz. The substrate used is the RT/Duroid 5880 laminate previously described. Table 4.4 contains the subtractor's optimized dimensions, illustrated in Figure 4.11(a). The scattering parameters simulation results are given in Figure 4.11(b). From the results, the proposed analog subtractor generates return loss below 10 dB for ports˚ 2 and 3 between 4 and 6 GHz. Therefore, a wideband operation with low return loss is achieved in the signal subtraction mode.

Table 4.4: Dimensions of the proposed analog subtractor.

Parameter	**W_1**	**W_2**	**W_3**	**W_4**	**L_1**	**L_2**	**L_3**
Value (mm)	0.60	0.86	0.38	0.80	11.07	0.60	1.80
Parameter	**L_4**	**R_1**					
Value (mm)	23	1					



(a) (b)

Figure 4.11: Designed subtractor using microstrip lines: (a) descriptive dimensions and (b) simulation results.

Additionally, the insertion losses are matched between 4 GHz and 6 GHz and vary from 3.2 dB to 4.2 dB. Thus, a maximum loss of about 1.19 dB is obtained within the desired bandwidth. Lastly, a variation of only 2.2˚ is obtained for the differential output phase between 4 GHz and 6 GHz.

Note that a commercial high-frequency resistor (CH0603-50RJNT from Vishay) is used as the 50 Ω isolation for the subtractor/unbalance-to-balance converter [148].

4.3.4 Gain-Tuning Block and Gain-Block Amplifier

To perform fine-tuning, attenuators are used to vary the gain of one signal path with respect to the other. Attenuators offer a few advantages over VGA for gain-tuning. One of the main advantages of discrete attenuators is their broader availability in the market compared to discrete VGAs. Another advantage is their relatively simpler bias circuit; hence, they are more area-efficient. Lastly, attenuators offer lower power consumption compared to VGAs. Conversely, the use of attenuators as gain-tuning elements inevitably drops the system gain below 0 dB. Nevertheless, a gain-block amplifier may be used to boost the output signal. The employment of attenuators and an output amplifier offers lower power consumption and better linearity than that of VGAs in the vector modulator. Since the second phase block generates a 90˚ phase shift, the phase range requirement of each phase quadrant of the non-quadrature modulator is 90˚. In this regard, the gain tuning range of each quadrant can be obtained using (4-6) and (4-7) and by solving the following equation:

$$\varphi_{out,max} - \varphi_{out,min} = \pi - \tan^{-1}\left(\frac{\sin(\Delta\varphi)}{A_{range} - \cos(\Delta\varphi)}\right) - \tan^{-1}\left(\frac{\sin(\Delta\varphi)}{\cos(\Delta\varphi) - 1/A_{range}}\right) = \frac{\pi}{2} \tag{4-19}$$

The solution of (4-19) is found as:

$$\frac{A_{max}}{A_{min}} = \frac{1+\sin(\Delta\varphi)}{\cos(\Delta\varphi)} = \sec\Delta\varphi + \tan\Delta\varphi \tag{4-20}$$

Provided that $\Delta\varphi = 45°$, a gain-tuning range of only $A_{range} = \frac{A_{max}}{A_{min}} = 2.41 \equiv 7.6$ dB is required to achieve 90˚ per quadrant phase range. Using (4-13), this, in turn, leads to a system gain imbalance of 1.4 dB. The low gain-tuning range requirement allows for a wide range of low-cost discrete attenuators suitable for the design. To this end, a commercial attenuator (F2250NLGK8 from Renesas) with an insertion loss of 2.6 dB and a return loss above 11 dB between 4 GHz and 6 GHz is selected [149].

The most important parameter of the gain block amplifier is its gain, which is expected to bring the modulator gain above 0 dB. As indicated previously, the maximum losses produced by the non-quadrature generator, the DPDT, the 90˚ phase block, the SPDTs, and the analog subtractor are respectively 0.42 dB, 0.95 dB, 0.43 dB, 0.43 dB, and 1.19 dB. Assuming an 8 dB attenuator tuning, the maximum loss produced by tuning the attenuators can be found using (4-11) to be 11.2 dB. Consequently, the overall worst-case

scenario loss produced by the system before gain boosting is estimated at 14.62 dB and sets the minimum gain requirement of the output amplifier. Therefore, a commercial amplification device (TQP369184 from Qorvo) with a gain ranging from 15 dB to 19 dB between 4 GHz and 6 GHz [150] is selected. The 6-pin device's bias circuit and linear measurement results are represented in Figure 4.12. The capacitance value of C2 in the circuit may be varied to obtain an optimum return loss within the desired band. Moreover, the typical 1-dB compression point,

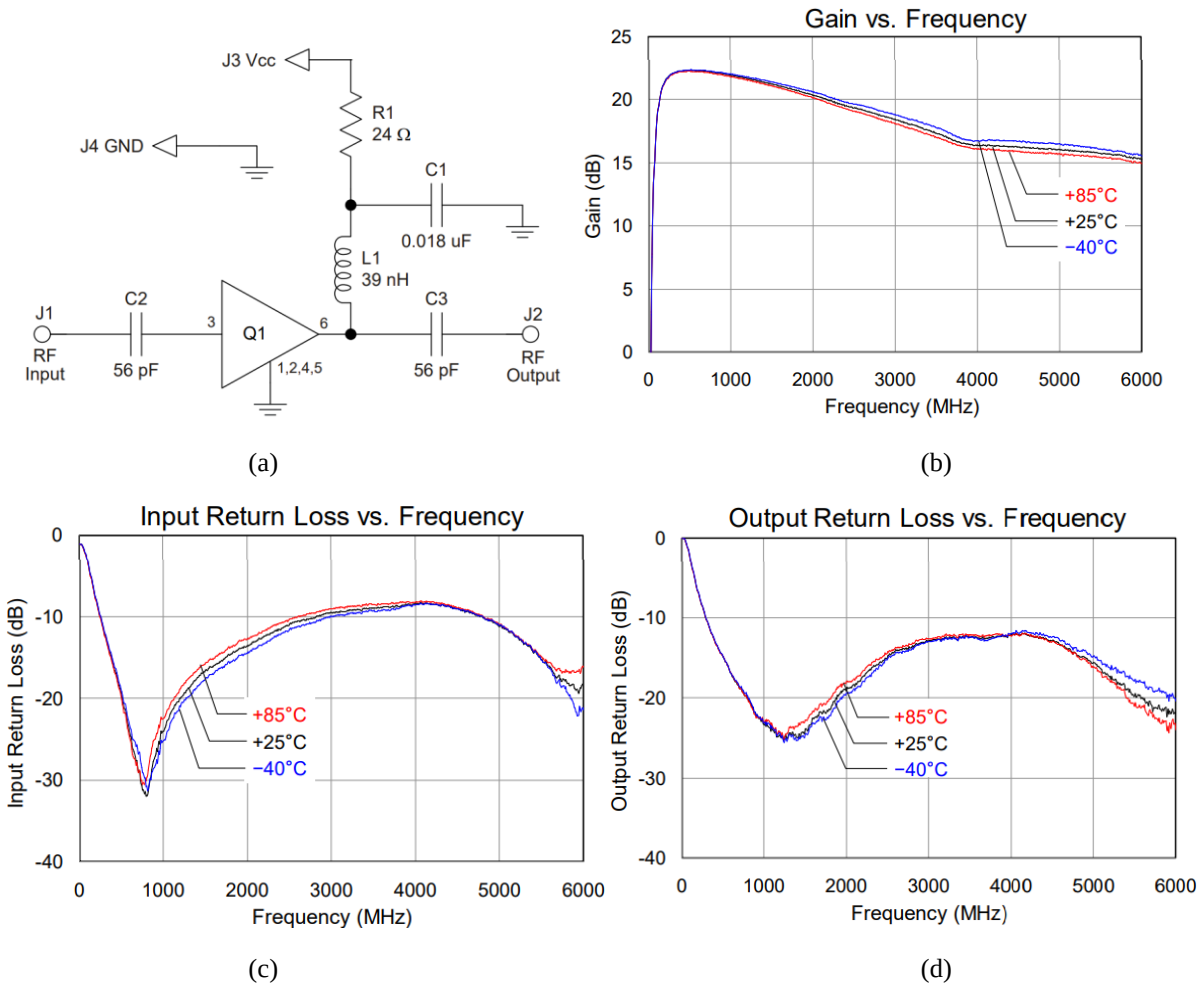


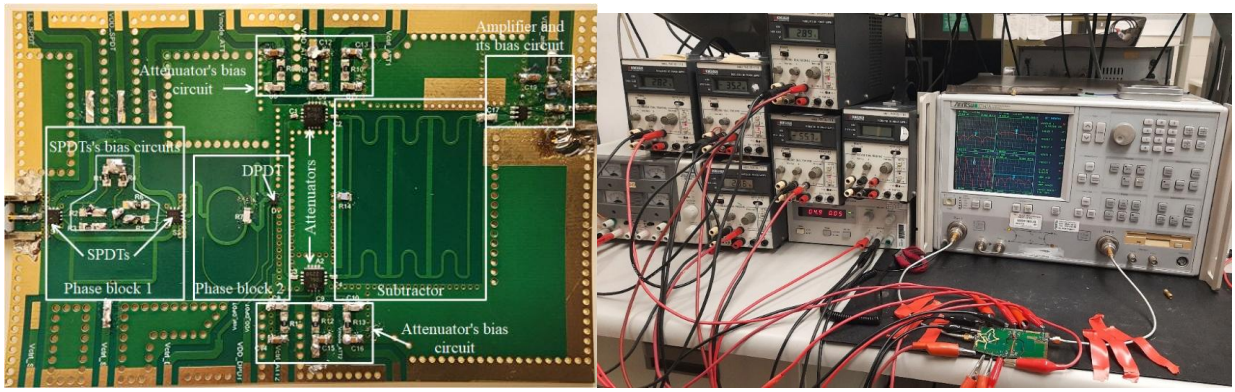
Figure 4.12: Gain-block amplifier [145]: (a) bias circuit and measurement results of (b) gain, (c) input return loss and (d) output return loss for three different temperature conditions.

output third-order intercept point and noise figure are respectively 11.4 dBm, 23.4 dBm, and 4.2 dB.

4.3.5 System Results

The constituent blocks of the proposed NQ vector modulator were combined and laid out on a PCB, with the RT/Duroid 5880 substrate described earlier. The fabricated PCB prototype without bias cables is

illustrated and labelled in Figure 4.13(a), and its S-parameter measurement setup comprising DC power supplies with bias cables and the Vector Network Analyzer (VNA) is represented in Figure 4.13(b). The fabricated prototype measures 83.1×53.5 mm^2. It is worth noting, however, that the dimension of the phase shifter without the bias circuitry extensions is around 83.1×28 mm^2. A bias variation between 0 to 1 V of the F2250NLGK8 attenuator generates a total attenuation of about 8 dB with a 4 V DC supply. In this regard, to achieve a full quadrant phase tuning with minimal insertion loss, the



(a) (b)

Figure 4.13: (a) Photograph and (b) measurement setup of the fabricated NQ phase shifter.

control voltage of one of the attenuators is set to 0 while that of the other is tuned between 0 and 1 V in a negative slope tuning process. The scattering parameters are measured with six tuning states for each quadrant, generating a total of 24 measurements. Moreover, the previously designed individual blocks are combined and simulated using the Momentum-extracted S-parameters of microstrip line blocks such as the 45º NQ generator, the 90º switched-line delay generator and the subtractor, as well as the S-parameter results of discrete components like the SPDT, DPDT, attenuator and gain-boosting amplifier provided by their respective manufacturers. It is worth noting that the S-parameter models of discrete components are only for specific bias points, which were not necessarily used, as the bias points and circuit components values were varied to obtain optimum phase shifter results during the measurement. Figures 4.14(a), (b), (c) and (d) represent the plots of the simulated (blue) and measured (red) results of the input reflection coefficient, output reflection coefficient, gain and phase of the designed vector modulator, respectively. It can be observed that the minimum input measured return loss obtained for the 4-quadrant operation is 10.6 dB, whereas the output return losses for all states lie above 7.5 dB between 2.7 GHz and 6.1 GHz. The simulated input and output reflection coefficients, on the other hand, are below -10 dB and -7.5 dB, respectively, from 3.6 GHz to 6 GHz. Moreover, the measured gain of the fabricated modulator ranges from -4.7 dB to 6.3 dB, with an average gain imbalance of less than 3 dB. In contrast, the simulated gain varies between 6.5 dB and -0.8 dB, with an imbalance of less than 4.1 dB within the same bandwidth, as shown in Figure 4.14(c). Additionally, a minimum of 372˚ analog phase range was achieved for only an 8

dB

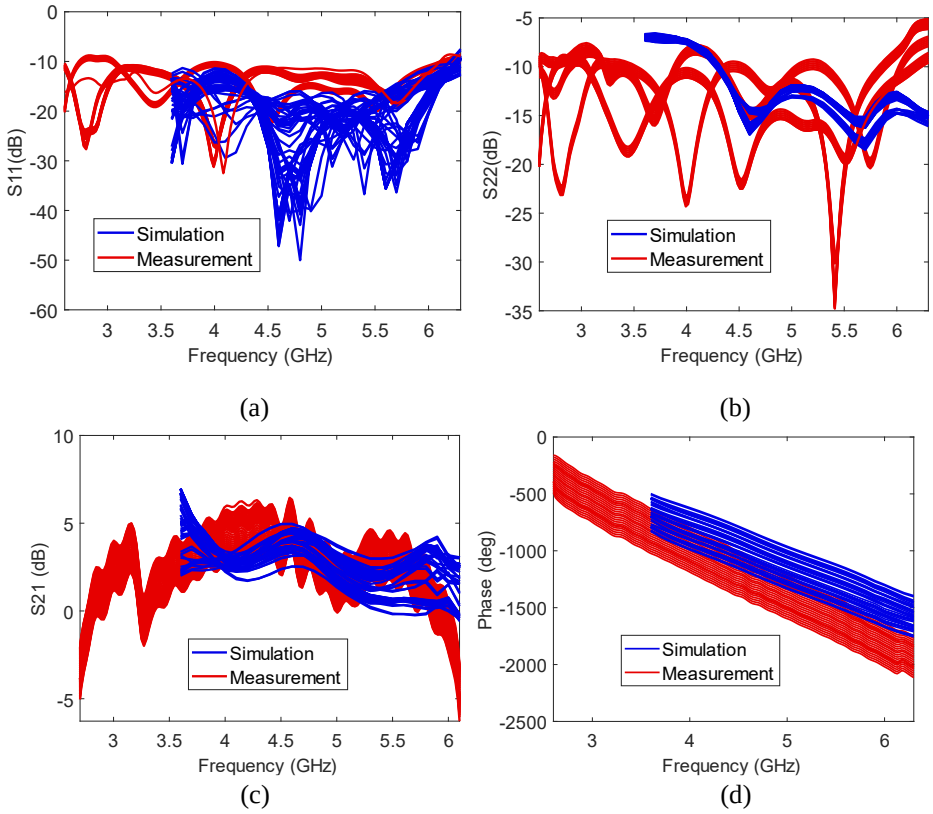
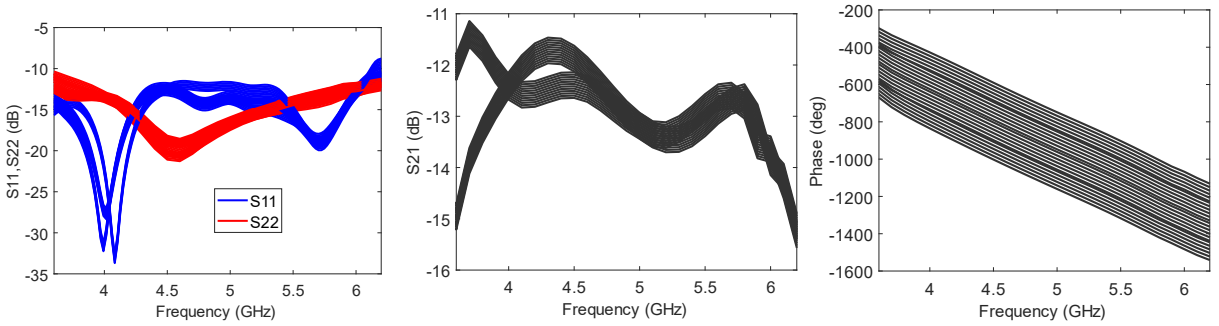


Figure 4.14: S-parameters simulation (blue) and measurement (red) results of the fabricated phase shifter with output amplification: magnitudes of (a) S11, (b) S22, (c) S21 in dB, and (d) phase of S21 for at least 24 phase states.

attenuator tuning range for both the simulation and measurement from 2.7 GHz to 6.1 GHz, as represented in Figure 4.14(d). The selected amplifier for this practice draws a DC current of about 50 mA from a 5 V supply, therefore generating a power consumption of 250 mW. It is worth noting that this power consumption may be significantly reduced by integrating the blocks in a CMOS technology such as the 130 nm BiCMOS with a 1 V supply voltage. Furthermore, it is intended to evaluate the performance of the phase shifter without the amplification block. To this end, the scattering parameters of the amplifier are de-embedded from those of the measured scattering parameters of the phase shifter with the amplifier. The results correspond to those of the phase shifter without the output amplification stage and are depicted in Figures 4.15(a), 4.15(b), and 4.15(c). Figure 4.15(a) displays the input (blue) and output (red) reflection coefficients of the phase shifter, which are below -8.9 dB and -10.5 dB, respectively between 3.6 GHz and 6.2 GHz for all tuning states. The insertion loss, on the other hand, varies from 11.3, dB to 15.6 dB, with an average gain imbalance of less than 2.5 dB, as illustrated in Figure 4.15(b). Lastly, the phase shifter without the amplification block generates a phase range of 372˚ for only an 8 dB attenuation range between 3.6 GHz and 6.2 GHz, as demonstrated in Figure 4.15(c).



(a) (b) (c)

Figure 4.15: S-parameters measurement results of the fabricated phase shifter without amplification: (a) S11 (blue) and S22 (red), (b) magnitude of S21 in dB and (c) phase of S21 for 24 phase states.

The performance of the designed NQ modulator with and without the output amplification stage is summarized and compared to relevant works in Table 4.5. One may observe that most reported electronic phase shifters are unable to provide a 360˚ continuous phase shift. In addition, the typical fractional bandwidth of passive and most active phase shifters is below 25%. Nevertheless, the proposed vector modulator provides more than 360˚ phase range with a continuous resolution for only an 8 dB gain-tuning range. Moreover, the employment of phase improvement techniques and a wideband analog subtractor led to a fractional bandwidth of more than 53%. The total power consumption of the proposed phase shifter without gain boosting emanates from the attenuators, which generate about 3 mW each and the area is estimated at $1.3\times0.6\ \lambda_g^2$ with the exclusion of the port connectors and the bias circuit extensions. As a result, the proposed analog phase shifter occupies relatively less area compared to state-of-the-art PCB-based phase shifters. Nevertheless, the insertion loss produced by the NQ modulator without amplification is above 10 dB. In this regard, the use of an output amplifier improves the system gain, which is measured at above 0 dB on average. Meanwhile, the power consumption, the 1-dB compression point, and the IP3 of the system are dictated by those of the amplifier and may be improved by integrating the design in an appropriate process technology. The amplifier consumes 250 mW, which adds to the 6 mW consumption from the attenuator, thereby generating a total of 256 mW DC power consumption. Furthermore, the 11.3 dB minimum loss of the modulator with no amplification raises the minimum 1-dB compression point of the system after amplification to 22.7 dBm.

4.4 Conclusion

In this chapter, a vector-sum phase shifter based on the generation and synthesis of two non-differential signals with a phase difference below 90º is proposed and implemented on PCB as a proof-of-concept. The phase shifter employs T-line resonators and a wideband analog subtractor with matched

Table 4.5: Performance summary of the proposed vector modulators and comparison with relevant works.

Reference	**[62]**	**[151]**	**[87]**	**[15]**	**This work 1***	**This work 2****
Technology	PCB	250nm BiCMOS	PCB	130nm CMOS	**PCB**	**PCB**
Type	RTPS	VSPS	VSPS	VSPS	**NQVSPS**	**NQVSPS**
f_0 /FBW (GHz / %)	2.5/20	10/40	1.175/21.3	5.4/18.6	**4.9/53.1**	**4.44/77.3**
Phase range/resolution (°/bits)	146.9/ continuous	360/6	320@1.16 GHz/ continuous	360/6	**360/ continuous**	**360/ continuous**
RMS phase error (°)	5.79	2-6.4	-	1.25-9.5	**-**	**-**
RMS gain error (dB)	-	1.6-2	-	0.5-0.7	**-**	**-**
Gain (dB)	-0.94±0.34	-4.5±2	-3.1±1	-0.1±1.15	**-13.45±2.15**	**0.8±5.5**
Minimum input P1dB					**-**	**22.7**
Area (λ_g^2)	-	-	0.99	-	**0.78****	**0.9****
Power consumption (mW)	**0**	**110**	**0**	**28**	**6**	**256**

* Modulator without output amplification.

** Modulator with output amplification.

*** Size without port connectors and bias extensions.

insertion loss to improve the phase bandwidth of building blocks and reduce the gain imbalance of the phase shifter. The implemented PCB prototype exhibits more than 360º analog phase shift with only 8 dB gain tuning. In addition, the phase shifter occupies $0.78\lambda_g^2$ and consumes 6 mW with an average insertion loss of -13.45 dB from 3.6 GHz to 6.2 GHz with no output amplification. With the presence of a gain-boosting amplifier, the power consumption, size and average insertion loss become 231 mW, $0.9\lambda_g^2$, and 0.8 dB, respectively, from 2.7 GHz to 6.1 GHz. Compared to most other recent designs, the proposed

phase shifter clearly performs better in terms of bandwidth, phase range per resolution and area per phase range as demonstrated by Table 4.1. The relatively high power consumption is due to the discrete single-ended output amplifier and may be reduced by integrating the blocks in a proper semiconductor process, as will be seen in the next chapter, which covers the design of an RF module containing the proposed NQ vector modulator and SPDT switches in the 130nm CMOS process.

Chapter 5

An X-Band Non-Quadrature Vector Sum Phase Shifter Module in the 130 nm BiCMOS Process

5.1 Introduction

This chapter covers a proof-of-concept design of an RF module with Tx/Rx switching in the X-band. The module is intended to be used in a phased array transceiver like the one represented in Figure 5.1. Shaded in red, the module comprises an input and output SPDT, a phase shifter unit, and a single-stage VGA. The block diagram of the vector modulator phase shifter is represented in Figure 4.3. The RF transceiver in Figure 5.1 is composed of other blocks such as a power amplifier, an LNA and an antenna and is meant for applications such as the phased array radar for weather monitoring.

The technology used is the 130nm Bipolar Complementary Metal-Oxide Semiconductor (BiCMOS) from the Taiwan Semiconductor Manufacturing Company (TSMC). The relatively cost-effective silicon design will include the following module's constituent blocks: Phase block 1, Phase block 2, the attenuator, the vector subtractor, the gain-block amplifier, and the SPDT. Table 5.1 displays the general target performance of the phase shifter module, which targets the X-band radar applications. The desired center frequency and fractional bandwidth are 10 GHz and 40%, respectively, with an insertion loss near 0 dB for all phase states. The target fractional bandwidth is better than that of most reported phase shifters. Although the measured results of the integrated circuit will not be reported, this chapter works through a complete proof-of-concept design of an RF module containing the proposed NQ modulator phase shifter with Tx/Rx switching in the X-band.

Table 5.1: Target design parameters of the X-band NQVSPS.

Parameter	**Center frequency (GHz)**	**FBW (%)**	**$\Delta\varphi$ (˚)**	**Gain (dB)**	**Phase range/resolution (˚/bit)**	**Gain imbalance (dB)**
Value	10	> 40	22.5	~ 0	360/continuous	< 4

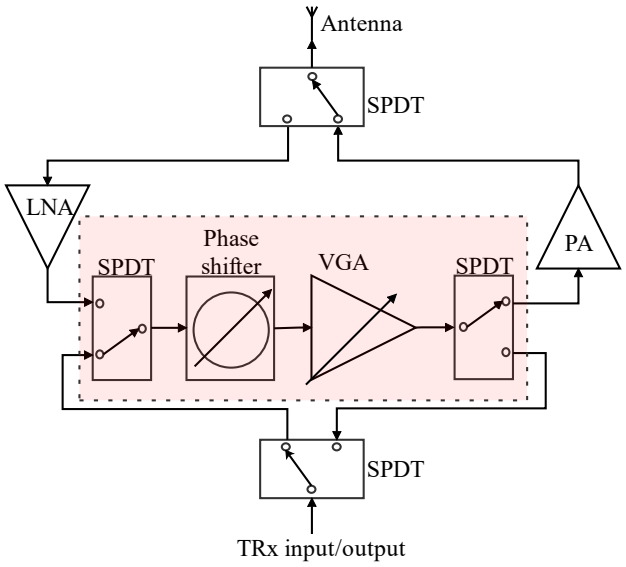


Figure 5.1: Phase array radar transceiver unit for weather monitoring.

5.2 Phase Block 1

The NQ vector generator can be designed using a power splitter and output delay generators that provide a phase difference of 22.5º. Here, it is preferable to realize the splutter using lumped elements like inductors and capacitors, as this results in a more space-efficient design than its transmission line counterpart in the X band. The structure of the vector modulator is depicted in Figure 5.2(a). It comprises a lumped-element power divider formed by the inductor L_1 and the Capacitor C_1, and a delay-generating capacitor C_2 coupled at the lower output of the structure. The lumped-element Wilkinson power splitter can be analogized to its transmission-line counterpart, which is illustrated in Figure 5.2(b). The quarter-wave transmission line in Figure 5.2(b) is equivalent to the L-C π-network formed by L_1 and C_1. In this regard, the values of L_1 and C_1 can be obtained by equating the phase φ_p and characteristic impedance Z_{0p} of the π-network in (2-9) and (2-11) to those of the transmission lines in the Wilkinson divider as follows:

$$\varphi_p = \cos^{-1}\left(1 + \frac{j\omega_0 L_1}{1/(j\omega_0 C_1)}\right) = \beta l_0 = \pi/2 \tag{5-1}$$

$$Z_{0p} = \frac{j\omega_0 L_1}{j\sin(\pi/2)} = \sqrt{2}Z_0 \tag{5-2}$$

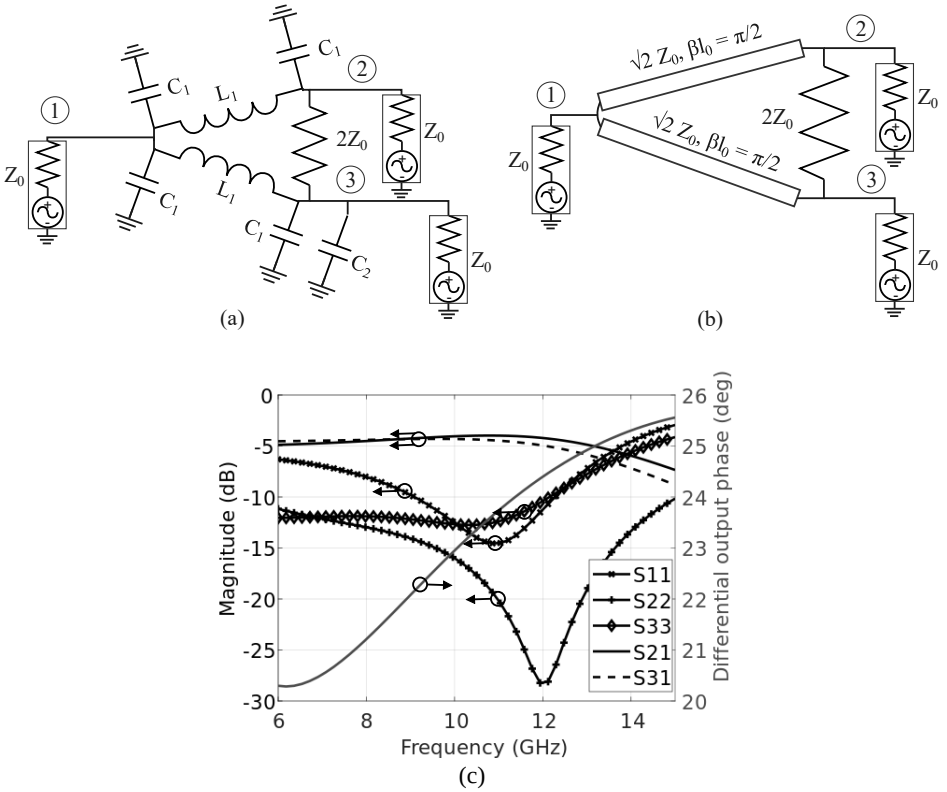


Figure 5.2: (a) Schematic of the non-quadrature vector generator, (b) Schematic of the Wilkinson power splitter. Post-layout S-parameter simulation results of the non-quadrature vector generator.

where β, Z_0 and $l_0 = \frac{\lambda_0}{4}$ are the phase constant, the input/output port impedance and the length of the line at the center frequency, respectively. The following expressions of L_1 and C_1 are obtained by solving (5-1) and (5-2):

$$L_1 = \frac{\sqrt{2}Z_0}{\omega_0} \tag{5-3}$$

$$C_1 = \frac{1}{\sqrt{2}Z_0\omega_0} \tag{5-4}$$

Given that $Z_0 = 50\ \Omega$ and $\omega_0 = 2\pi f_0 = 62.83 \times 10^9$ rad/s, the corresponding values at $f_0 = 10$ GHz are $L_1 = 1.13$ nH and $C_1 = 225$ fF. The power splitter comprising L_1 and C_1 has matched output phases. To create a phase shift between port 2 and port 3, a capacitor C_2 is added at port 3. A capacitance value of about $C_2 = 235$ fF is sufficient to create a phase shift of 22.5º at 10 GHz. These values assume the inductor and capacitors are ideal. In contrast, on-chip spiral inductors, in particular, have a limited Q-

factor and self-resonance frequency resulting from parasitic resistances and capacitors. To this end, first, the spiral inductor is designed and simulated using the Cadence EMX electromagnetic (EM) simulator to generate a 1.13 nH inductance value. Next, C_1 is tuned to resonate at $f_0 = 10$ GHz, starting with the ideal value of 225 fF. Then, the value of C_2 is optimized to generate an output differential phase of $\Delta\varphi \approx 22.5°$. To maintain the input matching at the desired center frequency, a series capacitance of about 3.4 pF is added at the input of the vector generator. The optimum values of C_1 and C_2 are approximately 643 fF and 1.35 pF, respectively. The capacitors C_1 and C_2 at port 2 form a single capacitor of 2 pF. The RF metal-oxide-metal (MOM) on-chip capacitor is used, which offers a relatively high Q-factor. Finally, the layout of the vector generator is designed with the obtained inductor and capacitors. The equivalent parasitic R-C circuit of the structure, excluding the inductors, is extracted using Siemens Calibre (Siemens) integrated in Cadence and simulated alongside the EM-extracted S-parameters of the inductors to obtain the insertion loss and phase plots of the NQ vector generator, as represented in Figure 5.2(c). The obtained insertion loss at $f_0 = 10$ GHz is about 4.2 dB, with a maximum insertion loss mismatch of 1.5 dB from 6 GHz to 15 GHz. Moreover, output return losses remain below 10 dB between 6 GHz and 12 GHz, whereas the maximum input return loss is 6.3 dB for the same frequency band, indicating a relatively narrow input matching of the lumped element power splitter. Meanwhile, the output phase difference varies between -25.6º and -20.3º from 6 GHz to 15 GHz.

The path selection of Phase block 1 is executed using a DPDT, whose schematic is illustrated in Figure 5.3 (a). The DPDT comprises two identical SPDTs with cross-coupled outputs. The SPDTs are built using synchronized switches, which are implemented using the NMOS transistors. When the control signal S is "high" (e.g. V_{DD}), and $\bar{S}$ is "low" (e.g. 0), the transistors M_1, M_2, and M6 are ON, whereas M_3, M_4, and M5 are OFF. Thus, the RF signals flow from the input port 1 to the output port 2, and from the input port 3 to the output port 4. This is called "State 1" of the DPDT. Similarly, when S is "low" and $\bar{S}$ is "high", the RF signals flow from port 1 to port 4 and from port 3 to port 2, constituting "State 2" of the DPDT. To maintain the insertion losses low, the width of the transistors M_1, M_2, M_4, and M_5 is given a high value (e.g. 60 µm) as the ON-resistance of a MOSFET is proportional to its width-to-length ratio (W/L) [135]. Additionally, the bulk floating technique is used to improve the insertion loss of the MOSFET switches [152]. To this end, the bulk of the transistors is connected to grounded resistors R_1 with high resistance values (e.g. 1.5 kΩ). M_3 and M_6 help ameliorate the isolation between port 1-port 4 and port 3-port 2, for State 1 as well as port 1-port 2 and port 3-port 4 for State 2. Their size is selected to be relatively small (e.g. 12 µm) to achieve decent isolation while maintaining the output matching at all states of the DPDT. The resistance of the gate bias resistors R_2 is also kept high (1.5 kΩ). The schematic in Figure 5.3(b) is used to generate the bypass (S) and its inverted signals ($\bar{S}$) from a single input control

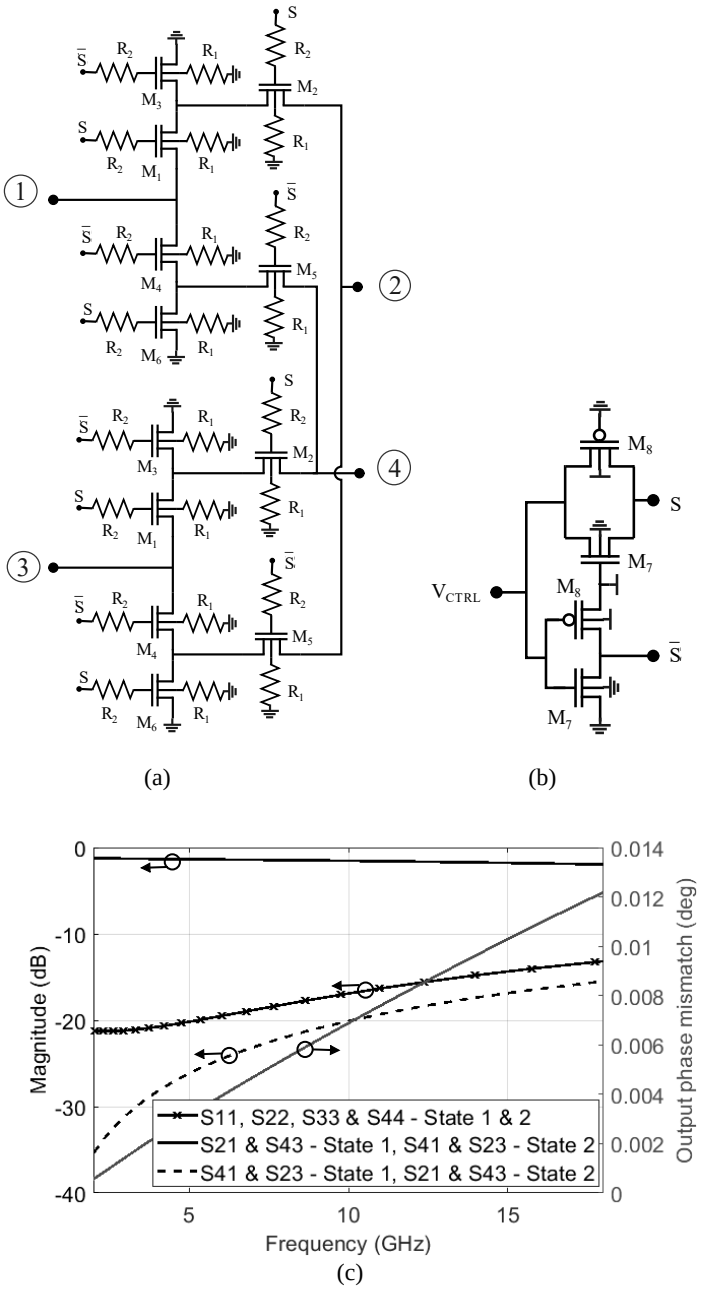


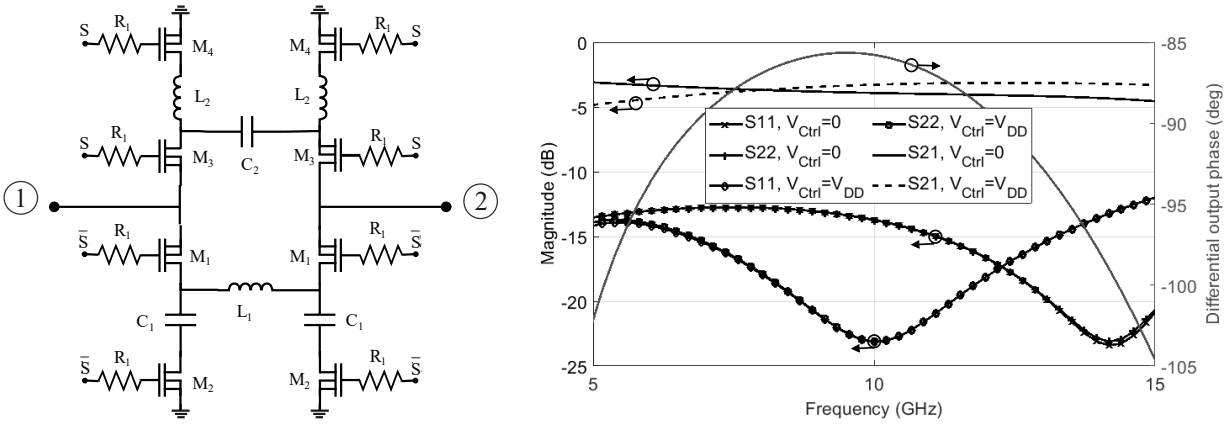
Figure 5.3: (a) Schematic of the proposed DPDT switch, (b) Schematic for generating bypass (S) and inverted ($\bar{S}$) signals from a single control voltage and (c) S-parameters simulation results the DPDT switch.

voltage (V_{CTRL}). The widths of the NMOS transistors M_7 and the PMOS transistors M_8 are 50 µm and 100 µm, respectively. The length of all transistors is kept minimal (130 nm). The supply voltage is V_{DD} = 1.2 V. The equivalent R-C circuit of the DPDT switch, including the control voltage generator, is extracted using Calibre. The S-parameters of the equivalent circuit are simulated and plotted in Figure 5.3(c). Represented in solid line, the insertion losses range from 1.4 dB to 1.8 dB between 5 GHz and 15 GHz at both states. Moreover, the return losses (solid line with x markers) and isolation (dashed line) are

below 14.3 and 16.6 dB, respectively, for the same frequency range. Lastly, the output phases appear to be matched, as their difference is approximately 0.

5.3 Phase Block 2

A theoretical phase shift of about $2\Delta\varphi \approx 45°$ for the second phase block is sufficient to obtain a 360º phase range. Nevertheless, this leads to a mismatched phase range for the four phase shifter quadrants. Moreover, the tuning range of two of the phase quadrants will be larger, increasing the demands on the attenuators (or VGAs). To balance the phase range of the quadrants, a phase shift of 90º can be created for Phase Block 2. This may be done through the high/low pass phase shifter, as represented by the block diagram in Figure 2.6(b). The schematic of the 90º delay generator, along with its switching path selector, is represented in Figure 5.4 (a). The filters are constructed using lumped elements in a π-configuration. The inductor L_1 and capacitor C_1 form the low-pass network, while L_2 and C_2 constitute the high-pass configuration. Since the low and high pass filters generate negative and positive phase shifts, respectively, the former may produce -45º, and the latter 45º to obtain a 90º total phase shift. In this regard, the corresponding ideal lumped element values may be obtained by solving (2-9) and (2-11). The values of L_1 and C_1 are obtained by setting $Z_{1p} = j\omega L_1$, $Z_{2p} = \frac{1}{j\omega C_1}$, $\varphi_p = -45°$, $Z_{0p} = 50\Omega$, and those of L_2 and C_2 are found by setting $Z_{1p} = \frac{1}{j\omega C_2}$, $Z_{2p} = j\omega L_1$, $\varphi_p = 45°$, $Z_{0p} = 50\Omega$, leading to L_1 = 560 pH, C_1 = 130 fF, L_2 = 1.9 nH, and C_2 = 450 fF. These values served as starting points for the actual ones where the lumped spiral inductors and the MOM capacitors present limited Q-factors.



(a) (b)

Figure 5.4: Low/high pass 90º delay block: (a) Schematic, and (b) S-parameters simulation results.

The path selection is done through the NMOS switches M_1, M_2, M_3, and M_4. When the control voltage S =V_{DD} = 1.2 V, and $\bar{S}$ = 0, the transistors M_1 and M_2 are ON while M_3 and M_4 are OFF. Consequently, the RF signal flows from the input port 1 to the output port 2 through the low-pass network. In contrast, the high-pass path is followed when the values of S and $\bar{S}$ are interchanged. M_1 and M_3 transistors are the primary switches with width $W_{1,3}$ = 60 µm, whereas M_2 and M_4 transistors with width $W_{2,4}$ = 100 µm are secondary and help improve the isolation between the high and low pass paths. The gates of the transistors are biased through resistors R_1 with a 1 kΩ resistance. An S and $\bar{S}$ generator identical to that of Figure 5.2(b) is used to control the delay block via a single input voltage V_{CTRL}. The 90º phase block is optimized and laid out. The optimum lumped element values after layout are L_1 = 540 pH, C_1 = 103 fF, L_2 = 1.5 nH and C_2 = 450 fF. The Calibre-extracted equivalent circuit of the structure, excluding the inductors, was simulated in conjunction with the EMX-extracted S-parameters of the inductors. The S-parameters simulation results are represented in Figure 5.4(b). The input and output reflection coefficients (the solid black lines with x, +, diamond and square markers) are all below -12 dB, and the insertion coefficients (solid and dashed black lines with no markers) range from -4.6 dB to -3 dB, with a maximum mismatch of 1.8 dB between 5 GHz and 15 GHz. In addition, the output phase difference (solid gray line) varies between -104.6º and -85.6º for the same frequency range.

5.4 Variable Attenuators

Attenuators have been selected for gain-tuning purposes as they offer simpler biasing and smaller areas. Since the phase range per quadrant is 90º, the required attenuation range is below 10 dB. The conceptual schematic of the unit attenuator is illustrated in Figure 5.5(a) and consists of a combination of the π- and T-configurations formed by the resistors with constant resistances R_1 and R_3 as well as variable resistance R_2. Figure 5.5(b) represents its practical schematic, where the variable resistors are replaced by the transistors M_1. The input resistance R_{in} and attenuation A of the structure can be written as:

$$R_{in} = [R_2//(R_1 + Z_0) + R_3]//R_2 + R_1 \tag{5-5}$$

$$A = \frac{Z_0 {R_2}^2}{R_{in}(R_1+R_2+Z_0)[R_2+R_3+R_2//(R_1+Z_0)]}(1 + \Gamma_{in}) \tag{5-6}$$

where Z_0 is the input/output port impedance and $\Gamma_{in} = \frac{R_{in}-Z_0}{R_{in}+Z_0}$, the input/output reflection coefficient. At the maximum attenuation state, $R_2 \gg R_1, R_3, Z_0$, which leads to the input impedance $R_{in}|_{A=A_{max}} \approx 2R_1 + R_3 + Z_0$ and the maximum attenuation $A_{max} \approx \left(\frac{Z_0}{2R_1+R_3+Z_0}\right)\left(\frac{4R_1+2R_3+2Z_0}{2R_1+R_3+2Z_0}\right)$. Clearly, the input

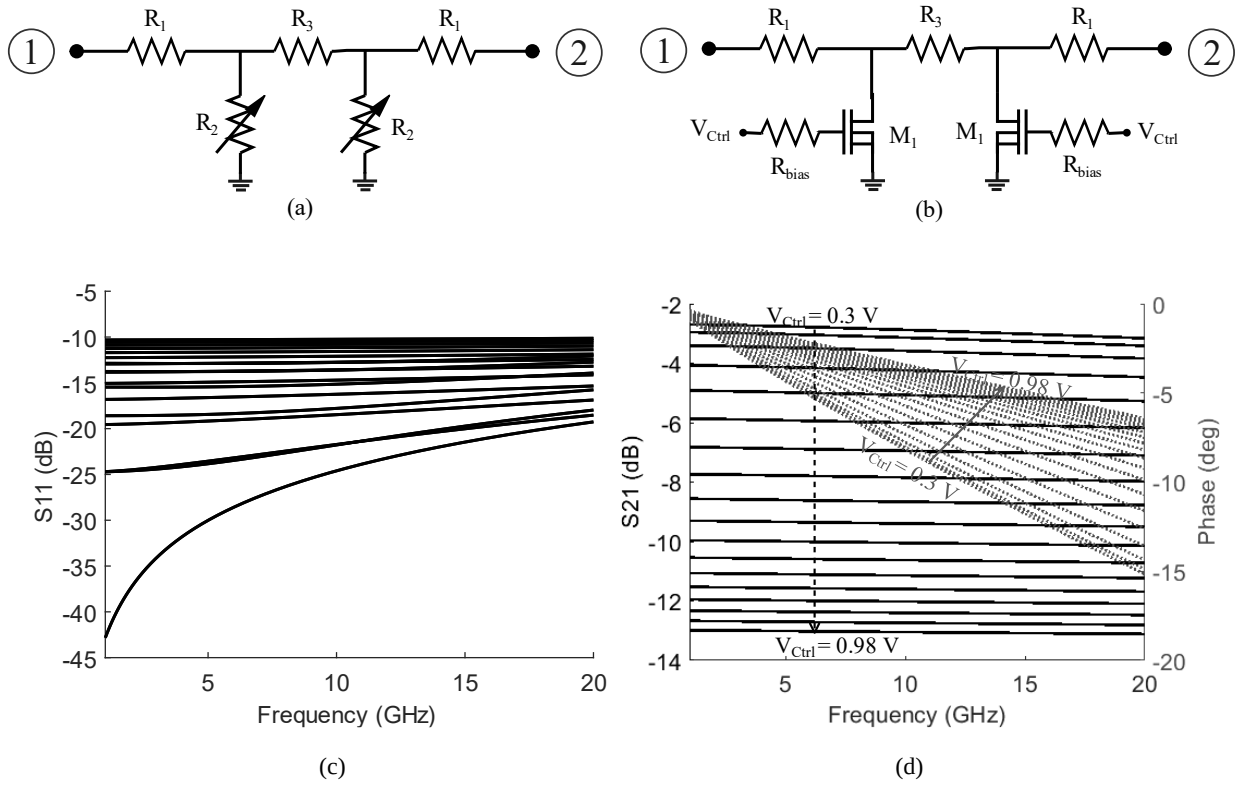


Figure 5.5: Variable attenuator: (a) conceptual schematic with variable shunt resistance R_2, (b) practical schematic with variable resistor implemented using NMOS transistors, (c) plot of the reflection coefficient S11/S22 in dB, and (d) magnitude/phase of attenuation for a VCtrl swept between 0.3 V and 0.98 V, with a step of 0.04 V.

impedance at the maximum gain state can not be perfectly matched to Z_0, since $2R_1 + R_3 \neq 0$. Assuming $R_1 = R_3$ and $Z_0 = 50\ \Omega$, to obtain a reflection coefficient $((R_{in} - Z_0)/(R_{in} + Z_0))$ of -12 dB (0.25), $R_1 = R_3 = 0.22Z_0 = 11.1\ \Omega$. This leads to a maximum attenuation of $A_{max} \approx 0.752 \equiv -2.48$ dB. It follows that the minimum gain state is estimated at -2.48 dB -10 dB ≈ -12.5 dB. Consequently, the required minimum value of R_2 can be found by setting the attenuation expression in (5-6) equal to 0.237 (-12.5 dB) or by using a simulation software and tuning R_2 until the desired attenuation value is obtained. This leads to $R_{2,min} \approx 34.5\ \Omega$. Subsequently, the corresponding reflection coefficient is found as -10.9 dB. Next, it is desired to select a suitable transistor that can provide the desired tuning range. An NMOS biased in the triode region with its drain-source voltage much smaller than its overdrive voltage ($V_{DS} \ll V_{OV}$) acts as a resistor with resistance R_{ON} expressed as [135]:

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{5-7}$$

where $\mu_n C_{ox}$, $\frac{W}{L}$, V_{GS}, and V_{TH} are the technology constant, the transistor width-to-length ratio, the gate-source voltage and the threshold voltage, respectively. For the 130 nm technology, an experimental DC

analysis shows a linear tuning range spanning from $V_{GS} \approx 0.45$ V to $V_{GS} \approx 0.9$ V in the triode region of the NMOS. In order to reduce the output phase variation at different attenuation states, the minimum transistor width that provides a minimum resistance of 34.5 Ω for $V_{GS} \leq 1$ V is selected. This results to $\left(\frac{W}{L}\right)_1 = \frac{16\mu m}{130nm}$ for the transistor M_1. The gate of the transistor is biased through a 1.4 kΩ resistor. Using the found resistances and transistor parameters, the layout of the variable attenuator is generated, and the R-C equivalent circuit of the structure is extracted using Calibre. The S-parameters simulation results of the extracted equivalent circuit are illustrated in Figure 5.5(c) and (d) for a control voltage swept between 0.3 V and 0.98 V with a 40 mV step. From Figure 5.5(c), the return losses of the variable attenuator appear to be below 10 dB for all states between 1 and 20 GHz. Moreover, the attenuation ranges from 2.85 dB to 13.06 dB within the same frequency interval as seen in Figure 5.5(d). Lastly, a maximum phase variation of 8.8º occurs at 20 GHz. This value reduces to 6.8º at 15 GHz.

5.5 Subtractor

As previously stated, analog signal subtraction can be generally done using a balun or transmission line coupling. Nevertheless, transmission line-based balance-to-unbalance signal generation faces a few drawbacks, including large areas and amplitude/phase mismatches, which result in substantial gain imbalance and phase/amplitude error if the phase shifter is to be digitally tuned. For these reasons, an active subtractor is proposed in this work, as shown in Figure 5.6 (a). It is based on current subtraction with phase compensation. The voltage signals at the two input ports (1 and 2) are converted to current signals by the NMOS transistors M_1 and M_2. The current signals are subtracted, and the result is inputted to a buffer, which precedes a single-stage VGA. An identical matching network (MN) is used to match the inputs of the subtractor to the output impedance of the attenuator. The conversion gain of the subtractor can be obtained by computing the transconductances from ports 1 and 2 to the input of the buffer, which is the load of the subtractor. In this regard, two different transconductance values are found: G_{m1} and G_{m2}, the voltage-to-current conversion gains through M_1 and M_2, respectively. G_{m1} is obtained by inputting an alternative current (AC) signal at port 1 and shorting port 2. G_{m2} is found in the vice-versa scenario. Assuming the matching networks exhibit high Q-factors (ideal), the conversion gains are expressed as:

$$G_{m1} \approx \frac{g_{m1}(r_{01}//r_{02})}{g_{m1}R_{in,buff}(r_{01}//r_{02})+R_{in,buff}+r_{01}//r_{02}} \tag{5-8}$$

$$G_{m2} \approx \frac{(1/g_{m1})//r_{02}}{(1/g_{m1})//r_{02}+R_{in,buff}}\, g_{m2} \tag{5-9}$$

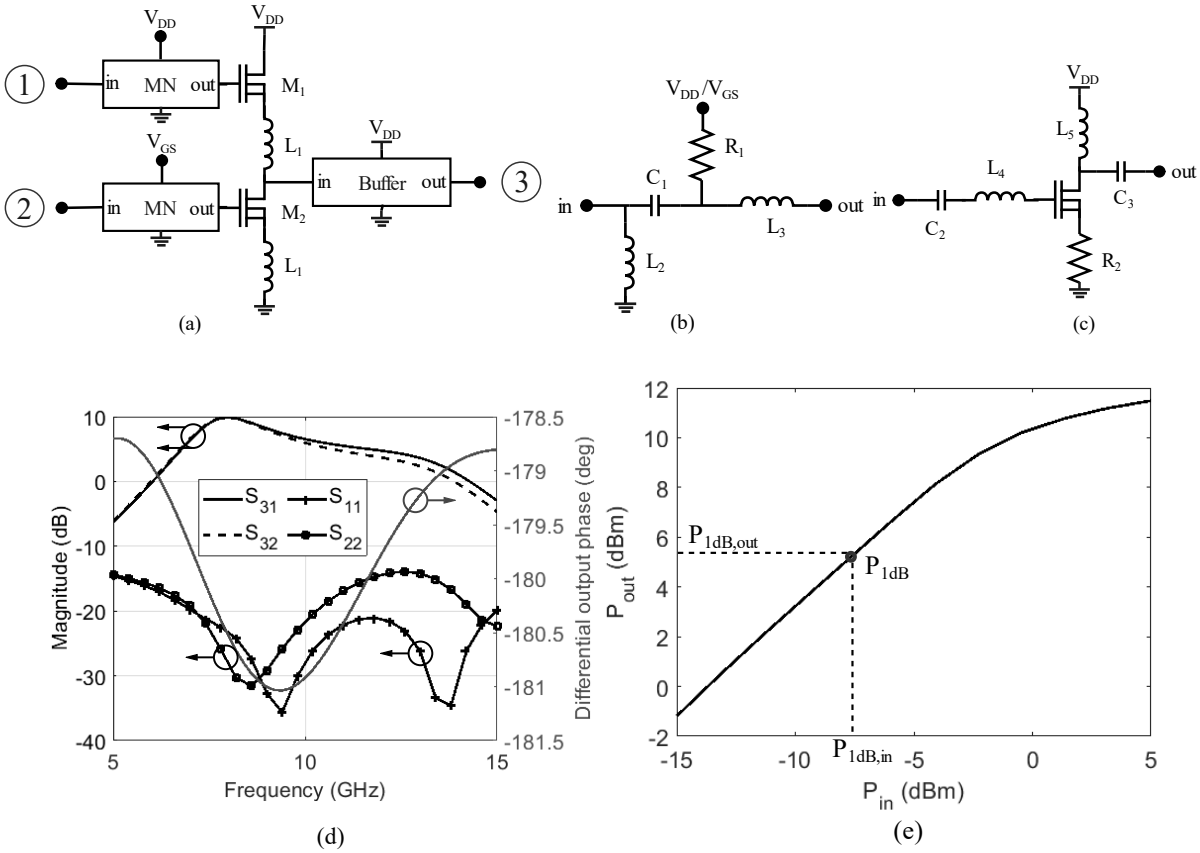


Figure 5.6: Proposed Subtractor: (a) general schematic, (b) input matching network (MN), (c) buffer schematic, and (d) S-parameter simulation results displaying the input reflection coefficients, gains and input-to-output differential phase, and (e) harmonic balance simulation results, showing the 1-dB compression point.

where g_{m1}, g_{m2}, r_{01}, r_{02}, are the intrinsic transconductances and output resistances of M_1 and M_2, respectively, whereas $R_{in,buff}$ is the input resistance of the buffer. If r_{01} and r_{02} are much larger than $R_{in,buff}$, $1/g_{m1}$, and $1/g_{m2}$, (5-8) and (5-9) reduce to:

$$G_{m1} \approx \frac{g_{m1}}{1+g_{m1}R_{in,buff}} \tag{5-10}$$

$$G_{m2} \approx \frac{g_{m2}}{1+g_{m1}R_{in,buff}} \tag{5-11}$$

Furthermore, equilibrated conversion gains are desired for proper signal subtraction. Accordingly, G_{m1} and G_{m2} must be matched ($G_{m1} = G_{m2} = G_m$), leading to the matching of the intrinsic transconductances of M_1 and M_2 ($g_{m1} = g_{m2} = g_m$). Under these circumstances, the conversion gain G_m from each input to the output, the differential mode gain A_d and common mode gain A_c of the subtractor are given as:

$$G_m \approx \frac{g_m}{1+g_m R_{in,buff}} \tag{5-12}$$

$$A_d \approx \frac{1}{2}[G_m - (-G_m)]R_{in,buff} = \frac{g_m R_{in,buff}}{1+g_m R_{in,buff}} \tag{5-13}$$

$$A_c \approx \frac{1}{2}[G_m - G_m]R_{in,buff} = 0 \tag{5-14}$$

Next, transistor sizes will be selected according to the above conditions. The intrinsic transconductance of an NMOS transistor can be formulated as [124]:

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{OV}} \tag{5-15}$$

where I_D and $V_{OV} = V_{GS} - V_{TH}$ are the transistor's drain current and overdrive voltage, respectively. Since the drain currents of M_1 and M_2 are equal, their width-to-length ratios must be equal to maintain matched conversion gain: $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{W}{L}$. Moreover, the maximum theoretical differential gain of the subtractor core (without buffer) is 0 dB and occurs for large values of g_m as demonstrated by (5-13). In this regard, assume $A_d = -3$ dB (0.71). Since $R_{in,buff} = 50\ \Omega$, the required intrinsic transconductance of the transistors is found from (5-13) to be $g_m \approx 50$ mS. To keep the power consumption relatively low, assume $I_D = 2$ mA (relatively low). Using (5-15) or DC simulation by setting $L = 130$ nm and sweeping W, results into $\frac{W}{L} \approx \frac{120\mu m}{130nm}$. Next, degenerative inductors with inductance value L_1 are added to compensate for the insertion phase drift by the parasitic capacitances of M_1 and M_2 at the desired center frequency of 10 GHz. The value of L_1 is found such that the insertion phases from the inputs to the output differ by about 180°. Under ideal input matching, L_1 = 540 pH. Furthermore, input-matching networks are designed to transform the output resistance of the attenuators to the input impedances of M_1 and M_2 under bias conditions (V_{DD} = 1.5 V, I_D = 2 mA). It is worth noting that the output/input resistance of the aforementioned designed attenuators ranges from 50 Ω to 96 Ω, thus an average of 73 Ω, while the input resistance of the biased transistors with L_1 is typically low. The wideband R-L-C matching network in Figure 5.6(b) is used to achieve this impedance transformation. The resistors with resistance value R_1 =120 Ω serve not only for biasing the transistors but also for increasing their low input resistances. The capacitors C_1 in the matching network can be used for further phase adjustment. Moreover, the schematic of the common-source (CS) buffer is given in Figure 5.6(c). The buffer has two main roles. The first one is to provide a fixed load impedance to the subtractor regardless of the signal variation at the preceding or succeeding stages, and the second one is to provide a substantial gain to the subtractor. The transistor M_3

is selected based on the maximum gain and minimum power consumption approach. By sweeping the CS transistor width and measuring the available gain and current at $f_0 = 10$ GHz, the optimum gate width and drain current are found to be $W_3 = 24$ µm and $I_D = 2.6$ mA, resulting in an available gain of 12 dB with a supply voltage of 1.5 V. The input resistance is brought to $R_{in,buff} = 50\ \Omega$ by the inductance L_4 = 1.9 nH and a small degenerative resistance, R_2 = 5.5 Ω, which also helps stability. The inductance L_5 = 700 nH is used to resonate with the parasitic capacitance of M_3 at the center frequency while acting as an RF choke for the transistor. A small capacitance C_2 = 370 fF blocks the DC signal from the previous stage and prevents the alteration of the biasing of the buffer. It also adjusts the phase of the subtractor after buffer loading. The layout of the wideband subtractor with the buffer is designed.

The S-parameter simulation was performed using the EM-analysis of the inductors and the extracted R-C circuits of the transistors, capacitors and resistors, and the results are given in Figure 5.6(d). It can be observed that the input reflection coefficients (dark lines with + and square markers) with reference port impedance corresponding to the attenuator output resistance are all below -14 dB from 5 GHz to 15 GHz. The gains (dark solid and dashed lines) range from -6.1 dB to 10 dB within the same frequency range, with a maximum variation of 1.6 dB. The output phase difference, on the other hand, varies between -181º and -178.7º. Moreover, a single-tone harmonic balance simulation was performed to evaluate the subtractor's linearity and power capability. Figure 5.6(e) displays the output power curve versus the input power swept from -15 dBm to 5 dBm. The simulated differential 1-dB input and output compression points are -7.3 dBm and 5.5 dBm, respectively. This simulated input 1-dB compression point falls above the maximum loss factor produced by the attenuators and phase blocks, which is estimated at - 13.4 dB.

5.6 Variable-Gain Amplifier

From (4-11)-(4-13), the gain of the phase shifter, including the phase blocks, attenuators and subtractor, is estimated to be between -7.8 dB and -2.4 dB. It is, therefore, necessary to use a gain-boosting element to bring the system gain above 0 dB. As the previously designed subtractor buffer demonstrated, a single-stage CS can provide up to 9 dB gain while maintaining stability. Therefore, a simple CS configuration with inductive degeneration has been chosen to fulfill the gain requirement of the system, as seen in Figure 5.7(a). The width of the transistor M_1 is chosen to be relatively large (e.g. W = 80 µm) for better power handling capability. With a supply voltage of V_{DD} = 1.5 V, the drain current and intrinsic transconductance of M_1 under the maximum available gain condition are I_{D1} = 7.8 mA and g_m = 56 mS. In this regard, the expected CS gain for ideal input and output matching with a 50 Ω load impedance ($Z_L = 50\ \Omega$) is $20\log(|g_m Z_L|)$ = 8.9 dB. The degenerative inductance L_1 = 410 pH and the

transistor series gate inductance L_2 = 1.16 nH provide a wideband matching. The inductance L_3 = 700 pH is used as an RF choke for DC bias and to resonate with the parasitic capacitance of M_1. The capacitances C_1 and C_2 help smooth the matching and block DC signals at high frequencies. The amplifier gain can be varied through the DC bias voltage applied at the gate of M_1 (V_G), which changes the bias current of the transistor. The gate bias resistance value is chosen high (R_1 = 5 kΩ). The minimum required VGA gain is 2.4, corresponding to the minimum loss produced by the previous blocks. The designed VGA is simulated using a combination of the Calibre-extracted equivalent circuit of the transistor and capacitors and the EMX-simulated S-parameters of the inductors. The linear simulation results are displayed in Figure 5.7(b) with four different values of V_G (0.36 V, 0.38 V, 0.42 V, and 0.56 V). It can be observed that the input and output reflection coefficients (dark solid lines with + and square markers) are below -5.6 dB at the center frequency of 10 GHz for all tuning states. The matching is altered as we move close to 5 GHz or 15 GHz. The gain (dark solid), on the other hand, varies between 4.1 dB and 8.1 dB at f_0. Moreover, the

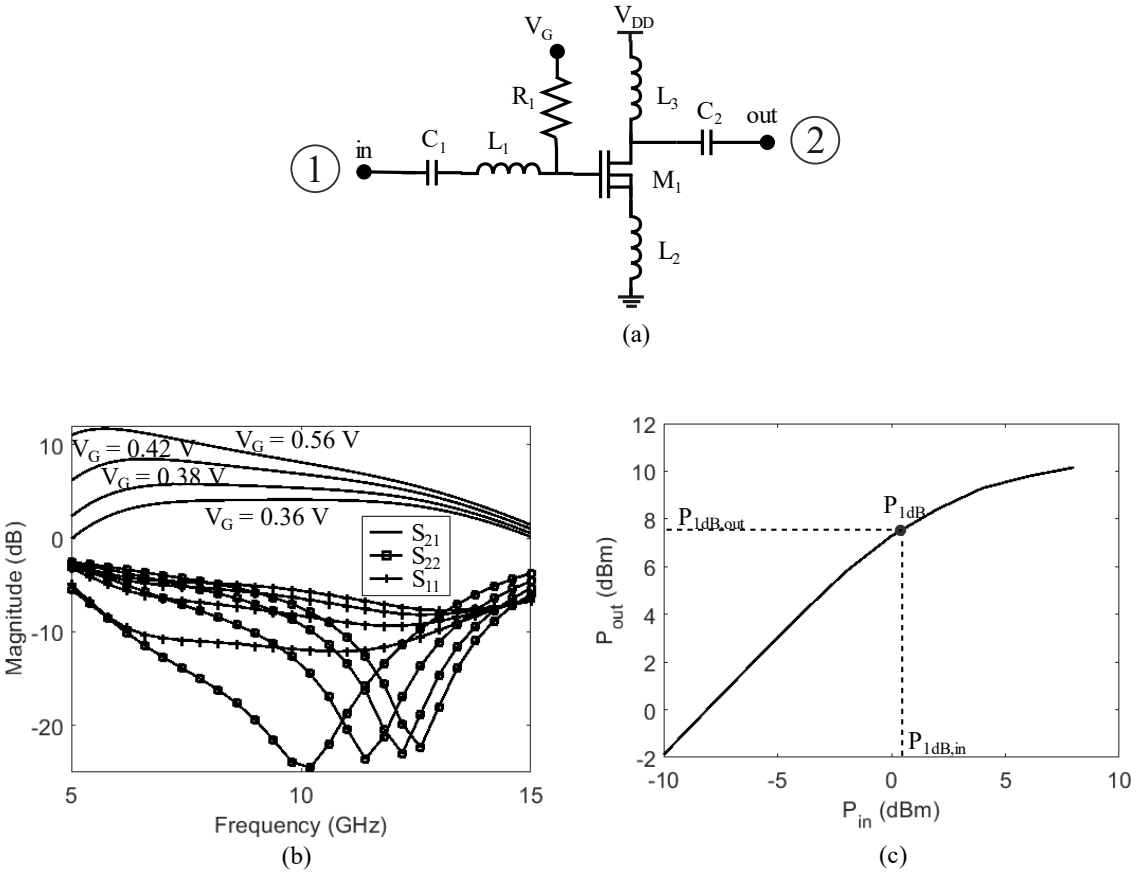


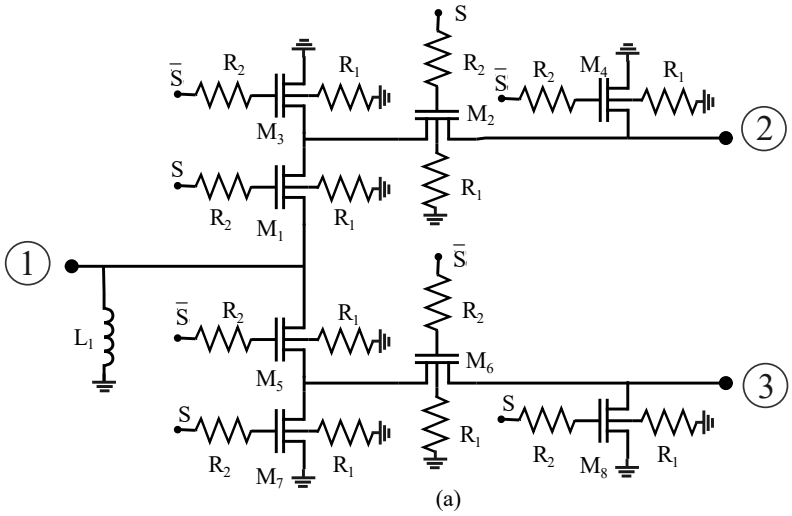
Figure 5.7: VGA: (a) schematic, (b) Plot of S-parameters simulation results, and (c) curve of the output power versus the input power showing the 1-dB compression point.

harmonic balance simulation is performed for the maximum linear gain state (8 dB) and by sweeping the

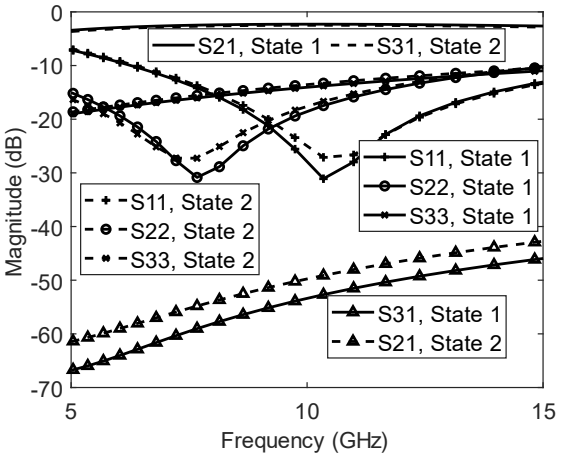
input power from -10 dBm to 8 dBm. An input 1-dB compression point of 0.397 dBm is obtained with a maximum power of over 10 dBm, as illustrated in Figure 5.7(c).

5.7 SPDT Switch

As represented in Figure 5.1, the SPDT switch at the module's input and output allows the system to be used in transmit or receive mode. Sharing blocks like the phase shifter and VGA between the paths leads to lower power consumption and smaller chip area. The schematic of the proposed SPDT switch is depicted in Figure 5.8(a). Similar to the DPDT switch designed in section 5.3, it is based on synchronized switching with boosted isolation. Here, it is crucial for the switch to exhibit high isolation (above 30 dB) to minimize signal leakage between the transmit and receive paths. When $S = V_{DD} = 1$ V (or "high") and $\overline{S} = 0$ ("low"), the transistors M_1, M_2, M_7, and M_8 are ON, while M_3, M_4, M_5, and M_6 are OFF. As a result, the RF signal flows from the input at port 1 to the top output at port 2. This is State 1 of the switch. During State 2, $S = 0$ and $\overline{S} = V_{DD}$, the signal flows from port 1 to port 3 in a similar mechanism. The insertion losses of the switch mainly depend on the ON resistance of M_1, M_2, M_5, and M_6, which are, therefore, chosen to have relatively large gate widths ($W_{1,2,5,6} = 60$ µm). In addition, the insertion losses are further improved by floating the bulk of the transistors through a large resistance $R_1 = 1.5$ kΩ. Moreover, the isolations are mainly controlled by M_3, M_4, M_7, and M_8. The widths of M_3 and M_7 are relatively large ($W_{3,7} = 60$ µm), offering low resistance to the ground during their OFF states. Meanwhile, smaller widths for M_4 and M_8 ($W_{4,8} = 9.6$ µm) exhibit ON resistances close to 50 Ω and, therefore, match the output port resistance in the non-transmitted signal path. Since the SPDT switch is the first and last block of the module, the shunt inductance $L_1 = 1$ nH is selected to resonate with the effective parasitic capacitance of the transistors and the RF input/output pad at the center frequency, therefore providing matching during signal transmission. Additionally, the shunt inductance L_1 helps protect the switch transistors from the electrostatic discharge (ESD). The gate control voltages of the transistor are applied through identical bias resistors with resistance $R_2 = 1.5$ kΩ. The bypass-inversion voltage generator circuit in Figure 5.3(b) is employed to control the switch through a single control voltage (V_{Ctrl}). In this regard, State 1 and 2 are produced when $V_{Ctrl} = V_{DD}$ and $V_{Ctrl} = 0$, respectively. The layout of the SPDT switch is designed, and the post-layout S-parameters and harmonic balance simulations are performed. As demonstrated by Figure 5.8(b), both states' linear simulation results appear identical. At the center frequency, the input and output reflection coefficients obtained are -25.7 dB and -17.2 dB, respectively, and the worst-case reflection coefficient is -7.1 dB between 5 GHz and 15 GHz. The insertion losses, on the other hand, range from 3 dB to 4.5 dB, within the same frequency range. Finally, the minimum



(a)



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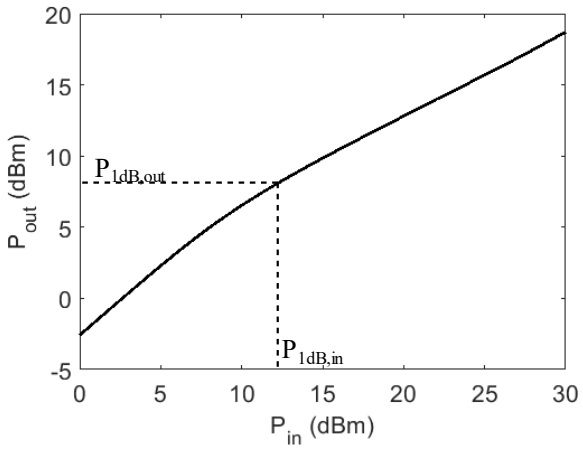


(c)

Figure 5.8: Proposed SPDT: (a) schematic, (b) Plot of S-parameters simulation results, and (c) harmonic balance simulation results of input-output power characteristic showing the 1-dB compression point.

isolation at the center frequency is 50.1 dB, with a worst-case of 42.9 dB from 5 GHz to 15 GHz. The nonlinear simulation results show the switch's high linearity and power handling capability with an input 1-dB compression point estimated at 12 dBm, as illustrated in Figure 5.8(c), which describes the input-output power characteristic.

5.8 System Results and Comments

The above-designed blocks were interconnected, and the layout of the RF module, including the phase shifter and the input/output SPDT switches, was generated in the 130 nm bulk technology. Illustrated in Figure 5.9, the layout of the overall module measures 2.40×1.11 mm^2. Nevertheless, the area

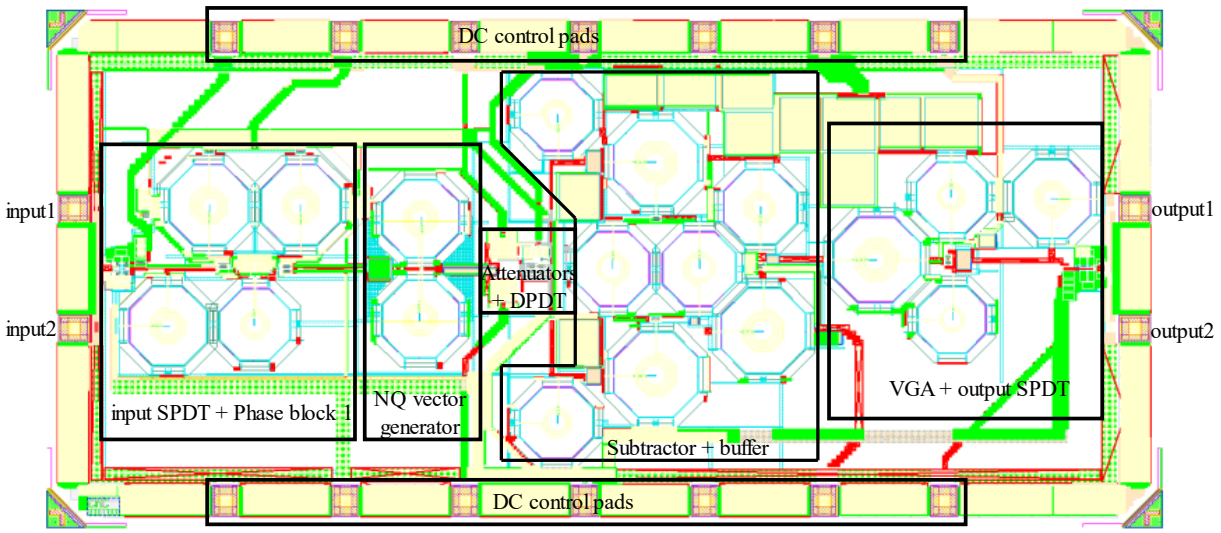
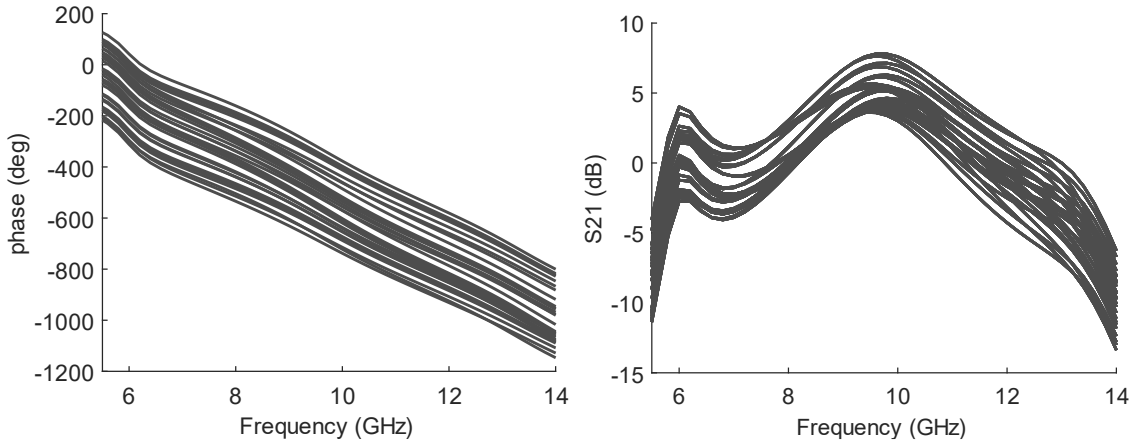


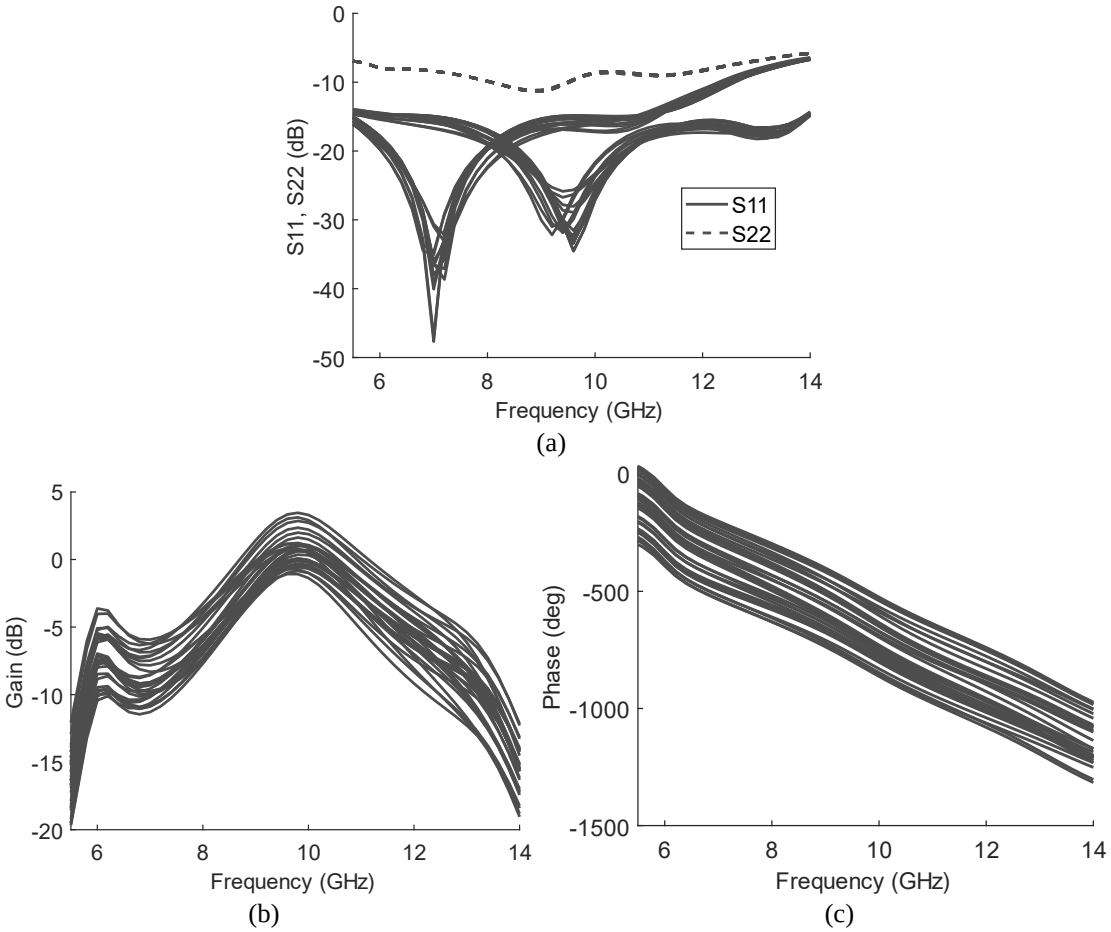
Figure 5.9: Graphic description of the designed IC module, containing the phase shifter blocks and input/output SPDTs.

occupied by the NQ modulator phase shifter core (including the output VGA) is 1.84×0.877 mm^2. The post-layout linear and non-linear simulations included the EMX-extracted S-parameters of the inductive elements and the Calibre-extracted parasitics of the transistors, capacitors, resistors and interconnect lines. The S-parameters phase and gain of the NQ vector modulator, with the output VGA maintained at its maximum gain state, were simulated by sweeping the attenuator control voltage from 300 mV to 700 mV, which corresponds to an attenuation range of about 8.1 dB, and the results are represented in Figure 5.10(a) and (b), respectively. It can be observed that the proposed phase shifter achieves a total phase shift of at least 360.8º with continuous resolution from 6.4 GHz to 15 GHz. On the other hand, an acceptable gain range is obtained from 6.4 GHz to 13 GHz, with a minimum and maximum of -7.1 dB and 7.79 dB, respectively. Thus, the frequency of the vector modulator is centered at 9.7 GHz with a bandwidth of 6.6 GHz. The maximum gain imbalance within this bandwidth is about 4.2 dB. Next, the linear simulation of the front-end system, with the inclusion of the SPDTs and the phase shifter, was performed. From Figure 5.11(a), the input reflection coefficients (solid lines) are below -11 dB from 5 GHz to 12 GHz; they increase to a maximum of -8.01 dB at 13 GHz for all phase states. The output reflection coefficients (dashed lines), on the other hand, vary between -11.3 dB and -6.95 dB within the desired frequency range. It is worth noting that the output reflection coefficient here serves as a stability factor instead of a signal reflection factor since the RF signal is unidirectional. The gain of the system ranges from -12.2 dB to 3.3 dB within the desired frequency range while maintaining a total phase range of more than 360º, as seen in Figures 5.11(b) and 5.11(c). The minimum isolation of the system, which is exhibited by the input SPDT, presents a value of 49.88 dB at 13 GHz, as shown in Figure 5.11(d). Lastly, the harmonic balance simulation of the system and the amplified phase shifter section was carried out to analyze their nonlinear



(a) (b)

Figure 5.10: (a) Phase and (b) gain simulation results of the proposed NQ vector modulator phase shifter for 32 tuning states.



(a)

(b) (c)

Figure 5.11: (a) Reflection coefficients, (b) gain and (c) phase simulation results of the designed RF front-end.

characteristics. A 2-tone harmonic balance simulation was performed at 9.6 GHz and 9.8 GHz by sweeping the input power from -5 dBm to 15 dBm, and the results are displayed in Figure 5.12(a) and

Figure 5.12(b). The system output-input characteristic at the fundamental frequency (e.g. 9.8 GHz) is plotted in dark solid lines along with that at the third-order intermodulation product (e.g. 10 GHz) (designated by dark solid line with x markers) in Figure 5.12(a). A system input and output 1-dB compression point of 3.78 dBm and 2.38 dBm are obtained, whereas the maximum output power reaches 6.6 dBm. Additionally, an input IP3 of 9.1 dBm is obtained. With regard to the phase shifter, an input 1-dB compression point, maximum output power and input IP3 of 0.05 dBm, 7.3 dBm and 7.2 dBm are obtained, respectively, as illustrated in Figure 5.12(b).

The performance of the designed NQVSPS is summarized in Table 5.2 and compared to state-of-the-art relevant works. The designed phase shifter without (Work1) and with (Work2) VGA biased at its maximum gain state was considered for performance comparison. The VSPS design in [151] achieves a 360º phase shift with a 6-bit phase resolution over a 40 % fractional bandwidth in the X-band. Despite having a gain range close to 0 dB and a relatively smaller chip area (1.645 mm^2), the designed phase shifter consumes a DC power of 110 mW, which is relatively high. [153] proposes an alternative digital STPS design with much lower power consumption while maintaining a 40 % fractional bandwidth. Nevertheless, besides displaying a limited phase control

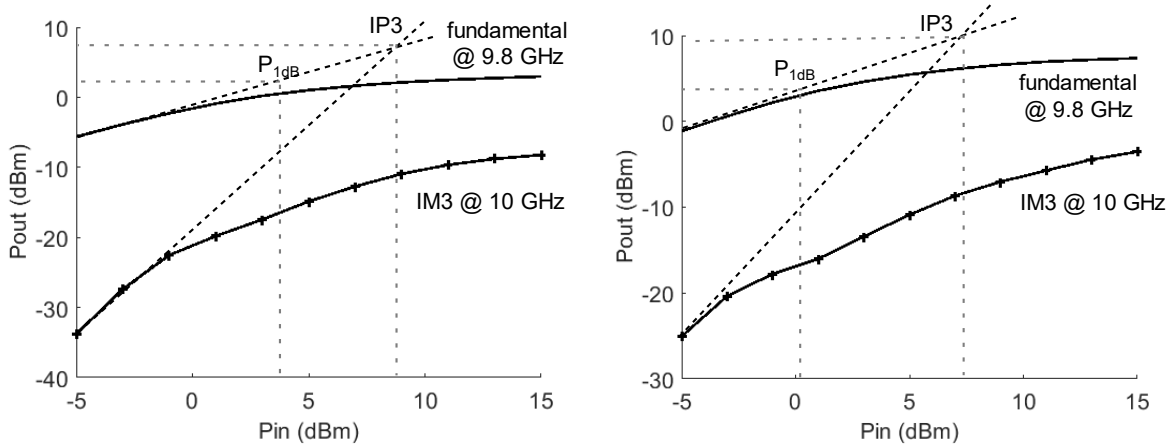


Figure 5.12: 2-tone harmonic balance simulation results of (a) the RF module including the phase shifter and the SPDT switches and (b) the vector modulator phase shifter. The fundamental frequency and IP3 are taken at 9.8 GHz and 10 GHz, respectively.

bit, it exhibits a mean insertion loss below 10 dB. The vector modulator proposed in [154] offers a continuous resolution at a center frequency of 22.5 GHz using the 130 nm CMOS technology. In contrast, its phase range is limited to only 150º. A 360º continuous phase shift was obtained in [155] with a mean loss of only 3.3 dB in the X-band. In spite of using the PCB technology with a larger design area, the achieved fractional bandwidth is limited to 8.7 %. Meanwhile, the proposed phase shifter achieves at least

360º of analog phase with a 68 % fractional bandwidth in the X-band. Additionally, the chip area and power consumption of the proposed NQ modulator, including the output VGA at its maximum gain state, are 1.6 mm^2 and 18.9 mW, respectively. Finally, the mean gain within the bandwidth is estimated at 0.345 dB, with an input 1-dB compression point of 0.05 dBm at the center frequency. Compared to reported designs in the X-band or beyond, the proposed phase shifter appears to exhibit relatively lower power consumption and smaller chip area while providing fine phase resolution.

Table 5.2*:* Performance summary of the proposed vector modulators and comparison with relevant works.

Reference	**[151]**	**[153]**	**[154]**	**[155]**	**Work1**	**Work2**
Technology	250nm BiCMOS	250nm GaN HEMT	130nm CMOS	PCB	**130nm BiCMOS**	**130nm BiCMOS**
Type	VSPS	STPS	VSPS	RTPS	**VSPS**	**VSPS**
f_0 /FBW (GHz / %)	10/40	10/40	22.5/22.2	11.5/8.7	**9.7/68**	**9.7/68**
Phase range/resolution (˚/bits)	360/6	360/5	150/cont.	>360/cont.	**>360/cont.**	**>360/cont.**
RMS phase error (˚)	2-6.4	2.52-6.23	<3.5	-	**-**	**-**
RMS gain error (dB)	1.6-2	0.41-1.16	<2	-	**-**	**-**
Gain (dB)	-4.5±2	-11.65±3.45	-8 @ 23 GHz	-3.3±0.5	**-7.8 @ 10 GHz**	**0.345±7.445**
input P_{1dB} @ f_0	-11	29	-	-	**0.4**	**0.05**
Size (mm^2)	1.646	6	0.435	400	**0.96**	**1.614**
Power consumption (mW)	110	0	18.5	-	**7.2**	**18.9**

Lastly, the performance metrics of the designed RF module, including the phase shifter and the SPDT switches, are summarized in Table 5.3. The wideband X-band RF module front-end holds a gain ranging from -12.2 dB to 3.3 dB with a minimum return loss of 8 dB. The module can be used in a transceiver with a minimum in-band isolation close to 50 dB. Meanwhile, it exhibits compression-driven

Table 5.3: Summary of the designed X-band RF module with SPDT switches and phase shifter.

Parameter	Technology	Frequency (GHz)	Gain (dB)	Return loss (dB)	Isolation (dB)	$P1_{dB,in}$ (dBm)	IIP3 (dBm)	P_{DC} (mW)	Size (mm^2)
Value	130nm CMOS	6.4~13	-12.2~3.3	>8.01	>49.88	3.78	9.1	18.9	2.66

and intermodulation-driven linearities for input signals below 3.78 dBm and 9.8 dBm, respectively. With digital and analog supply voltages of 1 V and 1.5 V, respectively, the module consumes a total DC power of 18.9 mW. The low-power, high-isolation and fine phase resolution qualities of the design RF module make it suitable for applications such as phase-array radars for weather monitoring or military surveillance. Moreover, the use of the 130nm process allows for a cost-effective transceiver design.

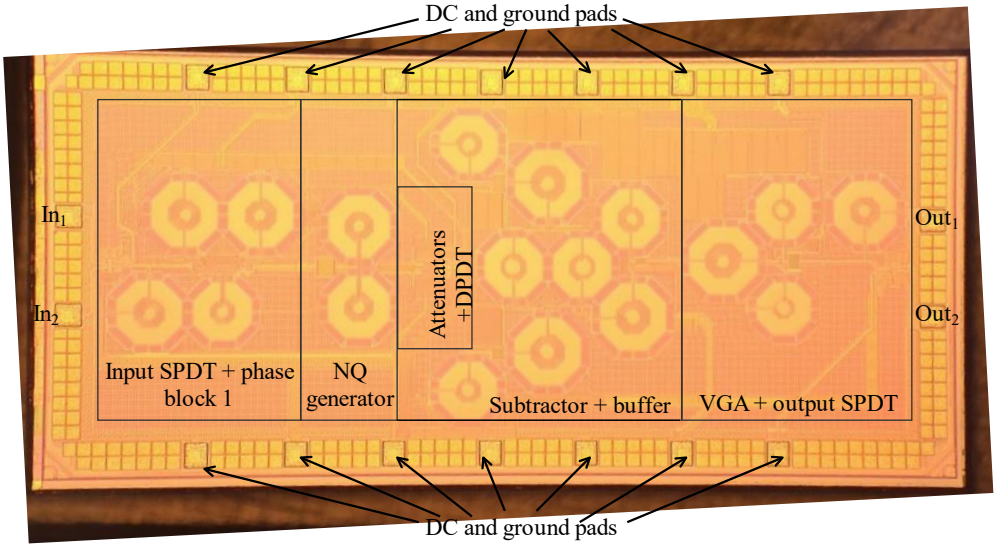
The designed RF module was manufactured as seen in Figure 5.13 (a), which displays a descriptive micrograph of the fabricated chip. The chip was wire-bonded to a package and assembled on a PCB test bench along with other components like off-chip DC coupling capacitors and RF chokes. The photograph of the packaged IC module is represented in Figure 5.13(b). Despite passing design rule checks (DRC) and layout-versus-schematic (LVS) verification, the measured performance exhibited little to no signal transmission from input to output, indicating a potential malfunction in the fabricated IC. Since the module lacked an integrated failure diagnosis mechanism (due to budget constraints), the exact cause of failure remains speculative. However, several plausible factors could explain the observed behavior:

- Improper DC biasing of active devices: The module incorporates active blocks, including a subtractor, buffer, and VGA, which rely on precise biasing to maintain transistor operating points. Inadequate biasing networks may force devices into cutoff, disrupting signal amplification. Additionally, insufficient DC decoupling capacitors could displace the devices' bias points and allow power supply noise to couple into sensitive nodes, leading to signal distortion or complete blockage.
- Excessively long bond wire parasitics: The bond wires (typically introducing 1–2 nH/mm of inductance) may have been excessively long, degrading impedance matching at RF frequencies. This can create parasitic resonances, causing signal reflections or attenuation, particularly at the input and output interfaces.
- Thermal stress during bonding: The high-temperature bonding process may have induced thermal stress in the die, potentially damaging interconnects or altering semiconductor

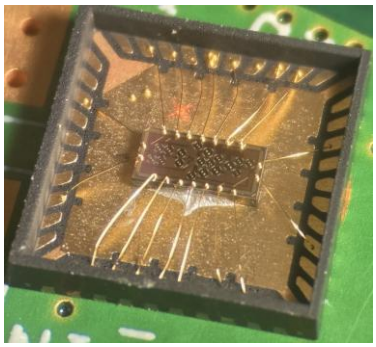
properties. This could lead to increased contact resistance, microcracks, or dopant diffusion, ultimately contributing to device failure.

- Electrostatic discharge (ESD) damage: ESD exposure during handling, assembly, or testing could have caused latent defects, such as gate oxide breakdown or junction failures in active devices. These defects might manifest as abnormal leakage currents or open circuits, disrupting signal propagation.

Although the measured results were unsatisfactory, the operating principles of the module remain valid, as confirmed by simulations. To mitigate these issues in future iterations, the following



(a)



(b)

Figure 5.13: (a) Micrograph of the fabricated RF module, (b) Photograph of the packaged RF module chip.

improvements are recommended:

- Redesign the biasing network for active blocks (subtractor and VGA) to ensure proper DC operation.
- Increase decoupling capacitance at supply nodes to stabilize bias voltages and suppress noise.
- Select the proper chip package and optimize bond wire length and placement to minimize parasitic inductance. Estimating the parasitics brought by the bond wires can also be useful in accounting for input and output mismatches.
- Implement an ESD protection and integrate a fault detection mechanism for improved robustness and diagnostics.

5.9 Conclusion

This chapter was dedicated to the design of an RF module comprising a novel vector modulator phase shifter and input/output SPDT switches in the 130 nm CMOS process. The constituent blocks of the modules were designed and simulated, and ultimately combined to obtain and evaluate the performance of the phase shifter and the overall system. The designed phase shifter generates at least 360º continuous phase range from 6.4 GHz to 13 GHz, with a median gain above 0.345 dB, a total DC power consumption of 18.9 mW and a size of 1.61 mm^2. With these performance metrics, the proposed vector modulator approach offers lower power consumption and smaller area compared to most state-of-the-art phase shifter designs while offering fine resolution. Additionally, the designed RF module possesses a path isolation above 49 dB, an input 1-dB compression point of 3.78 dBm, an input IP3 of 9.1 dBm and a total chip size of 2.66 mm^2, making it useful for applications involving cost-effective X-band phased array radars. In the next and final chapter, a summary of the dissertation is provided, along with projections for future work.

Chapter 6

Conclusions and Future Works

6.1 Conclusive Remarks

This dissertation was motivated by the cost and performance limitations of electronic phase shifters in antenna array systems, which are critical components in modern wireless communication and radar applications. The increasing user bandwidth demands of next-generation telecommunication systems impose stringent performance requirements on phase shifters, particularly in terms of phase resolution, size and power efficiency.

An extensive review of phase shifter technologies used in phased array systems was conducted, categorizing them by tuning mechanism: mechanical, ferromagnetic, electronic, MEMS, and liquid crystal-based designs. Among these, electronic phase shifters remain the most widely adopted due to their compact form factor, fast response time, and compatibility with semiconductor integration. A detailed comparative analysis was performed on four primary electronic phase shifter topologies—switched-type, reflective-type, loaded transmission line, and vector-sum phase shifters—identifying key bottlenecks and mitigation techniques. The vector-sum phase shifter (or vector modulator) emerged as a particularly promising solution due to its compact size and superior system gain. This study culminated in a review article published in the *International Journal of Circuit Theory and Applications* [156].

A study of the linearity and noise of conventional quadrature vector modulators was covered. These modulators incorporate nonlinear and noise-prone components, such as variable gain amplifiers (VGAs) and quadrature signal generators, which introduce gain compression, phase errors, and gain imbalance. As a rule of thumb, it is recommended to operate at input signal powers lower than $\sqrt{2}$ times the input 1-dB compression point of the VGAs to avoid significant performance degradation. Moreover, a phase noise created by the quadrature signal generator appears at the output of the modulator, and the noise figure of a vector modulator lies at least 3 dB below the maximum noise figure of individual signal branches.

Despite their prevalence in high-frequency applications, state-of-the-art quadrature vector modulators suffer from limitations such as restricted phase resolution, narrow bandwidth, and high power consumption. Moreover, generating precise quadrature and balanced signals remains a significant challenge. To address these issues, this thesis proposes a novel vector modulator architecture based on

unbalanced, non-quadrature signal generation and synthesis. A proof-of-concept PCB prototype demonstrated 360° analog phase tuning with a compact footprint. The design incorporates bandwidth-enhancing techniques, including open- and shorted-stub phase compensation, along with a novel wideband analog subtractor, achieving over 50% fractional bandwidth.

Furthermore, an X-band RF module integrating the proposed non-quadrature vector modulator and SPDT switches was designed and simulated in a 130nm CMOS process. Simulation results confirmed significant reductions in size and power consumption while extending operational bandwidth compared to existing solutions. These advancements suggest that the non-quadrature vector modulator approach offers superior phase resolution, lower power consumption, and a smaller form factor relative to traditional quadrature vector-sum phase shifters. This work has been disseminated through one conference paper [157], one letter [158], and one journal article [159].

6.2 Future Works

The ultimate goal of the proposed non-quadrature vector modulator is to enable low-cost, high-performance phased array systems for consumer applications, such as weather surveillance and remote sensing. To validate its real-world applicability, field testing of a complete phased array radar system—incorporating the developed phase shifter and its beamforming network—is essential. While the proposed active phase shifter demonstrates significant potential in bandwidth enhancement, power efficiency, and area reduction, further optimization in a cost-effective semiconductor technology is necessary to fully realize its advantages over existing solutions.

To this end, the following future research directions are proposed:

- **Design and Implementation of Non-Quadrature Vector Generators in CMOS**: Unlike conventional quadrature signal generators (e.g., baluns and couplers), the synthesis of wideband signals with phase differences below 90° remains largely unexplored. While basic non-quadrature vectors can be generated using power splitters and transmission lines, novel design techniques are required to maximize phase bandwidth and minimize size—particularly in CMOS implementations. This investigation will focus on optimizing phase accuracy and bandwidth while maintaining compactness.
- **Development of Wideband Analog Subtractors in CMOS:** Traditional analog subtraction relies on hybrid coupler baluns, which suffer from narrow bandwidth and amplitude mismatch, leading to gain imbalance in phase shifters. To overcome this

limitation, this work will explore advanced passive and active subtractor topologies with integrated phase compensation techniques. The goal is to enhance overall modulator bandwidth while minimizing gain and phase errors.

- **Fully Integrated 4-Element Transceiver with the Proposed Phase Shifter**: A key milestone will be the design and fabrication of a complete CMOS transceiver incorporating the novel phase shifter alongside essential RF and baseband components, including LNAs, PAs, SPDT switches, VGAs, mixers, transimpedance amplifiers, baseband filters, and ADCs. The anticipated reductions in chip area and power consumption from the phase shifter should translate into a more compact and energy-efficient phased array system.
- **Phased Array Radar Prototyping and Field Testing**: The final validation step involves integrating the transceiver with PCB-based antenna elements and deploying the system in real-world radar applications, such as weather monitoring, vital signs detection, or non-destructive testing. Signal processing will be performed using a computer, followed by field trials to evaluate performance under practical conditions.

By addressing these research directions, this work aims to transition the proposed non-quadrature vector modulator from a proof-of-concept into a viable, cost-effective solution for next-generation phased array systems.

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