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AN ALL-DIGITAL LOW-FREQUENCY VECTOR NETWORK ANALYZER

by

SUDHIR JHAJHARIA

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ABSTRACT

Vector transmission and reflection parameters of a device are measured in terms of the amplitude ratio and phase difference between the sinusoidal incident signal and the sinusoidal reflected or transmitted signals. The measurement system digitally synthesizes the incident signal and then samples the incident and reflected or transmitted signals at predetermined intervals. The signal samples are digitized, and the reflection or transmission coefficients calculated by sine curve fitting.

System performance is modeled on a computer to investigate the effects of input noise, harmonics, sampling time error and quantization error on the results of a simulated amplitude ratio and phase difference measurement. With 12 bit analog-to-digital conversion and the sampling rate of 200 kHz an accuracy of ±0.015 dB for magnitude and ±0.1° for phase can theoretically be obtained from 1 Hz to 20 kHz.

The uncertainties of the experimental system are within ±0.02 dB standard deviation in magnitude and ±0.2° standard deviation in phase in the frequency range from 1 Hz to 12 kHz. Measurements upto 24 kHz can be made with somewhat greater uncertainty.

ACKNOWLEDGEMENTS

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Chapter I

INTRODUCTION

The primary objective of this work has been to design, implement and evaluate a network analyzer which generates and detects signals using digital techniques. Without getting into the details of the process itself, a few words about the nature of the process should suffice to introduce the subject.

Network Analysis is primarily concerned with transmission and reflection characteristics of networks. While the transmission characteristics of a network (a device) specify how efficiently energy is transferred through the device, the reflection characteristics show the effectiveness of energy-transfer into the device. Frequency is an independent parameter, as a function of which the above two are measured.

1.1 DEFINITION OF NETWORK MEASUREMENT :

The purpose of network analysis is to completely characterize or describe a network, so that one will know how it will perform when stimulated by some signal.

Network analysis has two main subdivisions :

1. Scalar network measurements and
2. Vector network measurements.

Scalar network measurements involve magnitude and frequency information only. On the other hand, vector network measurements are the measurement of transmission and reflection characteristics of a device, in which both magnitude and phase are measured.

1.2 BASIC COMPONENTS OF A NETWORK ANALYZER :

In network measurements, the amplitude and phase information of the incident, reflected and transmitted waves are used to quantify the vector transmission and reflection characteristics of a device. The ratio of the power associated with the incident and the reflected (or transmitted) waves and the phase difference between them are measured by a network analyzer. In doing so, network analyzers employ scattering parameters, which are used to characterize a device. The reason for using s-parameters is that they are related to familiar terms such as gain, loss and reflection coefficient and the ease with which they can be measured by conventional reflection and transmission measurement techniques.

A typical network analyzer system consists of :

1. a source
2. a signal separation device
3. a receiver/detector and
4. a display.

The source generates the incident wave. It can be a sweep oscillator to characterize a device as a function of frequency or a single frequency source. To test a narrow-band device or a device with rapidly changing characteristics with frequency, synthesizers are used as sources. In the selection of a source, frequency range, output power, programmability for automatic measurement, frequency accuracy and repeatability are usually considered.

Signal separation in transmission measurements is obtained using either a 3-dB directional coupler or a broadband power splitter. In reflection measurements, separation of the incident and reflected signals is accomplished using a dual directional coupler or a power splitter/directional bridge.

The functions of the receiver are :

1. to convert high frequencies to DC or low frequencies and
2. to detect magnitude ratio and phase differences .

There are three basic receiver techniques used in network analysis.

1. Diode detection : The diode converts the high frequency signal level to a proportional dc level.
2. Fundamental mixing : In fundamental mixing, the local oscillator always tracks the RF signal by a fixed frequency equal to the I.F.. This allows a simple mixer conversion to a fixed low frequency I.F..

3. Harmonic mixing : The harmonic mixing uses the harmonic of a low frequency oscillator as the local oscillator signal to the mixer. This technique provides extremely wide frequency coverage with a single local oscillator.

The magnitude of the single low frequency signals are measured precisely to obtain the magnitude ratio. The phase measurements are accomplished by a phase detector.

The magnitude and phase characteristics thus measured are displayed in an appropriate form. The displays used are Rectilinear displays, to indicate magnitude, phase, or group delay. Polar displays are used to plot complex quantities in a single coordinate system. Addition of digital storage provides a flicker-free display for ease of parameter reading.

1.3 APPLICATIONS OF NETWORK ANALYZERS :

Typical applications of the network analyzer in the swept frequency mode, include characterization of transmission and reflection properties of components, devices and subsystems. A summary of applications is shown in Tablel.

Vector measurements of impedance are important in optimizing power-transfer in multistage amplifiers. To achieve this, the output impedance of a given stage must be the complex conjugate of the input impedance of the following stage. Knowledge of the complex impedance is also

necessary in designing feedback amplifiers. The proper feedback can be determined experimentally when the basic amplifier characteristics are not known.

Group delay measurements are important in audio- and video-frequency amplifiers and networks. In transmission systems with complex waveforms, a linear phase characteristic is necessary to prevent wave-shape degradation.

And finally, transmission loss and return loss measurements can characterize a dielectric material in the required frequency band and these measurements are an integral part of dielectric spectroscopy.

1.4 A DIGITAL NETWORK ANALYZER SYSTEM :

Of the many factors contributing to measurement uncertainty of the network analyzers, the most important are :

1. noise
2. temperature variation
3. reflections and
4. directivity

With the advent of digital technology, it has become possible to use digital signal processors to replace analog circuitry. Properly programmmed, these processors replace inductors, capacitors and op-amps and can oscillate, modulate, mix, filter, code, and decode in real time. They do so with superior accuracy and with a circuit-to-circuit consistency previously unattainable.

TABLE 1

SUMMARY OF APPLICATIONS OF NETWORK ANALYZERS

Vector network analyzers are used to measure

TRANSMISSION PROPERTIES

GAIN/LOSS

PHASE SHIFT

Group delay

Time delay

Electrical length

REFLECTION PROPERTIES

COMPLEX IMPEDANCE (ADMITTANCE)

REFLECTION COEFFICIENT (VSWR)

RETURN LOSS

These measurements can be made on

COMPONENTS	DEVICES	SUBSYSTEMS
Filters	Bipolar Transistors	Receivers
Amplifiers	FET's	IF Sections
Antennas	Diodes	
Cables	Tunnel Diodes	
Couplers	IC's	
Attenuators		
Phase shifters		
Connectors		

DIELECTRIC PROPERTIES OF MATERIALS

Dielectric Constant
Loss Factor

This alternative to a great extent, counteracts the above unwanted factors and provides the following major advantages:

1. Limited susceptibility to noise and interference.
2. Stablity as a function of temperature and aging.
3. Insensitivity to relatively large deviations in component parameters.
4. High accuracy.

The source (synthesizer) and receiver/detector of a network analyzer system can each be replaced by an all-digital processor. Figure 1 depicts the basic block diagram of such a system. This system has the potential of being developed into an independent stand-alone network analyzer and works as an intermediate stage leading to that final configuration.

Although computer-controlled analog circuitry for network measurement automation is widely known, use of digital signal processing for detection in network analysis has not been reported.

1.5 OUTLINE OF THE THESIS :

Chapter two reviews the network analyzer systems and presents, in brief, the organization of the Hewlett-Packard HP8407 network analyzer.

The third chapter explains the technique used to retrieve relative amplitude and phase from the digital data and

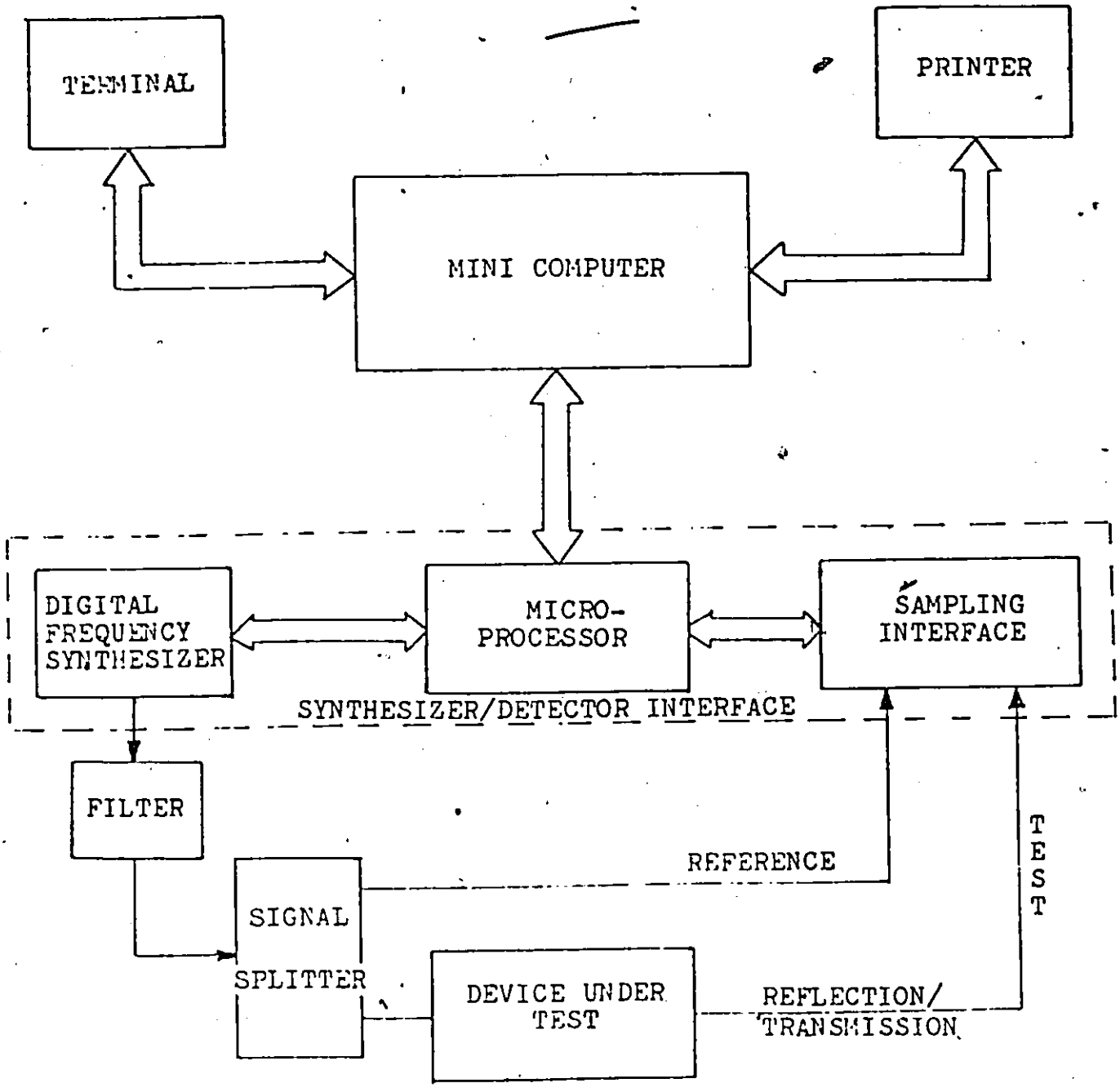


Figure 1: Basic block diagram of an all-digital network analyzer

details the principles of operation of the digital network analyzer.

Computer simulation of the measurement system is presented in chapter four. The simulation was used to investigate the effects of sampling rate, A/D converter bit resolution, amplitude ratio changes and signal/noise ratios on the measurement system in order to gain better understanding of the system.

Chapter five discusses the hardware aspects of the system emphasizing the non-standard components and the limitations of the hardware. Also presented in this chapter is the flowchart of the software. This implementation is semi-automatic, with a friendly human interface, requiring minimum operator intervention. This chapter also discusses the software under three main headings - operator interface, data acquisition and data processing, respectively.

The sixth chapter contains a critical evaluation of the system, followed in chapter seven by recommendations for further improvements and future work.

The main contribution of this work lies in establishing digital techniques for network analysis measurements, the procedural improvements resulting in the advantages stated in section 1.4, and the suggestions for future work. The tangible result is the easily understandable software in a high-level language which can be readily modified for further improvements and carried over into the implementation stage as recommended in chapter six.

Chapter II

A REVIEW OF THE STATE-OF-THE-ART

In the first part of this chapter, a brief account of the history of network measurements, using network analyzers, is reviewed. The second part contains a discussion on some of the aspects, of the present HP systems, which are suitable for replacement by digital processors.

2.1 A BRIEF HISTORY OF NETWORK ANALYZERS :

Complex microwave communication and radar system requirements regularly call for components with very small deviation from flatness and linear phase across wide bandwidths. These specifications demanding high measurement accuracy were first satisfied by the Hewlett-Packard automatic network analyzer-HP8540, in 1967.

Vector network analyzers derive their origin from the extension of the concept of vector voltmeter, a two-channel RF millivoltmeter and phase meter, into higher frequencies. A chronological development of network measurements is given by S.F.Adam in Automatic Microwave Network Measurements [2]. The concept of vector voltmeters made possible broadband network analyzers, capable of measuring magnitude and phase of reflection and transmission coefficients on the

swept-frequency basis. In actuality, it provided a means of obtaining full small-signal scattering parameters of both active and passive devices. It was a two-channel system using frequency translation by sampling technique to retain magnitude and phase information at an IF frequency.

Hackborn [5] and Adam [1] described how this system was connected to a digital minicomputer to achieve vector error correction. Systematic errors associated with directivity frequency response, and source and load mismatch effects are largely eliminated by measuring a series of known devices or standards. From this data, vector coefficients that model the error effects are computed, and when an unknown device is connected to the system and measured, the computer quickly corrects vector data. This system could generate standard laboratory quality data at 50 frequencies for 20 devices in an hour. The accuracies reported by Adam [1] for reflection coefficient measurement for system without phase lock were

Magnitude uncertainty

$$\pm(0.003 + 0.015\rho + 0.01\rho^2) \tag{2.1}$$

and phase angle uncertainty

$$\pm\left[0.5^\circ + \tan^{-1}\frac{0.003}{\rho} + 4\tan^{-1}(0.015\rho)\right]. \tag{2.2}$$

For a system with phase lock the corresponding figures were,

Magnitude uncertainty

$$\pm(0.0015 + 0.005\rho + 0.003\rho^2) \tag{2.3}$$

and phase angle uncertainty

$$\pm\left[0.25^\circ + \tan^{-1}\frac{0.0015}{\rho} + 4\tan^{-1}(0.005\rho)\right]. \qquad (2.4)$$

where ρ is the magnitude of the reflection coefficient Γ_L.

Over the past 16-years, a continuous series of improvements have been made to this family of Automatic Network Analyzers. Phase locking the signal source to a synthesizer derived receiver local oscillator provided both frequency repeatability and accuracy eliminating receiver harmonic skip errors. New methods of improving the accuracy were described using closed-form solutions of Kasa [10] for calibration.

With the advent of programmable instrumentation calculators and the IEEE standard-488 type of interface bus system, new flexible automation of the measurement system became feasible.

A semi-automatic network analyzer system was described using the IEEE interface bus [7]. This system used a desktop calculator, and fully corrected errors in one-port reflection measurements. Later on, phase locked sources, and two-port error correction models were added to this system to provide flexibility in tailoring accuracy requirements and costs. This system covers the frequency band from very low frequencies of a few hertz to frequencies as high as 18 GHz, but the cost restrictions still inhibit its general purpose use.

2.2 ORGANIZATION OF THE PRESENT HP SYSTEM :

The automated network analyzer configuration provides program control of the source output frequency, test set switching, receiver tuning, IF gain, and conversion of data to produce fully error-corrected transmission and reflection measurements from 100 kHz to 110 MHz, using the HP8407A, and from 0.11 to 18 GHz, using the HP8410 network analyzer [6].

Figure 2 shows the basic system configuration. It consists of a source, various transducers (depending on the application), the Network Analyzer mainframe and an appropriate display. A desktop computer with HP-IB interface, HP-IB accessories and a computer program with all instrument control, computation, and operator interface modules are added to the system to automate the instruments and provide accuracy enhanced measurements.

The system operation can be easily understood by dividing it into four major sections : the signal source, the network analyzer, the computer [5] and the accuracy enhancement calculations.

2.2.1 Signal source section :

The signal source section consists of a sweep oscillator which can control different RF signal sources for the required frequency band. The sweep oscillator is interfaced to the desktop computer to allow for digital programming of the RF frequency. Automatic level control (ALC) is used to

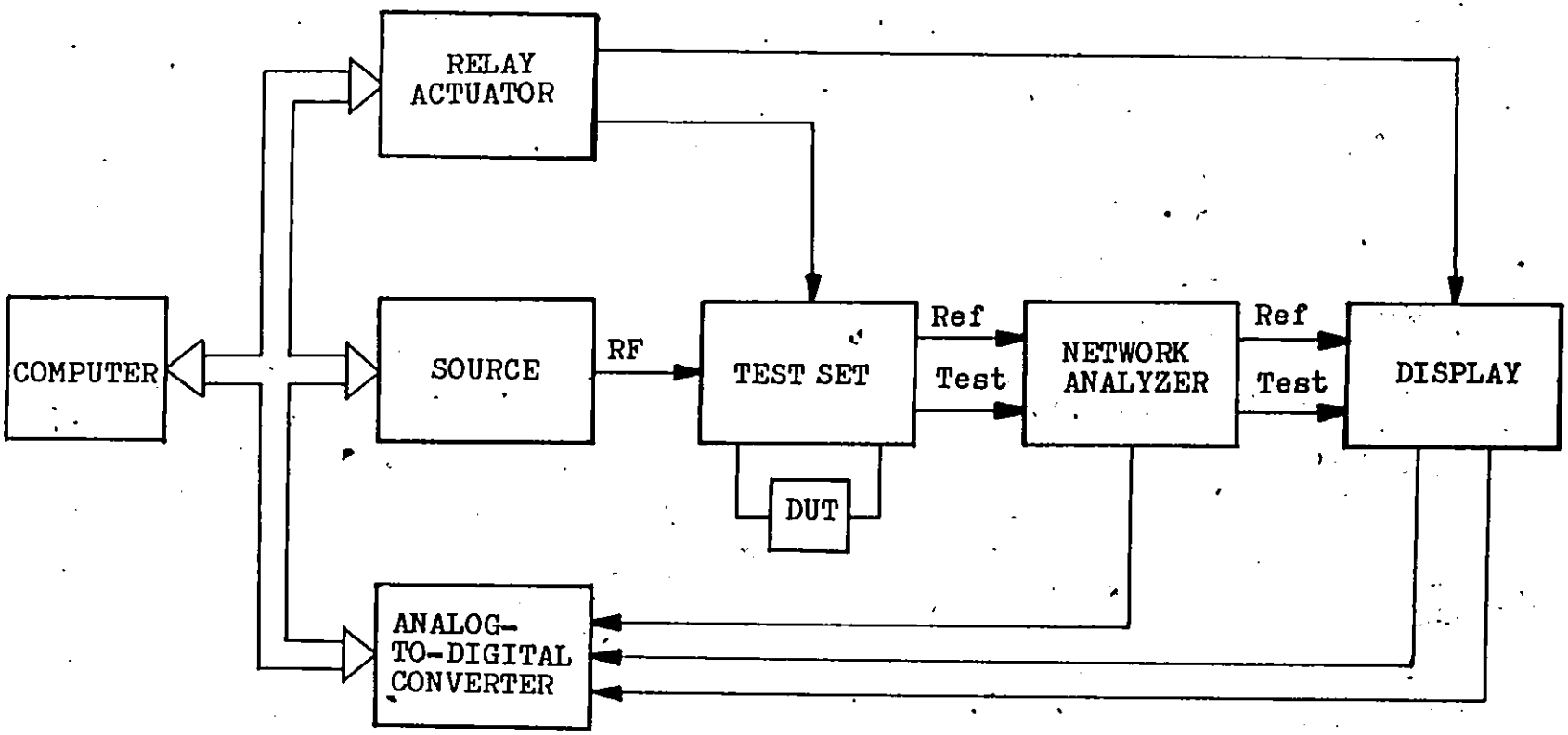


Figure 2: Basic single band automated network analyzer block diagram

insure a reasonably leveled input signal to the device being tested.

2.2.2 Network analyzer section :

The network analyzer section measures the s-parameters of the device being characterized. Any one of the four s-parameters representing a two-port device can be measured by switching the RF signals inside a two-port test unit. This switching is computer-controlled. The network analyzer portion of the subsystem is a ratio-meter. It requires both a test and a reference channel. The reference and test signals are each mixed in separate IF mixer circuits that are driven by a common local oscillator signal, which is held on frequency by phase locking the IF signal with a crystal oscillator. The reference signal is held constant within the ratio-meter and the test signal is compared to it. These signals then go to the display where both amplitude ratio and phase difference are measured. The network analyzer interface automatically programs the test channel IF gain to insure optimum signal to noise ratio. The magnitude and phase information from the displays are accurately digitized by A/D conversion for computer input.

2.2.3 Computer section :

The computer section consists mainly of a small desktop instrumentation computer with interface bus accessories. All the important functions of the instrument are controlled by the computer. It stores the system's own frequency dependent vector errors and corrects the raw measurement data for the device being tested. The corrected data are transformed into desired parameters for the device and displayed on a teletype.

The system has the provision of being removed from computer control and operated manually.

2.2.4 Accuracy enhancement calculations :

The vector accuracy enhancement program provides the means for reducing network analyzer measurement ambiguities. The measurement errors are of two types :

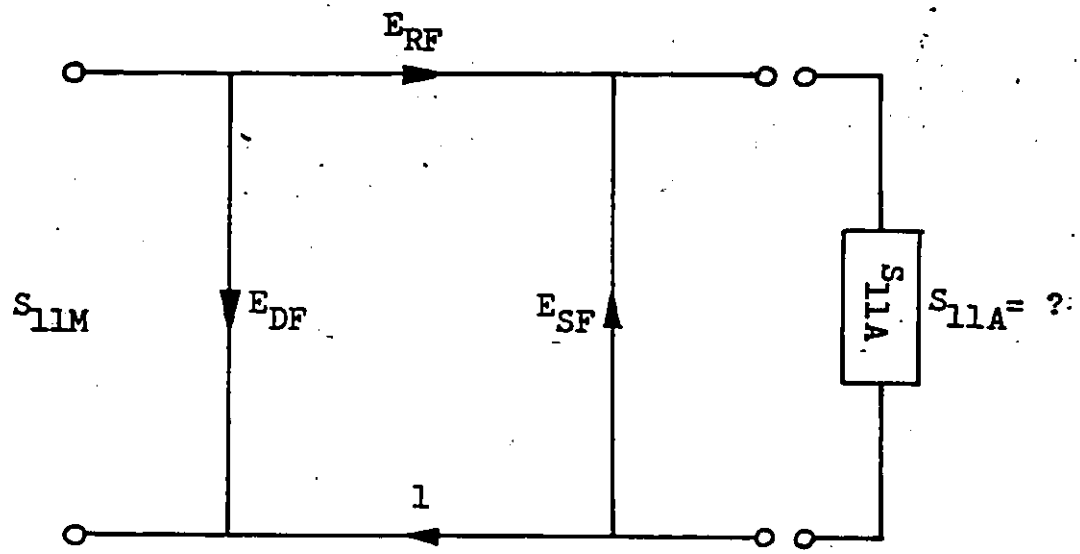
1. Random errors, which are non-repeatable measurement variations due to noise, temperature drift and other physical changes in the test setup between calibration and measurement, and
2. Systematic errors, which are repeatable errors that the system can measure.

The systematic uncertainties are quantified as directivity, source match, load match, isolation and tracking (frequency response).

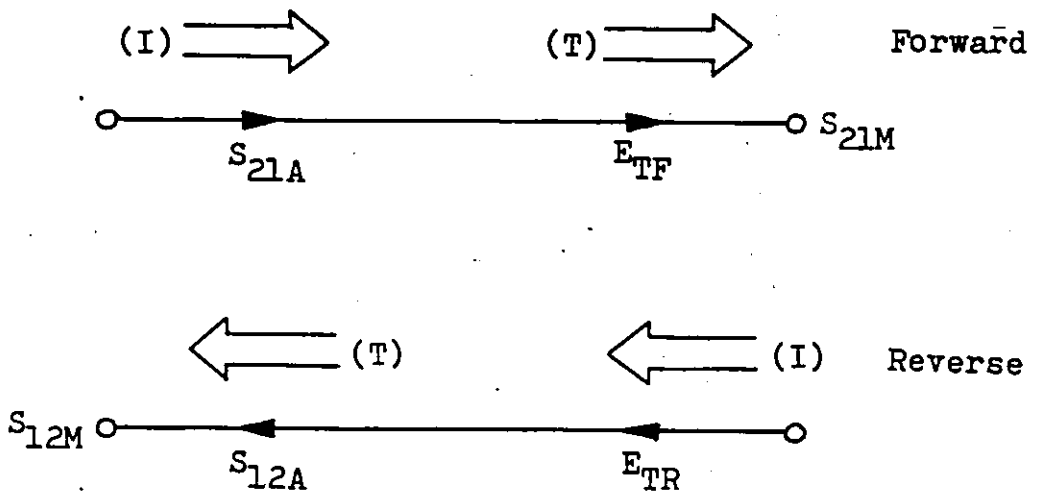
The program offers a choice between an eight- or a twelve-term error model. The eight-term error model provides directivity, source match and frequency response vector error correction for reflection measurements and simplified frequency only vector error correction for transmission measurements. This model is good for reflection measurements of one-port devices and fast transmission measurements on two-port devices where normalization of magnitude and phase frequency response errors give good measurement accuracy. The twelve-term error model provides full directivity, isolation, source match, load match and frequency response vector error correction for transmission and reflection measurements of two-port devices. It requires measurement of all four s-parameters of the two-port device.

The error model [7] for one-port error measurement can be given as in figure 3a. It assumes a perfect measuring port with all errors lumped into a two-port network using superposition theorem. In this system, the three errors, the Effective directivity E_{DF}, the Effective source match error E_{SF}, and the Reflection tracking error E_{RF}, are mathematically related to the actual, S_{11A}, and measured, S_{11M}, data by the following equation:

$$S_{11M} = E_{DF} + \frac{S_{11A} E_{RF}}{1 - E_{SF} S_{11A}} \qquad (2.5)$$



(a)



(b)

Figure 3: One-port error models

The three "E" errors are found by calibrating the system at the measurement plane at each frequency by using three independent standards, a "perfect load", a "short" and an "open circuit". The test device response is then measured and the actual device response is obtained by using the following equation :

$$S_{11A} = \frac{S_{11M} - E_{DF}}{E_{SF}(S_{11M} - E_{DF}) + E_{RF}} \qquad (2.6)$$

For transmission measurement error correction in case of the eight-term error model, the model used is as shown in figure 3b and the relationships for the actual response are:

$$S_{21A} = \frac{S_{21M}}{E_{TF}} \quad \text{and} \quad S_{12A} = \frac{S_{12M}}{E_{TR}} \qquad (2.7)$$

where S_{21M} and S_{12M} are the measured responses, E_{TF} is the forward transmission tracking term and E_{TR} is the reverse transmission tracking term.

The representative twelve-term error model for the forward and reverse case of a two-port device is shown in figure 4.

The errors denoted are as follows :

E_{DF} = Effective Directivity (forward)

E_{DR} = Effective Directivity (reverse)

E_{XF} = Isolation (forward)

E_{XR} = Isolation (reverse)

E_{SF} = Effective source match(forward)

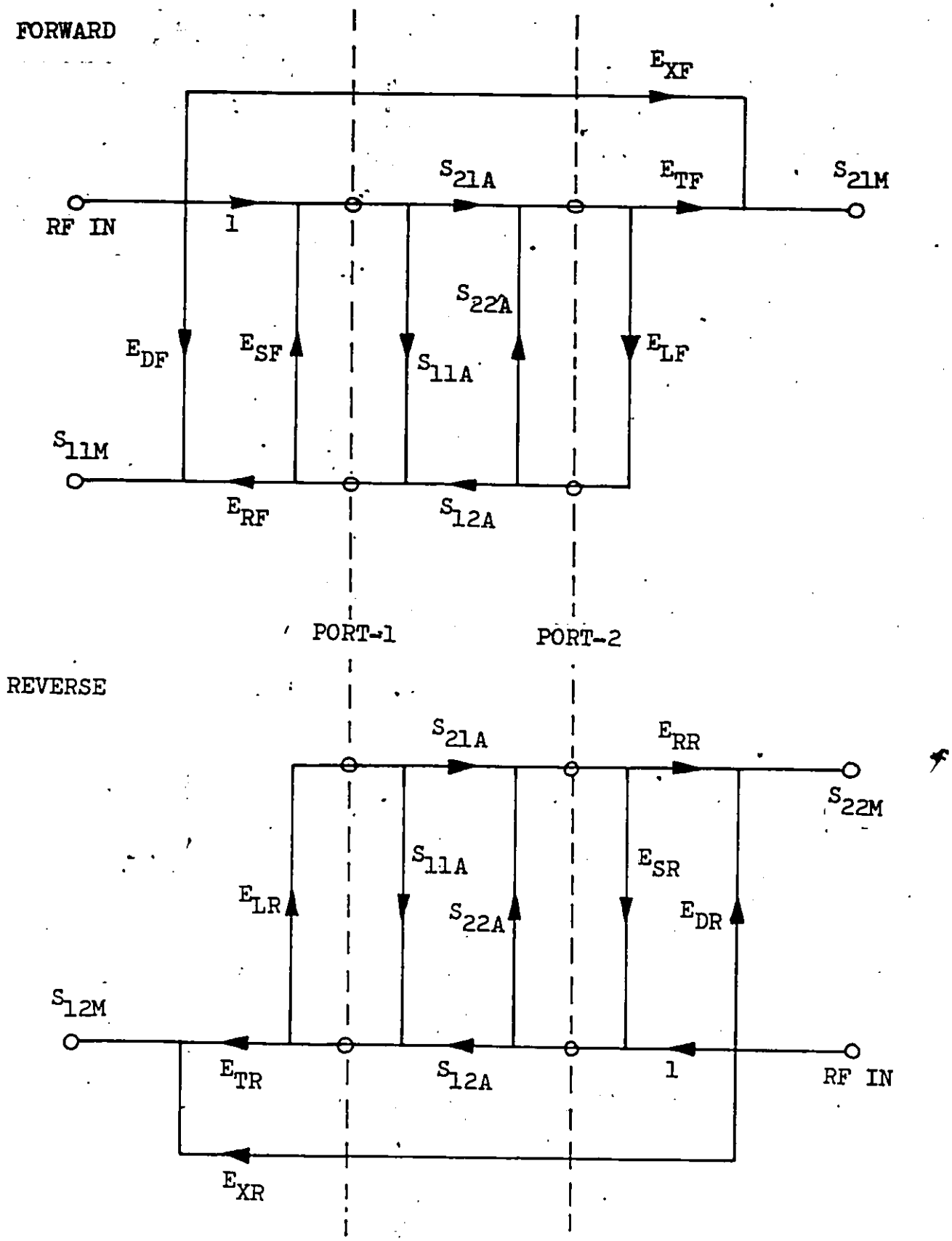


Figure 4: Two-port error models

$$S_{11A} = \frac{\left[\left(\frac{S_{11M}-E_{DF}}{E_{RF}}\right)\left[1+\left(\frac{S_{22M}-E_{DR}}{E_{RR}}\right)E_{SR}\right]\right]-\left[\left(\frac{S_{21M}-E_{XF}}{E_{TF}}\right)\left(\frac{S_{12M}-E_{XR}}{E_{TR}}\right)E_{LF}\right]}{\left[1+\left(\frac{S_{11M}-E_{DF}}{E_{RF}}\right)E_{SF}\right]\left[1+\left(\frac{S_{22M}-E_{DR}}{E_{RR}}\right)E_{SR}\right]-\left[\left(\frac{S_{21M}-E_{XF}}{E_{TF}}\right)\left(\frac{S_{12M}-E_{XR}}{E_{TR}}\right)E_{LF}E_{LR}\right]}$$

$$S_{21A} = \frac{\left[1+\left(\frac{S_{22M}-E_{DR}}{E_{RR}}\right)\left(E_{SR}-E_{LF}\right)\right]\left(\frac{S_{21M}-E_{XF}}{E_{TF}}\right)}{\left[1+\left(\frac{S_{11M}-E_{DF}}{E_{RF}}\right)E_{SF}\right]\left[1+\left(\frac{S_{22M}-E_{DR}}{E_{RR}}\right)E_{SR}\right]-\left[\left(\frac{S_{21M}-E_{XF}}{E_{TF}}\right)\left(\frac{S_{12M}-E_{XR}}{E_{TR}}\right)E_{LF}E_{LR}\right]}$$

$$S_{12A} = \frac{\left[1+\left(\frac{S_{11M}-E_{DF}}{E_{RF}}\right)\left(E_{SF}-E_{LR}\right)\right]\left(\frac{S_{12M}-E_{XR}}{E_{TR}}\right)}{\left[1+\left(\frac{S_{11M}-E_{DF}}{E_{RF}}\right)E_{SF}\right]\left[1+\left(\frac{S_{22M}-E_{DR}}{E_{RR}}\right)E_{SR}\right]-\left[\left(\frac{S_{21M}-E_{XF}}{E_{TF}}\right)\left(\frac{S_{12M}-E_{XR}}{E_{TR}}\right)E_{LF}E_{LR}\right]}$$

$$S_{22A} = \frac{\left[\left(\frac{S_{22M}-E_{DR}}{E_{RR}}\right)\left[1+\left(\frac{S_{11M}-E_{DF}}{E_{RF}}\right)E_{SF}\right]\right]-\left[\left(\frac{S_{21M}-E_{XF}}{E_{TF}}\right)\left(\frac{S_{12M}-E_{XR}}{E_{TR}}\right)E_{LR}\right]}{\left[1+\left(\frac{S_{11M}-E_{DF}}{E_{RF}}\right)E_{SF}\right]\left[1+\left(\frac{S_{22M}-E_{DR}}{E_{RR}}\right)E_{SR}\right]-\left[\left(\frac{S_{21M}-E_{XF}}{E_{TF}}\right)\left(\frac{S_{12M}-E_{XR}}{E_{TR}}\right)E_{LF}E_{LR}\right]}$$

Figure 5: S-parameter relations for models of fig.4

E_{SR} = Effective source match(reverse)

E_{TF} = Transmission tracking (forward)

E_{TR} = Transmission tracking (reverse)

E_{RF} = Reflection tracking (forward)

E_{RR} = Reflection tracking (reverse)

E_{LF} = Effective load match(forward)

E_{LR} = Effective load match(reverse)

In the figure, the S-terms with subscript "M" denote measured response and those with subscript "A" are actual parameters, which can be obtained from the equations shown in figure 5.

The overall accuracy of the system discussed above is given by Adam [1] as in section 2.1. The maximum uncertainty specified in the operation manual for the system is ± 0.05 dB for magnitude and ± 1° for phase measurements.

Chapter III

THEORETICAL BASIS FOR DIGITAL NETWORK ANALYSIS

Standard vector network analyzers use analog circuitry for their source section and network analyzer section. This chapter presents the basic principle to implement these sections using digital techniques. It also describes the principle of integrating the digital parts into a complete digital network analyzer system.

3.1 SIGNAL GENERATION TECHNIQUE :

Conventional frequency synthesizers use a single frequency to produce a large set of new frequencies. This is commonly achieved with analog circuits, or combinations of analog and digital circuits.

In a digital frequency synthesizer [13], a single frequency is used to establish a stable sampling time at which sample values are computed or fetched from a look-up table.

A sine wave signal sampled at constant intervals is given by

$$\sin(2\pi f_s nT + \theta) \qquad (3.1)$$

where T is the sampling interval, n is the index number of sample, f_s is the frequency of the sine wave generated, and

θ is an arbitrary phase. Furthermore, $f_s = kf_0$, where f_0 = lowest computed frequency. As a result, one can obtain only the multiples of the lowest frequency f_0.

Looking at the implementation aspects of the synthesizer it becomes clear that since the argument of the sine wave is an arithmetic series of the type $na + b$, an accumulator with a modulus of 2π can be used [11] to generate such a series. Alternatively, a counter running at multiples of the lowest sampling frequency can produce stored sine values to the digital-to-analog converter at a required speed. These sine-wave samples are used to drive the D/A converter of proper word length to produce analog samples. The output samples from the converter when interpolated by a smoothing filter give the sine wave at the required frequency.

The above algorithm introduces some distortion of the signal. In addition to the desired signal of fundamental frequency f_s, other components produced are as follows (figure 6) :

1. Harmonics : These components are generated due to the use of a waveform table with finite resolution and
2. Sampling components : These components appear at $nf_c \pm f_s$ (f_c = sampling frequency, n= an integer) for an ideal square step D/A converter.

The distortion due to sampling component can be reduced by a low pass filter with the characteristics as shown in figure 7.

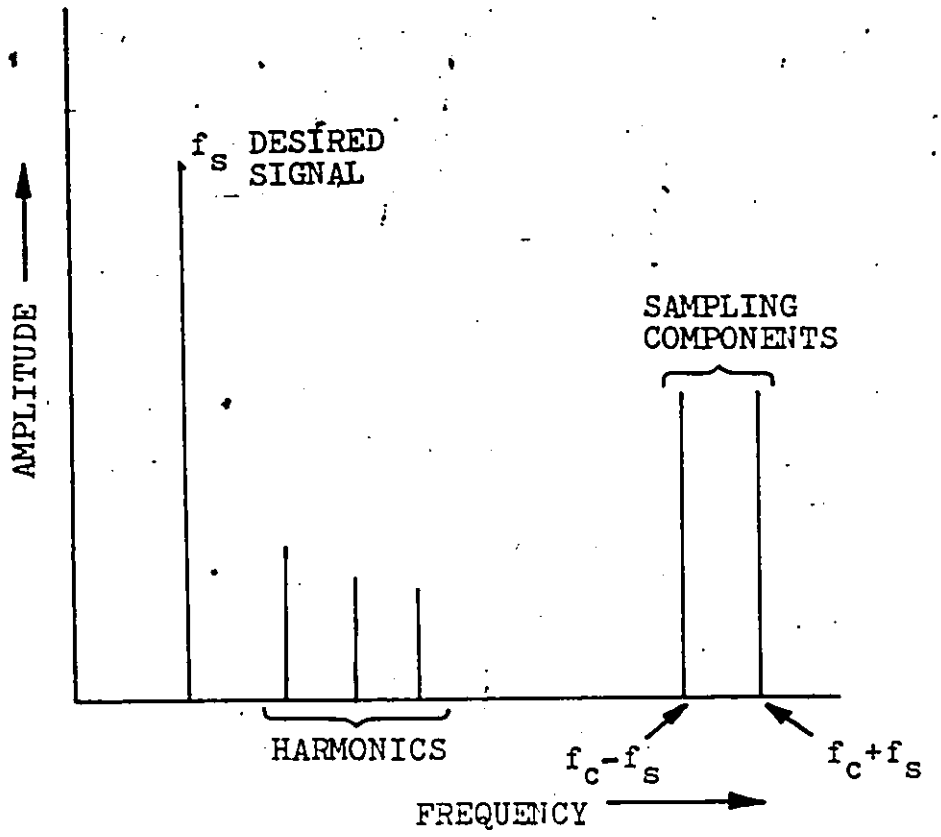


Figure 6: Frequency spectrum of digital synthesizer output

3.2 AMPLITUDE AND PHASE MEASUREMENT TECHNIQUES :

Traditional measurement methods for amplitude ratio of a.c. waveforms usually rely on some square-law device used as the detector.

In digital phase meters used for measuring phase differences, the two signals are converted to rectangular pulse trains. These pulse trains are then compared, using NOR gates and bistable multivibrators, to give a pulse-width-dependent signal proportional to the phase difference between the two signals. This pulse width is then measured to obtain the phase difference. The accuracy is of the order of ± 0.5°.

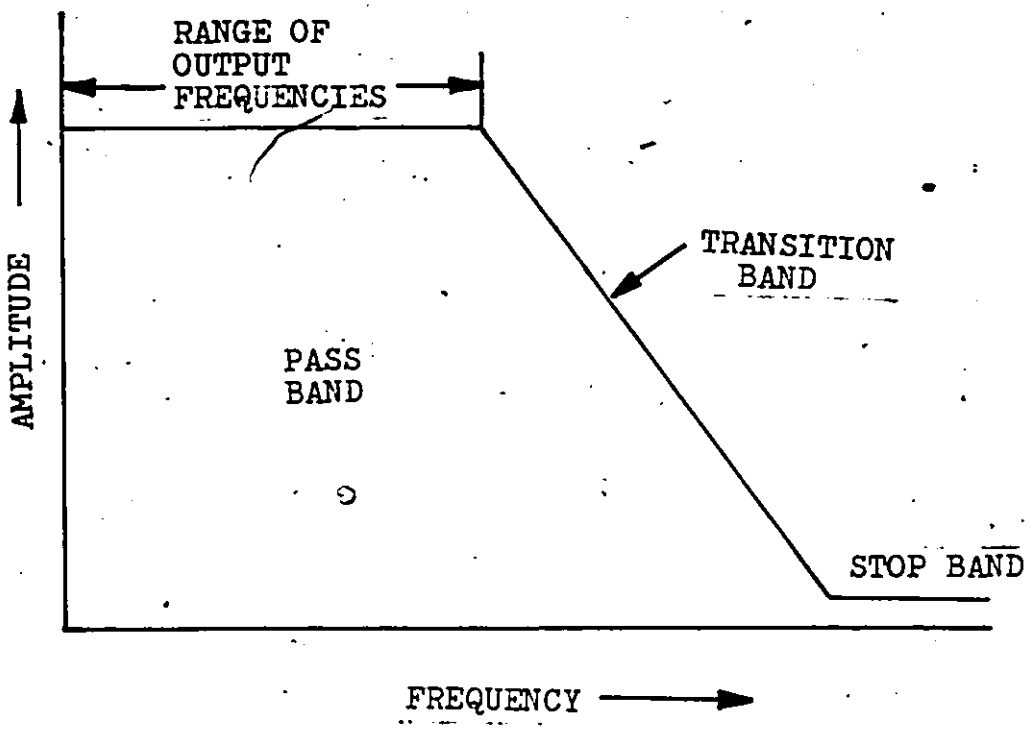


Figure 7: Low-pass filter characteristics

A sampling voltmeter was developed at NBS [4], which uses discrete Fourier transform techniques to provide an accuracy of ± 0.1%. But because of the high sampling frequency required, the maximum frequency was limited to 120 Hz.

The network analyzers use high quality sinusoidal signals as the reference signal and the test device affects only the amplitude and phase without changing the sinusoidal nature of the signal. The method selected in this work determines the amplitude ratio and phase difference by periodically sampling the reference and test waveforms and calculating the result from digitized values of measured instantaneous reference and test voltages by sine curve fitting [12].

Assuming that the signal used is a perfect sinusoid of a known frequency, "n" is the sample number and X_n is the nth sample value, the resulting signal is represented by

$$X_n = \alpha \cos(\beta n T_s + \gamma) \tag{3.2}$$

where T_s is the sampling interval. The estimate of the above signal is given by

$$\hat{X}_n = c \cos(\frac{2\pi}{T} n T_s + \delta) \tag{3.3}$$

where T is the period of cosine function. Alternatively,

$$\hat{X}_n = \alpha \cos\frac{2\pi}{T} n T_s + \beta \sin\frac{2\pi}{T} n T_s \tag{3.4}$$

where $\alpha = c \cos\delta$ and $\beta = -c \sin\delta$ (3.5)

also $c = \sqrt{(\alpha^2 + \beta^2)}$ and $\delta = \tan^{-1}(-\beta/\alpha)$ (3.6)

Using these relations α and β are determined by least squares curve fitting.

Assuming that "N" spans over integral number of cycles,

$$\alpha = \frac{\sum_{1}^{N} X_n \cos\frac{2\pi}{T} n T_s}{\sum_{1}^{N} \cos^2\frac{2\pi}{T} n T_s} \quad \text{and} \quad \beta = \frac{\sum_{1}^{N} X_n \sin\frac{2\pi}{T} n T_s}{\sum_{1}^{N} \sin^2\frac{2\pi}{T} n T_s} \tag{3.7}$$

Hence, the amplitude of the sampled sine wave is,

$$c = \sqrt{(\alpha^2 + \beta^2)} \tag{3.8}$$

and the phase of the sine signal is

$$\delta = \tan^{-1}(-\beta/\alpha) \tag{3.9}$$

Consequently, for $c_{ref.}$ and $\delta_{ref.}$ as the amplitude and phase of reference signal respectively and c_{test} and δ_{test} as those of test signal, the

$$\text{Amplitude ratio} = c_{test}/c_{ref.} \qquad (3.10)$$

$$\text{and} \quad \text{Phase difference} = \delta_{test} - \delta_{ref.} \qquad (3.11)$$

3.3 BASIC PRINCIPLES OF OPERATION :

This section contains explanations of the operation of the all-digital network analyzer system. Figure 8 is a simplified block diagram showing principal system sections and their interconnections.

As illustrated in figure 8, a digital network analyzer system consists of a frequency synthesizer, a low pass filter, a power splitter, the detector interface and a computer for data processing and system control. The synthesizer, and the detector interface are controlled by a microcomputer, which interfaces with the main computer.

During the measurement cycle, the operator interfaces with the minicomputer through a CRT terminal and specifies the measurement frequency. The minicomputer passes this information in appropriate form to the microprocessor which sets the synthesizer to generate the signal of required frequency. This digitally generated signal is filtered to remove the harmonic content and other distortions, and is

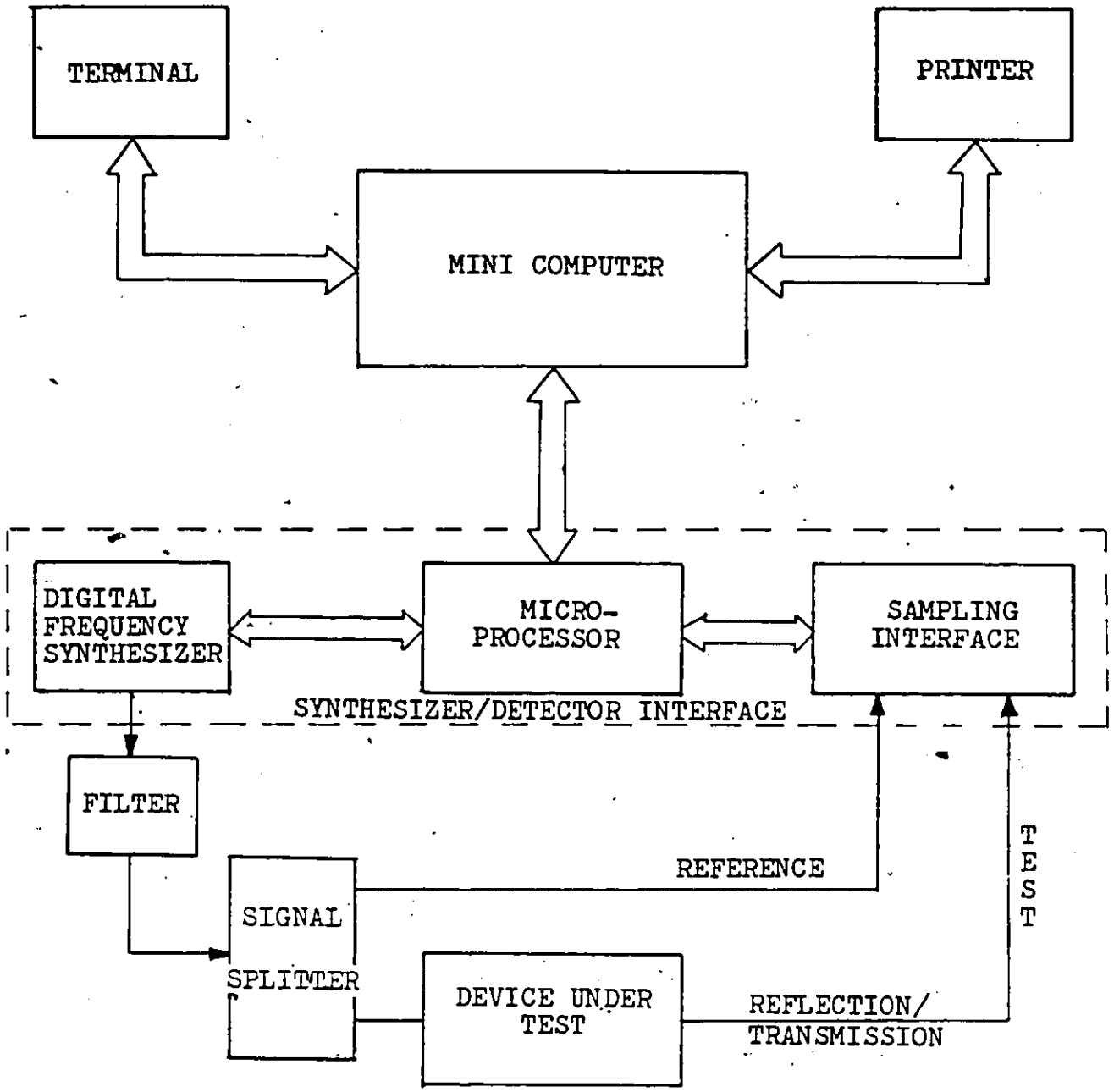


Figure 8: Simplified block diagram of digital network analyzer system

split by a power splitter to provide reference and test signals of equal amplitudes and phases.

The minicomputer instructs the operator to connect the device to the test channel, and the device output to the test input of the detector interface. The reference channel is connected to the reference input of the detector. Depending on the measurement frequency, the minicomputer calculates the required number of samples and the interval between the samples, and instructs the microcomputer to obtain these samples. The microprocessor under software control, activates the digitizer circuits to complete the required task of sampling and analog-to-digital conversion. These signal samples are then transferred to the minicomputer.

The fitting of sine curves, to the two sets of samples, is done by the minicomputer to obtain the relative amplitude and phase for the reference and test signals.

The above measurement cycle is repeated for each case of calibration with standard connections and then for the measurement with the unknown device. The amplitude ratio and the phase difference obtained with the standard connections provide the error terms similar to those in analog systems (section 2.2.4 for accuracy enhancement). These error terms together with the measurements on unknown device are used in the equations 2.5,2.6,2.7 and those in figure 5 to calculate the actual characteristics of the

unknown device. This data processing is done by the minicomputer and the final results are printed on a line printer.

The problem in detecting the signal amplitude and phase is twofold. The number of samples of the reference and test signals must be chosen so that the value of actual amplitude and phase can be approached within a given tolerance. Furthermore, the measurement must be made with sufficient accuracy in a given time interval.

According to the Nyquist sampling theorem, in order to reconstruct a waveform from sampled data, the minimum sampling rate must be at least twice the frequency of the highest sinusoidal frequency component contained in the signal. However, the conditions encountered in practice differ from the ideal case assumed for theoretical derivations, and therefore, the minimum sampling rate is seldom sufficient in actual cases.

Another problem with the digital detection is that as the input signal to the analog-to-digital converter goes down in amplitude, the effect of quantization errors increases because of the fixed number of bits. This will put a limit on the amplitude ratio measurable with sufficient accuracy by using this type of system.

Chapter IV

SIMULATION OF THE PROPOSED SYSTEM

In outlining the proposed technique for digital network analysis in chapter three, a number of assumptions were made regarding the nature of the measurement process. Most of these assumptions were based on purely theoretical considerations. In an actual system, disturbances due to noise, sampling time fluctuations, round-off errors due to the finite number of digits, harmonic content of the signal, etc., contribute to the overall error.

The purpose of the simulation is the determination of the maximum uncertainty of the measurement process. Simulation serves as a very useful tool in the development of new systems, and provides means by which various design concepts can be used to evaluate the performance of a given system prior to its implementation. Simulation provides information not only about the system's potential, but also about its limitations.

4.1 MATHEMATICAL MODELS :

Simulation involves a selection of a mathematical model [14,15] of the experimental system. This model is then used for calculation of the difference between the relative amplitude and phase, representing the analog inputs, and the response of the sampled-data system under various conditions effecting the system. In the present work, the system simulation was used to specify the system parameters, such as sampling frequency and analog-to-digital converter resolution, for its hardware implementation.

4.1.1 Signal generation :

For the purpose of simulation, the reference and the test signals at the input of the measurement system are represented respectively by

$$Y_1 = \sin(X_t) + A_{12}\sin(2X_t + \theta_{12}) + A_{13}\sin(3X_t + \theta_{13}) + A_{14}\sin(4X_t + \theta_{14}) \quad (4.1)$$

and

$$Y_2 = \frac{1}{R}\left[\sin(X_t + \theta_{21}) + A_{22}\sin(2X_t + \theta_{22}) + A_{23}\sin(3X_t + \theta_{23}) + A_{24}\sin(4X_t + \theta_{24})\right] \quad (4.2)$$

The amplitudes A_{1j}'s of the 2nd, 3rd, and 4th harmonics and their respective phase angles, θ_{1j}'s are assigned during the execution of the program from input data. Also, the value of R, used as amplitude ratio between the reference(Y_1), and the test(Y_2) signal is specified from input data.

4.1.2 Sample and hold circuit :

The sampling time X_t in eqn.4.1 and eqn.4.2 is expressed as a fraction of 2π depending on the number of samples, N, to be taken per cycle. So, X_t is calculated as

$$X_t = \frac{2\pi}{N} n \ , \quad (\ n = 1,2,\ldots\ldots N \ ). \qquad (4.3)$$

In any sample-and-hold circuit, the circuit switching for the sampling function takes certain amount of time which is randomly variable. To simulate these fluctuations occuring in real time systems, a "timing error" is added to each sampling time X_t. The values of these fluctuations, for each sample, are obtained by using normalized random numbers (ranging from -1 to +1) multiplied by the suitable weighting parameter specified in the program.

4.1.3 Pseudo-random noise generator :

Simulation of the AM noise is a very important part of the simulation of any measurement system. In the real experimental system it is sampled by the analog-to-digital converters along with the original signals.

For the purpose of simulation, the noise component is considered as Gaussian. It is simulated using the pseudo-random number generator providing numbers between 0 and 1.

From the Central Limit Theorem [12], the probability density function ($f_z(x)$) of the sum of a set of random variables $x_1, \ldots, x_n, \ldots$ with respective densities $f_i(x)$

tends to a normal curve for large n, regardless of the shape of $f_i(x)$. Thus, for the continuous type random variable x_i with

$$E\{x_i\} = \eta_i \qquad \sigma_{x_i}^2 = \sigma_i^2 \tag{4.4}$$

If $x = x_1 + \cdots + x_n$ (4.5)

its mean and variance are,

$$\eta = \eta_1 + \cdots + \eta_n \tag{4.6}$$

$$\sigma^2 = \sigma_1^2 + \cdots + \sigma_n^2 \tag{4.7}$$

and its density is

$$f(x) = f_1(x) * f_2(x) * \cdots * f_n(x) \tag{4.8}$$

Then,

$$f(x) \sim \frac{1}{\sigma\sqrt{2\pi}} e^{-(x-\eta)^2/2\sigma^2} \tag{4.9}$$

If x is properly scaled by $1/\sqrt{n}$ (to make the limit of resulting variance finite), then the inequality in (4.9) becomes an equality for $n \to \infty$ provided

(a) $$\sigma_1^2 + \cdots + \sigma_n^2 \to \infty \tag{4.10}$$

(b) For some $\alpha > 2$

$$\int_{-\infty}^{\infty} x^\alpha f_i(x)\, dx < C = \text{constant} \tag{4.11}$$

i.e. if $\sigma_i > C_1 > 0$,

and if all densities $f_i(x)$ are zero for $|x| > C_2$.

The resulting random variable "x" has a Gaussian density function. This value of "x" is scaled appropriately using input data and is included as the Gaussian noise in the calculation of the instantaneous amplitude Y.

4.1.4 Analog-to-Digital converter :

Each Y value sampled with a timing error and containing a noise term represents the analog reference and test voltages applied to the A/D converter. The converter, however, has a finite resolution of B bits (plus 1 sign bit). The value of B is specified during program execution. The remainder of the calculations are therefore carried out in the integer mode by multiplying Y_i by 2^B with appropriate rounding off by $\frac{1}{2}$ bit. Since, the subsequent calculations are done by a minicomputer, as shown in figure 8, it is not necessary to limit the number of bits during the processing of samples (section 3.2). But, if special hardware is to be used, the number of bits retained in each subsequent step of calculation should closely parallel the real time calculations in the actual system following the A/D conversion.

In the simulation program, the final results are then compared to the actual parameters obtained from input data.

The program has provisions for specifying the following parameters :

1. Frequency of the measurement (in Hertz)

2. Sampling interval (in microseconds) and the number of samples per cycle
3. Signal to noise ratio
4. Timing error (in picoseconds)
5. A/D converter resolution (in bits)
6. Amplitude ratio between the reference and the test voltages.

Figure 9 gives the flow diagram for the simulation program for both,data acquisition and data processing, phases.

4.2 RESULTS OF SIMULATION :

The performance of the hypothetical system for network analysis is shown in the computer printouts in Tables3-7. In these calculations, a basic set of parameters was chosen to correspond to the minimum requirements (initial conditions). These conditions are listed in Table2. The requirements were then upgraded till an acceptable "maximum error" is achieved for relative amplitude and phase measurements. For all the calculations, the phase difference between reference and test signals was varied from 0° to 360° to take into account all possible conditions since the two signals are asynchronous in the real system.

The first set of data in Table3 shows the variation with the sampling rate. In each case the signals are sampled for one period. The next two sets in this table show the same

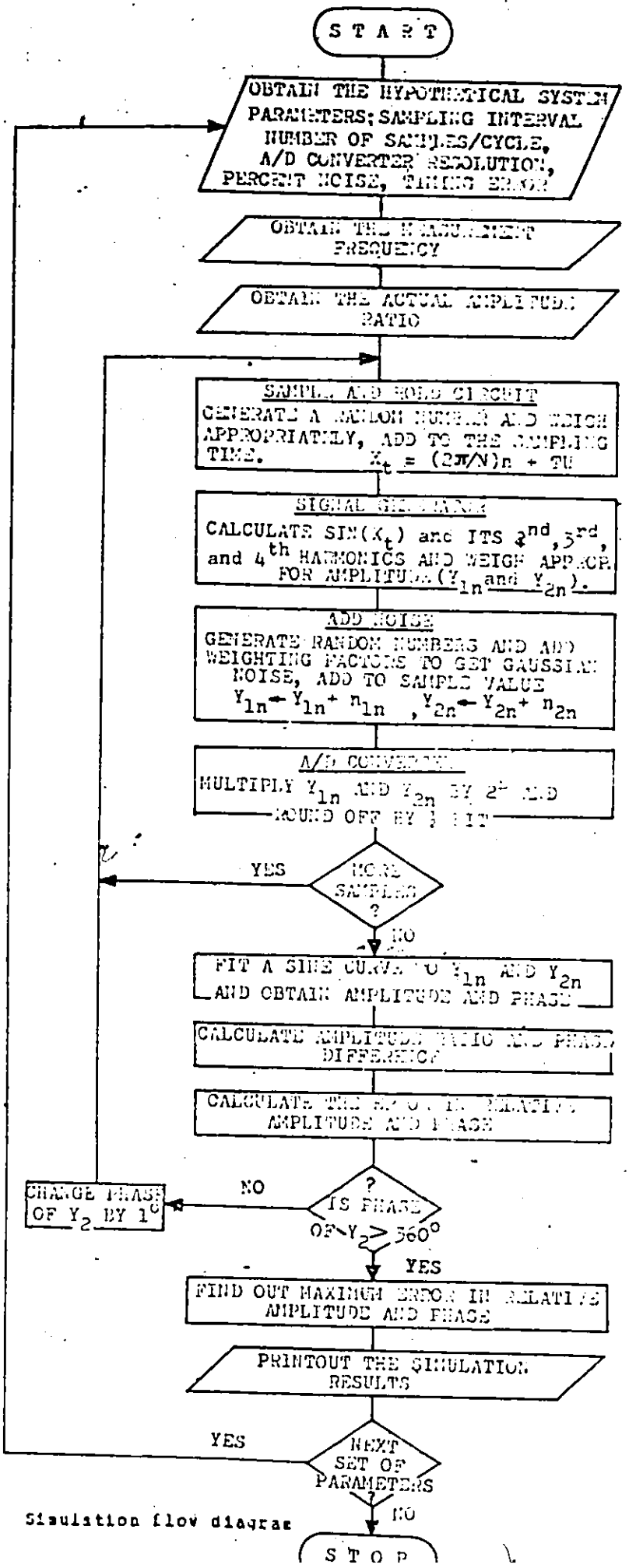


Figure 9: Simulation flow diagram

TABLE 2

Initial Conditions

Phase difference between reference and test signals	0°-360°
2nd, 3rd and 4th harmonic content	1.0%
Noise	0.0%
Timing error	0 ps
Frequency	20000 kHz
A/D converter resolution	8 bits
Relative amplitude	20 dB

variation with the A/D converter -bit resolution increased to 10 and 12 bits. The results show an appreciable decrease of the error in amplitude ratios and phase differences.

In the next three sets of results in Table4, the A/D converter resolution is further increased to 14, 16 and 18 bits. These calculations show the possibility of a very accurate system achievable with digital signal processing.

From the above six sets of data in Table3 and 4, the conditions for a typical system were chosen as 12 bits of A/D converter resolution and sampling rate of 10 times or 20 times signal frequency. The basis for this selection takes into account the maximum advantage available in

1. accuracy of measurement and
2. the implementation in hardware.

The second series of tests studied the effects of timing error and noise. The converter resolution and the sampling

rate imposes a limit on the measurement frequency. These limits were obtained for the amplitude ratio and phase difference measurement within acceptable error of ±0.015 dB and ±0.1°, respectively.

The two sections in Table5 show that the errors are relatively insensitive to random timing errors (in the sampling time). The system was studied for the errors of upto 500 ps, though the actual fluctuations for available sample and hold circuits are of the order of 20 ps only.

In Table6, the influence of noise in the input signal is demonstrated. For a noise content of 0.01% or less, only 10 samples per period are required. If the sampling rate is 20 times the signal frequency, noise content of upto 0.05% can be tolerated. If the number of signal periods sampled is increased from 1 to 16 with 10 samples per period, even 0.1% of noise in input signals produces valid results.

The last table (Table7) of simulation results show that if the sampling frequency is 200 kHz, the A/D converter resolution is 12 bits, maximum timing error is 50 ps and maximum noise content is 0.05%, the amplitude ratio limitation is 20 dB and the measurements can be made upto a frequency of 24 kHz with uncertainties of ±0.015 dB and ±0.1° in amplitude and phase, respectively.

TABLE 3

Simulation Results : Sampling rate effects

3ITAL NETWORK ANALYSIS

EQUENCY (HZ)	NO.OF POINTS	SAMPLING INTERVAL (MICROS)	ACTUAL MAG (DB)	ACTUAL PHASE (DEG)	MAX. ERROR MAG (DB)	MAX. ERROR PHASE (DEG)	PRCNT NOISE (%)	TIMING ERROR (PICOS)	NO.OF BITS
20000.	4	12.500	20.000	0.- 360.	0.4326	2.6598	0.000	0.	8.
20000.	8	6.250	20.000	0.- 360.	0.2734	2.0000	0.000	0.	8.
20000.	10	5.000	20.000	0.- 360.	0.2442	1.7279	0.000	0.	8.
20000.	12	4.166	20.000	0.- 360.	0.2385	1.3611	0.000	0.	8.
20000.	16	3.125	20.000	0.- 360.	0.2230	1.3000	0.000	0.	8.
20000.	20	2.500	20.000	0.- 360.	0.1650	1.1634	0.000	0.	8.
20000.	25	2.000	20.000	0.- 360.	0.1563	0.9594	0.000	0.	8.
20000.	30	1.666	20.000	0.- 360.	0.1195	0.8205	0.000	0.	8.
20000.	40	1.250	20.000	0.- 360.	0.1018	0.7789	0.000	0.	8.
20000.	50	1.000	20.000	0.- 360.	0.0963	0.3194	0.000	0.	8.
20000.	4	12.500	20.000	0.- 360.	0.0911	0.6598	0.000	0.	10.
20000.	8	6.250	20.000	0.- 360.	0.0528	0.4748	0.000	0.	10.
20000.	10	5.000	20.000	0.- 360.	0.0537	0.4464	0.000	0.	10.
20000.	12	4.166	20.000	0.- 360.	0.0520	0.4384	0.000	0.	10.
20000.	16	3.125	20.000	0.- 360.	0.0455	0.4201	0.000	0.	10.
20000.	20	2.500	20.000	0.- 360.	0.0354	0.2979	0.000	0.	10.
20000.	25	2.000	20.000	0.- 360.	0.0247	0.2340	0.000	0.	10.
20000.	30	1.666	20.000	0.- 360.	0.0230	0.2271	0.000	0.	10.
20000.	40	1.250	20.000	0.- 360.	0.0130	0.1753	0.000	0.	10.
20000.	50	1.000	20.000	0.- 360.	0.0117	0.1340	0.000	0.	10.
20000.	4	12.500	20.000	0.- 360.	0.0229	0.1801	0.000	0.	12.
20000.	8	6.250	20.000	0.- 360.	0.0204	0.1420	0.000	0.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	0.	12.
20000.	12	4.166	20.000	0.- 360.	0.0120	0.0821	0.000	0.	12.
20000.	16	3.125	20.000	0.- 360.	0.0114	0.0789	0.000	0.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	0.	12.
20000.	25	2.000	20.000	0.- 360.	0.0072	0.0290	0.000	0.	12.
20000.	30	1.666	20.000	0.- 360.	0.0070	0.0252	0.000	0.	12.
20000.	40	1.250	20.000	0.- 360.	0.0066	0.0233	0.000	0.	12.
20000.	50	1.000	20.000	0.- 360.	0.0062	0.0220	0.000	0.	12.

TABLE 4

Simulation Results : A/D converter resolution effects

GITAL NETWORK ANALYSIS

EQUENCY (HZ)	NO. OF POINTS	SAMPLING INTERVAL (MICROS)	ACTUAL MAG (DB)	ACTUAL PHASE (DEG)	MAX. ERROR MAG (DB)	MAX. ERROR PHASE (DEG)	PRCNT NOISE (%)	TIMING ERROR (PICOS)	NO.OF BITS
20000.	4	12.500	20.000	0.- 360.	0.0076	0.0410	0.000	0.	14.
20000.	8	6.250	20.000	0.- 360.	0.0051	0.0258	0.000	0.	14.
20000.	10	5.000	20.000	0.- 360.	0.0048	0.0229	0.000	0.	14.
20000.	12	4.166	20.000	0.- 360.	0.0042	0.0213	0.000	0.	14.
20000.	16	3.125	20.000	0.- 360.	0.0034	0.0212	0.000	0.	14.
20000.	20	2.500	20.000	0.- 360.	0.0031	0.0143	0.000	0.	14.
20000.	25	2.000	20.000	0.- 360.	0.0026	0.0130	0.000	0.	14.
20000.	30	1.666	20.000	0.- 360.	0.0026	0.0128	0.000	0.	14.
20000.	40	1.250	20.000	0.- 360.	0.0012	0.0102	0.000	0.	14.
20000.	50	1.000	20.000	0.- 360.	0.0012	0.0103	0.000	0.	14.
20000.	4	12.500	20.000	0.- 360.	0.0016	0.0093	0.000	0.	16.
20000.	8	6.250	20.000	0.- 360.	0.0011	0.0083	0.000	0.	16.
20000.	10	5.000	20.000	0.- 360.	0.0011	0.0070	0.000	0.	16.
20000.	12	4.166	20.000	0.- 360.	0.0012	0.0075	0.000	0.	16.
20000.	16	3.125	20.000	0.- 360.	0.0008	0.0057	0.000	0.	16.
20000.	20	2.500	20.000	0.- 360.	0.0006	0.0057	0.000	0.	16.
20000.	25	2.000	20.000	0.- 360.	0.0006	0.0055	0.000	0.	16.
20000.	30	1.666	20.000	0.- 360.	0.0005	0.0055	0.000	0.	16.
20000.	40	1.250	20.000	0.- 360.	0.0005	0.0054	0.000	0.	16.
20000.	50	1.000	20.000	0.- 360.	0.0006	0.0034	0.000	0.	16.
20000.	4	12.500	20.000	0.- 360.	0.0005	0.0025	0.000	0.	18.
20000.	8	6.250	20.000	0.- 360.	0.0004	0.0022	0.000	0.	18.
20000.	10	5.000	20.000	0.- 360.	0.0003	0.0017	0.000	0.	18.
20000.	12	4.166	20.000	0.- 360.	0.0003	0.0015	0.000	0.	18.
20000.	16	3.125	20.000	0.- 360.	0.0003	0.0015	0.000	0.	18.
20000.	20	2.500	20.000	0.- 360.	0.0002	0.0011	0.000	0.	18.
20000.	25	2.000	20.000	0.- 360.	0.0002	0.0011	0.000	0.	18.
20000.	30	1.666	20.000	0.- 360.	0.0002	0.0010	0.000	0.	18.
20000.	40	1.250	20.000	0.- 360.	0.0001	0.0010	0.000	0.	18.
20000.	50	1.000	20.000	0.- 360.	0.0002	0.0008	0.000	0.	18.

TABLE 5

Simulation Results : Timing error effects

:GITAL NETWORK ANALYSIS

:EQUENCY (HZ)	NO.OF POINTS	SAMPLING INTERVAL (MICROS)	ACTUAL MAG (DB)	ACTUAL PHASE (DEG)	MAX. ERROR MAG (DB)	MAX. ERROR PHASE (DEG)	PRCNT NOISE (%)	TIMING ERROR (PICOS)	NO.OF BITS
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	10.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	20.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	30.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	40.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	75.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	100.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	150.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	200.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	250.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	300.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.000	350.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0916	0.000	400.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0916	0.000	450.	12.
20000.	10	5.000	20.000	0.- 360.	0.0145	0.0916	0.000	500.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	10.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	20.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	30.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	40.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	75.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	100.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.000	150.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0591	0.000	200.	12.
20000.	20	2.500	20.000	0.- 360.	0.0108	0.0726	0.000	250.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0703	0.000	300.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0625	0.000	350.	12.
20000.	20	2.500	20.000	0.- 360.	0.0106	0.0652	0.000	400.	12.
20000.	20	2.500	20.000	0.- 360.	0.0106	0.0624	0.000	450.	12.
20000.	20	2.500	20.000	0.- 360.	0.0106	0.0624	0.000	500.	12.

TABLE 6

Simulation Results : Random - noise effects

IGITAL NETWORK ANALYSIS

REQUENCY (HZ)	NO.OF POINTS	SAMPLING INTERVAL (MICROS)	ACTUAL MAG (DB)	ACTUAL PHASE (DEG)	MAX. ERROR MAG (DB)	MAX. ERROR PHASE (DEG)	PRCNT NOISE (%)	TIMING ERROR (PICOS)	NO.OF BITS
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.001	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.0144	0.0860	0.005	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.0178	0.1254	0.010	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.0370	0.2451	0.050	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.0778	0.3741	0.100	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.2141	1.1332	0.300	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.3618	1.9189	0.500	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.7688	3.8563	1.000	50.	12.
20000.	10	5.000	20.000	0.- 360.	5.4850	11.8813	5.000	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.0105	0.0495	0.001	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.0142	0.0766	0.005	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.0147	0.0766	0.010	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.0189	0.1825	0.050	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.0414	0.2883	0.100	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.1219	0.9707	0.300	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.2102	1.5935	0.500	50.	12.
20000.	20	2.500	20.000	0.- 360.	0.4453	3.2563	1.000	50.	12.
20000.	20	2.500	20.000	0.- 360.	2.7188	11.1907	5.000	50.	12.
20000.	20	5.000	20.000	0.- 360.	0.0689	0.2306	0.100	50.	12.
20000.	40	5.000	20.000	0.- 360.	0.0375	0.2269	0.100	50.	12.
20000.	60	5.000	20.000	0.- 360.	0.0338	0.2011	0.100	50.	12.
20000.	80	5.000	20.000	0.- 360.	0.0220	0.1543	0.100	50.	12.
20000.	100	5.000	20.000	0.- 360.	0.0217	0.1368	0.100	50.	12.
20000.	120	5.000	20.000	0.- 360.	0.0204	0.1078	0.100	50.	12.
20000.	140	5.000	20.000	0.- 360.	0.0198	0.0887	0.100	50.	12.
20000.	160	5.000	20.000	0.- 360.	0.0180	0.0788	0.100	50.	12.
20000.	180	5.000	20.000	0.- 360.	0.0158	0.0780	0.100	50.	12.

TABLE 7

Simulation Results : Amplitude ratio and Frequency limitations

DIGITAL NETWORK ANALYSIS

FREQUENCY (HZ)	NO.OF POINTS	SAMPLING INTERVAL (MICROS)	ACTUAL MAG (DB)	ACTUAL PHASE (DEG)	MAX. ERROR MAG (DB)	MAX. ERROR PHASE (DEG)	PRCNT NOISE (%)	TIMING ERROR (PICOS)	NO.OF BITS
20000.	10	5.000	5.000	0.- 360.	0.0058	0.0165	0.050	50.	12.
20000.	10	5.000	10.000	0.- 360.	0.0084	0.0337	0.050	50.	12.
20000.	10	5.000	15.000	0.- 360.	0.0114	0.0558	0.050	50.	12.
20000.	10	5.000	20.000	0.- 360.	0.0131	0.1043	0.050	50.	12.
20000.	10	5.000	25.000	0.- 360.	0.0319	0.2279	0.050	50.	12.
20000.	10	5.000	30.000	0.- 360.	0.0451	0.3273	0.050	50.	12.
20000.	10	5.000	35.000	0.- 360.	0.0906	0.6985	0.050	50.	12.
20000.	10	5.000	40.000	0.- 360.	0.1567	1.0701	0.050	50.	12.
1.	200	10000.000	20.000	0.- 360.	0.0073	0.0250	0.050	50.	12.
10.	200	1000.000	20.000	0.- 360.	0.0066	0.0231	0.050	50.	12.
100.	200	100.000	20.000	0.- 360.	0.0074	0.0255	0.050	50.	12.
1000.	200	10.000	20.000	0.- 360.	0.0072	0.0252	0.050	50.	12.
5000.	80	5.000	20.000	0.- 360.	0.0095	0.0477	0.050	50.	12.
10000.	40	5.000	20.000	0.- 360.	0.0128	0.0616	0.050	50.	12.
11000.	200	5.000	20.000	0.- 360.	0.0058	0.0191	0.050	50.	12.
12000.	50	5.000	20.000	0.- 360.	0.0106	0.0424	0.050	50.	12.
13000.	200	5.000	20.000	0.- 360.	0.0056	0.0224	0.050	50.	12.
14000.	100	5.000	20.000	0.- 360.	0.0090	0.0397	0.050	50.	12.
15000.	40	5.000	20.000	0.- 360.	0.0110	0.0476	0.050	50.	12.
16000.	25	5.000	20.000	0.- 360.	0.0133	0.0552	0.050	50.	12.
17000.	200	5.000	20.000	0.- 360.	0.0058	0.0244	0.050	50.	12.
18000.	100	5.000	20.000	0.- 360.	0.0093	0.0355	0.050	50.	12.
19000.	200	5.000	20.000	0.- 360.	0.0065	0.0193	0.050	50.	12.
20000.	20	5.000	20.000	0.- 360.	0.0131	0.1043	0.050	50.	12.
21000.	200	5.000	20.000	0.- 360.	0.0065	0.0209	0.050	50.	12.
22000.	100	5.000	20.000	0.- 360.	0.0088	0.0404	0.050	50.	12.
23000.	200	5.000	20.000	0.- 360.	0.0061	0.0171	0.050	50.	12.
24000.	25	5.000	20.000	0.- 360.	0.0133	0.0523	0.050	50.	12.
25000.	24	5.000	20.000	0.- 360.	0.0207	0.1219	0.050	50.	12.
26000.	100	5.000	20.000	0.- 360.	0.0085	0.0342	0.050	50.	12.
27000.	37	5.000	20.000	0.- 360.	0.0152	0.1434	0.050	50.	12.
28000.	50	5.000	20.000	0.- 360.	0.0099	0.0370	0.050	50.	12.
29000.	69	5.000	20.000	0.- 360.	0.0106	0.0732	0.050	50.	12.
30000.	20	5.000	20.000	0.- 360.	0.0142	0.0764	0.050	50.	12.

4.3 THEORETICAL SYSTEM SPECIFICATIONS :

Based on the simulation results of the previous section, the measurements of the relative amplitudes and the phase differences can be summarized as follows.

For the network analysis with the uncertainty of ±0.015 dB in amplitude and ±0.1° in phase, at frequencies upto 24000 Hz and actual amplitude ratio of upto 20 dB, the measurement system should be able to sample the reference and test signals at the sampling frequency of 200 kHz with the timing error of maximum 350 ps, the analog-to-digital converter resolution should be 12 bits and the signal to noise ratio at the input of the system should be better than 66 dB.

With a measuring system meeting the above specifications, a sinusoidal signal of the required frequency is generated by a digital synthesizer, and the samples of the reference and test voltage waveforms are taken at predetermined intervals for an integral number of periods. The sampling interval is an integral fraction of the period or a sub-multiple of the period of the waveform. The values of the instantaneous signal voltage acquired by the s/h circuits are digitized using analog-to-digital converters with a resolution of 1 part in 2048. The sampling and quantization process is controlled by a microprocessor system. The digital values are then transferred to a minicomputer which determines the required s-parameters

after numerical calculations and outputs the results on a printer.

Chapter V

EXPERIMENTAL SYSTEM AND PROCEDURE

This chapter provides a description of the experimental system and measurement procedure.

The description of the system is divided into two sections : hardware and software. The hardware part describes the equipment and components used, while the software part deals with the algorithm and program development.

5.1 SYSTEM HARDWARE :

This section is concerned mainly with the hardware portion of the system. An overall block diagram is shown in figure 8.

Looking at the figure, it can be seen that the front end of the system is a minicomputer PDP 11/34 connected to a CRT terminal and a line printer. Also connected to the PDP 11/34 is the measurement hardware for network analysis and is treated as another terminal device by the computer.

The measurement hardware consists of a microprocessor controlled digital frequency synthesizer and synchronous detectors for the digital processing of reference and test signals. At the end, a low-pass filter, a power splitter, a

directional coupler for reflection measurements, and the device being tested complete the experimental system.

A brief description of all the components constituting the system is provided below with special emphasis on the synthesizer/detector interface.

5.1.1 Device under test :

The test device can be any active or passive device such as amplifier, attenuator or phase shifter, whose reflection and transmission characteristics are to be quantified. During the calibration process, the test device represents the load, short or shielded open for reflection calibration and "through" for transmission calibration.

5.1.2 Synthesizer/Detector interface unit :

The synthesizer/detector interface provides a link between the PDP 11/34 and the analog part of the system. This link between the analog and the digital sections is microprocessor controlled and has two subblocks :

1. Digital frequency synthesizer and
2. Digital detector

The main constituents of these blocks, and the components they are connected to, are described in the following sections.

5.1.2.1 Digital frequency synthesizer :

The digital synthesizer is implemented by using a counter to generate addresses for stored sine data. It provides the required incident signal for device characterization. The functional blocks of the hardware are shown in figure 10.

The synthesizer part of the interface consists of two binary counters, a look-up table and a digital-to-analog converter. An Intel 8085 microprocessor, under the control of the PDP 11/34, sets up the outputs of the data latch to the required digital frequency value f_d. This frequency value f_d, controls the counting sequence of the "clock frequency selection counter", which provides the appropriate clock frequency to the "address generation counter". Thus, the address generator runs at a particular speed depending on the frequency of the signal being generated. The two counters are made up of synchronous 4-bit binary counter IC's (74163) with a maximum operating speed of 32 MHz. The output of the address generator activates the 2716 16K(2Kx8) EPROM's, which contain the look-up table of 12-bit numbers and has an access time of maximum 450ns.

Depending on the address at its input, the memory circuit reads the 12-bit numbers at the input of the 12-bit D/A converter (AD 565J). The converter is set on offset-binary inputs for conversion and has a settling time of maximum 400ns as specified by the manufacturer. This speed makes it compatible with the memory access time for sine data.

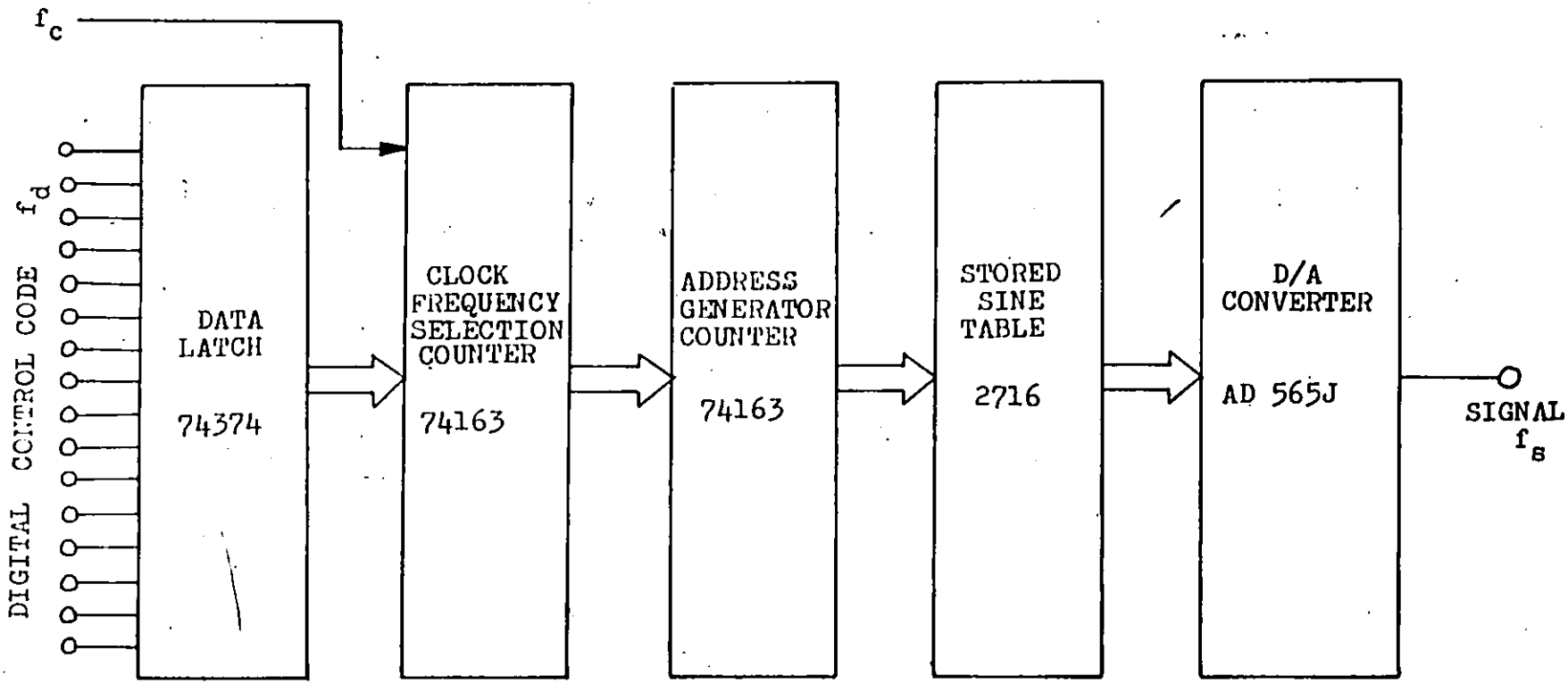


Figure 10: Functional blocks of digital synthesizer

The output of the D/A converter provides a signal of the required frequency f_s which contains harmonics and sampling components. The output voltage is ±1V and the output impedance is 50 Ω.

The synthesizer generates frequencies according to the following relation :

$$f_s = \frac{f_k}{(4095-f_d) + 1} \qquad (5.1)$$

In the above relation, f_k = 48kHz, 6kHZ or 1.5kHz and f_d = 0,1,2, ..., 4094.

5.1.2.2 Low-pass filter :

A low-pass filter is used in the system to smooth the sinusoidal signal generated by the digital synthesizer. The process of digital frequency synthesis introduces distortions of the generated signal due to harmonics and sampling components. The range of signal frequencies obtained from the above synthesizer vary from 1 Hz to 24 kHz, and consequently require a low-pass filter with variable pass band to smooth the generated sinusoidal signal. In the experimental setup, this requirement is satisfied by a KROHN-HITE model 3202 low-pass filter, which provides a wide range of cutoff frequencies from 20 Hz to 2 MHz. The filter is tuned manualy, but a filter providing hardware control of cutoff frequency should give better system performance. The effect of filtering on the signal from synthesizer is discussed in chapter six.

5.1.2.3 Power splitter :

A power splitter is a device which accepts an input signal and delivers multiple output signals with specific phase and amplitude characteristics. The circuit diagram of the power splitter used is shown in figure 11.

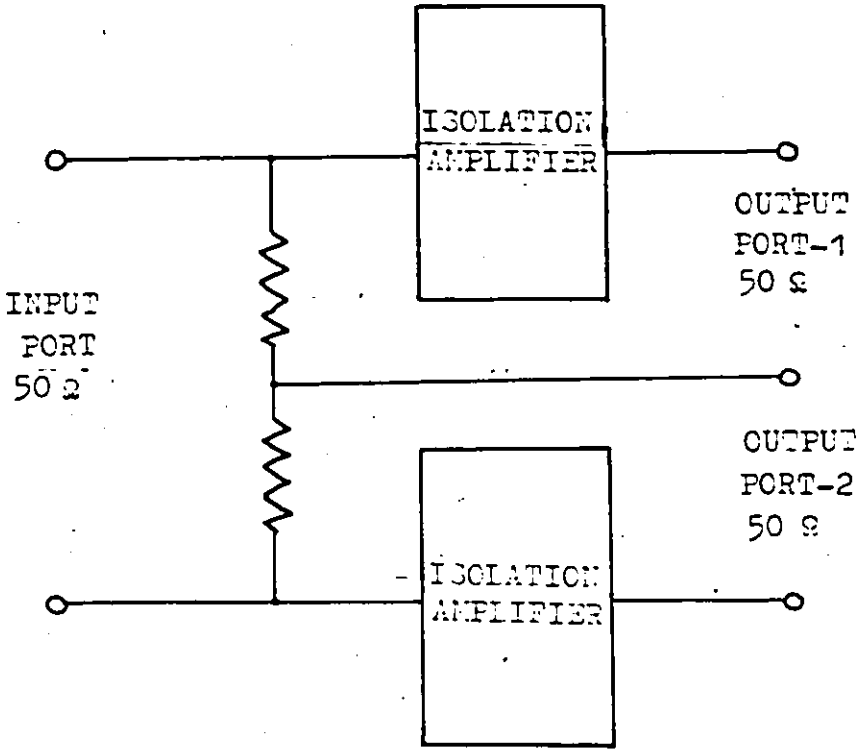


Figure 11: Power splitter circuit diagram

This two-way power splitter was designed to work at the measurement frequency range of 1 Hz to 24 kHz. The impedance presented by the circuit at all three ports is 50 ohms. This configuration of the circuit with instrumentation amlifiers in both the channels, provide high isolation (nearly infinite), between the two output ports. This is neccessary for making very accurate reflection and transmission measurements.

The input to the power splitter is obtained from the output of the low-pass filter. At its output ports, two equal amplitude and phase signals are obtained, one of which is used as a reference signal and the other as a test signal. The reference signal is fed directly to the reference port of the digital detector (section 5.1.2.5). In the case of transmission measurements, the test signal is the input to the device being tested. The output from the device is connected to the test port of the detector.

5.1.2.4 Directional coupler :

For the measurement of reflection parameters of a device, the test signal from the power splitter is fed to the output port of a directional coupler. The input port of the directional coupler is connected to the test port of the device. The reflected signal from the device port is obtained at the coupled port of the directional coupler which is connected to the test port of the digital detector.

The directional coupler used in the system was a Mini-Circuits' ZDC-15-6, which covers the frequency range from 10 kHz to 35 MHz. The coupler's main line loss is 0.3 dB, the coupling coefficient is (15 ± 0.5) dB, the VSWR is 1.15 and the directivity is 38 dB.

5.1.2.5 Digital Detector :

A functional block of the digital detector is shown in figure 12. It is used to sample the reference and test signals at predetermined intervals.

The "reference" signal is obtained at one of the ports of the power splitter and its power level is 3.0dB below the output from the digital synthesizer.

The "test" signal is fed to the detector after the signal at the second port of the power splitter has undergone amplitude and phase change due to the device being tested. It can be a transmitted signal at the output port of the test device or a reflected signal separated from the input to the device by a directional coupler and sampled at the output of its auxilliary port.

The two signals are fed to two high-impedance instrumentation amplifiers (AD 524J) which have gain of 10 and have a flat response from 1Hz to 100 kHz. The gain raises the ±0.5V inputs to the level required by sample and hold circuitry, that is ±5V peak. An important consideration in acurate phase measurement is that the phase shift be the same in both channels. The effect of small difference in phase shift is cancelled by the calibration phase of measurement procedure. The above two signals are fed to two parallel s/h circuits (HTC 0300) that are physically part of the converter unit. The maximum aperture uncertainty for these s/h circuits is 100ps. The sampled

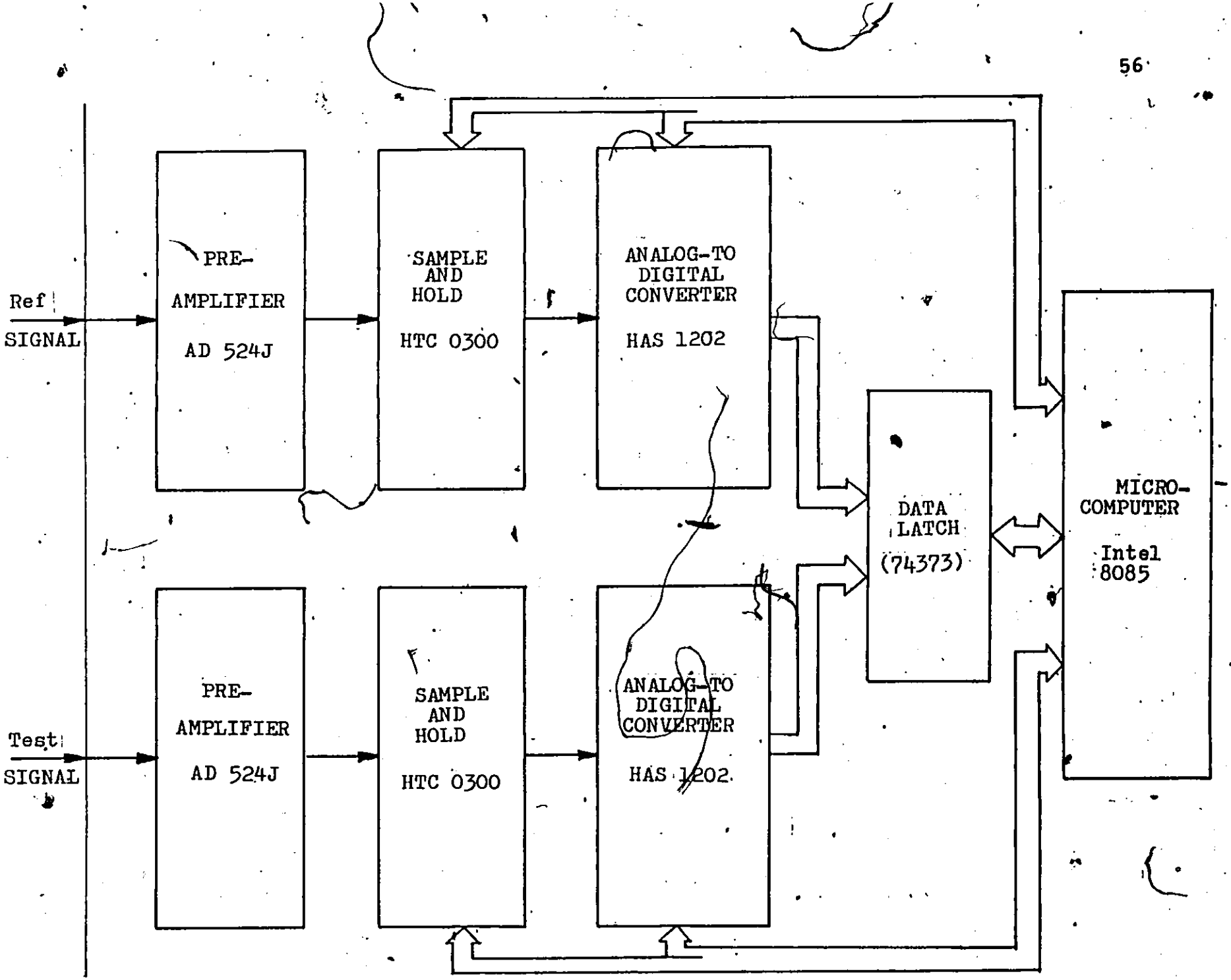


Figure 12: Functional blocks of digital detector

"instantaneous" voltages are retained at the outputs of the s/h amplifiers within the specified accuracy limits long enough for the analog-to-digital conversion to be completed. The A/D converters used are HAS1202 hybrid circuits with the conversion time of 2.2 μs maximum for complete 12-bit conversion with an accuracy of 0.012% of full scale. The two resulting 12-bit digital numbers are latched into a hardware register to be read by the microprocessor under program control.

The above configuration is preferable to perhaps the more usual one where analog multiplexer feeds signals to a single channel analog-to-digital converter. It avoids the additional errors introduced by analog multiplex switching circuits, but it requires equality of the analog-to-digital converters or a suitable correction. Specifications of commercially available units indicate that an overall short term accuracy of 0.01% can be maintained under favorable conditions.

Each of the analog-to-digital converters converts the analog input by the method of successive approximation to a 12-bit offset-binary number. The actual conversion time is typically 2.2 μs. Taking into account various settling times and the time required to transfer the output data, a minimum of 7.8125 μs is required between conversion cycles which is possibly fastest under Intel 8085 control at 3.072 MHz clock rate. Consequently, the maximum possible sampling

rate is 128 kHz. The whole process is pipelined and so it requires to undergo a few conversion cycles to clear the channel before correct digital values are obtained.

5.1.2.6 Microcomputer :

The microcomputer part of the interface is the controller for the frequency synthesis and the sampling of reference and test signals. It uses the Intel 8085 microprocessor and memory circuits with other control circuits to execute the job of a controller. It communicates with the minicomputer to obtain the instructions and transmit the samples.

5.1.3 The PDP 11/34 :

A PDP 11/34 minicomputer using the RSX-11M real time, multiprogramming operating system is utilized for data acquisition, data processing for sine curve fitting and error correction after calibration, and overall system control by means of commands to the Monitor Console Routine (MCR).

The computer system consists of a KD 11-LA console unit, the core/MOS memory unit and various peripheral devices connected through a Unibus [3]. It is connected to the CRT TERMINAL for operator interface and a LINE PRINTER to print out the measurement results.

The experimental setups for reflection and transmission measurements are shown in figure 13a and figure 13b, respectively.

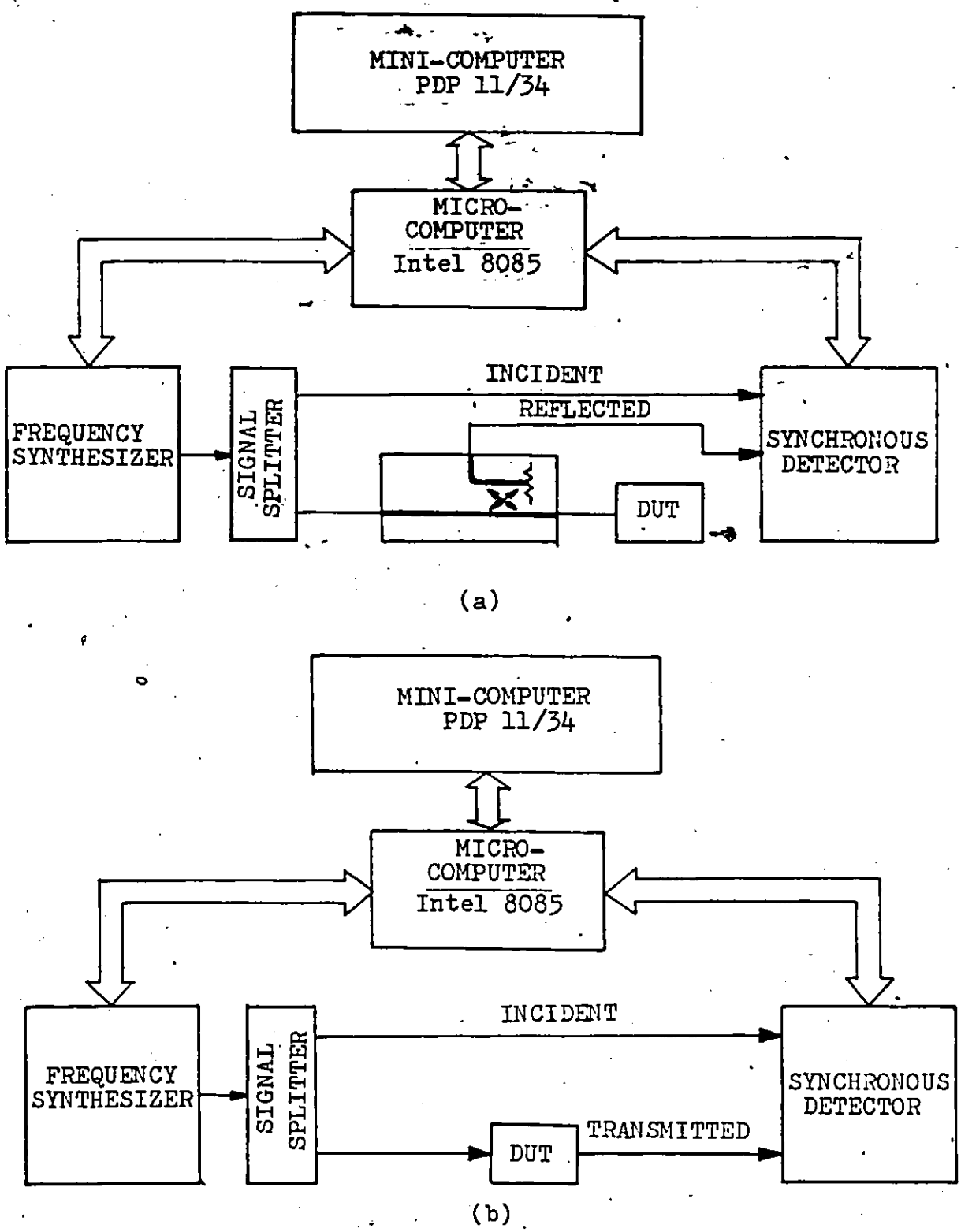


Figure 13: Experimental set-up (a) Reflection measurement
(b) Transmission measurement.

Note : DUT → Device under test

5.2 SYSTEM SOFTWARE :

The software discussed in this section is divided into two classes :

1. Interface control
2. System control

5.2.1 Interface control :

The control program for the synthesizer/detector interface is written in Intel 8085 assembly code [9] and is an extension of its basic monitor routine [8]. The three routines which have been added to the monitor are used for the following purposes:

1. Setting the synthesizer frequency.
2. Acquiring a specific number of samples of reference and test signals at the specified sampling interval and
3. Transmitting the acquired samples to the minicomputer.

The instruction format for these actions are

1. Frequency synthesis Fxxxx
   where xxxxH represent the hexadecimal digital frequency value f_d (section 5.1.2.1).
2. Sampling of signals Axxxx yyyy
   where xxxxH represent the delay to be introduced between the samples in order to maintain the required sampling interval and yyyyH is the number of samples,

of reference and test signals, to be acquired. The maximum value of allowable samples is 200 at the fastest sampling rate and 256 at slower rates.

3. Transmission of data Txxxx
   where xxxxH denotes the number of samples to be transmitted to the minicomputer.

The routines of the monitor interpret these instructions, which are compatible with the rest of the monitor instructions, and takes proper action by controlling the D/A- and A/D-based hardware described in section 5.1.2.

These routines extend the monitor by 603 bytes of memory. The execution times for the three routines are as follows :

1. Frequency setting takes 153.15 ms.
2. Execution time for sampling process depends on the number of samples and the sampling rate. It is given by the following expression:

   250.89 ms + sampling interval X number of samples

3. Execution time for data transmission also depends on the number of samples to be sent. It can be given by (228.71 + 75.56 N) ms, where N is the number of samples transmitted.

5.2.2 System control :

The system control software is discussed in this section under three basic headings. These are as follows :

1. Human interface
2. Data acquisition and
3. Data processing.

The data output part of control is distributed among three above parts.

A flow chart illustrating the overall system control structure is shown in figure 14. This figure closely parallels the description of the experimental procedure. The flow chart also shows the points in the procedure at which the system expects operator interaction, which falls under two categories. The first category consists of inputs by the operator which are expected by the system at specific points throughout the measurement. Such inputs include specification of measurement frequencies, selection of s-parameters etc. The second category instructs the operator for the mechanical action such as connecting the standard terminations for calibration, device and setting the filter cutoff frequency.

5.2.2.1 Operator interface :

This part of the software instructs the human operator as it steps through the entire measurement procedure. It also receives the signals from the operator informing the system

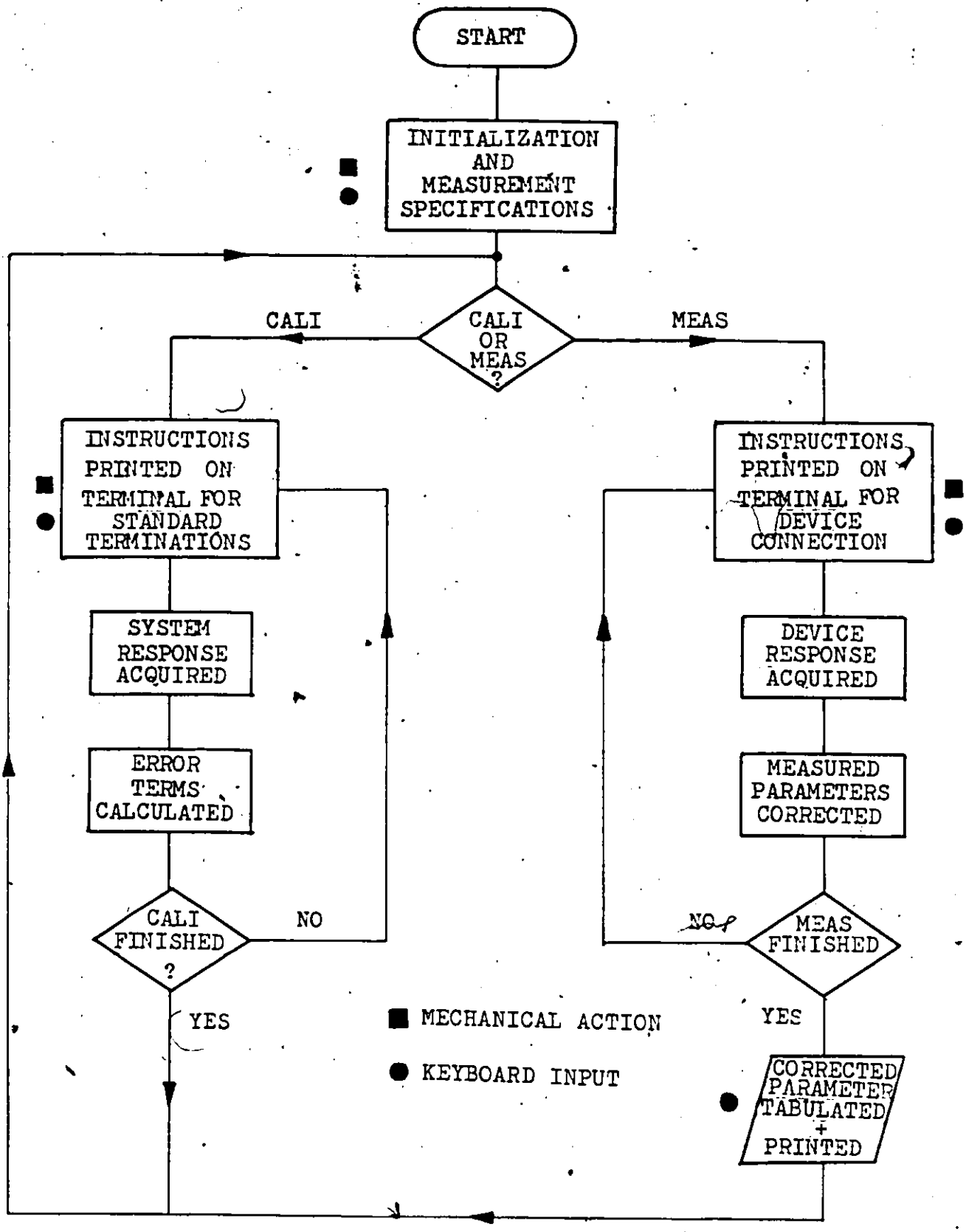


Figure 14: System flow diagram

that a certain required action has been taken and communicates to the operator as to which phase of the measurement is being performed. The prompts of the operator also specifies whether numerical or alphabetical parameters are to be entered.

The operator interfaces with the minicomputer through the CRT terminal and a keyboard. The user instructions appear on the terminal and the final output is also shown on the terminal. When requested by the operator, the final output is sent to the line printer.

5.2.2.2 Data acquisition :

In the data acquisition phase, the device characteristics are obtained on a point-to-point basis at the frequencies specified by the operator. The data are obtained as follows: The measurement frequency value (f_s) is first converted into a four-digit hexadecimal frequency value (f_d) according to the equation 5.1. Since only integer values are allowed, the program checks all three ranges and takes the nearest possible frequency value. This digital code is sent to the synthesizer interface and the corresponding output signal of the frequency f_s is produced. The output signal from the synthesizer, after being modified in the device under test, reaches the set of synchronous detectors. The program computes the number of samples and sampling interval for the frequency f_s and activates the detector

interface. Once the sampling is over, the data are received from the interface as two arrays of samples for reference and test signals.

The above sequence of operations is repeated for every measumement frequency, and for each case of calibration with different standard terminations, and for measurement with the unknown device.

5.2.2.3 Data processing :

This block of software can be partitioned into three functional subblocks. These are : sine curve fitting, determination of error terms during calibration, and calculation of final results for the device. The two sets of samples of reference and test signals at a particular frequency are fitted with sinusoidal curves using the relations of section 3.2. The amplitudes and phase thus obtained, are used to calculate the relative amplitude and phase, which are stored in another array. These values are used to obtain the error terms for the measurement system.

During the calibration for reflection measurement, if E_1, E_2 and E_3 represent the relative amplitude and phase for measurements with matched load, short and a shielded open, respectively, the error terms are calculated as follows :

Effective directivity error

$$E_{DF} = E_1 \qquad (5.2)$$

Effective source match error

$$E_{SF} = \frac{C(E_3-E_1) + (E_1-E_2)}{(E_3-E_2)} \qquad (5.3)$$

where C is the capacitance correction term for the shielded open used during calibration and is obtained from manufacturer specified values.

Reflection tracking error

$$E_{RF} = (1+ E_{SF})(E_1-E_2) \qquad (5.4)$$

During the calibration for transmission measurement, if E_4 is the relative amplitude and phase for measurement with "through" connection, the error term is given by

$$E_{TF} = E_4 \qquad (5.5)$$

The above error terms are calculated for each frequency points and stored in an array.

Once the calibration is complete, the system measures the relative amplitude and phase for the device being characterized. The values obtained are corrected, using the relations in section 2.2.4, for each frequency point. The final results are then stored as another array of data with respective frequency information.

5.3 EXPERIMENTAL PROCEDURE :

The measurement procedure rely on the external standards in order to be independent of such circuit parameters as drift, offset, gain, imperfections of signal separating device and effects of adapters. Each measurement sequence starts with the determination of error terms according to the modelled errors during calibration phase. These measurements are made in the same way as is done for the actual device, with the unknown device being replaced by a standard with known characteristics.

During the characterization of an unknown device, the appropriate set of calibration constants are used to correct the measured parameters. In this case, it is assumed that in the brief interval between calibration and measurement, the circuit parameters change only by negligible amounts and the computed values are independent of any circuit changes.

Chapter VI

EXPERIMENTAL RESULTS AND DISCUSSIONS

This chapter presents some experimental results and a critical evaluation of the system performance.

6.1 EXPERIMENTAL RESULTS :

The performance of the digital network analyzer was investigated in two stages. In stage one, the waveform generated by the digital synthesizer was analyzed for its harmonic contents using a spectrum analyzer. The testing of digital detector was accomplished by measurements of amplitude and phase characteristics of active and passive devices, in stage two.

6.1.1 Digital synthesizer performance evaluation :

The synthesizer performance was investigated to find the spectrum of the signal generated. The worst case of signal generation (ie. 24 kHz with 64 samples/period) was analyzed for harmonic contents, using a spectrum analyzer. The measurements were made 1) without low pass filtering and 2) with the low pass filter having the cutoff set at 50 kHz. The results are listed in table 8 and 9.

TABLE 8

Experimental Results of test on Digital Frequency synthesizer (without low pass filter)

Order of Harmonic	Percentage Amplitude (relative to fudamental)
1st	100
2nd	0.2512
3rd	0.1000
4th	0.0126
5th	0.0002
6th	0.0013
7th	0.0020
8th	0.0013
9th	0.0020
10th	0.0008
....	.....
63rd	0.0050
65th	------

The results show that the harmonic contents of digitally synthesized signal are reduced considerably (approximately 5 times) due to low pass filtering.

TABLE 9

Experimental Results of test on Digital Frequency synthesizer (with low pass filter)

Order of Harmonic	Percentage Amplitude (relative to fundamental)
1st	100
2nd	0.125900
3rd	0.020000
4th	0.000050
5th	0.000008
...	.....

6.1.2 Digital detector performance evaluation :

The detector part of the system was analyzed using a setup in figure 13. Due to the unavailability of a directional coupler for low frequency measurements, only transmission measurements were made.

The measurements on passive devices used standard attenuators of value 3 dB, 10 dB and 20 dB. These three attenuators were used in different combinations to obtain the attenuation values of 3 dB, 10 dB, 13 dB, 20 dB, 23 dB and 30 dB. Measurements were made over the available frequency range from 1 Hz to 24 kHz. For each measurement frequency, the experiment was repeated ten times and the mean and standard deviation for measured attenuation and

phase were calculated. Figures 15-26 show the experimental results for the measurements in the frequency range from 1 Hz to 10 kHz. The results for the frequency range from 12 kHz to 24 kHz are listed in Table 10.

Assuming that the attenuation remains constant over the frequency range from 1 Hz to 12 kHz, the mean of the results for each combination of attenuators was calculated. The calculated values are listed in Table 11. Since the phase shift of the attenuators is a variable parameter, the table shows the maximum standard deviation for phase measurements.

For the measurements on an active device, a Princeton Applied Research variable-gain amplifier was used. The digital network analyzer system was calibrated with a 20 dB attenuator in the test channel and then the measurements were made to obtain the amplifier response for 20 dB gain. The experimental results are listed in Table 12.

6.2 SYSTEM PERFORMANCE :

The experimental results of the last section show that the system can measure the relative amplitude and phase with an uncertainty of ±0.02 dB and ±0.2°, respectively, for the frequency range from 1 Hz to 12 kHz. Since the detector interface provides a maximum sampling rate of 128 kHz, the 16 kHz and 24 kHz signal are sampled at less than 10 times the signal frequency. This causes the higher uncertainty in the measurements at these frequencies.

TABLE 10

Experimental results for measurements on attenuators

FREQUENCY	ATTENUATION		PHASE	
	RMS	SD	RMS	SD
12000	2.92811	0.00511	0.08174	0.02251
16000	2.97078	0.00710	0.16369	0.06020
24000	2.93968	0.00732	0.14948	0.03771
12000	9.98874	0.00985	0.25114	0.04853
16000	10.05527	0.03137	0.41244	0.19555
24000	10.04271	0.00966	0.41215	0.07252
12000	12.93056	0.00935	0.26706	0.10101
16000	12.95351	0.04055	0.35846	0.12052
24000	12.96717	0.01361	0.45759	0.07374
12000	20.09546	0.01097	0.13653	0.13419
16000	20.10517	0.08085	0.38033	0.30752
24000	20.18505	0.02279	0.24406	0.15340
12000	22.98055	0.04045	0.19275	0.18174
16000	23.03090	0.06150	0.47768	0.46015
24000	23.12412	0.02808	0.20400	0.17250
12000	30.05651	0.02926	0.89997	0.27843
16000	29.98251	0.12054	1.53864	1.43052
24000	30.03876	0.05577	1.26396	0.39628

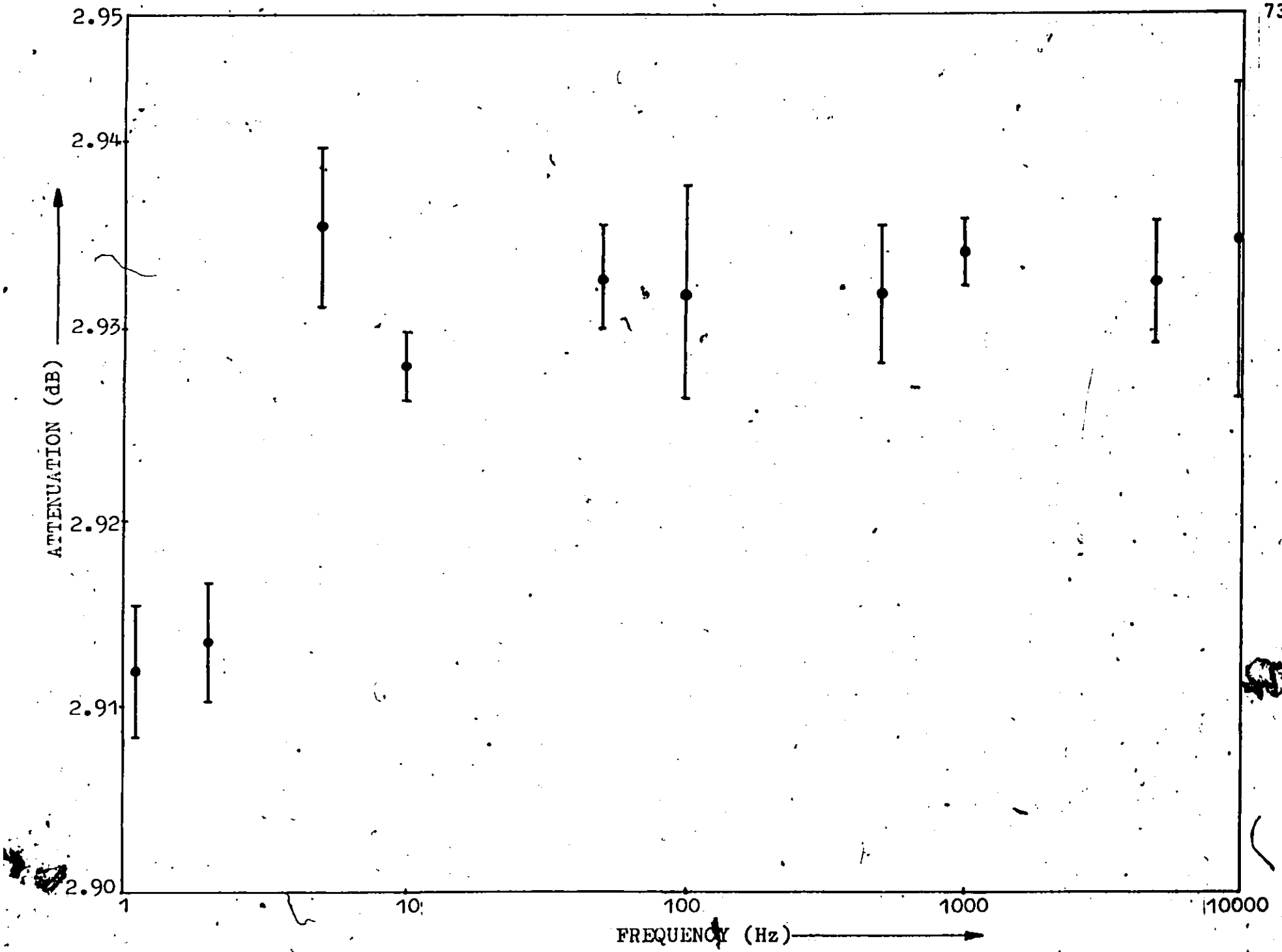


Figure 15: Experimental results : 3 dB attenuator amplitude characteristics

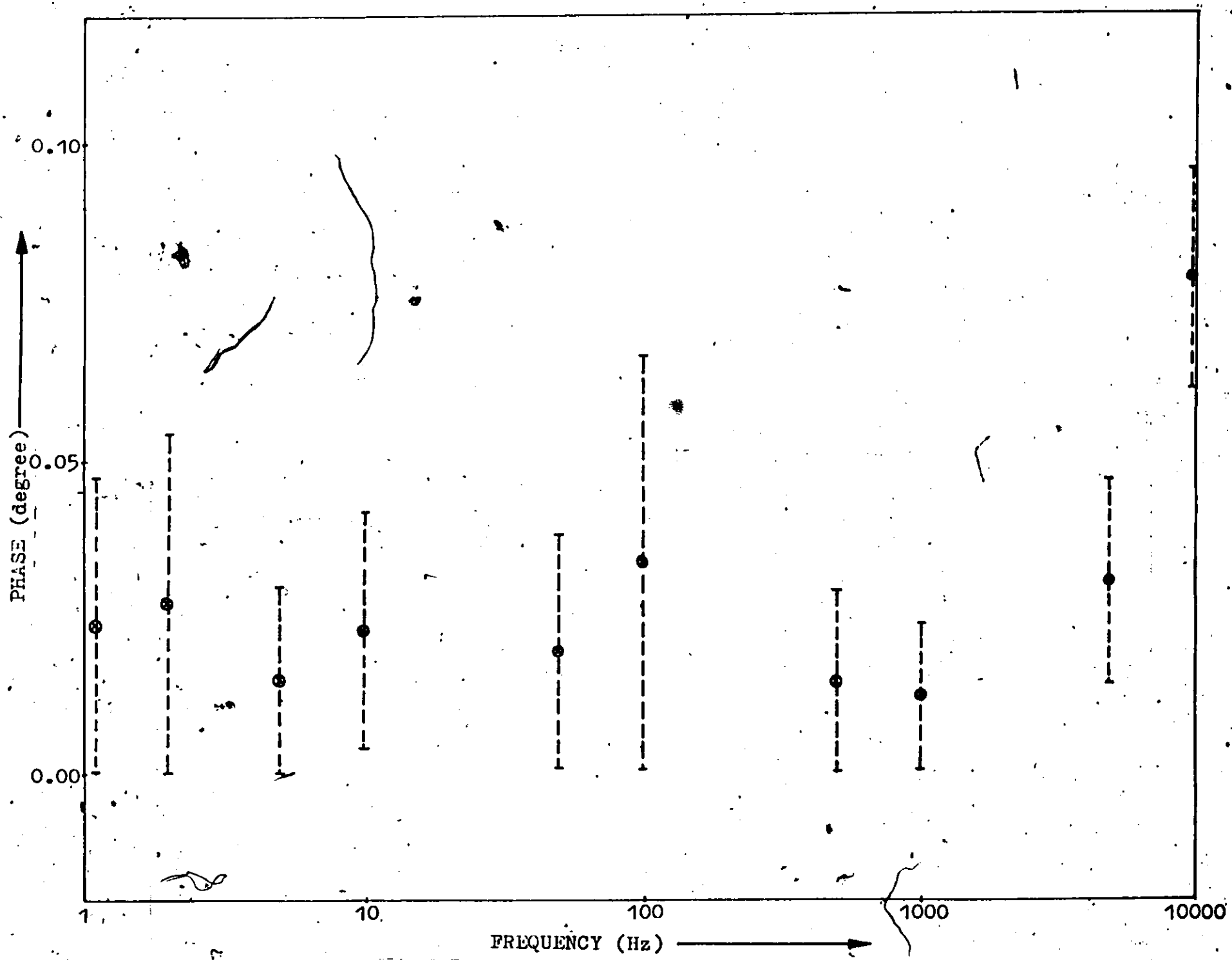


Figure 16: Experimental results : 3 dB attenuator phase characteristics

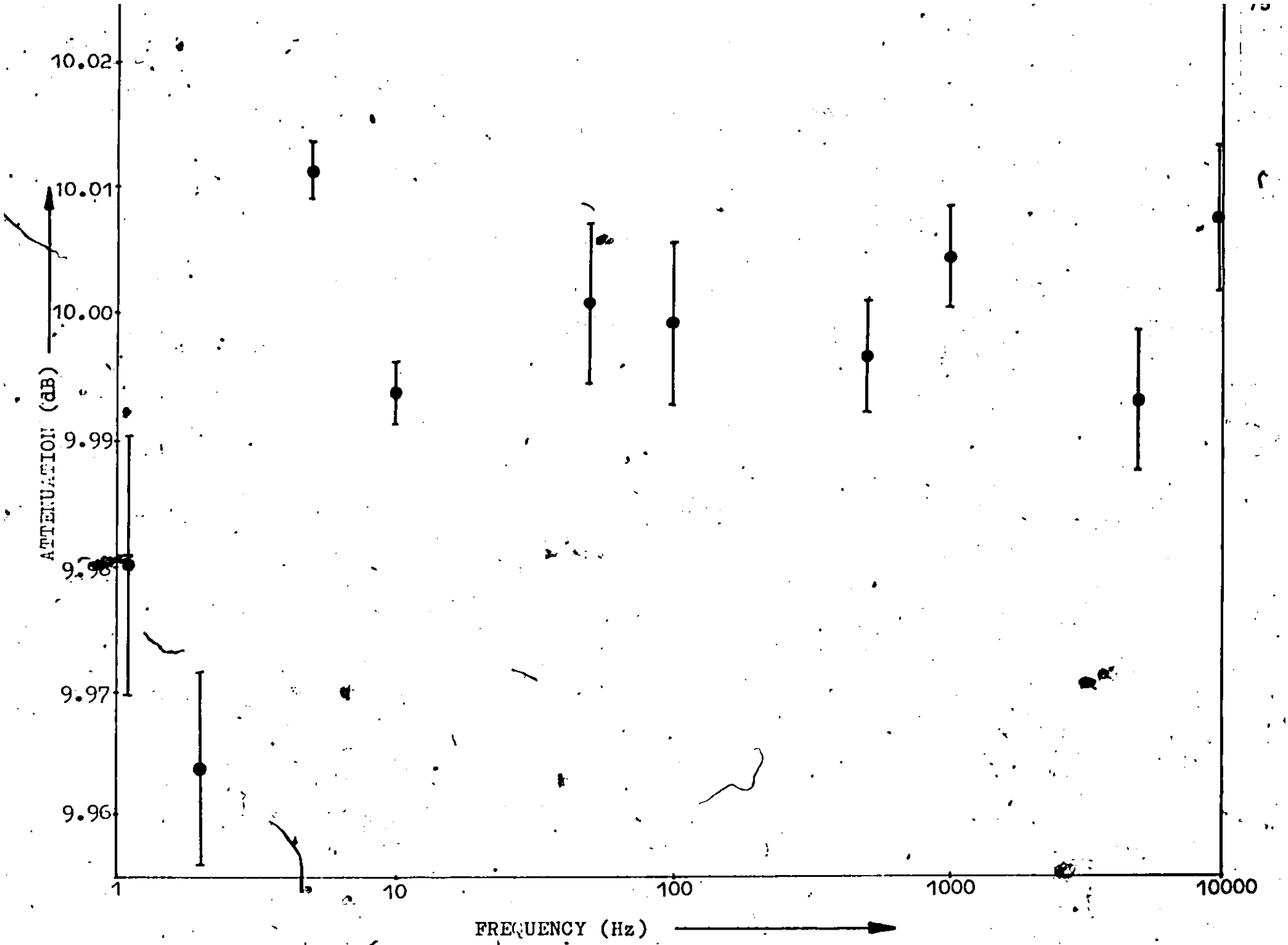


Figure 17: Experimental results : 10 dB attenuator amplitude characteristics

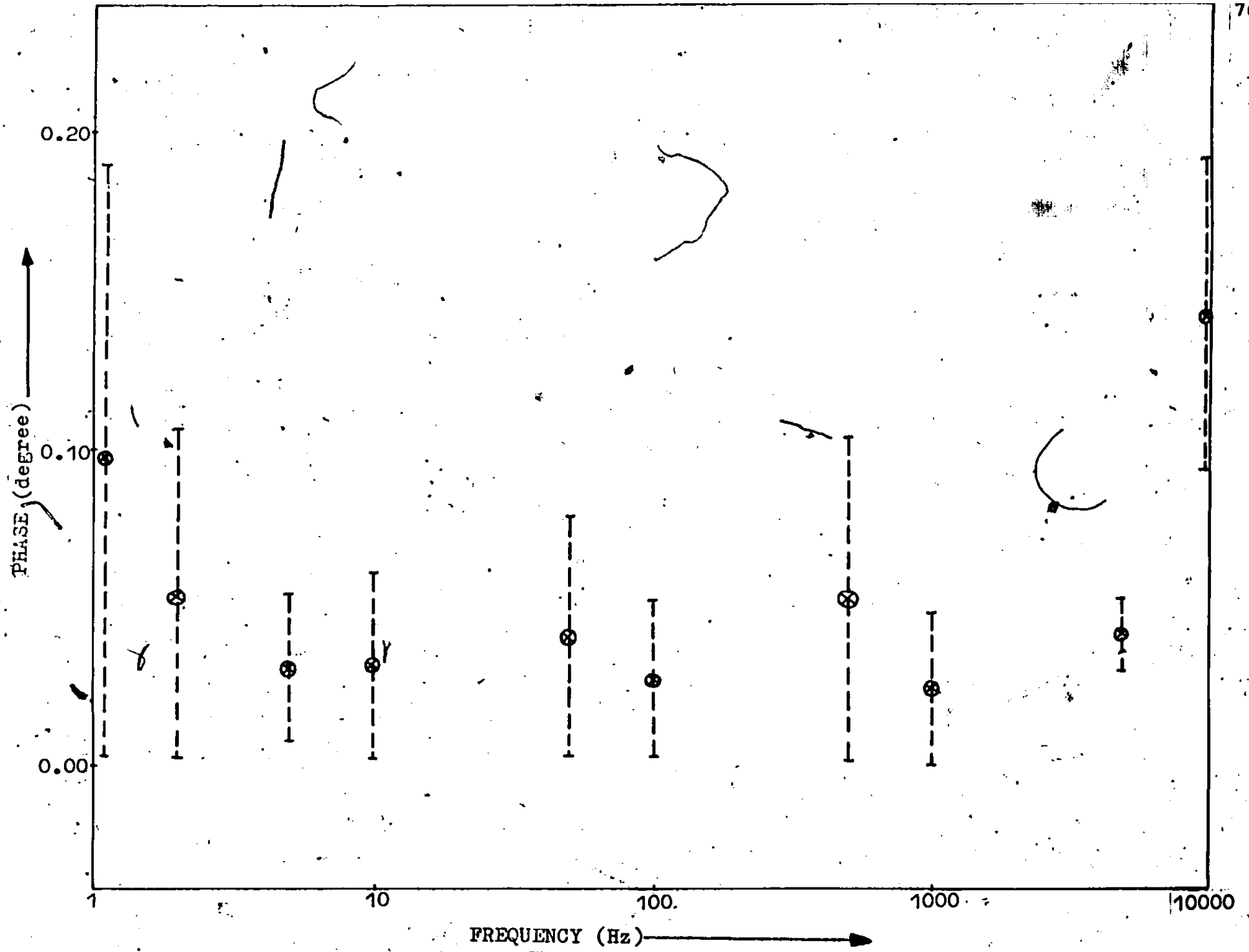


Figure 18: Experimental results : 10 dB attenuator phase characteristics

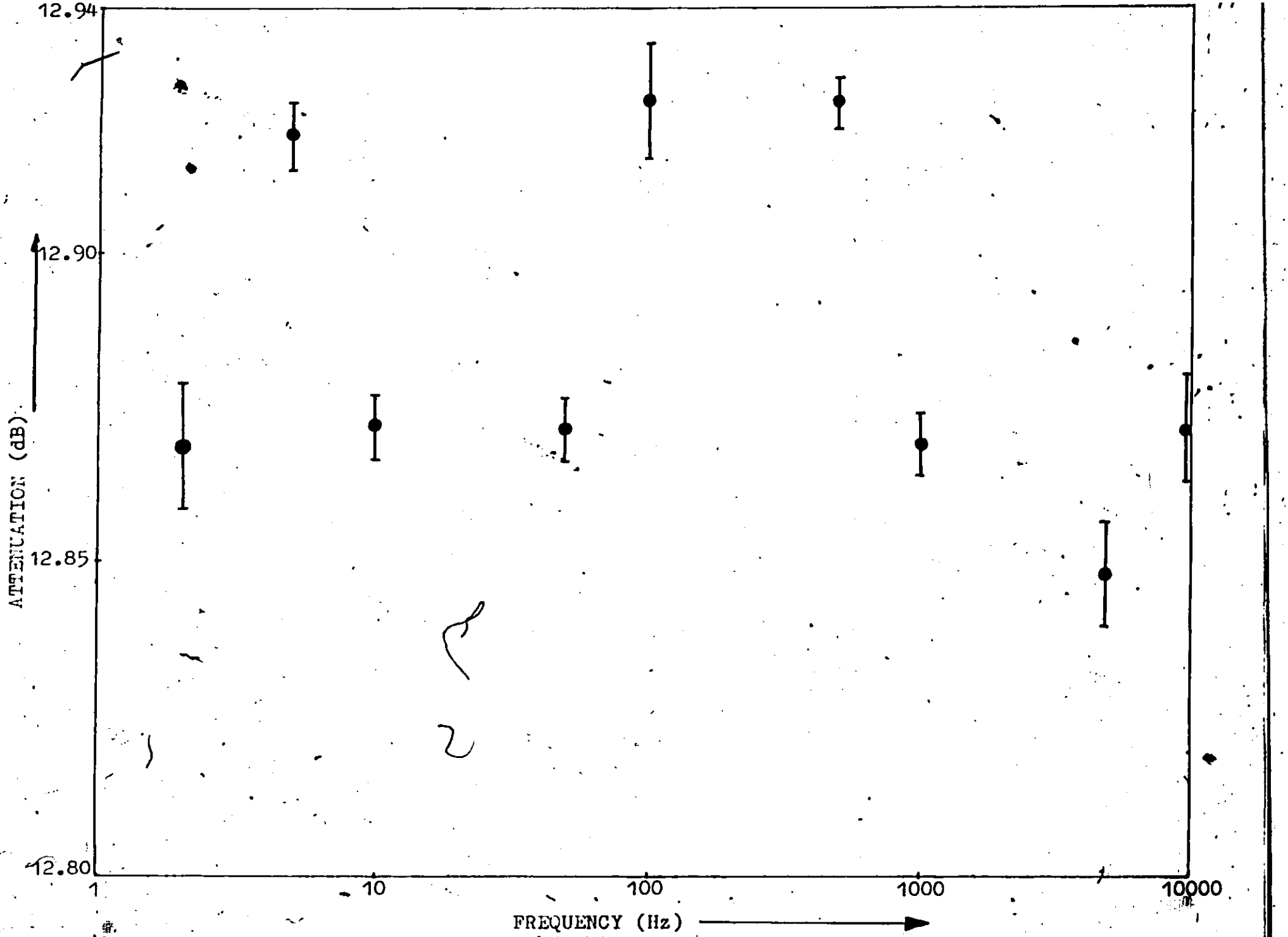


Figure 19: Experimental results : (10 + 3) dB attenuator amplitude characteristics

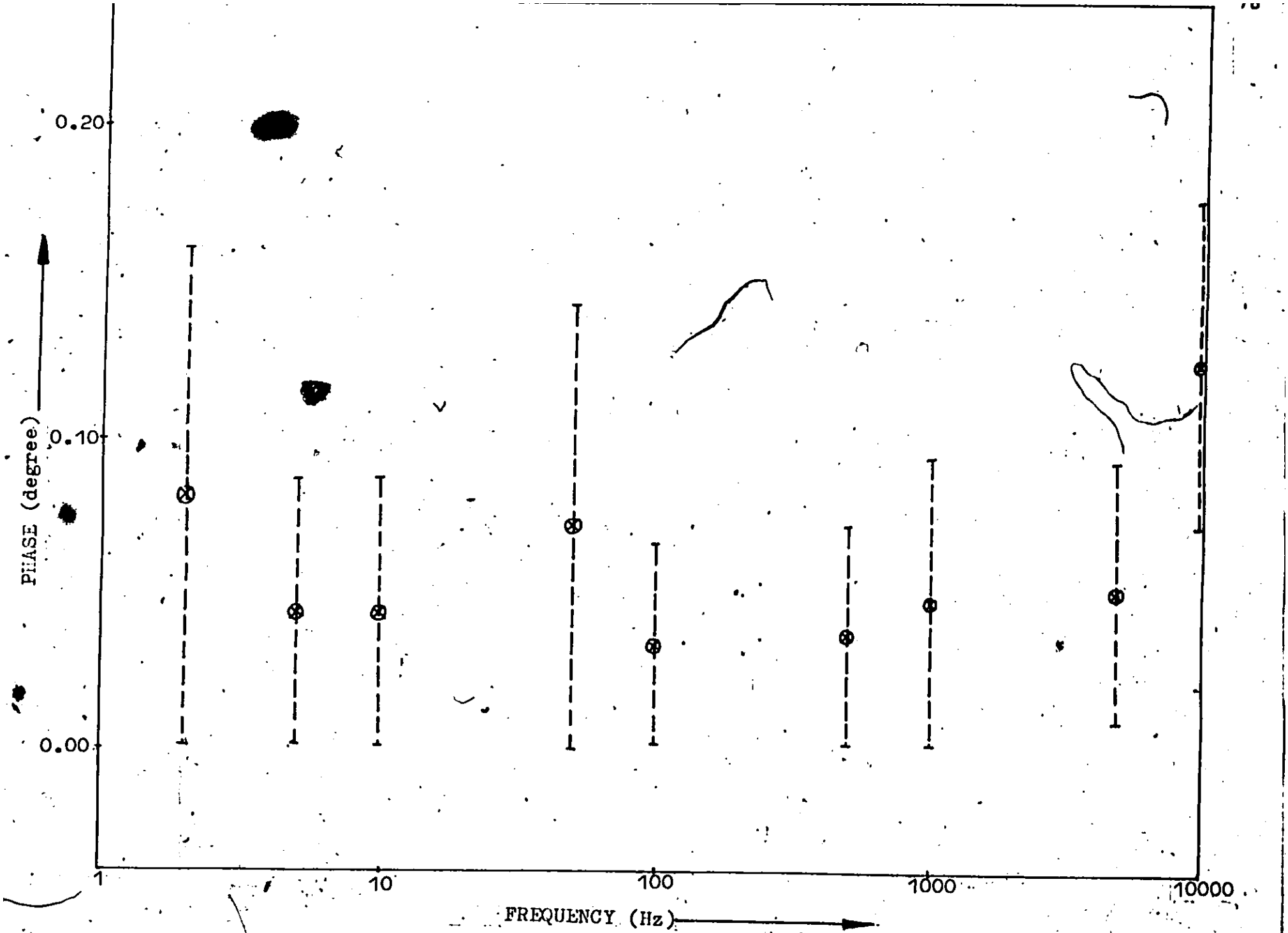


Figure 20: Experimental results : (10 + 3) dB attenuator phase characteristics

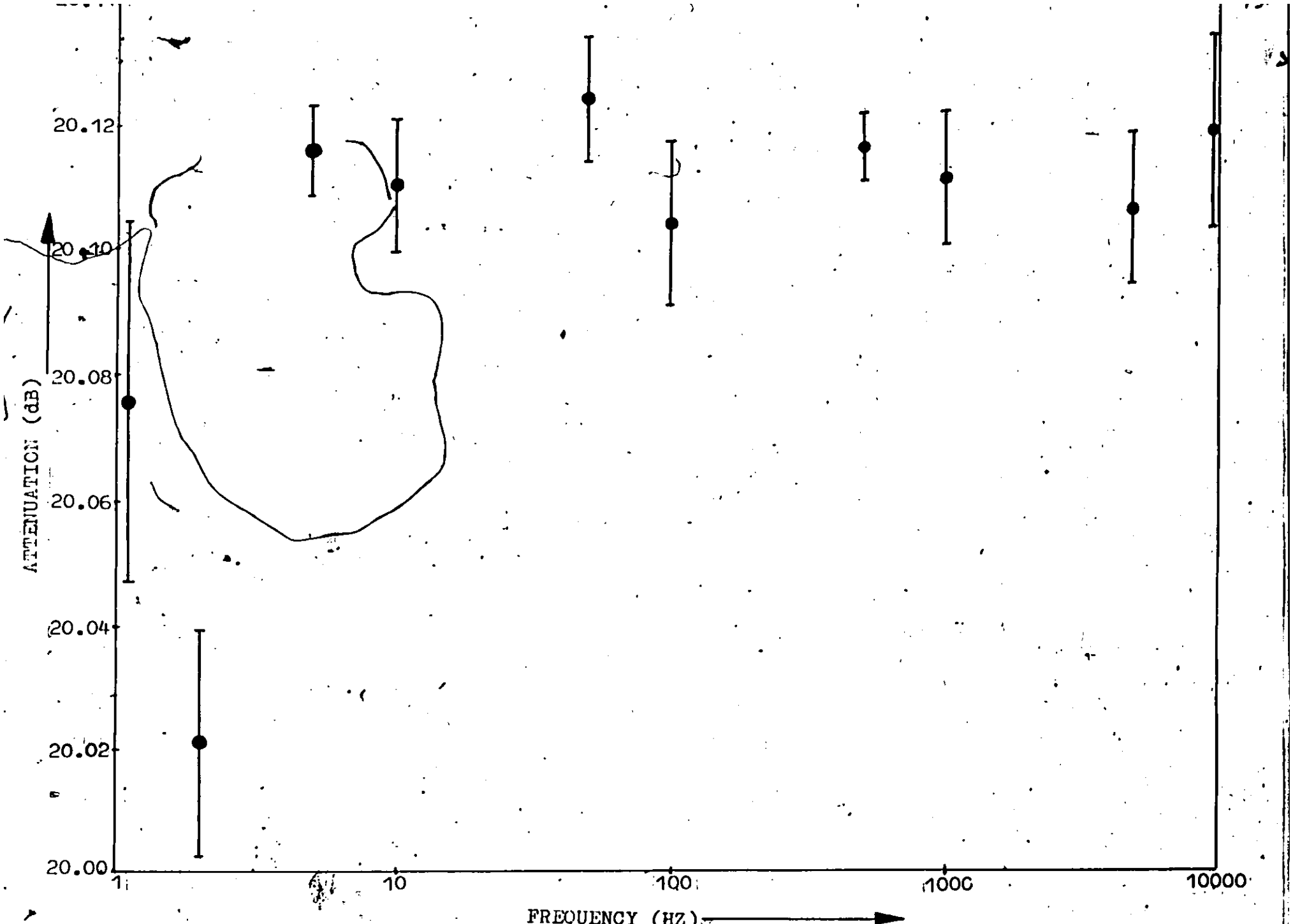


Figure 21: Experimental results: 20 dB attenuator amplitude characteristics

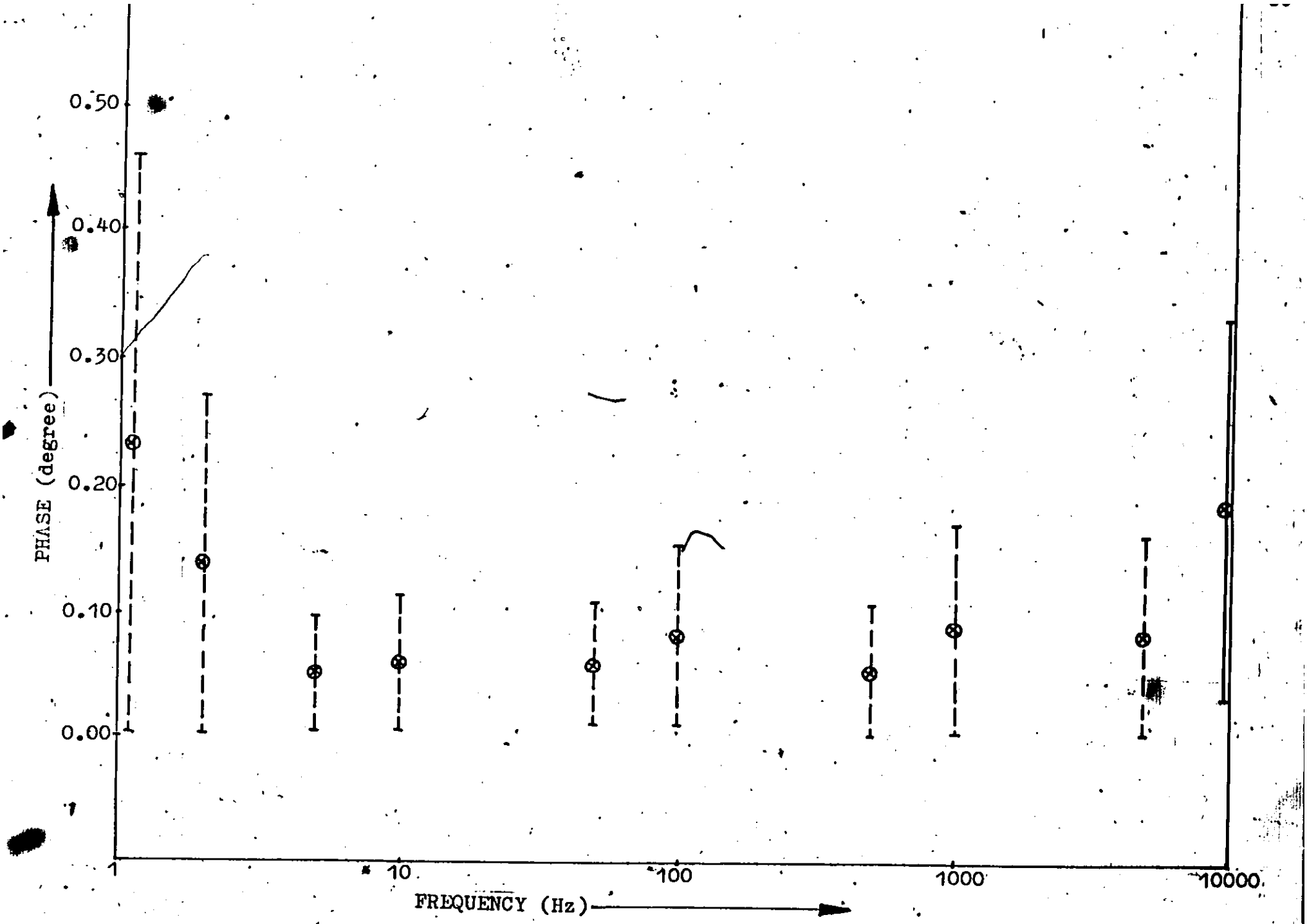


Figure 22: Experimental results : 20 dB attenuator phase characteristics

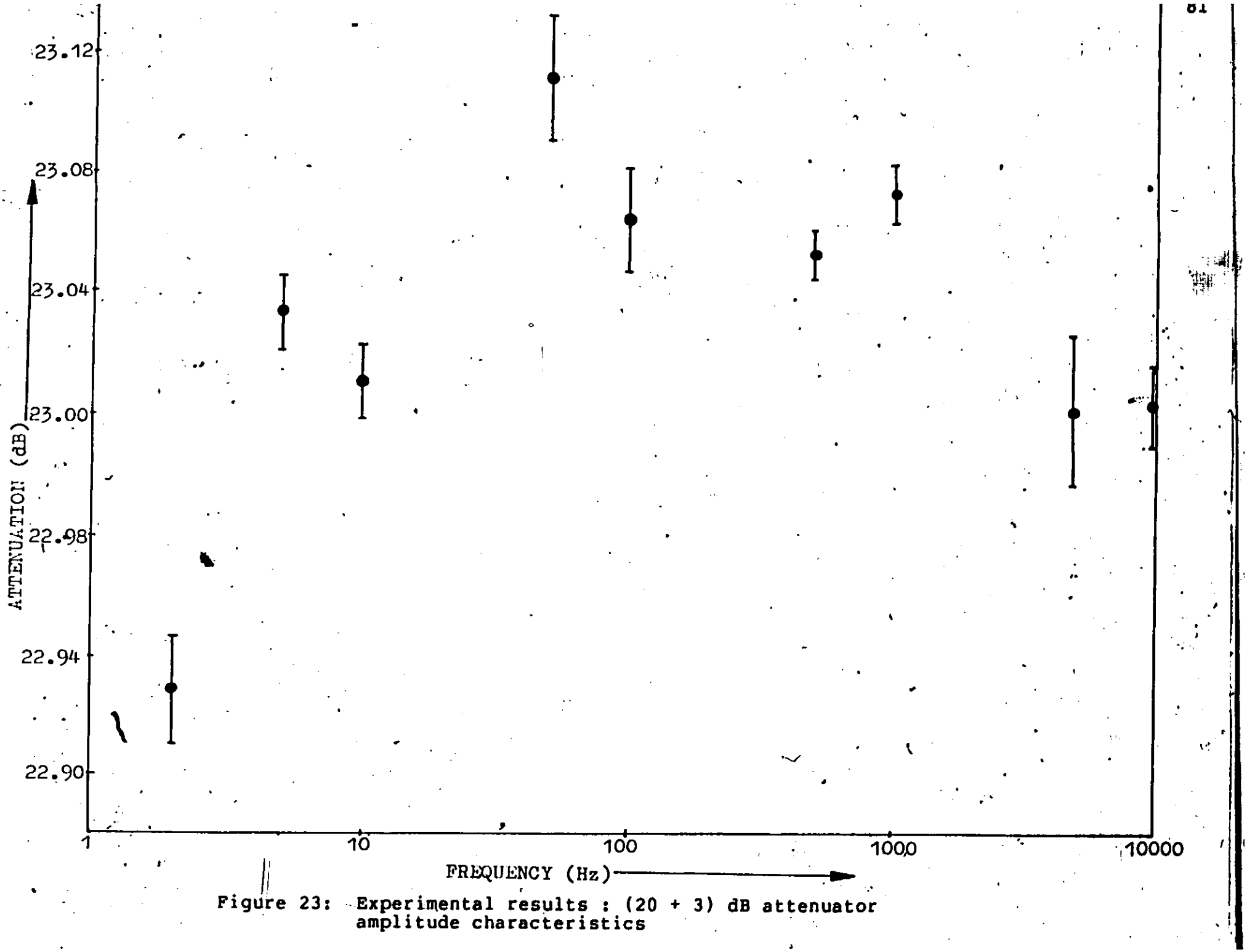


Figure 23: Experimental results : (20 + 3) dB attenuator amplitude characteristics

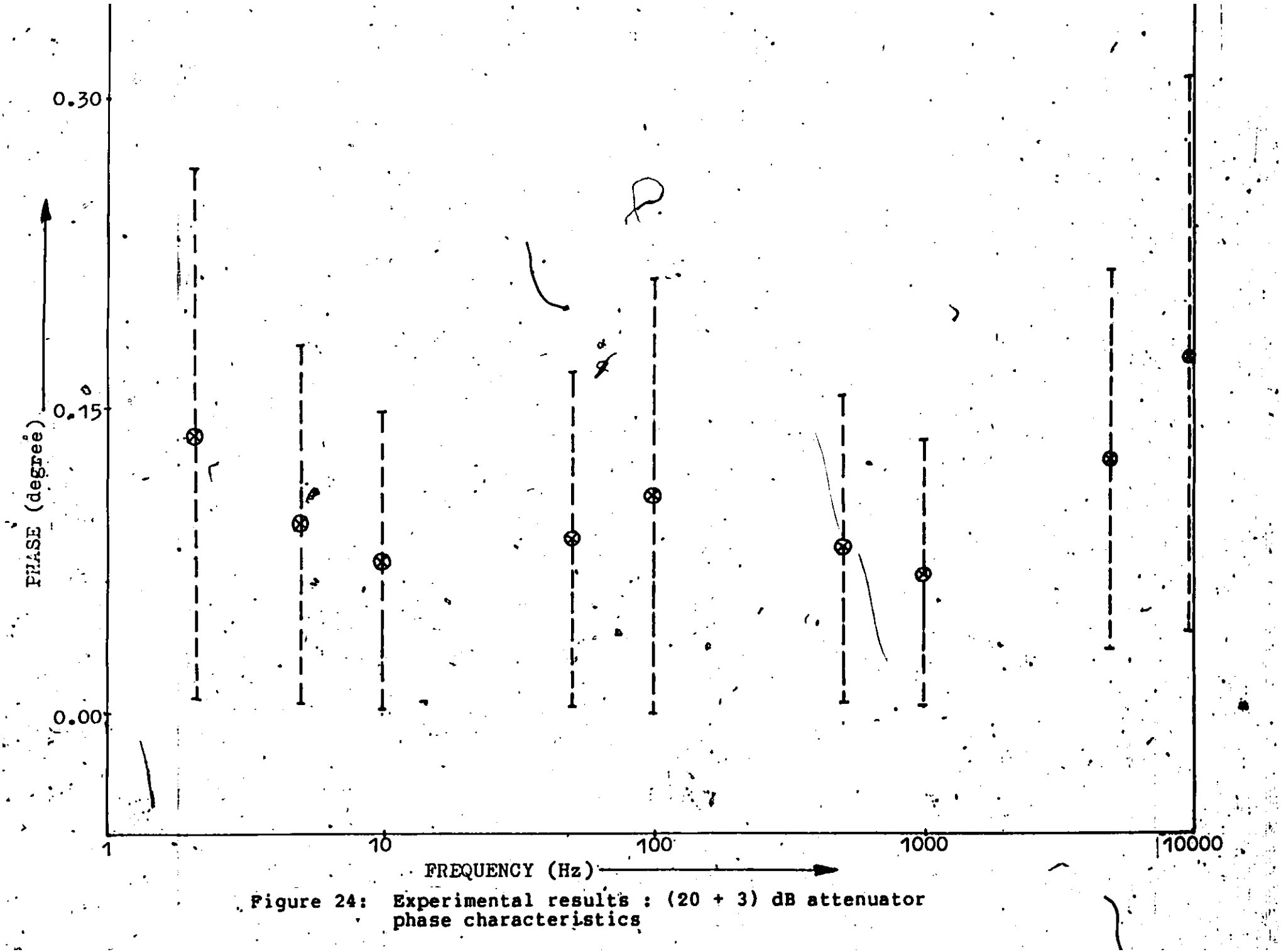


Figure 24: Experimental results : (20 + 3) dB attenuator phase characteristics

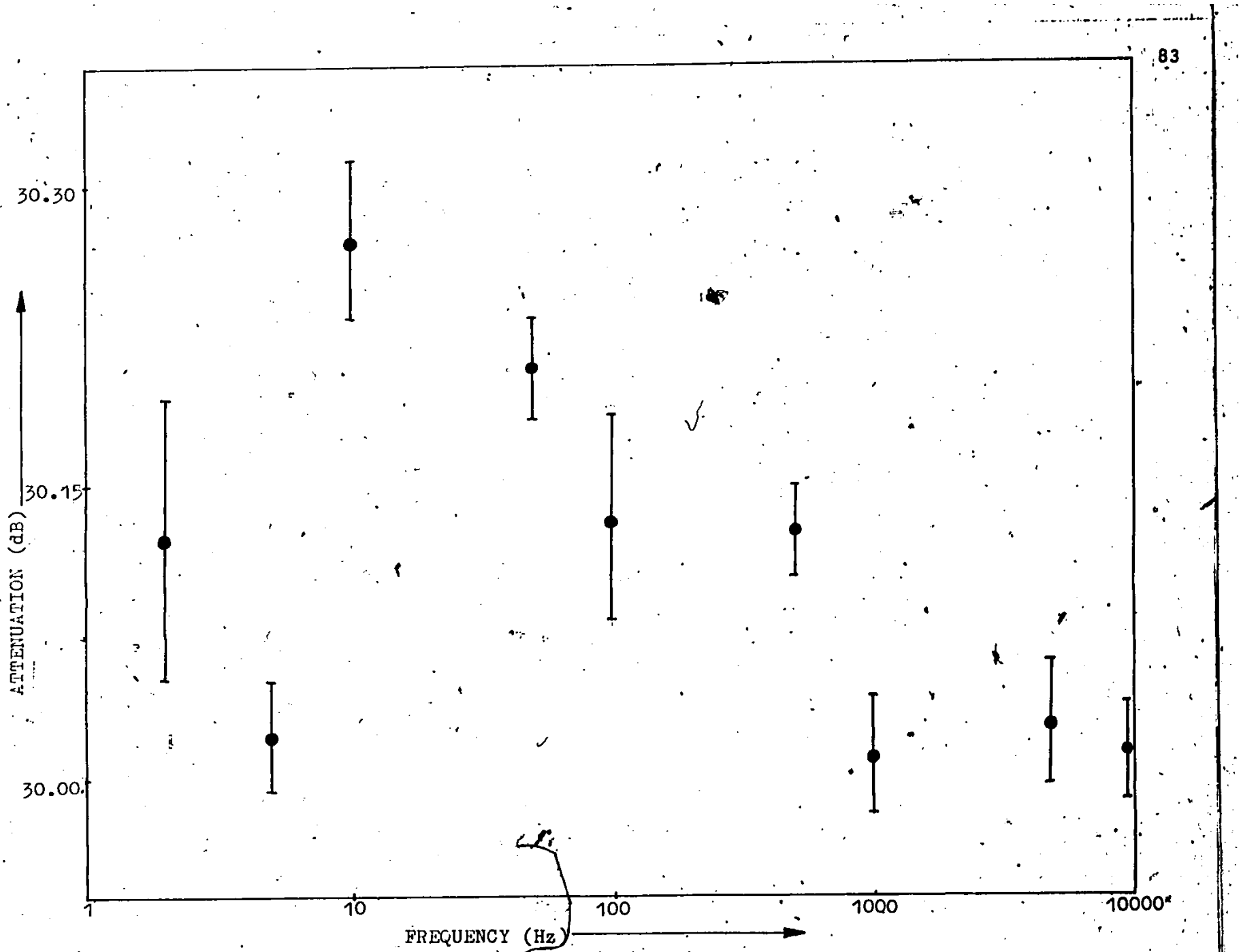


Figure 25: Experimental results : (20 + 10) dB attenuator amplitude characteristics

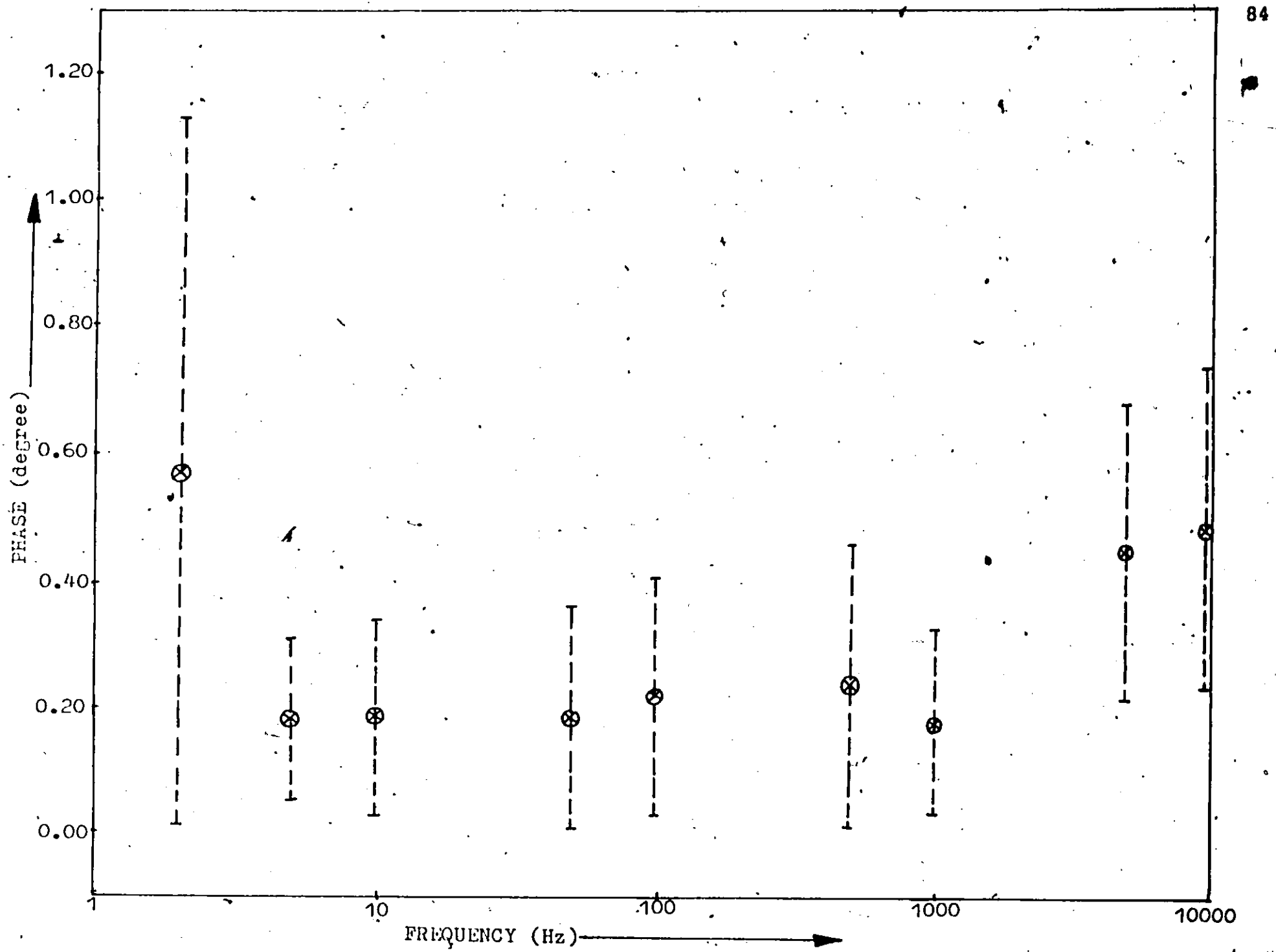


Figure 26: Experimental results : (20 + 10) dB attenuator phase characteristics

TABLE 11

Measured attenuator characteristics over the frequency range of 1 Hz to 12 kHz

ATTENUATOR	ATTENUATION		PHASE	
	MEAN	S.D.	MEAN	S.D.
3 dB	2.92856	0.0078	--	0.03379
10 dB	9.99430	0.0127	--	0.05247
13 dB	12.89060	0.0290	--	0.10101
20 dB	20.09650	0.0290	--	0.13789
23 dB	23.03400	0.0540	--	0.18174
30 dB	30.09940	0.0851	--	0.27843

The process of sine curve fitting to obtain the amplitude and the phase of a sinusoidal signal requires the samples to cover an integral number of periods of the signal. Since the sampling interface provides a fixed set of sampling rates, the above requirement is not satisfied for some of the frequency points. This causes the randomness of uncertainties in the measurements over the available frequency range.

Regarding the speed of measurement, there are two main sources of delay in the measurement procedure. The first one occurs during data acquisition, where the time required to obtain the samples is approximately 1 s for every 16 samples of reference and test signals. The second delay

TABLE 12

Experimental results of measurements on PAR amplifier

FREQUENCY	LOSS-FORWARD S21	
HZ	DB	ANG
1.099	-19.757	-0.49
2.000	-19.762	-0.36
3.000	-19.744	-0.23
4.000	-19.752	-0.29
5.000	-19.807	-0.30
6.000	-19.796	-0.20
7.001	-19.796	-0.16
8.000	-19.796	0.03
9.000	-19.811	-0.11
10.000	-19.797	-0.12
20.000	-19.777	-0.07
30.000	-19.789	-0.08
40.000	-19.796	0.03
50.000	-19.789	0.02
60.000	-19.776	0.13
70.005	-19.779	0.15
80.000	-19.799	-0.01
90.000	-19.813	-0.02
100.000	-19.782	0.00
200.000	-19.774	0.07
300.000	-19.826	0.03
400.000	-19.814	0.15
500.000	-19.807	0.28
600.000	-19.784	0.13
700.730	-19.777	0.21
800.000	-19.785	0.23
897.196	-19.819	0.40
1000.000	-19.769	0.33
2000.000	-19.765	0.36
3000.000	-19.759	0.89
4000.000	-19.745	1.46
4800.000	-19.774	1.65
6000.000	-19.781	2.09
6857.143	-19.776	2.29
8000.000	-19.784	2.96
9600.000	-19.766	3.27
12000.000	-19.795	4.16
16000.000	-19.816	5.57
24000.000	-19.842	7.69

appears during the sine curve fitting portion of data processing software. This delay is also proportional to the number of samples and it is approximately 1.5 s for every 16 samples of the two signals. This is caused by the trigonometric calculations to estimate the amplitude and the phase from the digital samples.

The system can fully characterize one device at 10 frequency points in less than an hour, and each subsequent device can be characterized in less than 30 minutes, provided the same frequency points are maintained. The speed is about one-eighth of the speed of the analog automatic network analyzer for measurements at microwave frequencies.

Chapter VII

CONCLUSIONS AND RECOMMENDATIONS

In this chapter, some recommendations for further improvement and future work are given. It also contains a summary of the work already completed.

7.1 RECOMMENDATIONS FOR FUTURE WORK :

The improvements enumerated in this section involve both hardware and software modifications. These changes should solve some of the problems present in the existing system.

The most thoroughgoing modification recommended is a new design altogether. It involves the replacing of PDP 11/34 by a microcomputer. Since the work performed by PDP 11/34 involves system control and data processing, using a microprocessor to do the job will lead to a stand alone system which should be the ultimate configuration for this kind of measurement system. Use of available hardware arithmetic logic units as slave processors for data processing will make that implementation as fast as the present one. Moreover, the software can be implemented on the microprocessor already used in the Synthesizer/detector interface.

The accuracy of the system can be further improved by using the analog-to-digital converters with higher bit resolution. This would also lower the sampling rate requirements (simulation results, Table4), and increase the measurement frequency range of the system.

Another improvement of the present system would involve design of a new digital frequency synthesizer. Since, the present configuration generates only two frequency points between 10 kHz to 20 kHz, a new synthesizer design should aim at covering this frequency range thoroughly so as to produce a system for measurement from 1Hz to 20 kHz.

The fourth hardware modification is the addition of a variable frequency low-pass filter for improving the signal purity of the synthesized waveform. With the provision of digital control of the filter, the interaction of the operator can be decreased and the system performance can be improved.

The changes recommended for software improvement include modification of the present routines for calibration with fixed standards to allow for calibration with variable standards. This will make possible, dielectric measurements of different materials with better accuracy.

Another software change could be the digital control of variable-gain preamplifier in the test channel. The amplifier characteristics at the frequencies provided by the synthesizer could be stored in the program and the system

can be made to switch the amplifier gain depending on the attenuation due to the device. This modification will improve the dynamic range of the system without degrading its accuracy.

Finally, the changes in the software to extend the calibration for 12-term error model will require addition of two routines and modification of two already included. The relations for the calculations are given in chapter one of this report. This modification will complete the spectrum of facilities which should be provided by a network analyzer.

7.2 SUMMARY AND CONCLUSIONS :

A new approach to the measurement of relative amplitude and phase, for vector network measurements, was investigated in this work. The need for accurate measurement of s-parameters arises from their use in monitoring dielectric properties of materials and biological substances. Measurement of s-parameters in 0 - 20 dB range can be made at low frequencies from 1 Hz to 24 kHz. This dynamic range can be increased by the addition of a calibrated attenuator/amplifier combination in the test channel.

This work reviews the network analysis technique for making vector network measurements. Some existing systems have been investigated and compared. A measurement procedure using digital signal processing has been

developed, and the realization of this procedure is described in terms of both hardware and software.

The procedure was analyzed for error limits by simulating the hardware configuration by means of its mathematical models. The study showed very good possibilities. To combine the cost and performance advantages, the error limit was chosen as ±0.015 dB in magnitude and ±0.1° in phase. The system parameters were specified theoretically from the simulation study.

The above design has been implemented and all of the software required to perform the functions of human interface, data acquisition, data processing and data output has been developed and documented. Some illustrative measurements and tests have been done and the results and system performance have been analyzed.

The inaccuracies in magnitude and phase measurements are of the order of ±0.02 dB and ±0.2° respectively. This can be further improved by increasing the resolution of analog-to-digital converters to 14 or 16 bits as shown by the simulation results.

Recommendations for future work based on these results and performance evaluations have been made. A clear definition of the work performed by the minicomputer shows the possibility of replacing it by a microprocessor. Due to the complex data processing requirements, a need for arithmetic slave processor in that system is envisaged.

Certain difficulties which were encountered have been mentioned and are hardware oriented. Some of the solutions proposed should be implemented in order to minimize these problems.

Now that the feasibility of using digital signal processing in network analysis has been demonstrated, implementation of the proposed recommendations could prove to yield better efficiency in terms of space, cost, accuracy, and versatility than many of the presently available systems. The main features of such a system would include a microprocessor with arithmetic slave unit controlling the whole system, computer-control of amplifier circuits and other hardware modifications suggested in the previous section.

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