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GaN Class-F Power Amplifier for UMTS/WCDMA Applications

Farzana Noor Khan

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in partial fulfillment to the thesis requirement for the degree of

MASTER OF APPLIED SCIENCE

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Abstract

The importance of wireless communications in today's telecommunications industry is indubitable. Wireless technologies are used in almost every aspect of our everyday life. Universal Mobile Telecommunications System (UMTS) technology has already implemented 3G communication standard for mobile communications.

Power amplifiers are the most power consuming unit in wireless communication systems. The power amplifiers used in UMTS devices need to be highly efficient. Improved efficiency not only extends the battery life but also reduces the DC power consumption, transmitter size and weight. Although the power amplifiers used in existing second generation GSM (Global System for Mobile Communications) transmitters are highly efficient, they cannot be applied to UMTS/WCDMA since GSM uses the constant envelope feature of GMSK (Gaussian Minimum Shift Keying) modulation which introduces phase variations only. In UMTS, a WCDMA system with QPSK modulation is used where both phase and amplitude variations are introduced by the modulation. The power amplifiers designed for WCDMA need to satisfy the contradicting operation requirement between linearity and efficiency.

In this thesis, a highly efficient class F power amplifier has been designed for WCDMA band with a center frequency of 2.14 GHz and bandwidth of 5 MHz using GaN transistor. The amplifier has been simulated using a high frequency circuit simulator namely, the Agilent Advanced Design System (ADS). The simulated results have shown a Power Added Efficiency (PAE) of 76.8% for an optimum input power of 30 dBm. The amplifier was then fabricated and measured. Measurement has shown a PAE of 75.9% for an optimum input power of 29.6 dBm which is in good accordance with the simulated results. Based on a literature review, and to the best of our knowledge, our circuit exhibited one of the highest measured PAE for a GaN class-F amplifier working at 2.14 GHz. The value of third and fifth order IM products of the designed class F PA is -13 dBc and -21 dBc respectively at peak power and -28.5 dBc and -43 dBc respectively at 6 dB back-off from peak power.

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Chapter 1 Introduction

1.1 Motivation

The importance of wireless communications in today's telecommunications industry is indubitable. Wireless technologies are used in almost every aspect of our everyday life. The practical application where wireless technology is being used includes industrial production line, security system, medical technology, automated highway systems, television remote control, cellular phones, smart homes and appliances, video conferencing and distant learning etc. Mobile communications which is the most attractive and highest emerged application of wireless communication play a very important role in the social, commercial, business and public safety sectors all over the world. It enables communication with a person at any time, any place and any form such as voice, text, video and so on. The need for efficient and secure technologies is becoming increasingly important with the enhanced usage of wireless technology. To accommodate the growing demands of high speed data transfer and multimedia applications third generation (3G) standards proposed in IMT-2000 (International Mobile Telecommunications-2000) started evolving in 2003 [1]. 3G provides the ability to transfer both voice and non-voice data and thus have become prominent for high data rate communication [2].Universal Mobile Telecommunications System (UMTS) technology has already implemented 3G communication standard for mobile communications which offers a potential worldwide coverage [3, 4]. The frequency range of operation for UMTS is close to 2 GHz and the technology adopted is WCDMA (Wideband Code Division Multiple Access). The bandwidth of WCDMA is 5 MHz which is 4 times larger than the conventional CDMA [5].

Typically UMTS devices are expected to deliver faster transmission of voice, video and multimedia applications of up to 2.4 Mbps (384 kbps for mobile systems and 2 Mbps for stationary systems) [1]. The modulation scheme used in UMTS is Quadrature Phase Shift Keying (QPSK) which provides higher bit rates per unit of bandwidth. In QPSK,

both amplitude and phase variations are introduced. High data rates demand a linear power amplifier output from the transmitter [5].

The power amplifiers used in UMTS devices need to be highly efficient since they are the key determining factors of battery life. Improved efficiency not only extends the battery life but also reduces the transmitter size and weight. Increasing efficiency helps reducing the DC power consumption. As a result, higher output power can be obtained for the same dissipation. Also, high efficiency makes it possible to reduce the operational costs. Although the power amplifiers for existing second generation GSM (Global System for Mobile Communications) transmitters are highly efficient, they cannot be applied to UMTS/WCDMA since GSM uses the constant envelope feature of GMSK (Gaussian Minimum Shift Keying) modulation which introduces phase variations only [5]. In UMTS, a WCDMA system with QPSK modulation is used. Because of the variation in amplitude a linear output is required from the transmitter. Class A amplifiers are highly linear but have a very low efficiency (typically 10-35%) [5]. The power amplifiers designed for WCDMA need to satisfy the contradicting operation requirement between linearity and efficiency.

In this thesis, a high efficient power amplifier has been designed using a commercial GaN transistor i.e., the CGH40010F from Cree Inc[1]. The class-F amplifier has been simulated using a high frequency circuit simulator namely, ADS[2]. The motivation of this work has to come from the growing interest in using GaN transistors to design power amplifiers for wireless applications. Si LDMOSFETs are widely used for modern base station power amplifiers. But above 3 GHz, their usefulness is hampered due to high parasitic capacitance. Also, they require complex linearization scheme to meet linearity, efficiency and output power specifications. [6]. Gallium arsenide (GaAs), indium phosphide (InP) and silicon germanium amplifiers exhibit high frequency operation but their usefulness is limited to primarily the low power, low voltage regimes [6]. As a result, GaN has recently seen an increase in international attention. GaN belongs to the family of wide bandgap semiconductors such as silicon carbide (SiC) and diamond and they have the ability to support high supply voltage resulting into high efficiency and

[1] www.cree.com
[2] Advanced Design System, Agilent Technologies, Palo Alto, CA

high power generation [6]. Since relatively less work has been done on GaN power amplifiers, it will be interesting to see how the power added efficiency and output power differ for these kinds of amplifiers than the ones using conventional Silicon MOSFETS and GaAs or InP HEMTs.

1.2 Contribution Overview

- In this thesis a class-F power amplifier has been designed and simulated for WCDMA band with a center frequency of 2.14 GHz and bandwidth of 5 MHz using a GaN HEMT from Cree Inc. Several important parameters such as power added efficiency; transducer power gain and third order intermodulation distortion have been examined to assess the efficiency and linearity performance of the power amplifier.
- The measured PAE was about 75.9% which is one of the highest measured PAE for GaN class-F amplifiers working at 2.14 GHz.
- One conference paper has been submitted [49] and another one will be shortly submitted in an international IEEE conference.

1.3 Thesis outline

The thesis is organized as follows:

Chapter 2 discusses the fundamentals of power amplifier design and the different kinds of power amplifiers. Based on our specific design criteria (high power added efficiency), class-F amplifier configuration was retained. Therefore, theoretical concepts of class-F amplifiers are introduced in Chapter 3. Since GaN transistors have the ability to support high supply voltage resulting into high efficiency, Chapter 4 discusses about GaN-based power transistors while Chapter 5 explains the operation of class F power amplifiers and as well as underlying design concepts and simulated results. Measurements are presented in chapter 6. An inverse class-F amplifier was also simulated for

comparison. Chapter 7 Summarizes the work presented in this thesis and also outlines the main contribution of this thesis. An outline of future work is also presented.

Chapter 2 RF Power Amplifiers

2.1 Introduction

Radio frequency (RF) power amplifiers are nonlinear circuits used to amplify a relatively low power RF signal into a larger signal of significant power either at a specified frequency or within a frequency band. Such devices often used to drive the antennas of transmitters, should exhibit good gain, high efficiency and linearity. Moderate gain levels reduce circuit's complexity since in this case the number of amplifying stages is reduced. Improved efficiency extends battery life and reduces DC power consumption as well as operational cost. Power amplifiers are expected to have good linearity to prevent interference to adjacent channels e.g., to keep Adjacent Channel Power Ratio (ACPR) low [5, 6].

An RF power amplifier typically includes an active device, usually a transistor, and two passive matching networks, one at the input and the other one at the output as shown in Figure 2.1 [7]. The active device amplifies the AC input signal. The input matching network is necessary to ensure maximum power transfer to the active device whereas the output matching network ensures a maximum power transfer to the amplifier load.

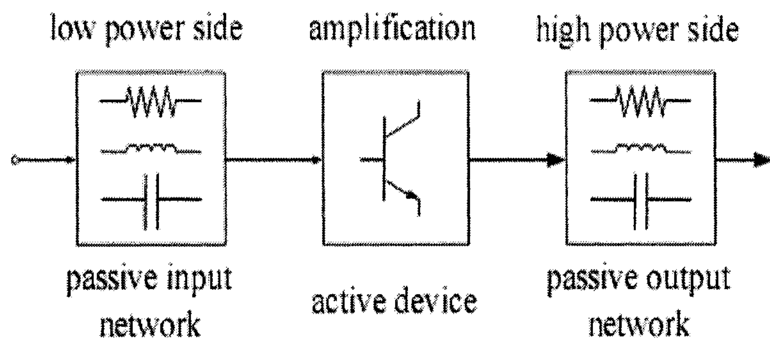


Fig 2.1: Signal flow of a single stage power amplifier (PA) [7]

2.2 Power and Gain

The schematic of a simple PA is shown in Figure 2.2 [7].

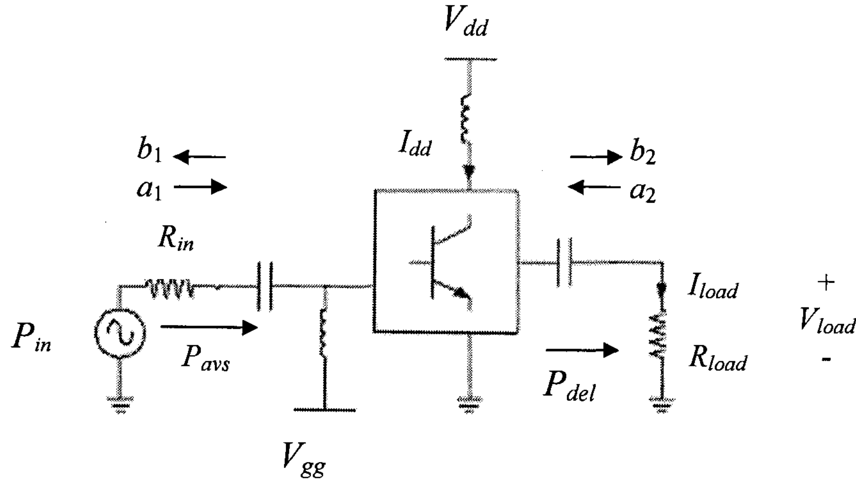


Fig 2.2: Schematic of a simple PA [7]

The power delivered to the load is the difference between the incident and reflected power as shown in the following equation [8].

$$P_{del} = \frac{1}{2}|b_2|^2 - \frac{1}{2}|a_2|^2 = \frac{1}{2}|b_2|^2\left(1 - |\Gamma_L|^2\right) \tag{2.1}$$

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.2}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.3}$$

a_k and b_k are defined as the incident and reflected waves of port k respectively. Γ_L is the reflection coefficient at the load and the S_{ij} are the elements of the scattering matrix (i, j = 1, 2). The power available from a source (of reflection coefficient Γ_S) is the power delivered by a source to the conjugately matched load, which is,

$$\Gamma_L = \Gamma^*_S$$

Thus the power available from the source is [8]

$$P_{avs} = \frac{1}{2}\left|b_1^*\right|^2 - \frac{1}{2}\left|a_1^*\right|^2 = \frac{\frac{1}{2}\left|b_1\right|^2}{\left(1-\left|\Gamma_S\right|^2\right)} \quad (2.4)$$

The input power of the transistor is given by [8]

$$P_{in} = \frac{1}{2}\left|a_1\right|^2 - \frac{1}{2}\left|b_1\right|^2 = \frac{1}{2}\left|a_1\right|^2\left(1-\left|\Gamma_1\right|^2\right) \quad (2.5)$$

The transducer power gain (G_T) of an amplifier is defined as the ratio of the power delivered to the load to the available power from the source which is given by

$$G_T = \frac{P_{del}}{P_{avs}} \quad (2.6)$$

The power gain (G_p) is defined as the ratio of the power P_L delivered to the load resistance to the network's input power (P_1).

$$G_p = \frac{P_{del}}{P_{in}} \quad (2.7)$$

2.3 Noise Figure

The noise figure is a measure of degradation of the signal to noise ratio. It is the decibel representation of the noise factor and its expression is given below [9].

$$NF = 10 * \log\left(\frac{\frac{Signal_{in}}{Noise_{in}}}{\frac{Signal_{out}}{Noise_{out}}}\right) \quad (2.8)$$

In wireless high frequency transmissions, it is common to observe noisy input signals. Increasing the output signal-to-noise ratio (maintaining a low noise figure) is a very important target in such frequencies.

2.4 Stability and Matching

Stability is a fundamental consideration in designing an amplifier. In other words, we have to make sure that the active device is stable, i.e., does not generate oscillation. The Rollet factor or stability factor of a transistor is defined from the following equation [8]

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \qquad (2.9)$$

In order to make an amplifier stable the source and load impedances should have real positive parts which imply that the magnitudes of the reflection coefficients for the source ($|\Gamma_S|$) and the load ($|\Gamma_L|$) should be less than 1. If,

$K > 1$, there will be two solutions of $|\Gamma_S|$ and $|\Gamma_L|$, one having a magnitude of greater than one and the one with a magnitude of less than unity [8].

If $K < -1$, the amplifier is unstable. It is required to match the input and the output of the amplifier simultaneously which is not possible [8].

If $-1 < K < 1$ the amplifier is conditionally stable and there are regions where oscillation will not occur [8].

$K=1$ is not practical since in this case both $|\Gamma_S|$ and $|\Gamma_L|$ are equal to 1 [8].

2.5 Power Added Efficiency (PAE)

Efficiency is a crucial parameter in the design of an amplifier since it is related to dc power consumption and operational cost [10].

Drain efficiency is the ratio of output RF power (P_{RFout}) to DC input power (P_{DC}):

$$\eta_D = \frac{P_{RFout}}{P_{DC}} \qquad (2.10)$$

Power added efficiency is defined as:

$$\text{PAE} = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \qquad (2.11)$$

PAE can also be written as:

$$\text{PAE} = \eta_D \left(1 - \frac{1}{G_p}\right) \qquad (2.12)$$

where G_p is the power gain [11].

2.6 Intercept Point

The Intercept point is a very important parameter to consider in designing an amplifier. As shown in Figure 2.3, it is a virtual point where the slopes of the fundamental and the 3rd order intermodulation product meet on a logarithmic chart of output power versus input power. In fact, in practical situations, the output power compresses before reaching this point and thus, the intercept point is measured by the extrapolation of the fundamental and the third order intermodulation output characteristics. The third order intermodulation products draw the most attention since they occur in the vicinity of fundamental tone [12] and the corresponding intercept point is known as third order intercept point (IP3). Intercept point is a better way of linearity measurement than intermodulation products since it can be specified independently of the input power level [13].

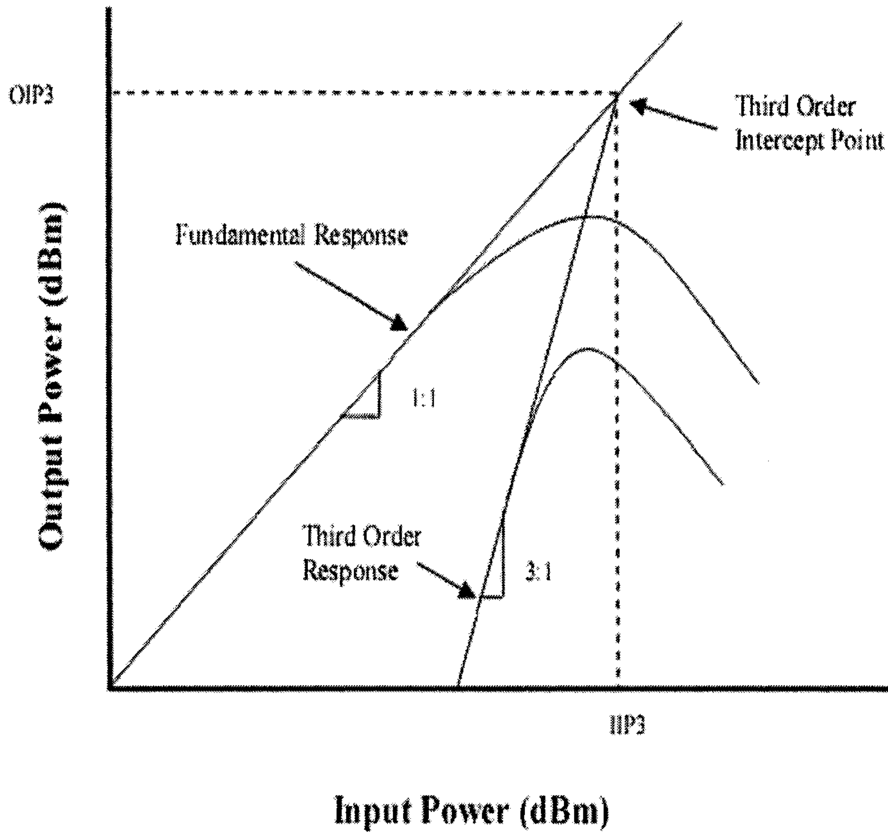


Fig 2.3: Third order intercept point [5]

2.7 Adjacent Channel Power Ratio (ACPR)

Adjacent channel power ratio is a critical aspect in designing power amplifiers. It is a measurement of the amount of interference or power in the adjacent frequency channel. It is the ratio of average power of the signal in the adjacent frequency channel to that in the transmitted frequency channel [14]. The leakage of power is mainly due to nonlinearities in the power amplifier (Figure 2.4).

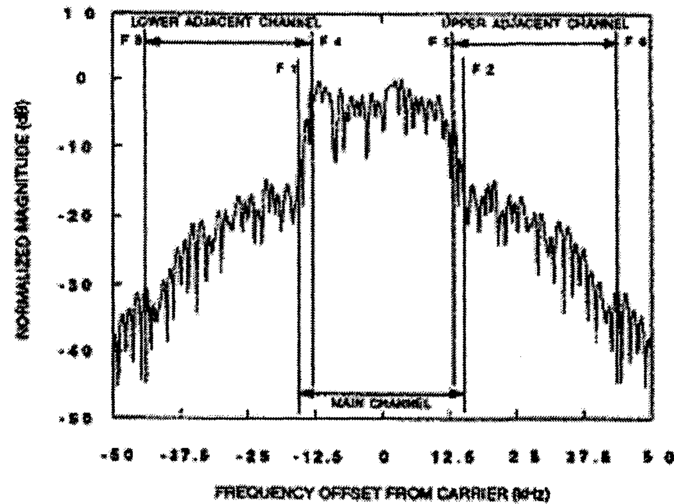


Fig 2.4: Adjacent channel power ratio [15]

2.8 1 dB Compression Point ($P_{1\text{-dB}}$)

The 1-dB compression point is a measure of the linear range of operation. When a power amplifier is operating in its linear region the gain is constant for a given frequency. But if the power of the input signal is increased, after a certain point the power of the output signal will decrease. As shown in Figure 2.5, the input 1-dB ($P_{1\text{-}dB}$) compression point on a P_{out} (output power) versus P_{in} (input power) graph refers to the point where an increase of the input signal causes the gain to drop by 1-dB. The corresponding output power is known as the output 1-dB compression point ($P_{1\text{-}dB,\ out}$) [12]. Once this point is reached there will be a rapid decrease in gain [16].

$$P_{1\text{-dB, out}} = P_{1\text{-dB}} + (\text{Gain} - 1)\ \text{dBm} \qquad (2.13)$$

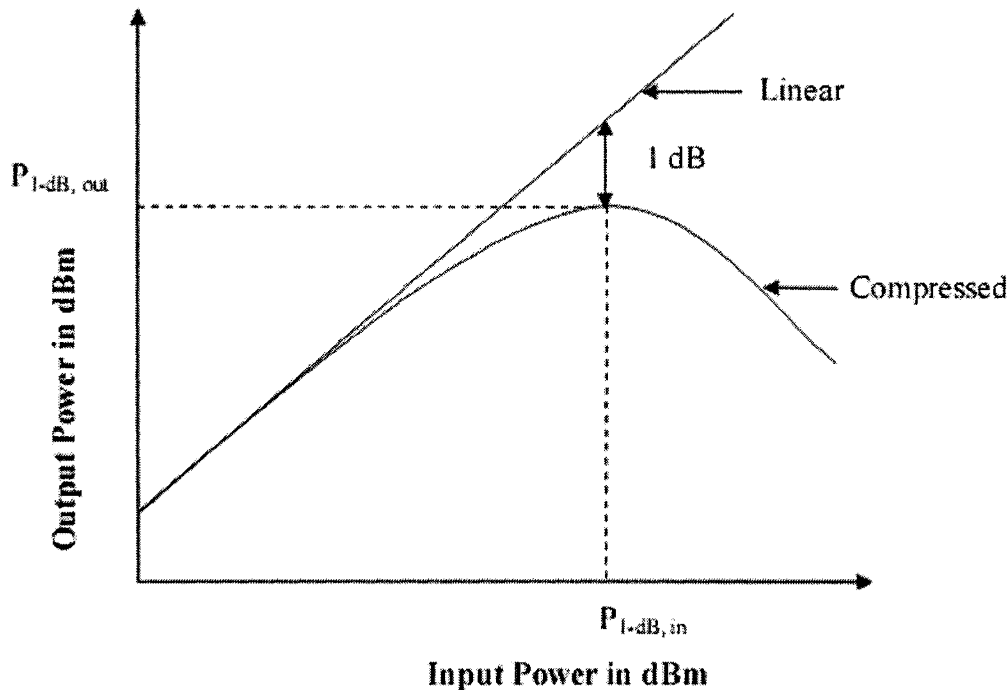


Fig 2.5: 1-dB compression point [5]

2.9 Intermodulation Distortion

Intermodulation products are caused by the non-linearity in the amplifier. Intermodulation distortion results when two or more non commensurate signals mix together and create additional non-harmonic frequencies. Third order intermodulation products are of biggest concern due to their highest strength. Additionally, it is difficult to filter them out since they appear at the vicinity of the fundamental tone [5]. Intermodulation products are particularly measured by two-tone test as analysis several stimulus tones can be very complex. In a two-tone test, the nonlinear circuit is excited with two sinusoidal signals of equal amplitude but of closely spaced frequencies. As a result, the output spectrum consists of various intermodulation products [12]. The frequencies of the intermodulation products are computed by the following equation [17]:

$$mf_1 \pm nf_2, \qquad \text{where } m, n = 0, 1, 2, 3...$$

The sum 'm+n' is called the order of the distortion product (Figure 2.6). The ratio of intermodulation to fundamental power is one way of measuring linearity [5].

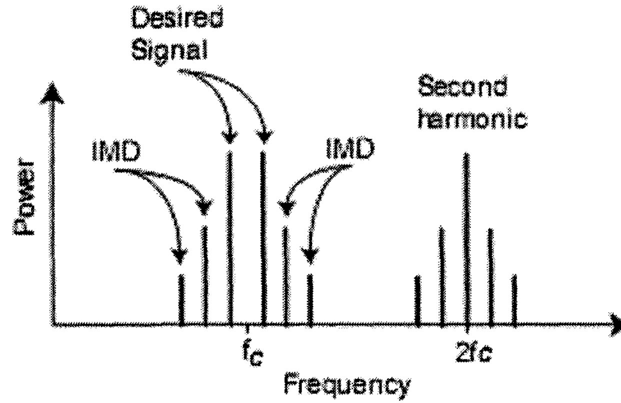


Fig 2.6: Intermodulation Distortion [18]

2.10 Power Output Capability

The power output capability of an amplifier can be expressed as [19]:

$$C_p = \frac{P_0}{I_{DM} V_M} = \frac{I_{DD} V_{DD}}{I_{DM} V_M} \tag{2.14}$$

Where P_0 is the dc power supply, I_{DM} is the peak value of the drain current and V_M is the peak value of the drain-to-source voltage. If there are N transistors then the equation becomes

$$C_p = \frac{P_0}{N I_{DM} V_M} = \frac{I_{DD} V_{DD}}{N I_{DM} V_M} \tag{2.15}$$

Class A amplifiers are conducted at the centre of the load line which allows maximum swing of voltage and current. For this reason, class A amplifiers have the highest power output capability [5].

2.11 Amplifier Classifications

There are several types of power amplifiers which are distinguished primarily by class of operation. Generally, power amplifiers are divided into two groups: linear and nonlinear power amplifiers. Nonlinear power amplifiers are also known as switching mode amplifiers. In linear amplifiers, the active device acts as a current source whereas it acts as a switch in case of nonlinear amplifiers [20]. Class A power amplifiers are known as linear power amplifiers, while class B and AB amplifiers are known as quasi-linear (weakly nonlinear) power amplifiers. On the other hand, class C, D, E and F amplifiers are nonlinear amplifiers. Although the later amplifiers exhibit nonlinear performances, they can achieve higher efficiency. Brief discussions of different classes of power amplifiers are presented in the next subsections.

2.11.1 Class A

Class A amplifier is the simplest and basic form of all power amplifiers. In comparison to other classes, class A has the maximum linearity [21]. For class A amplifier, the transistor is biased at the midpoint of linear region providing maximum voltage and current swings without cut-off and saturation (Figure 2.7). The conduction angle for class A amplifier is 360°. Here, a sinusoidal input signal produces a sinusoidal output current (Figure 2.8).

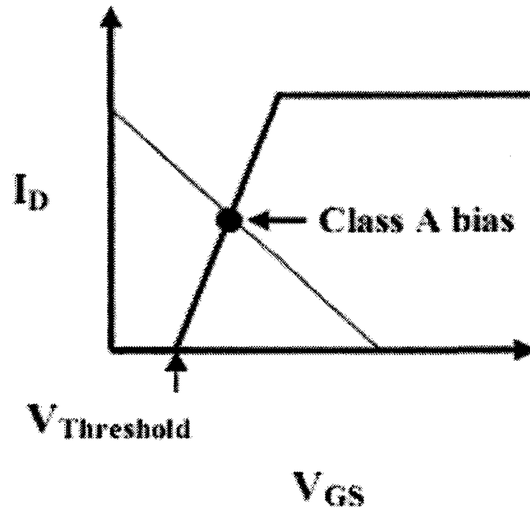


Fig 2.7: Biasing of class A amplifier [5]

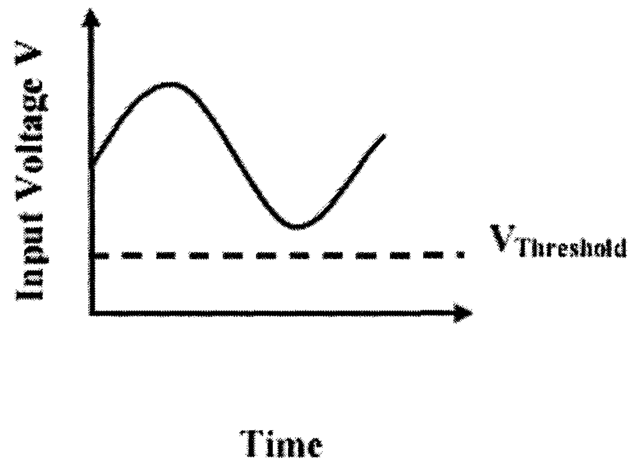


Fig 2.8: Input signal for class A amplifier [5]

Although class A amplifier has highest linearity, its efficiency is relatively poor. The reason behind this is that the transistor is always in active region. As a result, it constantly draws current which results into power loss. Theoretically, the maximum achievable efficiency of class A amplifier is 50%. However, it becomes as low as 20% for commercial class A amplifiers [5, 18].

2.11.2 Class B

The conduction angle of class B amplifiers is 180° which means that the device remains off during half period of the input cycle (Figures 2.9 and 2.10). In this case, the transistor is biased at its threshold voltage point. Sometimes, class B amplifiers are implemented using push-pull configuration where two transistors are used in parallel. The two transistors are driven 180° out of phase so that each of them remains active for half of the input cycle and turned off during the other half. As a result, it becomes possible to attain large saving in power loss.

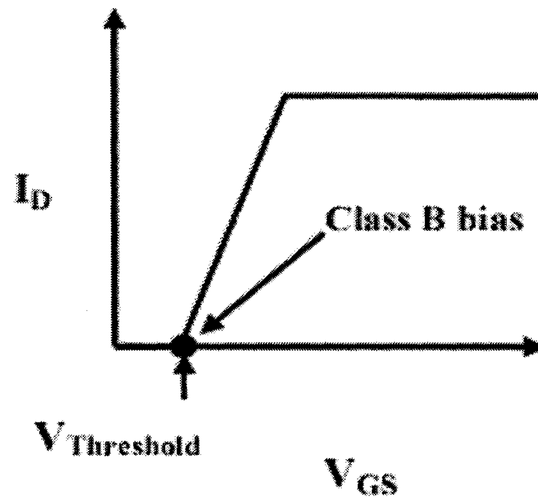


Fig 2.9: Biasing of class B amplifier [5]

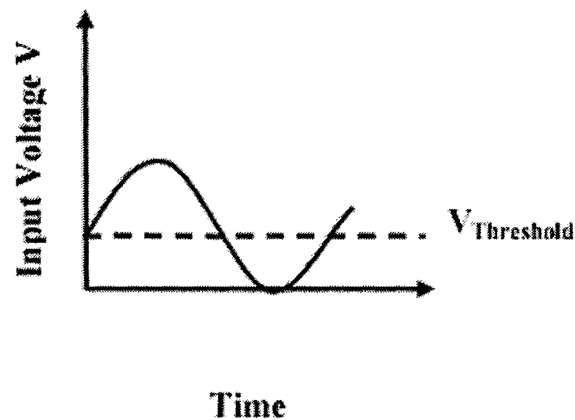


Fig 2.10: Input signal for class B amplifier [5]

Theoretically, the maximum achievable efficiency with class B mode is 78.5% which becomes 50-60% for commercial class-B amplifiers [5, 18].

2.11.3 Class AB

The operation of class AB is a compromise between class A and class B. In this case, the conduction angle is greater than π but less than 2π. Here, the transistor is biased above the threshold voltage but below the midpoint of the load line (Figure 2.11 and 2.12). In practice, one can choose the bias point depending on the linearity and efficiency requirement. The cross-over distortion effect of class B amplifiers gets minimized since the biasing produces small quiescent drain current [5]. As a result, the linearity improves. The linearity of class AB amplifiers is close to class A.

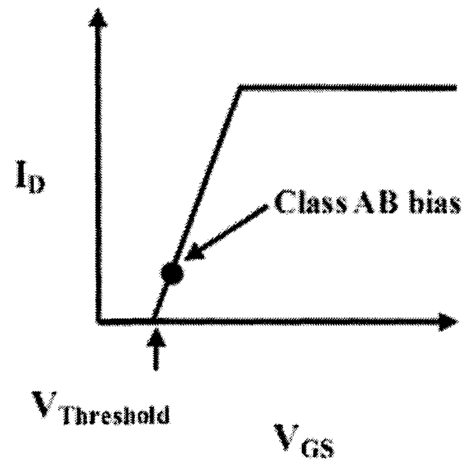


Fig 2.11: Biasing of class AB amplifier [5]

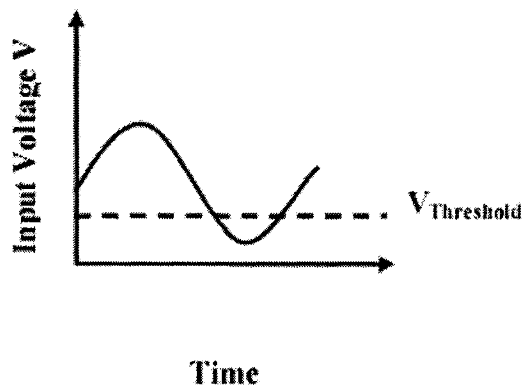


Fig 2.12: Input signal for class AB amplifier [5]

Class AB amplifiers are more efficient than class A amplifiers. Theoretically, the maximum achievable efficiency of class AB amplifiers is between 50% and 78.5%. However, commercial class AB amplifiers have 40-55% efficiency [5].

2.11.4 Class C

In class C amplifiers, the transistor is biased below threshold so that the output current is zero for more than half of the input cycle (Figure 2.13 and 2.14). Since the transistor is on for less than one half period, the efficiency increases. However, linearity is worst for class C amplifiers.

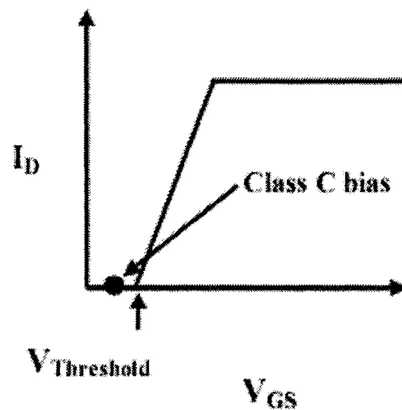


Fig 2.13: Biasing of class C amplifier [5]

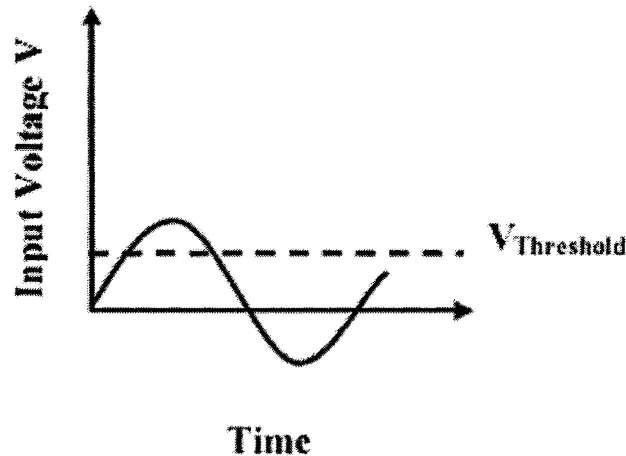


Fig 2.14: Input signal for class C amplifier [5]

Theoretically, the maximum achievable efficiency with class C operation is 100% [5]. However, this is only possible if the conduction angle is 0° which means there is no output power as no current flows through load. But this condition is useless. However, for example, if the conduction angle is 150° the PAE becomes 85% [22]. The efficiency of commercial class C amplifiers is 60% or more [5].

2.11.5 Class E

Class E is a switching mode high efficiency amplifier. In this case, the transistor acts as a switch (Figure 2.15).

The idea behind the Class E amplifier is that the output voltage and current waveforms do not overlap and the values of the voltage, current, and the derivative of the voltage with respect to time are limited during the transition between non-zero currents and non-zero voltages.

The transistor is stated as "on" when it starts conducting and "off" when it stops conducting. The power dissipation is reduced since the voltage across the transistor returns to zero just before it turns "on" and the current through the transistor returns to zero

just before it turns "off". As a result there is no overlapping of substantial voltage and current during the transitions.

Furthermore, the current through the transistor at the beginning of "on" state is zero as the voltage across the switch returns to zero with zero slope. Similarly the current through the transistor at the beginning of "off" state is zero as the voltage across the transistor returns to zero with zero slope. Theoretically, the maximum achievable efficiency of Class E amplifiers is 100%. However the efficiency of commercial class E amplifiers is around 60% [5].

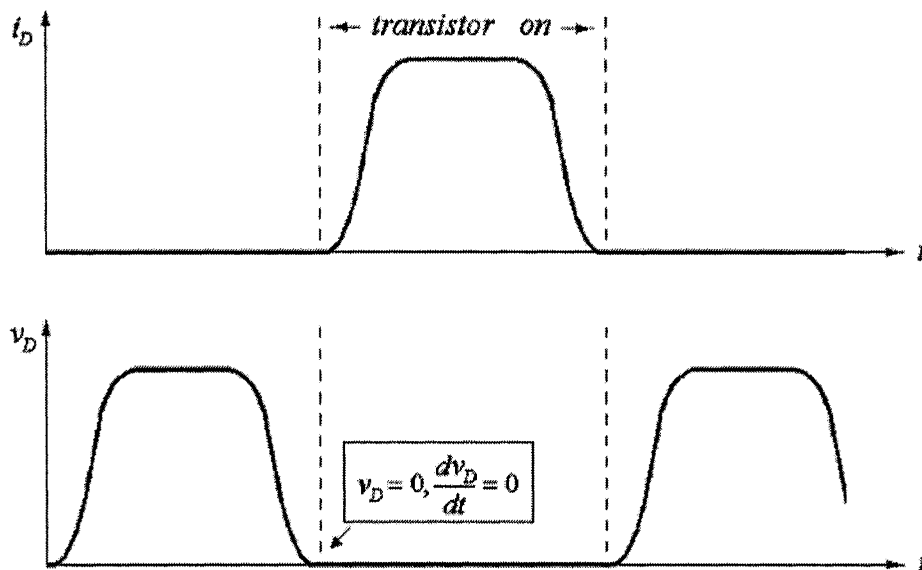


Fig 2.15: Waveforms of class E amplifier [23]

2.11.6 Class F and Inverse Class F

Class F amplifier is one of the techniques to improve efficiency. The main idea behind class F operation is to use a harmonic resonator in the output network to shape the

output current and voltage waveforms. The current waveform is half-sinusoidal whereas the voltage waveform appears to be square-wave (Figure 2.16).

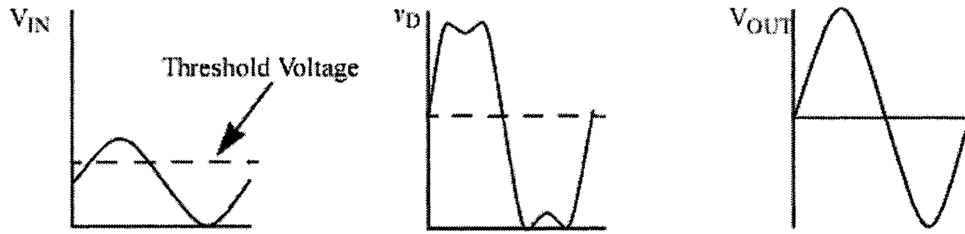


Fig 2.16: Waveforms of class F amplifier [24]

Theoretically, the maximum achievable efficiency of class F amplifiers is 100% although in practice it becomes less due to parasitic effects. Also, the high efficiency is associated with poor linearity. If the linearity is improved efficiency degrades.

On the other hand in inverse class-F amplifiers, the waveforms are interchanged requiring the opposite harmonic terminations. Here, the drain current is square wave and the drain voltage is a half sine wave. With an increased number of harmonic terminations, the efficiency of an inverse class F amplifier increases from 70% to 90%, and ideally to 100% [25].

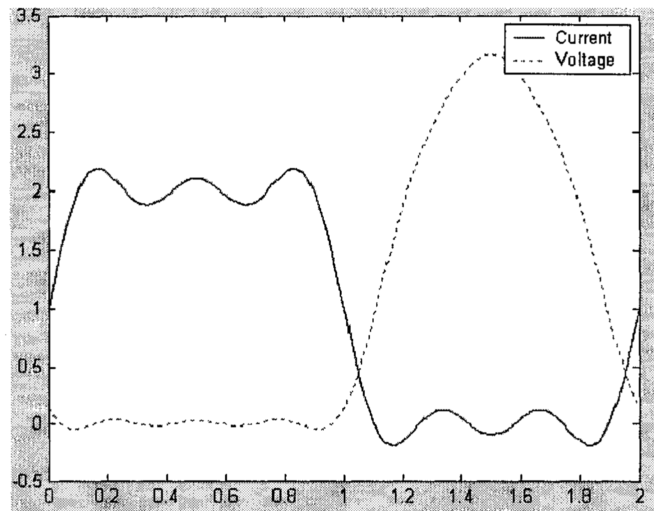


Fig 2.17: Voltage and current waveforms of inverse class F amplifier with 5 harmonics [25]

2.12 Conclusion

There are some other classes of amplifiers such as class D, class S, class G, class H, as well as Doherty and Chireix amplifiers. Since our specific design criteria is based on a high power added efficiency, class-F amplifier configuration is retained. Therefore, theoretical concepts of class-F amplifiers will be introduced in the next chapter. A brief comparison of the classes discussed in this chapter is given in Table 2.1.

Table 2.1 Comparison between Different Classes of operation in Power Amplifiers [25]

Class	A	B	AB	C	E	F	Inv F
Conduction angle	2π	π	π -2π	0-π	π	π -2 π	π-2 π
Linearity	Yes	Yes	Yes	No	No	No	No
Ideal efficiency (%)	50	78.5	50-78.5	~85	100	100	100

Chapter 3 Class-F Amplifier

3.1 Introduction

Class-F amplifiers are switching mode power amplifiers with higher efficiency. The main idea behind class F amplifiers is to control the harmonic contents of the drain voltage and current waveforms by several resonators. The resulting drain voltage of a class-F amplifier is square waves whereas the drain current is rectified sinusoids. When the current is high the voltage is low and vice versa which reduces the power dissipated by the device.

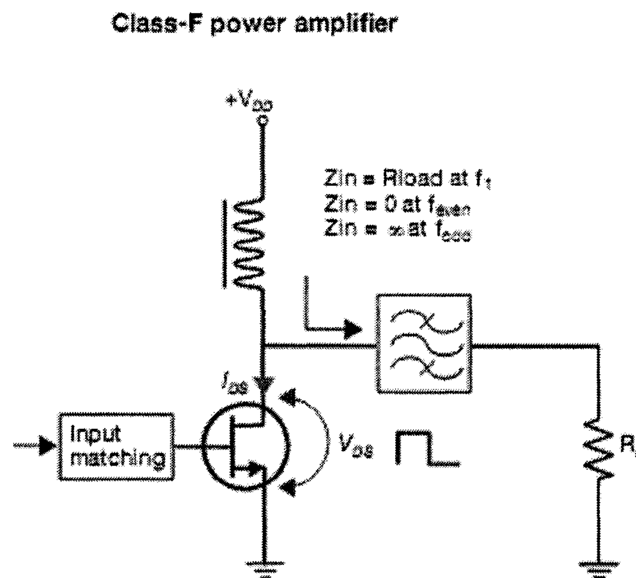


Fig 3.1: Basic class F amplifier topology [26]

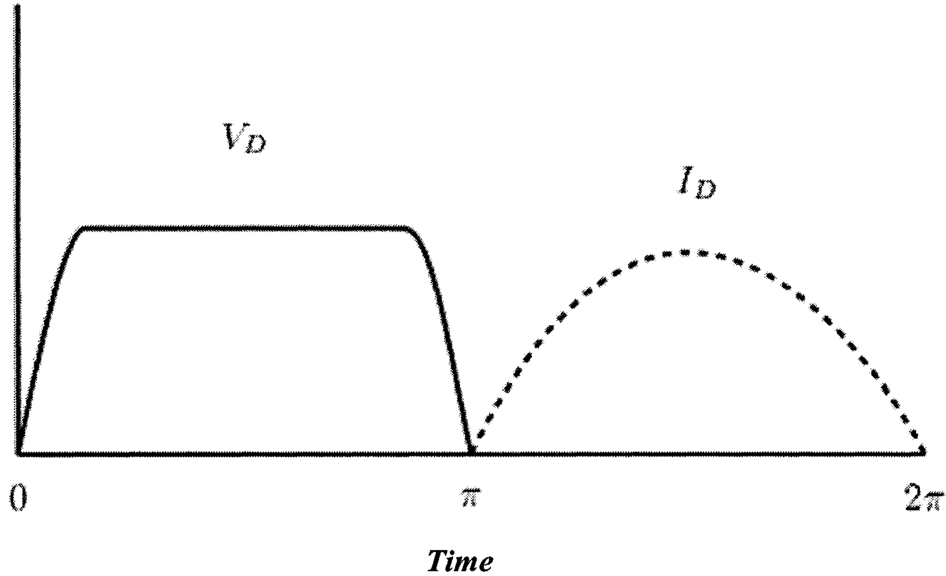


Fig 3.2: Ideal drain voltage and current waveforms of class-F amplifier [27]

3.2 Fundamentals of Class-F Amplifiers

Class-F amplifiers have higher output power, higher gain and improved efficiency which is achieved by proper harmonic terminations at the output. The idea of harmonic terminations was first introduced by Tyler [28]. Theoretically the drain voltage and current waveforms do not overlap in time and the PAE approaches 100%. In a class-F amplifier, a high impedance is presented to all odd harmonics whereas a low impedance is presented to all even harmonics. As a result, the square wave drain voltage contains only the fundamental and odd harmonics and the half sinusoid drain current contains the fundamental and all the even harmonics. The impedance conditions are summarized below:

$$Z_n = R_L = \frac{8}{\pi}\frac{V_{CC}}{I_s} \text{ for n=1}$$

$$Z_n = 0 \text{ for n =2,4,6.........} \qquad (3.1)$$

$$Z_n = \infty \text{ for odd n=3,5,7...........}$$

The ideal drain voltage and current waveform of class F amplifier can be expanded using Fourier series by the following equations respectively [29]:

$$i_D = I_{d,peak}\left(\frac{1}{\pi} + \frac{1}{2}\sin\omega_0 t - \frac{2}{\pi}\sum_{n=2,4,6....}\frac{1}{n^2-1}\cos n\omega_0 t\right) \tag{3.2}$$

$$v_D = V_{dc} - \frac{4.V_{dc}}{\pi}\sum_{n=1,3,5...}\frac{1}{n}\sin n\omega_0 t \tag{3.3}$$

In equations (3.2) and (3.3), V_{dc} and $\frac{I_{d,peak}}{\pi}$ are the DC voltage and Current respectively. The amplitude of the fundamental voltage is $V_{fund} = \frac{4.V_{dc}}{\pi}$ and the amplitude of the fundamental current is $I_{fund} = \frac{I_{d,peak}}{2}$.

The fundamental load impedance is given by:

$$Z_{fund} = \frac{V_{fund}}{I_{fund}} = \frac{8}{\pi}\frac{V_{dc}}{I_{d,peak}} \tag{3.4}$$

The expression of dc input power is:

$$P_{in}(dc) = \frac{V_{dc}.I_{d,peak}}{\pi} \tag{3.5}$$

While the fundamental output power can be expressed as:

$$P_{out}(RF) = \frac{I_{d,peak}}{2\sqrt{2}}.\frac{4.V_{dc}}{\pi\sqrt{2}} = \frac{I_{d,peak}V_{dc}}{\pi} \tag{3.6}$$

The efficiency of the amplifier is the ratio of the fundamental power delivered to the load and the DC power supplied to the transistor.

From equations (3.5) and (3.6) it is apparent that the DC power is equal to the fundamental power. Thus, for class F operation the efficiency becomes 100%. But in practice, it becomes less because of the power dissipated by the transistor. The power dissipated by the drain of the transistor is [30],

$$P_{diss} = \frac{1}{T}\int_0^T v_{DS}(t) * i_D(t)dt = P_{DC} - P_{out,f} - \sum_{n=2}^{\infty} P_{out,nf},$$

where

$$P_{out,nf} = \frac{1}{2} V_n * I_n * \cos(\theta) \tag{3.7}$$

Hence, the DC power delivered to the load can be expressed as:

$$P_{DC} = P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf} \tag{3.8}$$

Thus, the expression of efficiency becomes:

$$\eta = \frac{P_{out,f}}{P_{DC}} = \frac{P_{out,f}}{P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf}} \tag{3.9}$$

If the power dissipated by the transistor and the powers of the harmonics are minimized, the efficiency increases. The overlap between the drain voltage and current should be minimized to reduce the power dissipation. Furthermore, if the output matching network includes all the harmonics, the powers of the harmonics are reduced. But in practice, it is not possible to consider several harmonics since in that case the number of circuit elements required is infinite. So, only second and third harmonics are considered. So, the expression of the efficiency of the amplifier becomes:

$$\eta = \frac{P_{out,f}}{P_{DC}} = \frac{P_{out,f}}{P_{diss} + P_{out,f} + P_{out,2f} + P_{out,3f}} \tag{3.10}$$

The overlap between drain current and voltage makes the dissipated power greater than zero and the harmonic powers are also greater than zero. As a result, the 100% efficiency that was shown by theories degrades.

The zero power loss condition in Class F amplifiers is an ideal condition. It is practically achievable with only a transistor with zero saturation resistance (R_{ON}). But all practical transistors have a finite saturation resistance. As a result, there is a power loss and the efficiency is reduced. If two transistors are placed in parallel, the effect of saturation resistance is reduced but the output impedance is lowered and there are difficulties in output matching. It is possible to get better efficiency with a higher value of V_{dd} but there is a limit on this value because of the transistor's breakdown voltage [5].

3.3 Harmonics Control in Class-F Amplifier

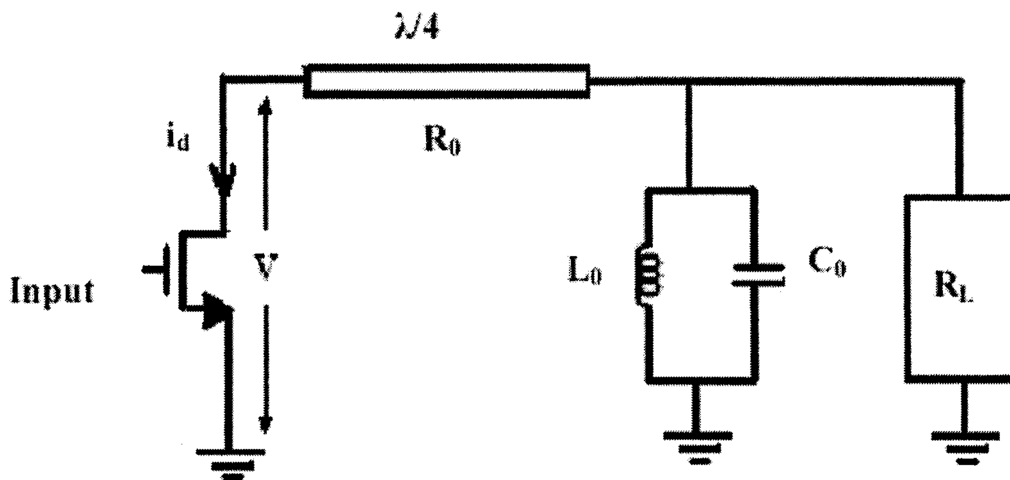


Fig 3.3: Output network of class F amplifier using quarter-wave transmission line [31]

Figure 3.3 shows the output network of a class F amplifier where a quarter-wave transmission line and a resonant tank circuit are used to achieve the desired drain voltage and current waveform. The shunted tank circuit has been designed at fundamental frequency so that it has infinite impedance at the fundamental frequency and zero impedance at all the harmonics. Then,

1. The input impedance of the transmission line at fundamental frequency is:

$$Z_{in} = \frac{Z_0^2}{Z_{load}} \tag{3.11}$$

   where Z_0 is the characteristic impedance of the transmission line. At even harmonics, the transmission line appears to be half wavelength or multiples of λ/2 long and a short-circuit at the output is regenerated at the drain [5].

2. At odd harmonics, the transmission line appears to be quarter wavelength or multiples of λ/4 long. The short circuit at the output is converted to an open circuit at the drain [5]. The DC component of the drain voltage, the fundamental and odd harmonic voltages produce a square-wave drain voltage.

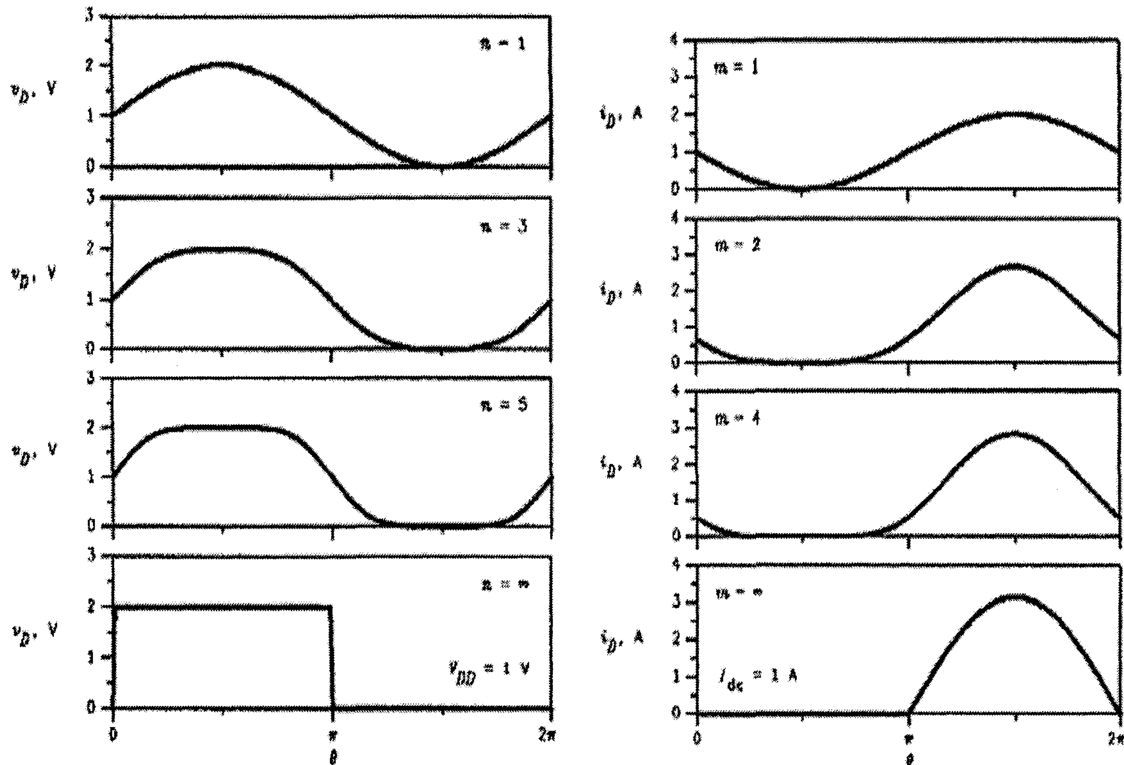


Fig 3.3: Drain voltage and current waveforms of the transistor in class-F amplifiers for different numbers of harmonic terminations [30]

3. At the fundamental frequency, the transmission line acts as impedance matching and transforms 50 Ohms to the appropriate termination.

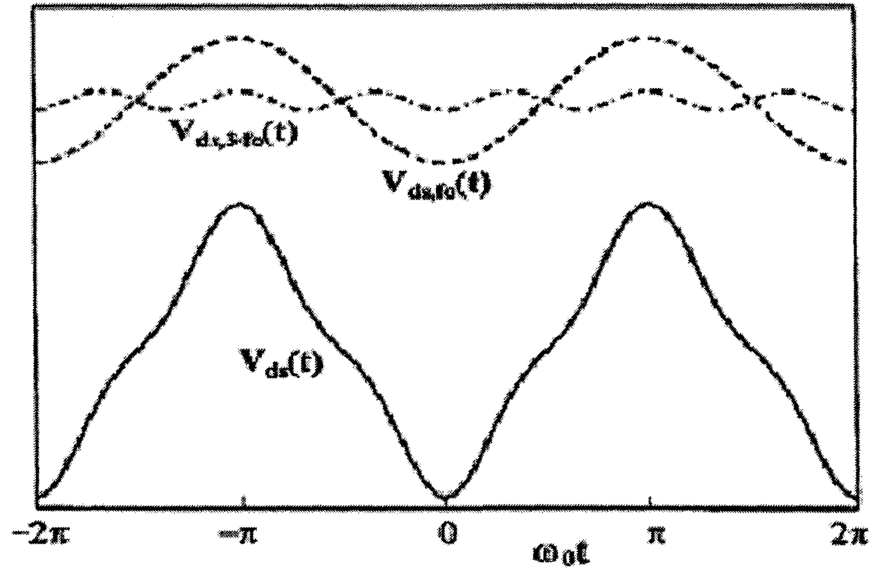


Fig 3.4: Output voltage when fundamental and third-harmonic voltage components are in-phase [32]

For proper class F operation it is necessary to bias the device from pinch-off to class A. If the device is biased below pinch-off the fundamental and third-harmonic voltage components are in phase with each other resulting in a peaked voltage waveform as shown in Figure 3.4. Consequently there is a decrease in output power and efficiency [32].

Since a third-harmonic component is added to the drain voltage, the negative peak of the voltage waveform is reduced while the magnitude of the fundamental-frequency component remains unaffected as shown in Figure 3.5. Maximum current occurs when the drain voltage waveform is near zero and maximum drain voltage occurs when no drain current flows. As a result, the power dissipated by the device is minimized and the size and weight of the power-amplifier heat sinks are reduced. In order to properly flatten the voltage wave-form, the third-harmonic voltage component must be of opposite phase with respect to the fundamental component which means the signs of the two voltage components must be opposite [32].

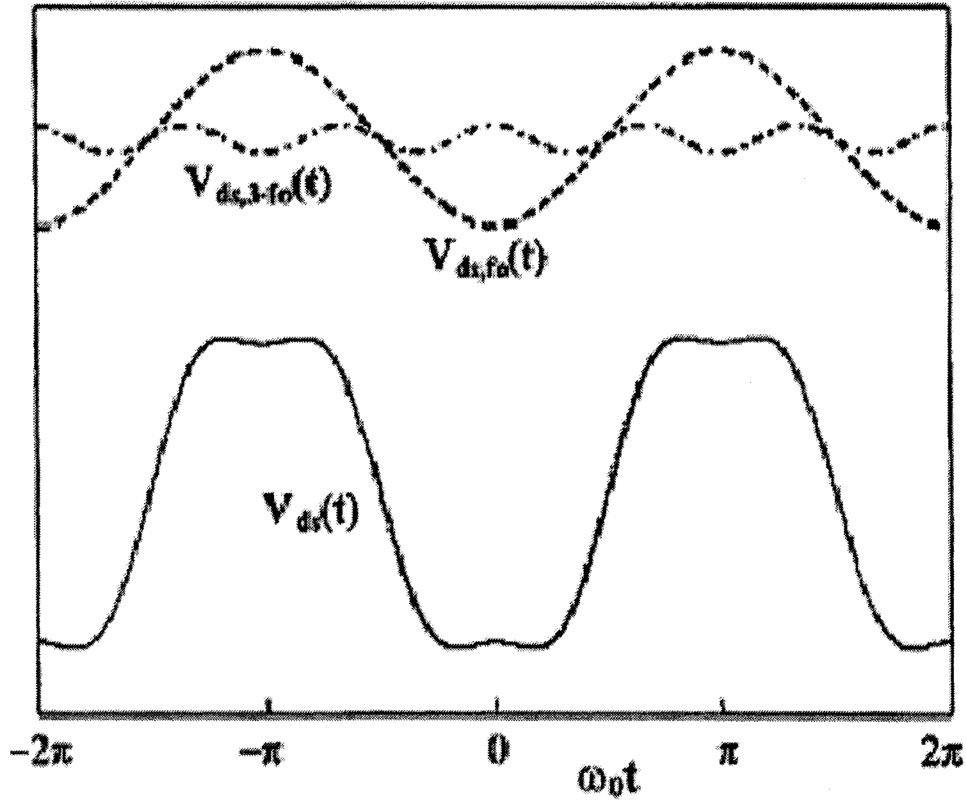


Fig 3.5: Output voltage when the fundamental and third-harmonic voltage components are out-of-phase [32]

Since the third harmonic voltage is obtained by loading the corresponding current component with a resistive termination, proper shaping can be obtained only if the third harmonic current component is negative [32]. The normalized amplitude of various current components as a function of current conduction angle is shown in Figure 3.6.

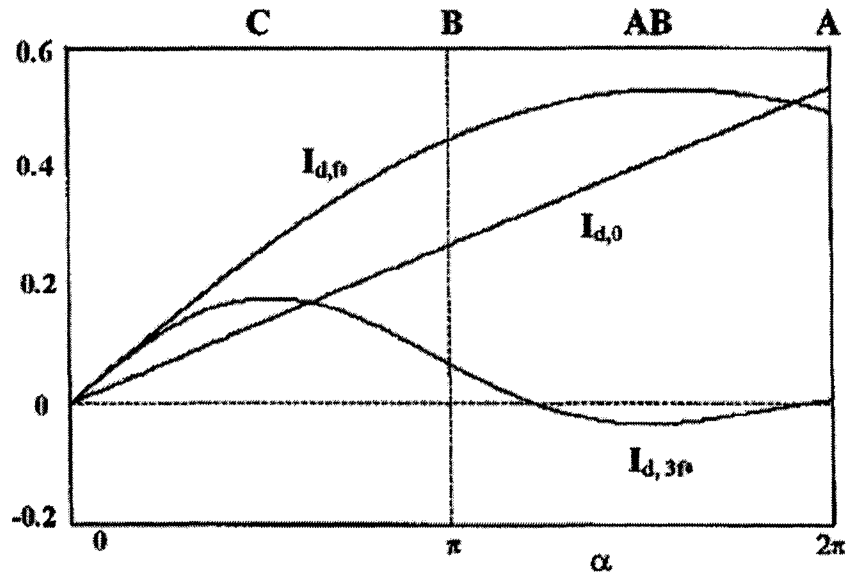


Fig 3.6: Normalized amplitude of DC, fundamentals and a third-harmonic components of the drain current as a function of drain current conduction angle [32]

3.4 Effect of Input Harmonics Termination

Some recent works have shown that input harmonic terminations also play an important role on the performance of class F amplifier [33-35]. Especially, Second input harmonic tuning has the most significant influence on efficiency and linearity.

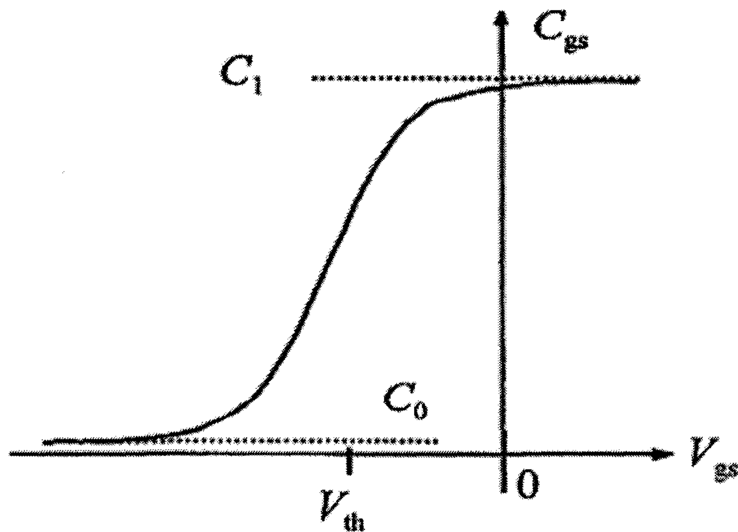


Fig 3.7: Typical gate capacitance characteristic of MESFET and HEMT [33]

The gate capacitance characteristic of RF field effect transistors shows severe non-linearity around threshold voltage, V_{th} as shown in Figure 3.7. There is a hard turn-off capacitance value around V_{th} due to abrupt departure of channel carriers when transistor turns off. Below V_{th},, in the gate fringing depletion region, there is only parasitic capacitance C_0. In low-high doped MESFET and HEMTs, which are highly used in RF power amplifiers, this characteristic is even more severe. The signal at the input gate gets distorted when the active device is biased around V_{th} in class F amplifiers. When the distortion is amplified, there is an unexpected current waveform at the output. Consequently, there is a bigger across area between the distorted drain current and rectangular voltage waveform and the power added efficiency decreases.

In the frequency domain, the distorted input voltage shows the increase of second order harmonic components. So, much attention should be paid to eliminate the second order harmonic components. Until now, various methods have been proposed such as bias capacitor, shunt shorting capacitor, series LC resonant network, diode etc. In all of these methods, the input sinusoid signal is retrieved by short circuit harmonic termination at the input resulting an output current waveform which is not distorted. As a result, the efficiency improves.

3.5 Conclusion

The necessary background on class F amplifier has been presented in this chapter. Based on this knowledge, a class F amplifier design for wireless application will be discussed in the next chapter.

Since power amplifiers used in UMTS devices need to be highly efficient, we should select a proper transistor. This choice comes from the growing interest in using GaN transistors in designing power amplifiers for wireless applications. GaN transistors have the ability to support high supply voltage resulting into high efficiency and high power generation [6]. The next chapter will discuss about such transistors.

Chapter 4 GaN Transistors

4.1 Introduction

Wide band-gap GaN HEMTs is one of the most promising emerging technologies for electronic and optical devices to deliver high frequency and high power operation at larger power densities [6]. This technology appeared around the 90s. The energy gap of GaN is three times larger than that of silicon. As a result, the performance degradation at high temperature reduces. It has high output power density due to high breakdown voltage. Figure 4.1 shows the physical structure of an AlGaN/GaN HEMT. Without even doping, the barrier layer, the AlGaN/GaN can have high charge carrier density to form 2DEG (2 dimensional electron gas) at the interface towards GaN layer.

The density is due to the piezoelectric and spontaneous polarization of GaN and AlGaN layer and is 10 times higher than that of conventional GaAs system [36].

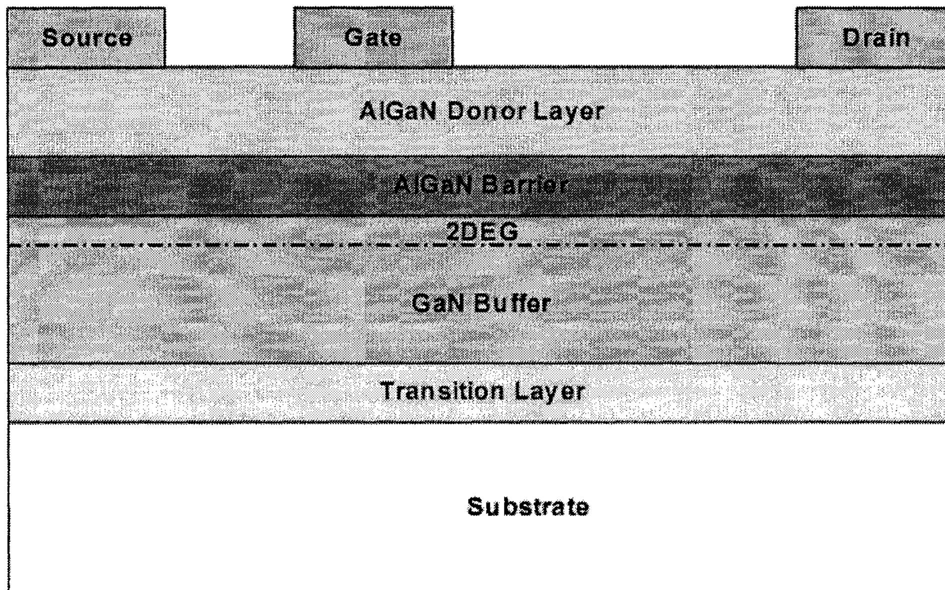


Fig 4.1: Schematic cross sectional view of AlGaN/GaN HEMT [6]

4.2 Comparison with Conventional MOSFETs and HEMTs

The comparison of the material properties of GaN, Si, GaAs and SiC are presented in the following table.

Table 4.1 Table of properties of Si, GaAs, SiC and GaN [6, 36]

Parameter	Si	GaAs	SiC	GaN
Energy gap [EV]	1.11	1.43	2.9	3.4
Breakdown field [V/cm]	5.7×10^5	6.4×10^5	3.3×10^6	3.8×10^6
Tmax	300	300	600	700
Electron mobility [cm^2/Vs]	1350	6000	800	1600
Thermal conductivity [W/Kcm]	1.5	.46	3.5	1.7
ε	11.4	13.1	9.7	9.5
BFOM ratio	1.0	9.6	3.1	24.6
JFM ratio	1.0	3.5	60	80

BFOM = Baliga's figure of merit for power transistor performance [$K*\mu*Ec^3$]
JFM = Johnson's figure of merit for power transistor performance [$Eb*Vbr*2\pi$]

Si LDMOSFETs are widely used in modern base station power amplifiers. They are of low cost technology, provide high output power, and have high breakdown voltage. But above 3 GHz, their usefulness is hampered due to high parasitic capacitance. III-V HEMTs offer high frequency performance but suffer from low power density. The Al-GaAs/GaAs HEMTs do not have large enough conduction band offset which restricts electrons although it is necessary for high frequency operation.

High breakdown electric field, high electron mobility and high saturation electron velocity have made AlGaN/GaN superior to other existing technologies. GaN HEMTs are able to provide high power and high frequency operation than SiGe. In GaN HEMTs, the GaN is processed on various substrates such as Si, SiC and Sapphire. Although GaN grown on SiC are more preferable since SiC is more thermally conductive. GaN HEMTs grown on SiC have shown superior frequency performance. Some of the best reported cut-off frequencies of AlGaN/GaN, AlGaAs/GaAs and InP HEMT devices are presented in table 4.2.

Table 4.2 Comparison of some reported f_Ts and f_{max}s of AlGaAs/GaAs, InP and AlGaN/GaN HEMTs [6]

Transistor	Gate Length (μm)	f_T (Transition frequency) [GHz]	f_{max} (Maximum frequency) [GHz]	Reference
AlGaAs/GaAs HEMT	0.1	113	110	[37]
InP HEMT	0.05	343	740	[38]
AlGaN/GaN-on-SiC HEMT	0.1	153	230	[39]
AlGaN/GaN-on- Si HEMT	0.5	32	27	[40]

GaN HEMTs show higher power density than Silicon and Gallium Arsenide based microwave transistors. The higher power per unit die of GaN reduces system cost since it eliminates the need of power combining. As a result, for the same output power, a reduction in device size can be possible using GaN HEMTs instead of conventional devices [36]. These smaller devices are easier to fabricate and they offer higher impedance. As a result it is easier to match them to a system. For conventional devices, the matching is a complex task since a larger matching ratio is needed. For example, a matching ratio which is 10 times larger might be needed for GaAs transistor. Consequently, the system complexity increases [36].

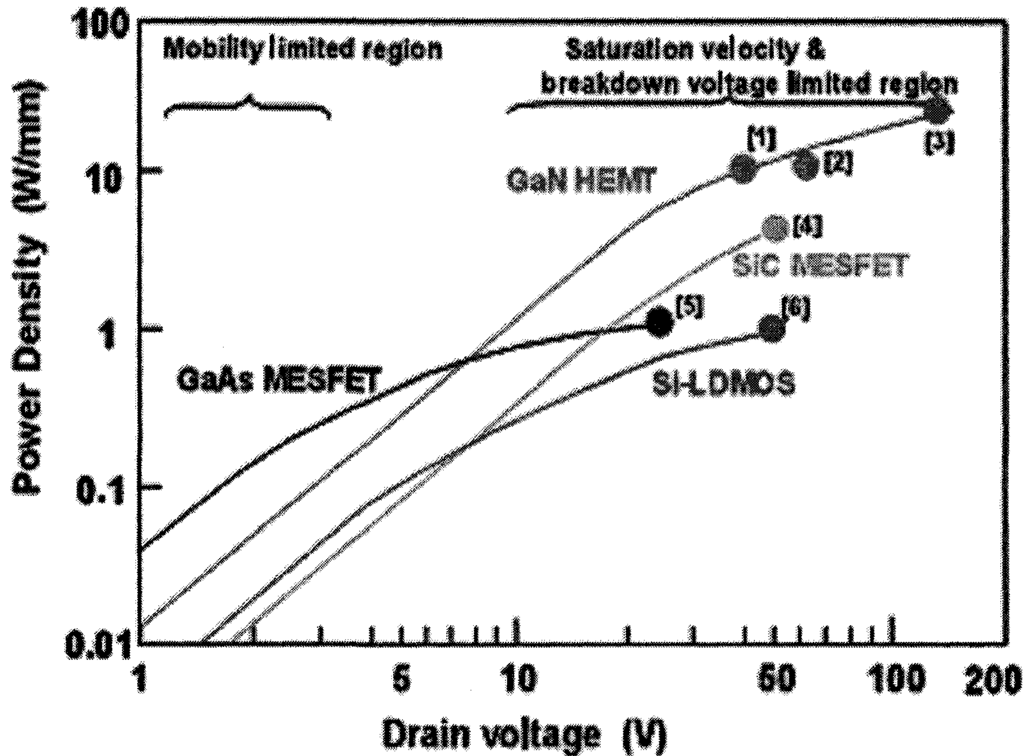


Fig 4.2: Comparison of RF power density of GaN HEMT
with other RF devices [41]

Another important aspect is that commercial systems such as wireless base stations operate at 28 volts [36]. GaN devices can easily operate at 28 volts and up to 42 volts. So, there is no need of voltage conversion. In case of a low voltage technology, a voltage step down should be performed. Since GaN HEMTs are capable to operate at higher voltage they provide higher efficiency. As a result, the power requirement and the weight of the cooling system are also reduced. Also, low distortion characteristic is required for base station amplifiers and GaN HEMTs show superior distortion performance [42, 43].

4.3 Conclusion

Although GaN HEMTs are well suited for high power application they have some demerits as well. The advantages and disadvantages of GaN HEMTs are summarized in table 4.3.

Table 4.3 Advantages and disadvantages of GaN technology

Advantages	Disadvantages
➢ High breakdown voltage ➢ High current density ➢ Wide band gap. ➢ Power amplifiers using GaN HEMT can achieve higher efficiency. ➢ High thermal conductivity. ➢ The power density is up to 10 times higher than that of GaAs PHEMT. ➢ Power amplifiers using GaN HEMT require low loss matching circuit and small, light cooling system.	➢ Expensive. ➢ Still immature, hampered by basic manufacturability and reliability issues.

The background on wide band gap GaN based HEMTs, their advantages and disadvantages have been discussed in this chapter. In this thesis, a class F amplifier using a GaN HEMT will be designed, simulated and measured. The GaN transistor was provided by Cree Inc.

Chapter 5 Design Concepts, Simulation and Results

5.1 Introduction

In the previous chapters, the basic principle and operation of the class F topology and the advantages of GaN transistor over other existing technologies have been explained. In this chapter a detailed design procedure of a class F amplifier at 2.14 GHz and its performance evaluation are explained. The amplifier uses a Cree's GaN transistor CGH40010F along with its design kit. The simulations have been performed using the ADS (Advanced Design System) circuit simulator from Agilent. Various design procedures involved in the design of class F amplifier such as DC simulation, bias point selection, S-parameter simulation, source-pull and load pull characterization, input and output matching network design, suitable harmonic termination and optimization are explained..

5.1.1 Design Criteria

The amplifier was designed to operate at WCDMA band (2.11 GHz – 2.17 GHz) with a center frequency of 2.14 GHz. Designing a high efficiency class F amplifier that fulfils the requirements of UMTS (Universal Mobile Telecommunication System) was the main goal of this thesis. The following conditions were set for the amplifier.

Table 5.1: Design Criteria

Design Frequency	2.14 GHz
Peak power	36 dBm
Min PAE @ peak output power	70%
Min PAE @ 6 dB back-off	30%
Third order IM products at maximum output power	-10 dBc
Third order IM products at 6 dB back-off from maximum output power	-25 dBc

5.1.2 Substrate

For simulation and realization of the designed class-F amplifier in microstrip environment the substrate used was RT Duroid 5870. The parameters of the substrate are given in table 5.2.

Table 5.2: Parameters of the used substrate

Dielectric constant, ε_r	2.33
Substrate height	31 mil
Conductor (Cu) thickness	35 μm
Loss tangent, tanδ	.0012

5.2 Design Procedure

5.2.1 DC Characteristics Analysis

Selecting the most suitable bias point is the first step in designing any power amplifier. Hence a DC simulation was performed first to get the DC characteristic of the GaN HEMT used in this work. If the gate and drain bias voltages are varied, the output characteristics of the transistor show the different regions of operation (ohmic, saturation, and cut-off) and transistor transfer characteristics show the pinch-off voltage for certain drain bias voltage [1]. The drain voltage was varied from 0 to 42 volts. In Figure 5.1, it is seen that the maximum value of drain current is 577 mA. A drain voltage of V_{DS} = 35 V has been chosen.

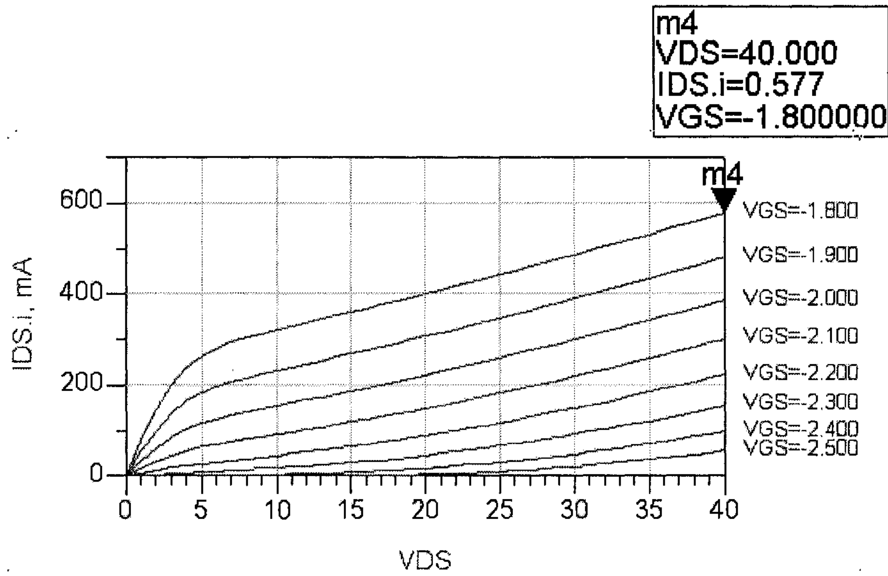


Fig 5.1: Transistor output characteristic

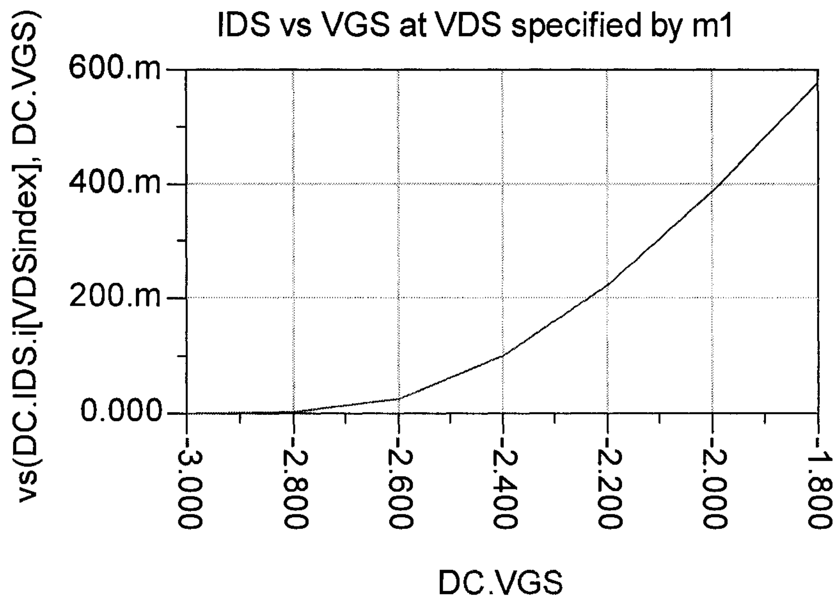


Fig 5.2: Transistor transfer characteristic

From Figure 5.2 it is observed that the pinch off voltage is around -3 volts.

Class F can be biased either as class AB or as class B. However, in this work class AB bias has been chosen where 35 volts of V_{DS} and -2.4 volts of V_{GS} have been selected to bias the transistor.

5.2.2 S Parameter Simulation

In the next step, it was verified that the ADS model of the transistor gives acceptable scattering parameters compared to ones given in the data sheet. However, slight differences between simulated and measured parameters can be expected. The S-parameters given in the data sheet have three different bias conditions (see Appendix A). The one with V_{DS}=28V and I_{DQ}=100mA was simulated and verified (Tables 5.3 and 5.4).

Table 5.3: Given S-parameters at V_{DS} = 28V and I_{DQ} = 100mA
(from the manufacturer's datasheets)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.8785	-143.68	12.55	101.09	0.0373	14.45	0.5687	-156.56
600 MHz	0.8740	-151.05	10.64	96.46	0.0380	10.48	0.5787	-161.57
700 MHz	0.8711	-156.75	9.22	92.62	0.0384	7.32	0.5817	-165.41
800 MHz	0.8690	-161.33	8.14	89.31	0.0386	4.68	0.5850	-168.51
900 MHz	0.8675	-165.18	7.27	86.35	0.0389	2.40	0.5872	-171.09
1.0 GHz	0.8664	-168.44	6.58	83.65	0.0390	0.38	0.5888	-173.31
1.1 GHz	0.8655	-171.33	6.00	81.14	0.0391	-1.45	0.5900	-175.27
1.2 GHz	0.8647	-173.91	5.52	78.77	0.0392	-3.15	0.5909	-177.04
1.3 GHz	0.8641	-176.25	5.12	76.51	0.0392	-4.73	0.5915	-178.65
1.4 GHz	0.8635	-178.42	4.77	74.33	0.0393	-6.23	0.5920	179.86
1.5 GHz	0.8630	179.56	4.46	72.22	0.0394	-7.65	0.5923	178.46
1.6 GHz	0.8625	177.66	4.20	70.17	0.0394	-9.02	0.5926	177.14
1.7 GHz	0.8620	175.86	3.96	68.15	0.0395	-10.35	0.5927	175.87
1.8 GHz	0.8615	174.13	3.75	66.18	0.0395	-11.63	0.5928	174.65
1.9 GHz	0.8610	172.47	3.57	64.23	0.0395	-12.89	0.5928	173.48
2.0 GHz	0.8606	170.86	3.40	62.31	0.0396	-14.11	0.5928	172.33
2.1 GHz	0.8601	169.29	3.25	60.41	0.0396	-15.32	0.5927	171.21
2.2 GHz	0.8597	167.76	3.11	58.53	0.0397	-16.50	0.5925	170.11
2.3 GHz	0.8592	166.26	2.99	56.66	0.0397	-17.67	0.5924	169.02
2.4 GHz	0.8587	164.79	2.87	54.80	0.0397	-18.83	0.5922	167.95
2.5 GHz	0.8582	163.33	2.77	52.94	0.0398	-19.97	0.5919	166.89
2.6 GHz	0.8577	161.89	2.67	51.10	0.0398	-21.10	0.5916	165.83
2.7 GHz	0.8571	160.46	2.58	49.26	0.0399	-22.23	0.5913	164.78
2.8 GHz	0.8566	159.04	2.50	47.42	0.0399	-23.35	0.5909	163.72
2.9 GHz	0.8560	157.62	2.42	45.58	0.0400	-24.46	0.5905	162.67
3.0 GHz	0.8555	156.21	2.35	43.74	0.0400	-25.57	0.5901	161.62
3.1 GHz	0.8549	154.80	2.29	41.91	0.0401	-26.68	0.5896	160.56
3.2 GHz	0.8542	153.38	2.23	40.07	0.0401	-27.79	0.5891	159.49
3.3 GHz	0.8536	151.97	2.17	38.23	0.0402	-28.89	0.5886	158.42
3.4 GHz	0.8529	150.54	2.12	36.38	0.0402	-29.99	0.5880	157.34
3.5 GHz	0.8523	149.11	2.07	34.53	0.0403	-31.10	0.5873	156.25
3.6 GHz	0.8516	147.68	2.02	32.68	0.0403	-32.20	0.5867	155.15
3.7 GHz	0.8508	146.23	1.98	30.81	0.0404	-33.31	0.5859	154.04
3.8 GHz	0.8501	144.77	1.94	28.95	0.0405	-34.41	0.5852	152.91
3.9 GHz	0.8493	143.30	1.90	27.07	0.0406	-35.52	0.5844	151.77
4.0 GHz	0.8485	141.81	1.86	25.18	0.0406	-36.64	0.5835	150.61
4.1 GHz	0.8478	140.31	1.83	23.29	0.0407	-37.76	0.5827	149.44
4.2 GHz	0.8469	138.79	1.79	21.38	0.0408	-38.88	0.5817	148.25
4.3 GHz	0.8461	137.25	1.76	19.46	0.0409	-40.01	0.5808	147.04
4.4 GHz	0.8452	135.70	1.73	17.53	0.0409	-41.15	0.5797	145.80
4.5 GHz	0.8443	134.12	1.71	15.59	0.0410	-42.29	0.5787	144.55

Table 5.4: Simulated S parameters (in ADS) at V_{DS} = 28V and I_{DQ} = 100mA

freq	S(1,1)	S(2,1)	S(1,2)	S(2,2)
500.0 MHz	0.880 / -141.276	11.814 / 101.848	0.041 / 14.899	0.530 / -152.451
600.0 MHz	0.875 / -148.948	10.038 / 96.990	0.041 / 10.654	0.537 / -157.883
700.0 MHz	0.872 / -154.876	8.711 / 92.968	0.042 / 7.244	0.542 / -162.014
800.0 MHz	0.869 / -159.650	7.668 / 89.493	0.042 / 4.383	0.546 / -165.304
900.0 MHz	0.868 / -163.626	6.877 / 86.395	0.042 / 1.899	0.548 / -168.021
1.000 GHz	0.867 / -167.031	6.220 / 83.565	0.043 / -0.314	0.549 / -170.332
1.100 GHz	0.866 / -170.014	5.678 / 80.935	0.043 / -2.327	0.551 / -172.346
1.200 GHz	0.865 / -172.678	5.223 / 78.464	0.043 / -4.189	0.552 / -174.138
1.300 GHz	0.864 / -175.095	4.837 / 76.088	0.043 / -5.934	0.553 / -175.759
1.400 GHz	0.864 / -177.319	4.505 / 73.814	0.043 / -7.586	0.554 / -177.248
1.500 GHz	0.863 / -179.388	4.216 / 71.613	0.043 / -9.163	0.555 / -178.631
1.600 GHz	0.863 / 178.668	3.964 / 69.470	0.043 / -10.680	0.555 / -179.931
1.700 GHz	0.862 / 176.825	3.741 / 67.375	0.043 / -12.146	0.556 / 178.836
1.800 GHz	0.862 / 175.065	3.543 / 65.319	0.043 / -13.571	0.556 / 177.658
1.900 GHz	0.861 / 173.373	3.365 / 63.296	0.043 / -14.961	0.557 / 176.521
2.000 GHz	0.861 / 171.738	3.206 / 61.300	0.043 / -16.321	0.557 / 175.420
2.100 GHz	0.861 / 170.149	3.062 / 59.327	0.043 / -17.655	0.558 / 174.348
2.200 GHz	0.860 / 168.599	2.932 / 57.372	0.043 / -18.968	0.558 / 173.297
2.300 GHz	0.860 / 167.081	2.813 / 55.432	0.043 / -20.262	0.559 / 172.265
2.400 GHz	0.860 / 165.589	2.704 / 53.506	0.043 / -21.540	0.559 / 171.246
2.500 GHz	0.859 / 164.118	2.605 / 51.590	0.043 / -22.805	0.559 / 170.236
2.600 GHz	0.859 / 162.663	2.513 / 49.682	0.043 / -24.057	0.560 / 169.232
2.700 GHz	0.858 / 161.222	2.429 / 47.781	0.043 / -25.298	0.560 / 168.233
2.800 GHz	0.858 / 159.790	2.350 / 45.885	0.043 / -26.531	0.560 / 167.235
2.900 GHz	0.857 / 158.365	2.278 / 43.992	0.043 / -27.756	0.561 / 166.236
3.000 GHz	0.857 / 156.943	2.210 / 42.102	0.043 / -28.974	0.561 / 165.234
3.100 GHz	0.857 / 155.524	2.148 / 40.213	0.043 / -30.187	0.561 / 164.227
3.200 GHz	0.856 / 154.103	2.089 / 38.324	0.043 / -31.394	0.561 / 163.215
3.300 GHz	0.856 / 152.679	2.035 / 36.433	0.043 / -32.599	0.561 / 162.194
3.400 GHz	0.855 / 151.251	1.984 / 34.541	0.043 / -33.800	0.562 / 161.164
3.500 GHz	0.855 / 149.817	1.936 / 32.646	0.043 / -34.998	0.562 / 160.124
3.600 GHz	0.854 / 148.374	1.891 / 30.746	0.043 / -36.196	0.562 / 159.071
3.700 GHz	0.853 / 146.921	1.848 / 28.842	0.043 / -37.392	0.562 / 158.005
3.800 GHz	0.853 / 145.456	1.809 / 26.932	0.043 / -38.588	0.562 / 156.925
3.900 GHz	0.852 / 143.981	1.771 / 25.016	0.043 / -39.784	0.562 / 155.830
4.000 GHz	0.852 / 142.490	1.736 / 23.093	0.043 / -40.982	0.561 / 154.718
4.100 GHz	0.851 / 140.984	1.703 / 21.162	0.043 / -42.180	0.561 / 153.588
4.200 GHz	0.850 / 139.461	1.671 / 19.221	0.043 / -43.381	0.561 / 152.439
4.300 GHz	0.850 / 137.920	1.642 / 17.272	0.043 / -44.585	0.561 / 151.270
4.400 GHz	0.849 / 136.360	1.614 / 15.311	0.043 / -45.791	0.561 / 150.080
4.500 GHz	0.848 / 134.779	1.587 / 13.340	0.043 / -47.002	0.560 / 148.869

5.2.3 Load Pull and Source Pull Simulation

Initially, it is assumed that the input and output impedances of the amplifier are 50 ohms. But in reality, this is not the case. To find the optimum output and input impedances of the amplifier, load pull and source pull simulation are needed to be performed.

Load pull is a technique where the load impedance seen by the device under test (DUT) is varied and the performance of the DUT is simultaneously measured [10]. Similarly in source pull the source impedance is varied and the performance of the DUT is measured. From the measured results, the optimum load and source impedance at which the device gives the best performance are determined. Power and efficiency contours of load pull and source pull analysis are not necessarily be aligned [44]. Hence, the load im-

pedance at which maximum output power is achieved may not give the maximum efficiency. Since in this work the efficiency is of the main interest, the load impedance that gives maximum efficiency has been taken into account. The input of a power amplifier is usually conjugate matched and the source pull is not always required. However in the design of a Class F power amplifier, the source pull is useful to determine the effects of the second harmonic termination [45]. These impedance values vary with bias.

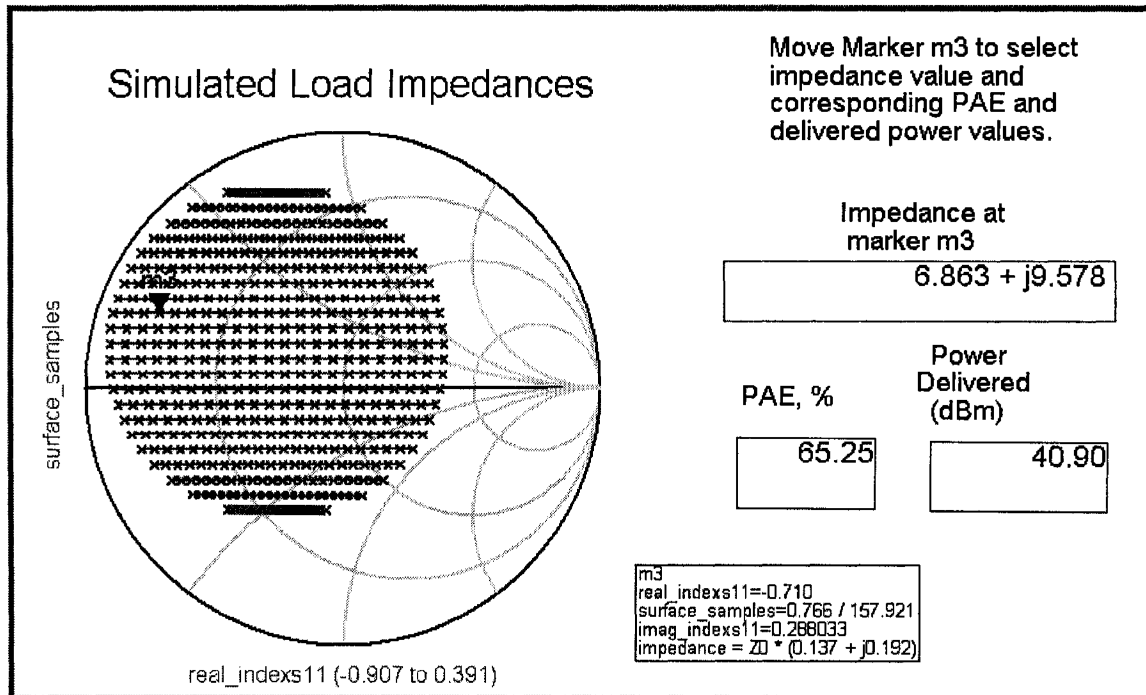


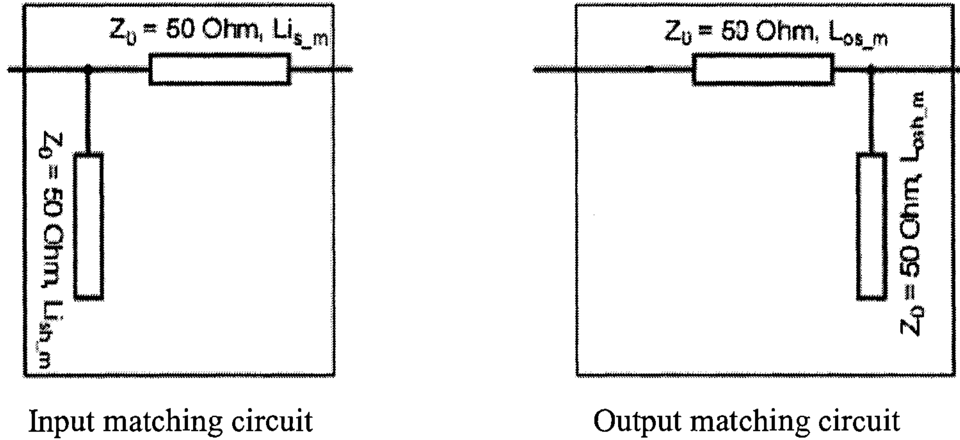
Fig 5.3: Load pull analysis

Load pull and source pull simulations were performed. The results obtained from these simulations show that the transistor needs to see an impedance of 6.863 + j9.578 ohms at the output and 2.142 – j3.036 ohms at the input to get the maximum efficiency.

5.2.4 Input and Output Matching Network Design

From the load-pull and source-pull simulations, it is observed that the optimum input and output impedances of the transistor are not 50 ohms. So it is necessary to design matching networks at the fundamental design frequency to achieve maximum effi-

ciency. Input and output matching networks can be designed using either lumped components or transmission lines. In this work the later one has been used to design the matching networks for the ease of fabrication.



Input matching circuit Output matching circuit

Fig 5.4: Input and output matching topology using transmission lines [1]

The input matching network for the fundamental frequency is designed using the source impedance obtained from the source-pull simulation. Similarly, the output matching network is designed with the load impedance obtained from the load-pull simulation [46, 47].

5.2.5 Harmonics Control

In class F amplifier the second and third order harmonics tuning need to be included in the output network to increase output power and efficiency. The higher order harmonics are ignored to avoid circuit complexity. Furthermore, the second and third order harmonics have most significant effects on the output waveforms of the amplifier.

The second harmonic has been tuned by using quarter-wave transmission lines at fundamental frequency instead of inductors in the bias networks. The end of each transmission line which is connected to the DC supply is grounded through a capacitor [48]. These transmission lines not only tune the second harmonic but also function as bias net-

works. These transmission lines provided a very good short circuit at not only the second harmonic frequency but also at the fourth and higher even order frequencies. An open circuited transmission line of length $\lambda/12$ at the fundamental design frequency has been used to tune the third harmonic [48]. By using these transmission lines the main operation principle of Class-F PA are well achieved. The square wave drain voltage and half-sinusoidal drain current are generated, having small overlap. As a result, the power dissipated by the active device decreases and the efficiency increases.

After the task of harmonic tuning, some other transmission lines are added in the amplifier circuit that are needed for the practical realization of the amplifier. Then optimization is performed to achieve higher efficiency.

5.2.6 Stability

The stability simulation was done to check the stability factor of the designed amplifier. Although the stability factor was less than 1 at the frequency of interest it was found that the impedances of the input and output matching network seen by the transistor from the drain and gate respectively are still in the stable region which are shown in Figure 5.6. Adding a resistor at the gate makes the stability factor greater than 1 but the efficiency in that case would decrease.

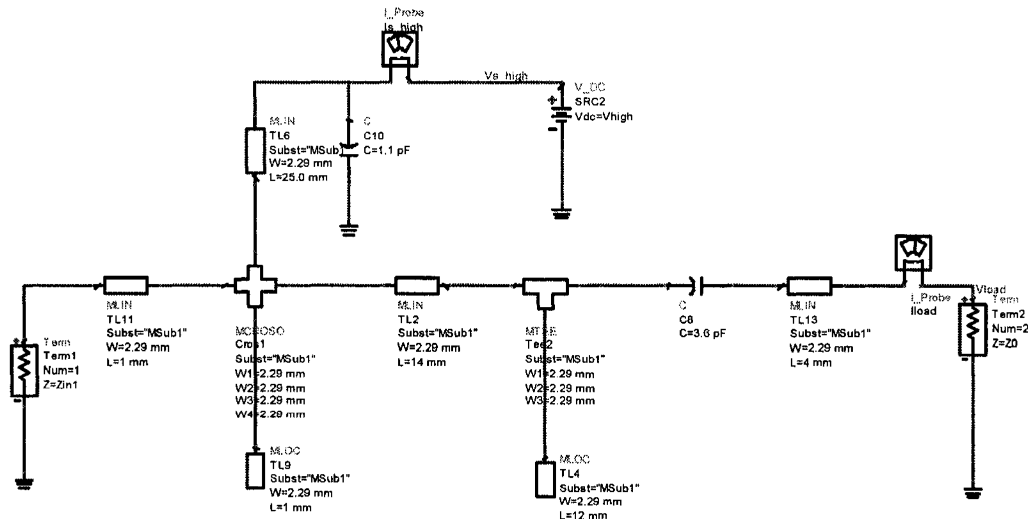


Fig 5.5: Simulation for output matching network (Z_L=Zin1)

Figure 5.6 shows the locations of the impedances of the input and the output matching network seen by the transistor from gate and drain, respectively.

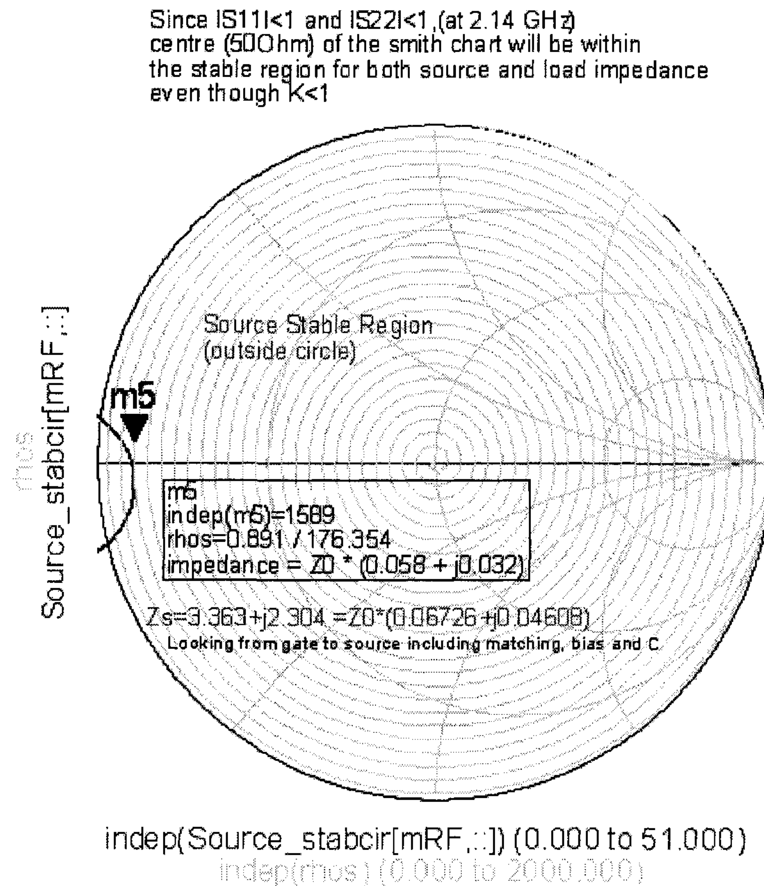


Fig 5.6-a: Location of the impedance of the input matching network seen by the transistor from gate

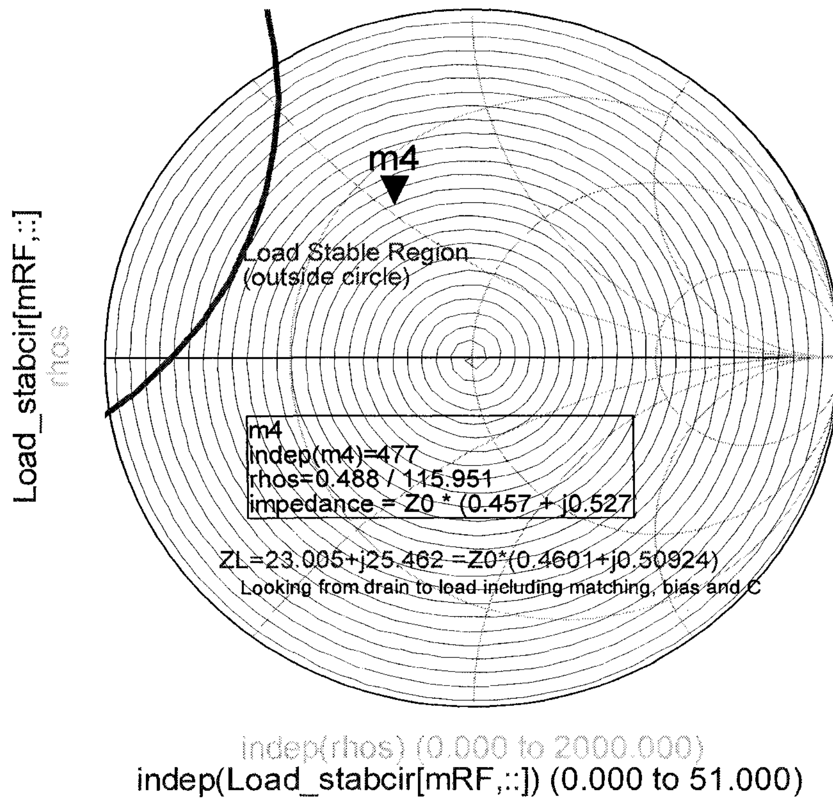


Fig 5.6-b: Location of the impedance of the output matching network seen by the transistor from drain

5.3 Simulation Results for Single Tone

A single-tone simulation was done to plot the voltage and current waveforms at drain. The resultant waveforms are given in Figure 5.7 and 5.8.

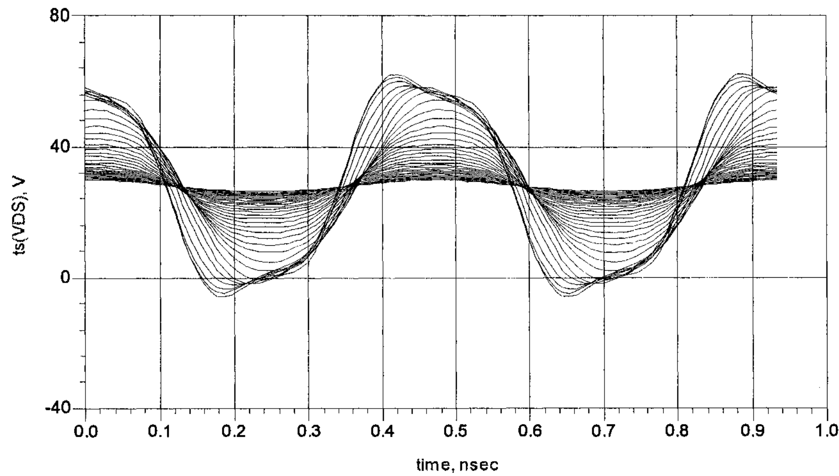


Fig 5.7: Drain voltage waveform of the designed amplifier for different input powers (0 dBm to 36 dBm, step size 1 dBm)

As seen in Figure 5.7 the drain voltage waveform of the amplifier is not exactly square wave. This is because of the presence of the third harmonic only. If higher order harmonics are added to the voltage waveform it would approach a square wave.

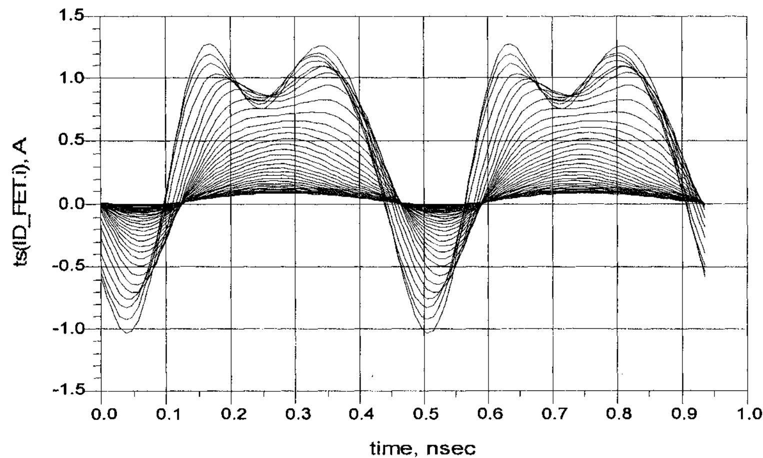


Fig 5.8: Drain current waveform of the designed amplifier for different input powers (0 dBm to 36 dBm, step size 1 dBm)

Figure 5.8 shows the drain current waveform. It approximates to rectified half-sinusoidal, but with negative spike. The reason behind this is the non-ideal cancellation of the reactive part of the transistor which can be reduced by optimization of the matching network [5]. From Figure 5.7 and 5.8 it can be seen that the current peaks occur when voltage is at its minimum and that the current minimum occurs when voltage has maximum values. As a result the power loss is reduced and efficiency increases.

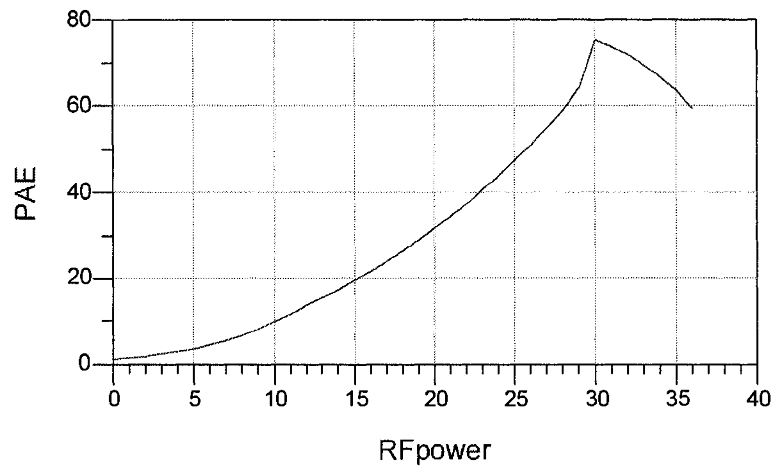


Fig 5.9: PAE (%) vs input power (dBm)

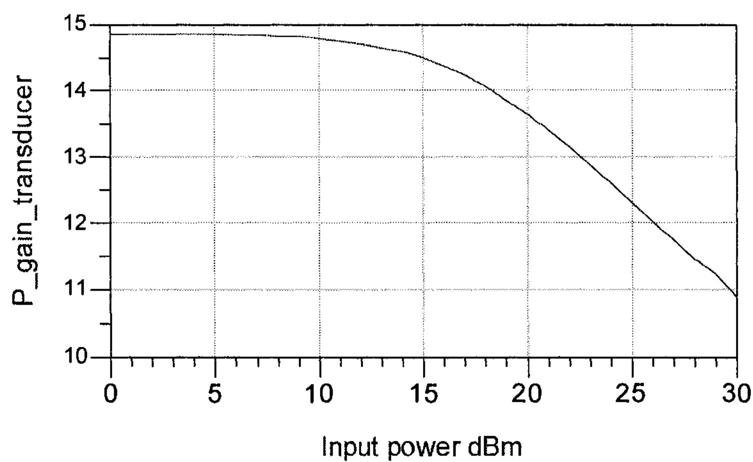


Fig 5.10: Plot of transducer power gain (dB) vs input power (dBm)

Figure 5.9 and 5.10 show the PAE and transducer power gain of the amplifier respectively. It is seen from Figure 5.9 that the maximum available PAE is around 76% with an input power of 30 dBm. In the transducer gain curve, $Pin_{1\text{-}dB}$ point is 18 dBm with 14dB gain. The rapid reduction of the gain is one characteristic of GaN technology.

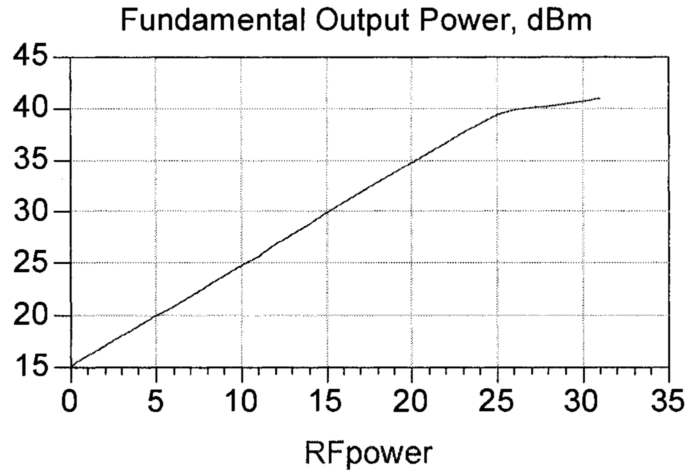


Fig 5.11: Plot of output power vs input power (dBm)

Table 5.5: Harmonic levels at the output

Available Source Power dBm	Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
0.0000	-85.60	-71.48	-118.8	-91.93
1.000	-84.60	-68.84	-114.4	-88.01
2.000	-83.60	-66.10	-110.1	-84.13
3.000	-82.61	-63.28	-105.7	-80.31
4.000	-81.63	-60.37	-101.3	-76.57
5.000	-80.67	-57.40	-97.06	-72.93
6.000	-79.74	-54.39	-92.87	-69.40
7.000	-78.85	-51.35	-88.78	-66.00
8.000	-77.99	-48.32	-84.79	-62.70
9.000	-77.18	-45.31	-80.86	-59.42
10.00	-76.40	-42.33	-76.96	-56.03
11.00	-75.62	-39.36	-73.02	-52.35
12.00	-74.75	-36.43	-69.08	-48.38
13.00	-73.59	-33.84	-65.83	-45.19
14.00	-72.12	-31.96	-63.76	-42.96
15.00	-70.66	-30.57	-62.37	-40.92
16.00	-69.26	-29.50	-61.47	-39.18
17.00	-67.90	-28.68	-60.92	-37.72
18.00	-66.56	-28.08	-60.69	-36.51
19.00	-65.26	-27.66	-60.79	-35.53
20.00	-64.06	-27.38	-61.09	-34.59
21.00	-62.99	-27.17	-61.42	-33.69
22.00	-62.05	-27.03	-61.74	-32.94
23.00	-61.22	-26.96	-61.92	-32.42
24.00	-60.49	-26.94	-61.80	-32.18
25.00	-59.86	-26.96	-61.31	-32.28
26.00	-59.31	-26.99	-60.53	-32.82
27.00	-58.78	-26.92	-59.84	-34.22
28.00	-58.11	-26.40	-60.24	-38.25
29.00	-57.06	-25.55	-63.67	-40.55
30.00	-55.51	-23.18	-66.30	-29.52

Since the PAE is optimum at 30 dBm (Figure 5.9), we will select this power level as the input power. Therefore, the output and drain voltage and current waveforms at 30 dBm input power are shown in Figure 5.12, 5.13, 5.14.

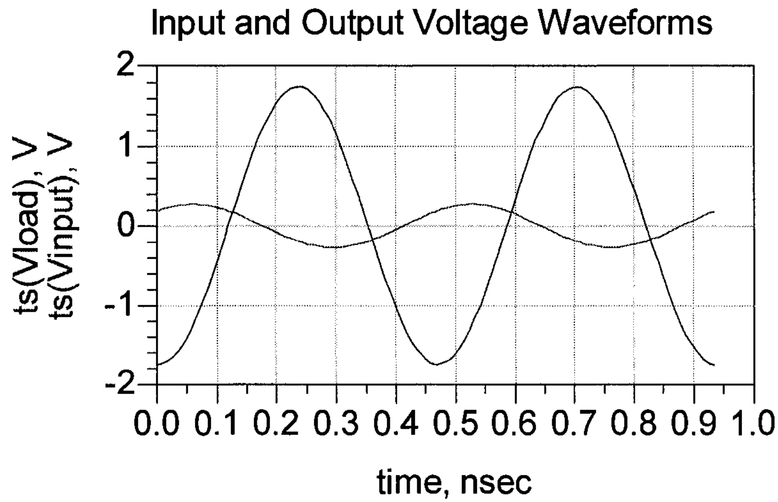


Fig 5.12: Input and output voltage waveform of the amplifier for 30 dBm input power

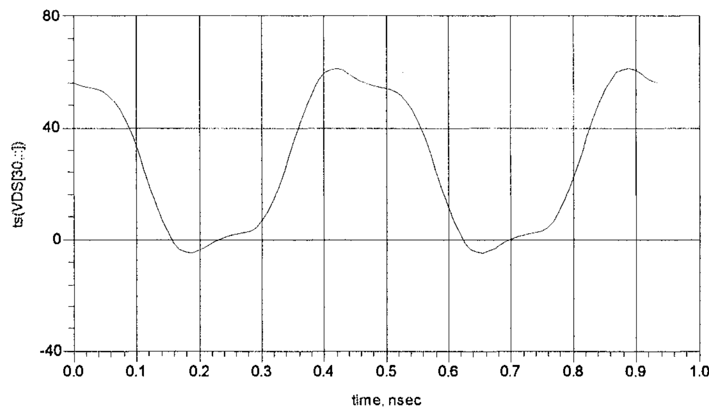


Fig 5.13: Drain voltage waveform of the amplifier for 30 dBm input power

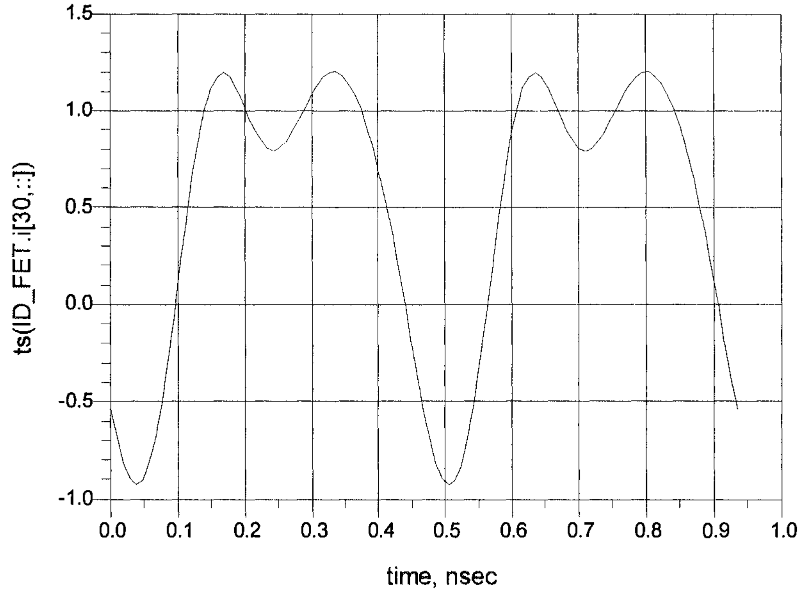


Fig 5.14: Drain current waveform of the amplifier for 30 dBm input power

5.4 Two Tone Simulation Results

In the next step, two-tone harmonic balance simulations were performed on the Class F amplifier. Harmonic balance is a frequency-domain analysis technique which determines the spectral content of voltages and currents in the circuit as well as the power added efficiency of the amplifier in the presence of interferers [5]. The two frequencies were chosen to be 2140.05 MHz and 2139.95 MHz. Seventh order harmonic balance simulation was performed. Figure 5.15 is a plot of the output spectrum of the Class F PA at 30 dBm input power.

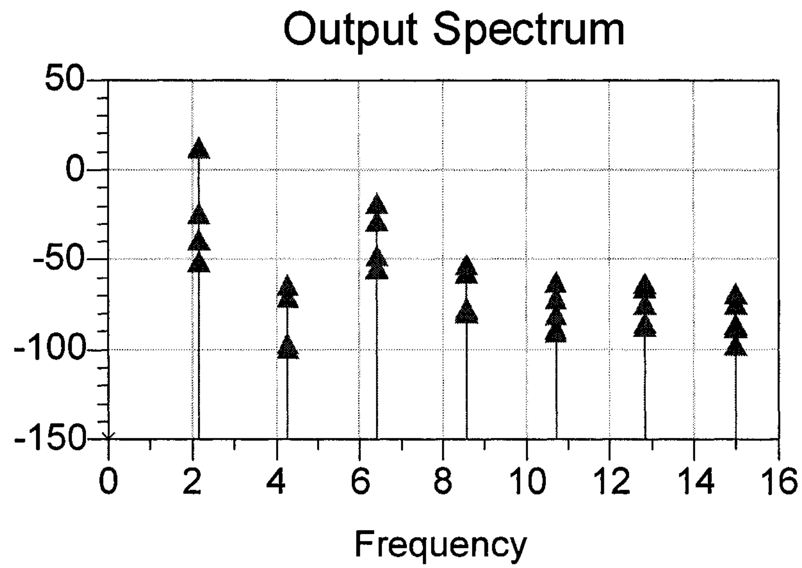


Fig 5.15: Output spectrum at 30 dBm input power

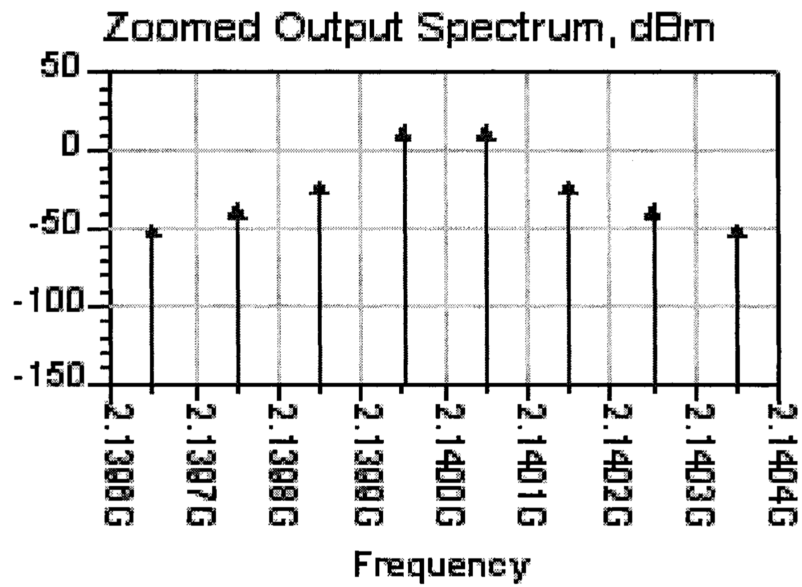


Fig 5.16: Zoomed output spectrum

Figure 5.16 is a zoomed output spectrum of the designed Class F amplifier where the third, fifth and seventh order intermodulation products have been shown. These intermodulation products are low enough vs. the fundamental power so that the amplifier two-tone behaviour is acceptable.

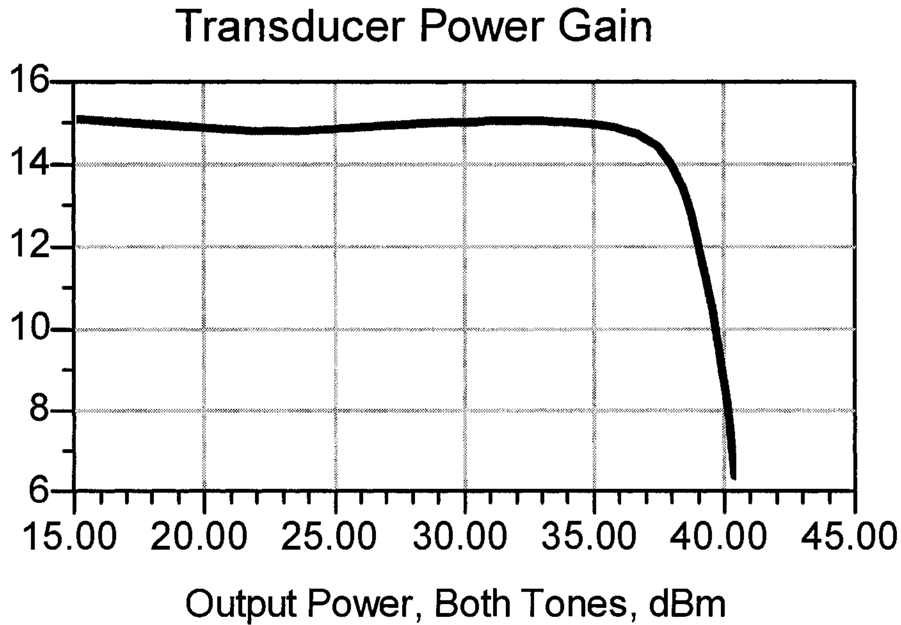


Fig 5.17: Transducer power gain (dB) vs output power (dBm)

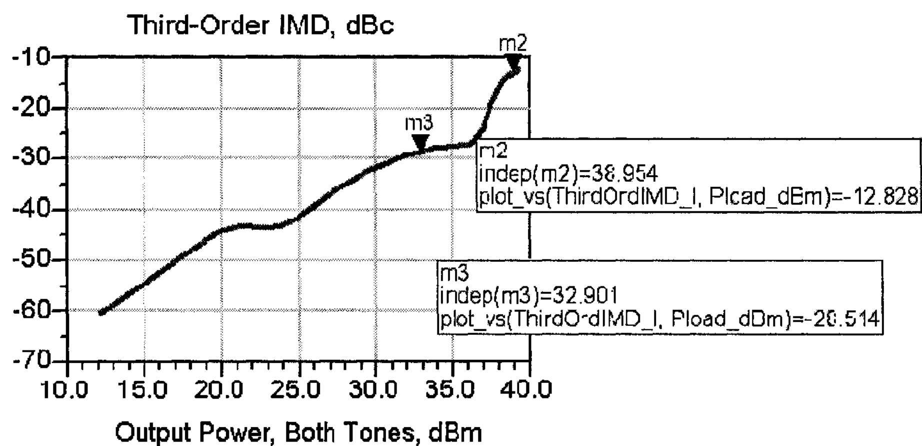


Fig 5.18: IMD3 (dBc) of the designed class F power amplifier

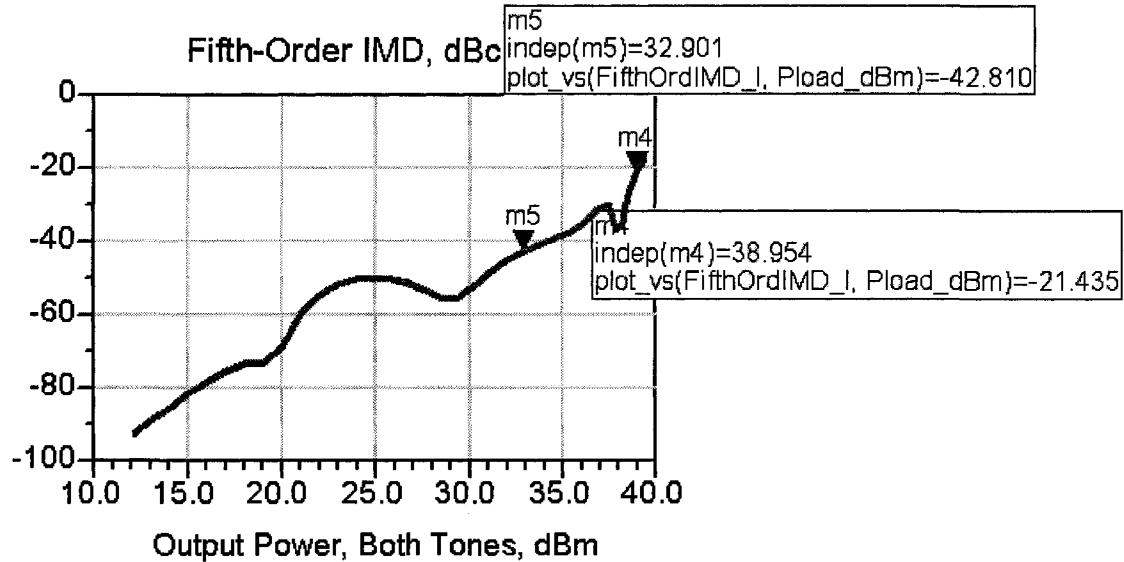


Fig 5.19: IMD5 (dBc) of the designed class F power amplifier

Figure 5.17 shows the power gain as a function of the output power and the simulated IMD3 and IMD5 response of the designed amplifier as a function of the output power have been shown in Figure 5.18 and 5.19. The value of third and fifth order IM products of the designed class F PA is suitable for our amplifier (almost -13 dBc and -21 dBc respectively at peak power and -28.5 dBc and -43 dBc respectively at 6 dB back-off from peak power).

5.5 Conclusion

A design procedure of the GaN HEMT amplifier has been performed. Simulated results are in good agreement with class F amplifier criteria.

The next step is the fabrication and tests of the designed amplifier.

Chapter 6 Circuit Fabrication and Tests

6.1 Introduction

The layout of the designed class F amplifier was generated in ADS-Momentum and thus the amplifier was fabricated and tested. Figure 6.1 shows the layout whereas Figure 6.2 shows the schematic of the designed amplifier.

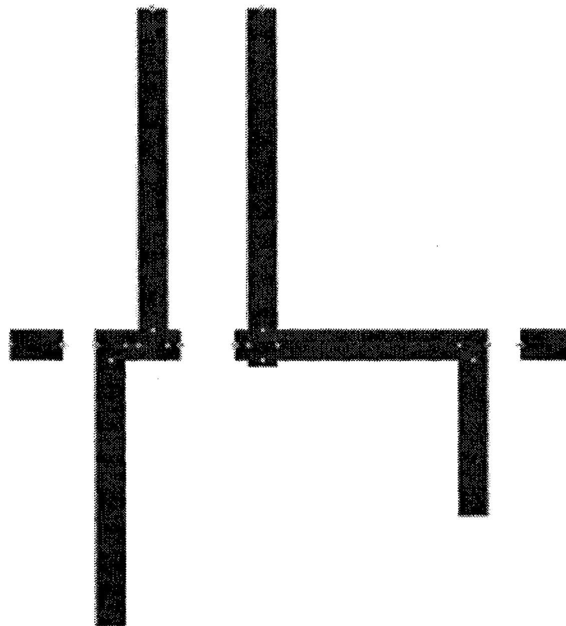


Fig. 6.1: Amplifier: layout in ADS-Momentum

Fig 6.2: Amplifier: Schematic in ADS

6.2 Measured Results

Figures 6.3 to 6.5 show a comparison between simulated and measured fundamental, second ad third output powers versus the input power level. For a better view, all the curves are shown in Figure 6.6.

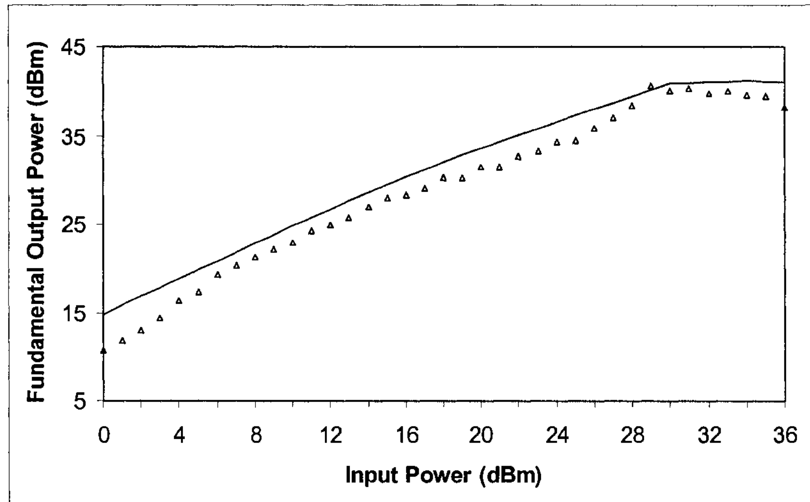


Fig. 6.3: Amplifier: Fundamental output power vs. input power: simulated (—) and measured (Δ)

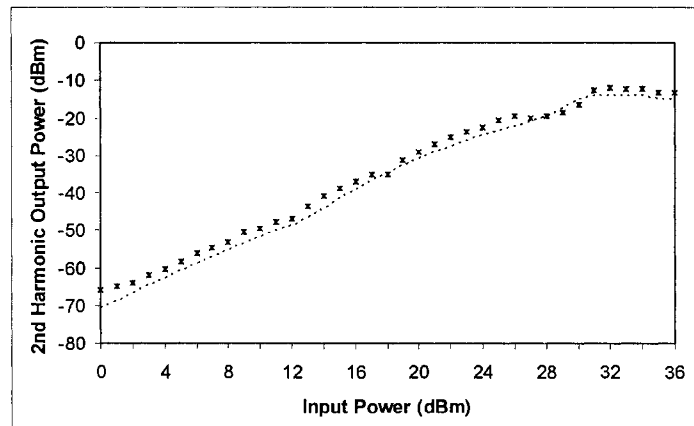


Fig. 6.4: Amplifier: Second harmonic output power vs. input power: simulated (--) and measured (*)

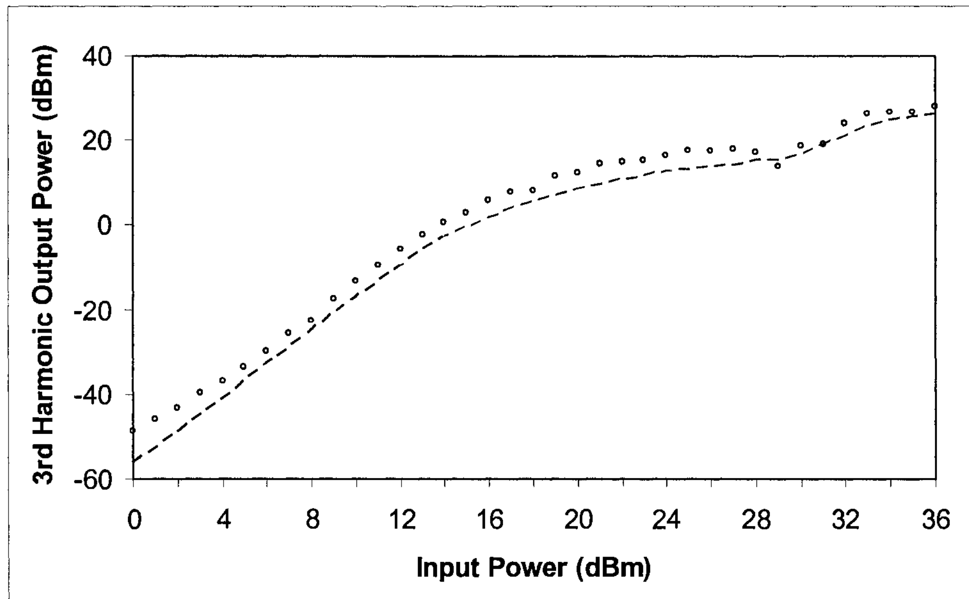


Fig. 6.5: Amplifier: Third harmonic output power vs. input power:

simulated (— —) and measured (o)

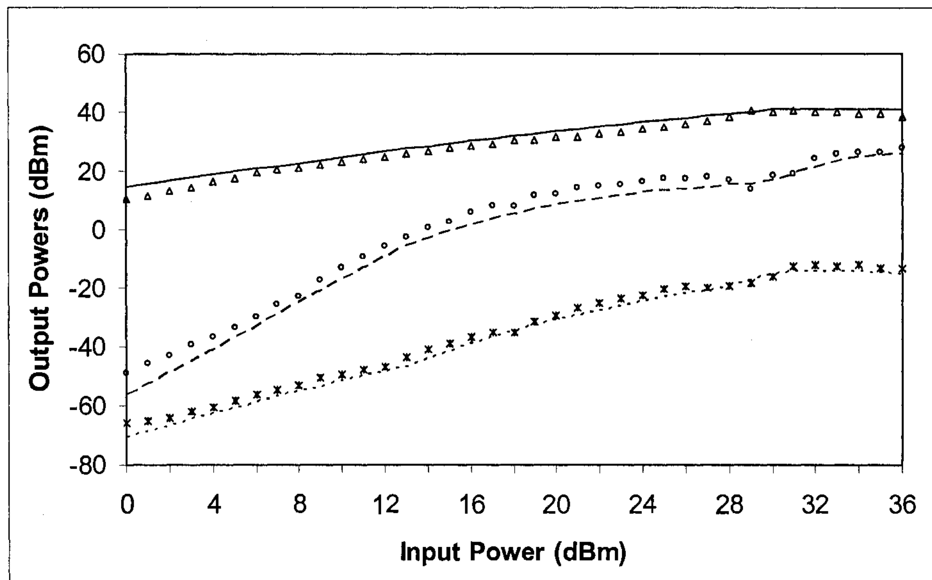


Fig. 6.6: Amplifier: Harmonic output powers vs. input power:

Fundamental output power: simulated (—) and measured (Δ)

Second harmonic output power: simulated (--) and measured (*)

Third harmonic output power: simulated (— —) and measured (o)

The gain and the PAE are displayed in Figure 6.7 and 6.8, respectively.

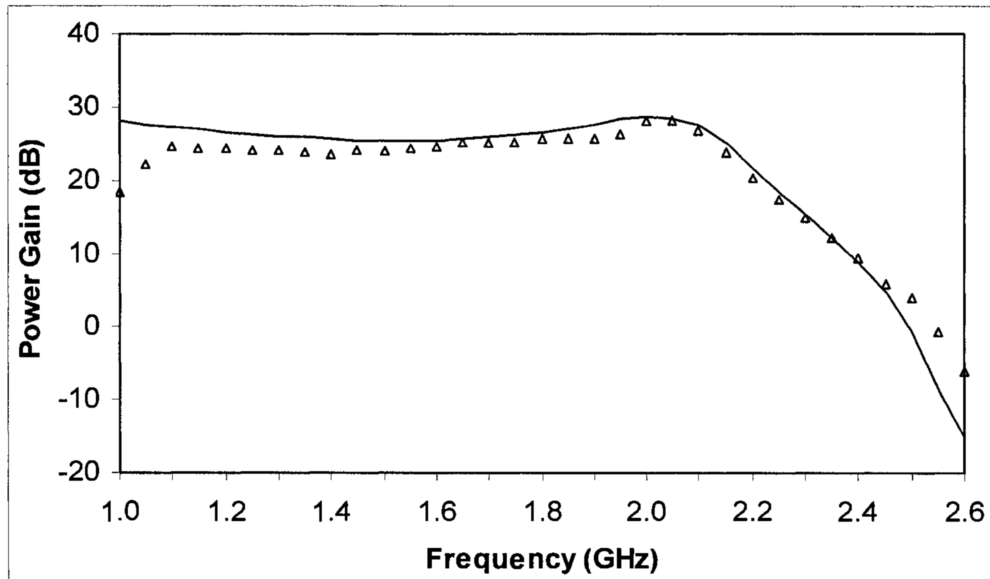


Fig. 6.7: Amplifier: Simulated (—) and measured (△) power gain vs. frequency

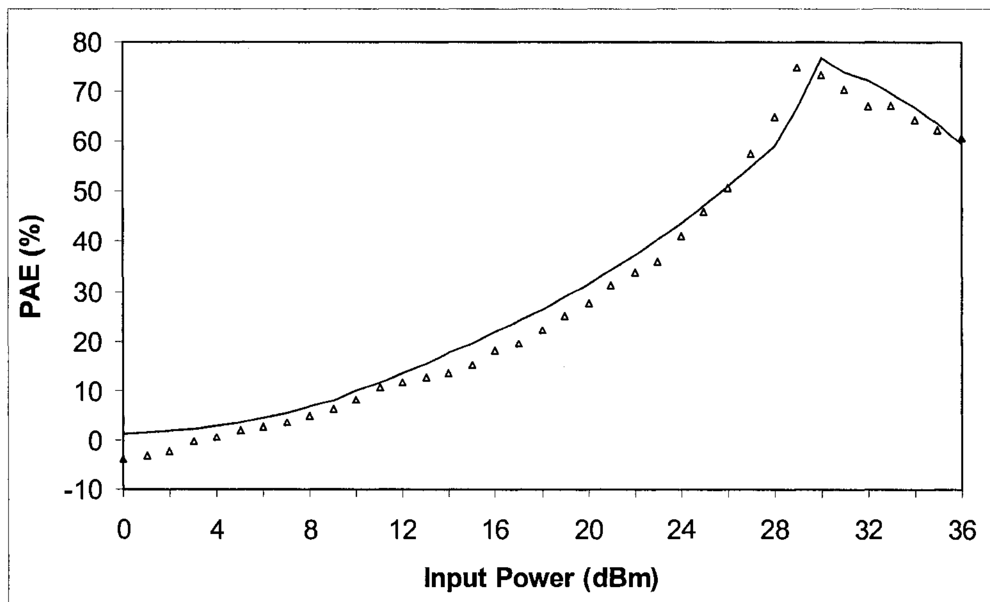


Fig. 6.8: Amplifier: Simulated (—) and measured (△) PAE in (%)

These curves exhibit some differences between simulated and measured curves. Such differences could be, in part, due to the differences we noticed between the transistor S parameters (Tables 5.3 and 5.4). For sure, the best would be to measure the transistor S parameters. However, due to practical constraints (the load-pull bench is operational but we were not able to find a transistor test fixture that can fit with our transistor), we were not able to perform such measurements. Therefore, we had to deal with simulated or datasheet values, knowing that those values are still approximate and cannot replace measured values.

Based on these considerations, we optimized the amplifier input/output matching networks.

For information, the S parameters of the two amplifiers are displayed in Figures 6.9 to 6.12.

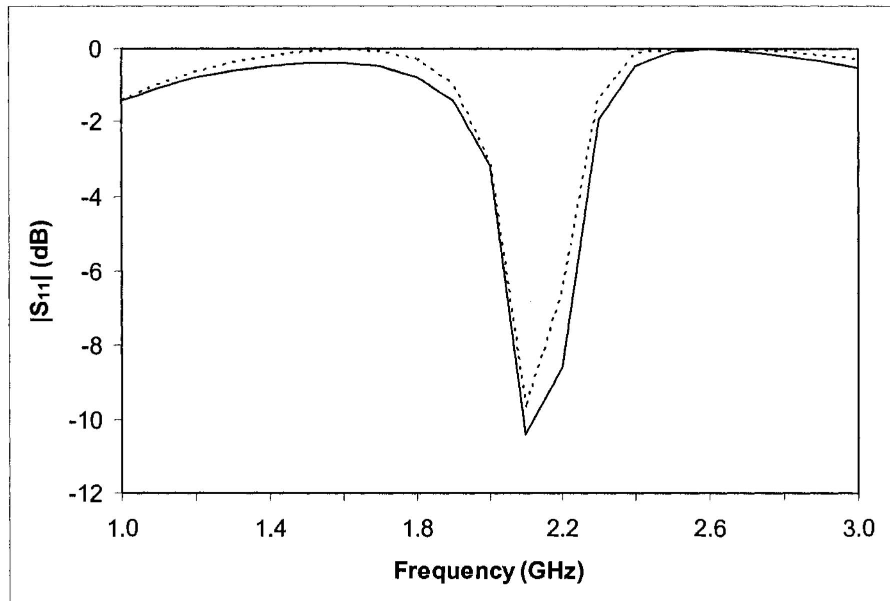


Fig. 6.9: Comparison of the S_{11} magnitude of the designed amplifier: First design (--) and second design (—)

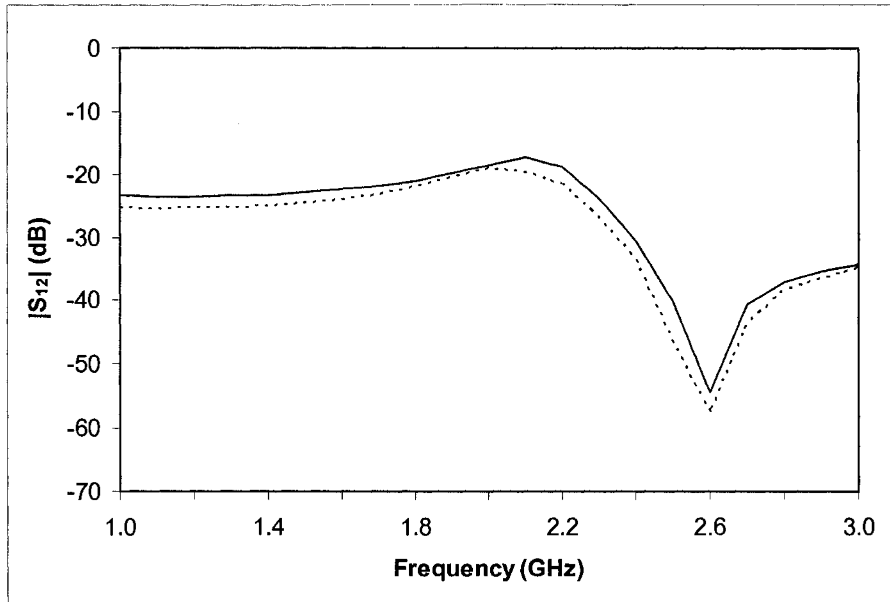


Fig. 6.10: Comparison of the S_{12} magnitude of the designed amplifier:
First design (--) and second design (—)

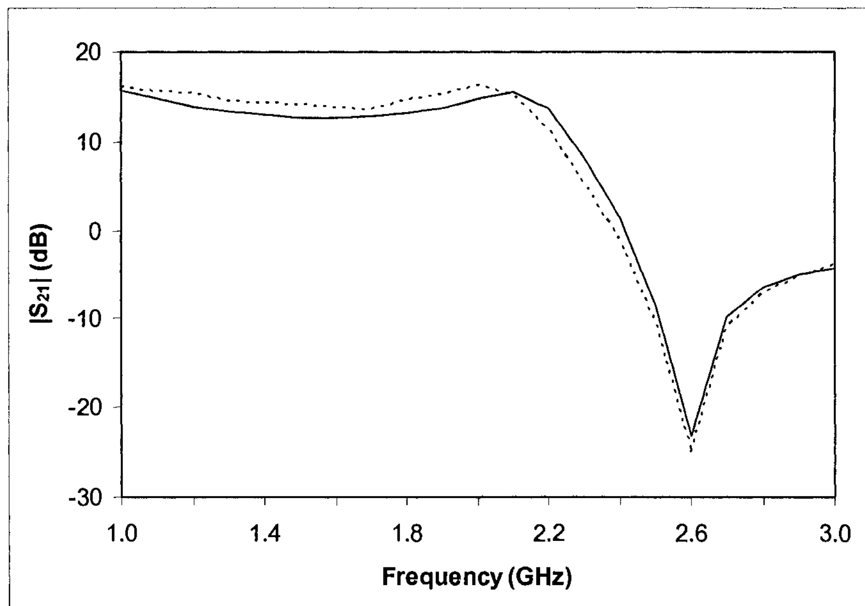


Fig. 6.11: Comparison of the S_{21} magnitude of the designed amplifier:
First design (--) and second design (—)

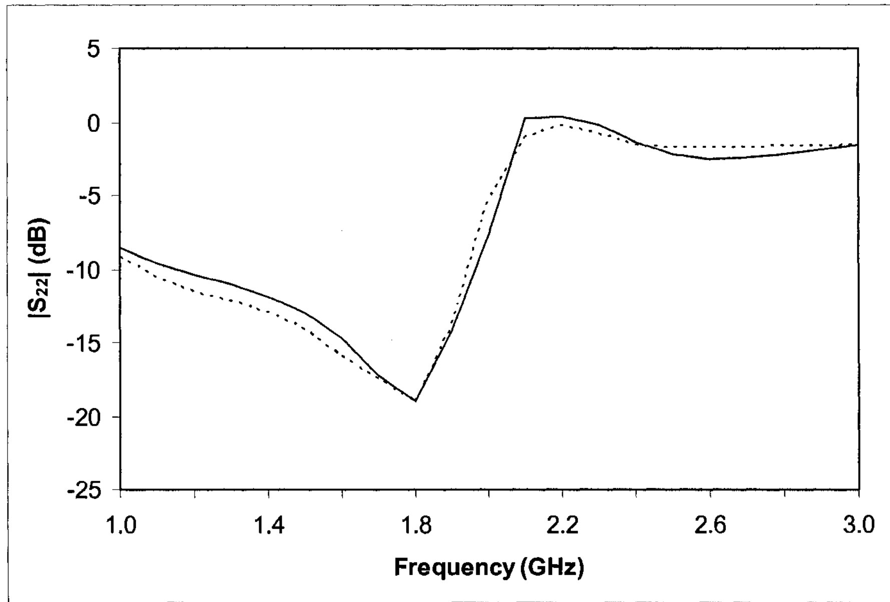


Fig. 6.12: Comparison of the S_{11} magnitude of the designed amplifier:
First design (--) and second design (—)

A picture of the amplifier is displayed in Figure 6.13.

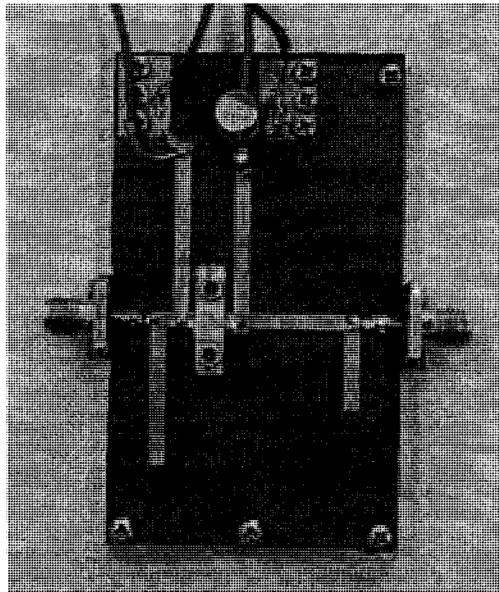


Fig. 6.13: Picture of the realized class F power amplifier

These changes allowed us to achieve a better design. In fact, as shown in Figure 6.14 we obtained a better PAE (75.9%), more close to the expected simulated value (76.8%) than the one obtained for the first amplifier (74.7%). These results were achieved for an optimum input power of 29.6 dBm close to the one obtained by simulation (30 dBm).

Furthermore, the power gain is better in the desired bandwidth (Figure 6.15).

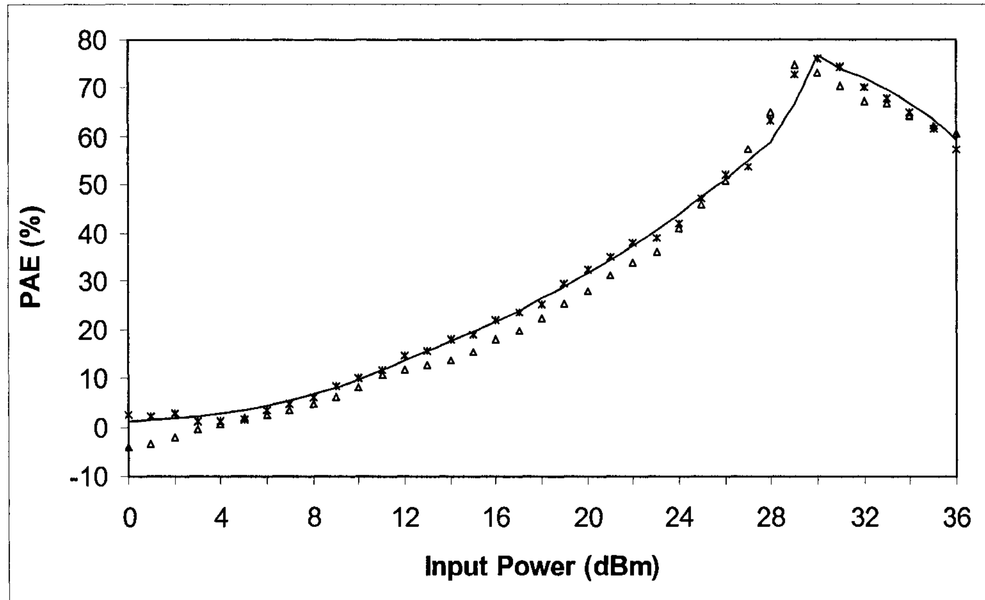


Fig. 6.14: Amplifier: PAE in (%): simulated (—), measured for the first amplifier (▵), measured for the second amplifier (*)

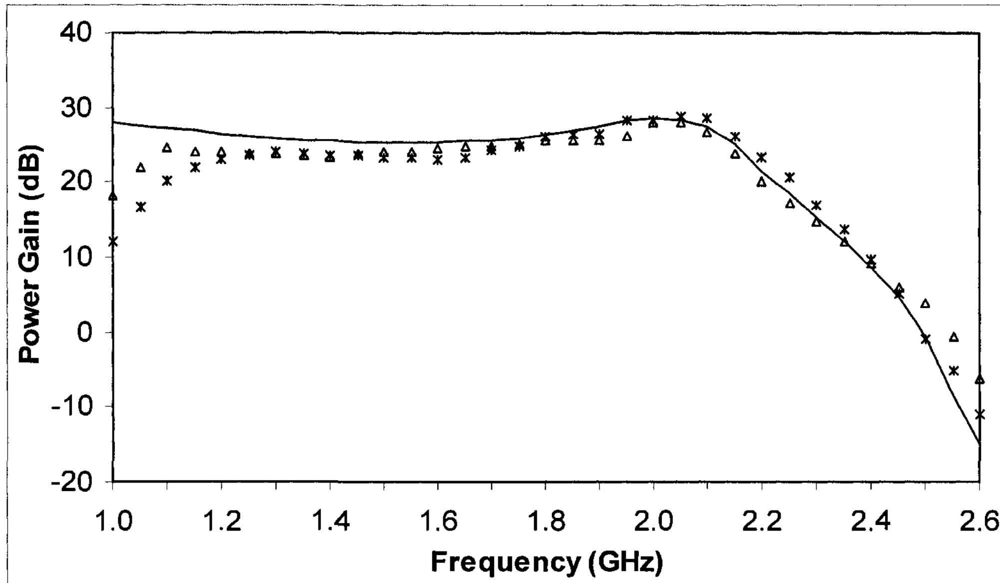


Fig. 6.15: Amplifier: Power gain: simulated (—), measured for the first amplifier (∆), measured for the second amplifier (*)

An inverse class F amplifier was also designed. Biasing the transistor, designing the input and output matching network were same as for class F amplifier except harmonic terminations. As we know, in a class-F amplifier, a high impedance is presented to all odd harmonics whereas a low impedance is presented to all even harmonics. As a result, the drain voltage is square wave and the drain current is half sinusoid. On the other hand for the inverse class-F amplifier, the waveforms are interchanged requiring the opposite harmonic terminations. Here, the current is square wave and the voltage is a half sine wave. To provide the third harmonic termination and second harmonic peaking for inverse class F operation, a RF short-circuited λ/6 microstrip line together with a combination of series microstrip line and open-circuit stub of λ/8 electrical length were used [50]. The simulated power gain, PAE curves and the schematic of the designed inverse class F amplifier are given in Figure 6.16, 6.17 and 6.18 respectively.

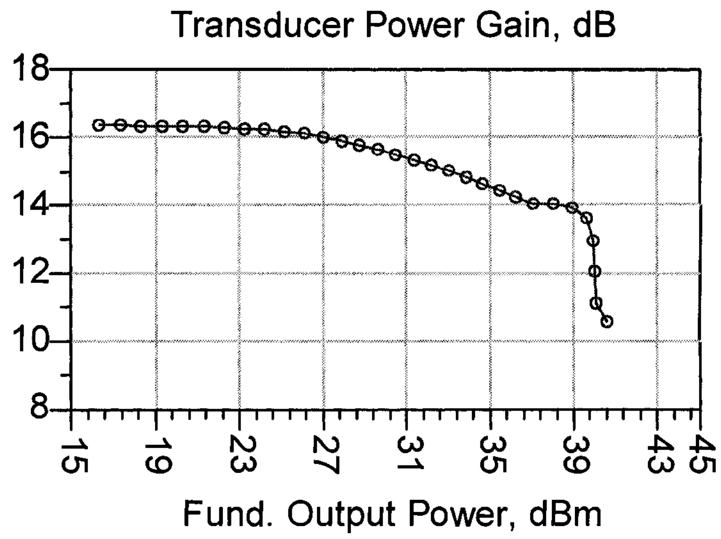


Fig 6.16: Plot of transducer power gain (dB) vs output power (dBm)

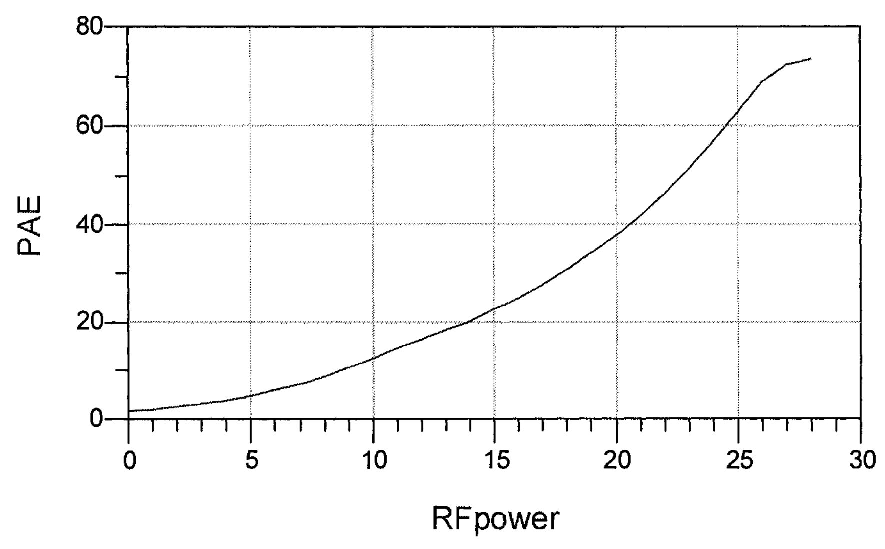


Fig 6.17: PAE (%) vs input power (dBm)

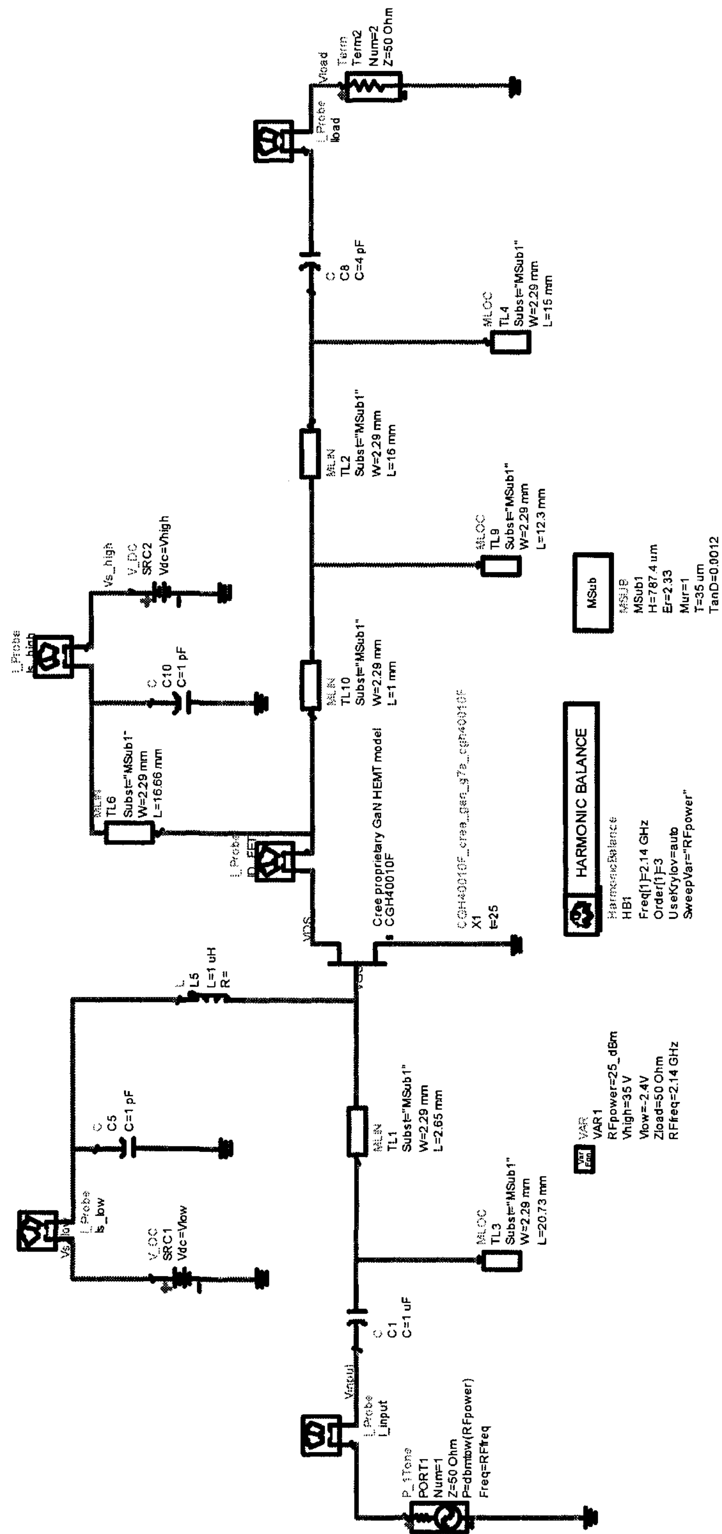


Fig 6.18: Schematic of the designed inverse class F amplifier

The designed inverse class F amplifier showed a maximum of around 74% PAE for an optimum input power of 28 dBm. According to theory, inverse class F amplifiers show better efficiency than class F amplifiers. Since we were not able to obtain more PAE with the inverse class F amplifier than the designed class F one and our main goal was to achieve better PAE, the inverse class F amplifier was not fabricated.

6.3 Conclusion

We designed and simulated a class-F amplifier. The amplifier has been simulated using a high frequency circuit simulator namely, the Agilent Advanced Design System (ADS). The simulated results have shown a Power Added Efficiency (PAE) of 76.8% for an optimum input power of 30 dBm. The value of third and fifth order IM products of the designed class F PA is -13 dBc and -21 dBc respectively at peak power and -28.5 dBc and -43 dBc respectively at 6 dB back-off from peak power. The amplifier was then fabricated and measured. After noticed the differences between measured and simulated results, we optimized the input/output matching networks. Measurement has shown a PAE of 75.9% for an optimum input power of 29.6 dBm which is in good accordance with the simulated results. Based on a literature review, and to the best of our knowledge, our circuit exhibited one of the highest measured PAE for a GaN class-F amplifier working at 2.14 GHz. An inverse class F amplifier was also designed and simulated. Since the efficiency was less than that of the class F amplifier, it was not fabricated.

Table 6.1: Comparison of performances of various class F PAs

Reference	51	52	53	54	55	This work
f_c (GHz)	2	2	1.9	2.4	2.14	2.14
PAE (%)	70.5	76	63	59	70.9	75.9
P_{out} (dBm)	19.85	21	30	22.2	40.2	40.8
Device	GaAs pHEMT	GaAs pHEMT	GaAs FET	GaAs MESFET	GaN HEMT	GaN HEMT

Chapter 7 Conclusion

7.1 Summary

In this work, a class F amplifier for WCDMA applications has been designed, simulated and measured using a GaN transistor from Cree Inc. The amplifier was biased as class AB amplifier.

In the course of this dissertation, the conventional PA types such as class A, AB, B and C as well as high efficiency PA such as class E were discussed. Following this, a detailed discussion on the theory of the class F amplifier was provided.

Based on the concept, a class F amplifier was designed. The selection of optimum bias points, design of input and output matching networks and the design of appropriate harmonic terminations were discussed. The design was simulated using Agilent's Advanced Design System. Two amplifiers were then fabricated and measured to improve the circuit PAE. The simulated and measured results were compared and acceptable agreement was found. An inverse class F amplifier was also designed and simulated. Since the efficiency was less than that of the class F amplifier, it was not fabricated.

7.2 Conclusion

The feasibility of class F amplifiers for WCDMA applications has been shown in this thesis by achieving around 76% PAE with acceptable linearity. At this frequency, and to the best of our knowledge, this is one of the highest PAEs exhibited by a Class-F amplifier based on a GaN transistor. Therefore, the key contributions of this thesis are as follows:

- A class F amplifier with a center frequency of 2.14 GHz for the WCDMA standard has been designed and simulated using a commer-

cial GaN transistor. The PA shows a maximum of 76.8% at around 30 dBm input power.

- Measurements have shown a PAE of 75.9% for an optimum input power of 29.6 dBm which is in good accordance with the simulated results.
- Based on a literature review, and to the best of our knowledge, our circuit exhibited one of the highest measured PAE (75.9%) for a GaN class-F amplifier working at 2.14 GHz [56-63].
- An inverse class-F amplifier has been simulated but not fabricated since it did not improve the obtained PAE.

7.3 Future Work

Several directions can be noted as for the expansion of this thesis.

- First of all, we used a commercial transistor form Cree Inc. principally because of its availability and thus, did not investigate for more other commercial transistors. However, an exhaustive review should be performed to select the most suitable GaN transistor for the desired bandwidth, output power, and PAE.
- From that, a whole large-signal transistor model should be generated to achieve proper design and to facilitate the amplifier performance optimization based on the transistor bias and its matching networks.
- The designed class-F PA can be used as the main PA within Doherty architecture in order to provide high efficiency at back off region to be utilized in 3G applications.
- The linearity of the designed class-F PA can be improved without degrading efficiency to meet more strict application requirements.
- Inverse class-F amplifiers have to be investigated more in details to obtain higher PAE.

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Appendix A: Measurement Setup

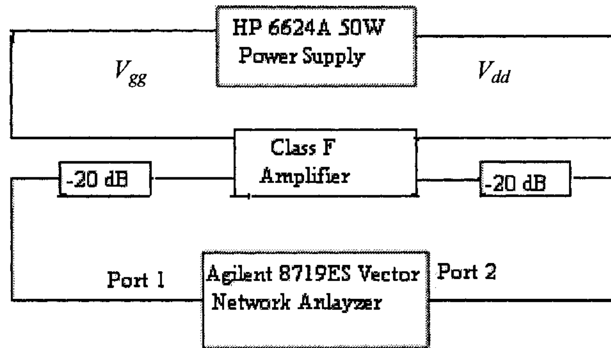


Figure A-1: Test bench for small signal measurements

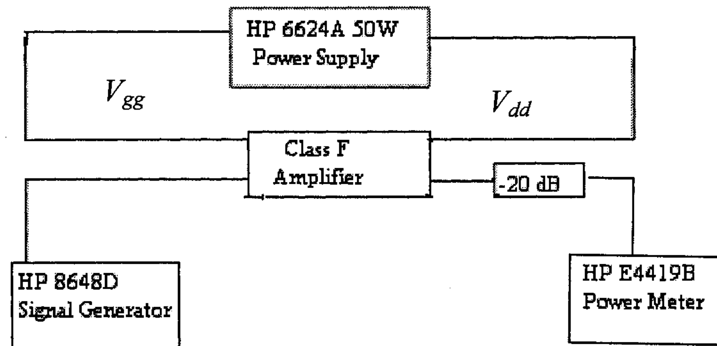


Fig A-2: Test bench for large signal measurements

Appendix B: CGH40010F Data Sheets

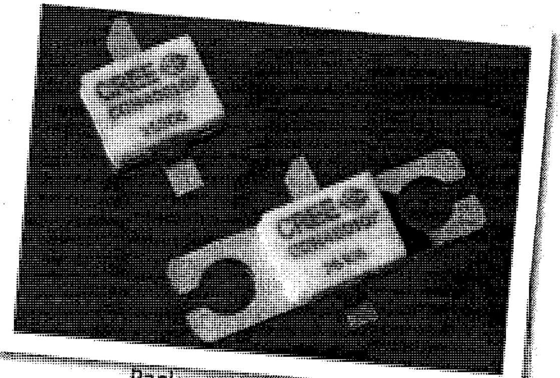
The datasheets of the GaN transistor from Cree Inc. are as follow.

PRELIMINARY

CGH40010

10 W, RF Power GaN HEMT

Cree's CGH40010 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40010, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. The transistor is available in both screw-down, flange and solder-down, pill packages.



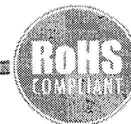
Package Types: 440166, & 440196
PN's: CGH40010F & CGH40010P

FEATURES

- Up to 4 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical P_{3dB}
- 65 % Efficiency at P3dB
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms



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Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	84	Volts
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts
Storage Temperature	T_{STG}	-55, +150	°C
Operating Junction Temperature	T_J	175	°C
Maximum Forward Gate Current	I_{GMAX}	4.0	mA
Soldering Temperature	T_S	245	°C
Thermal Resistance, Junction to Case [1]	$R_{\theta JC}$	5.0	°C/W
Screw Torque	T	60	in-oz

Note:
[1] Measured for the CGH40010F at P_{DISS} = 14 W.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[4]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.0	-2.5	-1.8	VDC	V_{DS} = 10 V, I_D = 3.6 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.0	–	VDC	V_{DS} = 28 V, I_D = 200 mA
Saturated Drain Current	I_{DS}	2.4	2.7	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	84	100	–	VDC	V_{GS} = -8 V, I_D = 3.6 mA
Case Operating Temperature	T_C	-10	–	+105	°C	
RF Characteristics (T_C = 25°C, F_0 = 3.7 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	12.5	14.5	–	dB	V_{DD} = 28 V, I_{DQ} = 200 mA
Power Output at 3 dB Compression	P_{3dB}	10	12.5	–	W	V_{DD} = 28 V, I_{DQ} = 200 mA
Drain Efficiency[1,2]	η	55	65	–	%	V_{DD} = 28 V, I_{DQ} = 200 mA, P_{3dB}
Output Mismatch Stress	VSWR	–	TBD	–	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 200 mA, P_{OUT} = 12 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	5.00	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	1.32	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.43	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Drain Efficiency = P_{OUT} / P_{DC}
[2] When tuned for best efficiency (see the applications chart in this data sheet).
[3] When tuned for best P_{1dB} (see the applications chart in this data sheet).
[4] Measured on wafer prior to packaging.

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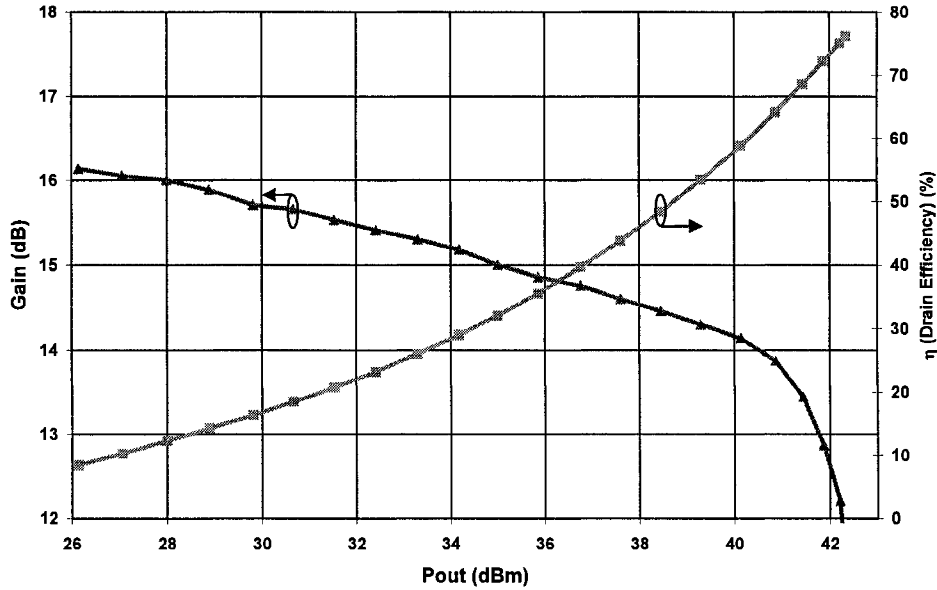
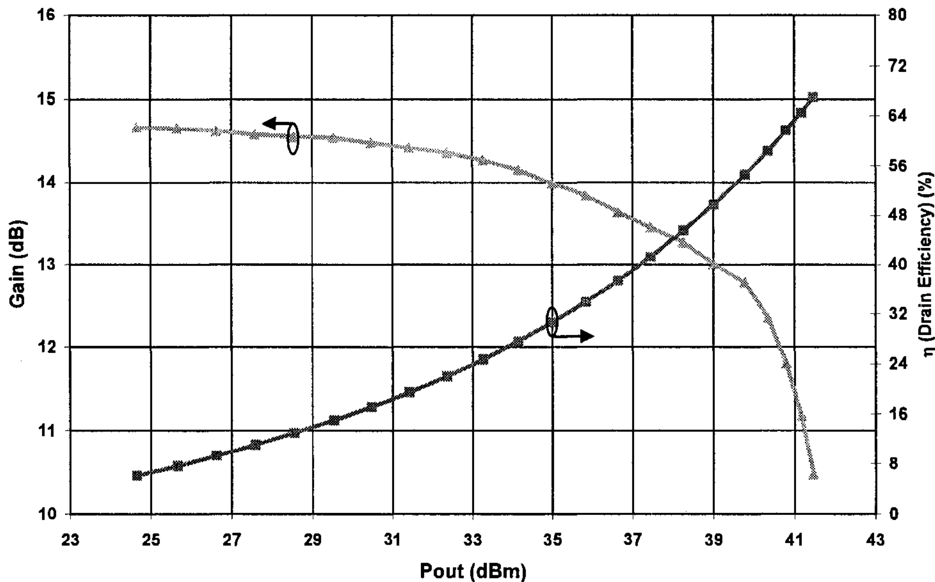
Typical Performance

Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 2.0 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA, Freq = 2.0 GHz



Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA, Freq = 3.6 GHz



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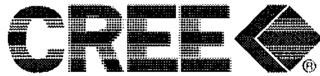
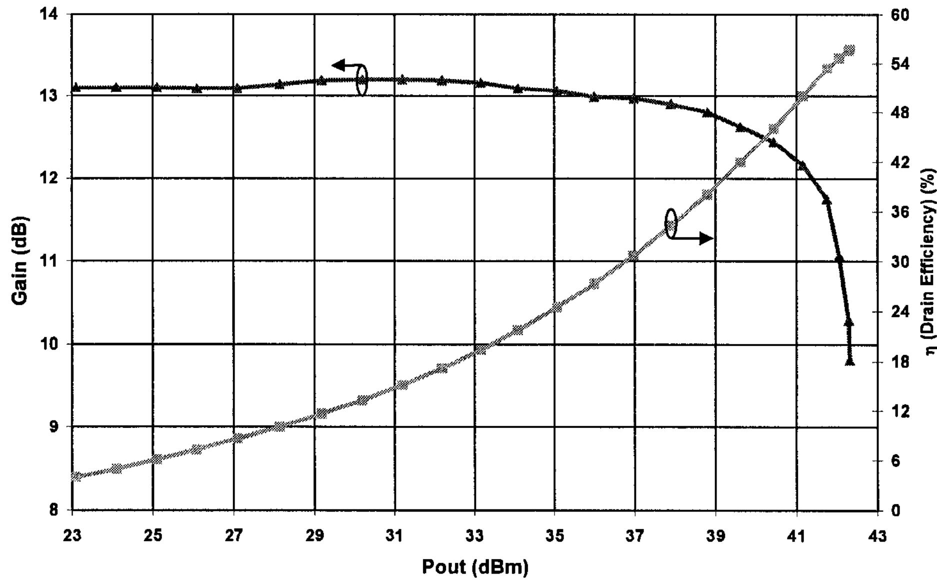
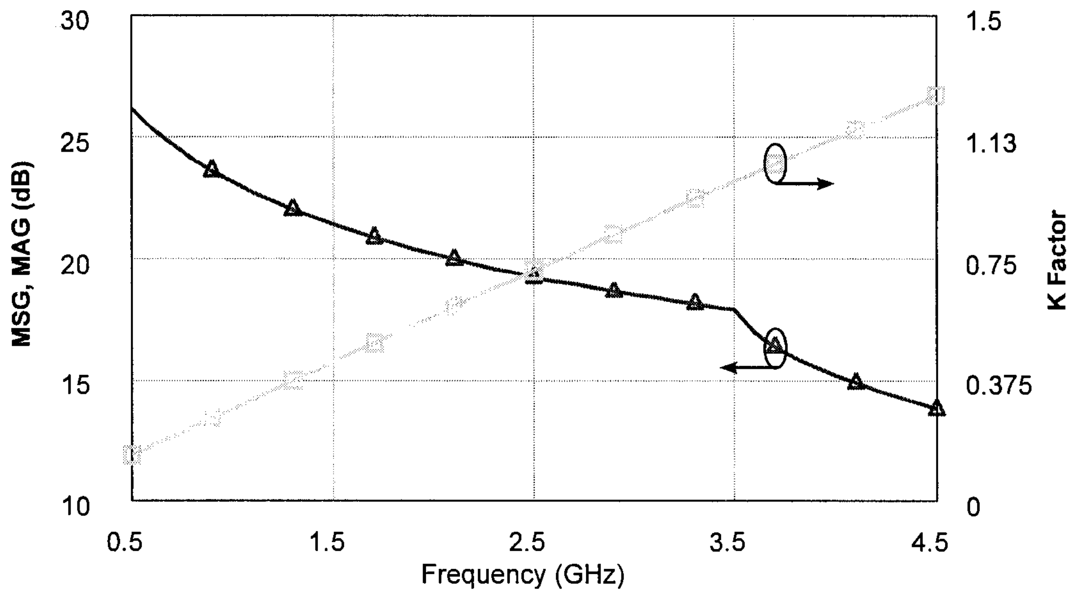


Typical Performance

Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for P1 Power at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA, Freq = 3.6 GHz



Simulated Maximum Stable Gain, Maximum Available Gain and K Factor of the CGH40010F
V_{DD} = 28 V, I_{DQ} = 200 mA



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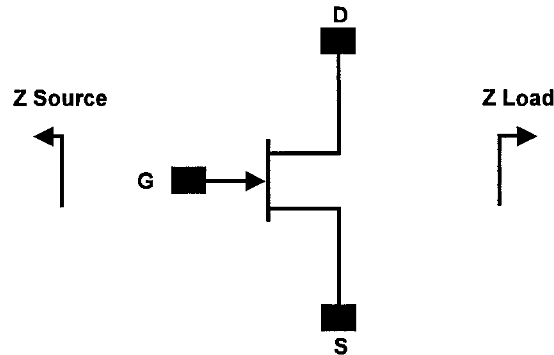
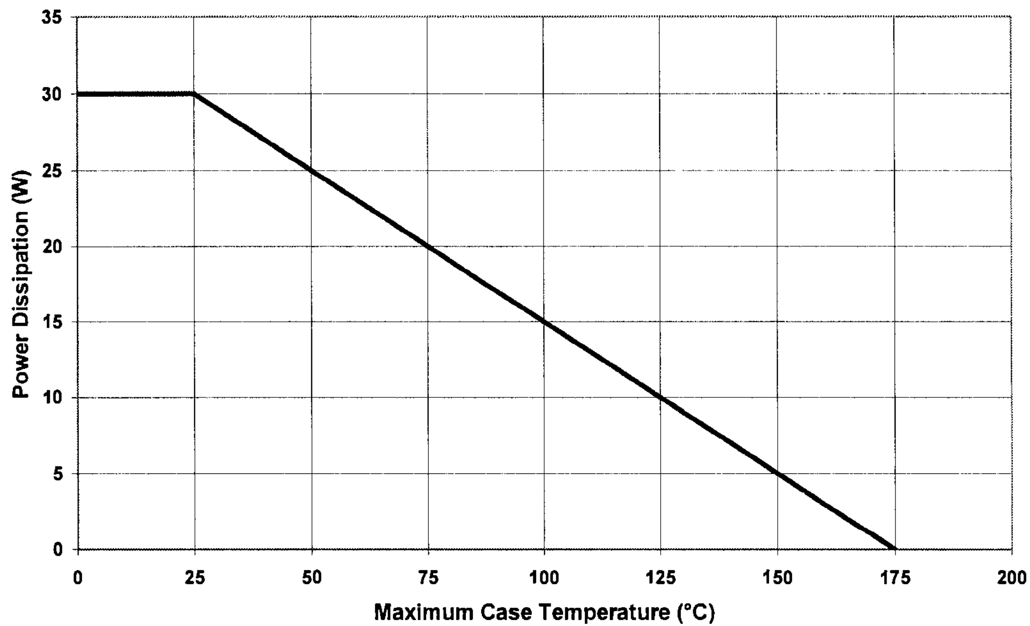
Source and Load Impedances



Frequency (MHz)	Z Source	Z Load
500	13.1 + j17	15.6 + j13.4
1000	9.2 + j10.7	12.96 + j8.25
1500	6.4 + j3.9	8.78 + j3.9
2500	4.0 - j4.0	6.37 - j0.1
3500	3.8 - j10.4	5.45 - j5.1

Note 1. V_{DD} = 28V, I_{DQ} = 200mA in the 440166 package.
Note 2. Optimized for P_{1dB}

CGH40010 Power Dissipation De-rating Curve



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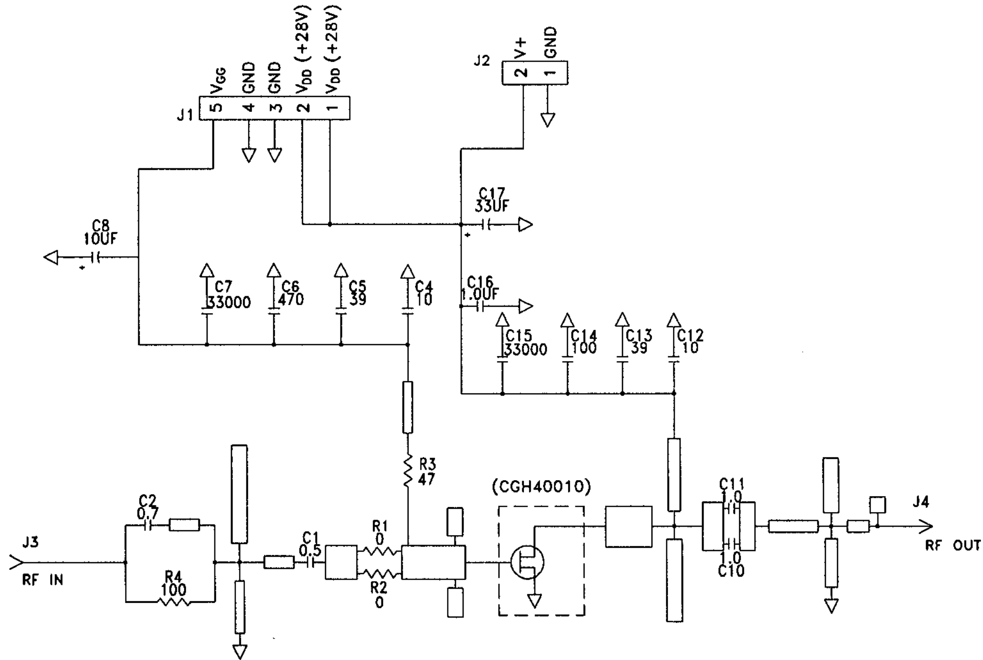
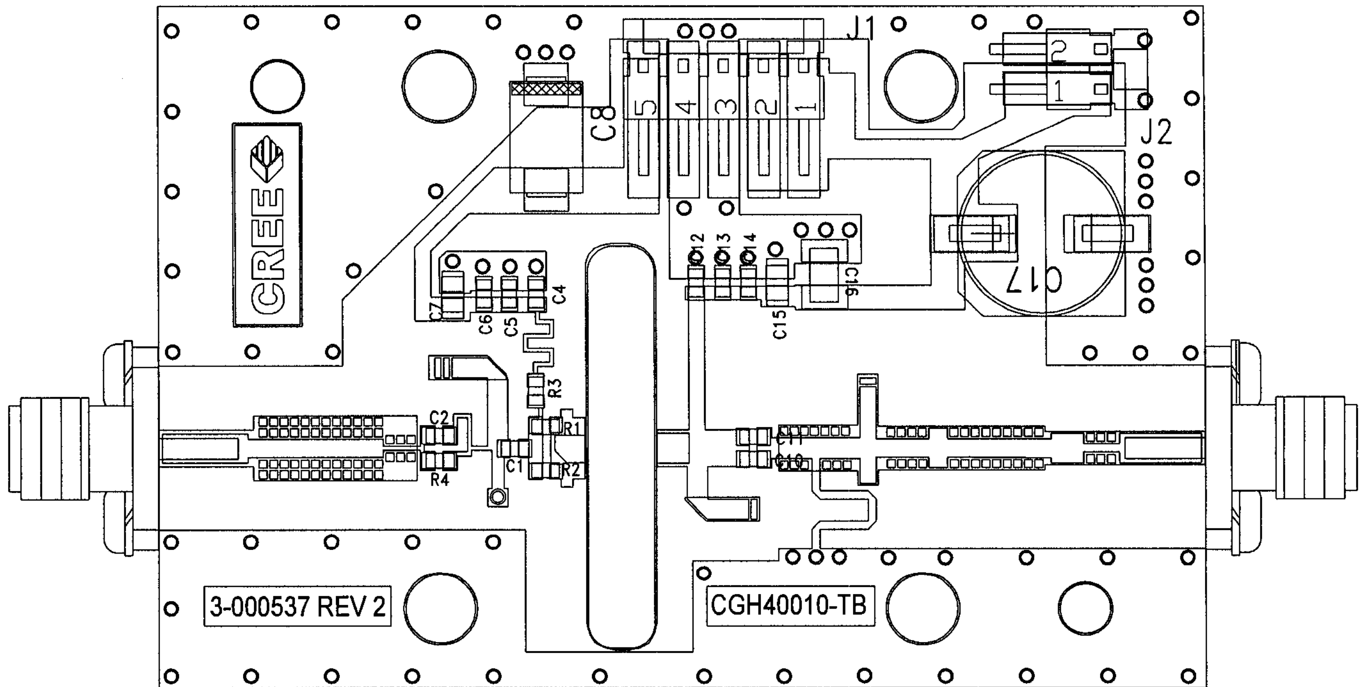
CGH40010-TB Demonstration Amplifier Circuit Schematic



CGH40010-TB Demonstration Amplifier Circuit Outline



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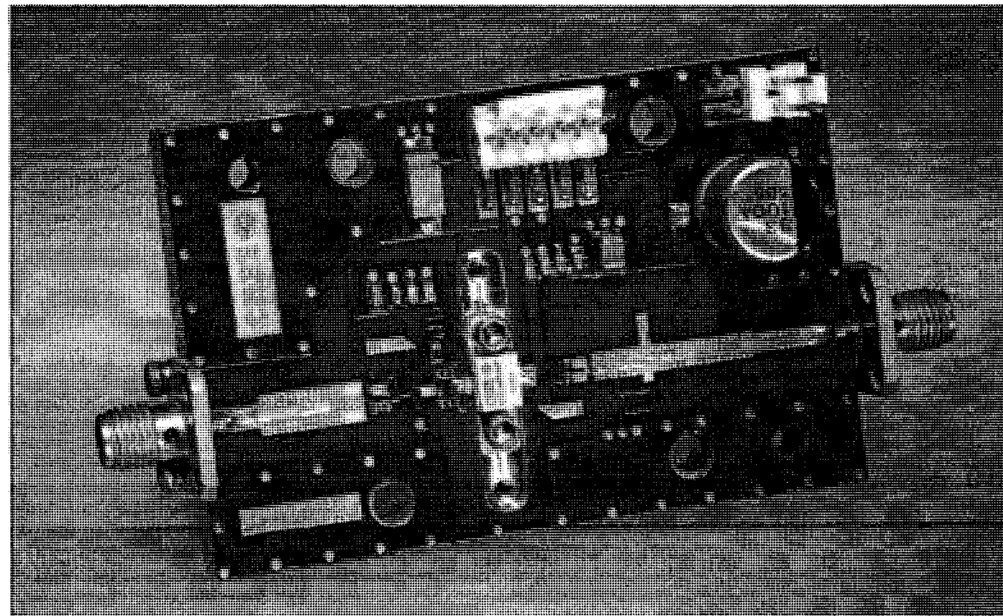
CGH40010-TB Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1,R2	RES,1/16W,0603,1%,0 OHMS	1
R3	RES,1/16W,0603,1%,47 OHMS	1
R4	RES,1/16W,0603,1%,100 OHMS	1
C6	CAP, 470PF, 5%,100V, 0603	1
C17	CAP, 33 UF, 20%, G CASE	1
C16	CAP, 1.0UF, 100V, 10%, X7R, 1210	1
C8	CAP 10UF 16V TANTALUM	1
C14	CAP, 100.0pF, +/-5%, 0603	1
C1	CAP, 0.5pF, +/-0.05pF, 0603	1
C2	CAP, 0.7pF, +/-0.1pF, 0603	1
C10,C11	CAP, 1.0pF, +/-0.1pF, 0603	2
C4,C12	CAP, 10.0pF,+/-5%, 0603	2
C5,C13	CAP, 39pF, +/-5%, 0603	2
C7,C15	CAP,33000PF, 0805,100V, X7R	2
J3,J4	CONN SMA STR PANEL JACK RECP	1
J2	HEADER RT>PLZ.1CEN LK 2 POS	1
J1	HEADER RT>PLZ .1CEN LK 5POS	1
Q1	CGH40010F or CGH40010P	1

CGH40010F-TB Demonstration Amplifier Circuit



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Typical Package S-Parameters for CGH40010F
(Small Signal, V_{DS} = 28 V, I_{DQ} = 100 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.8785	-143.68	12.55	101.09	0.0373	14.45	0.5687	-156.56
600 MHz	0.8740	-151.05	10.64	96.46	0.0380	10.48	0.5767	-161.57
700 MHz	0.8711	-156.75	9.22	92.62	0.0384	7.32	0.5817	-165.41
800 MHz	0.8690	-161.33	8.14	89.31	0.0386	4.68	0.5850	-168.51
900 MHz	0.8675	-165.16	7.27	86.35	0.0388	2.40	0.5872	-171.09
1.0 GHz	0.8664	-168.44	6.58	83.65	0.0390	0.38	0.5888	-173.31
1.1 GHz	0.8655	-171.33	6.00	81.14	0.0391	-1.46	0.5900	-175.27
1.2 GHz	0.8647	-173.91	5.52	78.77	0.0392	-3.15	0.5909	-177.04
1.3 GHz	0.8641	-176.25	5.12	76.51	0.0392	-4.73	0.5915	-178.65
1.4 GHz	0.8635	-178.42	4.77	74.33	0.0393	-6.23	0.5920	179.86
1.5 GHz	0.8630	179.56	4.46	72.22	0.0394	-7.65	0.5923	178.46
1.6 GHz	0.8625	177.66	4.20	70.17	0.0394	-9.02	0.5926	177.14
1.7 GHz	0.8620	175.86	3.96	68.15	0.0395	-10.35	0.5927	175.87
1.8 GHz	0.8615	174.13	3.75	66.18	0.0395	-11.63	0.5928	174.65
1.9 GHz	0.8610	172.47	3.57	64.23	0.0395	-12.89	0.5928	173.48
2.0 GHz	0.8606	170.86	3.40	62.31	0.0396	-14.11	0.5928	172.33
2.1 GHz	0.8601	169.29	3.25	60.41	0.0396	-15.32	0.5927	171.21
2.2 GHz	0.8597	167.76	3.11	58.53	0.0397	-16.50	0.5925	170.11
2.3 GHz	0.8592	166.26	2.99	56.66	0.0397	-17.67	0.5924	169.02
2.4 GHz	0.8587	164.79	2.87	54.80	0.0397	-18.83	0.5922	167.95
2.5 GHz	0.8582	163.33	2.77	52.94	0.0398	-19.97	0.5919	166.89
2.6 GHz	0.8577	161.89	2.67	51.10	0.0398	-21.10	0.5916	165.83
2.7 GHz	0.8571	160.46	2.58	49.26	0.0399	-22.23	0.5913	164.78
2.8 GHz	0.8566	159.04	2.50	47.42	0.0399	-23.35	0.5909	163.72
2.9 GHz	0.8560	157.62	2.42	45.58	0.0400	-24.46	0.5905	162.67
3.0 GHz	0.8555	156.21	2.35	43.74	0.0400	-25.57	0.5901	161.62
3.1 GHz	0.8549	154.80	2.29	41.91	0.0401	-26.68	0.5896	160.56
3.2 GHz	0.8542	153.38	2.23	40.07	0.0401	-27.79	0.5891	159.49
3.3 GHz	0.8536	151.97	2.17	38.23	0.0402	-28.89	0.5886	158.42
3.4 GHz	0.8529	150.54	2.12	36.38	0.0402	-29.99	0.5880	157.34
3.5 GHz	0.8523	149.11	2.07	34.53	0.0403	-31.10	0.5873	156.25
3.6 GHz	0.8516	147.68	2.02	32.68	0.0403	-32.20	0.5867	155.15
3.7 GHz	0.8508	146.23	1.98	30.81	0.0404	-33.31	0.5859	154.04
3.8 GHz	0.8501	144.77	1.94	28.95	0.0405	-34.41	0.5852	152.91
3.9 GHz	0.8493	143.30	1.90	27.07	0.0406	-35.52	0.5844	151.77
4.0 GHz	0.8486	141.81	1.86	25.18	0.0406	-36.64	0.5835	150.61
4.1 GHz	0.8478	140.31	1.83	23.29	0.0407	-37.76	0.5827	149.44
4.2 GHz	0.8469	138.79	1.79	21.38	0.0408	-38.88	0.5817	148.25
4.3 GHz	0.8461	137.25	1.76	19.46	0.0409	-40.01	0.5808	147.04
4.4 GHz	0.8452	135.70	1.73	17.53	0.0409	-41.15	0.5797	145.80
4.5 GHz	0.8443	134.12	1.71	15.59	0.0410	-42.29	0.5787	144.55

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(Small Signal, V_{DS} = 28 V, I_{DQ} = 200 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.884	-147.00	13.01	100.05	0.0316	14.05	0.6169	-163.03
600 MHz	0.881	-153.95	11.01	95.70	0.0320	10.50	0.6254	-167.20
700 MHz	0.878	-159.32	9.53	92.09	0.0323	7.70	0.6306	-170.47
800 MHz	0.877	-163.65	8.40	88.98	0.0326	5.39	0.6339	-173.14
900 MHz	0.875	-167.27	7.51	86.20	0.0327	3.41	0.6361	-175.43
1.0 GHz	0.874	-170.38	6.79	83.66	0.0328	1.67	0.6376	-177.42
1.1 GHz	0.873	-173.13	6.20	81.29	0.0329	0.11	0.6386	-179.22
1.2 GHz	0.873	-175.60	5.70	79.06	0.0330	-1.32	0.6393	179.14
1.3 GHz	0.872	-177.85	5.28	76.92	0.0331	-2.65	0.6397	177.62
1.4 GHz	0.872	-179.93	4.92	74.86	0.0332	-3.91	0.6398	176.19
1.5 GHz	0.871	178.12	4.61	72.86	0.0333	-5.10	0.6399	174.83
1.6 GHz	0.871	176.27	4.33	70.91	0.0334	-6.24	0.6398	173.53
1.7 GHz	0.870	174.52	4.09	69.00	0.0334	-7.33	0.6396	172.27
1.8 GHz	0.870	172.83	3.88	67.12	0.0335	-8.40	0.6393	171.05
1.9 GHz	0.869	171.21	3.69	65.27	0.0336	-9.43	0.6389	169.86
2.0 GHz	0.868	169.63	3.51	63.43	0.0337	-10.45	0.6385	168.70
2.1 GHz	0.868	168.09	3.36	61.62	0.0338	-11.44	0.6379	167.55
2.2 GHz	0.867	166.59	3.22	59.82	0.0339	-12.42	0.6374	166.42
2.3 GHz	0.867	165.11	3.09	58.03	0.0339	-13.39	0.6367	165.29
2.4 GHz	0.866	163.65	2.98	56.25	0.0340	-14.35	0.6360	164.18
2.5 GHz	0.866	162.21	2.87	54.47	0.0341	-15.30	0.6353	163.07
2.6 GHz	0.865	160.78	2.77	52.70	0.0342	-16.24	0.6345	161.97
2.7 GHz	0.864	159.36	2.68	50.93	0.0343	-17.18	0.6336	160.87
2.8 GHz	0.864	157.95	2.60	49.16	0.0345	-18.11	0.6327	159.76
2.9 GHz	0.863	156.54	2.52	47.39	0.0346	-19.05	0.6318	158.66
3.0 GHz	0.862	155.13	2.45	45.62	0.0347	-19.98	0.6308	157.55
3.1 GHz	0.862	153.73	2.38	43.84	0.0348	-20.91	0.6297	156.43
3.2 GHz	0.861	152.32	2.32	42.06	0.0349	-21.84	0.6286	155.31
3.3 GHz	0.860	150.91	2.26	40.28	0.0351	-22.78	0.6275	154.18
3.4 GHz	0.859	149.49	2.21	38.49	0.0352	-23.72	0.6263	153.04
3.5 GHz	0.859	148.06	2.16	36.70	0.0354	-24.66	0.6250	151.89
3.6 GHz	0.858	146.63	2.11	34.90	0.0355	-25.61	0.6237	150.73
3.7 GHz	0.857	145.18	2.07	33.09	0.0357	-26.56	0.6224	149.55
3.8 GHz	0.856	143.72	2.02	31.27	0.0358	-27.52	0.6210	148.37
3.9 GHz	0.855	142.25	1.98	29.44	0.0360	-28.48	0.6195	147.16
4.0 GHz	0.854	140.76	1.95	27.59	0.0361	-29.46	0.6181	145.94
4.1 GHz	0.853	139.26	1.91	25.74	0.0363	-30.44	0.6165	144.71
4.2 GHz	0.852	137.74	1.88	23.88	0.0365	-31.43	0.6150	143.46
4.3 GHz	0.851	136.20	1.85	22.00	0.0367	-32.44	0.6133	142.18
4.4 GHz	0.850	134.65	1.82	20.11	0.0369	-33.45	0.6117	140.89
4.5 GHz	0.849	133.07	1.79	18.21	0.0371	-34.47	0.6100	139.58

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Typical Package S-Parameters for CGH40010F
(Small Signal, V_{DS} = 28 V, I_{DQ} = 500 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.8907	-150.63	13.47	98.92	0.0258	13.90	0.6803	-168.90
600 MHz	0.8877	-157.10	11.37	94.88	0.0261	10.86	0.6882	-172.30
700 MHz	0.8858	-162.09	9.83	91.55	0.0264	8.52	0.6930	-175.03
800 MHz	0.8844	-166.13	8.66	88.67	0.0265	6.63	0.6960	-177.33
900 MHz	0.8834	-169.52	7.73	86.09	0.0267	5.05	0.6980	-179.33
1.0 GHz	0.8825	-172.46	6.99	83.72	0.0268	3.68	0.6992	178.87
1.1 GHz	0.8818	-175.05	6.38	81.52	0.0269	2.47	0.7000	177.23
1.2 GHz	0.8812	-177.40	5.87	79.43	0.0270	1.37	0.7004	175.70
1.3 GHz	0.8806	-179.54	5.44	77.43	0.0271	0.37	0.7006	174.26
1.4 GHz	0.8801	178.46	5.07	75.51	0.0272	-0.57	0.7006	172.89
1.5 GHz	0.8795	176.58	4.74	73.63	0.0274	-1.45	0.7004	171.56
1.6 GHz	0.8790	174.80	4.46	71.81	0.0275	-2.29	0.7001	170.28
1.7 GHz	0.8785	173.10	4.22	70.01	0.0276	-3.10	0.6996	169.03
1.8 GHz	0.8779	171.47	4.00	68.24	0.0277	-3.88	0.6991	167.81
1.9 GHz	0.8774	169.88	3.80	66.50	0.0278	-4.64	0.6984	166.61
2.0 GHz	0.8768	168.34	3.63	64.77	0.0280	-5.38	0.6977	165.42
2.1 GHz	0.8762	166.83	3.47	63.06	0.0281	-6.11	0.6969	164.24
2.2 GHz	0.8756	165.35	3.33	61.36	0.0283	-6.83	0.6961	163.07
2.3 GHz	0.8750	163.89	3.20	59.66	0.0284	-7.55	0.6952	161.91
2.4 GHz	0.8743	162.45	3.08	57.97	0.0286	-8.26	0.6942	160.75
2.5 GHz	0.8737	161.03	2.97	56.28	0.0288	-8.96	0.6931	159.60
2.6 GHz	0.8730	159.62	2.87	54.60	0.0289	-9.67	0.6920	158.44
2.7 GHz	0.8723	158.21	2.78	52.92	0.0291	-10.38	0.6908	157.28
2.8 GHz	0.8715	156.81	2.69	51.23	0.0293	-11.10	0.6896	156.12
2.9 GHz	0.8708	155.41	2.61	49.54	0.0295	-11.81	0.6883	154.95
3.0 GHz	0.8700	154.01	2.54	47.85	0.0297	-12.54	0.6869	153.78
3.1 GHz	0.8692	152.61	2.47	46.15	0.0299	-13.27	0.6855	152.60
3.2 GHz	0.8683	151.21	2.41	44.45	0.0301	-14.00	0.6840	151.41
3.3 GHz	0.8674	149.80	2.35	42.74	0.0304	-14.75	0.6825	150.21
3.4 GHz	0.8665	148.38	2.30	41.02	0.0306	-15.51	0.6809	149.00
3.5 GHz	0.8656	146.96	2.25	39.30	0.0309	-16.27	0.6793	147.78
3.6 GHz	0.8647	145.53	2.20	37.56	0.0311	-17.06	0.6776	146.54
3.7 GHz	0.8637	144.08	2.15	35.81	0.0314	-17.85	0.6758	145.29
3.8 GHz	0.8627	142.62	2.11	34.06	0.0316	-18.65	0.6740	144.03
3.9 GHz	0.8617	141.15	2.07	32.29	0.0319	-19.47	0.6722	142.75
4.0 GHz	0.8606	139.66	2.04	30.50	0.0322	-20.31	0.6703	141.46
4.1 GHz	0.8595	138.16	2.00	28.71	0.0325	-21.16	0.6683	140.14
4.2 GHz	0.8584	136.63	1.97	26.90	0.0328	-22.03	0.6663	138.81
4.3 GHz	0.8573	135.09	1.94	25.07	0.0331	-22.92	0.6643	137.46
4.4 GHz	0.8562	133.53	1.91	23.23	0.0334	-23.82	0.6622	136.09
4.5 GHz	0.8550	131.95	1.88	21.38	0.0338	-24.75	0.6600	134.69

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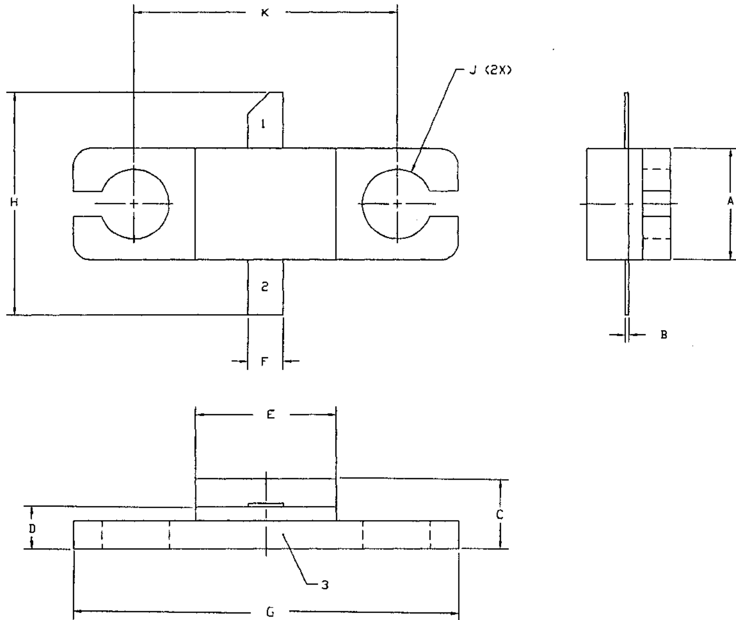
Product Dimensions CGH40010F (Package Type — 440166)



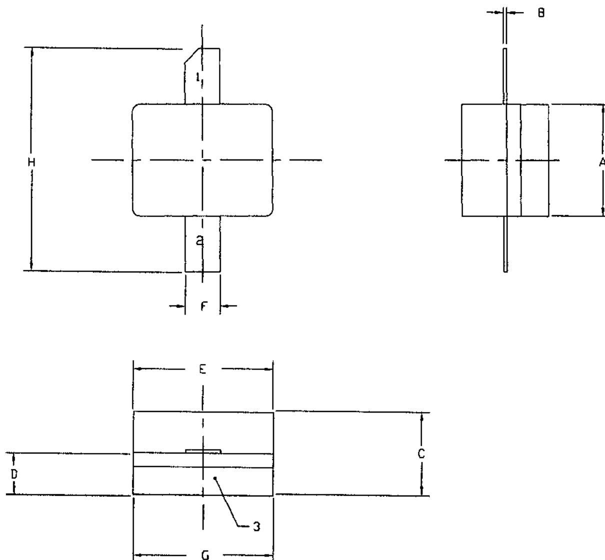
NOTES:

1. DIMENSIONING AND TOLERANICING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.004	0.006	0.10	0.15
C	0.115	0.135	2.92	3.43
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.545	0.555	13.84	14.09
H	0.280	0.360	7.87	8.38
J	ø .100		2.54	
K	0.375		9.53	

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

Product Dimensions CGH40010P (Package Type — 440196)



NOTES:

1. DIMENSIONING AND TOLERANICING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.003	0.006	0.10	0.15
C	0.115	0.135	2.92	3.17
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.195	0.205	4.95	5.21
H	0.280	0.360	7.112	9.114

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

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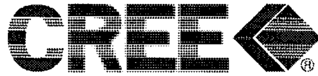

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