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Quantitative Capacitance Measurements Using a Scanning Probe Microscope

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Quantitative Capacitance Measurements Using a Scanning Probe Microscope

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Thesis submitted to the
Faculty of Graduate and Postdoctoral Studies
in partial fulfillment of the requirements
for the M.A.Sc. degree in Electrical Engineering

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I. Abstract

This thesis describes the theory, simulation and experimental implementation of a method by which an atomic force microscope with scanning capacitance microscopy (SCM) capability can be employed in a nontraditional fashion to quantitatively measure the capacitance of metal-oxide-semiconductor (MOS) structures.

The capability to deduce sample capacitances is based on resonant frequency shifting, which relies on the SCM's ultra-precise capacitance sensor. The technique, however, is distinct from scanning capacitance microscopy imaging, with the MOS capacitor an integral part of the system resonant circuit. SPICE simulations are performed to extract phenomenological resonant circuit parameters specific to the instrumentation, subsequently permitting sample capacitance to be quantitatively extracted from the system response.

Our technique represents a novel application of SCM instrumentation and has important applications in the analysis of on-chip passive components for future technology generations. Initial experimental results are promising, suggesting the extension of the technique to advanced technology nodes.

II. Acknowledgements

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VI. List of Acronyms

AFM – Atomic Force Microscope/Microscopy

SCM – Scanning Capacitance Microscope/Microscopy

SPM – Scanning Probe Microscope/Microscopy

MOS – Metal Oxide Semiconductor

ITRS – International Technology Roadmap for Semiconductors

DUT – Device Under Test

SSRM – Scanning Spreading Resistance Microscope/Microscopy

LIA – Lock-In Amplifier

1. Introduction

1.1. Motivation for work

Semiconductor integrated circuits are arguably one of the most pervasive items in modern life [1]. Present in everything from the clock radio that wakes us each morning to the electric toothbrush we use every night before bed, ICs are an integral part of our daily routine. Society's ravenous appetite for the modern conveniences provided by integrated circuits has contributed significantly to the semiconductor industry's unprecedented growth, both in rapid development of innovative designs and increased manufacturing volumes [2]. Though furious, the pace of this progress has been predictable to the point that a new term, Moore's law, was spawned to describe it.

Based on his observations of the growth of the electronics industry in the mid-1960's, Intel co-founder Gordon Moore predicted that the number of components incorporated into cutting-edge integrated circuits would double every two years [3]. As figure 1 demonstrates, manufacturing has progressed rapidly enough since that time to repeatedly obey this prophecy, and it has essentially become self-fulfilling [2]. In fact, a global consortium publishes a report every two years called the International Technology Roadmap for Semiconductors (ITRS), which includes short and long-term development targets for the industry based on the presumption that such an 18 to 24-month doubling cycle will persist. The roadmap also contains a discussion of imminent challenges and potential strategies for overcoming them, in order that Moore's Law might continue to hold true. In the 2005 edition of this document, it is predicted that with transistor dimensions in microprocessor units shrinking at the current rate, 2010 will see microprocessors containing over one billion transistors [4].

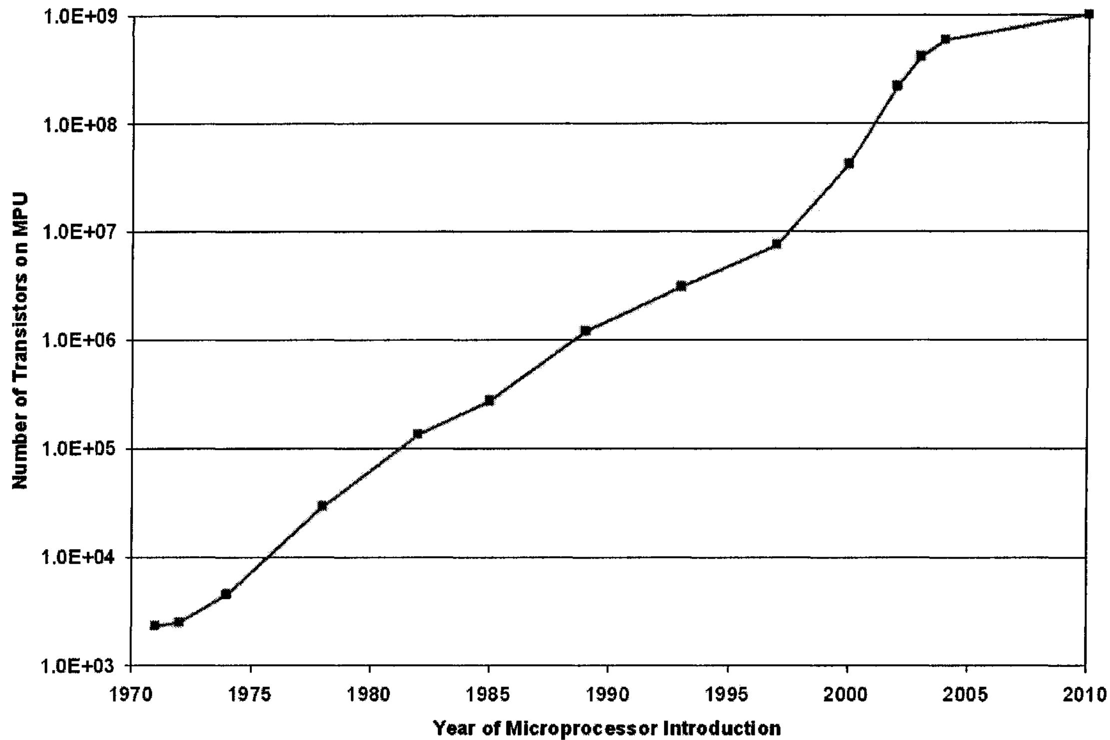


Figure 1 - Moore's law, as it applies to the number of transistors composing state-of-the-art microprocessor units. Source data from [5].

While metal-oxide-semiconductor (MOS) capacitors and transistors have traditionally incorporated silicon dioxide as an insulating material, the reduced dimensions projected for imminent generations of semiconductors will necessitate equivalent scaling of the insulating layer thickness [6], which spawns an important side effect. State-of-the-art designs are already beginning to exhibit leakage currents near tolerance levels, with unacceptable power dissipation levels, through these ultra-thin silica barriers [7]. The relentless march of progress marked by miniaturization has already begun to dictate that an alternative dielectric material, which can mimic the physical properties of a very thin SiO_2 layer while being thick enough to minimize current leakage, will soon be required in place of silicon dioxide [8], [9], [10]. It is important to be able to identify these exotic 'high-k' insulators to facilitate both device design and failure analysis processes [11], and measuring the capacitance they create is a direct method for doing so. Quantitative capacitance measurements on silicon structures

can allow the permittivity of unknown dielectric materials to be calculated [12], warranting our feasibility study to validate this method's usefulness as an analysis tool.

A typical parallel plate structure as the one shown in figure 2 will have capacitance as given in equation (1.1), below:

$$C = \frac{\varepsilon \varepsilon_0 A}{t_{ox}} \tag{1.1}$$

Since its value depends on both the dimensions of its charge-storing plates, and the thickness and permittivity of the insulating material separating them, one can employ measured capacitance along with observable physical dimensions to determine dielectric permittivity [12]. Unlike SiO_2 however, many of the dielectric materials in development can not yet be reliably incorporated into integrated circuits. The techniques for growth and deposition are still immature, and consequently they often yield erratic spatial composition and material properties [13]. To a manufacturer, the method proposed here could serve as a valuable tool for performing in-process characterization of such structures, allowing recipes to be refined at an early stage of the manufacturing sequence if necessary.

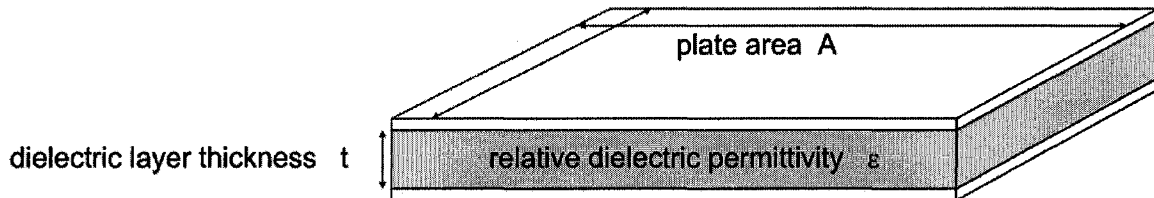


Figure 2 - Ideal capacitor model showing capacitance-dependent dimensions and material properties.

1.2. Goals and approach

The experiments conducted as part of this research were designed to focus on larger structures, on the scale of MOS capacitors. By examining the behaviour of the apparatus under the influence of these capacitive structures, where the significance of parasitic contributions and other side effects are small compared to the sample, the system response to comparatively smaller loads can be better understood. Seven MOS capacitors of varying dimensions, some of which are shown in figure 3, were probed using this technique. All were contained within a single flash memory device, in order to ensure that the dielectric layer composition and thickness remained constant. For perspective, the test capacitors comprising the data set for this thesis ranged in value between six femtoFarads (10^{-15} F) and 1.1 picoFarads (10^{-12} F). The experimental work was designed so that preliminary observations would reveal the system's large-scale behavioral trends, at which point the model could be refined to provide meaningful correlation between simulated and experimental results for smaller sample capacitances.

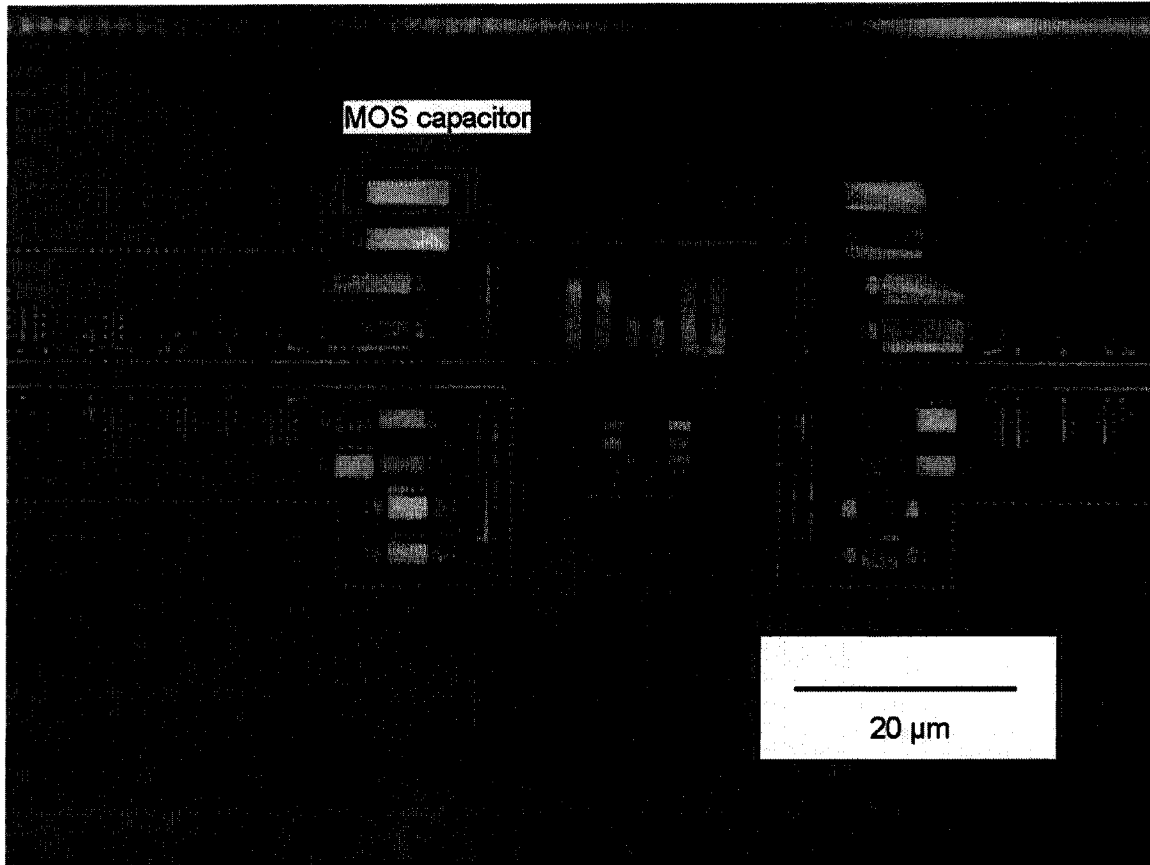


Figure 3 - Optical image of MOS transistors and capacitors from a flash memory device de-layered to expose poly-silicon structures.

The system being used is a commercially available instrument, but the method by which it is operated represents the unique aspect of this thesis. Designed to map physical topography and dopant concentration across a planar semiconductor surface, the *Veeco Dimension 3100* atomic force microscope (AFM) with scanning capacitance microscopy (SCM) module is necessarily equipped with both a nanoscale probe positioning system and an extremely precise capacitance detector. The goal of this work was to exploit the subsystems available in this existing tool to acquire a unique set of data, specifically absolute capacitance values of MOS structures. At present, this novel method expands the capabilities of an already useful instrument. Subsequent development might refine the technique to enable performance superior to that of apparatus normally used for capacitance measurements, especially when probing physically small samples having very low-capacitances.

1.3. Thesis organization

This thesis presents a novel technique for quantitatively measuring the capacitance of metal-oxide-semiconductor structures using scanning probe microscopy (SPM) hardware. In order to explain this method and justify its viability, three important areas must be examined. First, it is important to understand the fundamental operating principles of both atomic force and scanning capacitance microscopes, and more specifically their constituent components. Chapter 2 includes reviews of both AFM and SCM, to provide an understanding of how they normally function and why they would be appropriate choices for absolute capacitance measurements. A description of the sensors employed in scanning probe microscopy and an examination how a resonant circuit can be used for capacitance detection are also presented in the second chapter, with emphasis on characteristics that would optimize each component's suitability to this method. Having established a theoretical basis for the quantitative capacitance measurement technique's operation, subsequent testing of the method by means of electrical circuit simulation software is detailed in chapter 3. Presented here is the development of a model meant to simulate the capacitance detection circuitry, as well as the results of simulated experiments during which the model is subjected to both ideal and physically realistic loading and environmental conditions. Chapter 4 is devoted to a summary of experimental results, including data obtained from various types of capacitive loads measured using two types of sensors. Furthermore, this chapter contains an assessment of the data's accuracy, followed by a comparison between experimental and simulated results. Finally, chapter 5 concludes by addressing the ultimate feasibility of the proposed measurement technique, and suggests potential avenues for future research.

1.4. Summary of contributions

This thesis is my own original work, containing novel contributions to the fields of semiconductor characterization and electrical scanning probe microscopy. Specifically, it presents the following:

- Analysis of an SCM module's internal capacitance detector, including derivation and modeling of an equivalent system resonant circuit.
- Proposal of a new technique by which experimental artifacts may be removed, enabling extension of an existing instrument's capabilities to permit previously unattainable measurements.
- Completion of a feasibility study in which the capabilities and limitations of the aforementioned method are established and potential improvements suggested.

2. Extending traditional scanning probe microscopy – fundamental principles:

2.1. Introduction

The quantitative capacitance measurement method introduced in this work operates by observing the consequences when a load of unknown capacitance is incorporated into a resonant circuit. A typical SCM-equipped atomic force microscope contains four components critical to this novel technique. With the exception of AFM, which ensures accurate probe positioning, each one is used in an atypical manner in order to ensure the method's feasibility. It is important to evaluate whether or not the SCM and its internal resonant circuit capacitance detector, when used in conjunction with conductive probes and under appropriate conditions, can enable capacitance measurements of sufficient accuracy on the desired scale. This section includes a description of each of the aforementioned components, as well as an explanation of how each one would normally be used. Next, the suitability of each component is evaluated by comparing its specifications to those required for this task.

2.2. Atomic force microscopy

Initially introduced twenty years ago as a technique for obtaining high-resolution topographic images of non-conductive sample surfaces, AFM has evolved into a versatile atomic-scale imaging method, invaluable for applications ranging from biotechnology to semiconductor physics [14]. The following section shows the AFM's development by presenting some historical milestones and notable contributors. This is followed by an overview of the three imaging modes most commonly employed, with emphasis on characteristics that make contact mode the technique of choice for this work. Finally, the resolution and tolerance of modern instruments are specified, along with several factors that could significantly impact an AFM's capabilities. This analysis provides certainty that the AFM component of the proposed apparatus will be capable of adequately performing as required for this technique.

2.2.1. Historical development of AFM

The principles governing the operation of an atomic force microscope are derived from scanning tunneling microscopy (STM) theory [15], the development of which earned Gerd Binnig a share of the 1986 Nobel Prize in physics. First published that same year, the premise of AFM was that STM concepts could be modified to enable imaging of nonconductive and semiconductive samples [16]. Rather than determining topography by monitoring the tunneling current magnitude, AFM works by measuring the strength of inter-atomic forces between the sample surface and a sharp probe tip [17]. These forces are accurately described by the Lennard-Jones potential, which relates the magnitudes of inter-atomic forces to the distances separating them, as illustrated in figure 4. The horizontal axis represents increasing atomic separation, which equates to increasing tip-sample separation in the case of this work. Vertical values represent inter-atomic forces, which change direction at a separation distance approximately equal to the electron cloud radii. Strong Pauli repulsion behaviour dominates the tip-sample interaction at close range, arising as a consequence of overlapping electron orbitals [19], and resulting in cantilever deflection away from the semiconductor surface. As will be discussed further in the following section, contact mode imaging is performed within this regime since cantilever deflection can indicate tip-sample proximity [20]. Conversely, at larger distances the r^{-6} component of the Lennard-Jones potential dominates, as Van der Waals

interactions between atomic dipoles trigger attractive forces between the tip and sample [18], creating the oscillation-damping conditions critical for non-contact mode imaging. The following section describes each of the three AFM imaging modes, providing a clear picture of the physical interactions that occur during quantitative capacitance measurements.

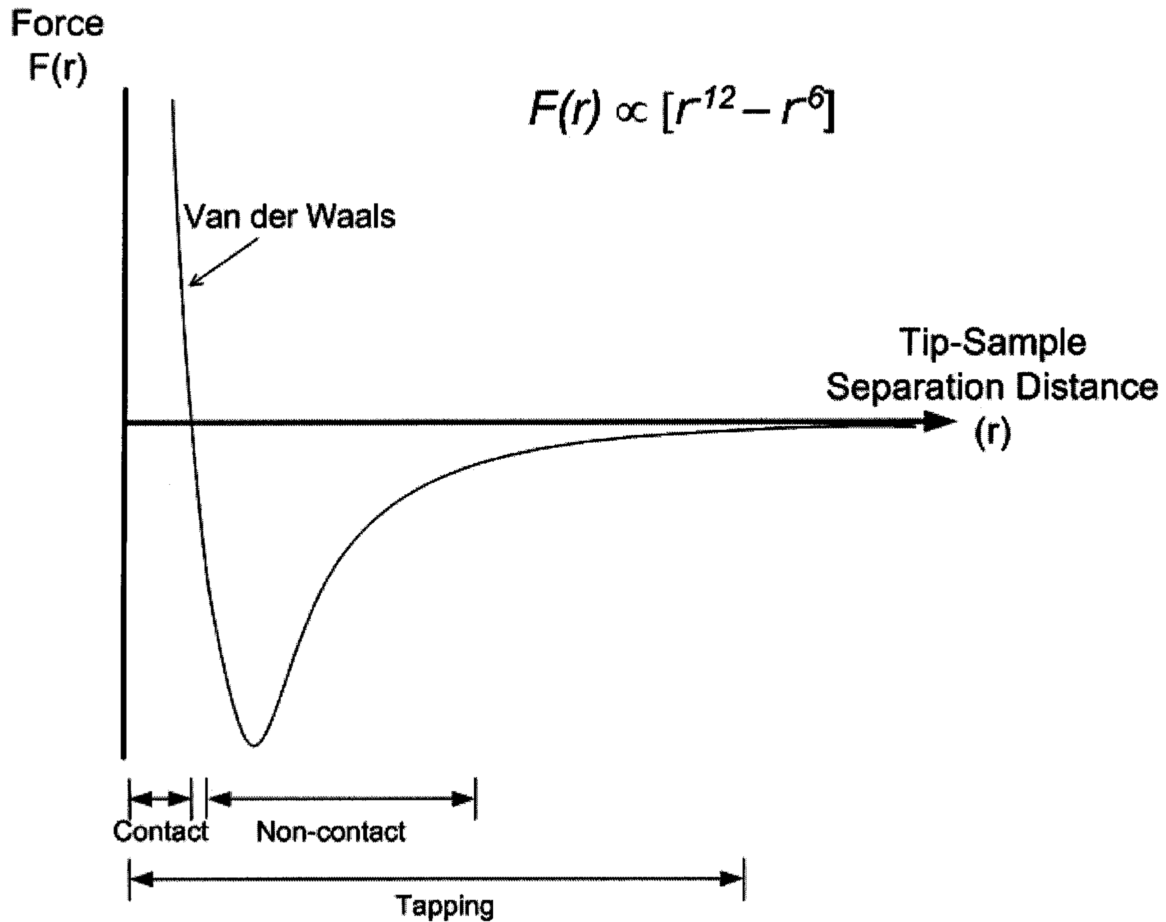


Figure 4 – Lennard-Jones potential illustrating Van der Waals force dependency over distance. AFM operating regimes are also shown. Adapted from [16], [18].

2.2.2. Operational theory

Of the three AFM imaging techniques employed – non-contact mode, tapping mode, and contact mode – each is most appropriate for a particular sample type, imaging environment and tip-sample separation distance. While topography determination is the primary motivation for using any of these modes, the sample preparation procedure

employed in this work yields nearly planar surfaces, leaving minimal topography to measure. The objective of AFM imaging in this experiment is to enable precise positioning of the probe tip over the desired contact regions on the sample, a task performed sufficiently well by all three modes. The contact mode of AFM imaging employed in this work is particularly well-suited to enabling low-impedance electrical contact between the tip and sample however [21], a critical requirement for quantitative capacitance measurements.

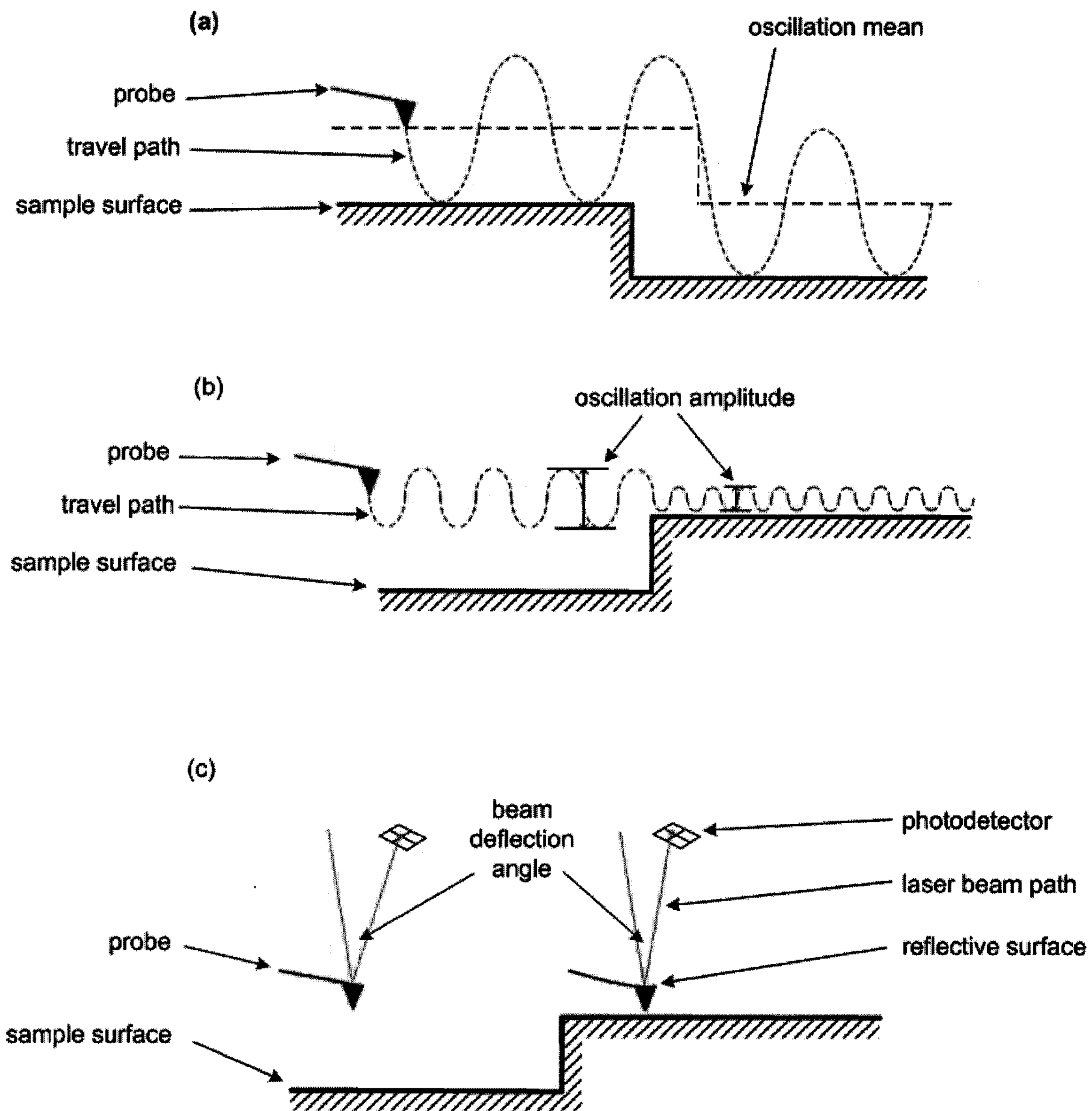


Figure 5 - Illustration of common AFM imaging techniques (a) tapping mode, (b) non-contact mode, and (c) contact mode

Tapping mode AFM, illustrated in figure 5(a), functions exactly as its name implies: The probe consists of a tip on the end of a cantilever, which is made to oscillate with considerable fixed amplitude (~100 nm) at its characteristic resonant frequency. The probe is mounted on a movable stage, whose height can be adjusted relative to the sample surface by applying voltage to a piezoelectric cylinder, forcing it to expand or contract. A feedback loop monitors the tip's oscillations as the stage is being lowered, until amplitude modulation indicates that physical contact has been made with the sample. This minor amplitude damping, resulting from both repulsive short-range forces encountered very near the surface and attractive forces that arise when the tip is being pulled out of physical contact with the sample, is then maintained by continuously adjusting the stage height as the probe moves laterally. Sample topography can be subsequently calculated based on this set of stage height data, generated when probe oscillations are modulated by surface forces. While this mode is capable of producing images with exceptional lateral resolution [22], incidents of physical contact with the sample are far too brief to acquire the desired capacitance data [23], making tapping mode unsuitable for the proposed measurement technique.

Non-contact AFM is similar to tapping mode in that the probe is made to oscillate, but for this technique the amplitude of fluctuation is usually no greater than 10 nanometers. The non-contact method relies on oscillatory driving forces being too weak to overcome the repulsive Van der Waals forces that arise between tip and sample with each oscillation. As the tip approaches the sample surface (by means of the piezoelectric stages), the increasing electron orbital forces dampen the oscillation and reduce its amplitude [24], as shown in figure 5(b). The stage height at which damping reaches a specified level directly indicates the underlying sample height. As in the case of tapping mode measurements, feedback control maintains a constant damping level while the probe is raster scanned.

Figure 5(c) illustrates the typical operation of contact mode AFM, the only technique in which the probe and sample are constantly touching [25], and therefore the method employed to conduct this research. A cantilever with a small tip attached at one end is mounted on a piezo-driven stage, and lowered and fixed in a position within the

repulsive region of the Van der Waals force curve. The probe is then scanned across the surface of a sample in a raster pattern, while the repulsive forces cause the cantilever to bend backward. This deflection is measured by means of a laser beam, which is made to strike a pair of photodiodes after reflecting off the cantilever's backside. Since variations in probe deflection can have a significant bearing on the laser beam's eventual point of incidence, the energy collected by each of the two photo detectors will vary as topography changes the tip-sample separation, and hence the intensity of repulsive surface forces. While the instrument is operating in constant height mode as described above, these variations in beam deflection correspond directly to the sample topography. Alternatively, constant force imaging involves providing the photodiode's beam incidence point to a feedback loop, which then adjusts the probe stage's height to maintain constant cantilever deflection. In this case, the stage height represents the sample's topography. Since this imaging mode relies on cantilever deflection due to repulsive Van der Waals forces, the tip and sample must remain constantly in very close proximity. It is this requirement that ensures good electrical contact at the tip-sample junction, making this AFM imaging mode the logical choice for use in this work.

2.2.3. Resolution and tolerances

When evaluating microscopic imaging techniques, resolution is arguably the most critical specification to consider, both in the lateral plane and with respect to the data being collected. The absolute capacitance measurement technique described in this work however relies very little on the AFM's topographic imaging capabilities and so the vertical resolution is less significant. Instead the instrument's lateral resolution, which determines how precisely the probe can be positioned, is of paramount importance.

An AFM's lateral resolution is heavily influenced by the tip shape [10]. If its end has a small radius of curvature for example, the resulting interactive forces will involve a minimal number of atoms on the sample surface, hence the attainable resolution will be high. As shown in figure 6, a tip terminated with a single atom is theoretically capable of generating atomic resolution images, if sufficiently close to the sample surface, while tips of larger radii lead to diminished imaging capabilities as a consequence of expanded tip-sample interactions. While the sample regions targeted in this work are large, in-situ device scanning and other potential future applications for the technique may require

higher resolution imaging. It is important therefore to validate the system's small-scale measurement capability, despite the fact that it is not currently needed.

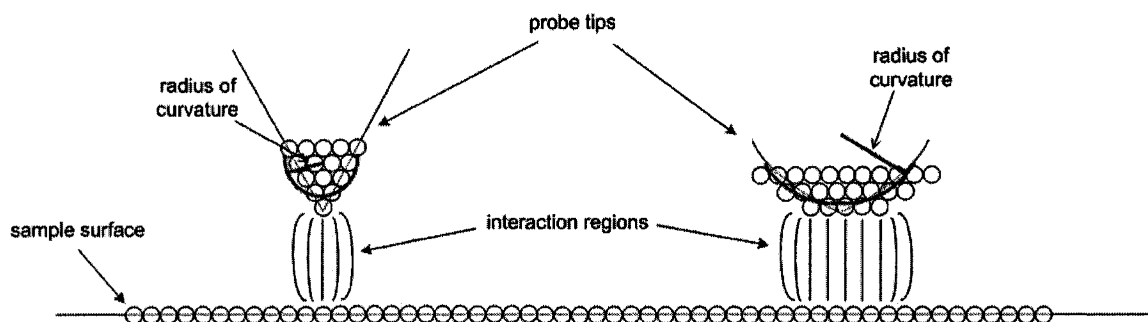


Figure 6 - Comparison of tip-sample interaction regions for sharp and blunt probe tips. The circles represent atoms and the field lines the dominant Van der Waals interaction region.

Vertical resolution is predominantly limited by the positioning capabilities of the z-scanner which, in the case of a piezoelectric tube, can be specified with sub-angstrom accuracy. The lateral scanning speed will also influence AFM imaging since the z-piezo does not respond instantaneously to steep height changes. At reduced scan rates however, it is possible to clearly delineate abrupt height variations as large as hundreds of nanometers. An AFM's vertical resolution is also influenced by the tip shape. Probe tips having steeper sidewall angles will allow more precise delineation of high-aspect-ratio surface features since such features can be approached much more closely. While planarizing samples as part of this technique means that extreme surface features are eliminated, the use of a narrow probe is also beneficial for minimizing parasitic effects during capacitance measurements, a topic discussed elsewhere. As illustrated in figure 7, the influence of tip geometry on imaging capabilities can vary considerably depending on the relative direction in which the sample is scanned, with optimal performance in this case occurring for data acquired while scanning in only one of the four cardinal directions.

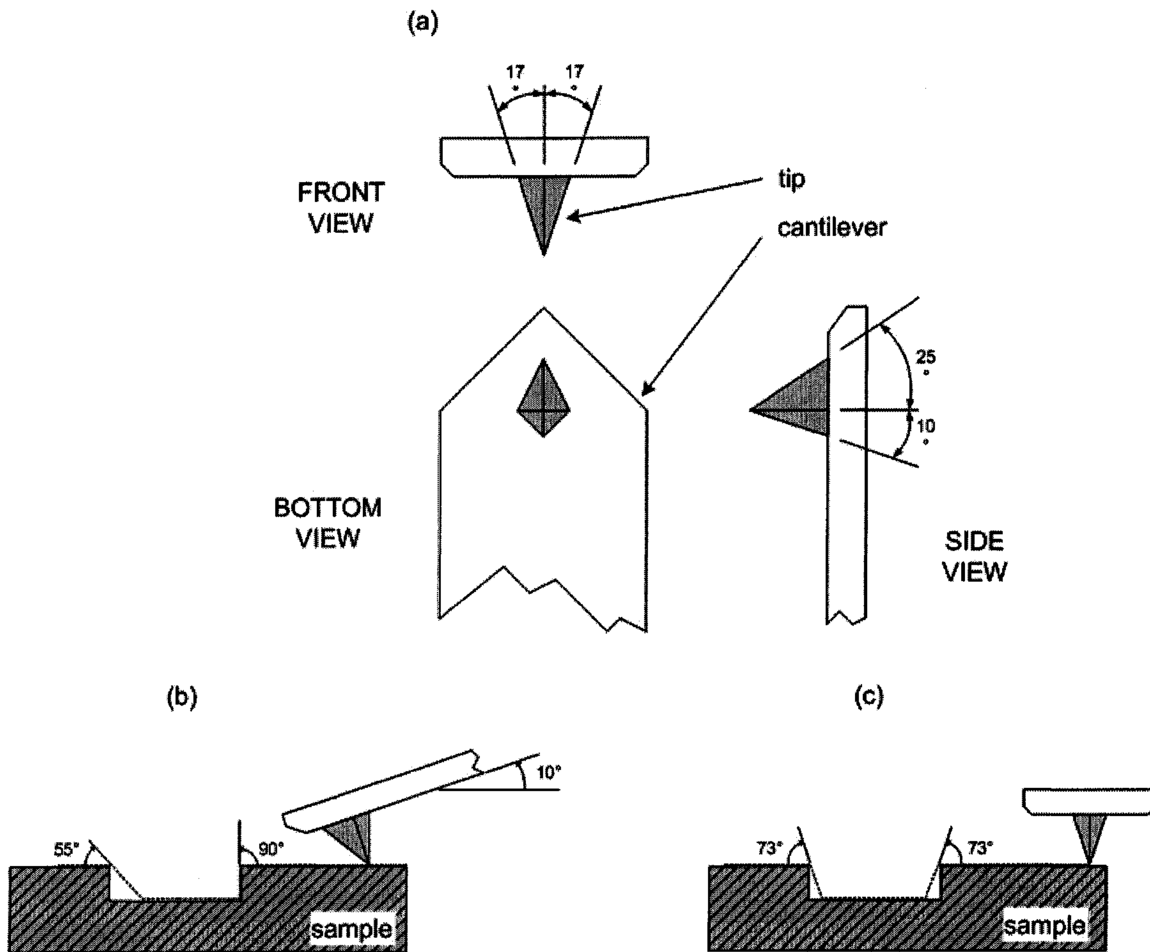


Figure 7 - Dependence of vertical feature imaging capability on probe tip geometry and scan direction. (a) The probe's physical geometry, path taken as probe scans (b) forward/backward, and (c) side to side across a trench. Figure adapted from [21].

Probes are mounted such that the cantilever extends down toward the sample at roughly ten degrees below horizontal. This angle, combined with the tip's sidewall angles, determines the maximum steepness of sample features that a particular tip can capably measure. To illustrate this assertion, consider the typical rectangular cantilever probe shown in figure 7(a). Since the left and right halves of the pyramidal tip are symmetric when viewed end-on, images acquired while the sensor is scanned along a path perpendicular to the cantilever can contain sidewalls no steeper than 73° figure 7(c). If the scan direction is shifted by ninety degrees however, the tip sidewall angles are asymmetrical and the image characteristics will differ. The structure imaged previously, when scanned along the same line with the probe being pushed away from and pulled

back toward its holder (rather than being swung side to side), instead produces the image in figure 7(b). Note that the mount angle negates the tip's back sidewall angle to allow one side of the structure to be faithfully imaged, but that features rising upward along the probe's front edge will appear to have no more than a 55° slope.

Finally, accurate lateral imaging requires that the components used to position the tip be capable of acting in a repeatable manner. Though piezoelectric devices are inherently prone to hysteretic behaviour, this tendency is well-defined for the system exploited for this work (a *Dimension 3100*); it easily corrected using compensatory software algorithms [11].

A further limiting factor depends on the sampling rate defined in software. Since a finite number of topographic measurements may be acquired on each scanned line, the scan window size may be the limiting factor in determining the image's lateral resolution. While a 1 μm x 1 μm region scanned at 128 samples per line will yield pixels spaced less than 10 nm apart (1000 nm / 128 = 7.81 nm), the same sampling rate applied over a 5 μm x 5 μm area gives almost 40 nm gaps between data points.

Accounting for all the factors listed above, the atomic force microscope apparatus employed for this work is capable of topographic imaging at lateral resolutions on the order of angstroms. Since the present requirement involves locating and placing an SPM probe above MOS capacitor contacts roughly 400 nm in diameter, the instrument's capabilities are more than adequate to meet the needs of this technique. Clearly AFM serves as an ideal tool to allow nanoscale navigation of sample surfaces, ensuring that probes are located very precisely above areas of interest. That the tip positioning mechanism is both highly stable and very repeatable are further important reasons why an atomic force microscope provides an excellent platform on which to conduct this research.

2.3. Scanning capacitance microscopy

While AFM improves on scanning tunneling microscopy by enabling topographic imaging of non-conductive and semiconductive samples, its use is certainly not restricted to these applications. In fact, the topographic data provided by an AFM becomes particularly invaluable when supplemented by other imaging techniques, such as scanning capacitance microscopy, whereby electrical data can be acquired simultaneously and correlated against topographic features. Scanning capacitance microscopy, or SCM, is one of several techniques that can broadly be described as electrical atomic force microscopy. The distinction is that by using a conductive probe to acquire AFM data, an instrument can concurrently measure a particular electrical property of the sample, such as depletion capacitance variations in the case of SCM. Images obtained using scanning capacitance microscopy techniques do not yield absolute capacitance values however; an imminent industry requirement that this work seeks to address. Nonetheless, this section presents the historical development and current capabilities of SCM in the context of its intended purpose, profiling two dimensional dopant levels in semiconductors, in order to illustrate how the novel method presented later differs from usual SCM techniques.

2.3.1. Historical development of SCM

The concept of measuring capacitance variations between a probe and surface was initially presented by RCA in 1978 [12], when a resonant circuit was used to read digital data stored as 8nm height variations on Videodisc media. This original concept, that fluctuations in tip-sample separation would present a varying capacitive load to an internal resonant circuit thus shifting its resonant frequency, has remained essentially unchanged in modern instruments. In 1984, Matey and Blanc first applied the RCA design to microscopy [13], and though they also recognized the technique's potential for imaging variations in dielectric constant, their 'scanning capacitance microscope' was used primarily to detect regions of excessive surface roughness. It was not until 1991 [14] that Barrett and Quate first demonstrated the inherent electrical measurement capabilities of this technique when they supplemented an AFM with an RCA-type capacitance sensor, enabling simultaneous electrical imaging and atomic force-feedback height control. While their publication focused on detecting charge stored in nitride-oxide-silicon systems rather than semiconductor dopant profiling, today's SCM instruments are

typically offered as a supplementary module designed to piggyback on an AFM, just as Barrett and Quate had originally proposed.

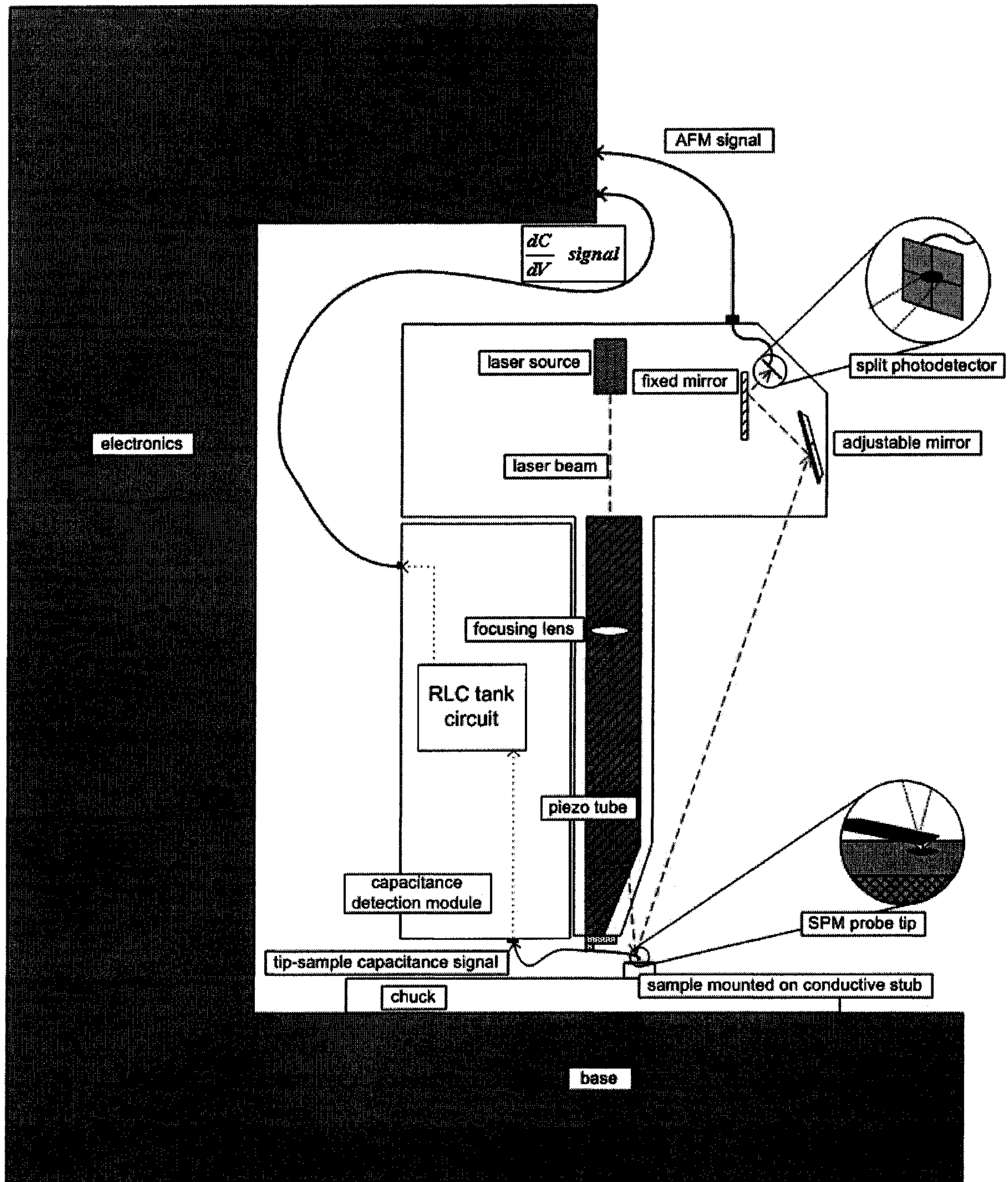


Figure 8 - Schematic of SCM imaging equipment showing path of information flow.

2.3.2. Physical principles of operation

The *Veeco* scanning capacitance microscopy module used in the experimental portion of this work was designed to be physically attached to the scanning head stage of the *Dimension 3100* atomic force microscope, as shown schematically in figure 8. This placement is important to ensure that the conductive probe, which acts as a transmission line link to the sample, is in close proximity to the resonant circuit. Probes employed in scanning capacitance microscopy behave identically to AFM probes, except that electrical signals generated at the tip-sample interface are relayed via a short wire to the SCM module, which contains both the aforementioned tank circuit and a high frequency driving oscillator. The laser deflection topography profiling mechanism discussed in section 2.1.2 is unimpeded by the SCM apparatus, allowing both images to be captured concurrently. A signal proportional to the detector's frequency response at the driving frequency, such as the amplitude of current flow through the tank circuit, is sent from the SCM module to the microscope controller for further analysis and display in software.

However the *Veeco* instrument, as with the Barrett microscope before it, is not intended to measure absolute capacitance directly, nor is capacitance ultimately the parameter of interest. Scanning capacitance microscopy's fundamental operating principle is that by observing the depletion behaviour of a doped semiconductor region in the vicinity of an electrically charged probe, the type and concentration of local dopant species can be determined.

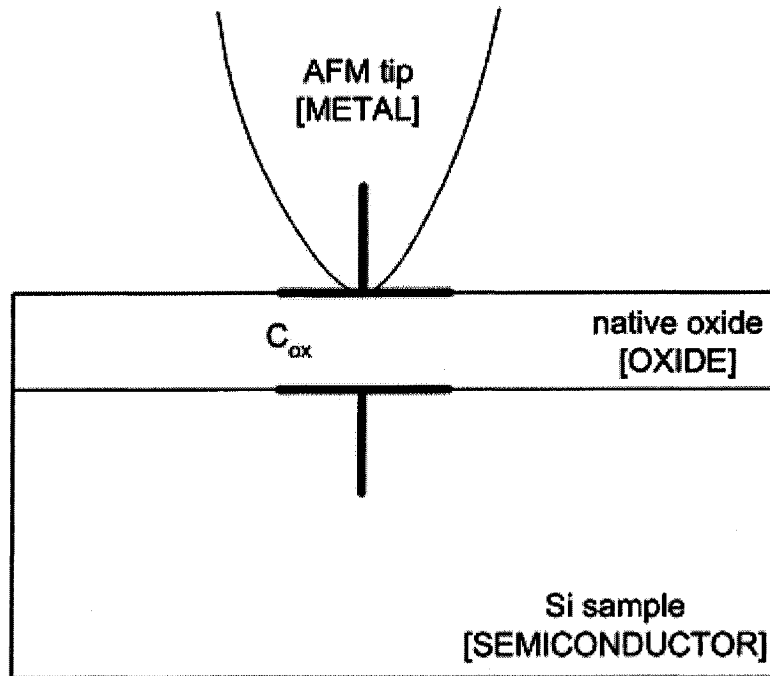


Figure 9 - MOS capacitor formed at SCM tip-sample interface.

The instrument's functionality relies on the presence of a thin native oxide layer grown on the surface of a planar silicon sample. When this SiO_2 layer is probed with a conductive AFM tip, a metal-oxide-semiconductor junction is formed as seen in figure 9. For the resonant circuit to which the tip is connected, the oxide gap in this MOS structure appears as a capacitive load, and the tank circuit's characteristic resonant frequency shifts accordingly. Furthermore, in semiconductor regions doped with ionic impurities, free carriers will either be drawn toward the sample surface below the probe or pushed into the substrate when a potential difference is applied between the tip and sample. A local depletion region appears below the probe as carriers are repelled from the semiconductor surface, and as shown in figure 10, the effective tip-sample capacitance changes accordingly. These depletion capacitance changes represent the measured quantity of interest, as they are related to the type and concentration of local dopant species.

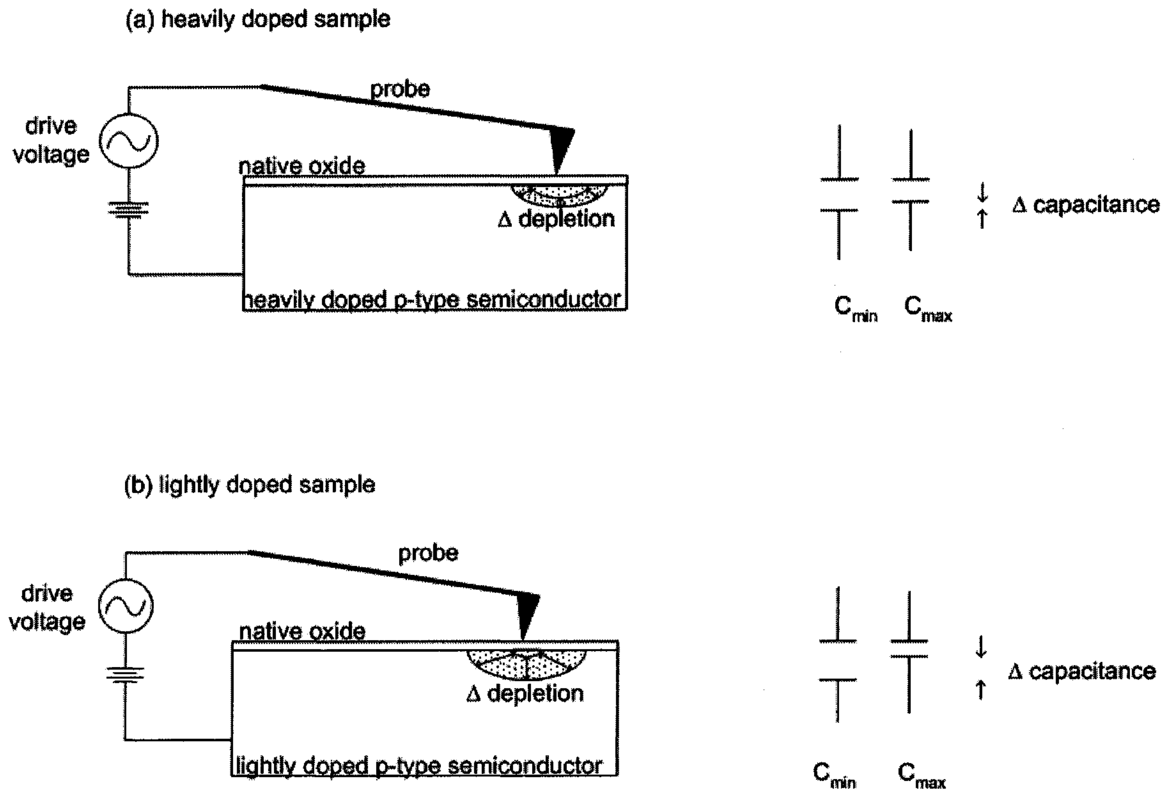


Figure 10 - Comparison of depletion and capacitance changes for (a) heavily and (b) lightly doped semiconductors in response to applied ac voltage.

In practice however, the capacitance variations triggered by carrier depletion are extremely small, particularly when compared to the system's parasitic capacitance levels. Though the RCA detector is very sensitive, it is incapable of distinguishing attoFarad (10^{-18} F) capacitance shifts in the presence of picoFarads (10^{-12} F) of stray capacitance. Instead, the applied voltage is modulated and the resonant circuit output passed through a lock-in amplifier (LIA) using the modulating sinusoid as a reference signal. This filtering mechanism is one element of the original RCA design that has remained an essential component in modern scanning capacitance microscopes.

A comparison of the LIA output and applied voltage amplitudes reveals the rate of capacitance change with respect to voltage fluctuations, allowing one to determine how the depletion depth varies in response to relative tip-sample potential. Since this ratio is determined by the type and concentration of dopant species beneath the probe, the $\frac{dC}{dV}$ data yielded by SCM can therefore be compared to well-characterized standard

samples to quantitatively determine local dopant levels. An SCM image results when the AFM tip is scanned in a raster pattern to produce a two-dimensional map depicting the relative dopant levels within the scan region. The capability to acquire such images on a 10nm scale met a requirement identified by the Semiconductor Industry Association in their 1997 industry roadmap [15], prompting the widespread adoption of SCM for dopant profiling.

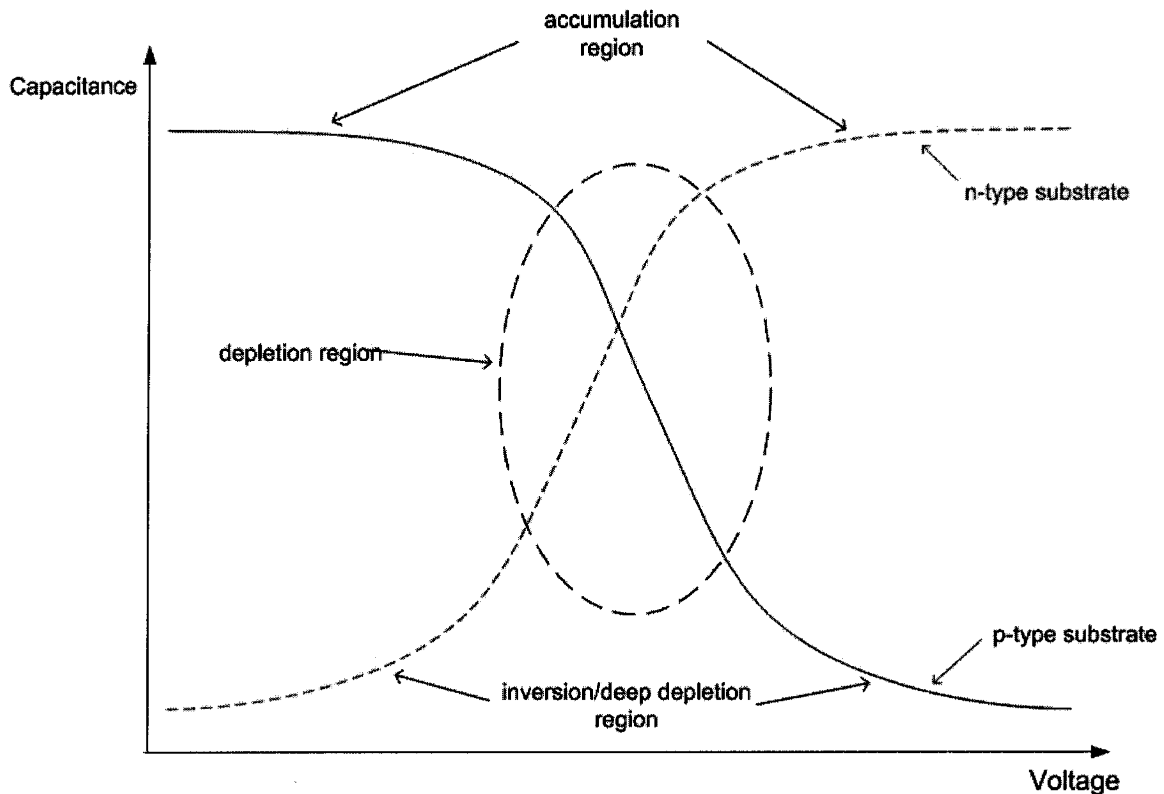


Figure 11 - Typical C-V curves for n- and p-type MOS capacitors.

2.3.3. Typical applications

The fundamental concept enabling scanning capacitance microscopes to reveal dopant distributions is the well-documented capacitive behaviour of a MOS structure under bias. Figure 11 shows characteristic capacitance-voltage (*C-V*) curves for MOS capacitors having p-type and n-type substrates[1], each of which can be seen to consist of

[1] Note that these curves are frequency-dependent [16], but since measurement frequencies below 100Hz affect only the deep depletion/inversion regions, these curves should be sufficiently accurate to illustrate typical SCM operation.

three distinct regions: accumulation, depletion and inversion or deep depletion. SCM is intended to exploit the depletion region of these curves, in which the slope's direction and steepness can be interpreted to yield dopant distribution. By modeling the metal-oxide-semiconductor interface under static biasing conditions using an energy band diagram, one is better able to understand the physical interactions leading to these capacitance-voltage relationships.

Figure 12(a) depicts an unbiased ideal n-MOS capacitor at equilibrium. The Fermi levels are aligned in order to satisfy the relationship

$$E_F(metal) - E_F(semiconductor) = eV \tag{2.1}$$

where V represents the voltage applied to the substrate relative to the tip, e the electronic charge constant, and E_F the Fermi levels in the electrode materials. Further assumptions describing this ideal MOS capacitor model include the following: (1) The semiconductor layer is sufficiently thick that energy levels will always remain at their equilibrium state deep within its bulk. (2) The oxide layer contains no charge centers and is thick enough to impede leakage current from passing though it. (3) The metal layer can be considered to be an equipotential region regardless of applied bias [18].

As figure 12(c) illustrates for an n-type capacitor, negatively biasing the substrate makes the grounded tip appear positively charged. This 'positive' biasing condition establishes an electric field which attracts free majority carrier electrons toward the oxide-semiconductor interface, where they accumulate beneath the tip. The potential, denoted by ψ, varies as a function of depth within the semiconductor, x, as defined by the equation

$$e \cdot \psi(x) = E_I^{\infty} - E_I(x) \tag{2.2}$$

where x increases from zero at the oxide-semiconductor interface, and E_I^{∞} represents the intrinsic Fermi level deep within the bulk. Equation (2.2) clearly obeys the first

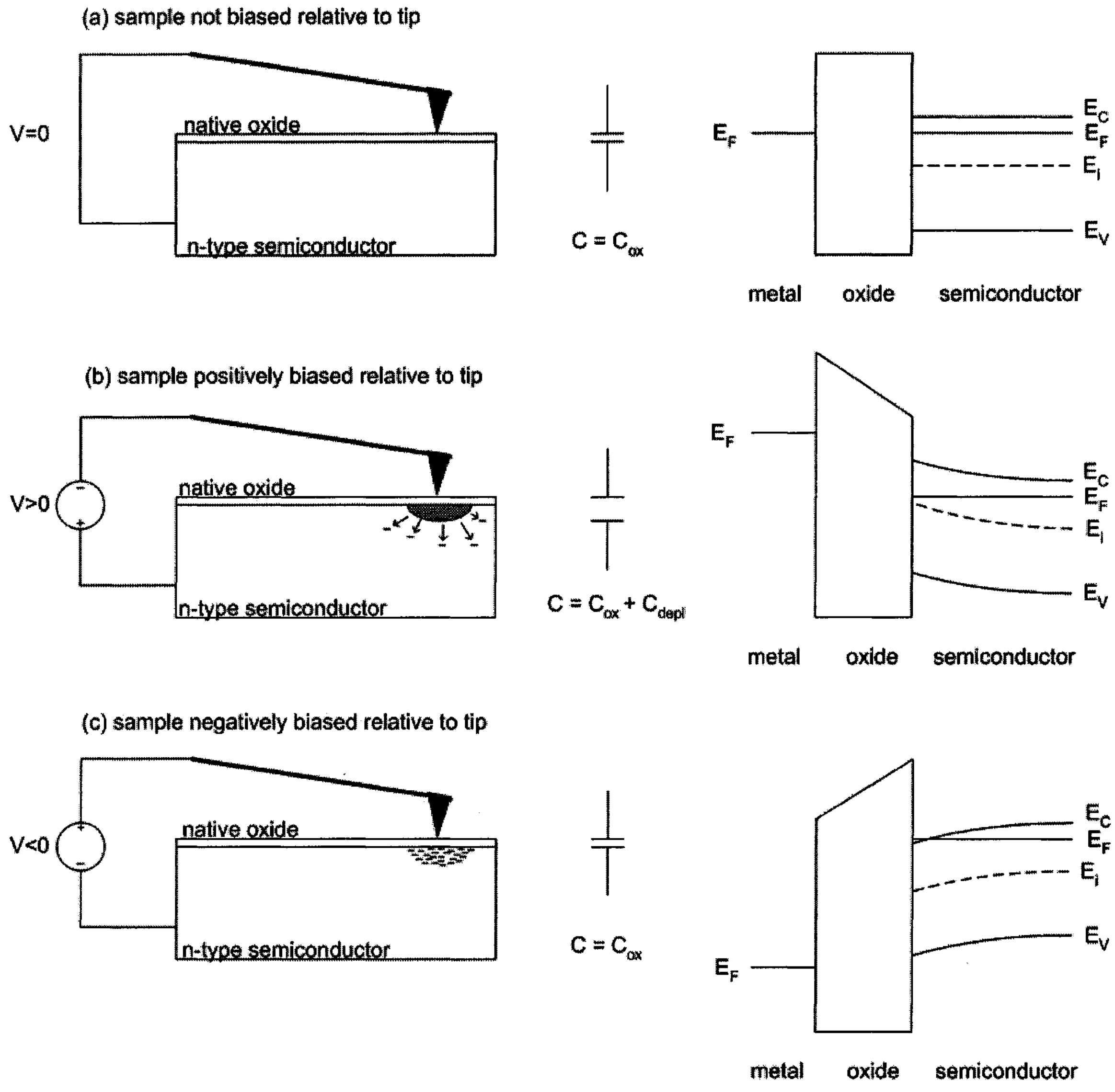


Figure 12 - Energy band diagrams for MOS junction under various biasing conditions.

assumption made earlier, since potential tends toward zero as x approaches infinity. At the oxide-semiconductor interface however, the intrinsic Fermi energy level, $E_I(0)$, must bend to match the boundary condition imposed by the surface potential, $\psi(0)$. In terms of energy levels, the applied bias causes the metal's Fermi level to drop relative to that of the semiconductor, and the conduction and valence band edges in the semiconductor are consequently deformed near the oxide interface. The electron concentration,

$$n = n_i \exp\left[\frac{(E_F - E_I(x))}{kT}\right] \tag{2.3}$$

grows as x approaches zero, causing majority carriers to accumulate below the tip. For obvious reasons, positive biasing produces a segment of the *C-V* curve called the accumulation region.

Figure 12(b) illustrates the opposite condition, negative biasing, in which the n-type substrate is positively biased with respect to the probe. In this situation, negative carriers are repelled from the tip-sample interface and driven into the semiconductor bulk. As the tip Fermi level rises, the semiconductor energy bands bend upward near the oxide interface to satisfy equation (2.2). If the band bending is severe enough that the intrinsic Fermi level equals E_F, the majority carriers become fully depleted at the semiconductor-oxide boundary. This range of bias voltages forms the depletion regime of the *C-V* curve, in which the dearth of electrons behaves as a dominant second capacitance, in parallel with the oxide layer.

Obviously, the direction and steepness of a *C-V* curve's slope within the depletion region indicates the type and concentration of dopant species used to form the corresponding capacitor substrate. To exploit this relationship and thereby construct an image of spatial carrier distribution is the fundamental goal of scanning capacitance microscopy.

2.4. SPM sensors

Despite being one of the smallest and most fragile components of a scanning probe microscope, the probe is arguably the most important part. Typically consisting of a microfabricated cantilever and tip, the probe, also called a sensor, is the instrument's primary point of contact with the sample. This section describes some of the parameters most commonly specified when selecting an SPM sensor, with particular focus given to characteristics that bear heavily on the experimental portion of this work. Next, a distinction will be made between the ideal specifications for a 'scanning capacitance probe' as compared to an 'absolute capacitance probe'. Finally, the suitability of three types of sensors is evaluated for use in this novel absolute capacitance measurement technique.

2.4.1. Coatings

A very important aspect of a sensor's composition is a coating applied over the internal silica or silicon nitride structure. Though typically only about thirty nanometers thick, a probe's coating layer plays a critical role in determining its suitability to particular imaging techniques. To acquire atomic force microscopy images in contact mode using the *Dimension 3100*, it is critical for sensors to have a layer of reflective material on the back side of the cantilever, opposite the tip. Often composed of gold or aluminum, this 'reflex coating' enables a laser beam to be reflected from the cantilever toward a split photodiode, allowing local topography data to be mapped based on the extent of tip deflection as illustrated in figure 13.

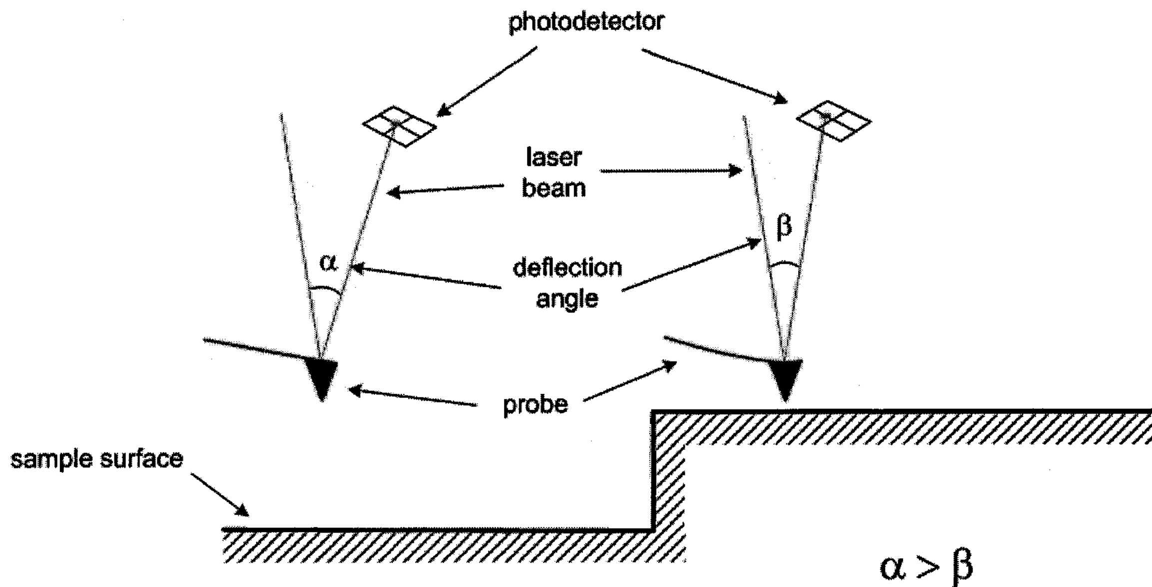


Figure 13 - Effect of tip deflection on laser beam reflection angle due to sample topography.

In order to acquire electrical data, the sensor's contact point must be either conductive or coated with a conductive layer, the composition of which will depend heavily on the intended application. Techniques that involve high tip-sample contact forces, such as scanning spreading resistance microscopy (SSRM), often deploy sensors made from boron-doped diamond. Alternatively, tips coated with chromium, platinum, iridium or combinations of these are usually sufficient for most electrical SPM imaging methods including scanning capacitance microscopy. Since both traditional SCM and absolute capacitance measurement techniques depend heavily on accurate electrical data, an important requirement for both methods is that they employ a probe having high conductivity, especially at its apex where tip-sample contact occurs. Though sensors made conductive by means of metal coatings are designed to allow near-Ohmic contact, repeated imaging erodes the coating layer until eventually the tip-sample contact region behaves more like a Schottkey junction as shown in figure 14. Unfortunately, when loads are combined with even a slight series resistance due to a worn tip, they can yield drastically misleading results. These conductive coatings are particularly prone to degradation during the absolute capacitance technique, when tips are made to scan over hard tungsten contact plugs. In an effort to ensure Ohmic tip-sample contact therefore,

one possible remedy is to employ a sensor formed entirely from a single conductive material, such as tungsten.

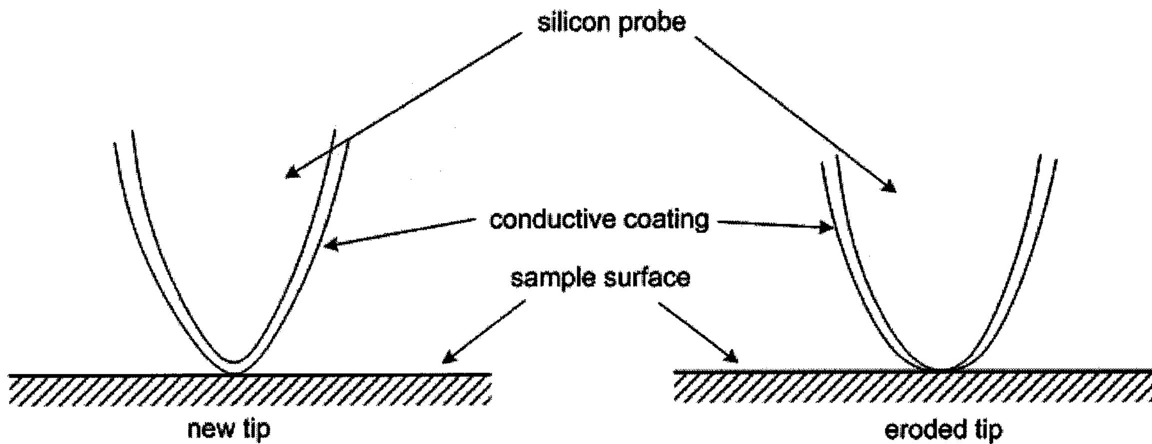


Figure 14 - Effect of conductive coating erosion on tip-sample contact.

2.4.2. Physical shape

A tip's sidewall angles and radius of curvature are two further parameters used to categorize sensors. Together, they describe the shape of the tip-sample interaction region, which can improve imaging resolution as its area is minimized. As discussed in section 2.1.3, employing a tip of sufficiently small radius to interact with individual sample atoms, and with sidewalls sloped steeply enough to allow delineation of sharp surface features, yields obvious benefits for both AFM and SCM imaging. The importance of using such a tip for these experiments is somewhat more obscure. Since the AFM's ultra-high precision imaging capabilities are useful but not strictly necessary for performing absolute capacitance measurements, a more important factor to consider when choosing an appropriate tip for this work is the impact of its geometry on stray capacitance levels.

Past literature has cited parasitic capacitance interactions between the microscope chuck and various segments of the probe – the tip, cantilever and body [18], and some have found stray capacitance levels to be dependent on the scanning direction [19]. Since physical proximity between sensor and sample surface has been shown to generate stray capacitance, it is reasonable to assume that probes having different physical shapes will yield disparate levels of parasitics.

2.4.3. Other parameters

Two further specifications to consider when choosing an SPM sensor are spring constant and resonant frequency. The latter is determined mainly by the cantilever length, and typical values range between ten and four hundred kilohertz. Though this specification is particularly relevant while imaging in non-contact or tapping modes, it may be advantageous to employ a sensor with a high resonant frequency even for contact mode imaging, so as to minimize the effects of stray environmental vibrations. The spring constant quantifies a cantilever's stiffness, which describes its sensitivity to force. A probe having a low spring constant, usually due to a narrow cantilever, will be deflected by smaller forces than would be required to bend a stiff sensor. While a probe with a low spring constant is desirable for producing accurate AFM data, a much thicker and stiffer cantilever would be necessary for SSRM imaging, to withstand the high forces involved.

2.4.4. Suitability for this work

Since sensors capable of rudimentary atomic force microscopy imaging will suffice for absolute capacitance measurements, the tip radius and sidewall angles are not of primary importance, though a reflective back coating is necessary. Similarly, the probes must be stiff enough to withstand considerable force and not be overly susceptible to stray vibrations, but most non-specialized sensors readily meet these requirements. Conductivity is critical for this application however, so it is important that the tips employed can maintain good electrical contact with the sample. While the forces involved in these measurements are not exceedingly high, the tip will often be dragged across metal contact plugs, which will erode coatings and eventually result in a non-Ohmic tip-sample interface.

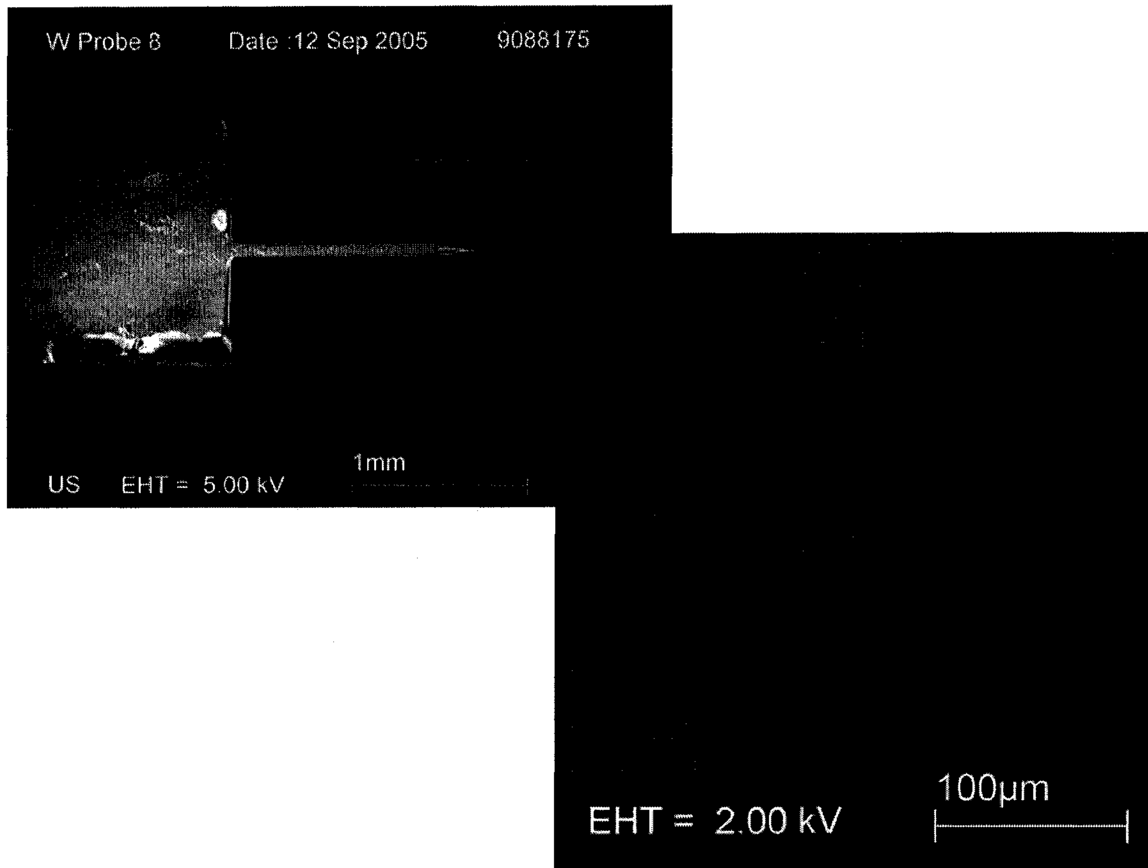


Figure 15 - Scanning electron microscope images of a solid tungsten SPM sensor.

Three types of SPM sensors were considered for use in the experimental portion of this work: Standard silica probes made conductive and reflective by means of a platinum-iridium coating, probes of the same geometry having solid boron-doped diamond tips, and solid tungsten sensors with a unique physical shape, illustrated in figure 15. Since electrical measurements were the objective of this work, tip conductivity was seen as the most critical specification. In this respect, tungsten and doped diamond tips were expected to be far superior to metal-coated probes, especially after extended use. The three alternatives were further distinguishable based on unit price, with platinum-coated tips being the least expensive and diamond the most costly. Stray capacitance was the final factor considered in selecting a suitable probe for these experiments, though insufficient information was available to conclusively determine each probe's influence on parasitic capacitance levels.

Ultimately, after considering these criteria in the order presented above, experiments were conducted using both platinum-coated and solid tungsten sensors. While it was clearly understood that the coated probes shown in figure 16 would be useful for only a brief period of time, the difference in price made their inclusion worthwhile. The tungsten sensors were seen to have durability comparable to doped diamond, but at a more reasonable price.

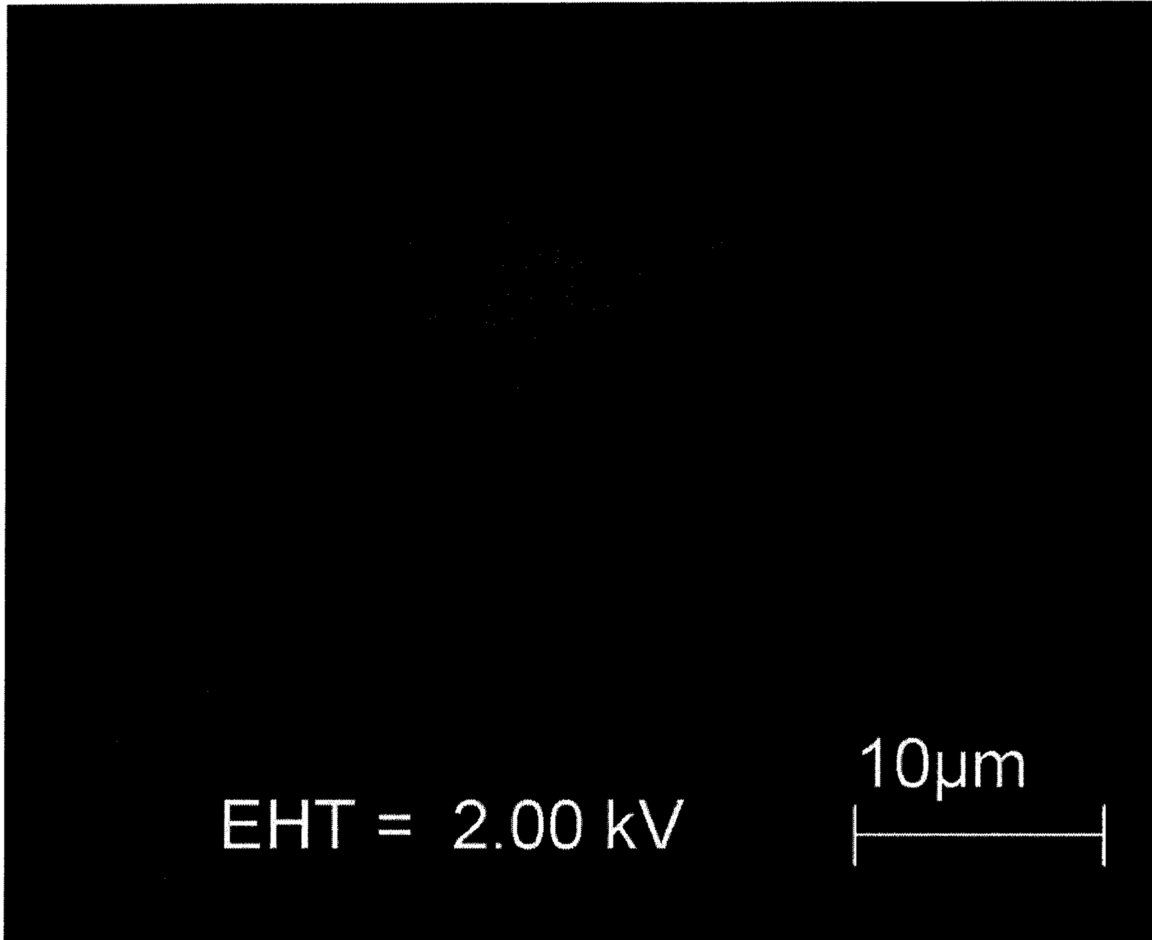


Figure 16 - SEM image of a platinum-coated probe viewed from below.

2.5. Resonant circuits

Just as in the original RCA design, the ultra-sensitive capacitance detector at the heart of *Veeco*'s SCM is based on a resonant circuit whose frequency response changes under load. Though the circuit's specific composition could not be disclosed, the system was treated as a black box and modeled with equivalent component values to evaluate its suitability for absolute capacitance measurements. This section explains some fundamental concepts of resonant circuits, presents an equivalent *Veeco* capacitance sensor design based on its published specifications, and describes the expected behaviour of such a circuit under the intended experimental conditions.

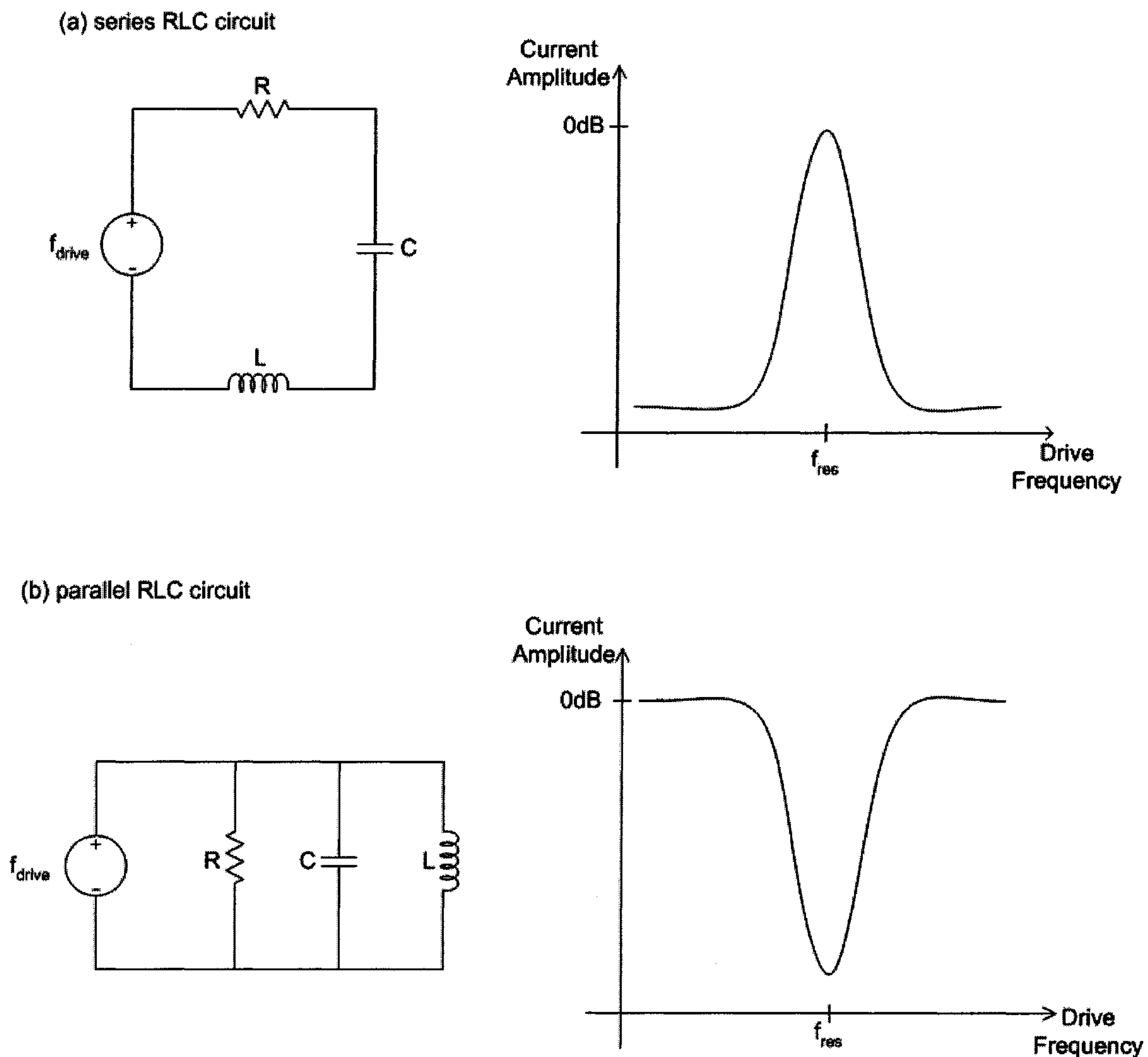


Figure 17 - Frequency response of RLC circuits in (a) series and (b) parallel configuration.

2.5.1. Basic RLC circuit analysis

Fundamentally, series and parallel RLC circuits are completely different, but in many respects they behave equivalently. When simplified, each is seen to consist of inductive, resistive and capacitive components, the respective arrangement of which determines the circuit's overall behaviour. Both configurations result in a circuit whose internal current amplitude depends on the driving frequency, and figure 17 illustrates the most obvious difference between the two. While a parallel circuit exhibits maximum impedance at its resonant frequency, driving a series RLC circuit at resonance causes internal reactive components to negate one another, ensuring minimal impedance thereby allowing maximum current flow. Since the instrument's Gaussian-shaped output represents voltage amplitude, the internal circuit from which it arises is likely equivalent to the series RLC configuration of figure 17(a). For this type of circuit, the resonant frequency,

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{2.4}$$

is equally dependent on both reactive components. Output bandwidth meanwhile, is typically described by a quantity called the Q-factor, defined as

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{2.5}$$

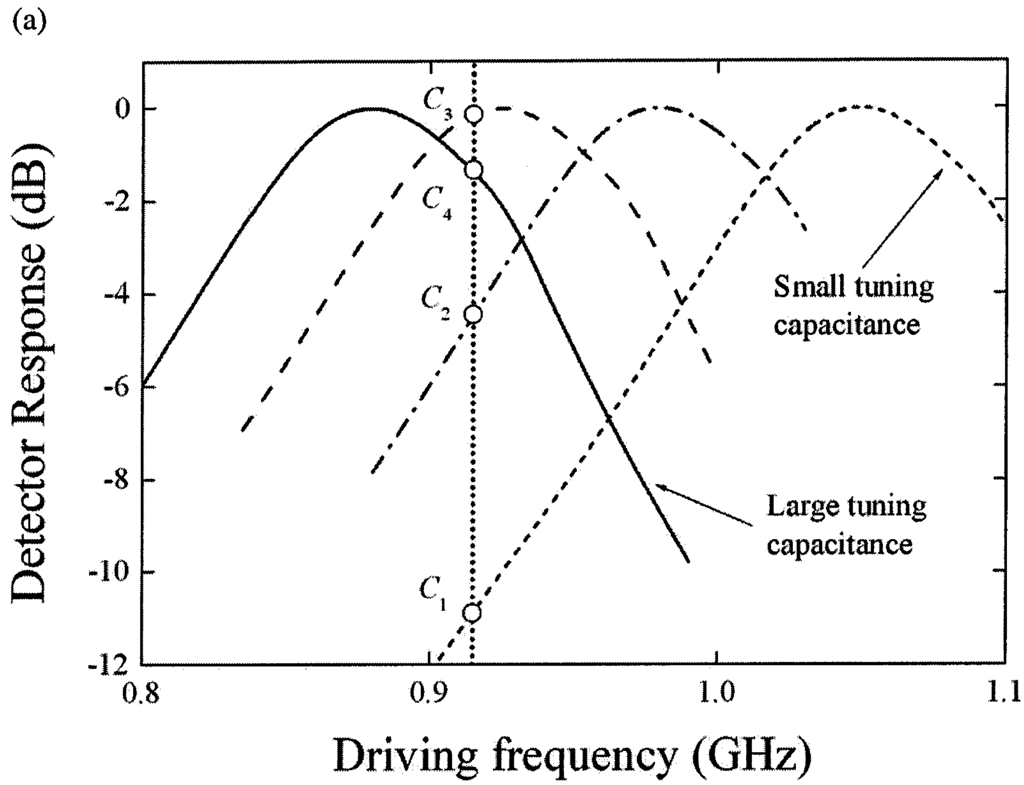
A circuit with a large Q-factor will have a very narrow and steep frequency response, and therefore a small bandwidth. For purposes of tank circuit design it is important to note that once resonant frequency is specified, L and C become fixed. Q-factor, and equivalently bandwidth, will therefore be entirely dependent on the value specified for the resistive element. For example, increasing resistance will lead to a lower Q and therefore a wider bandwidth. The relevance of these dependencies will become clear when loading effects are discussed in a subsequent section.

2.5.2. Tuning curves and design parameters

One significant difference exists between the 'resonant curve' one might expect an RLC circuit to generate, and the 'tuning curve' output observed when the SCM is employed experimentally. While RLC circuits are normally described by their frequency

response, which illustrates the current amplitude variation over a continuous range of driving frequencies, the *Veeco* capacitance detector is instead driven by a fixed frequency oscillator. Consequently, the output consists of a 'tuning curve', in which the tuning capability is provided by a voltage-controllable capacitive element, an internal varactor diode. A control signal allows the circuit capacitance to be varied, effectively shifting the resonant curve in frequency space. The overall tuning curve is constructed by driving the circuit at a fixed frequency, and plotting current amplitude against varactor capacitance as it sweeps over its tunable range. Figure 18 illustrates the equivalence between resonant and tuning curves by demonstrating how a tuning curve is constructed based on a set of resonant curves. Panel (a) shows four curves, representing the range over which the *Veeco* internal resonant circuit can be tuned by adjusting the control voltage supplied to a varactor diode. Since these curves retain their shape, their positions can be characterized by peak locations, which shift toward lower frequencies with increased tuning capacitance. A resonant curve illustrates how the amplitude of current in a circuit changes based on the frequency at which the circuit is driven. One particular drive frequency, as specified in equation 2.4, will cause a given RLC circuit to resonate, maximizing the output amplitude if the circuit is configured in series. However the Veeco instrument employs a 915 MHz fixed frequency driving oscillator, denoted by the vertical line. A tuning curve is constructed by sweeping C_{tune}, and plotting the amplitudes at which the corresponding resonant curves intercept the drive frequency. This is to say that rather than determining which drive frequency will maximize the output amplitude, a tuning curve peak indicates the value of variable capacitance which enables the circuit to resonate at 915 MHz.

(a)



(b)

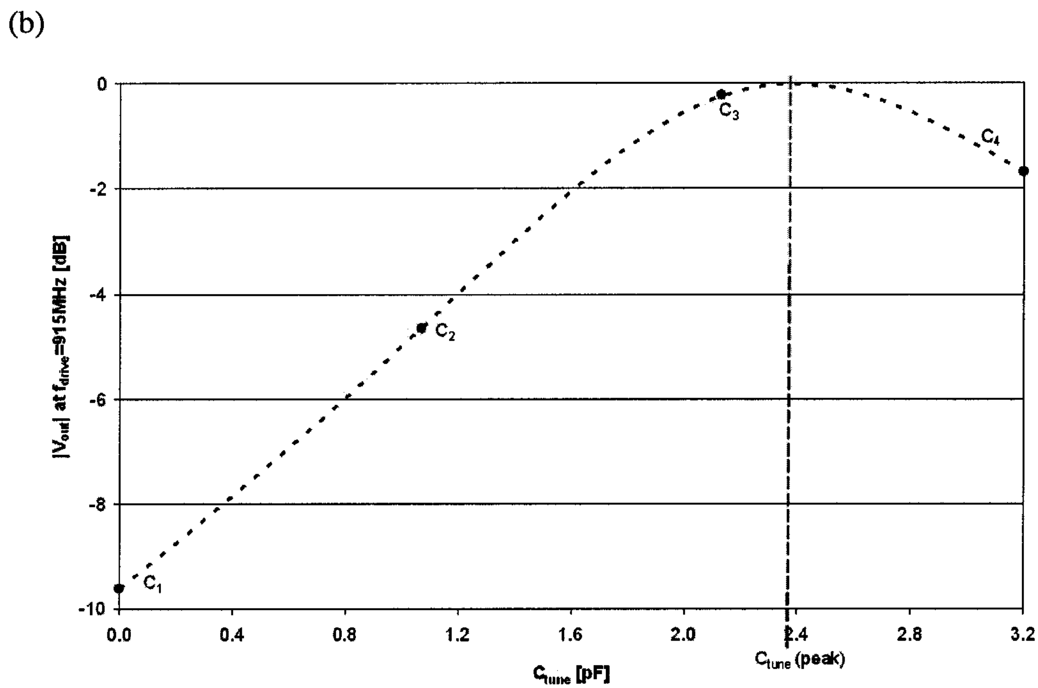


Figure 18 - Sweeping the internal tuning capacitance generates a set of resonant curves, as shown in (a). Since the circuit's drive frequency is fixed, each resonant curve's amplitude at that drive frequency is used to construct a corresponding tuning curve, (b).

While the quantitative details involved in the design and simulation of a capacitance sensor model will be thoroughly discussed in chapter three, the following provides a general overview of the influence one might theoretically expect each circuit component to exert on the sensor's overall behaviour. Since the circuit output can be modeled as a Gaussian curve, particular attention will be paid to the components that govern resonant frequency and bandwidth, analogous to mean and deviation respectively. As explained in the previous section, resonant frequency depends exclusively on reactive circuit components, so it makes sense for the absolute capacitance measurement technique to monitor changes in this characteristic affected when capacitive samples are probed. An optimally designed tank circuit will have C and L specified to enable tuning over a range surrounding the driving frequency, and R set to give a Q-factor large enough to facilitate resonant peak detection.

2.5.3. Effect of loading

When the probe is made to contact a capacitive sample, the DUT becomes connected in parallel with the tank circuit as shown in figure 19. The overall circuit capacitance increases since it is the sum of these contributions, and the resonant frequency decreases accordingly. The tip-sample junction is also expected to exhibit a nonzero contact resistance, supplementing the tank circuit's inherent resistance. Equation (2.5) shows that increasing R leads to a reduced Q-factor, which means larger bandwidth. Though determination of sample capacitances relies on f_{res}, whose value is independent of circuit resistance, maintaining the tuning curve shape under load is desirable since it facilitates peak detection.

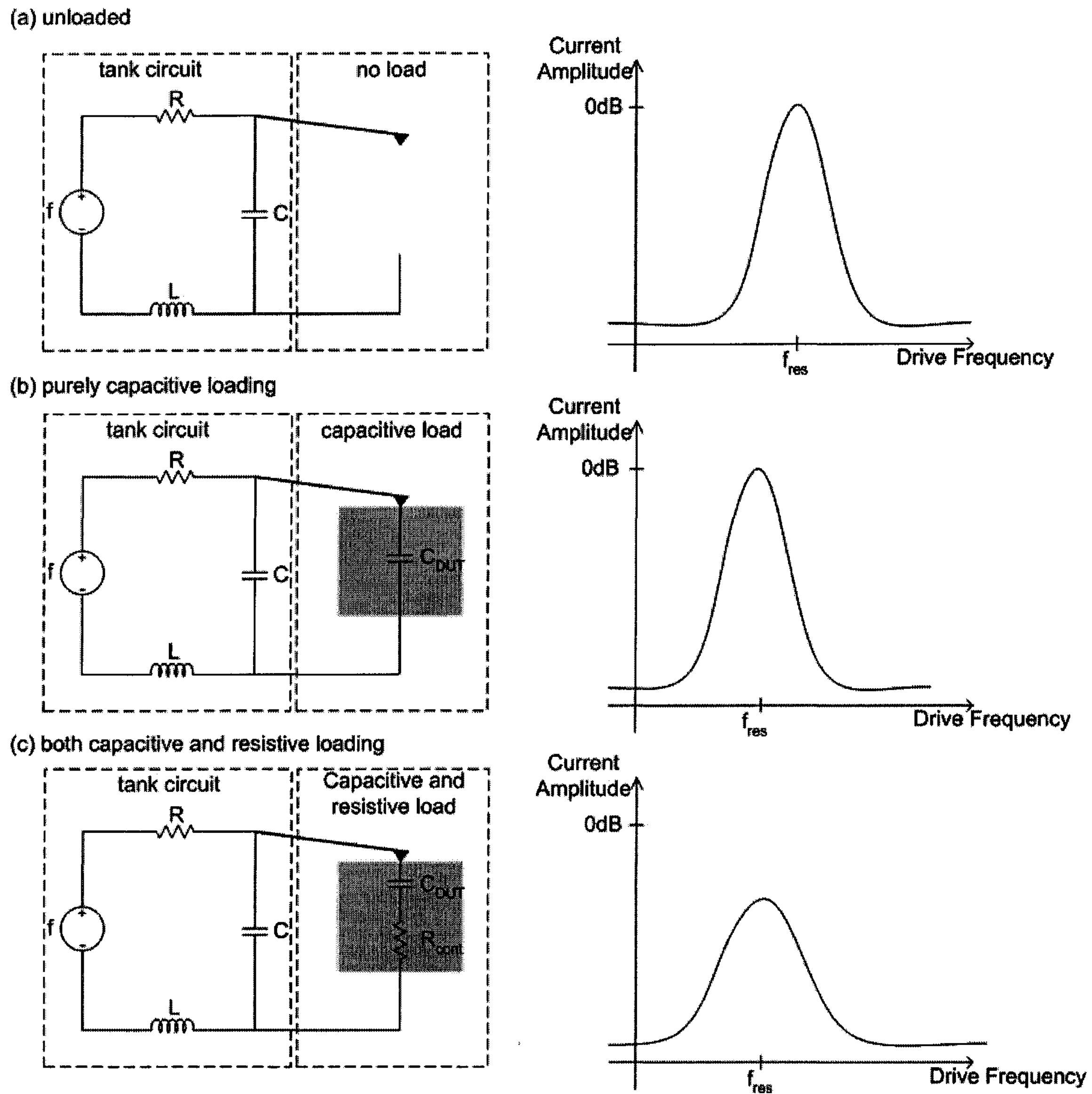


Figure 19 - Frequency response of a series RLC tank circuit under various loading configurations.

2.5.4. Suitability for this work

The most important consideration when evaluating the suitability of the *Veeco* capacitance sensor is whether the devices expected to be measured will trigger a discernable change in tuning curve peak location. The scanning capacitance microscope's capability for detecting minute depletion capacitance variations indicates that the circuit must inherently have a very high Q-factor, therefore even peak movements due to small sample capacitances should be relatively easy to observe.

2.6. Conclusions drawn from background theory

This section has examined three important components of the scanning capacitance microscope in light of each one's suitability to the proposed absolute capacitance measurement technique. All were found to be capable of the presumed performance requirements, so the method can be deemed to be theoretically feasible.

This chapter also included a thorough description of the typical SCM imaging method, for two reasons. First, several of the physical principles governing scanning capacitance microscopy are also important to the operation of this novel technique. Next, presenting the instrument's usual operation makes it easy to recognize aspects in which the two methods differ.

3. The system equivalent circuit model: simulating sensor response

To evaluate the feasibility of the proposed quantitative capacitance measurement technique, it is important to establish the capabilities and limitations of the entire apparatus. Data acquisition involves not only the embedded RLC capacitance sensor from *Veeco*'s SCM module, but also an SPM probe and the sample being measured. Together, these three components form a resonant system, whose equivalent circuit can be modeled and simulated using SPICE software in order to mimic the instrument's behaviour. Such a model is useful for two reasons: First, it allows observation of the interactions between components, qualitatively establishing the system's expected behaviour. Second, software simulation permits circuit parameters to be varied, enabling determination of both limitations and optimal operating conditions for the apparatus.

This chapter presents the development and refinement of a system equivalent circuit model meant to represent the quantitative capacitance measurement platform. Since only general aspects of the RLC circuit design are known, the simulation process begins in section 3.1 by testing a generic circuit, then refining parameter values based on experimental observations until its behaviour replicates that of the physical instrument. Having successfully modeled the basic capacitance sensor, section 3.2 focuses on testing various experimental parameters. This allows the consequences of employing probes of various compositions and geometries to be rapidly observed. Finally in section 3.3, the circuit is modeled to include loads representative of the samples to be used in the experimental work. This exercise enables a set of response curves to be constructed, against which the actual circuit's behaviour may be compared.

3.1. Construction of circuit model

This section is concerned with the process of designing a model representative of the capacitance sensor housed within the *Veeco* SCM module, based on its documented specifications. At this time the complex effects of incorporating probes and samples are disregarded, but both will be examined thoroughly in subsequent sections. While it was argued in section 2.5.1 that the *Veeco* capacitance sensor likely has a series RLC configuration, suitable component values must now be chosen for inclusion in the model. Since the defined circuit framework is sufficiently general that many sets of component values could yield the desired behaviour, selection is further restricted by stipulating that physically and practically realizable values must be chosen for each of the components. This section explains and justifies the design process followed in reconstructing an equivalent circuit representation of the capacitance sensor's behaviour.

3.1.1 Replicating voltage-controlled tuning

Though the internal capacitance sensor behaves as a standard RLC circuit, an accurate simulation will take into account two subtle variations: First, as explained in section 2.5.2, a fixed 915 MHz oscillator drives the circuit while a voltage-controllable varactor diode alters its resonant frequency. This is in contrast to a typical static circuit whose resonant frequency is determined by a sweeping drive signal, and dictates that the model should include a variable capacitor. Next, the *Veeco* circuit is known to incorporate a trimming capacitor, which can be manually adjusted to coarsely shift the varactor diode's tuning window. Since the coarse tuner remains unchanged throughout any given measurement session, it shall be modeled as a static capacitor. However, it is important that the model being developed distinguishes C_{trim}, the fixed trimming capacitor, and C_{tune}, the voltage-controlled varactor capacitance, by placing both components in parallel as illustrated in figure 20.

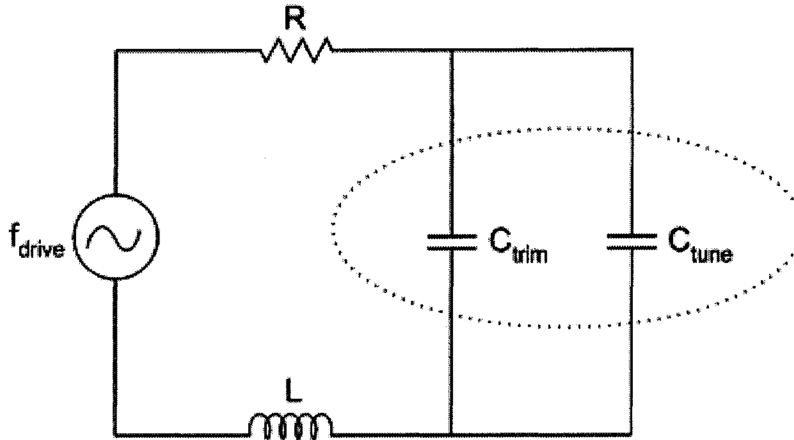


Figure 20 - Resonant circuit with trimming capacitor and varactor diode configured in parallel.

Since vendor documentation specifies that the unloaded circuit's resonant frequency can be varied between approximately 880 and 1050 MHz, the design process begins by choosing specific inductance-capacitance pairs whose product satisfies

$$f_{res} = \frac{1}{2\pi\sqrt{LC_T}} \tag{3.6}$$

where C_T, represents the sum of both the trimming and varactor capacitances. Figure 21 shows sets of L and C_T at both extremes of the equipment's resonant frequency range, based on which the circuit inductance will be selected.

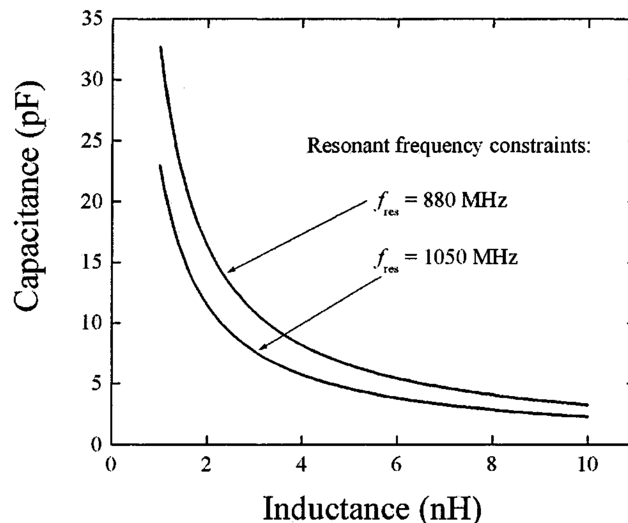


Figure 21 - Capacitance-induction pairings enabling resonance at 880 and 1050 MHz.

Though a value is specified at this stage to facilitate explanation of the design process, one's choice of L is arbitrary. Since the objective of this exercise is to mimic a physical system however, the selection of L is subject to several constraints: It is important to ensure both that the magnitude of C_T will be consistent with those of samples being probed, and that inductors, trimming capacitors and varactor diodes of the specified values can all be realized with physical devices. Ensuring consistency among the system's three prominent capacitances implies that the trimming capacitor will have the largest magnitude, followed by the varactor diode, C_{tune}, and then that of the DUT. This relationship reflects the relative significance of each component on tuning curve movement, with the largest capacitances being the most influential. To ensure that samples on the order of 1 pF will produce observable tuning curve shifts, C_T should be no more than an order of magnitude larger. According to figure 21, setting L to approximately 3 nH will give the appropriate range of C_T values.

For a fixed inductance, a corresponding range of C_T values can be calculated based on the known resonant frequency span: For $f_{res} = 880 \text{ MHz}$,

$$\begin{aligned} C_T &= \frac{1}{(2\pi f)^2 L} \\ &= 1.09\times10^{-11} \text{ F} \end{aligned}$$

and similarly, $C_T = 7.7\times10^{-12}$ F for $f_{res} = 1050$ MHz. It remains to be determined what proportion of this 7.7 to 10.9 picoFarad range should be assigned to the fixed trimming capacitor, with the remainder representing the varactor diode capacitance. Since this work employs loads with capacitances up to 1 pF, we presume that the voltage-controlled tuning mechanism should involve proportionately larger capacitances, and that coarse adjustment should require still larger components. As a result, the equivalent resonant circuit capacitance sensor model is set to include 7.7 pF of trimming capacitance, with a varactor diode whose capacitance can range from 0 to 3.2 pF. Recall that the simulations constitute a feasibility study, and that numbers are inserted at this stage only to facilitate the design process. Quantitative analysis would require that the model be refined based on experimental data.

3.1.2 Determining stray capacitance

This section expands the resonant circuit model developed thus far to account for a measurement artifact arising from interaction between the probe and sample surface. While the procedure was designed so that incorporation of a sample into the resonant circuit will have a measurable effect, stray capacitance is an inevitable consequence of placing the probe and sample in close proximity. Unless these parasitic effects can be recognized and separated from the true DUT capacitance, the technique cannot be considered viable. Here we propose that open-circuit measurements will enable the effects of stray capacitance to be distinguished and hence eliminated.

In order to accurately model *Veeco's* detection apparatus, the simulated circuit must be modified such that its behaviour replicates that observed in the physical instrument with the tip very near the sample surface, but not contacted. Since this parasitic effect contributes to the total measured capacitance, C_T, it is properly modeled as appearing in parallel with the trimming and tuning capacitors as shown in figure 22. Determining how much capacitance should be added to the model to account for stray contributions is done by comparing the difference in peak locations between simulated and experimental tuning curves.

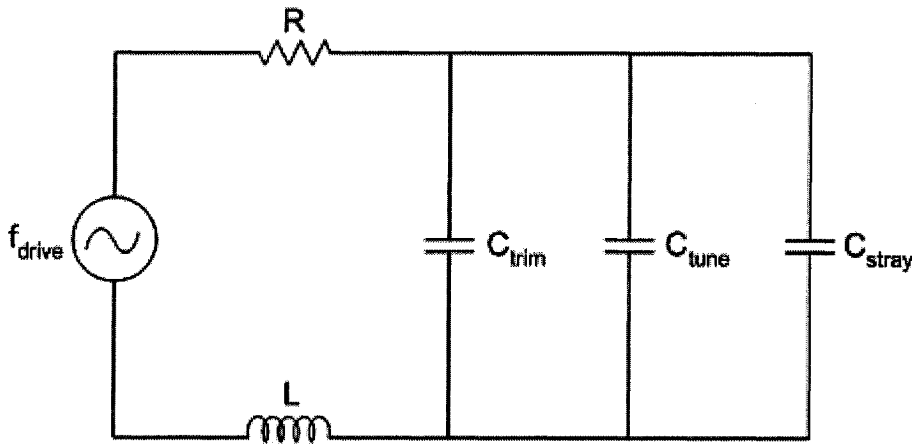


Figure 22 - Inclusion of stray capacitance into the circuit model.

Since the tuning curve peak location indicates the varactor diode capacitance for which the RLC circuit driven at 915 MHz becomes resonant, adding stray capacitance in parallel reduces the C_{tune} contribution necessary for resonance.

Graphically constructing the tuning curve or solving

$$C_{tune} = \left[\frac{1}{(2\pi f_{res})^2 L} \right] - C_{trim} \tag{3.7}$$

for $f_{res} = 915$ MHz and $C_{trim} = 7.7$ pF reveals that with C_{stray} omitted, the circuit model requires 2.4 pF of varactor diode capacitance in order to resonate at 915 MHz. In contrast, the experimental circuit with probe placed near the sample has a tuning curve, shown in figure 23, with peak location at 1.45 V.

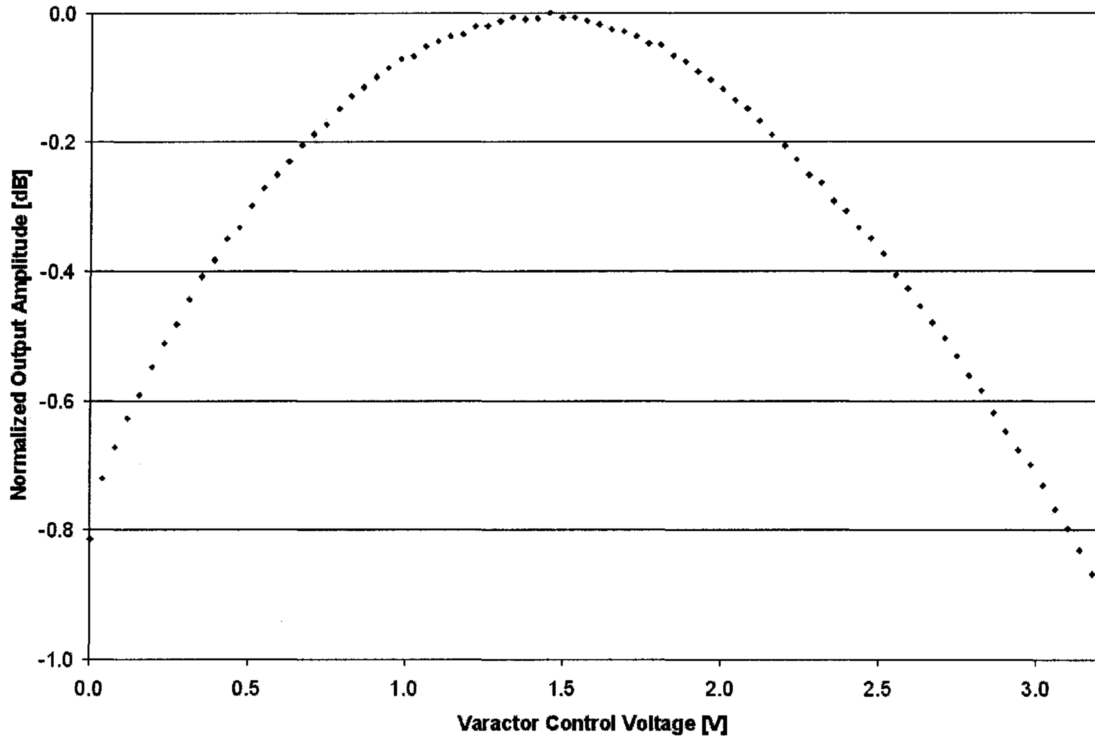


Figure 23 - Experimental tuning curve with tungsten probe engaged.

If the 0-10 V scale of varactor diode voltage is linearly overlaid by the 0-3.2 pF range of tuning capacitance used in simulations, then each volt can be taken to represent 0.32 pF of varactor diode capacitance. This places the experimentally observed peak at 0.464 pF, roughly 1.94 pF lower than in the simulation. This later value must therefore be added to the model circuit to account for stray capacitance. It is important to realize that the stray capacitance level determined by this exercise depends on the specified varactor diode tuning range, but not on the specified trimming capacitor value. This is to

say that if C_{trim} had been set at 5.7 pF in the previous example rather than 7.7 pF, then although equation 3.2 would yield a tuning curve peak at $C_{tune} = 4.4$ pF, the experimental peak would occur at 2.464 pF on the revised varactor diode tuning scale. Hence the stray capacitance level is independent of one's choice of trimming capacitor value. The stray capacitance tuning curve is thus the reference curve from which we determine sample capacitance.

3.1.3 Adjusting bandwidth

In order for the model circuit to accurately represent the experimental apparatus, the tuning curves they produce should have the same shape. To compare the respective tuning curve shapes we examine a characteristic called bandwidth, which is governed in part by a resonant circuit's internal resistance. As we will demonstrate in section 3.3, matching the experimental bandwidth conditions is of particular importance to the characterization of a second measurement artifact, contact resistance between the probe and sample. Since the resonant circuit's capacitance and inductance values have already been fixed, changing the resistive component allows tuning curve bandwidth adjustments to be made without affecting other performance characteristics. As we did when determining stray capacitance levels, experimental data will be studied, in this case the average engaged tuning curve for all tungsten probe measurements shown in figure 23. The model's internal resistor will then be set to ensure simulations will replicate the observed system behaviour. Unfortunately, stray capacitance levels present in this configuration cause the experimental tuning curve peak to shift toward the left edge of the varactor diode's tuning range. Consequently, the curve's amplitude at the left edge of the window, for $C_{tune} = 0$, is only -0.81 dB below peak level. Since this attenuation level also occurs to the right of the tuning curve's apex 3.14 V away, we can conclude that the experimental system's -0.81 dB bandwidth spans 31.4 percent of its varactor diode's tunable range. In order to ensure an equivalent model, R must be set such that the circuit's -0.81dB bandwidth will span one picoFarad of the overall 3.2 pF simulated tuning range. Repeated simulations while varying the circuit's resistance value yields the following linear dependence

$$BW[\text{pF}] = (0.5428) \cdot R[\Omega] - 0.017 \tag{3.8}$$

leading to the conclusion that $R = 1.87\ \Omega$ will produce the desired 1 pF bandwidth.

3.2 Modeling various sensor types

3.2.1 The system equivalent circuit – stray capacitance and contact resistance

After careful consideration of cost, composition and physical geometry, it was decided that both solid tungsten and platinum-iridium-coated types of SPM sensors would be employed in testing the absolute capacitance measurement technique. This section is devoted to modeling each one, accounting for the effect of their respective features by changing selected circuit parameters, shown in schematic as figure 24. Since a Pt-Ir probe's conductivity relies on the integrity of a thin coating, one might reasonably predict that the tip-sample junction would rapidly cease to behave as an Ohmic contact after only a few trials. Conversely, a tungsten sensor could be expected to maintain a low contact resistance through its useful life, since its apex should remain conductive despite tip wear. More unpredictable are the consequences of physical differences between the two types of sensors, particularly with respect to stray capacitance levels. Since the tungsten probe's geometry incorporates more metal in close proximity to the sample surface, it might be expected to trigger higher levels of C_{stray}.

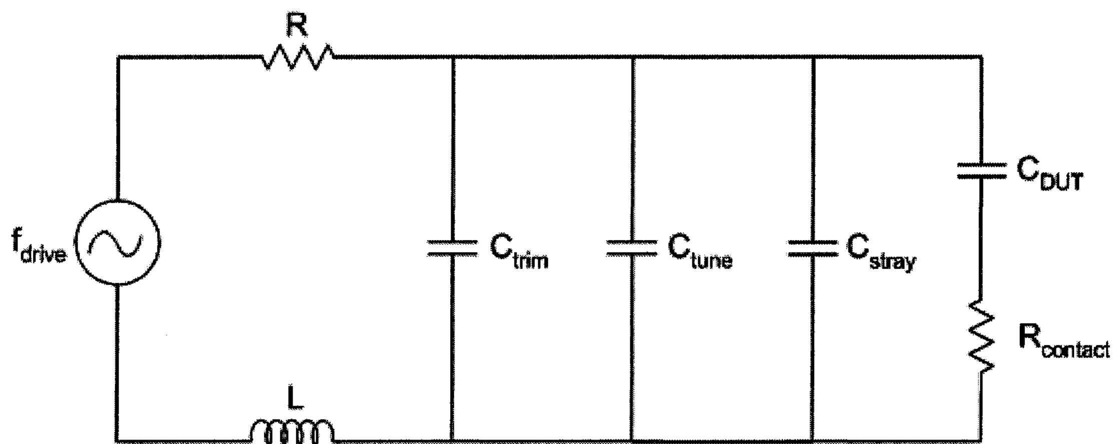


Figure 24 - System equivalent circuit including probe-sample effects

3.2.2 Platinum-iridium coating

Imaged using a scanning electron microscope and shown in figure 25, the platinum-iridium coated probe has a simple rectangular cantilever design typical of many SPM sensors. Though they are used regularly in scanning capacitance microscopy

applications, metal-coated probes have limited effectiveness for conductive imaging techniques entailing high contact forces.

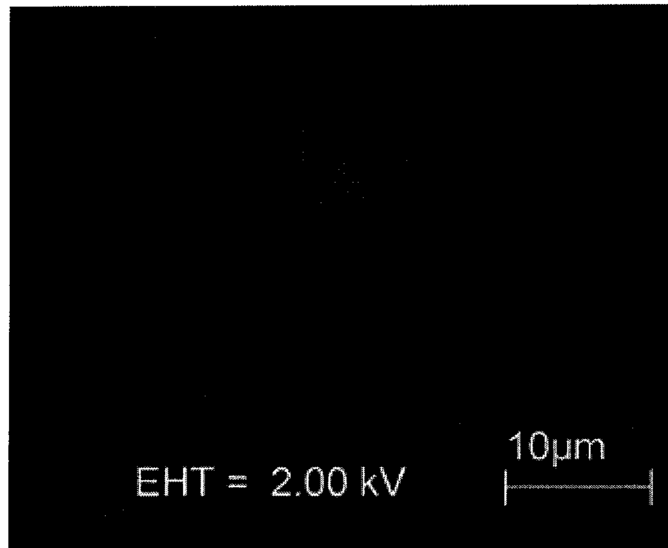


Figure 25 - Platinum-iridium coated SPM sensor viewed from below, showing the microfabricated tip

In theory, the absolute capacitance measurement technique should not require forces greater than those used to acquire SCM data. In practice however, the thin metal coating layer erodes far more rapidly while contacting hard tungsten contact plugs than it does while scanning over oxide, so the tip-sample region begins to exhibit high contact resistance, uncharacteristic of an Ohmic junction. Additional downward pressure is required in order to compensate for the nonconductive apex and maintain electrical contact, but this leads to further erosion, eventually rendering the tip blunt and useless. New platinum-iridium coated probes are modeled as excellent conductors therefore, with low contact resistance of roughly 100 Ohms. After five trials however, an accurate representation of these sensors in simulations should include a large resistance, on the order of kilo-ohms, in series with the tip-sample capacitance. As these speculative estimates of contact resistances suggest, the true physical magnitude of this effect is difficult to measure. Simulations were therefore performed using a wide range of contact resistance levels, to determine the model with which experimental results would best align.

A second probe-specific characteristic for which accurate simulations must account is the amount of stray capacitance resulting from interaction between the sample

and sensor. Previously published SCM simulations investigated the stray capacitance levels arising between equivalent platinum-iridium coated silicon probes and doped semiconductor samples [18]. By modeling the individual capacitive contributions of the tip, cantilever and probe housing, they predicted stray capacitance levels on the order of 0.2 pF. While the system used in this work should be similar, the inherent proximity of metal features on the sample surface suggests that stray capacitance would likely exceed the levels calculated in [18].

3.2.3 Solid tungsten

As the SEM image illustrates in figure 26, the tungsten probe's geometry differs in two ways from that of a typical metal-coated sensor: First, the tungsten tip is attached at the end of a standard silicon cantilever, rather than integrated beneath it. Also, the solid tip is longer than the pyramidal metal-coated one, leaving more space between the cantilever and sample surface. Though no prior investigation has been done to estimate the resulting stray capacitance levels, our experimental results showed parasitics on the order of 1.94 pF.

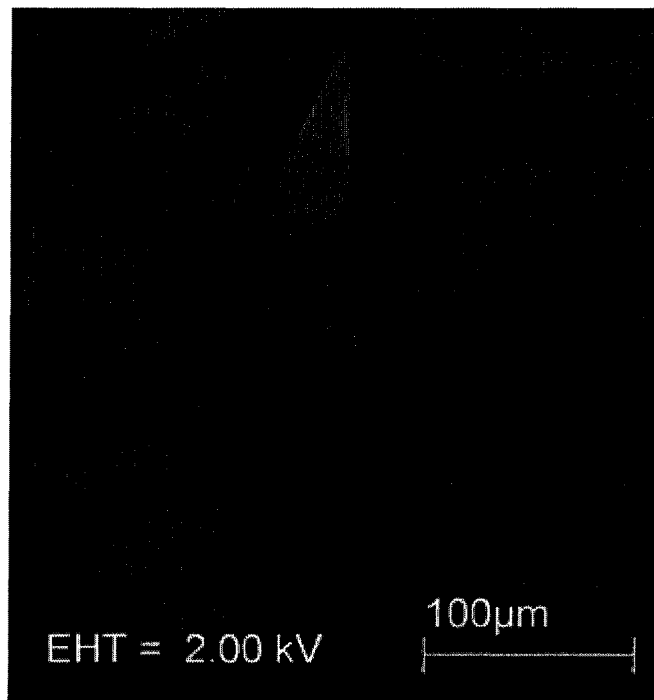


Figure 26 - Solid tungsten SPM probe attached to end of cantilever

Despite elevated levels of stray capacitance, tungsten tips offer several advantages as compared to metal-coated ones. For example, they can be expected to withstand larger contact forces and be less prone to degradation when scanned over metal features than their platinum-iridium coated counterparts. Furthermore, though the tip apex might become dull after extensive use [20], contact resistance would remain unaffected since the probes in question are formed entirely from tungsten. Simulated contract resistances on the order of 100 Ω are consistent with our findings, as we explain in the next section, 3.3

3.3 Simulated response under load – system parameter ranges

Both for tungsten and platinum-iridium sensors, simulations using capacitive loads revealed the relationship between resonant peak shifting and tip-sample capacitance under the simulated experimental constraints of stray capacitance and contact resistance. Repeating these simulations using different tip-sample contact resistances allows a set of response curves to be generated, based on which one can predict the experimental system's ideal operating regime. This section demonstrates how both stray capacitance and contact resistance affect the tuning curve, proposing limitations beyond which the technique ceases to be effective.

The effect of increased contact resistance can be illustrated by varying $R_{contact}$ in the system resonant circuit of figure 24. With C_{DUT} set to 0.1 pF, figure 27 provides a comparison of tuning curves for contact resistances of zero and 1 kΩ. This demonstrates the attenuation and bandwidth broadening due to increased contact resistance, as well as an apparent rightward peak shift. As we shall see in chapter 4 when discussing experimental results, attenuation due to contact resistance becomes a significant factor for samples having large capacitances, as the signal approaches the instrument's noise floor.

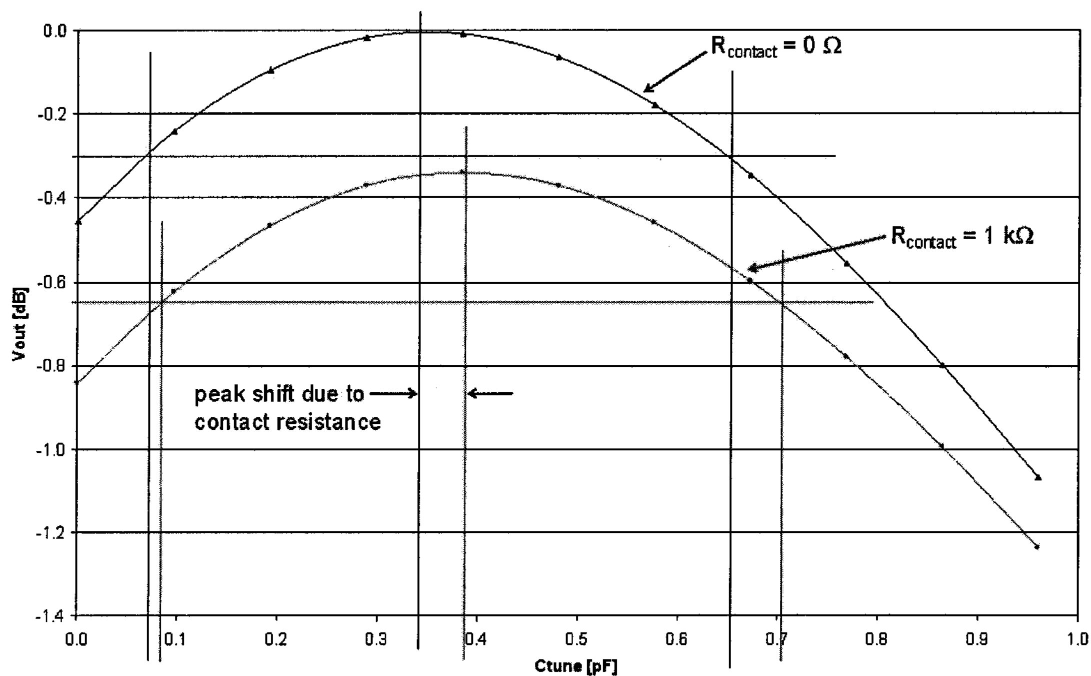


Figure 27 - Impact of increased contact resistance on simulated system tuning curve for a 0.1 pF sample

Consequently, the ideal linear response between sample capacitance and peak position in Ohmic systems begins to exhibit non-linearity with increased contact resistance. This is particularly true for samples of greater capacitances, though the effect only becomes significant to the method's effectiveness when it causes the response curve to stop monotonically increasing. A set of response curves showing the typical relation between sensor peak voltage values and the corresponding capacitance values is shown in figure 28.

Simulations of the system resonant circuit indicate that the technique's usefulness may potentially be limited by the unexpectedly high stray capacitance levels. Since C_{stray} appears in parallel with both C_{tune} and C_{DUT}, it effectively sets the tuning curve's reference position in preparation for device probing, with larger parasitics resulting in a smaller available measurement range. Using the circuit model and accounting for space required to accurately detect the tuning curve peak, observed stray capacitance levels of 1.94 pF should theoretically allow identification of DUT capacitances as large as one picofarad.

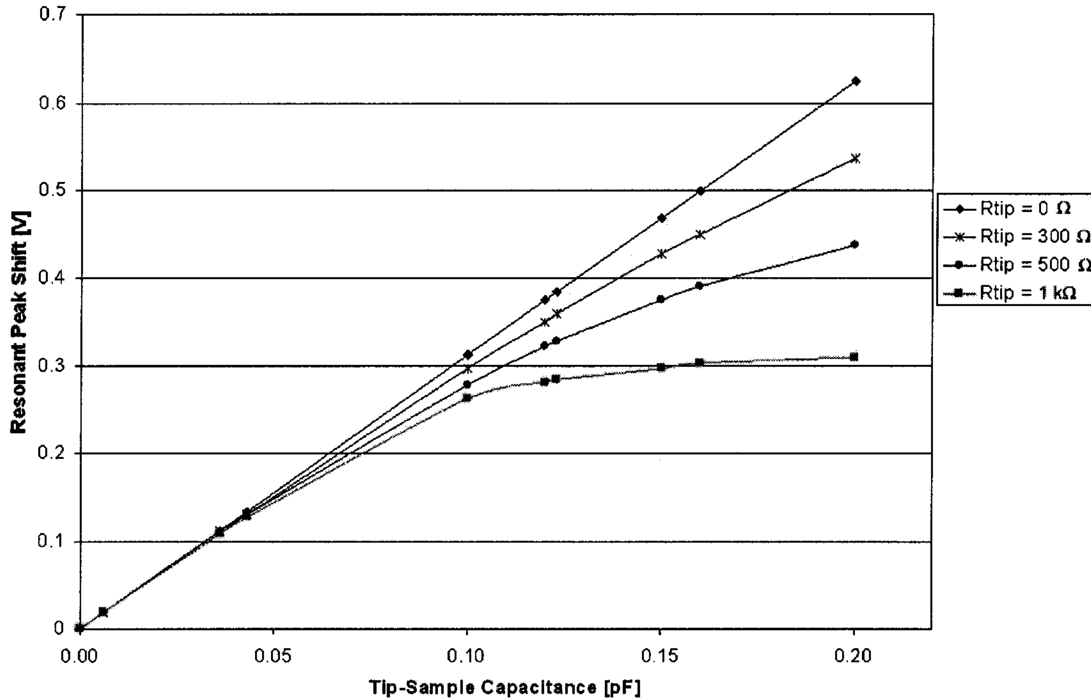


Figure 28 - Simulated response curves for system using tungsten probes

3.4 Conclusions

Though specific details concerning the *Veeco* capacitance sensing mechanism were unknown, an equivalent circuit design was proposed and simulated. Combining this model with observed stray capacitance levels allowed simulations to be performed in which the effects of both capacitive and resistive tip loading on the circuit's tuning curve peak position could readily be observed.

We found that the simulated system equivalent circuit behaved as theoretically expected, and that a physical system comprised of similar components would be viable for the desired types of measurements. The simulation exercise was also a valuable method by which capabilities and functional limitations of the equipment could be determined. Evaluation of the instrument's true performance is best done experimentally however, and these results are presented in chapter four.

4. Experimental results

4.1. Introduction

While preceding chapters have both described the principles by which this quantitative capacitance measurement technique should operate, and simulated the expected system response using modeling software, chapter four presents experimental results physically collected using the *Veeco* apparatus. This is done in order to test earlier hypotheses, and to evaluate the method's feasibility under true measurement conditions. This chapter begins with a description of the experimental method, noting distinctions from the SCM technique for which the apparatus was designed. We also propose tests to ascertain the validity of two critical assumptions concerning stray capacitance levels, upon which the values of all other data rely. Next, we discuss how the physical properties of the probe chosen will impact experimental results. Section 4.3 examines the qualitative effects of loading the resonant circuit directly, without the presence of a probe. Discrete precision capacitors are subsequently measured using SPM sensors, in order to quantitatively observe the system's response to samples with well-known capacitances. Though unintentionally, these experiments demonstrate the technique's limitations with respect to the scale of samples that could potentially be measured. Section 4.4 includes a detailed physical description of the metal-oxide-semiconductor (MOS) capacitive structures targeted in this work, along with an illustration of the typical raw data yielded by measurements of such structures. This data is analyzed in section 4.5, beginning with a general assessment to expose obvious anomalies, progressing to an explanation of the analysis technique, and finally to the application of weighting criteria by which the reliability of each datum is quantified. In section 4.6, the impact of various error sources on the data's precision is assessed, and measured results are compared to expected values as derived from simulated experiments. Finally, the feasibility of this novel method is discussed, along with several recommended developments for improving the technique's usefulness.

4.2. Measurement technique

This section presents a basic description of the apparatus and a complete list of procedures that were followed during the experiments. An important aspect of this work is that while it employs the same equipment, the techniques involved are different from those used in scanning capacitance microscopy imaging. Though SCM implies the capability to measure capacitance, it is actually intended to spatially map a sample's dopant concentration. The name refers to capacitance variations associated with probe-triggered carrier movements, yet SCM operating principles are entirely unique from those used in quantitative capacitance determination. A summary of these distinctions, and an explanation of each one's importance to our novel measurement technique, can be found in this section. This is followed by a detailed description of the data acquisition and analysis procedures undertaken during our experiments, including a method by which stray capacitance levels can be characterized. Finally, we examine both solid tungsten and platinum-iridium coated probes, to determine which type is best suited to acquiring reliable quantitative capacitance measurements.

4.2.1. Distinctiveness of technique to standard SCM

Despite the fact that it employs exactly the same apparatus, several important aspects distinguish this novel capacitance measurement technique from traditional scanning capacitance microscopy methods. Key among these distinctions is that in the case of SCM, the parameter of interest is the local carrier concentration rather than the true sample capacitance. Furthermore, though the presence of a native oxide layer on the sample surface is critical to negate the effects of surface states in SCM imaging, absolute capacitance measurements should instead incorporate a direct, Ohmic junction between the tip and sample. This explains why the method described in this work involves placing the probe directly against metal contact plugs, which oxidize more slowly than silicon regions of the die. Also, since carrier displacements in SCM systems typically produce minute changes in capacitance, while continuous probe movements generate constantly varying parasitic capacitance levels, lock-in amplification is essential to ensure feasible signal detection. In contrast, the absolute capacitance method used in this work is expected to measure considerably larger capacitances in the presence of constant parasitic levels. These conditions arise from the use of a stable, static probe, rendering a

lock-in amplifier unnecessary. Having summarized the differences between these two measurement methods, we now present the manner in which experimental data was acquired and analyzed.

4.2.2. Experimental procedure and generation of raw data

The experiments were performed using a *Veeco* Dimension 3100 atomic force microscope equipped with an SCM module, as shown in figure 8. Trials were carried out using both solid tungsten and platinum-iridium coated silicon probes, to observe the consequences of varying sensor composition and geometry. Measured samples of known capacitance were probed, including discrete precision capacitors and capacitive MOS structures from an *Atmel* 1M flash memory module[2]. The intention was to observe the tuning curve peak shift caused by each known device, then to construct a calibration curve suitable for deducing unknown sample capacitances.

While precision capacitor specifications are clearly defined by their manufacturers, analysis was required in order to determine the capacitance of selected MOS devices. Based on its feature size and date of manufacture, the dielectric layer found in the chosen flash memory module was determined to be SiO_2. A die was cross-sectioned and imaged using transmission electron microscopy (TEM) to determine the insulator thickness, and then viewed optically in plan view to allow measurement of capacitor plate dimensions. The expected capacitance could then be calculated using

$$C = \frac{\varepsilon_0 \varepsilon_r A}{t} \tag{4.1}$$

where A and t are the physical area and thickness dimensions respectively, $\varepsilon_r = 3.9$, the relative dielectric permittivity of SiO_2, and ε_0 denotes the free-space permittivity constant. Since all of the MOS structures examined incorporate a common twenty–three nanometer-thick insulating layer as observed by TEM, their relative capacitances depend solely on the surface areas of their respective plates. Calculated capacitance values for the seven MOS samples chosen ranged between 6 femtoFarads and 1.1 picoFarads, while the discrete precision capacitors were specified to have values between 0.1 and 1.0 pF.

A typical experimental trial proceeded in the following manner: First, conducting adhesive was used to mount the sample on a metal stub to facilitate handling. Precision

[2] Digi-Key P/N AT29BV010A-12JC-ND

capacitors were oriented with one electrode contacting the stub and the other exposed for probing. Dies containing MOS capacitors were mounted in plan view with the substrate backplane against the stub, and then planarized using diamond grit polishing surfaces to remove circuitry, exposing the capacitor plates and their electrical contacts. Samples could then be incorporated into the microscope's internal resonant circuit as shown schematically in figure 29.

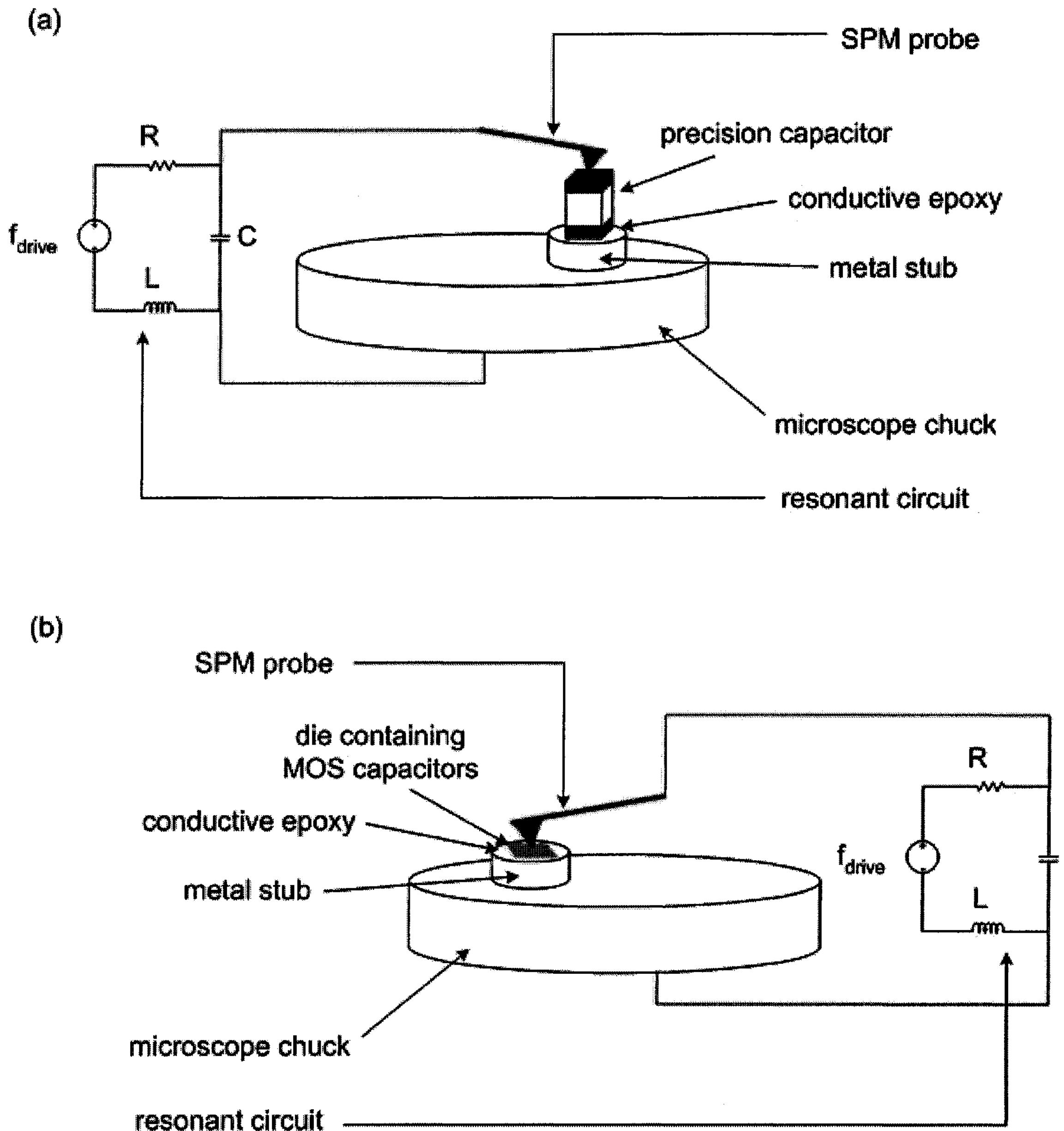


Figure 29 - Schematic of (a) precision and (b) MOS capacitors being connected with internal resonant circuit through probe.

The next step involved laterally positioning the SPM tip above the desired contact region on the sample surface. In the case of discrete components, the upward facing electrodes were large enough that the probe could be easily positioned using the integrated optical microscope. Locating the 400 nm diameter MOS contacts however, required the use of AFM/SCM imaging. In this case, a large region surrounding the contact point of interest was scanned at low resolution, and then the scan window was progressively contracted to eventually restrict probe movement only above the tungsten contact plug. Once the scan window was positioned and sized to ensure the probe movement would be bounded in an area exclusively above the target region, the two-step data acquisition process could begin.

The first measurement was conducted with the probe placed in close proximity to the sample surface but not in physical contact. The appropriate tip-sample separation distance was determined automatically by a feedback mechanism in the instrument, which used a stepper motor to move the probe toward the target until repulsive Van der Waals forces triggered a predetermined amount of cantilever deflection, as described in section 2.2.2. This deflection in turn caused a laser beam, reflected from the cantilever's back side, to shift its point of incidence on a photodiode. When the beam spot had been displaced by a specified distance, the tip was considered to be engaged with the surface. Separation distance between an engaged probe and sample depends on both the cantilever's rigidity and the specified deflection distance, but for this work it was found to be approximately five hundred nanometers. While a feedback loop maintains this constant tip-sample separation, one can observe the full effect of parasitic capacitance contributions on the resonant circuit in the absence of C_{DUT}. Custom *Veeco* control software generates output referred to as a 'tuning curve', shown in figure 30, by plotting the resonant circuit output amplitude in real-time while sweeping the varactor diode control voltage over a zero to ten volt range. This data is exported for analysis, where it will later be determined how much voltage was supplied to the varactor diode in order to maximize the resonant circuit output amplitude.

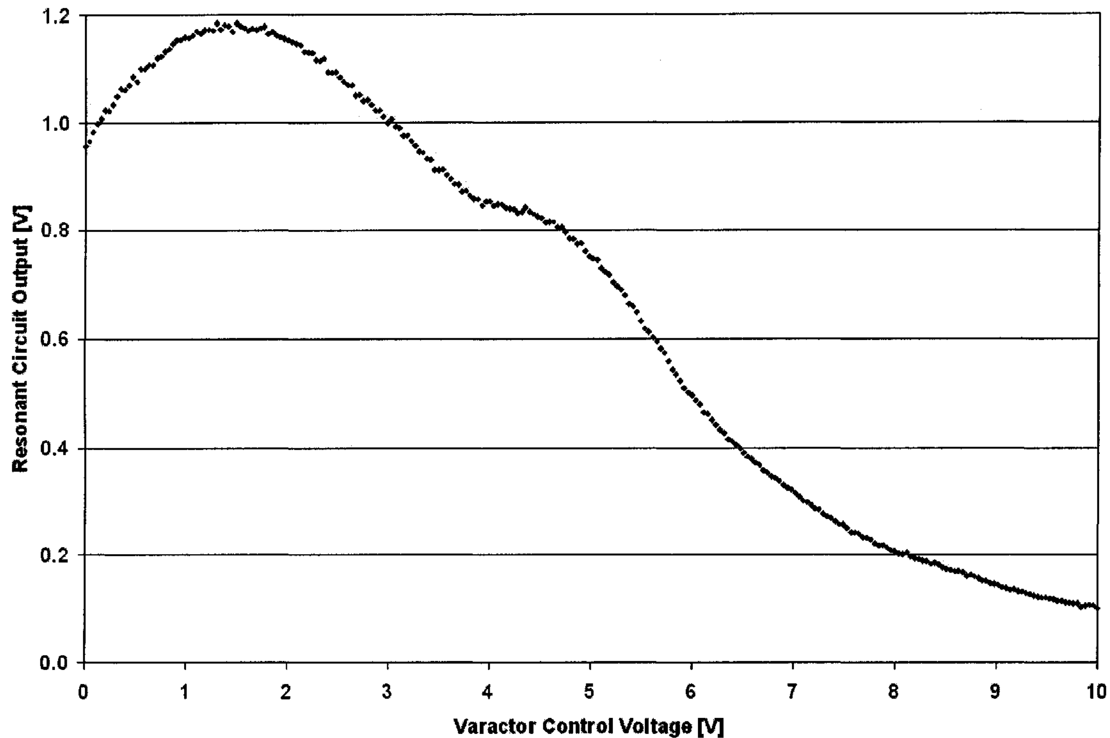


Figure 30 - Plot illustrating the shape of a typical tuning curve displayed by the SPM software

The second half of each experimental trial involves incorporating a sample into the resonant circuit. This is accomplished by using a software-controlled stepper motor, which lowers the tip from its engaged position until it physically contacts the sample surface. Placement of the probe in this state, referred to as 'contact', is accompanied by a visible shift and an overall attenuation of the real-time tuning curve. Furthermore, the tuning curve occasionally becomes unstable when the probe and sample are in contact, as evidenced by figure 31. This is because repulsive Van der Waals forces, which oppose the downward influence of the stepper motor, increase in intensity with diminishing separation distance. As the previous chapter's resonant circuit simulations have demonstrated, attenuation and shifting are both reasonable consequences to expect as the tip is brought into contact with the sample. The shift can be attributed to the additional capacitance introduced by C_{DUT}, while the tip-sample junction contributes a non-negligible contact resistance, resulting in attenuation. The contacted tuning curve data is

exported for comparative analysis against its associated engaged dataset, with the two curves forming a complete measurement trial.

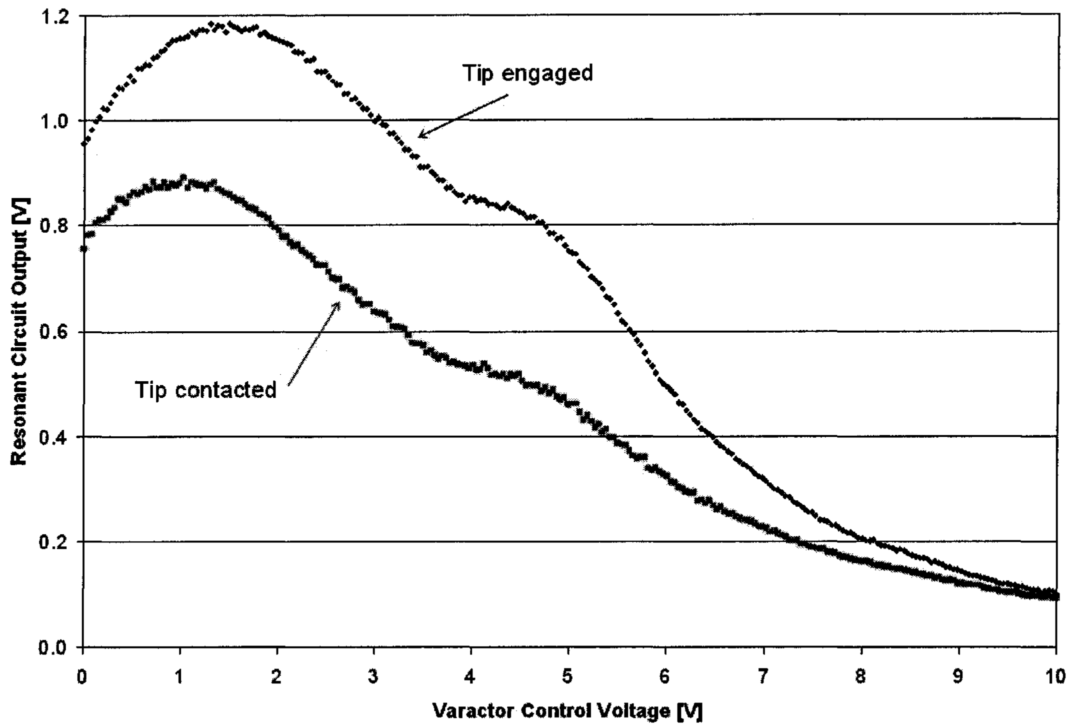


Figure 31 - Illustration of the typical change in tuning curve shape when a capacitor is probed

At this point it is important to note that the quantitative accuracy of our collected data relies on an assumption that the engaged tuning curve provides a good reference of stray capacitance levels. While it is well understood that parasitics vary depending on the probe being used, the physical profile of the sample, and the relative orientations of probe and sample with respect to one another, we must prove that C_{stray} present with the tip engaged is indicative of stray capacitance levels when the probe is made to contact the sample immediately afterward. This is to say that C_{stray} must be shown to be time-invariant and independent of small variations in tip-sample separation. To test the first criterion, we propose to fix the probe in its engage state above the sample for one hour, while capturing tuning curve data at five minute intervals. Analysis will then verify whether or not the peak exhibits any significant time-dependent shifting behaviour. The experiment to evaluate height dependence involves lowering the probe stage toward the

sample surface in 139 nm increments by means of a stepper motor, capturing tuning curve data each time until the tip makes contact. If the peak position remains unaffected, we can conclude that tip-sample separation changes on distance scales relevant to this work have no bearing on stray capacitance levels.

4.2.3. Observations on probe operability and reliability

At this juncture, we compare the two types of probes employed in experimental work, and conclude that those formed from solid tungsten yield the more reliable results. The decision to discard the inferior records generated by platinum-iridium coated probes was arrived at by evaluating acquired data in conjunction with SEM images of tips taken before and after probing. This assessment process was undertaken to evaluate each probe's effectiveness for use in quantitative capacitance measurements, and to conclusively determine which of the two would yield better results.

At less than one quarter the price, platinum-coated silicon probes were seen as a potential low-cost alternative to either solid tungsten or doped-diamond sensors. Though they are quite well-suited for use in scanning capacitance microscopy imaging, the quantitative capacitance measurement technique requires that tips be constantly dragged over abrasive metal contacts rather than a soft native oxide layer. So while it was understood that each metal-coated probe would likely withstand only a few trials before erosion severely degraded the tip-sample junction, it was hoped that they would behave comparably to other probes on a cost-over-lifetime basis. An additional factor motivating the use of platinum-coated sensors was their geometry. Since, as compared to tungsten probes, a smaller volume of metal would lie in close proximity to the sample surface, it was believed that these tips would generate less parasitic capacitance.

This assumption turned out to be false however, as average stray capacitance levels exceeded those generated by tungsten probes. More disappointing however was the seemingly random nature of the results. Even probes being used for the first time, though they demonstrated reliable electrical contact, did not consistently show leftward tuning curve shifts as might have been expected. Predictably, the probes deteriorated after minimal use, as shown in figure 32, until it eventually became difficult to achieve electrical contact between the tip and sample. Owing to inconsistent datasets acquired from each of the seven selected MOS capacitors using four platinum-coated probes, it

was decided that further measurements would not be attempted. The datasets were discarded.

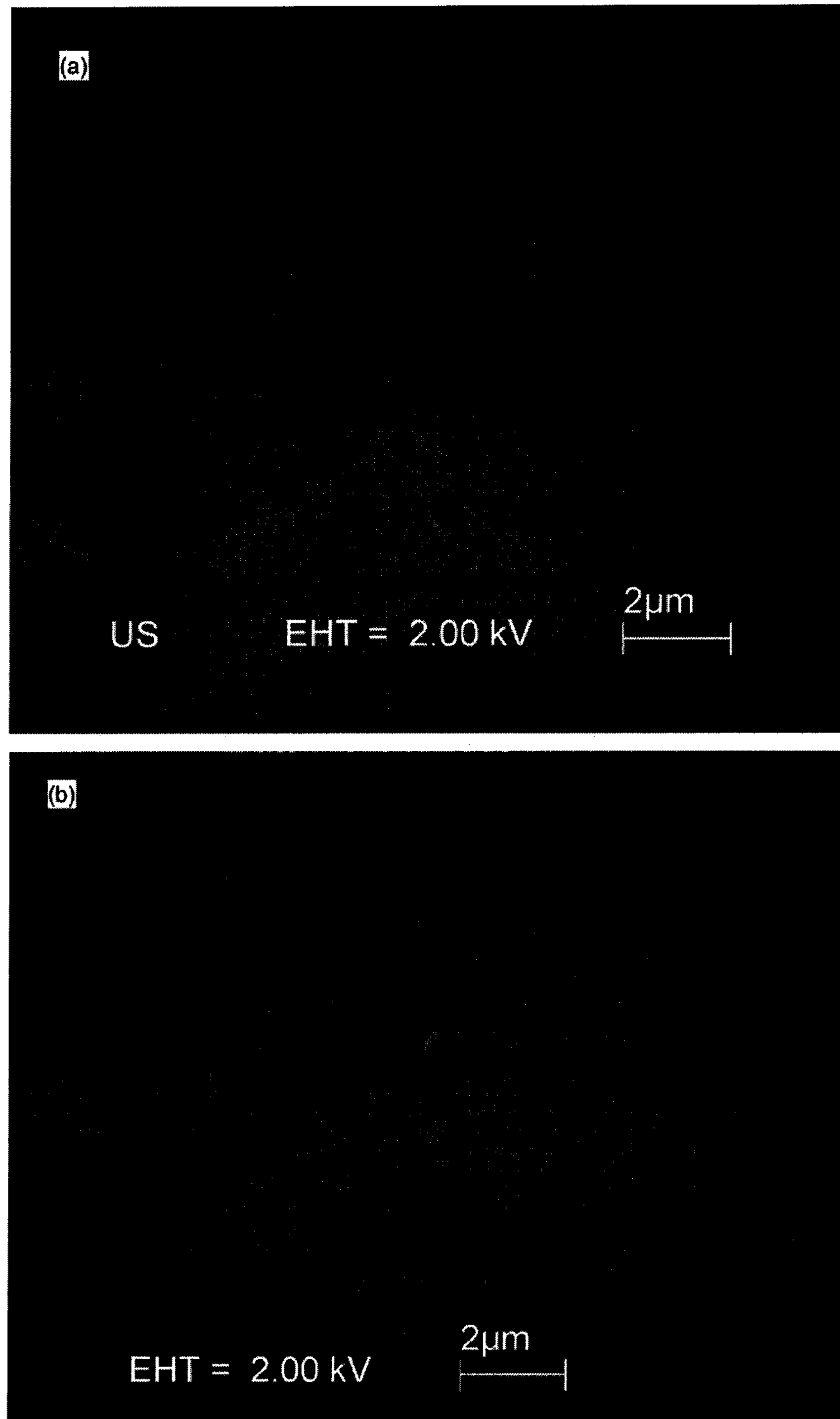


Figure 32 - Platinum-iridium coated probe tip imaged from below, (a) before and (b) after use in quantitative capacitive measurement

Tungsten probes were expected to perform very well when used for absolute capacitance measurements, although their high cost and large radius of tip curvature makes them poorly suited to traditional SCM imaging. Their main advantage is that unlike metal-coated probes, their electrical conductivity would not degrade as they became blunt. Lateral resolution limitations are the biggest shortcoming when using tungsten probes for SCM, since the tips are formed from drawn tungsten rather than micro-machined silicon and hence have a larger radius of curvature. But even the capability for horizontal resolution on the order of hundreds of nanometers makes tungsten probes more than adequate for the coarse probe positioning requirements of absolute capacitance measurements.

When planning the experiment, there was some uncertainty about how these sensors' unique geometry would interact with the sample surface. It was predicted, based on SEM images which revealed considerable metal volumes near cantilevers' ends, that measurements performed with tungsten probes would generate larger parasitic capacitance levels than those performed with platinum-coated sensors. Though the observed 1.94 pF of stray capacitance far exceeded expected levels, there appeared to be 0.3 picoFarads less parasitic capacitance present than when platinum-coated probes were used.

Tungsten probes were not nearly as robust as had been expected however. While erosion and loss of conductivity at the tip apex was negligible, damage in the form of bent and warped tips typically resulted from the extreme forces imposed on the tip-sample junction while attempting to attain electrical contact. In cases of severe apex deformation, as illustrated in figure 33, successfully achieving good Ohmic contact with a capacitor under test could become nearly as difficult as when degraded platinum-coated sensors were used.

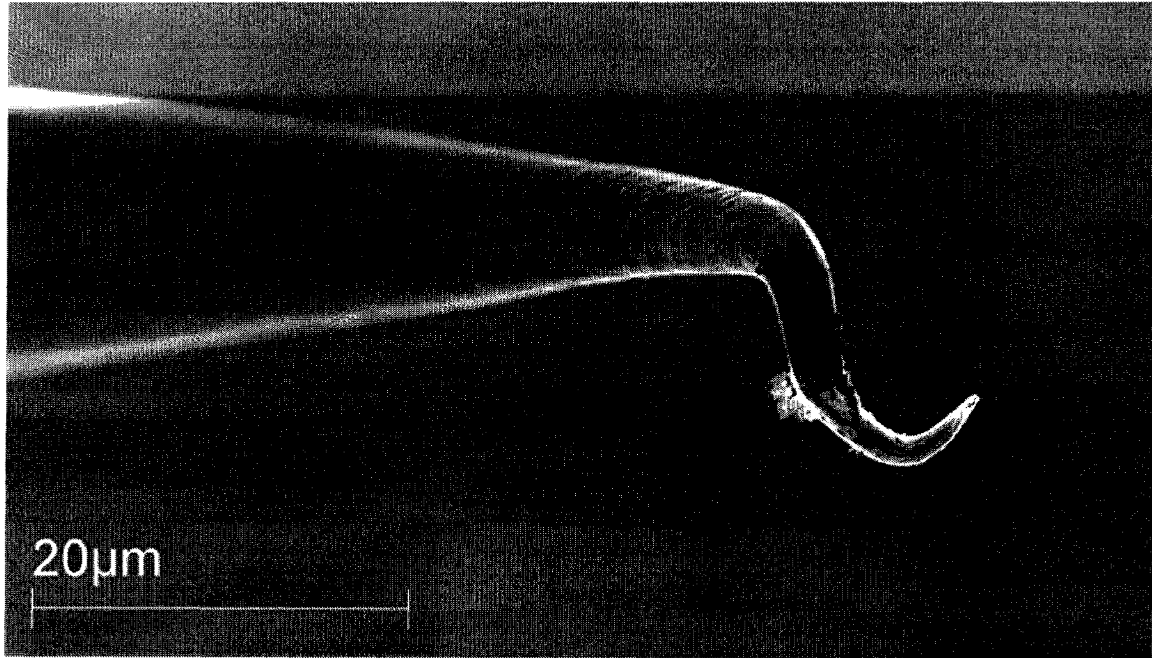


Figure 33 - SEM image of a solid tungsten probe, deformed due to excessive use

In trials performed using five different solid tungsten sensors, repeatable results were obtained and so the data was deemed to be valid. From 175 pairs of engage-contact measurements taken on seven different MOS capacitors using five tungsten probes, the data showed a clear trend toward increased resonant peak shifting in response to larger sample capacitances.

4.3. Limitations to loading sensor resonant circuit

The following section describes the resonant circuit's behaviour when the SPM probe was replaced by a discrete ceramic capacitor. This was done by qualitatively comparing the tuning curve displayed in software with no tip present to one generated when a 1 pF discrete ceramic capacitor[3] was connected between the chuck and the SCM module. This particular experiment was conducted in order to verify that the system behaved as software simulations and hypotheses predicted it should; specifically that the circuit's resonant frequency would decrease with the addition of capacitive load. While it was initially considered a logical first step in testing the method's feasibility, this approach was later discovered to have inherent flaws, discussed below, which prevented it from exhibiting the expected behaviour.

Observations, shown in figure 34, showed that the tuning curve amplitude with a capacitor in place became severely attenuated over its entire range, suggesting excessive load. Despite setting the internal trimming capacitor to its minimum value, the tuning curve shape became severely distorted upon connecting the DUT.

Figure 34 - Tuning curve observed when connecting a 1 pF ceramic capacitor to the resonant circuit in place of an SPM probe. Horizontal axis represents varactor diode control voltage [V], and vertical axis shows resonant circuit output amplitude [V].

No change was seen in the results when the experiment was repeated using ten identical components connected in series, meant to behave as a 0.1 pF capacitor. We then began to consider the possibility that the ceramic capacitors' dimensions were too

[3] *NTE Electronics* P/N 8901D0

large to allow them to operate at the resonant circuit's driving frequency. The instrument's capacitance sensor was designed to detect depletion region capacitances, so the millimeter-scale of these discrete components might have been producing unanticipated transmission line effects.

Since the ultimate application for our quantitative capacitance measurement technique is to characterize the impedance of unknown devices, we felt it was important to calibrate the apparatus using a set of well-known loads to ensure accuracy. For this purpose, a series of discrete precision capacitors made by *Susumu*[4] with capacitances ranging between 0.1 and 1.0 pF were measured. As illustrated in figure 29(a), conductive epoxy was used to mount precision capacitors on individual stubs. A probe was then placed above each sample in turn, and tuning curve data acquired in both the engaged and contacted positions. Since these components had sub-millimeter dimensions, it was anticipated that their behaviour would better mimic that of MOS capacitors. The entire tuning curve was once again attenuated upon probe-sample contact however, an outcome that recurred independently of both component capacitance and probe type. It appeared as though the sensor was not compatible with these samples, and that enabling the capability for measurements of this type would require modification of the internal circuit.

Despite unpredictable behaviour exhibited by the instrument during attempts to measure the more macroscopic discrete capacitors, we expect that it will be suitable for characterization of MOS structures, because such are built on a scale at which the SPM was designed to operate. The experiments described in this section have exposed a limitation of this quantitative capacitance measurement technique, namely its incompatibility with capacitors of larger dimensions. This weakness was not detrimental to MOS capacitor measurements however, the results of which are presented and discussed in the following section.

[4] Digi-Key P/N 408-10xx-1-ND

4.4. The experimental data

We provide a description of the MOS capacitor structures measured for this work, along with an explanation of how their estimated capacitances were calculated. This gives perspective as to the relative scale of components, and completes the physical picture of our measurement system. Some typical raw data sets are presented next, as validation that the experimental technique, when applied to appropriate types of samples, can yield measurable results. Also shown is the raw data acquired while testing the dependence of stray capacitance on both time and tip-sample separation. Though the associated analysis is reserved until section 4.5.3, a qualitative comparison of the raw tuning curves provides confidence in the validity of our assumption.

4.4.1. The samples – "flash memory" MOS capacitors

Analysis was performed on the capacitive components of a flash memory device, such as those shown in figure 35, for two reasons: First, flash devices in general tend to incorporate many large capacitors to fulfill their requirement for extensive charge storage. Also, it was important to choose components whose capacitance would be large enough that their effect on the system's resonant circuit would be clearly visible amid parasitic capacitance, but whose dimensions were small enough to ensure predictable interaction at the driving frequency. A further advantage is that the dimensions of electrical contacts to MOS capacitors are ideally suited to the SPM probing capabilities of our chosen instrument.

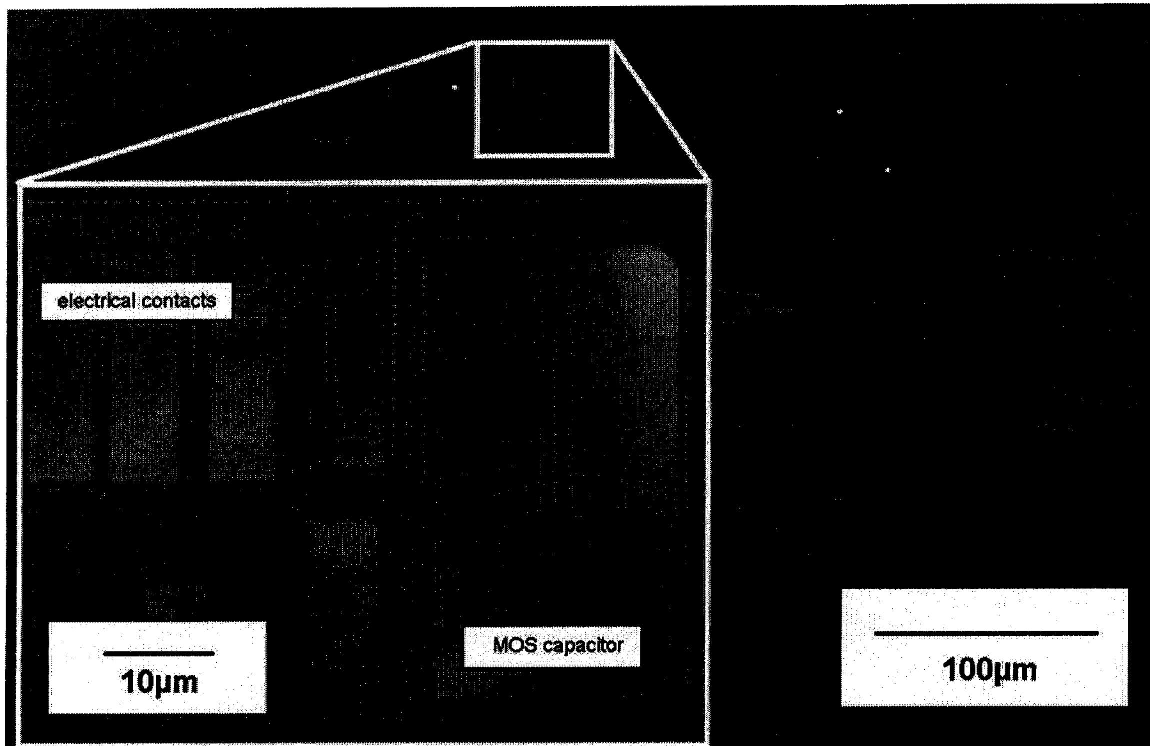


Figure 35 - Plan view optical image of flash memory device, showing MOS capacitors

Seven capacitors of different shapes and sizes were chosen as sample devices for testing. A portion of a typical capacitor and one of its electrical contacts is illustrated in figure 36. Since all of these components were formed at the same depth on a common die, we could be assured that each would contain a dielectric layer of the same composition and thickness. The date of manufacture for the *Atmel* flash module suggested that its insulating layer would almost certainly have been composed of uniform silica, the physical properties of which are well known. Therefore, the devices' relative capacitances would depend entirely on their respective plate surface areas. To determine these surface areas, the top capacitor plates were examined optically in plan view. The resulting images were then calibrated and device dimensions measured using *Quartz PCI* image analysis software.

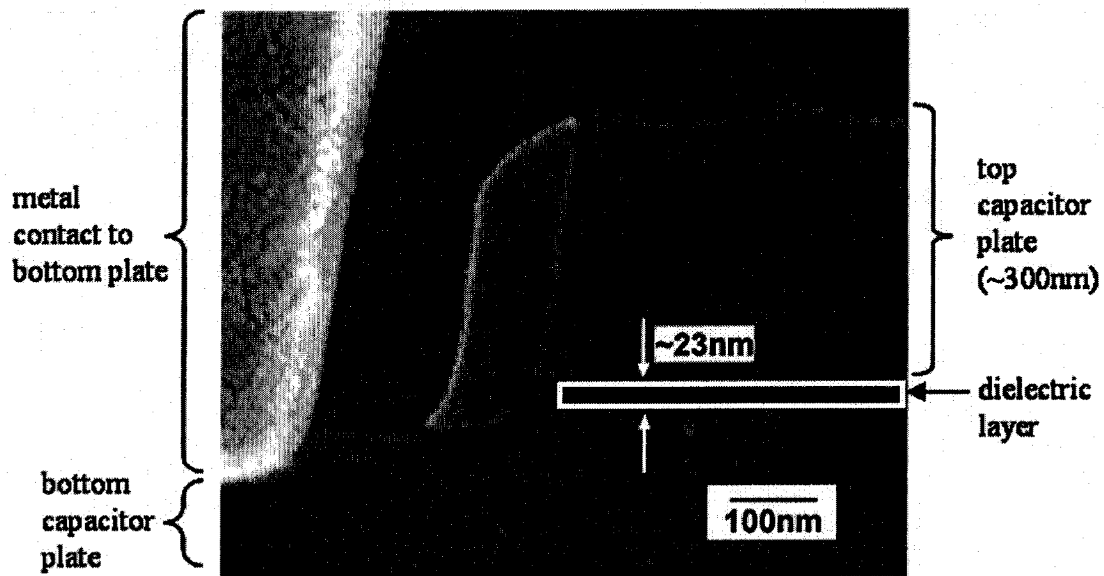


Figure 36 - Cross-section of MOS capacitor

Then, in order to calculate capacitance, the oxide thickness was determined by imaging a second, cross-sectioned die using TEM. Calculations based on these measured dimensions and the relative permittivity of SiO_2 predicted that the set of flash capacitors chosen should have values ranging from 0.006 to 1.1 pF, as summarized in table 1. Uncertainty in these calculations originates in measurement inaccuracy, which manifests itself as an error range about each structure's determined capacitance value.

Table 1 - Physical properties of measured MOS capacitors

DUT Identifier	Horizontal Dimension [μm] ± 2%	Vertical Dimension [μm] ± 2%	Surface Area [μm^2] ± 4%	Dielectric Layer Thickness [nm] ± 3%	Capacitance [pF] ± 7%
flashcap3	1.01	3.96	4.0	23	0.006
flashcap2	3.33	7.20	24.0	23	0.036
flashcap5	15.50	1.85	28.6	23	0.043
flashcapC	5.83	13.71	79.9	23	0.12
flashcap1	3.95	20.75	81.9	23	0.123
flashcap4	5.12	20.81	107.0	23	0.16
flashcapA	18.04	40.76	733.1	23	1.1

4.4.2. Presentation of raw data

Plots on the following page illustrate the typical shape of experimentally acquired tuning curves. Figure 37 includes a data set measured while incorporating a 0.043 pF MOS capacitor into the system resonant circuit (lower curve), along with a reference measurement which indicates the local parasitic capacitance level (upper curve). Comparison of these two plots clearly indicates how probe-sample contact both shifts the tuning curve peak leftward, owing to the sample capacitance, and attenuates the resonant circuit output, indicating a resistive tip-sample junction.

Figure 38 qualitatively illustrates the impact that varying C_{DUT} has on both the tuning curve's amplitude and position. Each of the tuning curves being compared represents the average of all experimental measurements taken on a particular MOS capacitor using a single tungsten probe. Though attenuation is so severe for the largest capacitor that the tuning curve shape becomes distorted, there is a detectable tendency for samples having larger capacitances to trigger greater curve shifting. Note as well the typically increased attenuation with increasing capacitance. This is anticipated for measurements generated at comparable contact resistances. The analyses of these data are presented in section 4.5.

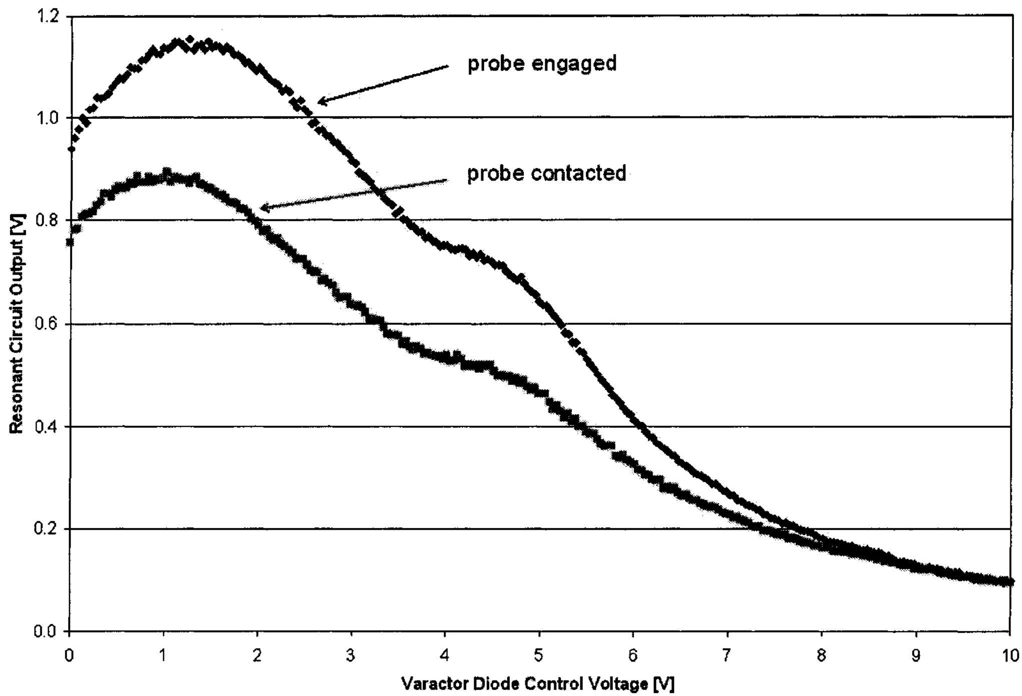


Figure 37 - Typical set of engaged and contacted tuning curves, mreasured on a 0.043 pF capacitor with a tungsten probe, from which one experimental data point will be extracted

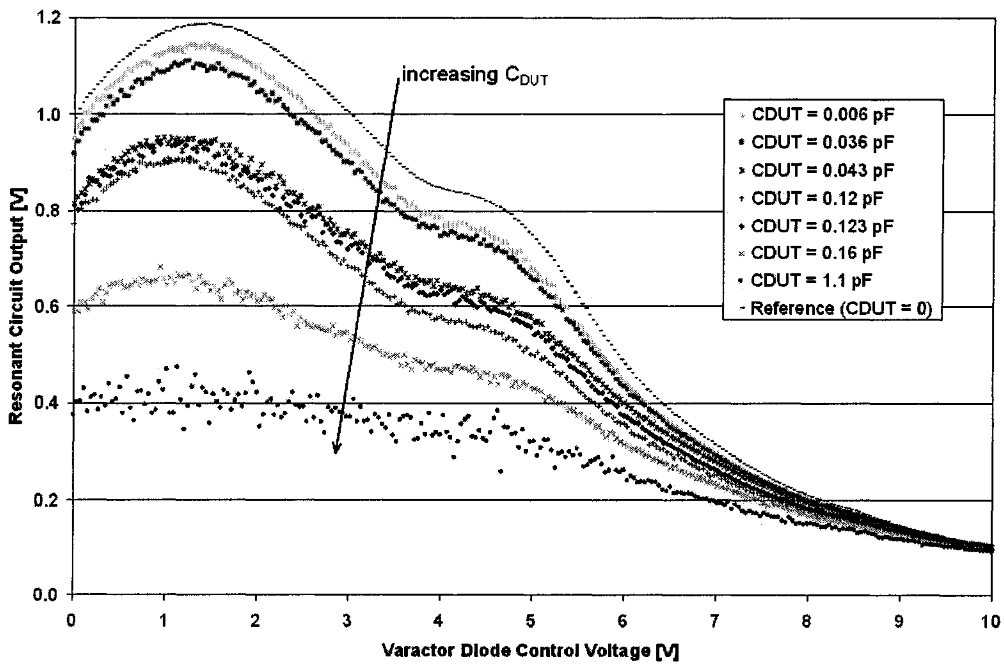


Figure 38 - Tuning curves for samples of various capacitances, derived from values averaged over multiple trials performed with a single tungsten probe

At a fundamental level, the validity of our experimental results depends on the predictability of the system's parasitic capacitance level throughout each trial. The procedure consists of two measurements, with the tip initially very near and then physically touching the sample surface, intended to remove the effects of stray capacitance. In order to effectively reference out parasitic levels therefore, two important conditions must be met: First, it is critical to demonstrate time invariance, ensuring that a static probe-sample system can maintain a stable level of stray capacitance. Next, it is important that parasitic levels remain effectively constant over a limited range of tip-sample separation distances, spanning the engage and contact positions.

To ensure that the first condition is satisfied, tuning curve data was acquired at five minute intervals over a one hour time span, with the tip engaged at a fixed location above the sample surface and the system isolated from its surrounding environment. A portion of the raw data obtained in this experiment is shown as figure 39, which demonstrates that the parasitic capacitance interaction between a static probe and sample surface exhibits very little fluctuation over time, as the analysis of these data, presented in section 4.5.3, confirms.

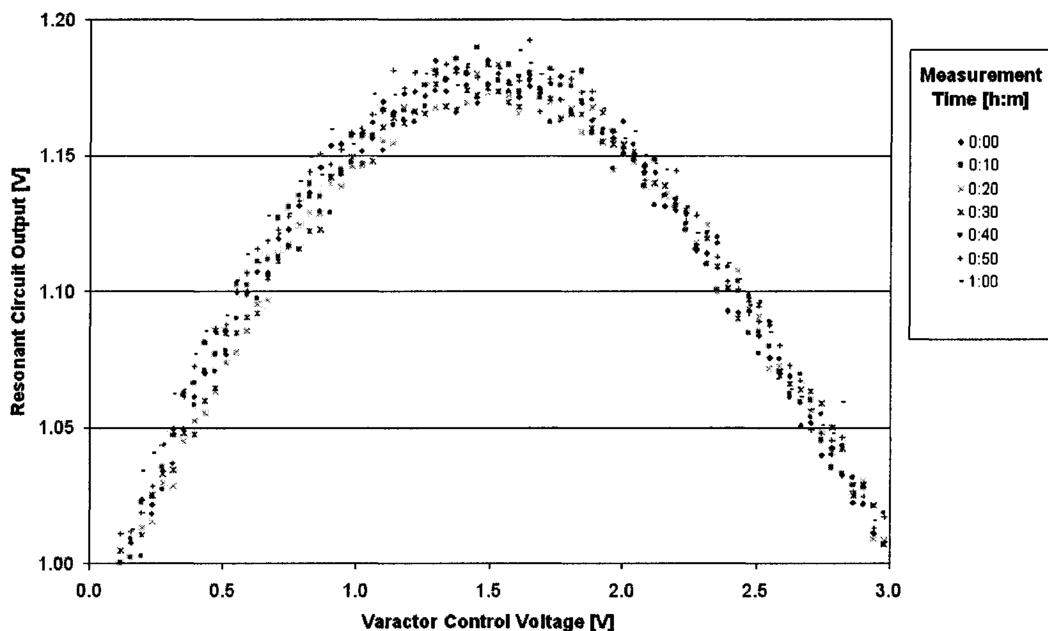


Figure 39 - Raw tuning curves acquired to test time-independence of stray capacitance levels

Testing the second assumption, that parasitic levels remain stable between engaged and contacted probe positions, was done in the following manner: First, the tip was placed in close proximity to the sample surface, but outside of electrical contact. Then, using a software-controlled stepper motor, the probe was lowered in 139 nanometer increments toward the sample. After each approach step, the tuning curve was captured for comparison. This process was repeated until a significant change in the tuning curve shape indicated an electrical connection between tip and surface. Since none of the collected data included the loading effect of the sample on the tuning curve, any observed fluctuations could be entirely attributed to probe height-dependent stray capacitance variation. As demonstrated by figure 40, repeated engage/contact movements did not cause the resonant curve to demonstrate any visible changes. This implies that parasitic levels remain effectively constant over tip-sample separation distances greater than one micron as the analysis of these data, presented in section 4.5.3, confirms.

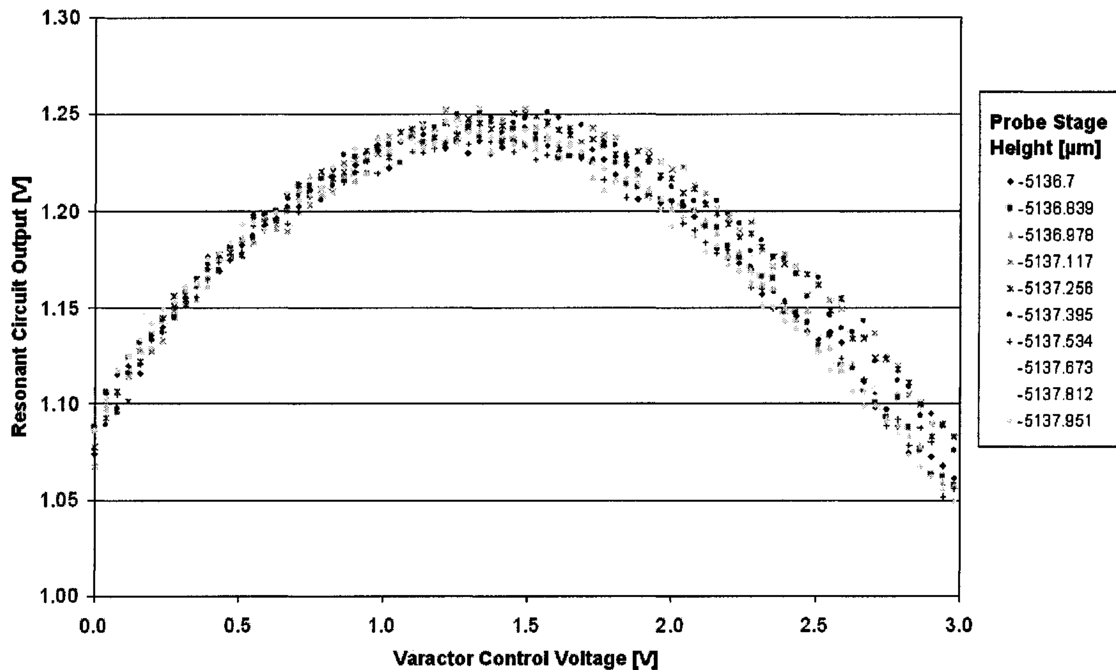


Figure 40 – Raw tuning curves acquired to test dependence of stray capacitance levels on tip-sample separation

4.5. Data evaluation and results

In this section, experimental data is examined with consideration given to the behaviour predicted by theory and simulations. This permits evaluation of each dataset's validity, and ultimately leads to the formulation of conclusions based on appropriately weighted results. Data acquired from integrated (MOS) samples, measured with both probe types, are evaluated in section 4.5.1 in order to conclusively determine the optimal experimental conditions. This is followed by a description of the data analysis algorithms we employed, which served to filter the raw data and extract the tuning curve peak location, our parameter of interest. Presented in section 4.5.3 are the results of experimental work meant to test and validate two fundamental assumptions regarding the behaviour of the system's stray capacitance levels; that parasitics exhibit minimal variation both over time and with changing tip-sample separation. Since this developmental measurement technique was being constantly refined throughout the data collection process, there were understandably some results about which we had legitimate reason for skepticism. For this reason we evaluated the origins of each extracted data point against a series of criteria, so that rather than omitting unreliable data, we could justify our decision to minimize its significance. A calibration curve is then constructed, based on these weighted data points, which characterizes the system's behaviour.

4.5.1. Meta assessment of raw data

During initial trials with platinum-coated sensors, very little stage movement was required to alternate between engaged and contacted probe positions. In subsequent measurements however, achieving reliable tip-sample contact became exceedingly difficult, often producing noisy tuning curves such as the one shown in figure 41. This behaviour was attributed to a rapid degradation of the tip's conductive coating layer due to erosion, manifesting itself as a high-resistance or insulating junction between the probe and sample surface. Based on observations of platinum-coated tips using SEM images captured both before and after measurements, shown in figure 32, this hypothesis was clearly confirmed. Unfortunately, since the platinum-coated probes had such a short useful lifespan and were available only in limited quantities, the data set collected was insufficiently large and far too erratic to permit conclusions to be drawn about the

system's behaviour under load. The results could not confidently be compared with those predicted by simulations, and were ultimately discarded.

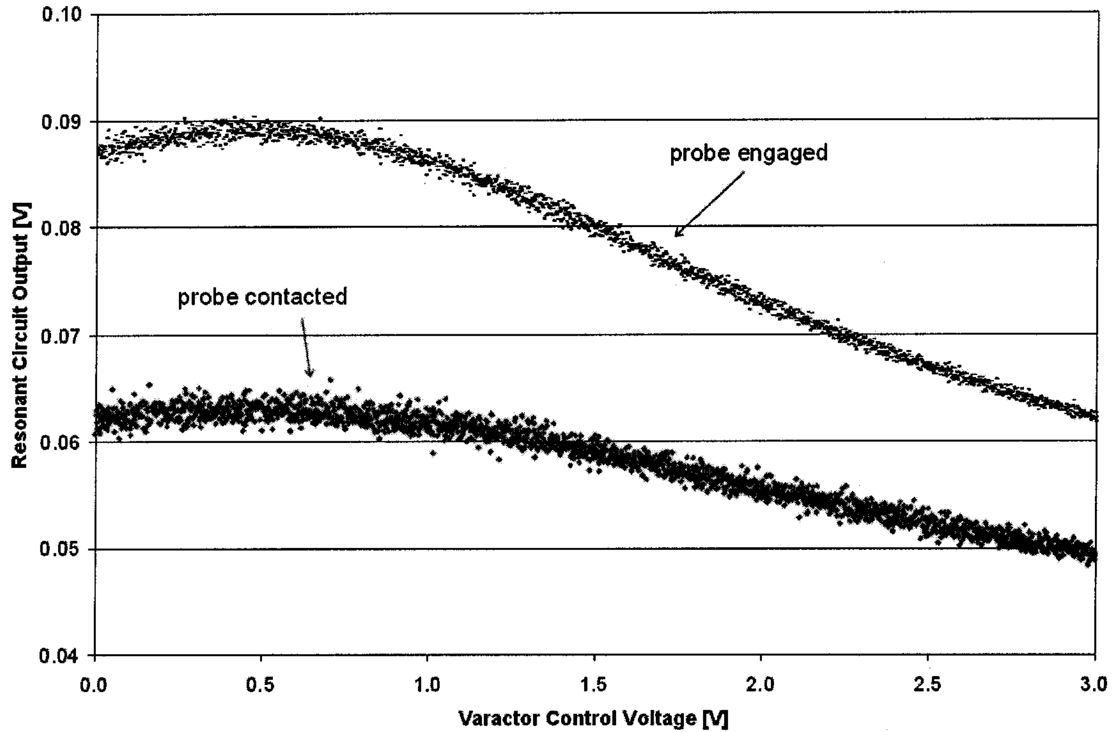


Figure 41 - Typical raw data acquired with Pt-Ir probe

The solid tungsten sensors yielded an extensive and consistent data set, showing a general trend in agreement with the behaviour anticipated based on theory and simulations. Though the software-modeled circuit was an arbitrary design, refinement of parameters such as contact resistance and stray capacitance enabled its behaviour to mimic the experimentally observed results. Using tungsten probes to measure MOS capacitors yielded the most reliable data set, so these results form the basis for all subsequent conclusions. Though tuning curves with atypical shapes seldom appeared, these data were discarded from the set of measured results. Figure 42 illustrates one such omitted curve, plotted next to a measurement acquired immediately afterward, under identical circumstances.

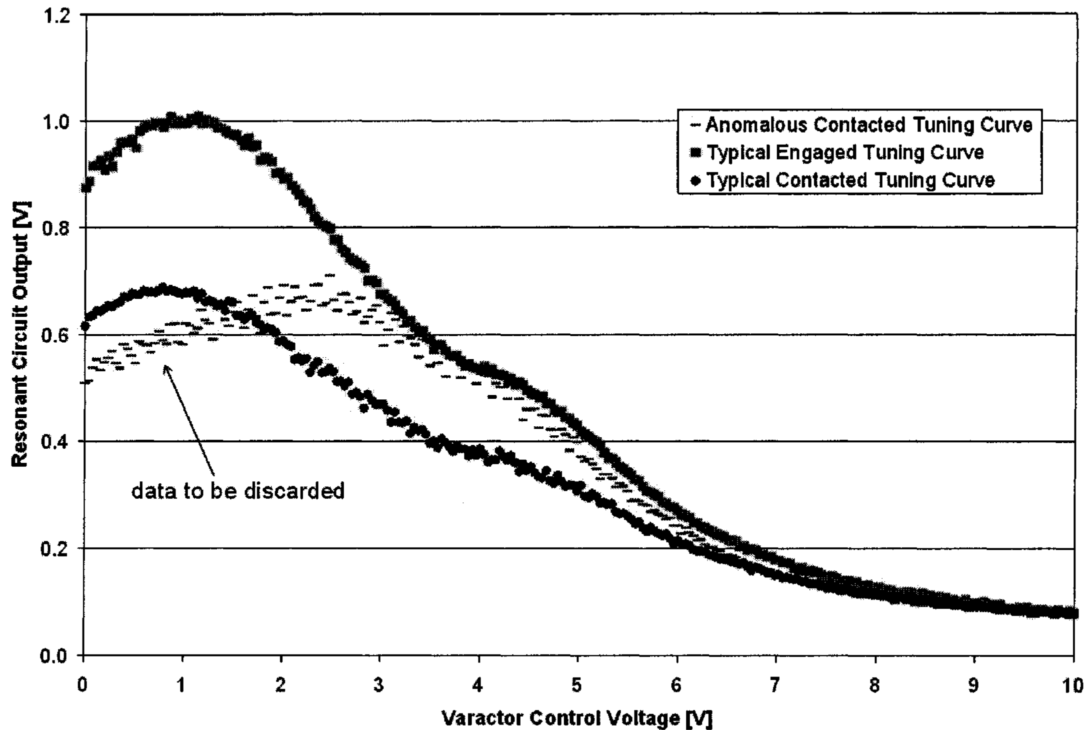


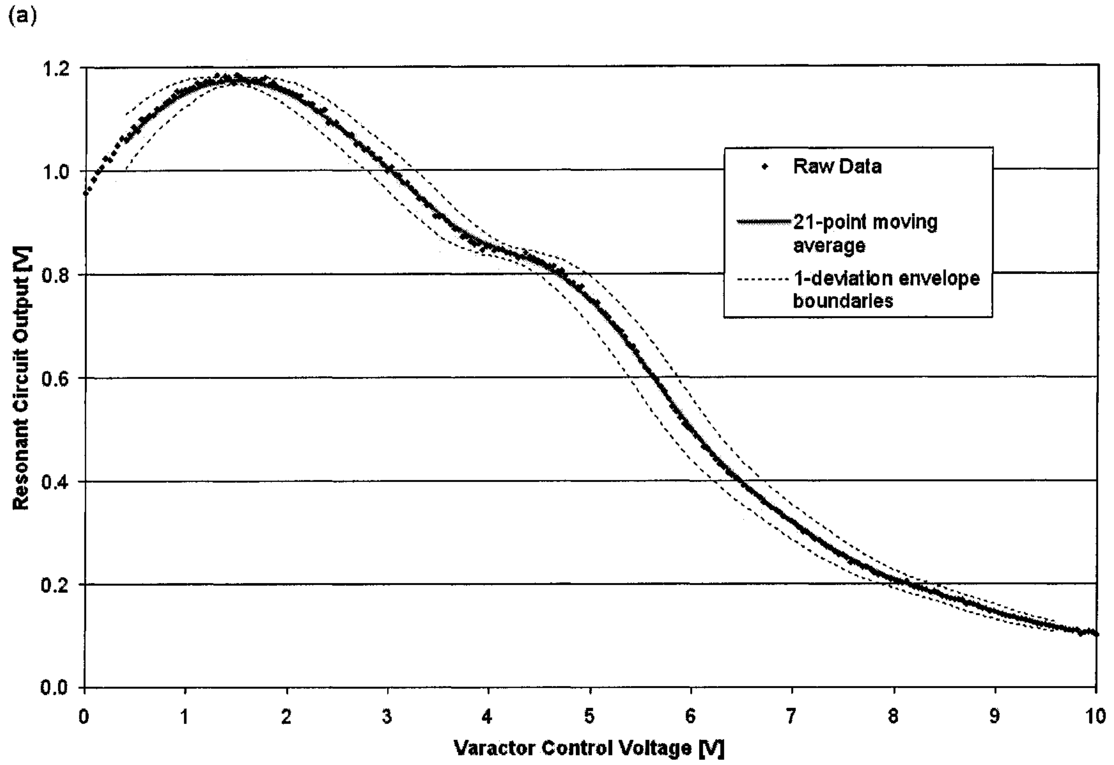
Figure 42 - Illustration of anomalous tuning curve shape

4.5.2. Preliminary analysis of valid data

Tuning curve analysis was performed using a custom application which carried out two principle functions, as illustrated in figure 43. First, each 256-point dataset was averaged using a moving window, to establish the curve's mean shape amid experimental noise. The number of data points enclosed in the averaging window was dictated by each tuning curve's specific amplitude. For example, since data sets produced by large sample capacitances were subjected to the most severe attenuation, they tended to have a lower signal-to-noise ratio and therefore required a larger window in order differentiate the peak from noise. Next, an envelope was applied whereby data points lying more than one standard deviation above or below the local average value were discarded. Having removed all outlying points thus eliminating their influence over the local average, the filtered data was again subjected to moving average analysis. The midpoint of the window whose constituent data points had the highest average value was defined as that particular tuning curve's peak. Note that since the abscissa of a tuning curve represents

the control voltage supplied to a varactor diode, each peak location is specified in units of voltage. The points in figure 43(a) denote raw data comprising a complete tuning curve, while each point on the solid line represents the average resonant circuit output amplitude of the surrounding twenty-one data points, the window size employed in this example. The dashed lines, inserted above and below the average curve, are separated by a distance of two local standard deviations. These represent the envelope within which data must fall to be deemed valid. Figure 43(b) shows the peak region of this same tuning curve in detail, with outlying data points removed. The tuning curve peak is located at the apex of the re-calculated moving average curve. A 21-point window is also included in this panel in order to illustrate scale.

(a)



(b)

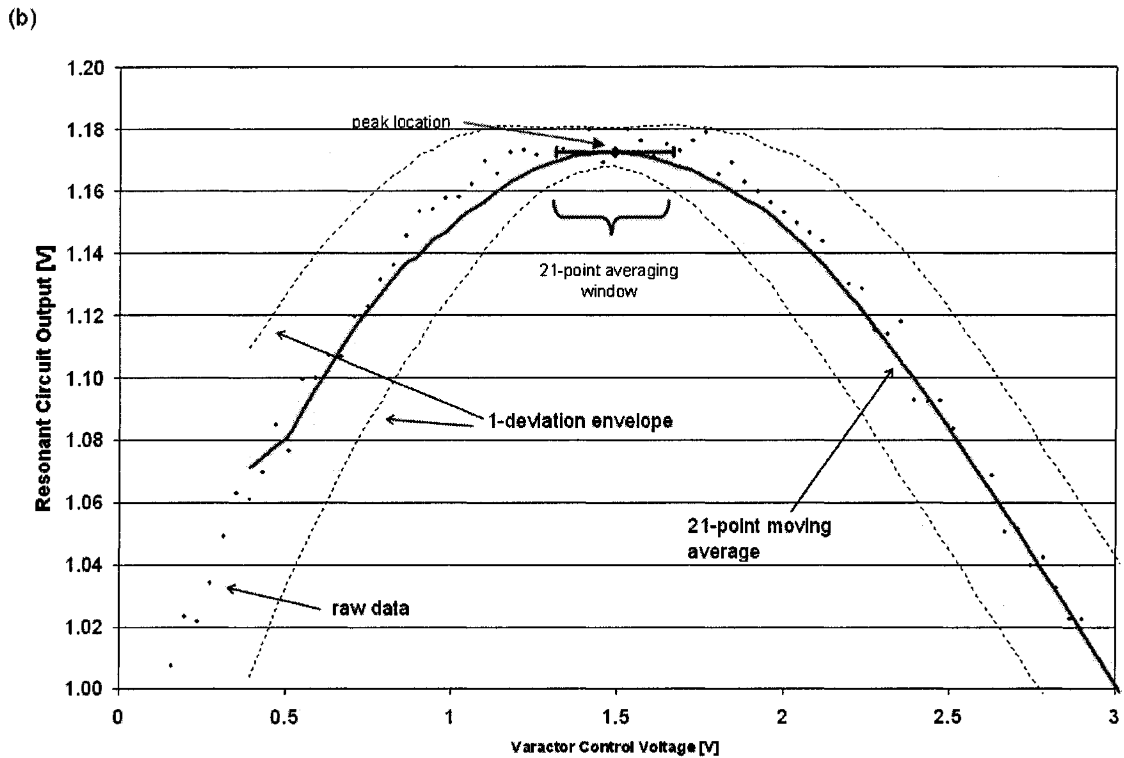


Figure 43 - Graphical representation of the data analysis process in which (a) results are filtered to eliminate noise spikes, and (b) remaining data is analyzed again to determine the peak location.

4.5.3. Stray capacitance determination – the reference

Though discussed in further detail in section 4.5.4, applying the analysis algorithm to a pair of engaged and contacted tuning curves allows the effects of parasitic capacitance to be referenced out. This is to say that each engaged tuning curve becomes the reference level for the subsequent contacted data set, enabling distinction between C_{stray} and C_{DUT}. Clearly, the preceding statement is only valid if we can assume that stray capacitance levels do not vary with variations in tip height or over time. The analysis techniques introduced in section 4.5.2 can now be applied to the experimental data presented in figures 39 and 40 in order to test our assumption. Figure 44 illustrates that the engaged tuning curve peak location does not vary substantially or systematically over time. This relationship was found to apply regardless of whether tungsten or platinum-coated tips were employed, and irrespective of a probe's physical orientation with respect to sample features, though both of these factors can affect the basic tuning curve shape.

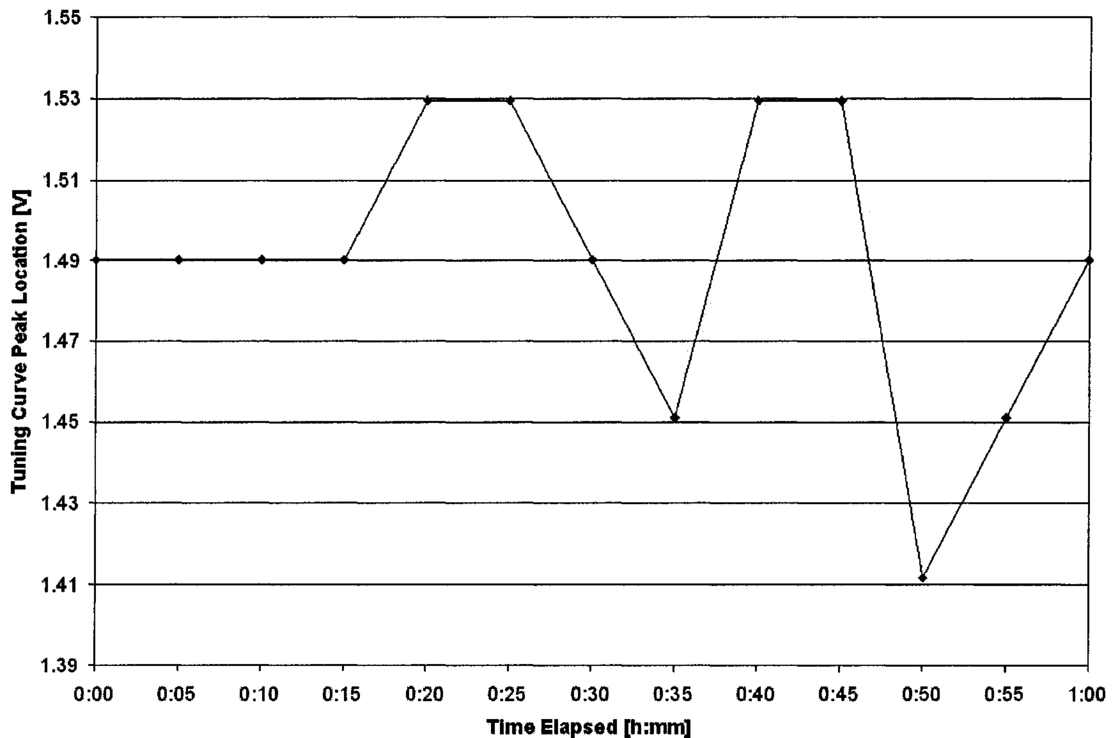


Figure 44 - Time-dependence of engaged tuning curve peak location - tungsten probe

Similarly, figure 45 illustrates how the same quantity varies as a tungsten probe is made to approach the sample surface. The distance scale is presented relative to the upper limit of the probe stage's travel range, but represents 1.25 μm of total displacement. Again, the engaged tuning curve does not appear to be systemically affected by tip-sample proximity within the normal range of probe travel.

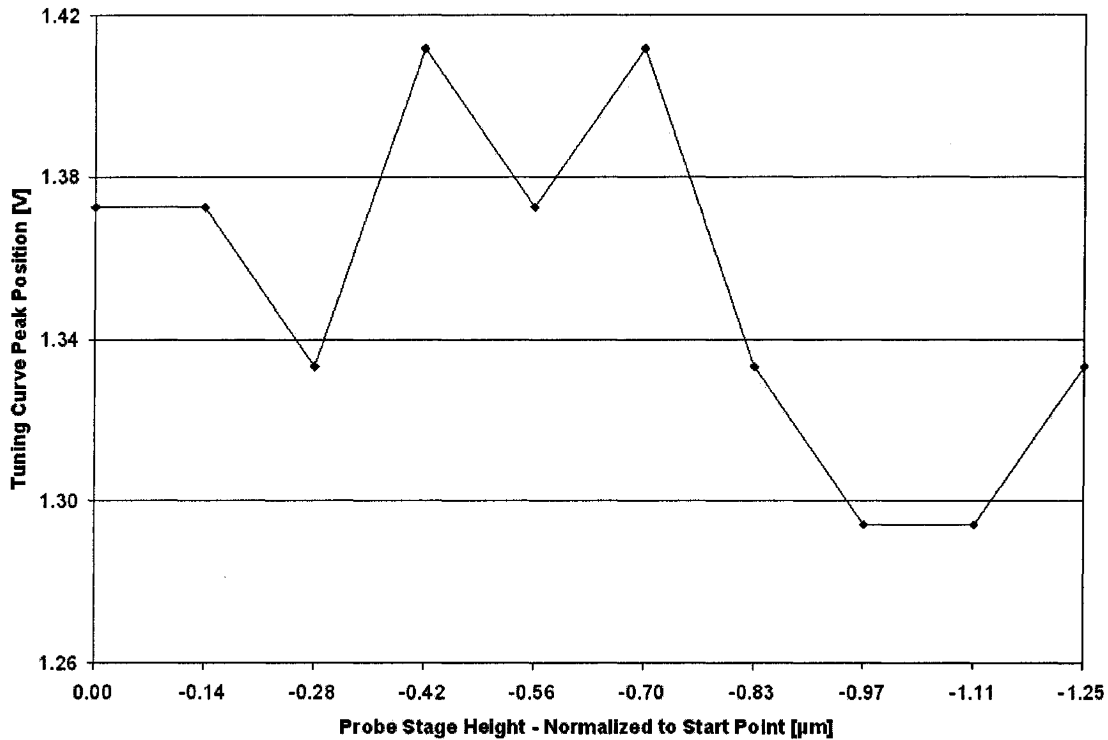


Figure 45 - Height dependence of engaged tuning curve peak location – tungsten probe

4.5.4. Sample capacitance determination – generating the dataset

In the course of experimental measurement, tuning curves are collected in pairs, though each is subjected separately to the algorithms of section 4.5.2. This analysis yields a set of tuning curve peak locations whose relative difference represents the change in varactor diode capacitance required to accommodate the measured DUT. This data set, consisting of 175 points obtained using tungsten probes and presented in figure 46, illustrates the relationship between sample capacitance and peak shifting.

The resolution at which each tuning curve is acquired, and consequently the window size used in performing analysis, is a vital factor in determining the data points presented in figure 46. Therefore, it is important to quantify the uncertainty that our peak

finding algorithm introduces to each measured value of tuning curve peak shift. For example, when 256 points of data are collected over a four volt span of varactor diode control voltage, each represents an increment of nearly 16 millivolts. Therefore a sampling window containing twenty-one data points will cover 328 mV, or 8.2 percent of the complete tuning curve.

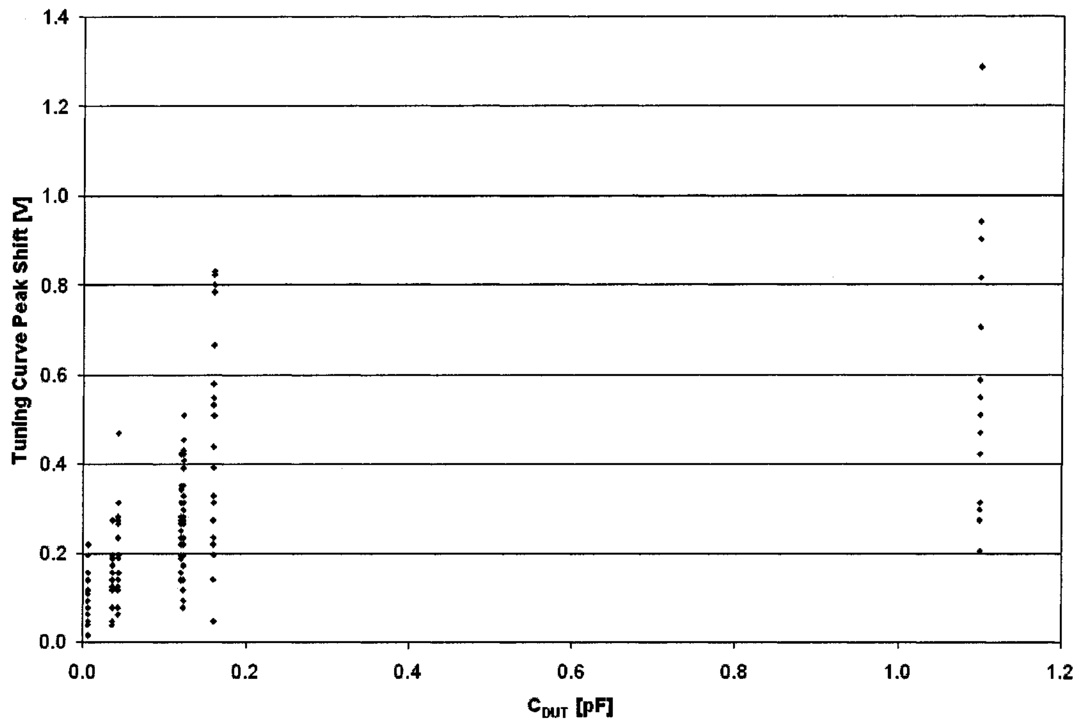


Figure 46 - All experimental data obtained from measuring MOS capacitors with tungsten probes.

For engaged tuning curves of the shape typically observed in this work, such a window covers a sufficient percentage to smooth out noise spikes, but not so much that the peak location becomes washed out by surrounding data. Contacted tuning curves are quite different however, since their shape changes drastically depending on the size of device being measured. As C_{DUT} becomes larger, contact resistance at the tip-sample junction causes increasingly severe broadening and attenuation of the tuning curve, and the signal-to-noise ratio is consequently reduced. Performing peak detection on noisier curves such as these requires an enlarged averaging window, which reduces the impact of noise, but also leads to an increased margin of error in peak position determination. That the

precision with which the peak can be located is directly related to the averaging window's size accounts for the largest capacitors having the most widely spread data points in figure 46. The wide deviation in peak shift measurements for each value of C_{DUT} make it difficult to confidently formulate the desired relationship, through which peak shifting can be used to indicate sample capacitance. As the following section will explain, factors such as probe wear and experimental inexperience could potentially lead to unreliable data. As a result, each datum is assigned a weighting based on the circumstances under which it was obtained. A probe-specific calibration curve can then be constructed by plotting the weighted average peak shift against the known sample capacitance, which in turn can be used to deduce the capacitance of unknown samples based on observed tuning curve peak shifts.

4.5.5. The calibration curve – reducing the dataset

From the complete data set presented in figure 46, we would like to better quantify the relationship between the amount of tuning curve peak shifting and the DUT capacitance being measured, since the spread of data indicates uncertainty in our peak position measurements. In doing so, it is important to account for experimental factors such as tip wear, which render some data points less reliable than others. Therefore, each experimental data point is assigned two weightings, and the weighted average shift is then calculated for each value of C_{DUT}.

The first weighting score is derived based on a subjective evaluation of the raw tuning curves from which peak shift values are determined. Figure 47 illustrates the difference occasionally seen in tuning curves despite having used a common probe to measure the same device. The noise present in the upper curve contributes to uncertainty when employing the peak-finding algorithm, and so its corresponding data point is weighted lower, ensuring its contribution to the average peak shift calculated for this DUT will be less that of smoother tuning curves.

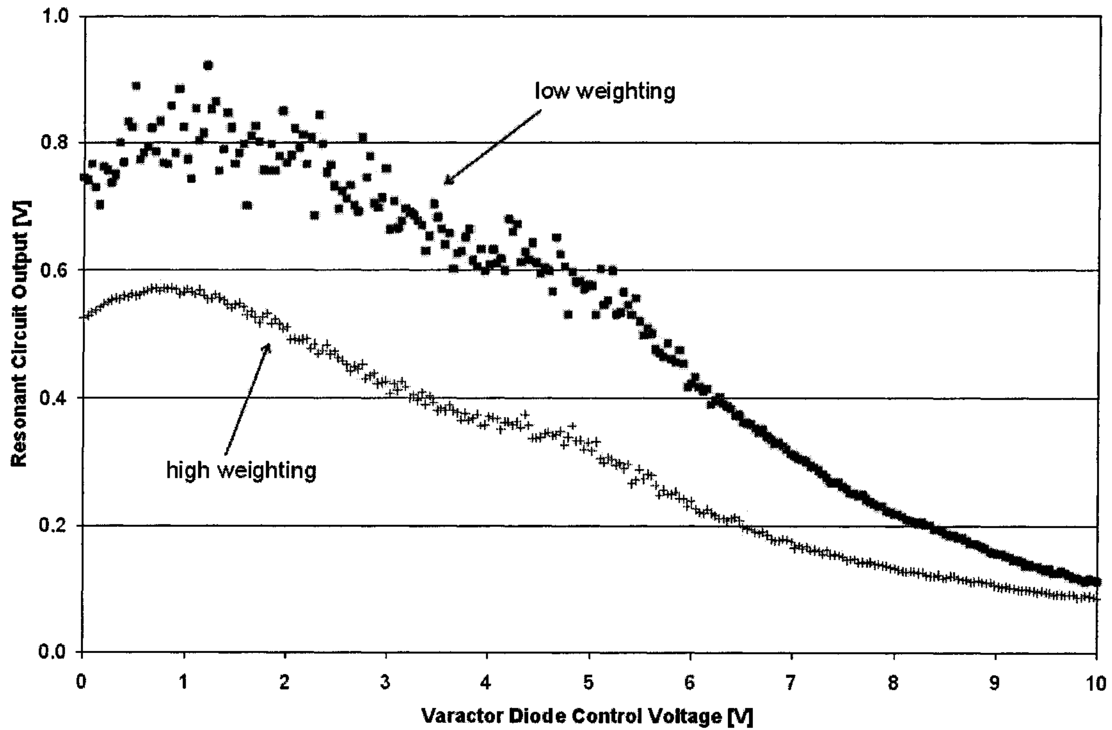


Figure 47 – Assignment of weightings to account for variation in tuning curve shapes

The second weighting factor is based on the useable lifetime of a probe, which has been estimated based on experimental results to span approximately sixty data points. Since the tip deteriorates with each measurement performed, a particular data point's weighting will depend on the probe's stage of life at the time it was acquired. Said another way, measurements with a new probe are considered more reliable than those performed with a probe used many times previously, hence data points are weighted accordingly. A calibration curve incorporating the effects both of these weighting factors is presented as figure 48. The trend line shown in this figure confirms that the probe-sample junction is affected by contact resistance, since the non-linear shape of this data set matches results predicted by simulations.

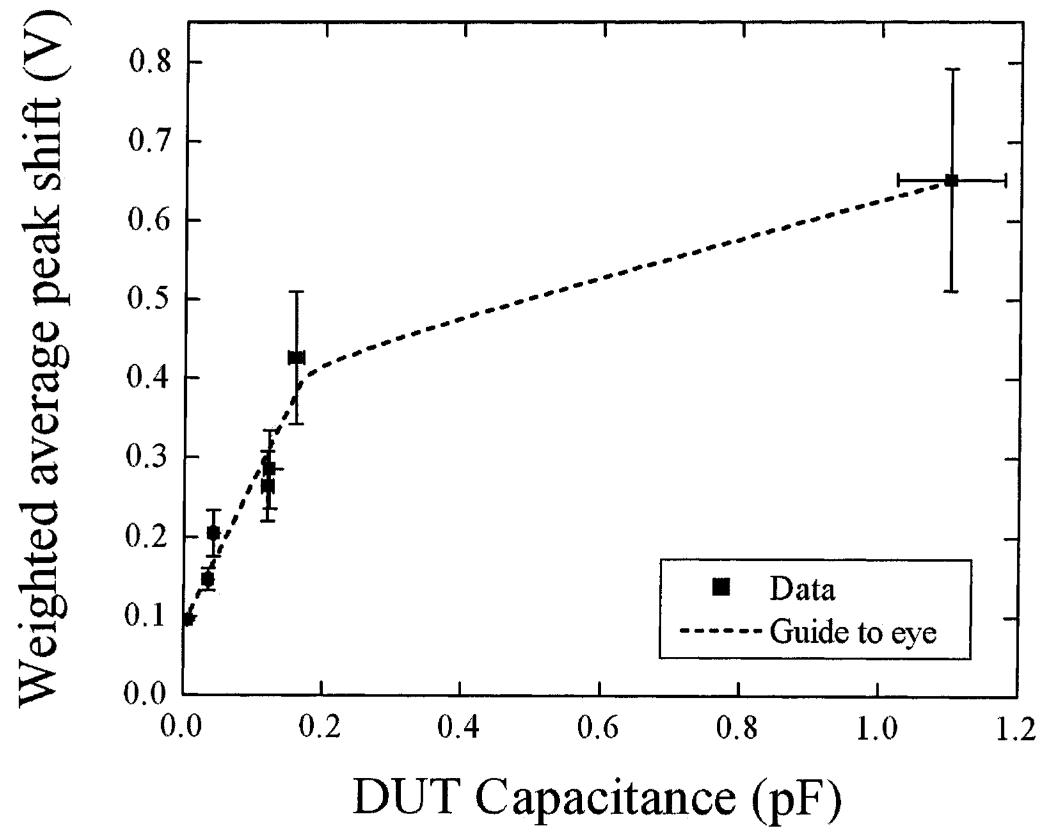


Figure 48 - Calibration curve for system using tungsten probes, constructed using experimental results.

If we disregard the 1.1 pF datum, all remaining points can be grouped to form the curve's linear region, in which contact resistance has a negligible influence. The results are shown in figure 49, along with a linear trend line whose non-zero y-intercept indicates a low level of remaining parasitic capacitance. While section 4.6 will address the origins of these error bars in more detail, the wide peak shift uncertainty for large capacitive samples is primarily due to contact resistance, which causes tuning curve attenuation and broadening. These effects, which become more pronounced as C_{DUT} increases, lead to declining accuracy in the peak finding algorithm.

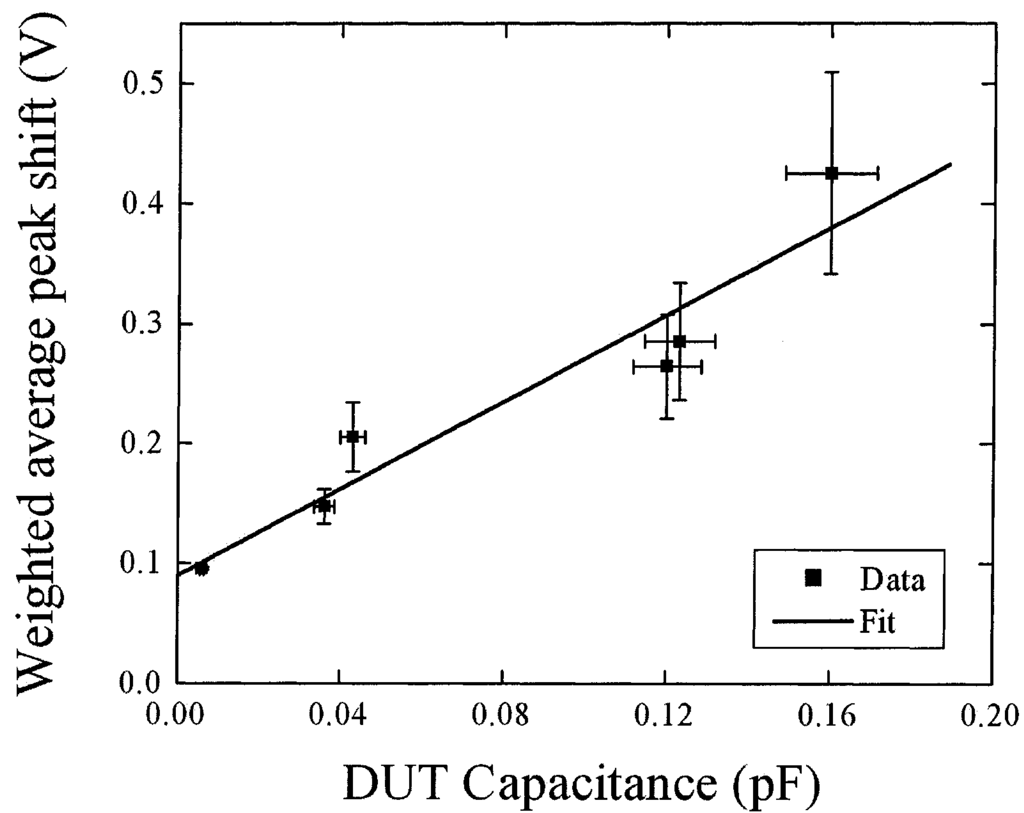


Figure 49 - Linear region of calibration curve constructed using weighted averaged data

4.6. Discussion

Having presented the results, in this section we give a more quantitative assessment and discussion of the data set obtained with tungsten tips on MOS capacitors. Included is a summary of all factors that might contribute to inaccuracies in these results, followed by an estimate of the measured data's overall precision.

4.6.1. Factors affecting data accuracy

Several factors, to varying degrees, influence the accuracy of experimental results. Each of these must be examined to determine their individual consequences and to evaluate the subsequent effect on overall data precision.

One potential source of error involves the physical degradation of probe tips over the course of repeated experimental trials. While this effect was certainly more pronounced when using platinum-coated probes, to the point that electrical contact sometimes became impossible to achieve, tungsten tips were also eventually seen to erode and deform due to overuse. SEM images illustrated that in both cases the tip-sample contact region tended to expand as a probe deteriorated, spawning potential contact resistance instabilities. Furthermore, the apices of warped tungsten tips were often difficult to locate with the instrument's integrated optical camera, introducing the possibility that bent tungsten probes might have contacted unintended portions of the sample surface.

Also of concern is the repeatability of the probe's engaged and contacted positions relative to the sample. Typically in contact mode imaging, an SPM sensor is lowered toward a surface until repulsive Van der Waals forces provoke a predetermined level of cantilever deflection as measured by the reflected laser. Our procedure dictates that from this position, the probe be manually lowered further by means of a stepper motor until it physically contacts the sample surface. Variations in Van der Waals forces, over time or due to relative tip-sample orientation, will manifest themselves as deviations in tip-sample separation distances, possibly leading to tuning curve inconsistencies over several trials.

An additional variable with potential influence over the accuracy of experimental data is the state of the dielectric layer within each capacitor. It has been reported [21] that factors such as the application of excessive bias voltage can cause insulators to fail

catastrophically, leaving a current leakage path which effectively short circuits the electrodes through the dielectric. The difficulty is not limited to recognizing a blown capacitor, since probing such a non-capacitive device would result in no visible tuning curve shift. Instead, the main potential for error arises when structures containing partially degraded dielectric material are tested, since their capacitances may not necessarily agree with calculated values. This scenario has possible repercussions when constructing system calibration curves, since peak shifts would be plotted against uncertain sample capacitances.

It is also important to consider the resolution specified for data acquisition, in conjunction with the algorithm employed for peak-finding. Since the tuning curve peak location is the primary quantity of interest in this work, the ability to locate it accurately amid measurement noise is critical. With an increased number of data points comprising a tuning curve, the size of the moving averaging window one must use to analyze will expand accordingly. In choosing a window size, one must balance the need to consider a sufficiently large number of data points to negate erroneous noise spikes, against the risk that averaging too many data at once will obscure the true tuning curve peak location. One's choice of window size should also depend on the shape of the curve being analyzed, since very broad, attenuated peak regions such as those generated by larger capacitors require a larger window. However the window size in turn influences the peak-finding algorithm's accuracy, explaining why the spread of data is so wide for larger samples.

4.6.2. Quantifying dataset variance

To understand the impact on measurement precision due to each factor listed above, it is important in each case to evaluate both the potential for error and the magnitude of the subsequent uncertainty. In some cases it is possible to conduct experiments which allow these quantities to be measured, but the potential impact of other factors can only be estimated.

For example, the extent of a probe's degradation can be monitored by comparing the amplitudes of tuning curves generated by both new and used tips. As contact resistance increases, simulations predict that these curves will become broadened and attenuated, hence the peak amplitude should give a good indication of whether or not a

probe should be replaced. Quantifying the impact of a worn tip on peak position is difficult however, since measurements were not repeated continuously on the same sample with the same probe. Instead, the approach taken in this work was to begin measuring a different target capacitor with each new probe, in the hope that every sample's data set would include measurements taken with tips in various stages of deterioration. Furthermore, data were assigned weightings based on the portion of probe life cycle in which they were acquired. The first thirty pairs of measurements made with a given probe were given full weight, while the subsequent twenty trials were weighted at 80%. When further data was acquired beyond any probe's fiftieth measurement, they were assigned to have half the weight of a datum obtained using a new tip.

Similarly, the impact of variations in tip-sample separation distance must be estimated rather than quantified experimentally. By recording the z-position of the probe stage prior to each measurement, one finds that although the absolute tip engage height varies from trial to trial, the difference between any pair of engaged and contacted positions remains nearly constant. It is most likely therefore that gradual variations in the sample surface are the cause of observed differences in engaged tip position, but that nearly constant levels of Van der Waals forces are present at all times and in all locations. While there is clearly some non-repeatability in the behaviour of the measurement apparatus, this factor likely has a negligible effect on the accuracy of observed results.

As dielectric material within a capacitor degrades, the device's behaviour begins to change. Only when the damage extends through the entire structure do its electrodes become short-circuited however, at which point the component no longer acts like a capacitor. The one instance in which this catastrophic failure occurred was easily identified, and an alternate sample was substituted immediately. It is presumed therefore that oxide degradation will not contribute significantly to measurement error except in the rare and easily-detectable case of punch-through.

Summarized in table 2, the vertical bars shown in figures 48 and 49 are based on the weighted standard deviations of the data discussed above. These deviations are consistent with the mean tuning curve uncertainties divided by the square root of the number of sample averages, as statistical theory would have us expect. Horizontal error

bars were determined based on physical measurement errors arising during calculation of each capacitor's dimensions.

Table 2 - Estimated error in peak shift magnitude for different values of C_{DUT}

Capacitance of Device Under Test [pF]	Window Size for Peak-Finding Analysis [V]	Experimentally Determined Peak Shift [V]	Estimated Error in Peak Shift Determination [V]
0.006	0.796	0.096	±0.029
0.036	0.796	0.147	±0.033
0.043	0.796	0.205	±0.054
0.12	1.194	0.264	±0.038
0.123	1.194	0.286	±0.049
0.16	1.194	0.426	±0.118
1.1	1.990	0.652	±0.151

4.6.3. Comparison with simulated behaviour – parameter representation

The circuit model developed in chapter 3 included three parameters, R, L, and C_{tune}, for which component values were chosen. Using experimental data, it is now possible to refine the model to better replicate our physical system. For example, the fact that a line fitted to our constructed calibration curve (excluding the 1.1 pF point) has a non-zero y-intercept suggests the presence of a constant level of parasitic capacitance for which our method was unable to account. If approximately 0.09 V is subtracted from each point of the experimentally-derived calibration curve, the data set can now be made to correspond to a particular curve constructed from simulations. Since the slope of a simulated curve's linear region is dictated by the chosen value of inductance, the model can be adjusted so that it too produces a calibration curve having such a slope. Finally, the 1.1 pF data point lies outside the linear region, so it can be used to determine the level of contact resistance present in the experimental system. Figure 50 shows the experimental and simulated calibration curves plotted on a common set of axes, with the observed peak shifts having been re-scaled to coincide with the capacitor tuning range specified for the software model.

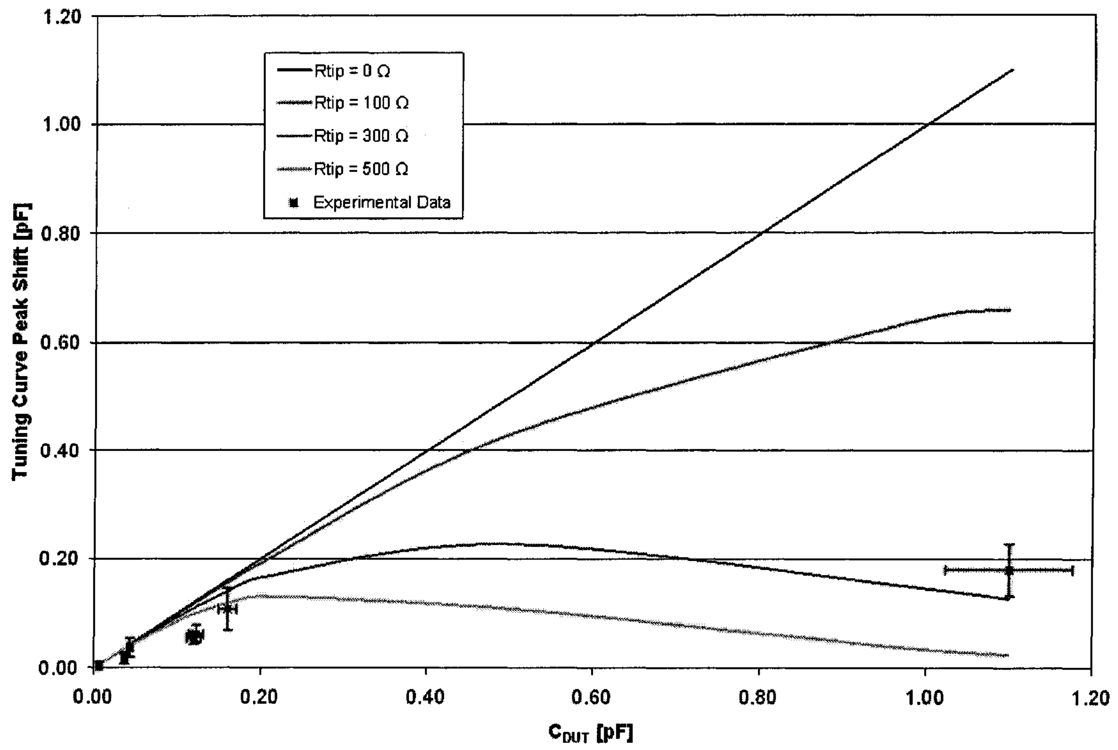


Figure 50 - Comparison of system's experimental behaviour to calibration curves predicted by simulations.

5. Conclusions

This thesis has presented a novel technique by which quantitative capacitance measurements can be performed on integrated MOS structures using an atomic force microscope and SCM module. Results obtained from examination of seven MOS capacitors compared favourably with expected behaviour, based on both theoretical analysis and software simulations. Limitations of the method's feasibility were demonstrated, and recommendations for expanding its usefulness were presented.

5.1. Summary

Presented here is an innovative technique by which particular features of a well-established semiconductor characterization tool are leveraged to enable additional measurement capabilities. In this case, an AFM system with scanning capacitance microscopy functionality has been made to operate as a precision electrical probing system able to measure minute capacitances and thereby determine dielectric permittivities. This is accomplished by exploiting the ultra-precise sensor positioning mechanism and the extremely sensitive resonant circuit-based capacitance detector, both integral to traditional scanning capacitance microscopy but manipulated within a novel framework to yield previously inaccessible results.

The proposed method appeared to be an effective way to measure MOS structures with calculated capacitances ranging from six to 160 femtoFarads. The system's resonant circuit detection mechanism quantified changes in DUT capacitance by proportionately scaling the amount by which its resonant peak shifted. Measured data demonstrated a linear relationship between sample capacitance and peak shifting, and suggested an improved parameterization by which the system's behaviour might be represented and modeled.

It was expected that this quantitative capacitance measurement method would initially be useful only for probing large MOS capacitors on the order of one picoFarad, but that improvements to the stray capacitance detection routine and optimized peak-locating algorithms would subsequently enable implementation on smaller scale devices. However it quickly became apparent both that the system was far more sensitive than expected, and that elimination of stray capacitance effects would not be trivial.

Though a systematic error in the experimental calibration curve revealed our measurement technique's inability to entirely reference out stray capacitance in the system, remaining parasitics represented only a small percentage of their initial levels. Not only were these exceptionally promising results for a first attempt, but if the capacitance for which our method did not account is assumed to be constant for all samples, it can easily be removed during post-experimental analysis.

One factor limiting this method's usefulness was the contact resistance present at the probe-sample junction. This undesired loading caused attenuation and broadening of

tuning curves, particularly when measuring large capacitive loads. As a result, the relationship between resonant frequency shifting and sample capacitance becomes nonlinear in the regime of high C_{DUT}. The beneficial aspect of this behaviour is that for contact resistances on the order of those seen in this work, the calibration curve non-linearity is negligible if $C_{DUT} < 0.2$ pF. Therefore, by collecting a sufficient number of data points, a fit line can be constructed which accurately portrays the system's true behaviour. In any case, if further investigation determines the observed contact resistance to be a quantity that remains constant both from tip to tip and throughout a particular probe's lifetime, a functional calibration curve can still be constructed and employed to allow measurements of larger samples.

A second factor limits this method's applicability to measure large sample capacitances, namely the level of stray capacitance present in the system. While prior publications [18], [22] suggested that stray capacitances associated with metal-coated probes could be expected to range between 0.1 and 0.5 pF, this parameter has been shown to be highly dependent on the geometry and composition of the SPM tip being employed. Clearly the solid tungsten probes, despite ensuring reliable conductivity, exerted a much larger parasitic influence on the resonant circuit than the conductively-coated silicon sensors cited in [18], [22]. This effectively shifts the instrument's tuning curve peak toward substantially lower frequencies before the sample load is even applied to the detection circuit. Since the observation frequency is fixed at a predetermined value and the tank circuit's built-in trimming capacitor can only vary its natural resonance frequency over a limited range, the stray capacitance level dictates how much of the varactor diode's tuning range will remain to accommodate DUT-triggered tuning curve shifts. Stray capacitance represents an experimental constraint on this technique, since it determines the upper bound for sample capacitances. If measurements are restricted to devices having capacitances within the linear region of the system's calibration curve however, this upper threshold should not be a factor.

Despite the limitation imposed by contact resistance, which restricts the accuracy to which large capacitances may be measured, the technique has been demonstrated to be capable of measuring MOS capacitances as large as 0.2 pF to within a probable error range of $\pm$ 15%. Since the predominant source of error results from the analysis rather

than the acquisition of data, refined peak-finding algorithms have the potential to greatly reduce this uncertainty. More rigorous control over tip wear to ensure repeatable contact quality is a further easily implemented measure that could significantly improve the system's accuracy.

5.2. Future work

The results of this initial study clearly indicate the technique's feasibility as a method for quantitatively measuring small MOS capacitors. The method yields results whose behaviour agrees with that predicted by both circuit theory and simulations.

Compared to measurements taken using an LCR meter and a standard probe station, the technique demonstrated here is more time consuming, since multiple measurements are required to ensure accurate results. With the appropriate refinements however, the potential exists for this method to quantify much smaller capacitances than would be possible by using other procedures. Given the trend toward progressively smaller features incorporating non-traditional insulators, a system employing AFM for probe positioning, a well-understood and meticulously calibrated resonant circuit for capacitance detection, and a procedural technique for negating parasitic contributions without the need for shielding certainly warrants further investigation.

With the goal of improving the precision of results obtained using this technique, several avenues are worthy of supplementary exploration. Key among these is the development and implementation of an algorithm capable of reliably and accurately locating a tuning curve's peak position in terms of applied varactor diode voltage, so that the number of independent measurements may be reduced. Improving this aspect of the technique becomes particularly critical as the method is applied to increasingly small capacitances, since absolute peak shifts will shrink and uncertainty will represent an increasingly significant percentage. Luckily, tuning curves associated with such small capacitances are typically well-shaped, since they are not heavily affected by contact resistance.

Rudimentary work to this point includes a technique for determining the midpoint of an arbitrary bandwidth, and a recursive routine designed to find the mean and standard deviation of a Gaussian curve to which the data best fits. Both of these techniques are based on the flawed assumption that the curve being examined is symmetric about its peak, inevitably leading to inaccuracies. The most reliable technique so far has been a moving window-based averaging routine combined with envelope-based filtering, but even this could potentially be improved by optimizing the window size to best suit each individual data set under consideration.

Another strategy to improve this measurement technique is to determine the source of tip-sample resistance, and take steps to reduce it. Though the associated non-linearities are not prominent on the scale of small MOS capacitors, abolishing contact resistance would eliminate calibration curve ambiguities for larger capacitive loads. Junctions at which current flow may be impeded include not only the tip-sample interface, but also the connection between the sample back plane and mounting stub, and where the stub contacts the microscope chuck. Internal interfaces such as those between contact plugs and the polysilicon top capacitor plate, and where the bottom plate meets the substrate are also potential resistive junctions, so thorough continuity probing would be required to reveal the source of this undesired series resistance.

It must be noted however that improving the system's series resistance alone will be not allow the instrument to measure larger capacitances. Since the observation frequency, based on which the tuning curve is constructed, is internally fixed at 915 MHz, the position of the engaged tuning curve, along with the peak detection algorithm, dictates the system's largest observable peak shift. While it might make theoretical sense to force the resonance toward higher frequencies by adding an inductive element, perhaps between the tip and the internal tank circuit, the order of the required inductor would be impractically small. Another option might be to effectively shield the tip from the chuck by means of an insulating cover, though the tip-chuck interaction is arguably insignificant at the distances in question when compared to tip-sample and tip-stub effects.

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