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**A 20 GHz FET AMPLIFIER
USING A COMBINATION OF FINLINE AND MICROSTRIP**

by

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A thesis presented to the
University of Ottawa
in partial fulfillment of the requirements
for the degree of
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Ottawa - Carleton Institute for Electrical Engineering
Department of Electrical Engineering
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UNIVERSITÉ D'OTTAWA
UNIVERSITY OF OTTAWA

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ABSTRACT

With the use of three terminal devices being extended into the millimeter wave range, new configurations for mounting these devices become necessary. This thesis describes a 20 GHz GaAs FET amplifier which uses a combination of finline and microstrip. A new transition which has been developed to integrate these two forms of transmission lines is described. Also described in this thesis is a transverse resonance program which has been used to calculate the effective dielectric constant, characteristic impedance and cutoff frequency of a finline with narrow gaps and finite metallization thickness.

CHAPTER I

INTRODUCTION

Field effect transistors (FETs) and more recently high electron mobility transistors (HEMTs) are being used in the design of low noise amplifiers in the 26.5 to 40 GHz frequency range [1], [2], [3]. In addition, an all FET receiver at 30 GHz [4] and a 60 GHz FET amplifier [5] have been reported. This signals the movement of three terminal active devices into the millimeter-wave frequency range, a region of the frequency spectrum previously dominated by two terminal devices.

In this thesis the design of a 20 GHz FET amplifier using a combination of finline and microstrip is described. Finline is a very attractive transmission line medium at millimeter-wave frequencies for many reasons. It exhibits lower dispersion and less losses than microstrip within this frequency range. Due to its inherent shielding, radiation losses are minimized. The tapered transitions from the finline to waveguide are easily realized by photolithographic techniques and provide a good return loss over a relatively large bandwidth.

Although this amplifier was designed at 20 GHz due to the availability of test equipment and devices, its design could be scaled to millimeter-wave frequencies where the true benefits of its design would become more apparent.

For the design of this amplifier scattering parameters for the transistor used (NEC NE67300) were available from the manufacturer up to 18 GHz. Since it was desirable to predict its performance above this frequency a device model was developed. This model is described in Chapter 2.

In Chapter 3 the design process which was used in the design of this amplifier is discussed. This involved designing an amplifier which was unconditionally stable, had a reasonable bandwidth and provided about 6 dB of gain at 20 GHz.

Chapter 4 describes how the amplifier which was designed in Chapter 3 was realized using a finline microstrip combination of circuitry. This chapter also describes the design of the tapers, finline to microstrip transition and FET mounting structure.

Chapter 5 presents the measured results of the amplifier described in Chapter 4.

Chapter 6 describes a transverse resonance program which was developed in order to investigate the properties of finlines with narrow gapwidths. This was required in order to evaluate the parameters (effective dielectric constant, characteristic impedance, and cutoff frequency) of a low impedance finline section in the transition section of the amplifier.

Chapter 7 presents the conclusions of this thesis.

The appendix contains a listing of the program described in Chapter 6 as well as the drawings used to make the split block housing which held the amplifier circuit.

In summary, this thesis describes the following original contributions:

- 1.) Broadband, low loss microstrip - to - finline transition.
- 2.) Fast and accurate finline design program which accounts for finite metallization thickness.
- 3.) Technology improvement : plated through holes which simplify mounting and performance of finline circuits.
- 4.) Configuration which allows an amplifier to be mounted in either a finline or waveguide environment.
- 5.) Novel biasing network which provides an overall unconditionally stable amplifier

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1. J. Rosenberg, P. Chye, C. Huang and G. Polickey, "A 26.5 to 40 GHz FET Amplifier," *1982 IEEE MTT-S Digest*, pp. 166-168.
2. E.T. Watkins, J.M. Schellenberg, H. Yamashaki, "A 30 GHz Low Noise FET Amplifier," *1985 IEEE MTT-S Digest*, pp. 321-323
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CHAPTER II

TRANSISTOR MODEL

The manufacturer of the transistor used in the design of the amplifier described in this thesis (NEC NE67300) supplies S-parameters for the frequency range 2-18 GHz. For investigating properties of the FET above 18 GHz, a device model was developed. This model was used to predict S-parameters up to 30 GHz. It was formulated based on the values of the measured S-parameters supplied by the manufacturer.

The optimization capabilities of a microwave CAD program, Super-Compact [1], were utilized to derive the component values in the model. By using an FET model existing in the Super-Compact library, the component values were chosen in such a way that the computed S-parameters of the model matched the manufacturer supplied S-parameters from 2-18 GHz. The model of the FET used by Super-Compact is shown in Figure 2-1. Initial predictions for the components shown in Figure 2-1 were taken from a typical FET model described by R. Pengelly [2].

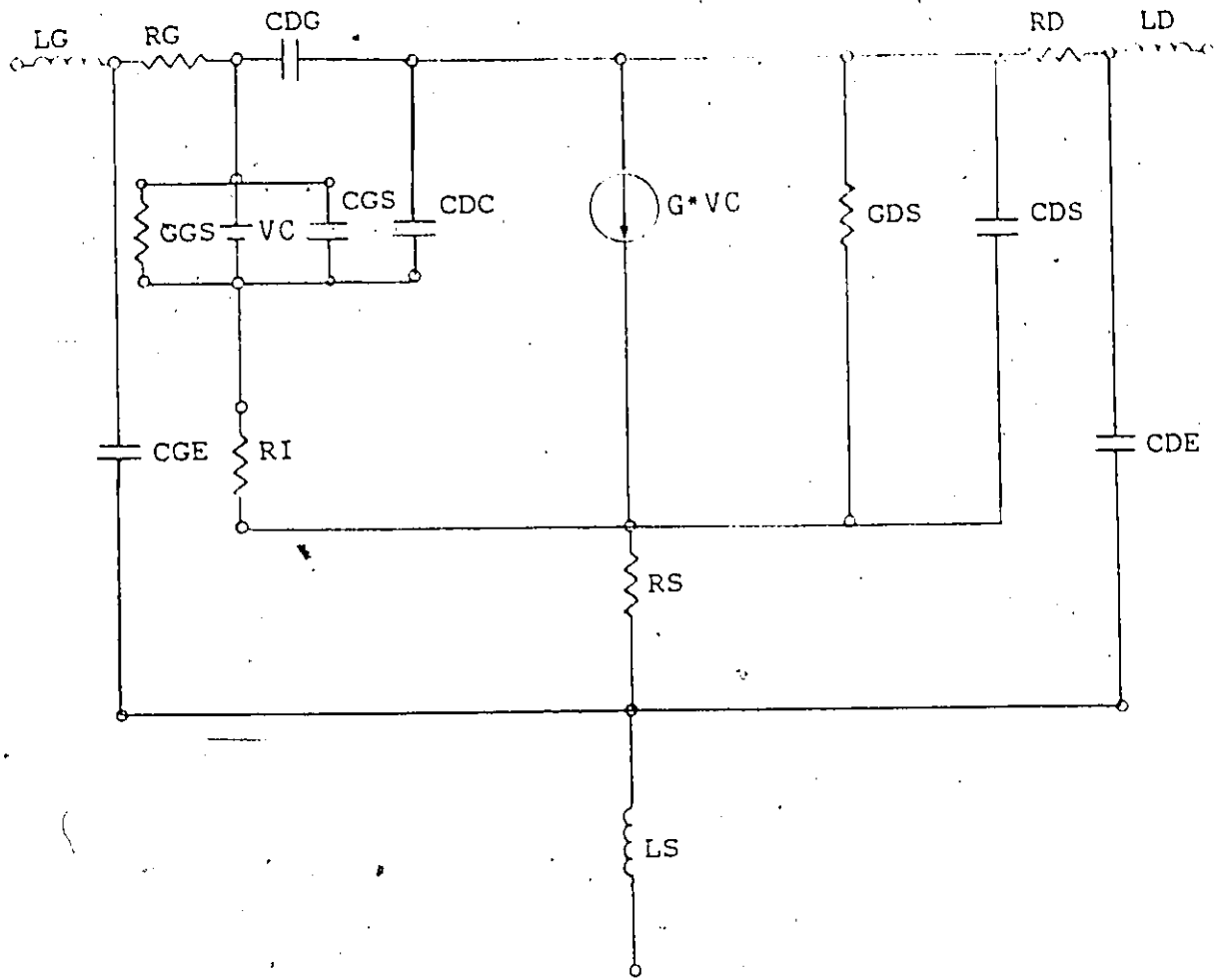


Figure 2-1 FET Model

Table 2-1
Component Values in Device Model

G	TRANSCONDUCTANCE	.07
CGS	GATE-SOURCE CAPACITANCE	.32 pF
GGS	GATE-SOURCE CONDUCTANCE	991X10-6
CDG	DRAIN-GATE CAPACITANCE	.03 pF
CDC	DIPOLE LAYER CAPACITANCE	.03 pF
CDS	DRAIN-SOURCE CAPACITANCE	.03 PF
GDS	DRAIN-SOURCE CONDUCTANCE	6.9X10-3
RI	CHANNEL RESISTANCE	10.3 Ohm
RG	GATE RESISTANCE	3.1 Ohm
RD	DRAIN RESISTANCE	3.2 Ohm
RS	SOURCE RESISTANCE	4.2 Ohm
GGE	EXTERNAL GATE CAPACITANCE	.04 pF
CDE	EXTERNAL DRAIN CAPACITANCE	.02 pF
LG	GATE LEAD INDUCTANCE	.03 nH
LD	DRAIN LEAD INDUCTANCE	.03 nH
LS	SOURCE LEAD INDUCTANCE	.01 nH

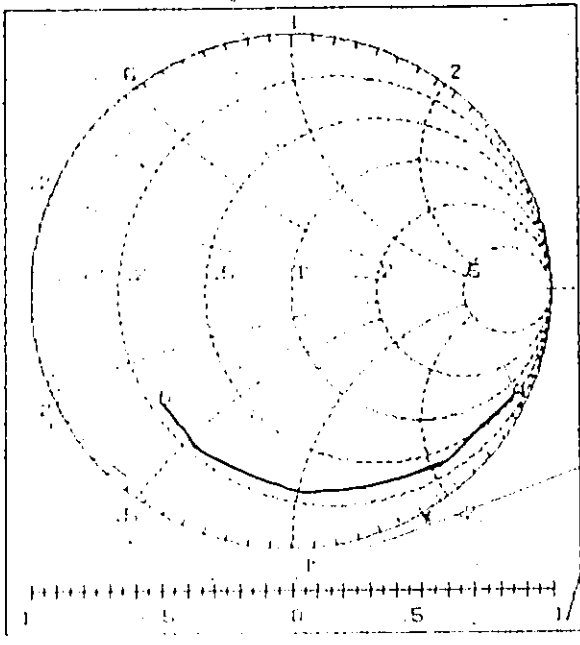
After optimization by Super-Compact the values assigned to the various components of the model were as shown in Table 2-1. In this table, G is the transconductance which relates I_{DS} , the drain to source current, to V_{GS} , the gate to source voltage. CDC is the dipole layer capacitance describing the effect of a dipole layer which is formed in the channel under the gate end of the drain. The other components in the model are self explanatory.

Table 2-2 shows the manufacturer supplied S-parameters from 2-18 GHz. Table 2-3 lists the S-parameters generated by the model.

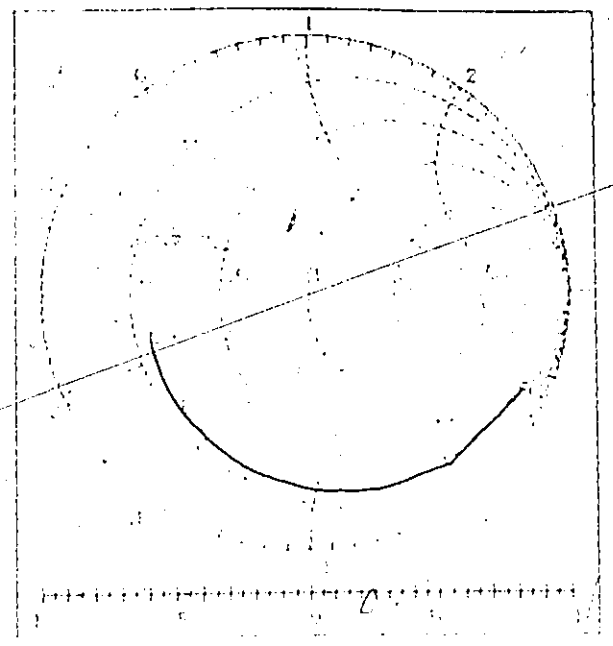
The manufacturer supplied values of S_{11} and S_{22} are compared to those generated by the model in Smith chart plots shown in Figure 2-2. S_{12} and S_{21} are compared in polar plots shown in Figure 2-3. These plots indicate that a fairly accurate description of the device is obtained with the device model.

Table 2-2
Manufacturer Supplied S-Parameters

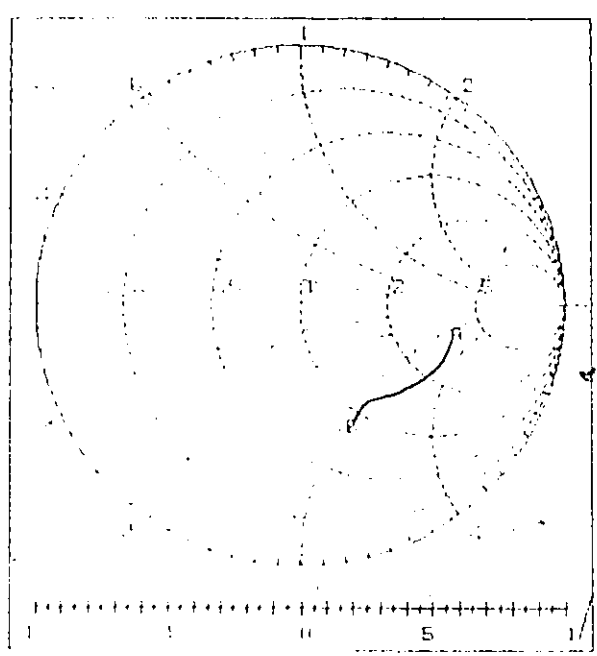
Freq GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2	0.950	-26.0	3.790	161.0	0.040	79.0	0.590	-13.0
4	0.890	-50.0	3.260	141.0	0.060	66.0	0.580	-24.0
6	0.820	-70.0	2.830	126.0	0.080	56.0	0.540	-33.0
8	0.780	-88.0	2.550	114.0	0.090	51.0	0.500	-42.0
10	0.730	-102.0	2.210	104.0	0.100	48.0	0.270	-48.0
12	0.710	-114.0	2.160	93.0	0.100	43.0	0.450	-55.0
14	0.710	-122.0	2.110	90.0	0.110	44.0	0.470	-62.0
16	0.670	-128.0	1.920	76.0	0.110	43.0	0.490	-64.0
18	0.660	-140.0	1.810	63.0	0.110	40.0	0.520	-70.0



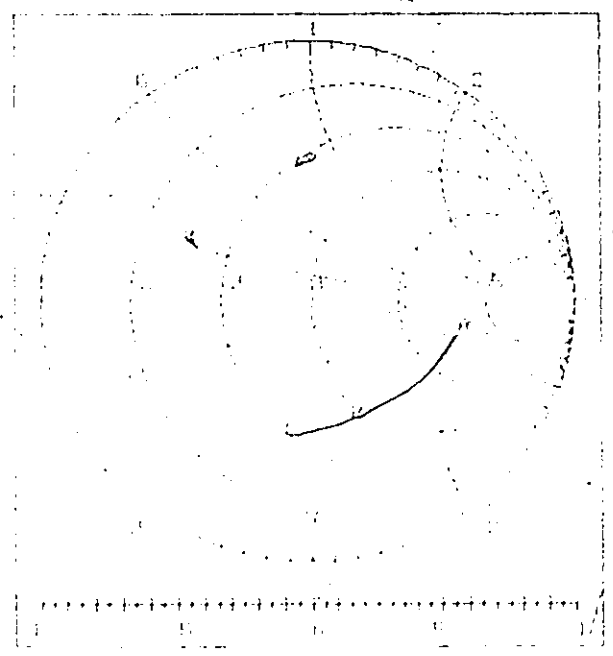
S₁₁ Manufacturer



S₁₁ Model

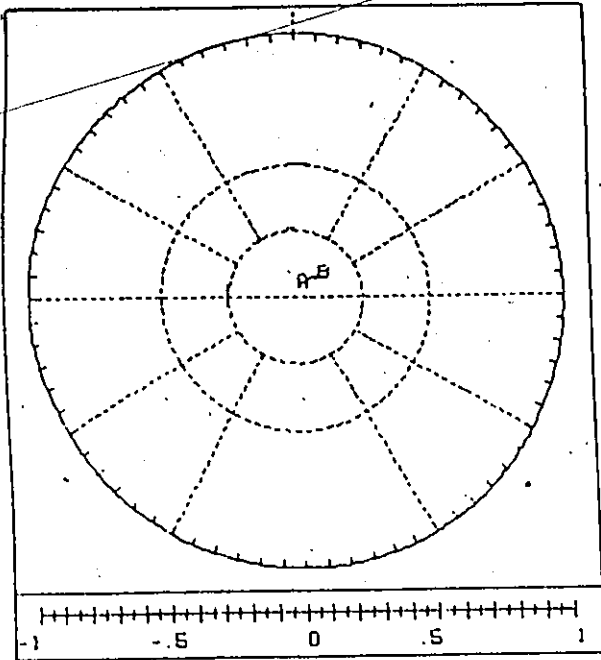


S₂₂ Manufacturer

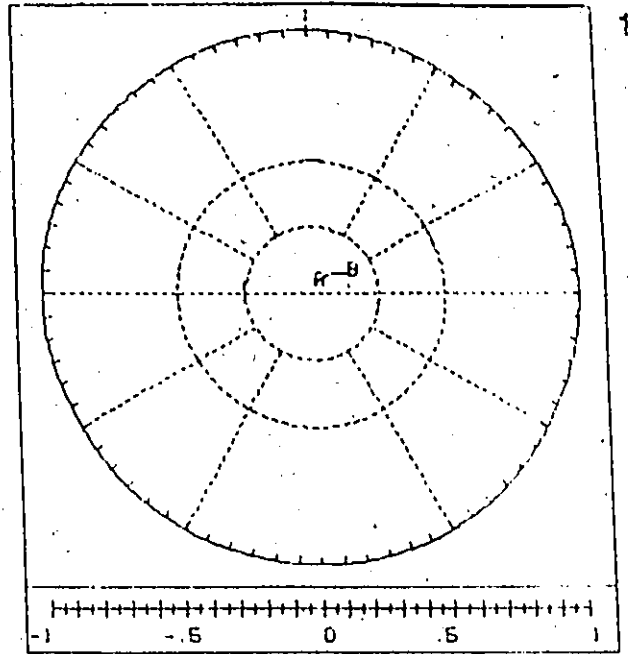


S₂₂ Model

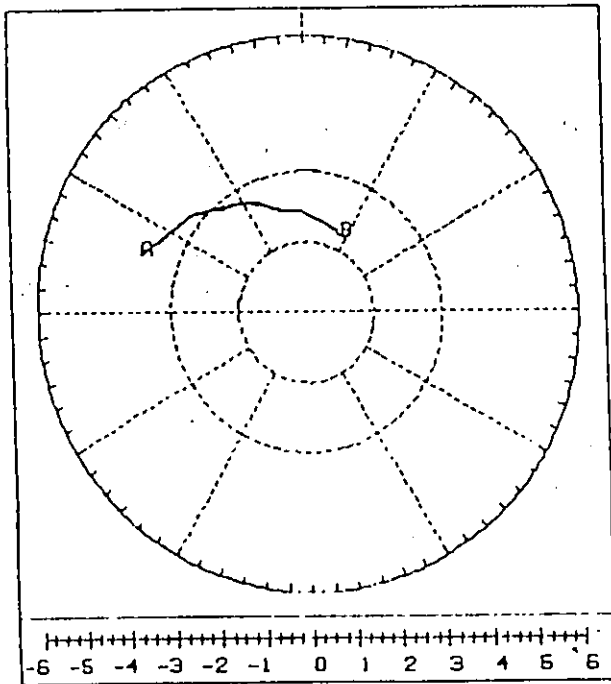
Figure 2-2 Model and Manufacturer S Parameters



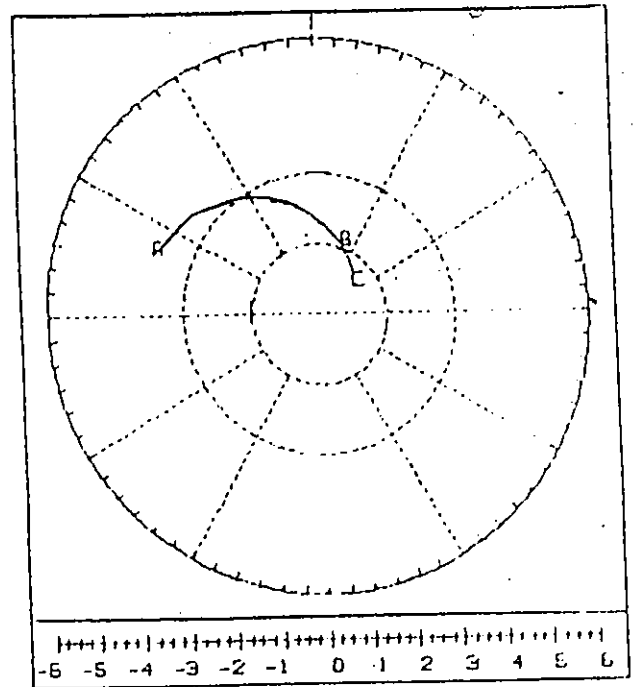
S₁₂ Manufacturer



S₁₂ Model



S₂₁ Manufacturer



S₂₁ Model

Figure 2-3 Model and Manufacturer S Parameters

Table 2-3
Model S-Parameters

Freq GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2	0.905	26.4	3.836	160.0	0.030	74.0	0.577	-12.2
4	0.862	-50.3	3.501	141.8	0.055	64.2	0.553	-23.2
6	0.813	-70.6	3.098	126.3	0.074	56.0	0.527	-32.5
8	0.769	-87.4	2.714	113.2	0.088	49.7	0.506	-40.4
12	0.707	-112.4	2.108	92.5	0.107	41.6	0.482	-53.8
14	0.686	-121.8	1.884	84.0	0.114	38.9	0.478	-59.8
16	0.670	-129.7	1.694	76.4	0.120	36.7	0.477	-65.5
18	0.657	-136.4	1.538	69.4	0.126	34.8	0.480	-71.0
20	0.647	-142.3	1.407	63.0	0.131	33.2	0.484	-76.3
22	0.639	-147.4	1.295	57.1	0.136	31.7	0.490	-81.4
24	0.632	-151.9	1.199	51.5	0.141	30.2	0.497	-86.4
26	0.627	-155.9	1.116	46.3	0.145	28.9	0.505	-91.2
28	0.622	-159.6	1.043	41.3	0.150	27.5	0.513	-95.8
30	0.618	-162.9	0.979	36.6	0.154	26.2	0.522	-100.3

The model has the most difficulty in simulating S₂₁ and S₂₂ due to their fairly nonlinear behavior with frequency as compared to the other two S-parameters. Since this model was not used in the design of the amplifier except to predict out of band performance, such as gain and stability, the fact that the model S-parameters did not exactly match the measured S-parameters caused no design errors.

Once initial investigations into the design of the amplifier were completed, more accurate measured S-parameters became available. These were supplied by the Space Electronics Division of the Communications Research Center in Ottawa. These measured S-parameters were used in the final circuit design. Table 2-4 shows the measured S parameter values. Table 2-5 shows the S-parameters modified to include the effect of bond wires. The bond wires are modelled as inductors equal to .2nH each at the gate and drain of the FET.

Table 2-4
Measured S Parameter Values

FREQ	MAG	ANG	DB	ANG	MAG	ANG	MAG	ANG
GHz	S11	S11	S21	S21	S12	S12	S22	S22
2.0	0.970	-36.0	12.477	150.000	0.610	67.000	0.610	-20.000
3.0	0.900	-49.0	11.868	138.000	0.050	60.000	0.570	-26.000
4.0	0.860	-60.0	10.828	128.000	0.060	53.000	0.550	-30.000
5.0	0.830	-74.0	10.000	123.000	0.060	52.000	0.530	-36.000
6.0	0.800	-85.0	9.337	113.000	0.070	45.000	0.510	-43.000
7.0	0.790	-94.0	8.563	104.000	0.070	44.000	0.510	-48.000
8.0	0.780	-101.0	7.889	96.000	0.080	39.000	0.520	-51.000
9.0	0.750	-108.0	7.421	95.000	0.080	41.000	0.520	-56.000
10.0	0.730	-112.0	6.888	88.000	0.080	37.000	0.490	-57.000
11.0	0.720	-118.0	5.575	84.000	0.080	38.000	0.510	-61.000
12.0	0.680	-122.0	5.343	79.000	0.080	37.000	0.510	-64.000
13.0	0.650	-123.0	4.190	78.000	0.080	38.000	0.530	-63.000
14.0	0.670	-128.0	4.959	72.000	0.090	35.000	0.520	-61.000
15.0	0.640	-135.0	4.910	67.000	0.090	40.000	0.500	-58.000
16.0	0.640	-143.0	4.454	67.000	0.090	42.000	0.470	-64.000
17.0	0.670	-147.0	4.660	64.000	0.100	46.000	0.460	-71.000
18.0	0.670	-151.0	3.107	62.000	0.100	45.000	0.470	-79.000
19.0	0.660	-153.0	2.984	54.000	0.100	48.000	0.450	-83.000
20.0	0.680	-157.0	2.212	53.000	0.090	51.000	0.430	-89.000

Table 2-5
Measured S Parameter Values
(Modified to Include the Effect of Bond Wires)

FREQ	MAG	ANG	DB	ANG	MAG	ANG	MAG	ANG
GHz	S11	S11	S21	S21	S12	S12	S22	S22
2.0	0.970	-36.582	12.648	149.006	0.041	66.069	0.606	-19.902
3.0	0.897	-50.578	12.174	136.030	0.052	58.030	0.560	-25.970
4.0	0.851	-63.100	11.275	124.766	0.063	49.766	0.534	-30.137
5.0	0.814	-79.631	10.603	117.981	0.064	46.981	0.505	-36.488
6.0	0.787	-94.156	10.082	105.917	0.076	37.917	0.475	-45.738
7.0	0.772	-106.588	9.433	95.814	0.077	34.814	0.461	-51.958
8.0	0.759	-117.377	8.867	84.729	0.090	27.729	0.457	-56.496
9.0	0.726	-128.165	8.469	81.432	0.090	27.432	0.446	-63.450
10.0	0.699	-135.970	7.958	72.360	0.090	21.360	0.398	-65.203
11.0	0.688	-145.991	6.706	66.026	0.091	20.026	0.407	-71.302
12.0	0.644	-154.293	6.477	58.950	0.091	16.950	0.392	-76.587
13.0	0.608	-158.759	5.374	56.469	0.092	16.469	0.405	-75.960
14.0	0.642	-168.153	6.123	48.220	0.103	11.220	0.375	-74.433
15.0	0.625	-179.742	5.930	41.413	0.101	14.413	0.343	-70.134
16.0	0.645	168.725	5.339	38.495	0.100	13.495	0.293	-80.993
17.0	0.693	162.053	5.492	32.300	0.110	14.300	0.266	-97.245
18.0	0.699	155.154	3.876	27.449	0.109	10.449	0.272	-114.125
19.0	0.697	149.992	3.639	17.157	0.108	11.157	0.241	-125.564
20.0	0.724	144.112	2.687	13.327	0.095	11.327	0.228	-143.141

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2. R. Pengelly, "*Microwave Field-Effect Transistors - Theory, Design and Applications*", Letchworth England: Research Studies Press, 1982, pp. 153-155.

CHAPTER III

DESIGN AND ANALYSIS OF THE AMPLIFIER

3.1 INTRODUCTION

The amplifier described in this thesis was designed as a narrowband, high gain device. Very little attempt was made to optimize either bandwidth or noise figure at the expense of gain since the purpose of the study was to develop a circuit configuration in which the transistor itself would provide stable gain. Further studies should be initiated in order to improve the bandwidth and noise figure of the amplifier. Since the finline to microstrip transition appears to be fairly wideband this would involve using a wideband matching network to increase the operating bandwidth of the amplifier.

3.2 STABILITY ANALYSIS

An important characteristic which must be carefully investigated when designing microwave amplifiers is that of stability. A microwave amplifier can be either unconditionally or conditionally stable. An unconditionally stable amplifier is one which can be considered stable (i.e. non oscillating) for all passive load and source impedances. For a conditionally stable amplifier however there exist certain load and source impedances which cause the real part of the input and output impedance of the network to become negative, thereby forcing the input or output reflection coefficients to be greater than unity. To determine whether or not a transistor is

conditionally or unconditionally stable Rollet's stability factor [1] is calculated.

$$K = 1 + \frac{|S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - \frac{|S_{22}|^2}{2|S_{12}S_{21}|}}{2|S_{12}S_{21}|} \quad (3-1)$$

The transistor is conditionally stable when K is less than unity. Woods [2] showed that for a device to be unconditionally stable, K must be greater than unity and the quantity B_1 must be positive.

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (3-2)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (3-3)$$

When the device is conditionally stable one can draw stability circles on a Smith chart to indicate the values of load and source impedance which will cause instability of the circuit. These circles can be determined as follows:

$$\text{Center } C_{Si} = \frac{(S_{ii} - \Delta S_{jj}^*)}{D_i} \quad (3-4)$$

$$\text{Radius } R_{Si} = \frac{|S_{12}S_{21}|}{D_i} \quad (3-5)$$

$$D_i = |S_{ii}|^2 - |\Delta|^2 \quad (3-6)$$

where $i=1, j=2$ when the input stability circle is being drawn, and $i=2, j=1$ when the output stability circle is being drawn. The ""

signifies the complex conjugate. The area on the Smith chart which represents stable operating conditions is either outside or inside the stability circle depending on whether $|S_{11}|$ is greater or less than unity and whether or not the origin of the Smith chart is enclosed by the circle. Here, $|S_{11}|$ is less than unity. In such a case, if the circle does not enclose the origin the region outside the stability circle represents the stable region. When the origin is enclosed by the stability circle the region within the stability circle represents stable operating conditions.

Based on the above equations, a stability analysis of the transistor (NE67300) used in this study was undertaken. Table 3-2 depicts the results of a Touchstone [3] analysis and shows the value of K and B_1 . From these results one can see that this transistor is only conditionally stable at most frequencies below 10.0 GHz. The locations of the stability circles and the region of stability is indicated in Table 3-1. The magnitude, angle and radius of the circles are given for the input (SB1) and the output (SB2). In all cases the stable region is located outside the stability circle. A plot of the stability circles is shown in Figure 3-1.

These figures and Table 3-1 emphasize the fact that the transistor is only conditionally stable. However, there are two ways of assuring stable operation when using a potentially unstable device, 1) alter the network so that the stability circles lie outside the Smith chart or 2) limit the gain such that the network operates in the stable region. The second method is treated in [4]. If one chooses to limit the gain of the amplifier, it must be kept below the

maximum stable gain (MSG) to ensure stability. This can be calculated using:

$$\text{MSG} = |S_{21}/S_{12}| \quad (3-7)$$

The values of the MSG are shown along with K and B_1 in Table 3-2. When K is > 1 the maximum available gain is shown. Maximum available gain is defined in the next section of this chapter. Early attempts at designing the amplifier described in this thesis were based on designs which limited the gain to below MSG and utilized source and load reflection coefficients outside the stability circles. These designs proved unsuccessful in that they still tended to be unstable at low frequencies. One reason for their instability is due to the fact that the transistor was seeing the reactance of a cutoff finline at low frequencies (i.e. below cutoff). There are presently no means to calculate the reactance of a finline below cutoff. This makes it very difficult to predict whether or not a conditionally stable transistor placed in a finline will oscillate at frequencies below the cutoff frequency of the finline.

Early attempts at mounting a FET directly in a finline circuit resulted in unpredictable oscillations due to the low frequency cutoff behavior of the finline. At this point it became clear that the combination of finline and microstrip described in this thesis would be better suited in this application. The impedance seen by the FET at low frequencies could be predicted so that these oscillation conditions could be avoided. By proper design of the bias circuit the lower out of band frequencies would see a 50 ohm load. As seen from

the stability circles this represents a stable load at all frequencies.

At the design frequency the bias circuit is designed such that the FET would see the finline. The circuit configuration which allows this is described in the next chapter.

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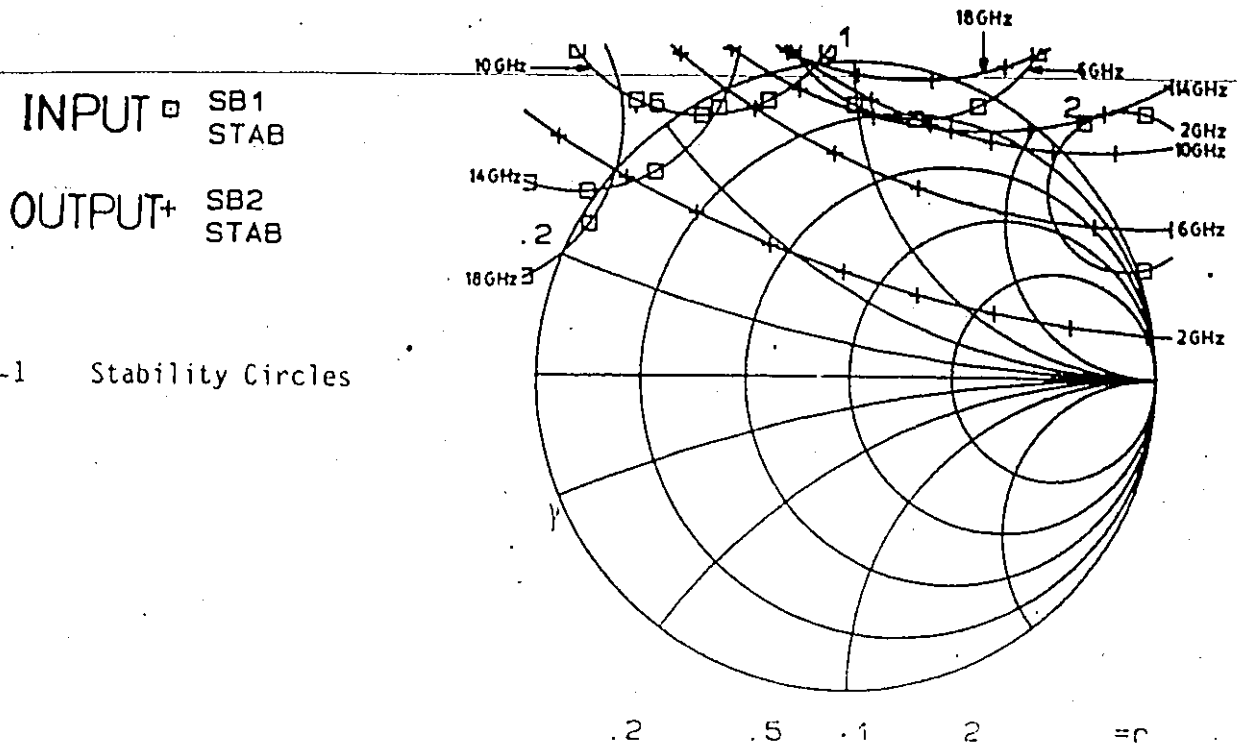


Figure 3-1 Stability Circles

Table 3-1 Stability Circle Locations

FREQ-GHZ	MAGLSB1J STAB	ANGLSB1J STAB	RADLSB1J STAB	PARLSB1J STAB	MAGLSB2J STAB	ANGLSB2J STAB	RADLSB2J STAB	PARLSB2J STAB
2.00000	1.034	39.037	0.090	1.000	2.871	73.058	2.369	1.000
4.00000	1.174	63.459	0.129	1.000	2.053	51.481	0.874	1.000
6.00000	1.317	94.201	0.429	1.000	2.845	77.577	2.099	1.000
8.00000	1.345	110.349	0.439	1.000	2.549	81.737	1.747	1.000
10.0000	1.400	119.640	0.416	1.000	2.305	79.735	1.336	1.000
12.0000	1.460	128.722	0.395	1.000	1.964	78.606	0.859	1.000
14.0000	1.512	136.069	0.454	1.000	2.013	77.054	0.925	1.000
16.0000	1.526	148.104	0.416	1.000	2.042	74.910	0.869	1.000
18.0000	1.418	153.575	0.347	1.000	1.896	85.154	0.776	1.000
20.0000	1.403	157.823	0.270	1.000	2.024	91.541	0.760	1.000

FREQ-GHZ	K	B1	DB[GMAX]
	B267300	B267300	B267300
2.00000	0.344	1.219	15.218
3.00000	1.039	1.221	12.742
4.00000	1.401	1.210	8.864
5.00000	1.780	1.225	7.095
6.00000	0.639	1.218	16.218
7.00000	0.697	1.218	15.830
8.00000	0.701	1.181	14.914
9.00000	0.748	1.178	14.680
10.0000	0.947	1.185	14.413
11.0000	1.059	1.158	12.272
12.0000	1.234	1.115	10.725
13.0000	1.484	1.053	8.946
14.0000	1.189	1.080	10.308
15.0000	1.317	1.083	9.540
16.0000	1.389	1.141	8.969
17.0000	1.095	1.202	10.456
18.0000	1.283	1.191	8.359
19.0000	1.391	1.203	7.766
20.0000	1.657	1.245	6.823

Table 3-2 Stability Analysis and Maximum Available Gain

3.3 MATCHING NETWORK DESIGN

An initial step in the design process was to determine the maximum available gain at 20 GHz, the design frequency. The maximum available gain (MAG) is defined as the power available at the output of the amplifier divided by the power available at the input when both input and output are simultaneously conjugately matched. The value of MAG can be determined using:

$$\text{MAG} = \frac{|S_{21}|}{|S_{12}|} (K - \sqrt{K^2 - 1}) \quad (3-8)$$

Using the S-parameters from Table 2-5 and the value of K found in Table 3-2, MAG was found to be 6.8 dB at 20 GHz. The load and source terminations which enable a simultaneous conjugate match are found using the following equations. The input and output reflection coefficients of a two-port when terminated by an arbitrary source and load are given by:

$$\Gamma_{in} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (3-9)$$

$$\Gamma_{out} = S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (3-10)$$

When these equations are solved simultaneously for $\Gamma_S = \Gamma_{in}^*$ and $\Gamma_L = \Gamma_{out}^*$ the following equations result.

$$\Gamma_{MS} = \frac{B_1 - \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad (3-11)$$

$$\Gamma_{ML} = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (3-12)$$

Where B_1 is previously defined in equation 3-2 and

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (3-13)$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad (3-14)$$

$$C_2 = S_{22} - \Delta S_{11}^* \quad (3-15)$$

Δ is as defined in equation 3-3.

Using the S-parameters for 20 GHz listed in Table 2-5 and solving the above equation yields:

$$\Gamma_{MS} = .79 \angle -145$$

$$\Gamma_{ML} = .46 \angle 132$$

These correspond to the reflection coefficients which the input and output of the transistor must see in order to achieve the maximum available gain of 6.8 dB. By denormalizing this to 50 ohms these reflection coefficients correspond to impedances of:

$$Z_{in} = 6.8 - j15.3 \quad Y_{in} = \frac{1}{Z_{in}} = .023 + j.055$$

$$Z_{out} = 21.5 + j18.6 \quad Y_{out} = \frac{1}{Z_{out}} = .027 - j.023$$

A single parallel stub is used to realize the input and output matching network. The smith chart shown in Figure 3-2 illustrates the design of the input matching network while Figure 3-3 shows the design of the output matching network. The input matching network consists of an open circuited stub $.190\lambda$ long at a distance $.006\lambda$ from the FET. The output matching network is a $.374\lambda$ long stub situated $.478\lambda$ away from the FET. All the lines are assumed to be 50 ohm. Table 3-3 shows the calculated results of the reflection coefficients when using these parallel stub matching networks. As shown in the table we can see that these results are very close to the desired reflection coefficients at 20 GHz. In the next chapter the microstrip realization of this matching network as well as the realization of the rest of the amplifier circuit is discussed.

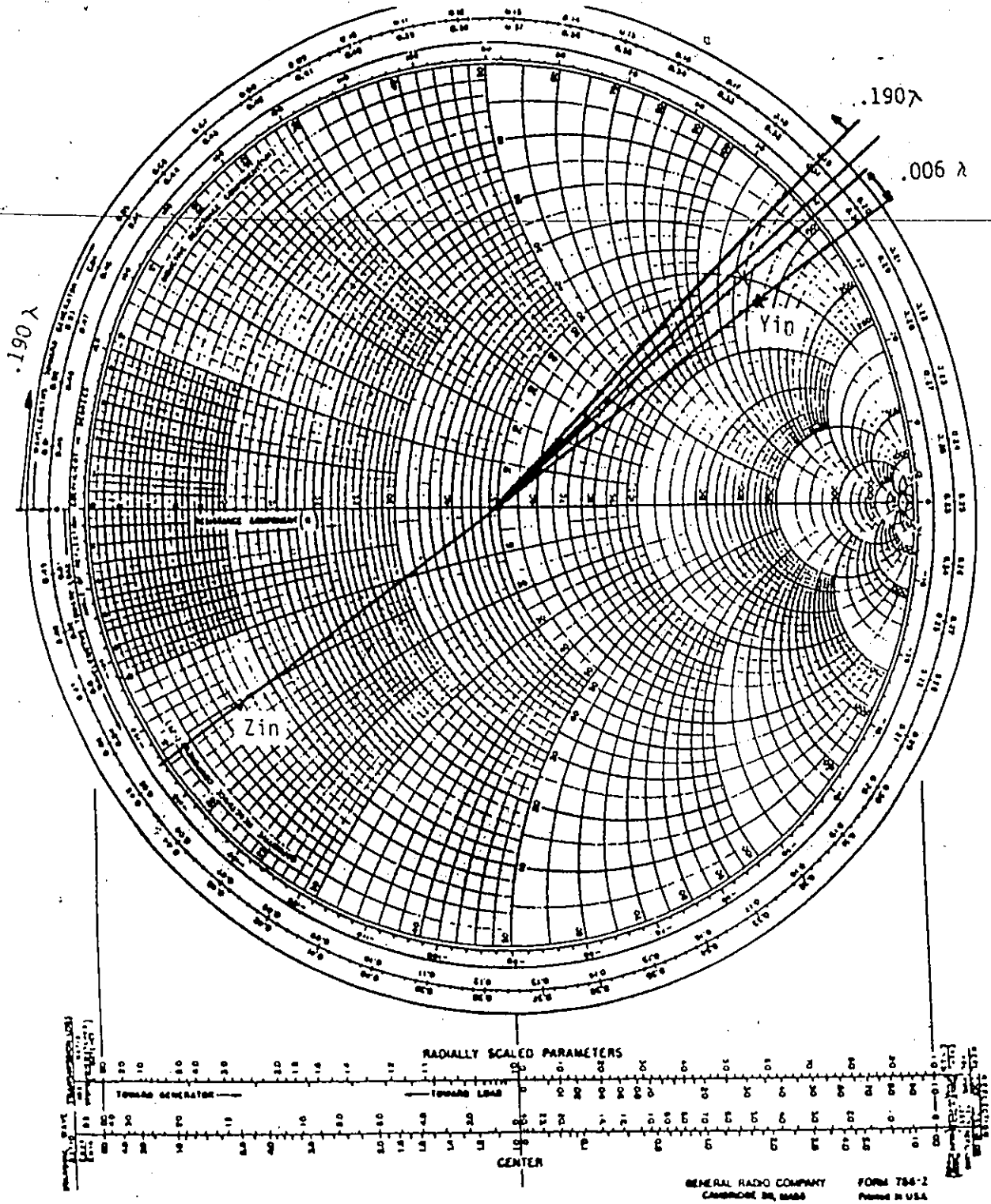


Figure 3-2 Input Matching Network Design

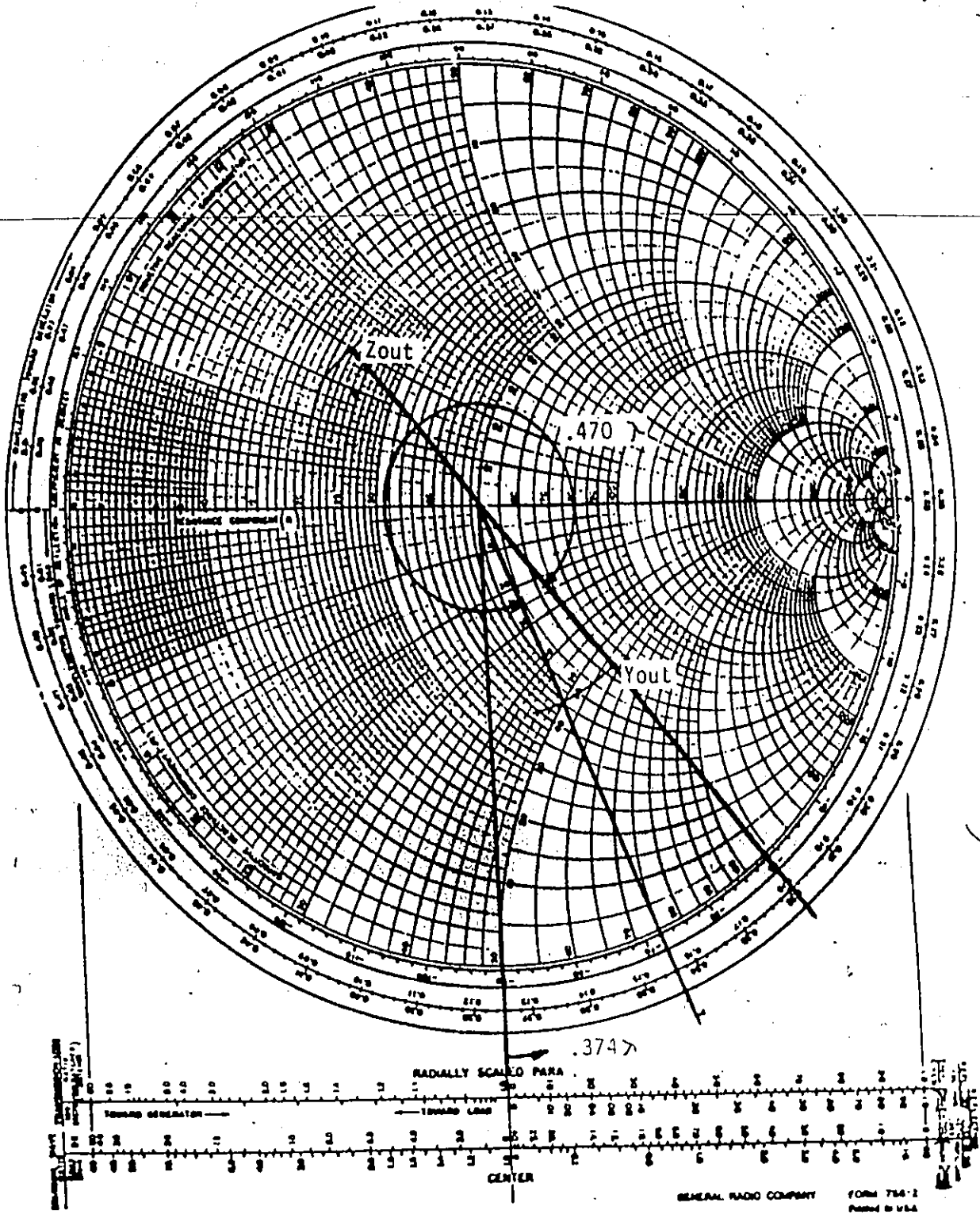


Figure 3-3 Output Matching Network Design

Table 3-3 Analysis of Input and Output Matching Networks

FREQ-GHZ	MAG[G1]	ANG[G1]	MAG[G1]	ANG[G1]
	MATCH2	MATCH2	MATCH3	MATCH3
18.0000	0.678	-136.601	0.646	-179.387
19.0000	0.731	-141.075	0.549	156.479
20.0000	0.784	-145.946	0.460	133.374
21.0000	0.836	-151.239	0.379	111.057
22.0000	0.885	-156.966	0.305	89.332
23.0000	0.928	-163.113	0.236	68.047
24.0000	0.963	-169.636	0.172	47.077
25.0000	0.988	-176.455	0.110	26.325
26.0000	0.999	176.543	0.051	5.707

3.4 NOISE ANALYSIS

It is known that the noise factor of a linear two-port can be related to the source admittance Y_S by:

$$F = F_{\min} + \frac{R_n |Y_S - Y_{\text{opt}}|^2}{G_S} \quad (3-19)$$

where $Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}}$ is the source admittance at which $F = F_{\min}$ and $Y_S = G_S + jB_S$. R_n is the normalized equivalent noise resistance of the two-port. For the design of a low noise amplifier the values of F_{\min} , R_n and Y_{opt} (in terms of Γ_{opt}) are often specified by the transistor manufacturer. For the transistor used, these parameters are shown in Table 3-4.

Table 3-4
NOISE FIGURE DATA FOR NE67300

Freq. GHz	MIN NOISE FIGURE dB	OPT NOISE SOURCE		NORM Rn
		MAG	ANG	
4.0	0.40	0.640	69.0	0.380
8.0	0.80	0.550	115.0	0.200
12.0	1.40	0.480	155.0	0.200
18.0	1.90	0.460	-33.0	0.400

Using the specified optimum source reflection coefficient and specifying a conjugate match at the output we can determine the achievable transducer gain if the optimum noise figure is desired. Using Super-Compact it was found that this gain corresponds to 2.9 dB at 18 GHz for a noise figure of 1.9 dB.

Since noise data is only available up to 18 GHz the amplifier could not be analyzed for noise figure at the design frequency calculated. However in the next chapter results are given up to 18 GHz.

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3. Touchstone version 1.4 (computer program) *EEsof*, 31194 La Baya Drive, Westlake Village, CA 91362.
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CHAPTER IV

REALIZATION OF THE AMPLIFIER IN FINLINE

4.1 MOUNTING A FET IN FINLINE

Previously, FETs have been mounted in finline in at least four different circuit configurations. Jacob et al. [1] realized a FET oscillator by mounting a FET between two finlines in a four-port finline junction as shown in Figure 4-1a. Feedback was provided by printing a metal strip on the back of the circuit between the drain and gate.

Meinel [2] designed a 30 GHz oscillator by mounting a FET inside a T-type finline series junction as shown in Figure 4-1b. By changing the length of the gate drain resonator some degree of mechanical tuning was achieved. This circuit, although well suited for oscillator applications, could not be used to mount a FET in an amplifier configuration due to the gate-drain feedback which leads to an unstable circuit.

Ebner et al. [3] have designed a transistor mount which can be used to mount a FET in a configuration suitable for use as an amplifier. Their circuit consists of antipodal to microstrip transitions at the input and output ports similar to that described by van Heuven [4]. The transistor is then mounted in microstrip using conventional means. A dissipative slot is incorporated in one of the antipodal fins to provide a resistive load to the transistor at frequencies below cutoff of the finline. This graphite slot is located

near the waveguide housing away from the finline slot so that it has little influence on the dominant finline mode. Although this circuit allowed stable operation of all transistors tested by the authors, the transitions accounted for at least 2.5 dB insertion loss at X band.

L'Ecuyer et al. [5] described an FET amplifier at 17 GHz which was constructed using finline. The configuration used is shown in Figure 4-1c. The circuit was designed such that the FET sees only the bias circuit at frequencies below cutoff of the finline. This circuit was difficult to tune and had a relatively low gain.

An initial attempt at designing the amplifier described in this thesis used a circuit configuration similar to that used by Jacob [1]. The circuit is shown in Figure 4-2. Jacob's circuit utilized a metallic strip on the back of the substrate in order to increase the feedback from the drain to gate to have an oscillation condition. Since in this amplifier as little feedback as possible was desired, the input and output arms of the circuit were separated by plated through holes as well as metallic septums both above and below the circuit. A window was cut in the metal septum above the circuit where the FET was bonded. The bias circuit was designed in coplanar waveguide similar to L'Ecuyer's design. A 100 ohm chip resistor was bonded between the gate and source to act as a load at low frequencies. Sliding finline shorts were used to achieve maximum coupling between the FET bond wires and the finline slots.

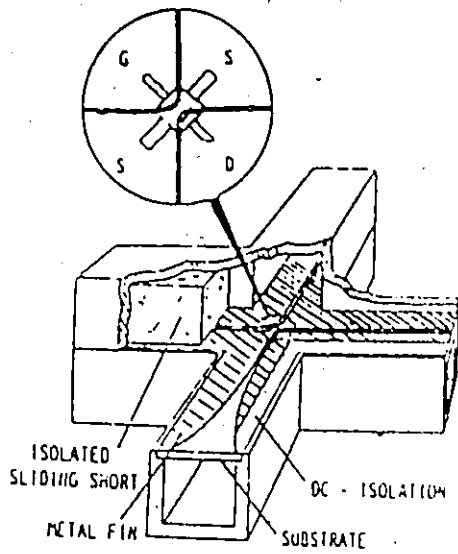
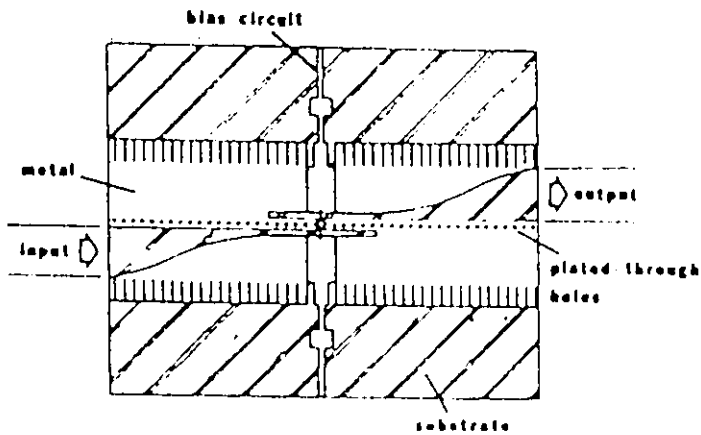
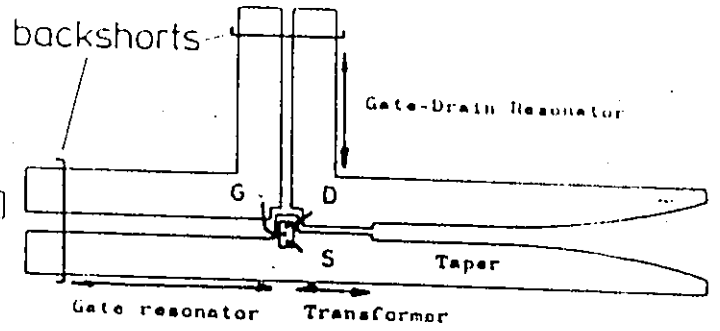


Figure 4-1a FET Oscillator after Jacob [1]

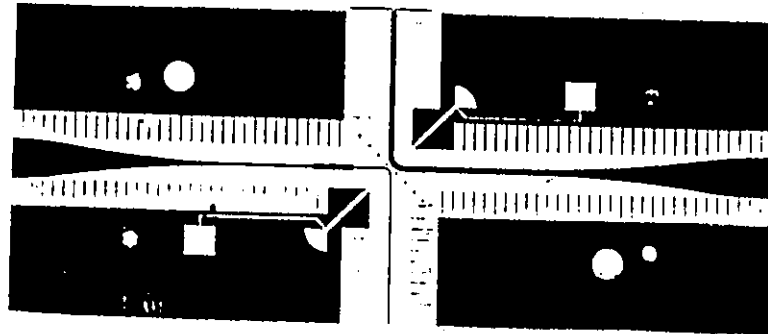
Figure 4-1b FET Oscillator after Meinel [2]



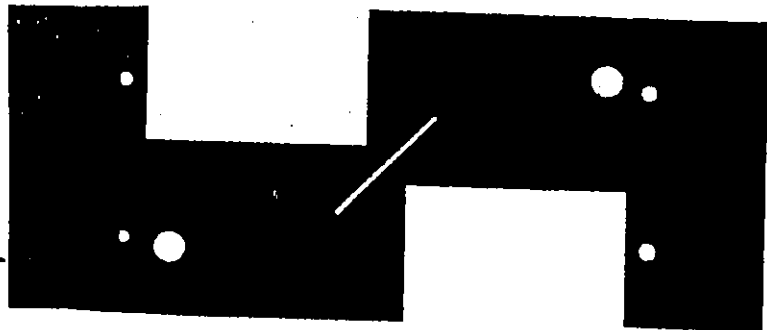
METALIZATION PATTERN OF FIN LINE AMPLIFIER

Figure 4-1 FET Mounting Structures

Figure 4-1c FET Amplifier after Leever [3]



Front



Back

Figure 4-2 Initial Circuit Topology

Analysis showed that this resistor only lowered the gain slightly at the design frequency. This circuit was found to be very susceptible to instability and did not provide much flexibility with tuning. Because of this, a new circuit configuration was chosen which is perfectly stable while providing a much greater flexibility in tuning. The new circuit topology is shown in Figures 4-3a, 4-3b and 4-3c. Figure 4-3a shows the front of the circuit which consists of the finline input and output circuitry. Figure 4-3b shows the backside of the circuit which consists of the amplifier matching and bias networks. Figure 4-3c shows an overlay of the two circuits to show how they match up together when printed on the substrate. The circuit was manufactured at Bolriet Technologies using a thin film process. In this process a thin layer of copper is sputtered onto the bare substrate. This thin layer is then etched. The etched circuit is plated to the desired thickness and gold flashed. Because a very thin layer of copper is being etched, very fine lines and spaces can be realized with this technique. This circuit was manufactured on RT Duroid 5880 material which has a dielectric constant of 2.20. The design and operation of the circuit is described in the following sections.

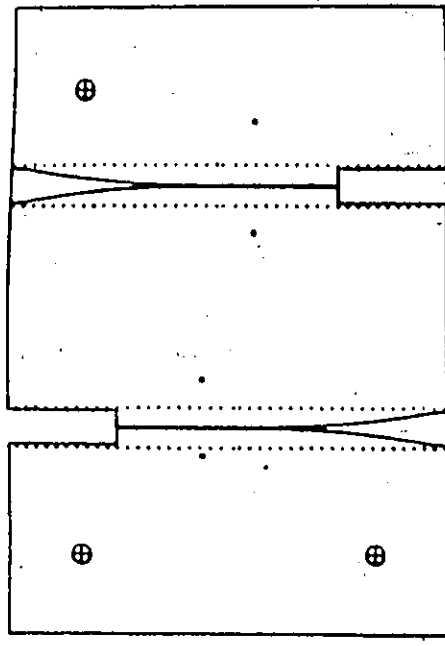


Figure 4-3a Back

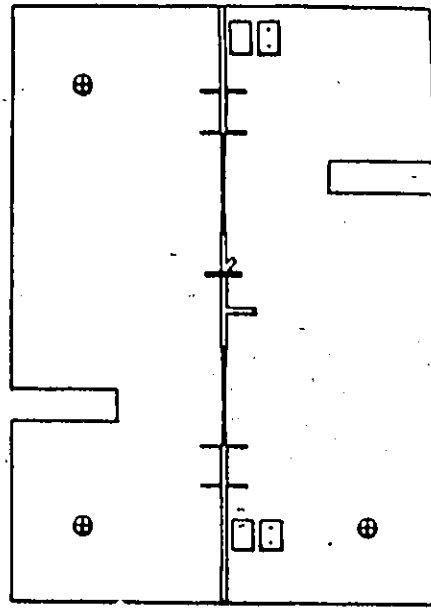


Figure 4-3b Front

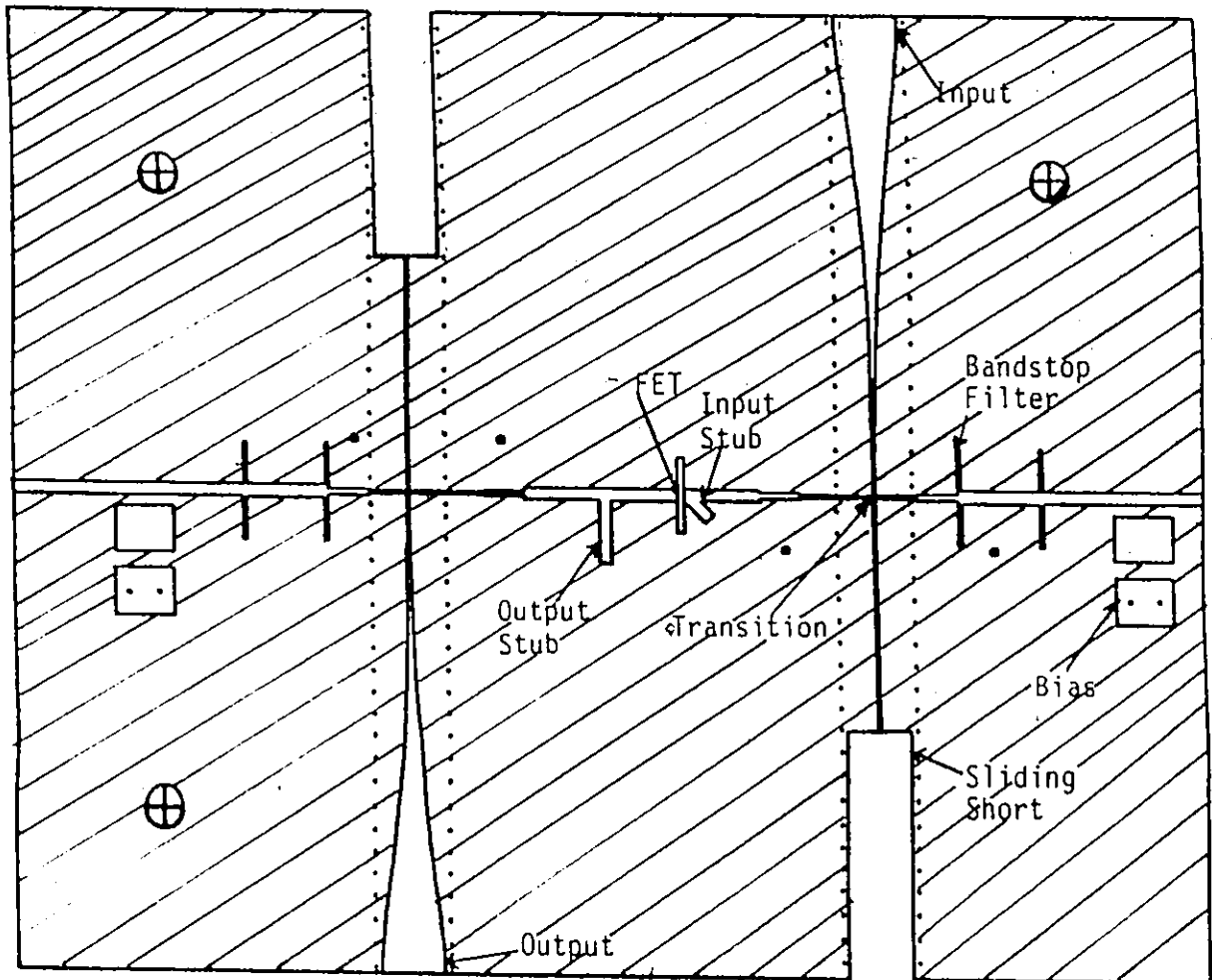


Figure 4-3c Overlay

4.2 INPUT AND OUTPUT TAPER DESIGN

The input and output of the amplifier consists of transitions from waveguide to finline to microstrip. In this circuit the transition from waveguide to finline consists of a taper. Although quarter-wave transformers have been used for this purpose they provide a relatively narrow band match as compared to that of a tapered transition. There are various taper profiles which may be used. These include exponential, parabolic and cosine squared tapers. Optimum design data for these tapers have been described by Pramanick et al. [6]. A taper profile described by Beyer et al. [7] has been used in this thesis. The taper profile is determined by two circular arcs. The authors show that this easily realizable taper provides greater than 30 dB return loss from 18 to 26.5 GHz. Using equations developed in [7] one chooses the impedance at the midpoint ($l/2$) of the taper to equal the algebraic mean of the end impedances, so that at $z = l/2$:

$$Z_0(l/2) = \frac{Z_b + Z_d}{2} \quad (4-1)$$

where Z_b is the impedance of a full height waveguide (470 ohms) and Z_d is the finline impedance. The authors give expressions for the radius and centers of circular arcs which will provide smooth continuous transitions with the impedance at $z = l/2$ being $Z_0(l/2)$.

Both input and output tapers were 25 mm long. This corresponds to approximately 1.5 times the length of the finline guided wavelength. The transitions were analyzed using Touchstone by dividing each transition into ten cascaded transmission lines 2.5 mm in length. The characteristic impedance and effective dielectric constant at 20 GHz was determined for each finline section. In this way each of the finline sections could be treated as general transmission lines. The results of this analysis are shown in Figure 4-4. In the analysis shown, dispersion effects were not included. That is to say, the characteristic impedance and effective dielectric constant of the finline sections were assumed to not vary over the frequency range of interest. This approximate analysis shows the transitions to have a return loss greater than 40 dB from 18 to 26 GHz.

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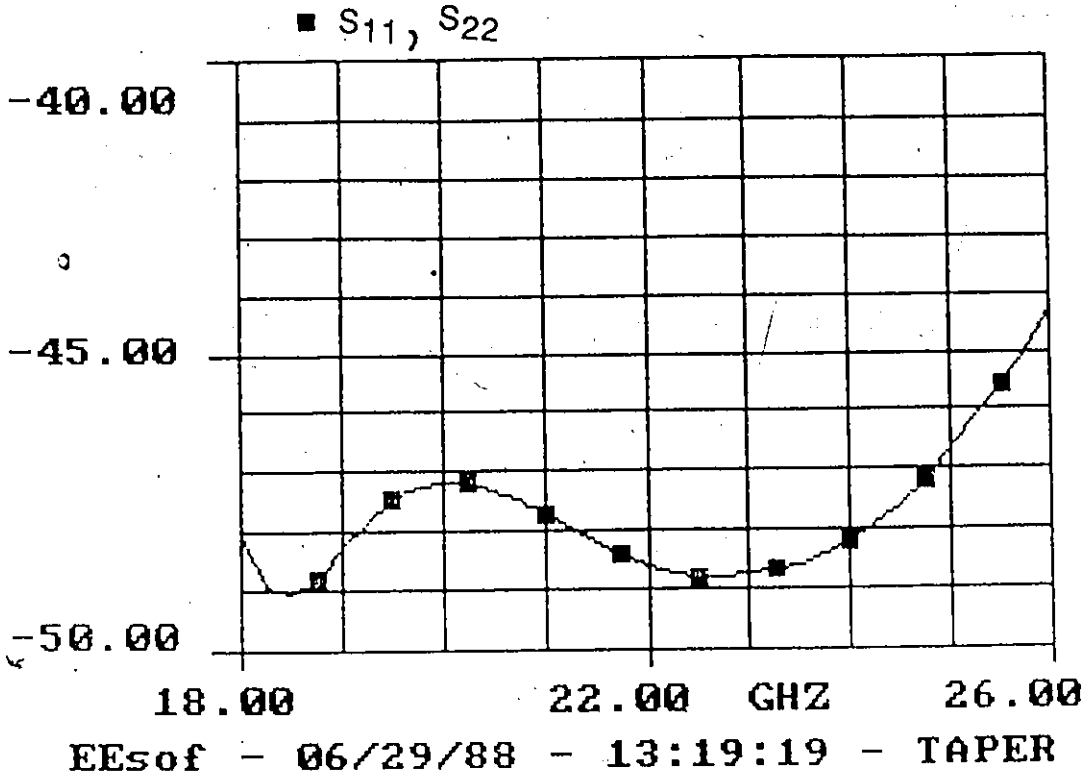


Figure 4-4 Input and Output Taper Analysis

4.3 FINLINE TO MICROSTRIP TRANSITION

Design of the finline to microstrip transition is based on designs of slotline to microstrip transitions. To check the validity of treating the finline as a slotline, data taken from a paper by Mariani et al. [8] for the characteristics of slotline was compared to data generated by a finline spectral domain program using the same parameters. Mariani et al. calculated a .137 inch thick substrate with an $\epsilon_r = 20.3$ and a slot width of .024 inches to have a characteristic impedance of 45 ohms and an effective dielectric constant (ϵ_{eff}) of 8.60. The finline program yielded a Z_0 of 50.5 ohms and ϵ_{eff} equal to 8.80 when the waveguide walls were moved a large distance away (approximately 100x slot width). Additionally it was postulated that because a very narrow slot was being used in the amplifier circuit ($d = .15\text{mm}, d/b = .03$) the walls would have little effect on the characteristic impedance and effective dielectric constant so that the model of a slotline to microstrip transition could be used for the finline to microstrip transition.

Knorr developed a model for slotline to microstrip transitions in a paper on slotline transitions, [9]. Figure 4-5 shows a typical slotline to microstrip transition and its equivalent circuit. As shown in Figure 4-5, the transition consists of a slotline and microstrip crossing each other at right angles. The slotline is terminated by a short circuit $\lambda/4$ from the junction. The microstrip line is terminated in an open circuit a distance $\lambda/4$ from the junction. In the model shown, the reactance X_{os} represents the

inductance of a short circuited slotline, C_{oc} is the capacitance due to the end effect of an open microstrip line. Z_{os} and Z_{om} are the characteristic impedances of the slot and microstrip. Figure 4-5c shows the equivalent finline to microstrip transition which is used in this thesis. In this figure Z_{of} is the finline impedance and Z_{om} is the microstrip impedance. The value of the turns ratio n for the transformer is dependant on the fields in the slotline. Knorr defined n as the ratio:

$$n = \frac{V(h)}{V_o} \quad (4-2)$$

where V_o is the voltage across the slot and $V(h)$ is the voltage on the microstrip side of the circuit. Based on the slot field, Knorr derived an equation for n as:

$$n = \cos 2\pi \frac{Du}{\lambda_0} - \cot q_0' \sin \frac{2\pi Du}{\lambda_0} \quad (4-3)$$

$$q_0' = \frac{2\pi Du}{\lambda} + \tan^{-1} \frac{u}{v} \quad (4-4)$$

$$u = \sqrt{\epsilon_r - \left(\frac{\lambda}{\lambda'}\right)^2} \quad (4-5)$$

$$v = \sqrt{\left(\frac{\lambda}{\lambda'}\right)^2 - 1} \quad (4-6)$$

$$\frac{\lambda}{\lambda'} = \sqrt{\epsilon_{eff}} \quad (4-7)$$

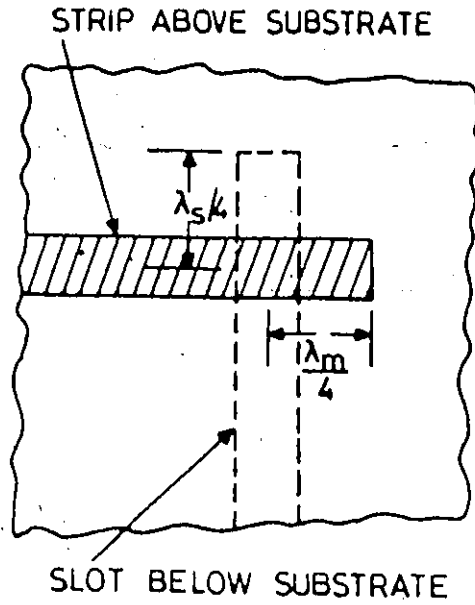


Figure 4-5a Geometry

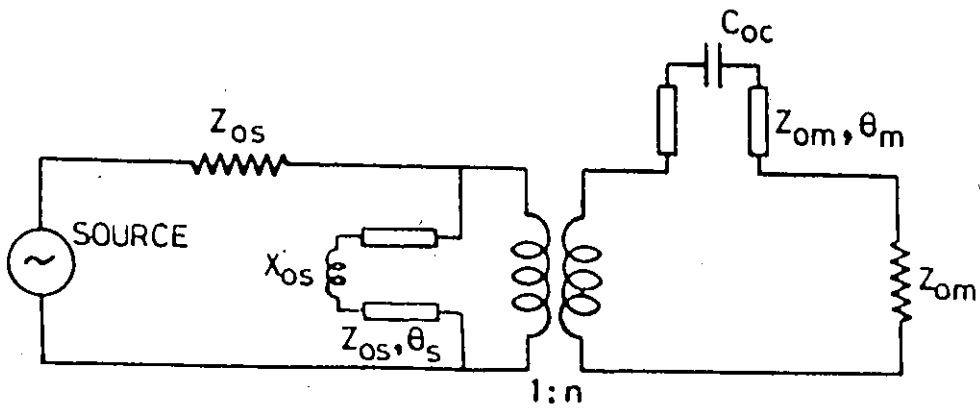
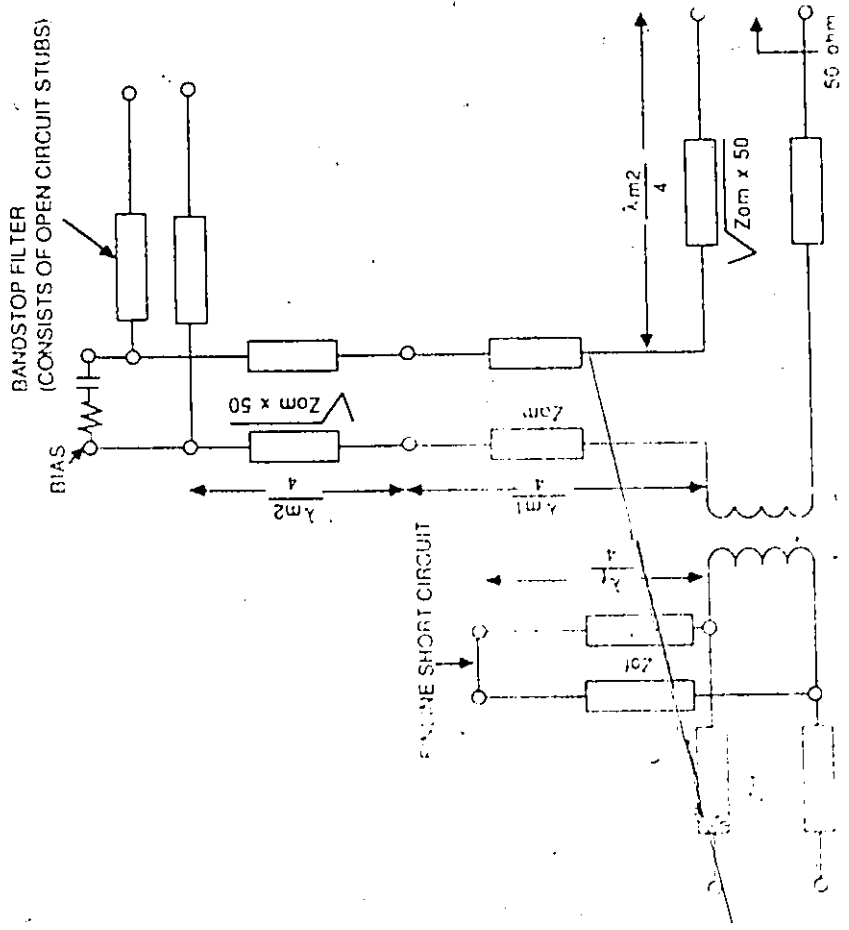
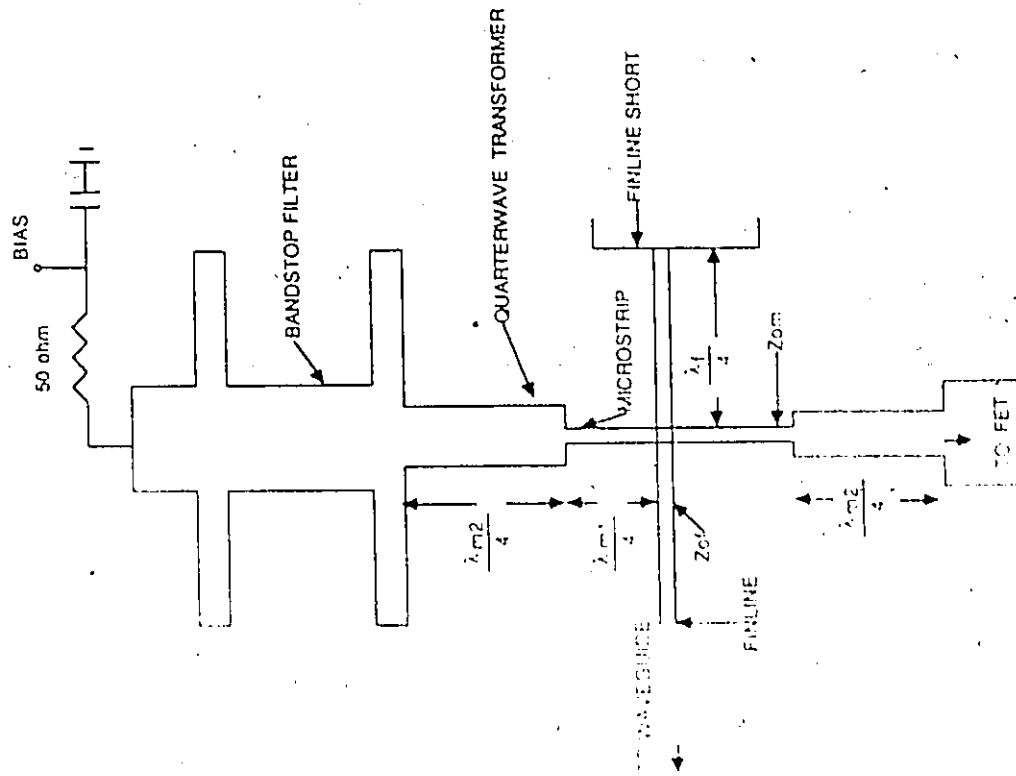


Figure 4-5b Equivalent Circuit

Figure 4-5 Slotline to Microstrip Transition



$Z_{om} = 121 \text{ ohm}$; $\lambda_{m1}, \lambda_{m2} = \text{GUIDED WAVELENGTH IN MICROSTRIP}$
 $Z_{of} = 130 \text{ ohm}$; $\lambda_f = \text{GUIDED WAVELENGTH IN FINLINE}$

Figure 4-5c Finline To Microstrip Transition

In these expressions λ' is the guided wavelength. D is the substrate thickness. A relatively low impedance finline (130 ohms) was chosen for the transition. This impedance was chosen to be low enough to match the microstrip assuming a small turn ratio, however not too low so the finline gap became too narrow to realize. Also if the gap becomes too narrow losses in the finline increase significantly. In order to have a 130 ohm finline within a WR-42 waveguide housing at 20 GHz the slot width was found to be .15 mm. This configuration yields an ϵ_{eff} of 1.16. This data was generated using a transverse resonance program which is described in the last chapter. This program became necessary when it came to analyzing a finline with extremely narrow slots. As will be shown in the last chapter the characteristics of a finline with narrow slots can be very dependent on the metallization thickness.

From looking at the model, if we assume no end effect of either the microstrip line or slotline we have:

$$Z_{om} = n^2 Z_{os} \quad (4-8)$$

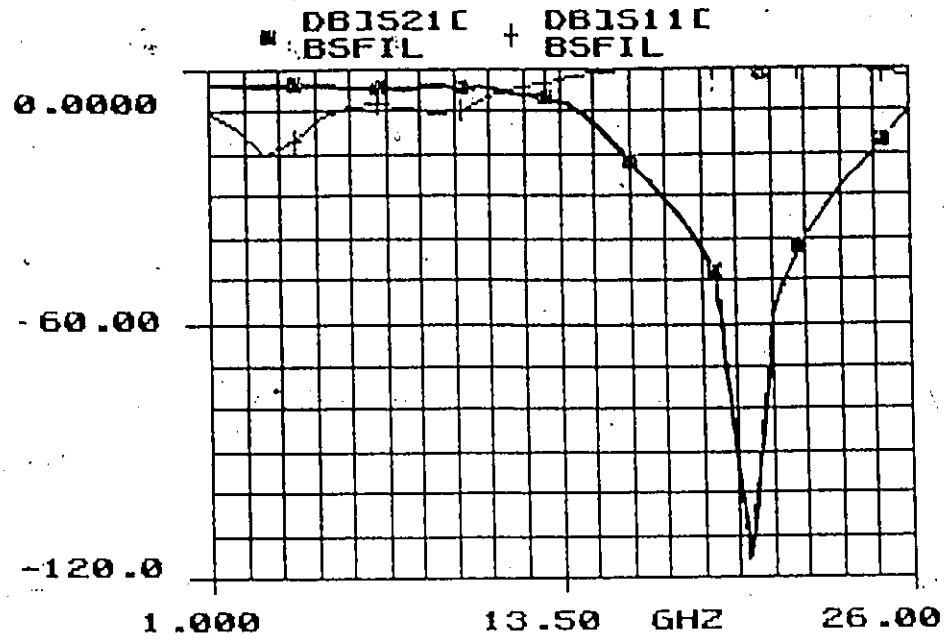
These assumptions are valid in this case because in the circuit configuration used an open ended microstrip stub is not utilized in the transition and an almost perfect finline short is formed using a sliding short which fills the waveguide. If we substitute $\epsilon_{eff} = 1.16$ and $D = .254$ mm into equations 4-3 through 4-6, we get $n = .96$. Substituting this into 4-8 for n and 130 ohms for Z_{os} ($=Z_{of}$) we get $Z_{om} = 121$ ohms.

The microstrip open circuit stub is realized by placing a 20 GHz band stop filter a half wavelength from the transition junction. This filter is realized using two pairs of 100 ohm quarter wavelength long open circuit stubs which are separated by a half wavelength 50 ohm line. A 50 ohm resistor and 36 pf capacitor terminate the filter section at the point bias is applied. Figure 4-6 shows a Touchstone analysis of the bandstop filter. The graph shows that the filter has low losses below the cutoff frequency of the finline. This is necessary so that at low frequencies the FET sees the 50 ohm terminating resistor which represents a stable load at these frequencies. Placed in front of the bandstop filter, within the half wavelength line was a 78 ohm quarter wave transformer to transfer the 121 ohm microstrip line impedance to the 50 ohms of the bias circuit.

The finline noncontacting short circuit was realized with a brass block which could slide in the waveguide channel. This block had a slot cut in it which was slightly larger than the substrate thickness. This allowed the block to slide over the fin and provided a very good sliding short circuit. The optimum position for this short circuit is a quarter wavelength (2.8 mm) from the transition junction. The complete transition was analyzed using Touchstone. The results of the analysis are shown in Table 4-1 and Figure 4-7

From these results a relatively broadband transition can be anticipated. The results show less than 2 dB insertion loss over more than half the waveguide band. The return loss is better than 25 dB at 20 GHz. To test the transition separately from the amplifier a back to back transition was fabricated and tested in the amplifier

housing. The two transitions were separated by about half an inch of 50 ohm line. Figure 4-8 shows the results. The measurements were done on a Hewlett Packard 8510 network analyzer at Bolriet Technologies. These two transitions together showed an insertion loss of 1.5 dB at the design frequency of 20 GHz. The return loss was 25 dB. The transitions show less than 2 dB loss from 18 to 23 GHz, which is quite low considering the loss includes losses due to two tapers, two finlines and a short length of microstrip. Also shown in this plot is the predicted response. The two results are in close agreement. The analysis showed .1 dB insertion loss at the design frequency whereas the measurements demonstrate .75 dB loss per transition. This difference is probably due to the fact that the Touchstone model doesn't include losses for the microstrip line or the finline. Since this transition shows very little loss it is possible to design a one stage amplifier which provides reasonable gain.



FREQ (GHz)	DB1521C BSFIL	DB1511C BSFIL
1.00000	-3.451	-19.345
2.00000	-3.250	-13.346
3.00000	-3.091	-20.105
4.00000	-3.144	-16.719
5.00000	-3.407	-11.067
6.00000	-3.699	-8.637
7.00000	-3.820	-7.930
8.00000	-3.702	-8.701
9.00000	-3.510	-10.093
10.00000	-3.260	-9.290
11.00000	-4.247	-8.119
12.00000	-5.207	-5.169
13.00000	-6.711	-3.114
14.00000	-8.879	-1.870
15.00000	-14.870	-0.507
16.00000	-21.719	-0.168
17.00000	-29.041	0.085
18.00000	-37.155	-0.087
19.00000	-47.726	0.086
20.00000	-115.506	-0.087
21.00000	-57.969	-0.062
22.00000	-41.866	0.074
23.00000	-31.391	-0.039
24.00000	-24.697	0.167
25.00000	-18.690	-0.427
26.00000	-9.591	-1.666

Figure 4-6 Analysis of Bandstop Filter

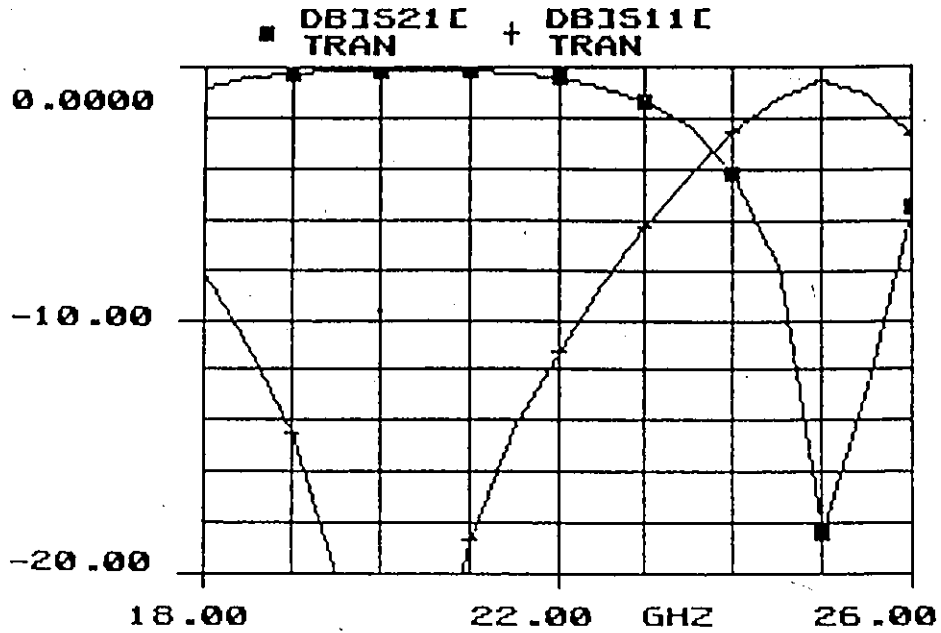


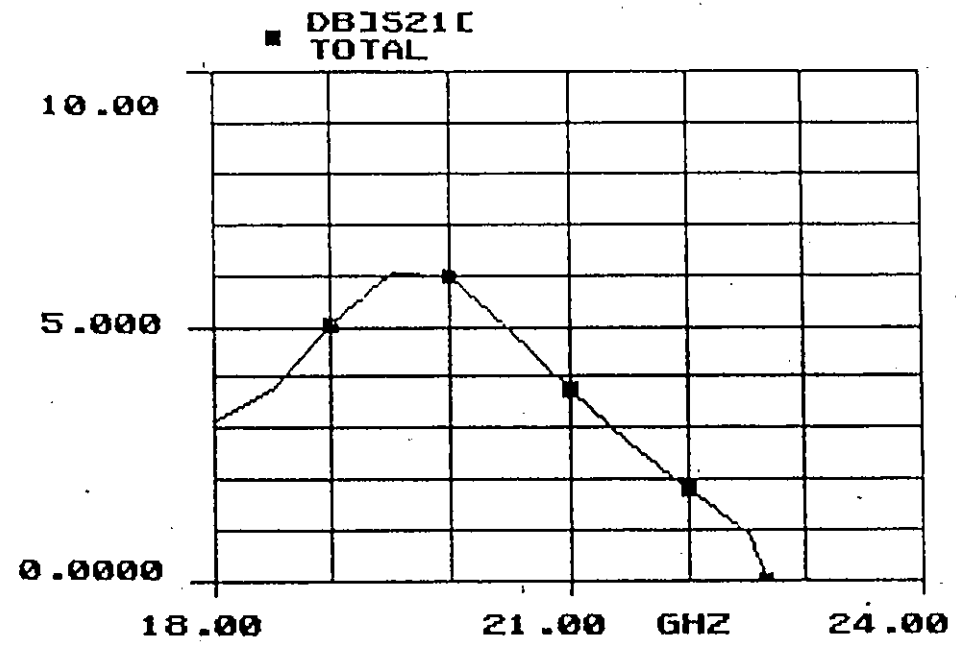
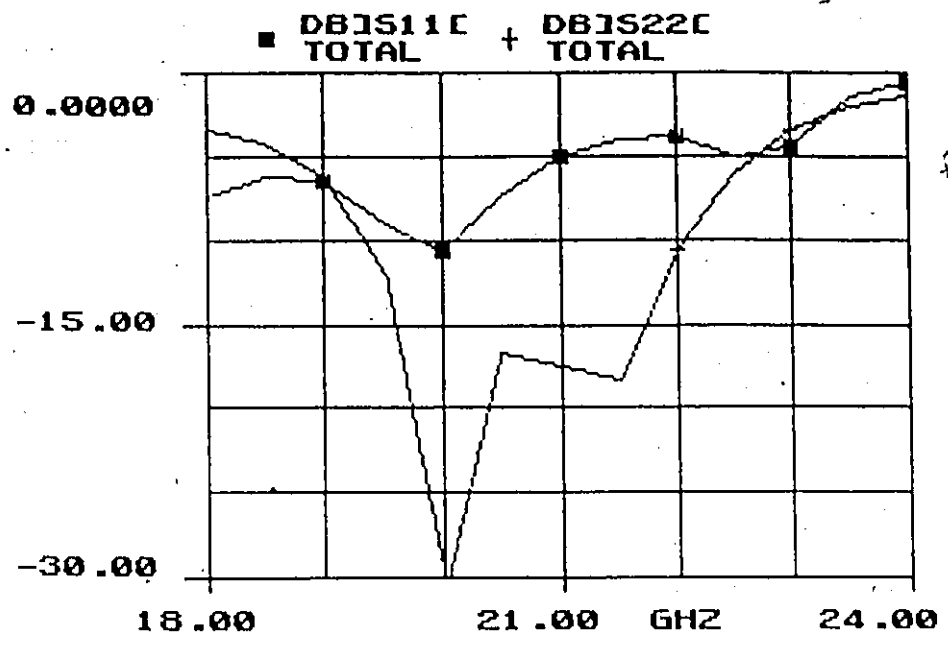
Figure 4-7 Analysis of Finline to Microstrip Transition

FREQ-GHZ	DB[S21] TRAN	DB[S11] TRAN
18.0000	-0.834	-0.225
18.5000	-0.460	-11.018
19.0000	-0.245	-14.558
19.5000	-0.135	-19.656
20.0000	-0.090	-27.212
20.5000	-0.091	-25.675
21.0000	-0.142	-18.597
21.5000	-0.250	-14.273
22.0000	-0.440	-11.236
22.5000	-0.765	-8.617
23.0000	-1.326	-6.309
23.5000	-2.317	-4.256
24.0000	-4.151	-2.507
24.5000	-7.892	-1.199
25.0000	-18.352	-0.600
25.5000	-12.529	-1.017
26.0000	-5.492	-2.708

Table 4-1 Analysis of Finline to Microstrip Transition

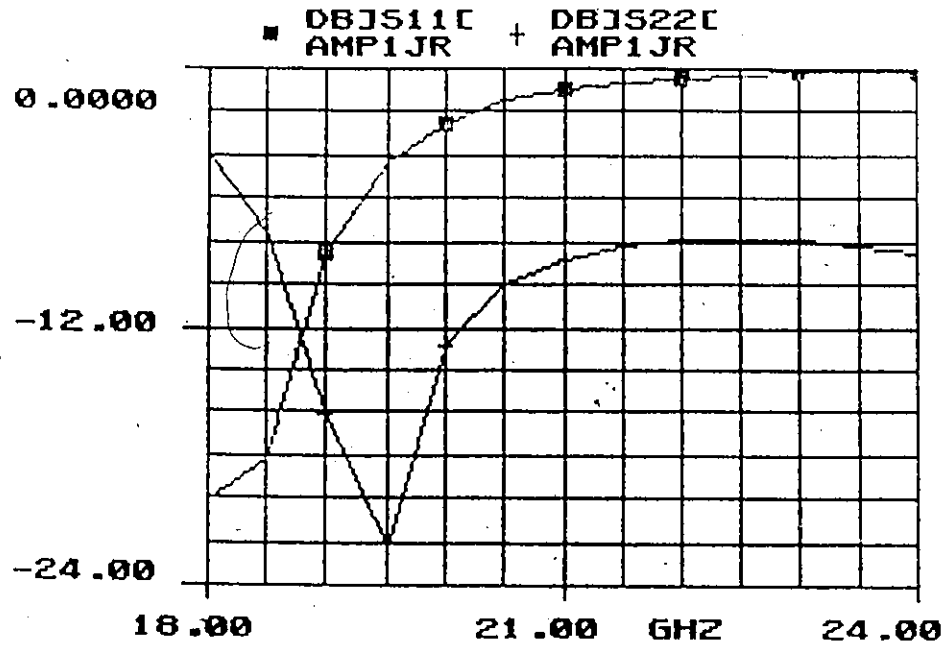
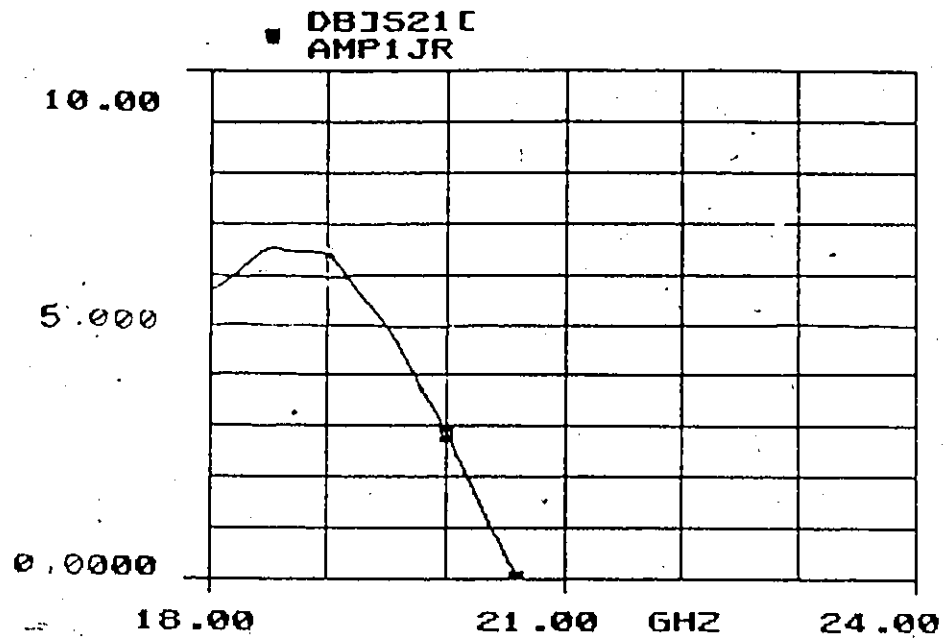
4.4 MATCHING NETWORK REALIZATION

The single stub matching network which was discussed in the previous chapter was realized using microstrip. To find the microstrip equivalent circuit of the transmission line elements discussed previously a computer program Linecalc [10] was used. The microstrip input matching network required an 81 mil long 50 ohm stub which was 2.6 mils from the input bonding wires. The output network required a 159 mil long stub located 204 mils from the output bond wires. A Touchstone file was written to analyze the amplifier separately from the transition and bias circuitry. The results of this analysis are shown in Figure 4-9. These results show that the center frequency of the amplifier is shifted down by about 500 MHz. This shift could be due to errors in reading the smith charts or the end effect of the stub. The input matching network described above is impossible to realize in practice due to the short distance required between the FET and the stub (2.6 mils). Since the width of the stub is 30 mils, the center of the stub must be located at a distance of at least 15 mils, therefore, the stub was moved to a distance of 15 mils from the FET. The analysis of the circuit was again performed to see the degradation due to moving the stub. These results are shown in Figure 4-10. There is a large degradation in performance due to shifting the stub. The gain is now only 3 dB at 20 GHz compared to the 6 dB previously attained.



FREQ-GHZ	DB(S21) TOTAL	DB(S11) TOTAL	DB(S22) TOTAL
18.0000	3.157	-7.522	-3.507
18.5000	3.755	-6.221	-4.315
19.0000	5.002	-6.514	-6.327
19.5000	6.009	-9.116	-12.096
20.0000	5.996	-10.622	-30.333
20.5000	4.985	-7.364	-16.666
21.0000	3.755	-5.086	-17.513
21.5000	2.695	-3.991	-18.282
22.0000	1.812	-3.836	-10.574
22.5000	0.912	-4.978	-6.048
23.0000	-1.890	-4.397	-3.370
23.5000	-0.890	-1.477	-2.059
24.0000	-17.420	-0.644	-1.451

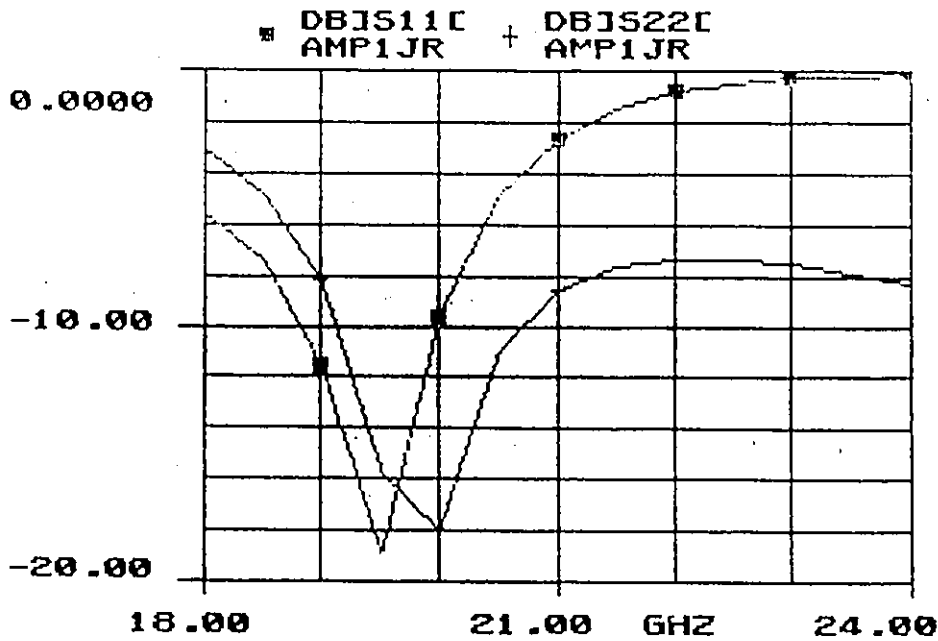
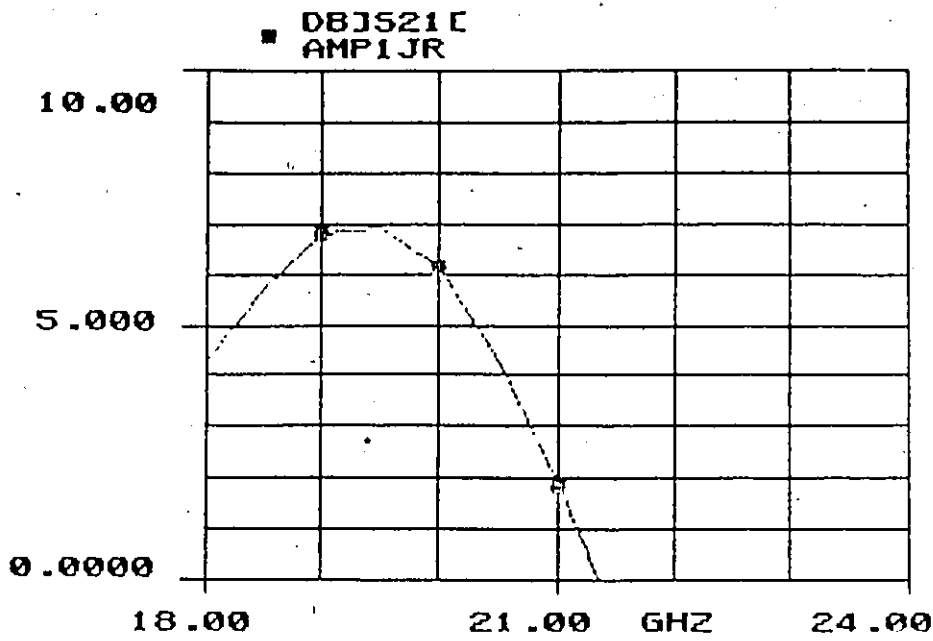
Figure 4-9 Amplifier Module Analysis using Touchstone



FREQ-GHZ	DB(S21) AMP1JR	DB(S11) AMP1JR	DB(S22) AMP1JR
18.0000	5.679	-20.147	-4.001
18.5000	6.430	-18.748	-7.611
19.0000	6.752	-8.490	-16.159
19.5000	4.970	-4.419	-22.131
20.0000	2.845	-2.510	-12.907
20.5000	0.443	-1.523	-10.049
21.0000	2.120	-0.986	-8.799
21.5000	-4.007	0.632	-8.705
22.0000	-7.648	0.424	-7.943
22.5000	-10.700	-0.294	-7.883
23.0000	-14.094	-0.214	-7.971
23.5000	-18.073	-0.186	-8.106
24.0000	-22.202	0.129	-8.315

Figure 4-10 Amplifier Module Analysis with Input Stub Shifted by 15 mils

The circuit was optimized over the range 19.5-20.5 GHz to yield optimum gain. The parameters which could vary were the input and output stub length and distance to the FET. A minimum distance of 15 mils from the FET was enforced. Touchstone was used to perform the optimization. The new stub lengths and positions were as follows: input matching stub was 64 mils long and 15 mils from the bond wires, output stub was 197 mils from the bond wires and 164 mils long. Also on the matching circuit is a quarter wave transformer which matches the 50 ohm amplifier to the 121 ohm microstrip used in the transition. The results of the new design are shown in Figure 4-11. Looking at the return loss curves we can see that the output is very well matched however the input return loss is only 10 dB due to the position of the stub. The gain curve shows 6 dB gain at 20 GHz. This optimized design was chosen as the one which would be fabricated.



FREQ-GHZ	DB[S21] AMP1JR	DB[S11] AMP1JR	DB[S22] AMP1JR
18.0000	4.300	-5.662	-3.142
18.5000	5.691	-7.419	-4.885
19.0000	6.747	-11.552	-8.237
19.5000	6.922	-18.917	-15.729
20.0000	6.080	-9.664	-18.046
20.5000	4.311	-4.912	-11.168
21.0000	1.893	-2.660	-8.634
21.5000	-0.906	-1.491	-7.663
22.0000	-3.968	-0.856	-7.358
22.5000	-7.286	-0.505	-7.369
23.0000	-10.951	-0.311	-7.555
23.5000	-15.189	-0.206	-7.861
24.0000	-20.559	-0.152	-8.266
24.5000	-29.039	-0.128	-8.755
25.0000	-43.074	-0.120	-9.297
25.5000	-28.867	-0.122	-9.600
26.0000	-25.164	-0.128	-10.209

Figure 4-11 Analysis of the Optimized Amplifier Module

4.5 PREDICTED PERFORMANCE OF THE COMPLETE CIRCUIT

Once all the sections of the complete circuit were analyzed separately, a complete circuit analysis was done using Touchstone. This circuit file is shown in Table 4-2. The results are shown in Figure 4-12. The complete amplifier analysis shows a gain of 6 dB at 20 GHz, an input return loss of 10 dB and output return loss of 30 dB. A noise analysis was done on the amplifier up to 18 GHz since noise data was not available above that frequency. The total amplifier noise figure was calculated to be 2.4 dB at 18 GHz. The noise figure should be only slightly higher at 20 GHz. Since the measurement equipment required to measure the noise figure of the amplifier was not available a comparison with actual measured noise figure could not be made.

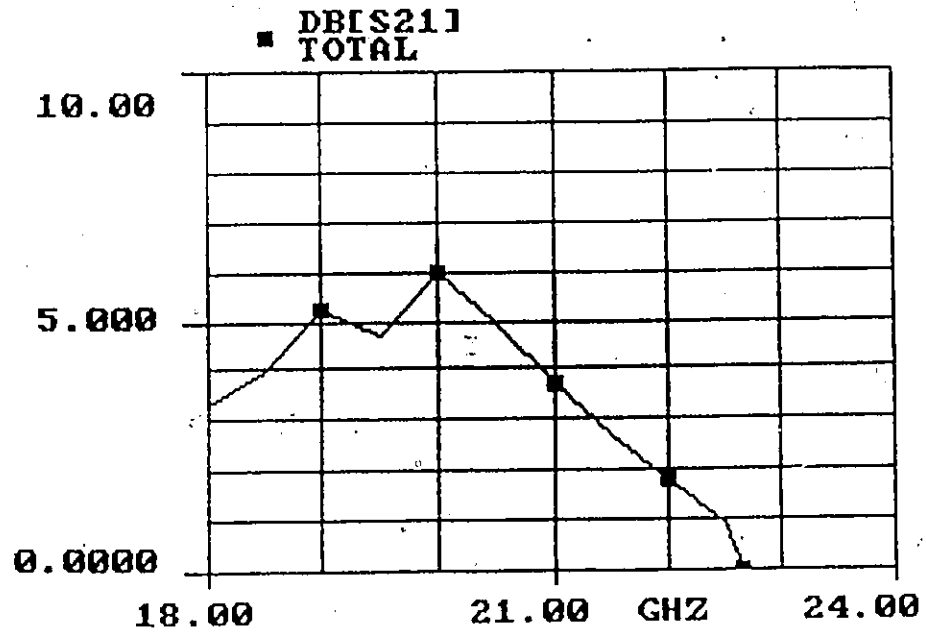
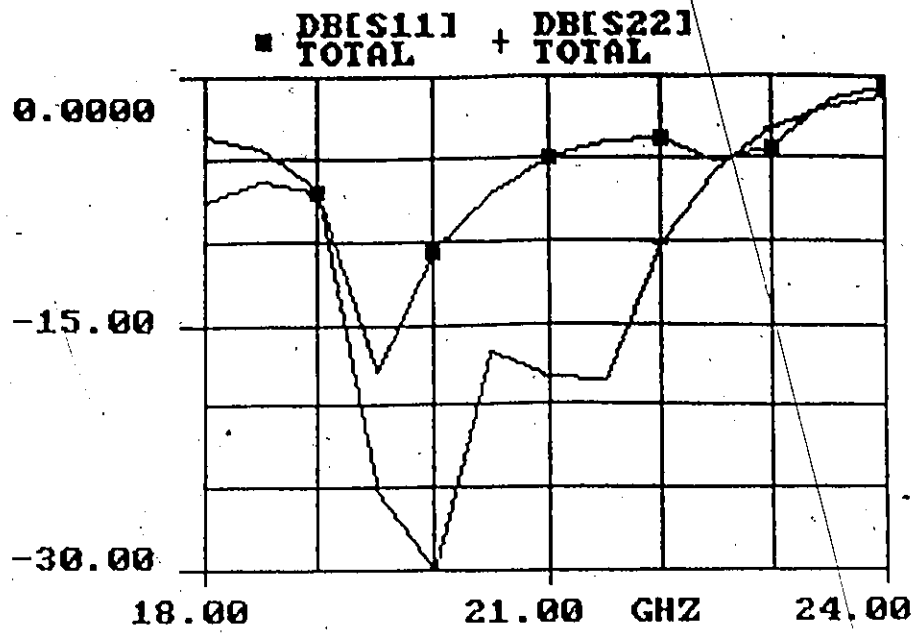
DIM
 FREQ GHZ
 RES OH
 IND NH
 CAP PF
 LNG MIL
 TIME PS
 COND /OH
 ANG DEG

CKT

MSUB ER=2.2 H=10 T=.67 RHO=1 RGH=0
 MLIN 15 1 W=14.7 L=109
 MLIN 1 2 W=30.6 L=100
 MCROB2 2 3 4 5 W1=30.6 W2=8.9 W3=30.6 W4=8.9
 MLEF 3 W=8.9 L=111
 MLEF 5 W=8.9 L=111
 MLIN 4 6 W=30.6 L=214
 MCROB2 6 7 8 9 W1=30.6 W2=8.9 W3=30.6 W4=8.9
 MLEF 7 W=8.9 L=111
 MLEF 9 W=8.9 L=111
 MLIN 8 10 W=30.6 L=100
 RES 10 11 R=50
 CAP 11 0 C=56
 DEF2P 15 10 BSFIL
 TLIN4 21 22 23 24 Z=131 E=90 F=20
 SHOR 23
 UNIT 23 24
 XFER 22 25 24 26 N=1.04
 SHOR 26
 TLSC 22 24 Z=131 E=90 F=20
 MLIN 25 27 W=5.6 L=112
 BSFIL 27 30
 MLIN 25 28 W=5.6 L=100
 MLIN 28 29 W=14.7 L=109
 DEF2P 21 29 TRAN
 MLIN 41 42 W=30.6 L=250
 MLEF 42 W=30.6 L=64
 MLIN 42 43 W=30.6 L=15
 IND 43 44 L=.2
 B2PA 44 45 0 B267300
 IND 45 46 L=.2
 MLIN 46 47 W=30.6 L=197
 MLEF 47 W=30.6 L=164
 MLIN 47 48 W=30.6 L=250
 DEF2P 41 48 AMP
 TRAN 50 51
 AMP 51 52
 TRAN 53 52
 DEF2P 50 53 TOTAL
 TERM
 TOTAL .447 0 .447 0
 OUT

TOTAL DB(S21) GR1
 TOTAL DB(S11) GR2
 TOTAL DB(S22) GR2
 FREQ
 SWEEP 18 24 .5
 GRID
 RANGE 18 24 1
 GR1 0 10 1
 GR2 0 -30 5
 OPT
 RANGE 19.5 20.5
 TOTAL DB(S21)=6.8

Table 4-2 Touchstone Amplifier Circuit File



FREQ. GHZ	DBIS211 TOTAL	DBIS111 TOTAL	DBIS221 TOTAL
18.0000	3.811	-7.005	3.579
18.5000	3.953	-6.411	4.400
19.0000	5.240	-6.977	6.777
19.5000	4.702	-17.868	25.134
20.0000	5.969	-10.689	30.071
20.5000	4.950	-7.259	10.791
21.0000	3.720	-5.013	-10.334
21.5000	3.668	3.949	10.440
22.0000	1.736	-3.858	10.191
22.5000	0.908	-5.234	-5.761
23.0000	-2.175	-4.377	3.130
23.5000	-9.725	-1.368	1.809
24.0000	-13.785	-0.611	1.797

Figure 4-12 Analysis of Complete Amplifier

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CHAPTER V

RESULTS

The amplifier circuit described in the previous chapter was fabricated and integrated into a brass housing, the drawings of which are shown in the appendix. The waveguide input and output were WR-42 (K band), which has a specified frequency range of 18 - 26.5 GHz. The housing had pockets milled out of the top half to allow easy tuning of the matching network. As stated previously, the circuit was fabricated on .010" RT Duroid 5880 material. In the center of the circuit a small slot .020" x .200" was cut out of the duroid. This was accurately done on an Aristomat machine at Shaw Photogrammetrics in Nepean. Beneath this slot a kovar tab was silver epoxied to the ground plane. The FET was epoxied to this so that the source could be bonded directly to the kovar tab. This configuration provided a good ground connection. The bonding of the FET chip onto the circuit was done in the Space Electronics labs at the Communication Research Center. All microwave tests were done on the HP 8510 network analyzer at Bolriet Technologies Inc. in Carleton Place. Figure 5-1 shows the measured results of the amplifier before any additional tuning is done.

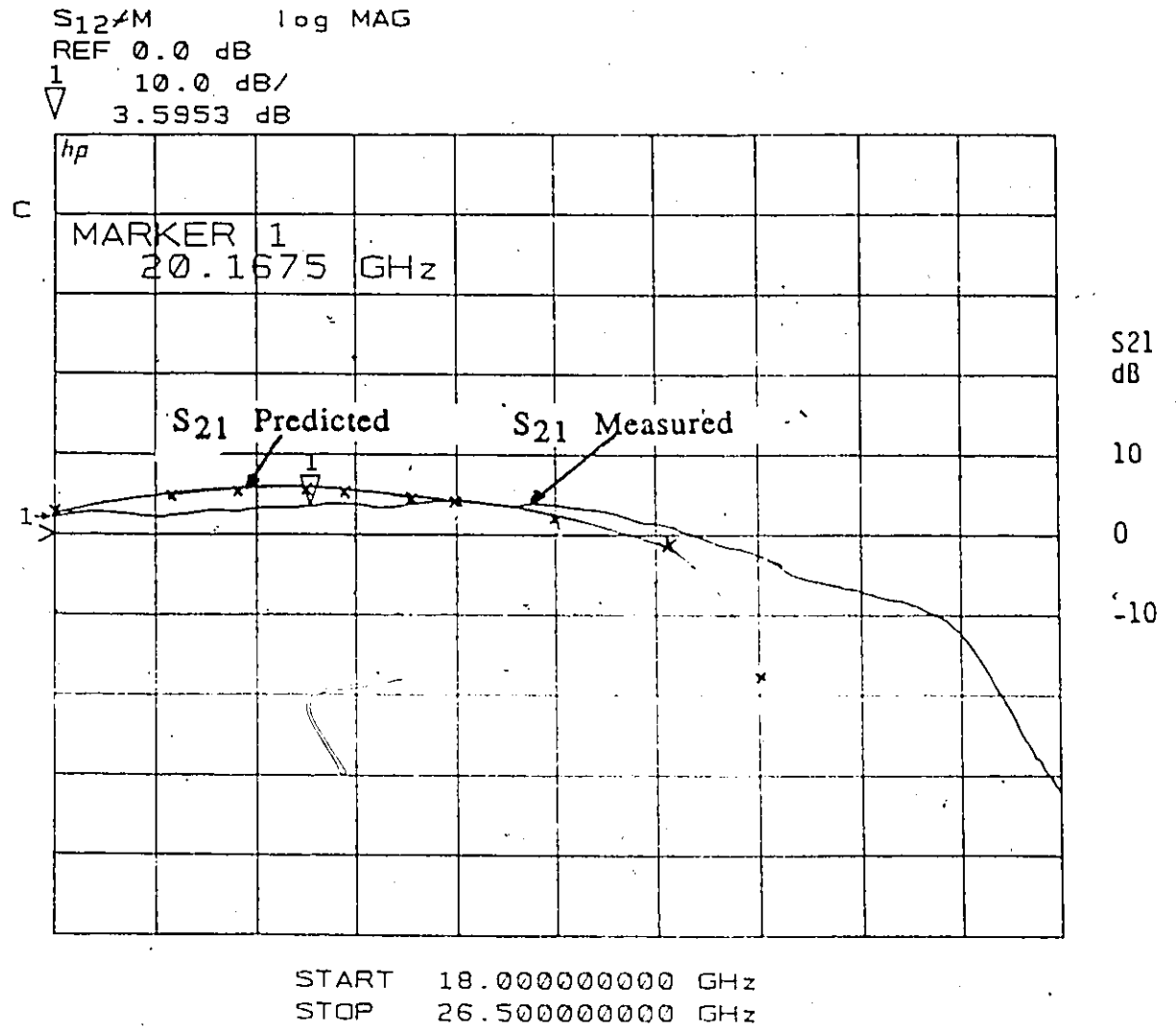


Figure 5-1 Amplifier Results Before Tuning

The FET drain voltage was 3V and drain to source current 20 mA. The results show 3.6 dB gain at 20 GHz, 12 dB input return loss, and 15 dB output return loss. This measurement includes the loss due to the two transitions, so the actual amplifier gain is closer to 5 dB. The amplifier provides gain up to approximately 23.4 GHz where the gain curves fall below the 0 dB line. Also shown in this figure is the predicted gain. The predicted gain tends to fall off much more rapidly than the measured gain. This signifies that the optimum match for maximum gain has not been realized. For example, to design a broadband amplifier, one must tradeoff gain for bandwidth. An attempt was made at tuning the amplifier for optimum match using small pieces of copper foil. It was found that three small pieces were sufficient. A small piece was used to lengthen both the input and output stub. It may be necessary to lengthen the stubs to correct for errors in the open ended microstrip model used in Touchstone. Itoh [1] investigated the effect of dispersion on Δl (increase in length due to capacitive effect). He found that Δl is much smaller at small wavelengths than that computed by quasistatic methods. Since Touchstone uses a quasistatic model for the end effect it is possible that in the optimization process the program kept the stubs shorter than necessary to counter the apparent increase in electrical length. In the book on C.A.D. of microwave circuits by Gupta, Garg and Chadha [2], the authors say that quasistatic models are only good up to about 10 GHz. The third tuning stub used was approximately 80 mils long and 80 mils from the FET. A comparison was made of the input

reflection of this new circuit compared to the initially designed circuit. The initial circuit had an S_{11} of $.49 \angle -156$. The tuned circuit had an S_{11} of $.60 \angle -170$. These points are shown on the Smith chart in Figure 5-2. As one can see from this figure the points are quite close to each other. This slight difference in reflection coefficients could be due to errors in the initial S-parameters taken for the FET since they can vary from lot to lot. Also the FET used in this amplifier was run at a slightly different bias point than that FET used to measure the S-parameters.

Figure 5-3 shows the measured and predicted gain of the tuned amplifier. The amplifier shows a gain of 6.7 dB at 20 GHz. This measurement also includes losses due to the transition so that the actual amplifier circuit gain is approximately 1.5 dB higher. The amplifier has greater than 6 dB gain over a 1.2 GHz bandwidth. The return loss is shown in Figure 5-4. The output return loss is -30 dB and the input return loss is -13 dB at 20 GHz. The output was expected to have a better return loss than the input since as was discussed in the previous chapter the input could not be optimally matched due to the optimum location of the open circuited stub. Figure 5-5 shows the isolation between the output and input of the amplifier. The isolation is 17 dB at 20 GHz. Figure 5-6 shows the amplifier gain as a function of bias conditions (drain voltage and drain-source current). The bias point 3V 10 ma gives the lowest gain in this figure, however those bias conditions would yield a better noise figure than the higher gain bias of 4V 20 ma since this amplifier was designed to have maximum gain 4V 20 ma was chosen as the bias point.

There are a number of typical amplifier specifications which were not measured such as noise figure, harmonic content of the output and gain compression. This was due to the unavailability of test equipment.

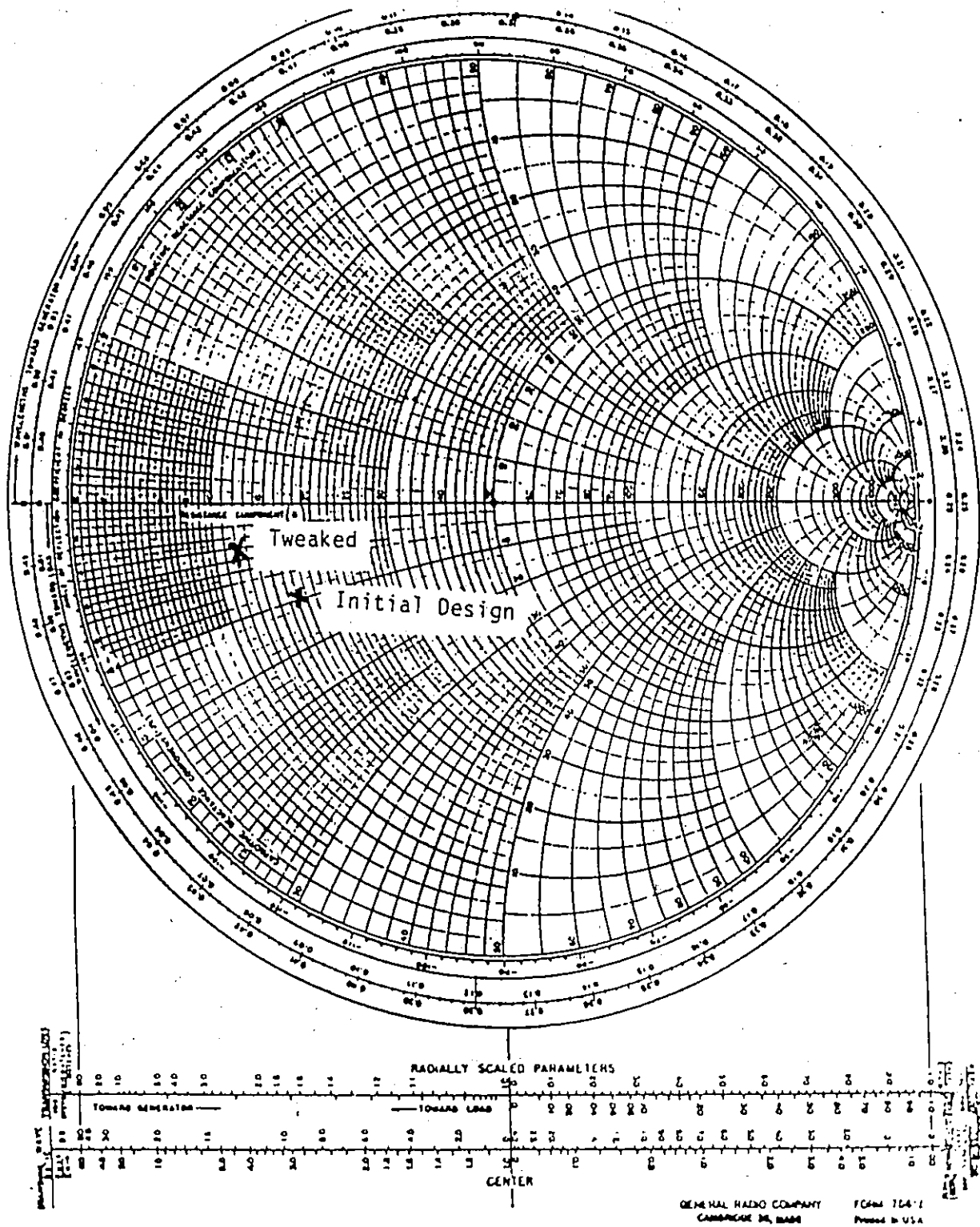


Figure 5-2 Design and Tweaked Input Reflection Coefficient

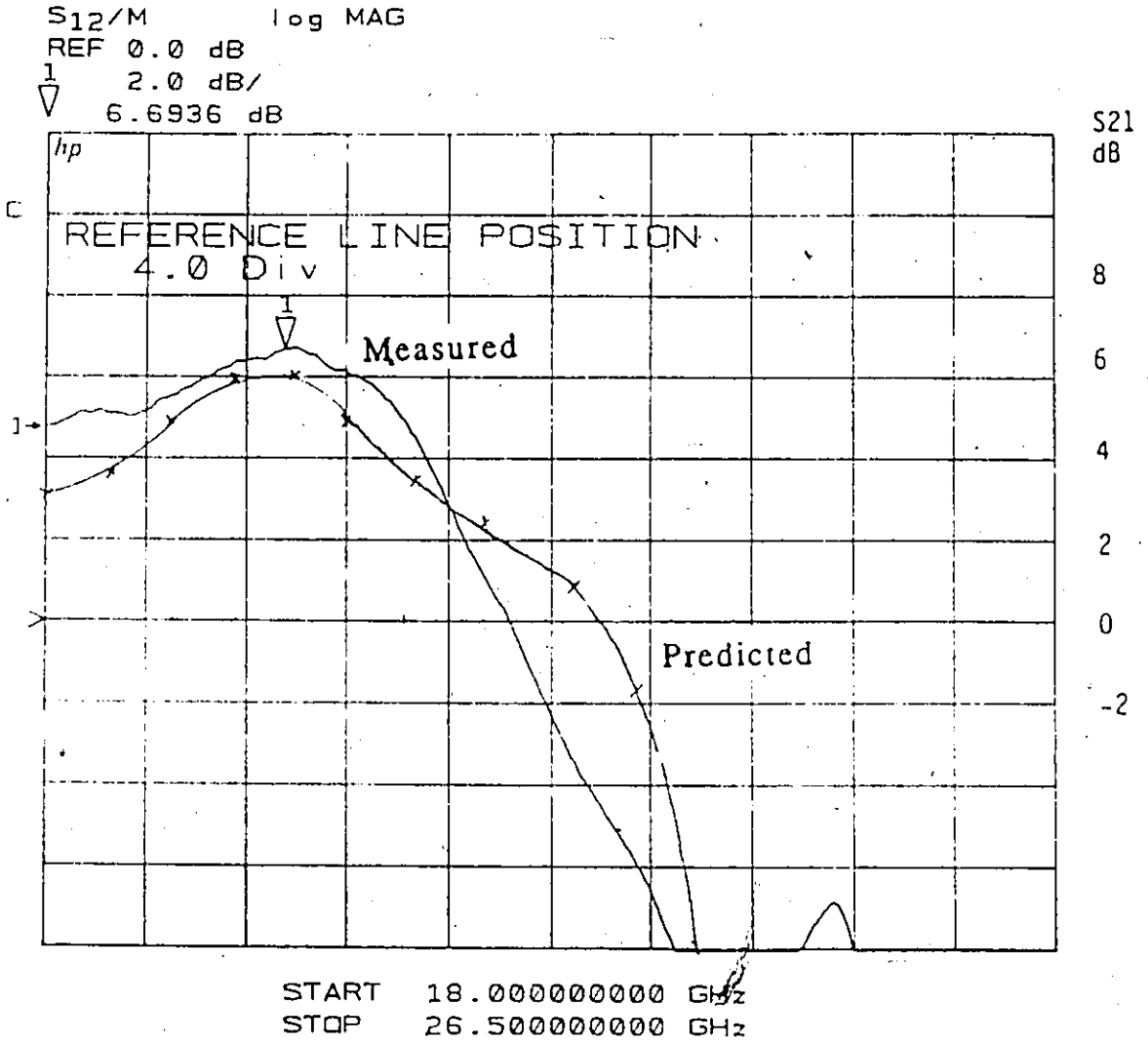


Figure 5-3 Measured and Predicted Gain of Tuned Amplifier

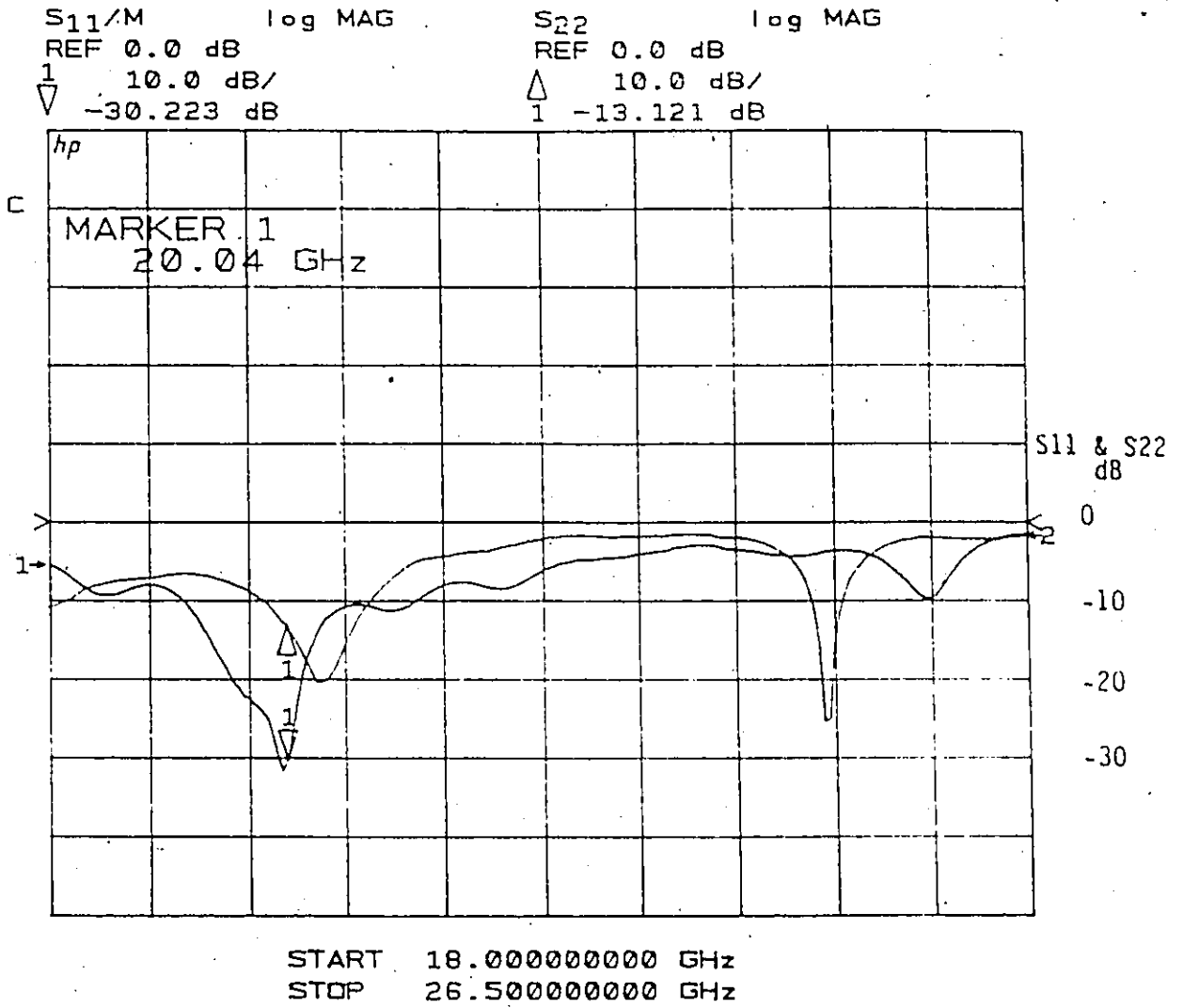


Figure 5-4 Measured Return Loss of Tuned Amplifier



REF 0.0 dB
1 10.0 dB/
▽ -17.381 dB

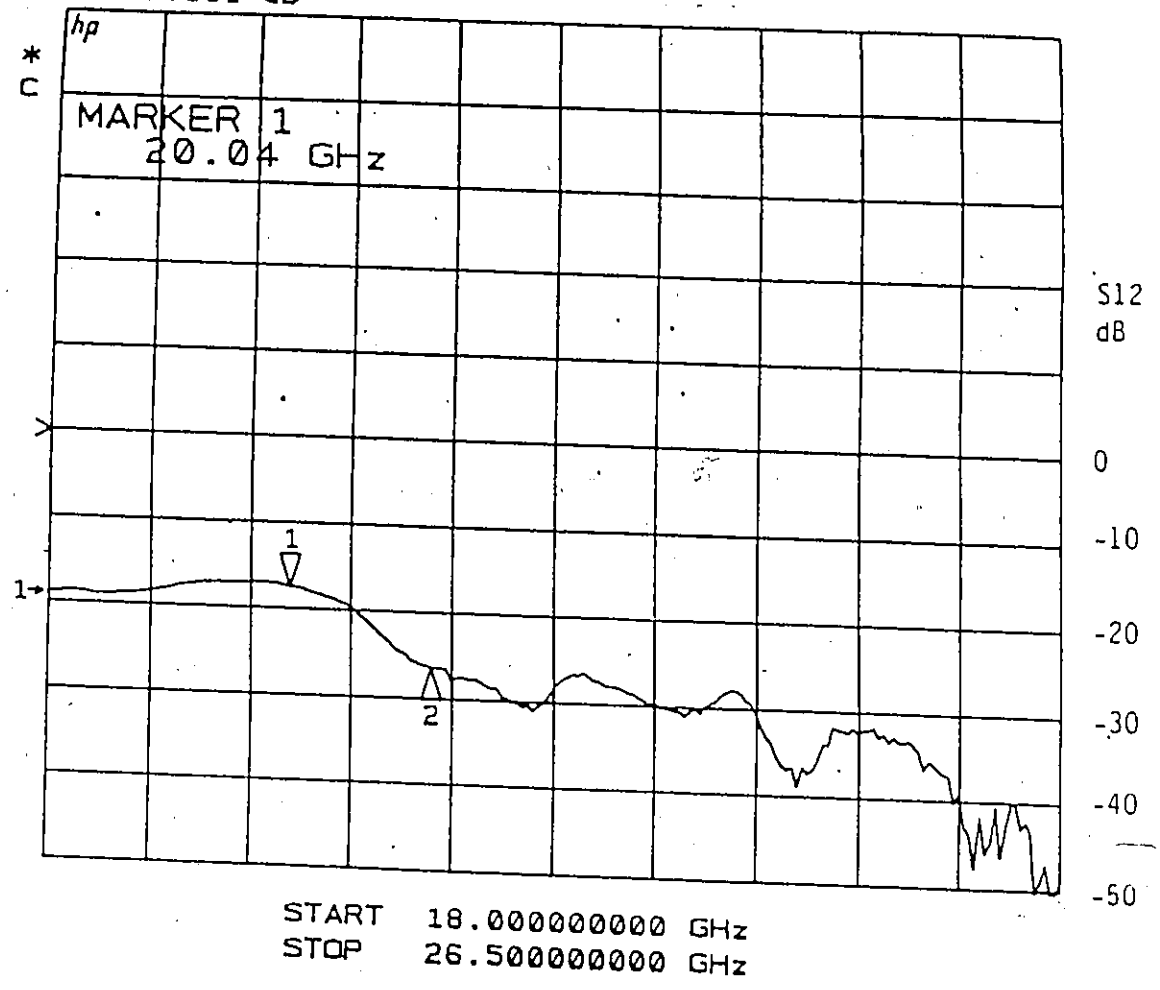


Figure 5-5 Isolation Between Input and Output

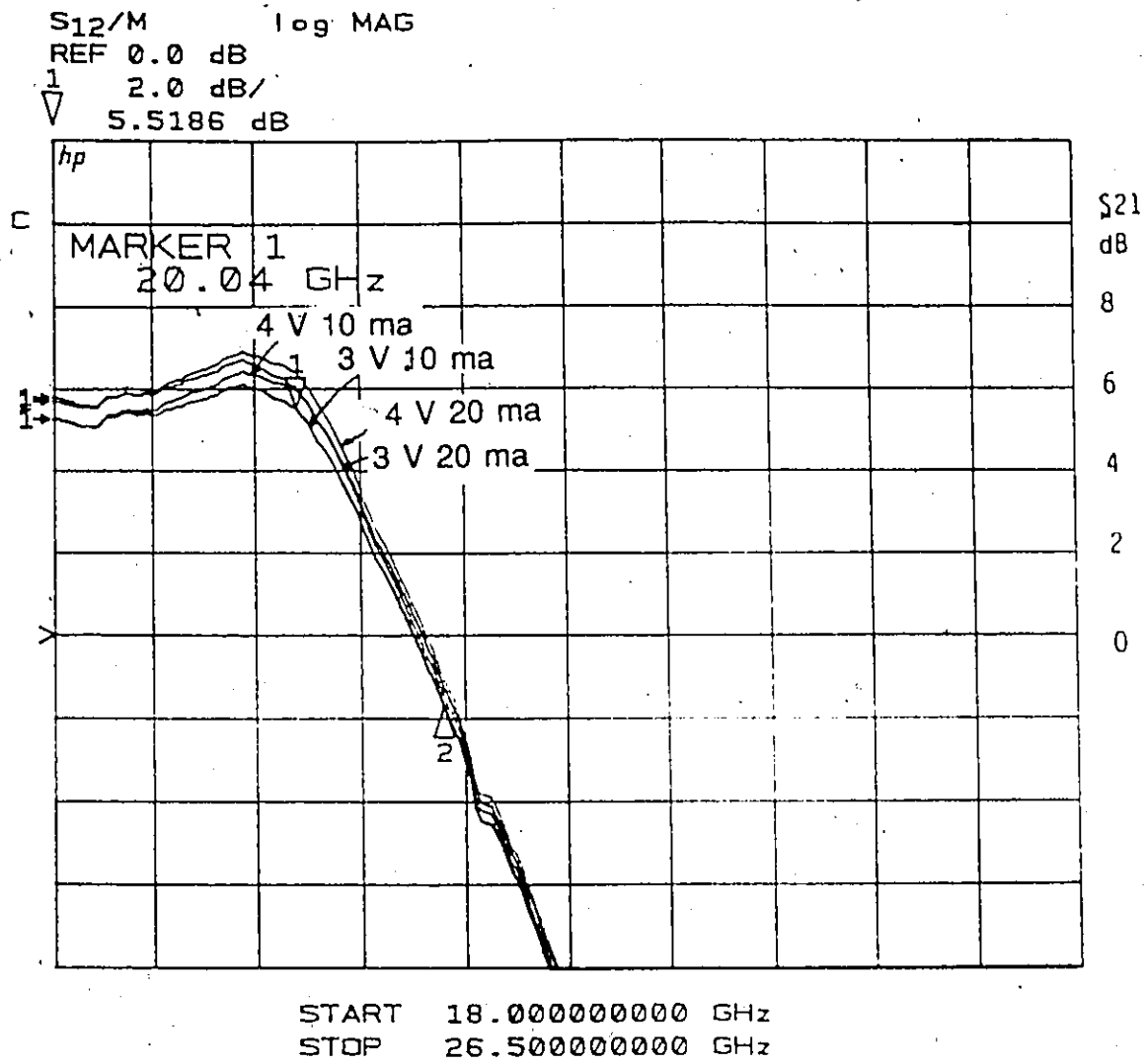


Figure 5-6 Measured Amplifier Gain vs. Drain Bias

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CHAPTER VI

FINLINE ANALYSIS USING TRANSVERSE RESONANCE METHOD

6.1 INTRODUCTION

Although a spectral domain program for analyzing unilateral finline was available for the design of this amplifier, it was found that the program suffered from convergence problems as the slot width became narrow. The mode matching technique as described by Vahldieck and Hofer [1], when used to analyze finline, also shows convergence problems for narrow gaps. Since the design of this amplifier required very narrow gaps in order to achieve the low impedances necessary to realize the finline to microstrip transition, another method of analysis which does not suffer from convergence problems was required. It was found that the transverse resonance solution provides rapid and reliable data for finlines with narrow gap widths. The effect of metallization thickness was included in the solution since this parameter has an increasing effect as the gap between the fins becomes increasingly narrow.

The transverse resonance analysis which was performed in this study is similar to that used by Cohn for the study of slotline characteristics [2]. Hofer also used the transverse resonance technique to study finline characteristics [3], however his derived expressions required a correction factor and did not include the effect of finite metallization thickness.

6.2 FORMULATION OF EQUATIONS

Figure 6-1 shows the finline resonator analyzed in this study. At the lowest resonance of the dominant finline mode, the length of that cavity is $\lambda_g/2$. Figure 6-2 shows a cross section of the resonator and its equivalent transverse network. Y_0 , Y_1 , Y_2 and Y_3 are the $TE_{1,0}$ mode to x characteristic admittances of a rectangular waveguide with an 'a' dimension of $\lambda_g/2$. The $TE_{1,0}$ mode characteristic admittance of a rectangular waveguide can be expressed as:

$$Y_{TE} = \frac{ay}{j2b\eta k} \quad (6-1)$$

where 'a' and 'b' are the guide dimensions and the other parameters are defined as follows:

For the air filled regions:

$$\gamma_a = k_a v \quad (6-2)$$

$$k_a = \frac{2\pi}{\lambda} \quad (6-3)$$

$$\eta_a = \sqrt{\frac{\mu_0}{\epsilon_0}} \quad (6-4)$$

$$v = \sqrt{\epsilon_{eff} - 1} \quad \epsilon_{eff} > 1 \quad (6-5)$$

$$v = j\sqrt{1 - \epsilon_{eff}} \quad \epsilon_{eff} < 1 \quad (6-6)$$

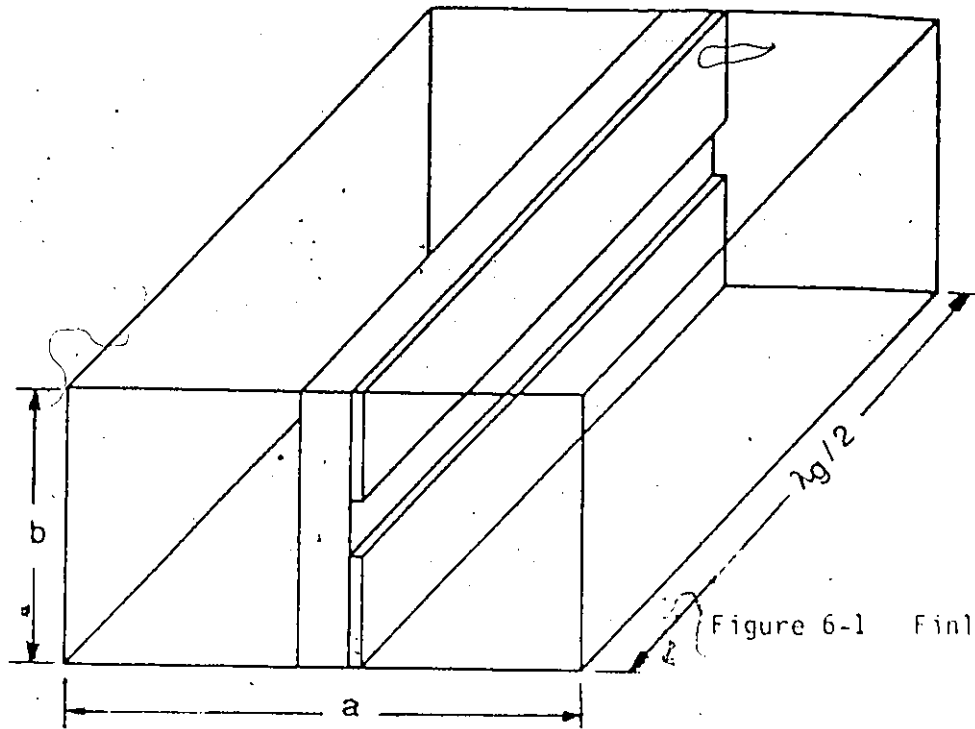


Figure 6-1 Finline Resonator

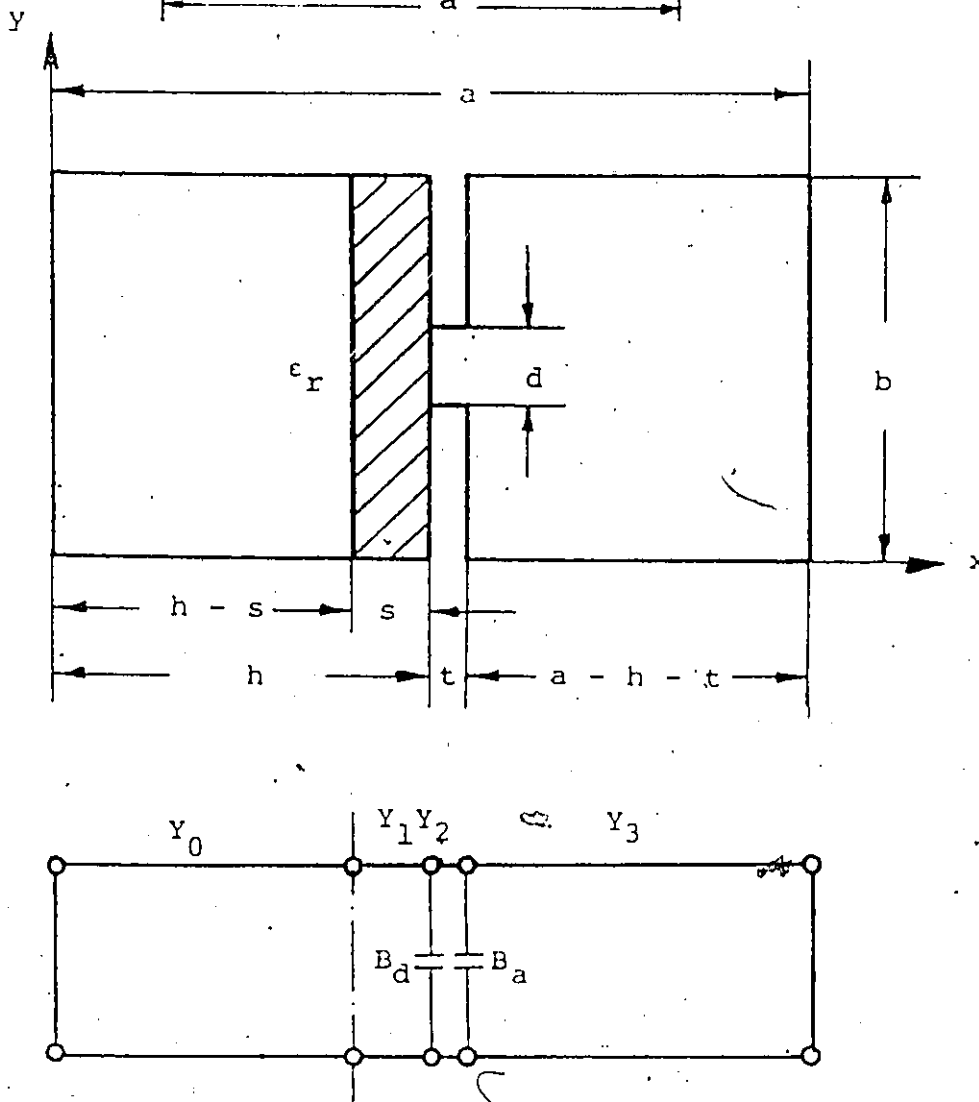


Figure 6-2 Equivalent Transverse Network

For the dielectric filled regions :

$$\gamma_d = k_d u \quad (6-7)$$

$$k_d = \frac{2\pi\sqrt{\epsilon_r}}{\lambda} \quad (6-8)$$

$$\eta_d = \frac{\eta_a}{\sqrt{\epsilon_r}} \quad (6-9)$$

$$v = \sqrt{\epsilon_r - \epsilon_{eff}} \quad (6-10)$$

Since the 'a' dimensions of the cavity is $\lambda_g/2$ and $\lambda_g = \lambda/\sqrt{\epsilon_{eff}} = \lambda/p$, 'a' can be replaced by $\lambda/2p$ in the above equation for Y_{TE} so that:

$$Y_0 = \frac{v\lambda}{j4bp\eta} = Y_3 \quad (6-11)$$

$$Y_1 = \frac{u\lambda}{4bp\eta} \quad (6-12)$$

$$Y_2 = \frac{v\lambda}{j4d\eta} \quad (6-13)$$

In Figure 6-2, B_d is the stray susceptance at the metallization - dielectric interface. B_a is the stray susceptance at the metallization - air interface. Expressions for these values were derived from Cohn's [2] paper and are as follows for $\epsilon_{eff} > 1$:

$$B_d = \sum_{1,2 \dots} \left\{ \frac{\epsilon_r \tanh r_n - p^2 F_{n1}^2 \coth q_n}{\left(1 + \left(\frac{bp}{n\lambda}\right)^2\right) F_{n1}} \cdot u^2 \right\} \left(\frac{\sin^2 n\pi\delta}{n(n\pi\delta)^2} \right) \quad (6-14)$$

$$B_a = \frac{1}{2p\eta} \sum_{1,2 \dots} \left\{ \frac{v^2 \left(1 - \frac{1}{F_n}\right) (\sin^2 n\pi\delta)}{n(n\pi\delta)^2} \right\} \quad (6-15)$$

where :

$$F_{n1} = \frac{b\gamma_{n1}}{2n\pi} \quad (6-16)$$

$$\gamma_{n1} = \frac{2n\pi}{b} \sqrt{1 - \left(\frac{bu}{n\lambda}\right)^2} \quad (6-17)$$

$$F_n = \frac{b\gamma_n}{2n\pi} \quad (6-18)$$

$$\gamma_n = \frac{2n\pi}{b} \sqrt{1 + \left(\frac{bv}{n\lambda}\right)^2} \quad (6-19)$$

$$r_n = \gamma_{n1} s + \tanh^{-1} \frac{\gamma_{n1}}{\epsilon_r \gamma_n} \quad (6-20)$$

$$q_n = \gamma_n s + \coth^{-1} \frac{\gamma_n}{\gamma_{n1}} \quad (6-21)$$

$$p = \sqrt{\epsilon_{\text{eff}}} \quad (6-22)$$

$$\delta = \frac{d}{b} \quad (6-23)$$

In the above equations v is replaced by jv for $\epsilon_{\text{eff}} < 1$ Cohn [2] limits the validity of the above equations to $d/b \leq 0.14$, $d \leq s$ and $s \leq \lambda/4\sqrt{\epsilon_r}$.

The transverse resonance condition can now be derived from Figure 6-2 by setting the sum of admittances seen at the interface between the metallization and the dielectric equal to zero.

Y_0' is the admittance seen looking to the left at the plane of the air - dielectric interface. This is a short circuit transformed a distance $l_0 = h-s$ within a medium with a propagation constant $\beta_0 = -j2v\pi/\lambda$. Therefore Y_0' becomes:

$$Y_0' = -jY_0 \cotan \frac{-j2v(h-s)\pi}{\lambda} \quad (6-24)$$

In order to transform this admittance through the dielectric region we can set:

$$-jY_0 \cotan \frac{-j2v(h-s)\pi}{\lambda} = -jY_1 \cotan \beta_1 l_0' \quad (6-25)$$

and solve for $\beta_1 l_0'$.

$$\beta_1 l_0' = \tan^{-1} \left\{ \frac{-jY_1}{Y_0} \tanh \frac{-j2v(h-s)\pi}{\lambda} \right\} \quad (6-26)$$

Y_1' is the admittance seen looking to the left at the metallization - dielectric interface.

$$Y_1' = -jY_1 \cotan(\beta_1 l_1 + \beta_1 l_0') \quad (6-27)$$

After some substitutions the above equation becomes:

$$Y_1' = \frac{-ju\lambda}{4bp\eta} \cotan \left\{ \frac{2su\pi}{\lambda} + \tan^{-1} \left[\frac{u}{v} \tanh \frac{2v\pi(h-s)}{\lambda} \right] \right\} \quad (6-28)$$

Transforming the short circuit from the right and adding the susceptance B_a yields at the plane of the metallization - dielectric interface, when looking towards the right:

$$Y_2' = \frac{-jv\lambda}{4dp\eta} \cotanh \left\{ \frac{2vt\pi}{\lambda} + \cotanh^{-1} \left[\frac{4dp}{v\lambda} \left(\frac{v\lambda}{4bp} \cotanh \frac{2v\pi(a-h-t)}{\lambda} - \eta\beta_a \right) \right] \right\} \quad (6-29)$$

When $\epsilon_{\text{eff}} < 1$ the above equations become:

$$Y_1' = \frac{-ju\lambda}{4bp\eta} \cotan \left\{ \frac{2su\pi}{\lambda} + \tan^{-1} \left[\frac{u}{v} \tan \frac{2v\pi(h-s)}{\lambda} \right] \right\} \quad (6-30)$$

$$Y_2' = \frac{-jv\lambda}{4dp\eta} \cotan \left\{ \frac{2vt\pi}{\lambda} + \cotan^{-1} \left[\frac{4dp}{v\lambda} \left(\frac{v\lambda}{4bp} \cotan \frac{2v\pi(a-h-t)}{\lambda} - \eta\beta_a \right) \right] \right\} \quad (6-31)$$

Setting the sum of admittances at the plane of the metallization - dielectric interface equal to zero yields:

$$Y_1' + Y_2' + jB_d = 0 \quad (6-32)$$

6.3 CALCULATION OF EFFECTIVE DIELECTRIC CONSTANT

These equations were programmed on a computer and solved to yield ϵ_{eff} using a root finding routine. The effect of various finline dimensions on ϵ_{eff} is shown in Figures 6-3, 6-4, and 6-5. Figure 6-3 shows the effect of metallization thickness and gap width on ϵ_{eff} at the center of the waveguide band. From the graph we can see that for a 0.0 micron metallization thickness, ϵ_{eff} increases as the gap between the fins decreases. This occurs because as the distance between the fins decreases, a greater part of the electric field becomes concentrated in the dielectric, thus raising the effective dielectric constant. However, when the effect of metallization is included, there is a point when ϵ_{eff} begins to decrease again. This is a phenomenon which has not yet been clearly explained. Indeed, as the gap becomes very narrow, the fins begin to behave as a parallel plate waveguide due to the finite metallization. This, in turn, assures that a large part of the electromagnetic energy travels within the air-space between the fins, thus reducing ϵ_{eff} . The phenomenon becomes more pronounced as the gap width decreases and the metallization thickness increases. This graph also illustrates that metallization thickness has less effect on the calculations of ϵ_{eff} as the gap width increases.

Figure 6-4 shows the effect of frequency and metallization thickness on ϵ_{eff} . As the frequency is increased the field becomes more concentrated in the dielectric and, as a result, ϵ_{eff} increases.

Figure 6-5 shows the effect of metallization thickness and ϵ_r on ϵ_{eff} . For the case shown, ϵ_{eff} decreases with increasing metallization thickness since the electric field becomes more concentrated in the air gap between the fins. There are however other cases as described by Vahldieck and Hofer [1] in which ϵ_{eff} will increase with increasing metallization thickness. This occurs predominantly at low frequencies when less field is concentrated in the dielectric than in the air and the finline behaves as a ridged waveguide, so that the propagation constant increases as the fin becomes wider.

WR(42) waveguide, $s=0.381$ mm, $f=226$ Hz, $\epsilon_r=2.2$

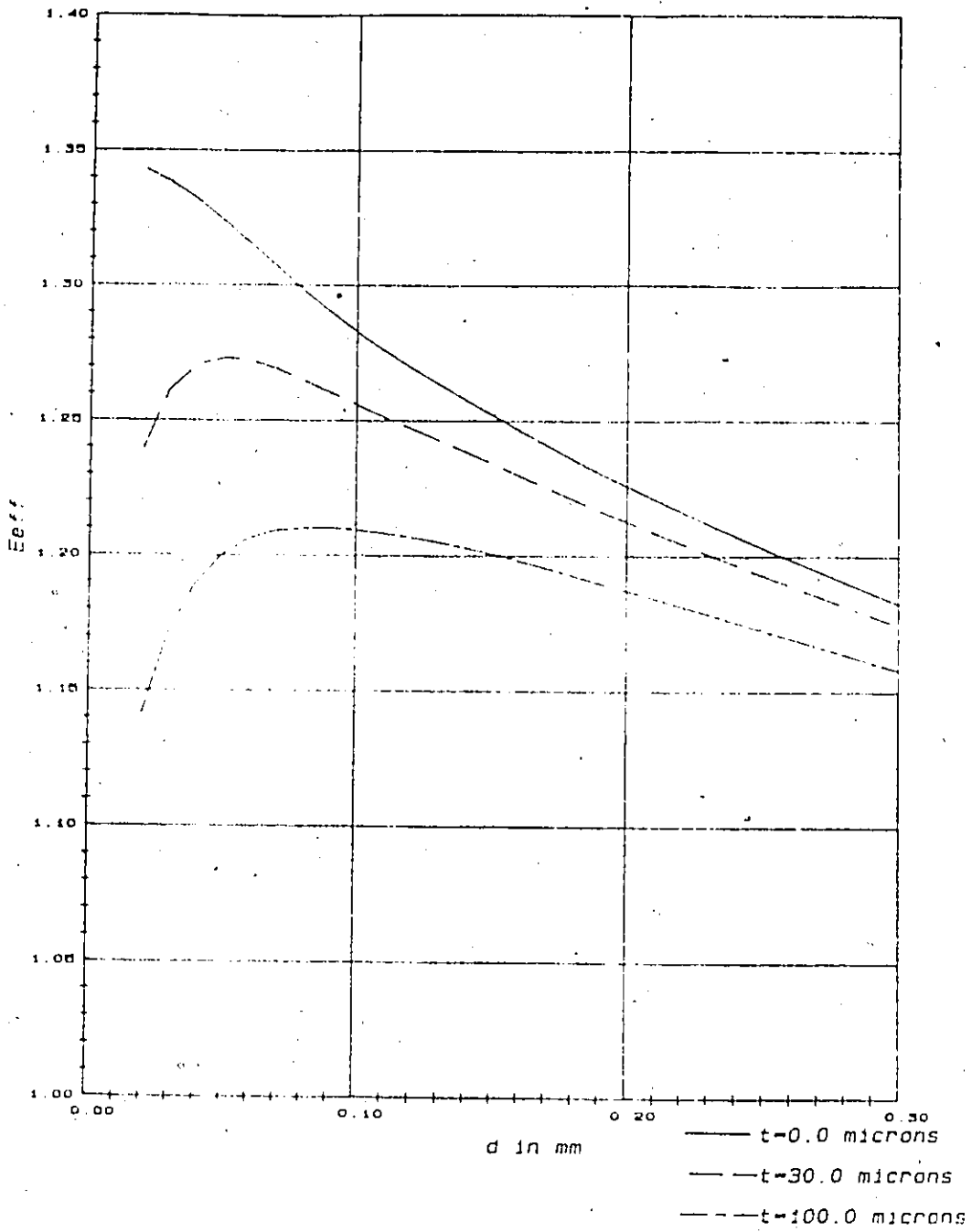


Figure 6-3 E_{eff} vs Gap Width

WR(42) waveguide, $s=.381$ mm, $d=.1$ mm, $\epsilon_r=2.2$

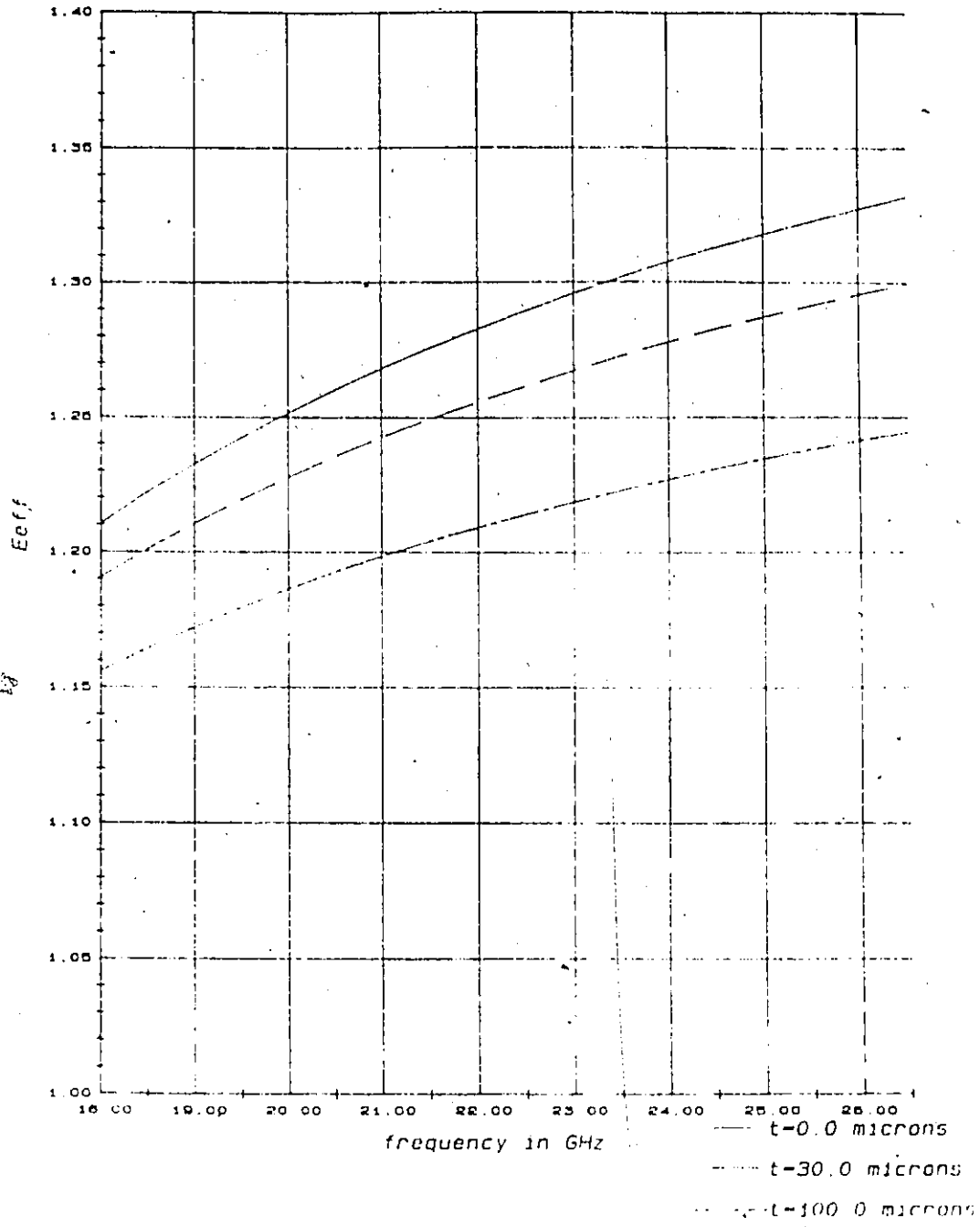


Figure 6-4 E_{eff} vs Frequency

WR(42) waveguide, $s=0.381$ mm, $d=0.1$ mm, $f=22$ GHz

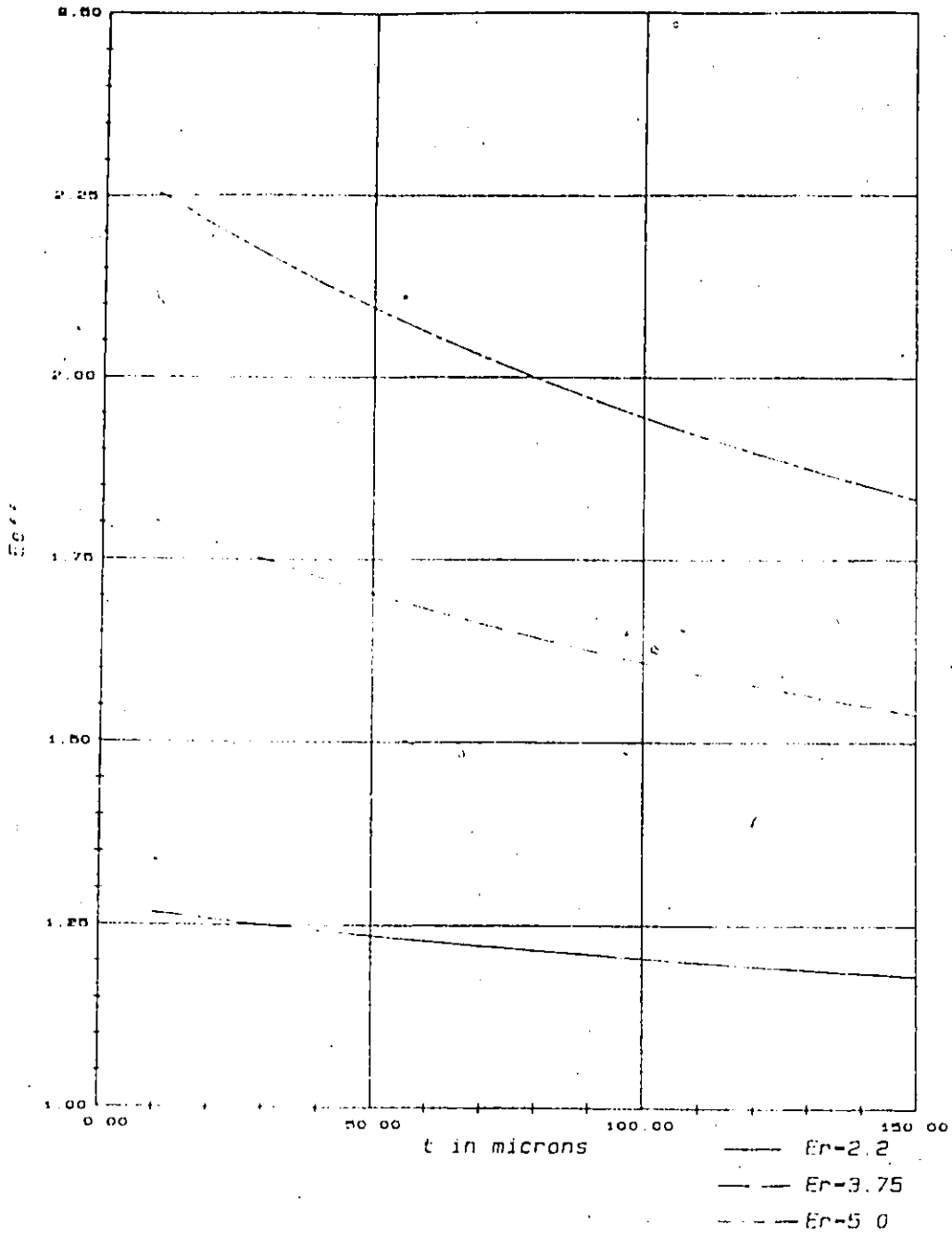


Figure b-5 E_{eff} vs Metallization Thickness

6.4 CALCULATION OF CHARACTERISTIC IMPEDANCE

Using results from the above transverse resonance program one can calculate Z_0 based on Meier's [4] approximate expression. The characteristic impedance of a finline can be calculated as:

$$Z_0 = \frac{Z_{0\infty}}{\sqrt{\epsilon_{\text{eff}}}} \quad (6-33)$$

In the above expression, $Z_{0\infty}$ is the characteristic impedance at infinite frequency of a ridge loaded guide with the same dimensions as the finline. The following expression, which is based on the power voltage definition of impedance was taken from Hofer's Finline Design Manual [5]:

$$Z_{0\infty} = \frac{120\text{db}\pi^2}{b\lambda_{\text{cr}}} \frac{\frac{2d}{\lambda_{\text{cr}}} \cos^2\left(\frac{s\pi}{\lambda_{\text{cr}}}\right) \text{ncsc} \left[\frac{d\pi}{2b} + \frac{s\pi}{2\lambda_{\text{cr}}} + \frac{1}{4} \sin \frac{2s\pi}{\lambda_{\text{cr}}} \right] \left[\frac{\frac{d}{b} \cos^2 \frac{s\pi}{\lambda_{\text{cr}}}}{\sin^2 \frac{(a-s)\pi}{\lambda_{\text{cr}}}} \right] \left[\frac{(a-s)\pi}{2\lambda_{\text{cr}}} - \frac{1}{4} \sin \frac{2\pi(a-s)}{\lambda_{\text{cr}}} \right]}{(6-34)}$$

In the above expression λ_{cr} is the cutoff wavelength of a ridged waveguide with the same dimensions as the fins. The expression for λ_{cr} is taken from a paper by Hofer and Burton [6] which describes

closed form expressions for ridged waveguides. The expression for λ_{cr} is as follows:

$$\lambda_{cr} = 2(a - t) \sqrt{1 + \left(1 + \frac{.2\sqrt{b}}{a-t}\right) \frac{4b}{(a-t)\pi} \operatorname{Incsc} \frac{d\pi}{2b} + \left(2.45 + \frac{.2t}{a}\right) \frac{tb}{d(a-t)}}$$

(6-35)

Using the above equations, the effect of various finline parameters on the characteristic impedance was examined. Some results are presented in Figures 6-6, 6-7 and 6-8. Figure 6-6 shows the effect of the gap width and metallization thickness on Z_0 . This graph shows how the impedance decreases with decreasing gap width. As well, one can see the increasing effect of metallization thickness as the gap becomes narrow. Figure 6-7 shows that there is a decrease in characteristic impedance as the metallization is increased. This occurs because $Z_{0\infty}$ decreases more rapidly than $\sqrt{\epsilon_{eff}}$ with increasing metallization. Figure 6-8 shows that the characteristic impedance is relatively constant with frequency over a waveguide band. Z_0 becomes more dependent on frequency however at frequencies close to cutoff since ϵ_{eff} approaches zero.

Z₀ vs gap width
 WR(42) waveguide, s=.981 mm, Er=2.2, f=22 GHz

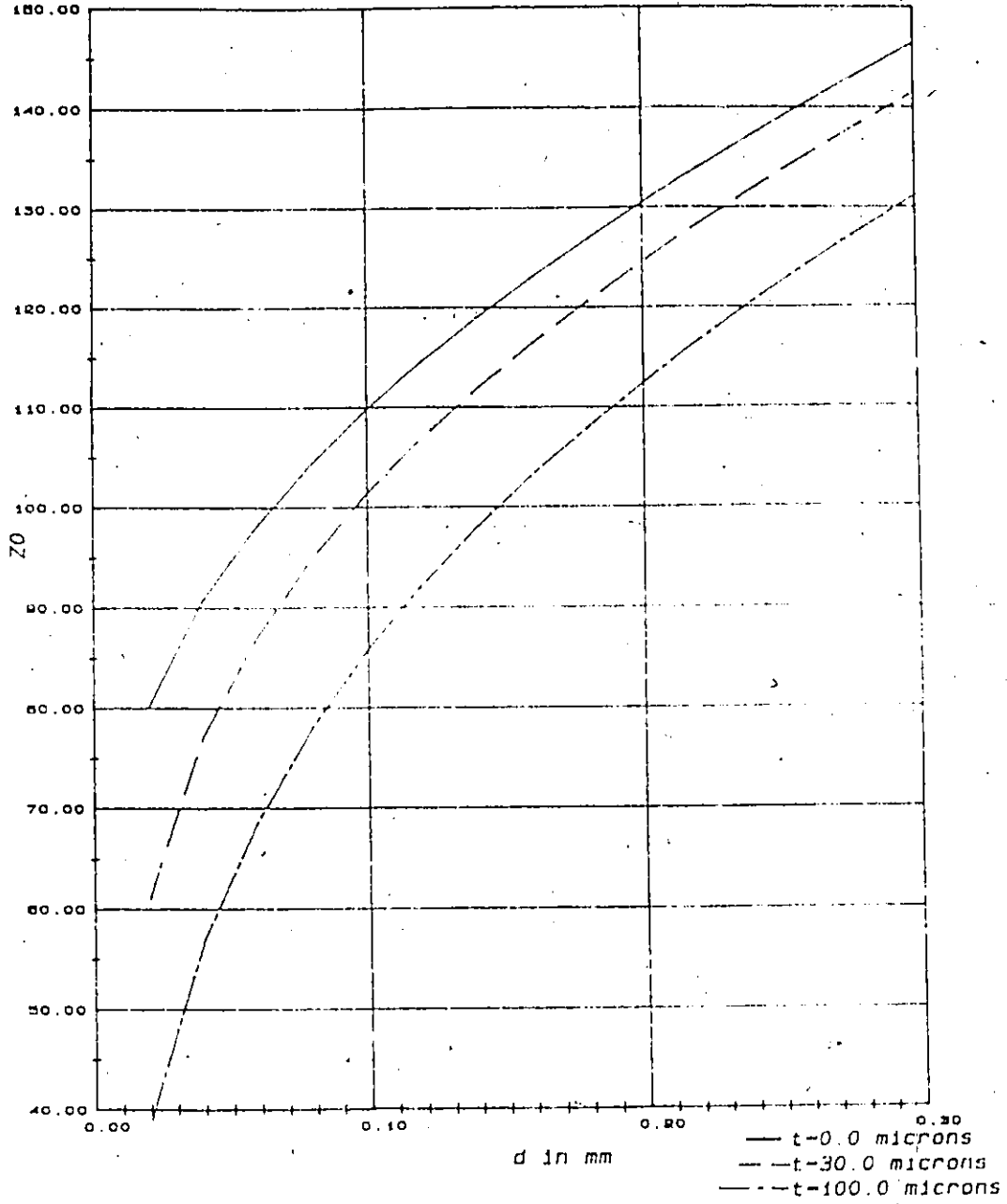


Figure 6-6 Z₀ vs Gap Width

WR (42) waveguide, $s = .381$ mm, $d = .1$ mm

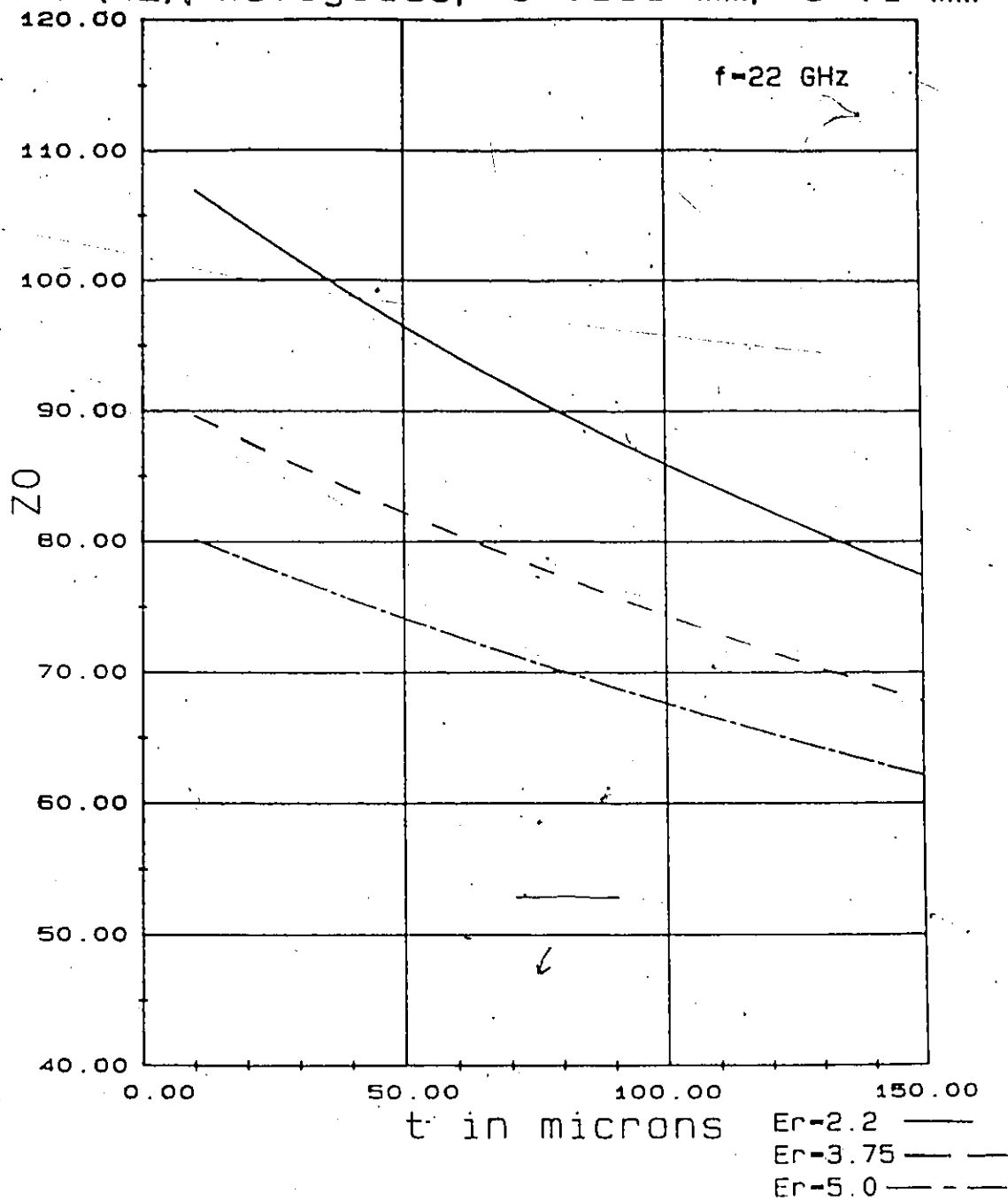


Figure 6-7 Z_0 vs Metallization Thickness

WR(42) waveguide, $s=0.381$ mm, $d=0.1$ mm, $\epsilon_r=2.2$

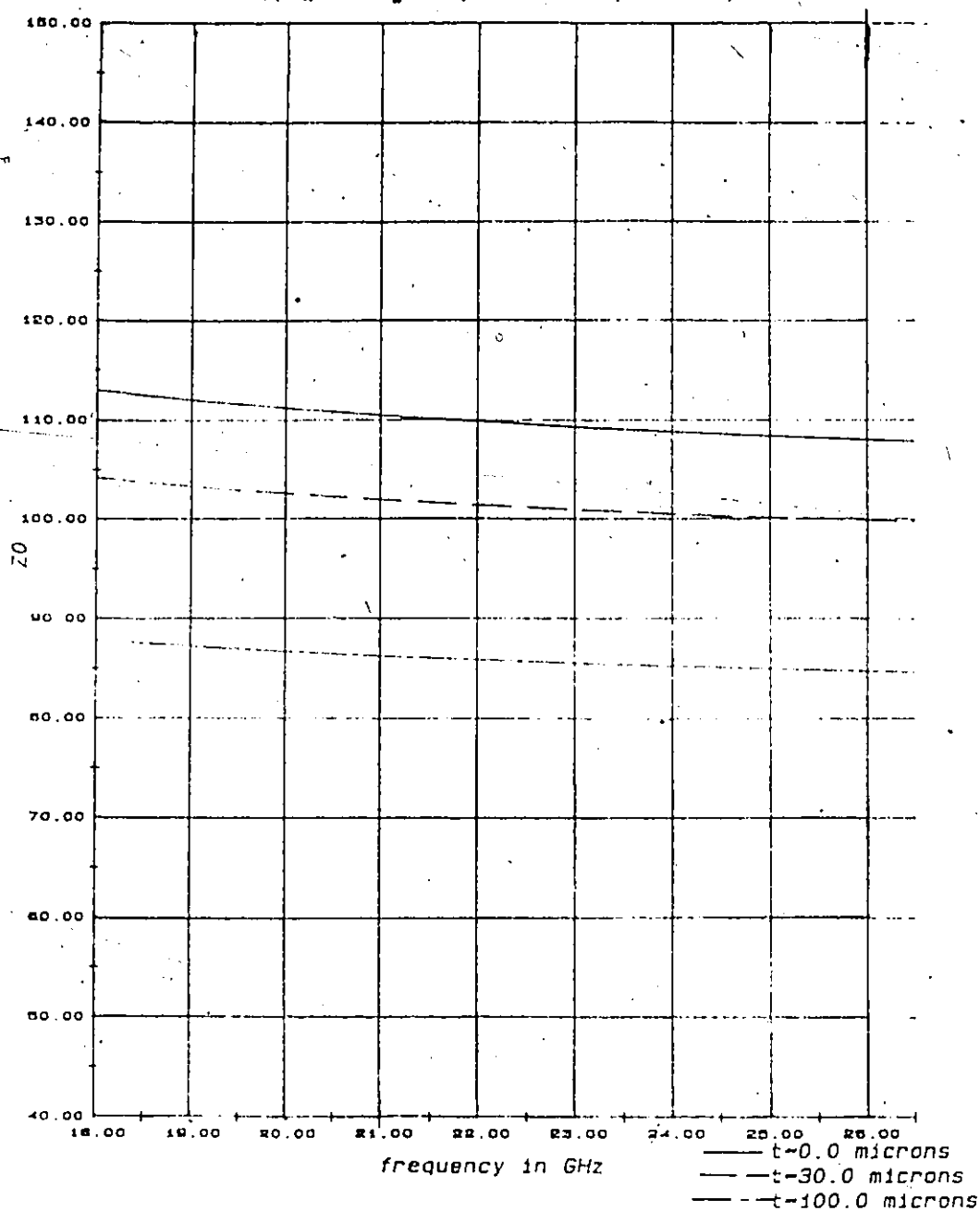
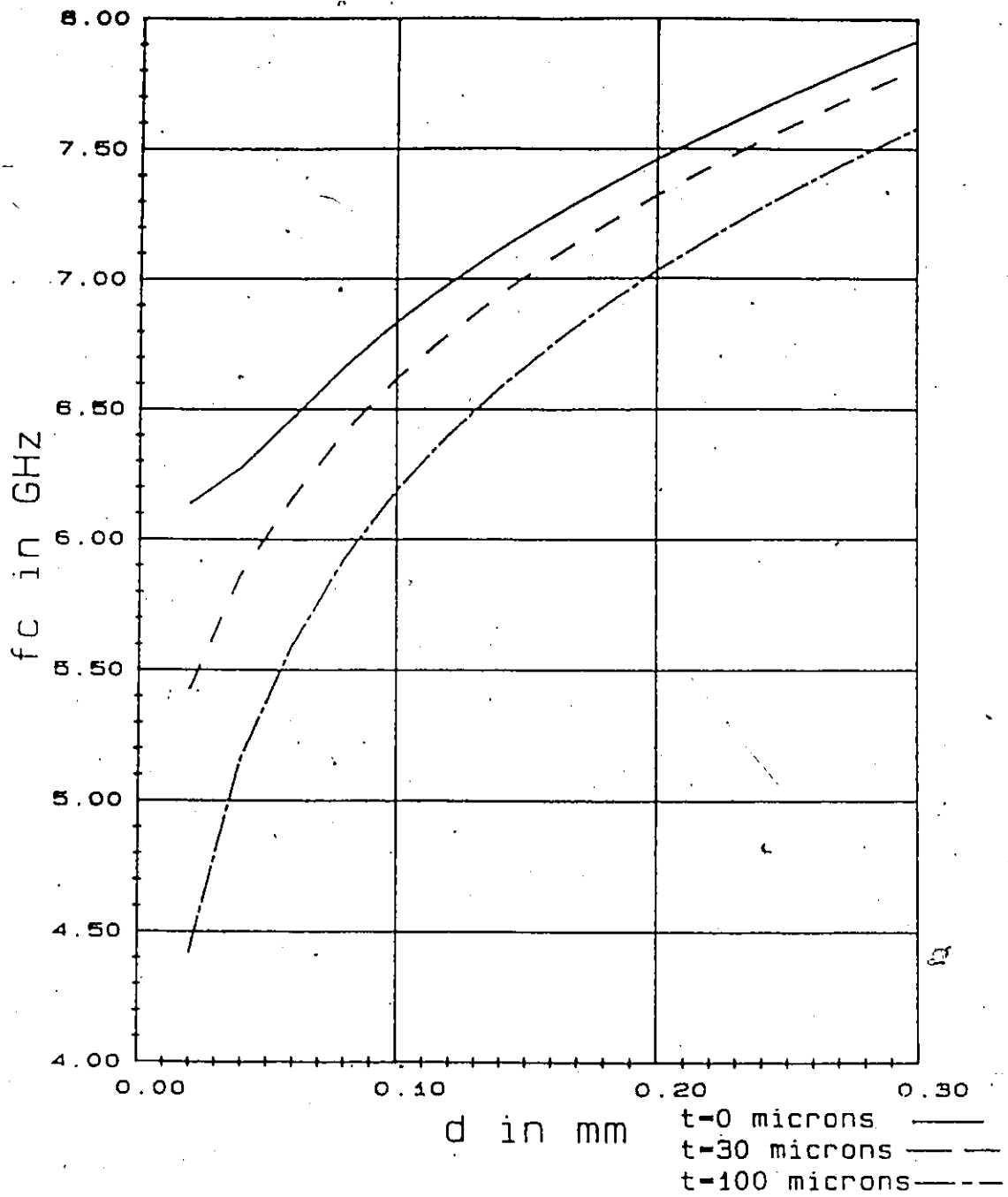


Figure 6-8 Z_0 vs Frequency

6.5 CALCULATION OF CUTOFF FREQUENCY

Using the same transverse resonance program, one can also determine the cutoff frequency of the finline. At cutoff ϵ_{eff} equals zero. Therefore, by setting $\epsilon_{\text{eff}} = 0.0$ and solving for frequency, one can determine the cutoff frequency of the finline. In practice, however, one cannot set $\epsilon_{\text{eff}} = 0.0$ since in the above transverse resonance equations, ϵ_{eff} is in the denominator. One can however set ϵ_{eff} very small and find the cutoff frequency without sacrificing accuracy. This method was implemented and the results are shown in Figures 6-9 and 6-10. These figures indicate that both an increase in metallization thickness and a decrease in gap width lower the dominant mode cutoff frequency of a finline. This is due to the increase in capacitive loading which occurs in both cases. Also, since capacitive loading of the waveguide increases with ϵ_r the dominant mode cutoff frequency is reduced accordingly.

WR(42) waveguide, $s = .381$ mm, $\epsilon_r = 2.2$ Figure 6-9 f_c vs Gap Width

WR(42) waveguide, $s=0.981$ mm, $d=1$ mm

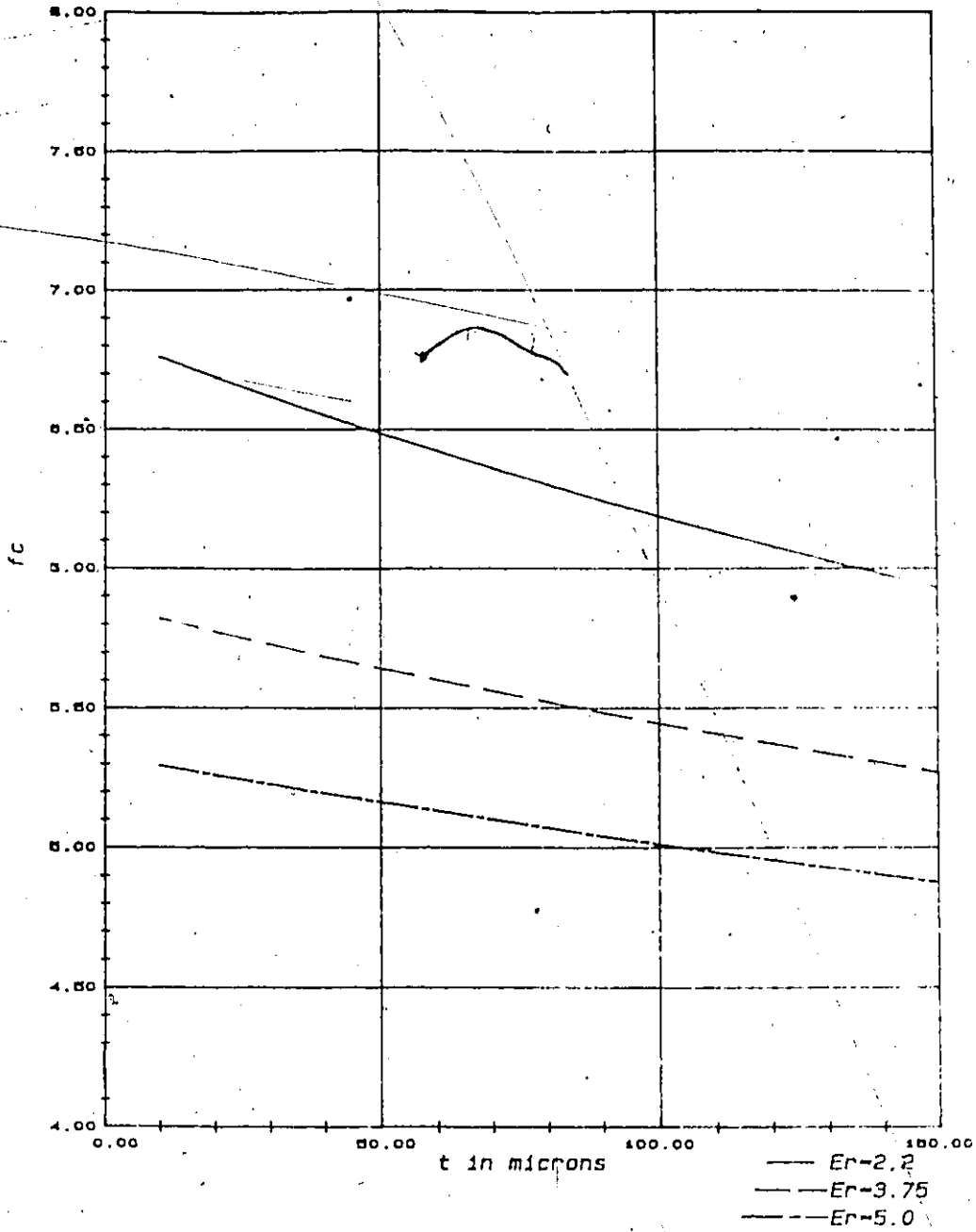


Figure 6-10 f_c vs Metallization Thickness

6.6 CONCLUSIONS

This chapter has presented some results obtained with a transverse resonance program which was developed to investigate the effect of metallization thickness on unilateral finlines with narrow gaps. The program is very versatile in that it can handle a wide range of housing aspect ratios, dielectric constants, substrate thicknesses, metallization thicknesses, gap widths, and either centered or non-centered circuits. The study has shown that one must pay particular attention to the metallization thickness when designing a finline circuit with narrow gaps. While at low frequencies, the effective dielectric constant of a finline always increases with metallization thickness, it can fall below the dispersion curve of zero thickness lines at higher frequencies due to a concentration of energy in the air gap in the case of very small gaps and/or large metallization thicknesses.

REFERENCES

1. R. Vahldieck and W.J.R. Hofer, "The Influence of Metallization Thickness and Mounting Grooves on the Characteristics of Finlines", *1985 IEEE MTT-S Int'l Microwave Symp. Digest*, pp. 143-144
2. S. Cohn, "Slotline on a Dielectric Substrate", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-17, pp. 768-778, October 1969
3. W.J.R. Hofer, "Finline Design Made Easy", *1978 IEEE MTT-S Int'l Microwave Symp. Digest*, p. 471
4. P.J. Meier, "Integrated Fin-Line Millimeter Components", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 1209-1216, December 1974
5. W. J. R. Hofer, "Finline Design Manual", *CRC Contract Report Series No. DOC-CR-SP-83-014*, p. 1.93
6. W. J. R. Hofer and M. Burton, "Closed Form Expressions for the Parameters of Finned and Ridged Waveguides", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 2190-2194, December 1982

CHAPTER VII

CONCLUSIONS

This thesis has described the design of a 20 GHz GaAs FET amplifier which has been realized using a combination of finline and microstrip. Specifically the amplifier exhibited unconditional stability with a gain of 6.7 db at 20 GHz. As shown in Chapter 5 there was a high degree of agreement between the predicted and measured results. This demonstrates the validity of the design process which was used in this thesis. In designing the amplifier an optimum transition from finline to microstrip was developed. This transition provides relatively low losses and a low V.S.W.R. over 60 % of a complete waveguide band. Also in this thesis a transverse resonance program was described which calculates the finline effective dielectric constant, characteristic impedance and cutoff frequency. The results of this program have shown the importance of including the effect of finite metallization thickness in the calculations when fins with narrow gaps are used. This thesis has also described a technology improvement which is in the form of plated through holes. The plated through holes are used in place of the standard serrations which are used to contain microwave energy within the waveguide housing. This amplifier has an advantage over many other designs in that it can be integrated into either a waveguide or finline environment. Also the amplifier is inexpensive to realize since it utilizes photolithographic techniques.

Appendix A

Transverse Resonance Analysis

Program Listing

```

0001 C
0002 C
0003 C
0004 C
0005 C
0006 C THIS PROGRAM COMPUTES EFFECTIVE DIELECTRIC CONSTANT AND IMPEDANCE
0007 C OF A FINLINE WITH NARROW GAP,
0008 C FOLLOWING IS THE MAINLINE SEGMENT OF THE PROGRAM,
0009 C VARIABLES ARE DEFINED AS FOLLOWS:
0010 C a is the width of the waveguide in mm,
0011 C b is the width of the waveguide in mm,
0012 C d is the gap width between the fins,
0013 C t is the metallization thickness,
0014 C h is the distance from sidewall to dielectric metal interface(dielectric side)
0015 C s is substrate thickness
0016 C Er is substrate relative dielectric constant
0017 C xi is a/lambda
0018 C xi is d/b
0019 C
0020 C
0021 C
0022 C
0023 C
0024 C
0025 C
0026 C
0027 C
0028 C
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0033 C
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0051 C
0052 C
0053 C
0054 C
0055 C
0056 C
0057 C
0058 C
0059 C
0060 C
0061 C
0062 C
0063 C
0064 C
0065 C
0066 C
0067 C
0068 C
0069 C
0070 C
0071 C
0072 C
0073 C
0074 C
0075 C
0076 C
0077 C
0078 C
0079 C
0080 C
0081 C
0082 C
0083 C
0084 C
0085 C
0086 C
0087 C
0088 C
0089 C
0090 C
0091 C
0092 C
0093 C
0094 C
0095 C
0096 C
0097 C
0098 C
0099 C
0100 C

```

IMPLICIT REAL (A-H,O-Z)
 COMMON a,b,d,t,h,s,Er,freq,xi,r,FI,FLAG,K
 EXTERNAL FC1
 C Enter finline parameters on the terminal
 1 WRITE(5,5)
 5 FORMAT (/,' ENTER WIDTH a AND HEIGHT b OF WAVEGUIDE IN mm ','\$)
 ACCEPT a,b
 10 WRITE(5,10)
 FORMAT (/,' ENTER GAP WIDTH BETWEEN FINS d IN mm ','\$)
 ACCEPT d
 15 WRITE (5,15)
 FORMAT (/,' ENTER METALLIZATION THICKNESS t IN MICRONS ','\$)
 ACCEPT t
 20 WRITE (5,20)
 FORMAT(/,' ENTER DISTANCE FROM SIDEWALL
 TO METAL/SUBSTRATE h IN mm ','\$)
 ACCEPT h
 25 WRITE(5,25)
 FORMAT (/,' ENTER SUBSTRATE THICKNESS s IN mm ','\$)
 ACCEPT s
 26 WRITE(5,26)
 FORMAT (/,' ENTER NUMBER OF TERMS ','\$)
 ACCEPT n
 30 WRITE(5,30)
 FORMAT (/,' ENTER Er AND FREQUENCY freq IN GHZ ','\$)
 ACCEPT Er,freq
 **a/(3.0E11/(freq*1.0E09))
 t=t/1000.
 FI=ACOS(-1.0)
 r=d/b
 C Initialize FLAG to 1.0 ie assume EEFF GT. 1.0
 FLAG=1.0
 XLI=1.0E0001
 XRI=Er-.01
 C Assume root lies between XLI and XRI


```

C FUNCTION SUBPROGRAM FCI(ROOT)
C THIS FUNCTION IS THE TRANSVERSE RESONANCE CONDITION FUNCTION
C AND IS GIVEN FOR BOTH CASES, IE WHEN EEFF IS LESS THAN AND
C GREATER THAN 1.0, THIS FUNCTION IS CALLED BY THE ROOT FINDING
C ROUTINE TO DETERMINE EEFF AND THE CUT-OFF FREQUENCY.

```

```

      FUNCTION FCI(ROOT)
      IMPLICIT REAL (A-H,L-Z)
      COMMON A,B,D,T,H,S,E,F,FREQ,X,F,PI,FLAG,K
      ATANH(Z)=(ALOG((1.0+Z)/(1.0-Z)))/2.0
      COTANH(Z)=1.0/TANH(Z)
      COTANH(Z)=1.0/TANH(Z)

```

```

C THE FOLLOWING FUNCTIONS ARE DEFINED BY COHN AND ARE
C USED TO FIND SUSCEPTANCE DUE TO FIRS.

```

```

      GANH1(N)=2.0*PI*K*(SQRT(1.0-(b**k)/(n**k))**2.0)/b
      GANH0(N)=2.0*PI*K*(SQRT(1.0+(b**k)/(n**k))**2.0)/b
      GANH0(N)=2.0*PI*K*(SQRT(1.0+(b**k)/(n**k))**2.0)/b
      FRI(N)=b*GANH1(N)/(2.0*PI*n)
      FN(N)=GANH1(N)*STATANH(GANH1(N)/(E*GANH0(N)))
      FN0(N)=GANH1(N)*STATANH(GANH1(N)/GANH0(N))
      FN(N)=b*GANH(N)/(2.0*PI*n)
      FN0(N)=b*GANH0(N)/(2.0*PI*n)

```

```

C IF THE FLAG IS 3.0 THE CUT-OFF FREQUENCY IS BEING
C CALCULATED SO SET EEFF SMALL
      IF (FLAG.EQ.3.0) THEN

```

```

          EEFF=1E-09
      ELSE
          EEFF=ROOT

```

```

      END IF
      V=SQRT(ABS(EEFF-1.0))
      U=SQRT(EF-EEFF)
      A2=B/(2.*X*SQRT(EEFF))

```

```

C INITIALIZE ALL SUMS
      SUH=0.0
      SUH1=0.0
      SUH2=0.0
      SUH3=0.0
      SUM0=0.0
      SUM1=0.0
      SUM2=0.0
      SUM3=0.0
      SUH4=0.0
      SUH5=0.0

```

```

C IF FLAG IS 1.0 EEFF IS GREATER THAN 1
      DO 10 I=1,N

```

```

          N=I*1.0
          SUH5=((SIN(PI*N*d/b))**2.0)/(n*(PI*N*d/b)**2.0)
          SUM0=((EXP(STATANH(N0(N)))-EEFF*(FRI(N))**2.0)*COTANH(GN0(N)))
          I/((1.0+(b/(2.*a2*n))**2.0)*FRI(N))-U**2.0)*SUH5
          SUH4=SUM4+SUH5
          SUM10=SUM0+SUM10
          SUH20=((V**2.0)**(1.0-1/(FN0(N)))*SUH5

```

```

0058      SUM30=SUM20+SUM30
0059      CONTINUE
0060      C10=COTANH(2.*PI*V**2**/a)
0061      C29=(2.*d/(a2*v))*((a2*v/(2.*b))*COTANH(2.*PI*V*(a-h-t))*k/a)
0062      C30=(C10+C20-1.)/(C10+C20)
0063      C30=SUM4+SUM30/(2.*SORT(EFF))
0064      C FCTO IS TRANSVERSE RESONANCE CONDITION WHEN EFF LT. 1.0
0065      FCTO=-((a2*v/(2.*b))*COTANH(2.*PI*V*(a-h-t))*k/a)
0066      FCTO=-((a2*v/(2.*b))*k/a)+((u**2.0)*SUM4+SUM10)/
0067      1 (2.*SORT(EFF))-(a2*v/(2.*d))*C30
0068      FCT=FCO
0069      RETURN
0070
0071      C IF EFF GT. 1.0 THEN USE THE FOLLOWING EQUATIONS
0072      DO 20 I=1,K
0073      N=I+1
0074      SUM5=((SIN(PI*N*d/b))*2.0)/(n*(PI*n*d/b)**2.0)
0075      SUM=((EXP(TANH(n(n))) - EFF*(FRI(n))**2.0)*COTANH(an(n)))
0076      1 /((1.0+(b/(2.*a2*n))**2.0)*FRI(n)) - u**2.0)*SUM5
0077      SUM4=SUM4+SUM5
0078      SUM1=SUM+SUM1
0079      SUM2=(V**2.0)*(1.0-1/(FN(n)))*SUMS
0080      SUM3=SUM2+SUM3
0081      CONTINUE
0082      C1=COTANH(2.*PI*V**2**/a)
0083      C2=(2.*d/(a2*v))*((a2*v/(2.*b))*COTANH(2.*PI*V*(a-h-t))*k/a)
0084      1 -((V**2.*SUM4+SUM3)/(2.*SORT(EFF)))
0085      C3=(C1+C2+1.)/(C1+C2)
0086      C FCT IS TRANSVERSE RESONANCE CONDITION WHEN EFF IS GT. 1.0
0087      FCT=-((a2*v/(2.*b))*COTANH(2.*PI*V*(a-h-t))*k/a)
0088      1 (2.*SORT(EFF)) + ((u**2.0)*SUM4+SUM1)/
0089      1 (2.*SORT(EFF)) - (a2*v/(2.*d))*C3
0090      RETURN
0091      END

```

```

0001 C THE FOLLOWING SUBROUTINE CALCULATES NORMALISED CUTOFF WAVELENGTH
0002 C OF A RIDGED WAVEGUIDE, THIS SUBROUTINE IS CALLED LAMCR, THE EQUATION
0003 C IS EQUATION 1.52 IN THE FIN LINE MANUAL, ALL VARIABLES ARE TRANSFERRED
0004 C VIA THE COMMON STATEMENT, ALAMCR IS THE RETURNED VALUE,
0005 C
0006 C
0007 C
0008 C
0009 C
0010 C
0011 C
0012 C
0013 C
0014 C
0015 C
0016 C
0017 C
0018 C
0019 C

```

```

0001 C THE FOLLOWING SUBROUTINE Z0INFI CALCULATES Z0 INFINITY USING A VOLTAGE
0002 C POWER DEFINITION, THE EQUATION IS EQUATION 1.60 IN THE FINLINE MANUAL,
0003 C
0004 C
0005 C
0006 C
0007 C
0008 C
0009 C
0010 C
0011 C
0012 C
0013 C
0014 C
0015 C
0016 C
0017 C
0018 C
0019 C

```

```

0001 C
0002 C
0003 C
0004 C
0005 C
0006 C
0007 C
0008 C
0009 C
0010 C
0011 C
0012 C
0013 C
0014 C
0015 C
0016 C
0017 C
0018 C
0019 C

```

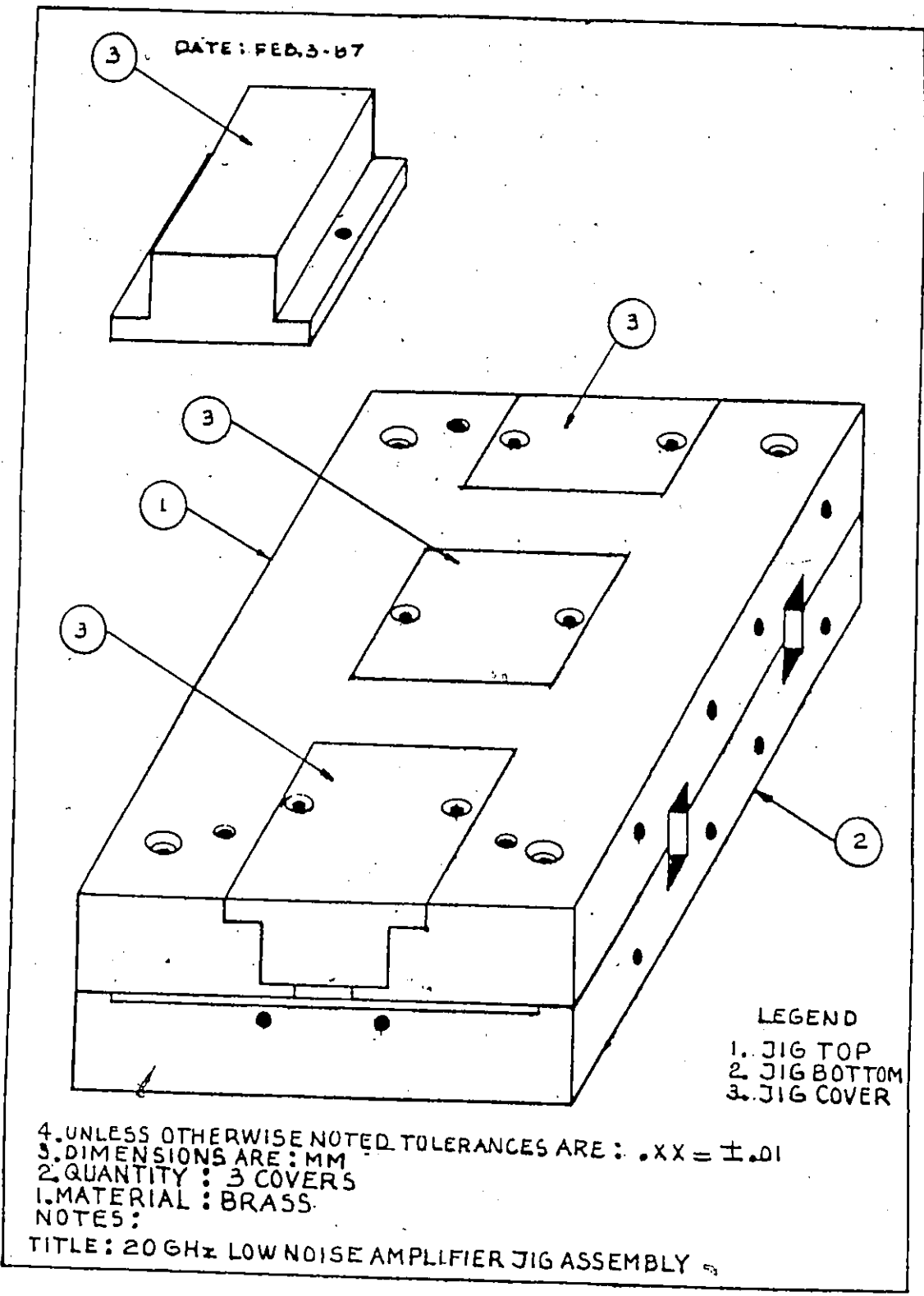
```

SUBROUTINE LAMCR(ALAMCR)
  IMPLICIT REAL (A-H,O-Z)
  COMMON a,b,d,t,h,s,E,r,freq,n,r,F,FLAG,K
  CALL LAMCR(ALAMCR)
  Z0INF=(120*(PI**2,0)*d**k*ALAMCR/(b**a)))/((2*k*ALAMCR
  1/a)*((COS(PI*k*ALAMCR/a))**2,0)*ALOG(1/SIN(PI*k*d/(2*b))))
  1+PI*k*ALAMCR/(2*a))+SIN(2*PI*k*ALAMCR/a))/4+((d/b)*
  1*(COS(PI*k*ALAMCR/a))**2,0)/((SIN(PI*k*ALAMCR*(1-t/a)))**2,0))
  1*(PI*k*ALAMCR*(1-t/a))/2-(SIN(2*PI*k*ALAMCR*(1-t/a)))/4))
  RETURN
END

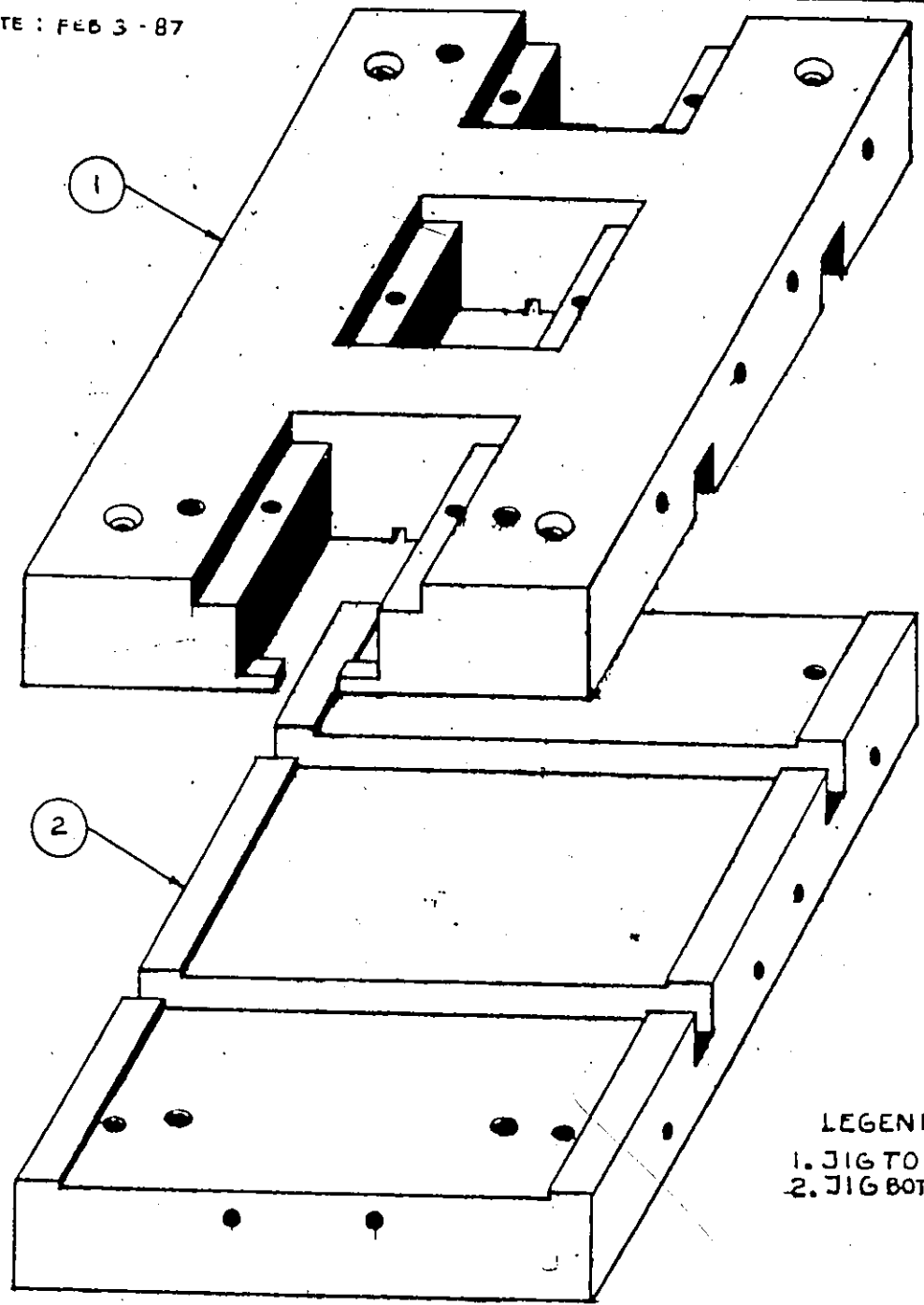
```

Appendix B

Amplifier Test Jig Drawings



DATE : FEB 3 - 87



LEGEND
1. JIG TOP
2. JIG BOTTOM

TITLE : 20 GHz LOW NOISE AMPLIFIER JIG ASSEMBLY