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Name of candidate: ELMASRY, Mr. Mohamed I.Y.

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This thesis has been prepared under my supervision

P.M. Thompson
(Thesis Supervisor)
(signature)
September 30th, 1970
(Date)

We, the undersigned, certify that we have approved this thesis, and that the candidate has defended it successfully.

1. O. Celinski ..... Date: September 30th, 1970
(Signature of examiners)

2. C. Lemyre ..... Date: September 30th, 1970

3. S.R. Das ..... Date: September 30th, 1970

4. ..... Date: .....

5. ..... Date: .....

6. ..... Date: .....

7. ..... Date: .....

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L.A. Beauchesne *(Dean of Graduate Studies)*

LOGIC AND CIRCUIT DESIGN OF HIGH SPEED DIGITAL SYSTEMS

by

Mohamed I.Y. Elmasry

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Department of Electrical Engineering
Faculty of Pure and Applied Science
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Logic and Circuit Design
of High Speed Digital Systems

Abstract

The speed of operation of digital systems can be increased by improving the logic or the circuit design. In this thesis, the logic and the integrated circuit design are considered using a unified approach. The logic design is based upon partitioning the input variables according to their time sequence such that each logical operation is predetermined by intermediate outputs. This system is shown to be compatible with a two-level current mode realization. The integration of this realization is economical of Silicon area and employs a novel non-linear collector-load structure.

Acknowledgements

The author wishes to express his thanks to his supervisor Professor P.M. Thompson for his guidance in carrying out this research work and his constructive suggestions in the preparation of this thesis; to Dr. C.L. Sheng, Dr. S.R. Das and Mr. H. Seemann for their assistance with the material presented in this thesis. He would also like to thank Mr. J. Rywak, Mr. M. King and the staff of Northern Electric Company Limited for fabricating sample circuits and giving the author the opportunity to study design problems related to this work. He wishes to thank his wife, Elizabeth, for her typing and encouragement through the preparation of this thesis. Finally, the financial support of the National Research Council of Canada under grant A3379 is gratefully acknowledged.

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List of Symbols

C	Output capacitance
C_s	Stray capacitance
C_{Te}	Emitter transition capacitance
C_{Tc}	Collector transition capacitance
C_{dc}	Diffusion collector capacitance
D_n	Electron diffusion constant
D_p	Hole diffusion constant
f_T	Gain-band width product
h	A binary digit
I_E	Emitter current
I_C	Collector current
I_b	Base current
I_o	Constant current, switching current
I_L	Load current, lateral current
I_V	Vertical current
k	A binary digit
m	Number of output variables
n	Number of input variables
NM_0	Logical zero noise margin
NM_1	Logical one noise margin
P	Partial product, power dissipation
Q	A charge, a transistor
Q_B	Base charge

$r_{bb'}$	Base extrinsic resistance
r_{cc}	Collector extrinsic resistance
R	Resistance
t	Time
t_s	Time interval
t_p	Time interval
T	Transition time
T_d	Delay time
T_c	Collector time constant
T_E	Emitter time constant
T_B	Base time constant
T_s	Excess stored-charge recombination time constant
V_t	Threshold voltage
V_{in}	Input voltage
V_{out}	Output voltage
V_1	Logical one voltage
V_0	Logical zero voltage
V_ℓ	Logical swing
V_{eb}	Emitter base voltage
V_{cb}	Collector base voltage
V_{ce}	Collector emitter voltage
V_r	Reference voltage
V_j	Junction voltage
V_s	Supply voltage
V_T	Thermal voltage
V_L	Load voltage

W	Base width
W_e	Emitter width
x	An input variable
y	A control input
z	An output variable
α	Common base current gain
β	Common emitter current gain

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Logic and Circuit Design of High Speed Digital Systems

Introduction

An important application of logic circuits is in real-time computers, such as used in control or communication systems. In such systems, the time required for computation is a critical factor in the stability of the overall system or the handling of data at the required rate. Pattern recognition, signature analysis, terrain radar are other examples which call for minimum computation time and high speed logic circuits are required for their realization.

In order to design high speed logic circuits, it is necessary to consider system, logic and circuit design in addition to fabrication and device technology. In the Department of Electrical Engineering, University of Ottawa, Professor J.A. Brozozowski and his students have studied high speed logic design using asynchronous sequential circuits [1, 2] and Professor C.L. Sheng has made contributions [3] to some of the theoretical aspects related to high speed logic design. Professor P.M. Thompson has done some preliminary investigation into circuit configuration for the high speed realization of asynchronous circuits [4].

This thesis is primarily concerned with the semiconductor integrated circuit design of general purpose high speed logic circuits using bipolar circuit elements. However, it also explores the interdisciplinary areas between circuit and device design and between circuit and logic design. The performance of devices in circuits and of circuits in logic systems is studied in terms of models.

In chapter 1, the two basic models are developed; a system model describing a logic circuit in a logic system (section 1-2) and a circuit model describing the switching element (bipolar transistor) in a logic circuit (section 1-3). Section 1-1 states

the basic concepts used in developing the logic design procedure of chapter 2.

In chapter 2, we introduce a general procedure for designing high speed logic systems, based on partitioning the input variables according to the time sequence of their arrival, and using logic blocks whose logic function is predetermined by intermediate outputs of other blocks. Related high speed logic design approaches have been considered in the literature, but they deal mainly with specific arithmetic operations [5, 6, 7].

In chapter 3, an integratable Emitter Coupled Logic Circuit, with a novel non-linear load structure is used for realizing the building blocks developed in chapter 2. The circuit offers advantages over some of the high speed logic circuits which have been reported recently [8, 9, 10]. The non-linear load offers advantages in both static and dynamic characteristics over the conventional diffused load resistors.

In chapter 4, a realization of such load is considered and some experimental results are given.

CHAPTER 1

Integrated Logic Circuits

In this chapter, the logic, the system and the circuit aspects of logic circuits are discussed. The first section presents a brief discussion of the logical concepts of designing combinatorial and sequential circuits. The second section gives a system model relating the system parameters to the circuit design. In the final section the integrated circuit realization using transistor as the switching device is considered and a general figure of merit for integrated logic circuits is proposed.

1-1 Logical Design Aspects of Integrated Logic Circuits

The purpose of this section is to state the basic logic design concepts which will be used in developing the high speed logic design approach described in chapter 2. Consider a general model of a logic system (switching system) as shown in Fig. 1-1.

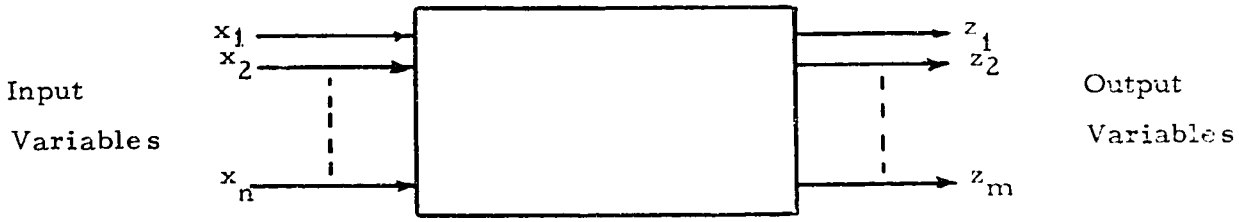


Fig. 1-1 General Model of a Logic System

The n input variables $x_k(t)$, k = 1, 2, ... n and the m output variables $z_i(t)$, i = 1, 2, ... m are assumed to be function of time. The variables are binary variables; i. e., they take one of two distinct values '0' and '1'. The system (machine or circuit) is said to be combinatorial if at any particular time, the present value of the outputs are determined solely by the present value of the inputs. Alternatively, if the present value of the outputs are dependent not only on the present value of the inputs, but also on the present state of the system, the system is called a sequential system [11, 12, 13, 14].

1-1-a Combinatorial Circuits

In combinatorial circuits, the relationship between an output (z_i) and the input variables (x_1, ... x_n) can be represented in a table form (truth table) or as a relation in Boolean algebra of the form:

$$z_i = f_i(x_1, x_2, \ldots x_n) \qquad (1\text{-}1)$$

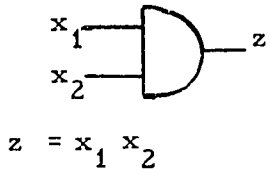
where f_i is a switching function.

Any switching function can be realized in two or more logic levels. These two realizations are called parallel and serial logic systems respectively. Since each level of logic adds to the total delay of the system, a parallel logic system is generally faster than a serial system [15, 16].

A switching function can be simplified using the rules of Boolean algebra or one of the two systematic methods available; the Karnaugh-map (K-map) and the Quine-McKlusky method. Because the K-map is used as a design tool in chapter 2 it is described in the next section.

1-1-b The K-map Representation of Switching Functions

The K-map is a restatement of the truth table in a graphical form. Whereas, in a truth table the output variable is directly tabulated against the input variables, in a K-map the input variables are ordinates for the output variable [17]. The truth table and the K-map of AND function is shown in Fig. 1-2.



Truth Table

x_1	x_2	z
0	0	0
0	1	0
1	0	0
1	1	1

K-map

x_2 \ x_1	0	1
0	0	0
1	0	1

Fig. 1-2 AND Gate Representation

1-1-c Level and Pulse Logic Signals

In logic systems, time is divided into increments or intervals. Usually the time intervals are all of equal duration, say t_s. If the signal representing a certain variable maintains the same constant value for t_s, then the signal is called a level signal. If it maintains a constant value for t_p ($t_p \ll t_s$) and is zero for the rest of the interval, then the signal is called a pulse signal [18]. In this thesis, the logic signal is assumed to be of the first type.

1-1-d Synchronous and Asynchronous Sequential Circuits

In sequential circuits the outputs are function of the inputs and the present state. This state is indicated by the output of a memory device (state variable) as shown in Fig. 1-3.

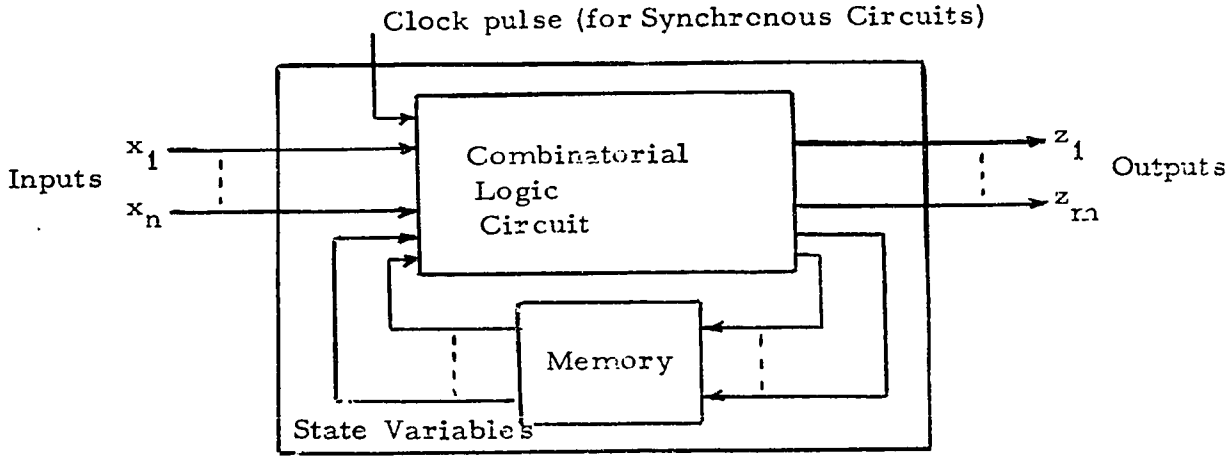


Fig. 1-3 A Model for Sequential Circuits

In synchronous circuits, a clock input pulse is used. The outputs and the next state variables are not computed unless a clock pulse exists. Thus at each time interval there is precisely one computation step. In asynchronous sequential circuits, no clock pulse is used. The beginning of each time interval is marked by a change of at least one input. The inputs are never changed unless the circuit has completed its computation step which is indicated by a 'completion' signal [18].

The most commonly sited purpose of using asynchronous circuits is to attain the maximum possible speed of the switching devices used because none of the devices need to wait for a clock pulse. The penalty paid for this approach is the difficulty of designing a system with sufficient stability margins. This difficulty is due to race and hazard problems [18]. The unwanted response of such a system can be eliminated by inserting delay devices in appropriate lines [19], but this itself involves a reduction of the overall system speed.

1-2 System Design Aspects of Integrated Logic Circuits

System aspects of logic circuits have been described in the literature [20, 21, 22, 23, 24, 25, 26, 27]. In this section, a system model is used to define logic system parameters.

1-2-a System Model

In an electronic logic system, the basic logic operation is transferring a logic signal from a logic block (logic source) to the input of another logic block (logic detector) through a transmission system (Fig. 1-4). A logic block has usually more than one input and each output is used as an input variable for a number of other logic blocks. The number of inputs is called the fan-in and the number of blocks driven by one output is called the fan-out. For simplicity only single-input-single-output logic blocks are considered.

The logic signal can be a level or a pulse signal. Because high speed logic design of combinatorial circuits is considered in chapter 2, only level signals are used.

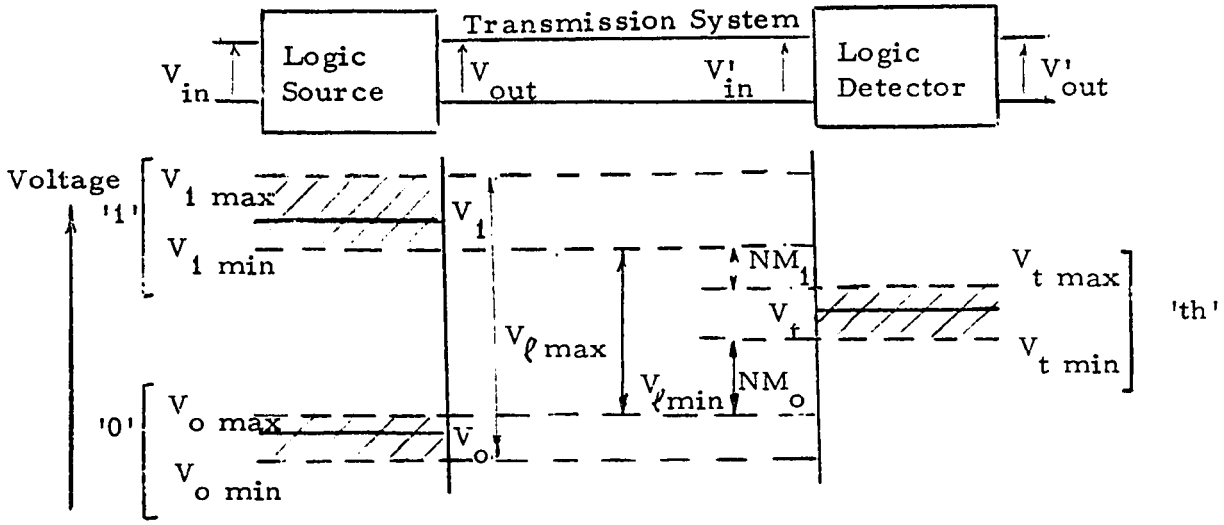


Fig. 1-4 System Model and Logic Levels

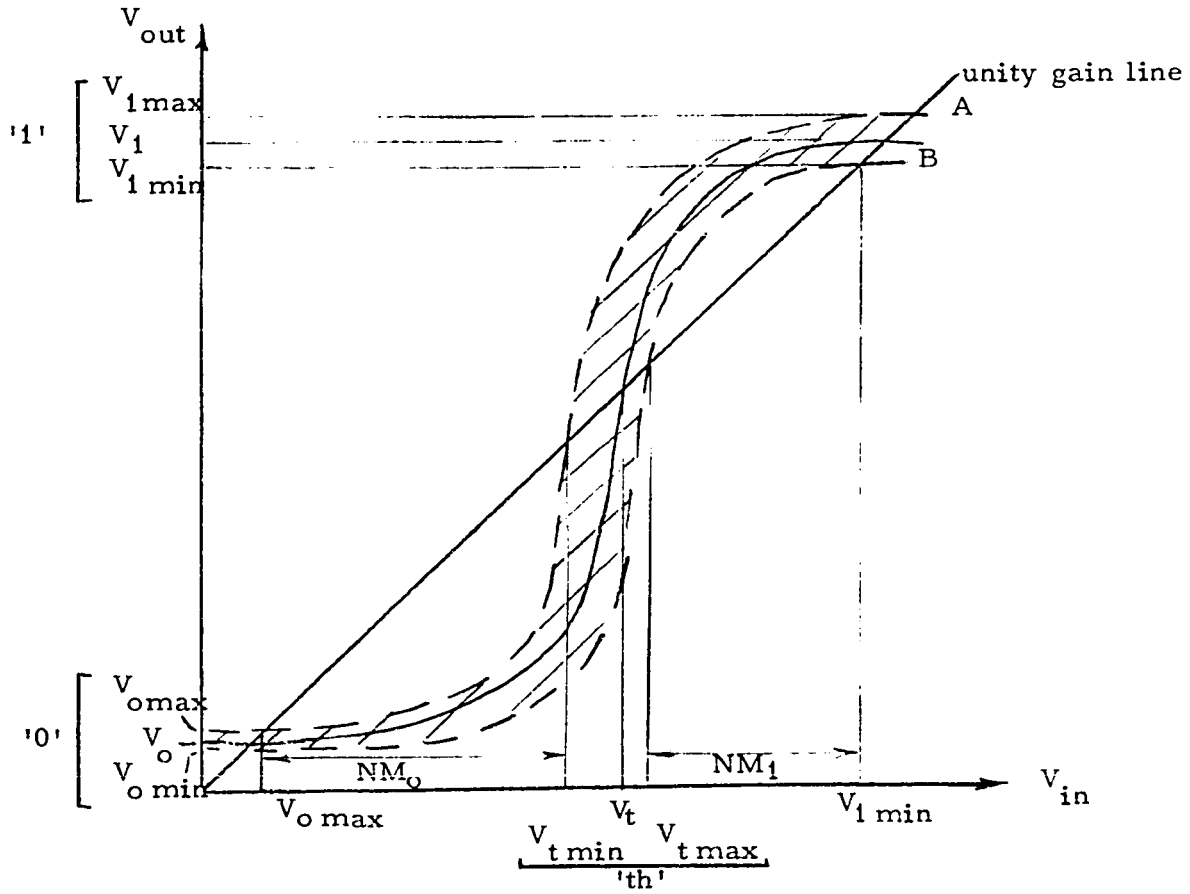


Fig. 1-5 DC Transfer Characteristic of a Non-inverting Logic Block

The output level signal is at one of binary levels, representing the bits of information, '0' or '1' . These two levels can be voltage, current, energy ... or impedence. However, in present day integrated circuits voltage levels, V_0 and V_1 are used. The logic system used here is a positive logic system, where the logical '1' level is positive with respect to the logical '0'.

At the input, the voltage signal is detected with respect to a threshold voltage V_t. In non-inverting logic blocks, if the input voltage is greater than V_t, the output voltage will be at logical '1' and if the input voltage is less than V_t the output voltage will be at logical '0'.

1-2-b Noise Margins

Signal distortion, due to attenuation or system noise, causes a reduction of the system reliability. Since distortion is primarily introduced by the noise in the system, it is conventional to refer to the margin allowed for distortion of the logic levels as the noise margins. Two noise margins are defined (Fig. 1-4)

$(NM)_0 \equiv$ noise margin for a logical '0' $= V_{t\ min} - V_{0\ max}$

and

$(NM)_1 \equiv$ noise margin for a logical '1' $= V_{1\ min} - V_{t\ max}$

1-2-c DC Transfer Characteristic

Signal and noise margin definitions have been stated by considering the transmission system, the input and the output ports. Alternatively the input-output gate relationship (the DC transfer characteristic) also provides information about the system. In Figure 1-5, the unity gain line (with slope $\frac{dV_{out}}{dV_{in}}$ = unity) intersects the transfer characteristics at three points, the logical '0' , the logical '1' and the threshold level 'th'. As the parameters of a particular design are varied over their tolerance ranges, the transfer characteristic (of a non-inverting gate) will be as shown by the dotted curves

A and B. The shaded region between the limit envelops A and B represents the region of possible transfer characteristics. Since the output does not reach its static value at the instant of the input, a further spreading of the transfer characteristic results. Because of these static and dynamic tolerances, each level becomes a zone as shown in Figure 1-4 and Figure 1-5. The above definitions of noise margins are shown. It is also shown that:

(a) when the input is in the region ($V_{0\ min} \lesseqgtr V_{in} \lesseqgtr V_{t\ min}$)

the output is in the region ($V_{0\ min} \lesseqgtr V_{out} \lesseqgtr V_{t\ min}$)

(b) when the input is in the region ($V_{t\ max} \lesseqgtr V_{in} \lesseqgtr V_{1\ max}$)

the output is in the region ($V_{t\ max} \lesseqgtr V_{out} \lesseqgtr V_{1\ max}$)

i.e., the circuit will recognize and maintain two determined levels; a '1' above $V_{t\ max}$ and a '0' below $V_{t\ min}$. The region ($V_{t\ min} \lesseqgtr V_{in} \lesseqgtr V_{t\ max}$) represents undetermined output and the logic signal lies in this region only during transitions from one level to the other.

1-2-d Logic Swing and Propagation Delay

The difference between the two levels V_1 and V_0 is called the logic swing V_ℓ. The time it takes the output signal to transfer from one level to another through the undetermined region is called the transition time (T) and the time it takes the input signal to change the output signal is called the delay time (T_d).

1-3 Circuit Realization

The development of high speed logic circuits requires a model which adequately describes the operation of the device in the circuit. A complete non-linear transistor model needs computer computational techniques [28, 29]. For binary circuits, it is sufficient to develop expressions for the two states and a discrete analysis can be used to study the transition from one state to another.

1-3-a Charge Control Transistor Model

In this section, a simple approach is developed from charge control theory [30, 31, 32]. The usefulness of thismethod stems from the fact that the variation of non-linear elements with time does not have to be considered. The transistor can be switched from one state to another by changing the base charge and it is only necessary to be concerned with movement of a discrete amount of base charge.

It is convenient to consider that the transistor performance in binary circuits as divided into four regions of operation [33] :-

(a) Cutoff Region

(b) Normal Active Region

(c) Partial Saturation Region (Soft Saturation)

(d) Saturation Region

It is useful at this point to introduce a charge distribution diagram (Fig. 1-6) which shows the approximate minority charge distribution in the base region.

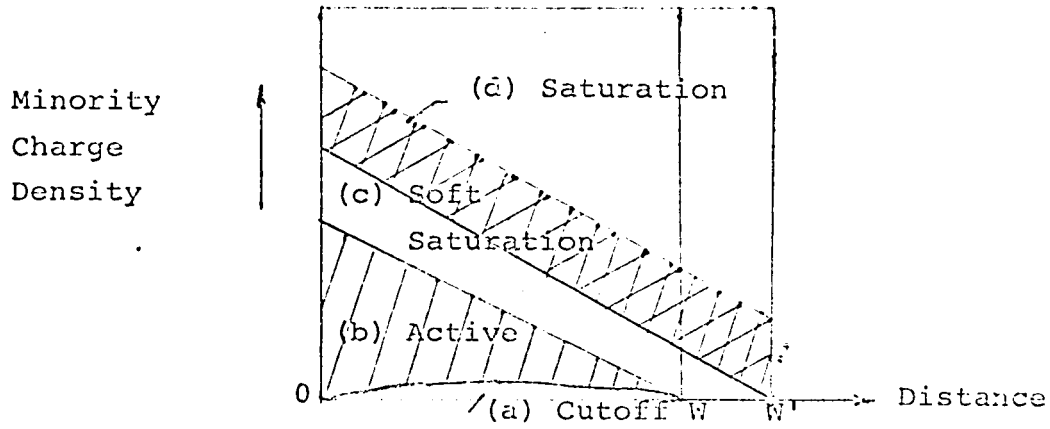


Fig. 1-6 Minority Charge Distribution in a Transistor Base

(a) Cutoff Region

In this region both junctions are reverse-biased. An equilibrium concentration of holes and electrons in the base region exists and the base charge Q_B can be assumed to be zero.

(b) Normal Active Region

In this region the emitter junction is forward biased and the collector junction is reverse biased. The change of the collector current (ΔI_C) is proportional to the change in the base charge (ΔQ_B):

$$\Delta I_C = \Delta Q_B / T_C \tag{1-2}$$

where T_C is the collector time constant. The change in base and emitter currents can be expressed with similiar relations :

$$\Delta I_E = \Delta Q_B / T_E \tag{1-3}$$

$$\Delta I_B = \Delta Q_B / T_B \tag{1-4}$$

where the base, the collector and the emitter time constants (T_B, T_C and T_E) are related by:

$$T_B = \beta T_C \tag{1-5}$$

$$T_E = \alpha T_C \tag{1-6}$$

where $T_E = \dfrac{W^2}{2 D_n}$ (1-7)

α and β are the normal active common base and common emitter current gains. W and D_n are the base width and the electron diffusion constant.

Figure 1-7 shows an equivalent circuit of a transistor operating in the active region. The base-emitter current I_{be} is divided into two components, $\dfrac{Q_B}{T_B}$ and $\dfrac{dQ_B}{dt}$. The first component is the static base current necessary to maintain the collector current I_C and accounts for the charge that recombines in the base region. The second component is a transient current, which accounts for the base control-charge. A diode represents the non-linear behavior of the emitter and collector junctions. The characteristic of the base-emitter diode is a function of the collector current and this is indicated by an arrow. The collector-emitter voltage is the difference between the

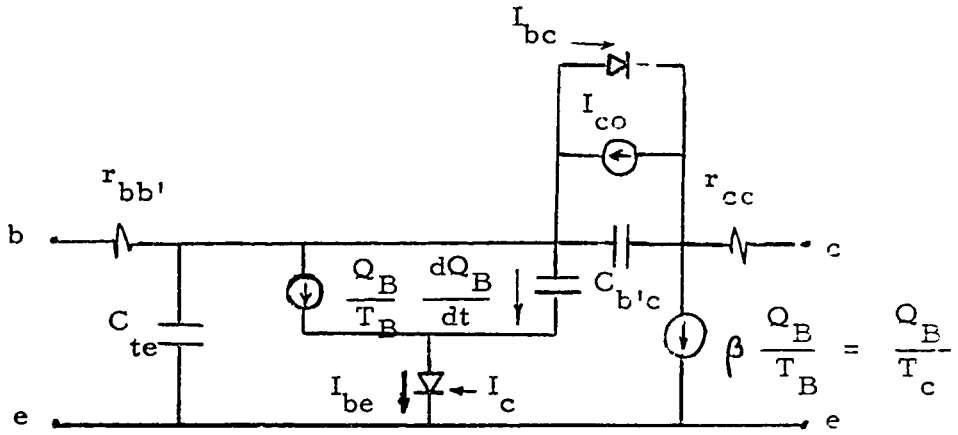


Fig. 1-7 Charge-control Equivalent Circuit for Active Region

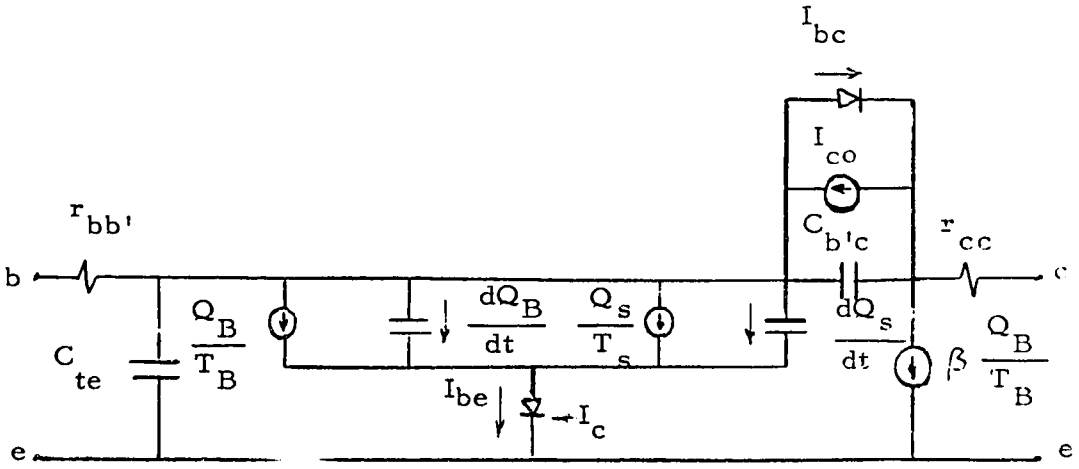


Fig. 1-8 Equivalent Circuit for the Partial and Total Saturation Regions

base-collector and the base-emitter diode voltage drops. The model also includes the following parasitic effects:

1 - The collector leakage current I_{co}.

2 - The extrinsic base and collector resistances $r_{bb'}$ and $r_{cc'}$.

3 - The transition capacitances C_{te} and C_{tc}, which are due to the space charge regions across the emitter and the collector junctions and the diffusion capacitance C_{dc}, which is due to the change of injected minority carriers in the base. The two capacitances C_{tc} and C_{dc} are combined into $C_{b'c}$.

(c) Partial Saturation Region

The emitter junction is forward biased and the base-collector junction is still in a low conductance state. Note that the current in the base-emitter junction producing the base control charge is greater than the current producing the stored charge in the base-collector junction. Figure 1-8 shows a transistor equivalent circuit for the partial and total saturation region. Neglecting I_{C_o} and the junction capacitances, the base-collector and the base-emitter currents are given by:

$$I_{bc} = \frac{Q_s}{T_s} + \frac{dQ_s}{dt} \tag{1-7}$$

$$I_{be} = \frac{Q_B}{T_B} + \frac{dQ_B}{dt} + \frac{Q_s}{T_s} + \frac{dQ_s}{dt} \tag{1-8}$$

where : Q_B and Q_s are the base control and the base stored charges.
T_B and T_s are the base control-charge time constant and excess stored-charge recombination time constant.

In partial saturation region, the collector current increases as more base control-charge Q_B is stored. As the transistor approaches total saturation, more of Q_B is stored as excess stored-charge and β decreases.

(d) Saturation Region

Both junctions are forward biased in this region. The excess current $(I_{be} - \frac{Q_B}{T_B})$ contributes primarily to the build up of the stored-charge Q_s.

1-3-b High Speed Circuit Considerations

(1) Transistor Saturation

The base stored charge Q_s represents a charge which must be removed from the base region before the transistor can start to traverse the active region to the cutoff region. Thus a storage delay elapses while the stored charge is being removed. Therefore, in high speed logic circuit the transistors should be kept out of saturation.

(2) Base Width Modulation and Partial Saturation

The base width W is dependent upon the widths of both the emitter and collector junction space charge layers; hence upon V_{eb} and V_{cb} [34, 35]. Since the emitter space-charge layer is narrow under normal bias conditions and the voltage variations produced by the normal range of bias currents are very small, only the dependence of W on V_{cb} is of significance. As the collector reverse bias is decreased and the transistor enters the partial saturation region the base width is increased and so T_c. This effect is called base width modulation. To achieve the maximum speed, the effect of base width modulation should be kept minumum by reducing the change of V_{cb} during the transition region. Transistor operation in the partial saturation region (small Q_s) where β starts to fall should also be avoided.

1-3-c Saturating and Non-saturating Logic Circuits

The circuits used to implement logic functions can be classified into saturating and non-saturating logic circuits (Fig. 1-9) [36, 37].

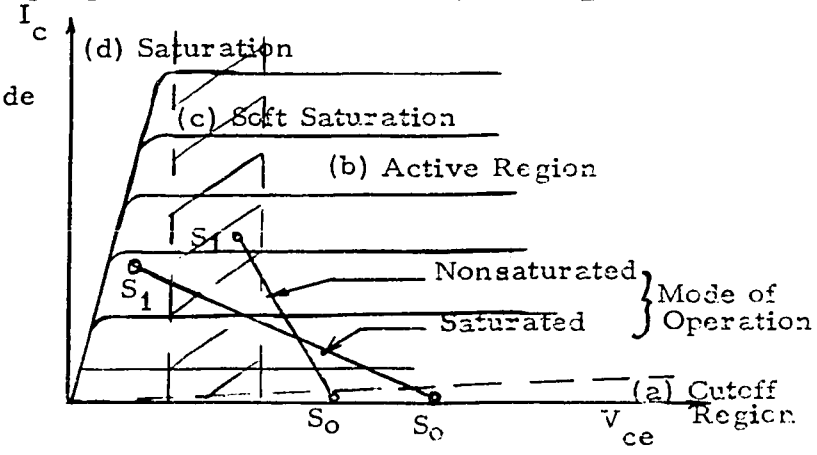


Fig. 1-9 Saturated and Nonsaturated Mode of Operation

It has been shown above that the excess stored-charge which results when one of the states of a transistor lies in the saturation region causes extra delay. Several circuit arrangements which prohibit saturation of the transistor have been developed and one way of doing this is by controlling the collector current. This can be done by designing the circuit so that the emitter current is determined by the circuit and essentially indepentent of the base drive. Circuits which use this design philosophy are called current mode logic circuits and the emitter-coupled logic is one form of this class.

1-3-d Emitter-Coupled Logic (ECL)

Figure 1-10 shows a simplified ECL circuit containing only those elements necessary for the explanation of its operation. The logical '1' and logical '0' voltage values are chosen to be more and less positive than the reference voltage V_r.

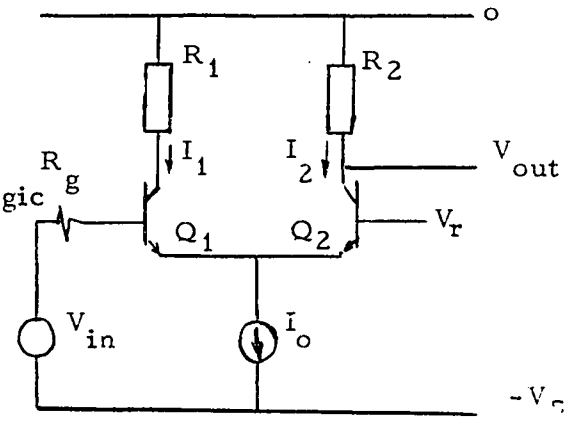


Fig. 1-10 Emitter Coupled Logic

Suppose that the input variable is '0', Q_1 will be cutoff and the current I_o will flow into Q_2. If the input variable change to '1', I_o will flow into Q_1 and no current will flow in Q_2 and as a result the output voltage changes to '1'. This behavior is summarized by Fig. 1-11.

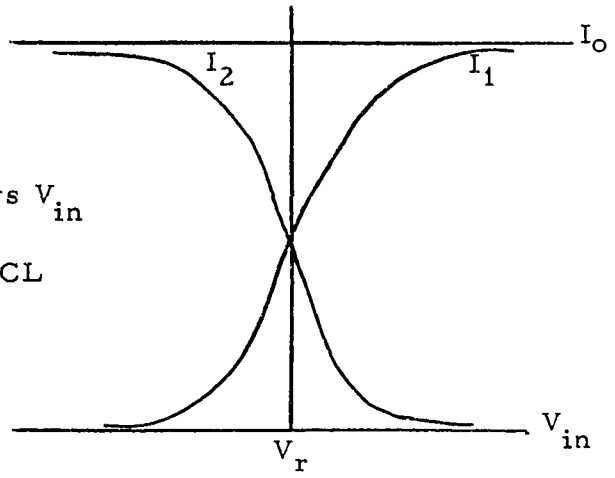


Fig. 1-11 I_{out} vs V_{in} for ECL

In general the output logic signal consists of voltage levels which vary about a reference level different from the input reference level. Direct coupling, therefore, cannot be employed unless very low logic swing is used; otherwise, coupling circuits are used to translate the output signal to the proper input level [38]. This coupling introduces extra delay and extra power dissipation, in addition to complicating the circuit and using a larger area of silicon.

Transient Analysis

In order to determine the parameters that affect the speed of ECL, which will be used in a modified form in chapter 3, a simple transient analysis is given here [39, 40, 41]. The switching of the current I_o from Q_2 to Q_1 will be analyzed with the following assumptions:

(1) The current I_o is constant.

(2) The input voltage step V is sufficient to transfer the full current I_o from Q_2 to Q_1.

(3) The current available at the base of Q_1 is $I_B = \dfrac{V - V_r}{R_g + 2r_{bb'}}$ and can be considered as a step of base current.

(4) The resultant load resistance at the output is sufficiently small, so that, the output capacitance can be neglected.

(1) Turn-on Delay Time

When Q_1 is turned on, the initial base current supplies a charge (Q_{oB}) to the emitter and collector junction depletion layer capacitances C_{te} and C_{tc} plus any stray capacitance C_s. Thus no collector current is produced until the emitter junction becomes slightly forward biased. The time required to supply this charge is the turn-on delay time and for the case of a step base current, it can be written as $(T_d)_{on} = \frac{Q_{oB}}{I_B}$ (1-9)

where $Q_{oB} = q_e + q_c$ (1-10)

q_e and q_c are the off-bias charge stored in the emitter and the collector junctions.

$$q_e + q_c = \int_{V_{ob}}^{V_J} C_{ib}\, dV_{be} + \int_{V_c - V_{ob}}^{V'_c - V_J} C_{ob}\, dV_{cb}$$

C_{ib} and C_{ob} are the input and output capacitances.

V_{ob} is the base off-bias voltage.

V_c and V'_c are the off and on collector voltage.

V_J is the base junction voltage.

Note that $V_c = V'_c$ and q_c is minimum if $R_1 = 0$ and in this case $(T_d)_{on}$ is minimum.

(2) Turn-on Transition Time (Rise Time)

In order to turn on a transistor, sufficient charge must be supplied to do the following:

(1) Establish the proper carrier gradient in the base region to permit the desired collector current ($\approx I_o$) to flow. This charge is called Q_B and is given by $Q_B \approx I_o\ T_o$ (1-11)

where $T_o \equiv$ the characteristic time constant of the transistor $= (2\pi f)^{-1}$

$f \equiv$ the gain-band width product.

(2) Allow for recombination, this charge is called Q_R

$$Q_R = \int_o^{T_{on}} \frac{q_b}{T_B} \, dt \qquad (1\text{-}12)$$

The turn-on transition time(T_{on}) is given by

$$T_{on} = (Q_B + Q_R) / I_B \qquad (1\text{-}13)$$

For rapid changes of base current, the recombination component Q_R can be neglected, and in this case:

$$T_{on} = I_o T_o / I_B \qquad (1\text{-}14)$$

To keep (T_{on}) minimum, T_o should be kept small by operating the transistor away from partial saturation (see section 1-3-b). Note that increasing I_B will increase the power dissipation.

(3) Turn-off Delay Time (Storage Time)

Turn-off delay time results from a transistor being driven into saturation. The input charge must equal the internal charges:

(a) The excess base charge. The amount of this charge will be called Q_s and is proportional to the excess base current I_{bs},

$$Q_s = I_{bs} \; T_s \qquad (1\text{-}15)$$

where T_s is the saturation time constant.

(b) The recombination charges, Q_{Rs} caused by recombination of the excess carriers and Q_{Ra} caused by recombination of the active carriers.
For a step of reverse current I_B:

$$I_B(T_d)_{off} = Q_s + Q_{Rs} + Q_{Ra} \qquad (1\text{-}16)$$

In ECL, the transistors are in the active region and therefore $Q_s = o$ and $Q_{Rs} = o$, so:

$$(T_d)_{off} = \frac{Q_{Ra}}{I_B}$$

$$= \frac{I_o T_a}{I_B} \qquad (1\text{-}17)$$

where T_a = lifetime of the active charge.

(4) Turn-off Transition Time (Fall Time)

Similiar expression to equation (1-14) can be derived for the turn-off transition time (T_{off}).

$$T_{off} = \frac{I_o T_o}{I_B} \qquad (1\text{-}18)$$

1-3-e Design of Integrated Logic Circuits

The strong connection between integrated electronics and logic circuits is demonstrated by the proportion of integrated circuits designed and built for digital applications[42]. Therefore, some design parameters and cost functions must be modified to take integrated circuit realization into consideration. For example, the cost function should be based on the silicon area used for realization rather than the number of gates. Saving of silicon area can be achieved; e.g., by considering the realization of a compound logic operation (AND-OR, OR-AND,.....) instead of realizing one logic operation at a time. However, most of the design parameters used for discrete circuit realization; e.g., the power-delay time product, noise margins and fan-numbers are also applicable to integrated circuits[26].

All these parameters can be conveniently combined in one figure (Logic Circuit Figure of Merit, LCFM):

$$LCFM = \frac{(NM)\ (FO)\ (FI)}{(SA)\quad (P)\quad (D)} \qquad \text{per logic performed}$$

(NM) = Average noise margin mV

(FO) = Max Fan-out number

(FI) = Max Fan-in number

(SA) = Silicon area used to realize the logic performed mil^2

(P) = Total power dissipated mW

(D) = Total average delay time n sec

For example, if we have two circuits which perform the logic functions AND-OR:

Circuit I	Circuit II	
(NM) = 300	200	mV
(FO) = 3	3	
(FI) = 3	3	
(SA) = 100	150	mil^2
(P) = 50	60	mW
(D) = 3	1.5	n sec

then $(LCFM)_I$ = 18% per AND-OR

$(LCFM)_{II}$ = 13% per AND-OR

Although a single figure of merit is defined above, it is not absolute and for different system requirements (low power, high speed,.... or high noise margins) the figure of merit will change accordingly.

CHAPTER 2

Designing High Speed Logic Systems Using the Predetermination Concept

It was stated in the previous chapter that a parallel logic system is faster than a serial system. However, in a practical system, there are circuit limitations; e.g., fan-in, fan-out capability, the number of connections on a circuit package and the complexity of the interconnection pattern. Figure 2-1 shows the effect of fan-in on the delay of a single gate of Motorola ECL's (MECL's) [43]. Increasing the fan-in number, the delay time increases especially so for high speed gates (MECL III).

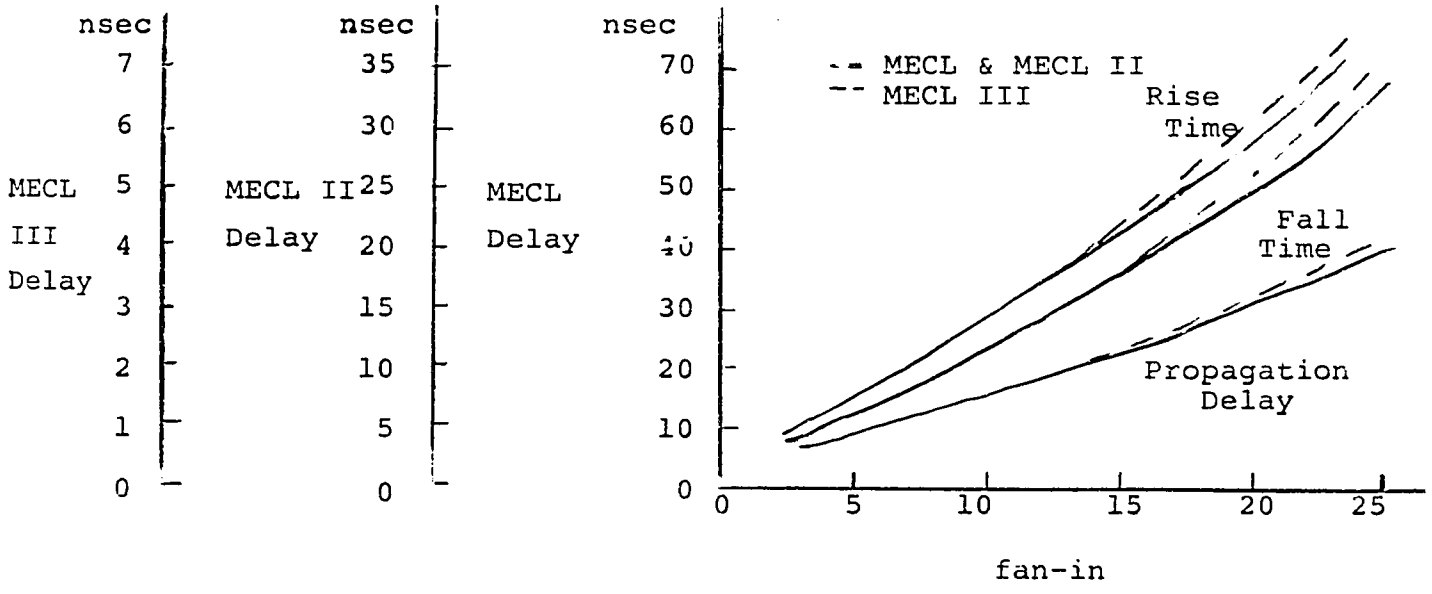


Fig. 2-1 MECL Circuit Speed vs Fan-in

As a result, a system of fully parallel logic may not be optimum, especially if a high fan-in number is required. The partitioning of a system into logic blocks, whose logic function is controlled by previous logic operations (predetermined logic system), offers the possibility of designing high speed logic systems within the above circuit limitations. If the partitioning is on the basis of the time of arrival of inputs, minimum delay systems can be designed.

In this chapter, we describe a technique for designing such a system. The Karnaugh-map is used as a logic design tool and only single output combinatorial logic circuits are considered. An iterative-multiplier cell is given as a design example. The basic logic block of such a system is suitable for current mode realization and this is considered in the next chapter.

2-1 High Speed Logic Design

Logic systems designed to perform specific logic operations at high speed have been studied [45,46,47,48,49,50]. Asynchronous circuits are used in some systems [50], and as indicated in section 1-1 asynchronous circuits have stability problems. Here we shall consider only single output combinatorial circuits and a generalized design procedure applicable to such circuits is given. Consider a single output combinatorial circuit with n inputs ($x_1, x_2, \ldots\ldots x_n$) and an output z (Fig. 2-2).

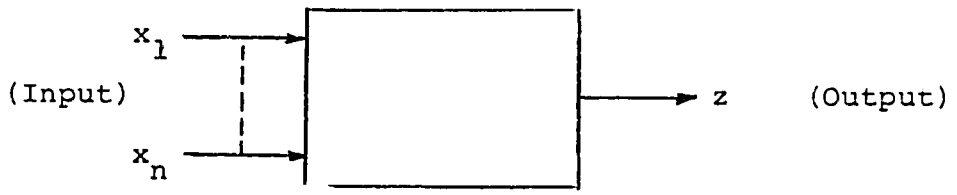


Fig. 2-2 Single Output Combinatorial Circuit

The inputs can be partitioned into N groups or sub-input sets $(I_1, I_2, \ldots I_N)$ where the sub-input set I_i contains n_i inputs as shown in Figure 2-3.

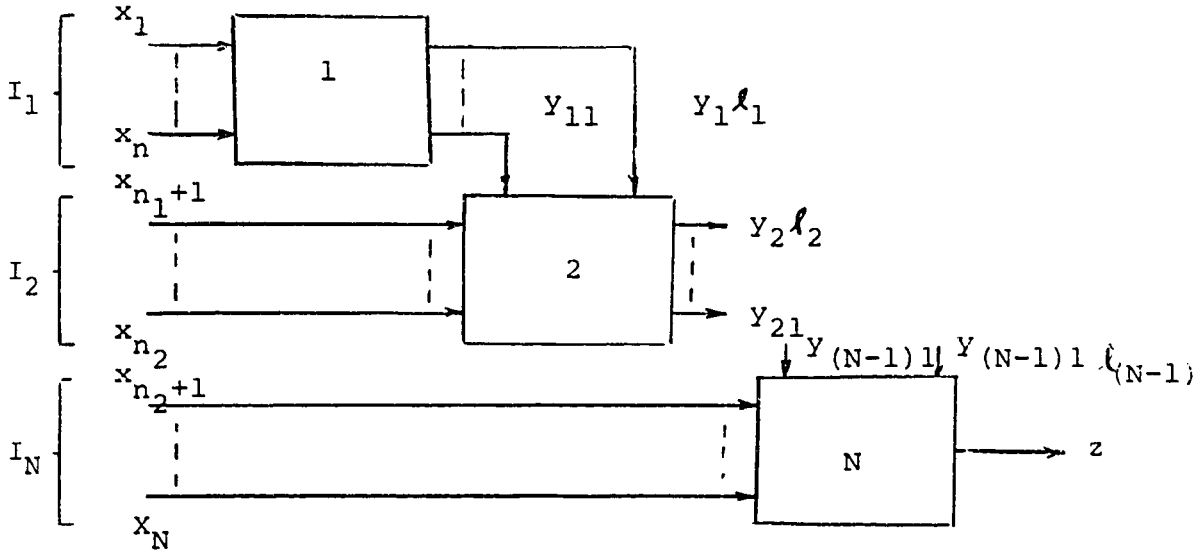


Fig. 2-3 Partition into N Blocks

The partitioning can be on the basis of any desired criteria. It can be based on the fan-in capability of the circuits used, or the simplicity of the logic building block. Some methods of simplifying the realization are based on the decomposition of the switching function [52,53] and others on using a single simple building block [54,55]. Alternatively, if the delay per logic operation and the signal path can be estimated from the overall system design, the partitioning can be on the basis of the time of arrival of the inputs and a minumum delay system can be designed. In this case the time sequence is assumed to be $I_1, I_2, \ldots I_N$. The outputs of a block are called intermediate outputs or control functions and are labled $Y_{i1}, \ldots Y_{i\ell_i}$ for the ith block where ℓ_i is the number of the control functions. The control functions are used as control inputs to the next block. The design procedure is now summarized and followed at each step by a generalized example.

2-2 Design Procedure

Step 1 Procedure:

Starting with the truth table, the Karnaugh-map is used to plot the function as a partition with two blocks [$(x_1, x_2, \ldots, x_p)$, $(x_{p+1}, x_{p+2}, \ldots, x_n)$].

Example:

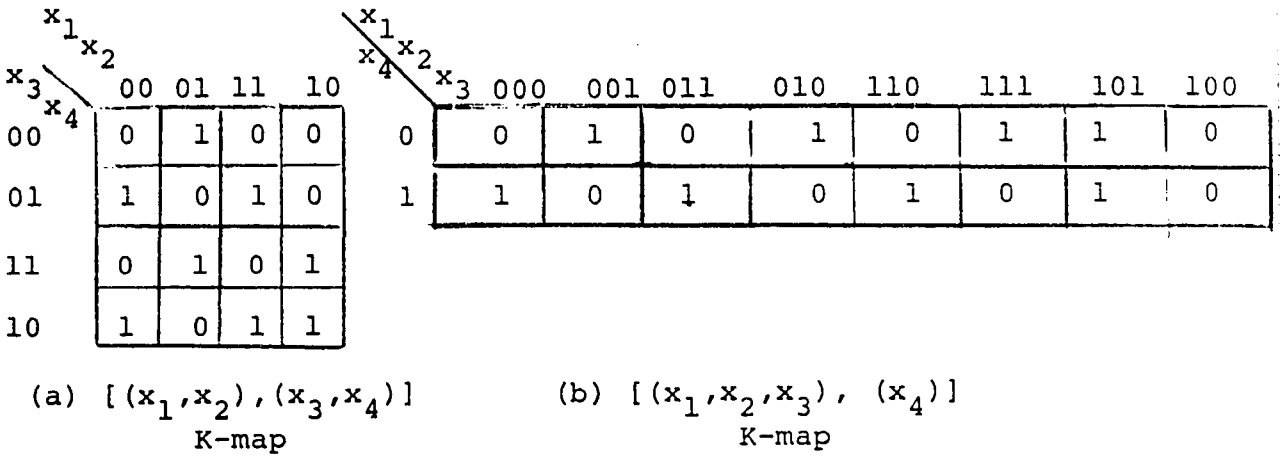
Table 1 shows the truth table of a 4 variable function. In Fig. 2-4 two different partitions are made.

(a) [(x_1, x_2) , (x_3, x_4)]

(b) [(x_1, x_2, x_3) , (x_4)]

Table 2-1: Truth table of a 4 variable function

x_1	x_2	x_3	x_4	z (output)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



x_3x_4 \ x_1x_2	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	0	1	0	1
10	1	0	1	1

(a) $[(x_1,x_2),(x_3,x_4)]$ K-map

x_4 \ $x_1x_2x_3$	000	001	011	010	110	111	101	100
0	0	1	0	1	0	1	1	0
1	1	0	1	0	1	0	1	0

(b) $[(x_1,x_2,x_3),(x_4)]$ K-map

Fig. 2-4 K-map for example 1

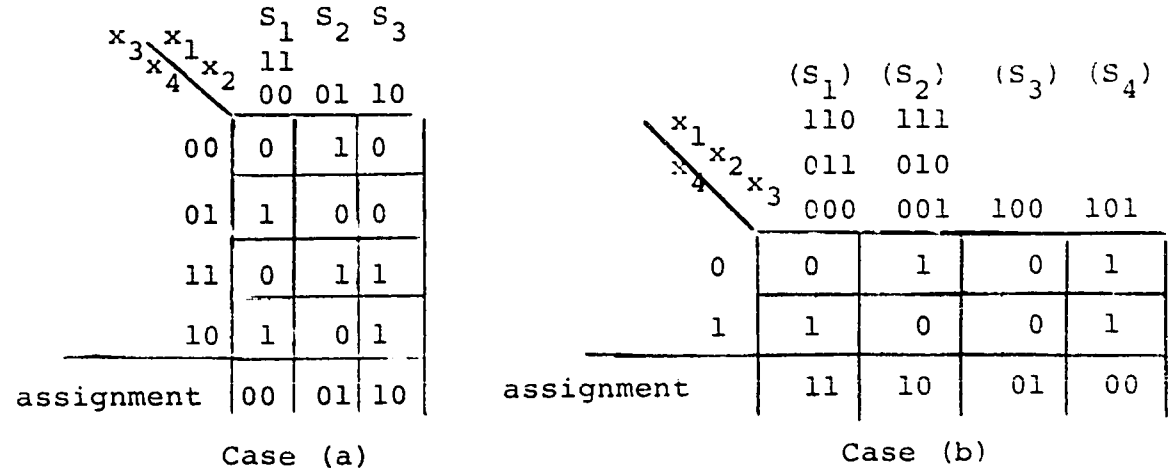
Step 2 Procedure:

If similar columns in the k-map are defined as the columns where 0's and 1's occur in the same positions, the k-map is reduced to control function map (C-map) by combining similar columns. Each column in the C-map is called a state (S) and an assignment is given to each state.

This assignment problem is similar to the assignment problem which has been studied in sequential circuits [56,57].

Example:

Fig. 2-5 shows the C-maps of example 1 and only the simplest assignments are given.



x_3x_4 \ x_1x_2	S_1 00	S_2 01	S_3 10
00	0	1	0
01	1	0	0
11	0	1	1
10	1	0	1
assignment	00	01	10

Case (a)

x_4 \ $x_1x_2x_3$	(S_1) 000	(S_2) 001	(S_3) 100	(S_4) 101
	110	111		
	011	010		
0	0	1	0	1
1	1	0	0	1
assignment	11	10	01	00

Case (b)

Fig. 2-5 C-maps for example 1

Step 3 Procedure:

The control function (y) can be expressed, according to the assignment given, as function of $(x_1, x_2, \ldots, x_p)$. For each state the output z is expressed as function of $(x_{p+1}, \ldots x_n)$.

Example:

[a] $y_{11} = x_1 \bar{x}_2$

$y_{12} = \bar{x}_1 x_2$

In state S_1 : $z = x_3 \bar{x}_4 + \bar{x}_3 x_4$

In state S_2 : $z = x_3 x_4 + \bar{x}_3 \bar{x}_4$

In state S_3 : $z = x_3$

[b] $y_{11} = \bar{x}_2 + x_1 x_2$

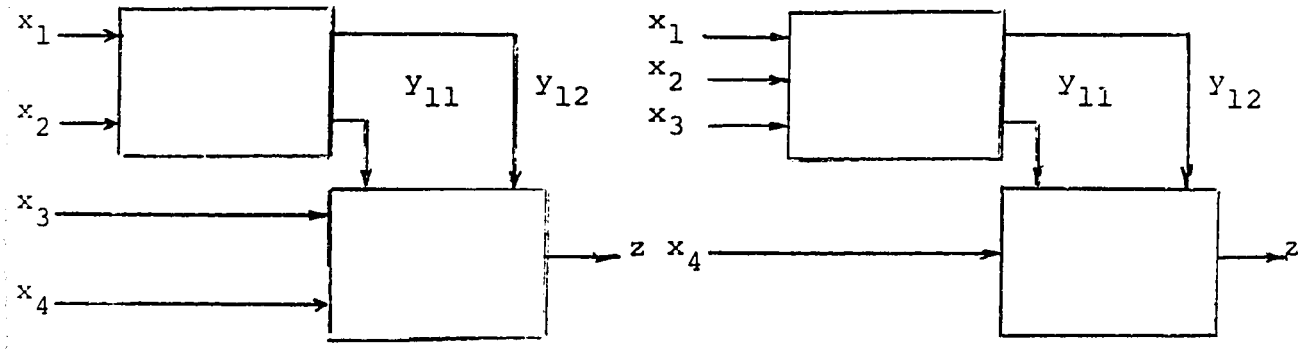
$y_{12} = \bar{x}_2 \bar{x}_3 + x_1 x_2 \bar{x}_3 + \bar{x}_1 x_2 x_3$

In state S_1 : $z = x_4$

In state S_2 : $z = \bar{x}_4$

In state S_3 : $z = 0$

In state S_4 : $z = 1$



Case (a) Case (b)

Fig. 2-6 Block Realization of example 1

Figure 2-6 shows the realization of the example with two blocks. Since the partition is assumed to be done on the basis of the time sequence of the inputs, there is no need to examine other partitions.

In the above realizations, the output is realized as a function of the direct inputs and the control functions:

Case [a]

$$z = (\bar{y}_{11})\ (\bar{y}_{12})\ (x_3\bar{x}_4+\bar{x}_3x_4) + (\bar{Y}_{11})\ (Y_{12})$$

$$(x_3x_4 + \bar{x}_3\bar{x}_4) + (Y_{11})\ (\bar{y}_{12})\ (x_3)$$

where $Y_{11} = x_1\ \bar{x}_2$

$$y_{12} = \bar{x}_1\ x_2$$

Case [b]

$$z = (y_{11})\ (y_{12})\ x_4 + y_{11}\ \bar{y}_{12}\ \bar{x}_4 + \bar{Y}_{11}\ \bar{y}_{12}$$

where $y_{11} = \bar{x}_1 + x_1\ x_2$

$$y_{12} = \bar{x}_2\ \bar{x}_3 + x_1\ x_2\ \bar{x}_3 + \bar{x}_1\ x_2\ x_3$$

Note that these are expanded versions of a two level realization (sum-of-products or product-of-sums form).

Step 4 Procedure:

The above procedure yields a partition with two blocks only. If more than two blocks are desired it can be repeated on the first of the two blocks, considering each control function at a time.

Example: Only case (b) is considered, since the first block, case(a), has two inputs.

Figure 2-7 shows a 3 block realization of our example. In this case the function is expressed in the form:

$$z = (\bar{y}_{21})(y_{22}x_3 + \bar{y}_{22}\bar{x}_3)(x_4) + (\bar{y}_{21})(\bar{y}_{22} + \bar{x}_3)(y_{22} + x_3)(\bar{x}_4)$$

$$+ (y_{21})(\bar{y}_{22} + \bar{x}_3)(y_{22} + x_3)$$

[(x_1x_2), (x_3)] k-map for Y_{11}

x_3 \ x_1x_2	00	01	11	10
0	1	1	1	0
1	1	1	1	0

C-map

	(S_1)	(S_2)
x_3 \ x_1x_2	11 01 00	10
0	1	0
1	1	0
assignment	0	1

$Y_{21} = x_1 \bar{x}_2$

In S_1 : $y_{11} = 1$

In S_2 : $y_{11} = 0$

$y_{11} = \bar{y}_{21}$

[(x_1,x_2), (x_3)] k-map for y_{12}

x_3 \ x_1x_2	00	01	11	10
0	1	0	1	1
1	0	1	0	0

C-map

	(S_1)	(S_2)
x_3 \ x_1x_2	01 00	10 11
0	0	1
1	1	0
assignment	1	0

$y_{22} = \bar{x}_1 x_2$

In S_1 : $y_{12} = x_3$

In S_2 : $y_{12} = \bar{x}_3$

$y_{12} = y_{22} x_3 + \bar{y}_{22} \bar{x}_3$

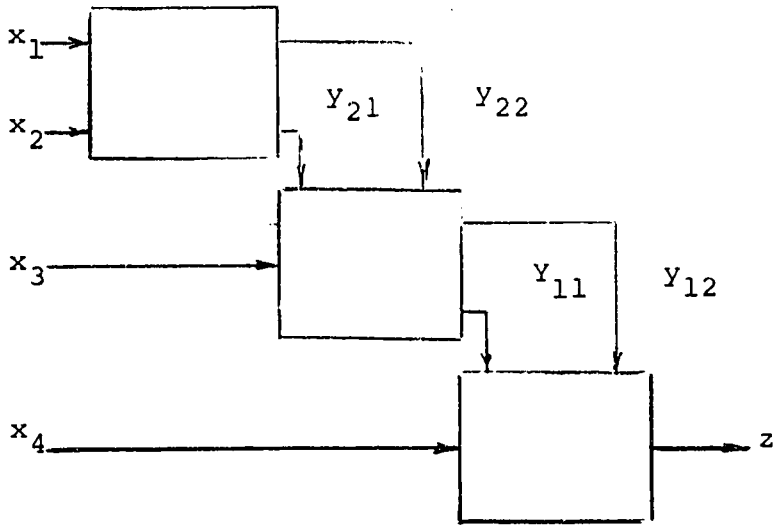


Fig. 2-7 3 Block Realization of example 1

After the general example given above the procedure is applied to two particular examples, a module for a ripple-through adder with a fast carry and a module for an iterative multiplier.

2-3 Ripple-through Adder

Figure 2-8 shows a block diagram for part of a ripple-through adder.

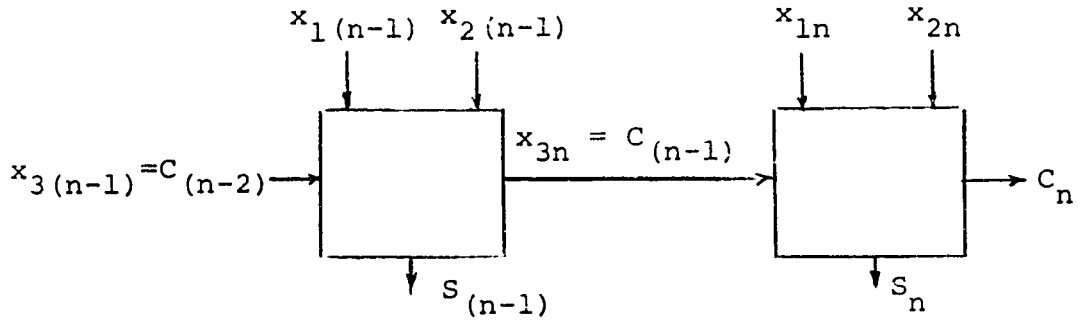


Fig. 2-8 Ripple-through Adder

It is evident that the time taken for the S_n, the nth sum, to reach its final value is given by:

$$T_{sn} = T_s + (n-1)\ T_c$$

where T_s and T_c are the delay times for the sum and carry, in a single module, because it is assumed that x_1 and x_2 are available immediately.

The carry output above will be considered, since the above expression is most sensitive to the value of T_c. Figure 2-9 shows a two block realization, where the carry is expressed as

$$z = \bar{y}_{11}\ \bar{y}_{12}\ x_3 + y_{11}\ \bar{y}_{12}$$

Truth table

x_1	x_2	x_3	z (carry)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$[(x_1,x_2),(x_3)]$ K-map

x_3 \ x_1x_2	00	01	10	11
0	0	0	0	1
1	0	1	1	1

$[(x_1,x_2),(x_3)]$ C-map

x_3 \ x_1x_2	00	01 10	11
0	0	0	1
1	0	1	1
assignment	01	00	10

(S_1) (S_2) (S_3)

S_1: Carry = 0

S_2: Carry = x_3

S_3: Carry = 1

$$y_{11} = x_1\ x_2$$

$$y_{12} = \bar{x}_1\ \bar{x}_2$$

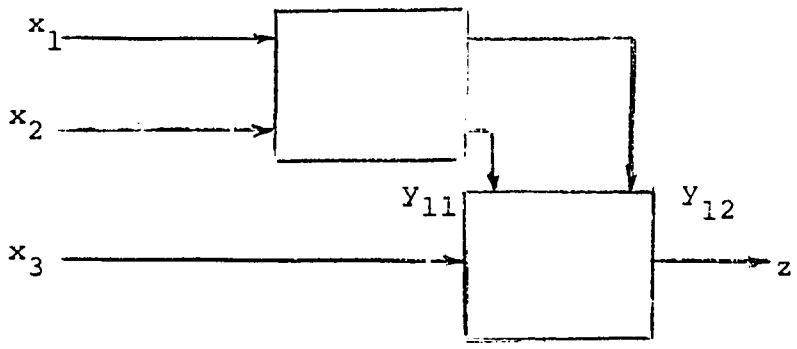


Fig. 2-9 Carry of a Ripple-through Adder

2-4 An Iterative Multiplier Module

In the above example, the sequence of arrival of the input variables is determined by inspection.

A more complicated system is chosen for the second particular example, an iterative multiplier, composed of similar modules [58]. In order to determine the sequence of inputs for the module the overall system must first be studied.

The multiplier is of the form shown in (Fig. 2-10) and carries are proragated both horizontally and vertically.

It can be shown that the time it takes the carries to reach any point is given by:

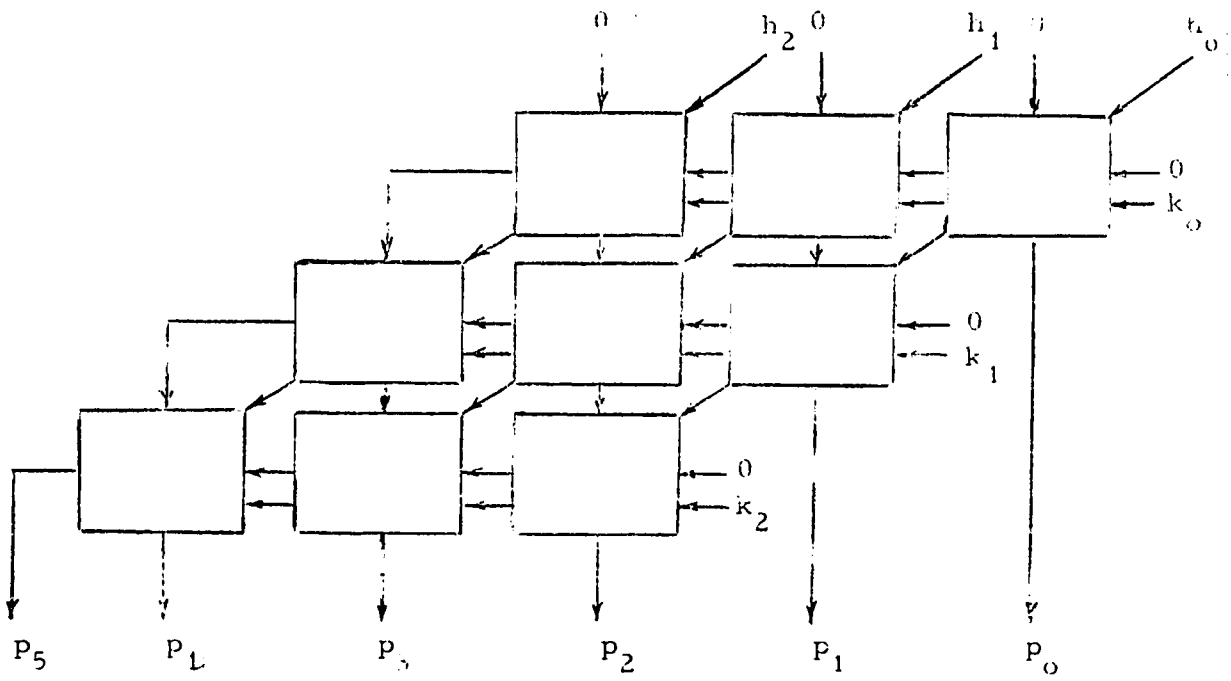
$$T = (n - 1)\, h + (m - 1)V$$

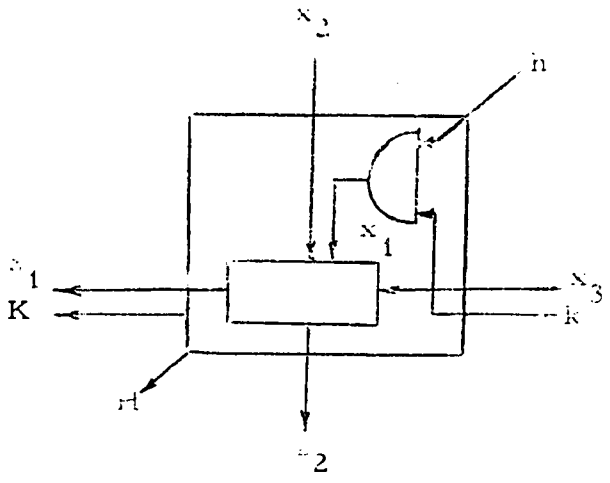
where

h is the horizontal delay

V is the vertical delay

n and m ar the horizontal and vertical positions of the module in the system.





Multiplier Cell

x_1 = hk

x_2 = previous sum

x_3 = previous carry

H = h

K = k

z_1 = carry of $(x_1 \oplus x_2 \oplus x_3)$

z_2 = $(x_1 \oplus x_2 \oplus x_3)$

Fig. 2-10 A 3 bit iterative multiplier.

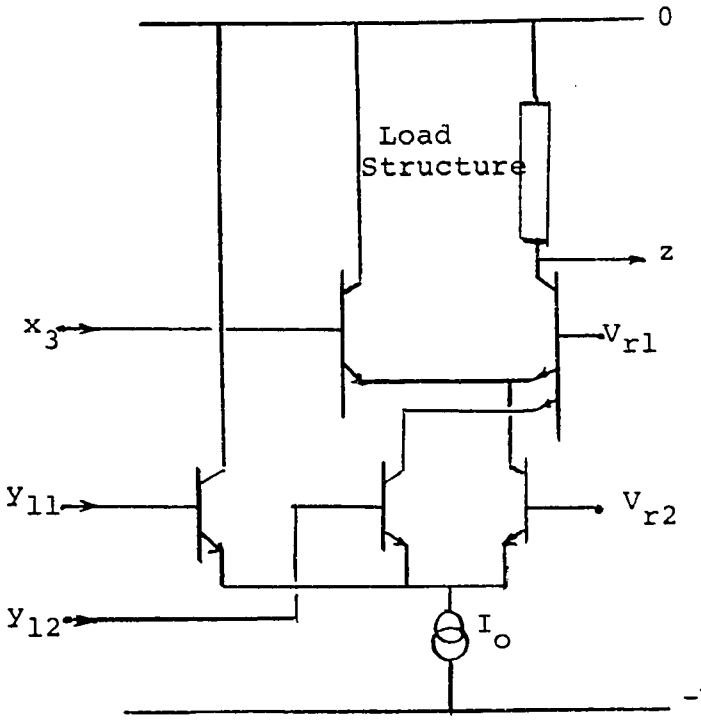
If N is the number of the bits, then it follows that the total delay is

$$T_N = (2N - 1)\, h + (N - 1)V$$

The sequence of arrival of the vertical and horizontal carries cannot be known in advance. However because h_i and k_i are available before the carries, their product can be used as a control function. The module now becomes a full adder with two input variables and a single control function.

2-5 Circuit Realization

Because the logic blocks employed in systems designed using the predetermination concept have both direct and control inputs, a two-level current mode realization is applicable [59]. The control inputs may be applied to one level and the direct inputs to the other. Figure 2-11 shows a realization for the carry output of the ripple-through adder of Figure 2-9.



	S_1	S_2	S_3
$y_{11}y_{12}$	01	00	10
z	0	x_3	1

Fig. 2-11 Two-level Current Mode Realization of Fig. 2-9

Note that the control inputs are applied to the lower level transistors and the direct input to the upper. V_{r1} and V_{r2} are reference voltages for the upper and lower levels respectively. The inputs x_3, y_{11} and y_{12} steer a single current I_o to the load structure.

2-6 Conclusions

The general procedure, demonstrated above, allows a high speed combinatorial logic system to be designed by partitioning on the basis of sequence of arrival of input variables and reducing the fan numbers. Multi-output systems can be partitioned by considering a single output at a time. The determination of the sequence of arrival is straightforward in iterative systems.

The concept of control functions determining the logic operation of a gate appears to be suitable for multi-level current mode logic realization and in the next chapter such realization is considered.

CHAPTER 3

A Current Mode Logic Circuit for Predetermined Logic Systems

It is shown in chapter 2, that the application of the predetermination concept allows the design of high speed logic systems within typical circuit limitations. The basic block of such a system is shown in Figure 3-1, where the control inputs predetermine the logic performed by the block and it is always assumed that the control inputs are available before the direct inputs.

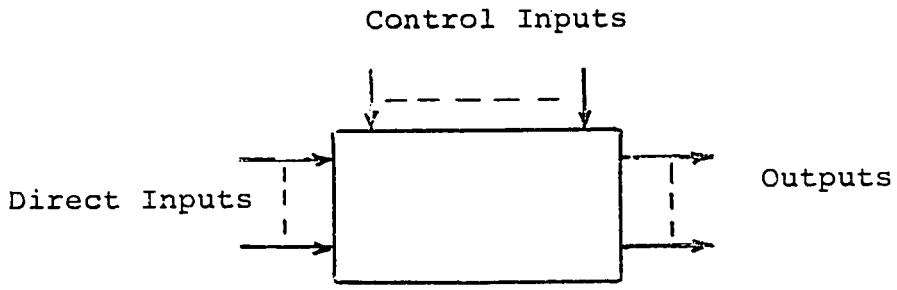


Fig. 3-1 The Basic Building Block of Predetermined Logic Systems

Thus a logic circuit in which one part controls the function performed by another part is required for the realization of such a block. Since in general, a current mode logic (CML) circuit represents the fastest circuit configuration, as

indicated in section 1-3, it is reasonable to realize the block as a two level emitter coupled circuit (ECL) in which the lower level transistors control the logic performed by the upper level.

This chapter relates the circuit requirements of a predetermined logic system to circuit design, and an ECL realization which uses a novel load structure is described.

3-1 Circuit Requirements

The primary requirements for logic circuits suitable for the predetermined system are listed below, with a few words of explanation.

(1) Speed

High speed is a primary requirement for many logic systems, not only to perform logic operations in less time, but also because speed of operation is a critical factor in the stability of some systems. As indicated in section 1-3-e, the overall delay of a system can be used as a design criterion to indicate the speed of the circuits.

(2) Logic Swing and Noise Margins

A compromise must be made between the requirements of high speed and reliability in the presence of noise. High speed leads to the choice of low logic levels, while reliability requires high noise margins and high logic swing. The noise margins are also affected by the theshold width as indicated in section 1-2.

(3) Power Dissipation

To allow high degree of packaging, the power dissipation should be kept to a minimum.

(4) Integration and Cost

One advantage of medium and large scale integration is low cost. Thus to be acceptable, the circuits should be fully integratable.

(5) Logical Flexibility

The circuits should have the logical flexibility demanded by a predetermined logic system; i.e., they are suitable for realizing standard building blocks.

3-2 Circuit Design

From the above circuit requirements, the following design approach is considered.

(1) An ECL circuit with high speed transistors [60,61] is designed to meet the high speed requirement. Only one collector load is used to reduce the effects of base width modulation and collector base capacitance. The DC coupling stage is ellimi-nated, with the advantage of decreasing both the total delay and the power dissipation (section 1-3-b and 1-3-d).

(2) The small logic swing with reasonably high noise margins requires a close control of the logic levels and the threshold region. Thus a DC load line which defines these levels with minimum tolerance is required. The non-linear load structure meets this requirement and is considered in section 3-5.

(3) The current source of the ECL is used to perform as many logic operations as possible, with the advantage of reducing the total power dissipation.

(4) The circuit is fully integratable. The logic performed per unit area of the silicon chip is kept high, because the realization is based upon logic building blocks rather than separate gates.

(5) A two-level ECL with non-linear load is used for the realization of the building blocks of a predetermined logic system. The fan-in and the fan-out are chosen to be three which results in adequate logic flexibility for the logic system (chapter 2).

3-3 Single Level ECL Circuit

The function block of a predetermined logic system is one without control inputs and a single level ECL is used for its realization. Assuming the input variables and their complements are available, an OR-AND circuit will be suitable for realizing such a block (Fig. 3-2), where the output is expressed as:

$$Z = (x_1 + x_2 + x_3)\ (x_4 + x_5 + x_6)\ (x_7 + x_8 + x_9)$$

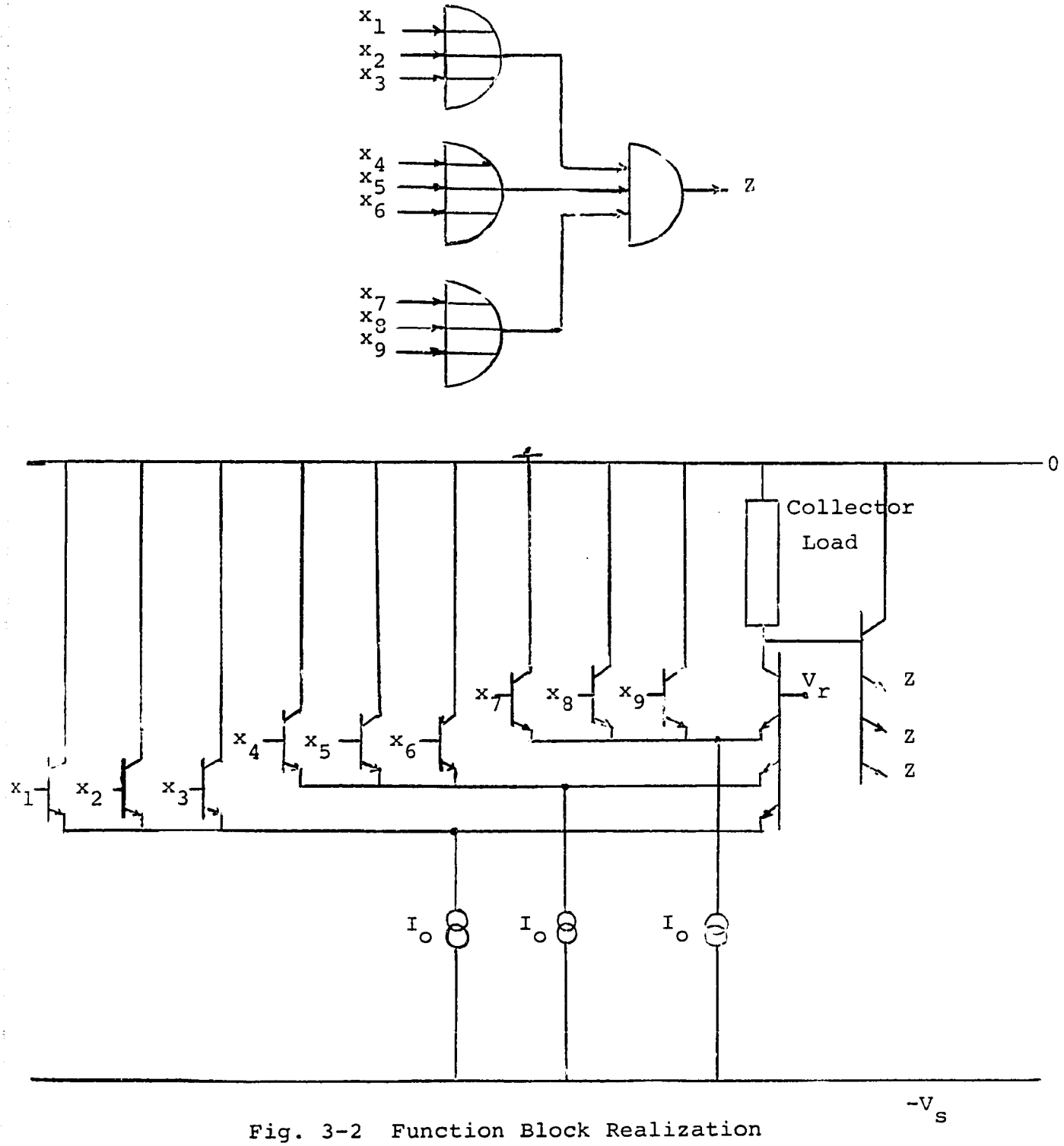


Fig. 3-2 Function Block Realization

Only three current sources are used to realize this function while the usual realization with four separate gates needs four current sources, one for each gate. Designing the fixed bias transistor (with V_r as a reference voltage) as multiemitter device results in a saving of silicon area.

3-4 Two Level ECL Circuit

Figure 3-3 shows a two level ECL circuit, where y_1, y_2 and y_3 are the control inputs and x_1, x_2, ... x_6 are the direct inputs. The control inputs can have the assignments 000, 100, 010 and 001 representing four states. The other assignments 110, 011, 101 and 111 are excluded because of sharing the current I_o among the upper levels. Then, the output Z is given by

$$Z = \bar{y}_1 \bar{y}_2 \bar{y}_3 + y_1 \bar{y}_2 \bar{y}_3 (x_1 + x_2 + x_3) + \bar{y}_1 y_2 \bar{y}_3 (x_4 + x_5 + x_6)$$

The direct and the control inputs may be increased to more than six and three respectively, but this represents a technology and packaging problem [62,63].

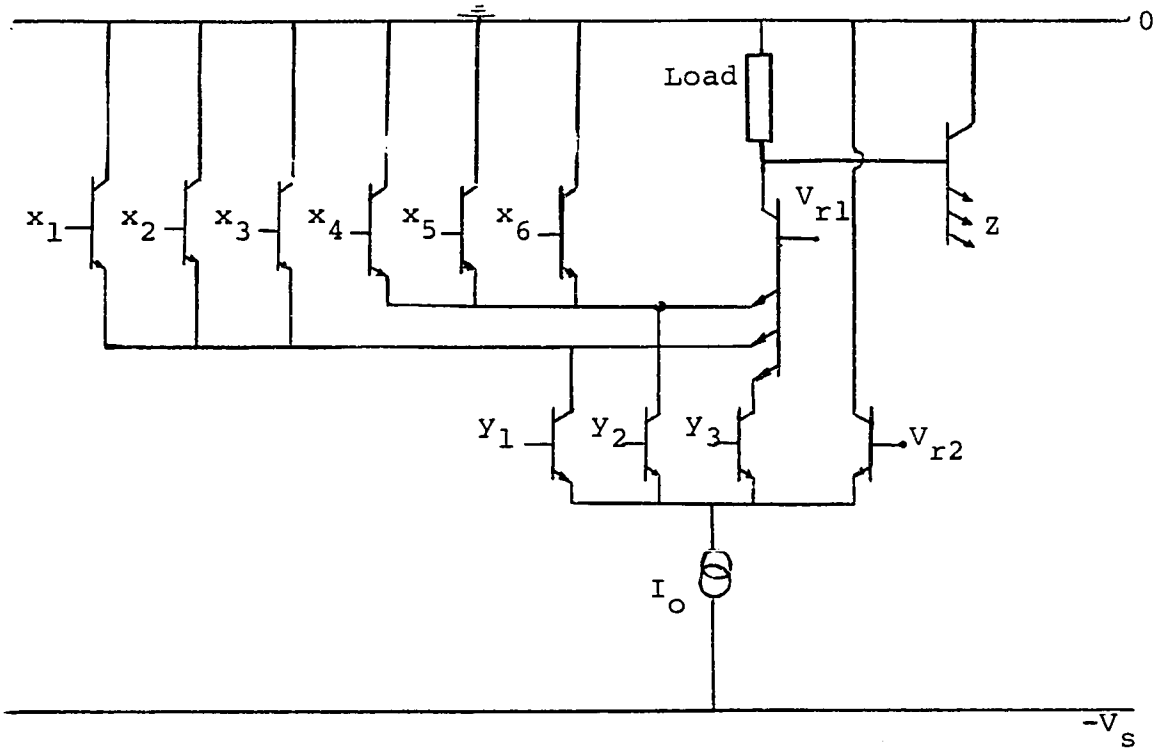


Fig. 3-3 Two Level ECL Circuit Realization

The above two realizations of single and two level ECL have a common input-output circuit structure as shown in Fig. 3-4.

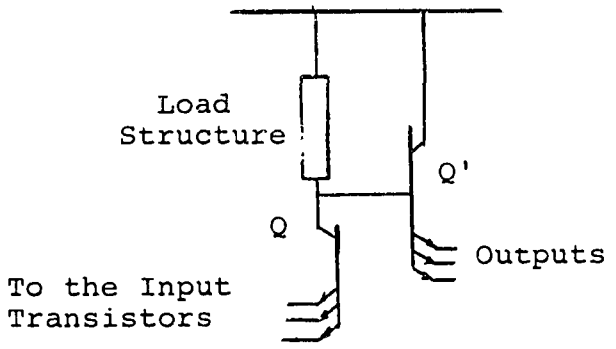


Fig. 3-4 Input-Output Structure
for Single and Two Level ECL

It consists of two multiemitter transistors; a fixed bias transistor Q, each of its emitter is connected to an input transistor and a fixed collector-voltage transistor Q', its base is connected to a single load. The inputs are connected, directly or through a second level, to current sources, one for each emitter. The current source realization is considered in chapter 4.

3-5 Load Structure

When integrated ECL circuits are used in the realization of logic blocks, it should be possible to synthesize the optimum integratable load structure. Most of the integrated ECL circuits presently in use employ diffused resistors as collector loads [64, 65]. In discrete circuits, advantages have been claimed for tunnel diodes and tunnel diode pair-resistor combinations [66], but they have not been integrated on a silicon chip.

In the following sections the static and dynamic characteristics of ECL with three alternative load lines (Fig. 3-5) are given. These are:

a) A simple linear resistance.
b) A non-linear load which can be characterized by three linear regions , two low positive resistance regions at the logic

levels (AB and CD) and a voltage controlled negative resistance region (BC).

c) A non-linear load which can be characterized by three linear regions, two low positive resistance regions as the above (AB' and C'D) and an infinite resistance region (B'C').

Note that the above represents only three cases of a continuous range of possibilities.

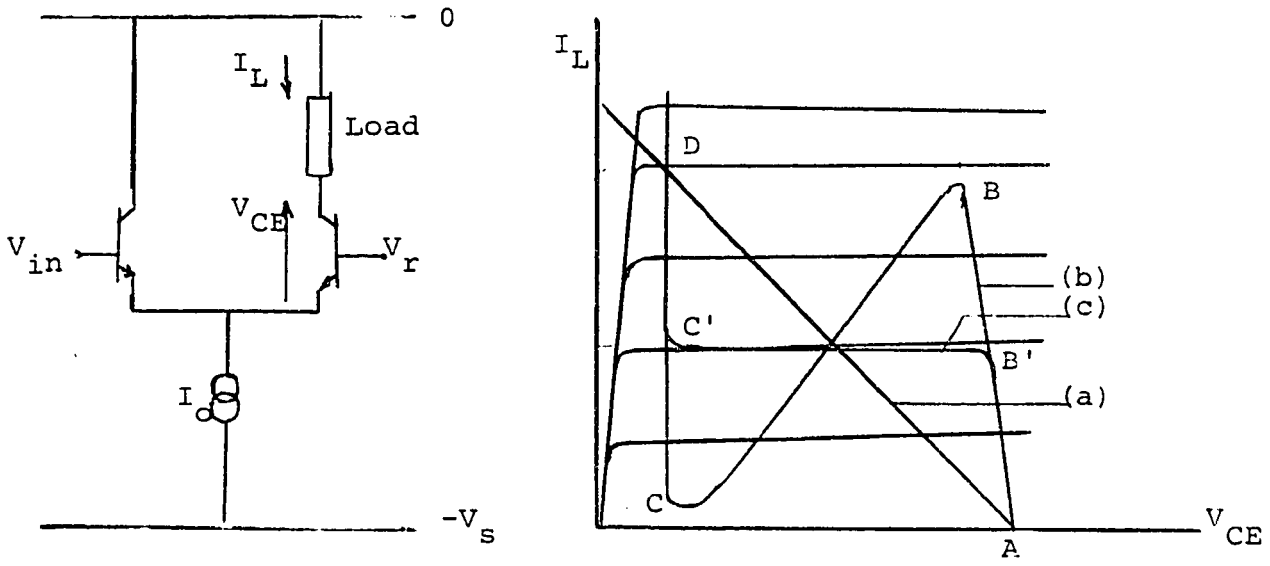


Fig. 3-5 ECL with Different Load Lines

3-6 DC Analysis of ECL with Different Load Structures

In this section the dc relationships between the voltages and currents at the various terminals of the integrated ECL with different load structure are expressed analytically. The desired relationships are:

1] The transfer characteristic (output voltage versus input voltage)

2] The input characteristic (input current versus input voltage)

3] The output characteristic (output current versus output voltage)

From these relationships the dc logic characteristic can be derived. These are the logic swing, the noise margin, the power

dissipation and the effects of tolerances on the logic performance.

1] The Transfer Characteristic

In deriving this characteristic, one begins by finding the load current I_L, at different values of input voltages. This calculation involves not only the non-linear characteristics of the switching transistors but also device tolerances and temperature variations. Assuming indentical switching transistors and constant current source I_o the current can be expressed as [67]:

$$I_L = \alpha_o I_o \; / \; 1 + m_d \exp\left[(V_{in} - V_r) \; / \; V_T\right]$$

where : α_o = common base short circuit current gain

m_d = number of driven inputs

V_T = thermal voltage

$\approx$ 25 mV at room temperature

If we assume $m_d = 1$ and $V_r = -350$ mV Figure 3-6 shows $(I_L \; / \; I_o)$ vs V_{in}.

According to the load structure, a load line is then placed on this characteristic. The V_{out} vs V_{in} can be obtained by using V_{in} vs I_L and I_L vs V_{out} plots. If it is required to take device tolerances and temperature variations into account this graphical solution can be programmed on a digital computer [68,69]. A typical (I_L/I_o) vs V_{in} is shown in Figure 3-7 with typical parameter tolerances and temperature variations taken into account [65]. Ideal load characteristics are then superimposed and the corresponding transfer characteristics are obtained. The logic and threshold levels and hence, the noise margin can be obtained from these transfer characteristics [see section 1-2]. These are compared in Figure 3-8 for the three types of load structures. As shown the infinite resistance load line reduces the threshold width and improves the noise margins, while the negative resistance load line improves each noise margin to almost the complete logic swing. However, the negative resistance load line introduces a bistable characteristic into the logic circuit with all the associated system implications.

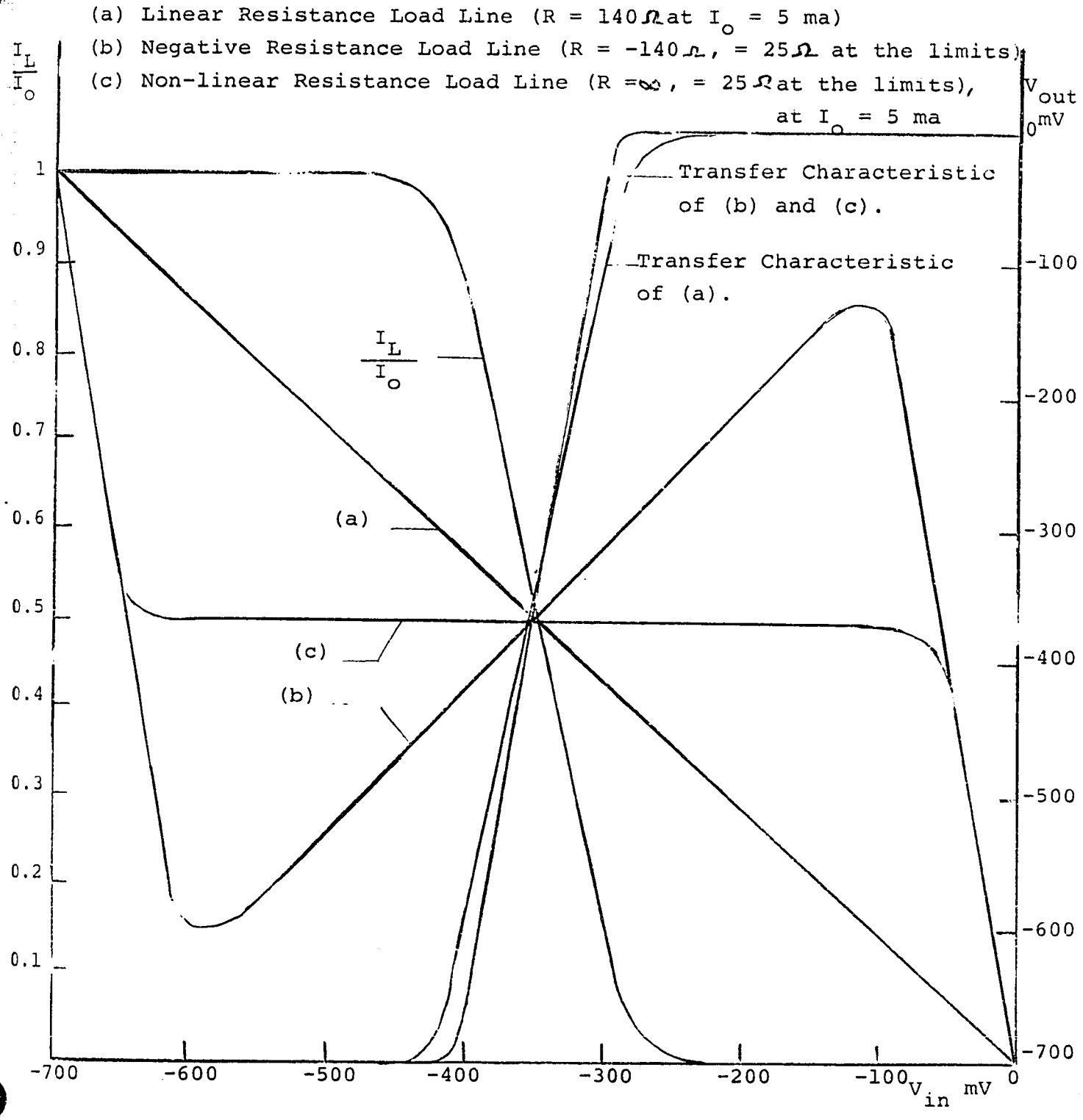


Fig. 3-6 ECL Transfer Characteristic

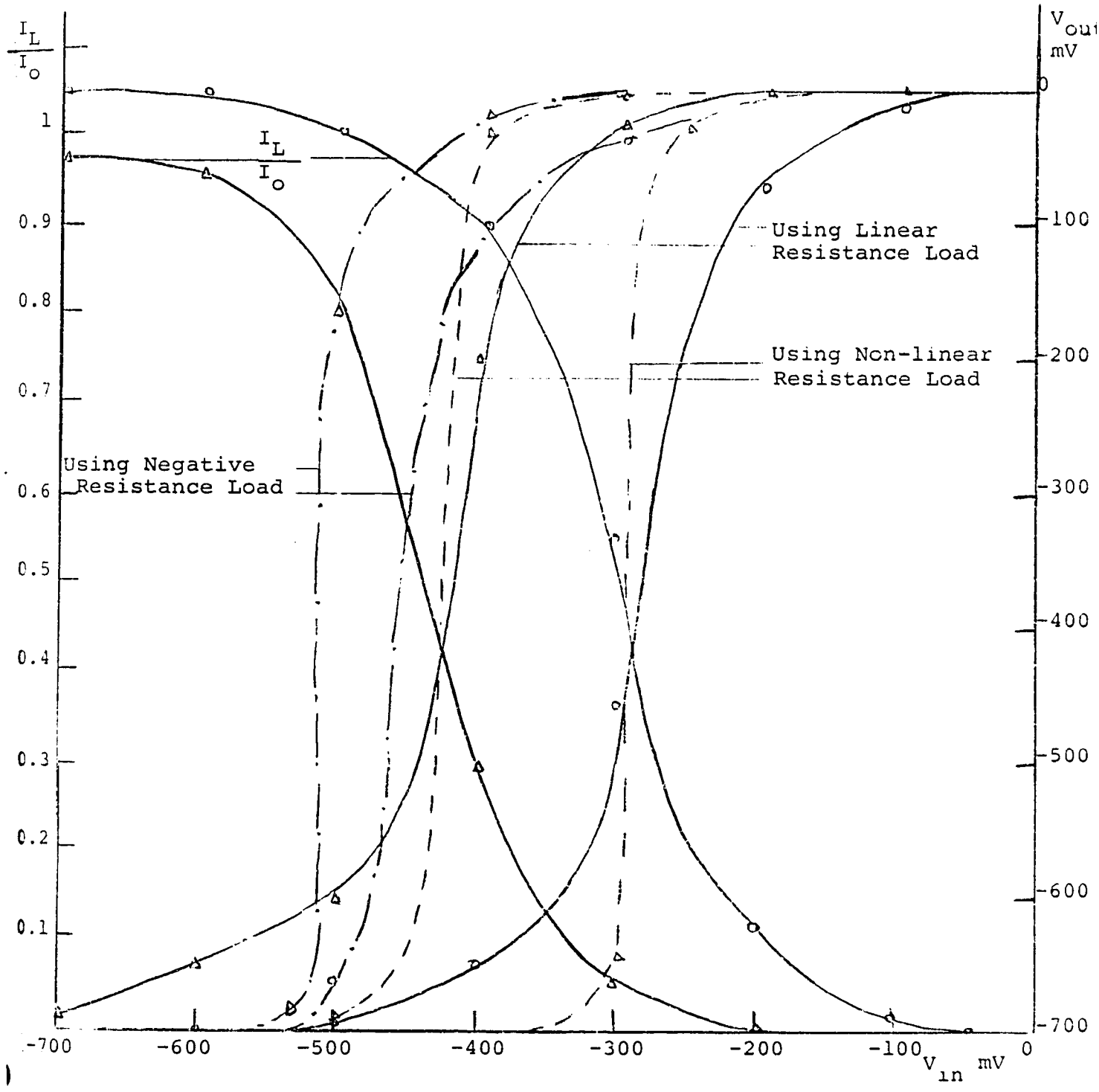
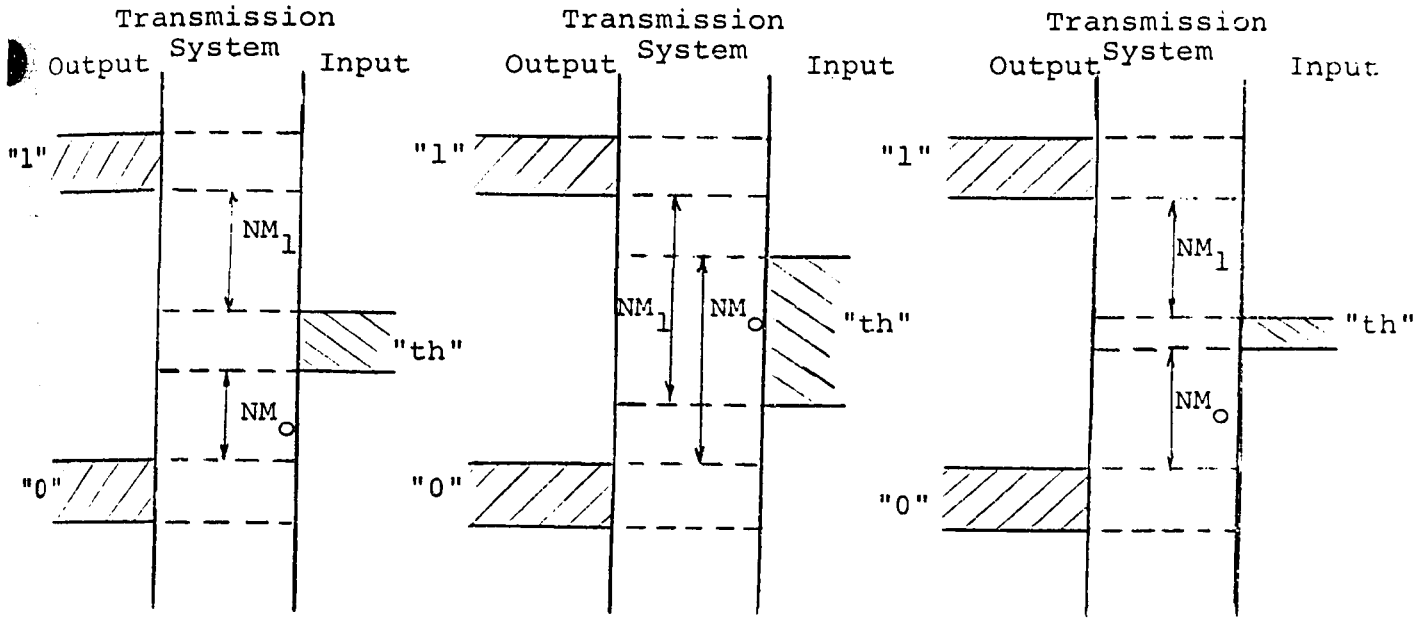


Fig. 3-7 Effect of Tolerances on Transfer Characteristics



(a) Linear Resistance Load.

(b) Negative Resistance Load.

(c) Non-linear Resistance Load

Fig. 3-8 Comparison of Logic Level and NM's for Load Lines (a), (b) and (c)

Both case (b) and (c) above have relatively precise logic levels.

2] Input Characteristics

For ideal current source I_o and $m_d = 1$, the input base current is given by [67]:

$$i_b = \frac{(1 - \alpha_o)\, I_o}{1 + e^{(V_r - V_{in})/V_T}}$$

It is clear that the input characteristic (Fig. 3-9) is independant of the load structure.

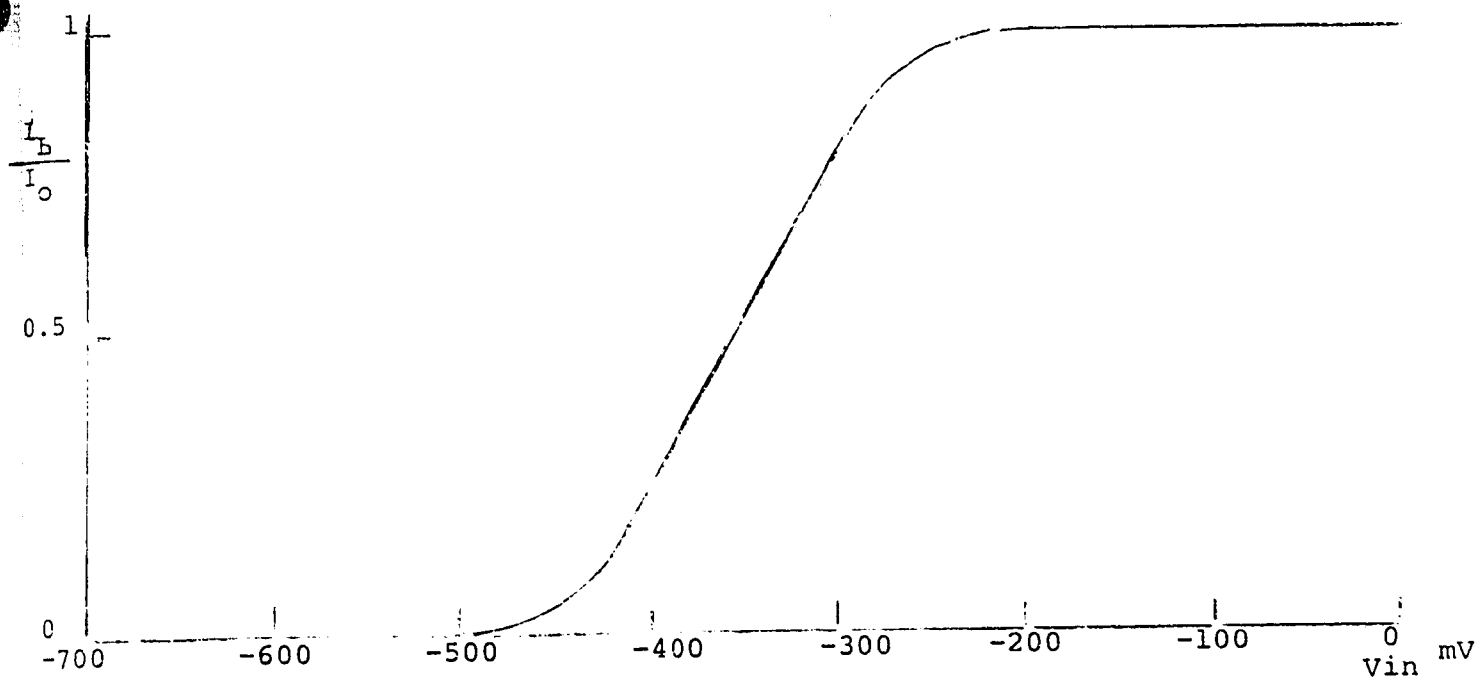


Fig. 3-9 ECL Input Characteristic

3] Output Characteristics

The output characteristic is the relationship between output current and output voltage where the output current is defined as flowing into the output terminal. The output characteristics consist of two curves, one for a logical "0" input and the other for a logical "1" input (Fig. 3-10). Together with input characteristic, the output curves are useful in estimating loading effects and dc fan-out capability of the circuit. Since in the case of a linear resistance load the output impedance is the load resistance itself, a dc fan-out limitation arises. To overcome this, an emitter follower coupling stage can be used [67], but this stage introduces extra delay in the system. Alternatively, in the case of a non-linear load line the output impedance at the two logic levels is low and a higher dc fan-out can be tolerated. In this case, the fan-out capability is limited by restrictions on transient response rather than dc considerations.

(a) Linear Resistance Load.

(b) Negative Resistance Load.

(c) Non-Linear Resistance Load.

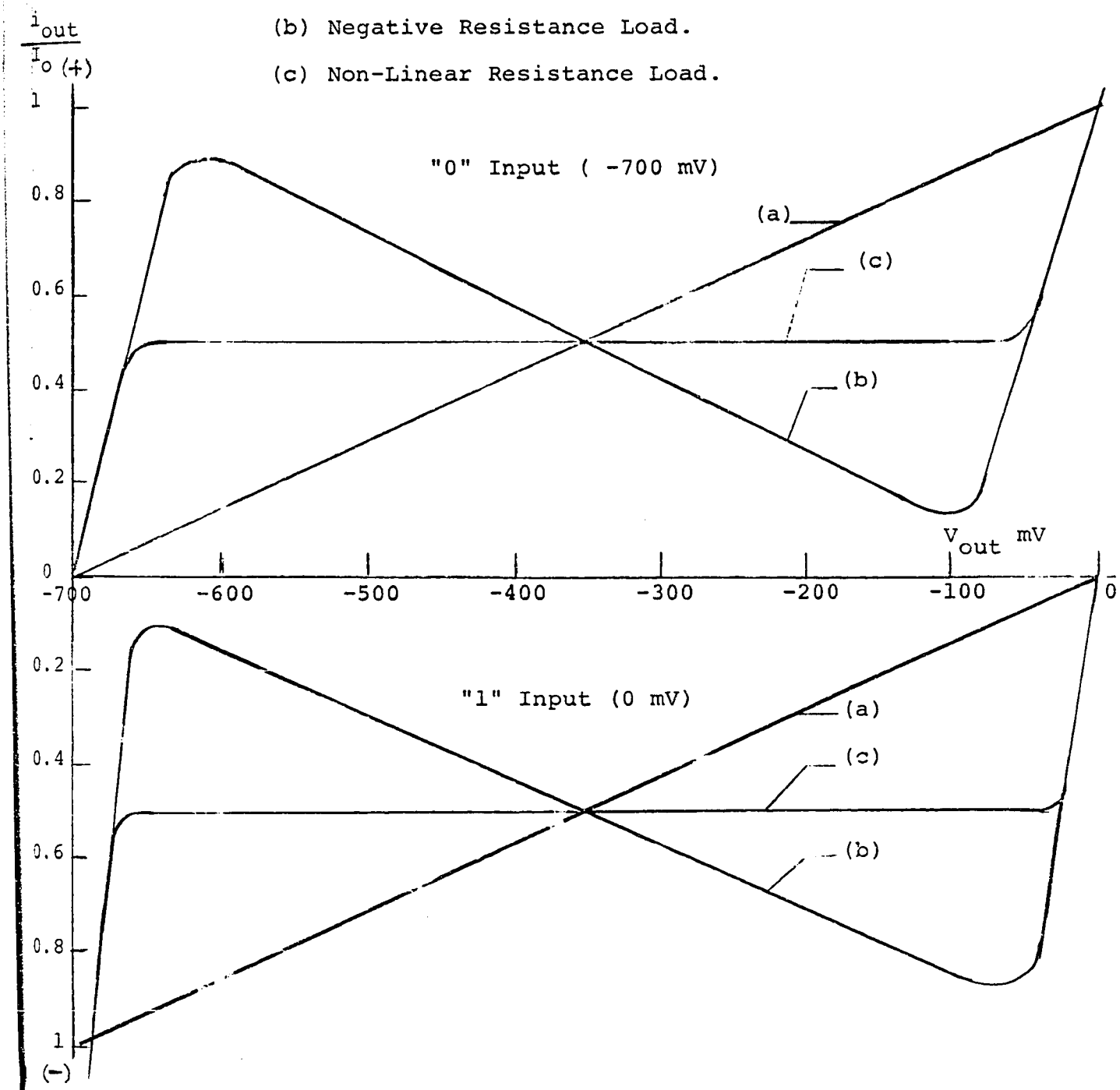


Fig. 3-10 ECL Output Characteristics

4] Power Dissipation

One of the quantities used to evaluate the performance of a logic circuit is its power dissipation. The ECL circuit dissipates approximately the same amount of power for both a logical "1" and a logical "0" output. If we neglect the power supplied by V_r, the power dissipation in either state can be given appriximately by:

$$P = V_s I_o$$

and thus the average power is

$$P_{av} = V_s I_o$$

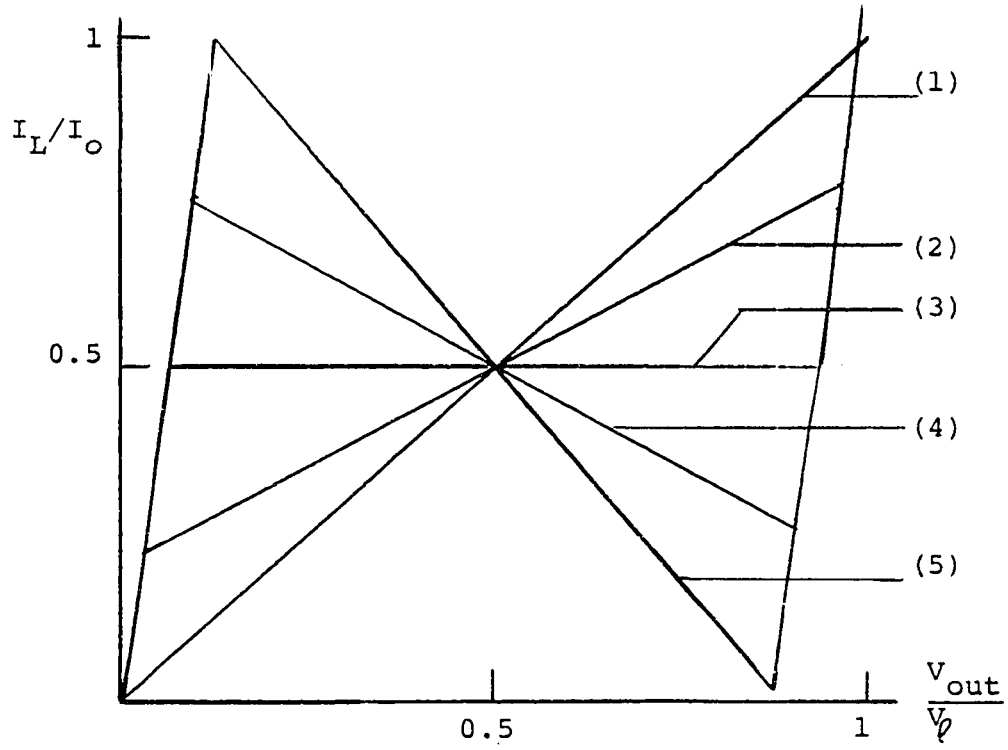
If we assume the same power supply V_s is used with different load sturctures, the non-linear load has the advantage of working with less I_o without affecting the logic swing, which means less power dissipation. As mention before, an emitter follower is necessary in the case of linear load structure. This dissipates extra power, thus the total power dissipation by the circuit is larger than in the case of non-linear load structure.

3-7 Transient Analysis of ECL with Different Load Structures

In Section 1-3, a transient analysis of ECL is given without taking the output circuit effects (load structure and output capacitances) into consideration. In this section only, the output circuit effects on the transient performance is considered. Assuming the same circuit conditions for the ECL, except the load structure used, Figure 3-11 shows the normalized transient response for five ideal load structures (Appendix 1).

If an arbitrary definition of a rise time is taken as (10% - 90%) of V the rise times are:

		(T_r) / RC
load structure	1	3
" "	2	2
" "	3	1.8
" "	4	1.5
" "	5	∞



Ideal Load Line Characteristics

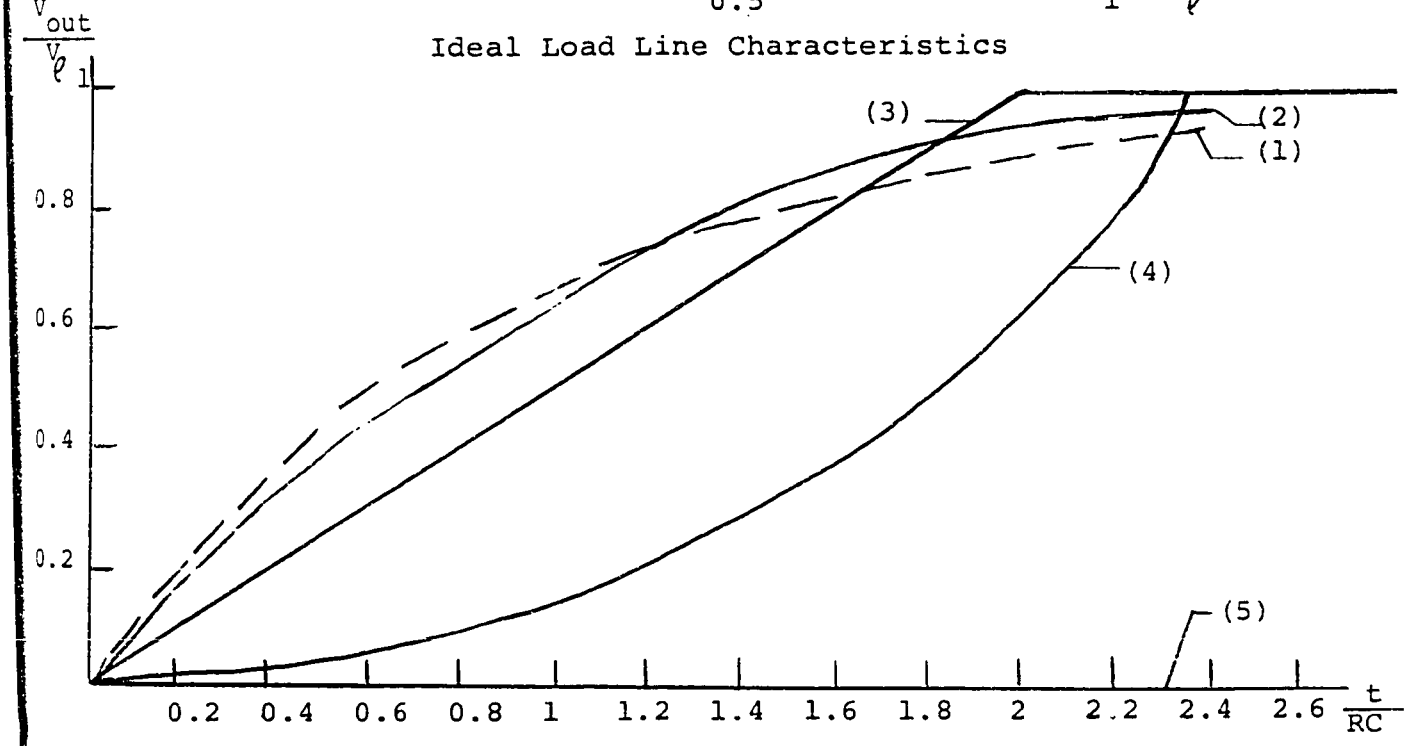


Fig. 3-11 ECL Transient Characteristics

and if an arbitrary definition of a delay time is taken as (up to 10% of V) the delay times are:

load structure		(T_d) / RC
load structure	1	0.1
"	2	0.13
"	3	0.2
"	4	0.8
"	5	∞

As shown the tunnel diode gives the smallest rise time and the longest delay time, provided that the switching current I_o is larger than the peak current. The linear resistance gives the smallest delay time and the largest rise time, if case 5, which is impractical, is omitted.

3-8 Load Structure Realization

(a) Linear Resistance Load Structure

This structure is the one commonly used in ECL circuits today [70,71]. To reduce the distributed capacitance associated with a diffused resistance, the value of the resistance should be small. A value of 50 or 100 Ω is frequently used. This reduces the logic swing unless the switching current is increased and as a result the power dissipation increased. A power dissipation in the order of 50 mW per gate is claimed for Motorola ECL III (MECL III).

(b) Negative Resistance Load Structure

A tunnel diode by itself does not give a symmetrical ideal negative resistance load structure and a tunnel diode pair resistance load is used instead [66]. This requires an additional power supply and close tolerance in the load parameters. Moreover, the structure does not give an integratable circuit.

(c) Non-linear Load Structure

The structure can be realized by a transistor in parallel with a diode (Fig. 3-12). The diode can be a hot carrier diode with a small carrier life time (Schottcky diode) [72] and the transistor is a lateral pnp [73].

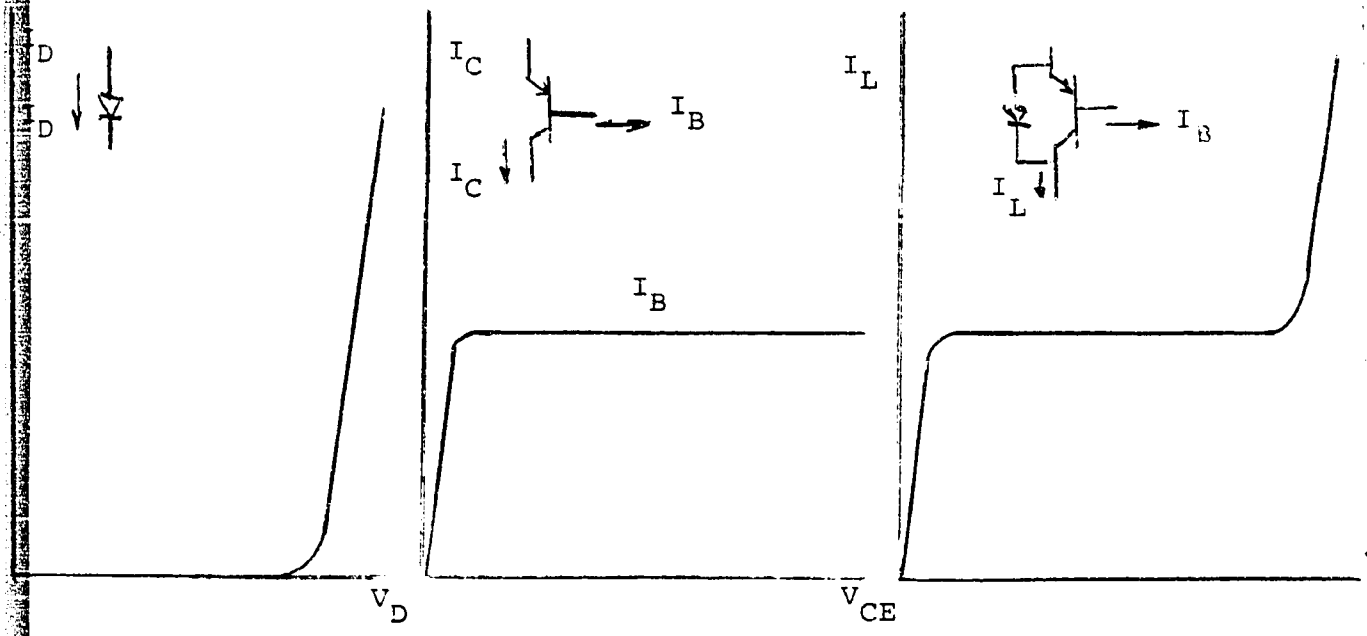


Fig. 3-12 Non-linear Load Realization

The load has the following advantages:

1) It is fully integratable.
2) It provides a higher noise margin than a linear resistance.
3) Its power dissipation is less than that of a linear resistance if the same logic swing is assumed.
4) It provides faster speed of operation than the linear resistance load structure if the same output capacitance is assumed.

3-9 Conclusions

An ECL circuit realization for the standard building block of a predetermined logic system is given. A common integratable input-output circuit structure (Fig. 3-4) is noted to be common to both the single and the two level ECL circuits, and it may be used as a standard building structure. The realization is based on logic blocks rather than logic gates. This design approach has the advantages of, saving of silicon area, reducing power

dissipation, increasing speed of operation and obtaining a standard circuit structure.

The above approach to the design of load structure leads to the development of a non-linear load for current switching logic with significant advantages over those that have been used previously. Furthermore, the load structure promises to have applications outside the circuit for which it was developed. e.g. Its current threshold is applicable to a system of majority logic [74,75], and it introduces some interesting possibilities in Transistor-Transistor-Logic (TTL).

In the following chapter the realization of such a load structure is discussed.

CHAPTER 4

A Non-linear Load Structure for Emitter-Coupled Logic

As indicated in Chapter 3, the non-linear load structure improves the operation of emitter coupled logic circuit. In this chapter, the realization of such load structure, as an integrated lateral pnp transistor in parallel with a Schottky barrier diode, is considered, experimental results are given and integrated circuit fabrication problems are indicated.

4-1 Lateral PNP Transistor

Improvements in npn integrated circuit technology have made it possible to form a pnp transistor, whose emitter and collector are fabricated side by side on the same silicon chip (Fig. 4-1). In this arrangement injected minority carriers flow parallel to the surface, hence the name "lateral transistor" [76,77,78]. A simple equivalent circuit is shown in figure 4-2 for the lateral transistor. The total base current I_B consists of vertical components I_v injected at the bulk side of the emitter and the current I_B^*, which traverses the active zone of the base as a result of surface and volume recombination. The static current gain is given by [77]:

$$\beta = \frac{I_c}{I_B} = \frac{I_c}{I_B^*}\,\frac{I_B^*}{I_B} \cong \frac{I_L}{I_B^*}\,\frac{I_B^*}{I_B}$$

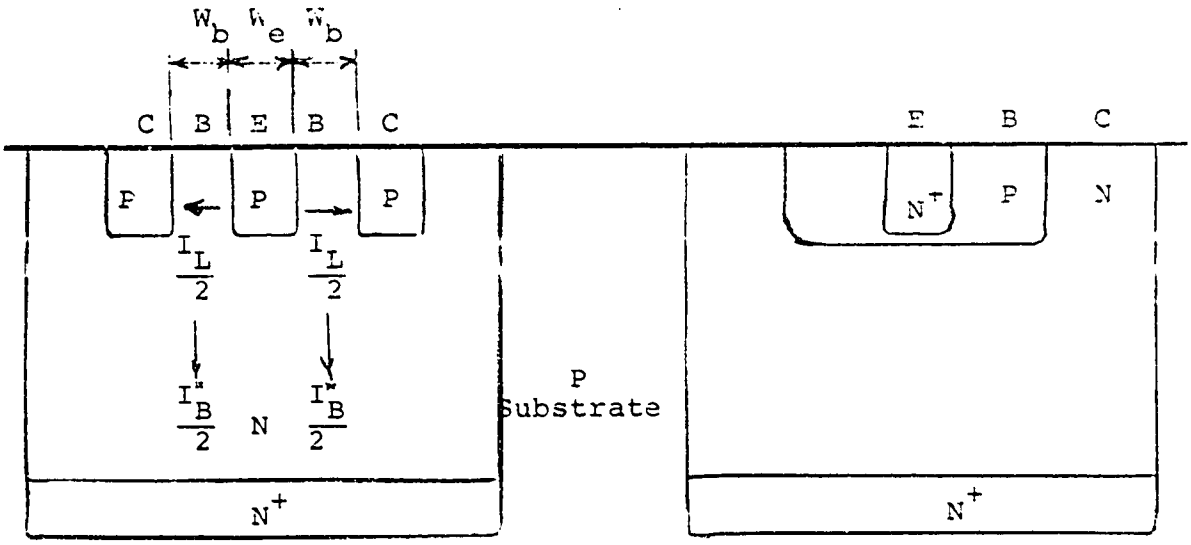
where

$$\frac{I_L}{I_B^*} = \frac{2L_p d}{W_e W_b}$$

$$L_p = (D_p T_p)^{1/2}$$

D_p = diffusion constant of holes

T_p = hole life time



Lateral pnp transistor npn transistor

Fig. 4-1 NPN and Lateral PNP Transistors

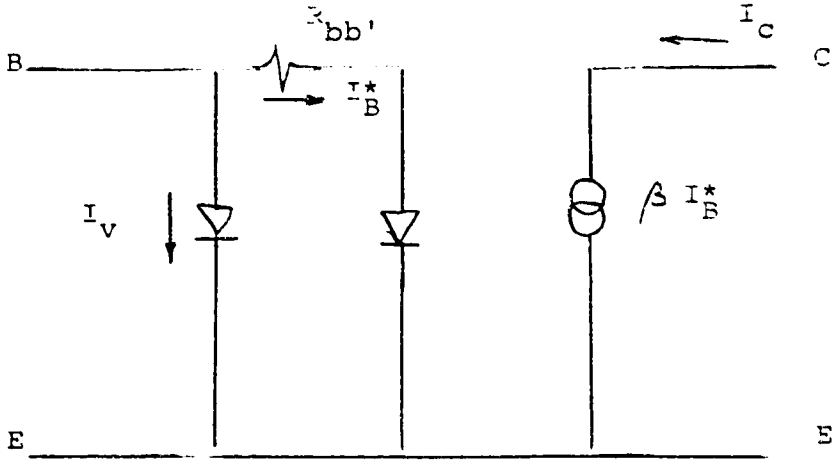


Fig. 4-2 Equivalent Circuit for PNP Lateral Transistor

Apart from the problem of controling the dimensions during the fabrication to obtain a predicted (I_L/I_B^*), the ratio (I_B/I_B^*) is difficult to control and percentage change of β from one device to another is of order of 30% with the present technology [77].

4-2 Load Diode Realization

The load diode is realized as a Schottky (metal-semiconductor, hot carrier) diode because it has a small storage time (less than 1 nsec compared with 10 nsec of PN junction diode) [80]. Schottky diode is a metal in contact with an N or P semiconductor as shown in Figure 4-3. The carriers are majority carriers and the forward voltage depends upon the metal and semiconductor used [80,81,82].

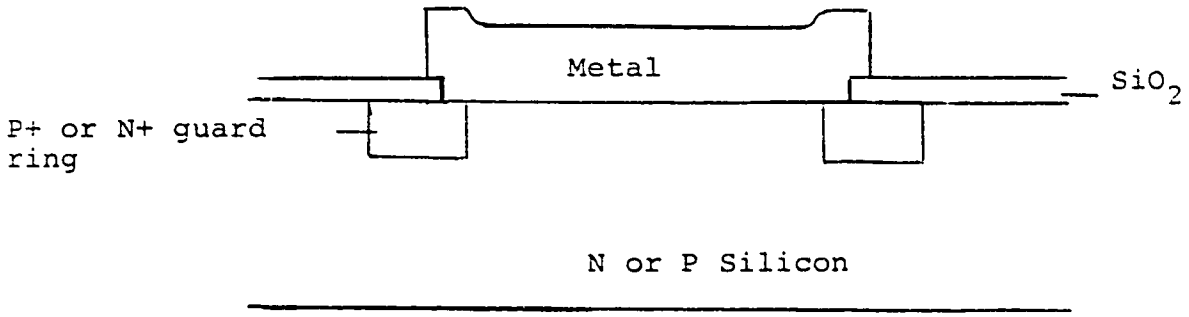


Fig. 4-3 Schottky Barrier Diode

Aluminum on a p-silicon gives a forward voltage of 400 mV. Using aluminum as a metal, formation of Schottky diode in a monolithic IC is compatible with standard processing because aluminum itself is used for metalization.

4-3 Biasing Circuit for the Load Structure

It is desirable to set the threshold current of the load at $I_o/2$, not only to have equal noise margins but also to ensure symmetry in transient performance. The problem of controlling I_o and the bias current of the load reduces to the control of β of the lateral transistor to 1/2 if I_o is used as bias current (Fig. 4-4). Close matching of current sources can be accomplished in integrated circuits, but variations in β have always been a problem especially in lateral transistors [71].

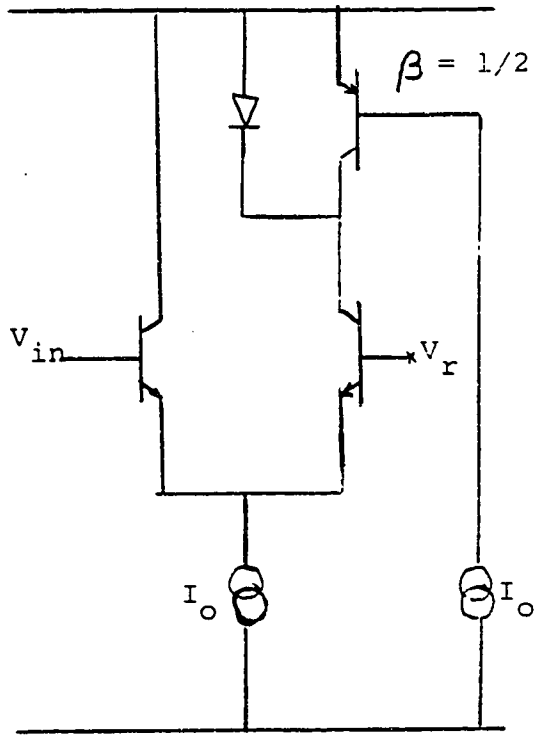


Fig. 4-4 Biasing Circuit for the Load Structure

A more promising approach is to obtain a collector current of $I_o/2$ by a feed back circuit and Figure 4-5 shows a proposed configuration [79]. It consist of a 4 collector lateral transistor where two of these collectors are driven by a current source I_o, matched to the emitter current source, the remaining two collectors are available as loads (C_1 and C_2). A differential pair Q_1 and Q_2 regulates the base current to ($I_o/2$) for each collector.

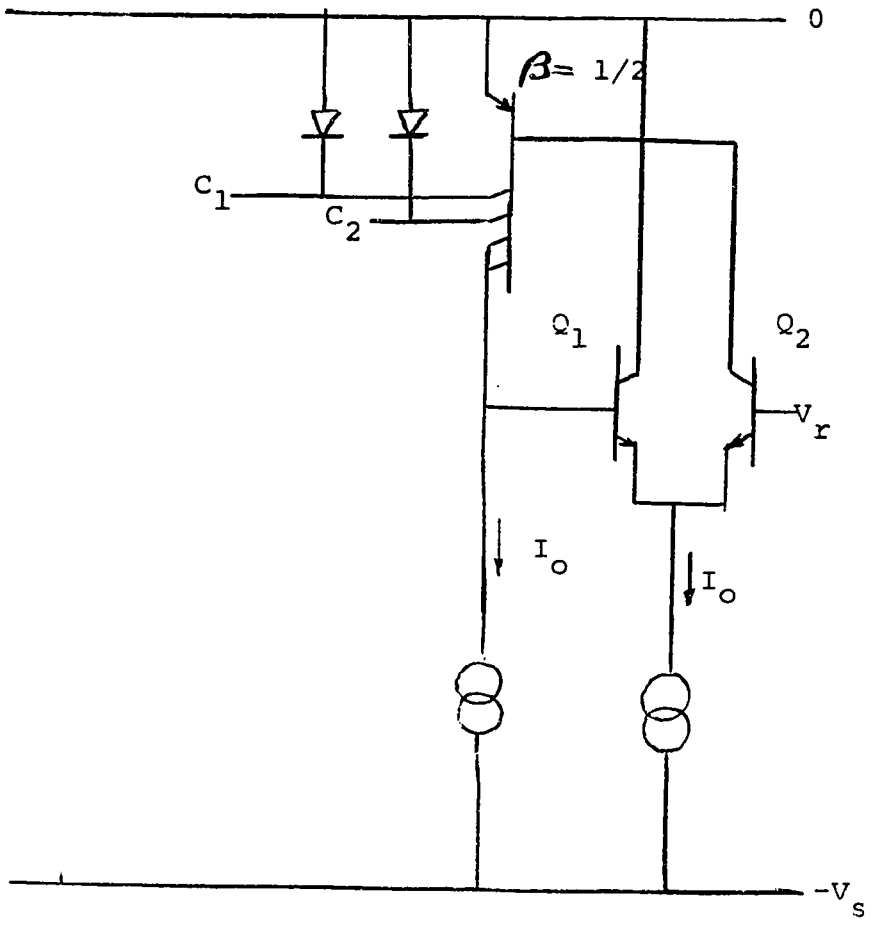


Fig. 4-5 Feed Back Biasing Circuit for the Load Structure

4-4 Current Source Realization

Since in integrated circuits, the base-emitter junctions have similar characteristics, transistors can be voltage biased. The emitter current source for the ECL circuits are realized by voltage biased transistors as shown in Figure 4-6. The value of the collector resistance R of Q_5 determines the value of I_o,

$$I_o = \frac{V_s - V_j}{R}$$

where V_s is the supply voltage
V_j is the junction voltage.

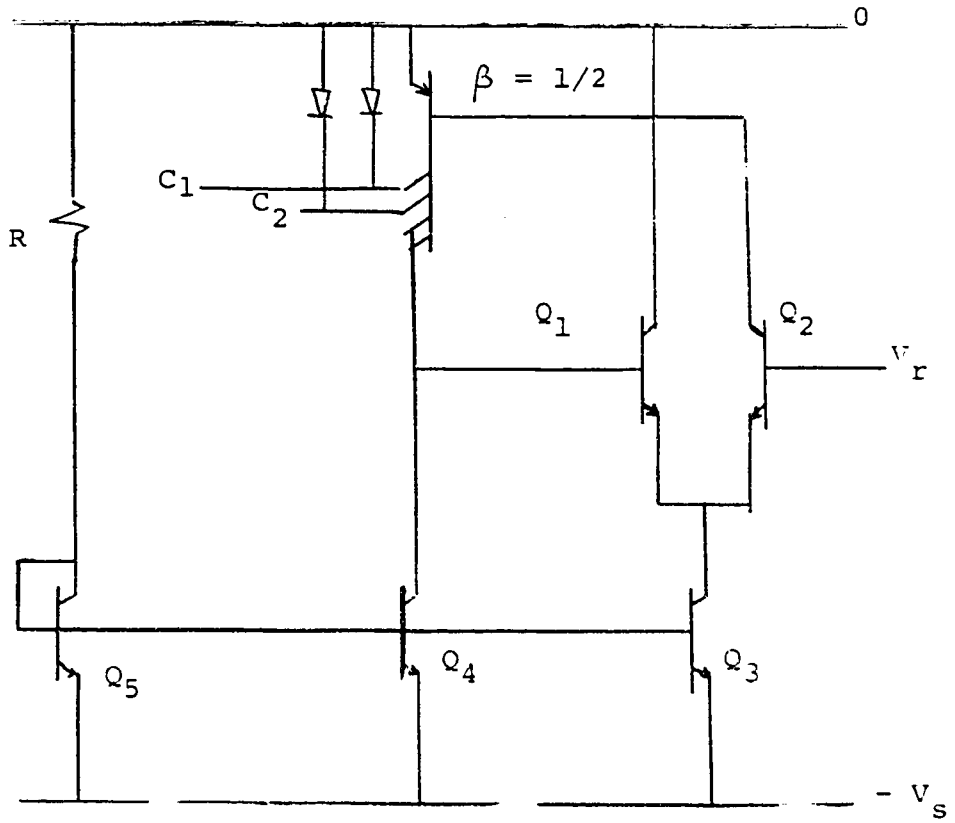


Fig. 4-6 Current Source Realization

4-5 Reference Voltage Realization

The reference voltage V_r for the fixed biased transistors is obtained by a voltage divider across the supply voltage. Since a collector-emitter voltage of 700 mV is required for a transistor operation in the active region, a supply voltage of 2 volts is required for single level ECL and 3 volts supply for two level ECL. The reference voltage is -350 mV for the ECL circuits developed in Chapter 3. The effective source resistance of V_r can be decreased by using an emitter follower stage (Fig. 4-7) and in this case V_r can be used to biased more than one transistor.

$$-V_r = V_s \frac{R_1}{R_1 + R_2} - V_j$$

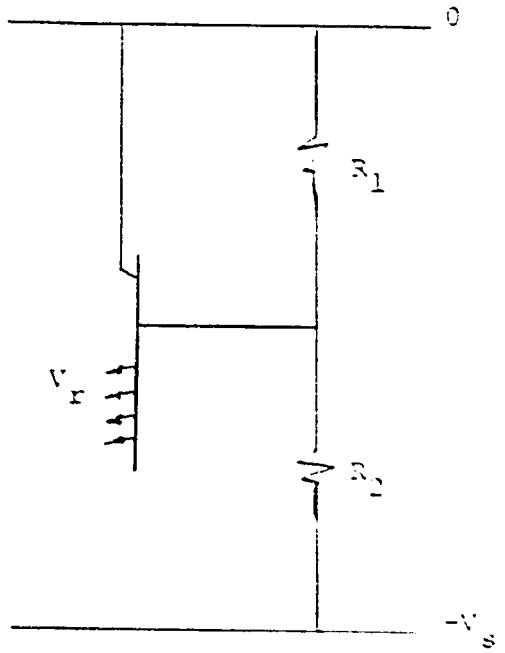


Fig. 4-7 Reference Voltage Realization

4-6 Results

4-6-a Circuit Realization Using Discrete Components

(1) The non-linear load structure is realized using a Schottky diode (HP 5082) and a pnp transistor (2N4402) and its DC characteristics are shown in Figure 4-8.

(2) An ECL circuit is constructed (Fig. 4-9) using 2N4400 npn transistors and its DC transfer characteristic is measured where the collector load is:
   1) A linear resistance,
   2) A RCA 40571 tunnel diode, or
   3) The non-linear load constructed in (a) above.

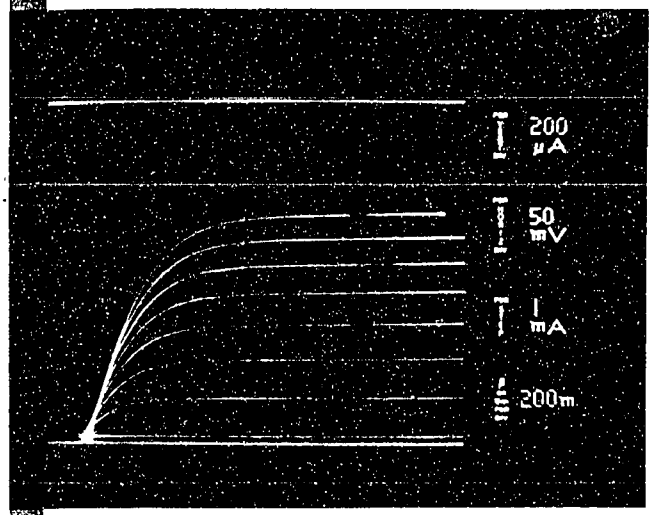
   The DC terminal characteristics of the load structures are shown in figure 4-10 and the DC transfer characteristics are shown in figure 4-11. The experimental results agree with the theory given in Chapter 3 and show that the non-linear load structure gives higher DC noise margins and a higher DC gain than those of a linear resistance.

(3) The output wave forms of two cascaded ECL circuits are shown in figure 4-12 and they agree with the simple analysis given in Chapter 3.

4-6-b Integration of the Non-linear Load Structure

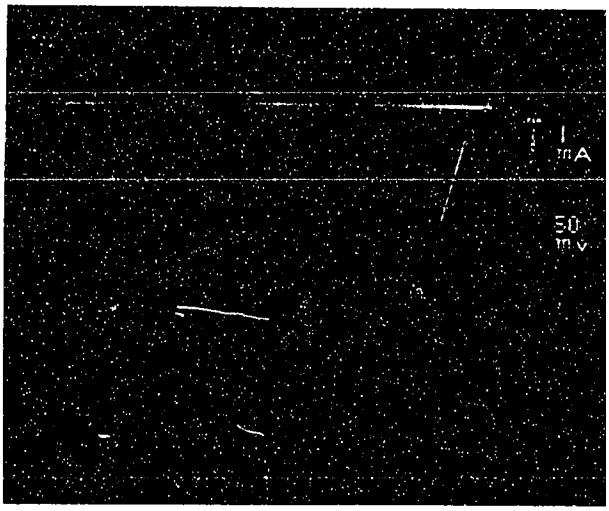
Figure 4-13 shows an integrated circuit realization of the non-linear load structure. The lateral transistor is Q and the npn transistors are Q_1, Q_2, Q_3 and Q_4. By designing the collector region of Q_2 to be the base region of the lateral transistor, a saving of silicon area results. Isolation regions are required for Q_1, Q_3, and Q_4.

A

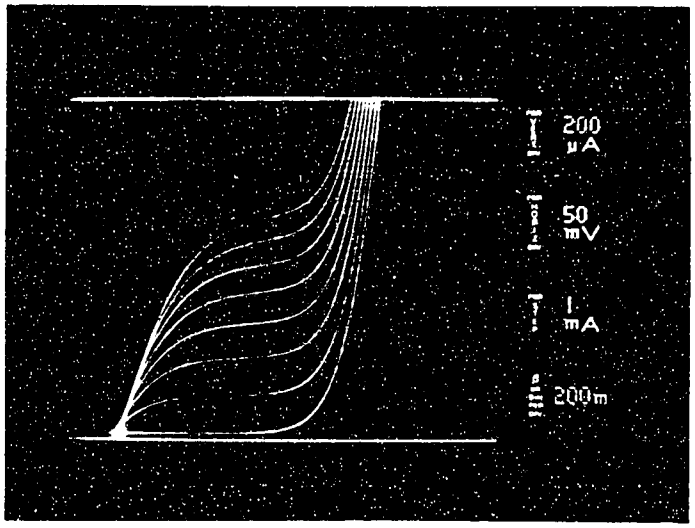


(a) I_C vs V_{CE} PNP Transistor Characteristic

B



(b) I_D vs V_D Schottky Diode Characteristic



Scale
Horiz 50 mV/di
Vert 200 μa/d

(c) DC Characteristic of the Non-linear Load Structure

Fig. 4-8 Non-linear Load Structure DC Characteristic

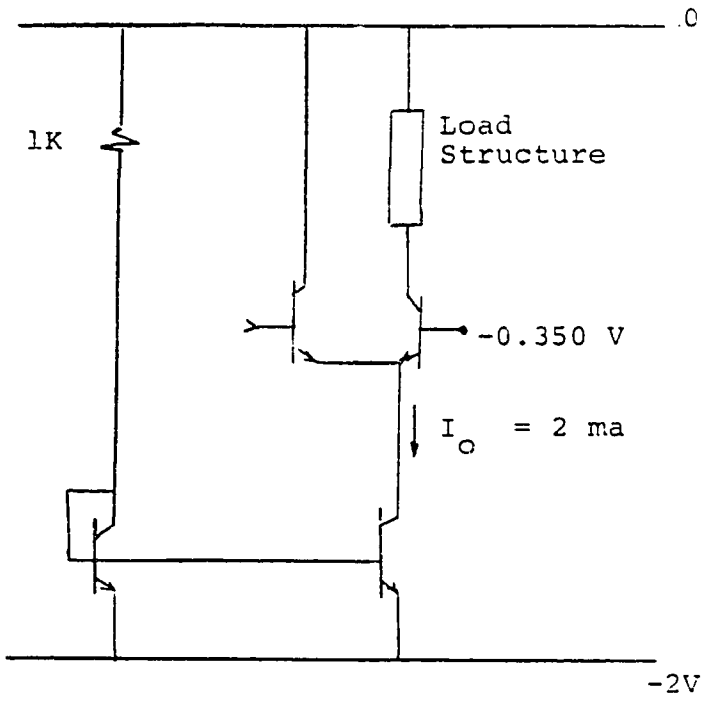
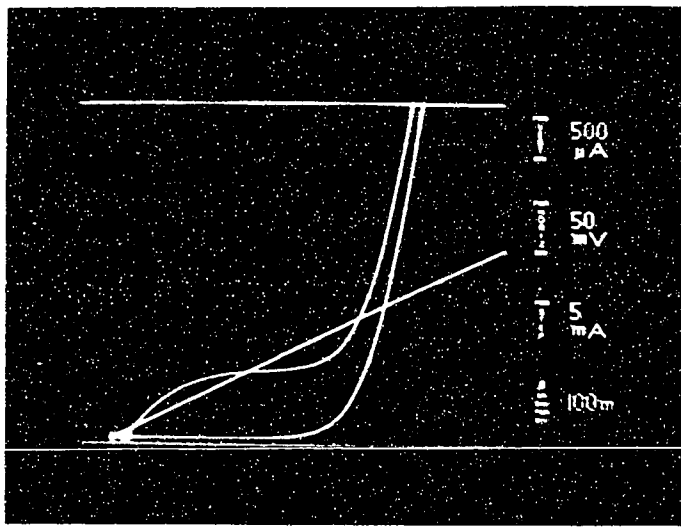


Fig. 4-9 ECL Circuit

Fig. 4-10 DC Characteristic of the Load Structures:
(1) 200 Ω Linear Resistance.
(b) Tunnel Diode with peak current of 1.4 ma - Valley current of 0.2 ma - Switching Voltage of 50 mV and 500 mV.
(c) Non-linear Load with Threshold Current of 1 ma.
Scale:
Horiz 50 mV/div
Vert 500 μa/div



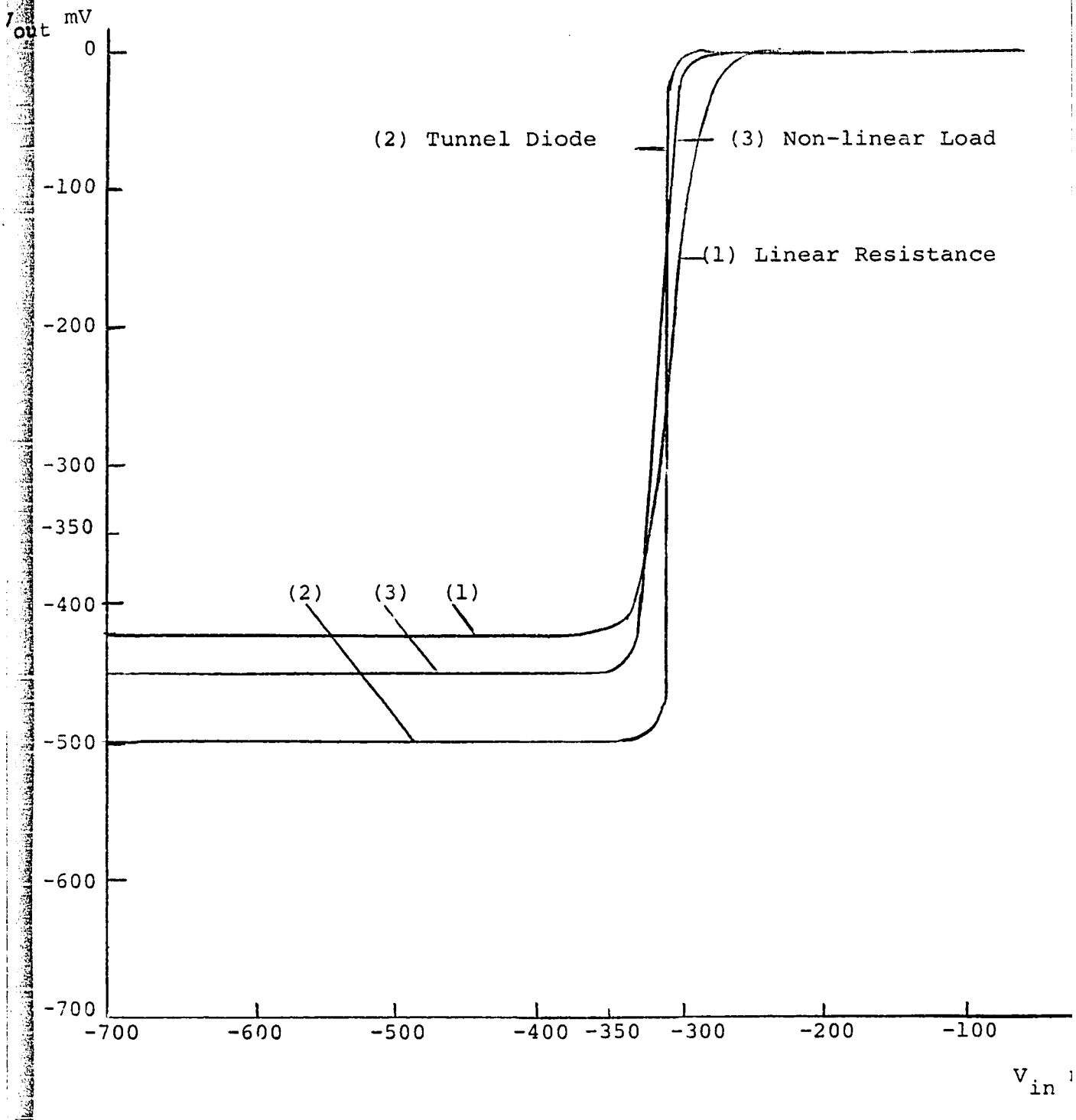
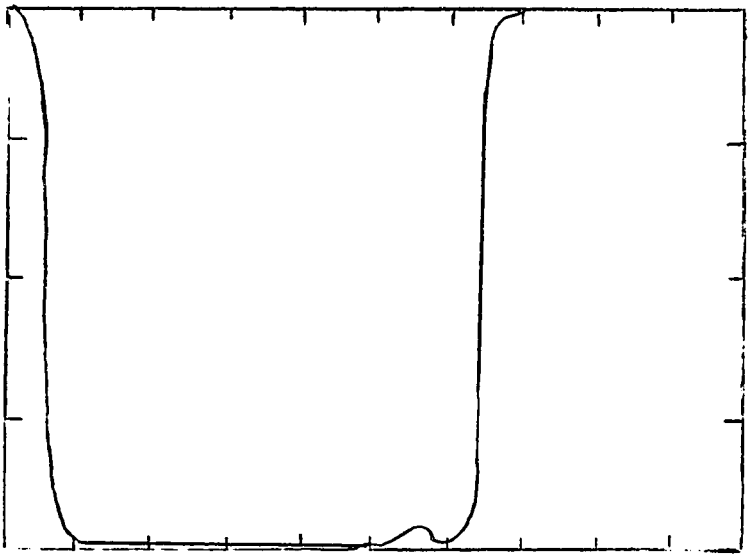
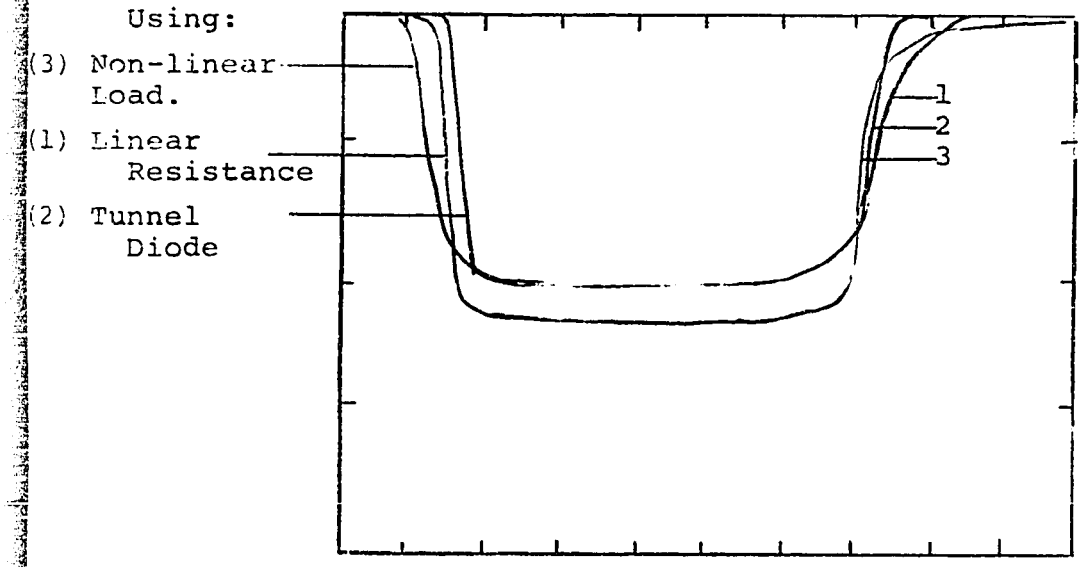


Fig. 4-11 ECL Measured DC Characteristic

Horizontal Scale 1 nsec / div
Vertical Scale 250 mV / div



Input Wave Form



Output Wave Form

Fig. 4-12 Input - Output Wave Forms

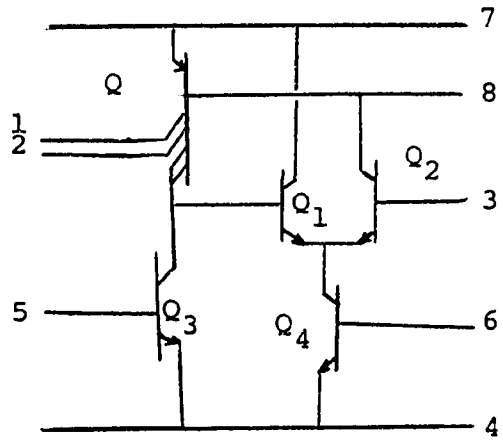


Fig. 4-13-a Non-linear Load Structure Integrated Circuit

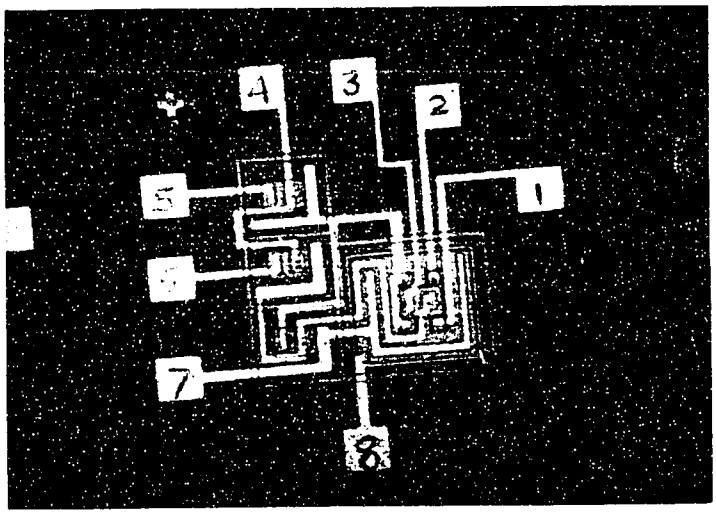


Fig. 4-13-b Integrated Non-linear Load Structure

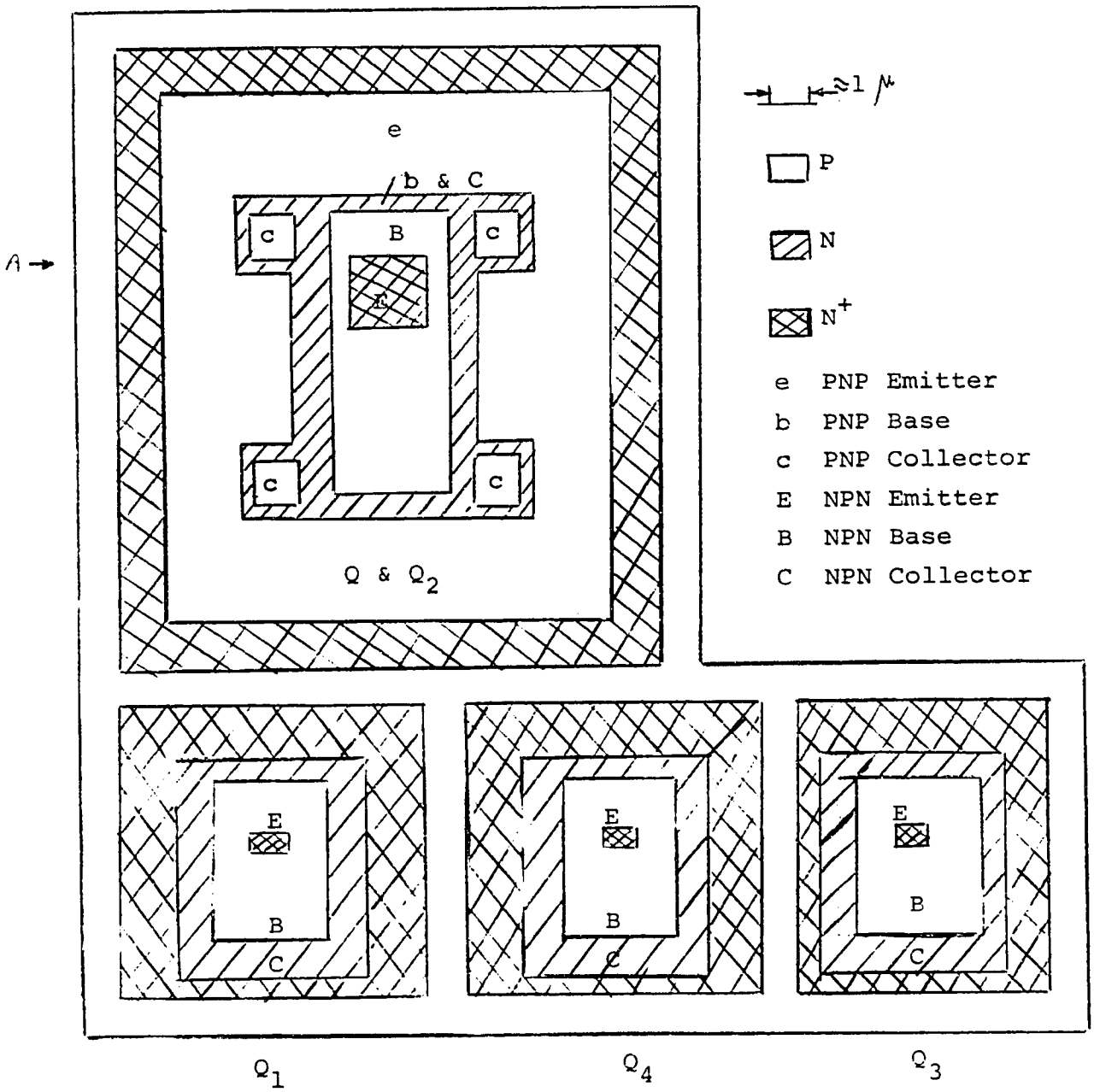
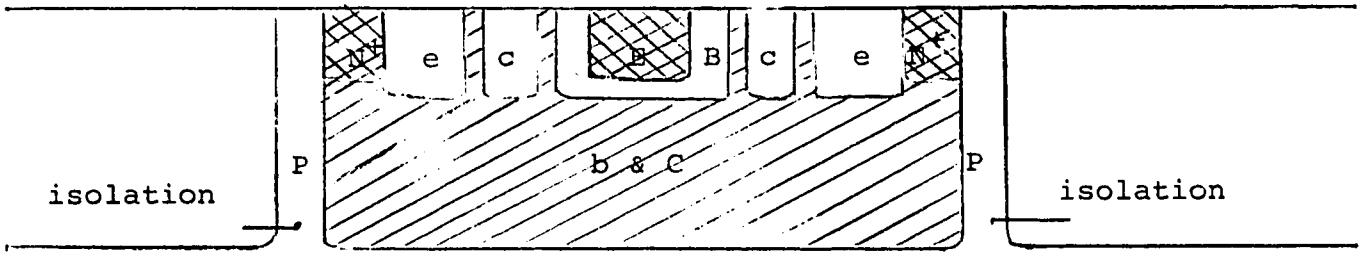


Fig. 4-13-c Load Structure - Top View



P Substrate

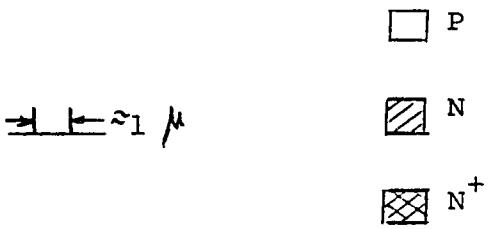


Fig. 4-13-d Load Structure - Cross Section A

Conclusions

This thesis has attempted to develop a unified approach to logic and integrated circuit design. The vehicle for this concept was a generalized high-speed digital system suitable for real-time computation in control and communication systems. The results of this approach were:

(1) The development of a general procedure of partitioning a logic system on the basis of the sequence of arrival of inputs and

(2) The development of a standard logic circuit block suitable for current mode integrated circuit realization.

There have also been several integrated circuit developments such as the non-linear collector load structure with a well defined current threshold.

The work has suggested several areas which require investigation:

(1) The logic design procedure of Chapter 2 dealt only with single output combinatorial systems. A similar procedure suitable for multi-output combinatorial systems should be developed.

(2) Because the design procedure of Chapter 2 takes the time sequence of inputs into consideration, it may be applicable to asynchronous logic systems and lead to solutions to race problems.

(3) It was demonstrated that the logic design procedure of chapter 2 is applicable to some iterative systems and it is possible that further development will lead to some standard logic cells.

(4) The circuit design approach given in chapter 3 for realizing complicated logic operations might be made more systematic and a digital computer programme might be developed.

(5) The DC and the transient analysis of the ECL with different load structures is given in chapter 3 using a simple circuit model. A more complete analysis may be obtained by using non-linear models.

(6) It was indicated in chapter 3 that the non-linear collector load structure has advantages over the diffused resistor. The optimum collector load for the ECL can be obtained only by a more exact analysis, requiring a computer programme.

(7) Because the non-linear load structure has a threshold current, it can find applications in the realization of threshold gates.

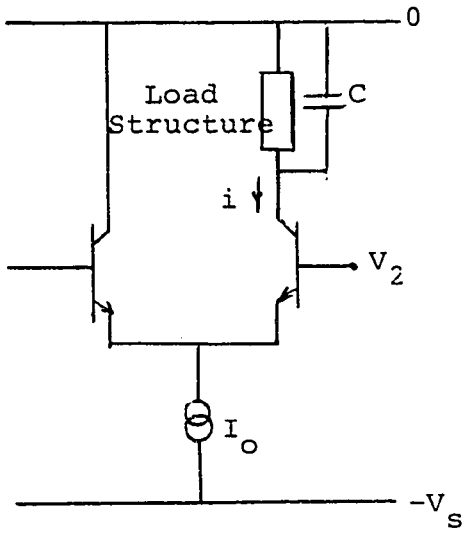
(8) The realization suggested for the collector load structure requires further work on the integrated circuit technology. Also, other circuit configurations should be investigated.

Finally, it must be emphasized that the work reported in this thesis represents only a small part of the present research into high-speed computation techniques. The time required for a given arithmetic operation is becoming shorter; e.g., It should now be possible to construct a 64 bit multiplier with a delay in the order of 50 nanoseconds. Thus, it is clear that this time is becoming less significant in relation to the time taken by other functions in an overall system; e.g., the time taken for transmission of information from one part of the system to another and changes in system organization will be necessary.

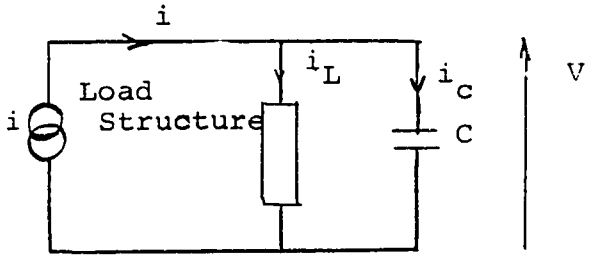
Appendix 1

(a) Transient Analysis of the Load Structure Using Simple Models

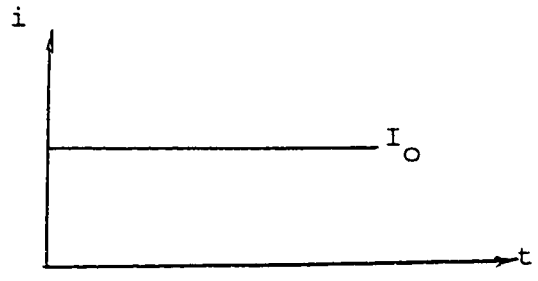
The transient effects of the load are analyzed by the simple circuit shown in Figure (b), it consists of the load structure in parallel with a constant capacitance C representing the output capacitance of the circuit. The parallel combination is fed by a step current as shown in Figure (c). The step current represents the switching current I_o.



(a) Emitter Coupled Logic Circuit

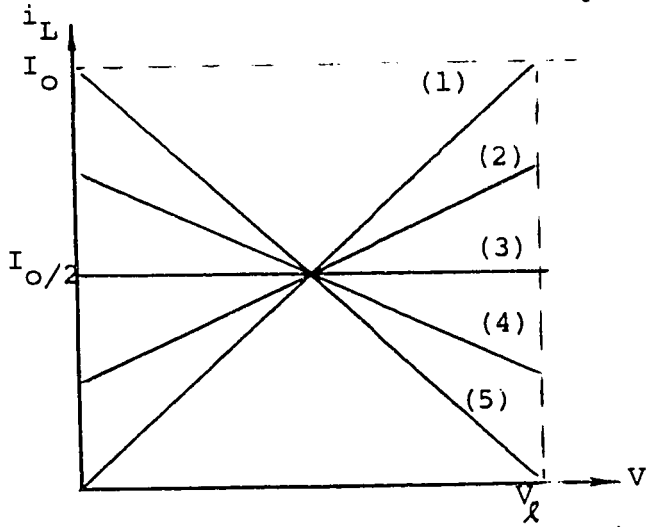


(b) Output Circuit



(c) Input Current

The ideal DC load characteristic during switching can take one of the forms shown in Figure (d), where V_ℓ is the logic swing.

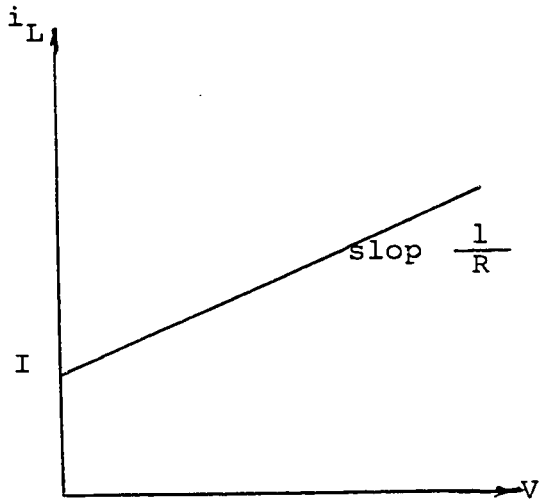


(d) Ideal DC Load Characteristics

The load current can be expressed as: $i_L = I + \frac{V}{R}$

where I is the load current at V = 0

1/R is the slop of the I-V characteristic.



The transient equation representing the circuit shown in Figure (b) is:

$$i = i_c + i_L$$

$$I_o = c\frac{dV}{dt} + I + \frac{V}{R}$$

$$V\left(P + \frac{1}{RC}\right) = \frac{I_o - I}{CR} R$$

Where P is the operator $\frac{d}{dt}$

From the above equation V is given by

$$V = (I_o - I)R\ (1 - e^{-t/RC}) \quad \ldots\ldots\ldots\ldots (1)$$

For the above load lines, the following transient characteristics are obtained using equation (1):

(1) Linear Resistance

$$R = \text{load resistance} = \frac{V_\ell}{I_o}$$

$$I = 0$$

$$V = V_\ell\ (1 - e^{-t/RC}),\ R = \frac{V_\ell}{I_o}$$

(2) Non-linear Positive Resistance

$$R = \frac{V_\ell}{I_o}$$

$$I = \frac{I_o}{4}$$

$$V = \frac{3}{2} V_\ell\ (1 - e^{-T/RC}),\ R = \frac{2V_\ell}{I_o}$$

(3) Non-linear Infinite Resistance

$$R = \infty$$

$$I = \frac{I_o}{2}$$

$$V = \frac{V_\ell}{2}\ \frac{t}{CR},\ R = \frac{V_\ell}{I_o}$$

(4) Non-linear Negative Resistance

$R = 2V_{\ell} / I_o$

$I = \frac{3}{4} I_o$

$V = \frac{V_{\ell}}{2} (e^{t/RC} - 1)$, $R = \frac{V_{\ell}}{I_o}$

(5) Non-linear Negative Resistance

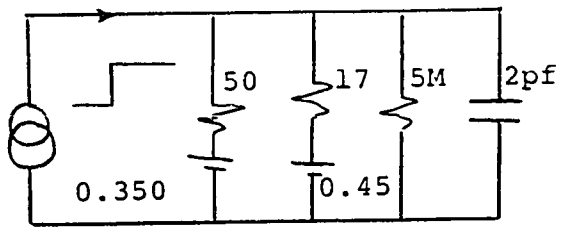
$R = \frac{V_{\ell}}{I_o}$

$I = I_o$

$V = 0$

(b) Transient Analysis Using the Computer Program (ECAP)

The IBM Electronic Circuit Analysis Program (ECAP), with non-linear circuit models, is used to verify the simple analysis given above. The first program is shown on page 74 to describe the non-linear model of the Schottky diode given below. The results are shown on page 75 which gives the plot of the output voltage vs time. The second program is for the transient analysis of the non-linear load structure.

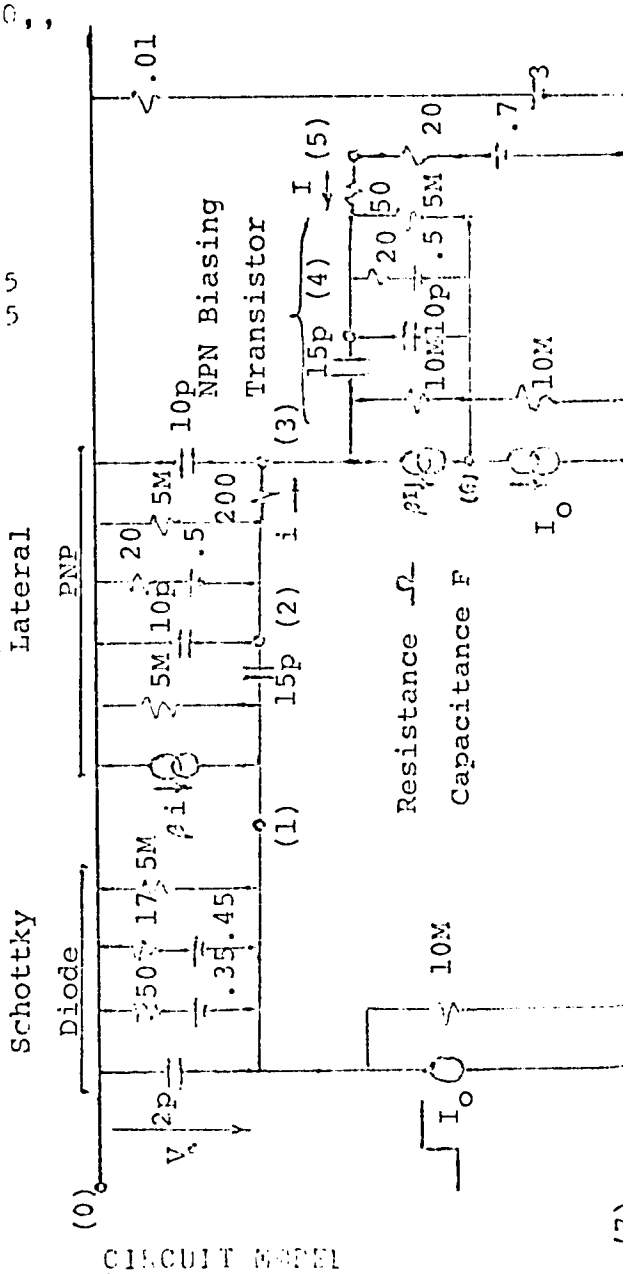


ECAP Program I

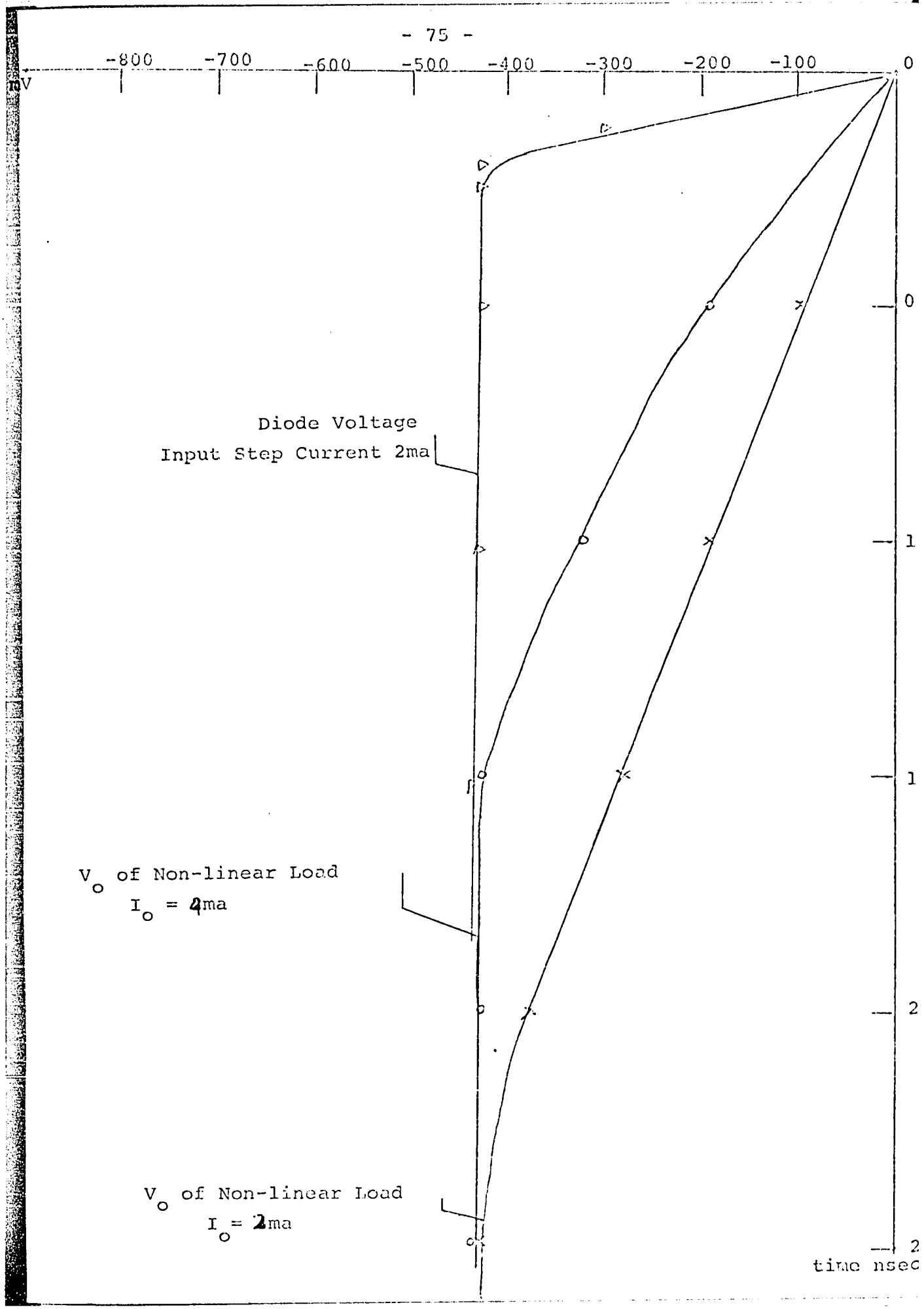
```
000500   $ECAP,ECAP
000600   C       CIRCUIT CHARACTERIZATION
000700   C       SCHOTTKY DIODE (EP 50-2-2-80)
000800           TRANSIENT ANALYSIS
000900   B1      N(1,0),R=5E6
001000   B2      N(1,0),R=(10E6,50),E=-0.35
001100   B3      N(1,0),R=(10E6,17),E=-0.45
001200   B4      N(1,0),C=2E-12,I=0.005
001300   S1      B=2,(2),OFF
001400   S2      B=3,(3),OFF
001500           TIME STEP=0.001E-9
001600           OUTPUT INTERVAL=10
001700           FINISH TIME=2E-3
001800           PRINT,NV
001900           PLOT,NV
```

ECAP Program II

```
000100   $JOB,AAAAAA,UUUUUU,**,DDDD,2,1500,,
000200   $SCHED,CORE=60,SCR=5
000300   $MAP=N
000400   S*DEF(0,W,ECAP,8161,FCAP,,,I)
000500   $ECAP,ECAP
000600   C       CIRCUIT CHARACTERIZATION
000700   C       LOAD LINE
000800           TRANSIENT ANALYSIS
000900   B1      N(0,1),C=5E-12
001000   B2      N(0,1),R=(10E6,50),E=-0.35
001100   B3      N(0,1),R=(10E6,17),E=-0.45
001200   B4      N(0,1),R=5E6
001300   B5      N(1,2),C=15E-12
001400   B6      N(0,2),C=10E-12
001500   B7      N(0,2),R=(10E6,20),E=-0.5
001600   B8      N(0,2),R=5E6
001700   B9      N(0,3),C=10E-12
001800   B10     N(2,3),R=200
001900   B11     N(3,4),C=15E-12
002000   B12     N(3,6),R=10E6
002100   B13     N(4,6),C=10E-12
002200   B14     N(4,6),R=(10E6,20),E=-0.5
002300   B15     N(4,6),R=5E6
002400   B16     N(5,7),R=20,E=-0.7
002500   B17     N(5,4),R=50
002600   B18     N(7,6),R=10E6,I=2E-3
002700   B19     N(0,7),R=0.01,E=-3
002800   B20     N(7,1),R=10E6,I=2E-3
002900   S1      B=2,(2),OFF
003000   S2      B=3,(3),OFF
003100   S3      B=7,(7),OFF
003200   S4      B=14,(14),OFF
003300   T1      B(10,4),BETA=0.5
003400   T2      B(17,12),BETA=50
003500           TIME STEP=0.1E-9
003600           OUTPUT INTERVAL=1
003700           FINISH TIME=5E-9
003800           PRINT,NV(1)
003900           PLOT,NV(1)
004000           EX
004100   C       THANK YOU
```



CIRCUIT MODEL


-800
-700
-600
-500
-400
-300
-200
-100
0
mV
0
1
1
2
2
time nsec
Diode Voltage
Input Step Current 2ma
V_o of Non-linear Load
I_o = 4ma
V_o of Non-linear Load
I_o = 2ma

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Vita

Name: Mohamed I.Y. Elmasry

Born: Cairo, Egypt December 24, 1943

Education:

Primary: Shoubra High School
Cairo, Egypt

Secondary: Tawifikia High School
Cairo, Egypt

University: Cairo University
Cairo, Egypt

B.Sc. E.E. (honors) (1965)

Experience:

Teaching: Instructor - Cairo University (1965-1968)
Demonstrator - Ottawa University (1968-1970)

Industrial: Northern Electric Company
R & D Labs
Ottawa (Summer 1970)

Errata

Page	Line	Error	Correction
1	12	Brozozowski	Brozowski
1	14	Professor C.L. Sheng	Das and Sheng
1	16	high speed logic design	Logic design
4	4	(machine or circuit)	delete
4	5	are	is
4	7	the present state	the past history
4	20	one of the two	any of the
4	21	McKlusky	McCluskey
4	26	are ordinates	are coordinate
5	7	AND Gate Representation	Truth Table and K-map of AND function
5	9	increments or	delete
5	16	the inputs	the present inputs
6	1	is used	is usually used
6	4	is used	is usually used
6	8	sited	cited
6	20	is transferring	is that transferring
9	17	it takes	that takes
9	19	it takes	that takes
10	8	consider that	consider
10	18	reverse-biased	reverse biased
13	15	Neglecting I_{C_o}	Neglecting I_{c_o}
15	13	to '0'	to '0' (negative voltages)
15	14	to '1'	to '1' (0 voltages)
19	7	Similiar expression	Expression similiar
23	Fig. 2-3	x_n	x_{n_1}
23	Fig. 2-3	X_N	x_n
23	Fig. 2-3	$y_{(N-1)1}\ell_{(N-1)}$	$y_{(N-1)}\ell_{(N-1)}$
23	4	criteria	criterion
24	6	Example	Example 1:
24	7	Table 1	Table 2-1
25	3	k-map	K-map
25	4	k-map	K-map
25	Fig. 2-5 (case a)	assignment	assignment of $y_{11}y_{12}$
25	Fig. 2-5 (case b)	assignment	assignment of $y_{11}y_{12}$
26	11	$y_{11} = \bar{x} + x_1x_2$	$y_{11} = \bar{x}_2 + x_2$
26	12	$y_{12} = \bar{x}_2\bar{x}_3 + x_1x_2\bar{x}_3 + \bar{x}_1x_2x_3$	$y_{12} = \bar{x}_2\bar{x}_3 + x_1\bar{x}_3 + \bar{x}_1x_2x_3$

Page	Line	Error	Correction
26	13	$z=X_4$	$z = x_4$
28	1	k-map	K-map
28	3	assignment	assignment for y_{21}
			assignment for y_{22}
29	Fig. 2-8		add: x_{1i} x_{2i} x_{3i} are the inputs for the full adder, C_i is the output carry, S_i is the output sum where i = 1, ... n.
30	10	Z =	z =
30	12	assignment	assignment for $y_{11}y_{12}$
33	15		add: where '0' is a negative voltage and '1' is a zero voltage.
37	7	elliminated	eliminated
37	32	Z =	z =
37	Fig. 3-2	Z	z
39	11	sharing the current	sharing of the current
39	12	Z	z
39	13	Z	z
39	15	a technology	a technological
40	4	its emitter	its emitters
41	11	load structure	load structures
42	11	current gain	current gain = 0.95
43	Fig. 3-6	V_{in} mV	V_{in} and V_{out} mV
45	1	Both case	Both cases
46	Fig. 3-9	$\frac{i_b}{I_o}$	$\frac{i_b}{I_o (1 - \alpha_o)}$
46	3	defined as	defined as that
48	6	appriximitely	approximately
48	10	assume the same	assume that the same
48	14	power,	power;
52	7	e.g.	delete
53	15	, hence	and hence
53	26		add: d = junction depth
55	1	controling	controlling
55	4	of order of	of the order of
58	4	are	is
59	10	to biased	to bias
60	10	A RCA	An RCA
68	19	to race	of race
69	13	e.g.	delete
70	5	(b),	(b);
72	4	$I_o = c$	$I_o = C$

Page	Line	Error	Correction
72	12	R	R_1
72	14	R	R_1
72	16	R	R_2
72	18	R	R_2
72	20	R	R_3
72	22	R	R_3
73	2	R	R_4
73	4	R	R_4
73	6	R	R_5
76	2	Brozożowski	Brożowski
76	7	Sheng, C.L. and S.R. Das	Das, S.R. and C.L. Sheng
77	8	Brozozowski	Brozowski
77	8	Shengh	Singh
79	31	no.	no. 70-10