SiN Drum Resonator Fabrication and Integrated Actuation Using Substrate Capacitors

Gengyang Mu

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University of Ottawa

Abstract

Freestanding low pressure chemical vapor deposition (LPCVD) silicon nitride (SiN) membrane resonators are widely investigated as Nano-Electromechanical System (NEMS) for their outstandingly low mechanical dissipation and high mechanical quality (Q) factor. The high Q-factor brings better sensitivities to force, displacement, and temperature excitations. However, integrated actuation methods are not trivial to implement on this platform and are required to harness their high Q-factor in practical applications.

The first goal of this research is to develop a recipe for fabricating large area low stress LPCVD SiN membrane since commercial membranes are relatively expensive and have limited flexibility in terms of geometries. Starting from 4 inches, 500 μm thick, (100) single crystal silicon wafers double-side coated with 100 nm LPCVD SiN, we successfully fabricate five different sizes (i.e., 1 mm, 1.5 mm, 3 mm, 6 mm and 12 mm) of square shape membrane chips. The developed recipe is universally applicable for any size (i.e., under 12 mm) of square shape SiN membrane from the same type of wafer. All recipe parameters are presented in this work, along with experienced challenges and their associated solutions.

The second part of this work is to develop an on-chip actuation method for these resonators. We develop a new method for creating acoustic waves in the silicon substrate using metal – silicon nitride – silicon capacitors. Acoustic waves due to the voltage-dependent mechanical stress arising

from charge attractions was already observed previously in silicon substrate p-n junction resonators but is observed here for the first time in a capacitively coupled metal-dielectric-semiconductor (MDS) assembly. In the MDS system, we model three main possible actuation regimes, i.e., depletion, accumulation, and thermal expansion. Both depletion and accumulation rely on electrostatic attraction forces in MDS capacitors when an AC electrical current flows through. The same current can also generate thermal expansion forces resulting from resistive dissipation in the silicon. This contribution, however, is found to be negligible.

In experimental measurements on 1.5 mm membranes in high vacuum, the accumulation MDS is found to perform better than the depletion one in terms of membrane actuation amplitude. With 2 V drive voltage, the membrane achieves up to 10 nm displacement for fundamental mode (1, 1). The contribution of thermal expansion forces is found to be negligible, with resonator temperature changes smaller than 4 mK. A comparison of energy dissipation between a conventional external piezo actuation method and our approach is also presented, through which we find that both methods have comparable power consumption.

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In the end, this is for my grandma. I'm so sorry that I was not there when I should be. It has been over two years. I miss you so much.

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1. Introduction

In a recent couple of decades, free-standing silicon nitride (SiN) membranes became widely used in Micro-Electromechanical System (MEMS) and Nano-Electromechanical System (NEMS) fields for their high mechanical quality (Q) factor (i.e., low energy dissipation in resonance [1]–[3]). Thus, thin mechanical resonators made by SiN membranes have become promising for various MEMS applications, such as optomechanics [4], mass sensing [5], force sensing [6], thermal sensing [7], flow measurement [8], etc. Furthermore, our group relies on such membranes for several research projects on thermal radiation sensing in the far-field [9] and near-field [10].

For example, one of projects in our laboratory is to build a high sensitivity thermal radiation sensor using large area SiN membranes [7], [11]. In this research, our lab confirmed that the radiative heat transfer can dominate total heat transfer between a large size SiN membrane and a heat source, overcoming the conductive heat transfer [11]. Using a high mechanical Q-factor SiN membrane resonator as a thermal radiative sensor can eliminate the Johnson-Nyquist electrical noise [7]. Removing this source of noise could potentially result in two orders of magnitude noise floor improvement, compared to current photodetection [7], [10].

Another use of the SiN membrane by our lab is to accomplish Near-Field Thermophotovoltaic (NFTPV) energy conversion [13]. As very close distances (i.e., in the near-field, typically < 100 nm [14]), thermal radiation heat transfer can exceed the black body heat transfer limit between a hot emitter and a cold photovoltaic cell [15]. Theoretical models show that using this effect could lead to high efficiency energy conversion from waste heat to electricity on a small portable scale [16]. Thin silicon nitride membranes are a tool for these applications. A hot membrane can be

brought close to a PV cell and excited in mechanical resonance, with a controlled amplitude, in order to adjust the Membrane-PV cell distance, and thus achieve near-field heat transfer. Additionally, large size membranes can allow more radiation heat transfer, and thus more power.

Usually, when research groups use SiN membranes resonators, they either fabricate their own membranes with the desired geometry or rely on commercially available membranes (see Figure 1.1). However, most groups publish only general fabrication process steps instead of detailed recipes; such fabricating of such membranes for the first time remains a substantial challenge.

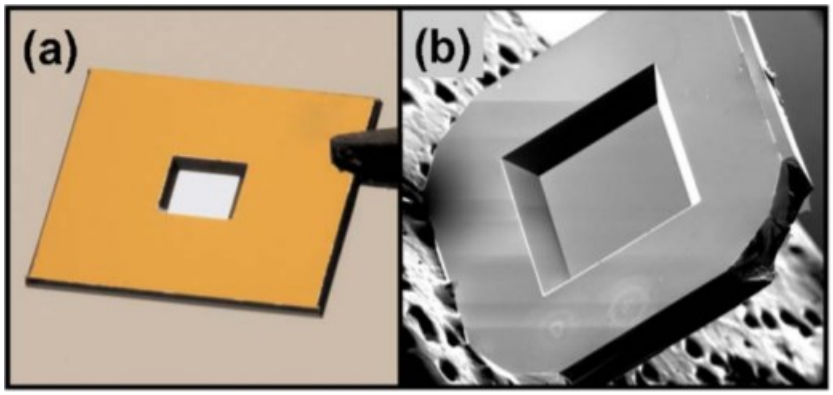

Figure 1.1 (a) Photograph of a 1mm x 1mm x 50 nm SiN Membrane from Norcada. (b) Scanning Electron Microscopy (SEM) of a 1mm x 1mm x 50nm SiN Membrane from SPI. Taken from [17]

The first of two goals of this thesis is to develop a detailed recipe for fabricating large area, rectangular shape Low Pressure Chemical Vapor Deposition (LPCVD) SiN membrane at uOttawa. This goal is a cornerstone of most projects in our laboratory that employ SiN membranes, most notably the two projects described above [9], [10]. Before fabricating our own SiN membranes, we relied on membranes bought from the company Norcada. They are made from 200 μm double side polished single-crystal silicone (Si) wafer with 200 nm LPCVD SiN coated. Since they are very easy to break under tweezer manipulation due to the thin frame, we decided to use 500 μm

single side polished single-crystal Si wafer with 100 nm LPCVD SiN coated for our own fabrication. We choose thinner membranes, which lead to a higher mechanical Q-factor for the same size area (see Figure 1.2) [18]. We use standard photolithographic techniques to fabricate SiN membrane, which will be explained in detail in the following chapters.

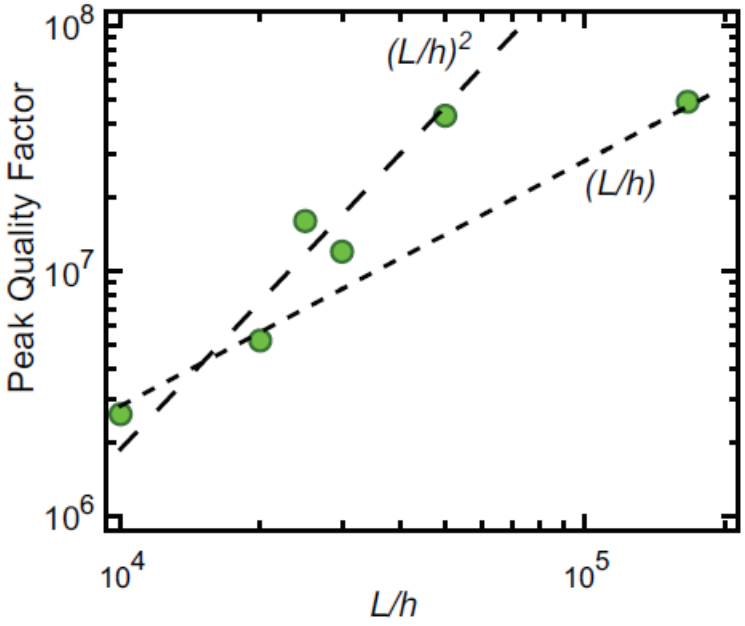

Figure 1.2 Peak mechanical quality factors versus film geometry parametrized by the ratio of membrane width (L) to membrane thickness (h). Taken from [18]

The second goal of this thesis is to develop an integrated mechanical actuator for exciting the mechanical resonances of these membranes. For membranes resonators, various actuation methods exist, which can be classified into two main categories: off-chip actuation and on-chip actuation. Piezo actuation is a common off-chip actuation method, i.e., actuation using the acoustic wave created by a piezo-electric piece of ceramic glued close to the membrane chip [19]. Optical actuation using the radiation pressure of photons is another example of off-chip actuation [20], [21]. Both are classified under the off-chip category because they do not integrate the driving

device on the resonator. On the other hand, on-chip actuation methods can drive the membrane film directly with a device built on the resonator. There are three main types of on-chip actuation methods that can be applied to membrane resonators: electrothermal, magnetomotive and electrostatics.

The actuation method currently employed by our lab is off-chip piezo actuation, combined with an optical interferometer for vibration sensing [7]. Usually, MEMS and NEMS resonators are designed to fit in small and limited space. Therefore, as an off-chip actuation method, the piezo actuator works fine for driving the membrane at its resonance frequency in a laboratory setting, but it is unpractical for an eventual mature product. On-chip actuation methods can deliver better applicability since they can be fabricated on membrane chips within a desired small space.

In the long run, the finished device will be used for thermal radiation sensing in high vacuum. Radiation sensing is not the goal of this thesis itself, but it defines several requirements, as it prevents the use of several existing actuation methods. For example, it prevents the use of the electrothermal actuation method [22], which would cause actuation heat to interfere with the detected heat signal. Similarly, magnetomotive actuation [23] uses an electrical conductor in a magnetic field. The electric current in the conductor creates a Lorentz force that drives the resonator. This actuation method requires external magnets, which can be complex to implement in limited spaces. Joule heating in the wire is also a concern. Electrostatic actuation takes advantage of the electrostatic force between two charged electrodes to drive resonators. There is electric current passing between two electrodes but minimal heat dissipation from the circuit if the resistance is small. Therefore, Joule heating can be avoided from this actuation method. This

method also usually requires deposition of an electrically conductive layer on the membrane, which can result in detrimental Q-factor reductions (i.e., high Q-factor is key to thermal sensor's sensitivity). Optical actuation [24] is applicable for small spaces and can result in limited heat interference. However, its force is relatively small to drive large size membranes such as ours. The requirement of a highly stable laser is also a drawback in many practical situations.

This work focuses on developing a new actuation method by generating acoustic waves in the underlying silicon substrate supporting the resonator. Previously, the effect of utilizing acoustic waves from p-n junction under reverse bias [25] for actuation was observed in cantilever resonators. Similar to this actuation method, in this work, a capacitively coupled metal-dielectric-semiconductor (MDS) on-chip actuation system is developed for multiple eigen vibration modes based on large size high Q-factor LPCVD SiN membranes.

In terms of thesis contribution, the microfabrication technique used for membrane fabrication is relatively standard [26]. Therefore, the contribution in this work is mostly optimizing the procedure and fine-tuning of the recipe (e.g., photoresist spin coating thickness, reactive ion etching time, KOH temperature, and so on) for future users of our lab. The shadow mask process for the aluminum metal electrodes deposition is non-standard (see Chapter 3.2.1). It is developed with an ultra-fast laser in Dr. Weck's lab. The junction actuation technique is comparable to previous work on micro-cantilever [27]. However, it is used for the first time to actuate SiN drum resonators, and is therefore the subject of a research article submitted to Sensors and Actuators A: Physical.

Because of these two distinct goals, the thesis can be divided into two distinct parts. Part 1 consists of Chapter 3. It describes the SiN membrane fabrication with the detailed recipe and corresponding failure mechanisms and solutions. Part 2 consists of chapters 4 – 6, which describe the actuation technique modeling (Chapter 4), measurements (Chapter 5) and discussion (Chapter 6). Chapters 4, 5, and 6 are in large part excerpts of an article being prepared for submission. Readers should expect to find some repetitions between these chapters and the introduction (chapter 1), literature review (chapter 2), and fabrication (chapter 3) sections.

2. Literature Review

The literature review is separated into two subsections on (1) large SiN membrane fabrication and (2) metal-dielectric-semiconductor (MDS) on-chip actuation.

2.1 Silicon Nitride Membrane Fabrication

The most common optimized fabrication technique for obtaining large-area Low Pressure Chemical Vapor Deposition (LPCVD) silicon (Si) nitride (SiN) membranes is the standard lithographic method. It is similar to typical semiconductor fabrication, such as integrated circuits used in the computer's central process unit (CPU). Figure 2.1 shows the general procedure for the fabrication of SiN membranes.

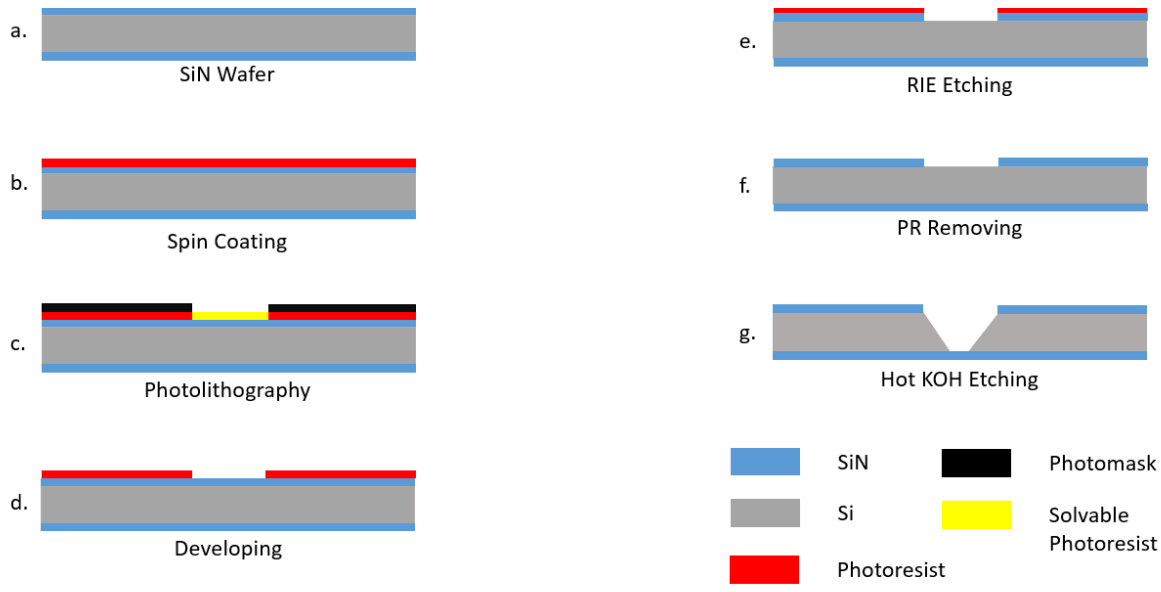

Figure 2.1 General Procedure of Standard Lithographic Method for Rectangular Shape SiN Membrane Fabrication.

In this case, the LPCVD silicon nitride is coated onto the (100) single-crystal silicon substrate (see Figure 2.1.a). The (100) is the Miller convention for the notation to identify a specific lattice plane in Miller Indices (see Figure 2.2) for single crystal materials such as Silicon. The wafer is first coated with a photoresist (PR) by spin coating. After soft bake (low temperature heating step), the PR polymerizes to a thin layer on the wafer shown in Figure 2.1.b. This PR layer is extremely sensitive to ultraviolet (UV) light. The polymerized PR layer will become soluble in some specific developer solutions after UV light illumination, called exposure. Therefore, a UV light is applied to the PR through a photomask to form desired patterns on the PR layer (see Figure 2.1.c). The photomask is a rectangular chrome coated quartz glass plate with designed patterns, ordered from NanoFAB in the University of Alberta. After a rinse with the developer, the solvable PR is removed, which is shown in Figure 2.1.d. Figure 2.1.e illustrates the result of the reactive ion etching (RIE) process. The principle of the RIE method, a dry etching method, is to use chemical reactive plasma to remove materials on the substrate in a plasma chamber. The etch rate depends on various factors, such as the chemical species in plasma gas, plasma gas flow rate, chamber pressure, input power, materials' properties on the substrate, etc. [28] Hence, an optimized recipe for every specific etching machine is critical for controlling etching rate. During RIE etching, the plasma attacks everything on the wafer surface with different etch rates for different materials. However, the PR layer protects the SiN layer underneath. Thus, the plasma only removes the SiN that is not covered by PR. Then, the silicon substrate is exposed. After removing the PR (see Figure 2.1.f), the wafer is immersed into a hot potassium hydroxide (KOH) solution for wet etching. The single-crystal silicon has the three relevant lattice planes shown in Figure 2.2. A commonly used silicon wafer is a (100) single-crystal silicon wafer, meaning that a 100 plane is exposed on the front surface. There is a 54.7˚ angle between the (100) plane and the (111) plane (see Figure 2.3) [29], [30]. During the

hot KOH etching, the solution will attack the (100) plane and the (110) plane much faster than the (111) plane. Therefore, the final shape of the etched silicon frame of the wafer is defined by the (111) plane. Furthermore, only rectangular shape membranes can be fabricated with hot KOH etching because of the etching along the (111) plane. With proper control of the etching temperature, the KOH solution concentration and the etching time, rectangular shape SiN membranes are created at the wafer's bottom (see Figure 2.1.g). This general procedure is also applicable for fabricating microcantilever beams and strings[31], [32].

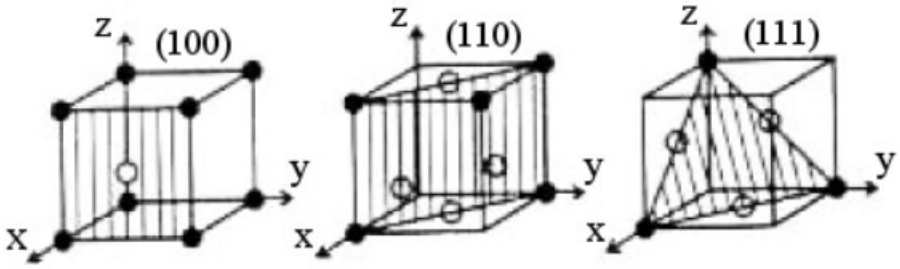

Figure 2.2 Three Specific Planes in Miller Indices for Single-crystal Silicon. Taken from[30]

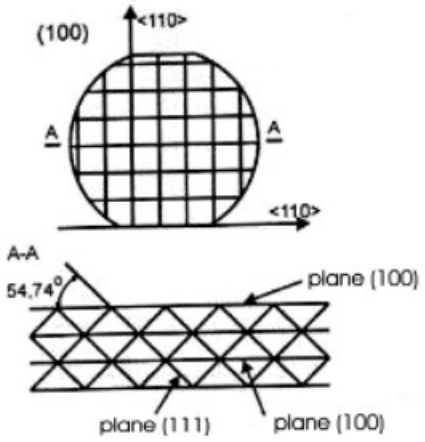

Figure 2.3 Planes Configuration for (100) Single-crystal Silicon Wafers. Taken from [30]

The hot KOH etching is the foremost step to isolate the SiN membrane from the Si frame. The relative working principle is the large selectivity ratio between SiN and Si. The selectivity of Si:SiN in [29] is 49000:1 for a temperature setpoint of 85 °C. When the temperature is under 85 °C, the selectivity reduces and reaches about 33000:1 [29]. Therefore, in hot KOH etching, it is customary to lose some of the SiN layer thickness. For example, etching 500 µm of silicon would consume approximately 11 nm of the SiN film. The precise SiN layer thickness at the end of the process should be experimentally verified if needed.

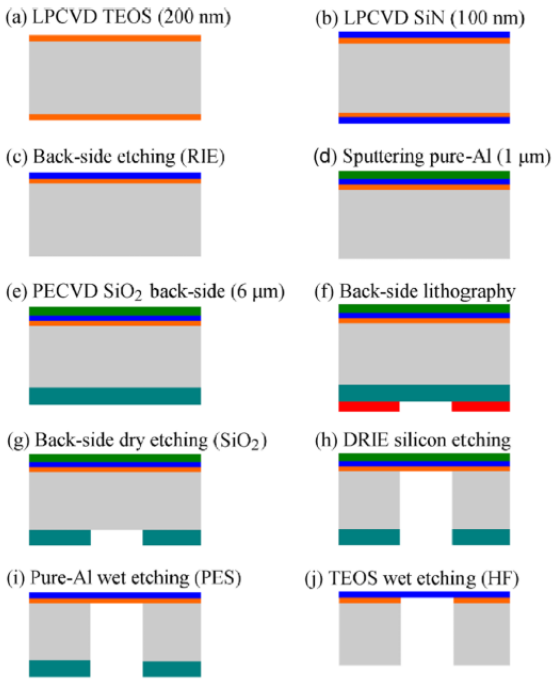

Figure 2.4 (a)-(j) Large-area Circular Silicon Nitride Membrane Fabrication Steps. Taken from [33]

Variants exist for non-rectangular (e.g., circular) membranes. Figure 2.4 depicts the general fabrication procedure for large area circular silicon membranes [33] with the Deep Reactive Ion Etching (DRIE) method in lieu of KOH etching. In this case, etching does not have to follow the

crystal planes, as for KOH, such that nonrectangular shapes can be obtained at the expense of a more complicated fabrication process. A double-side-polished Si wafer with 500 μm thickness is firstly immersion cleaned with 99% HNO_3 and 65% HNO_3 at 110 ℃. Then, 200 nm thick silicon dioxide layers are deposited onto both sides of the substrate with the LPCVD method by using tetraethylorthosilicate (TEOS) as a precursor in step (a). In step (b), a 100 nm thick silicon nitride layer is added two both sides by LPCVD. With backside etching, the silicon substrate is exposed in step (c). During step (d), a 1 μm thickness pure aluminum layer is sputter on the top surface to protect the silicon nitride layer during DRIE. For protecting the required silicon frame from the DRIE, another 6 μm thickness silicon dioxide layer is deposited on the backside with plasma enhanced chemical vapor deposition (PECVD) in step (e). From the step (f-g), the circular shape pattern is formed by combining the photolithographic method and dry etching method, the Reactive Ion Etching (RIE). The silicon dioxide has a relatively large selectivity ratio to silicon during DRIE. Therefore, the DRIE will etch through the silicon substrate locally with a small amount of silicon dioxide layer sacrificed in step (h). The aluminum layer and the silicon dioxide layer are separately removed in step (i-j).[33] This fabrication procedure is not only suitable for circular shape silicon nitride membranes, but also other complex shape membranes.

2.2 Review of Actuation Methods for High Q Membranes

Membrane mechanical resonators require actuation methods for accomplishing their intended purpose. Actuation methods can be summarized into two main categories, off-chip and on-chip. They are introduced in the following subsections with several representative examples.

2.2.1 Off-chip Actuation Method

2.2.1.1 Piezo-actuated

As an off-chip actuation method, piezo actuation is widely used for driving MEMS or NEMS resonators. It is simple to use a piezo-electric piece of ceramic as an actuator to drive resonators by mounting a piezo, with glue or tape, on the resonator's frame or some components connected to the frame of the resonator [9], [10]. Its working principle is to use the expansion and contraction phenomena due to the piezoelectric crystal charging. The expansion and the contraction originate from the crystal structure in the piezo ceramic [34]. The nature of the crystal structure is similar to a capacitor (i.e., unlike charged electrodes produce attraction, like charged electrodes produce repulsion). Therefore, sending different electrical signals can make crystal structure either expand or shrink respectively. With high-frequency change on electrical signal for piezo, the piezo can also produce acoustic waveform in terms of high-frequency vibrational mechanical motion due to quick expansion and contraction .

As mentioned earlier, this actuation method is currently employed in our laboratory to drive the SiN membrane resonator (see Figure 2.5) [35]. As shown in Figure 2.5 and Figure 2.6, the membrane chip is attached to one side of the glass slide with double-sided tape, and the piezo ceramic cube is mounted on the glass side with nickel paste. The acoustic wave generated by the piezo propagates through the glass slide and the frame of the membrane chip to the SiN membrane resonator.

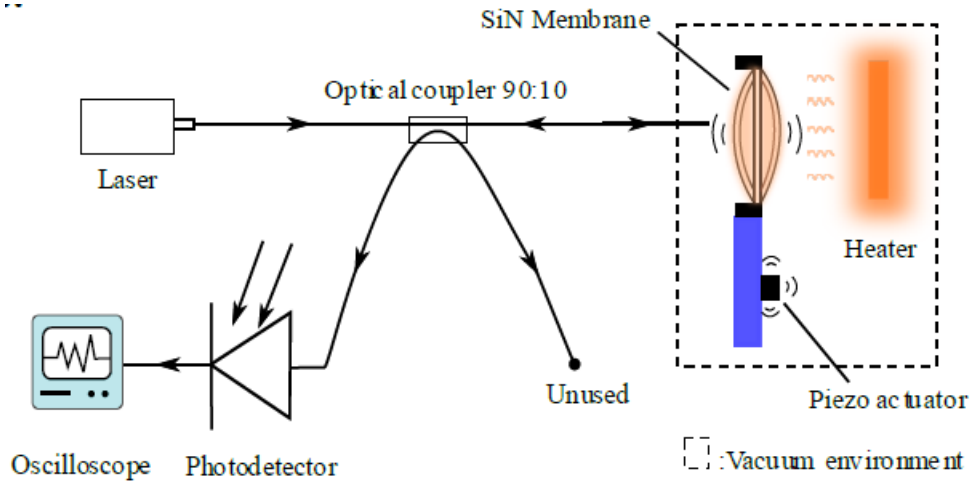

Figure 2.5 SiN Membrane Thermal Radiation Sensor with Piezo Actuation and Optical Detection. Taken from [35]

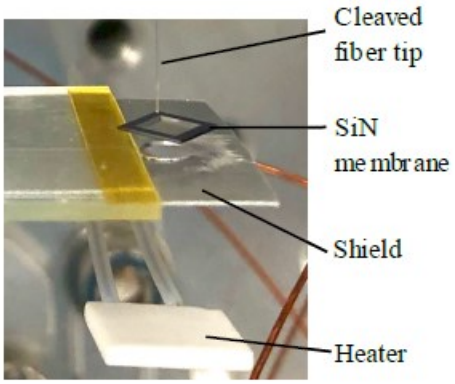

Figure 2.6 A Detailed Look for SiN Membrane in Vacuum for Figure 2.5. Taken from[35]

2.2.1.2 Optical

The optical actuation method can be classified into three types by force forms: radiation pressure, gradient optical force, and photothermal force [36]. Among these three methods, radiation pressure is the most basic form of optical force, which can be used as off-chip actuation methods for MEMS and NEMS resonators [36]. The working principle of it is to transfer momentum from the propagating electromagnetic field of light to the resonator (see Figure 2.7) [36]. For example, in [37], a microtoroid structural resonator is driven by radiation pressure which is generated from a

tapered optical fiber connected to a single-mode, tunable, external-cavity laser (see Figure 2.8).

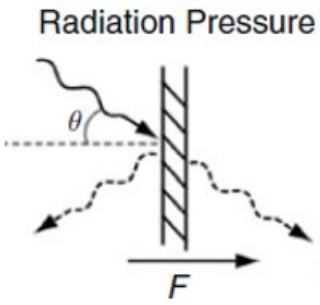

Figure 2.7 Schematic for the Radiation Pressure Working Principle of Optical Actuation. Taken from [36]

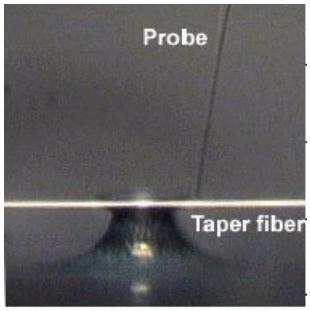

Figure 2.8 A Microtoroid Structural Resonator Actuated by Radiation Pressure from A Single-mode, Tunable, External-cavity Laser Transported by A Tapered Optical Fiber. Taken from [38]

2.2.2 On-chip Actuation Method

2.2.2.1 Electrostatic (Capacitive) Actuation Method

The electrostatic force is well known as an actuation method for membrane resonators, as well as MEMS and NEMS in general. It can be simply achieved by depositing a thin conducting layer on the membrane resonator surface as one electrode and adding one more fixed electrode externally to form a capacitive actuation (see Figure 2.9). However, the electrode may be detrimental to the resonator performance. Having a continuous conducting layer requires relatively large metal

thickness (e.g., 5 nm Chromium and 17-20 nm gold on 230-250nm SiN film [39]). Coating the whole resonator with metal was proven to increase effective mass and degraded mechanical quality factor [19], [39] (i.e., higher mechanical dissipation). In most applications, this cannot be tolerated since the membrane's high Q factor and lightweight are essential, especially for sensors [40]. Additionally, metallization of the membranes will also cause undesired bending and buckling from thermal stress. Fortunately, there is a circumvention method by only applying mental deposition on the area, which does not have a strong impact on the Q factor of the resonator [19], [41]. In this case, the metallization is gradually applied onto the ceramic microcantilever from both the clamped end and the free end, as shown in Figure 2.10.

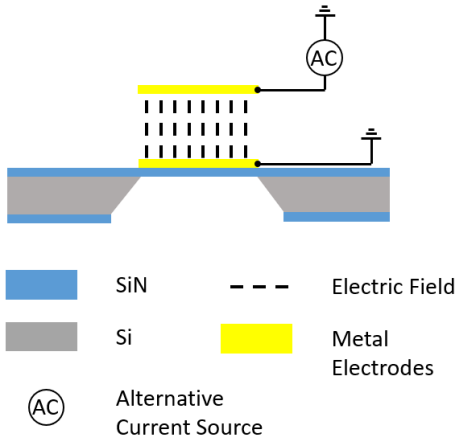

Figure 2.9 Schematic for A Typical Capacitive Actuation System on SiN Membrane

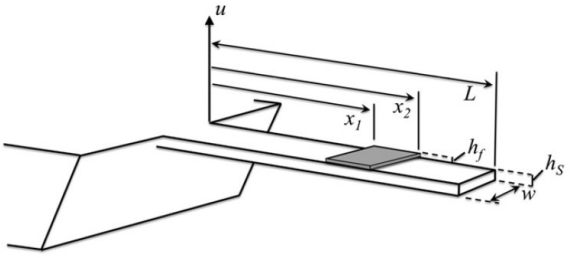

Figure 2.10 Schematic illustration of a microcantilever beam of length L with a thin film coating over a portion of the top surface. Taken from [41]

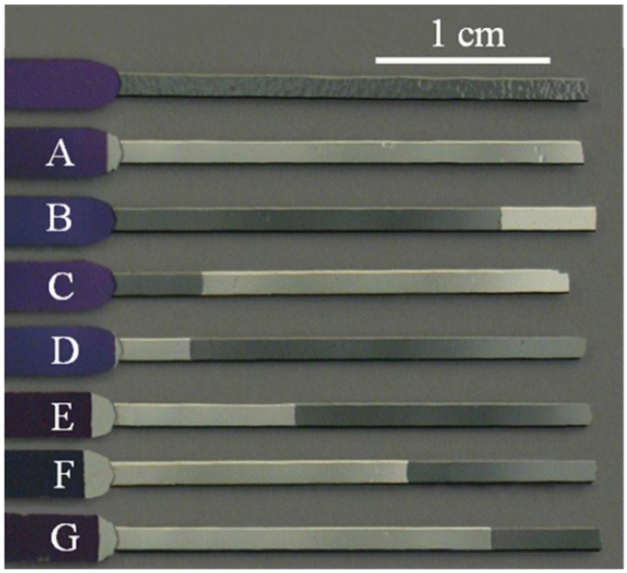

Figure 2.11 Composite Photograph of Representative Single-crystal Silicon Microcantilever Patterned Electively with 100 nm Thick Films of Aluminum with respect to Table 2.1. Taken from [41]

Table 2.1 Details of Selective Metallization for the Seven Sets of Single-crystal Silicon Microcantilevers. Taken from [41]

	Beam set	Start position (x_1/L)	End position (x_2/L)
	Set A—fully coated	0	1
	Set B—coated 20% from tip	0.80–0.81	1
	Set C—coated 80% from tip	0.17–0.21	1
	Set D—coated 20% from root	0	0.16–0.17
	Set E—coated 40% from root	0	0.39–0.41
	Set F—coated 60% from root	0	0.59–0.65
	Set G—coated 80% from root	0	0.80–0.84

There are seven microcantilevers shown in Figure 2.11 with different selective metallization geometries with numerical represented in Table 2.1. There is also one bare microcantilever without metallization as a reference sample. The result (see Figure 2.13) clearly shows how little (near to zero) the metallization does affect the microcantilever if it starts from the free end tip. In contrast, the selective metallization, which starts from the clamped end, performed quite the opposite, as shown in Figure 2.12. Two vibration modes were studied in this research. Each of them exhibits different characters in both Figure 2.13. and Figure 2.12. Meanwhile, for the same mode, comparing two different metallization starting points, the result represents the opposite relationship between the normalized length of selective metallization and the fractional damping increase.

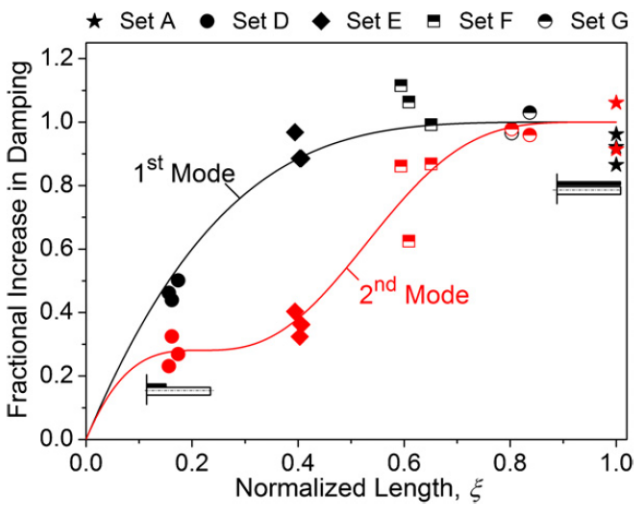

Figure 2.12 Comparison of damping measured in partially metalized silicon beams with the length (0.2L, 0.4L, 0.6L, 0.8L and 1.0L), which starts from the clamped end, that they cover along the axis of the beam for the first mode and the second mode. Taken from [41]

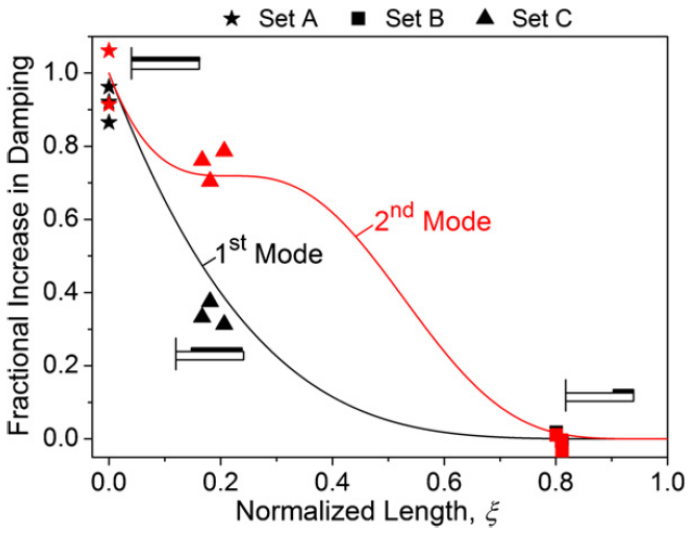

Figure 2.13 Comparison of damping measured in partially metalized silicon beams with the length (0.2L, 0.8L and 1.0L), which starts from the free end, that they cover along the axis of the beam for the first mode and the second mode. Taken from [41]

In short, metallization geometry can minimize the impact of the metal film on the resonator damping coefficient. However, there are some other considerations as well. For example, with the same metallization geometry on the resonator, different target resonance modes can result in different levels of Q-factor degradation. It is also possible to compromise between the higher capacitance and the Q-factor degrading. From [41], with the same size metalized area (i.e., considering to provide same capacitance), the damping ratio varies significantly for different metallization positions on the resonator (i.e., There is a more negligible damping effect to the resonator when the metallization locates at the cantilever free end than the clamped end). Although this selective metallization technique is studied on the microcantilever resonator, in theory, it is also applicable for large size membrane resonators. For example, [19] showed that avoiding metal at the membrane clamping points leads to lower Q-factor deduction due to the metallization.

Besides the selective metallization technique, graphene coating can be another solution because of

its extremely lightweight and excellent electrical conductivity. In theory, the conductive graphene coating for silicon nitride membranes reduces the quality factor by less than 30% on average [42]. This graphene coating technique fully covers the top of the membrane. As shown in Figure 2.14, the two gold strips attached to the monolayer graphene are used for conducting electricity and use the graphene as an electrode in the actuation system. The other conductive electrode is the silver mirror on the piezo stack which can be found in the system shown in Figure 2.15. Therefore, with the target resonant frequency and the gate voltage, Vg, applied between these two electrodes, the membrane can be driven to the desired resonance frequency. Vg consists of both DC and AC voltage sources. The DC source defines the amplitude of the membrane deflection, while the AC source provides the drive frequency. This actuation system has two frequency detection methods, electrical and optical. The electrical detection, which is also a capacitive detection, uses the drain gold strip in Figure 2.14 to receive the radio frequency (RF) signal created by the capacitance change between the silver mirror and the graphene coating. This RF signal is relatively weak and needs to be amplified for further processing. For the optical detection, the Fabry-Perot cavity formed between the silver mirror and the graphene can vary the reflected light from the laser source for further optical signal detection by the fast photodiode. The two signals from each detection system are processed in the network analyzer to tune the frequency and the deflection amplitude for actuating the graphene-on-silicon-nitride high Q resonator [43] in a close control loop.

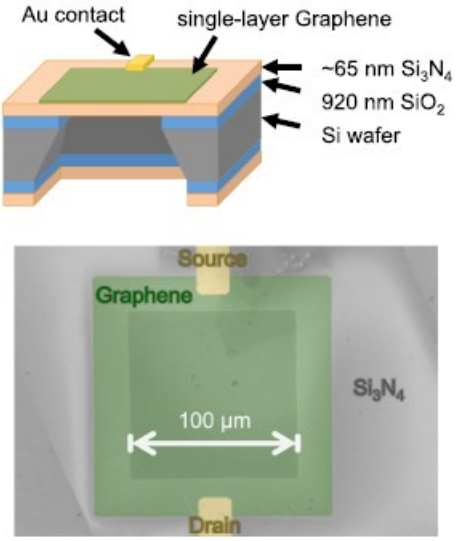

Figure 2.14 Graphene-on-silicon-nitride High Q Resonator Device Layout and Corresponding Scanning electron microscope (SEM) micrograph. Taken from[43]

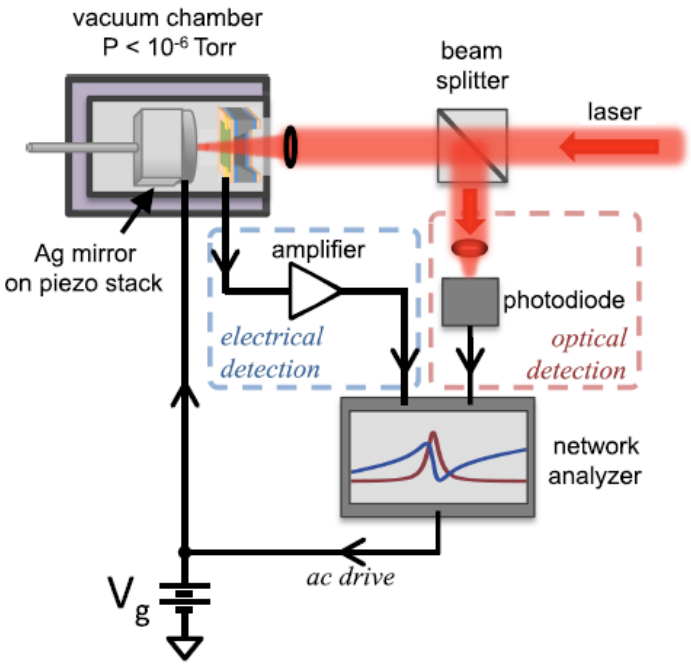

Figure 2.15 Schematic of Capacitive Graphene-on-silicon-nitride High Q Resonator. Take from[43]

2.2.2.2 Magnetomotive Actuation Method

This actuation method relies on the Lorentz force in magnetic fields, i.e., forces perpendicular to the direction of charge displacement in magnetic fields. For example, in Figure 2.16 (taken from [23]), the Lorentz force is used for both membrane excitation and detection. As shown in Figure 2.17, two sets of Halbach array magnets are used to create a strong magnetic field at the membrane location. In order to take advantage of the Lorentz force as much as possible, the membrane chip is placed between two magnets with its three electrodes perpendicular to the magnetic field lines. By applying alternate current to actuation electrodes with the frequency matching to the resonance frequency, two opposite directions of Lorentz forces, which are all perpendicular to the membrane, will act on actuation electrodes and drive the membrane to target resonant mode. During the membrane's deflection, the corresponding motion of the readout electrode in the magnetic field will generate induced current, which can be picked up by the lock-in amplifier as electrical detection. According to the signal from the readout electrode, both the movement and the frequency of the membrane's motion can be measured.

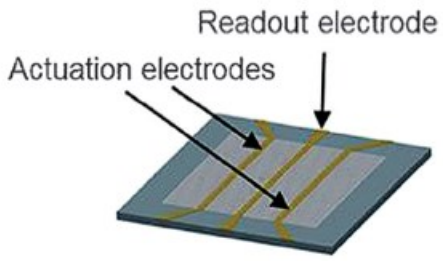

Figure 2.16 On-Chip Magnetomotive Actuation Resonator. Taken from[23]

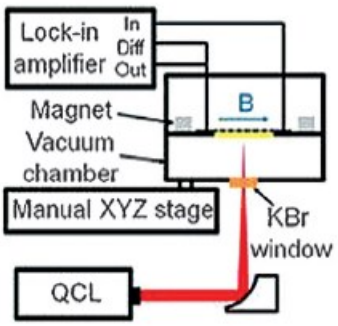

Figure 2.17 Magnetic Transduction Scheme for Silicon Nitride Membrane. Taken from [23]

2.2.2.3 Electrothermal Actuation Method

The working principle of the electrothermal actuation method is to use the thermal effect due to the Joule heating. First, this actuation method requires at least two layers made of different materials with large thermal expansion coefficient differences, which can induce large bending phenomena due to the different amounts of thermal expansion at the same temperature. This bilayer structure is also referred to as a bimorphic structure. Besides the oscillating component of the resonator (i.e., the SiN) is by default one of the two layers, the second material requires electrical conductivity to induce Joule heating due to the electric current passage. This is also a reason for building the second layer as a "U" shape to form a circuit loop. High melting points is another significant characteristic that the second layer should possess to prevent melting incident occurring during the heating actuation period [22]. Since the bilayer will be deformed during the actuation, the second layer material needs relatively higher yield stress to avoid plastic deformation [22]. According to these restrictions mentioned above, for the specific case in [22], as shown in Figure 2.18, nickel (Ni) is chosen to be deposited on the SiN to form two bimorphic actuators. When two actuators are electrically charged, based on the thermal expansion difference between the Ni and the SiN, the central SiN membrane will be rotated by the twist of two bimorphic actuators. As soon

as the power supply to actuators is switched off, the two actuators will return to their original place and generate oscillations which can propagate to the central SiN membrane to accomplish electrothermal actuation.

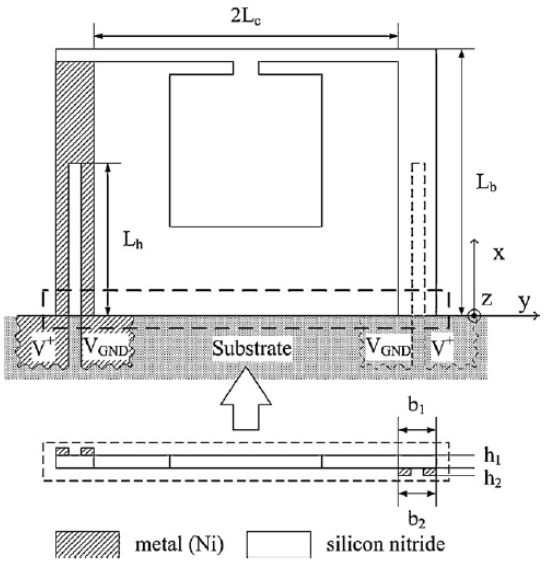

Figure 2.18 Schematic diagram for a twisting-type micromirror actuation system *with two bimorph actuators: top and cross-sectional views. Taken from [22]*

2.2.2.4 Optical Actuation Method

Instead of using radiation pressure to directly drive resonators as mentioned previously, utilizing a waveguide with gradient optical force [24] provides an integrated on-chip actuation method. The confined light with a symmetric optical mode in the waveguide cannot generate the gradient optical force by itself. Instead, it requires a driven part which is the nanostring in Figure 2.19a to induce the force and accomplish displacement readout function with an on-chip Mach-Zehnder interferometer (MZI) (see Figure 2.19b). From the result in [24], the gap distance between waveguide and nanostring negatively correlates to the optical force magnitude with other fixed parameters. Therefore, the magnitude of the force also can be increased by narrowing the

nanostring's width.

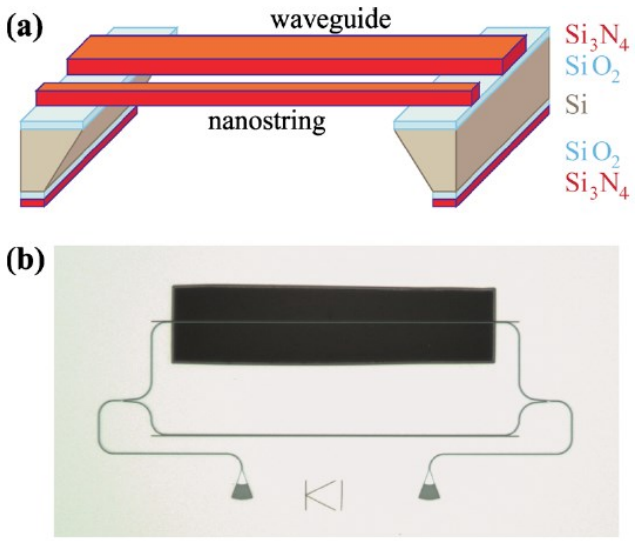

Figure 2.19 (a) Schematic illustration of the suspended waveguide and nanostring structure. (b) Optical micrograph of the device. Taken from [24]

2.2.2.5 Semiconductor Junction Actuation Method

This actuation method uses charges depletion in semiconductor junctions (i.e., p-n junction) to create vibration in the semiconductor substrate and lead to resonator actuation [25], [44]. The device in Figure 2.20 is a transducer from electronic energy to mechanical energy. When the device is charged by an AC voltage, the electrostatic force induced in the depletion layer varies, creating mechanical vibration in the structure. The induced force is relatively small, but when the drive frequency matches the resonator's resonant frequency, the vibration amplitude is amplified enormously according to its Q-factor.

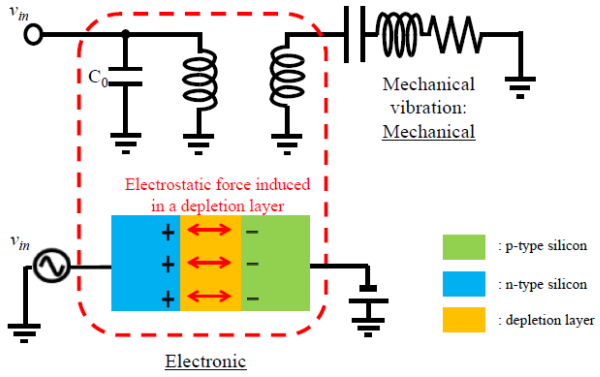

Figure 2.20 Schematic drawing of the principle of a p-n diode actuator. Taken from [25]

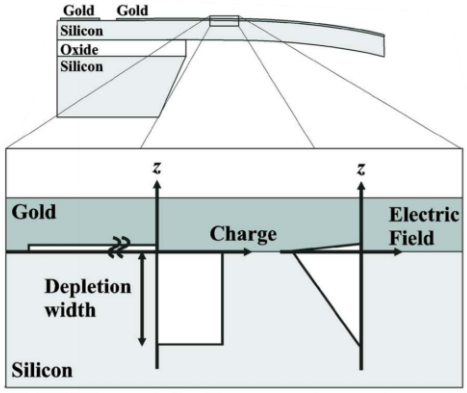

Figure 2.21 Silicon depletion layer actuator. Taken from [27]

This junction actuator technique works not only for n-type silicon and p-type silicon but also in metal-semiconductor junctions. In [27], a metal-semiconductor junction is formed between the silicon cantilever resonator a gold coating on the top surface (see Figure 2.22). The charge distribution in the gold layer and silicon cantilever generates forces due to voltage-dependent charges in both materials, and leads to mechanical stress to bend cantilever, as shown in Figure 2.21 for actuation.

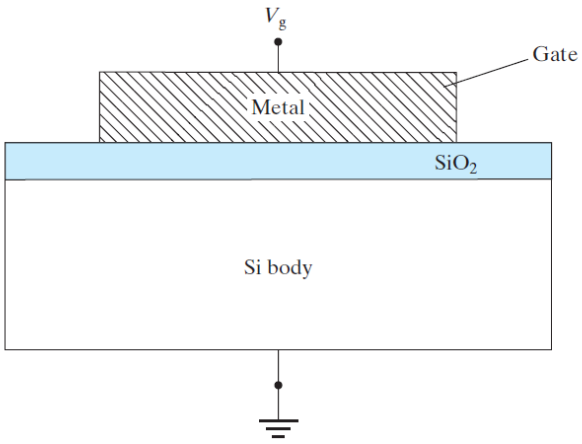

Figure 2.22 The MOS capacitor. Taken from [27]

Similar charge depletion and accumulation effects can also be observed in metal-oxide-semiconductor (MOS) structures [45], [46], although those have never been investigated for mechanical actuation. For example, in a MOS capacitor (see Figure 2.21), the depletion layer is created by the metal gate (or n-type silicon) and the p-type silicon substrate. Under the electric field's influence, charges distributed in the metal gate and the substrate induces electrostatic forces which can be utilized for resonator actuation.

The electrostatic forces are induced from metal gate and substrate charge distributions in the electric field. Particularly, when the workfunction difference between metal gate and substrate is in reverse bias to depletion case, the accumulation layer is formed and also leads to electrostatic forces for actuation due to accumulation charges in the capacitor. Both scenarios have the potential to create mechanical vibrations for resonator actuation.

2.2.3 Comparison of Actuation Methods

Among these actuation methods mentioned above, the piezo actuation method is arguably the most

convenient way to drive a resonator in a laboratory setting since it can be simply mounted by tape or glue. Once the piezo actuator is activated, the resonator frequency will tend to sync with the actuator. However, it is not optimal to use a piezo actuator in a mature product. Compared to the size of the resonator, the size of the piezo is relatively large. Usually, the product will not be designed to have ample space for piezo.

The radiation pressure of the optical actuation method requires optical equipment to emit a laser to drive the resonator. When the radiation pressure is propagated to the illuminated subject, it will also generate heat to the subject, which needs to be avoided for our projects [7], [11]. Nevertheless, it can also be used in driving and sensing schemes to build a fully integrated actuation system. Usually, optical equipment is more expensive. It is also more complex. With the same equipment, the optical system can be applied to more fundamental research projects.

In order to make use of the Lorentz force to achieve magnetomotive actuation, an electrical conductor needs to be placed into a magnetic field and have an alternative current passing through to generate Lorentz force. The electric current passage can induce the Joule heating effect, which must strictly be avoided for thermal radiation sensing. Magnetomotive actuation also requires external magnets to provide the magnetic field. For many applications, there is limited space for the resonator which means nowhere for external magnets. Except for these two shortages, a frequency readout scheme can be formed by means of the inverse utilization of the Lorentz force (i.e., the conductor moving in the electromagnetic field can produce induced current). Hence a fully integrated actuation system can be achieved by the magnetomotive actuation method.

Throughout actuation methods mentioned previously, the electrothermal actuation method allows for the largest deflection on oscillating component of the resonator, but there are also limitations for it to drive the resonator to high frequency [22]. Comparing with other on-chip actuation methods, it is easier to fabricate (i.e., only deposit electrically conductive material on the oscillating component), but it cannot be used for thermal sensors which means our project cannot use electrothermal actuation method.

The electrostatic (capacitive) actuation method described above [43] consists of two parallel electrodes and a capacitive cavity. Electrodes are usually made of electrically conductive materials (i.e., aluminum, gold, graphene) by metallization on the resonator. In order to maximize the deflection that the oscillator can achieve to drive the resonator, it requires higher electrostatic force exists between two electrodes. Based on the capacitance equation of the capacitor, this can be accomplished by narrowing the distance between two electrodes. However, locating two electrodes too close can also result in limited space for the deflection of the oscillator. Therefore, this becomes a trade-off between the deflection distance of the oscillator and the space between the two electrodes. There is also another limitation to the electrostatic actuation method. The electrode formed by metallization can degrade the Q-factor of the resonator which has an adverse impact on our project since we require the high Q-factor for thermal radiation sensing [7], [11]. However, metallization on the oscillating component selectively can minimize the impact on Q-factor [41].

The semiconductor junction actuation method utilizes charge depletion in the semiconductor substrate to produce varying electrostatic forms upon applying an electrical potential. In a typical MOS capacitor, charges distributed in the metal gate will create attractive forces with charges in

the p-type silicon depletion layer. These forces form internal mechanical stress and store strain energy in resonators. By varying the applied voltage, stored strain energy will be repeatedly released and restored, which will generate acoustic waves to excite resonators. For the accumulation model, it works the same way except obtaining charges in the accumulation layer instead of the depletion layer. Compared to the electrostatic actuation method, this method also requires metal deposition on the device chip [27]. However, the acoustic wave can propagate along the device substrate (see Figure 2.23), which means the junction device does not have to be on the resonating part of the device to accomplish actuation (i.e., traditional electrostatic actuation method requires metal deposition on resonator). The MOS capacitor can be formed by the metal deposition on the resonator frame if it is made of semiconductor material. In our case, acoustic waves can be created in the silicon chip frame and propagate to the membrane resonator. Additionally, the Q-factor reduction by the metal deposition on resonator in regular electrostatic actuation can therefore be eliminated.

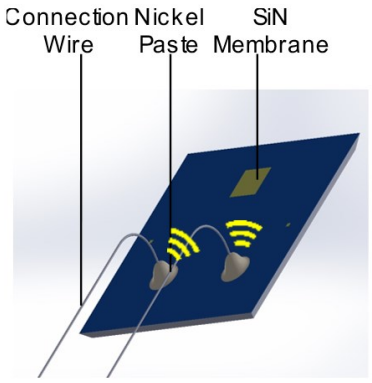

Figure 2.23 Acoustic wave propagates along the device substrate to the membrane resonator.

3. Fabrication of SiN membranes and actuation electrodes

3.1 SiN Membrane Fabrication

Development of the fabrication process of square shape large area size Low Pressure Chemical Vapor Deposition (LPCVD) Silicon Nitride (SiN) membrane chip—i.e., the first of the two goals of this thesis—is described in this chapter. The general process [26] is described in section 3.1.1, and more detailed information is provided for each specific step in section 3.1.2. Understanding these fabrication steps is required for the design of the photomasks, which is presented in section 3.1.3. After multiple trials and errors, our final recipe is developed and detailed for future users in chapter section 3.1.4. Finally, in the last section of this chapter (section 3.1.5), all overcome problems and corresponding procedure adjustments are listed to help future researchers avoid the same mistakes.

3.1.1 Overview

Figure 3.1 shows the general procedure of LPCVD SiN membrane chip fabrication starting from a four-inch single-side polished (100) single-crystal silicon wafer coated with LPCVD SiN. First, the wafer needs to be spin coated with photoresist (PR) on both sides (see Figure 3.1.b, c). Both coating processes need the soft bake heating process to polymerize the PR (i.e., decrease its solubility) [26]. During the exposure step, a photomask is then used to partially block ultraviolet (UV) light from the photomask aligner's lamp, thus forming patterns for further etching processes (see Figure 3.1.d). The etching step defines the final shape and size of the membrane. After the wafer is exposed to UV light, the exposed PR area becomes much more soluble than the protected PR area (covered by chrome on the photomask) in the developer solution [26]. A developer is associated explicitly with each PR series to remove soluble PR. After the development step, the

pattern of the photomask should be reproduced on the wafer. A proper rinse step for the wafer is required to clean the developer's residue before the wafer goes into the reactive ion etching (RIE) etching chamber. Figure 3.1.f shows a schematic of a membrane window expected after RIE etching. The SiN film under the developed area should be entirely removed by RIE etching [26]. The unexposed PR area should still have a thin PR layer left after RIE. RIE etching is the second step that can change the final geometry of SiN membranes after the photolithography. The RIE etching is used to duplicate the pattern from the PR layer to the SiN film. After the etching process, we will nominally have a perfect pattern match between the PR layer and the SiN film. However, many factors can affect the pattern duplication result, which means there will be changes in the geometry of the SiN film pattern (see subchapters 3.1.2.5 and 3.1.2.7). After RIE etching, the rest of PR needs to be removed by acetone before hot KOH etching (see Figure 3.1.g and subchapter 3.1.2.7). After KOH etching, the Si frame will be etched off from the designed SiN membrane area to have freestanding SiN membranes (see Figure 3.1.h) [26]. Hot KOH etching is the last step that can affect the membrane geometry significantly. Based on the Si frame's crystal structure (see section 3.1.2.7 and 3.1.3), the opening geometry on the unpolished SiN film formed from the RIE etching process is a bit wider than the final geometry of membranes that come out from the polished SiN film.

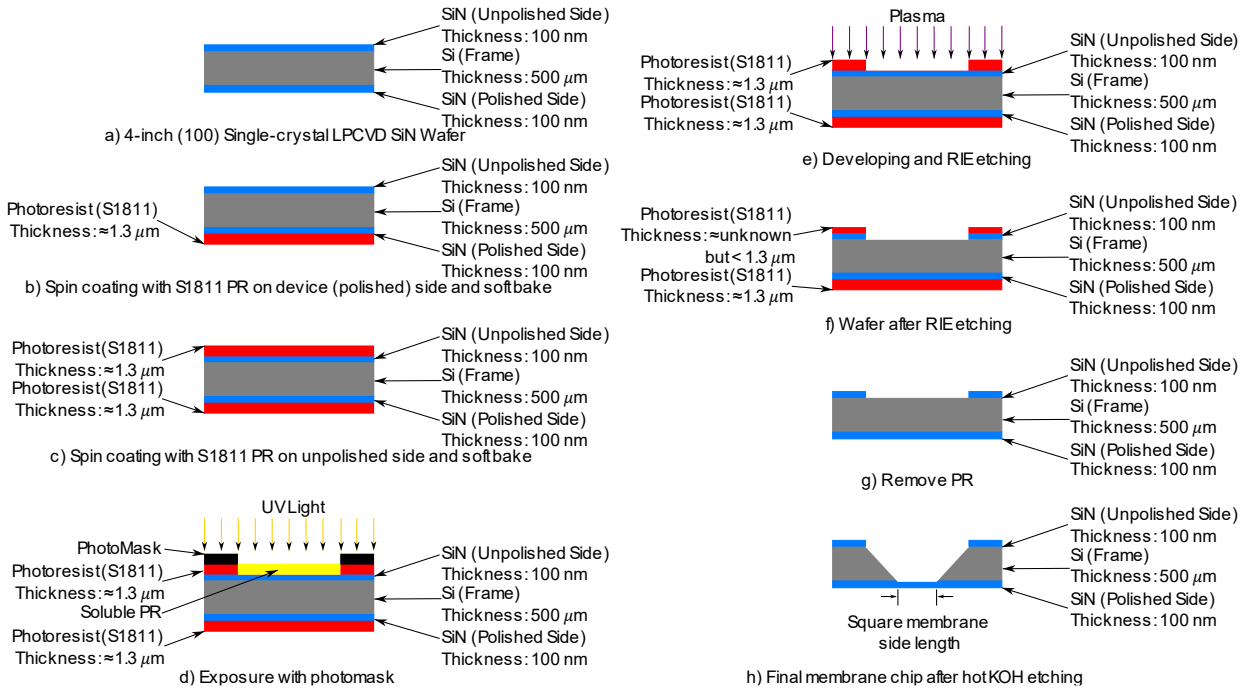

Figure 3.1 General Fabrication Procedure for SiN Membrane

According to this general SiN membrane fabrication procedure, we developed a detailed protocol for large area size SiN membrane chip fabrication. The following sections describe in more detail each fabrication step.

3.1.2 Extended Discussion for Each Fabrication Step

3.1.2.1 Spin Coating

Spin coating is used for spreading PR evenly on the wafer. There are two types of PR (i.e., positive PR and negative PR). The positive PR is turned soluble under exposure of the UV light. On the contrary, negative PR polymerizes (i.e., becomes insoluble) under UV light exposure. Therefore, after the exposure process, positive PR dissolves in the developer, but negative PR becomes extremely difficult to do so. However, negative PR without UV light exposure will dissolve in the developer.

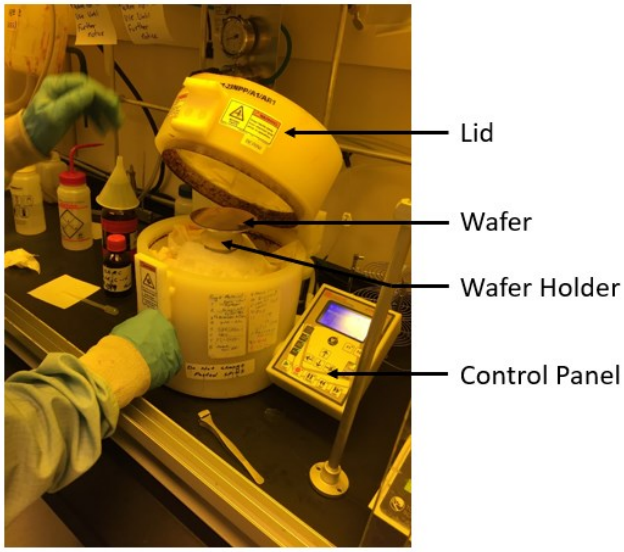

Figure 3.2 Laurell Technologies - ø150 mm Spin Coater

The spin coating machine uses centrifugal force to spread the PR evenly on the wafer to form a thin layer. Then, the PR is placed onto the wafer. As the wafer spins, excess PR is thrown away from the wafer, and the rest of PR stays on the wafer as a layer. In order to hold the wafer in place during the spinning process, there is a vacuum pipe inside to suck out the air between the wafer and the wafer holder to stabilize the wafer. The control panel is programmable for the spinning speed and time of spin coating. For different PR layer thickness requirements, the spinning speed and the time varies. For a given PR, a higher spinning speed (in RPM) results in a thinner layer and vice versa (see Figure 3.3). For certain spinning speeds, the uniformity has a logarithmic growth curve as a function of time [47]. As Figure 3.4 shows, as the spinning time increases, the profile of the film will tend to be flatter (i.e., more uniform). Giving enough time for spinning can eventually bring out a uniform film after spin coating. Therefore, the spinning coating program usually comprises at least three stages: acceleration, constant speed and deacceleration. The constant speed stage is the main stage for PR spin coating process.

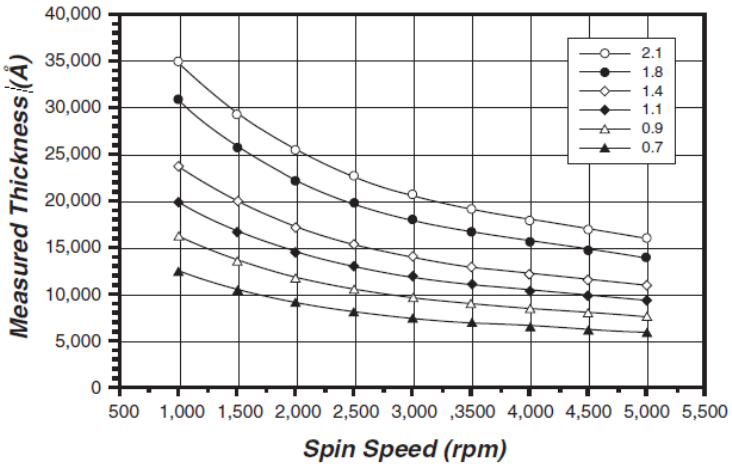

Figure 3.3 Spin Speed Curve of SPR955-CM Series Photoresist

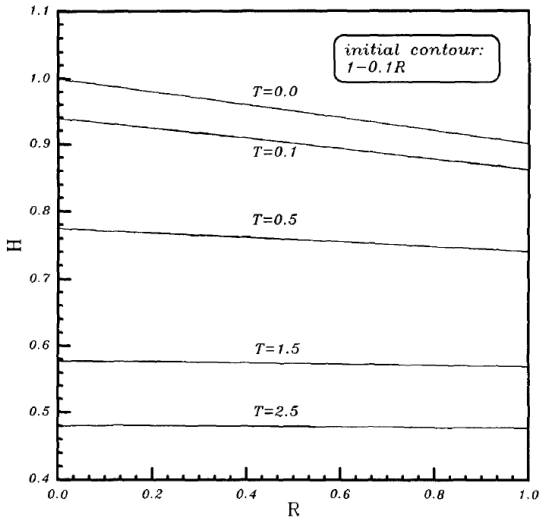

Figure 3.4 The Profile of Uniformity with Different Spinning Time Duration; H is the thickness of the film; R is the fractional radius of the wafer from the center to the edge; T is the time factor increased with longer spinning time duration. Taken from [47].

The original PR is in viscous liquid form. The PR can be diluted into a less viscous form with solvent, usually acetates. Thus, there are several grades for the same type of PR (i.e., different PR concentrations). In Figure 3.3, there are six grades for SPR955-CM series PR. The higher grade

means the higher viscosity and the higher concentration. With the same spinning coating process, the PR with a higher grade can form a thicker PR layer. This PR layer thickness difference can provide the wafer with various protection levels in RIE etching.

3.1.2.2 Soft Bake

The soft bake process is a slow heating process to polymerize the PR layer after the spin coating process from the viscous liquid form before the exposure step. Without a soft bake step, the viscous PR can contaminate the photomask during the exposure. Additionally, the soft PR layer from spin coating will lose its thickness uniformity during the hard contact step in the following exposure process. This can further affect the result after the RIE etching.

The temperature and the heating time for soft bake are specified for each PR. For example, as shown in Table 3.1, the soft bake process of S1813 PR is 115 ℃ for 60 seconds on a hotplate. The temperature and the duration of the soft bake process are linked to the type of solvent in the PR.

Table 3.1 Recommended Process Conditions for S1813 PR

High Resolution Process Parameters (Refer to Figure 1)	
Substrate:	Polysilicon
Photoresist:	MICROPOSIT®S1813® PHOTO RESIST
Coat:	12,300Å
Softbake:	115°C/60 sec. Hotplate
Exposure:	Nikon 1505 G6E, G-Line (0.54 NA), 150 mJ/cm^2
Develop:	MICROPOSIT® MF®-321 DEVELOPER
	15 + 50 sec. Double Spray Puddle (DSP) @ 21°C

3.1.2.3 Photolithography

The photolithography process comprises two sub processes: mask alignment and exposure. The photomask is the critical equipment of the photolithography process. As mentioned previously, the photomask (ordered from the University of Alberta nanoFAB in our case) is a rectangular single-side quartz glass plate coated with chrome patterns.

In the mask alignment process, the photomask must have its chrome-coated side facing the wafer. The frame of the photomask is made of quartz glass with high transparency to UV light. The transparent glass will allow the UV light to pass through, but process control is still crucial to ensure that the pattern in the PR reproduces as closely as possible the pattern of the photomask. It is the nature of the light to scatter. Too long exposure time, or a large gap between the photomask and the wafer, will create deformed (i.e., enlarged) patterns in the PR. Comparing to the Figure 3.5.b, the UV light scatters more to the PR layer in Figure 3.5.a and Figure 3.5.c. The more scattering UV light to the PR layer will result in less control on the geometry of soluble PR formation, which also means undesired PR layer pattern geometry after developing. After the mask alignment, the wafer needs to be pushed towards to photomask to avoid any gaps in between. There are two steps to push the wafer. The first one is to use a wafer holder with a screw underneath to control the height. Once the screw reaches its limit, there is an air jet to blow the wafer towards the photomask. This is commonly called hard contact. Hard contact is the best way to minimize the gap between the wafer and the photomask to avoid UV light scattering as much as possible.

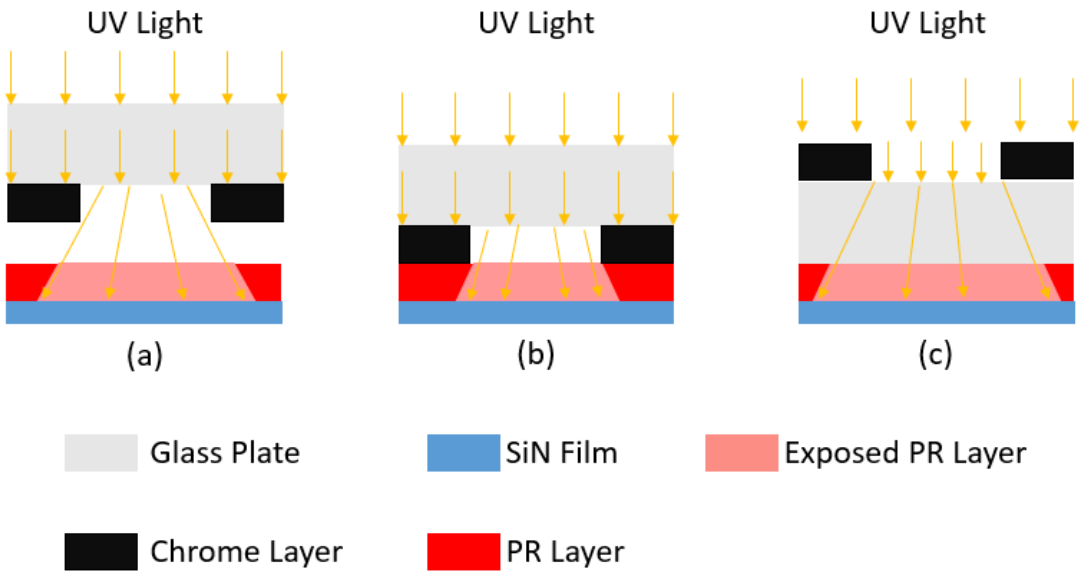

Figure 3.5 (a) Chrome Side Facing Down with Gap Between the Mask and the Wafer; (b) Chrome Side Facing Down without Gap Between the Mask and the Wafer; (c) Chrome Side Facing Up without Gap Between the Mask and the Wafer

For the exposure process, the key factor is the input energy of the UV light. There is a well-tested exposure energy input for each PR series with a unit of [mJ/cm^2]. Correspondingly, the output energy of the UV light lamp is in [mW/cm^2]. Therefore, the power and the time of exposure are two elements of input energy. By using Eqn 3.1, it is simple to have a precise exposure time. However, it is difficult to expose the PR with the same time period as calculated since the machine cannot be adjusted to milliseconds. Fortunately, there are different filter plates that can lower the intensity of the UV light which means less input power. Therefore, different filter combinations make it possible to be more precise on input energy with longer exposure time and lower input power. Furthermore, the input power can be read with an UV light intensity reader equipment. Although, the input energy of exposure can be set up strictly following the number given by the PR instruction menu, there are always some possibilities to have some errors due to different situations (i.e., less precise control on input energy quantity due to timer's fineness, light filter

selection, etc.).

$$\frac{Energy\ Input}{Input\ Power} = Exposure\ Time \tag{3.1}$$

There are three possible statuses after exposure (i.e., under exposure, correct exposure and over exposure). For correct exposure, the photomask pattern is perfectly copied to the PR layer after developing. After RIE etching, the SiN film will be removed in designed area and the rest area will still have a thin protection PR layer left on the top of the SiN film.

Insufficient UV light energy input can cause under exposure. It means not enough energy for PR to change chemical structure to become completely soluble. After developing, there will be some PR residual left on the pattern that should be removed. This can significantly affect the result after RIE etching. It needs more RIE etching time duration to accomplish the original etching goal. The original etching goal is shown in Figure 3.6.a. After the RIE etching, there should be some protection PR left on the top of the SiN film. Specifically, for under exposure, the PR protection for other areas may run out before the goal is achieved in RIE etching (see Figure 3.6.b). If the RIE etching is continued to remove the SiN film in the designed area, the SiN film in the unexposed area will also be etched off partially. Losing some thickness of the SiN film was found to be detrimental to membrane chip fabrication since it allows the KOH solution to penetrate through the thin SiN film, leading to critical process failure.

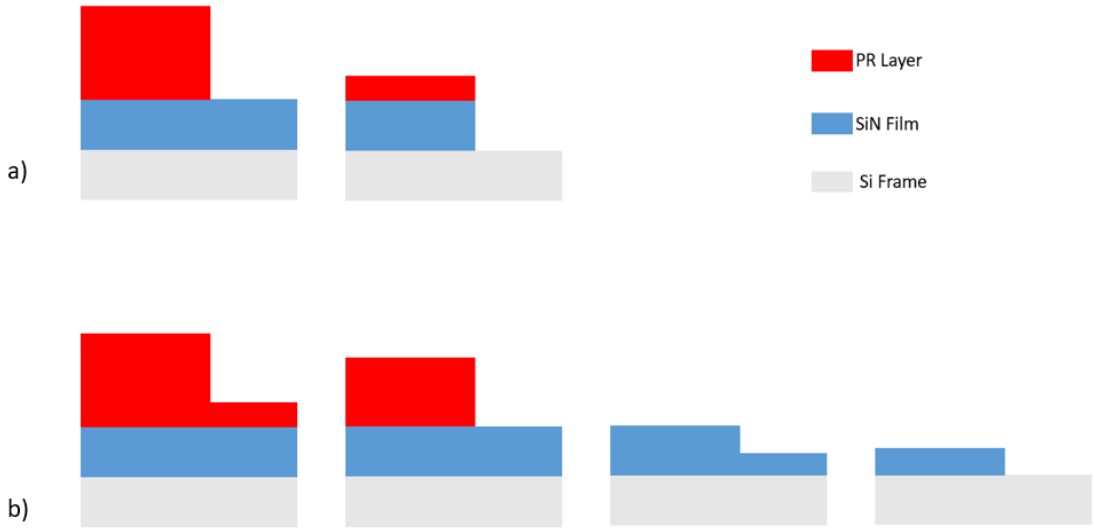

Figure 3.6 a) Correct Exposure in RIE Etching; b) Under Exposure in RIE Etching

Over exposure is usually caused by excess UV light energy input. It enlarges the soluble PR patterns and changes the final production geometry after etching processes.

3.1.2.4 Developing

The developer is a solvent solution to dissolve the soluble PR after exposure. Each specific PR series has its own developer which can be found in the PR's spec sheet (see Table 3.1). There are two different developing methods: immersion and spray. The spray method is more economical than immersion developing for industries using large quantities of the developer. In academia, immersion development is more straightforward and requires less specialized equipment. At the end of the developing process, both methods require a rinse process to remove developer residuals. The rinse step is usually carried with Deionized (DI) water.

3.1.2.5 RIE Etching

RIE etching uses plasma to gradually attack the surface of a target material by a mixture of

chemical reaction and physical ablation. The plasma in various types of inlet gases. Therefore, different input gas recipes can result in various etching rates for specific target materials. Additionally, RIE etching not only can be used for etching but also can clean some specific surface contaminations. For example, organic contaminations can be burned out and vaporized by oxygen plasma. There are various factors that can affect the etching result (i.e., input gas types, input gas flow rate, input power, vacuum chamber pressure and etching time duration). After developing a particular RIE etching recipe, it is crucial to control the etching time duration. Shorter and longer etching time duration can cause over etched and under etched situations respectively. In our case, the etching duration must be sufficient to remove the desired SiN pattern and prepare the wafer for further processing.

In ideal conditions, the plasma only removes the surface materials vertically from the substrate. In reality, it is possible to have some particles removed from the substrate by the plasma scattering to other directions, and then physically ablate around to form a larger cavity on the substrate. It will only cause a significant impact on extreme precise size control of patterns. Since we are planning to fabricate large area size SiN membrane, this issue can be neglected.

3.1.2.6 Rinse (PR Removal)

After RIE etching, there will still be some PR left on the wafer. Before proceeding to the hot KOH etching, the PR needs to be removed entirely. Acetone is a suitable solvent to dissolve PR quickly. However, after cleaning PR with acetone, there will be some residual from acetone which can contaminate the KOH solution. Therefore, isopropyl alcohol (IPA) and DI water can eliminate the residual from acetone and IPA respectively. The immersion rinsing method is applied for every

rinse step to maximize cleaning purposes.

3.1.2.7 Hot KOH Etching

Hot KOH etching can etch the Si frame to isolate the SiN film. The typical hot KOH etching requires 80 ℃ as etching temperature and 30% (w/w) KOH solution. During the etching process, an oil bath heating method is used to maintain a constant temperature for a constant etching rate. Changing the etching rate in the etching process can cause different surface roughness on the Si frame.

To prepare the KOH solution before heating and etching, pure KOH salt needs to be dissolved in clean DI water inside a clean glass breaker to guarantee the purity of the KOH solution. Since KOH is a strong base, dissolving KOH salt will generate a large amount of heat. Thus, the KOH salt needs to be added to DI water gradually.

For the heating method, the oil bath is chosen because oil has a much higher boiling point than water (see Figure 3.7). The temperature of the liquid bath is always higher than the temperature of the target solution (KOH solution in this case). Therefore, the temperature of the liquid bath needs to exceed 80 ℃. The water bath method is inappropriate since its boiling point is only 100 ℃. Another reason to use an oil bath is that the oil has a much lower evaporation rate than water does at the same temperature. This eliminates the need to add liquid to the bath during the etching process to maintain the liquid level.

Figure 3.7 KOH etching setup

The hot KOH etching rate is determined by two main factors: etching temperature and KOH concentration. It is intuitive to understand the effect of temperature: higher temperature results in a higher etching rate. The effect of KOH concentration is counterintuitive: lower KOH concentration increases the etching rate in a specific KOH concentration range [48]. However, there is a trade-off between the concentration of KOH solution and the etching temperature for etching rate. KOH solution with a lower concentration has a lower boiling point. During the hot KOH etching, it is dangerous to have the solution boiling since the KOH is a strong base. It is necessary to leave a safety margin between the KOH solution boiling point and the etching temperature. Therefore, it is essential to choose an optimal spot that compromises etching temperature and KOH concentration. For hot KOH etching, 80 ℃ and 30% (w/w) are the common standard as the etching temperature and the concentration of the solution respectively [28]. Constant etching rate requires constant etching temperature and constant KOH concentration. A

repeatable recipe is very important for the quality control of membrane fabrication. Controlling variables is essential for a repeatable recipe. The etching temperature is kept as a constant by the oil bath. It is not easy to control the concentration of KOH solution since heating a solution can cause faster evaporation. There are two main techniques helping in keeping the concentration steady. Firstly, more solvent (DI water in this case) can be added during the process to reach back to the original concentration. Secondly, it is possible to prevent any evaporation using a reflux condenser (a concave lid) (see Figure 3.8). For the first method, it is difficult to measure the exact amount of solvent evaporated. Another problem is to keep the etching temperature unchanged at the same time. Even by adding solvent at the same temperature as the solution, the temperature of the final mixed solution will change due to the exothermic nature of the dilution process. Therefore, it is unpractical to keep a constant etching environment by adding solvent. A reflux condenser can form a closed solvent circulation for a stable etching environment. However, it is difficult to measure the etching temperature since there is no opening to place a temperature measurement device into the KOH solution. Any opening can result in solvent vapor leaking. However, there is an indirect way to measure the etching temperature. When the oil bath heating system is in equilibrium, the oil temperature and the etching temperature will remain constant over time. After multiple trials, it is possible to find the correct oil temperature corresponding to the desired etching temperature. Therefore, a steady etching environment can be formed with a reflux condenser and temperature probe in oil.

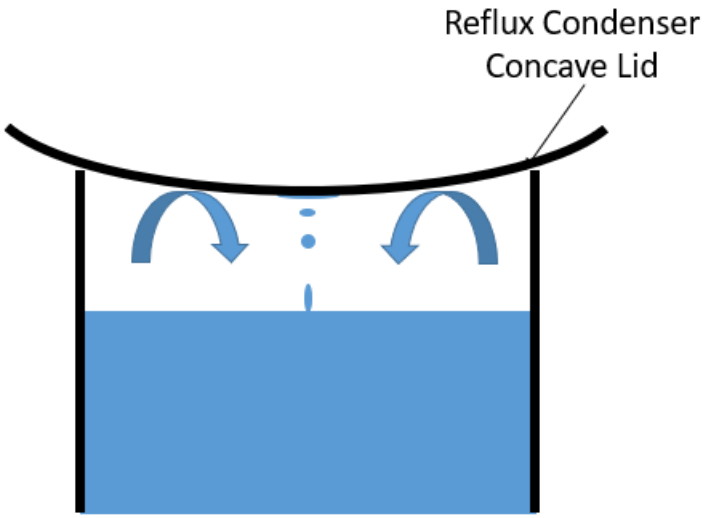

Figure 3.8 Reflux Condenser for Hot KOH Etching

The chemical reaction between Si and KOH shown in Eqn 3.2 generates a large number of bubbles (Hydrogen H_2):

$$Si + 2OH^- + 2H_2O + 2K^+ \rightarrow Si(OH)_4 + H_2(g) + 2K^+ \quad (3.2)$$

Due to the buoyancy force, H_2 bubbles will float to the surface. As shown in (see Figure 3.9.a), the device side SiN film faces upward. As a result, H_2 bubbles can be trapped under the SiN film and the rest Si frame. As the etching process keeps generating H_2 bubbles, the buoyancy force will be large enough to lift the wafer and cause continuous unstable movement for the wafer. There is another extreme case in Figure 3.9b. If the etching of the Si frame is almost finished, the H_2 bubble under the SiN film will float upward and break the SiN film. This is a catastrophic issue for SiN membrane fabrication. The correct wafer placement in hot KOH etching lets the device side SiN film face down and lets the H_2 bubble float up to the surface freely (see Figure 3.9.c).

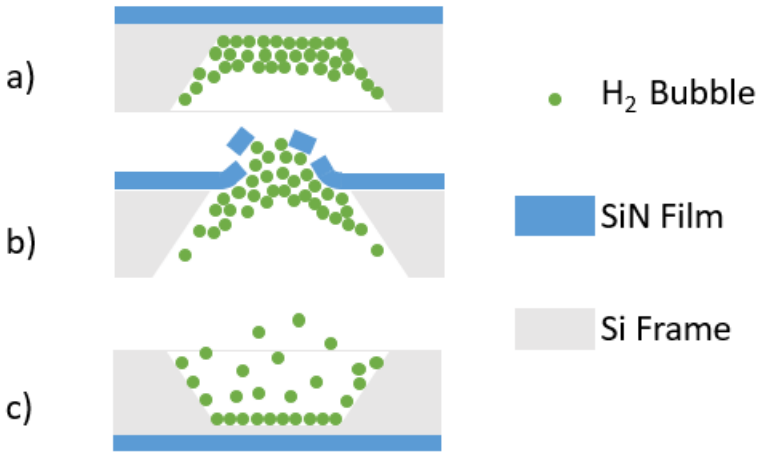

Figure 3.9: a) H_2 Bubbles Trapping Under the SiN Film When the SiN Film Facing Up; b) Broken SiN Film Due to a Large Amount of H_2 Bubbles Trapped under the SiN Film; c) H_2 Bubbles Floating When the SiN Film Facing Down

3.1.2.8 Cleaning and Storage

Before packing membrane chips in sample boxes, cleaning membrane chips is crucial. It is similar to the PR removal step. The differences are applying second time DI water rinse and using an N_2 gas gun blowing dry after rinse.

Since the final product is high mechanical Q-factor SiN membranes, it is important to make sure that nothing is stuck on membranes that can prevent Q-factor degradation. The contamination can be classified into two types (organic and inorganic). Applying acetone and IPA rinses is to make sure no organic contamination on membranes. Two times DI water rinses can minimize the residual left from acetone and IPA rinses. The DI water can also rinse off some inorganic contaminations: silicon dust from the Si frame, SiN shards from the SiN film, and KOH solution.

After the rinse process, membrane chips need to be blown dry. Letting membranes air-dry takes

much longer time and it is also easy to catch some contamination over time. In the lab, there are usually two types of gas guns (the air gun and the N_2 gun). The air-gun is commonly supplied by the air compressor. Although there are some filters in the pipeline, it is still possible that it contains some atomized oil from operating the air compressor and moisture from the air itself. Compressed air guns should therefore never be used. However, the N_2 spray gun is more suitable for the task since it is cleaner and drier than the air. The N_2 spray gun is a standard configuration for cleanroom use. In order to dry membranes without breaking them, it is essential to control the N_2 gas flow rate manually and blow N_2 gas flow parallel to the membrane from the top to the bottom of the chip (see Figure 3.10). The N_2 spray gun has a relatively large follow rate range. To dry membrane chips, it does not need to be fully functioning. Only a tiny portion of its capacity is needed.

Figure 3.10 Blowing Method for Drying Membranes with N_2 Gun

3.1.3 Photomask Design

In order to control the geometry of final membrane products, it is essential to be precise on every fabrication step. It is also important to have accurate geometry on the photomask since the photolithography is the first process to define membrane geometry. Photomask design is the

cornerstone of actual membrane fabrication.

During photomask design, it is necessary to predict and understand feature size changes during exposure, RIE etching and hot KOH etching processes. Since we hope to fabricate membranes of relatively large sizes (in the millimeter range), it is acceptable to have geometry errors in several micrometers. In contrast, a process that would target the fabrication of features on the order of 1 μm would be critically affected by the same variation. Therefore, the common error from exposure and RIE etching can be neglected in our case. The primary geometry change in the membrane fabrication is from the hot KOH etching step. As mentioned previously, a 54.7˚ angle will form to the Si frame during the hot KOH etching process [30]. According to the Pythagorean theorem, the shrunk size from the opening window on the SiN film unpolished side to the actual membrane on the SiN film device side can be calculated with the 54.7˚ angle and the 500 µm Si frame thickness (see Figure 3.11). Therefore, based on desired membrane sizes, the opening windows have to be 0.708 mm longer on each side. For example, if the demand size of the membrane is 1 mm by 1 mm, the corresponding opening window should be 1.708 mm by 1.708 mm. There is a 354 µm horizontal distance between the edge of the opening window and the edge of the membrane.

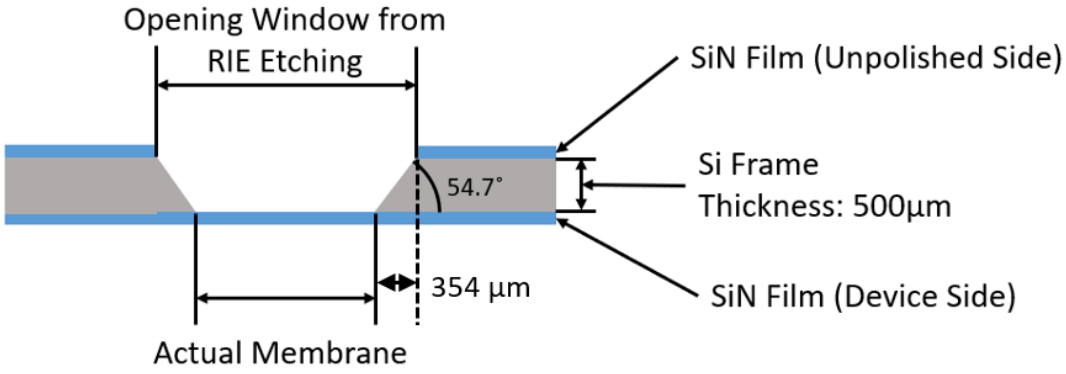

Figure 3.11 Schematic of SiN Membrane Chip

According to the result in [11], membrane thermal coupling can be radiation-dominated when the square shape SiN membrane has a length of more than 3 mm, with 100 nm thickness. In order to compare this result with data, it is necessary to have some membranes with different side lengths. Therefore, membrane side lengths of 1.5 mm, 3 mm and 6 mm membranes are planned to fabricate. We will also attempt to fabricate 12 mm by 12 mm SiN membranes, which can push the membrane thermal coupling towards a fully radiation-dominated further. This size is larger than most SiN membranes in the commercial market, and therefore will be challenging to fabricate. Besides the thermal radiation sensing project, another preliminary accelerometer project from our lab also needs some smaller size membranes with some materials deposition by 3D printing. Therefore, square shape membranes with 1 mm side length are suitable for this project. Since these membranes are used for testing the possibility of depositing materials with 3D printing, they do not have to be on individual chips. These membranes are planned to be fabricated as an array on each membrane chip (see Figure 3.13).

The second goal of this thesis is to develop a fully integrated actuation system on SiN membranes with a selective metallization method and electrostatics actuation method. In order to provide electricity to the metal, some pad features are required to be deposited on the frame of the membrane chip. These pads can be used to connect wires by wire bonding. Metal pads should be away from the membrane. Charged metal pads can generate electrical fields which can disturb the performance of the electrostatic actuation system. Most commercial square shape SiN membranes are located at the center of the membrane chip. In our case, since metal pads are needed, the membrane should be off centered (see Figure 3.12). As shown in Figure 3.12, the green area is

going to be etched off from the unpolished SiN film during the RIE etching. There are two small squares symmetrically located aside of the membrane. These two squares are used for alignment during metal deposition. The side length of these small squares is 0.9 mm. Based on the previous hot KOH etching calculation, at the end of fabrication, membrane windows from these squares will have about 0.19 mm as the side length. With the location of these two small membranes, the following metal deposition can be precisely aligned onto the membrane chip.

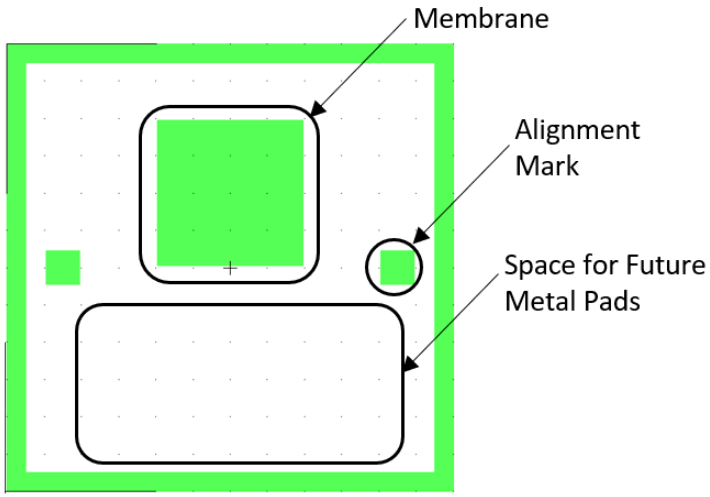

Figure 3.12 3mm x 3mm Membrane Chip Design on Photomask

As shown in Figure 3.13, eleven 1 mm x 1 mm membranes are in the same chip area. The reason to leave blank area in the four corners is that hot KOH etching will etch off all outer corners of the membrane chip. In addition, the final shape of these corners will be rounded after hot KOH etching. Therefore, the membrane located at the corner will not survive eventually.

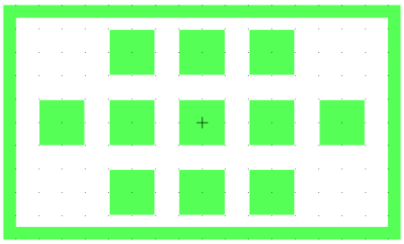

Figure 3.13 1 mm × 1 mm Membrane Array Chip Design on Photomask

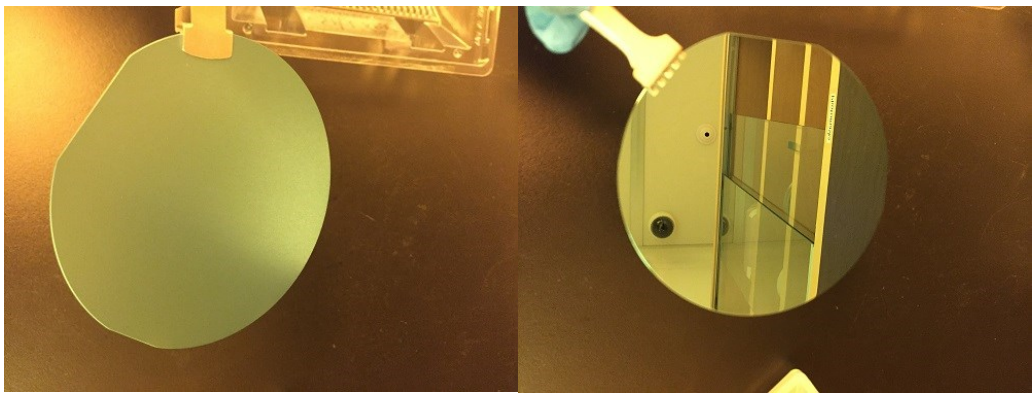

Figure 3.14 Unpolished Side and Device Side of the 4-inch LPCVD SiN Coated Single Side Polished (100) Single-crystal Si Wafer

The wafer used for fabrication is a 4-inch (100 mm) LPCVD SiN coated single side polished (100) single-crystal Si wafer (see Figure 3.14). The wafer is not in a perfect circular shape but has two flat edges. These edges allow us to align the photomask with the silicon crystal structure orientation. Every membranes' side should be parallel to flat edges in order to have the final membrane chip fabricated as expected in the design stage. The long rectangular shape polygons at the bottom of Figure 3.15 are used for mask alignment in photolithography. The photomask is aligned with the crystal structure when one of rectangular polygons is parallel to the flat bottom edge of the wafer.

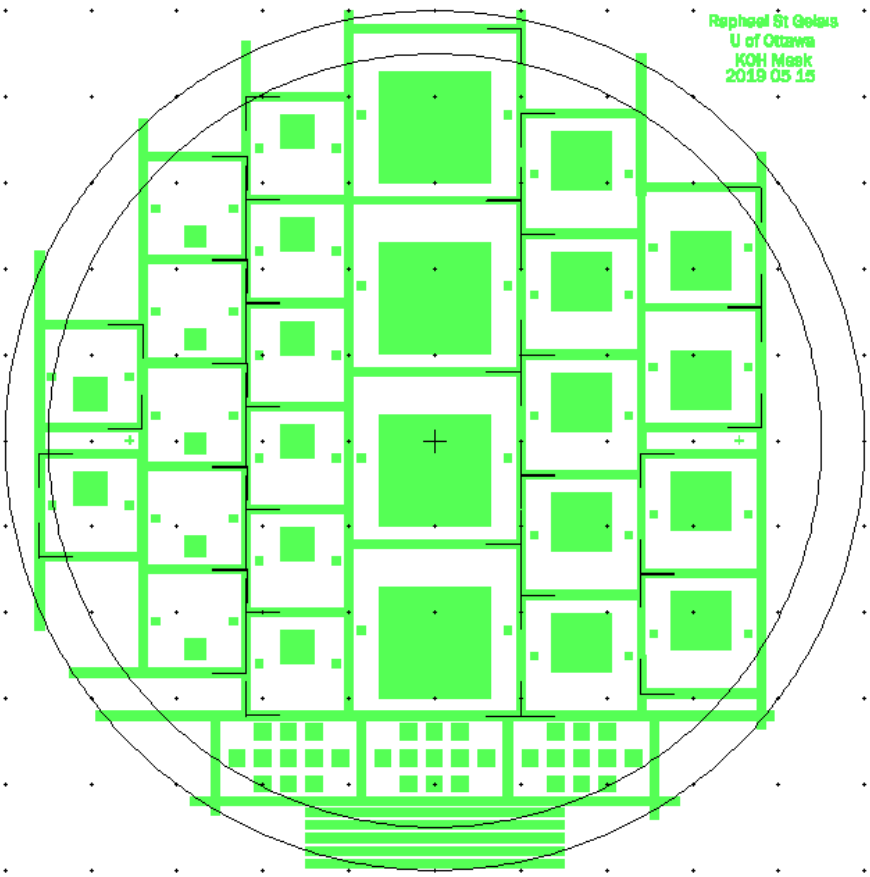

Figure 3.15 Photomask design

The SiN film on the wafer is by the LPCVD method. It is possible to have nonuniform SiN film thickness near to the wafer edge. Therefore, it is better to avoid fabricating membranes in the area near the edge of the wafer. In Figure 3.15, The outer circle defines the actual size of the wafer. The 5 mm gap between the two circles is the safety margin decided by us. Every membrane is located inside the inner circle.

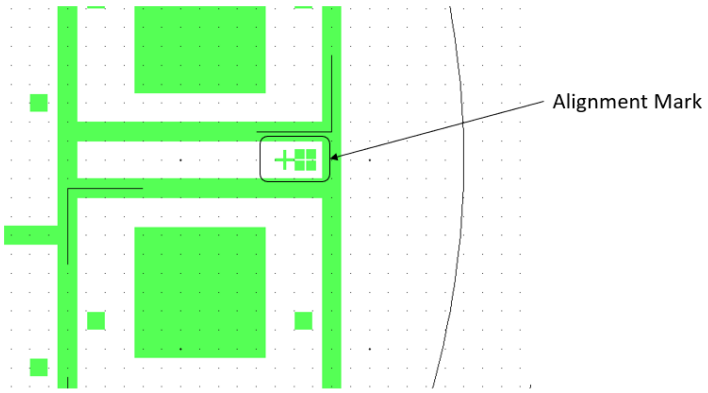

Figure 3.16 Alignment Mark

The Figure 3.16 shows the alignment mark for the pattern on the photomask. Each alignment mark is 35.1 mm away from the center point and located on the same horizontal line with the center point. In this thesis, there is only one PR layer formed on the wafer. In the future, these alignment marks can be used to form more PR layers and more complicated features with other photomasks as long as every photomask has the same alignment mark at the same location. The two small squares are alignment marks as well. They are designed for possible single chip alignment with photomask or shadow mask in the future.

In Figure 3.15, there are 0.9 mm wide lines separating each membrane chip. They are parting lines to let chips automatically separate from each other after hot KOH etching. Chip parting by either bending or cutting can cause unpredictable results. The force to bend the wafer can result in vibration to break membranes. The silicon dust can be created by the cutting process which means contamination for membranes. In order to have chips automatically separated after hot KOH etching, the 500 μm Si frame has to be etched completely. From the previous hot KOH etching calculation, a 0.708 mm gap is enough to meet the requirement. However, the 54.7 angle is just the ideal etching angle. It is always possible to have deviations. Thus, the parting gap between

each chip is set as 0.9 mm to guarantee automatic chip separation after hot KOH etching.

3.1.4 Final Optimized Recipe

The SiN membrane fabrication recipe is developed from the nanofabrication facility in the Center for Research in Photonics of the University of Ottawa and Prof. Michel Godin's Laboratory. Since the PR is extremely sensitive to UV light, several processes (i.e., spin coating, soft bake, photolithograph and developing) have to be done in the ARC 333A room, a yellow cleanroom, to avoid any UV light. The RIE etching uses the SAMCO RIE-10NR etcher in the ARC 333B room. The PR removal, hot KOH etching and final cleaning processes are done in the fume hood of Prof. Godin's Lab which locates in STM481. The detailed membrane fabrication recipe is shown below.

Reasons for these protocol choices can be found in the Problem encountered section (3.2.3).

List of chemicals needed:

Photo Resist: S1811

Developer: MF-321

Deionized water

Acetone

IPA

KOH salt

Safety precautions:

1. Wear gloves during photolithography.
2. Do not look at the UV light lamp from the mask aligner.

3. Do not look at the purple plasma flame without proper eye protection during RIE.
4. Wear gloves during acetone and IPA handling.
5. Wear heavy-duty gloves, coverall suits and proper face covering during KOH handling
6. Do not do microfabrication alone. Always use a buddy system.

I. Spin Coating

a) Procedure outline

i. Spin coater (see Figure 3.17): Laurell Spin Processor - WS-650-23 (ARC 333A)

Figure 3.17 Spin Coater.

ii. Photo Resist: S1811 (we use an expired bottle from the CRPUO cleanroom, but it is not a problem apparently. Pour a little portion in one small glass sample bottle which is in the CRPUO general use cabinet.) Theoretical Thickness: 1.2 μm / 3000 RPM 1.5 μm / 2000 RPM from Figure 3.18.

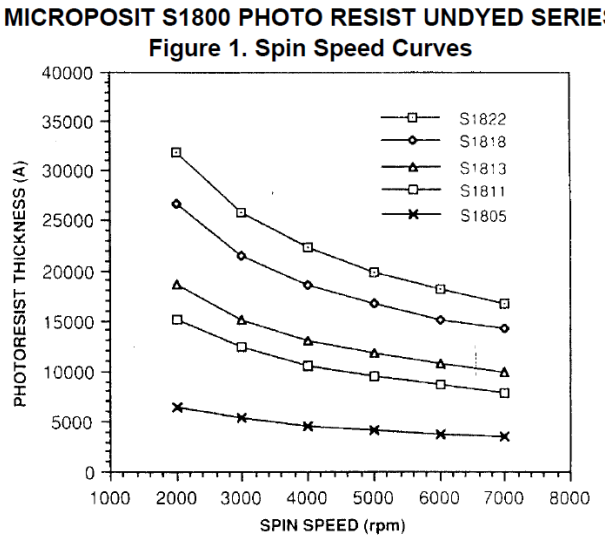

Figure 3.18 S1800 series photoresist spin speed curve

We use a low speed (2000RPM) to effectively cover the asperities on the rough side of the wafer.

iii. Pre-program the spin coater

1. First Stage: 20[s]; acceleration: 100[RPM/s]; speed: 0=>2000[RPM]
2. Second Stage: 60[s]/ acceleration: 2[RPM/s]; speed: 2000=>2000[RPM]
3. Third Stage: 20[s]/ acceleration: 100[RPM/s]; speed: 2000=>0[RPM]

b) Detail procedure

i. Open the 3 valves: N2, CDA & Vacuum

ii. Turn the power on.

iii. Choose recipe #18, click [run program] to enter and adjust the program. Do not trust that the program parameters have not changed.

iv. Open the lid and place the suitable wafer holder. For a 4-inch wafer, the 2-inch wafer holder is suitable. The wafer holder should be smaller than your wafer.

v. Place the wafer onto the center of the holder and press the vacuum button to fix the

wafer on the holder. Pressing the vacuum button again can release the wafer. On the control panel, 00~01 (around zero) means no vacuum between the wafer and the holder; 18~20 means the wafer is stuck to the holder due to vacuum.

vi. Use a pipette to put the PR on the wafer. Squeeze out the air from the top air pocket of the pipette. Insert the pipette into the PR sample bottle and release the pressure on the air pocket to let the PR be sucked into the pipette. Spin the wafer manually by touching the edge only with your finger. While the wafer spins, gradually drop the PR onto the wafer as evenly as possible. You do not need to use PR drops to cover the whole wafer. That would be too much for spin coating. Use the dropper as a butter knife to spread the PR all over the wafer but do not touch the wafer except the edge. Use the dropper to blow all bubbles away from the wafer. There are detailed operating drawings in the next subchapter.

vii. Close the lid and press start if it shows ready on the screen.

viii. After the spin coating is done, open the lid carefully. During the spinning, the exceeded PR left on the spin coater's lid could drop onto the wafer and ruin the work. Press the vacuum button to release the wafer and transfer the wafer to the hotplate for soft bake.

ix. Spin coat on smooth side (see Figure 3.19) first to protect the device side SiN film for future membrane.

x. Spin coat on the rough side (see Figure 3.20) for photolithography.

c) Spin coating examples

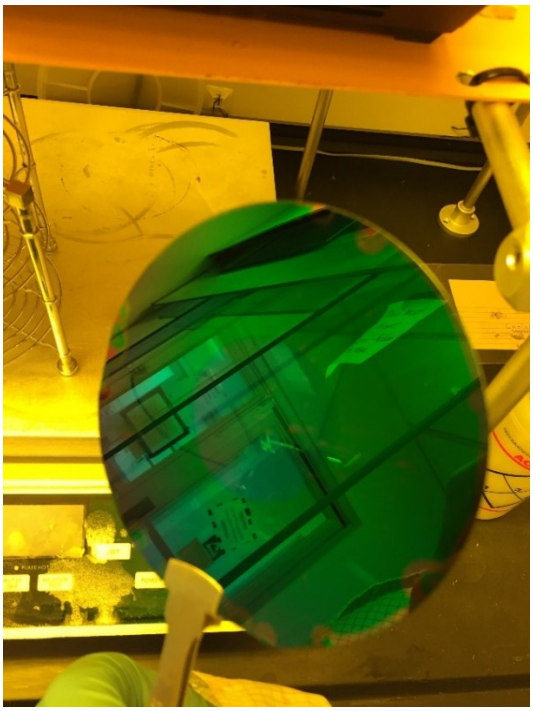

Figure 3.19 Smooth Side of the wafer with PR coated.

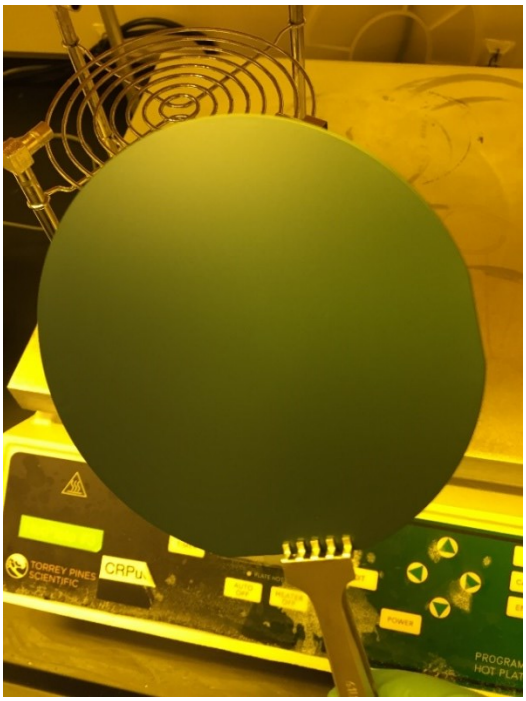

Figure 3.20 Rough side of the wafer with PR coated.

d) Cleaning after use:

i. Find the bottle labeled “General Use Acetone”.

ii. Find the used cleanroom tissue.

iii. Use them to clean the PR residual left on the spin coater’s inside surface.

II. Soft Bake

a) General requirements

i. Temperature: 115 ℃

ii. Time: 1min

iii. Cooling

b) Detailed procedure

i. Set 1min Alarm

ii. Set 115 ℃ for the hot plate. Wait 5 mins for the hot plate to become uniform.

Prepare the hotplate before spin coating.

iii. Soft bake the wafer and start the alarm.

iv. Once the alarm is ringing, transfer the hot wafer to the cooling shelf to cool down.

III. Photolithography

a) General requirements

i. Mask aligner: OAI Model 204IR (ARC 333A)

ii. Input Power: 23 mW (without any light filter)

iii. Time: 10 s (Over-exposed. We do not have any small size feature.)

iv. Wafer Side: Rough Side

v. Photo Mask: Chrome coated side contacts the wafer. Glass side faces up.

vi. Contact Type: Hard Contact

b) Detailed procedure

i. Follow the instruction sheet under the mask aligner.

ii. Warm up the lamp before the spin coating process.

iii. Place the photomask top side towards you for easy access.

iv. Chrome coated side is darker than the glass side. The chrome coated side must be in contact with the wafer.

v. Use acetone to clean the photomask before and after the exposure.

IV. Wet Developing

a) General requirements

i. Developer: MF-321 (Bottom left cabinet under the spin coater)

ii. Method: Immersion

iii. Time: 1min

iv. Rinse: DI water

b) Detailed procedure

i. Prepare two glass beakers wide enough for the 4-inch wafer.

ii. Set 1 min alarm.

iii. Pour proper amount of the developer. 5 mm to 10 mm height of developer in the beaker is enough for immersion developing. Prepare a half full beaker with DI water

iv. Place the wafer from the cooling shelf into the developer solution and start the alarm.

v. Once the alarm is ringing, take out the wafer and place it into DI water for rinsing.

vi. Take out the wafer and use N_2 gun to blow all water away from the wafer.

vii. Place the dry wafer (see Figure 3.21) in the sample box and proceed to RIE etching.

viii. Example:

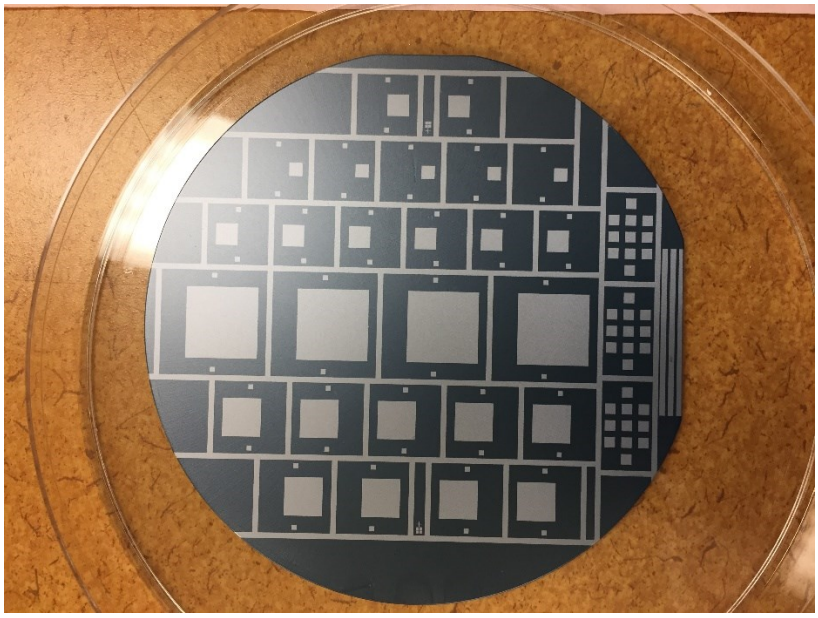

Figure 3.21 Wafer after developing (silicon wafer in a test trial, no SiN coating)

ix. Dump all liquid wastes in the organic waste bottle.

V. RIE Etching

a) General requirements

i. Etcher: SAMCO RIE-10N (ARC 333B)

ii. Parameter Setting (Pre-programming):

1. CF_4: 25 sccm
2. O_2: 5 sccm
3. Power:100 W
4. Pressure: 8 Pa
5. Time: 1 min

iii. Time (in total): 2 min

b) Detailed procedure

i. Open valves.

1. O_2
2. CF_2
3. N_2

ii. Turn on the chiller (ARC330 mechanical room).

iii. Set up etching parameters on the etcher.

iv. Test run the etcher without the wafer.

v. Take a picture of the wafer under microscope. Compare with Figure 3.22.

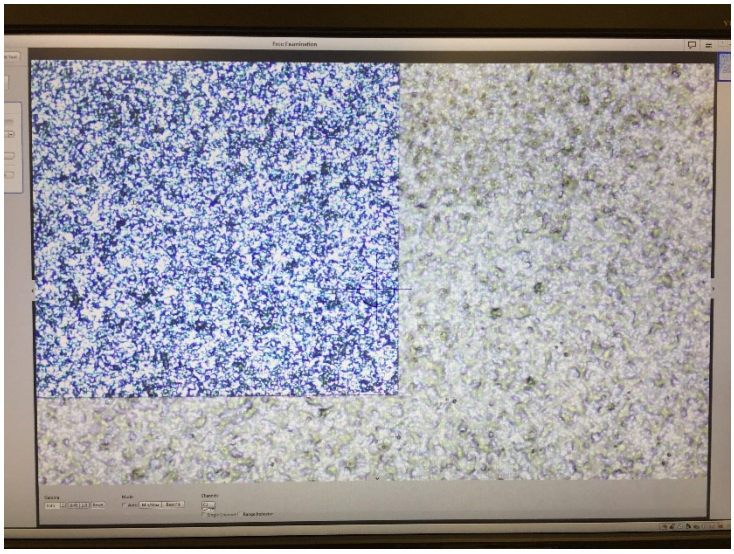

Figure 3.22 Picture taken before RIE etching under the microscope.

vi. Insert wafer into the etcher and start etching. Let the unpolished side face upward.

vii. Take out the wafer and take a picture under microscope. Compare the picture of the wafer appearance with Figure 3.23 and Figure 3.24.

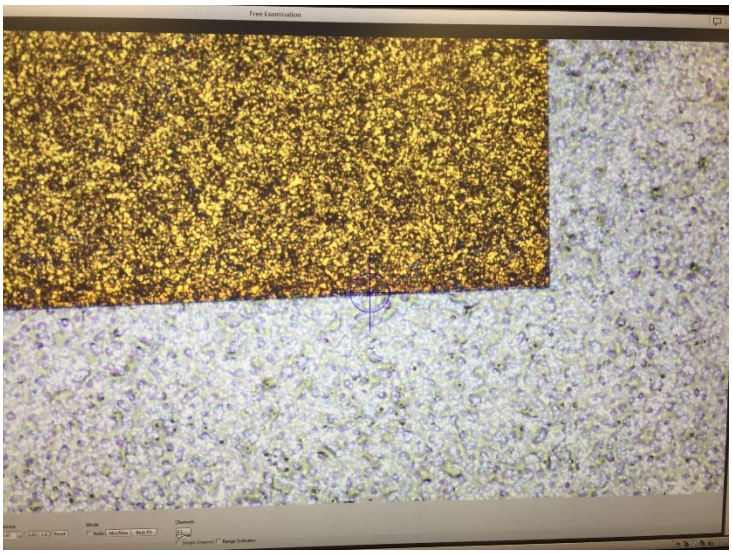

Figure 3.23 Picture taken after 1 min RIE etching under the microscope.

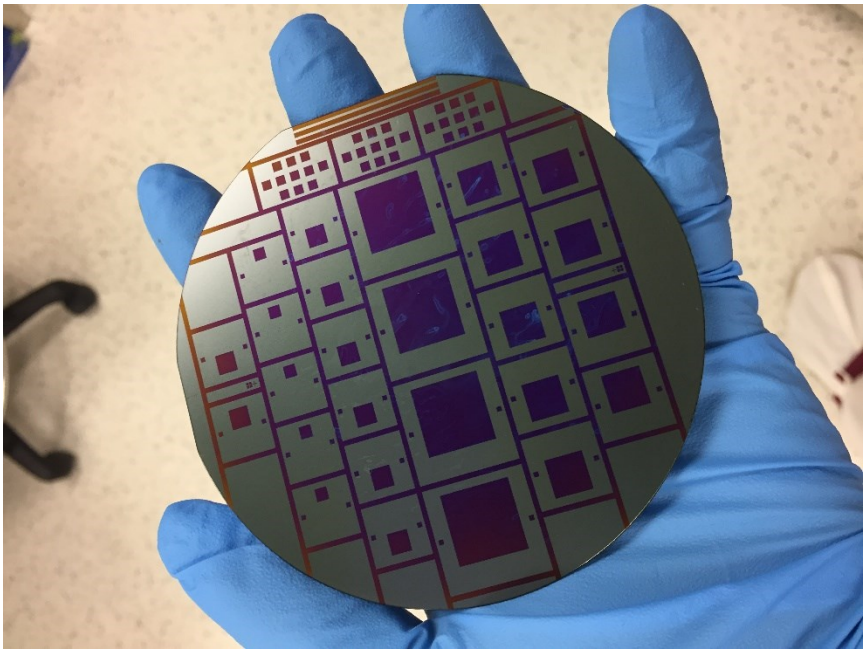

Figure 3.24 Wafer appearance after 1 min RIE etching.

viii. Put the wafer back to the etcher and start the second time RIE etching. Let the unpolished side face upward.

ix. Take out the wafer and take a picture under microscope. Compare the picture of the wafer appearance with Figure 3.25 and Figure 3.26.

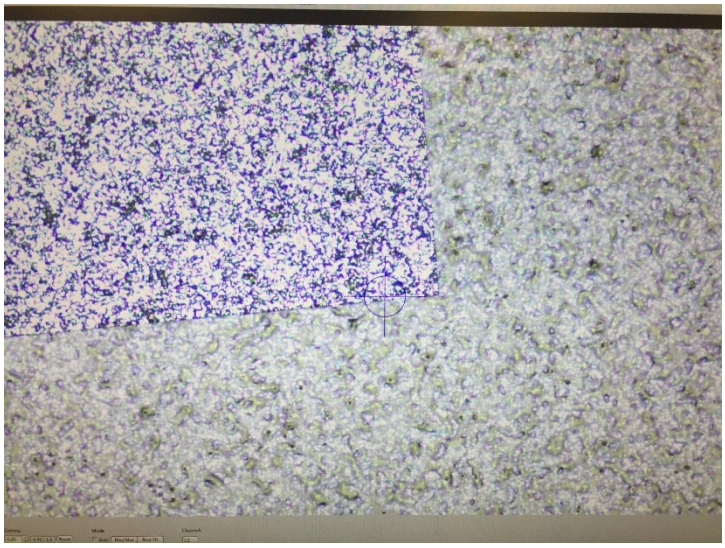

Figure 3.25 Picture taken after 2 mins RIE etching under the microscope.

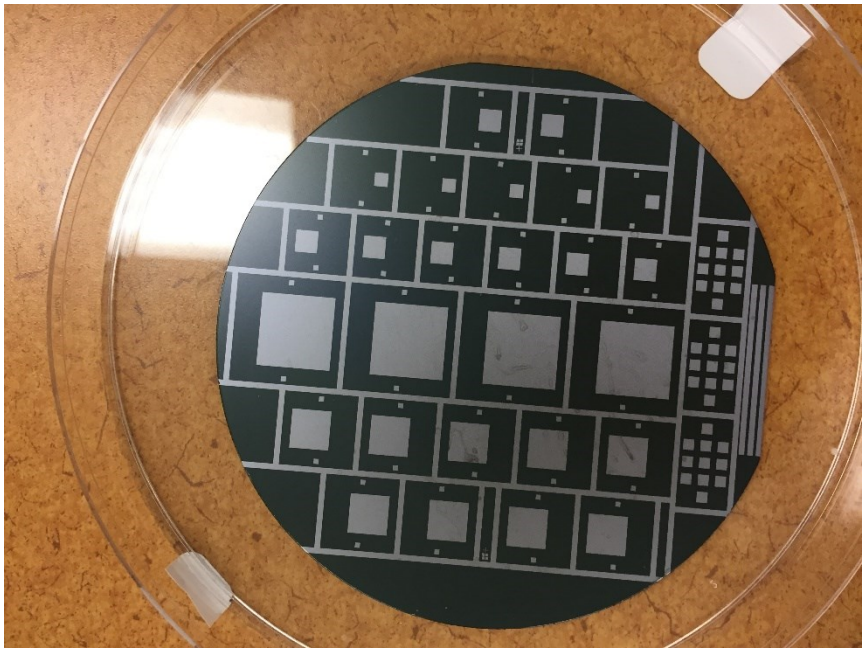

Figure 3.26 Wafer appearance after 2 mins RIE etching.

x. Store the wafer in the sample box. Do not remove the PR if the wafer is not going into the hot KOH etching right away.

VI. PR Removal

a) General requirements:

i. Three glass beakers (larger than 4-inch)

ii. Acetone

iii. IPA

iv. DI water

b) Detail procedure

i. Pour proper amount of acetone, IPA and DI water into three different glass beakers.

ii. Rinse the wafer with acetone, IPA and DI water in order.

iii. Dump all liquid wastes into the organic waste bottle.

VII. Hot KOH Etching

a) General requirements

i. Fume hood (Prof. Godin's Lab, STEM 481)

ii. Cooking hot plate

iii. Lab hot plate

iv. Glass beaker

v. Magnetic stirrers

vi. Stainless steel pot

vii. Concave glass lid

viii. Corn oil

ix. DI water: 280 ml

x. KOH salt: 120 g

xi. Hot KOH etching Teflon equipment (see Figure 3.27).

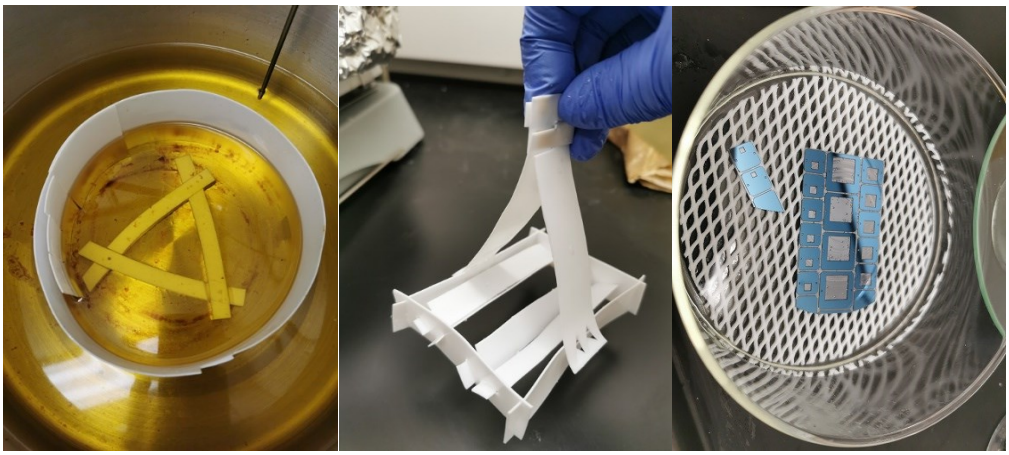

Figure 3.27 Teflon holder, spacer; rack, rack lifter; mesh.

b) Detail procedure

i. Heat up the oil in the stainless steel pot on the cooking hot plate with maximum power. Place the Teflon glass holder into the oil. Connect the temperature probe with the lab hot plate.

ii. Prepare 280 ml DI water in the glass beaker. Do not use hot DI water. Place the larger magnetic stirrer into the beaker. Put the beaker onto the lab hot plate and start the stirring function with 150 RPM stirring speed.

iii. Measure 120 g KOH salt and gradually put it into DI water for mixing.

iv. Prepare the Teflon etching setup #1(put beaker in the holder and cover the lid)

v. Slowly place the glass beaker which contains KOH solution with a small angle into the oil bath. The small immersion angle can prevent air trapped under the glass beaker.

vi. Turn off the cooking hot plate and place the stainless steel pot onto the lab hot plate.

vii. Turn on the heat of the lab hot plate and set 100 ℃. Place the temperature probe into the oil with at least 5 mm depth. Do not let the probe touch the pot or glass beaker.

viii. Place the glass lid on the top of the glass beaker.

ix. When the oil temperature is over 84 ℃, change the set-up temperature to 85 ℃ and place the wafer into the hot KOH solution. The patterned side has to be facing upward.

x. Start 2 hours etching.

xi. Prepare a half-full glass beaker with DI water.

xii. Take out the wafer with gloves on. Separate wafer into strips for same size membranes by bending the wafer along the parting lines (see Figure 3.28).

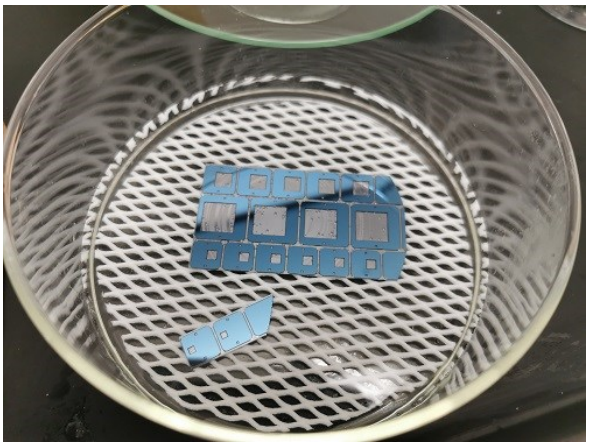

Figure 3.28 Separate the wafer into strips.

xiii. Prepare the Teflon etching setup #2: Preserve wafer strips into the DI water glass beaker. Put small size wafer strips (except for 12mm membrane chips) on the Teflon rack (see Figure 3.29).

Figure 3.29 Membrane chip strips on Teflon rack.

xiv. Prepare a half-full glass beaker with clean DI water.

xv. Start etching for about 2 hours. If no more H_2 bubbles are generated from the membrane area, the etching process is done. The etching time may vary a bit every time.

xvi. Use tweezers to take out membrane chips carefully. Carefully place chips into the DI water with the membrane side up.

xvii. Etch the rest small wafer strips and repeat step (xiv)-(xvi).

xviii. For etching large, delicate membranes (i.e., 12 mm ones), change the setup temperature to 65 ℃ on the lab hot plate. Wait for it until the oil temperature reaches 65 ℃ and stabilizes.

xix. Put large wafer strips (12mm membrane chips) on the Teflon rack and repeat step (xiv)-(xvi). The etching time is around 4 hours.

xx. Turn off the lab hot plate.

xxi. The KOH solution waste should be dumped into the 20L waste container with KOH waste labeled.

VIII. Final Cleaning

a) General requirements

i. Glass beakers

ii. Petri dishes

iii. DI water

iv. Acetone

v. IPA

vi. N_2 Gun

b) Detail procedure

i. Prepare two glass beakers with DI water, one petri dish acetone and one petri dish with IPA.

ii. Rinse membrane chips with two times of DI water, one time acetone and one time IPA in order.

iii. Use N_2 gun to dry membrane chips.

iv. Used acetone and IPA wastes should be dumped into the organic waste bottle.

3.1.5 Discussion on Problems Encountered and Developed Solutions

In this section, several problems and adjustments, during the membrane fabrication process developing, will be discussed.

3.1.5.1 PR Excess for Spin Coating

Issue:

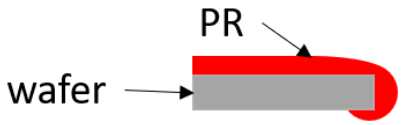

Figure 3.30 The Excess PR Went to the Back Side of the Wafer

During the spin coating process, the PR went to the back of the wafer from the polished side to the unpolished one and formed several spots onto the edge of the back surface, the unpolished side (see Figure 3.30). This could lead to uneven surface coating when the PR is applied to the unpolished side of the wafer.

Reason:

The PR was gradually added onto the wafer until the wafer was fully covered by the PR without any blank spot. This amount of PR is too much for spinning coating. As the wafer spins, due to the surface tension of the PR and the centrifugal force, the PR will be automatically spread out to cover the whole wafer surface. It is not necessary to fully cover the wafer with PR droplets from the pipette before the spin coating process.

Solution:

Although, it is not recommended to use PR droplets to cover the wafer. It is still better to have a very thin PR covering the wafer. With the limited amount of PR solution, it is possible to spread the PR to fully cover the wafer with a pipette. The following are the detailed steps.

Use the pipette to put the PR droplets onto the wafer like the way shown in Figure 3.31.

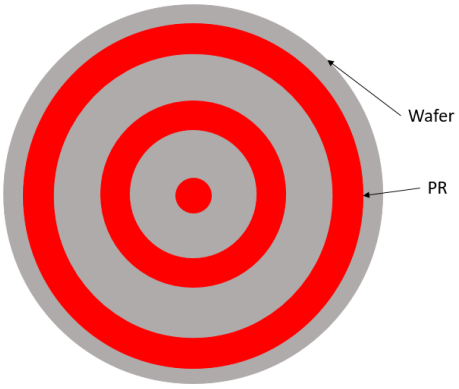

Figure 3.31 Schematic for Adding PR on the Wafer (Top View)

Then, use the pipette to spread the PR all over the wafer (see Figure 3.32).

Figure 3.32 Schematic for Spreading PR to Fully Cover the Wafer (Side View)

Attach the pipette onto the wafer like the way shown above and spin the wafer holder manually.

Result:

Fewer PR spots with smaller sizes left to the back of the wafer.

3.1.5.2 PR Layer Thickness Lacking

Issue:

The whole wafer got etched during the hot KOH etching. In the end, there is nothing left

Reason

For hot KOH etching, the selectivity ratio between Si and SiN is huge. Based on this ratio, theoretically, the Si frame is supposed to be removed selectively and SiN film is supposed to be

isolated in the designed area. However, during the hot KOH etching, the KOH solution attacks the whole wafer. The device side SiN film remained when there was still Si frame left. The unpolished side SiN film is all gone. Near the end of the etching process, the whole wafer became very thin. In the end, the whole wafer vanished.

Before the wafer proceeded to hot KOH etching, it was confirmed that there was still a SiN film left on the rough side of the wafer with the pattern from the photomask.

The superficial reason for this issue is that the SiN film on the rough side did not protect the Si frame underneath. However, as mentioned previously, the selectivity ratio should let the SiN film protect the Si frame underneath during the hot KOH etching. Therefore, the real cause is that the SiN film got attacked by RIE so that the SiN film is too thin to protect the Si frame. It is not optimal to increase the SiN film thickness since the desired SiN film thickness is 100 nm and SiN film thicknesses for both sides are the same due to the furnace coating process. The underlying reason for this issue is that the PR layer was too thin to protect the SiN film underneath and made the Si fame under the same area get exposed in the KOH solution.

The experimental trials before the actual fabrication used the 100 nm thickness SiN coated polished Si wafer. The operating side for actual fabrication is the unpolished surface. The reason why we did not use the rough side during experimental trials is that it is impossible to see the nanometer level depth difference made by RIE etching on the surface profile since the rough surface has about ± 2 μm uncertainty.

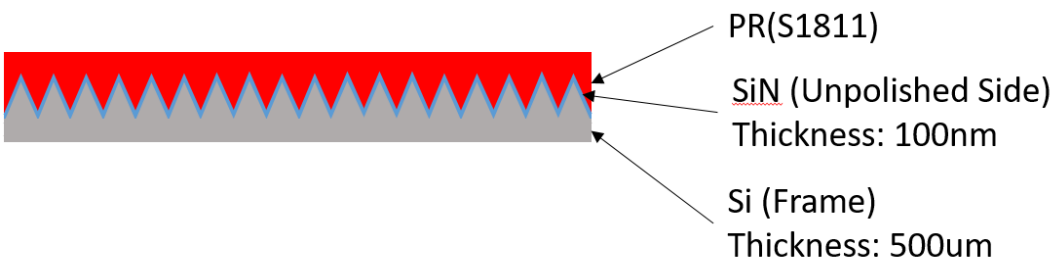

Figure 3.33 Unpolished Side of the Wafer Before RIE

From the Figure 3.33, the spikes can determine the rough surface profile. During the spin coating, the PR will try to fill those valleys which means thicker PR on valleys and thinner PR on peaks. Therefore, it is possible to have much thinner PR on peaks than those inspected from previous trials on the polished side surface. After RIE etching, the PR layer may not be able to protect the SiN film located at those peaks and result in the condition shown in Figure 3.34. It is also possible that the Si frame located at those peaks will be etched partially with a bit longer RIE etching time. Therefore, the top priority is to have the PR layer as thick as possible.

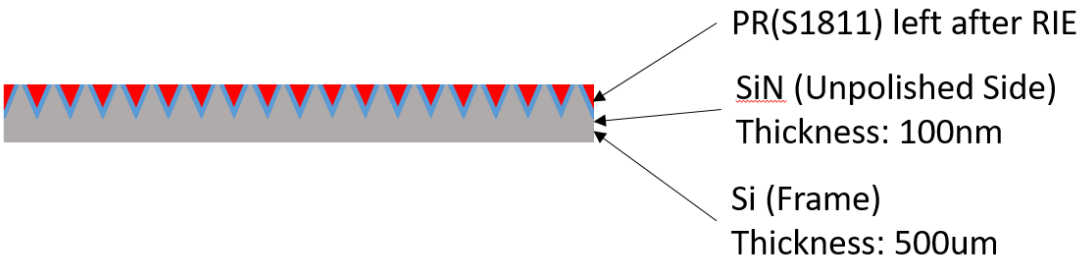

Figure 3.34 Unpolished Side of the Wafer After RIE

Solution

Previously, the SPR 955-CM grade 0.7 was used for PR with 3000 RPM spin coating speed. From the Figure 3.3, 3000 RPM can make 700 nm thickness PR coated onto the wafer. In order to increase the PR thickness, the S1813 PR was then used because it can make the PR layer thickness

in the micrometers range. Additionally, to maximize the thickness of the PR layer, the speed of spin coating was set as 2000 RPM (see Figure 3.18).

Reducing the RIE etching time is supposed to be a decent option to solve this problem. However, from several trials before the actual fabrication, the RIE etching rate on the SiN film is about 80~95nm per minute. The previous etching time was set as 40 seconds for two times which is 1 min and 20 seconds in total. This etching time is about just enough to remove SiN film based on previous trials. Therefore, the etching time remains the same, 40 seconds for two times.

Result

The hot KOH solution slowly starts to attack the exposed Si frame from the edge to the center of the wafer. The whole wafer will undoubtedly be etched by KOH solution normally after a while. However, the etching depth across the whole wafer will be different (i.e., the edge will have a deeper etching depth than the center part does) which is not desired. Fortunately, this phenomenon can confirm that the PR layer is thick enough to protect the SiN film underneath.

3.1.5.3 Lacking RIE Etching Time

Issue:

The KOH solution did not etch all exposed Si areas at the same time. The etching slowly started from the edge to the center of the wafer (see Figure 3.35).

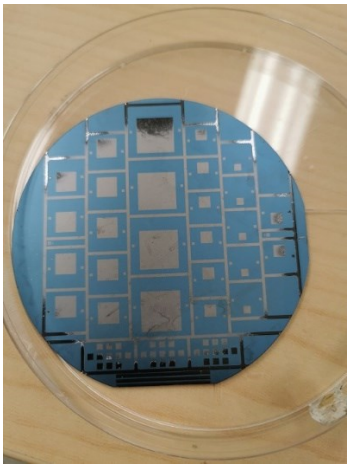

Figure 3.35 Wafer with insufficient RIE etching time duration.

Reason:

If the Si frame is exposed to the hot KOH solution, the etching process should start right away. At the beginning of the hot KOH etching process, the center part Si frame exposed area of the wafer did not show any sign of etching. The only material on the wafer that can stop the KOH etching is SiN. Therefore, the cause of this problem is that a very thin SiN film covers the Si frame in the area which is supposed to be exposed.

There are two possible causes for the phenomenon that the etching started from the edge to the center of the wafer. During the membrane fabrication processes, the edge of the wafer is the part that will most likely be worn. Thus, the SiN film on the edge was already worn out before the hot KOH etching. The corresponding Si frame underneath is then exposed to KOH solution. This can be one of two possible causes for this issue. Another hypothesis for this issue is that the plasma in the RIE chamber etches the edge more than the center part of the wafer. Either way, there is a thin PR layer left on the area that is supposed to have Si exposed.

Solution

From the photomask design, there is no membrane located at the edge of the wafer. Therefore, the wear issue of the wafer edge does not affect the membrane quality. Since it is highly possible that there is a very thin SiN film left in the area the Si frame is supposed to be exposed, removing this thin SiN film by adding more etching time in the RIE etching process is the most practical solution. The only concern is about the PR layer thickness. The PR layer needs to be thick enough to protect the SiN film underneath with increased etching time. For uneven RIE etching between the center and the edge, it can be neglected since the difference is under micrometer.

Eventually, based on the original RIE etching time, 40 seconds for two times, the new RIE etching time is then set as 1 minute for two times.

Result

In the hot KOH solution, every exposed Si frame area starts etching at the same time as the wafer is put into the solution.

3.1.5.4 Automatic Chip Separation Breaks Membranes

Issue

At the later period of hot KOH etching, all membrane chips were disconnected from each other before finishing the membrane isolation process. Membrane chips floated randomly and collided with each other. Most membranes were damaged by collision with other chips' edges. Lots of membrane products were lost in this way. There are only eight membranes survived on three 1mm side length membrane chips.

Reason

The H_2 bubbles generated by the chemical reaction of etching can stick on the membrane chip for a while and merge with each other to form bigger bubbles. Giant combined H_2 bubbles tend to float up to the solution surface due to the buoyancy force. During their random floating movements, bubbles can lift and push membrane chips in random directions. Therefore, chips are floating in the solution in random directions and eventually sink to the beaker bottom due to gravity. During these random movements, some collisions can happen between membranes and membrane chip edges. These collisions have a large chance of destroying membranes.

Solution:

The main point for solving this problem is to reduce collisions. It can be simply achieved by reducing the number of membrane chips in the etching. Therefore, the whole wafer can be divided into two parts with a diamond cleaver. Before the hot KOH etching, use the diamond cleaver to scratch repeatedly to make a clear mark along with the (100) crystal plane structure at the bottom of the wafer. Gently bending two sides of the wafer with gloves on hands can easily separate the wafer into two pieces. Etching about half of membrane chips can reduce the possibility of collisions during the hot KOH etching which means less broken membranes.

Result

Because the wafer is cleaved by half, all 12 mm side length membrane chips are destroyed. After membrane chips separated in the KOH etching, all useless chips were taken out to further minimize the collision possibility. Only membrane chips were left in the KOH solution for finishing membrane isolation. Eventually, most membranes survived after hot KOH etching. There are still

some membranes broken by the same issue. Among all membrane chips, 6 mm side length ones are more likely to be broken than those with smaller sizes. More space for each chip during the etching does improve the surviving rate of membranes. However, we still believe that there is room for improvement.

3.1.5.5 Hard to Pick Up Chips With a Tweezer from the KOH Solution

Issue

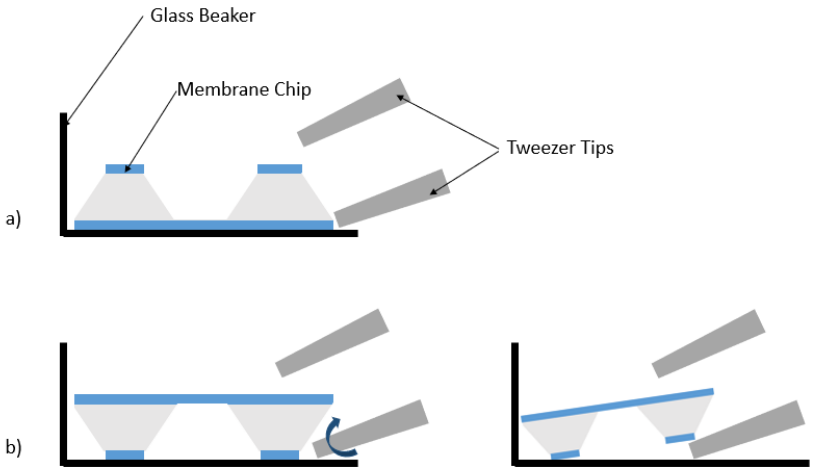

Figure 3.36 The Difficulty for Picking Up Membrane Chips from the Glass Beaker with a Tweezer. a) With Device Side Facing Down; b) With Device Side Facing Up

It is not practical to use bare hands to take out membrane chips from hot KOH solution, even with gloves on. Stainless steel made tweezer is the common tool to pick up membrane chips from the hot KOH solution. However, it is not easy to use because chips, the tweezer and the glass beaker all have glazed surfaces. It is hard to find a decent angle to use the tweezer to pick up membrane chips (see Figure 3.36.a). Additionally, any slight reckless movement can break membranes easily.

Reason

When the wafer is put into the KOH solution, the unpolished side with the pattern etched by RIE faces up. After the hot KOH etching, the membrane chip will have the device side facing the bottom of the glass beaker. It is hard to use a tweezer to pick chips up since there is not enough room between the chip and the beaker to allow the tweezer to go in and lift the chip. Once the chip is lifted up, the chip has to be flipped over (see Figure 3.36.b) for later easier manipulation. When the chip's device side is facing up, with the 54.7˚ etch angle, it will be much easier for the tweezer to pick the chip up. Therefore, it is important to have membrane chips flipped over from the KOH solution.

Solution:

Place a Teflon made mesh under the wafer can be a solution to this issue. The Teflon does not react with KOH solution. It will not interact with the etching process. It also has a larger density than the KOH solution which means it will sink down to the bottom and will not float (i.e., If its density is lower than the KOH solution, there is a big chance that the mesh can float to the solution surface with the wafer, and then the etching stops.). The mesh opening size needs to be big enough to allow the tweezer's tip to go in (see Figure 3.37). The mesh can make chips off-contact with the glass beaker. The tweezer can pick up chips in a much easier way.

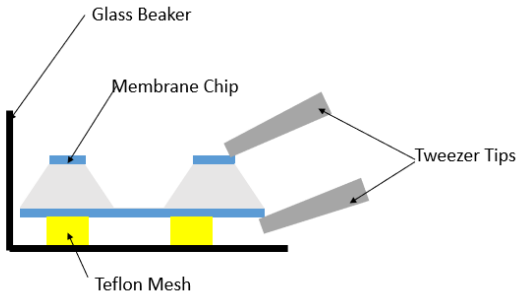

Figure 3.37 Membrane Chip Pick Up with a Tweezer on Teflon Mesh

Result:

The Teflon mesh does help a lot for picking up chips with the tweezer.

3.1.5.6 Mesh Traps Bubbles

Issue

The Teflon mesh floats to the water surface during the etching process. The wafer on the mesh is lifted out of the KOH solution which means the etching process is stopped. The mesh needs to be pushed down to the bottom manually for multiple times since the heat from the oil bath keeps vaporizing the KOH solution.

Reason

The mesh can trap many bubbles from the solution vaporization during the etching process. Due to the buoyancy force, these bubbles can stick to the mesh and make it float to the solution surface. Pushing down the mesh and separating bubbles from the mesh are palliative. In a couple of minutes, bubbles trapped on the mesh will be enough to float the mesh up again. The main reason is that the density difference between the Teflon and the KOH solution is not big enough to keep the mesh at the bottom of the beaker with trapped bubbles.

Solution:

The magnetic stirrers are made with metal cores inside and the Teflon shell outside. These stirrers can be placed on the top of the mesh as weights.

Result

All three stirrers are placed on the top of the mesh in the KOH solution. The mesh does not float up anymore.

3.1.5.7 Need to Save 12 mm Large Membranes

Issue

Cleaving the wafer by half can result in losing all 12 mm side length square membranes. Before the cleaving, during the hot KOH etching process, 12 mm side length square membranes got separated from the frame and floated up to the surface level with a thin Si layer left. This means that 12mm membranes get destroyed even before the finish of the hot KOH etching process. Whether cleave the wafer or not, 12mm membranes cannot survive from the hot KOH etching with certain conditions. We need to find a way to fabricate 12mm side length square membranes to collect more data in the other projects.

Reason

The 12mm membrane has the largest area comparing to other membranes. This can result in a violent chemical reaction. During the hot KOH etching, it is seen that the edge part of the membrane finishes SiN film isolation faster than the center part. At the very end of the SiN film isolation, there is always one or several Si spots left in the center part of the membrane. For 12 mm membranes, after the edge part is finished etching first, the clamp end of the membrane will become stress concentration spots since the center part with a thin Si layer covered can result in lower yield strength. With a relatively large buoyancy force from the H2 bubbles stuck on the membrane, the 12 mm membrane will start to break from the edge.

Solution:

The recipe for the hot KOH etching uses 80 ℃ as the temperature and 30% (w/w) for the KOH solution concentration. The main idea to make 12 mm membranes survive is to slow down the etch rate. From previous materials, lower temperature or higher concentration can decrease the etch rate for hot KOH etching. Comparing to changing the concentration, cooling down the etching temperature is relatively easier to achieve. Therefore, in order to fabricate 12 mm membranes, 65 ℃ is used for oil bath temperature, and the concentration of the KOH solution remains the same.

To avoid the membrane chips collision problem, the wafer can be half etched and divided into several parts to isolate 12 mm membrane chips. It is the same principle as cleaving the wafer. Patterns between each chip are cleaving lines. Except for 12 mm membrane chips, the rest of membrane chips can still use 80 ℃ as etch temperature to finish the rest of etching. For 12 mm membranes, use 65 ℃ for oil bath temperature.

Result

All 12mm membranes survived with 65 ℃ as the oil bath temperature. However, there are still some broken membranes due to membrane chip collisions.

3.1.5.8 Membrane Chips Collision Issue

Issue

Some membranes still are broken by membrane chip collision.

Reason

Bubbles formed from KOH solution vaporization can be trapped on the mesh and form the bigger

size of bubbles. These big bubbles can lift membrane chips during the elevation due to the buoyancy force. After the lift, membrane chips will tend to float horizontally in other directions. These movements can result in broken membranes. Even with fewer membrane chips for each time etching, there are always some membranes broke during the etching process, especially at the ending time period.

Solution:

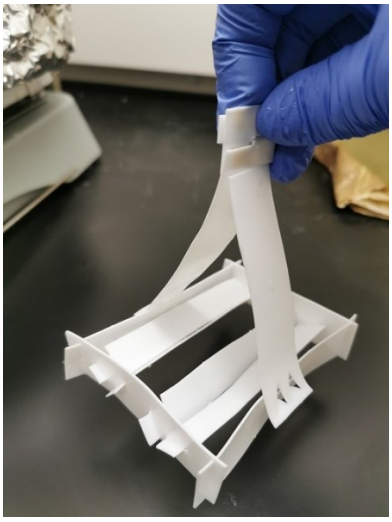

Figure 3.38 Teflon Rack for Hot KOH Etching

During the etching, membrane chips are flat lying on the mesh. Therefore, bubbles trapped under chips have to lift chips for a gap to float to the solution surface. If chips are in an oblique position or have a gap from the mesh, the interference of bubbles for chips can be minimized.

Another etching Teflon rack is then made for the solution (see Figure 3.38). After the half etched wafer is separated into several parts, membrane chips can be placed on the Teflon rack with oblique placement.

Result:

This Teflon rack completely solved this problem. All membrane chips survived after the hot KOH etching process. Additionally, membrane chips can be left on the rack. The whole rack can be lifted out of the KOH solution with the designed clamp and transported to DI water for further membrane chip cleaning steps. Since the rack is made of Teflon sheet, it is relatively soft for bending. Therefore, the tweezer can simply push the rack slightly to form a gap between the chips and the rack to pick up the chip easily.

3.1.6 Results of Membrane Chip Fabrication

During the whole fabrication period, we fabricated eight wafers full wafers. The first two wafers did not produce any useful membrane due to overetching (wafer 1) and under etching (wafer 2) during the RIE step. As seen in Table 3.2, the fabrication yield gradually increased after every batch. The cause of this improvement is not only due to fine-tuning of the recipe, but also to an improvement of chip manipulation skills.

Table 3.2 Membrane chips survival status for each fabrication batch.

Membrane Size / Batch #	1 mm (3 chips)	1.5 mm (5 chips)	3 mm (8 chips)	6 mm (9 chips)	12 mm (4 chips)
1	0	0	0	0	0
2	0	0	0	0	0
3	3	0	0	0	0
4	3	3	0	0	0
5	3	4	5	5	1
6	3	5	6	6	1
7	3	5	7	8	2
8	3	5	8	7	2

We have also quantified the deviation of fabricated membrane dimensions from the nominal dimensions to the actual fabricated devices. This data was used for the work in [10], but is reproduced here in table 3.3 theoretical for completeness. We note that the membrane sizes are typically larger by 120 um compared to the designed dimensions. This can be explained by the uncertainty on the initial substrate thickness, and also by the non-zero etch rate of KOH along the <111> planes.

Table 3.3 Actual membrane dimensions compared to designed membrane dimensions. Measurements are performed on up to four different membranes.

Designed Membrane Dimensions (mm)	Actual Membrane Dimensions (mm)			
1.5	1.613	1.609	N/A	N/A
3	3.114	3.101	3.144	3.153
6	6.108	6.119	6.129	6.169
12	12.11	12.106	12.121	N/A

3.2 Actuation Device Fabrication

For the on-chip actuation method, we fabricated two types of metal-dielectric-semiconductor structures. This chapter shows the procedure to fabricate the two types of metal electrodes on the SiN layer of the membrane chip. The first subsection (3.2.1) explains the principle behind each step of the fabrication procedure. The second subsection (3.2.2) provides specific process step parameters. Finally, the last section (3.2.3) describes several challenges and corresponding adjustments performed during the recipe development.

3.2.1 Fabrication Procedure Overview

This subchapter introduces the procedure for depositing the aluminum layer onto SiN membrane chips, fabricated from the recipe described previously, and for connecting wire to either the aluminum layers or the SiN film on the frame area. In order to deposit aluminum on SiN membrane chips in the evaporator, a shadow mask is used to cover the rest area on the chip. The shadow mask is made from a 51 μm thick steel metal shim and cut by the ultra-fast laser-cutting machine available at Prof. Arnaud Weck's laboratory. Then, the chip with the mounted shadow mask goes inside of the evaporator for 100 nm aluminum deposition (see Figure 3.39). After deposition, compatible vacuum wire is attached to those aluminum pads with nickel paste. The nickel paste is applied with toothpicks and then undergoes a heat curing process, as instructed in the product spec

sheet.

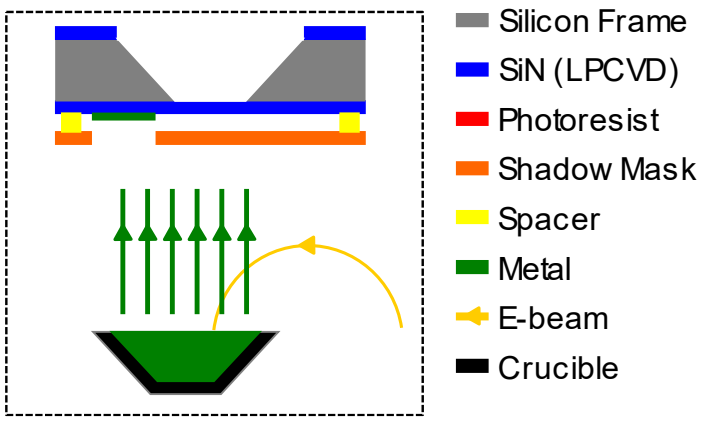

Figure 3.39 Metal deposition in the evaporator.

3.2.1.1 Shadow Mask Laser Cutting

There exist many possible ways to fabricate shadow masks. However, all share some standard fundamental requirements. The first requirement is vacuum compatibility since it will go for aluminum deposition with high vacuum environment in evaporator. Photolithography on a chip with suspended membranes is not possible due to the risk of breaking the devices. In contrast, using sheet metal is much easier, especially with the help of ultra-fast laser cutting.

The ultra-fast laser cutting machine is located in Prof. Arnaud Weck's Lab. The laser delivers energy to vaporize the target material (i.e., metal sheet in this case) to perform material removal on the laser moving path. In order to obtain fine edges, multiple passes are used to remove sharp spikes from the edges. The vaporized material returns to solid as dust falls on the mask. An ultrasonic bath and clean room tissue wiping are used for cleaning the mask after cutting. A detailed procedure for these steps is listed later in this section.

Using of laser cut shadow mask has pros and cons. The laser cutting method is relatively fast and flexible—multiple designs for different geometries can be produced at a very low cost (i.e., sheet metal is not expensive). In contrast, photolithography requires relatively expensive photomasks, and they are permanent. The sheet metal mask is also straightforward to mount onto chips, with double-sided tape in this case. In contrast, photolithography demands several complex processes (i.e., spin coating, baking, exposure, etc.). Sheet metal masks also have disadvantages. They usually have rough etches and imprecise geometries. In fact, laser cutting itself is precise, but the bending of the metal sheet can occur and lead to geometry changes. Spikes from cutting edges can easily stab and break membranes. The uncertainties of geometries can also change the size of the aluminum pad area after deposition. Nevertheless, these weaknesses are not critical to our devices. The mask can be lifted up with spacers between mask and chip to protect membranes from spikes located at cutting edges. This can cause enlarging aluminum pads a bit and obtaining blur boundaries around pads after deposition. However, our device is not restricted to precise deposited pad geometries.

3.2.1.2 Aluminum Electrode Pads Deposition

Aluminum electrode pads are used for depletion metal-dielectric-semiconductor (MDS) capacitors. The shadow mask is mounted onto the chip with double-sided tapes. The deposition takes place in the evaporator.

The evaporator uses an electron beam (e-beam) to melt and vaporize the material in the crucible (see Figure 3.39). In high vacuum, the vaporized metal molecules travel directly from the crucible to the exposed area in the chamber. The evaporator is equipped with a sensor to monitor the layer

thickness during deposition. The electrical power adjustment of the e-beam can control the deposition rate. Usually, a rate as steady as possible is required since different rates result in different roughness levels of the deposited layer surface.

In this work, during the deposition, shadow mask cavities will be the path for evaporated aluminum vapor to float up and attach to the chip to obtain an aluminum layer in the evaporator.

3.2.1.3 Nickel Paste Wire Mounting

In order to deliver an electrical signal to the MDS device, wires have to be attached to each pad. The mounting adhesive is nickel paste (PELCO® High Performance Nickel Paste and Product No. 16059, 16059-10) since it is vacuum compatible and has good electrical conductivity. It also can be attached either to the aluminum pads or to the SiN layer directly in the accumulation case.

3.2.2 Detailed Recipe

This section will introduce the procedure for the actuation device. The first step is to have a shadow mask machined from steel sheet metal by the ultra-fast laser located in Prof. Arnaud Weck's Lab. Then, the mask is mounted on the membrane chip with double-sided tape. After that, the masked chip is mounted onto the sample disk in the evaporator for aluminum deposition. Eventually, aluminum pads on the chip are attached with vacuum compatible wires for electric connection as the depletion model. For the accumulation model, wires can be directly mounted onto the chip by Nickel paste without metal deposition.

I. Shadow mask design and machining

   a) The shadow mask can be designed using Solidworks software. The export file should be

in DXF file. This type of file can be turned into code for laser cutting paths in Prof. Arnaud Weck's lab computer.

b) Use femtosecond laser (PHAROS from light Conversion, Inc.) to machine the blue tempered high carbon steel shim. Here are parameters for laser running:

   i. Power: 0.36 W

   ii. Speed: 0.1 mm/s

   iii. Frequency: 1 kHz

c) For laser machining, only one pass is needed to cut through the sheet metal. However, it has rough cutting edges. In order to have smoother profile on cutting edges, it needs to be cut at least three times.

d) After machining, the mask is covered with a lot of dust. First, use cleanroom tissue to wipe clean. Then, use an ultrasonic bath to have a deep cleaning with Elmasonic P 30 H Ultrasonic cleaning unit. The ultrasonic unit is set with the following parameters:

   i. Power: 30% total power

   ii. Frequency: 80 kHz

   iii. Time: 5 min

e) See the picture of the shadow mask in Figure 3.40.

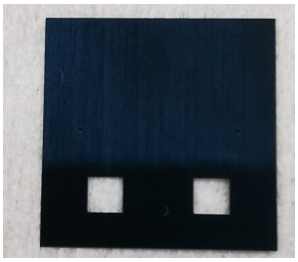

Figure 3.40 Shadow mask made of steel sheet metal.

II. Shadow mask mounting.

In order to protect membranes, the mask should not make contact with the suspended membrane at any contact point. Therefore, a spacer is needed to mount the mask and the chip together with a gap for membrane protection. The Figure 3.39 schematizes the spacer location. We vacuum compatible Kapton double-sided tape as a spacer.

III. Aluminum deposition

a) Before the deposition, mount the sample onto a glass slide with double-sided tape.

b) In the evaporator vacuum chamber (Angstrom Nexdep series Thermal/Electron Beam Evaporator), the sample needs to be mounted onto the sample holder shown in Figure 3.41.

Figure 3.41 Sample glass side mounted on the evaporator sample holder.

c) Put this holder onto the top of the chamber and connect the wire plug properly. Close the shutter to shield the holder (see Figure 3.42).

Figure 3.42 Assembled sample holder with the shutter closed.

d) Check the crucible for the right deposition materials (Ti and Al).

e) Lock the door of the evaporator chamber and start the pump down sequence from the computer controller.

f) Start deposition when the vacuum reaches 9E-7 Torr. Use pattern 2 (see Figure 3.43) or 6 for crucible protection.

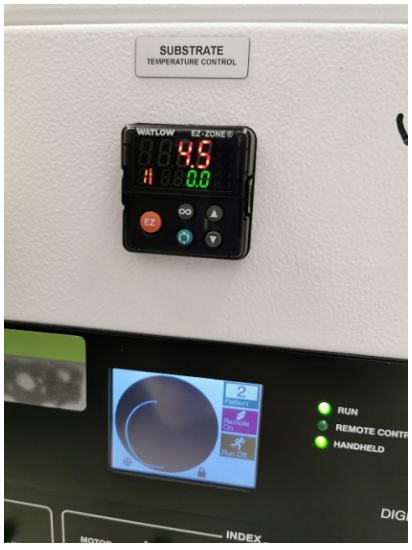

Figure 3.43 E-beam sweep pattern in use.

g) Deposit 5 nm Titanium for adhesion layer.

h) Deposit 100 nm Aluminum.

i) Pump up the inner pressure back to ambient pressure. Open the chamber and detach the glass side from the holder.

j) Reassemble the evaporator and close the chamber with a rough pump down process ongoing.

IV. Nickel paste wire attachment

a) Use soft tip tweezers to detach the mask from the chip. (Clean the mask with an ultrasonic bath after every use.) Remove double-sided tape spacers.

b) Prepare following items for wire attachment:

i. Silver plated copper wire in Figure 3.44, 34 AWG from Accu-Glass (Part#: 110824)

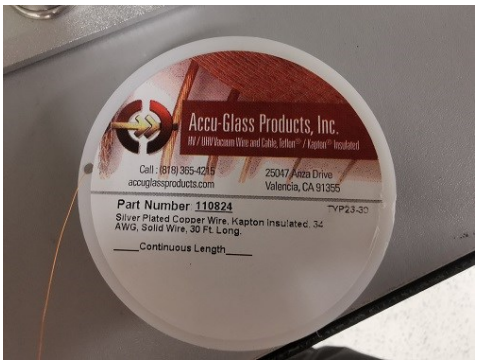

Figure 3.44 Vacuum compatible wire.

ii. 2-inch-long sandpaper strip (180 Grit) in Figure 3.45.

Figure 3.45 Sandpaper box.

iii. PELCO® High Performance nickel paste in Figure 3.46

Figure 3.46 Nickel paste.

iv. Bamboo toothpicks

v. Glass slide

vi. Hot plate

vii. Aluminum foil

viii. Multimeter

ix. Vacuum compatible double-sided tape

c) Set the hot plate at 50 °C. Mount the chip on the glass slide with double-sided tape. Place the glass slide onto the hot plate to heat up the chip.

d) Take a piece of sandpaper and fold it like shown in Figure 3.47.

Figure 3.47 Kapton insulation removal tool made by sandpaper piece.

e) Cut two pieces of wires with lengths measured in advance and use sandpaper to remove the Kapton insulation for both wire ending tips.

f) Use a multimeter to read the resistance of the wire to make sure that insulation is successfully removed. (the readout of resistance should be around 2 Ω)

g) Use a sharp tip tweezer to bend the wire tips into a small hook shape.

h) Use a toothpick to take out a piece of nickel paste and place it on the wire hook.

i) Quickly attach the wire hook to the aluminum pad area and use another clean toothpick to press down the nickel paste piece on the chip for at least 30 s.

j) The nickel paste should be dried out and turns to lighter grey from the original dark grey color. Then, the toothpick can be lifted from the paste.

k) Repeat steps from h) to j) for the second wire attachment. See Figure 3.48 for depletion model actuation device.

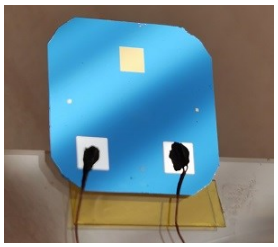

Figure 3.48 Picture of depletion model actuation device with aluminum pads.

l) Shut down the hot plate and remove the glass slide.

m) Let the paste have about 2 to 4 hour set period at room temperature, followed by 93 °C curing on the hot plate for 2 hours.

n) The procedure above is to build a depletion model (i.e., with aluminum pads). For the accumulation case, it only requires steps from b) to m) to attach wires directly to the chip. See Figure 3.49 for the accumulation model actuation device.

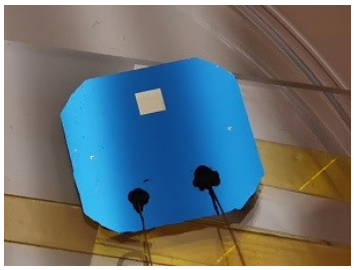

Figure 3.49 Picture of accumulation model actuation device with a nickel layer.

o) Connect wires with a lock-in amplifier and point the optical fiber to the center of the membrane in the vacuum chamber. Test the circuit connection through the lock-in amplifier and pump down the chamber for further measurement.

3.2.3 Discussion on Problems Encountered and Developed Solutions

In this section, several difficulties faced and adjustments made accordingly, during the procedure development, will be presented.

3.2.3.1 Shadow Mask Breaks Membrane due to Contact

Issue:

While mounting the mask on the chip, the mask physically touches the membrane and breaks it. The previous mounting method used the crystal bond. It requires about 70 °C to melt and will recrystallize when the temperature drops. There is no gap between the mask and the chip. The purpose is to minimize the deviation of the metal deposition geometry.

Solution:

Use double-sided tape to mount and use it as spacers at the same time. The aluminum pads are designed as 2 mm × 2 mm size. The deviation during deposition caused by the gap in between will not impact the geometry too much. It is acceptable.

Result:

With spacers in between and careful manipulation, the mask cannot touch the membrane anymore. The membrane can survive after mask mounting. The geometry of aluminum deposition does not have any significant changes.

3.2.3.2 Adhesion Issue between Aluminum and SiN

Issue:

After the nickel paste wire attachment, the mounting was easily peeled off from the aluminum layer and peeled off the aluminum layer partially from the chip (see Figure 3.40).

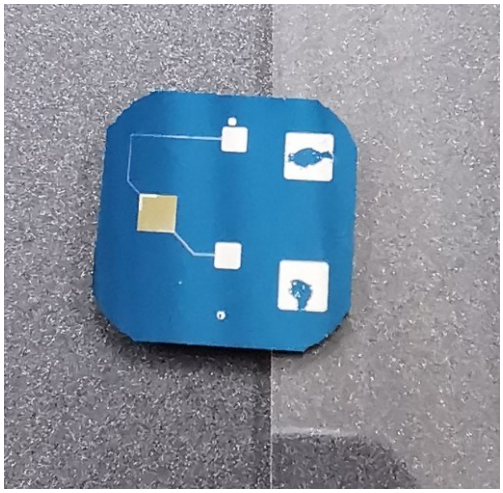

Figure 3.50 Adhesion issue between aluminum layer and SiN layer.

Solution:

The cause is the poor adhesion between the aluminum and SiN. In this case, we decided to add an adhesion layer in between. In order to minimize the distance change between the metal layer and the silicon substrate, only 5 nm titanium is added in between.

Result:

With a 5 nm titanium adhesion layer, the wire attachment is fairly strong to allow further measurements.

4. Actuator Modeling

Following the comparison of actuation methods in the literature review section, we decided to build a metal-dielectric-semiconductor (MDS) capacitor actuation system (see Figure 4.1) on SiN membrane chips that were fabricated from the recipe mentioned earlier (see section 3.1). Therefore, in our case, the MDS capacitor actuation system is built as metal-SiN-silicon capacitors.

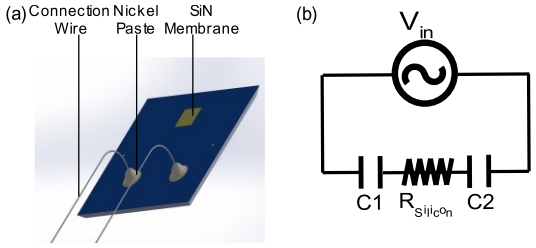

Figure 4.1 (a) SiN resonator actuation device schematic and (b) equivalent circuit.

With our MDS capacitor actuation system, we experimentally observe the actuation of SiN drum resonators by applying an alternative (AC) voltage source on double MDS capacitors assembly shown in Figure 4.1b. We hypothesize that such AC electrical current is able to actuate the membrane by creating acoustic waves in the substrate, which can originate from either electrostatic attraction forces in the capacitors (see subchapter 4.1) or thermal expansion forces in the substrate (see subchapter 4.2). In the following, we present our experimental observations as well as first-principal models for these two possible mechanisms. In the electrostatic case, voltage-dependent mechanical stress arising from charge attraction in the Metal-SiN-Si capacitor structure creates acoustic waves that can travel in the substrate and actuate the membrane. Such effect was previously observed in cantilever resonators with p-n junction under reverse bias [25], but not in the context of a capacitively coupled metal-dielectric-semiconductor (MDS) assembly. In the thermal expansion case, periodic Joule heating creates a similar acoustic wave in the substrate. A similar effect has been analyzed previously in the context of electrostriction studies in silicon [49].

Our calculations show that electrostatic attraction in the capacitors is most likely the dominant effect in the present configuration as it likely dominated over thermal effects by several orders of magnitude

4.1 Electrostatic Model

In an MDS capacitor (see Figure 4.2), varying the applied voltage influences the electrical charge distribution, which in turn can create varying mechanical stress resulting from electrostatic attraction forces. As within any solid object, we can expect that time-dependent strain will create an acoustic wave, which can travel in the substrate and reach the membrane, thus enabling actuation.

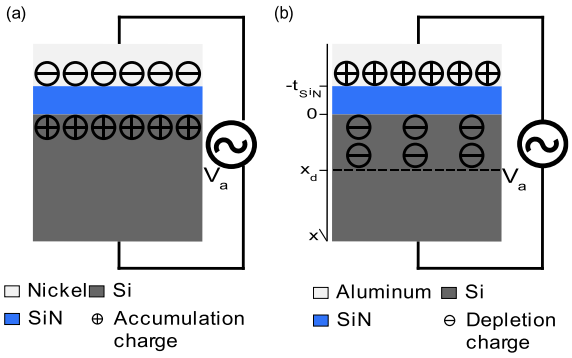

Figure 4.2 Actuation schematics with (a) accumulation regime and (b) depletion regime.

In the following subsections (i.e., 4.1.1 and 4.1.21), we analyze charge interaction inside MDS capacitors within the framework of two possible regimes—charge accumulation or charge depletion—which occur depending on the workfunction differences (V_{fb} in Figure 4.3) between the metal (ψ_m) and the semiconductor (ψ_s). Theoretical description of these regimes is widely available in the context of Metal-Oxide-Semiconductor (MOS) devices [46]. Unless otherwise noted, all descriptions below are for p-type semiconductors.

4.1.1 Accumulation

We first investigate stress in the accumulation regime (i.e., $\psi_m > \psi_s$, see Figure 4.2a). In this case, charges accumulate in a sheet-like matter on each side of the dielectric (see Figure 4.2a), and a simple parallel plate capacitor model suffices for calculating the mechanical stress. We define the capacitance per unit area as $C_{SiN} = \frac{\varepsilon_{SiN}}{t_{SiN}}$, with ε_{SiN} as the dielectric constant for SiN, and t_{SiN} as the dielectric thickness. The electrical energy stored in a capacitor is given by $\frac{CV^2}{2}$. By taking the derivative of the capacitor energy along the thickness, we obtain the attractive force between the sheet charges, $F = \frac{C_{SiN}V^2A}{2t_{SiN}}$, where A is the metal contact area. We express the effective spring constant of the dielectric layer, in a one-dimensional approximation, as $k = \frac{E_{SiN}A}{t_{SiN}}$, where E_{SiN} denotes the Young's Modulus. By combing the expressions of force and stiffness, we obtain the strain energy stored in the capacitor as a function of voltage, in quasi-static conditions:

$$U = \frac{F^2}{k} = \frac{V^4 {\varepsilon_{SiN}}^2 A}{4 {t_{SiN}}^3 E_{SiN}}. \tag{4.1}$$

The voltage V in Eq. (4.1) includes the applied voltage, V_{in}, as well as the flat band voltage $V_{fb} = \psi_m - \psi_s$, i.e., $V = V_{in} - V_{fb}$ [46]. Substituting in Eq. (4.1), we finally obtain:

$$U_{acc}(V_{in}) = \frac{\left(V_{in} - V_{fb}\right)^4}{4} \frac{{\varepsilon_{SiN}}^2 A}{{t_{SiN}}^3 E_{SiN}}. \tag{4.2}$$

When applying a time-dependant actuation voltage V_{in} on a single capacitor, the peak-peak variation in stored strain energy is given by:

$$U_{p-p,acc}(V_{in}) = U_{acc}(V_{in}) - U(-V_{in}) = \frac{2{\varepsilon_{SiN}}^2 A}{{t_{SiN}}^3 E_{SiN}} (V_{fb} {V_{in}}^3 + {V_{fb}}^3 V_{in}). \tag{4.3}$$

In the equivalent circuit shown in Figure 4.1b, two capacitors are in series and each capacitor sees half of the applied potential, such that the peak-to-peak variation of mechanical energy in the

capacitors becomes:

$$U_{p-p,2,acc}(V_{in}) = 2\left(U_{acc}\left(\frac{V_{in}}{2}\right) - U_{acc}\left(-\frac{V_{in}}{2}\right)\right) = \frac{2{\varepsilon_{SiN}}^2 A}{{t_{SiN}}^3 E_{SiN}}\left(\frac{V_{fb}{V_{in}}^3}{4} + {V_{fb}}^3 V_{in}\right). \quad (4.4)$$

We note that Eq. (4.3) and (4.4) yield null values if $V_{fb} = 0$, meaning that only harmonic actuation would be possible in this case.

4.1.2 Depletion

In the depletion case (i.e., $\psi_m > \psi_s$, see Fig. 1d), three-dimensional charge distribution (see Figure 4.2b) in the semiconductor imposes that we integrate the stress along the depletion region (x_d), which dimension is illustrated in Figure 4.2b and given by [46]:

$$x_d(V_{in}) = -\frac{\varepsilon_{Si}}{C_{SiN}} + \sqrt{\left(\frac{\varepsilon_{Si}}{C_{SiN}}\right)^2 + \left(\frac{2\varepsilon_{Si}}{qN_A}\right)\left(V_{in} - V_{fb}\right)}, \quad (4.5)$$

where ε_{Si} is the dielectric constant of silicon, $q = 1.602 \times 10^{-19}$ C is the electron charge, and N_A is the acceptor concentration. From continuum mechanics [25], the local stress σ at a given position x_e in the junction is given by integrating forces in the junction $\sigma(x)$, starting from the stress-free position at $x = x_d$ (i.e., we assume no stress where the electrical field is null):

$$\sigma(x_e) = -\int_{x_d}^{x_e} dF(x), \quad (4.6)$$

where $dF(x) = \mathrm{E}(x) \cdot \rho(x) \cdot dx$, $\rho(x)$ is the charge density, and $\mathrm{E}(x)$ as the electric field. In the depletion region, $\rho(x) = -qN_A$ and $\mathrm{E}(x) = \frac{qN_A(x_d - x)}{\varepsilon_{Si}}$ [45], such that the integral yields:

$$\sigma(x) = \frac{(qN_A)^2}{\varepsilon_{Si}}\frac{(x_d - x)^2}{2}, for\ 0 < x < x_d. \quad (4.7)$$

By ensuring the continuity of stress (i.e., force balance) at the Si/SiN interface, and by assuming no stress outside of the junction region, we also find:

$$\sigma(x) = \begin{cases} \frac{(qN_A)^2}{\varepsilon_{Si}} \frac{{x_d}^2}{2} \text{ , } for\ -t_{SiN} < x < 0. \\ 0, for\ x < -t_{SiN}\ or\ for\ x > x_d. \end{cases} \quad (4.8)$$

The strain energy stored in a thickness dx of the junction is given by $dU = \frac{1}{2}\sigma\epsilon\, d\forall$ with $d\forall = A \cdot dx$. By considering the stress-strain relation $\epsilon = \sigma/E$, we can integrate $dU = \frac{1}{2E} A\, \sigma^2\, dx$ over the junction length (i.e., from $-t_{SiN}$ to x_d), to obtain the total expression for the strain energy stored in the junction:

$$U_{dep}\big(x_d(V_{in})\big) = \frac{A(qN_A)^4(x_d)^4}{8(\varepsilon_{Si})^2}\left(\frac{t}{E_{SiN}} + \frac{x_d}{5E_{Si}}\right). \quad (4.9)$$

Note that this relation depends on the applied voltage V_{in} through Eq. (4.5). In the depletion case, analyzing two capacitors in series is not as straightforward since the capacitor values are voltage-dependent; we therefore do not derive a simple expression as in Eq. (4.3) – (4.4) for the charge accumulation case.

Nevertheless, we can get a sense of which of the two regimes produces the most variation in strain energy by comparing Eq. (4.2) with Eq. (4.9), as shown in Figure 4.3. We note that a capacitor in the accumulation regime stores more mechanical energy, which is likely due to the weaker junction capacitance occurring in the depletion regime.

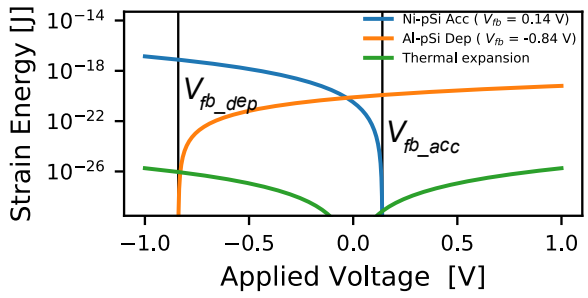

Figure 4.3 Theoretical stored strain energy vs. applied voltage with accumulation model and depletion model comparing to thermal model. A capacitor area of 2×2 *mm*^{2} *and a SiN layer thickness of 100 nm is used for the calculations.*

In a practical situation, such as for the experimental results presented later in chapter 5, the applied voltage (V_{in}) can typically extend beyond the flatband voltages of the capacitors. Capacitors can therefore undergo a change of regime, between accumulation and depletion, during each actuation cycle. It is therefore likely that the choice of metal (i.e., the flatband voltage) does not have a critical influence on actuation performances.

4.2 Thermal Expansion Model

Current flowing in the silicon substrate may also cause an acoustic wave resulting from thermal expansion-induced mechanical stresses. The strain energy due to a temperature change ΔT in a volume $\forall$ is given by [50]:

$$U = \frac{1}{2} \forall E \varepsilon^2 = \frac{1}{2} \forall E_{Si} \alpha^2 \Delta T^2, \tag{4.10}$$

where α is the thermal expansion coefficient of the material, silicon in our case. $\forall$ represents the effective silicon volume that expands under the effect of Joule heating.

Assuming a simple lumped thermal capacitance model [51], the amplitude of time-dependent temperature signal ΔT is proportional to the dissipated power P_{in}, and is filtered by a one-pole

low-pass filter of characteristic response time τ_{th}:

$$\Delta T = P_{in} \cdot R_{th} \frac{1}{1 + \omega \tau_{th}}, \tag{4.11}$$

where the R_{th} is the thermal resistance, in units of [K/W], between the heated volume and its surrounding environment. The angular frequency of actuation is denoted by ω, while the characteristic thermal response time is $\tau_{th} = R_{th} \cdot C_{th}$. In turn, the thermal capacitance $C_{th} = \forall \rho c_p$ (in units of J/K) is derived from the element volume $\forall$, its density (ρ) and specific heat (c_p). If we now assume that the thermal response is much slower than the actuation frequency (i.e., $\omega \gg 1/\tau_{th}$), Eq. (4.11) simplifies to a form a that does not depend on R_{th}:

$$\Delta T = \frac{P_{in} \cdot R_{th}}{\omega \cdot R_{th} \cdot C_{th}} = \frac{P_{in}}{\omega \cdot C_{th}}. \tag{4.12}$$

By substituting Eq. (4.12) into Eq. (4.10), we obtain the following expression of thermal strain as a function of the dissipated electrical power P_{in}:

$$U_{th} = \frac{1}{2} \forall E_{Si} \alpha^2 \left(\frac{P_{in}}{\omega \cdot C_{th}} \right)^2. \tag{4.13}$$

Referring to the equivalent electrical circuit in Figure 4.1b, we express the dissipated electrical power as $P_{in} = R_{Si} \cdot I^2$. We assume (with experimental evidence given later in Figure 5.3) that the capacitor's impedance Z_c is the factor limiting the current I. Therefore, by using $I = \frac{V_{in}}{Z_c} = V_{in} \cdot j \cdot \omega \cdot C_{eq}$, the dissipated power P_{in} can be rewritten as a function of the applied voltage:

$$P_{in} = R_{Si} \cdot V_{in}^2 \cdot \omega^2 \cdot \left(\frac{C_{SiN} A}{2} \right)^2, \tag{4.14}$$

where V_{in} is the input voltage and $\frac{C_{SiN} A}{2}$ is the equivalent capacitance of the two capacitors in series. Substituting in Eq. (4.13), the strain energy as a function of applied voltage is given by:

$$U_{th} = \frac{1}{32} E_{Si} \alpha^2 \omega^2 V_{in}^4 \left(\frac{R_{Si} C_{SiN}^2 A^2}{C_{th}} \right)^2 \forall. \quad (4.15)$$

In Eq. (4.15), we can finally substitute geometrical parameters to estimate the magnitude of thermal expansion forces relative to electrostatic forces. As a rough first-principle approximation, we approximate the interaction volume $\forall$ as the cylinder depicted in Figure 4.4, with $L \approx 4$ mm given by the spacing between the electrodes, and A as the electrode area (e.g., 4 mm^2 in our typical configuration). We use $R_{Si} \approx \frac{\rho_{el} \cdot L}{A}$ with ρ_{el} as the resistivity of silicon. Eq. (4.15) can finally be rewritten as:

$$U_{th} = \frac{1}{32} E_{Si} \alpha^2 \omega^2 V_{in}^4 \left(\frac{\rho_{el} \varepsilon_{Sin}^2}{t_{SiN}^2 \rho_{Si} c_{si}} \right)^2 \forall. \quad (4.16)$$

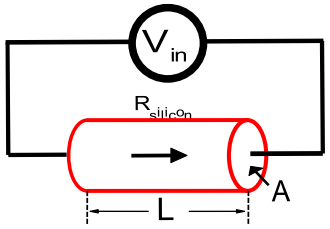

Figure 4.4 Equivalent simplified geometry and circuit for the thermal expansion model.

Considering our interaction volume of ~ 16 mm^3 and an actuation frequency of 83 kHz (representative of our experimental conditions described below), values of U_{th} are presented in Figure 4.3 and are found to be very low compared with electrostatic strain. We therefore expect the contribution of thermal expansion forces to be negligible.

5. Actuation Measurements

This chapter details the experimental setup, as well as electrical coupling measurements and mechanical actuation measurements for two types of MDS capacitor devices. Except for the description of the experimental setup, the content consists more of unprocessed raw data that is included here for the purpose of completeness and archival. The following chapter (6) contains more compiled results and their associated discussions.

5.1 Experimental Setup

Two types of MDS capacitors are experimentally investigated in the present work. The first type is formed by depositing two 2×2 mm^2 aluminum pads on the silicon substrate using a shadow masks process and electron beam metal evaporation (see Figure 3.39). The second type is formed by attaching wires to the silicon nitride layer using the same nickel paste but without aluminum contact pads. The two types of fabricated samples are shown in Figure 5.1 (b, c).

As shown in the schematic of the MDS capacitor actuation (Figure 5.1 a), MDS capacitors are excited by a lock-in amplifier (See Figure 5.2) providing a sinusoidal AC voltage signal centered on one of the membrane resonance eigenfrequency. The excitation frequency is adjusted in real-time using a digital phase-locked-loop (PLL) that keeps the excitation signal centered on the membrane eigenfrequency. Membrane displacement is measured using an optical fiber interferometer to form a low finesse cavity between the optical fiber cleaved end and the membrane [52] (see Figure 5.1a). The experiment is conducted in high vacuum ($\sim 1 \times 10^{-6}$ hPa). Samples are mounted in the chamber using double-sided high vacuum compatible tape.

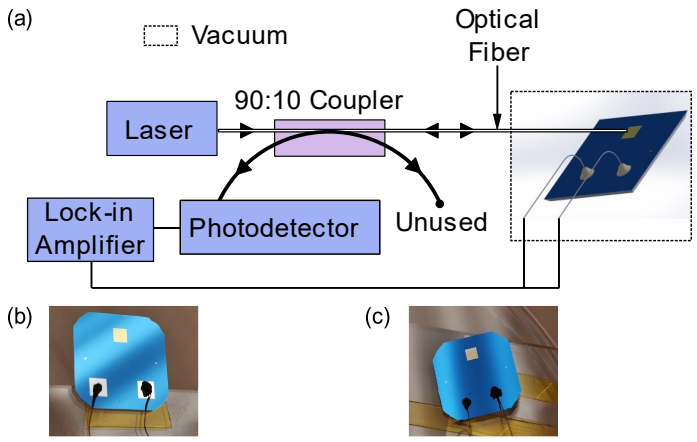

Figure 5.1 (a) Schematic illustration of the MDS capacitor actuation system driven by lock-in amplifier with optical readout scheme on SiN drum resonator in vacuum. (b, c) Metal electrodes made of (b) aluminum and (c) nickel paste

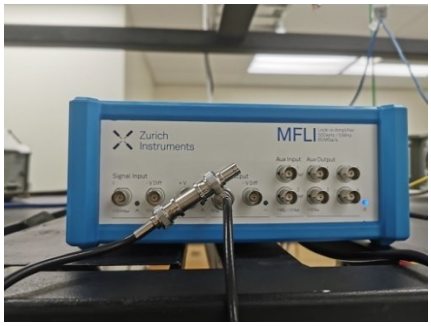

Figure 5.2 Zurich Instrument MFLI 500 kHz Lock-in Amplifier

5.2 Capacitive Coupling

Prior to performing actuation experiments, we validate that our metal contacts are indeed capacitively coupled with the substrate. In Figure 5.3, we clearly see that the current flowing between the electrode scales with the drive frequency, which is a signature of a capacitive impedance. The magnitude of the current is much higher for the aluminum pads assembly. This is likely due to the much larger contact areas enabled by the deposited aluminum pads, resulting in a lower impedance. At high frequencies, the experimental curves deviate slightly from a purely linear behavior, which likely points out to a small resistive contribution of the substrate to the total

impedance.

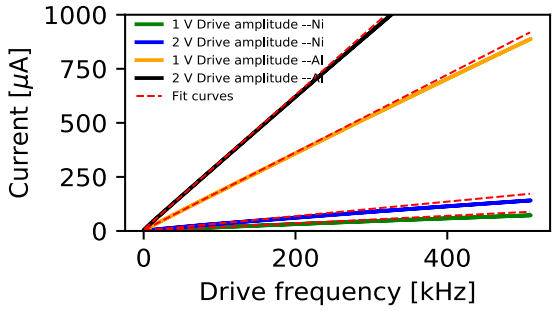

Figure 5.3 Current flow between electrodes vs. drive frequency for 1 V and 2 V drive voltages with nickel pads and aluminum pads respectively.

5.3 Membrane Displacement Measurement

This subchapter presents all relevant measurement results for both nickel layer and aluminum layer actuators on 1.7 mm × 1.7 mm membrane chips. Raw data sets include (1) calibration data on optical fiber optical interference fringe, (2) resonance frequency for each eigenmode, (3) Q-factor ringdown curve, (4) have phase-locked-loop (PLL) to lock the target resonant frequency and (5) readout from sweeping actuation voltage.

At the beginning of the measurement, in order to achieve the highest sensitivity of the readout signal, we place the optical fiber perpendicular to the membrane and move the fiber back and forth to adjust the distance between the fiber tip and the membrane. In general, the closer distance grants higher sensitivity. However, it also has a higher risk of touching the membrane which can cause major damage to the membrane resonator. Therefore, the distance between the fiber and the membrane should be adjusted slowly and carefully. The detailed procedure of this operation will be detailed in Appendix A. Figure 5.4 shows that the fiber is successfully placed to grant high

readout signal sensitivity (i.e., at the highest slope point of the interference fringe) with a sufficiently small distance to the membrane (i.e., good fringe contrast). The measurement of the maximum and minimum voltage of the interference fringes in Figure 5.4 is used for membrane displacement calculation with the drive voltage sweep charts that will be introduced later in this subsection (see Eqn. 5.2).

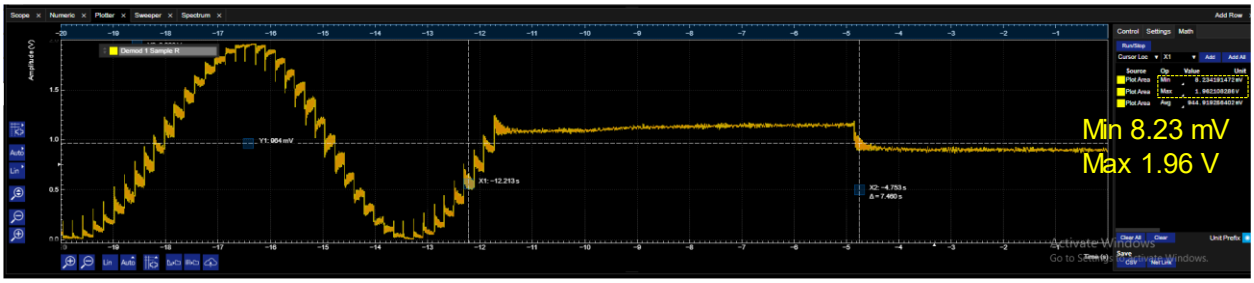

Figure 5.4 Voltage signal out of the photodetector, as a function of time, when moving the optical fiber back and forth for calibration purposes. The maximum and minimum voltages are achieved here to convert voltage signal later on into displacement signal.

Secondly, resonant frequencies ($f_{m,n}$) for each eigenmode are linked to membrane geometry by the following equation [53]:

$$f_{m,n} = \frac{1}{2}\sqrt{\frac{\sigma_b}{\rho_{SiN}}\left(\left(\frac{m}{a}\right)^2 + \left(\frac{n}{a}\right)^2\right)}, \tag{5.1}$$

where m and n determine eigenmode number, σ_b presents biaxial tensile strength (100 MPa in our case), ρ_{SiN} is the SiN density (i.e., 2.7 g/cm^2) and a is the side length of our square membrane ($a = 1.7$ mm). Therefore, Table 5.1 can be used to infer mode number (m, n) for each resonant frequency spotted from the optical readout.

Table 5.1 Theoretical resonant frequencies ($f_{m,n}$) in vacuum for each eigenmode 1.7 mm × 1.7 mm membranes.

m	n	Theoretical Frequency [kHz]
1	1	80.049
1	2	126.568
2	2	160.097
1	3	178.994
2	3	204.085
3	3	240.146

Thirdly, Q-factors are measured for each resonant frequency. After locating the resonant frequency and exciting the membrane with drive voltage, the mechanical Q-factor can be calculated from the measured exponential ringdown of the vibration after turning off the drive voltage source (see Figure 5.5).

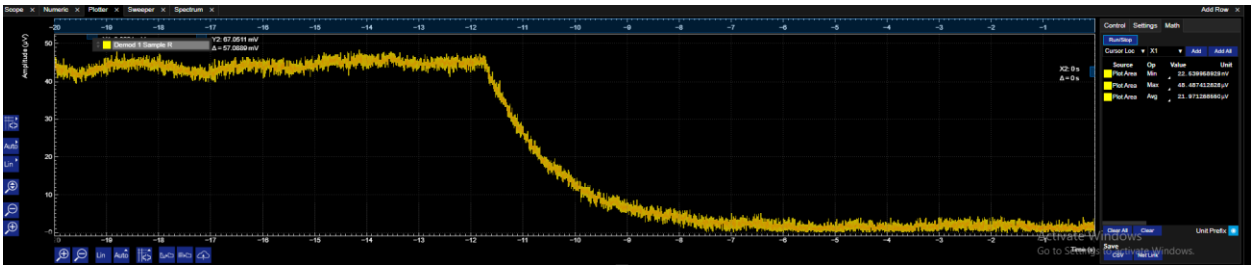

Figure 5.5 Q-factor ringdown curve with signal in voltage, as a function of time, when the drive voltage is turned off.

Higher Q-factor leads to higher mechanical susceptibility to actuation forces in resonances. Therefore, Q-factor is a relevant metric that is reported for every characterized mode in the following section. Additionally, the Q-factor value influences parameters of the frequency tracking scheme [54].

Fourthly, the phase-locked-loop (PLL) function targets the resonant frequency under actuation (see typical PLL parameters in Figure 5.6). In order to have the target frequency locked by the PLL, in the beginning, the center frequency in Figure 5.6 has to be as close as possible to the target resonant

frequency. By using the advisor panel, the PID setting suggestion can be given and applied to the PLL. Then, giving the lower and the upper limits allows the PLL to lock the frequency continuously under frequency fluctuations. Eventually, in the PLL panel, properly adjusting the setpoint value from the input section can eliminate the error in the PID setting section to lock the frequency.

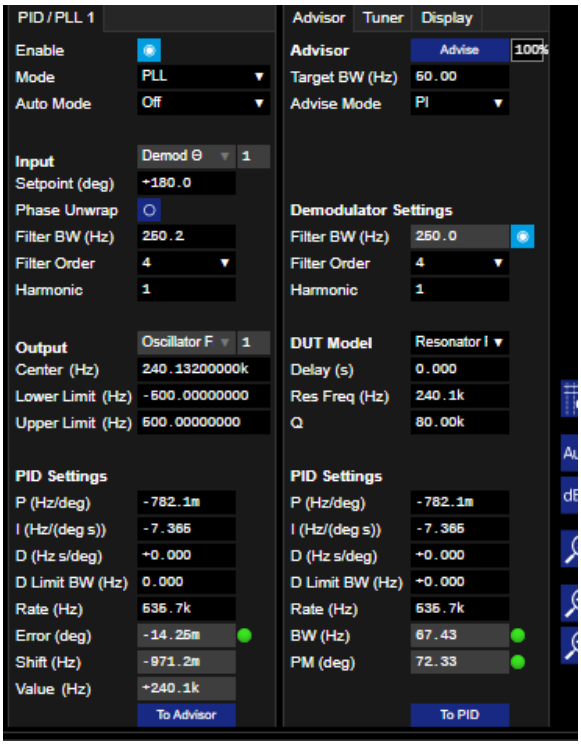

Figure 5.6 Phase-loop-lock (PLL) function for locking target resonant frequency in real-time under frequency fluctuation.

In the end, with the target frequency locked by the PLL, the membrane actuation amplitude (Fig 5.7, pink curve) can be swept and measured by varying the excitation voltage signal. Bidirectional sweeping is done to confirm data repeatability. Simultaneously, measuring the frequency shifts during the sweep (Fig 5.7, yellow curve) helps us identify possible temperature changes (see Eqn. 6.3) of the resonator which will be represented with details in subchapter 6.3. The optical readout signals strength in voltage is the raw data for membrane actuation amplitude.

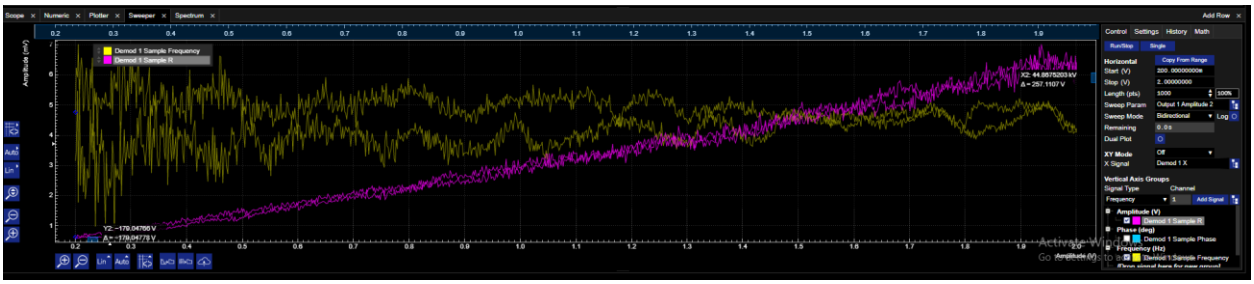

Figure 5.7 Bidirectional drive voltage sweep under PLL control. The yellow curve represents the resonant frequency shift tracking. The purple curve shows the membrane actuation amplitude in voltage from optical readout signal.

In order to find out the actual membrane displacement amplitude during the actuation, maximum and minimum fringes (V_{fmax} and V_{fmin}) measured in the first measurement step (see Figure 5.4 as an example) are used in the membrane displacement amplitude (Δd) calculation with the equation given by [52]:

$$\Delta d = \frac{\lambda \Delta V}{2\pi (V_{fmax} - V_{fmin})} \tag{5.2}$$

where $\lambda = 1563.52$ nm is the wavelength of the laser for the interferometer used in the setup and ΔV is the voltage signal amplitude from optical readout. After gathering these four sets of raw data for each metal layer (i.e., nickel and aluminum) with six different membrane vibration modes (i.e., from mode (1, 1) to mode (3, 3)), the following two subsections (5.3.1 and 5.3.2) provide measurement result on membrane displacement amplitude and target resonant frequency tracking in the function of drive voltage amplitude. Corresponding discussions are given in the following section 6.

During measurements, there are noticeable uncertainties on membrane actuation displacement amplitude for the same eigenmode with the same driving parameters. Usually, the result is going lower on amplitude. This can be explained by the small possible shifting of the optical fiber

location, which means the degradation on the fringe range of the fiber detector (i.e., V_{max} and V_{min}). Therefore, the fringe should be readjusted at most every 30 minutes by moving the fiber to avoid about 5% to 10% of uncertainty. Even with this precise fiber location control, it is also possible to have uncertainties on results for several eigenmodes. On the one hand, we do not know the exact mode shape. Hence, it is hard to find the precise location to detect. On the other hand, we do not know the precise fiber location. The fiber location adjustment is made by our bare eyes and three picomotors based on the response from the amplitude results. Therefore, according to these two reasons, it is highly possible that we do not have the highest displacement amplitudes for some modes.

5.3.1 Measurement Data for Nickel Layer Actuation (Charge Accumulation)

This subsection provides raw measurement results (see Figure 5.9 – 5.14) for the nickel layer actuation device that has two ≈ 1 mm^2 nickel electrode pads (see Figure 3.49).

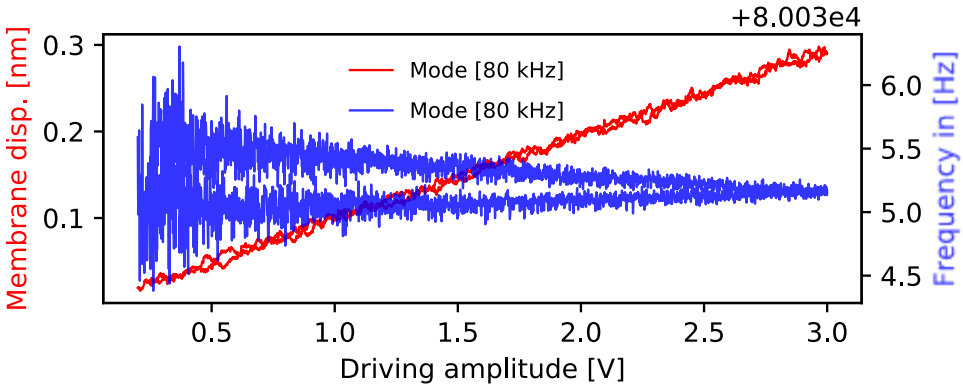

Figure 5.8 Membrane displacement and resonant frequency shift from nickel layer device for mode (1, 1) at 80 kHz with Q-factor = 308,863.

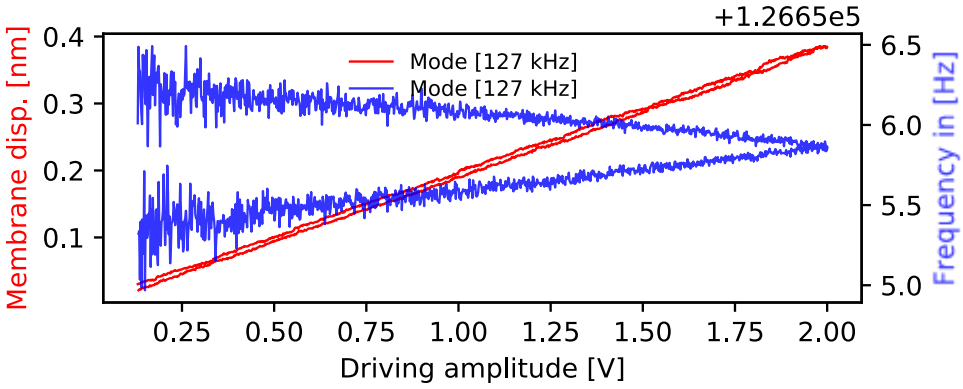

Figure 5.9 Membrane displacement and resonant frequency shift from nickel layer device for mode (1, 2) at 126 kHz with Q-factor = 260,564.

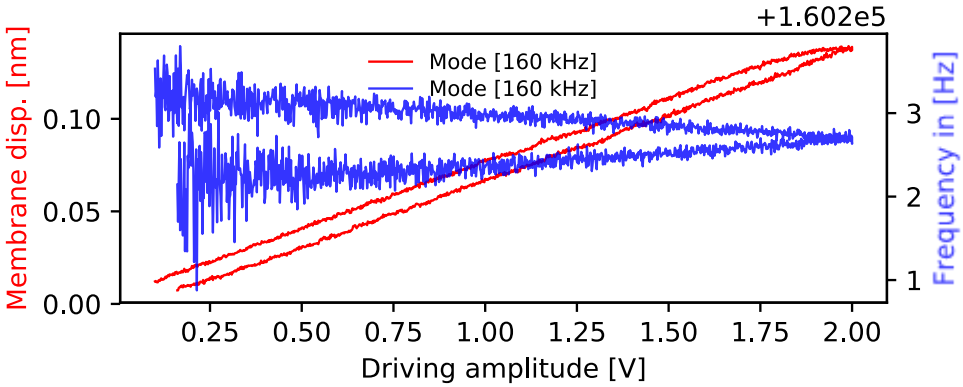

Figure 5.10 Membrane displacement and resonant frequency shift from nickel layer device for mode (2, 2) at 160 kHz with Q-factor = 1,232,847.

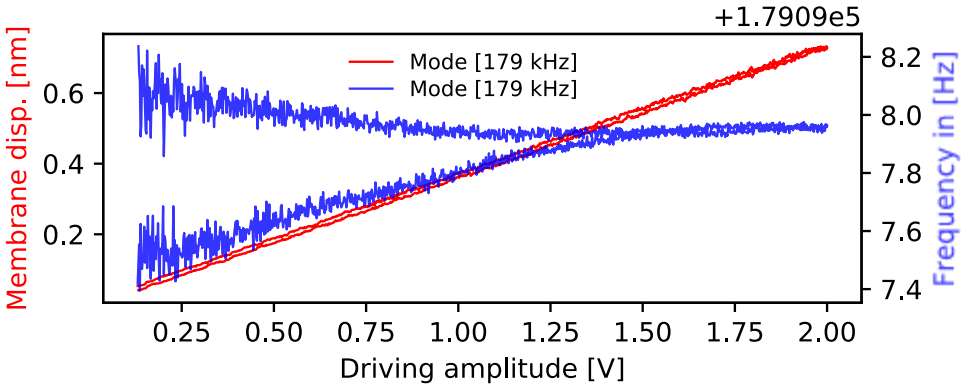

Figure 5.11 Membrane displacement and resonant frequency shift from nickel layer device for mode (1, 3) at 179 kHz with Q-factor = 354,696.

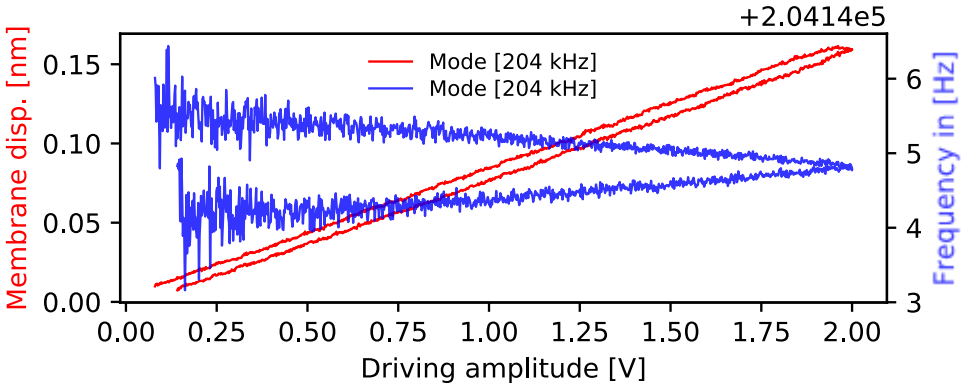

Figure 5.12 Membrane displacement and resonant frequency shift from nickel layer device for mode (2, 3) at 204 kHz with Q-factor = 916,479.

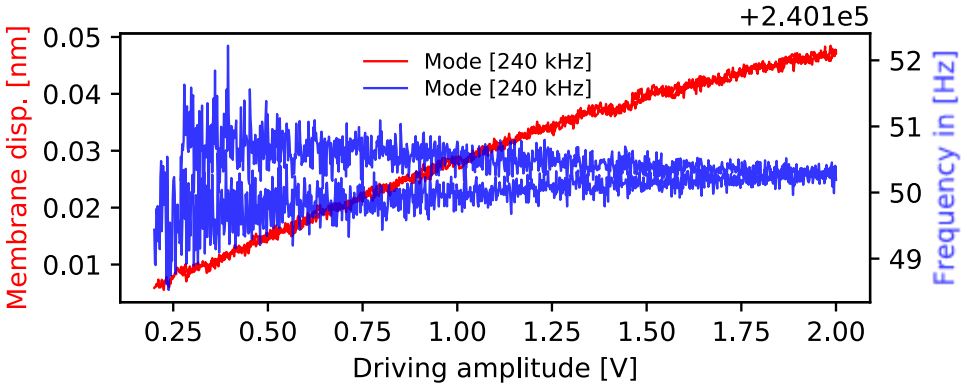

Figure 5.13 Membrane displacement and resonant frequency shift from nickel layer device for mode (3, 3) at 240 kHz with Q-factor = 290,453.

5.3.2 Measurement Data for Aluminum Layer Actuation (Charge Depletion)

This subsection provides measurement results (see Figure 5.15 – 5.20) for the aluminum layer actuation device that has two 2 mm × 2 mm aluminum electrode pads (see Figure 3.48).

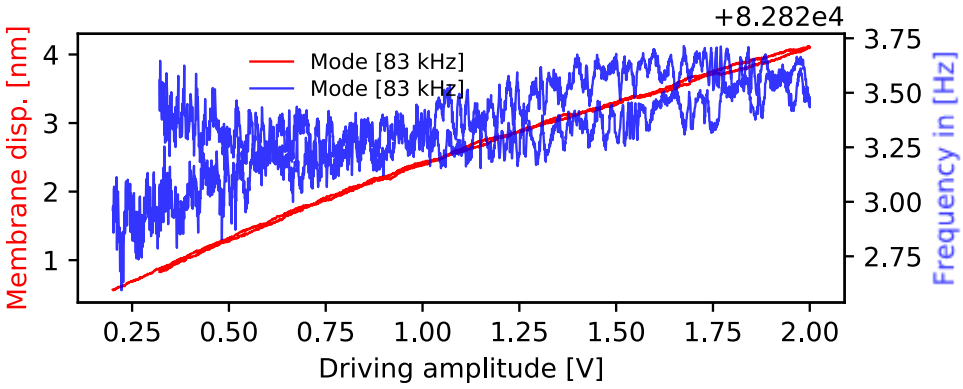

Figure 5.14 Membrane displacement and resonant frequency shift from aluminum layer device for mode (1, 1) at 83 kHz with Q-factor = 130,013.

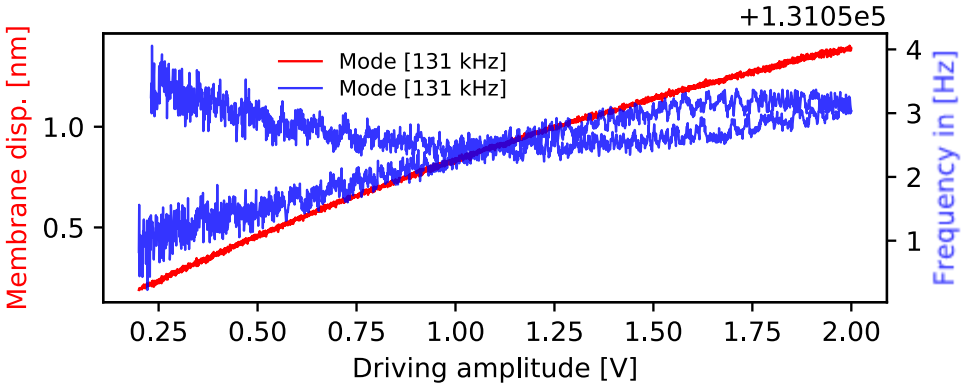

Figure 5.15 Membrane displacement and resonant frequency shift from aluminum layer device for mode (1, 2) at 131 kHz with Q-factor = 169,012.

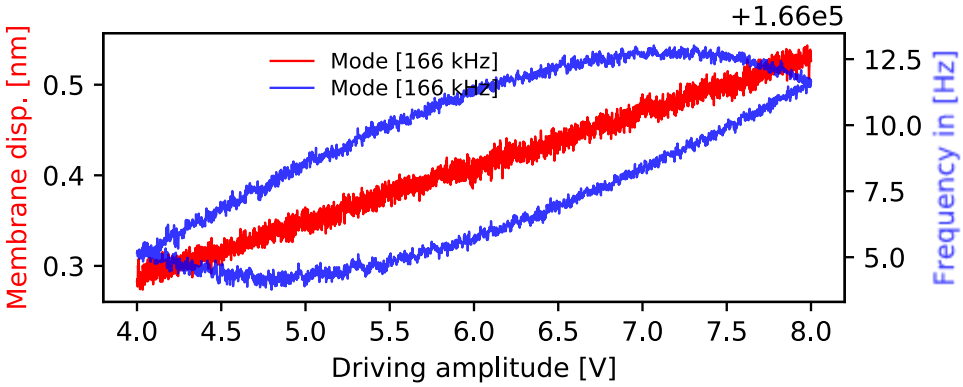

Figure 5.16 Membrane displacement and resonant frequency shift from aluminum layer device for mode (2, 2) at 166 kHz with Q-factor = 260,856.

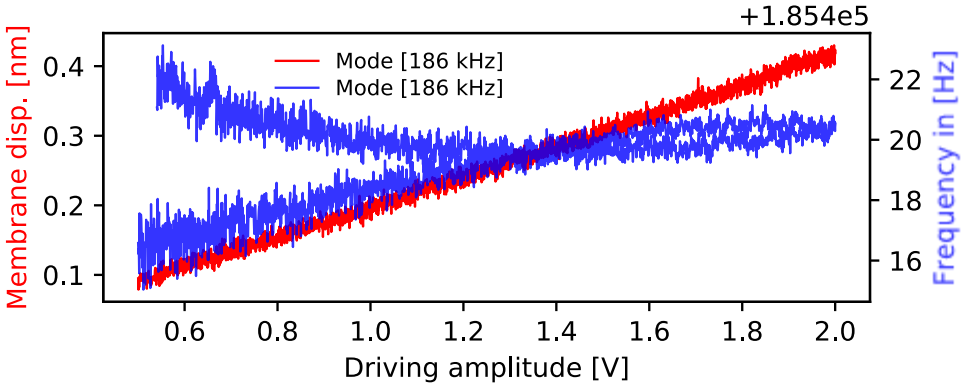

Figure 5.17 Membrane displacement and resonant frequency shift from aluminum layer device for mode (1, 3) at 186 kHz with Q-factor = 110,674.

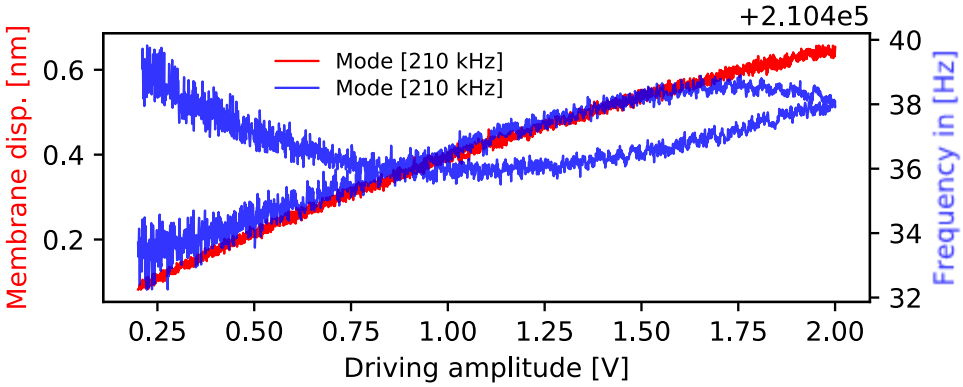

Figure 5.18 Membrane displacement and resonant frequency shift from aluminum layer device for mode (2, 3) at 210 kHz with Q-factor = 234,275.

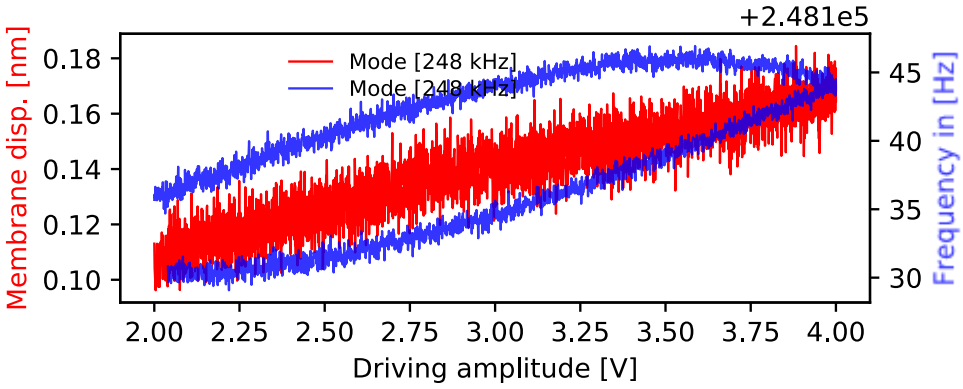

Figure 5.19 Membrane displacement and resonant frequency shift from aluminum layer device for mode (3, 3) at 248 kHz with Q-factor = 110,012.

6. Discussion on actuation results

This chapter compiles and compares the actuation results for the two types of actuators in terms of (1) actuation amplitude, (2) eigenmodes dependence, (3) power dissipation spurious heating and (4) harmonic drive.

6.1 Comparison of Accumulation and Depletion Actuation

Measurement results in section 5.3 tend to confirm our theoretical prediction that charge accumulation (i.e., Ni-pSi in our case) is more effective than charge depletion (Al-pSi) for actuating SiN membranes. Results of section 5.3 are compiled in Figure 6.1. We find that the Ni-pSi capacitor assembly achieves a 10 nm membrane actuation amplitude for a 2 V excitation signal, as opposed to 5 nm for the Al-pSi assembly. Although these amplitudes are on the same order of magnitude, the Ni-pSi achieves this result with a much smaller effective contact area (i.e., lower electrical power input), as indicated by the much lower current measurements in Figure 5.3. Additionally, the nickel layer is much easier to fabricate than the aluminum layer, requiring only vacuum compatible nickel paste as mentioned earlier in subsection 3.2.1.

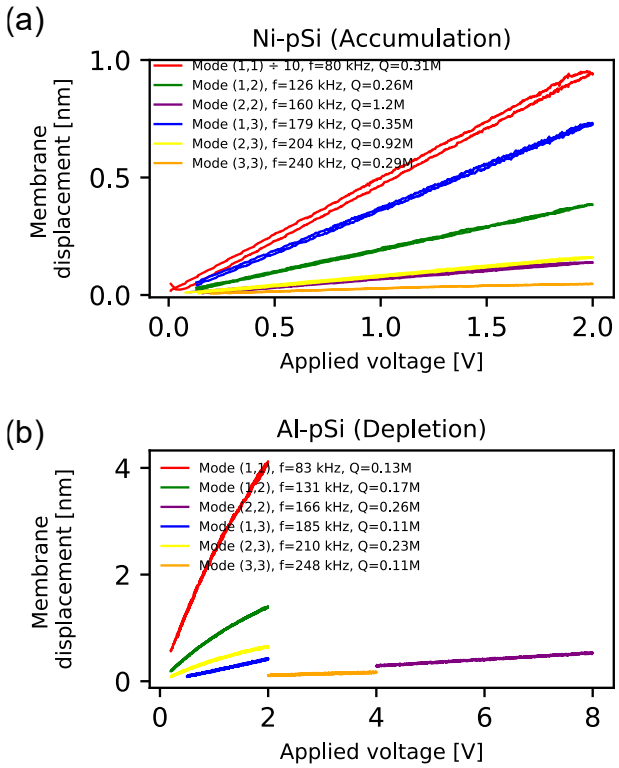

Figure 6.1 Actuation amplitude with (a) nickel layer and (b) aluminum layer for six different eigenmodes.

6.2 Actuation Performances for Different Eigenmodes

From Figure 6.1, we note that actuation amplitude decreases rapidly for higher frequency modes for both actuation models. This reduction can be partially explained by the expected increase in membrane stiffness ($k = m_{eff}\omega^2$) at higher frequencies, or by changes of mechanical susceptibility resulting from variations mechanical quality (Q) factors for the different modes (Q values are indicated in the legend in Figure 6.1). Another possible explanation is the fact that our readout optical fiber is approximately positioned at the membrane center, which corresponds to displacement antinodes only for certain modes. Moreover, modes that nominally have an antinode at this position may also be hybridized to a different mode shape [18] and show smaller amplitudes. The discontinuities shown in Figure 6.1 (b) for mode (2, 2) and mode (3, 3) can also be explained

by these reasons. When the displacement is too small for our optical readout to detect, we increase the applied voltage until the PLL can lock the resonance frequency and excite the membrane. This is why some scans do not start at 0 V, but at a higher voltage in Fig 6.1b. A more thorough investigation of acoustic coupling of the electrodes with the substrate and the membrane would be necessary for predicting actuation amplitude as a function of frequency. We note that at a typical frequency of 200 kHz, the acoustic wavelength in silicon ($\sim$1.1 cm) is comparable to the chip dimension and to the electrode spacing. It this therefore likely that these geometrical parameters play a significant role, which exact nature is beyond the scope of the present first-observation work. Likewise, the reason why some curves in Figure 6.1 (b) present a non-linear response is not entirely clear. Possible effects include change of capacitance as a function of applied voltage or mode shape changes with the excitation voltage.

6.3 Power Dissipation

We find that the dissipated power in the chip is on the order of microwatts, causing limited spurious chip heating. For example, considering the 80 kHz fundamental mode (1, 1) of the Ni-pSi case, the actuation power ($V \times I$) for a 2 V excitation is 56 µW if we use I values from Figure 5.3. Moreover, due to the mostly capacitive impedance demonstrated in Figure 5.3, only a small fraction of this power is dissipated in the chip itself, while most of the power is dissipated in the external drive circuit. The power dissipated in the chip is given by:

$$P_{MDS} = R_{silicon} \cdot I^2 \approx \rho_{el} \cdot \frac{L}{A} \cdot I^2, \quad (6.1)$$

which is approximately 0.1 µW considering $L \approx 4$ mm, $A \approx 1$ mm^2, and the measured current from Figure 5.3. In contrast, a typical shear piezoelectric stack (e.g., Thorlabs, PL5FBP3) routinely used for membrane excitation can dissipate energy given by:

$$P \approx \frac{\pi}{4} \cdot tan\delta \cdot f \cdot C \cdot {V_{pp}}^2, \tag{6.2}$$

where $tan\delta \approx 0.02$ is the dissipation factor, f is the drive frequency, C is the capacitance and V_{pp} represents the Peak-to-peak drive voltage. Considering the same membrane driving voltage and frequency, the dissipated power for a piezo actuator would be approximately 32 μW. Obviously, such comparative analysis is qualitative, since the voltage needed with a piezo actuator depends strongly on the interface between the piezoelectric actuator and a silicon chip. Nevertheless, the fact that the dissipated power values are on the same order of magnitude allows us to expect limited spurious heating from our capacitive actuation scheme.

To experimentally confirm limited chip heating during actuation, we measure the eigenmode frequency shift occurring during the actuation voltage sweeps (see Figure 5.9 – 5.20). Frequency shifts of the eigenmodes (Δf) can be related to the silicon substrate temperature increase using [55]:

$$\Delta T = \frac{2\Delta f \cdot (1 - v)\sigma_{SiN}}{f_0 \cdot E_{Sin} \cdot (\alpha_{Si} - \alpha_{SiN})}\ , \tag{6.3}$$

where f_0 is the original resonance frequency of the mode, $\sigma_{SiN} \approx 100$ MPa is the formation stress of SiN, v is the Poisson ratio for SiN ($v = 0.28$), and α denotes material thermal expansion coefficients ($\alpha_{Si} = 8 \times 10^{-6}\ \mathrm{K}^{-1}$ and $\alpha_{SiN} = 3.7 \times 10^{-6}\ \mathrm{K}^{-1}$). Table 3.1 uses Eqn. (6.3) for calculating temperature changes occurring during measurements. The nickel device definitely has less temperature changes, which can be explained by the lower current flow for the same drive voltage. We note that the aluminum device shows more heating for mode (2, 2) and mode (3, 3). This is consistent with higher actuation voltage (Figure 6.1) and hence higher current flow and dissipation.

Table 6.1 Frequency shifts and temperature changes for nickel layer and aluminum layer with measured six eigenmodes.

Mode	Nickel Layer			Aluminum Layer		
	f_0 [kHz]	Δf [Hz]	ΔT [mK]	f_0 [kHz]	Δf [Hz]	ΔT [mK]
(1,1)	80.03	0.5	0.70	82.82	0.4	0.54
(1,2)	126.65	0.7	0.62	131.05	2.8	2.41
(2,2)	160.20	1.0	0.70	166.00	8.5	5.77
(1,3)	179.09	0.6	0.38	185.42	5.8	3.53
(2,3)	204.14	1.5	0.83	210.43	6.0	3.21
(3,3)	240.15	1.6	0.75	248.13	15.6	7.09

6.4 Harmonic Excitation

We finally observe that harmonic excitation, whereas the voltage excitation signal is at the mode eigenfrequency divided by an integer *n*, can give better results than direct excitation in some cases. This is illustrated by Figure 6.2 (b), where harmonic 2 yields better performances than direct excitation for the Al-pSi assembly. Efficient harmonic excitation is not surprising given the polynomial dependence of the capacitor's energy with the applied voltage (see Eqn. (4.2) for example). A predictive model on the efficiency of harmonic excitation is, however, beyond the scope of this first-observation work.

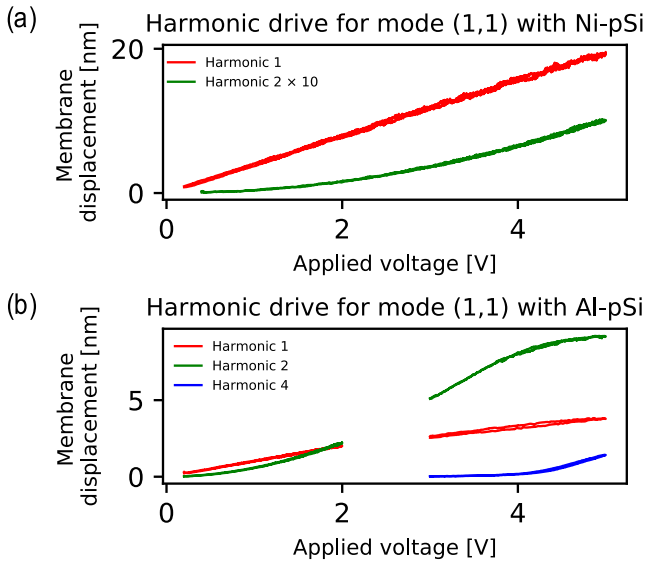

Figure 6.2 (a) Harmonic actuation on the frequency with orders of 1 and 2 for fundamental mode (1, 1) with nickel layer. (b) Harmonic actuation on the frequency with orders of 1,2 and 4 with nickel layer 4 for fundamental mode (1,1) with aluminum layer. In panel (b), the measurements were conducted in two different sweeps (0.2-2 V and 3-5 V) which explain the curve discontinuities.

7. Conclusion

As mentioned earlier in the introduction, the first goal of this work was to develop a repeatable fabrication recipe for silicon nitride (SiN) membrane chips of various membrane sizes. The current survival rate from the latest batch is 86.2%, and the leading cause of failure is imperfect membrane chip manipulation during the last rinse operation. This can be improved by more chip manipulation practice, and by designing more advanced chip holders. The current chip rack for the hot KOH etching is simply made of thin PTFE sheets manually cut and assembled with no other tools than scissors. Based on what we have learned in this work, this equipment can be upgraded to a machined PTFE piece to prevent chips' random movement during the hot KOH etching, and provide safe chip transportation during the rinsing process. Such a holder is currently being designed by our lab.

The second goal of this work—developing an on-chip actuation method—is accomplished with metal-dielectric-semiconductor (MDS) capacitors deposited on the silicon substrate. We have developed first-principle analytical models, which we find are consistent with our experimental observations. As predicted in the modeling section (Chapter 4), the charge accumulation regime (Ni-pSi) is more efficient at membrane resonator actuation than the charge depletion regime (Al-pSi) because the accumulation regime can store more strain energy during each actuation cycle. We also observe limited frequency shifts due to spurious heating during actuation, which confirms that thermal effects are minor, as predicted by our model.

Building an MDS capacitive actuation system on the membrane chip is remarkably simple, which is one of the most significant advantages of our developed technique. Applying metal paste on the

chip frame and connecting it with wires suffices to build the actuation device, providing that the substrate is a semiconductor. It is also effortless to actuate any of the membrane eigenmodes at various amplitudes by adjusting the drive voltage and frequency. In terms of power dissipation, our technique consumes less power than a typical external piezoelectric actuator for the same applied voltage and frequency.

In future work, several unexplored aspects of the work can be investigated. Firstly, higher membrane actuation displacement amplitude could be achieved by increasing the area of the metal electrodes. A larger area leads to higher charge accumulation, meaning more electrical energy can be transduced to mechanical vibrations. Secondly, the distance between two metal electrodes could be investigated. Reducing this distance between the electrodes could decrease the substrate electrical resistance, which would also decrease the power dissipation. Thirdly, the distance between the actuation electrodes and the membrane resonator could be investigated in terms of its influence on the membrane actuation displacement amplitude. We hypothesize that moving the metal electrodes closer to the membrane resonator could reduce the dissipation of the acoustic wave in the chip frame, resulting in higher membrane actuation displacement amplitude. Fourthly, the chip and membrane sizes could be investigated. Smaller frames could potentially confine the acoustic excitation better and allow for stronger actuation. Likewise, acoustic interference effects inside the frame have not yet been considered and likely play a significant role, especially since the acoustic wavelength in silicon is comparable to the chip dimensions at several frequencies of interest. Finally, the mounting method is another variable that could make the membrane resonator perform differently. In this work, chips were mounted with double-sided tape that is known to participate in dissipating mechanical vibrations (i.e., it can lead to Q-factor reductions). A more

rigid mounting (e.g., Crystalbond™ 509 from TED PELLA, Inc) probably can reduce this effect and may have the membrane reach higher Q-factors, meaning higher actuation displacement amplitude.

Appendix A – Interferometer calibration

In Appendix A, the interferometer fringe parking procedure is introduced with extra details as mentioned earlier in subchapter 5.3. It is always necessary to check fringes with optical fiber's location (i.e., the distance between the fiber and the membrane) before any measurement after each setup change. It is also highly recommended to check the fringe for every hour, especially during the vacuum pumping down (i.e., internal pressure change).

The fringe parking procedure relies on one axis moving stage that has an optical fiber attached (see Figure A1). The stage moves the fiber back and forth pointing to the membrane. The motion of the stage is controlled by the picomotor which is connected to a computer controller. The movement of each step of the picomotor is about 25 nm.

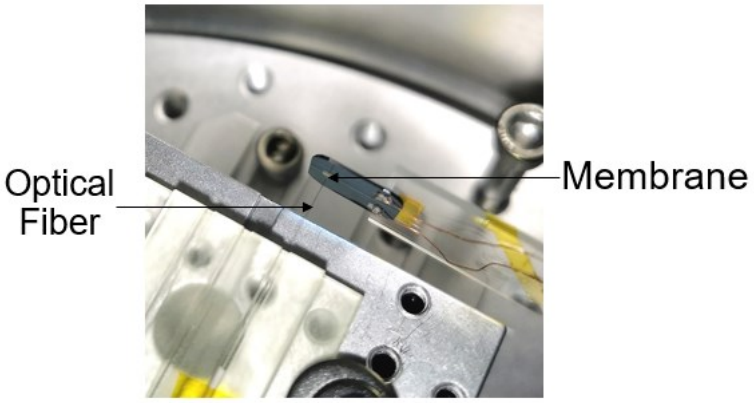

Figure A1 Optical fiber points onto the membrane.

Moving the fiber in one direction, either towards the membrane or away from it, will show a sinusoidal wave as a function of time on the readout screen (see Figure A2). In the meantime, the maximum and minimum fringes in voltage are shown at the right side of the sinusoidal curve. The difference between these two extreme fringe values is determined by the distance between the fiber

and the membrane. The difference gets larger when the distance is closer which means more reflected light from the membrane can be received by the optical readout system. However, the fiber cannot reach the membrane too close which can increase the risk of touching and damaging the membrane. In assumption, every equipment in the vacuum chamber is mounted stably. Nevertheless, some minor movements in nm can frequently happen. Therefore, we cannot to pursuing the maximum strength of the reflected light input by risking the membrane. This is a tradeoff between them. So, the target distance between the fiber and the membrane is to let the minimum fringe reach 5 mV or slightly below. In this circumstance, the distance is at a balanced point between the safety of the membrane and the strength of the reflected light for the readout system.

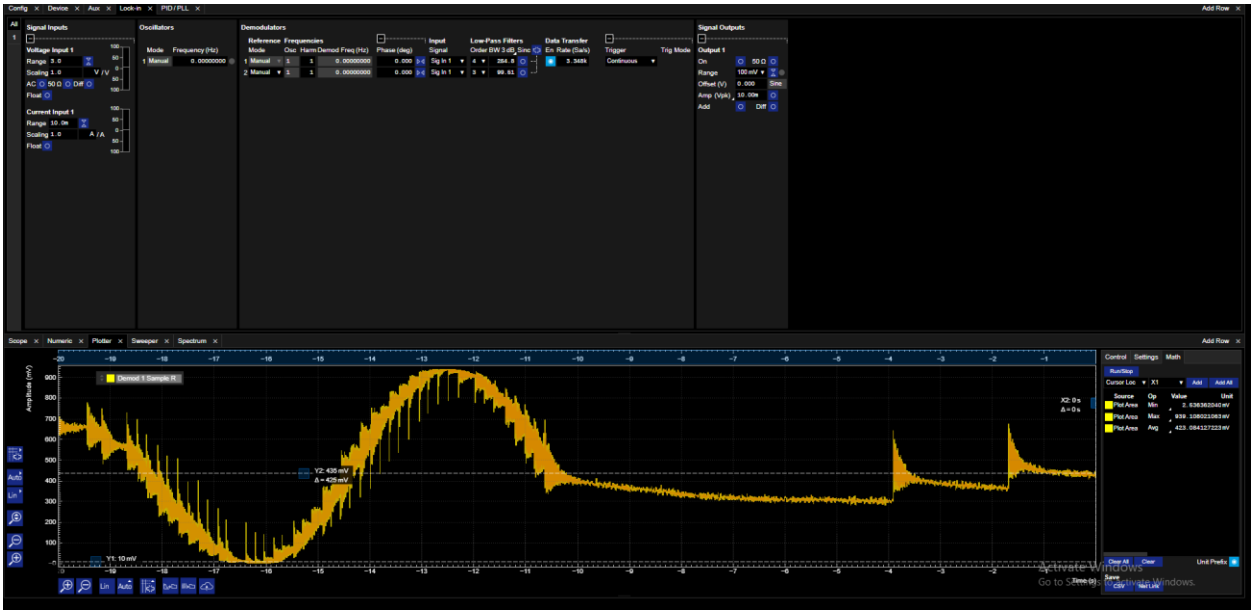

Figure A2 Readout signal curve as a function of time during fringe adjustment with optical fiber moving.

After roughly locating the fiber location, the readout signal should stay at the middle between maximum and minimum fringes to achieve the highest sensitivity for detecting the membrane displacement. This can be accomplished by moving the fiber backward with a proper number of steps with the picomotor controller.

Appendix B – Membrane metallization results

During the actuation model development, we went through several other models. There is one actuation model that is tested multiple times and has a particular shadow mask mounting procedure developed accordingly. This mounting procedure is presented in this chapter with details.

This model requires metal deposition on the membrane. Figure B1 shows one sample of the shadow mask made from ____ sheet metal by laser machining (i.e., the laser machining process can be found in subchapter 3.2.). The feature on the mask has two hollow paths from square pads location to the membrane. After the metal deposition in the evaporator, the deposited metal electrodes on the membrane can be found in Figure B2. The geometry of these electrodes is designed precisely with calculations. Therefore, it is important to duplicate the pattern precisely from the mask (see Figure B3) to the membrane. This requires direct contact between the mask the membrane which means the mounting has to be stable the whole time. The rest of this chapter describes the mounting procedure in detail.

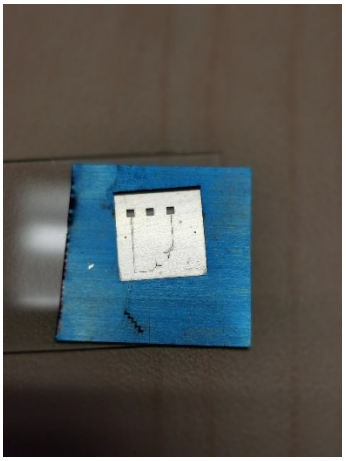

Figure B1 Shadow mask laser machined from blue tempered high carbon steel shim. Silver color is due to aluminum deposition in the evaporator.

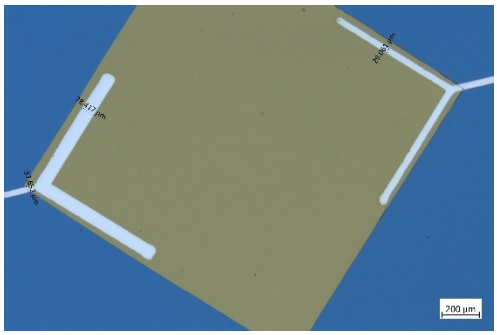

Figure B2 Image of aluminum deposition for electrodes on membrane under the microscope.

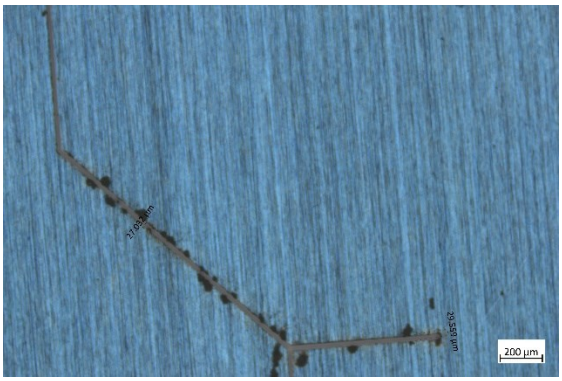

Figure B3 Image of shadow mask feature machined by laser under the microscope.

In order to do the mask-chip mounting with crystal bond, we designed the alignment stage shown in Figure B4. The membrane chip is placed with the membrane side facing downward. The chip frame is mounted on the rack with double-sided tape. The size of the tape should be minimized to avoid the difficulty of detaching afterward. The chip is mounted onto the Z-axis rack which is connected to the H-axis stage on the 1-inch post rod. The H-axis stage gives a rough location of height for the chip. Precise height is adjusted with Z-axis stage by the hand screw. The shadow mask is manipulated with the stage combination (i.e., X-axis, Y-axis and θ-axis) below. Since our features are relatively small (i.e., in μm), it requires a microscope for a better view. The Microscope in the Figure B4 can connect with a computer and show the live video in VLC media player (see Figure B5). To get a better resolution, the microscope is moveable with the adjustable

rack. This whole alignment stage is basically a sample version of the mask aligner in the cleanroom. Relevant experience of the mask aligner is an asset to this setup. Practice on a dummy chip without the heater in Figure B6 is highly recommended.

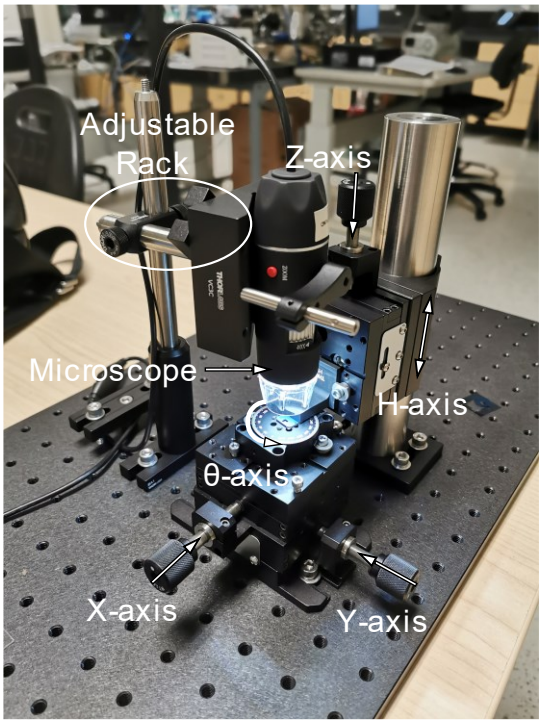

Figure B4 Stage for mask-chip alignment.

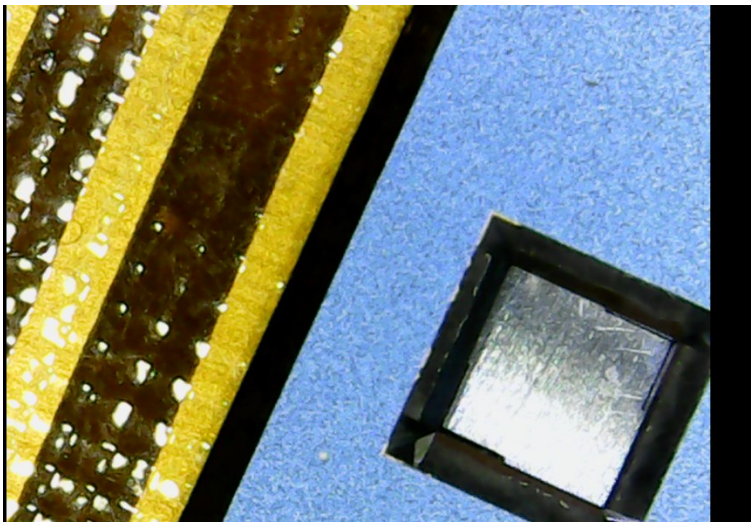

Figure B5 Screenshot from VLC media player during mask-chip alignment.

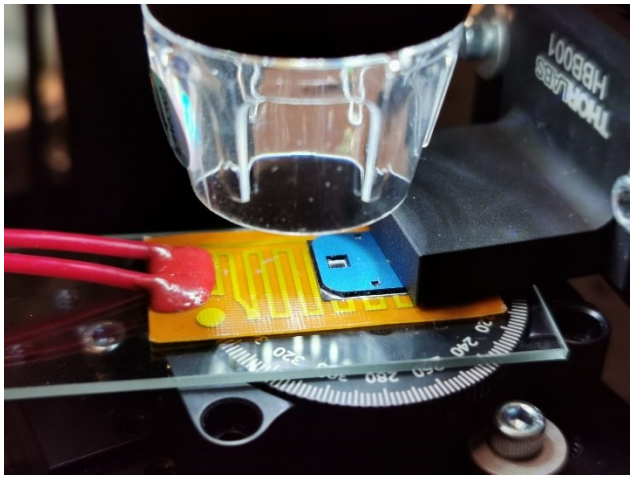

Figure B6 The chip is aligned with the shadow mask with the pad heater underneath.

After the mask-chip alignment, the crystal bond has to be melted and recrystallized to connect them. This requires a heat source. The regular lab hot plate is way too large for this mission. Therefore, a flat electrical pad heater (see Figure B6) is induced to provide the heat to melt the crystal bond with a power supply (see Figure B7). The pad heat has 3M tape on one side which can be placed on a glass slide. The glass slide is mounted onto the θ-axis stage with double-sided tape. The alignment is done with the mask on the heater. After the alignment, gently press down the chip with the Z-axis stage to let the chip contact with the mask and avoid breaking the membrane (i.e., require patience). The operator should feel the tension from the screw on the Z-axis stage when the chip is fully attached to the mask. During the chip pressing down, it is possible that the mask moves. Therefore, it requires another alignment operation if mask movement happens.

Figure B7 The power supply for the pad heater to melt the crystal bond piece. The current and the voltage should be set as shown in the picture for melting the crystal bond.

Before turning on the heater, it is recommended that crack the crystal bond rod into small pieces that can be manipulated with the tweezer. To melt the crystal piece, the power supply is gradually raised to a certain power level found in Figure B7. Then, use a tweezer to gently press the crystal piece onto the two outer corners of the chip (see Figure B8). The amount of melted crystal bond requires a bit of control without too much excess. The excessive crystal is able to flow off from the mask and bond the mask to the heater after cooling down. This can increase the difficulty of detaching the mask-chip combination from the heater. When lifting the rest crystal piece up, try to avoid the wiredrawing from the melted crystal. This could contaminate the membrane or even break it.

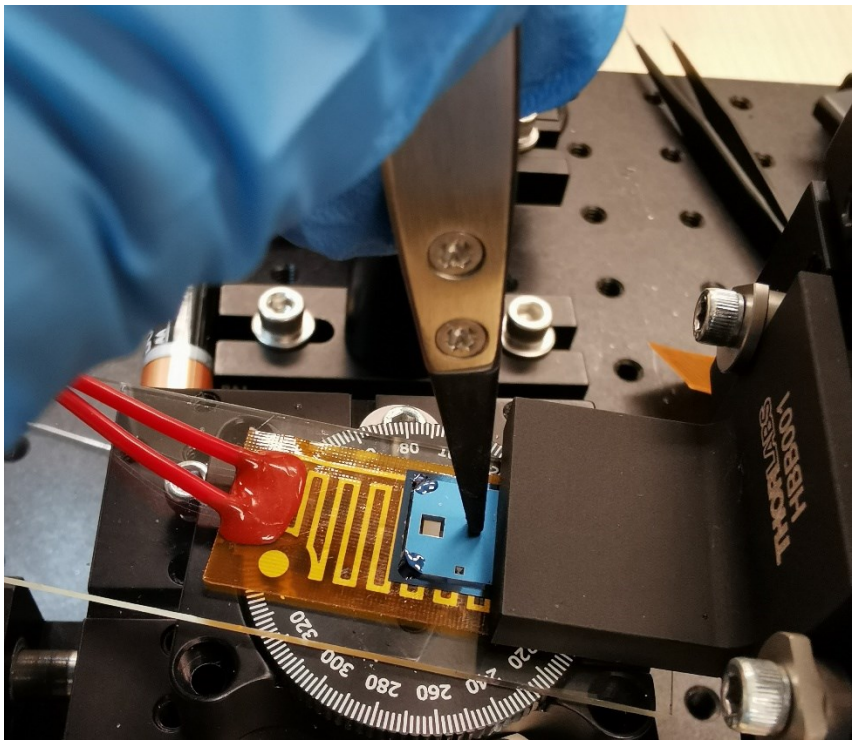

Figure B8 Use a soft tip tweezer to help detach the chip from the black bracket. The picture also shows the location of crystal bond mounting points.

After cooling down, the Figure B8 also shows the way to use a soft tip tweezer to gently press on the chip frame and lift up the Z-axis stage (i.e., about half turn on the crew). As long as the chip frame is detached from the black bracket, release the tweezer and move it away (see Figure B9).

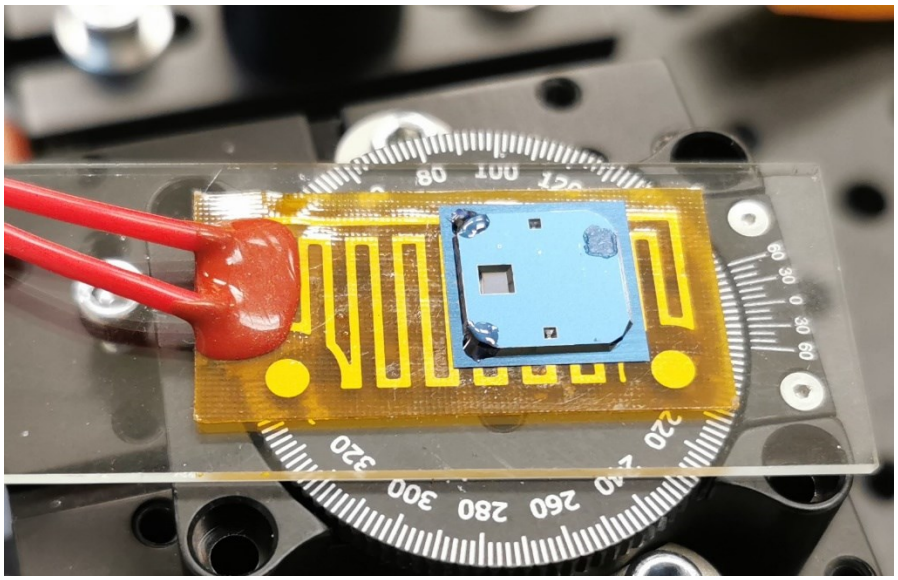

Figure B9 Completely detach the chip from the Z-axis stage.

The mask could be sticky with the heater. Insert a piece of sheet metal underneath the mask to separate it from the heater (see Figure B10). Then, use a soft tip tweezer carefully transfer the sample from the stage to a glass slide with double-sided tape mounting (see Figure B11). Eventually, the sample is ready for metal deposition.

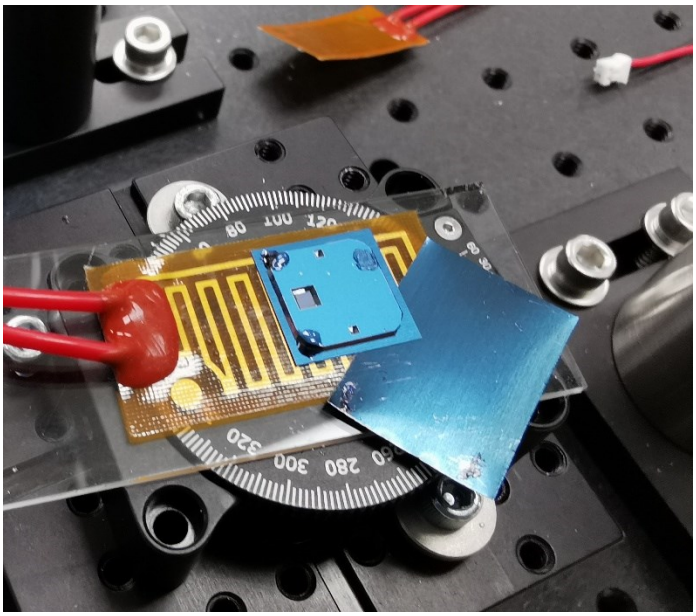

Figure B10 Illustration of detaching the mask from the heater with a piece of metal shim if the mask is stuck on the heater.

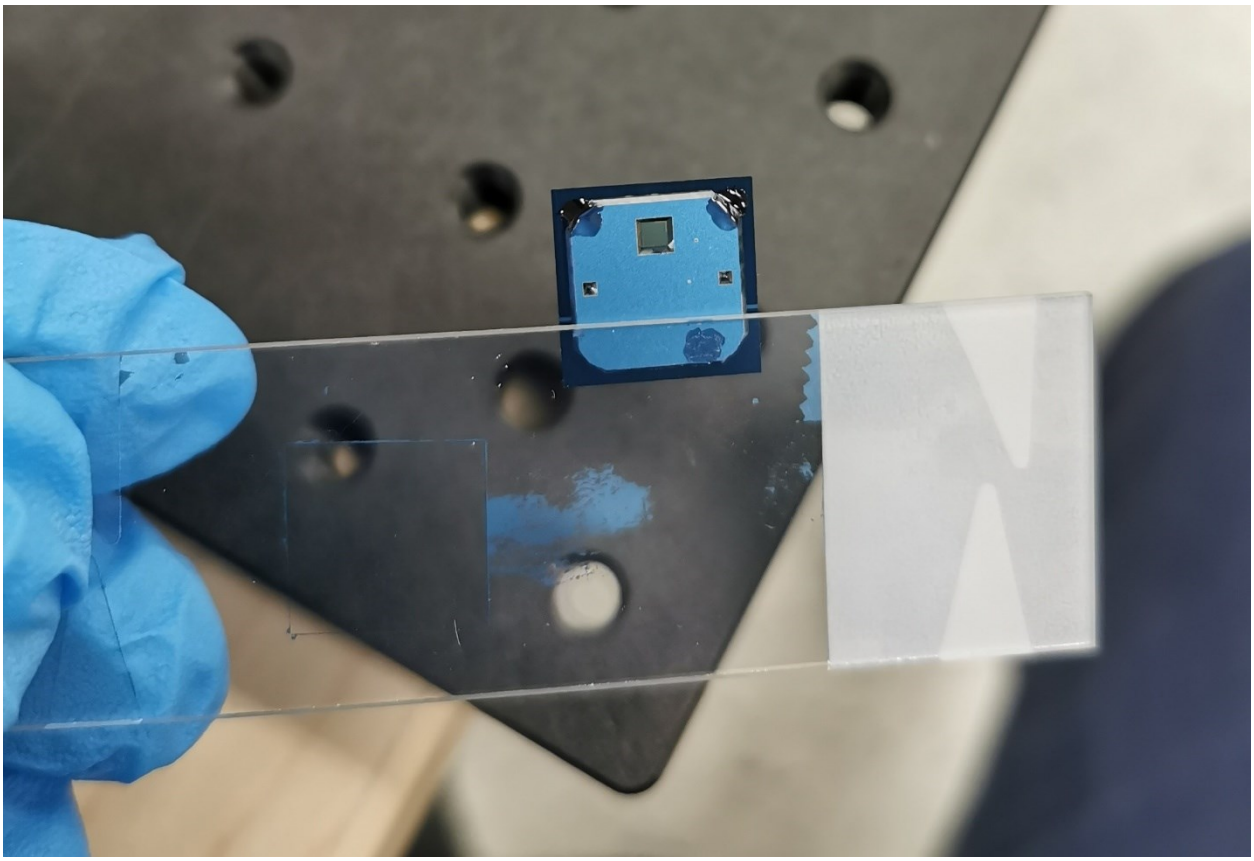

Figure B11 Sample mounted on the glass slide is ready for metal deposition.

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