Signal and Noise Time-domain Models for Microwave FETs

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Abstract

Accurate characterization of active devices is one of the most crucial steps in efficient microwave circuit design. As the operating frequency increases, the dimensions of the electrodes of microwave transistors such as FETs become comparable to the wavelength, highlighting the parasitic effect of wave propagation and phase cancellation. Thus, this effect needs to be accurately evaluated in the device model to assure a reliable design.

In this work, we proposed new small- and large-signal FET models for efficient millimeter-wave circuit design. In our approach, the device width was divided into an infinity number of segments, while each segment was considered as a combination of three coupled lines and a conventional FET equivalent circuit. By solving a set of multi-conductor transmission line equations using the Finite-Difference Time-Domain (FDTD) technique, an accurate and efficient transistor modeling approach has been introduced.

Furthermore, a new distributed noise FET model was proposed. It consists in a three- coupled excited transmission line (TL) structure in which the Laplace transformation was applied to determine the noise currents and voltages of lines. The structure was also analyzed by applying the Green's function concept as a wave approach. The proposed distributed mm-wave noise FET model has been demonstrated through successful comparison with measurements

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List of Acronyms

CAD	Computer Aided Design
CPU	Central Processing Unit
DUT	Device Under Test
FET	Field Effect Transistor
FDTD	The Finite Difference Time Domain
FIT	Finite Integration Technique
GaAs	Gallium Arsenide
GHz	Giga Hertz
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HP	Hewlett Packard
InP	Indium Phosphide
JAC	Jacobian Matrix
K	Rollet Stability Factor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuits
MSG	Maximum Stable Gain
NF	Noise Figure
NEC	Nippon Electronic Corporation
RF	Radio Frequency
Si	Silicon
TL	Transmission Line
VLSI	Very Large Scale Integration

List of Symbols

A	Internal resistance
A_0	Curtice model parameter
a_1	incident wave for port 1
A_1	Curtice model parameter
a_2	Incident wave for port 2
A_2	Curtice model parameter
A_3	Curtice model parameter
α	Curtice model parameter
B	Internal Inductance
β	Curtice model parameter
$CA_{U.P.L}$	The unit-per-length noise correlation matrix of the FET
C_{Yl}	Admittance correlation matrix of the FET
C_{ds}	The drain-to-source capacitance of the FET
C_{gd}	The gate-to-drain capacitance of the FET
C_{gs}	The gate-to-source capacitance of the FET
C_{pds}	The parasitic drain-to-source capacitance of the FET
C_{pgs}	The parasitic gate-to-source capacitance of the FET
D	Drain terminal for the field effect transistor
D_{gd}	Gate-to-Drain diode
D_{gs}	Gate-to-Source diode
F_c	Curtice parameter
F_{min}	Minimum noise figure
G	Gate terminal for the field effect transistor
G_m	Channel transconductance
G_{ds}	Drain to source conductance
γ	Curtice model parameter

g_{ds}	The output conductance of the field effect transistor
g_m	The transconductance of the field effect transistor
I_{ds}	The DC drain-to-source current of the field effect transistor
I_{ds0}	The DC component of the drain-to-source current
I_{ds}	The radio-frequency component of the drain-to-source current
I_{dss}	Zero-gate saturation drain current
j_n	Noise equivalent current source
L	Gate length of the field effect transistor
λ	Curtice model parameter
L_{dd}	The drain inductance of the field effect transistor
L_{gg}	The gate inductance of the field effect transistor
L_{pdk}	Drain packaging inductance
L_{pgk}	Gate packaging inductance
L_{ss}	The source inductance of the field effect transistor
M_{gd}	Mutual inductances between drain and gate
M_{gs}	Mutual inductances between source and gate
M_{ds}	Mutual inductances between source and drain
Q_{gs}	The gate-to-source stored charge
R_d	The drain resistance of the field effect transistor
R_{ds}	The output resistance of the field effect transistor
R_{gg}	The gate resistance of the field effect transistor
R_i	The channel resistance of the field effect transistor
R_{ss}	The gate resistance of the field effect transistor
S	Source terminal for the field effect transistor
S	Laplace transformation
S_v	Voltage eigen value vector
S_i	Current eigen value vector
σ	Electrical conductivity

T	Temperature in degrees Celsius
τ	The transconductance delay
v_n	Noise equivalent voltage source
v_p	Pinch-off voltage
V_{bi}	Built-in potential of the Schottky gate
V_{ds}	The DC drain-to-source voltage of the field effect transistor
v_{ds}	Pulsed drain-to-source voltage amplitude
V_{ds0}	Drain-to-source model at model evaluation point
V_{gs}	The DC gate-to-source voltage of the field effect transistor
ε_r	Relative dielectric permittivity
V_{TO}	Curtice model threshold voltage
ω	The angular frequency
W	Gate width for the field effect transistor
Y	The admittance matrix
Z	The impedance matrix
γ	Propagation constant
Γ	Matrix of eigenvalues of propagation constant

Chapter 1 Introduction

1.1 Motivation

In this century of communication, microwave integrated circuits constitute the key elements of a wide range of microwave and millimeter-wave communication systems. Their technology can be said to be in its third “era”: in the first era, the GaAs metal Semiconductor Field Effect Transistors (MESFET) were extensively used and many key design techniques were pioneered. In the second era, heterojunction devices like High Electron Mobility Transistors (HEMTs) were improved rapidly and enabled circuits to operate over 100GHz, with new performance benchmarks being set at nearly every workshop and conference. In the third era, HEMT technology has matured and Monolithic Microwave Integrated Circuits (MMICs) operating above 100GHz have become standard products [1]-[4].

Such devices are based on a large number of closely packed passive and active structures, transmission lines, and discontinuities operating at high speeds and frequencies and sometimes over very broad bandwidths. It is thus anticipated that the design of MMICs should involve powerful design tools especially in the upper part of the microwave frequency spectrum where electromagnetic-based parasitic effects can significantly affect the circuit performance. [5]- [7]

Indeed, in the millimeter-wave range, integrated circuit design encounters the severe problem of dealing with non-negligible electromagnetic effects like undesired radiation and parasitic coupling between circuit elements. Such complex effects require a full-wave approach to accurately analyze them. This implies solving Maxwell’s equations and taking into account the interaction between parasitic electromagnetic waves and circuit elements comprehensively. Since this interaction can affect the overall system performance, the entire system needs to be characterized as a whole package by a full- wave analysis incorporating all devices, particularly transistors like MESFETs and HEMTs, which are the core of modern communication systems.

Indeed, as the operating frequency of a FET increases to the millimetre-wave range, the physical dimensions of the electrodes become comparable to the wavelength [8]. As a consequence, the impedance at the input of the device electrode becomes different from that at the output side of the electrode [9]. Thus, the electrodes of the device exhibit different phase velocities for input and output signals and then affect the overall performance of the device because of this mismatch in phase velocities. This forces millimetre-wave designers to carefully consider wave propagation effects in any modeling approach, which globally excludes lumped-equivalent circuit representations of FETs in favour of distributed-equivalent circuit models. Conventional modeling approaches based on lumped-equivalent circuits may also be inappropriate for the following reasons:

- Distributed effects and coupling phenomena occurring at very high frequencies may strongly affect the transistor performance. Such behaviour cannot be easily described by standard lumped parasitic elements [1]–[3]. Either distributed effects should be taken into account in the device model or rather complicated equivalent circuit structures have to be considered [4]–[18].
- Parameters of lumped equivalent circuits are usually scaled with device size and finger number according to different approaches from very simple linear rules to completely empirical algorithms [19]–[21]. Some of these approaches may not be sufficiently accurate at relatively high operating frequencies, and a large number of measurements on different device structures could be needed to obtain a good scalable model. Particular care must be paid in any case to parasitic network modeling and characterization.

The possibility of achieving this type of modeling should be then addressed by full-wave device analysis and global circuit modeling as presented in [10]–[13]. The full- wave analysis involves a fair amount of advanced numerical techniques and different algorithms that results in a very expensive computational cost [14]. Although, some numerical methods have been recently proposed to reduce the simulation time [15]–[16], they are still perfectible, leaving open the door to other approaches that might be easier to implement as computer aided design (CAD) routines in commercial circuit simulators.

Among existing transistor models developed for millimetre-wave applications, we can mention the so-called semi-distributed models (S.D. models) [17]-[19]. In these models, with the assumption of a quasi-transverse electromagnetic (TEM) approximation, the device can be divided into N numbers of cascaded cells, each cell being represented by the lumped-equivalent circuit model discussed above [18], [19]. The value of N is related to the device size and the operating frequency, thus, to keep the ratio $W/N.\lambda$ small (less than "few percent" as stated in [17]). Here, W is the transistor gate-width and λ the propagation wavelength. However, these semi-distributed models have some limitations. In fact, by increasing the frequency, they cannot precisely take into account the wave propagation effect and phase cancellation phenomena in the overall device performance since the core of the model is still based on lumped elements. Therefore, to achieve accurate results in high-frequency applications, one needs to develop a more general distributed model.

Indeed, to overcome these limitations, we have introduced for the first time the concept of a new distributed FET model. In the proposed approach, each infinitesimal segment of the model was divided into two parts namely, active and passive, whose elements are all per unit length. The passive part describes the behaviour of the transistor as a set of three coupled lines while the active part relates to a distributed equivalent circuit [19]; in time-domain, this approach leads to a set of differential equations that should be solved to fully characterize the model.

However, merging both transmission lines and distributed equivalent circuit in one model can significantly increase its complexity, and therefore, the time required to characterize it (i.e., solving the equations that describe the model behavior). In fact, in one side, compared to both lumped and semi-distributed models, the proposed approach is expected to significantly increase the transistor model accuracy. However, on the other side, the CPU time required to analyze this model could be huge, affecting its efficiency as transistor model for circuit design and optimization. Therefore, the method to be used to solve the set of differential equations should be adequately selected.

As one of the most efficient discretization techniques, the lumped segmentation approach (also called the transmission line method) was selected to analyze each infinitesimal segment of the proposed model [20]-[24].

Then, to numerically obtain the model element values, the Finite Difference Time Domain (FDTD) method was preferred. In fact, this method is widely used in solving various kinds of electromagnetic problems, wherein lossy, nonlinear, and inhomogeneous media and transient problem can be considered [25]-[27].

By applying this modeling technique, the scattering parameters of a sub micrometer-gate FET transistor were obtained. The results were compared with those obtained by the lumped model and as expected, the proposed model reacts better than the lumped model at the upper side of the frequency spectrum.

We also introduced a three-coupled Transmission Line (TL) structure as a new noise model of the FET. There, the Laplace transformation was applied as a circuit model to determine the noise performance of the transistor device. Then we introduced a wave approach, relying on the Green's function concept, to analyze the model. Some noise parameters of the transistor were plotted to prove reliability and ability of our proposed model in noise analysis of microwave FETs.

1.2 Contribution Overview

The major contributions of this work expected from the successful fulfillment of the research objectives are listed below:

1. A novel and accurate small-signal modeling procedure for microwave FETs as active coupled transmission lines is presented; this linear distributed model considers the effect of wave propagation along the device electrodes. In this modeling technique, the active multiconductor transmission line equations are obtained, which satisfy the TEM wave propagation along the FET electrodes. This modeling procedure was applied to FETs by solving the equations using Finite-Difference Time-Domain (FDTD) technique. [18], [19]-[28], [30]-[31].
2. A novel and efficient large-signal modeling approach for microwave FETs as nonlinear active transmission lines is also presented. The nonlinear active multiconductor transmission line equations are obtained by considering the transistor as three active coupled lines operating in a nonlinear regime. [25], [35]-[36].

3. A new noise model of FET is proposed. The three coupled transmission line structure is analyzed by applying the Green's function concept as a wave approach. Then, noise performance of the device is compared with the lumped model and the well- known lumped equivalent circuit model. [29], [32]-[34].

Beside the above points, the proposed method allows the computation of the complete matrix of the device and a fast evaluation of the effects of scaling and of different topological choices: the model is thus suitable for implementation as a computer-aided-design (CAD) package for MMIC design. This technique has been successfully applied to the modeling of several FET families and topologies.

1.3. Thesis Outline

The research work presented in this thesis is, therefore, sectioned as follows. Chapter 1 describes the issues to be addressed and the motivation behind different methods of FET analysis. The state of art of the new method is briefly reviewed.

Chapter 2 gives an overview of the numerical methods have been used in order to analyze noise and signal of FETs. Also, an accurate modeling procedure for FETs is presented and applied to a FET by solving the equations based on three active coupled transmission lines using the Finite-Difference Time-Domain (FDTD) technique.

We introduce a nonlinear active multi-conductor transmission line equation using the new wave model by considering the distributed effect of the source electrode in chapter 3. These equations can accurately predict the behavior of microwave/millimeter wave transistors in a nonlinear regime. The FDTD technique was used to solve these nonlinear equations in the time domain. This modeling approach is applied to a FET and the results were compared to lumped model.

Chapter 4 builds up to a noise model. The proposed model is derived and discussed in this chapter. There we applied the Laplace transformation to determine the noise currents and voltages of lines. Here the structure is analyzed by applying the Green's function concept as a wave approach. The details of the approach and some important results will be presented in the following sections of this chapter.

In chapter 5 the proposed small- and large-signal models were incorporated into commercial simulators to design a wideband distributed low-noise amplifier and an E-band power amplifier, respectively. The results have been successfully compared to those ones obtained from lumped model analysis and/or to measurements.

Chapter 6 presents a thesis summary, conclusions and recommendations for future research works

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Chapter 2 Linear FET Modeling and Analysis

2.1 Introduction

Accurate characterization of active devices is one of the most important steps in efficient microwave circuit analysis. As the operating frequency increases, the dimensions of the electrodes of microwave transistors such as FETs become comparable to the wavelength, highlighting the parasitic effect of wave propagation. Thus, this effect needs to be accurately evaluated in the device model to assure a reliable design. Full wave analysis and global modeling approaches can be used to consider the wave propagation effect along the device structure [1]. However, this type of analysis necessitates a huge CPU time. Although some numerical methods have been recently proposed for simulation time reduction [2], it sounds that this analysis approach needs more attention for efficient implementation in simulation software. On the other hand, active device behavior in high frequencies can be described using semi-distributed (S.D) model easily implementable in CAD routines of simulators [3]-[5]. However, by increasing the frequency, this model cannot precisely model the wave propagation effect and phase cancellation phenomena on the electrical performance. Therefore, to achieve more accurate design in millimeter-wave applications, one needs to develop a more advanced distributed model. Thus, a new approach should be proposed to take into account the fact that when the active device physical dimensions become comparable to the wavelength, the input active transmission line, e.g., the gate electrode in common- source FETs, will exhibit a different reactance from the output transmission line, e.g., the drain electrode. Therefore, input and output signals will have different phase velocities, affecting the performance of the device due to the phase velocity mismatching [6], [7]. In other words, since wave propagation effect influences the electrical performance of the device, this phenomenon needs to be accurately considered in device modeling.

In this work, we proposed a new modeling approach for FETs that considers the effect of wave propagation along the device electrodes. In our model, the device width has been divided into an infinity number of segments, while each segment is considered as a

combination of three coupled lines and a conventional FET equivalent circuit. Therefore, the transmission line theory can be applied to each segment of the transistor electrode. Then, the obtained system of differential equations has to be solved. Since a time-domain analytical solution does not exist for this kind of system, a numerical solution should be considered. The Finite Difference Time Domain (FDTD) method is widely used in solving various kinds of electromagnetic problems, wherein lossy, nonlinear, inhomogeneous media and/or transient problems are considered [8]-[10]. This technique was then retained to solve the obtained equations.

2.2 Small-signal Equivalent Circuit Model

A small-signal model will be used in determining the FET linear model. Device small-signal modeling has been covered extensively in the literature [11]–[17]. The model used in this work is superimposed on the cross section of a FET as in Fig.2.1. The parameters are bias-dependent but frequency independent.

Fig.2.1. Device small-signal model on a cross section of a FET

At the heart of the model are the gate-source capacitance, C_{gs}, and the transconductance, G_m (with $G_m = G_{m0}\, e^{j\omega\tau}$). The phase associated with G_m, $\omega\tau$, is a necessary

delay that accounts for channel charge to redistribute after a change in gate voltage. The drain-source resistance, R_{ds}, is a measure of how effectively a signal can be extracted from the device. This is because it will reduce the effective load of the device.

R_i is regarded as the physical channel resistance or the charging resistance for C_{gs}. Because it is hard to extract separately from the gate resistance, R_{gg}, the two are sometimes lumped together. The gate-drain capacitance, C_{gd}, is setup by the space charge region between gate and drain, similar to C_{gs}, but typically an order of magnitude smaller. It introduces a bothersome feedback, which reduces the high-frequency performance of the device. The gate-drain resistance, R_{gd}, is also argued as a charging resistance for C_{gd}. Any capacitance between the drain and source, which will be very small, is accounted for with C_{ds}. The parameters C_{gs}, G_m, R_i, R_{ds}, R_{gd}, C_{gd}, and C_{ds} taken together are referred to as the *intrinsic* elements of the device. The other elements of the model are side effects of having to provide physical connections to the device and the parasitic and distributed effects that occur when operating at frequencies in the GHz range. These parasitic elements are called the *extrinsic* elements of the device.

The drain and source resistances, R_d and R_s, come from physical processes. The source is the nonideal ohmic contact behavior between the metal pads and the semiconductor. These resistances scale directly with the device width. Because the gate length is short, the resistances of the gate metals contribute to R_{gg}. From an ac viewpoint, the signal decays as it propagates along the length of the gate resistance. A distributed model argument shows this resistance to be approximately 1/3 of its dc value [14]. All of these resistances generate thermal noise. R_s and R_{gg} will be important for modeling the noise figure as seen later. Because R_d is at the output, and its magnitude of noise is far smaller than the channel noise, it can be usually ignored. [15].

The drain, gate, and source inductances, L_{dd}, L_{gg}, and L_{ss}, respectively, account for signal delay along the various contact pads. L_{gg} is usually the largest, and will affect any input match (noise or power) to the device. Finally, there are various pad capacitances between their respective device terminals: C_{GS}, C_{GD}, and C_{DS}. C_{GS} and C_{GD} are small, while C_{DS} for devices used in this work is of the same order as C_{GD} [18].

2.3 Model Identification

As shown in Fig.2.2, a FET can be modeled as a set of three coupled electrodes where M_{ds}, M_{gd}, and M_{gs} represent the mutual inductances between drain-source, gate-drain and gate-source, respectively. So, the transmission line properties of the electrodes need to be investigated to evaluate the effect of wave propagation along them [6], [7]. To derive the instantaneous voltage-current relationships in the transistor, we consider an element portion of length of a three-active transmission line network. We intend to find an equivalent circuit for this line and derive the transistor equations. An equivalent circuit of an infinitely small segment of the transistor is shown in Fig.2.2. In this figure, the segment is represented by a 6-port equivalent circuit, which combines a conventional FET small signal circuit model with a distributed network to account the coupled transmission line effect of the electrode structure where the all parameters are per unit length.

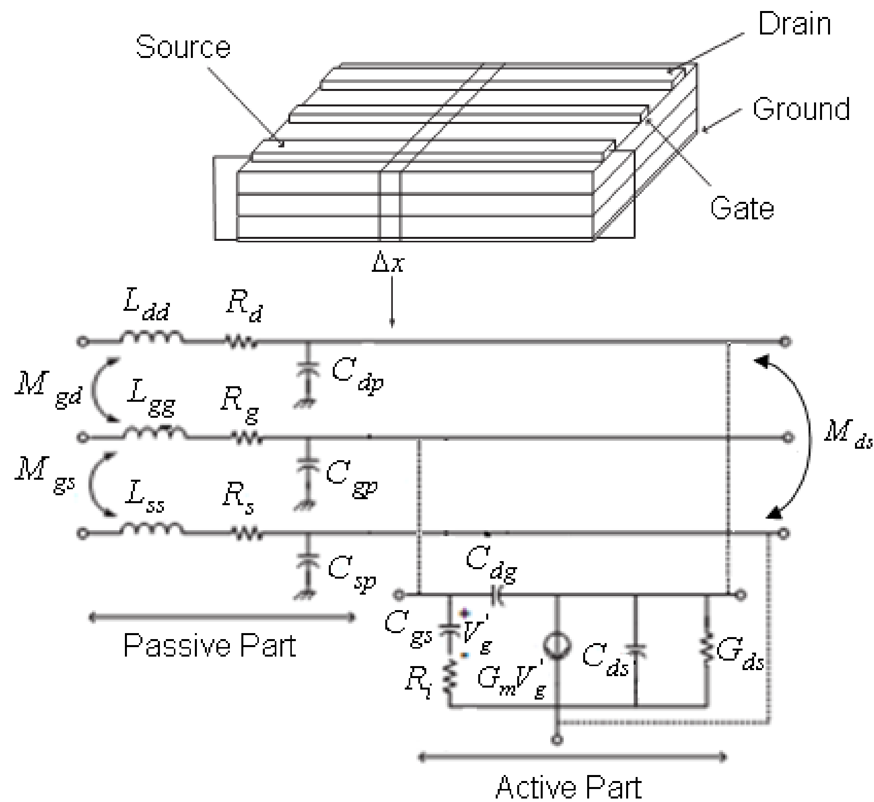

Fig.2.2. The different parts of a segment in the distributed model (with linear model for the active part)

By applying Kirchhoff's laws to the conventional FET circuit of Fig.2.2, we obtain the following equations

$$I_d(x+\Delta x,t)+C_{11}\Delta x\frac{\partial V_d(x+\Delta x,t)}{\partial t}-C_{12}\Delta x\frac{\partial V_g(x+\Delta x,t)}{\partial t}-C_{13}\Delta x\frac{\partial V_s(x+\Delta x,t)}{\partial t}$$
$$+G_m\Delta xV'_g(x,t)+G_{ds}\Delta x(V_d(x,t)-V_s(x,t))=I_d(x,t) \quad (2\text{-}1)$$

$$V_d(x+\Delta x,t)+R_d\Delta xI_d(x,t)+L_{dd}\Delta x\frac{\partial I_d(x,t)}{\partial t}+M_{gd}\Delta x\frac{\partial I_g(x,t)}{\partial t}+M_{ds}\Delta x\frac{\partial I_s(x,t)}{\partial t}=V_d(x,t)$$
$$(2\text{-}2)$$

Setting $\Delta x\to 0$, we obtain [6]

$$\frac{\partial I_d(x,t)}{\partial x}+C_{11}\frac{\partial V_d(x,t)}{\partial t}-C_{12}\frac{\partial V_g(x,t)}{\partial t}-C_{13}\frac{\partial V_s(x,t)}{\partial t}+G_mV'_g(x,t)+G_{ds}(V_d(x,t)-V_s(x,t))=0$$
$$\frac{\partial V_d(x,t)}{\partial x}+R_dI_d(x,t)+L_{dd}\frac{\partial I_d(x,t)}{\partial t}+M_{gd}\frac{\partial I_g(x,t)}{\partial t}+M_{ds}\frac{\partial I_s(x,t)}{\partial t}=0 \quad (2\text{-}3)$$

By applying the same procedure, we get similar equations for gate and source electrodes

$$\frac{\partial I_g(x,t)}{\partial x}+C_{22}\frac{\partial V_g(x,t)}{\partial t}-C_{12}\frac{\partial V_d(x,t)}{\partial t}+C_{gs}\frac{\partial V'_g(x,t)}{\partial t}=0 \quad (2\text{-}4)$$

$$\frac{\partial V_g(x,t)}{\partial x}+R_gI_g(x,t)+L_{gg}\frac{\partial I_g(x,t)}{\partial t}+M_{gd}\frac{\partial I_d(x,t)}{\partial t}+M_{gs}\frac{\partial I_s(x,t)}{\partial t}=0 \quad (2\text{-}5)$$

$$\frac{\partial I_s(x,t)}{\partial x}+C_{33}\frac{\partial V_s(x,t)}{\partial t}-C_{13}\frac{\partial V_d(x,t)}{\partial t}-C_{gs}\frac{\partial V'_g(x,t)}{\partial t}-G_mV'_g(x,t)$$
$$+G_{ds}(V_s(x,t)-V_d(x,t))=0 \quad (2\text{-}6)$$

$$\frac{\partial V_s(x,t)}{\partial x}+R_sI_s(x,t)+L_{ss}\frac{\partial I_s(x,t)}{\partial t}+M_{ds}\frac{\partial I_d(x,t)}{\partial t}+M_{gs}\frac{\partial I_g(x,t)}{\partial t}=0 \quad (2\text{-}7)$$

Also, the gate-source loop leads to another equation, which could be written as

$$V'_g(x,t)+V_s(x,t)+R_iC_{gs}\frac{\partial V'_g(x,t)}{\partial t}-V_g(x,t)=0 \quad (2\text{-}8)$$

where

$C_{11} = C_{dp} + C_{ds} + C_{dg}$ $\quad$ $C_{22} = C_{dp} + C_{dg}$ $\quad$ $C_{33} = C_{sp} + C_{ds}$

$C_{12} = C_{dg}$ $\quad$ $C_{13} = C_{ds}$

Then, the above equations could be reformatted into two matrix equations

$$\frac{\partial}{\partial x}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \\ 0 \end{bmatrix} + \frac{\partial}{\partial t}\begin{bmatrix} C_{11} & -C_{12} & -C_{13} & 0 \\ -C_{12} & C_{22} & 0 & C_{gs} \\ -C_{13} & 0 & C_{33} & -C_{gs} \\ 0 & 0 & 0 & R_i C_{gs} \end{bmatrix}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V_g'(x,t) \end{bmatrix} + \begin{bmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{bmatrix}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V_g'(x,t) \end{bmatrix} = 0 \tag{2-9}$$

$$\frac{\partial}{\partial x}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \end{bmatrix} + \frac{\partial}{\partial t}\begin{bmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{bmatrix}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{bmatrix} + \begin{bmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{bmatrix}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{bmatrix} = 0 \tag{2-10}$$

where V_d, V_g, and V_s, are the drain, gate and source voltages, respectively, V'_g is the voltage across gate-source capacitor, while I_d, I_g, and I_s are the drain, gate and source currents, respectively. These variables are time-dependent and function of the position x along the device width.

The proposed FET model is embodied in the linear equations

$$\frac{\partial}{\partial x}[\mathrm{I}'(x,t)] + [\mathrm{C}]\frac{\partial}{\partial t}[\mathrm{V}'(x,t)] + [\mathrm{G}][\mathrm{V}'(x,t)] = 0 \tag{2-11a}$$

$$\frac{\partial}{\partial x}[\mathrm{V}(x,t)] + [\mathrm{L}]\frac{\partial}{\partial t}[\mathrm{I}(x,t)] + [\mathrm{R}][\mathrm{I}(x,t)] = 0 \tag{2-11b}$$

with

$$[\mathrm{I}'(x,\mathrm{t})] = \begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \\ 0 \end{bmatrix} \quad [\mathrm{V}(x,\mathrm{t})] = \begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \end{bmatrix} \quad [\mathrm{V}'(x,\mathrm{t})] = \begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'_g(x,t) \end{bmatrix} \quad [\mathrm{I}(x,\mathrm{t})] = \begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{bmatrix}$$

$$[L] = \begin{bmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{bmatrix}, [R] = \begin{bmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{bmatrix}$$

$$[C] = \begin{bmatrix} C_{11} & -C_{12} & -C_{13} & 0 \\ -C_{12} & C_{22} & 0 & C_{gs} \\ -C_{13} & 0 & C_{33} & -C_{gs} \\ 0 & 0 & 0 & R_i\,C_{gs} \end{bmatrix} \qquad [G] = \begin{bmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{bmatrix}$$

2.4 Solution of the Linear System

To solve the system of linear equations described in (2.11), an efficient time- domain numerical method should be used. Since 1966, when the finite difference time- domain method (FDTD) was proposed by Yee [9], numerical methods for EM field simulation have advanced a lot and have gained a large popularity [10]. Besides FDTD, several other time-domain methods have evolved, such as the transmission line matrix (TLM) method [8] and the finite integration technique (FIT) [12].

There are many significant differences between these three methods. The FDTD approach employs approximations to a differential equation using a discrete difference and is restricted to coordinate meshes, but a variety of schemes on other types of meshes also exists [10].

Due to its simplicity and accuracy compared to the other above methods, the FDTD technique was used to solve the above equations. Applications of the FDTD method to the full-wave solution of Maxwell's equations have shown that accuracy and stability of the solution can be achieved if the electric and magnetic field solution points are chosen to alternate in space and be separated by one-half the position discretization, e.g., $\Delta x/2$, and to

also be interlaced in time and separated by $\Delta t/2$. The condition for this set of recursion relations to be stable is the Courant condition [14]

$$\Delta t \leq \frac{\Delta x}{v}$$

which states that the time step must be not greater than the propagation time over each cell. The Δx discretization is chosen sufficiently small such that each Δx section is electrically small at the operating frequency range. In order to insure stability in the FDTD solution, the discrete voltage and current solution points are not physically located at the same point but staggered one-half cell apart [10]. However, the lumped terminal constraints such as in (2-11) require that the current and voltages solution points be collocated.

One approximate approach to address this dilemma has been to interpolate the current solution points to the nearest adjacent voltage solution point and then use (2-11). It also turns out that the discrete voltages and currents must be similarly staggered or "interlaced" in time with the time points for the voltages and for the currents being spaced one-half temporal cell apart [19]. To incorporate these constraints into the FDTD solution of the transmission-line equations, we divided each line into Nx sections of length Δx, as shown in Fig.2.3.

Similarly, we divided the total solution time into segments of length Δt. In order to insure the stability of the discretization process and to insure second-order accuracy, we interlaced the $Nx+1$ voltage points, V_1, V_2 ... V_{Nx+1} and the Nx current points, I_1, I_2 ... I_{Nx}. Each voltage and adjacent current solution points were separated by $\Delta x/2$.

Fig.2.3. Relation between spatial and temporal discretizations to achieve second-order accuracy in the discretization of the derivatives.

Then, (2-11) can lead to

$$\frac{1}{\Delta x}\left([I'^{n+1/2}_{k}]-[I'^{n+1/2}_{k-1}]\right)+\frac{1}{\Delta t}[\mathrm{C}]\left([V'^{n+1}_{k}]-[V'^{n}_{k}]\right)+\frac{1}{2}[\mathrm{G}]\left([\mathrm{V}'^{\mathrm{n+1}}_{\mathrm{k}}]+[\mathrm{V}'^{\mathrm{n}}_{\mathrm{k}}]\right)=0$$

$$\frac{1}{\Delta x}\left([V^{n+1}_{k+1}]-[V^{n+1}_{k}]\right)+\frac{1}{\Delta t}[\mathrm{L}]\left([I^{n+3/2}_{k}]-[I^{n+1/2}_{k}]\right)+\frac{1}{2}[\mathrm{R}]\left([\mathrm{I}^{\mathrm{n+3/2}}_{\mathrm{k}}]+[\mathrm{I}^{\mathrm{n+1/2}}_{\mathrm{k}}]\right)=0 \qquad (2\text{-}12)$$

with

$$[V^{j}_{i}]\equiv[V((i-1)\Delta x, j\Delta t)] \qquad [V'^{j}_{i}]\equiv[V'((i-1)\Delta x, j\Delta t)]$$

$$[I^{j}_{i}]\equiv[I((i-\frac{1}{2})\Delta x, j\Delta t)] \qquad [I'^{j}_{i}]\equiv[I'((i-\frac{1}{2})\Delta x, j\Delta t)]$$

Solving these equations give the required recursion relations:

$$[\mathrm{V}'^{n+1}_{k}]=\left(\frac{1}{\Delta t}[C]+\frac{1}{2}[G]\right)^{-1}\left\{\left(\frac{1}{\Delta t}[C]-\frac{1}{2}[G\}\right)[\mathrm{V}'^{n}_{k}]-\frac{1}{\Delta x}([I'^{n+1/2}_{k}]-[I'^{n+1/2}_{k-1}])\right\} \qquad (2\text{-}13)$$

$$[\mathrm{I}_k^{n+3/2}] = \left(\frac{1}{\Delta t}[L] + \frac{1}{2}[R]\right)^{-1} \left\{\left(\frac{1}{\Delta t}[L] - \frac{1}{2}[R]\right)[\mathrm{I}_k^{n+1/2}] - \frac{1}{\Delta x}([V_{k+1}^{n+1}] - [V_k^{n+1}]\right\} \qquad (2\text{-}14)$$

The leap-frog method was used to solve the active transmission line equations because of its simplicity and accuracy [10]. First, the solutions started with an initially relaxed line having zero voltage and current values. Then, voltages along the electrode of transistor were solved for a fixed time from (2-13) while currents were solved for from (2-14).

2.4.1. Boundary Conditions

Equation (2-13) for $k = 0$ and $k = Nx+1$ becomes

$$[\mathrm{V}_1'^{n+1}] = \left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G]\right)^{-1} \left\{\left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G]\right)[\mathrm{V}_1'^{n}] - \frac{2}{\Delta x}([I'^{n+1/2}_1] - [I'^{n+1/2}_0]\right\} \qquad (2\text{-}15)$$

$$[\mathrm{V}_{Nx+1}'^{n+1}] = \left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G]\right)^{-1} \left\{\left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G]\right)[\mathrm{V}_{Nx+1}'^{n}] - \frac{2}{\Delta x}([I'^{n+1/2}_{Nx+1}] - [I'^{n+1/2}_{Nx}]\right\} \qquad (2\text{-}16)$$

By considering Fig.2.3, this equation requires that we replace Δx with $\Delta x/2$ only for $k = 1$ and $k = Nx+1$. We will denote the currents at the source point ($x = 0$) as I_0 and at the load point ($x = L$) as $I_{Nx+1.}$ So according to Fig.2.4 we obtain

$$[I_0] = \frac{1}{2}[R_s]^{-1}\left([V_{in}^n] + [V_{in}^{n+1}] - [V_1^n] - [V_1^{n+1}]\right) \qquad (2\text{-}17)$$

$$[V_{in}] = \begin{bmatrix} V_{ind} \\ V_{ing} \\ V_{ins} \end{bmatrix}, \qquad [G_s] = [R_s]^{-1} = \begin{bmatrix} G_{sd} & 0 & 0 \\ 0 & G_{sg} & 0 \\ 0 & 0 & G_{ss} \end{bmatrix}$$

$$[I'_0] = \frac{1}{2}[R'_s]^{-1}\left([V'^n_{in}] + [V'^{n+1}_{in}] - [V'^n_1] - [V'^{n+1}_1]\right) \qquad (2\text{-}18)$$

$$[V_{in}]=\begin{bmatrix}V_{ind}\\V_{ing}\\V_{ins}\\0\end{bmatrix},\qquad [G_s]=[R_s]^{-1}=\begin{bmatrix}G_{sd}&0&0&0\\0&G_{sg}&0&0\\0&0&G_{ss}&0\\0&0&0&0\end{bmatrix}$$

Similarly, we impose the terminal constraint at $x = L$ by substituting I_{Nx+1} into (2-16) as follow:

$$[I_{Nx+1}]=\frac{1}{2}[R_L]^{-1}\left([V_{Nx+1}^{n}]+[V_{Nx+1}^{n+1}]\right) \tag{2-19}$$

where

$$[G_L]=[R_L]^{-1}=\begin{bmatrix}G_{Ld}&0&0\\0&G_{Lg}&0\\0&0&G_{Ls}\end{bmatrix}$$

$$[I'_{Nx+1}]=\frac{1}{2}[R'_L]^{-1}\left([V'^{n}_{Nx+1}]+[V'^{n+1}_{Nx+1}]\right) \tag{2-20}$$

and

$$[G'_L]=[R'_L]=\begin{bmatrix}G_{Ld}&0&0&0\\0&G_{Lg}&0&0\\0&0&G_{Ls}&0\\0&0&0&0\end{bmatrix}$$

The finite difference approximation of (2-13) can be written as follows:

- For $k = 1$

$$[\mathrm{V}_1'^{n+1}]=\left(\frac{1}{\Delta t}[C]+\frac{1}{2}[G]\right)^{-1}\left\{\left(\frac{1}{\Delta t}[C]-\frac{1}{2}[G]\right)[\mathrm{V}_1'^{n}]-\frac{2}{\Delta x}([I'^{n+1/2}_1]-[I'^{n+1/2}_0]\right\}=$$

$$\left(\frac{1}{\Delta t}[C]+\frac{1}{2}[G]+\frac{1}{\Delta x}[R_s']^{-1}\right)\begin{cases}\left(\frac{1}{\Delta t}[C]-\frac{1}{2}[G]-\frac{1}{\Delta x}[R_s']^{-1}\right)[V'^{n}_1]\\-\frac{2}{\Delta x}\left([I'^{n+1/2}_1]-\frac{1}{2}[R_s']([V'^{n}_{in}]-[V'^{n+1}_{in}])\right)\end{cases} \tag{2-21}$$

- For $k = 2, .., Nx$

$$[\mathrm{V}'^{n+1}_{k}] = \left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G]\right)^{-1} \left\{ \left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G]\right)[\mathrm{V}'^{n}_{k}] - \frac{1}{\Delta x}([I'^{n+1/2}_{k}] - [I'^{n+1/2}_{k-1}]\right\} \quad (2\text{-}22)$$

- For $k = Nx+1$

$$[\mathrm{V}'^{n+1}_{Nx+1}] = \left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G]\right)^{-1} \left\{ \left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G]\right)[\mathrm{V}'^{n}_{Nx+1}] - \frac{2}{\Delta x}([I'^{n+1/2}_{Nx+1}] - [I'^{n+1/2}_{Nx}]\right\} =$$

$$\left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G] + \frac{1}{\Delta x}[R'_L]^{-1}\right)\left\{\left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G] - \frac{1}{\Delta x}[R'_L]^{-1}\right)[V'^{n}_{Nx+1}] + \frac{2}{\Delta x}\left([I'^{n+1/2}_{Nx}]\right)\right\} \quad (2\text{-}23)$$

As for (2-14):

- For $k = 2, 3, \ldots, Nx$

$$[\mathrm{I}^{n+3/2}_{k}] = \left(\frac{1}{\Delta t}[L] + \frac{1}{2}[R]\right)^{-1} \left\{ \left(\frac{1}{\Delta t}[L] - \frac{1}{2}[R]\right)[\mathrm{I}^{n+1/2}_{k}] - \frac{1}{\Delta x}([V^{n+1}_{k+1}] - [V^{n+1}_{k}]\right\} \quad (2\text{-}24)$$

The voltages and currents were solved by iterating k for a fixed time and then iterating time.

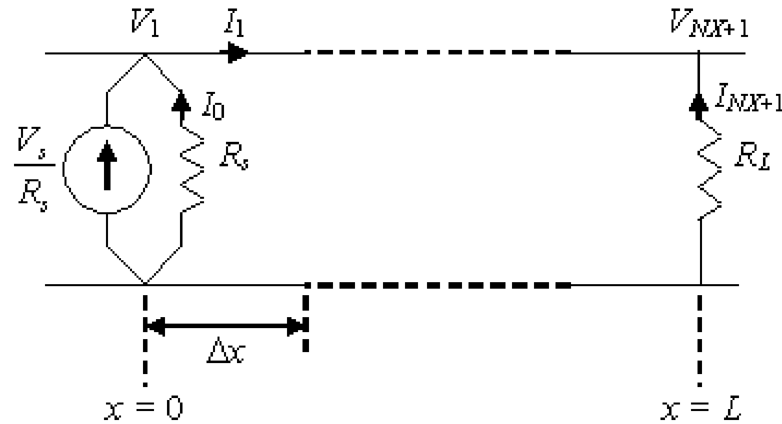

Fig.2.4. Discretization of the terminal voltages and currents.

2.5 Experimental Results

2.5.1. Load-pull Measurements

The proposed approach was used to model a sub micrometer-gate GaAs transistor (NE710) [24]. The device has a 0.3 µm × 280 µm gate.

The first step consisted to characterize the transistor. In order to capture both the linear and nonlinear device behaviors (this later will be discussed in the next chapter), we used a load-pull bench.

Load pull measurements involve embedding the device to be tested into measurement circuitry that can be impedance tuned. The measurement system simultaneously monitors the tuned impedance of the characterization circuitry and the performance of the device. Device response is then recorded under the variable load conditions.

The resulting loci of impedances required to obtain a constant performance parameter (i.e. output power or power added efficiency) are displayed on a smith chart in the form of closed contours. The load-pull contours are determined one frequency at a time. Also the load-pull contours apply to only one incident power level used in the measurement.

In this work, we used a bench from Focus microwave that consists on a probing station, the HP 8340B synthesized signal generator, the Agilent 8565EC spectrum analyzer, the CMMT1808 tuners, the Anritsu ML2438A power meter, and the Agilent ML2438A power supplies.

The block diagram of the measurement setup is shown in Fig.2.5 while the bench used in this work is shown in Fig.2.6.

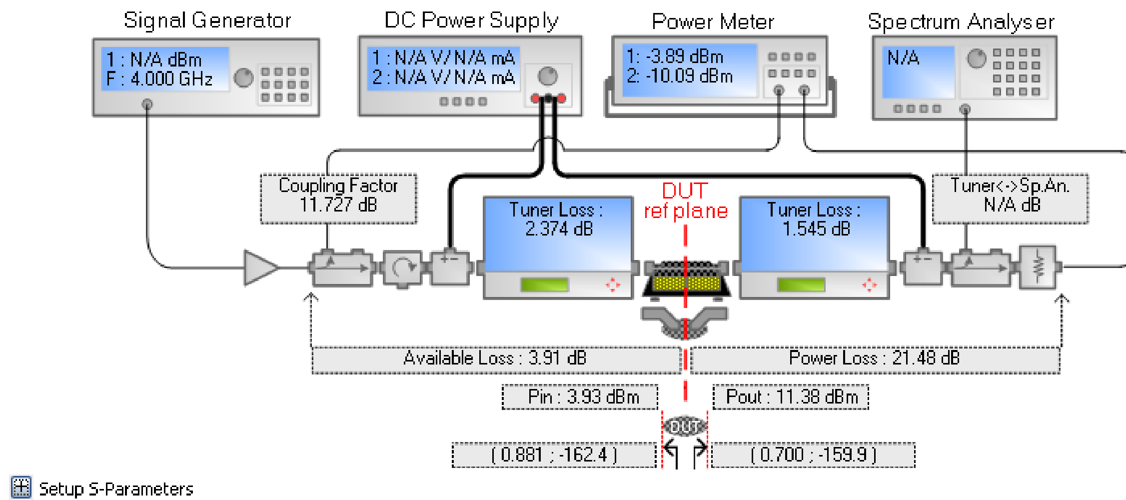

Fig.2.5 Block diagram of the load-pull experimental setup [25]

Fig.2.6. Load-pull bench used to characterize the device

The input and output nodes were connected to the beginning of the gate electrode and at the end of the drain electrode, respectively. The transistor was biased at V_{ds} = 3 V and I_{ds} = 10 mA. The source and load resistances were settled to 50 Ω. Moreover, the two terminals of the source electrode were grounded. The scattering parameters of this transistor were simulated over a frequency range of 2-26 GHz using our proposed model and they are compared to S.D model and measured data as shown in Fig.2.7. It is clearly shown that even at such relatively low microwave frequencies our model is more accurate compared to the S.D model. Fig.2.8 shows the measured and modeled data of the FET for various DC and pulsed voltages. The model shows very good fitting of the data. This transistor showed a breakdown above 12 V. The channel was completely pinched off at -2 V. The maximum drain current was 90 mA.

Figs. 2.9 and 2.10 show the experimental load-pull and source-pull characteristics of this optimized transistor structure. When matched, it has an output power of 16 dBm with a 10% PAE at 10GHz. In Fig.2.9, the output RF power is shown as a function of the complex output impedance matching conditions of the device. The Smith chart is normalized to 50Ω. Maximum power for this transistor occurs at the darkest colored square in the diagram, and corresponds to an impedance of about (2.5- j5.0) Ω. This optimized impedance value does not include the effects of external parasitic such as bonding pads etc. The intrinsic equivalent circuit model was obtained using well-known hot and cold modeling techniques [13]. After removing the extrinsic components via de- embedding methods, a hot modeling technique was utilized to obtain the intrinsic elements. Then, an optimization was performed by varying the values of the intrinsic FET elements in the vicinity of 10% of their mean value until the error between measured and modeled S-parameters was found acceptable (i.e., less than 2%). The obtained values of the extrinsic and intrinsic elements are summarized in Table 2.1.

Note: While introducing our model, we stated that it should be more suitable in millimeter-wave frequencies than the well-known S.D models or even the semi-distributed models. Therefore, measurements had to be performed up to the millimeter-wave range. However, due to practical constraints, we were able to measure the transistor parameters only up to 26 GHz. Even if this

maximum frequency was well below the targeted millimeter-wave frequency range, it was sufficient to demonstrate that our model is more accurate that the other models while compared to measurements. Thus, if, as expected, this tendency is maintained while increasing the operating frequency, our model should continue to be closer to measurements than the other models, helping us to claim that the proposed model will be more accurate in the millimeter-wave frequency range.

2.5.2. Results with Different Transistor Sizes

Optimum device periphery selection in actual design tasks often requires a different model for each particular device layout in a given technological process. In order to avoid this problem, scalable models are available allowing the designer to select the optimum device geometry (i.e., number and width of gate fingers) for the specific application through the evaluation of suitably defined figures of merit and design criteria [1], [2]. Scalable models also allow for important time saving during the characterization of foundry processes.

In order to further test the predictive capabilities of the proposed approach, the model was adopted to predict the electrical behavior of three different device structures namely, two, three, and four times the gate-with of the NE7100 we already characterized (i.e., 0.3 μm$\times$ 560 μm, a 0.3 μm $\times$ 840 μm and a 0.3 μm $\times$ 1120 μm). The parameters of these transistors were obtained using the scaling method. Figures 2.11, 2.12 and 2.13 show the respective scattering parameters obtained for the three device structures by using the new approach and the S.D model, respectively.

Based on the above note regarding the accuracy of our model in the millimeter-wave range, we can say that by increasing the device dimensions and the frequency, the difference between the proposed approach and the S.D model should also increases. Also, as for practical applications, large gate periphery devices are used to generate sufficient total output power levels. With the increase of device gate periphery, the self-heating effect and the defect trapping effect will both be more profound.

This is due to the fact that our model is based on solving the wave equation in the transistor structure while the S.D model is based on circuit modeling.

Therefore, the proposed model can consider the effect of wave propagation along the device electrode more accurately than the S.D model, especially when the device dimension is comparable to the wavelength.

Because the gate electrode has a different reactance from the drain electrode, the two electrodes exhibit different phase velocities for the input and output signals, respectively. By increasing frequency, the phase cancellation phenomena due to the phase velocity mismatching cannot be neglected. This effect can be now considered in our approach.

Fig.2.14 depicts the voltage gain as a function of the gate width at 60 GHz. It is obvious that by increasing the gate width, voltage gain decreases periodically due to the phase cancellation.

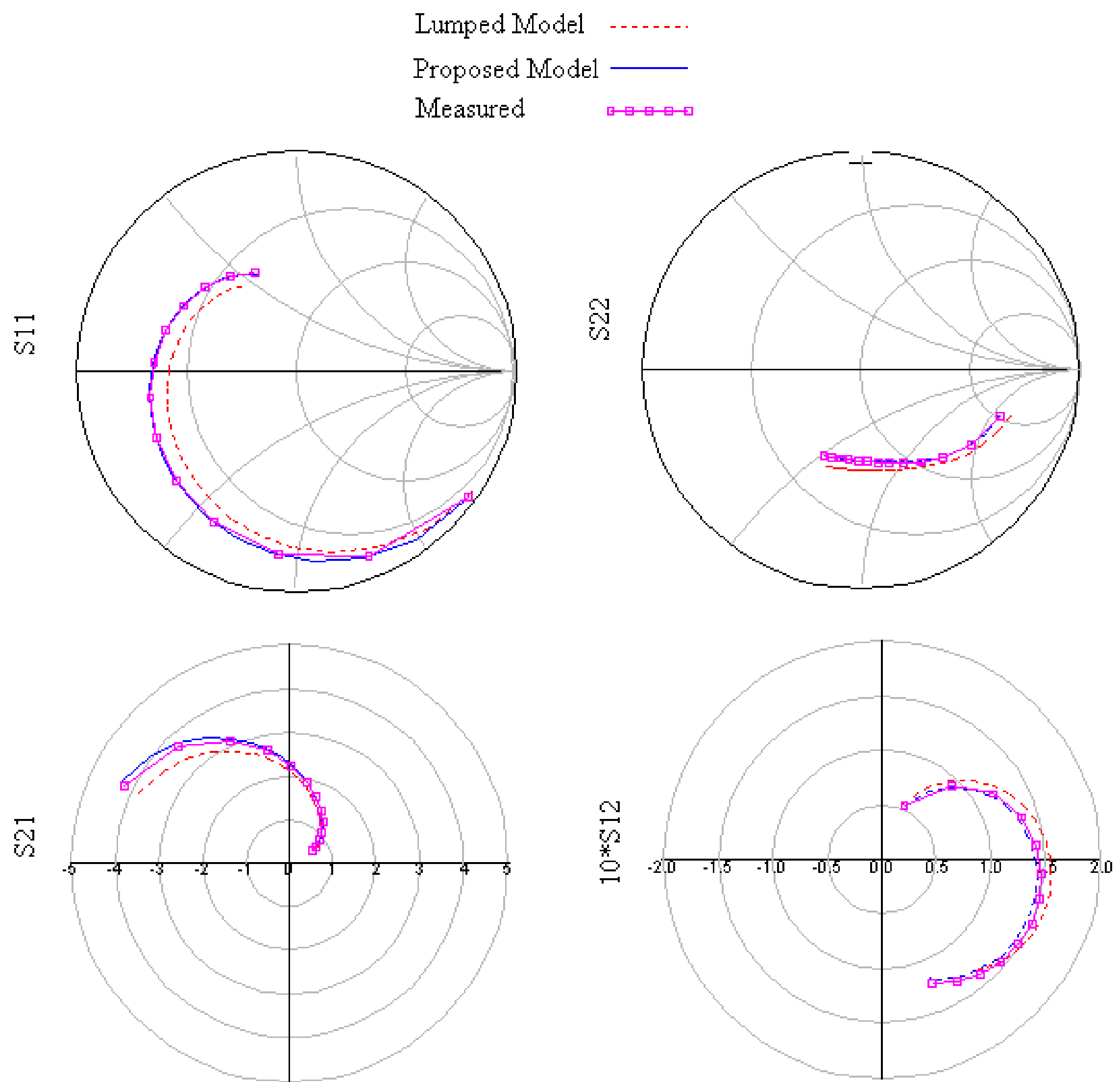

Fig.2.7 Comparison of measured S-parameters with those obtained using the lumped model and the proposed model

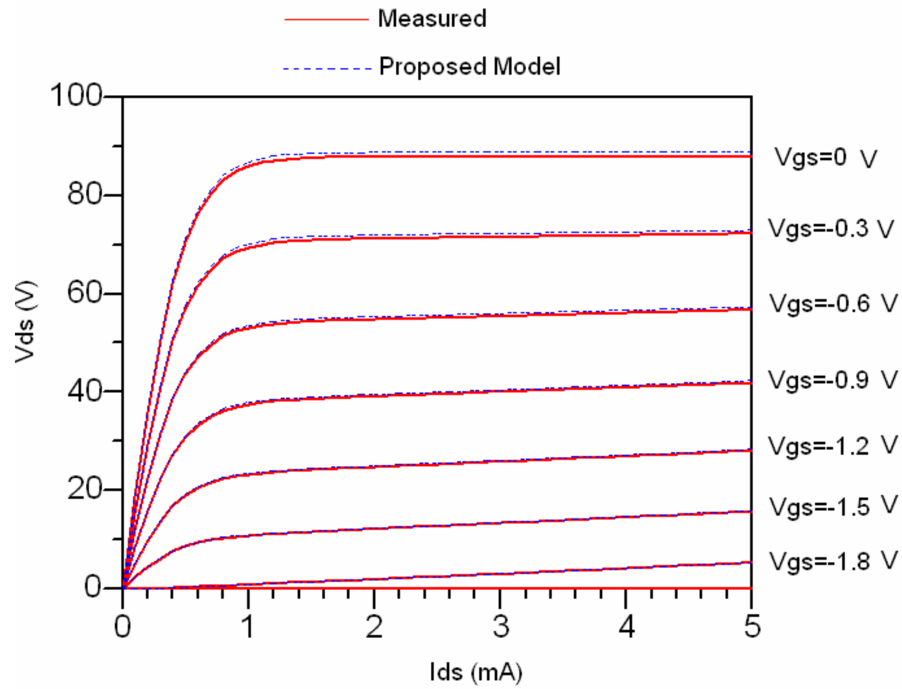

Fig.2.8.I-V curves for the NE710 with large signal fitting models.

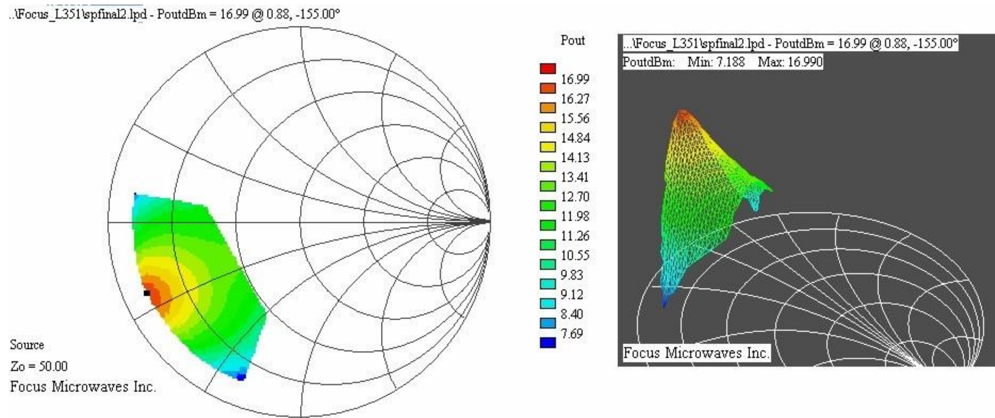

Fig.2.9. Output power as function of load impedance for an optimized structure at 10GHz

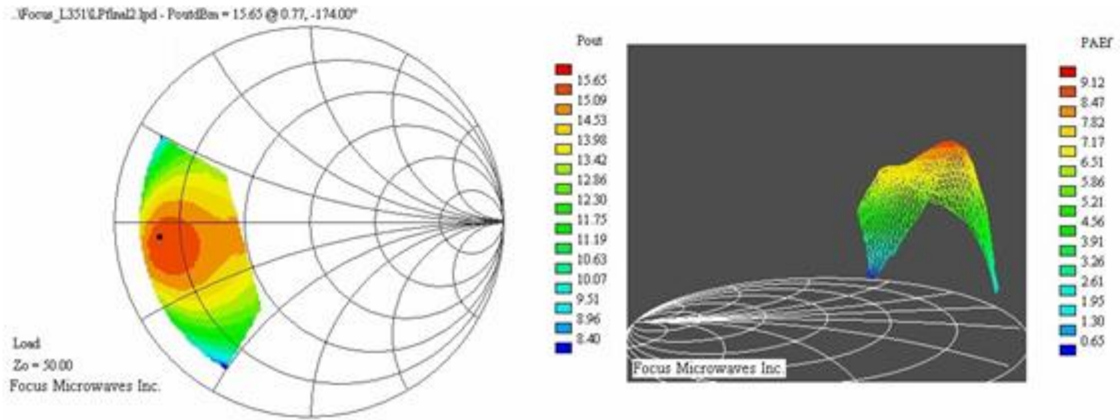

Fig.2.10. Pout and PAE as function of load impedance for an optimized structure at 10 GHz.

Table2.1: Numerical values of extrinsic and intrinsic elements. (The transistor was biased at V_{ds} = 3 V and I_{ds} = 10 mA)

The distributed model elements	Numerical Values(per unit length)
L_{dd}	780 nH/m
Lss	780 nH/m
Lgg	161 nH/m
Mgd	360 nH/m
Mgs	360 nH/m
Mds	240 nH/m
Rd	900 Ω/m
Rs	900 Ω/m
Rg	34.300 Ω/m
Cgp	0.6 pF/m
Cdp	87 pF/m
Csp	148 pF/m
Cds	0.0178 nF/m
Cgd	0.1178 nF/m
Gm	146.42 S/m
Ri	0.002 Ω/m
Gds	15.46 mho/m
Cgs	0.771 nF/m

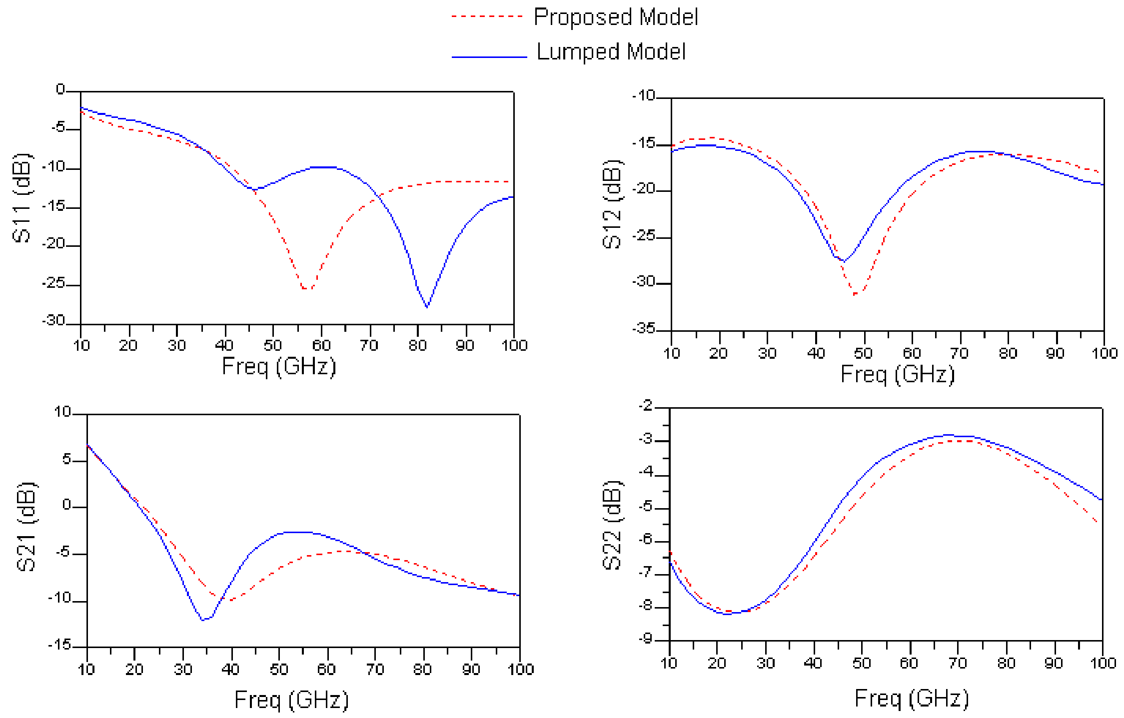

Fig.2.11. S-parameters of transistor with 560 μm gate

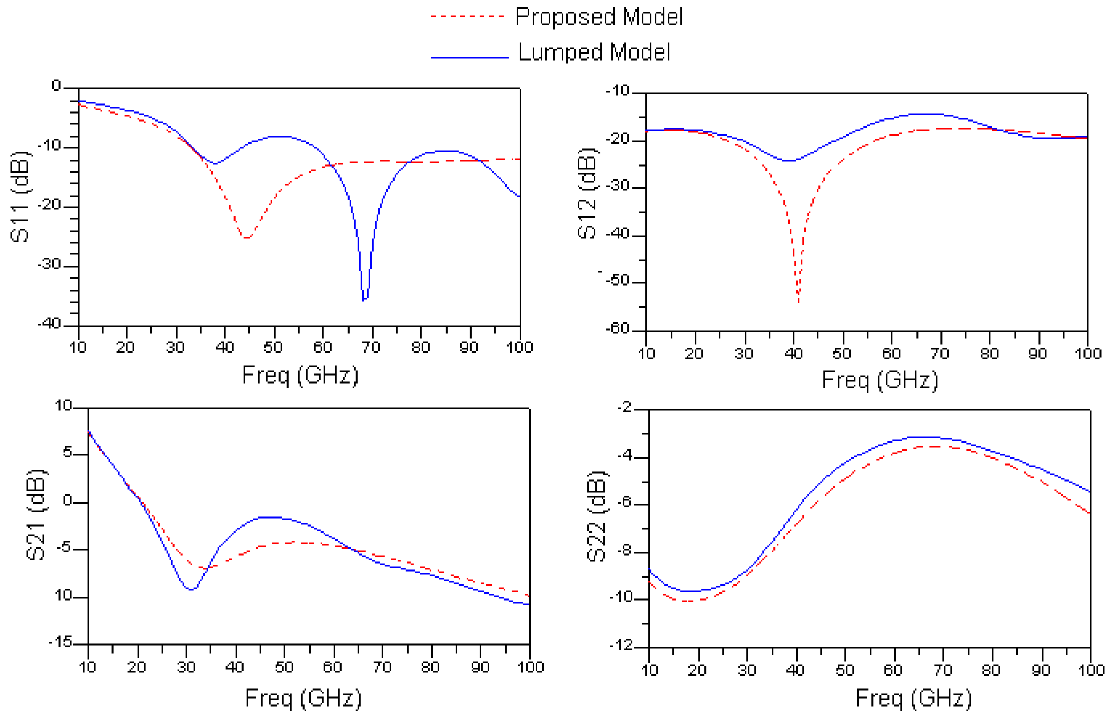

Fig.2.12. S-parameters of transistor with 840 μm gate

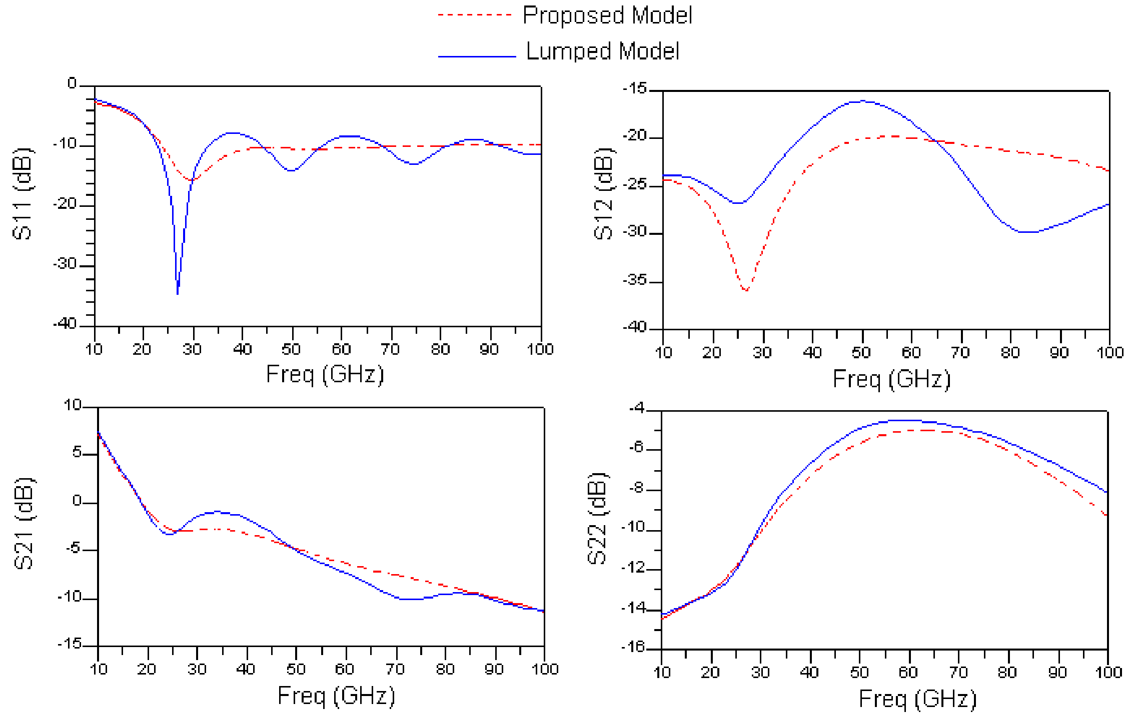

Fig.2.13. S-parameters of transistor with 1120 μm gate

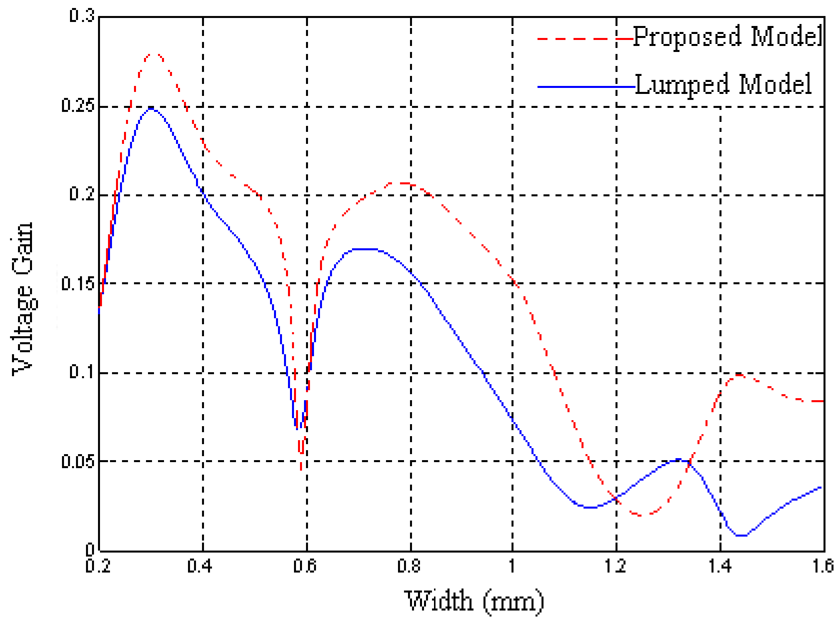

Fig.2.14.Transistor voltage gain versus gate width at 60 GHz frequency

The time-domain load voltages obtained from both the proposed and the lumped models for different gate widths and frequencies are shown in Figures.2.15 to 2.18.

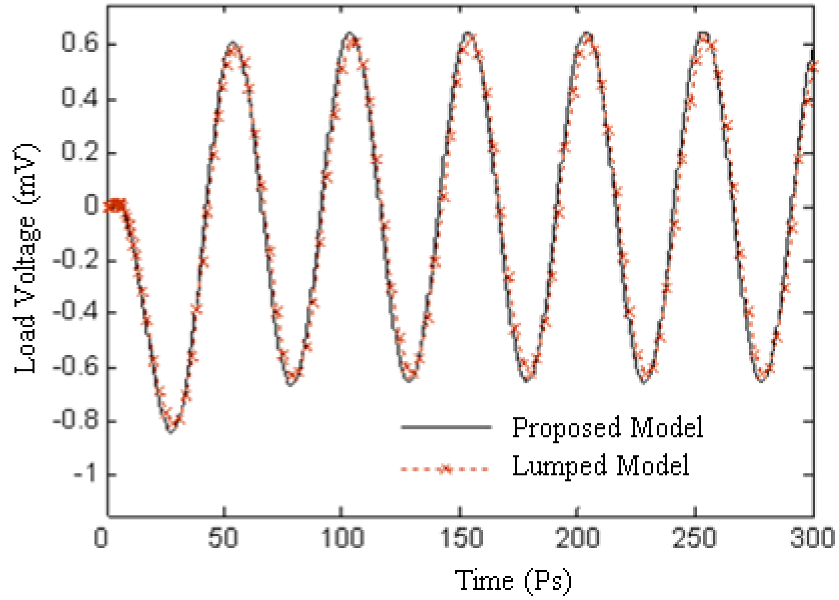

Fig.2.15. Output voltage of transistor with 280 μm gate width at 20GHz

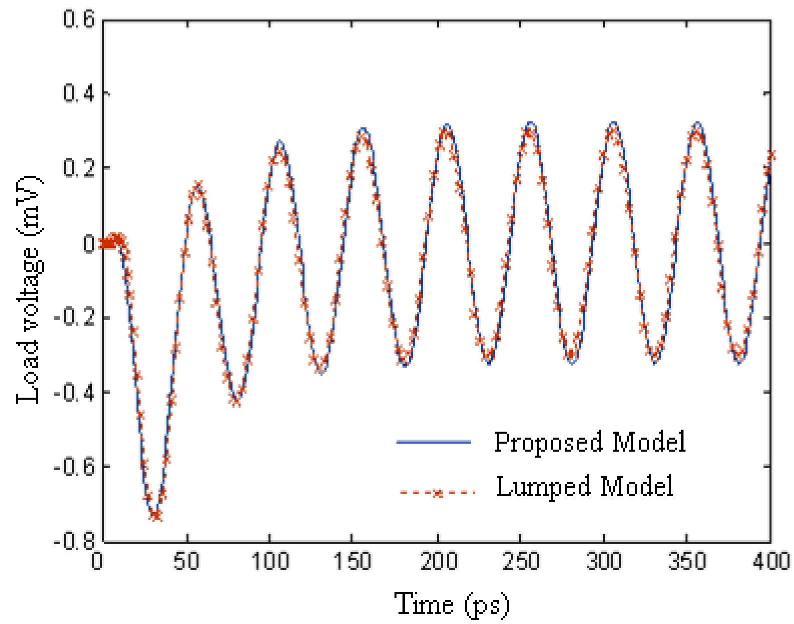

Fig.2.16. Output voltage of transistor with 560 μm gate width at 20GHz

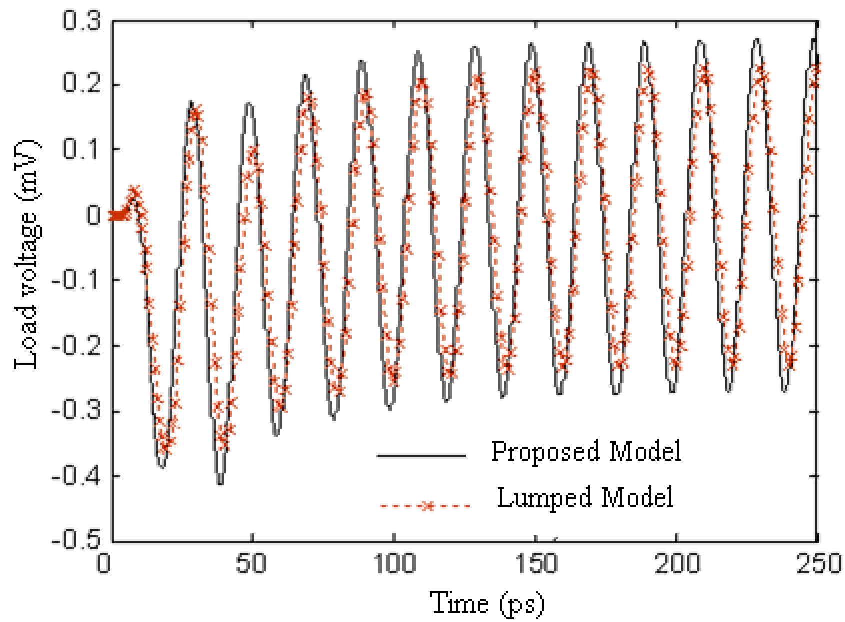

Fig.2.17. Output voltage of transistor with 560 μm gate width at 60GHz

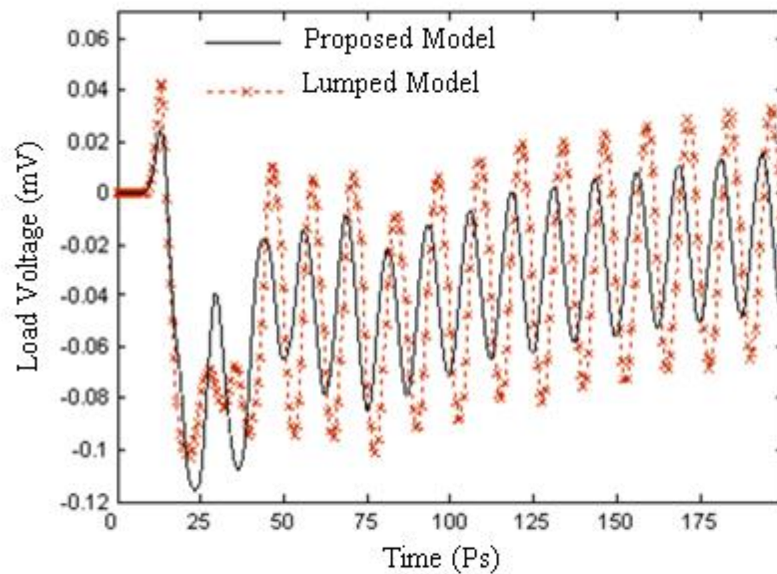

Fig.2.18. Output voltage of transistor with 1120 μm gate width at 80GHz

As the frequency is increasing, the magnitude and phase from the proposed model are more different than those from the lumped model. The most important reason for this difference is the phase cancellation that is taken account by the proposed model. Figs.2.19 and 2.20 show the time domain variation of voltage at 80 GHz at the beginning and the end

of drain and gate electrodes, respectively. The voltage magnitude at the end of the gate electrode is less than the voltage at its beginning. This is mainly due to the gate ohmic resistance.

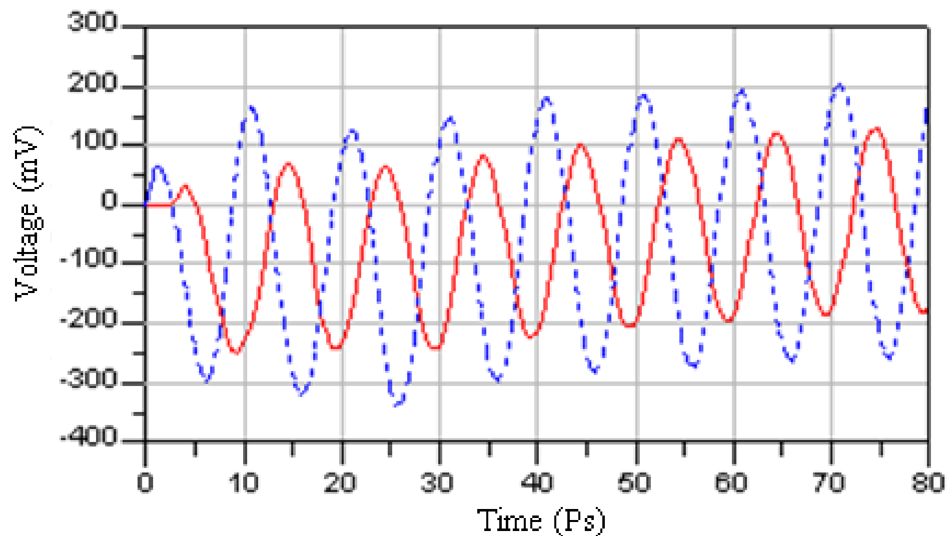

Fig.2.19. The voltage of transistor with 560 μm gate width at the beginning ("solid line") and the end of the drain electrode ("dash line")

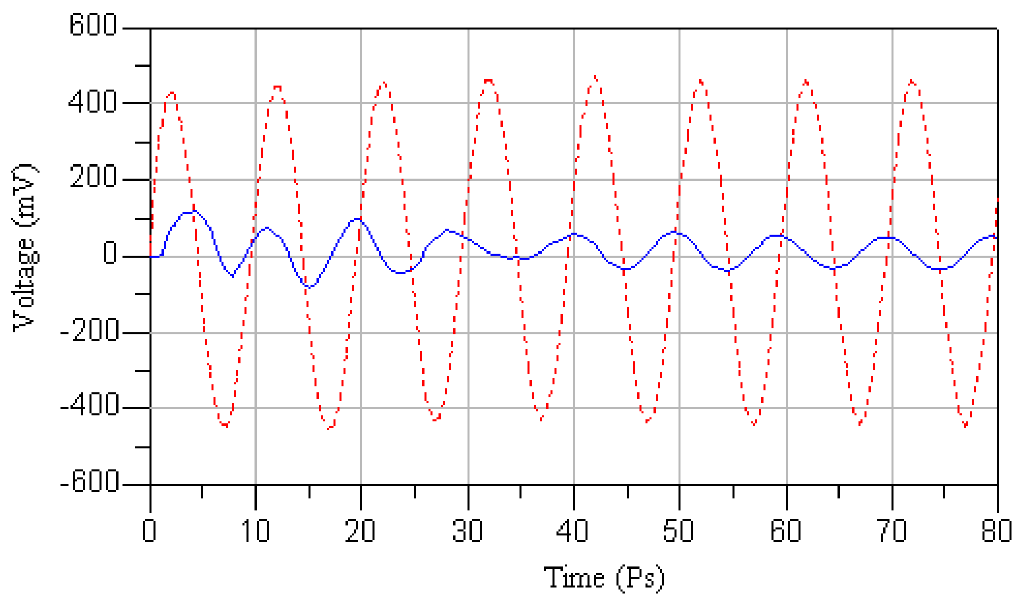

Fig.2.20. Output voltage with 560 μm gate width at the beginning ("dash line") and the and the end of the drain electrode ("solid line")

2.5.3 The Effect of the Location of Excitation/Extraction Contact Points

In microwave FETs, the location of the excitation⁄extraction contact points is critical for optimal transistor performance. It is obvious that in FETs with small gate widths, the place of the probes is not critical.

However, for mm-wave FETs, due to the phase and amplitude differences in different points of the electrodes, the location of excitation and extraction of signals affect both signal and noise performances of the device. Therefore, several configurations of excitation⁄extraction points were analyzed as shown in Fig.2.21. The input and output VSWR in frequency range of 5-30GHz are presented in Fig.2.22 and Fig.2.23, respectively. The maximum stable gain (MSG) and power gain for these four cases are shown in Fig.2.24 and Fig.2.25, respectively. We can observe that case 3, which is excited and loaded from the beginning of the gate and drain electrodes, respectively, has the minimum input VSWR and maximum MSG compared to the other configurations. Besides, it has the minimum output VSWR from 5-12.5GHz. In the range of 12.5- 30GHz, case 4 exhibits the minimum output VSWR. It can be seen that the gain of the device is higher for cases where the signals are injected and extracted from the middle of gate and drain electrodes like in case 2. This is due to a decrease in the effective gate resistance. Indeed, by increasing the gate width, voltage gain decreases periodically due to the phase cancellation. Our simulation shows that exciting and extracting the signal from the opposite ends of the electrodes (case 4) causes a very stable device, i.e., a Rollet stability factor (K) much higher than unity. This is also due to the effect of the equivalent resistance of the signal path, which is maximal in this case. So we can conclude that case 3 could be considered as the best structure in terms of signal analysis.

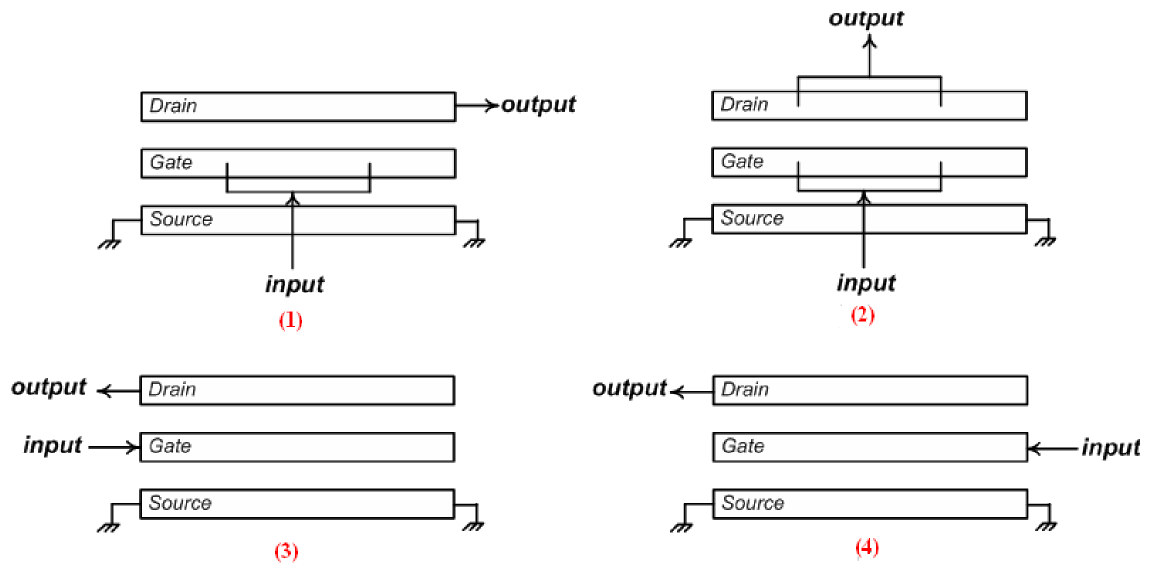

Fig.2.21. Different configuration of excitation/extraction contact points

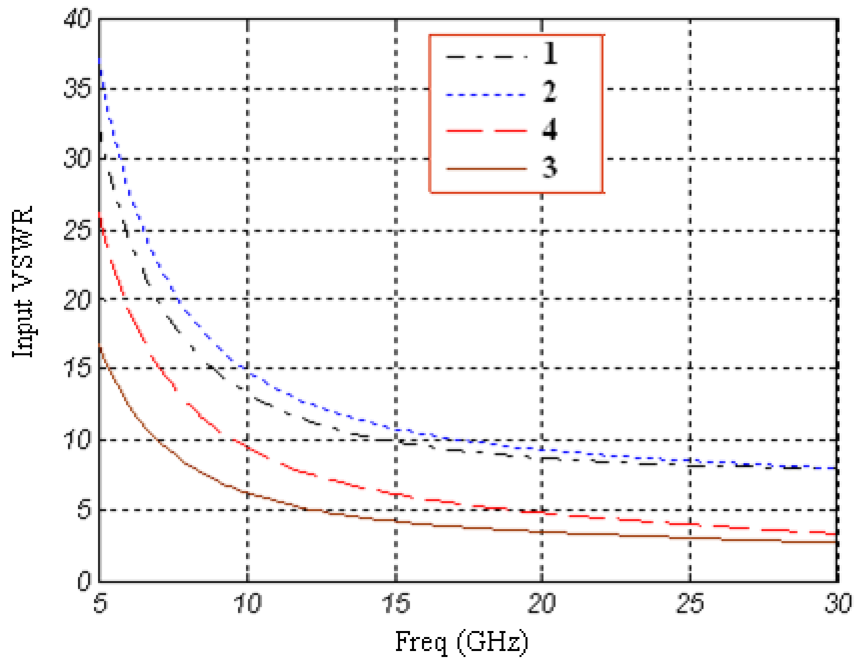

Fig.2.22. Input VSWR for all four configurations

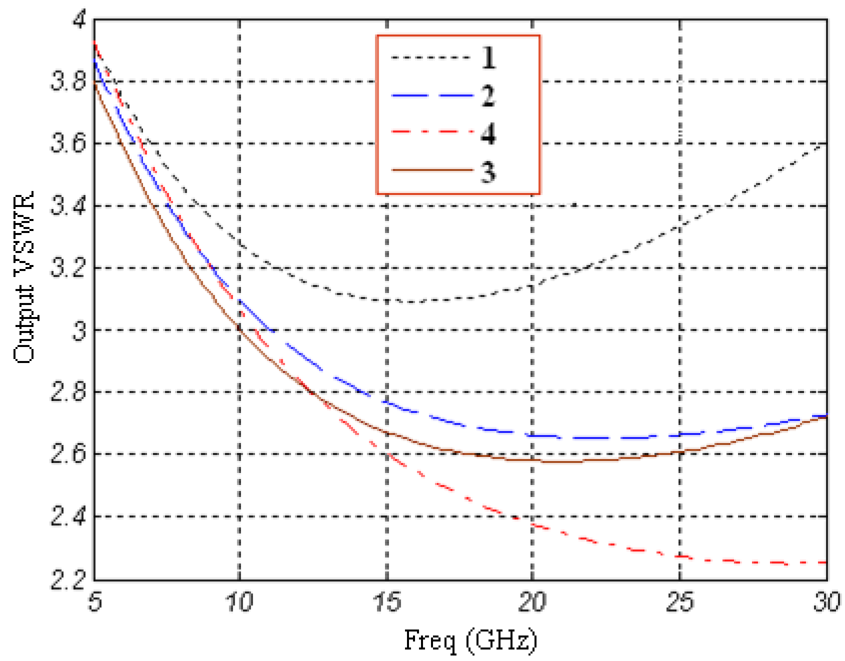

Fig.2.23. Output VSWR for all four configurations

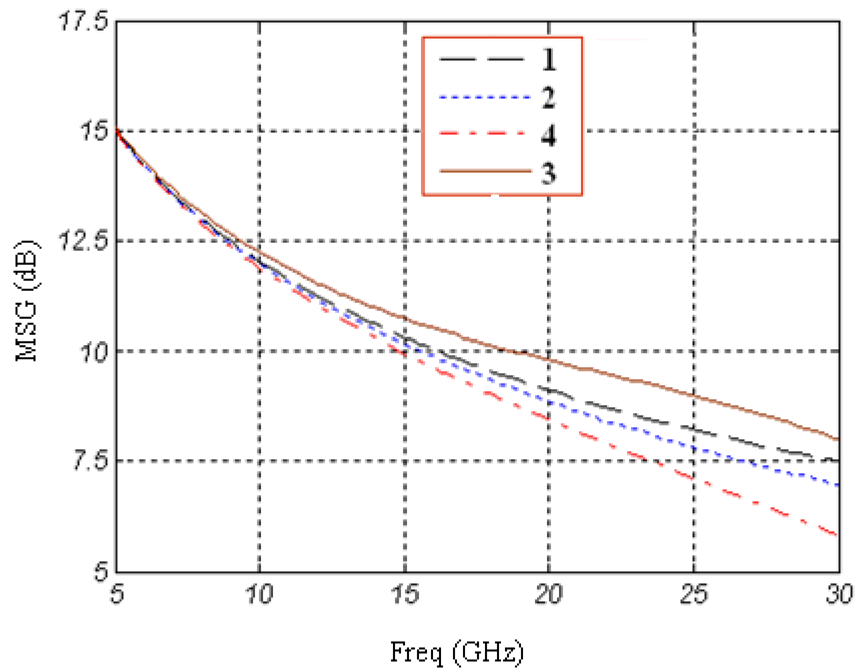

Fig.2.24. MSG for all four cases

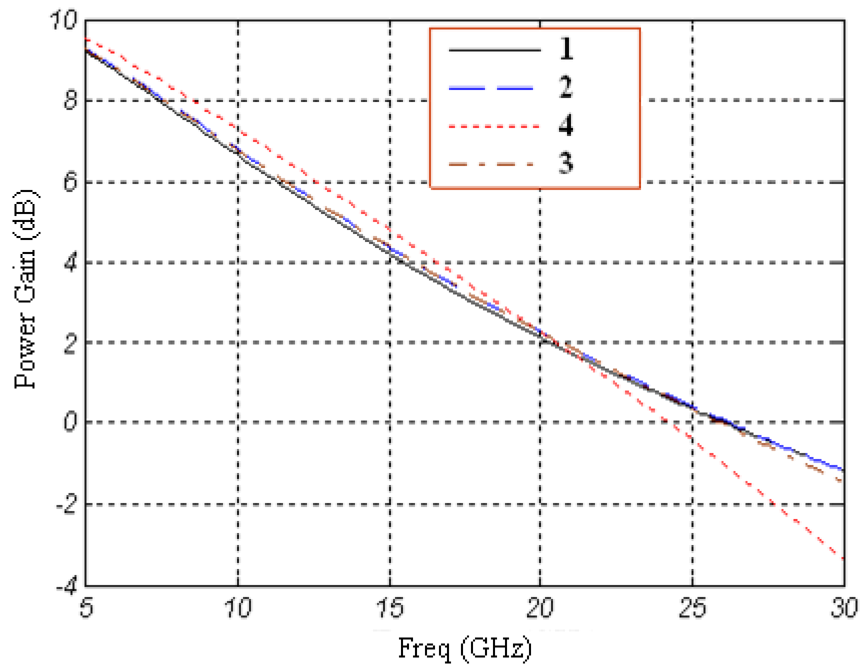

Fig.2.25. Power Gain for all four cases

2.5.4 Distributed Effects on Source Electrode

In a transistor where the width is much smaller than the wavelength, we can consider the source electrode grounded all over its surface [21]-[23]. But by increasing the frequency or device width, this assumption could become invalid. In this part, we first considered the source grounded only at the beginning and at the end of the electrode. By this assumption, the system of differential equations of the three coupled active lines was derived using the transmission line theory. Then, we compared the results with the case in which the transistor is modeled as a three line structure. It should be also noted that we considered effects of all parasitic elements in this case. Fig.2.26 shows the schematic of the proposed transistor including parasitic elements indicating bounding effects.

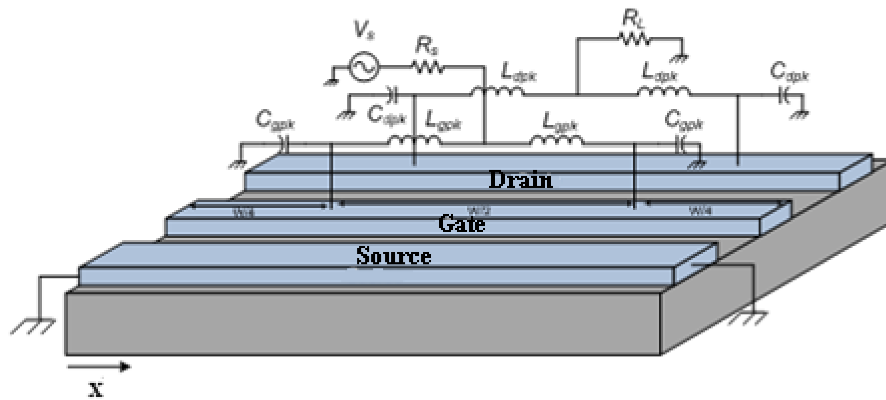

Fig.2.26. Schematic of a pi-gate FET including parasitic elements

The values for active and passive parts are already shown in Tables 2.1. Parasitic elements values used in simulation are [12]:

$L_{gpk} = 0.766$ nH $\quad$ $L_{dpk} = 0.868$ nH

$C_{gpk} = 0.036$ pF $\quad$ $C_{dpk} = 0.0296$ pF

$R_L = 50\Omega$ $\quad$ $R_s = 50\Omega$

The most important point about the NE710 transistor is its unique symmetrical geometry, which enabled us to split it into two separate sections. Since it is symmetrical at x = w/2, where w is gate width, we can assume a magnetic wall at this point and instead of simulating the whole structure, we just simulated half circuit as shown in Fig.2.27. It is worth to mention that by splitting the transistor into two parts, source and load resistors as well as parasitic elements become twice as in the initial circuit. As depicted in Fig.2.27, the boundary conditions in this case at the beginning and the end of the electrode and at x = w/4 were considered. The schematic of the circuit differential length model is shown in Fig.2.28.

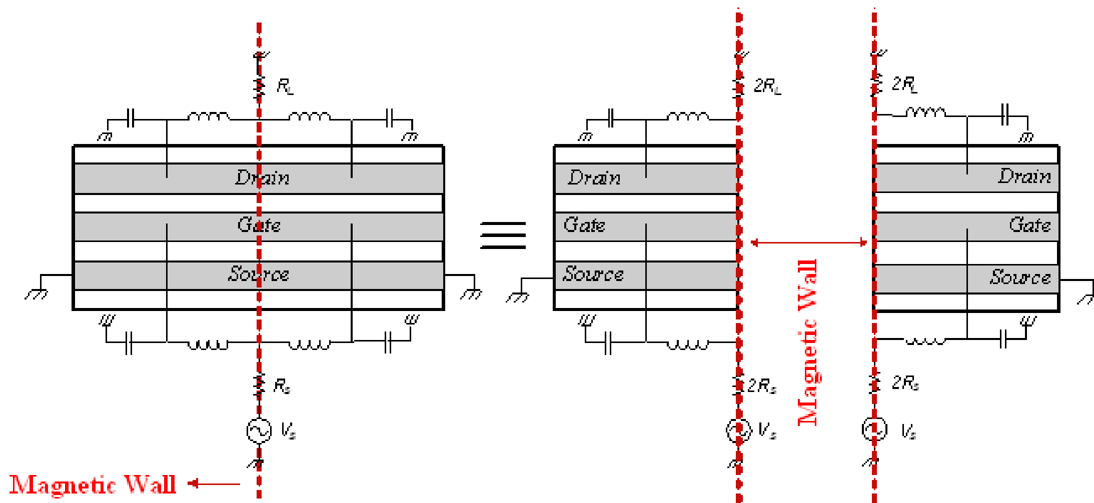

Fig.2.27. Splitting transistor into two separate sections using magnetic wall concept

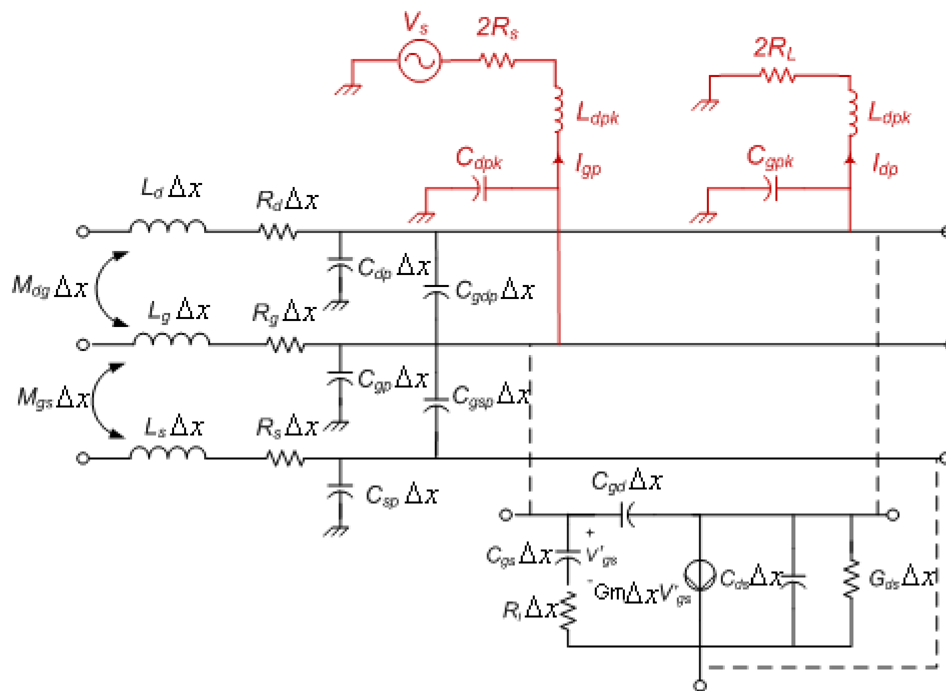

Fig.2.28. Equivalent circuit model of a differential length of a FET

This new circuit model does not affect the Kirchhoff's voltage law (KVL) equations obtained earlier, but the Kirchhoff's current law (KCL) equations will become

$$\frac{\partial I_d(x,t)}{\partial x} + C'_{11}\frac{\partial V_d(x,t)}{\partial t} - C_{12}\frac{\partial V_g(x,t)}{\partial t} - C_{13}\frac{\partial V_s(x,t)}{\partial t} + G_m V'_g(x,t) + G_{ds}(V_d(x,t) - V_s(x,t)) + \frac{I_{dp}}{\Delta x} = 0 \quad (2\text{-}25)$$

$$\frac{\partial I_g(x,t)}{\partial x} + C'_{22}\frac{\partial V_g(x,t)}{\partial t} - C_{12}\frac{\partial V_d(x,t)}{\partial t} - C_{23}\frac{\partial V_s(x,t)}{\partial t} + C_{gs}\frac{\partial V'_g(x,t)}{\partial t} + \frac{I_{gp}}{\Delta x} = 0 \quad (2\text{-}26)$$

$$\frac{\partial I_s(x,t)}{\partial x} + C_{33}\frac{\partial V_s(x,t)}{\partial t} - C_{23}\frac{\partial V_g(x,t)}{\partial t} - C_{13}\frac{\partial V_d(x,t)}{\partial t} - C_{gs}\frac{\partial V'_g(x,t)}{\partial t} - G_m V'_g(x,t) + G_{ds}(V_s(x,t) - V_d(x,t)) = 0 \quad (2\text{-}27)$$

where

$$C'_{11} = C_{11} + \frac{C_{dpk}}{\Delta x}$$

$$C'_{22} = C_{22} + \frac{C_{gpk}}{\Delta x}$$

Since two new variables, I_{gpk} and I_{dpk}, appear in these equations, we need to add two more equations to solve them. By applying the KVLs to source and load loops we obtain

$$-V_g(x,t) + L_{gpk}\frac{\partial I_{gp}(t)}{\partial t} + 2R_s I_{gp}(t) + V_{in}(t) = 0 \quad (2\text{-}28)$$

$$-V_d(x,t) + L_{dpk}\frac{\partial I_{dp}(t)}{\partial t} + 2R_L I_{dp}(t) = 0 \quad (2\text{-}29)$$

Using the FDTD algorithm leads us to

$$-\frac{V_{gk}^{n} + V_{gk}^{n+1}}{2} + L_{gpk}\frac{I_{gp}^{n+1} - I_{gp}^{n}}{\Delta t} + 2R_s\frac{I_{gp}^{n+1} + I_{gp}^{n}}{2} + \frac{V_{in}^{n} + V_{in}^{n+1}}{2} = 0 \quad (2\text{-}30)$$

$$-\frac{V_{dk}^{n}+V_{dk}^{n+1}}{2}+L_{dpk}\frac{I_{dp}^{n+1}-I_{dp}^{n}}{\Delta t}+2R_{L}\frac{I_{dp}^{n+1}+I_{dp}^{n}}{2}=0 \qquad (2\text{-}31)$$

In addition to boundary conditions at w/4, boundary conditions at point x = 0 and w/2 will be formulated as

$$I_{d0}^{n}=I_{g0}^{n}=0 \qquad I_{d\,Nx+1}^{n}=I_{g\,Nx+1}^{n}=0$$

The algorithm required to solve the above equations for the NE710 excited from 3w/4 and w/4 is the same as the one in which the transistor is excited from the beginning and the end. Fig.2.29 shows the source voltage obtained from three- and two-line structures at the middle of the source electrode for gate width of 560µm at 20GHz.

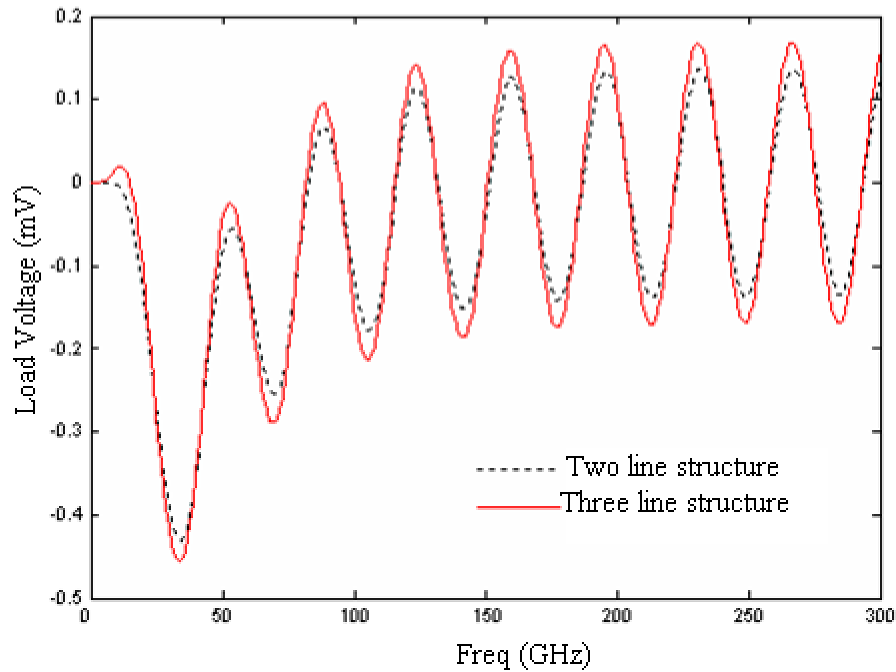

Fig.2.29. Waveform of load voltage obtained from two-line structure compared with three-line structure for scaled transistor at 20 GHz

Fig.2.30 shows the waveform of the load voltage for a scaled transistor of three-line structure. The effect of source electrode is clearly shown in this figure. We observe that by increasing the gate width due to distributed effect on source electrode, the voltage amplitude

is increased at the middle of the source. The scattering parameters of the scaled transistor obtained for two- and three-line structures in the range of 1-100GHz are shown in Figs 2.31-2.34. It is clearly shown that by increasing frequency, the difference between the two structures will be increased. As operating frequency of FET increases up to the millimeter range, the dimensions of the electrodes become comparable to the wavelength. So we cannot ignore distributed effects of source electrode. As a result, for modeling of transistor at millimeter range, we should take source electrode into account.

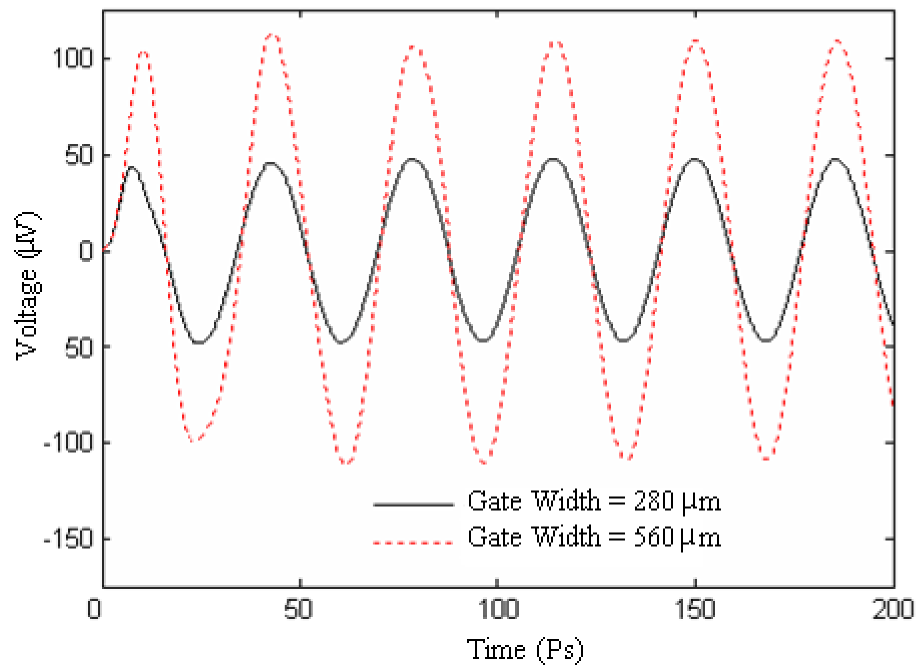

Fig.2.30. waveform of source voltage obtained from three-line structure at the middle of the source electrode

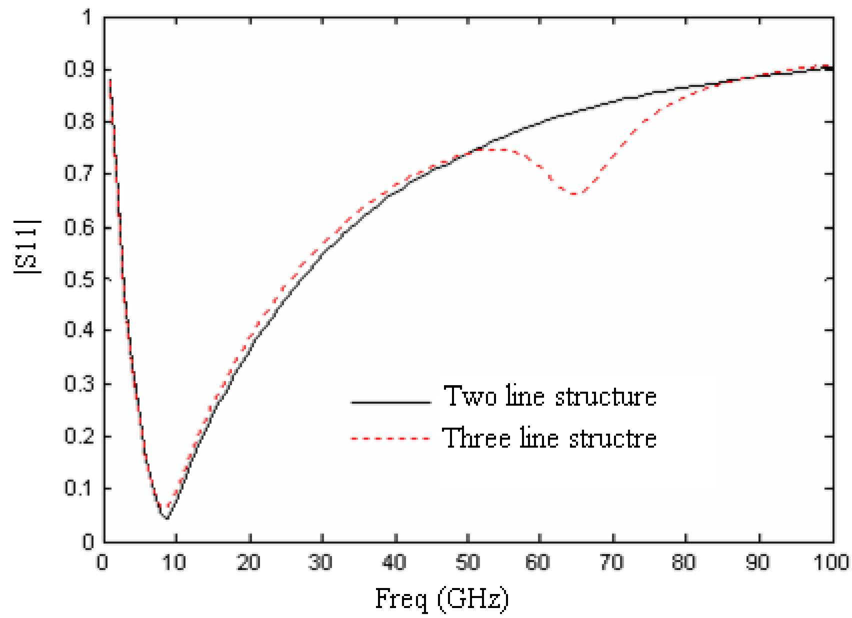

Fig.2.31. $|S_{11}|$ in frequency range of 1-100GHz for two and three line structures

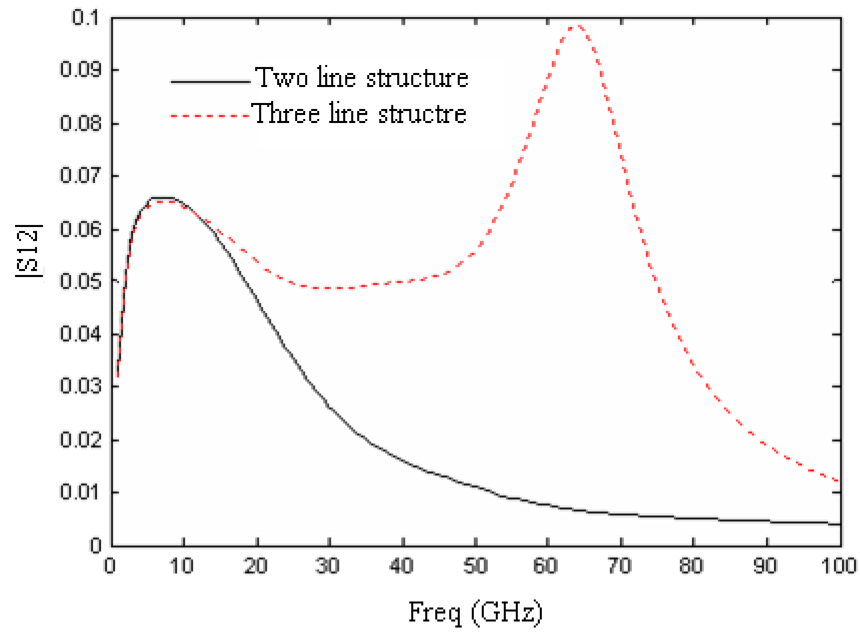

Fig.2.32. $|S_{12}|$ in frequency range of 1-100GHz for two and three line structures

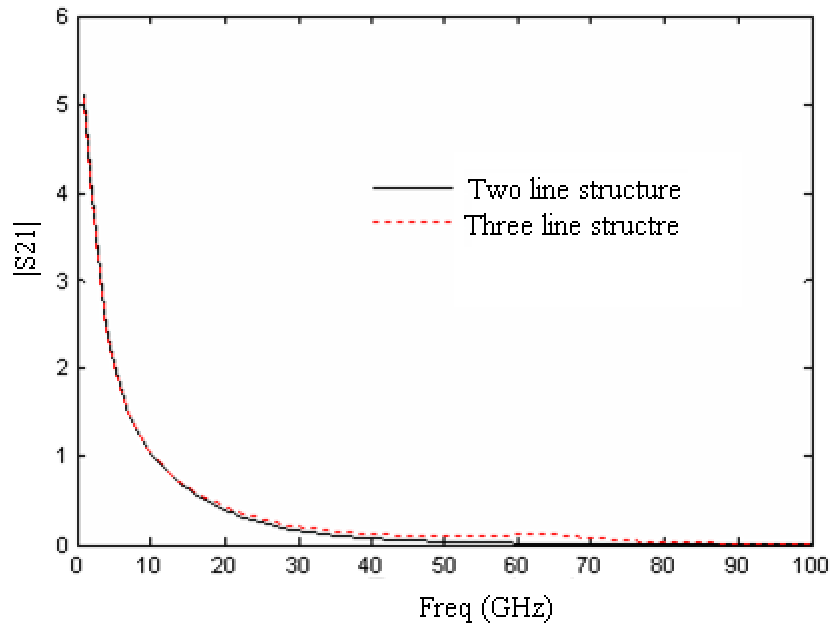

Fig.2.33 $|S_{21}|$ in frequency range of 1-100GHz for two and three line structures

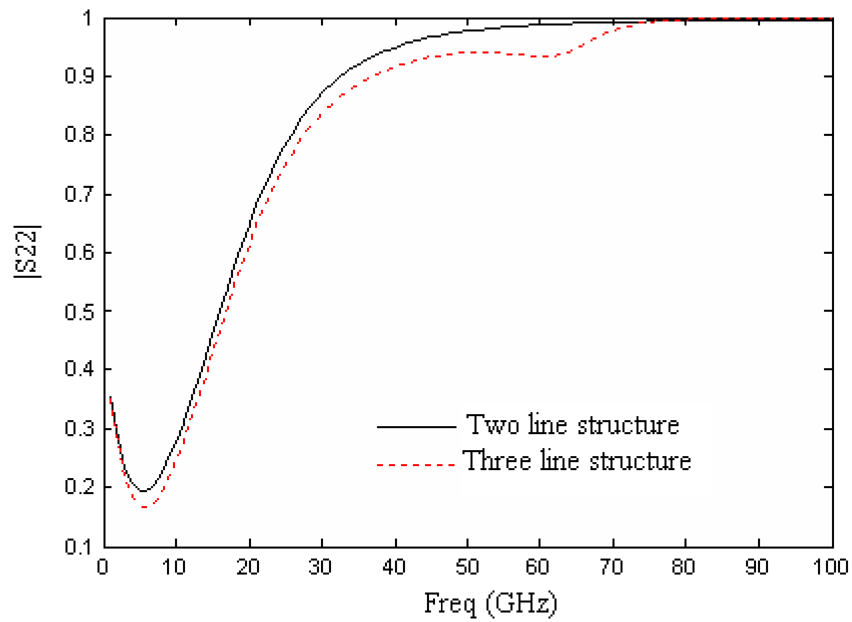

Fig.2.34 $|S_{22}|$ in frequency range of 1-100GHz for two and three line structures

2.6 FET Modeling Considering the Skin Effect

Skin effect impedance of interconnect conductors is usually insignificant in slower speed systems but cannot be neglected in millimeter-wave frequency range. In fact, the conductor resistance increases as the square root of frequency as the current crowds closer to the conductor surfaces [16].

The effective conductivity of the dielectric surrounding the conductors exhibits frequency dependence, which is primarily due to polarization loss. The time-domain analysis of transmission line equations is relatively simple where the lines are considered lossless. It becomes significantly more complicated for lossy transmission lines.

A primary reason is that the resistive losses of the device electrodes are due to skin effect and vary with frequency as $\sqrt{f}$. In this work, the skin effect is approximated by [7]

$$Z_i(x,s) = A(x) + B(x)\sqrt{s} \tag{2-32}$$

i.e., the internal impedance contains both resistance and internal inductance. The s variable is the Laplace transform variable.

2.6.1 Lossy Transmission Line Equations

An equivalent circuit of an infinitely small segment of the transistor is shown in Fig.2.35. By applying the Kirchhoff's laws to the conventional FET circuit of Fig.2.35, The TL equations in frequency-domain are given by [19]:

$$\begin{aligned} &\frac{\partial}{\partial x}[I(x,s)] + s[C][V(x,s)] + [G][V(x,s)] = 0 \\ &\frac{\partial}{\partial x}V[(x,s)] + s[L][I(x,s)] + [Z_i(s)][I(x,s)] = 0 \end{aligned} \tag{2-33}$$

where

$$[G]=\begin{bmatrix} G_{ds} & \dfrac{G_m}{1+sR_iC_{gs}} & \dfrac{-G_m}{1+sR_iC_{gs}}-G_{ds} \\ 0 & \dfrac{sC_{gs}}{1+sR_iC_{gs}} & \dfrac{-sC_{gs}}{1+sR_iC_{gs}} \\ -G_{ds} & \dfrac{-G_m-sC_{gs}}{1+sR_iC_{gs}} & \dfrac{G_m+sC_{gs}}{1+sR_iC_{gs}}+G_{ds} \end{bmatrix} \tag{2-34}$$

$$[C]=\begin{bmatrix} C_{11} & -C_{12} & -C_{13} \\ -C_{12} & C_{22} & 0 \\ -C_{13} & 0 & C_{33} \end{bmatrix} \tag{2-35}$$

$$[\mathrm{V}(x,s)]=\begin{bmatrix} V_d(x,s) \\ V_g(x,s) \\ V_s(x,s) \end{bmatrix} \quad [\mathrm{I}(x,s)]=\begin{bmatrix} I_d(x,s) \\ I_g(x,s) \\ I_s(x,s) \end{bmatrix} \tag{2-36}$$

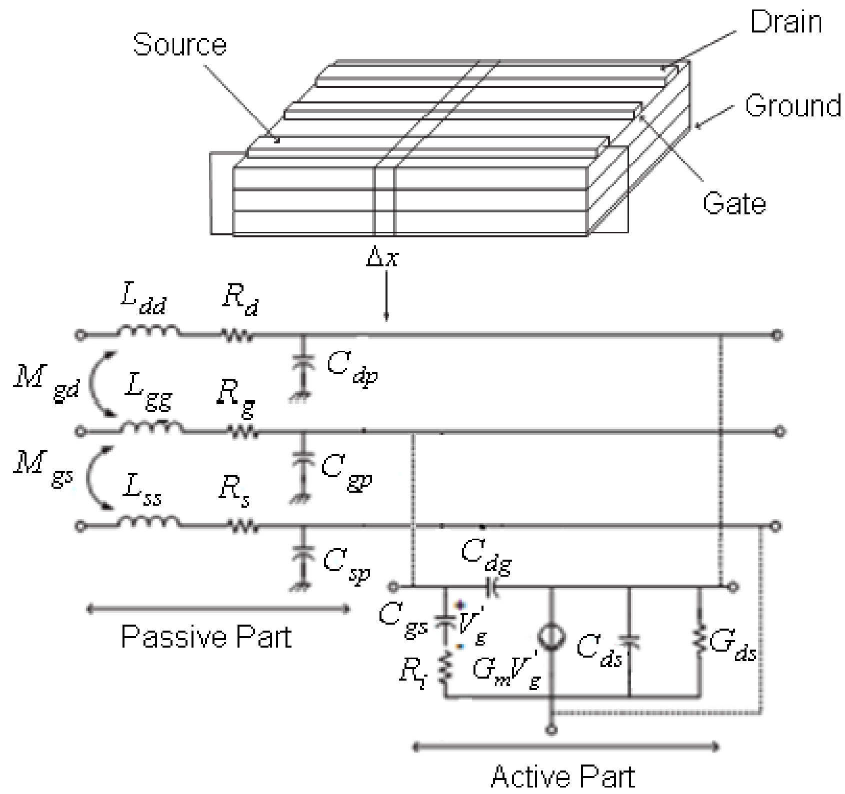

Fig.2.35. The different parts of a segment in the distributed model.

[V] and **[I]** are vectors of the line voltages and line currents, respectively. The internal impedance contains both resistance and internal inductance (due to magnetic flux internal to the conductors) as

$$[Z_i(s)] = [R(s)] + s[L_i(s)] \tag{2-37}$$

2.6.2 Numerical Solution of Lossy Transmission Lines

According to (2-11), the lossy TL equations in time-domain become [12]

$$\begin{aligned} &\frac{\partial}{\partial x}[\mathrm{I}'(x,t)] + [\mathrm{C}]\frac{\partial}{\partial t}[\mathrm{V}'(x,t)] + [\mathrm{G}][\mathrm{V}'(x,t)] = 0 \\ &\frac{\partial}{\partial x}[\mathrm{V}(x,t)] + [\mathrm{L}]\frac{\partial}{\partial t}[\mathrm{I}(x,t)] + [\mathrm{Z}_i(t)]*[\mathrm{I}(x,t)] = 0 \end{aligned} \tag{2-38}$$

Since the product of the internal impedance and the current in Eq. (2.33) can be translated in time domain to a convolution as

$$[Z_i(s)][I(x,s)] \quad \Leftrightarrow \quad [Z_i(t)]*[I(x,t)] \tag{2-39}$$

Substituting the skin effect approximation in Eq. (2-39) gives

$$\begin{aligned} &[\mathrm{Z}_i(t)]*[\mathrm{I}(x,t)] = \mathscr{L}^{-1}([\mathrm{A}] + [\mathrm{B}]\sqrt{s})*[\mathrm{I}(x,t)] = \\ &[\mathrm{A}][\mathrm{I}(x,t)] + [\mathrm{B}]\mathscr{L}^{-1}(\sqrt{s})*[\mathrm{I}(x,t)] = [\mathrm{A}][\mathrm{I}(x,t)] + [\mathrm{B}]\mathscr{L}^{-1}(\frac{1}{\sqrt{s}})*\frac{\partial}{\partial t}[\mathrm{I}(x,t)] \end{aligned} \tag{2-40}$$

where $\mathscr{L}^{-1}$ is considered here as the Inverse Laplace transform. Since the inverse Laplace transform of $\frac{1}{\sqrt{s}}$ is [7]:

$$\mathscr{L}^{-1}(\frac{1}{\sqrt{s}}) = \frac{1}{\sqrt{\pi t}} \tag{2-41}$$

we obtain,

$$[\mathrm{Z}_i(t)]*[\mathrm{I}(x,t)] = [\mathrm{A}][\mathrm{I}(x,t)] + [\mathrm{B}]\int_0^t \frac{1}{\sqrt{\pi u}} \underbrace{\frac{\partial}{\partial(t-u)}[\mathrm{I}(x,t-u)]}_{\mathrm{K}(x,t-u)} du \tag{2-42}$$

Applying the finite difference approximation to Eq. 2.38 gives:

$$\frac{1}{\Delta x}\left([I'^{n+1/2}_{k}]-[I'^{n+1/2}_{k-1}]\right)+\frac{1}{\Delta t}[\mathrm{C}]\left([V'^{n+1}_{k}]-[V'^{n}_{k}]\right)+\frac{1}{2}[\mathrm{G}]\left([\mathrm{V}'^{\mathrm{n+1}}_{\mathrm{k}}]+[\mathrm{V}'^{\mathrm{n}}_{\mathrm{k}}]\right)=0 \tag{2-43}$$

The finite difference approximation of convolution in (2.42) becomes

$$\int_0^t \frac{1}{\sqrt{\pi u}}\underbrace{\frac{\partial}{\partial(t-u)}\mathrm{I}(,t-u)}_{\mathrm{K}(z,t-u)}du \approx \int_0^{(n+1)\Delta t}\frac{1}{\sqrt{\pi u}}\mathrm{K}(x,(n+1)\Delta t-u)\,du \tag{2-44}$$

The function K(t) is approximated as constant over the time segment [16], so

$$\int_0^{(n+1)\Delta t}\frac{1}{\sqrt{\pi u}}K(x,(n+1)\Delta t-u)du \cong$$
$$\sum_{m=0}^{n}\int_{m\Delta t}^{(m+1)\Delta t}\mathrm{K}\left(x,\left(n-m+1\right)\Delta t\right)\frac{1}{\sqrt{\pi u}}du \cong \sqrt{\frac{\Delta t}{\pi}}\sum_{m=0}^{n}\mathrm{K}\left(x,\left(n-m+1\right)\Delta t\right)\int_{m\Delta t}^{(m+1)\Delta t}\frac{1}{\sqrt{\pi u}}du =$$
$$\sqrt{\frac{\Delta t}{\pi}}\sum_{m=0}^{n}\mathrm{K}(x,\left(n-m+1\right)\Delta t)\mathrm{F}_{\circ}(m)=\sqrt{\frac{\Delta t}{\pi}}\sum_{m=0}^{n}\frac{\mathrm{I}_k^{n-m+3/2}-\mathrm{I}_k^{n-m+1/2}}{\Delta t}F_{\circ}(m) \tag{2-45}$$

where

$$F_{\circ}(m)=\int_m^{m+1}\frac{1}{\sqrt{u}}du \tag{2-46}$$

Applying the finite difference approximation to Eq. 2.38 and substituting into Eq.2.45 leads to:

$$\frac{1}{\Delta x}\left([V^{n+1}_{k+1}]-[V^{n+1}_{k}]\right)+\frac{1}{\Delta t}[\mathrm{L}]\left([I^{n+3/2}_{k}]-[I^{n+1/2}_{k}]\right)+\frac{1}{2}[\mathrm{A}]\left([\mathrm{I}^{\mathrm{n+3/2}}_{\mathrm{k}}]+[\mathrm{I}^{\mathrm{n+1/2}}_{\mathrm{k}}]\right)$$
$$+\frac{1}{\sqrt{\pi\Delta t}}\sum_{m=0}^{n}F_0(m)\left([I_k^{n-m+3/2}]-[I_k^{n-m+3/2}]\right)=0 \tag{2-47}$$

Solving equations (2.43) and (2.47) gives the required recursive relations for the device electrodes

Thus,

$$[\mathrm{I}_k^{n+3/2}] = \left(\frac{1}{\Delta t}[L] + \frac{1}{2}[A] + \frac{F_\circ(0)}{\sqrt{\pi\Delta t}}[B]\right)^{-1} \left\{ \begin{array}{l} \left(\frac{1}{\Delta t}[L] - \frac{1}{2}[A] + \frac{F_\circ(0)}{\sqrt{\pi\Delta t}}[B]\right)[\mathrm{I}_k^{n+1/2}] - \frac{1}{\Delta x}([V_{k+1}^{n+1}] - [V_k^{n+1}] \\ - \frac{1}{\sqrt{\pi\Delta t}} B \sum_{m=1}^{n} F_\circ(m)\left([I_k^{n-m+3/2} - I_k^{n-m+1/2}]\right) \end{array} \right\}$$

(2-48)

$$[\mathrm{V}_k'^{n+1}] = \left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G]\right)^{-1} \left\{ \left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G\}\right)[\mathrm{V}_k'^{n}] - \frac{1}{\Delta x}([I'^{n+1/2}_k] - [I'^{n+1/2}_{k-1}]) \right\} \quad (2\text{-}49)$$

In the next stage, the boundary condition should be applied to Eq. (2.48). This equation for $k = 1$ and $k = N_{x+1}$ (the beginning and the end of the electrode) becomes

- For $k = 1$

$$[\mathrm{V}_1'^{n+1}] = \left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G]\right)^{-1} \left\{ \left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G]\right)[\mathrm{V}_1'^{n}] - \frac{2}{\Delta x}([I'^{n+1/2}_1] - [I'^{n+1/2}_0] \right\} =$$

$$\left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G] + \frac{1}{\Delta x}[R_s^{'}]^{-1}\right) \left\{ \begin{array}{l} \left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G] - \frac{1}{\Delta x}[R_s^{'}]^{-1}\right)[V'^{n}_1] \\ -\frac{2}{\Delta x}\left([I'^{n+1/2}_1] - \frac{1}{2}[R_s^{'}]([V'^{n}_{in}] - [V'^{n+1}_{in}])\right) \end{array} \right\} \quad (2\text{-}50)$$

- For $k = 2, .., Nx$

$$[\mathrm{V}_k'^{n+1}] = \left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G]\right)^{-1} \left\{ \left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G]\right)[\mathrm{V}_k'^{n}] - \frac{1}{\Delta x}([I'^{n+1/2}_k] - [I'^{n+1/2}_{k-1}] \right\} \quad (2\text{-}51)$$

- For $k = Nx+1$

$$[\mathrm{V}_{Nx+1}'^{n+1}] = \left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G]\right)^{-1} \left\{ \left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G]\right)[\mathrm{V}_{Nx+1}'^{n}] - \frac{2}{\Delta x}([I'^{n+1/2}_{Nx+1}] - [I'^{n+1/2}_{Nx}] \right\} =$$

$$\left(\frac{1}{\Delta t}[C] + \frac{1}{2}[G] + \frac{1}{\Delta x}[R_L^{'}]^{-1}\right) \left\{ \left(\frac{1}{\Delta t}[C] - \frac{1}{2}[G] - \frac{1}{\Delta x}[R_L^{'}]^{-1}\right)[V'^{n}_{Nx+1}] + \frac{2}{\Delta x}\left([I'^{n+1/2}_{Nx}]\right) \right\} \quad (2\text{-}52)$$

2.6.3 Numerical Results

This procedure was used to model the NE710 while taking into account the skin effects. Thus, input and output nodes were connected to the beginning and the end of the gate and the drain electrode, respectively. The source electrode is grounded at the beginning and the end of the electrode. The transistor was biased at V_{ds}=3V, I_{ds}=10mA. The values for the device dimensions and material constant of the device were chosen as follows [16]:

Source length (l_s) = drain length (l_d) = 24 µm;

Gate length (l_g) = 0.3 µm, electrode height (h) = 140 µm;

Source–gate separation (d) = 2 µm;

Drain–gate separation (d') = 2 µm;

Gate width = 280 µm, $t_d = t_g = t_s = 0.2$ µm;

$\varepsilon_r = 12.9$, $\sigma_m = 4 \times 10^7$ S/m.

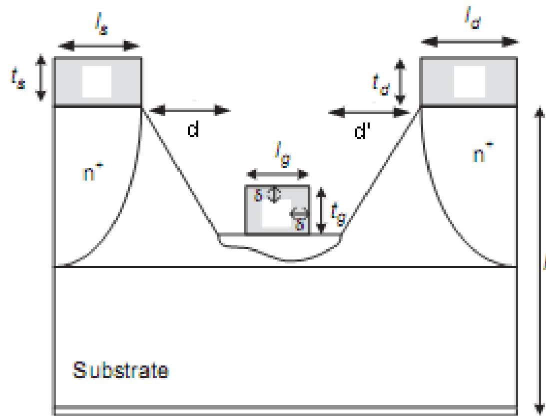

Fig. 2.36. Cross-section structure of the FET. The gray areas show effective current path at the high frequency. δ indicates the skin depth

The cross-section of the transistor is shown in Fig.2.33. The transistor is terminated at the beginning and the end of gate and drain electrodes with 50Ω loads.

First, the transistor is excited by a 1-mV pulse with a 10 ps rise/fall time and a width of 10 ps. The per-unit-length dc resistance of the electrodes (A) and the B factor (from Eq 2.32.) are computed using [17]:

$$[A]=\begin{bmatrix}\frac{1}{\sigma t_d l_d} & 0 & 0\\ 0 & \frac{1}{\sigma t_g l_g} & 0\\ 0 & 0 & \frac{1}{\sigma t_s l_s}\end{bmatrix}=\begin{bmatrix}5.2083\times10^3 & 0 & 0\\ 0 & 4.1667\times10^3 & 0\\ 0 & 0 & 5.2083\times10^3\end{bmatrix}\frac{\Omega}{m}$$

(2-53)

$$[B]=\sqrt{\frac{\mu}{\sigma}}\begin{bmatrix}\frac{1}{2(t_d+l_d)} & 0 & 0\\ 0 & \frac{1}{2(t_g+l_g)} & 0\\ 0 & 0 & \frac{1}{2(t_s+l_s)}\end{bmatrix}=\begin{bmatrix}0.0158 & 0 & 0\\ 0 & 0.1772 & 0\\ 0 & 0 & 0.0158\end{bmatrix}\frac{\Omega}{m\sqrt{Hz}}$$

(2-54)

Figs.2.38 and 2.39 show the voltage waveform of the transistor at the beginning of gate and drain, respectively. While the skin effect is considered in the simulation of the transistor behavior, these results are compared with the results of the transistor without skin effect. Figs.2.40 and 2.41 depict the voltage at the end of the gate and drain electrodes, respectively.

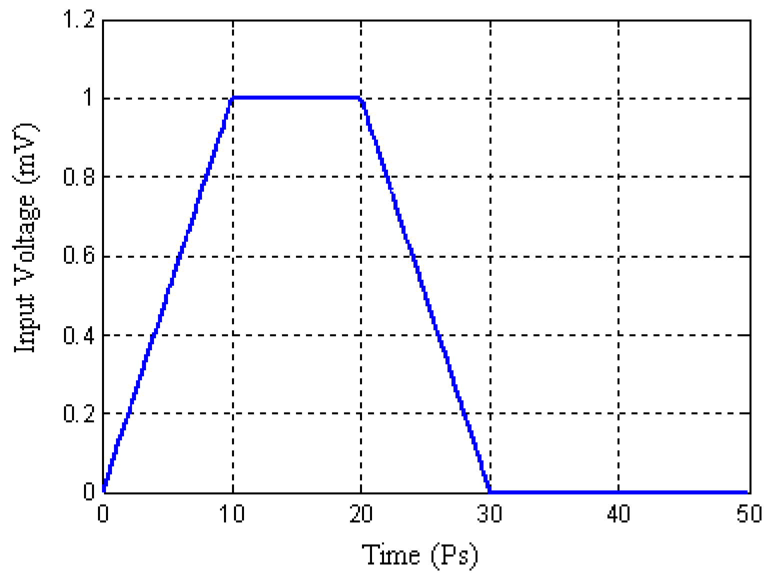

Fig.2.37. AC waveform of the input voltage (1mv pulse with a 10 ps rise/fall time and a width of 10 ps)

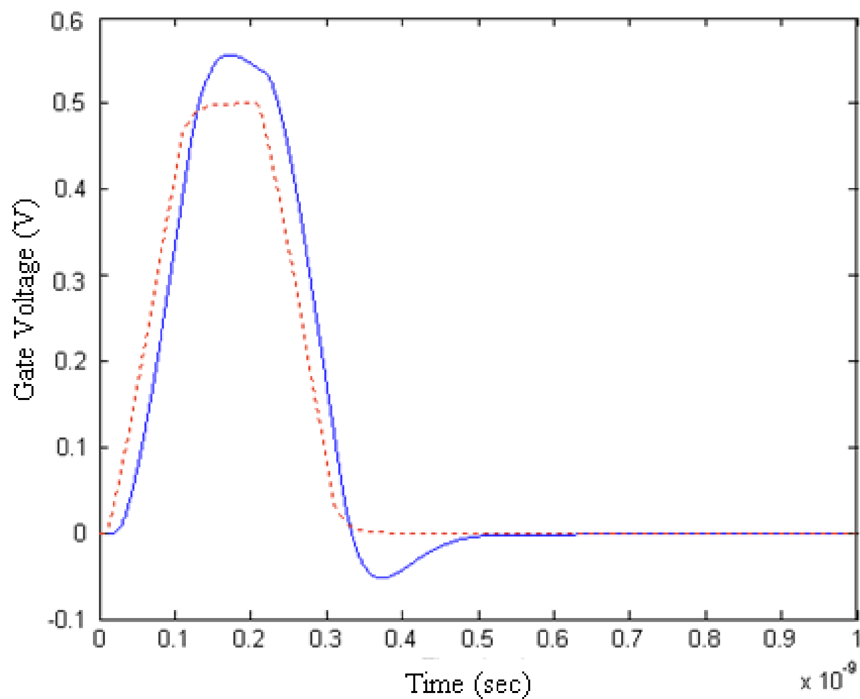

Fig.2.38 AC waveform of the voltage at the beginning of the gate electrode for a transistor with skin effect losses (dashed-line) and without skin effect losses (solid-line)

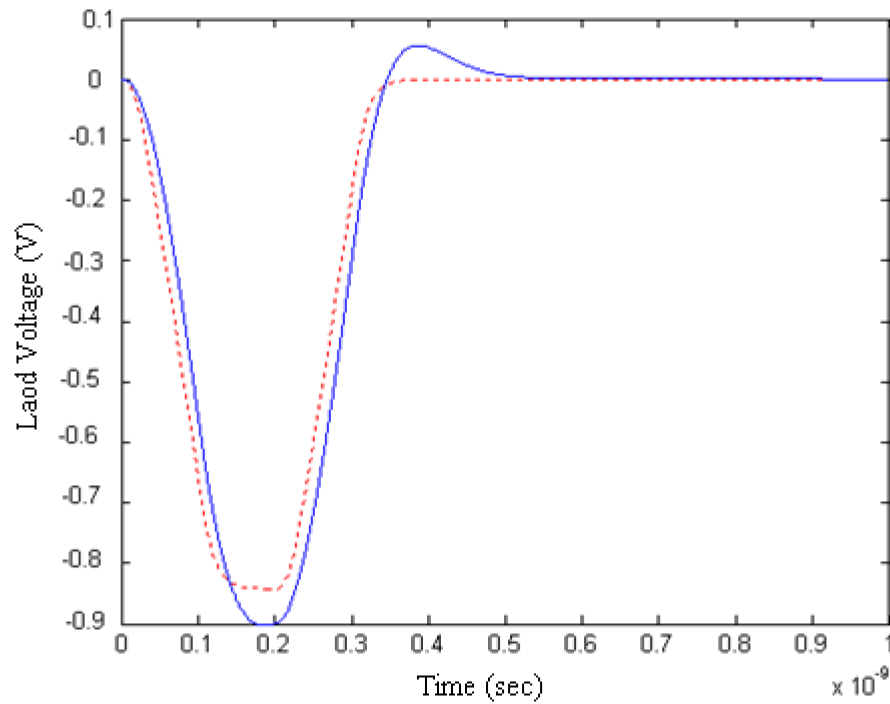

Fig.2.39. AC waveform of the voltage at the beginning of the drain electrode for a transistor with skin effect losses (dashed-line) and without skin effect losses (solid-line)

Due to the skin effect, a high-frequency resistance and inductance is added to the low-frequency resistance and inductance. Therefore, there is a phase shift and a magnitude reduction between lossy and lossless active transmission lines. This is clearly shown in Figs.2.40 and 2.41. The comparison between these excitation shows why the skin effect should be considered in high-frequency device modeling.

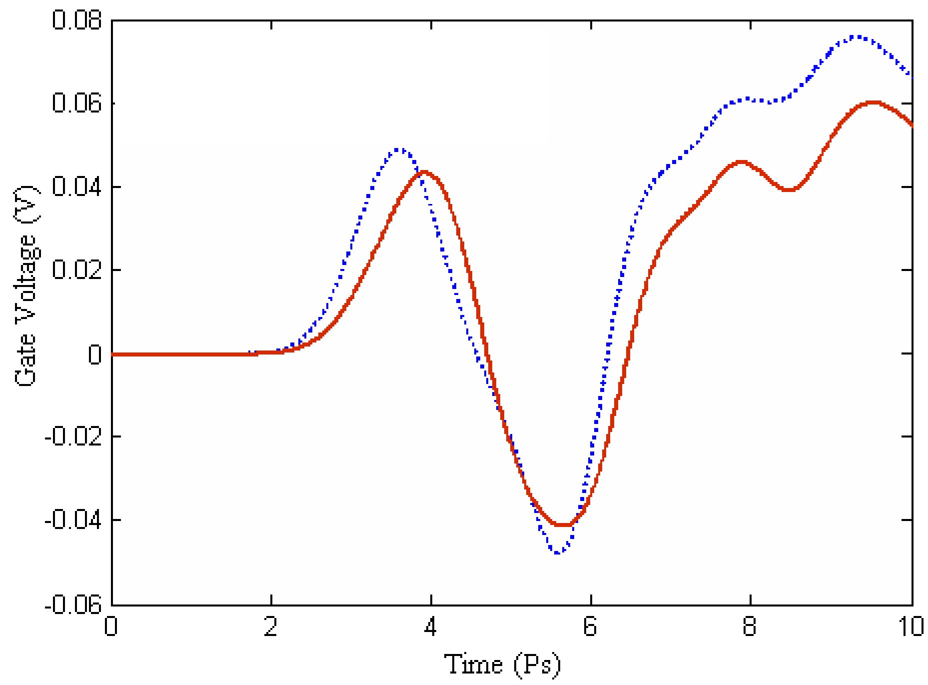

Fig.2.40. AC waveform of the voltage at the end of the gate electrode for a transistor with skin effect losses (dashed-line) and without skin effect losses (solid-line)

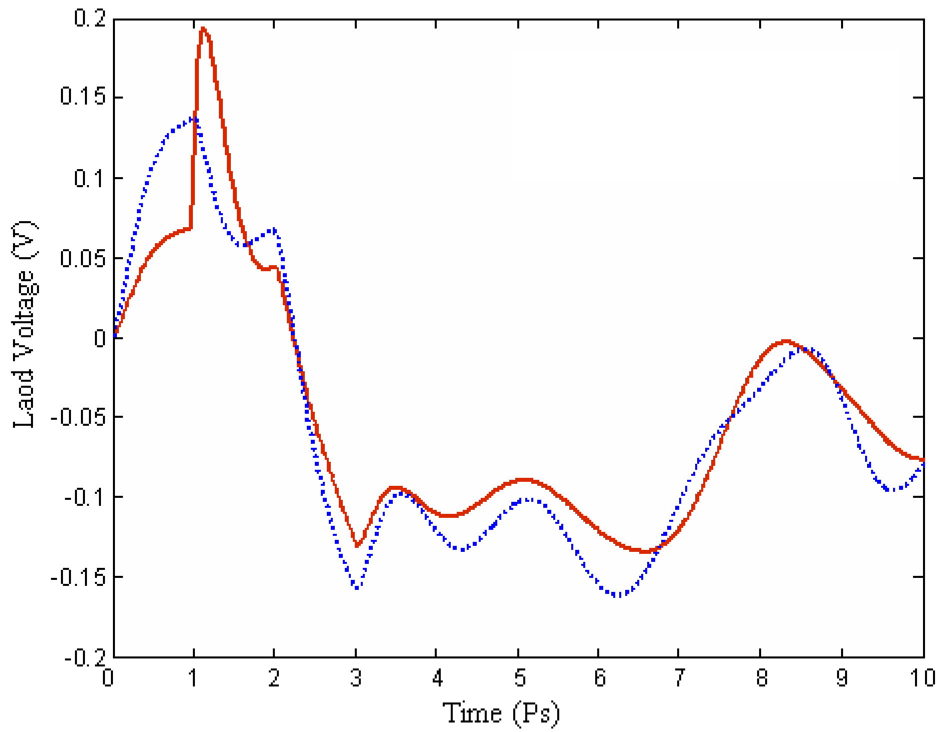

Fig.2.41. AC waveform of the voltage at the end of the drain electrode for a transistor with skin effect losses (dashed-line) and without skin effect losses (solid-line)

2.7 Conclusion

A new approach for analyzing microwave field effect transistors has been presented. This new method can accurately consider the effect of wave propagation along the device electrodes. The derived equation was solved using the FDTD technique. The results show that by increasing the frequency up to the mm-wave range, difference appears between the proposed model and the S.D model. This is due to the wave propagation and phase cancellation effects. We discussed the measurement frequency range and explained why our model should be more suitable for such frequency range. Also, the model shows to be easily scalable to predict different-size device behaviors.

The proposed FET model extends the ability to predict modeled device parameters to high frequencies for any gate width. Normally gate widths are kept to a minimum to avoid loss and standing waves on the gate line. This new mode allows prediction of larger gate-width. Besides, the influence of the different loads in the both ends of the gate and the drain for mm-wave FETs have been analyzed which shows that a proper loading causes to a device with good signal and noise characteristics.

We also highlighted the impedance skin effect of the FET electrode conductors in a transistor behavior. Such effect is often neglected in the analysis of FETs, leading to non accurate models in high frequencies. In fact, as the current crowds closer to the conductor surfaces, this effect is manifested by an increase in the electrode conductor resistance as the square root of frequency. In addition, a portion of the magnetic flux internal to the conductors gives rise to an internal inductance of the conductor that decreases as the square root of frequency. Thus, the time domain analysis of lossy transmission lines becomes significantly more difficult since the resistive losses of the device electrodes due to skin effect vary with frequency as $\sqrt{f}$. Then, a new method for time domain analysis of TL equations including skin effect was proposed.

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Chapter 3 Nonlinear FET Modeling and Analysis

3.1 Introduction

In the previous chapter, the transistor model shown in Fig.2.4 was assumed to be linear. However, in nonlinear circuits such as oscillators, mixers, high-power amplifiers, and frequency multipliers …, harmonics of the excitation source will be generated in the circuit. Hence, the effect of wave propagation along the device electrodes will have a more significant influence on the circuit performance as compared to a linear circuit. In such cases, for accurate modeling, the wave propagation nonlinear effect needs to be considered in the device modeling [1]-[3].

Thus, we introduce in this chapter a nonlinear active multiconductor transmission line equation by considering the distributed effect at the source electrode [4]-[7]. To obtain these equations, the device width was first divided into infinity segments. Each segment was considered as a system with a combination of three coupled lines and a nonlinear FET equivalent circuit. To do so, we used the well-known Curtice cubic model [8], reaching to a system of nonlinear differential equations. Here again, the FDTD technique was used to solve the nonlinear equations and the results compared with the lumped model at several bias points.

3.2 Nonlinear Active Transmission Line Equation

As in the previous chapter, the transistor is divided into two passive and active part and the active transmission line equations can be generalized using the proposed modeling approach.

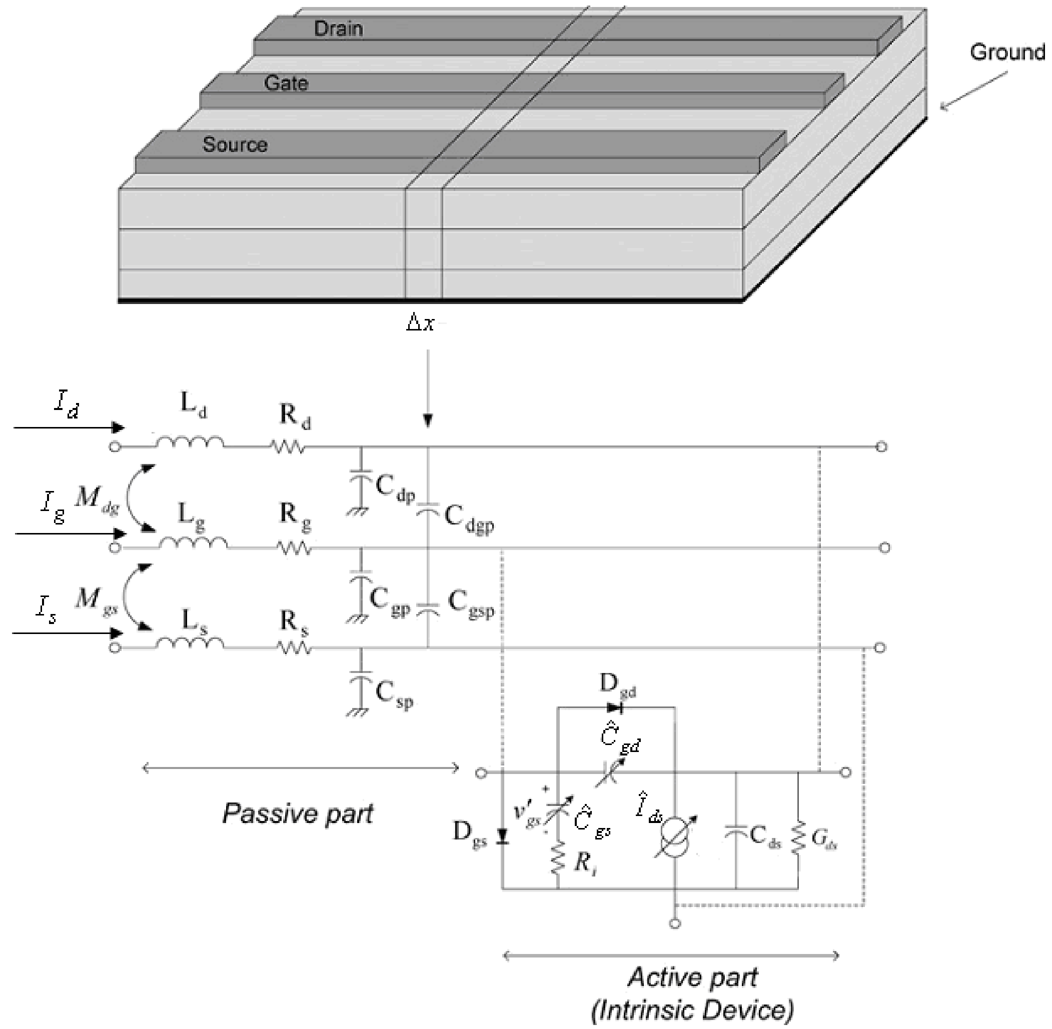

Fig.3.1 Different parts of a differential slice in the proposed nonlinear distributed model ("$\wedge$" represents nonlinear elements)

A differential section of the device is shown in (Fig.3.1). It combines a passive part and an active part that describe the electromagnetic interaction between the coupled lines and the intrinsic device in nonlinear regime, respectively. By considering the left loop of the circuit shown in Fig.3.1 with $\Delta x \to 0$, we obtain the following three equations [4], [9]

$$\frac{\partial I_d(x,t)}{\partial x} + \widehat{C}_{11}\frac{\partial V_d(x,t)}{\partial t} - \widehat{C}_{12}\frac{\partial V_g(x,t)}{\partial t} - C_{13}\frac{\partial V_s(x,t)}{\partial t} + G_m V'_g(x,t) + G_{ds}(V_d(x,t) - V_s(x,t)) + \widehat{I}_{ds} = 0 \tag{3-1}$$

$$\frac{\partial I_g(x,t)}{\partial x} + \widehat{C}_{22}\frac{\partial V_g(x,t)}{\partial t} - \widehat{C}_{12}\frac{\partial V_d(x,t)}{\partial t} - C_{23}\frac{\partial V_s(x,t)}{\partial t} + \widehat{C}_{gs}\frac{\partial V'_g(x,t)}{\partial t} = 0 \qquad (3\text{-}2)$$

$$\frac{\partial I_s(x,t)}{\partial x} + C_{33}\frac{\partial V_s(x,t)}{\partial t} - C_{23}\frac{\partial V_g(x,t)}{\partial t} - \widehat{C}_{13}\frac{\partial V_d(x,t)}{\partial t} - \widehat{C}_{gs}\frac{\partial V'_g(x,t)}{\partial t} - G_m V'_g(x,t) + G_{ds}(V_s(x,t) - V_d(x,t)) - \widehat{I}_{ds} = 0 \qquad (3\text{-}3)$$

where

$\widehat{C}_{11} = C_{dp} + C_{ds} + C_{dsp} + \widehat{C}_{dg} + C_{dgp}$ $\qquad$ $\widehat{C}_{22} = C_{gp} + C_{gsp} + \widehat{C}_{dg} + C_{dgp}$

$C_{33} = C_{sp} + C_{ds} + C_{dsp} + C_{gsp}$ $\qquad$ $C_{23} = C_{gsp}$

$\widehat{C}_{12} = \widehat{C}_{dg} + C_{dgp}$ $\qquad$ $C_{13} = C_{ds} + C_{dsp}$

Similarly, by applying the Kirchhoff's law to the main node of the circuit with $\Delta x \to 0$, we obtain

$$\frac{\partial V_d(x,t)}{\partial x} + R_d I_d(x,t) + L_{dd}\frac{\partial I_d(x,t)}{\partial t} + M_{gd}\frac{\partial I_g(x,t)}{\partial t} + M_{ds}\frac{\partial I_s(x,t)}{\partial t} = 0 \qquad (3\text{-}4)$$

$$\frac{\partial V_g(x,t)}{\partial z} + R_g I_g(x,t) + L_{gg}\frac{\partial I_g(x,t)}{\partial t} + M_{gd}\frac{\partial I_d(x,t)}{\partial t} + M_{gs}\frac{\partial I_s(x,t)}{\partial t} = 0 \qquad (3\text{-}5)$$

$$\frac{\partial V_s(x,t)}{\partial z} + R_s I_s(x,t) + L_{ss}\frac{\partial I_s(x,t)}{\partial t} + M_{ds}\frac{\partial I_d(x,t)}{\partial t} + M_{gs}\frac{\partial I_g(x,t)}{\partial t} = 0 \qquad (3\text{-}6)$$

We can also write another equation as follows

$$V'_g(x,t) + V_s(x,t) + R_i\widehat{C}_{gs}\frac{\partial V'_g(x,t)}{\partial t} - V_g(x,t) = 0 \qquad (3\text{-}7)$$

where I_d, V_d, I_g, V_g and I_s, V_s are the drain, gate and source currents and voltages, respectively; V_g' is the gate-source capacitance voltage, and $\widehat{I}_{ds}$ the drain–source current.

The Curtice cubic nonlinear model was selected to model the active part [8]. In this model, the drain–source current ($\widehat{I}_{ds}$) is formulated as

$$\widehat{I}_{ds} = I_{ds0} \tanh(\gamma V_{ds}) \tag{3-8}$$

with

$$I_{ds0} = A_0 + A_1 v_1 + A_2 v_1^2 + A_3 v_1^3$$

where

$$v_1 = \begin{cases} V_{gs}(1+\beta(V_{out0} - V_{ds})) & V_{ds} \geq 0 \\ V_{gd}(1+\beta(V_{out0} + V_{ds})) & V_{ds} < 0 \end{cases}$$

γ is the saturation parameter. β models the pinch-off voltage dependence on the drain-source voltage. Parameters A_0, A_1, A_2 and A_3 are polynomial fitting coefficients, and V_{out0} is the drain-source voltage at which the polynomial coefficients are evaluated. v_p is pinch-off voltage. Note that for values of v_1 below the maximum pinch-off voltage (v_{pmax}), $\widehat{I}_{ds}$ is replaced by

$$I_{ds0} = A_0 + A_1 v_p + A_2 v_p^2 + A_3 v_p^3$$

The drain–source and gate–drain charge and capacitance are formulated in the Curtice cubic as follows

If $V_{gs}^{'} < F_c V_{bi}$,

$$\tilde{Q}_{gs} = 2V_{bi}\, C_{gso} \left[1 - \sqrt{1 - \frac{V'_{gs}}{V_{bi}}} \right] \tag{3-9}$$

$$\tilde{C}_{gs} = \frac{\partial \tilde{Q}_{gs}}{\partial V'_{gs}} = \frac{C_{gso}}{\sqrt{1 - \frac{V'_{gs}}{V_{bi}}}} \tag{3-10}$$

If $V'_{gs} > F_c V_{bi}$,

$$\tilde{Q}_{gs} = 2V_{bi} C_{gso} \left[1 - \sqrt{1 - F_c}\right] + \frac{C_{gso}}{\sqrt[3]{1 - F_c}} \left[\left(1 - \frac{3F_c}{2}\right)\left(V'_{gs} - F_c V_{bi}\right)\left(\frac{V'^{2}_{gs} - \left(F_c V_{bi}\right)^2}{4V_{bi}}\right)\right] \tag{3-11}$$

$$\tilde{C}_{gs} = \frac{\partial \tilde{Q}_{gs}}{\partial V'_{gs}} = \frac{C_{gso}}{\sqrt[3]{1 - F_c}} \left[1 - \frac{3F_c}{2} + \frac{V'_{gs}}{2V_{bi}}\right] \tag{3-12}$$

If $V'_{gd} < F_c V_{bi}$,

$$\tilde{Q}_{gd} = 2V_{bi} C_{gdo} \left[1 - \sqrt{1 - \frac{V_{gd}}{V_{bi}}}\right] \tag{3-13}$$

$$\tilde{C}_{gd} = \frac{\partial \tilde{Q}_{gd}}{\partial V_{gd}} = \frac{C_{gdo}}{\sqrt{1 - \frac{V_{gd}}{V_{bi}}}} \tag{3-14}$$

If $V'_{gd} > F_c V_{bi}$,

$$\tilde{Q}_{gd} = 2V_{bi} C_{gdo} \left[1 - \sqrt{1 - F_c}\right] + \frac{C_{gdo}}{\sqrt[3]{1 - F_c}} \left[\left(1 - \frac{3F_c}{2}\right)\left(V_{gd} - F_c V_{bi}\right)\left(\frac{V_{gd}^{2} - \left(F_c V_{bi}\right)^2}{4V_{bi}}\right)\right] \tag{3-15}$$

$$\tilde{C}_{gd} = \frac{\partial \tilde{Q}_{gd}}{\partial V_{gd}} = \frac{C_{gdo}}{\sqrt[3]{1 - F_c}} \left[1 - \frac{3F_c}{2} + \frac{V_{gd}}{2V_{bi}}\right] \tag{3-16}$$

Since the value of each element should be per unit length, some of the Curtice-cubic parameters should be converted into per unit parameters.

Equations (3-1)–(3-3) and (3-4)–(3-7) can be simplified into two matrix equations as

$$\frac{\partial}{\partial x}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \end{bmatrix} + \frac{\partial}{\partial t}\begin{bmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{bmatrix}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{bmatrix} + \begin{bmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{bmatrix}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{bmatrix} = 0 \quad (3\text{-}17)$$

$$\frac{\partial}{\partial x}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \\ 0 \end{bmatrix} + \frac{\partial}{\partial t}\begin{bmatrix} \widehat{C}_{11} & -\widehat{C}_{12} & -C_{13} & 0 \\ -\widehat{C}_{12} & \widehat{C}_{22} & -C_{23} & \widehat{C}_{gs} \\ -C_{13} & -C_{23} & \widehat{C}_{33} & -\widehat{C}_{gs} \\ 0 & 0 & 0 & R_i\,\widehat{C}_{gs} \end{bmatrix}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'(x,t)_g \end{bmatrix} +$$

$$\begin{bmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{bmatrix}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'_g(x,t) \end{bmatrix} + \begin{bmatrix} -\widehat{I}_{ds} \\ o \\ \widehat{I}_{ds} \\ 0 \end{bmatrix} = 0 \quad (3\text{-}18)$$

The nonlinear proposed model of an FET is embodied in the following equations

$$\frac{\partial[\mathrm{I}'(x,t)]}{\partial x} + [\widetilde{\mathrm{C}}](V_d, V_g, V_s, V'_{gs})\frac{\partial[\mathrm{V}'(x,t)]}{\partial t} + [\mathrm{G}][\mathrm{V}'(x,t)] + [\widetilde{\mathrm{I}}_{\mathrm{NL}}](V_d, V_g, V_s) = 0 \quad (3\text{-}19)$$

$$\frac{\partial[\mathrm{V}'(x,t)]}{\partial x} + [\mathrm{L}]\frac{\partial[\mathrm{I}'(x,t)]}{\partial t} + [\mathrm{R}][\mathrm{I}(x,t)] = 0 \quad (3\text{-}20)$$

where

$$[\mathrm{I}(x,\mathrm{t})] = \begin{bmatrix} I_d(x,t) & I_g(x,t) & I_s(x,t) \end{bmatrix}^t$$

$$[\mathrm{V}(x,\mathrm{t})] = \begin{bmatrix} V_d(x,t) & V_g(x,t) & V_s(x,t) \end{bmatrix}^t$$

$$[\widetilde{\mathrm{I}}_{\mathrm{NL}}(x,t)] = \begin{bmatrix} \widehat{I}_{ds} & 0 & -\widehat{I}_{ds} & 0 \end{bmatrix}^t$$

$$[\mathrm{V}'(x,\mathrm{t})] = \begin{bmatrix} V_d(x,t) & V_g(x,t) & V_s(x,t) & V'_{gs}(x,t) \end{bmatrix}^t$$

$$[\mathrm{I}'(x,\mathrm{t})] = \begin{bmatrix} I_d(x,t) & I_g(x,t) & I_s(x,t) & 0 \end{bmatrix}^t$$

and

$$[L]=\begin{bmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{bmatrix},\ [R]=\begin{bmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{bmatrix}$$

$$[\tilde{C}]=\begin{bmatrix} \widehat{C}_{11} & -\widehat{C}_{12} & -C_{13} & 0 \\ -\widehat{C}_{12} & \widehat{C}_{22} & -C_{23} & \widehat{C}_{gs} \\ -C_{13} & -C_{23} & \widehat{C}_{33} & -\widehat{C}_{gs} \\ 0 & 0 & 0 & R_i\,\widehat{C}_{gs} \end{bmatrix} [G]=\begin{bmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{bmatrix}$$

Note that these first order nonlinear partial differential equations are coupled. Here the superscript $[]^t$ stands for the matrix transpose.

3.3 Solutions of the Nonlinear Equations

As in chapter 2, The FDTD technique was used to discretize the above equations [13]-[15]. Thus, each voltage and adjacent current solution point is separated by $\Delta x/2$. In addition, the time points are also interlaced, and each voltage time point and adjacent current time point are separated by $\Delta t/2$. To ensure the stability of the discretization and the second-order accuracy, we interlace the $N_x + 1$ voltage points, V_1, V_2, . . . , V_{Nx} , V_{Nx+1}, and the N_x current points, I_1, I_2, . . . , I_{Nx}. Discretizing the derivatives in the nonlinear equations using the proposed algorithm gives

$$\frac{1}{\Delta x}\left([I'^{n+1/2}_{k}]-[I'^{n+1/2}_{k-1}]\right)+\frac{1}{\Delta t}[\hat{C}]\left([V'^{n+1}_{k}]-[V'^{n}_{k}]\right) + \frac{1}{2}[\mathrm{G}]\left([\mathrm{V}'^{\mathrm{n}+1}_{\mathrm{k}}]+[\mathrm{V}'^{\mathrm{n}}_{\mathrm{k}}]\right)+[\hat{I}'_{NL}]=0 \qquad k = 1, 2\ldots N_x + 1 \qquad (3\text{-}21)$$

$$\frac{1}{\Delta x}\left([V^{n+1}_{k+1}]-[V^{n+1}_{k}]\right)+\frac{1}{\Delta t}[\mathrm{L}]\left([I^{n+3/2}_{k}]-[I^{n+1/2}_{k}]\right) + \frac{1}{2}[\mathrm{R}]\left([\mathrm{I}^{\mathrm{n}+3/2}_{\mathrm{k}}]+[\mathrm{I}^{\mathrm{n}+1/2}_{\mathrm{k}}]\right)=0 \qquad k = 1, 2\ldots N_x + 1 \qquad (3\text{-}22)$$

with

$$[V_i^j] \equiv [V((i-1)\Delta x, j\Delta t)]$$

$$[V_i'^j] \equiv [V'((i-1)\Delta x, j\Delta t)]$$

$$[I_i^j] \equiv [I((i-\frac{1}{2})\Delta x, j\Delta t)]$$

$$[I_i'^j] \equiv [I'((i-\frac{1}{2})\Delta x, j\Delta t)]$$

$$I'_{NL} \equiv \begin{bmatrix} I'_{ds} & 0 & -I'_{ds} & 0 \end{bmatrix}^T$$

where

$$\tilde{I}'_{ds} = I'_{dso} \tanh\left(\gamma \frac{V_{dk}^n + V_{dk}^{n+1} - V_{sk}^n - V_{sk}^{n+1}}{2}\right) \quad (3\text{-}23)$$

$$I'_{dso} = A_o + A_1 v'_1 + A_2 v'^2_1 + A_3 v'^3_1 \quad (3\text{-}24)$$

$$v'_1 = \begin{cases} \dfrac{V_{gk}^{n+1} + V_{gk}^n - V_{sk}^{n+1} - V_{sk}^n}{2}\left(1+\beta\left(V_{out0} - \dfrac{V_{dk}^{n+1} + V_{dk}^n - V_{sk}^{n+1} - V_{sk}^n}{2}\right)\right) & V_{gk}^{n+1} + V_{gk}^n \geq V_{sk}^{n+1} + V_{sk}^n \\ \dfrac{V_{gk}^{n+1} + V_{gk}^n - V_{dk}^{n+1} - V_{dk}^n}{2}\left(1+\beta\left(V_{out0} + \dfrac{V_{dk}^{n+1} + V_{dk}^n - V_{sk}^{n+1} - V_{sk}^n}{2}\right)\right) & V_{gk}^{n+1} + V_{gk}^n \prec V_{sk}^{n+1} + V_{sk}^n \end{cases}$$

For values of v'_1 below the maximum pinch-off voltage (v_{pmax}), $\hat{I}_{ds0}$ is replaced with the following expression

$$I'_{dso} = A_o + A_1 v_p + A_2 v_p^2 + A_3 v_p^3 \quad (3\text{-}25)$$

The drain–source and gate–drain charges and capacitances are modeled in the Curtice cubic model as

If $V_{gsk}^n + V_{gsk}^{n+1} > 2F_c V_{bi}$

and

$$\tilde{Q}_{gs} = 2V_{bi}\, C_{gso}\left[1 - \sqrt{1 - \frac{V_{gsk}^{n} + V_{gsk}^{n+1}}{2V_{bi}}}\right] \tag{3-26}$$

$$\tilde{C}_{gs} = \frac{\partial \tilde{Q}_{gs}}{\partial V'_{gs}} = \frac{C_{gso}}{\sqrt{1 - \frac{V_{gsk}^{n} + V_{gsk}^{n+1}}{2V_{bi}}}} \tag{3-27}$$

If $V_{gsk}^{n} + V_{gsk}^{n+1} < 2F_c V_{bi}$

$$\tilde{Q}_{gs} = 2V_{bi}\, C_{gso}\left[1 - \sqrt{1 - F_c}\right] + \frac{C_{gso}}{\sqrt[3]{1 - F_c}}\left[\left(1 - \frac{3F_c}{2}\right)\left(\frac{V_{gsk}^{n} + V_{gsk}^{n+1}}{2} - F_c V_{bi}\right)\left(\frac{\left(\frac{V_{gsk}^{n} + V_{gsk}^{n+1}}{2}\right)^2 - \left(F_c V_{bi}\right)^2}{4V_{bi}}\right)\right] \tag{3-28}$$

$$\tilde{C}_{gs} = \frac{\partial \tilde{Q}_{gs}}{\partial V'_{gs}} = \frac{C_{gso}}{\sqrt[3]{1 - F_c}}\left[1 - \frac{3F_c}{2} + \frac{V_{gsk}^{n+1} + V_{gsk}^{n}}{4V_{bi}}\right] \tag{3-29}$$

If $V_{gk}^{n} + V_{gk}^{n+1} - V_{dk}^{n} - V_{dk}^{n+1} < 2F_c V_{bi}$

$$\tilde{Q}_{gd} = 2V_{bi}\, C_{gdo}\left[1 - \sqrt{1 - \frac{V_{gk}^{n} + V_{gk}^{n+1} - V_{dk}^{n} - V_{dk}^{n+1}}{2V_{bi}}}\right] \tag{3-30}$$

$$\tilde{C}_{gd} = \frac{\partial \tilde{Q}_{gd}}{\partial V_{gd}} = \frac{C_{gdo}}{\sqrt{1 - \frac{V_{gk}^{n} + V_{gk}^{n+1} - V_{dk}^{n} - V_{dk}^{n+1}}{2V_{bi}}}} \tag{3-31}$$

If $V_{gk}^{n}+V_{gk}^{n+1}-V_{dk}^{n}-V_{dk}^{n+1}>2F_c V_{bi}$

$$\tilde{Q}_{gd}=2V_{bi}\,C_{gdo}\left[1-\sqrt{1-F_c}\right]+\frac{C_{gdo}}{\sqrt[3]{1-F_c}}\left[\left(1-\frac{3F_c}{2}\right)\left(\frac{V_{gk}^{n}+V_{gk}^{n+1}-V_{dk}^{n}-V_{dk}^{n+1}}{2}-F_c\,V_{bi}\right)\times\left(\frac{\left(\frac{V_{gk}^{n}+V_{gk}^{n+1}-V_{dk}^{n}-V_{dk}^{n+1}}{2}\right)^2-\left(F_c\,V_{bi}\right)^2}{4V_{bi}}\right)\right] \quad (3\text{-}32)$$

$$\tilde{C}_{gd}=\frac{\partial\tilde{Q}_{gd}}{\partial V_{gd}}=\frac{C_{gdo}}{\sqrt[3]{1-F_c}}\left[1-\frac{3F_c}{2}+\frac{V_{gk}^{n}+V_{gk}^{n+1}-V_{dk}^{n}-V_{dk}^{n+!}}{4V_{bi}}\right] \quad (3\text{-}33)$$

Simplifying (3-21) and (3-22) leads to

$$\mathrm{F}_{\mathrm{NL}}\,(V_{mk}^{n},V_{mk}^{n+1},V'^{n}_{gsk},V'^{n+1}_{gsk},I_{mk}^{n+1/2})=0 \qquad m=d,g,s \quad (3\text{-}34)$$

$$[\mathrm{I}_k^{n+3/2}]=\left(\frac{1}{\Delta t}[L]+\frac{1}{2}[R]\right)^{-1}\left\{\left(\frac{1}{\Delta t}[L]-\frac{1}{2}[R]\right)[\mathrm{I}_k^{n+1/2}]-\frac{1}{\Delta x}([V_{k+1}^{n+1}]-[V_k^{n+1}]\right\} \quad (3\text{-}35)$$

Because of its simplicity and efficiency, the leap-frog algorithm was used to solve these equations. In this algorithm, the solutions started first with an initially relaxed line having zero voltage and current values. Then, voltages along the electrode of the transistor were solved for a fixed time from (3-34), and then currents were solved using (3-35). [11]-[15].

3.3.1 Solution of the Nonlinear Equation $F_{NL} = 0$

Equation (3-34) should be solved to calculate the voltage along the electrodes of the transistor. One of the most useful and best-known algorithms to solve nonlinear systems of equations is the Newton–Raphson method that converges faster than the bisection and false position methods [19]. More specifically, (3-34) is a set of four algebraic nonlinear equations with four unknown parameters

$$\mathrm{F}_{NL} = \begin{pmatrix} F_{1NL} \\ F_{2NL} \\ F_{3NL} \\ F_{4NL} \end{pmatrix} \tag{3-36}$$

Our purpose was to obtain the four unknown parameters $V_{sk}^{n+1}, V_{gk}^{n+1}, V'^{n+1}_{gsk}, V_{dk}^{n+1}$. In this technique, we started first with initial values and then the Jacobian matrix was calculated upshot. The value of the unknown parameters were calculated in the next stage as follows

$$\left[\mathrm{V}_k'^{n+1}\right]^{m+1} = \left[\mathrm{V}_k'^{n+1}\right]^{m} - \mathrm{JAC}\left[\left[\mathrm{V}_k'^{n+1}\right]^{m}\right]^{-1} \mathrm{F_{NL}}\left[\left[\mathrm{V}_k'^{n+1}\right]^{m}\right] \tag{3-37}$$

This iterative algorithm was run until $\left|F_{NL}((V_k^{n+1})^m) \le \varepsilon\right|$. The Jacobian matrix is given as

$$\mathrm{JAC} = \frac{\partial \mathrm{F_{NL}}}{\partial \mathrm{V}'} = \begin{pmatrix} \frac{\partial F_{1NL}}{\partial V_{dk}^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{gk}^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{sk}^{n+1}} & \frac{\partial F_{1NL}}{\partial V'^{n+1}_{gsk}} \\ \frac{\partial F_{2NL}}{\partial V_{dk}^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{gk}^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{sk}^{n+1}} & \frac{\partial F_{2NL}}{\partial V'^{n+1}_{gsk}} \\ \frac{\partial F_{3NL}}{\partial V_{dk}^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{gk}^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{sk}^{n+1}} & \frac{\partial F_{3NL}}{\partial V'^{n+1}_{gsk}} \\ \frac{\partial F_{4NL}}{\partial V_{dk}^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{gk}^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{sk}^{n+1}} & \frac{\partial F_{4NL}}{\partial V'^{n+1}_{gsk}} \end{pmatrix} \tag{3-38}$$

This procedure gave us the voltages along the electrodes of the transistor. Also, the voltage of the gate–source capacitance was obtained. Then, using the voltage at the new time step, we obtained the current at the new step using (3-35).

3.3.2 Boundary Conditions

In many microwave applications, transistors are used in the common source configuration because of its high stability and high gain. In this configuration, the source electrode is grounded at the beginning and at the end of the electrode. Also, the transistor is usually excited at the beginning of the gate electrode and loaded at the end of drain electrode [16]-[18]. Thus, we need to investigate in details this case of loading and exciting configuration, whereas the other configurations can be simply investigated using the nonlinear equations. Fig. 3.2 shows the assumed structure of the transistor with the biasing and loading circuits.

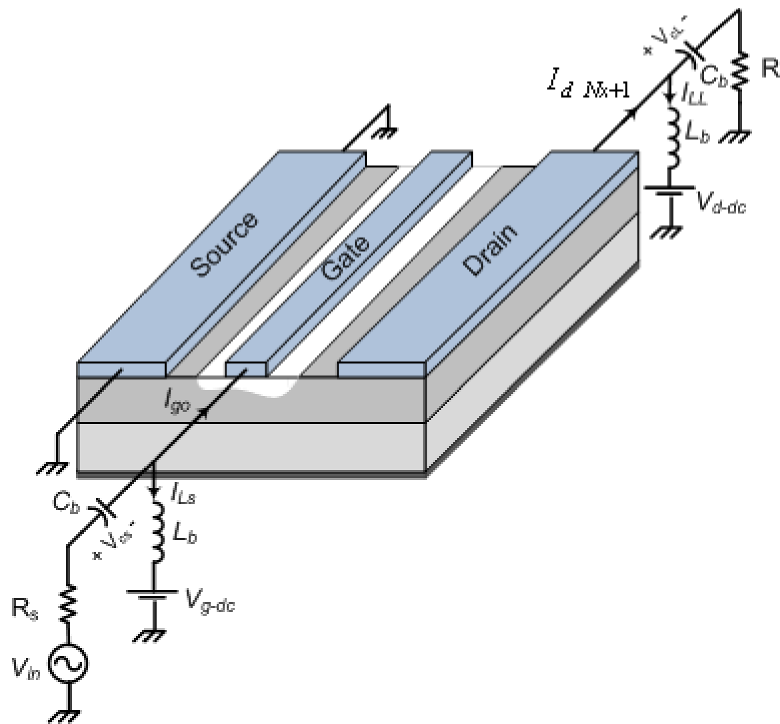

Fig.3.2 Biasing and loading circuits considered for the transistor

Equation (3-21) for $k = 1$ and $k = N_x + 1$ becomes

$$[F_{NL}|_{k=1}] = \frac{2}{\Delta x}\Big([I'^{n+1/2}_{1}] - [I'^{n+1/2}_{0}]\Big) + \frac{1}{\Delta t}[\hat{C}]\Big([V'^{n+1}_{1}] - [V'^{n}_{1}]\Big) + \frac{1}{2}[\mathrm{G}]\Big([\mathrm{V}'^{\mathrm{n+1}}_{1}] + [\mathrm{V}'^{\mathrm{n}}_{1}]\Big) + [\hat{I}'_{NL}|_{k=1}] = 0 \tag{3-39}$$

$$[F_{NL}|_{Nx+1}] = \frac{2}{\Delta x}\Big([I'^{n+1/2}_{Nx+1}] - [I'^{n+1/2}_{Nx}]\Big) + \frac{1}{\Delta t}[\hat{C}]\Big([V'^{n+1}_{Nx+1}] - [V'^{n}_{Nx+1}]\Big) + \frac{1}{2}[\mathrm{G}]\Big([\mathrm{V}'^{\mathrm{n+1}}_{\mathrm{Nx+1}}] + [\mathrm{V}'^{\mathrm{n}}_{\mathrm{Nx+1}}]\Big) + [\hat{I}'_{NL}|_{k=Nx+1}] = 0 \tag{3-40}$$

Since the transistor is excited at the beginning of the gate electrode and loaded at the end of the drain electrode, two more unknown parameters are introduced; thus, two more equations should be added to the previous set of equations. The biasing circuit at the end of the drain electrode gives

$$[F_{5NL}\Big|_{k=1}] = -\frac{1}{2}([V^{n}_{in}] + [V^{n+1}_{in}] + R_s\, C_b\, \frac{1}{\Delta t}([V^{n+1}_{cs}] - [V^{n}_{cs}]) + \frac{1}{2}([V^{n+1}_{cs}] + [V^{n}_{cs}]) + \frac{1}{2}([V^{n+1}_{g1}] + [V^{n}_{g1}]) \tag{3-41}$$

$$[F_{5NL}\Big|_{k=Nx+1}] = R_L\, C_b\, \frac{1}{\Delta t}([V^{n+1}_{cL}] - [V^{n}_{cL}]) + \frac{1}{2}([V^{n+1}_{cL}] + [V^{n}_{cL}]) - \frac{1}{2}([V^{n+1}_{d\,Nx+1}] + [V^{n}_{d\,Nx+1}]) \tag{3-42}$$

$$[F_{6NL}\Big|_{k=1}] = -V_{g\,dc} - L_b\, \frac{1}{\Delta t}([I^{n+1}_{Ls}] - [I^{n}_{Ls}]) + \frac{1}{2}([V^{n+1}_{g1}] + [V^{n}_{g1}]) \tag{3-43}$$

$$[F_{6NL}\Big|_{k=Nx+1}] = -V_{d\,dc} - L_b\, \frac{1}{\Delta t}([I^{n+1}_{LL}] - [I^{n}_{LL}]) + \frac{1}{2}([V^{n+1}_{d\,Nx+1}] + [V^{n}_{d\,Nx+1}]) \tag{3-44}$$

So F_{NL} for $k = 1$ and $k = N_x + 1$ becomes $F1_{NL}$ and FL_{NL}, respectively

$$F1_{NL} = F_{NL}\Big|_{k=1} = \left(F_{1NL}, F_{2NL}, F_{3NL}, F_{4NL}, F_{5NL}, F_{6NL}\right)^T\Big|_{k=1} \tag{3-45}$$

$$FL_{NL} = F_{NL}\Big|_{k=Nx+1} = \left(F_{1NL}, F_{2NL}, F_{3NL}, F_{4NL}, F_{5NL}, F_{6NL}\right)^T\Big|_{k=Nx+1} \tag{3-46}$$

Considering Fig.3.3 and applying KCL at input node, we can rewrite $[I_{d0}^{n+1/2}],[I_{g0}^{n+1/2}]$

$$\begin{aligned} &[I_{g0}^{n+1/2}] = \frac{1}{2}\left([I_{LL}^{n}] + [I_{LL}^{n+1}]\right) + \frac{C_b}{\Delta t}\left([V_{cL}^{n+1}] - [V_{cL}^{n}]\right) \\ &[I_{d0}^{n+1/2}] = 0 \end{aligned} \tag{3-47}$$

Also, applying KVL at output loop, we can rewrite $[I_{gNx+1}^{n+1/2}],[I_{dNx+1}^{n+1/2}]$ as

$$\begin{aligned} &[I_{d\,Nx+1}^{n+1/2}] = -\frac{1}{2}\left([I_{Ls}^{n}] + [I_{Ls}^{n+1}]\right) + \frac{C_b}{\Delta t}\left([V_{cs}^{n+1}] - [V_{cs}^{n}]\right) \\ &[I_{g\,Nx+1}^{n+1/2}] = 0 \end{aligned} \tag{3-48}$$

One of the advantages of these nonlinear equations is that we can simply update them with any load connected to the source, gate and drain electrodes.

For example if we consider the transistor shown in Fig.3.3, the amount of currents at the beginning and at the end of the electrodes will be

$$\begin{aligned} &[I_{g0}^{n+1/2}] = \frac{1}{2}\left([I_{LL}^{n}] + [I_{LL}^{n+1}]\right) + \frac{C_b}{\Delta t}\left([V_{cL}^{n+1}] - [V_{cL}^{n}]\right) \\ &[I_{d0}^{n+1/2}] = -\frac{1}{2R_{sd}}\left([V_{d1}^{n}] + [V_{d1}^{n+1}]\right) \\ &[I_{s0}^{n+1/2}] = -\frac{1}{2R_{ss}}\left([V_{s1}^{n}] + [V_{s1}^{n+1}]\right) \\ &[I_{d\,Nx+1}^{n+1/2}] = -\frac{1}{2}\left([I_{Ls}^{n}] + [I_{Ls}^{n+1}]\right) + \frac{C_b}{\Delta t}\left([V_{cs}^{n+1}] - [V_{cs}^{n}]\right) \\ &[I_{g\,Nx+1}^{n+1/2}] = \frac{1}{2R_{Lg}}\left([V_{g\,Nx+1}^{n+1}] + [V_{gNx+1}^{n}]\right) \\ &[I_{s\,Nx+1}^{n+1/2}] = \frac{1}{2R_{Ls}}\left([V_{s\,Nx+1}^{n+1}] + [V_{s\,Nx+1}^{n}]\right) \end{aligned} \tag{3-51}$$

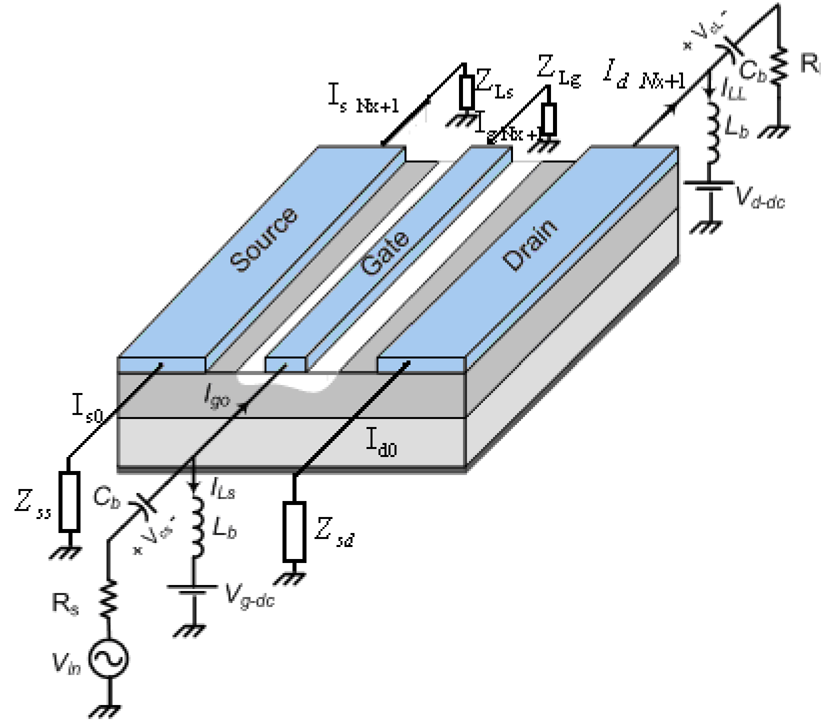

Fig.3.3. FET biasing while considering terminated loads at the beginning and end of each electrode

By substituting (3-51) into (3-39) and (3-40), $I_0^{n+1/2}, I_{Nx+1}^{n+1/2}$ will be eliminated. So F_{NL}, turn into six nonlinear equations with six unknown parameters $V_{s\,Nx+1}^{n+1}, V_{g\,Nx+1}^{n+1}, V_{gs\,Nx+1}^{n+1}, V_{d\,Nx+1}^{n+1}, V_{cL}^{n+1}, V_{LL}^{n+1}$. These equations at input point will turn into six nonlinear equations with six unknown variables $V_{s1}^{n+1}, V_{g1}^{n+1}, V_{gs1}^{n+1}, V_{d1}^{n+1}, V_{cs}^{n+1}, V_{Ls}^{n+1}$. For the other points, on the other hand, we will have four nonlinear equations with four unknown parameters $V_{sk}^{n+1}, V_{gk}^{n+1}, V_{gsk}^{n+1}, V_{dk}^{n+1}$. Thus, the finite difference approximation of the nonlinear equations can be written as follows

$$\left[V_1'^{n+1}\right]^{m+1} = \left[V_1'^{n+1}\right]^m - \mathrm{JAC}_1\left[\left[V_1'^{n+1}\right]^m\right]^{-1} \mathrm{F1}_{\mathrm{NL}}\left[\left[V_1'^{n+1}\right]^m\right] \qquad k = 1 \qquad (3\text{-}52)$$

$$[V_1''^{n+1}] = \left[V_{d1}^{n+1}, V_{g1}^{n+1}, V_{s1}^{n+1}, V_{gs1}^{n+1}, V_{cs}^{n+1}, I_{Ls}^{n+1}\right]^t \qquad (3\text{-}53)$$

and

$$\mathrm{JAC}_1 = \frac{\partial \mathrm{F1}_{\mathrm{NL}}}{\partial \mathrm{V}_1''^{n+1}}\bigg|_{\mathrm{V}_1''^{n+1}} = \begin{pmatrix} \frac{\partial F_{1NL}}{\partial V_{d1}^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{g1}^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{s1}^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{gs1}'^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{cs}^{n+1}} & \frac{\partial F_{1NL}}{\partial I_{Ls}^{n+1}} \\ \frac{\partial F_{2NL}}{\partial V_{d1}^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{g1}^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{s1}^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{gs1}'^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{cs}^{n+1}} & \frac{\partial F_{2NL}}{\partial I_{Ls}^{n+1}} \\ \frac{\partial F_{3NL}}{\partial V_{d1}^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{g1}^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{s1}^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{gs1}'^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{cs}^{n+1}} & \frac{\partial F_{3NL}}{\partial I_{Ls}^{n+1}} \\ \frac{\partial F_{4NL}}{\partial V_{d1}^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{g1}^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{s1}^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{gs1}'^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{cs}^{n+1}} & \frac{\partial F_{4NL}}{\partial I_{Ls}^{n+1}} \\ \frac{\partial F_{5NL}}{\partial V_{d1}^{n+1}} & \frac{\partial F_{5NL}}{\partial V_{g1}^{n+1}} & \frac{\partial F_{5NL}}{\partial V_{s1}^{n+1}} & \frac{\partial F_{5NL}}{\partial V_{gs1}'^{n+1}} & \frac{\partial F_{5NL}}{\partial V_{cs}^{n+1}} & \frac{\partial F_{5NL}}{\partial I_{Ls}^{n+1}} \\ \frac{\partial F_{6NL}}{\partial V_{d1}^{n+1}} & \frac{\partial F_{6NL}}{\partial V_{g1}^{n+1}} & \frac{\partial F_{6NL}}{\partial V_{s1}^{n+1}} & \frac{\partial F_{6NL}}{\partial V_{gs1}'^{n+1}} & \frac{\partial F_{6NL}}{\partial V_{cs}^{n+1}} & \frac{\partial F_{6NL}}{\partial I_{Ls}^{n+1}} \end{pmatrix} \quad (3\text{-}54)$$

$$\left[\mathrm{V}_k'^{n+1}\right]^{m+1} = \left[\mathrm{V}_k'^{n+1}\right]^{m} - \mathrm{JAC}\left[\left[\mathrm{V}_k'^{n+1}\right]^{m}\right]^{-1} \mathrm{F}_{\mathrm{NL}}\left[\left[\mathrm{V}_k'^{n+1}\right]^{m}\right] \quad k = 2, 3 \ldots Nx \quad (3\text{-}55)$$

with

$$\mathrm{JAC} = \frac{\partial \mathrm{F}_{\mathrm{NL}}}{\partial \mathrm{V}'} = \begin{pmatrix} \frac{\partial F_{1NL}}{\partial V_{dk}^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{gk}^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{sk}^{n+1}} & \frac{\partial F_{1NL}}{\partial V_{gsk}'^{n+1}} \\ \frac{\partial F_{2NL}}{\partial V_{dk}^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{gk}^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{sk}^{n+1}} & \frac{\partial F_{2NL}}{\partial V_{gsk}'^{n+1}} \\ \frac{\partial F_{3NL}}{\partial V_{dk}^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{gk}^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{sk}^{n+1}} & \frac{\partial F_{3NL}}{\partial V_{gsk}'^{n+1}} \\ \frac{\partial F_{4NL}}{\partial V_{dk}^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{gk}^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{sk}^{n+1}} & \frac{\partial F_{4NL}}{\partial V_{gsk}'^{n+1}} \end{pmatrix} \quad (3\text{-}56)$$

$$\left[\mathrm{V}''^{n+1}_{Nx+1}\right]^{m+1} = \left[\mathrm{V}''^{n+1}_{Nx+1}\right]^{m} - \mathrm{JAC_L}\left[\left[\mathrm{V}''^{n+1}_{Nx+1}\right]^{m}\right]^{-1} \mathrm{FL}_{\mathrm{NL}}\left[\left[\mathrm{V}''^{n+1}_{Nx+1}\right]^{m}\right] \quad (3\text{-}57)$$

Also

$$
\mathrm{JAC_L} = \frac{\partial \mathrm{FL_{NL}}}{\partial \mathrm{V}''^{n+1}_{Nx+1}}\Bigg|_{\mathrm{V}''^{n+1}_{\mathrm{Nx+1}}} = \begin{pmatrix}
\frac{\partial F_{1NL}}{\partial V^{n+1}_{d\,Nx+1}} & \frac{\partial F_{1NL}}{\partial V^{n+1}_{g\,Nx+1}} & \frac{\partial F_{1NL}}{\partial V^{n+1}_{s\,Nx+1}} & \frac{\partial F_{1NL}}{\partial V'^{n+1}_{gs\,Nx+1}} & \frac{\partial F_{1NL}}{\partial V^{n+1}_{cL}} & \frac{\partial F_{1NL}}{\partial I^{n+1}_{LL}} \\
\frac{\partial F_{2NL}}{\partial V^{n+1}_{d_{Nx+1}}} & \frac{\partial F_{2NL}}{\partial V^{n+1}_{g\,Nx+1}} & \frac{\partial F_{2NL}}{\partial V^{n+1}_{s\,Nx+1}} & \frac{\partial F_{2NL}}{\partial V'^{n+1}_{gs\,Nx+1}} & \frac{\partial F_{2NL}}{\partial V^{n+1}_{cL}} & \frac{\partial F_{1NL}}{\partial I^{n+1}_{LL}} \\
\frac{\partial F_{3NL}}{\partial V^{n+1}_{d\,Nx+1}} & \frac{\partial F_{3NL}}{\partial V^{n+1}_{g\,Nx+1}} & \frac{\partial F_{3NL}}{\partial V^{n+1}_{s\,Nx+1}} & \frac{\partial F_{3NL}}{\partial V'^{n+1}_{gs\,Nx+1}} & \frac{\partial F_{3NL}}{\partial V^{n+1}_{cL}} & \frac{\partial F_{1NL}}{\partial I^{n+1}_{LL}} \\
\frac{\partial F_{4NL}}{\partial V^{n+1}_{d\,Nx+1}} & \frac{\partial F_{4NL}}{\partial V^{n+1}_{g\,Nx+1}} & \frac{\partial F_{4NL}}{\partial V^{n+1}_{s\,Nx+1}} & \frac{\partial F_{4NL}}{\partial V'^{n+1}_{gs\,Nx+1}} & \frac{\partial F_{4NL}}{\partial V^{n+1}_{cL}} & \frac{\partial F_{1NL}}{\partial I^{n+1}_{LL}} \\
\frac{\partial F_{5NL}}{\partial V^{n+1}_{d\,Nx+1}} & \frac{\partial F_{5NL}}{\partial V^{n+1}_{g\,Nx+1}} & \frac{\partial F_{5NL}}{\partial V^{n+1}_{s\,Nx+1}} & \frac{\partial F_{5NL}}{\partial V'^{n+1}_{gs\,Nx+1}} & \frac{\partial F_{5NL}}{\partial V^{n+1}_{cL}} & \frac{\partial F_{5NL}}{\partial I^{n+1}_{LL}} \\
\frac{\partial F_{6NL}}{\partial V^{n+1}_{d\,Nx+1}} & \frac{\partial F_{6NL}}{\partial V^{n+1}_{g\,Nx+1}} & \frac{\partial F_{6NL}}{\partial V^{n+1}_{s\,Nx+1}} & \frac{\partial F_{6NL}}{\partial V'^{n+1}_{gs\,Nx+1}} & \frac{\partial F_{6NL}}{\partial V^{n+1}_{cL}} & \frac{\partial F_{6NL}}{\partial I^{n+1}_{LL}}
\end{pmatrix} \tag{3-58}
$$

$$
[\mathrm{I}^{n+3/2}_k] = \left(\frac{1}{\Delta t}[L] + \frac{1}{2}[R]\right)^{-1} \left\{\left(\frac{1}{\Delta t}[L] - \frac{1}{2}[R]\right)[\mathrm{I}^{n+1/2}_k] - \frac{1}{\Delta x}([V^{n+1}_{k+1}] - [V^{n+1}_k]\right\} \tag{3-59}
$$

The voltages and currents are solved by iterating k for a fixed time step and then iterating the time.

3.4 Numerical Results

Since we already characterized the nonlinear behavior of the NE710, we used those experimental data to demonstrate the efficiency of our approach. The input and output nodes were connected to the beginning and at the end of the gate and drain electrodes, respectively. The source electrode was grounded at the beginning and at the end of the electrode. The structure of the considered transistor and its biasing and loading circuits are shown in Fig.3.3. The values of the elements used in the distributed model are shown in Table 3.1 and the Curtice cubic model parameters are listed in Table 3.2. This transistor was simulated at several bias points and its results compared to those obtained with the S.D. model.

Table 3.1 Numerical values of the distributed model

Distributed model elements	Numerical Values (per unit length)
L_{dd}	780 nH/m
Lss	780 nH/m
Lgg	161 nH/m
Mgd	360 nH/m
Mgs	360 nH/m
Mds	240 nH/m
Rd	900 Ω/m
Rs	900 Ω/m
Rg	34.3 kΩ/m
Cgp	0.6 pF/m
Cdp	87 pF/m
Csp	148 pF/m
Cgdp	29 pF/m
Cgsp	29 pF/m
Cdsp	61 pF/m

Table 3.2 Curtice cubic parameter values

$A_0 = .058$	$C_{gd0} = .021pF$	$R_i = 0\,\Omega$
$A_1 = .1034$	$V_{bi} = .76V$	$R_{ds0} = 273.8\,\Omega$
$A_2 = -.00924$	$V_{ds0} = 5V$	$V_{dsc} = 5V$
$A_3 = -.048$	$V_{T0} = -1.2\,V$	$F_c = .5$
$C_{gs0} = .04821pF$	$\gamma = 2.345$	$\beta = .0212$

The transistor was biased at $V_{gs} = 0$ V, $V_{ds} = 3$ V and excited by a 20 GHz sinusoidal excitation source with a 1 V amplitude. Figs.3.4 shows the voltage at the end of the drain electrode exhibiting a good agreement between the proposed and S.D. models.

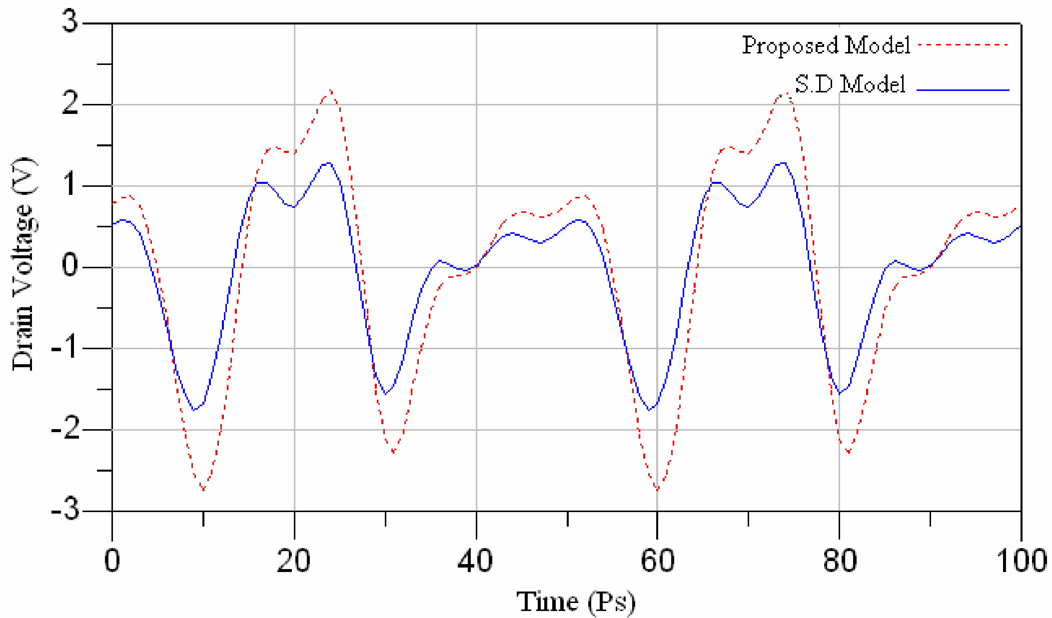

Fig.3.4 Voltage at the end of drain electrode when the device is biased at V_{ds} =3 V, V_{gs} =0 V and excited by a 20 GHz sinusoidal excitation source with 1 V amplitude

The drain voltage spectrum at the end of the drain electrode is presented in Fig.3.5, which describes the nonlinear characteristic of the transistor under this condition very well. The load cycle for this transistor, at V_{gs} = -0.5 V, V_{ds} = 5 V, excited by a source with a 2 V amplitude and 30 GHz when the load is a 50 Ω resistance is shown in Fig.3.6.

The results of the proposed model are compared with that of the circuit-based model. Fig.3.7 depicts the results of the proposed and S.D. models at V_{gs} = -0.5 V, V_{ds} = 2 V and with an excitation source with a 1 V amplitude but at a frequency of 60 GHz. In this figure, wave propagation behavior on drain electrode is depicted. The waveform at three different points of gate width (w) is obtained.

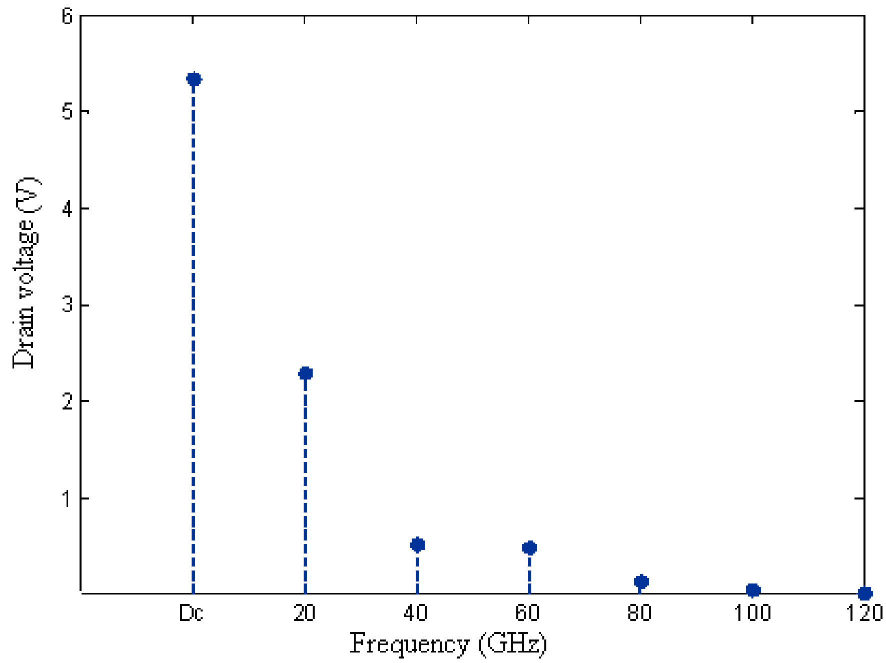

Fig.3.5 Drain voltage spectrum at the end of drain electrode when the device is biased at V_{ds} = 5 V, V_{gs} = 0 V and excited by a 20 GHz sinusoidal excitation source with 1.5 V amplitude

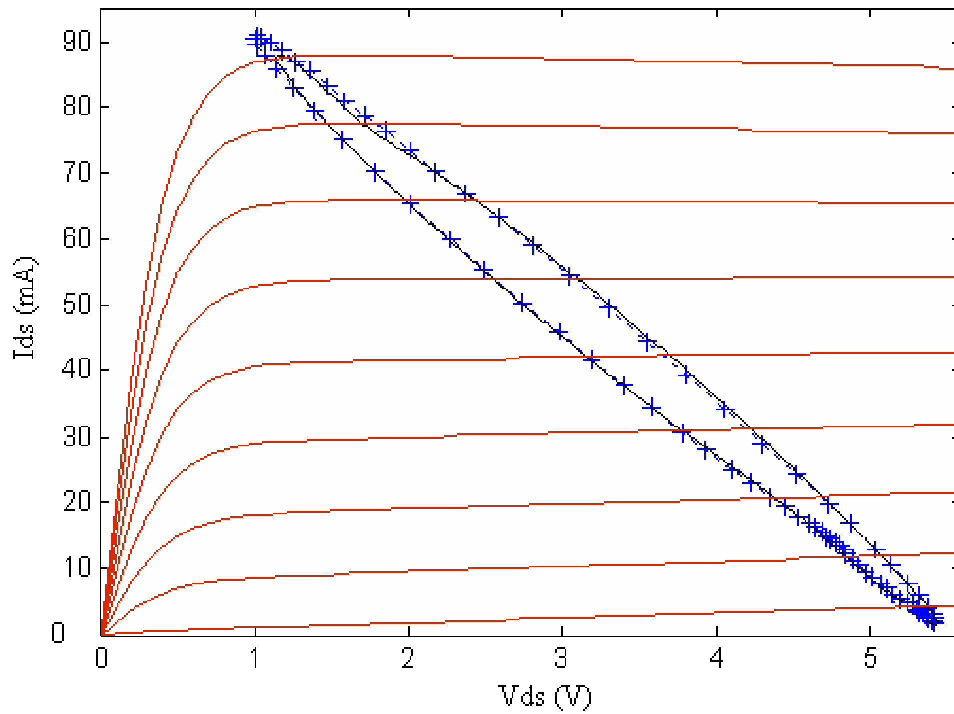

Fig.3.6 Load cycle at V_{ds} = 5 V and V_{gs} = -0.5 V and a source with 2 V amplitude and f = 30 GHz when load is a 50 Ω proposed model (+++) and S.D. model (----)

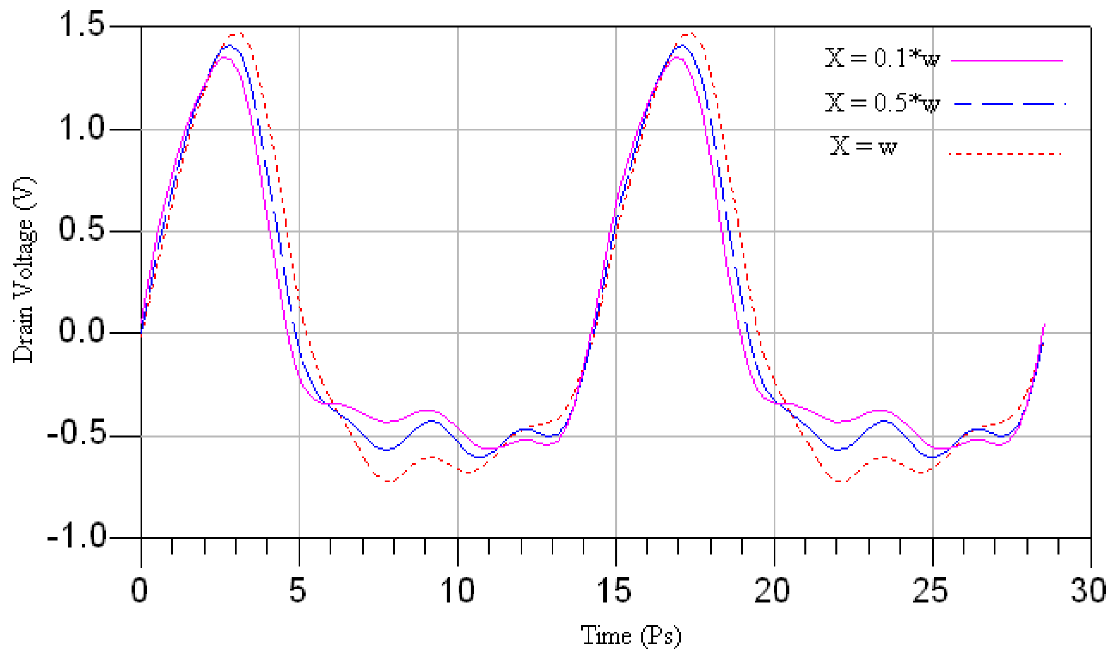

Fig.3.7. Voltage at the end of drain electrode when the device is biased at V_{ds} = 2 V, V_{gs} = -.5 V having a source with 1 V amplitude and f = 60 GHz

In a nonlinear circuit, these effects are more present than in linear circuits. In most cases, the source electrode is assumed grounded all along the electrode whereas here the source electrode is grounded at the beginning and at the end. In this work, the distributed effect of the source electrode is considered to obtain accurate results. The voltage at the middle of the source electrode at a bias of V_{gs} = -0.5V, V_{ds} = 4V with a 20 GHz sinusoidal excitation source and a 1.5 V amplitude is shown in Fig.3.8. This figure shows that the distributed effect of the source electrode must be accounted for the analysis of high-frequency devices and circuits.

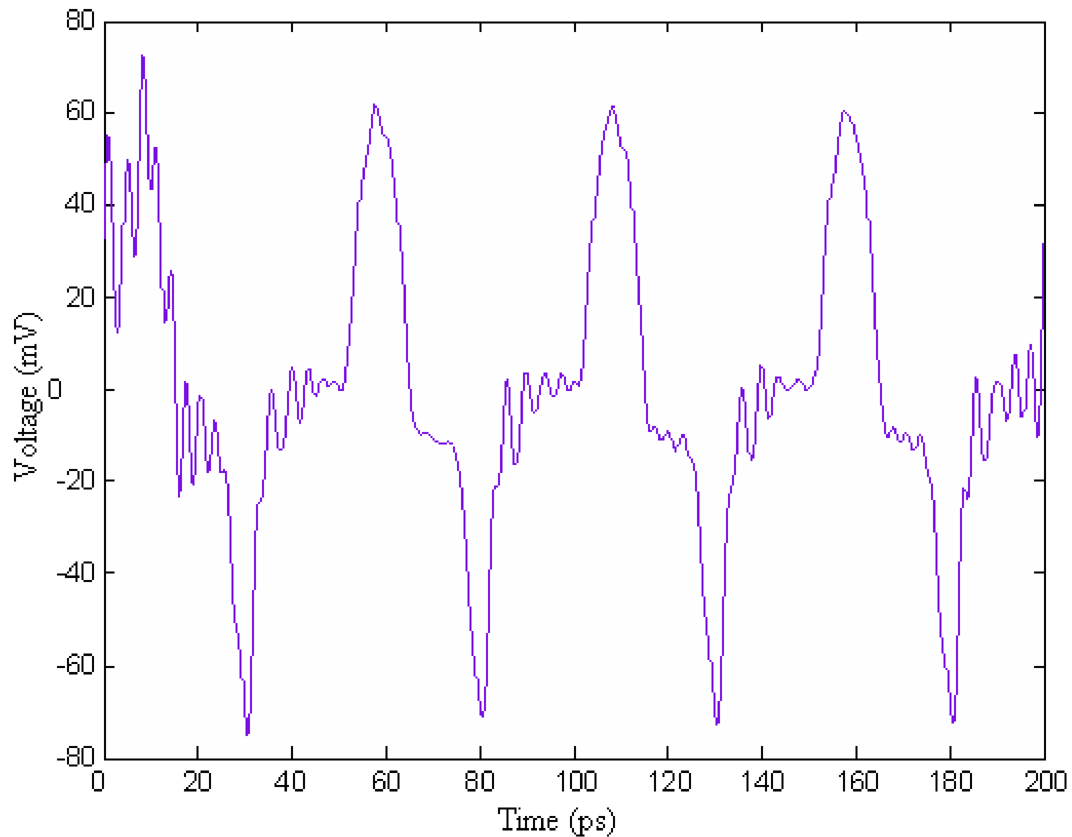

Fig.3.8. Voltage at the middle of source electrode at V_{ds} = 4 V, V_{gs} = -0.5 V and excited by a 20 GHz sinusoidal excitation source with 1.5 V amplitude

3.5. The Effect of the Location of Excitation/Extraction Points

To further investigate this effect, we analyzed some configurations with different excitation/extraction points as shown in Fig.3.9. In all cases, the transistor is biased at V_{gs} = -1V, V_{ds} = 4V with a 30 GHz or 70GHz sinusoidal excitation source and a 1 V amplitude. Tables 3.3 and 3.4 report the amplitude of the output voltage up to the fifth harmonic for 30GHz and 70GHz, respectively.

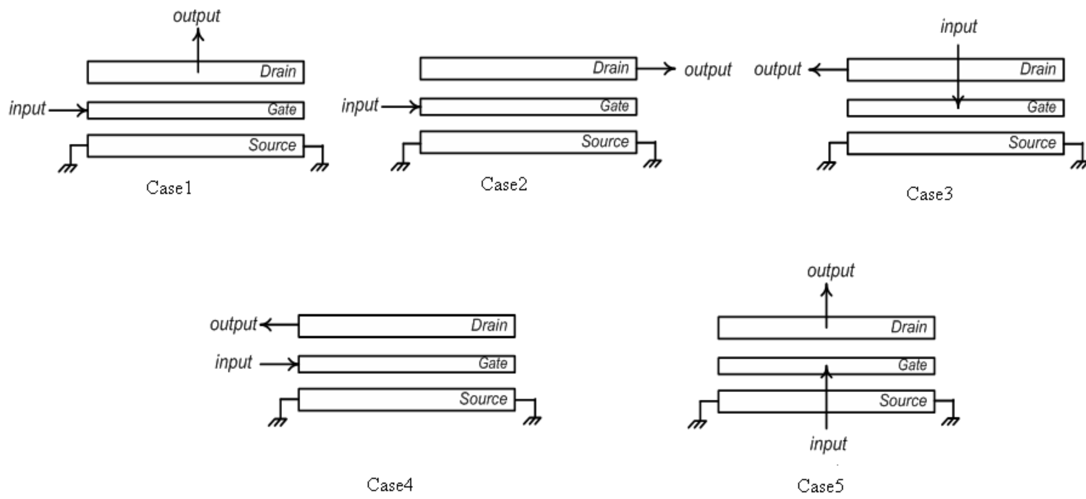

Fig.3.9. Different combination for excitation/extraction for FET transistor

Table 3.3. Output voltage harmonics for different combinations of Fig.3.10 at 30GHz (Values are in Volt)

	DC	**First Harmonic**	**Second Harmonic**	**Third Harmonic**	**Forth Harmonic**	**Fifth Harmonic**
Case1	5.37	1.90	0.37	0.30	0.14	0.06
Case2	5.40	1.90	0.41	0.29	0.09	0.01
Case3	5.25	2.10	0.27	0.24	0.08	0.04
Case4	5.29	2.07	0.28	0.26	0.14	0.08
Case5	5.24	2.07	0.26	0.26	0.08	0.02

In Table 3.3, all five combinations exhibit almost the same amplitude. But technically, case 5 has the minimum DC value and second harmonic as compared to the fundamental.

However, in Table 3.4, since the frequency is higher, the distributed effects cannot be neglected and thus, the behavior of each combination differs from each other. In fact, since case 5 has the lowest high-order harmonics, it could be the best configuration to design power amplifiers. Case 2 has the minimum fundamental amplitude while it generates the highest amplitude at second and third harmonics. So it could be the best option for frequency multipliers. So using the proposed CAD algorithm we can choose the best case for optimum circuit design in regard of the application.

Table3.4. Output voltage harmonics for different combinations of Fig.3.10 at 70GHz

	DC	**First Harmonic**	**Second Harmonic**	**Third Harmonic**	**Forth Harmonic**	**Fifth Harmonic**
Case1	5.04	1.02	0.10	0.05	0.01	0.05
Case2	5.05	0.85	0.14	0.22	0.06	0.05
Case3	5.06	1.23	0.13	0.11	0.02	0.00
Case4	5.05	1.23	0.14	0.14	0.03	0.03
Case5	5.05	1.24	0.09	0.05	0.00	0.01

3.6 Conclusion

Based on the three-line structure we proposed in the previous chapter, a set of nonlinear active multi-conductor transmission line equations have been introduced. These equations can accurately predict the behavior of microwave/ millimeter wave transistors in a nonlinear regime. The FDTD technique was used to solve these nonlinear equations in the time domain and the simulated results waveforms were compared to those obtained using the existing S.D model. A systematic procedure has been given to derive an accurate non-linear proposed FET model. This model was extracted from its S.D low frequency equivalent circuit, and its geometrical configuration. The results obtained have been compared with that of the S.D equivalent circuit at millimeter waves. It must be noted that the model allows the FET-designer to optimize the place of the gate and drain access-input along the width of the corresponding electrode, following the desired application (power amplification, frequency multiplication etc.) at millimeter waves.

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Chapter 4   Noise FET Modeling

4.1 Introduction

Accurate signal and noise analysis of active components is the main step in microwave active circuit analysis. The performances of transistors like MESFETs, pseudomorphic and lattice-match HEMTs indicate the important role of such devices for further mm-wave applications such as phased-array radars, mobile communication systems, satellite communication systems, anti-collision radars and intelligent vehicle highway systems. On the other hand, to predict more accurately the system performance, device modeling, circuit design and simulation, wave propagation effects on the device and circuit structure should be accurately evaluated. To characterize, compare, and improve the noise performance of active devices, a theoretical framework is needed to identify the noise sources, how these sources contribute to the overall noise, and how the noise varies with external operating conditions, such as bias and matching. A common approach is to add discrete noise sources to a small-signal model [1]-[3]. Depending on the model, the sources may be correlated, adding complexity to the derivation and interpretation of the model behavior. This chapter reviews the noise sources in a FET noise model, defines the FET noise parameters and proposes a new noise model for FETs.

4.2 Noise Sources

The two most common types of noise are shot and thermal noise. Both are referred to as “flat” or “white,” meaning the noise power versus frequency is constant.

4.2.1 Thermal Noise

Thermal noise was first studied in detail by Johnson in 1927 [4], and explained mathematically by Nyquist [5]. Its physical origin is the agitation of electrons in a conductor. The random scattering of electrons by atoms followed by their relaxation back to a ground

state leads to fluctuations that can be measured as a voltage or current. The use of statistical analysis and thermal physics [6] leads to the following expression that represents the available noise power from a resistance into a matched load [7]

$$P_{Thermal} = \left[\frac{hf}{2} + \frac{hf}{\exp\left(\frac{hf}{kT}\right) - 1} \right] \Delta f \tag{4-1}$$

where h is the Planck's constant, k the Boltzmann's constant, T the temperature, and f the frequency. The term Δf is the bandwidth in which the noise is being calculated. When values are quoted and a bandwidth is not specified, it is assumed to be a 1 Hz bandwidth.

This equation can be usually simplified at high frequencies as

$$P_{Thermal} \cong kT\Delta f \tag{4-2}$$

A handy value from this expression is that the available noise at room temperature in a 1 Hz bandwidth is -174 dBm (4×10^{-21} W).

When the resistive part of load is not matched, or the noise needs to be expressed as a voltage or current (described by a variance), the following forms are useful:

$$\begin{aligned} \langle v_n^2 \rangle &= 4kTR\Delta f \\ \langle i_n^2 \rangle &= \frac{4kT}{R} \Delta f \end{aligned} \tag{4-3}$$

R is the noise resistance. A 1kΩ resistor generates $4nV/\sqrt{Hz}$ of noise.

Ideal reactive components do not generate noise. However, because real inductors and capacitors are lossy, the equivalent circuit of these components will generate thermal noise. Also, these components shape the bandwidth of the noise in ways similar to shaping a signal.

4.2.2 Shot Noise

Shot noise was reported and explained by W. Schottky in 1918. The analogy of this noise to buck shot being dropped into a bucket is the basis for its name [14]. Shot noise exists when two conditions are met: (1) a dc current is flowing and (2) the charge carriers composing the dc current cross a potential barrier. This second condition is why resistors and the channel of a HEMT do not generate shot noise. The noise exists because a charge is discrete and cross the potential barrier at *random* times. Using random mathematics [9], shot noise is described by the following equation for current fluctuations:

$$\left\langle i_n^2 \right\rangle = 2qI_{dc}\Delta f \qquad (4\text{-}4)$$

with q the electronic charge I_{dc} the dc current, and Δf the bandwidth of interest.

4.2.3 Other Sources of Noise

Shot and thermal are the most important noise sources for NF modeling. Others exist, and at frequencies lower than RF should be considered. Flicker and generation-recombination noise are important for oscillator phase noise, but are not of concern for NF measurements in the RF frequency range. Burst noise is interpreted as a type of low-frequency noise with a $1/f^2$ spectrum. Avalanche noise is a form of shot noise, and usually applies to a semiconductor junction. With a high enough field across a junction, avalanche multiplication can occur [10].

4.3 Noise Figure and Noise Parameters

A device can add noise to the input noise source due to its intrinsic noise sources. This makes the signal-to-noise ratio at the output worse than at the input. Expressing a ratio of these two ratios at a reference temperature leads to the definition of the noise figure NF [3].

$$NF = \frac{(S/N)_{in}}{(S/N)_{out}}\Bigg|_{T=room\,temperature} \qquad (4\text{-}5)$$

Sometimes NF is also called noise factor, F. Traditionally, the names were interchangeable, but it is common that noise figure is the noise factor expressed in decibels ($NF = 10\log_{10}(F)$). Sometimes it can be expressed in terms of temperature

$Tnoise = (F - 1)\ Troom\ temperature$

Noise sources can be added as in Fig.4.2. I_{noise} is the equivalent short-circuited noise current source and E_{noise} the equivalent open-circuited noise voltage source. Together, they account for all noise sources in the device, which can now be modeled as a noiseless two-port network. These two sources will likely be correlated because of the various physical noise sources of the device that contribute to them [8]. Models that describe these sources of noise are discussed in the next section.

An input is connected to the device, represented as source impedance in Fig.4.1. This input will generate its own noise, represented as E_{source} .

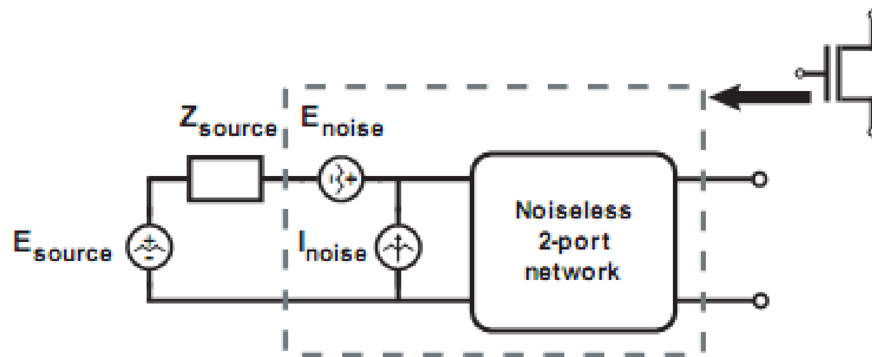


Fig.4.1. Equivalent model of a transistor driven by a noisy source of impedance Z_{source}.

This could be thermal noise from a passive network and/or active device noise. From this, F (and hence, NF) can be written as [8]

$$F = 1 + \frac{\left\langle \left| E_{noise} + I_{noise} Z_{source} \right|^2 \right\rangle}{\left\langle E_{source} \right\rangle^2} \quad (4\text{-}6)$$

As can be seen, the value of the source impedance actually affects the noise figure. Once E_{noise} and I_{noise} are determined through whichever model is applied, the noise figure can be predicted for changing source impedance. F can also be expressed as [18], [19]:

$$F = F_{\min} + \frac{4R_n}{Z_0} \frac{\left|\Gamma_{source} - \Gamma_{opt}\right|^2}{\left(1 - \left|\Gamma_{source}\right|^2\right)\left|1 + \Gamma_{opt}\right|^2} \qquad (4\text{-}7)$$

Γ_{source} is the reflection coefficient of the source impedance. Equation (4.7) contains parameters that taken together are called the **noise parameters**. They are:

F_{min} The minimum achievable noise figure. It occurs only when the source impedance is set to Z_{opt} (conversely $\Gamma_{opt} = \left|\Gamma_{opt}\right| \angle \Gamma_{opt}$).

$|\Gamma_{opt}|$ The magnitude of the source reflection coefficient that provides the minimum noise figure, F_{min}.

$\angle\Gamma_{opt}$ The angle of the source reflection coefficient that provides F_{min}

R_n An effective "slope." The larger its value, the quicker the noise figure increases as Γ_{source} is changed from its optimum value. (Conversely g_n)

4.4 FET Noise Models

Several FET noise models have been proposed in the technical literature. Those proposed by Van Der Ziel, Pucel, Fukui, and Pospieszalski can be seen as the foundations of most modern noise models [1]- [3], [11].

4.4.1 Van Der Ziel and Pucel Model

The theoretical work for noise sources in microwave FETs was introduced by Van Der Ziel in the early 1960s [3], [14]-[15]. He derived noise sources for the channel and "induced gate noise." This gate noise was explained as fluctuating noise in the channel

capacitively coupling to the gate through C_{gs} and C_{gd}, causing an effective, and correlated, noise source at the gate. The gate noise, channel (drain) noise, correlation (C), and cross-term $\langle i_g i_d^* \rangle$ can be written as [3]

$$\langle i_g^2 \rangle = 4kT_a \delta \frac{\omega^2 C_{gs}^2}{5G_{d0}} \Delta f \tag{4-8}$$

$$\langle i_d^2 \rangle = 4kT_a \Gamma_{opt} G_{d0} \Delta f \tag{4-9}$$

$$C = \frac{\langle i_g i_d^* \rangle}{\sqrt{\langle i_g^2 \rangle \langle i_d^2 \rangle}} \tag{4-10}$$

$$\langle i_g i_d^* \rangle = \frac{2}{3} j\omega C_{gs} kT_a \Delta f \tag{4-11}$$

ω is the angular frequency, T_a the ambient temperature, G_{d0} the drain-source conductance at V_{ds} = 0V, and δ an empirical parameter set equal to 4/3. Van der Ziel originally found a correlation of 0.395j for JFETs [3]. For aggressively-scaled HEMTs, the correlation was experimentally found to be ~0.7j [16]-[18].

While the above gate and drain noise expressions allow for noise prediction, for accurate results the correlation must be evaluated. This is because small changes in correlation can have a large effect in predicting noise parameters. Also, the noise sources are bias-and frequency-dependent. In 1975, Pucel *et al*. took what was learned from Van Der Ziel and extended it in a very detailed publication [2]. Their work was explicitly for a GaAs MESFET (and applicable to a HEMT), whereas Van Der Ziel's work was mainly for JFETs. The Pucel modeling takes into account velocity saturation and how the noise changes with bias, based on changes in the small-signal parameters and their noise variables. The model also uses gate and drain noise sources that are correlated, as shown in the small-signal model in Fig.4.2.

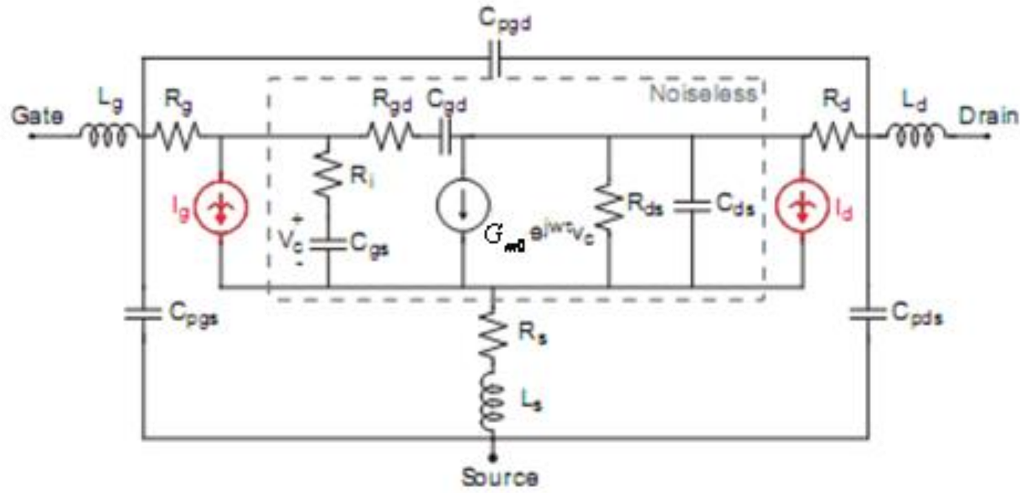


Fig.4.2.Pucel noise model in a small-signal circuit [2]

In this figure, the gate and drain noise sources account for all noise generated by the intrinsic device (inside the dashed "Noiseless" box). The parasitic resistances, R_g, R_s, and R_d, still generate thermal noise. The gate and drain noise sources are related to the noise variables by

$$P = \frac{\left\langle i_d^2 \right\rangle}{4kT_a |Y_{21}|^2 \Delta f} = \frac{\left\langle i_d^2 \right\rangle}{4kT_a G_m \Delta f} \tag{4-12}$$

$$R = \frac{|Y_{21}|^2}{4kT_a |Y_{11}|^2 \Delta f} \left\langle i_g^2 \right\rangle = \frac{G_m}{4kT_a \omega^2 C_{gs}^2 \Delta f} \left\langle i_g^2 \right\rangle \tag{4-13}$$

and the same correlation as in equation (4.10). Although Pucel determined very detailed expressions for these noise variables, the model had to be fitted to data for accurate results. Today, the parameters are determined empirically [7], fitting to noise figure measurements.

4.4.2 Fukui Model

Fukui garnered much attention in the late 1970s with the introduction of his noise empirical model [19]. Although it involved empirical parameters, his model was far simpler than the previously reported noise models. This model was directly expressed in terms of noise parameters and made clear how key small-signal parameters contributed to the noise performance. The model is also convenient because the noise at different frequencies and device scaling can be easily determined. His expressions for the noise parameters are [11]

$$F_{\min} = 1 + k_1 f\, C_{gs} \sqrt{\frac{R_g + R_s}{G_m}} \tag{4-14}$$

$$R_{opt} = k_3 \left[\frac{1}{4G_m} + R_g + R_s \right] \tag{4-15}$$

$$X_{opt} = \frac{k_4}{f\, C_{gs}} \tag{4-16}$$

$$R_n = \frac{k_2}{G_m^2} \tag{4-17}$$

The variables k_{1-4} are the fitting parameters that depend on the device technology and bias. While this model can be useful for hand calculations, the Pucel and Pospieszalski models are more complete and directly usable in a circuit simulator such as ADS.

4.4.3 Pospieszalski Model

In the late 1980's, Pospieszalski introduced a new noise figure model that took a different approach than the previous methods by removing correlation between the noise sources [1].

There are only two noise sources for the entire transistor: thermal noise of R_i and R_{ds}. Instead of these resistors being at ambient temperature, T_a, they are at higher effective temperatures T_g and T_d, shown in Fig.4.3.

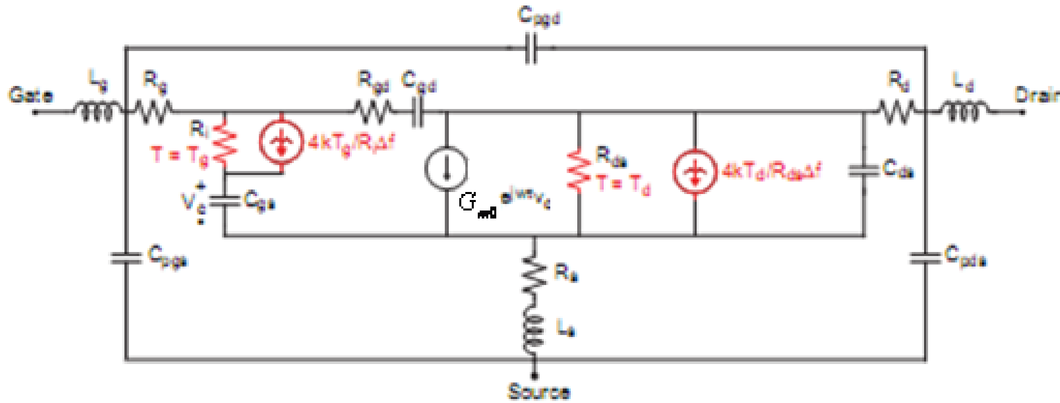


Fig.4.3.Pospieszalski noise model in a small-signal circuit [1]

T_g is usually (but not always) close to room temperature, while T_d can be of several thousand Kelvin degrees. These elevated temperatures are not linked to a physical temperature. There have been attempts to link these noise temperatures to the device physics, but none was viewed as successful. The noise can be described by the noise temperatures T_g and T_d as [1]

$$F_{\min} = 1 + 2\left(\frac{f}{f_T}\right)^2 \frac{R_i T_d}{R_{ds} T_a} + \frac{2f}{f_T T_a}\sqrt{\frac{R_i T_g T_d}{R_{ds}} + \left(\frac{f}{f_T}\right)^2 \frac{R_i^2 T_d^2}{R_{ds}^2}} \quad (4\text{-}18)$$

$$R_{opt} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{T_g R_i R_{ds}}{T_d} + R_i^2} \quad (4\text{-}19)$$

$$X_{opt} = \frac{1}{\omega C_{gs}} \quad (4\text{-}20)$$

$$R_n = \frac{T_g R_i}{T_a} + \frac{T_d}{T_a R_{ds} G_m^2}\left(1 + \omega^2 C_{gs}^2 R_i^2\right) \quad (4\text{-}21)$$

where f_T is unity-gain frequency. After measuring the scattering and noise parameters, the noise temperatures can be extracted by solving the above equations. A criteria that Pospieszalski mentions for the model to work is

$$1 \le 4\frac{R_{opt}}{R_n(F-1)} < 2 \qquad (4\text{-}22)$$

The lower limit is fundamental because the noise of a 2-port modeled by a pair of noise sources must be Hermitian and non-negative definite as shown by Pospieszalski [20]. The upper limit comes from the model itself [1]. As with the other models, it can be used to determine the match for noise and expected noise at other frequencies. The model is criticized for its dependence on R_i as a thermal noise source, which is hard to determine precisely, and for the noise temperatures not having a physical basis. As with the other models, the noise parameters must be measured prior to modeling. Thus, the model does not "predict" noise. In addition, the noise temperatures change with device bias [21].

4.5. The Proposed Model

Noise modeling of mm-wave field-effect transistors (FETs) has been studied by different research groups. In the lumped model [22]-[24], the gate-width was divided into slices in which the ratio of guided wavelength to slice width is small. Then, for each slice, a classical lumped model was defined to analyze the device noise performance.

However, these semi-distributed models have some limitations. By increasing the frequency, they cannot precisely take into account the wave propagation effect and phase cancellation phenomena in the overall device performance. Therefore, to achieve accurate results in high-frequency applications, one needs to develop a more general distributed model [32].

In this work, a new distributed noise FET model is proposed. It consists in a three-coupled excited transmission line (TL) structure in which the Laplace transformation was applied to determine the noise currents and voltages of lines. [28]. The structure was also analyzed by applying the Green's function concept as a wave approach.

4.5.1. Signal Modeling of High-Frequency FET

Fig.4.5 (a) shows a unit cell of a mm-wave FET, while Fig.4.4 (b) indicates that we can take the model as a six-port structure that consists of parallel active and series passive parts. The impedance and admittance matrices of the three coupled lines model can be written following the general form of transmission lines:

$$[Z(\omega)] = [R(\omega)] + j\omega[L(\omega)]$$
$$[Y(\omega)] = [G(\omega)] + j\omega[C(\omega)] \qquad (4\text{-}23)$$

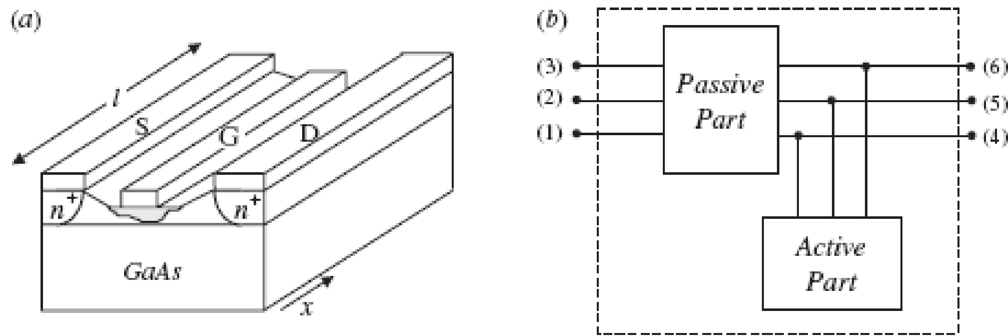


Fig.4.4 (a) Unit cell of mm-wave FET (b) The six-port active TL model of the FET

The FET impedance [Z] and admittance [Y] matrices can be determined by using the electrical and physical characteristics of the transistor [25]-[26]. By solving the second-order differential equations of the model, its voltage and current vectors can be written as

$$[V(x)] = [S_v]\exp(-[\Gamma x])[V^+] + [S_v]\exp(+[\Gamma x])[V^-] \qquad (4\text{-}24)$$

$$[I(x)] = [S_i]\exp(-[\Gamma x])[I^+] - [S_i]\exp(+[\Gamma x])[I^-] \qquad (4\text{-}25)$$

where $[V(x)] = [V^d(x) \quad V^g(x) \quad V^s(x)]$ and $[I(x)] = [I^d(x) \quad I^g(x) \quad I^s(x)]$ represent the voltage and current vectors of drain, gate and source conductors, respectively. [Γ] is the matrix of [Z].[Y] (or [Y].[Z]) eigenvalues (the three mode propagation constants) and [S_v] and [S_i] are matrices that include eigenvectors of [Z].[Y] and [Y].[Z], respectively [26]. Considering the boundary conditions of the model (as a six-port structure), the undetermined matrices V^+ and V^- can be determined.

By applying equations (4-24) and (4-25) for $x = 0$ and $x = l$, the voltages and currents of each port can be deduced, leading to the impedance ($[Z_l]_{6*6}$) or admittance ($[Y_l]_{6*6}$) matrix of the distributed FET model.

4.5.2 Three Coupled Excited Transmission Lines (Distributed Noise Model)

Let us consider the three coupled excited transmission lines shown in Fig.4.5.as the distributed noise model of a microwave FET. If we assume that distributed noise sources are independent of x and by choosing the well-known lumped model for the differential subsection, we will get partial equation for three coupled transmission lines in matrix form as

$$\begin{cases} \dfrac{d^2[V(x)]}{dx^2} - [Z(\omega)][Y(\omega)][V(x)] = [Z(\omega)][j] - \dfrac{d[v]}{dx} \\ \dfrac{d^2[I(x)]}{dx^2} - [Y(\omega)][Z(\omega)][I(x)] = [Y(\omega)][v] - \dfrac{d[j]}{dx} \end{cases} \tag{4-26}$$

where vectors $[v]$ and $[j]$ are the linear density of exciting voltage and current noise sources, respectively.

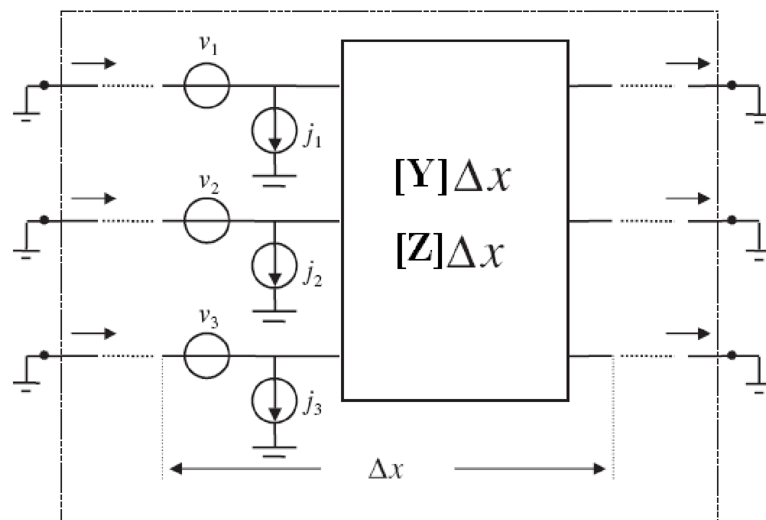


Fig.4.5. Differential subsection of excited transmission line

As already mentioned, the homogenous response of (4-26) is the same as for a single line. So we just need to determine the particular response for these sets of equations.

$$s^2[V(s)]-[Z][Y][V(s)]=\mathscr{L}\left\{[Z]\,[j]-\frac{d[v]}{dx}\right\} \tag{4-27}$$

As in the single line, the particular response is due to three modes of propagation coefficients $[\gamma_1 \quad \gamma_2 \quad \gamma_3]$ and constant coefficients $[V_0^i]$, where $[\gamma_1^2 \quad \gamma_2^2 \quad \gamma_3^2]$ are the eigenvalues and $[V_0^i]$ the eigenvectors of the [Z][Y] matrix. Therefore,

$$\begin{aligned}&\gamma_i^2[V_o^i]=[Z][Y][V_o^i]\\&\sum_{i=1}^{3}\gamma_i^2[V_o^i]=[Z][Y]\sum_{i=1}^{3}[V_o^i]\end{aligned} \tag{4-28}$$

Equation (4-28) can be written in a matrix form as

$$\left[[V_o^1] \quad [V_o^2] \quad [V_o^3]\right]\begin{bmatrix}\gamma_1^2 & 0 & 0\\ 0 & \gamma_2^2 & 0\\ 0 & 0 & \gamma_3^2\end{bmatrix}\begin{bmatrix}1\\1\\1\end{bmatrix}=([Z][Y])\left[[V_o^1] \quad [V_o^2] \quad [V_o^3]\right]\begin{bmatrix}1\\1\\1\end{bmatrix} \tag{4-29}$$

By introducing the $[S_v]$ matrix, (4-29) can be written as

$$[S_v][\Gamma^2]=([Z][Y])[S_v] \tag{4-30}$$

Reaching the following diagonal matrix

$$[\Gamma^2]=\begin{bmatrix}\gamma_1^2 & 0 & 0\\ 0 & \gamma_2^2 & 0\\ 0 & 0 & \gamma_3^2\end{bmatrix} \tag{4-31}$$

with $[\Gamma^2]=([Z][Y])$. A similar relation can be obtained using the $[S_i]$ matrix. By utilizing (4-30) and (4-31), we can simplify (4-27) as

$$[V(s)]=\left(s^2[U_{3\times3}]-[\Gamma^2]\right)^{-1}\mathscr{L}\left\{[Z]\,[j]-\frac{d[v]}{dx}\right\} \tag{4-32}$$

where [U] is the identity matrix and $(s^2[U_{3\times3}]-[\Gamma^2])$ a diagonal matrix whose inverse is

$$\left[s^2[U_{3\times3}]-[\Gamma^2]\right]^{-1}=\begin{bmatrix}\frac{1}{s^2-\gamma_1^2} & 0 & 0\\ 0 & \frac{1}{s^2-\gamma_2^2} & 0\\ 0 & 0 & \frac{1}{s^2-\gamma_3^2}\end{bmatrix} \tag{4-33}$$

So according to what we discussed for a single transmission line, a particular response for a set of three coupled transmission lines will be

$$[V_p(x)]=-[\Gamma]^{-1}\sinh([\Gamma x])*\left([Z][j]\right)+[\Gamma]^{-1}\sinh([\Gamma x])*\frac{d[v]}{dx} \tag{4-34}$$

with

$$\sinh([\Gamma x])=\begin{bmatrix}\sinh(\gamma_1 x) & 0 & 0\\ 0 & \sinh(\gamma_2 x) & 0\\ 0 & 0 & \sinh(\gamma_3 x)\end{bmatrix} \tag{4-35}$$

The total responses are then

$$\begin{aligned}[V(x)]&=[S_v]\exp(-[\Gamma x])[V^+]+[S_v]\exp(+[\Gamma x])[V^-]-[\Gamma]^{-1}\sinh([\Gamma x])*\left([Z][j]\right)+\\ &\qquad [\Gamma]^{-1}\sinh([\Gamma x])*\frac{d[v]}{dx}\\ [I(x)]&=[S_i]\exp(-[\Gamma x])[I^+]+[S_i]\exp(+[\Gamma x])[I^-]-[\Gamma]^{-1}\sinh([\Gamma x])*\left([Y][v]\right)+\\ &\qquad [\Gamma]^{-1}\sinh([\Gamma x])*\frac{d[j]}{dx}\end{aligned} \tag{4-36}$$

where * denotes the convolution operator (that here shows the superposition of the all internal noise sources) and $\sinh([\Gamma x])$ is a square matrix, containing the hyperbolic sine of the $[\Gamma x]$ matrix elements.

4.5.3 Internal Noise Sources of Transistor

To calculate the noise source density, referring to Fig.4.6, we consider a noisy FET subsection with gate width Δx. For each subsection, equivalent to a noisy six-port, a model (including a noiseless six-port circuit and equivalent noise sources at its input ports) can be assigned.

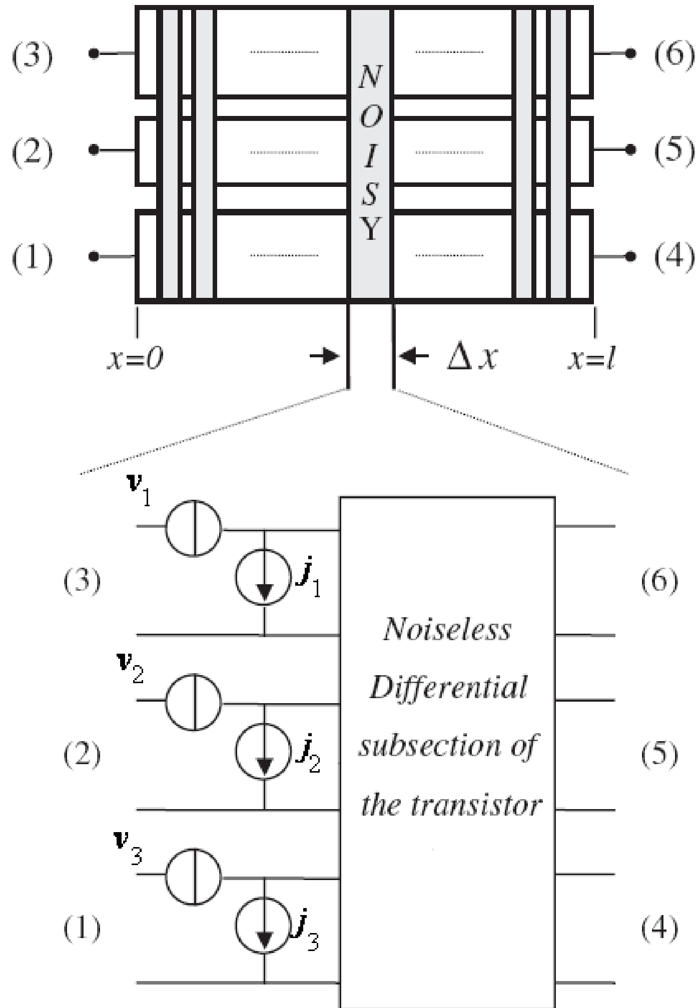


Fig.4.6 Noise equivalent voltage and current sources

In [26], a method to determine the density of these equivalent noise sources in the form of [*v*] and [*j*] vectors is introduced. In order to analyze the transistor noise behavior, it is necessary to consider these sources as excited sources.

In this case, relation (4-36) can be expressed as

$$[V(x)] = [S_v]\exp(-[\Gamma x])[V^+] + [S_v]\exp(+[\Gamma x])[V^-] - [\Gamma]^{-1}\sinh([\Gamma x]) * \left([Z][j]\right)$$
$$[I(x)] = [S_i]\exp(-[\Gamma x])[I^+] + [S_i]\exp(+[\Gamma x])[I^-] - [\Gamma]^{-1}\sinh([\Gamma x]) * \left([Y][v]\right) \quad (4\text{-}37)$$

The above equation, as transistor noise model response, is the main tool to analyze transistor noise.

4.5.4 Noise Correlation Matrix of Transistor

By knowing the transistor noise correlation matrix, we will be able to analyze the transistor noise behavior. In this part, by using the transmission line model correlation matrix, we can obtain the transistor noise parameters as a six-port network. To do so, we need first to get the vector components of [*v*] and [*j*]; then, by applying the boundary conditions at short-circuited terminals ($x = 0, x = l$), the unknown coefficients V^+ and V^- will be determined. According to [25]-[27], the unit-per-length noise correlation matrix for a chain representation of the transistor ($CA_{U.P.L}$) can be deduced

$$CA_{UPL} = \left\langle \begin{pmatrix} [v] \\ [j] \end{pmatrix} \begin{pmatrix} [v] \\ [j] \end{pmatrix}^+ \right\rangle = \left\langle \begin{matrix} CA_{U.P.L}^{11} & CA_{U.P.L}^{12} \\ CA_{U.P.L}^{21} & CA_{U.P.L}^{22} \end{matrix} \right\rangle \quad (4\text{-}38)$$

where $\langle\ \rangle$ denotes the ensemble average and "+" the complex conjugate transpose operator. From the correlation matrix definition, we can calculate [*v*] and [*j*], and thus fully describe the proposed FET noise model. In fact, the unknown coefficients of (4-37) can be determined using the boundary conditions at short-circuited terminals

$$\begin{cases} [V(x=l)] = [S_v]\exp(-[\Gamma l])[V^+] + [S_v]\exp(+[\Gamma l])[V^-] - [\Gamma]^{-1}\left(\int_{x'=0}^{l} \sinh([\Gamma x'])dx'\right)[Z]\,[j] = [0_{3\times1}] \\ [V(x=0)] = [S_v][V^+] + [S_v][V^-] - [\Gamma]^{-1}\left(\int_{x''}^{l} \sinh([\Gamma x'])dx'\right)[Z]\,[j] = [0_{3\times1}] \end{cases}$$

(4-39)

where $[\,0_{3\times1}\,]$ is a 3×1 vector which elements are all zeros. After calculating the integrals and using equations (4-28)-(4-30), we could write (4-39) in a matrix form

$$\begin{bmatrix} [S_v] & [S_v] \\ [S_v]\exp(-[\Gamma l]) & [S_v]\exp(+[\Gamma l]) \end{bmatrix} \begin{bmatrix} [V^+] \\ [V^-] \end{bmatrix} = \begin{bmatrix} (\cosh([\Gamma l]) - [U_{3\times3}])[Y]^{-1}][j] \\ (\cosh([\Gamma l]) - [U_{3\times3}])[Y]^{-1}][j] \end{bmatrix} \quad (4\text{-}40)$$

or

$$[K]\times\begin{bmatrix} [V^+] \\ [V^-] \end{bmatrix} = [N_y]\times\begin{bmatrix} [j] \\ [j] \end{bmatrix} \quad (4\text{-}41)$$

with

$$[N_y] = \begin{bmatrix} [\cosh(\Gamma l) - U_{3\times3}][Y]^{-1} & [0_{3\times3}] \\ [0_{3\times3}] & [\cosh(\Gamma l) - U_{3\times3}][Y]^{-1} \end{bmatrix} \quad (4\text{-}42)$$

From equations (4-40)-(4-42), we can evaluate the unknown coefficient matrix as

$$\begin{bmatrix} V^+ \\ V^- \end{bmatrix} = [K]^{-1}\times[N_y]\times\begin{bmatrix} j \\ j \end{bmatrix} \quad (4\text{-}43)$$

Thus, the currents at short-circuited ports can be achieved using equation (4-37).

$$\begin{cases} [I(x=l)] = [S_i]\exp(-[\Gamma l])[V^+] + [S_i]\exp(+[\Gamma l])[V^-] - (\cosh[\Gamma l] - [U_{3\times3}])([Z]^{-1}\,[v]) \\ [I(x=0)] = [S_i][V^+] + [S_i][V^-] - (\cosh[\Gamma l] - [U_{3\times3}])[Z]^{-1}\,[v] \end{cases}$$

(4-44)

From those equations, the noise currents at the output ports, as a six-port active network, can be written in the following matrix form

$$\begin{bmatrix} I_o \\ I_l \end{bmatrix} = \begin{bmatrix} -[S_i] & [S_i] \\ [S_i]\exp(-[\Gamma l]) & -[S_i]\exp(+[\Gamma l]) \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \end{bmatrix} - \begin{bmatrix} -(\cosh[\Gamma l] - [U_{3\times3}])[Z]^{-1}[v] \\ (\cosh[\Gamma l] - [U_{3\times3}])[Z]^{-1}[v] \end{bmatrix} \quad (4\text{-}45)$$

or

$$\begin{bmatrix} I_0 \\ I_l \end{bmatrix} = [M]\times\begin{bmatrix} V^+ \\ V^- \end{bmatrix} - [N_z]\times\begin{bmatrix} v \\ v \end{bmatrix} \quad (4\text{-}46)$$

where

$$[N_z]=\begin{bmatrix}[\cosh(\Gamma l)-U_{3\times 3}][Z]^{-1} & [0_{3\times 3}] \\ [0_{3\times 3}] & [\cosh(\Gamma l)-U_{3\times 3}][Z]^{-1}\end{bmatrix}$$

$$[M]=\begin{bmatrix}-[S_i] & [S_i] \\ [S_i]\exp(-[\Gamma l]) & -[S_i]\exp(+[\Gamma l])\end{bmatrix} \tag{4-47}$$

which reaches to the admittance correlation matrix of the noisy six-port FET

$$CY_l=\left\langle \begin{bmatrix}I_0\\ I_l\end{bmatrix}\begin{bmatrix}I_0\\ I_l\end{bmatrix}^+\right\rangle \tag{4-48}$$

By substituting (4-45) into (4-47) we can rewrite (4-48) as

$$CY_l=\left\langle \left\{([M][K^{-1}][N_y])\begin{bmatrix}j\\ j\end{bmatrix}-[N_z]\begin{bmatrix}v\\ v\end{bmatrix}\right\}\left\{([M][K^{-1}][N_y])\begin{bmatrix}j\\ j\end{bmatrix}-[N_z]\begin{bmatrix}v\\ v\end{bmatrix}\right\}^+\right\rangle \tag{4-49}$$

After some mathematical derivations, the correlation matrix of the transistor as

$$[CY_{tr}]=[[M][K]^{-1}[N_y]\left\langle\begin{bmatrix}j\\ j\end{bmatrix}\begin{bmatrix}j\\ j\end{bmatrix}^+\right\rangle[[M][K]^{-1}[N_y]]^+-[M][K]^{-1}[N_y]]\left\langle\begin{bmatrix}j\\ j\end{bmatrix}\begin{bmatrix}v\\ v\end{bmatrix}^+\right\rangle[N_z]^+$$

$$-[N_z]\left\langle\begin{bmatrix}v\\ v\end{bmatrix}\begin{bmatrix}j\\ j\end{bmatrix}^+\right\rangle[[M][K]^{-1}[N_y]]^{-1}+[N_z]\left\langle\begin{bmatrix}v\\ v\end{bmatrix}\begin{bmatrix}v\\ v\end{bmatrix}^+\right\rangle[N_z]^+ \tag{4-50}$$

Using the $CA_{U.P.L}$ matrix elements leads to

$$[CY_{tr}]=[M][K]^{-1}[N_y]\begin{bmatrix}CA_{U.P.L}^{22} & CA_{U.P.L}^{22}\\ CA_{U.P.L}^{22} & CA_{U.P.L}^{22}\end{bmatrix}[[M][K]^{-1}[N_y]]^+-$$

$$[M][K]^{-1}[N_y]\begin{bmatrix}CA_{U.P.L}^{21} & CA_{U.P.L}^{21}\\ CA_{U.P.L}^{21} & CA_{U.P.L}^{21}\end{bmatrix}[N_z]^+-[N_z]\begin{bmatrix}CA_{U.P.L}^{12} & CA_{U.P.L}^{12}\\ CA_{U.P.L}^{12} & CA_{U.P.L}^{12}\end{bmatrix}[[M][K]^{-1}[N_y]]^{-1}$$

$$+[N_z]\begin{bmatrix}CA_{U.P.L}^{11} & CA_{U.P.L}^{11}\\ CA_{U.P.L}^{11} & CA_{U.P.L}^{11}\end{bmatrix}[N_z]^+ \tag{4-51}$$

The above equation shows the correlation matrix of the whole FET.

4.6. Green's function

Assume we would like to find the solution of a linear equation in the form of

$$L\{\Psi(x)\} = f(x) \tag{4-52}$$

where L is a linear operator applied to a dependent variable $\Psi(x)$ and $f(x)$ a basis function [30], [31]. Green's function provides an alternative approach, other than an analytical method, for solving inhomogeneous boundary-value problems by reducing the inhomogeneous problem to a homogeneous one. If we define the basis function as an unit impulse function at the point ($x = x'$), equation (4-52) becomes

$$L\{\Psi_G(x)\} = \delta(x - x') \tag{4-53}$$

Replacing the basis function $f(x)$ with unit impulse function $\delta(x - x')$ leads to $L\{\Psi_G(x,x')\} = \delta(x - x')$ .where $\Psi_G(x,x')$ is considered response to $\delta(x - x')$. Considering the same boundary condition for (4-52) and (4-53), solving the second one would be much easier than the first one. Clearly, the response to a Dirac delta function with constant amplitude $f(x')$

$$L\{\Psi(x)\} = f(x')\delta(x - x') \tag{4-54}$$

can be written as

$$\Psi(x) = f(x')\Psi_G(x,x') \tag{4-55}$$

Since L is a linear operator, to obtain the total response we need to superpose all delta functions. Since $f(x)$ can be expressed as the integral of all unit point sources

$$f(x) = \int_{-\infty}^{+\infty} f(x')\delta(x - x')dx' \tag{4-56}$$

the total response will be

$$L\{f(x)\} = L\{\int_{-\infty}^{+\infty} f(x')\delta(x - x')dx'\} = \int_{-\infty}^{+\infty} f(x')L\{\{\delta(x - x')\}dx' \tag{4-57}$$

$$\Psi(x) = \int_{-\infty}^{+\infty} f(x')\Psi_G(x,x')dx' \tag{4-58}$$

4.6.1 Green's function in TL

To solve the linear equations (4-26) (i.e. to determine the response of the excited line) we should use a proper form of the Green's function, suitable for TL structure analysis [32]. The voltage differential equation of an excited TL is

$$\left\{\frac{d^2}{dx^2}-\gamma^2\right\}V^I(x)=Z\ j(x) \tag{4-59}$$

where $V^I(x)$ is the voltage response of a line excited by distributed current source j(x). By replacing the basis function of (4-59) with a point current source at $x = x'$ with a unity amplitude $1\times\delta(x-x')$ instead of a unit impulse function, we can rewrite the equation as

$$\left\{\frac{d^2}{dx^2}-\gamma^2\right\}V_G^I(x,x')=Z\delta(x-x') \tag{4-60}$$

where $V_G^I(x,x')$ is the voltage Green's function of the line. The voltage function of the line is the superposition of the voltage Green's functions (similar to wave problems)

$$V^I(x)=\int j(x')V_G^I(x,x')dx' \tag{4-61}$$

The current Green's function can be subsequently determined as

$$I_G^I(x,x')=-\frac{1}{Z}\frac{dV_G^I(x,x')}{dx} \tag{4-62}$$

The same procedure can be used to find the voltage and current functions of the TL excited by distributed voltage sources. Note that in general, the voltage and current functions of the TL, excited by both distributed voltage and current sources, can be written as

$$\begin{aligned}V(x)&=\int j(x')V_G^I(x,x')dx'+\int v(x')V_G^V(x,x')dx'\\ I(x)&=\int j(x')I_G^I(x,x')dx'+\int v(x')I_G^V(x,x')dx'\end{aligned} \tag{4-63}$$

where $I^{I}(x)$ is the response of a line excited by distributed current source $j(x)$ and $I^{V}(x)$ is the current response of a line excited by distributed voltage source $v(x)$.

4.6.2 Model Analysis

Fig.4.7. shows the distributed model of a transmission line excited by point voltage and current sources, located at $x = x'$ and terminated by specific loads at input and output. Dividing the structure into two source-free Left and Right sections, we can use equations (4-24) and (4-25) to determine the Green's functions.

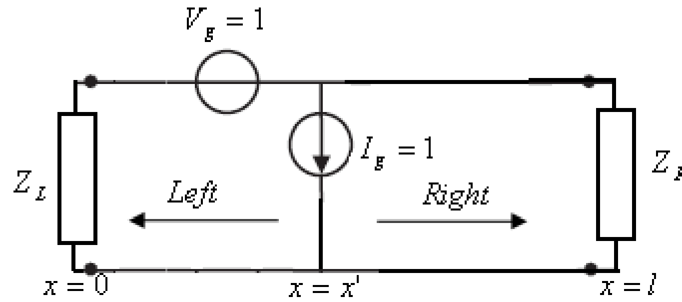


Fig.4.7. Transmission line excited by delta sources with unit amplitude

The equations have two unknown coefficients in each section. Applying Kirchhoff's laws to the following boundary conditions ($x = 0$, $x = l$) and sources ($x = x'$)

$$\begin{cases} [V_L^G](x=0) = -Z_L[I_L^G](x=0) \\ [V_R^G](x=l) = Z_R[I_R^G](x=l) \end{cases} \qquad (4\text{-}64)$$

gives

$$\begin{cases} [V_L^G](x=x') - [V_R^G](x=x') = 1^V \\ [I_L^G](x=x') - [I_R^G](x=x') = 1^I \end{cases} \qquad (4\text{-}65)$$

where superscripts L and R denote the Left ($x < x'$) and Right ($x > x'$) sections, respectively. 1^I and 1^V represent unit current and voltage delta functions. Fig.4.8. shows the modified TL model of the FET, excited by point voltage and current sources, located at $x = x'$.

Dividing the structure into two source-free Left and Right sections, leads to

$$[V_L^G(x)] = [S_v]\exp(-[\Gamma x])[V_L^+] + [S_v]\exp(+[\Gamma x])[V_L^-] \qquad x < x^{'}$$

$$[I_L^G(x)] = [S_i]\exp(-[\Gamma x])[V_L^+] + [S_i]\exp(+[\Gamma x])[V_L^-] \tag{4-66}$$

$$[V_R^G(x)] = [S_v]\exp(-[\Gamma(x - x^{'})])[V_R^+] + [S_v]\exp(+[\Gamma(x - x^{'})])[V_R^-] \qquad x > x^{'}$$

$$[I_R^G(x)] = [S_i]\exp(-[\Gamma(x - x^{'})])[V_R^+] + [S_i]\exp(+[\Gamma(x - x^{'})])[V_R^-] \tag{4-67}$$

To find the admittance correlation matrix of the transistor as a noisy six-port active network, the values of currents in the ports should be determined when they are all assumed short-circuited simultaneously [26]. At simultaneously shorted ports (i.e. at $x = 0$ and $x = l$),

$$\begin{cases} [V_R(x = l)] = [S_v]\exp(-[\Gamma(l - x^{'})])[V_R^+] + [S_v]\exp(+[\Gamma(l - x^{'})])[V_R^-] = [0_{3\times1}] \\ [V_L(x = 0)] = [S_v][V_L^+] + [S_v][V_L^-] = [0_{3\times1}] \end{cases} \tag{4-68}$$

and by applying Kirchoff's laws at $x = x^{'}$,

$$\begin{cases} [V_L(x = x^{'})] - [V_R(x = x^{'})] = ([S_v]\exp(-[\Gamma x^{'}])[V_L^+] + [S_v]\exp(+[\Gamma x'])[V_L^-]) - \\ \qquad ([S_v][V_R^+] + [S_v][V_R^-]) = [1_{3\times1}^v] \\ [I_L(x = x^{'})] - [I_R(x = x^{'})] = ([S_i]\exp(-[\Gamma x^{'}])[V_L^+] - [S_i]\exp(+[\Gamma x^{'}])[V_L^-]) - \\ \qquad ([S_i][V_R^+] - [S_i][V_R^-]) = [1_{3\times1}^I] \end{cases} \tag{4-69}$$

where $[1_{3\times1}^V]$ and $[1_{3\times1}^I]$ are 3×1 vectors with unit elements, indicating the point voltage and current sources, respectively.

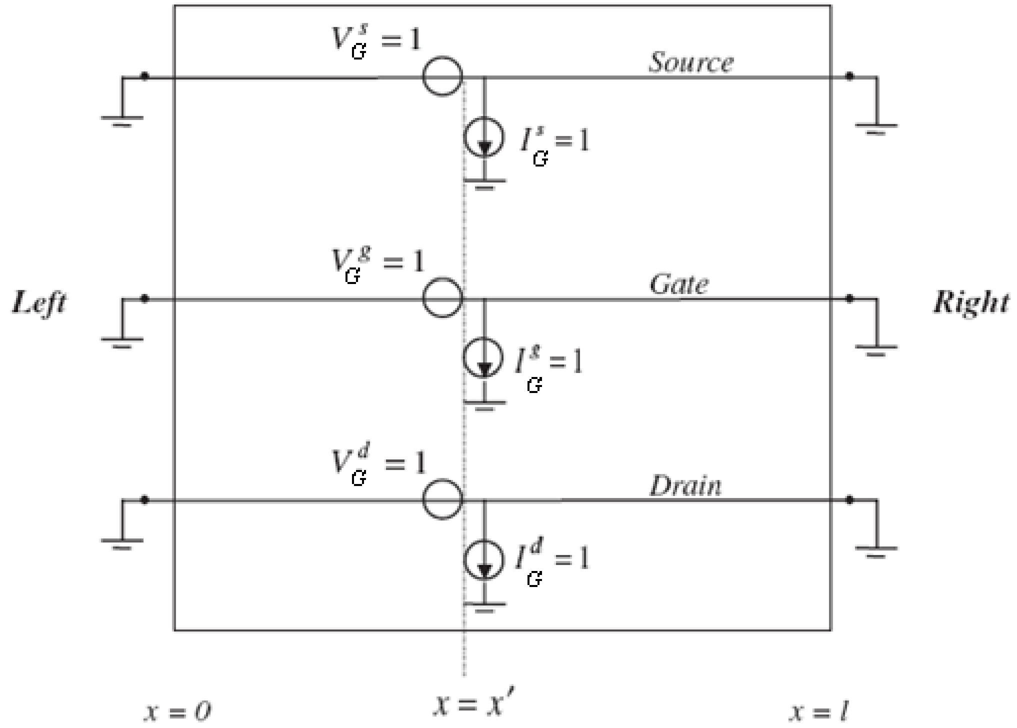


Fig.4.8. TL model of the FET excited by point voltage and current sources

Equations (4-68) and (4-69) can be written in a matrix form as follow

$$\begin{bmatrix} -[S_v] & -[S_v] & [S_v]e^{-[\Gamma x']} & [S_v]e^{[\Gamma x']} \\ -[S_i] & [S_i] & [S_i]e^{-[\Gamma x']} & -[S_i]e^{[\Gamma x']} \\ e^{-[\Gamma(l-x')]} & e^{-[\Gamma(l-x')]} & 0_{3\times3} & 0_{3\times3} \\ 0_{3\times3} & 0_{3\times3} & U_{3\times3} & U_{3\times3} \end{bmatrix} \begin{bmatrix} [V_R^+] \\ [V_R^-] \\ [V_L^+] \\ [V_L^-] \end{bmatrix} = \begin{bmatrix} 1_{3\times1}^v \\ 1_{3\times1}^I \\ 0_{3\times1} \\ 0_{3\times1} \end{bmatrix} \tag{4-70}$$

By solving this set of 12 equations in (4-70) and considering the boundary conditions, the undetermined constant vectors $[V_R^\pm]$ and $[V_L^\pm]$, can be determined. From the third and fourth rows of the above matrix, traveling and reflecting wave coefficients in the two regions can be expressed as

$$\begin{cases} [V_R^-] = -e^{-2[\Gamma(l-x')]}[V_R^+] \\ [V_L^-] = -[V_L^+] \end{cases} \tag{4-71}$$

Replacing (4-71) into the boundary condition (4-70) leads us to

$$\begin{cases} [V_R^+] = \frac{1}{2} e^{[\Gamma(l-x^{'})]} (\sinh[\Gamma l])^{-1} \left\{ -\cosh[\Gamma x^{'}][S_v]^{-1}.[1_{3\times1}^v] - \sinh[\Gamma x^{'}].[S_i]^{-1}.[1_{3\times1}^I] \right\} \\ [V_L^-] = \frac{1}{2} (\sinh[\Gamma l])^{-1} \left\{ -\cosh[\Gamma(l-x^{'})][.S_v]^{-1}.[1_{3\times1}^v] - \sinh[\Gamma(l-x^{'})][S_i]^{-1}.[1_{3\times1}^I] \right\} \end{cases} \quad (4\text{-}72)$$

By substituting $[V_R^{\pm}]$ and $[V_L^{\pm}]$ into (4-66) and (4-67), the Green's functions can be written as

$$\begin{cases} [V_L^G] = [S_V].\sinh[\Gamma x].(\sinh([\Gamma l])^{-1} \left\{ \cosh[\Gamma(l-x^{'})].[S_v]^{-1}.[1_{3\times1}^v] - \sinh[\Gamma(l-x^{'})][S_i]^{-1}.[1_{3\times1}^I] \right\} \\ [I_L^G] = [S_i].\cosh[\Gamma x].(\sinh([\Gamma l])^{-1} \left\{ -\cosh[\Gamma(l-x^{'})].[S_v]^{-1}.[1_{3\times1}^v] + \sinh[\Gamma(l-x^{'})].[S_i]^{-1}.[1_{3\times1}^I] \right\} \end{cases}$$
(4-73)

$$\begin{cases} [V_R^G] = [S_V].\sinh[\Gamma(l-x)].(\sinh[\Gamma l]^{-1} \left\{ -\cosh[\Gamma x^{'}].[S_v]^{-1}.[1_{3\times1}^v] - \sinh([\Gamma x^{'}]).[S_i]^{-1}.[1_{3\times1}^I] \right\} \\ [I_R^G] = [S_i.]\cosh[\Gamma(l-x])].(\sinh[\Gamma l])^{-1} \left\{ -\cosh([\Gamma x^{'}]).[S_v]^{-1}.[1_{3\times1}^v] - \sinh([\Gamma x^{'}]).[S_i]^{-1}.[1_{3\times1}^I] \right\} \end{cases}$$
(4-74)

The currents at the short-circuited ports can be determined by substituting the current Green's functions of (4-73) and (4-74) into (4-63):

$$\begin{cases} [I](x=0) = [I_L](x=0) = \int_{x^{'}=0}^{l} [I_L^G](x=0,x^{'})\Big|_{\begin{cases}([1_{3\times1}^v]=[v]) \\ ([1_{3\times1}^I]=[j])\end{cases}} dx^{'} \\ [I](x=l) = [I_R](x=l) = \int_{x^{'}=0}^{l} [I_R^G](x=l,x^{'})\Big|_{\begin{cases}[([1_{3\times1}^v]=[v]) \\ ([1_{3\times1}^I]=[j])\end{cases}} dx^{'} \end{cases} \quad (4\text{-}75)$$

where the point sources with unity amplitude were replaced by the linear density of the distributed noise-equivalent voltage and current sources. Integration over the gate width, $x' = [0, l]$ in (4-75) indicates the superposition of all distributed sources.

Then the currents of the short-circuited ports can be determined as

$$\begin{cases} \begin{bmatrix}[I_0]\\ [I_l]\end{bmatrix} = \begin{bmatrix}-[I(x=0)]\\ +[I(x=l)]\end{bmatrix} = \begin{bmatrix}[A] & [B]\\ -[A] & [B]\end{bmatrix}\begin{bmatrix}[v]\\ [j]\end{bmatrix} = [K]\times\begin{bmatrix}[v]\\ [j]\end{bmatrix} \\ [A]=[Z]^{-1} \\ [B] = -[S_i].[\Gamma]^{-1}.(\sinh[\Gamma l])^{-1}.(\cosh[\Gamma l]-[1_{3\times 1}]).[S_i]^{-1} \end{cases} \quad (4\text{-}76)$$

According to [28], the admittance correlation matrix of the six-port noise model of the FET can be finally written as

$$[CY_{tr}] = \left\langle \begin{bmatrix}[I_0]\\ [I_l]\end{bmatrix}\begin{bmatrix}[I_0]\\ [I_l]\end{bmatrix}^+ \right\rangle = \left\langle \left([K]\begin{bmatrix}[v]\\ [j]\end{bmatrix}\right)\left([K]\begin{bmatrix}[v]\\ [j]\end{bmatrix}\right)^+ \right\rangle$$

$$[CY_{tr}] = [K]\left\langle \begin{bmatrix}[v]\\ [j]\end{bmatrix}\begin{bmatrix}[v]\\ [j]\end{bmatrix}^+ \right\rangle [K]^+ = [K]\begin{pmatrix}\langle [v][v^+]\rangle & \langle [v][j^+]\rangle \\ \langle [j][v^+]\rangle & \langle [j][j^+]\rangle\end{pmatrix}[K]^+ = [K]\times CA_{U.P.L}\times[K]^+ \quad (4\text{-}77)$$

4.7. Experimental Setup

The noise figure of any device is a function of the device noise parameters and the source impedance presented to the input of the device. Noise figure measurements at different source impedance are required to determine the noise parameter of the device. The noise figure measurement setup used in this work is from Focus Company (Fig.4.9).

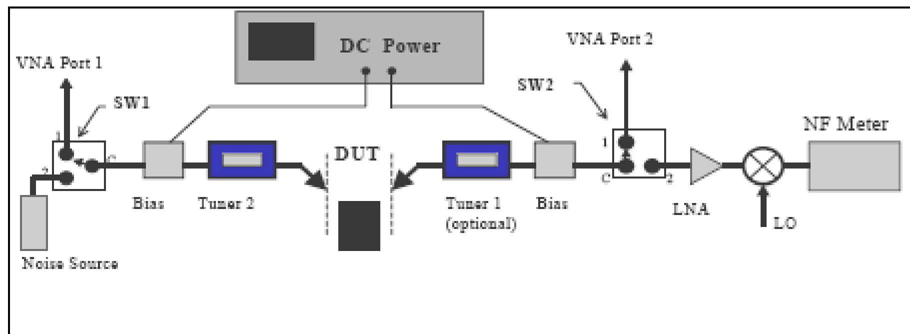
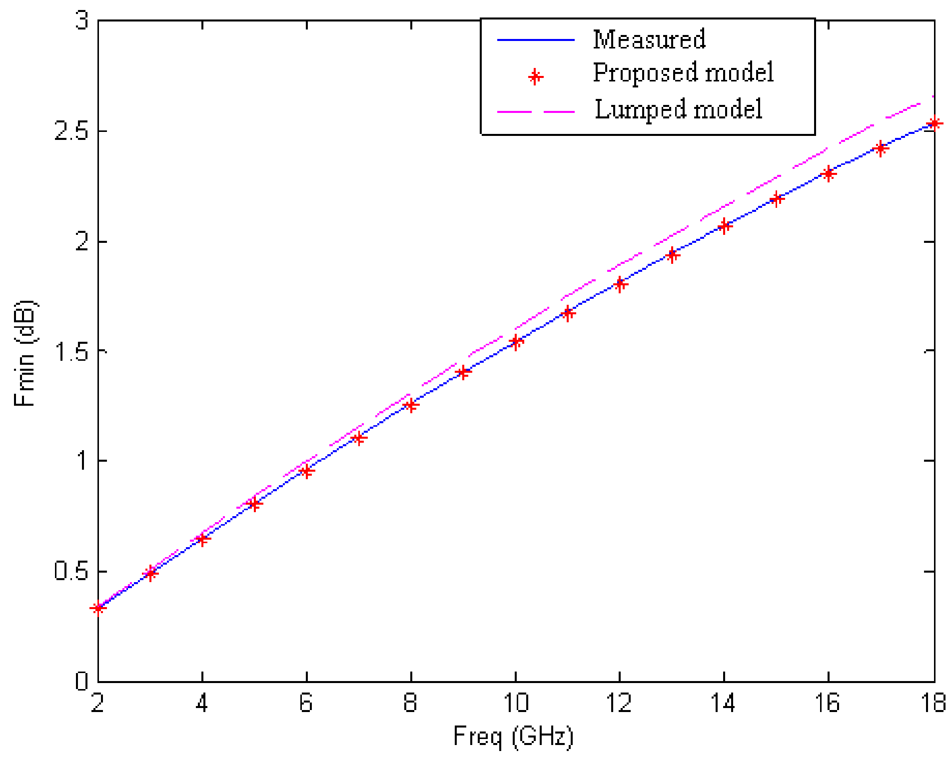


Fig.4.9.Schematic of the source-pull noise figure setup.

The losses between the DUT output and the receiver LNA must be as low as possible. A programmable tuner is inserted in the input network of the setup and used to control the source impedance presented to the DUT, while the output tuner is optional. Bias networks are positioned on the opposite side of the tuner(s). Two switches (SW1 and SW2) are required for a fully automated setup. The switches allow performing setup calibration and S-parameter measurements on the DUT without manual user interaction, thus improving the system accuracy and measurement repeatability. Noise figure measurements were performed with a PC–controlled source–pull noise figure setup. The HP 8970S noise-figure meter system consists of the HP 8970B noise figure meter, the HP 8970C test set, and a signal generator that acts as a local oscillator for the 8970C. Typical error is ±0.15 dB. To find the device minimum noise figure, variable source impedance is generated by a CCMT1809 mechanical motorized tuner. The load tuner was set to 50Ω. The device gain during measurement could have been improved by moving the load tuner to a small-signal match, but due to a combination of hardware and software problems better measurements were obtained with it at the reference impedance. However, the software automatically calculates the gain for a noise input match and power output match.

The devices S-parameters at each bias are needed. A MT998C RF switch box and an HP 8722D vector network analyzer (VNA) made it possible to seamlessly switch between noise and S-parameter measurements of devices. All components were controlled over a general-purpose interface bus (GPIB) by a software program, which calculates the noise parameters. To prove the accuracy of the proposed wave treatment in noise analysis, the calculated results are compared to both measured values and simulated results from the lumped model. Calculated and measured values of minimum noise figures and normalized equivalent noise admittance are plotted in Fig.4.10. Amplitude and phase of the optimum reflection coefficient are plotted in Fig.4.11. As shown, we have excellent agreement between our results and measured data. For larger widths, the thermal noise of the gate increases due to the higher gate resistance while for smaller gate widths, the minimum noise figure increases as the capacitances do not scale proportionally with the gate width due to an offset in capacitance at gate width zero [28].



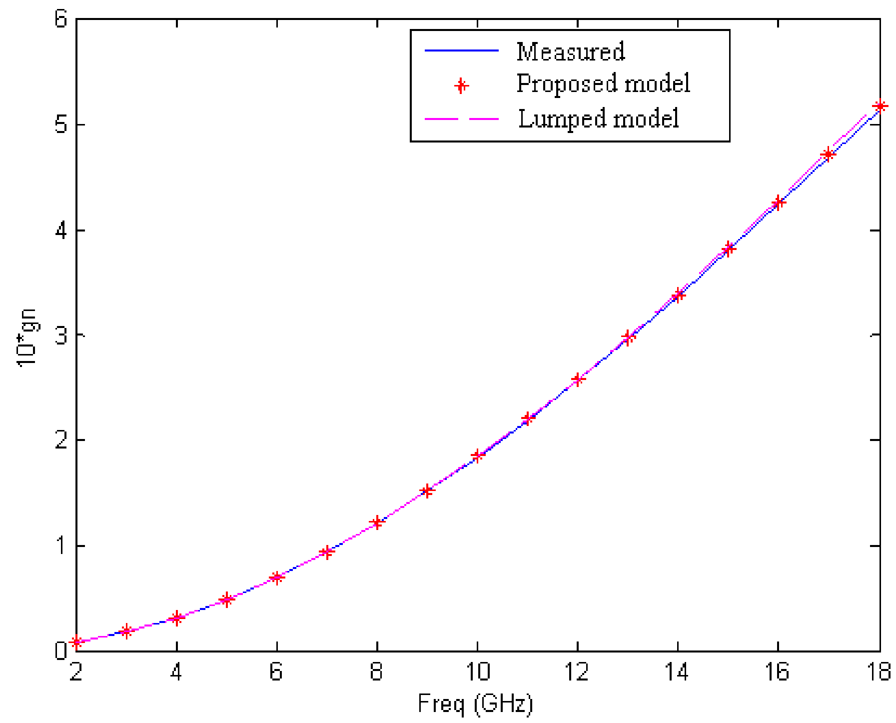


Fig. 4.10. Normalized equivalent noise admittance and noise figure for measured, proposed model and lumped model

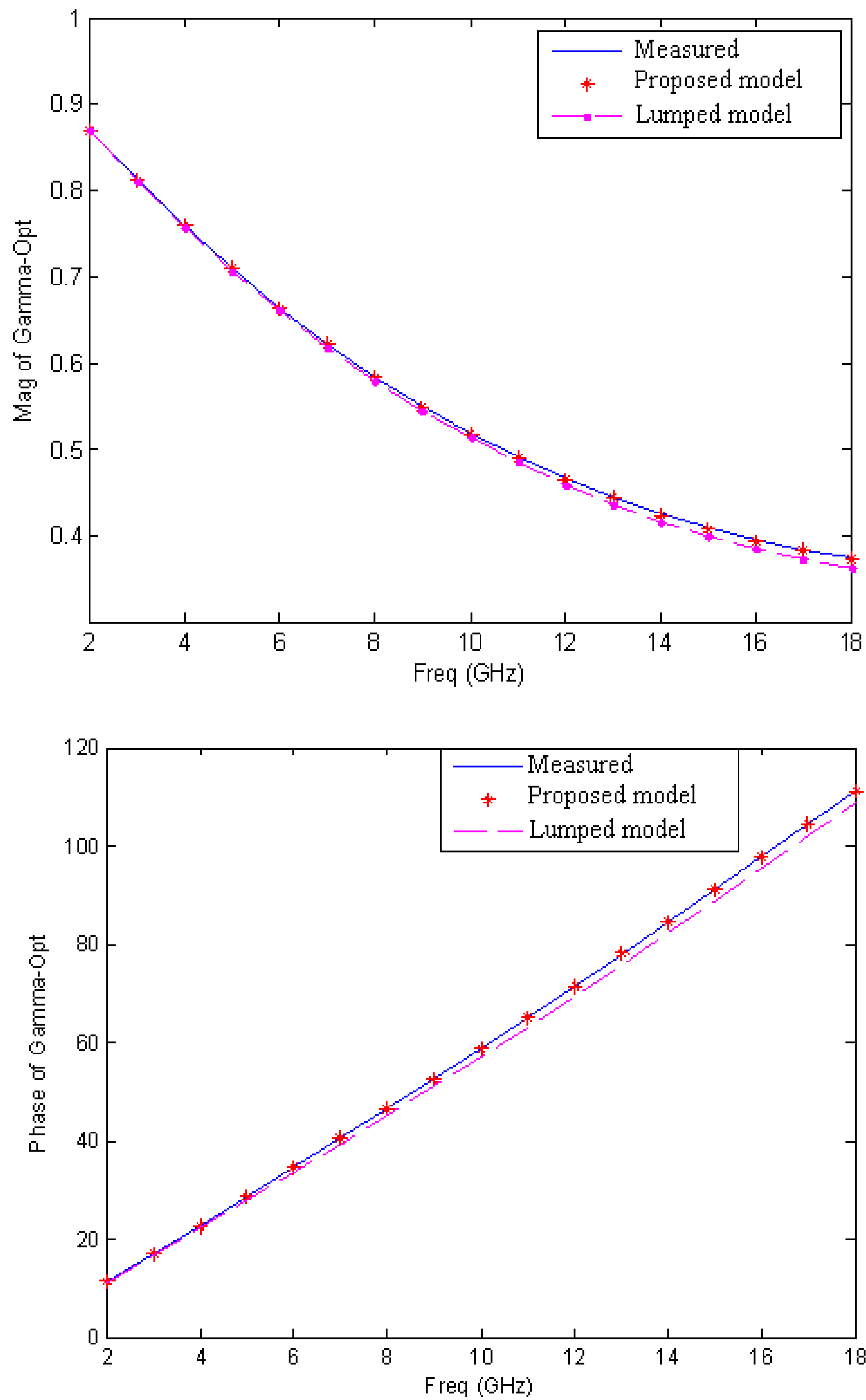


Fig. 4.11. Optimum reflection coefficient: simulated results (lumped model and proposed model) vs. measured values

4.8. Numerical Results

The above noise analysis approach was applied to analyze the NE710 FET biased at V_{ds} = 3V and I_{ds} = 10mA [29]. Based on the Green's function concept, we developed a code by which the signal and noise performance of the transistor can be analyzed simultaneously. We first generated the constant noise figure and power gain of the above FET. Fig.4.12 and Fig.4.13 show the constant noise figure and available power gain circles for three different frequencies, respectively. Thus, we can apply our approach for a specified noise figure and available power gain. To determine the proposed wave model in noise analysis, our results were compared to those obtained with the circuit-based model [31] and the Laplace approach.

Indeed, as shown in Fig.4.14 to 4.16, our results are in good agreement with the Laplace approach for the minimum noise figure (F_{min}), the normalized equivalent noise admittance (g_n=1/R_n), and the amplitude and phase of the optimum reflection coefficient, respectively.

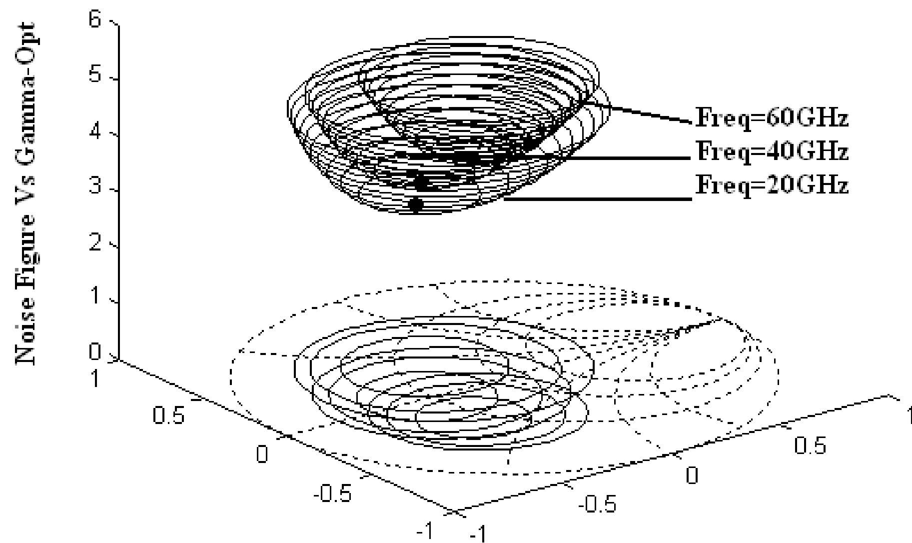


Fig.4.12. Noise figure circles for three different frequencies versus the source admittance

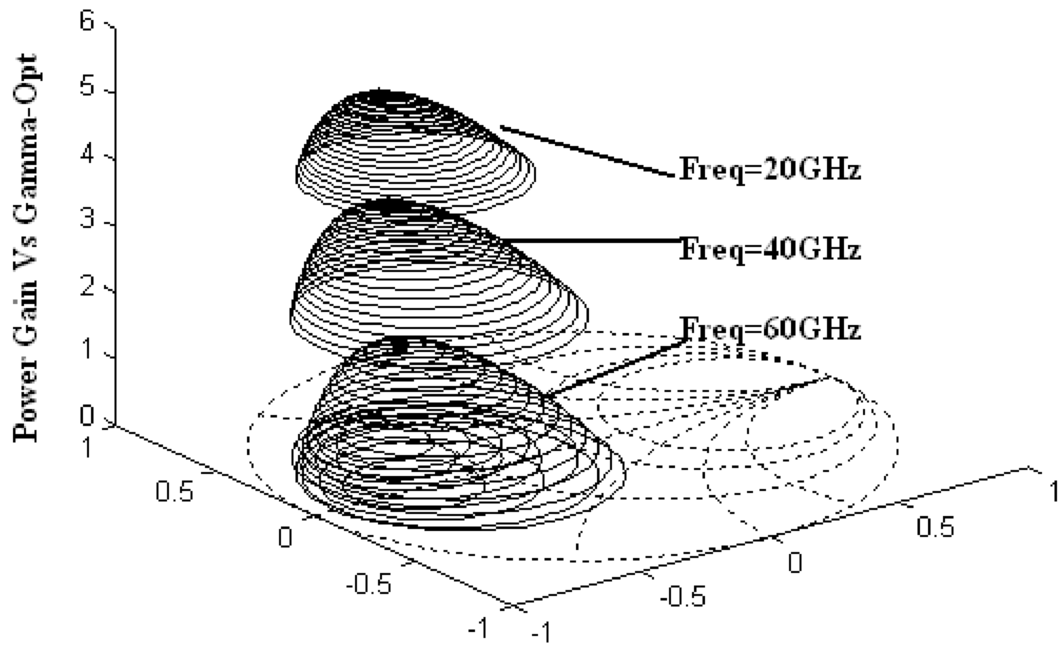


Fig.4.13. Power Gain circles for three different frequencies versus the source admittance

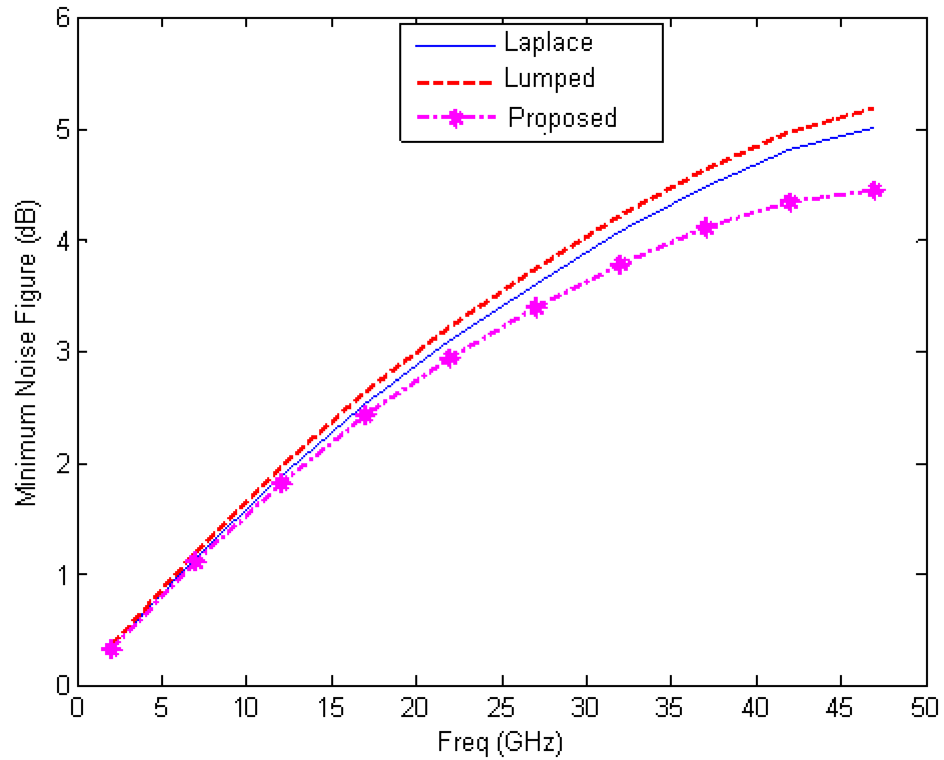


Fig.4.14.Minimum noise figure for lumped model, Laplace method and proposed model

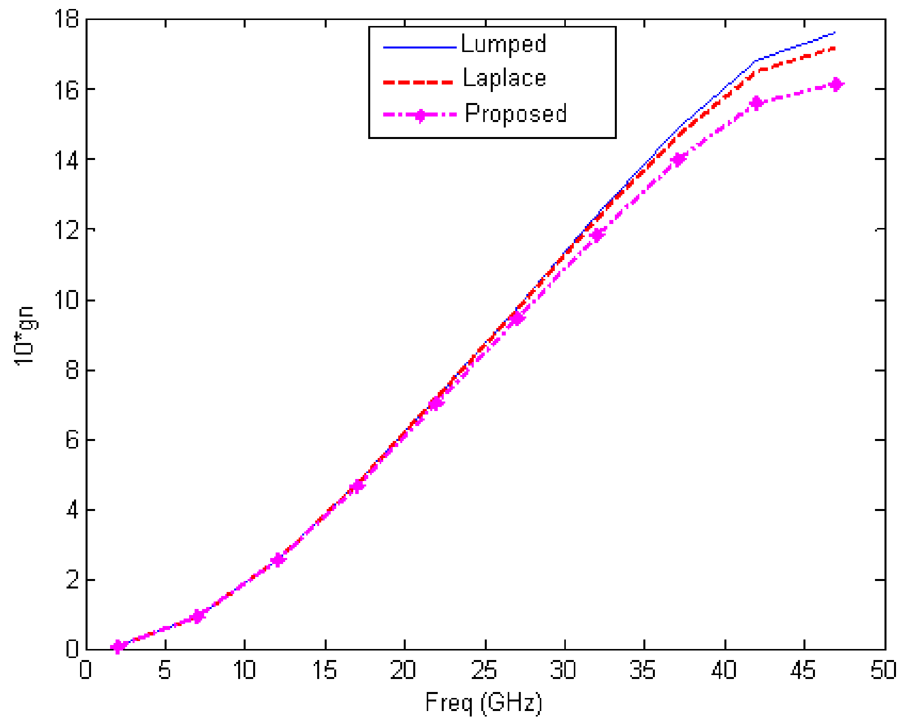


Fig.4.15. Normalized equivalent noise admittance for lumped model, Laplace method and proposed model

5.5 Conclusion

A new modeling approach for noise analysis of high frequency transistors was presented. This method can accurately take into account the effect of wave propagation along the device electrodes. The promising model can be applied to solve issues related to simultaneous signal and noise analysis, as well as in modeling traveling wave FETs in which the gate width is much higher than that of a usual FET. In addition, FET model makes it possible to predict the noise parameters up to the millimeter-wave range. This theoretical prediction should be confirmed with further experimental investigation as amid-term target for the research team. To demonstrate the efficiency of our model in terms of noise, we applied the Laplace transformation and the Green's function method to the device as an active multi-conductor transmission line structure and successfully compared the simulated response to measurements. Furthermore, by easily including the effects of scaling, the proposed algorithm is suitable for integration in computer-aided-design (CAD) packages for MMIC design.

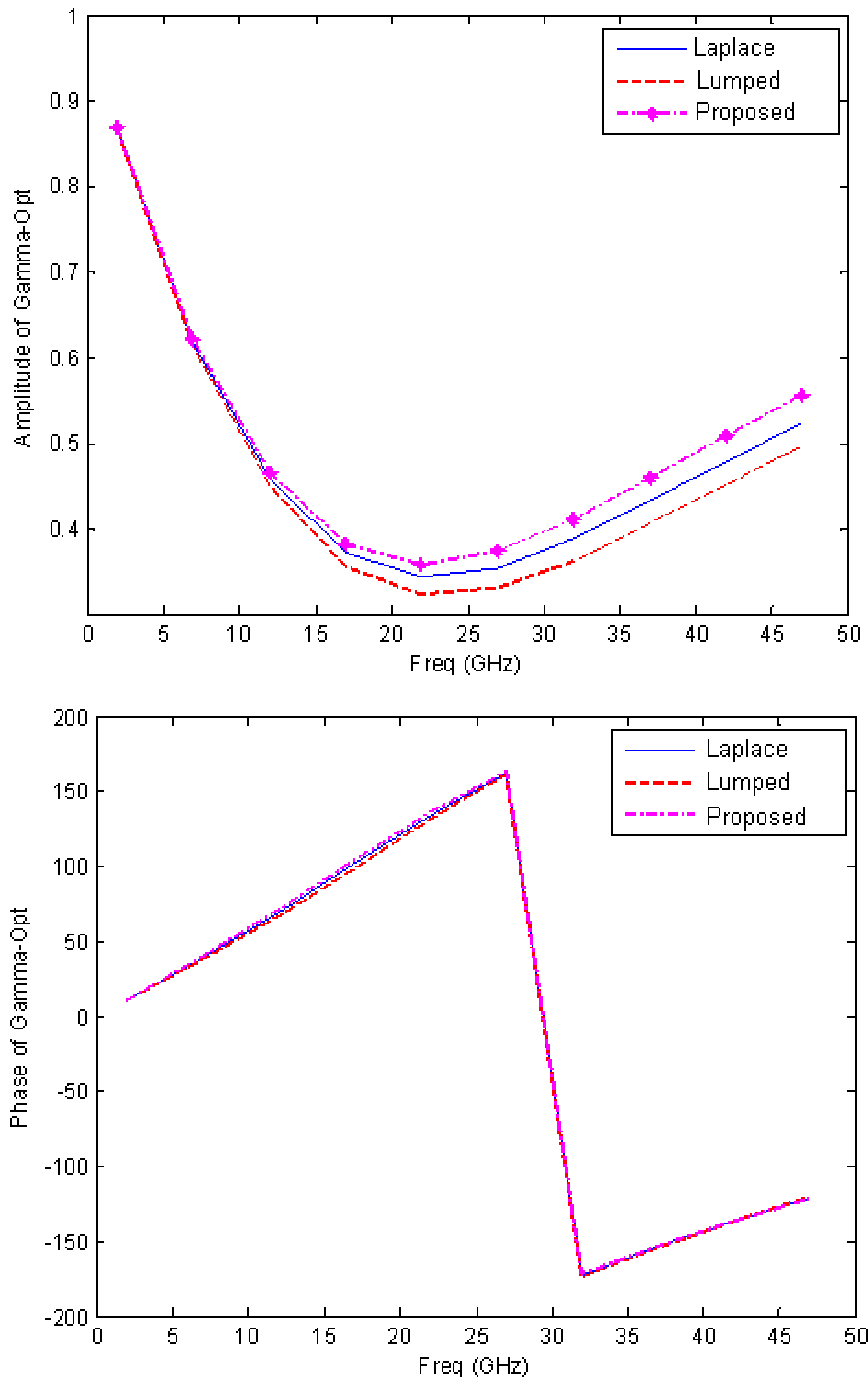


Fig.4.16. The results of lumped modeling, proposed model and Laplace method of amplitude and the phase of optimum reflection coefficient

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Chapter 5 Amplifier Design based on the FET Models

5.1. Introduction

The linear and nonlinear transistor models have been validated at the component level. To further demonstrate their efficiency, they should be integrated at the circuit level. For this aim, we first designed and tested a three-stage low noise distributed amplifier. Then, a fully integrated E-band power amplifier was simulated using the 90 nm CMOS technology.

5.2. Distributed Low Noise Amplifier Characteristics

Distributed amplifiers were first introduced by Ginzton in 1948 [1]. From this time, extensive successful research and development efforts have been made in broadband communication systems and various applications that require wideband amplification with good phase linearity [2]. In the early 80's, distributed amplifiers were successfully implemented as monolithic microwave integrated circuits (MMICs), which inspired a new wave of exploration, including design guidelines [3], noise analysis [4], application of new circuit techniques [5], to name a few. Distributed amplifiers have also been implemented in state-of-art silicon technologies [6], [7].

A distributed amplifier is made up of a series of active device cells distributed between two transmission lines. A schematic representation of a five section FET distributed amplifier is shown in Fig.5.1. The resultant transmission lines are referred to as the gate and drain lines coupled by the transconductances of the FETs. An RF signal applied at the input end of the gate line travels down the line to the terminated end. Assuming the transmission lines to be lossless, the FET transistors could be modeled as a gate source capacitance, drain source capacitance and a transconductance. Since the transmission lines are periodically loaded with the devices, these capacitances can be assumed to be uniformly distributed across the length of a unit cell transmission line, i.e., C_{gs} of each transistor across a gate line length of l_g, from $-l_g/2$ to $l_g/2$ to and C_{ds} of each transistor across a drain line length of l_d, from $-l_d/2$ to $l_d/2$ for each section.

If the intrinsic gate and drain lines have their distributed parameters given by L_d, C_d, L_g and C_g then the propagation constant and the characteristic impedance of the loaded lines are given by [2]

$$\gamma_g = \alpha_g + j\beta_g = \sqrt{ZY} = \sqrt{j\omega L_g \left(j\omega C_g + \frac{j\omega C_{gs}/l_g}{1 + j\omega R_i C_{gs}} \right)} \tag{5-1}$$

$$Z_g^c = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_g}{C_g + C_{gs}/l_g}} \tag{5-2}$$

for the gate line and

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{ZY} = \sqrt{j\omega L_d \left(\frac{1}{R_{ds} l_d} + j\omega (C_d + C_{ds}/l_d) \right)} \tag{5-3}$$

$$Z_d^c = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}} \tag{5-4}$$

for the drain line.

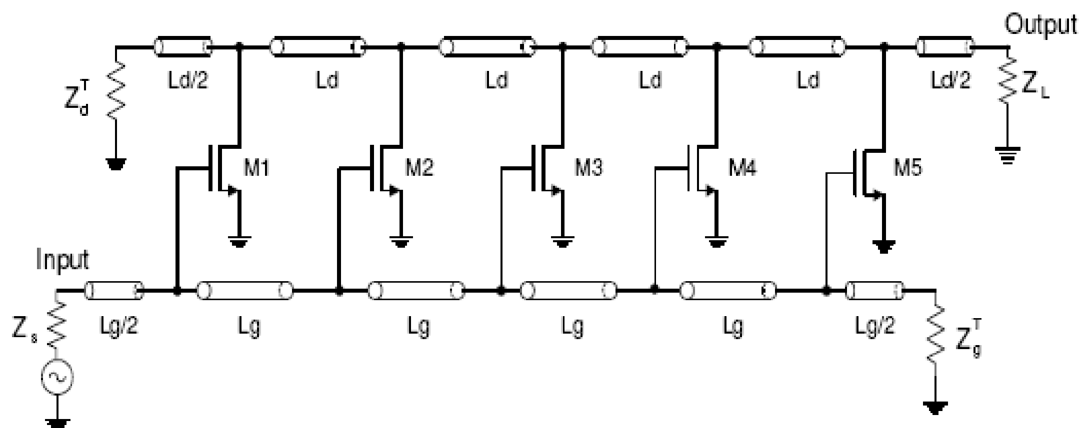


Fig.5.1. Schematic of FET distributed amplifier

5.2.1 Gain of the Distributed Amplifier

The current due to the transconductance can be assumed to be spread across each segment of the line. Under perfect matching conditions, both lines are terminated by their characteristic impedances i.e.

$$Z_s = Z_g^c = Z_g^T \tag{5-5}$$

and

$$Z_L = Z_d^c = Z_d^T \tag{5-6}$$

Assuming phase synchronization on each of the lines, we have

$$\beta_g l_g = \beta_d l_d = \beta l = \theta \tag{5-7}$$

According to [2], the distributed amplifier voltage gain is given by

$$A_v = -\frac{N g_m Z_d^C}{2} e^{-jN\theta} \tag{5-8}$$

where N is the number of stages and G_m the transconductance. The theoretical power gain of the distributed amplifier (assuming lossless transmission lines) can be written as [1]

$$G = \frac{N^2 G_m{}^2 Z_d^C Z_g^C}{4} \tag{5-9}$$

Note that the contribution of the imaginary part of the propagation constants is negligible in the useful frequency range [1], [4].

Under phase synchronization condition of (5.7), the power gain of the amplifier can be approximated as [2]

$$G \approx \frac{G_m^2 Z_d^C Z_g^C}{4} \left| \frac{e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d}}{\alpha_d l_d - \alpha_g l_g} \right| \qquad (5\text{-}10)$$

5.2.2 Noise Figure of the Distributed Amplifier

In order to design an amplifier with low noise characteristics one needs to identify the important noise sources in the amplifier and the key controllable contributors to the overall noise figure of the amplifier. Referring to Fig.4.4, the intrinsic noise sources of the transistor are [2]:

- *Drain channel noise* ($\bar{i}_{nd}^2$): This is the thermal noise due to the carriers in the channel region. This is given by $\bar{i}_{nd}^2 = 4kT\gamma G_{m0}\Delta f$ where γ is a bias dependent parameter, G_{m0} the zero drain voltage conductance of the device, k the Boltzmann's constant, T the temperature of the carriers in the channel and Δf the noise bandwidth.
- *Gate resistance noise* ($\overline{V}_{ng}^2$): This is the thermal noise generated by the gate resistance and is given by $\overline{V}_{ng}^2 = 4kT\frac{R_g}{3}\frac{W}{L}\Delta f$, where W is the gate width and L the length of the channel region.
- *Induced gate noise* ($\bar{i}_{ng}^2$): This noise is due to the thermal noise generated by the carriers in the channel, which capacitively couples itself onto the gate node as a gate current and is given by $\bar{i}_{ng}^2 = 4kT\delta\frac{\omega^2 C_{gs}^2}{5G_{m0}}\Delta f$ where δ is the gate noise coefficient.

Since the channel drain noise and the induced gate noise have the same physical origin, they are correlated with a correlation coefficient defined as $c = \frac{\overline{i_{ng}.i_{nd}^*}}{\sqrt{i_{ng}^2.i_{nd}^2}}$.

The long channel value of c is theoretically j0.4 and approaches j0.3 as the frequency of operation increases.

Assuming that the losses due to the transmission lines can be ignored for simplicity, the only other noise contributors are the termination and the source resistors. Again, the noise due to each transistor can be considered uncorrelated. Now, assuming that the drain current source is distributed across each segment of the transmission line implies that the drain line is periodically driven by a noise current given by $\frac{i_{nd}}{l_d}$.

The proposed equivalent circuit is shown in Fig.5.2.The noise voltage at the load due to the noise current source of the kth section is [2]-[5]

$$v_{nd,k} = \int_{(k-1)l_d}^{kl_d} \frac{i_{nd}}{l_d} \frac{Z_d^c}{2} e^{-j\beta_d(Nl_d - x_d)} dx_d = \frac{1}{2} i_{nd} Z_d^c \left(\frac{\sin\frac{\theta}{2}}{\theta/2} \right) e^{-j\theta(N-k+\frac{1}{2})} \qquad (5\text{-}11)$$

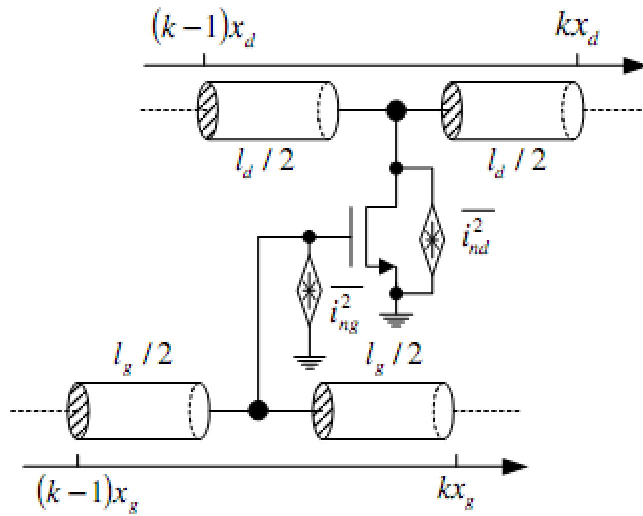


Fig. 5.2. Noise model of a unit-section of the distributed amplifier

When the gate noise is injected into the kth section gate line at $(k-1)l_g$ then the noise voltage due to the gate noise at the load has two components [8]-[9]; one due to the forward propagation

$$v_{ng,k}^{+} = \frac{1}{4} G_m Z_g^C Z_d^C i_{ng} \left(N - k + \frac{1}{2} \right) e^{-j\left(N-k+\frac{1}{2}\right)\theta} \tag{5-12}$$

and one due to the reverse propagation

$$v_{ng,k}^{-} = \frac{1}{4} G_m Z_g^C Z_d^C i_{ng} \frac{\sin\left(k - \frac{1}{2} \right)\theta}{\theta} e^{-j\left(N-\frac{1}{2}\right)\theta} e^{-j\left(N-k+\frac{1}{2}\right)\theta} \tag{5-13}$$

where N is number of stages in distributed amplifier. Combining (5.11), (5.12) and (5.13) results in the total output noise voltage in the kth section

$$v_{n0,k} = \left[\left(\frac{\sin \frac{\theta}{2}}{\theta} \right) i_{nd} + \frac{1}{4} M(k) G_m Z_g^c i_{ng} \right] Z_d^c e^{-j\left(N-k+\frac{1}{2}\right)\theta} \tag{5-14}$$

where

$$M(k) = \left(N - k + \frac{1}{2} \right) + \frac{\sin\left(k - \frac{1}{2} \right)\theta}{\theta} e^{-j\left(k-\frac{1}{2}\right)\theta}.$$

The currents i_{ng} and i_{nd} are correlated with a correlation coefficient c. Hence i_{ng} can be decomposed into two parts; one correlated with i_{nd} (i.e., i_{ngc}) and the second completely uncorrelated and noted i_{ngu}. Hence, [6]-[10]

$$i_{ng} = i_{ngu} + i_{ngc} \tag{5-15}$$

where

$$\bar{i}_{ngu}^{2} = 4kTG_u \Delta f \tag{5-16}$$

$$i_{ngc} = F_c i_{nd} \tag{5-17}$$

and

$$G_u = \delta \frac{\omega^2 C_{gs}^2}{5G_{m0}} (1 - |c|^2) \tag{5-18}$$

$$F_c = j|c| \sqrt{\frac{\delta}{5\gamma}} \frac{\omega C_{gs}}{G_{m0}} \tag{5-19}$$

By substituting them into (5.14), the total noise power at the load due to the transistor is given by

$$P_{n0} = 4kTG_m Z_d^c \frac{\gamma}{\alpha} \Delta f \sum_{k=1}^{N} \left| \frac{\sin \frac{\theta}{2}}{\theta} + \frac{1}{4} G_m Z_g^c F_c M(k) \right|^2 + \frac{1}{4} kTG_m^2 G_u (Z_g^c)^2 Z_d^c \Delta f \sum_{k=1}^{N} |M(k)|^2$$

(5-20)

where $\alpha = \frac{G_m}{G_{m0}}$. Note that in the above equation, the contribution of the gate resistance noise is ignored.

The output noise power due to the drain line termination impedance Z_d^T is given by

$$P_{ndT} = kT\Delta f \tag{5-21}$$

while the one due to the gate line termination impedance is given by

$$P_{ngT} = kT\Delta f G \left| \frac{\sin N\theta}{N\theta} \right|^2 \tag{5-22}$$

and the one due to the source resistance is given by

$$P_{nS} = kT\Delta f \tag{5-23}$$

Hence from the definition of a noise figure, the noise figure of an *N*-stage distributed amplifier is given by [11]

$$F = 1 + \frac{P_{ngT} + P_{ndT} + P_{n0}}{P_{nS} G} \tag{5-24}$$

where the gain *G* is given by (5.9). Thus,

$$F = 1 + \left| \frac{\sin N\theta}{N\theta} \right|^2 + \frac{4}{N^2 G_m^2 Z_d^c Z_g^c} + \frac{16}{N^2 G_m Z_g^c} \frac{\gamma}{\alpha} \sum_{k=1}^{N} \left| \frac{\sin \frac{\theta}{2}}{\theta} + \frac{1}{4} G_m Z_g^c F_c M(k) \right|^2 + \frac{1}{N^2} G_u Z_g^c \sum_{k=1}^{N} \left| M(k) \right|^2$$

(5-25)

Equation (5.25) can be further simplified by assuming large values of *N*. In that case

$$\sum_{k=1}^{N} \left| M(k) \right|^2 \approx \sum_{k=1}^{N} \left| (N - k + \frac{1}{2}) \right|^2 = \frac{N^3}{3} \tag{5-26}$$

Hence,

$$\sum_{k=1}^{N} \left| \frac{\sin \frac{\theta}{2}}{\theta} + \frac{1}{4} G_m Z_g^c F_c M(k) \right|^2 \approx N \left(\frac{\sin \frac{\theta}{2}}{\theta} \right)^2 + \frac{1}{16} G_m^2 (Z_g^c)^2 \left| F_c \right|^2 \frac{N^3}{3} \tag{5-27}$$

By ignoring the second and third terms in (5.25) for large N, the noise figure expression for the distributed amplifier with real transmission lines is given by [6], [10]

$$F = 1 + \frac{1}{NZ_g^c}\frac{4\gamma}{\alpha}\frac{1}{G_m}\left(\frac{\sin\frac{\theta}{2}}{\frac{\theta}{2}}\right) + NZ_g^c\frac{\alpha\delta}{3}\frac{\omega^2 C_{gs}^2}{5G_m} \tag{5-28}$$

The second term in (5.27) is not included in (5.28) because this term after substitution in (5.25) results in a term which is $|c|^2$ times the second term in (5.28). Since the value of $|c|$ is small and less than 1, $|c|^2$ is even smaller than 1 and hence the term can be ignored as compared to the second term in (5.28).

Thus, there exists an optimum value of NZ_g^c that gives a minimum noise figure at a particular frequency and is given by [10]

$$(NZ_g^c)_{opt} = \frac{2}{\alpha}\sqrt{\frac{15\gamma}{\delta}}\left(\frac{\sin\frac{\theta}{2}}{\frac{\theta}{2}}\right)\frac{1}{\omega C_{gs}} \tag{5-29}$$

while this minimum noise figure expression is given by [11]

$$F_{\min} = 1 + 4\sqrt{\frac{\delta\gamma}{15}}\frac{\omega C_{gs}}{G_m}\left(\frac{\sin\frac{\theta}{2}}{\frac{\theta}{2}}\right) \tag{5-30}$$

5.3 Layout and Simulation Results

In this work we modeled a Pi-gate FET transistor suitable for low-noise applications [8, 10]. The schematic of the proposed transistor including parasitic elements is shown in Fig. 5.3; the end of each electrode is supposed to be open. This configuration can be specified by a 2×2 S matrix (with the source grounded at all points).

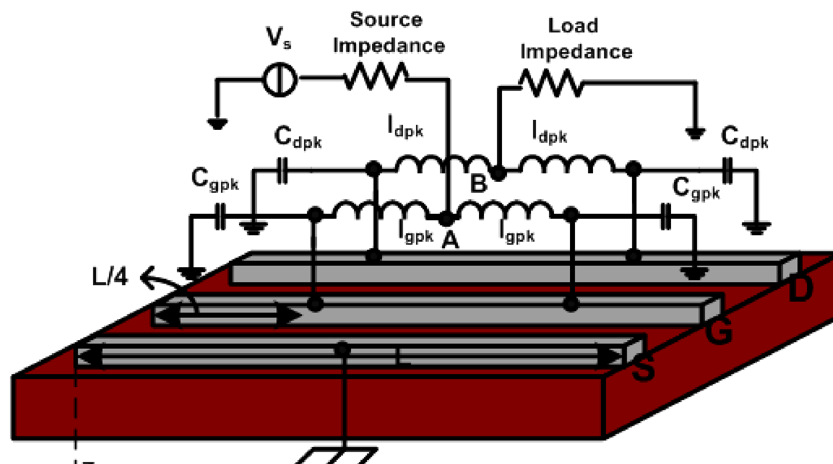


Fig.5.3. The schematic of a pi-gate FET including parasitic elements

The topology of the Gate and Drain lines as transmission lines for transmission line modeling with FDTD is shown in Fig. 5.4 (a). As we can see, coupling between lines should be considered to achieve more accurate results.

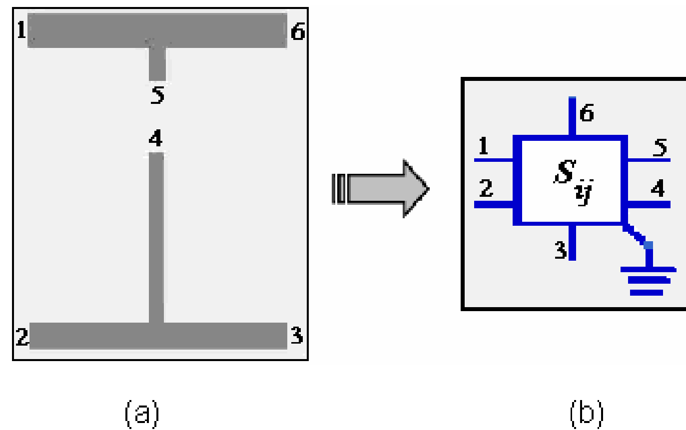


Fig.5.4. (a) Gate and Drain lines topology (b) Equivalent wave model

In this work, a three-stage distributed amplifier has been designed, simulated and optimized with the desired specifications

- 3-11 GHz frequency band
- Power-Gain =13 dB
- $|S_{11}| < -10\,dB, |S_{22}| < -10\,dB$
- $NF_{min} < 6$ dB

First, the lumped FET model and the quasi static approach for transmission lines are considered (see Fig.5.5). Then, we used the simulated transistor S-parameters of the transistor and the quasi static approach for transmission lines as shown in Fig .5.6. To accurately predict the amplifier performance, the transmission lines were simulated using a three-dimensional FDTD approach.

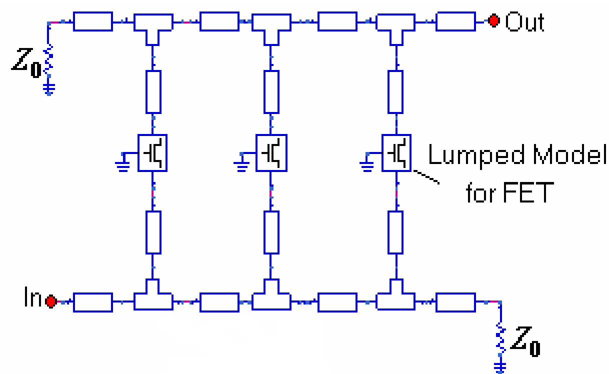


Fig.5.5. Schematic of distributed amplifier considering lumped model of FETs

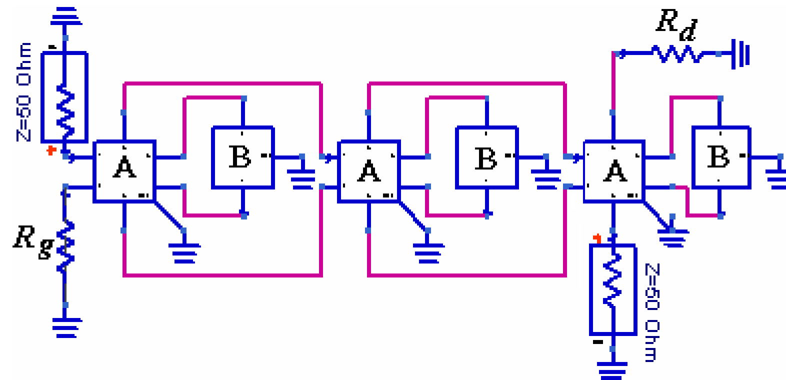


Fig.5.6. Schematic of distributed amplifiers, considering FDTD approach applied to Transmission Lines and FETs

5.4 The Measurement System

Fig. 5.7 shows the layout of the designed 3-stage distributed amplifier (Fig.5.8. We used The HP 8970S noise-figure meter system, the HP 8662A synthesized signal generator,

and the Agilent 8565EC spectrum analyzer as the main components of the measurement setup (Fig.5.9).

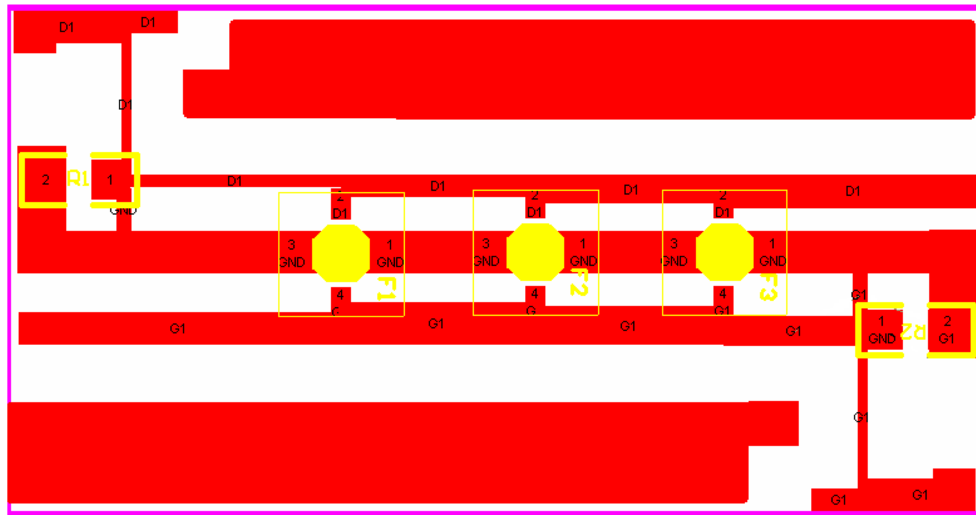


Fig.5.7 Layout of the 3-stage distributed amplifier

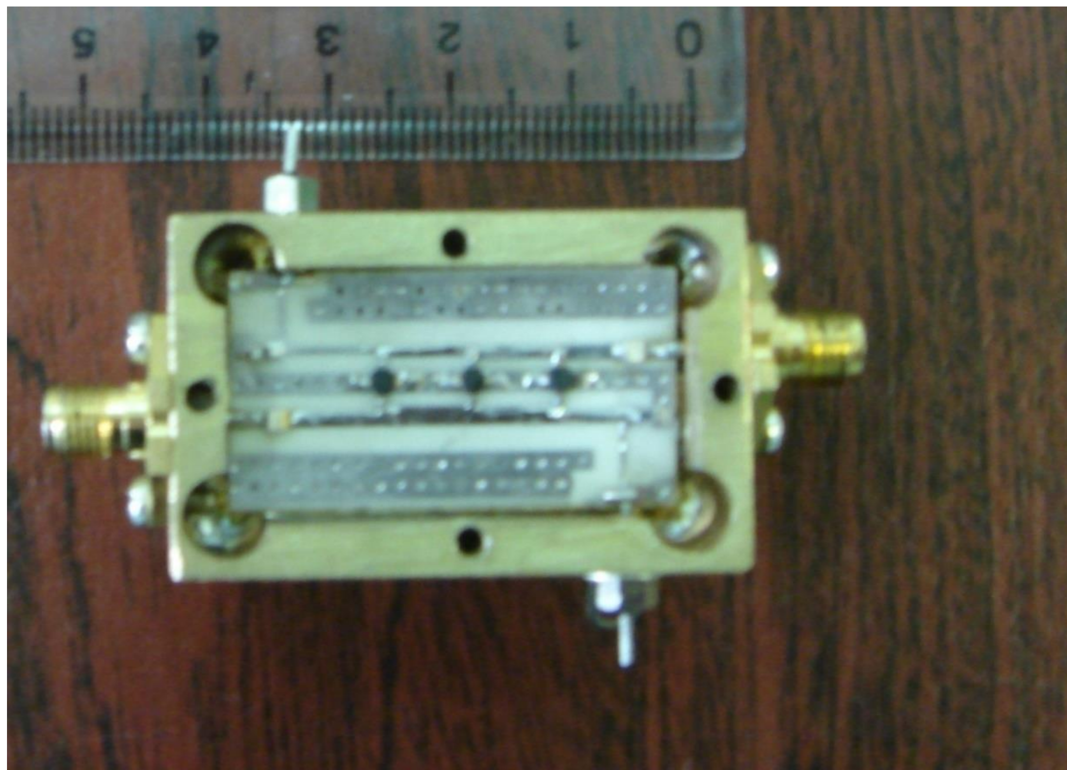


Fig.5.8.Fully assembled 3.1 to 10.6GHz distributed amplifier

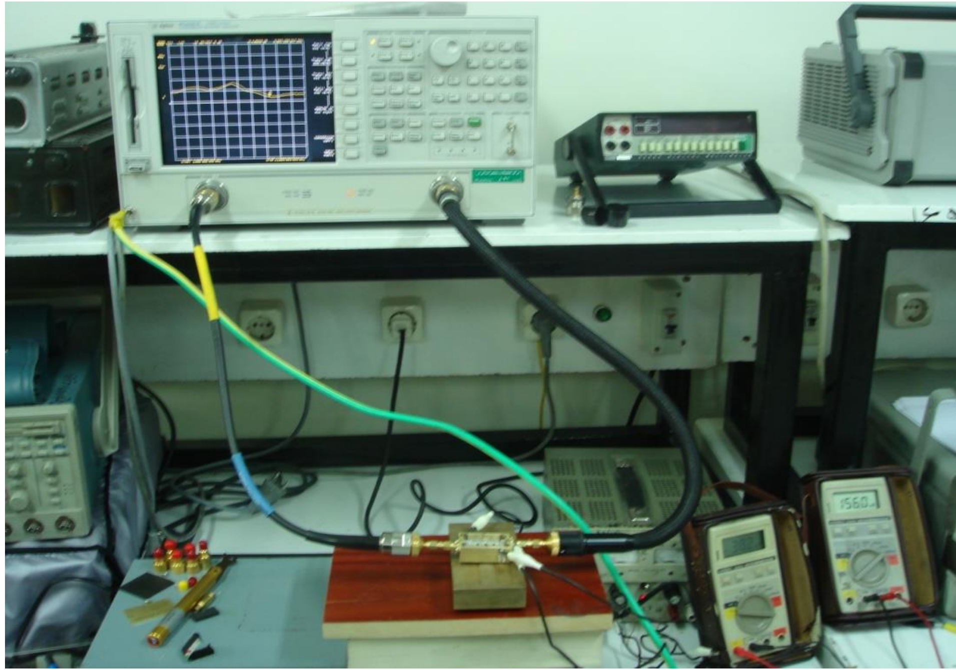


Fig.5.9 Lab set-ups for small-signal measurements of the distributed amplifier

5.5 Experimental Results

The drain line was biased at 1.2V whereas the gate line was biased at -0.6V. Note that the characteristic impedance of the loaded lines (assumed to be 50Ω under condition of perfect termination) is used in the calculations as the impedance that the drain current of each transistor would see.

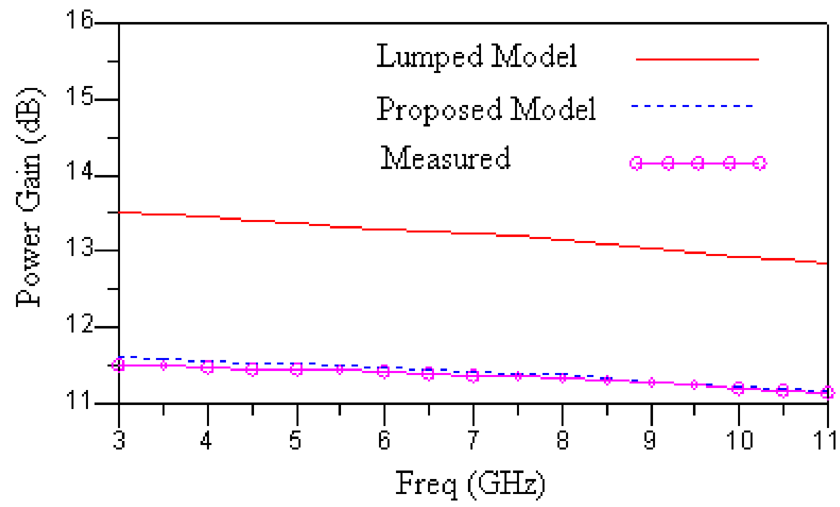


Fig.5.10 Power Gain comparison for measured, proposed model and lumped model

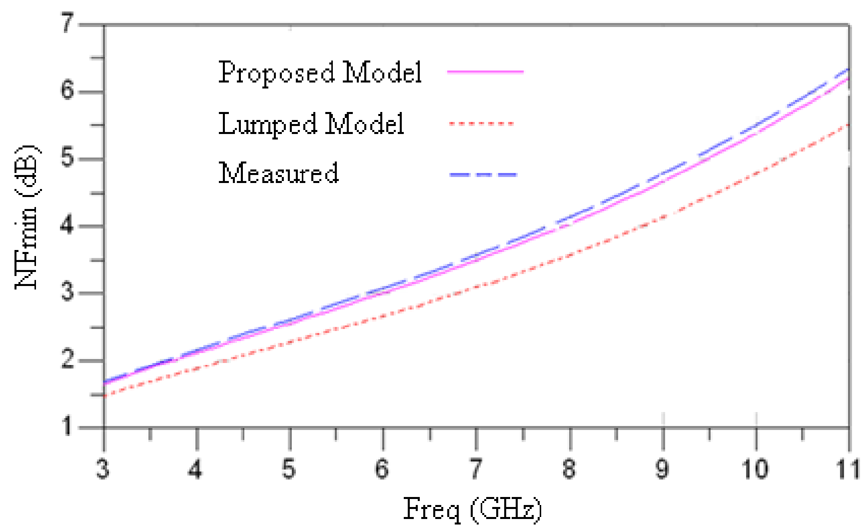
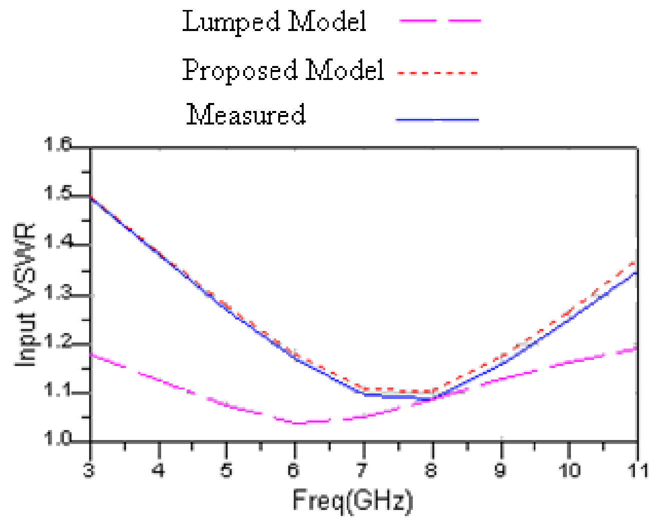


Fig.5.11. Minimum noise figure



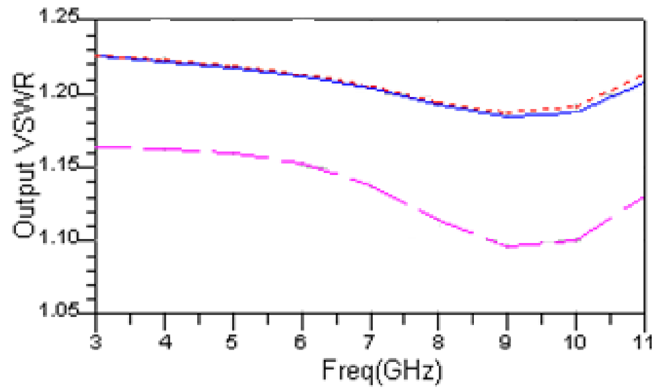


Fig.5.12 Input and output return loss comparison for measured, proposed model and lumped model

Table 5.1. Performance of the designed distributed amplifier

Parameter	Measurements results	Simulation results	Specification
Power Gain	13±0.5 dB	>13 dB	13 dB
Input Return Loss	<-10 dB	<-10 dB	<-10 dB
Output Return Loss	<-10 dB	<-10 dB	<-10 dB
Noise Figure	< 7 dB	< 6 dB	< 6 dB
Frequency Range	3.1GHz to 10.6 GHz	3GHz to 11 GHz	3GHz to 11 GHz

5.6. Power Amplifier Characteristics

For further demonstrate the efficiency of our approach, we implemented our nonlinear model into commercial software in order to design a fully integrated E-band power amplifier. The commercial use of the spectrum in the 71-76 GHz, 81-86 GHz, and 92-95 GHz bands becomes available for ultra high speed data communications as announced by the US Federal Communications Commission [11]-[12]. This decision was based on ever-increasing demands in millimeter-wave (mm-wave) frequency bands from both industrials and researchers. In fact, the 71-76 and 81-86 GHz bands (also known as "E-band") are permitted for ultra high capacity point-to-point communications. Therefore, the available 10 GHz of spectrum, which represents by far the most ever allocated at any one time, enables fiber-like gigabit per second (Gbps) and greater data rates that cannot be achieved at existing lower bandwidth-limited microwave frequency bands [13]-[16].

In our work, we designed and simulated a 74 GHz CMOS PA with two coscode stages along with an output common-source stage.

5.7. Power Amplifier Design

The schematic of the designed power amplifier is shown in Fig. 5.13 using the simulator Cadence [18], while the passives were designed in ASITIC (Analysis and Simulation of Inductors and Interconnect for Integrated Circuits) [19] using design rules for 90-nm RF-CMOS technology. This ensures that the inductance, resistance and capacitance of interconnect are adequately accounted for. Inductor 2-Ω models extracted from ASITIC simulations are used in the circuit schematics to capture the skin effect and substrate parasitic at high frequencies. The designed inductors are with outer diameter from 100 to 200 μm, metal strip width from 10 to 15 μm and space between neighboring segments from 1 to 2 μm, while all interconnects are MIM capacitors, which already exist in 90nm Cadence library. Fig. 5.14 shows a photograph of the implemented amplifier, which consists of two cascode stages (first stage with inductive degeneration) followed by a common-source (CS) output buffer operating in class A. The cascode topology was preferred to get higher gain and larger output impedance. The choice of a common-source configuration was considered to achieve

good efficiency [2], [20], [21]. Simulations were conducted with digital MOSFET models from the 90nm Cadence library.

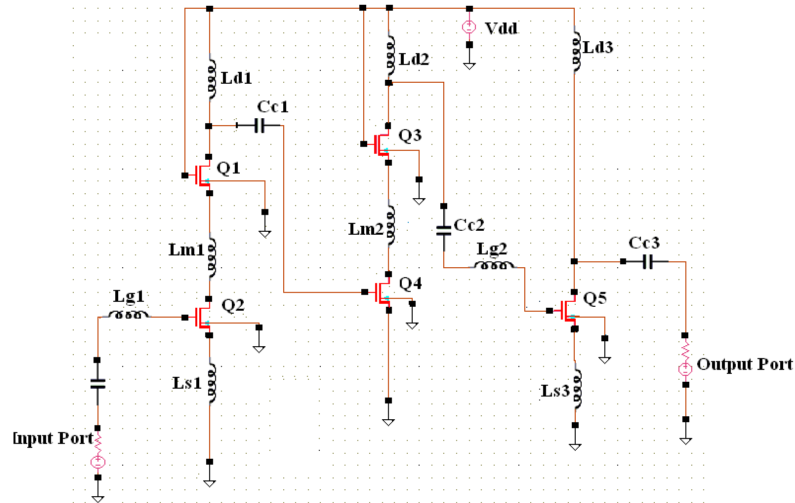


Fig.5.13.Three-stage amplifier schematic

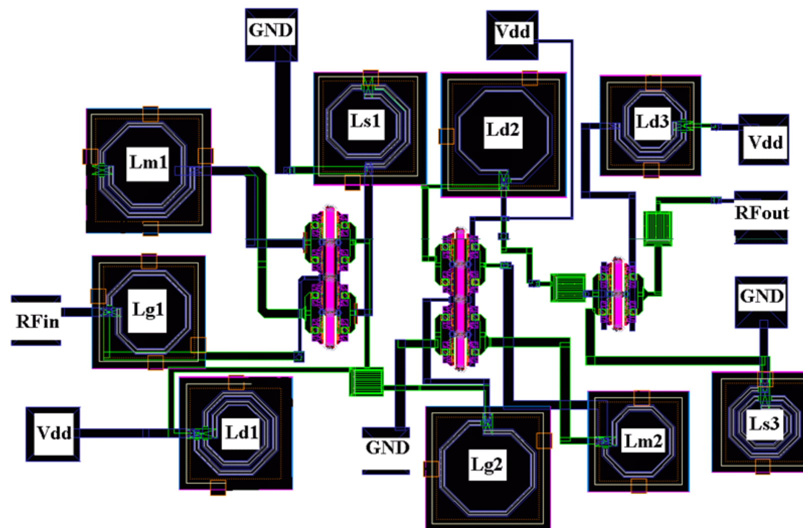


Fig.5.14. Layout photograph of the amplifier

For the first stage, as in low-noise amplifiers, we used simultaneous noise and input impedance matching approaches.

The input impedance Z_{in} of the amplifier

$$Z_{in} = \omega_T L_{s1} + j\left(\omega L_{s1} + \omega L_{g1} - \frac{\omega_T}{\omega g_{m2}}\right), \tag{5-31}$$

is now tuned to match the Z_o source impedance (usually 50Ω) using the two inductors L_{s1} and L_{g1} (same for the third stage with L_{s3} and L_{g2}) as in Fig. 5.14 [22]-[24]. Here ω_T and ω represent the angular frequencies corresponding to f_T and to the operating frequency f, respectively. The parameter g_{mi} represents the transconductance of transistor Q_i (i = 1 to 5).

By separating (5-31) into real and imaginary parts, one yields the required values of $L_{s1,3}$ and $L_{g1,2}$

$$L_{s1,3} = \frac{Z_0}{\omega_T} \tag{5-32}$$

$$L_{g1,2} = \frac{\omega_T}{\omega^2 g_{m1,5}} - L_{s1,3} \tag{5-33}$$

Finally, an inductive load is employed to maximize the amplifier gain and linearity. When the first stage is matched at its both input and output, the power gain is given by

$$|G| \cong \frac{1}{2}\left(\frac{\omega_T}{\omega}\right)^2 \frac{Z_P}{Z_o} \tag{5-34}$$

According to load line theory yielded in Fig. 5.15**,** the bias current density was set to 0.32 mA/µm to maximize linearity for second and third stages. Then, the design constraints relatively to the 1-dB compression point (P_{1dB}) will determine the bias conditions and thus, the transistor width

$$P_{1dB} = \frac{I_{dc} \times (V_{dd} - V_{ds,sat})}{2} \tag{5-35}$$

The output stage was sized for a saturated output power of 12 dBm with 1.5 $V_{peak\text{-}to\text{-}}$

$_{peak}$ output swing. Once the dc current I_{dc} is obtained using (5-35), the transistor size can be determined. In (5-35), V_{dd} is the dc voltage and $V_{ds,sat}$ the drain-to-source saturation voltage. The output network L_{d3}-C_{c3} is obtained such a way that could meet requirements for load pull theory. Note that based on the above technique and current density value for each stage, gate width for all transistors can be obtained: the transistor sizes are 32×1µm (Q1, Q2), 38×1µm (Q3, Q4) and 42×1µm (Q5).

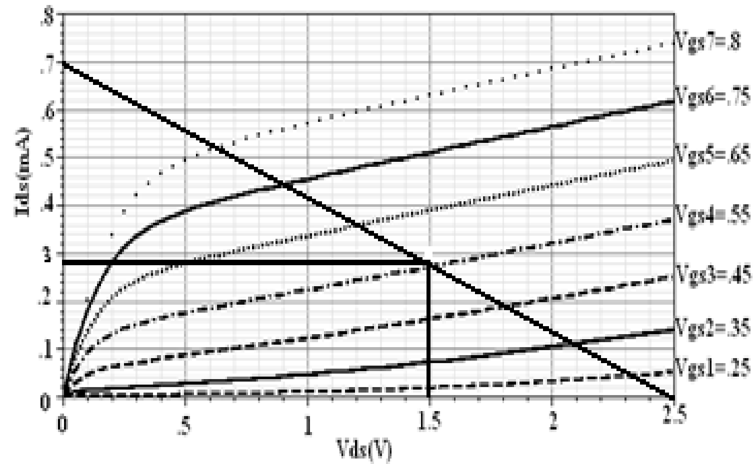


Fig.5.15. Optimal load line for common source configuration

5.7 Simulation Results

At the operating frequency of 74 GHz, the small-signal gain is equal to 17 dB with a 3-dB bandwidth exceeding 5 GHz (i.e., 71-76 GHz) as shown in Fig.5.16. Also, broadband matching is achieved ($|S_{22}|_{dB}$, $|S_{11}|_{dB} < -17$dB) in the 68-80 GHz range. Furthermore, with a 1.5 V dc power supply, the power amplifier presents a noise figure less than 5.2 dB over the 68-80 GHz range (Fig.5.17). Fig.5.18 shows the large signal performance of the PA with 1-dB output compression point of 7.2 dBm and a saturated output power of 11.5 dBm at 74 GHz. As expected, maximum gain and linearity occur when the final stage is biased at 0.28mA/µm. A maximum power added efficiency of 20% was also achieved (Fig.5.19). The obtained simulated parameters of the power amplifier are summarized in Table 5.2 and

compared, in Table 5.3, to those of previously reported power amplifiers operating near 74 GHz.

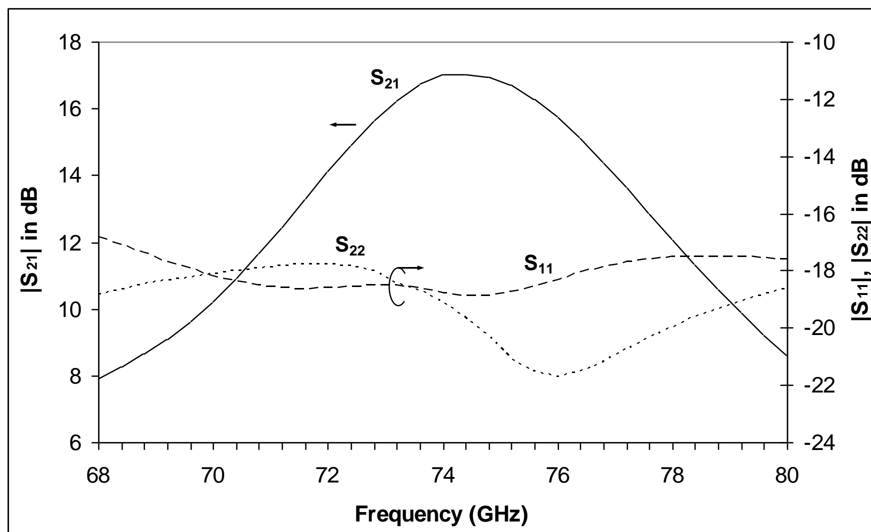


Fig.5.16.Simulated S-parameters

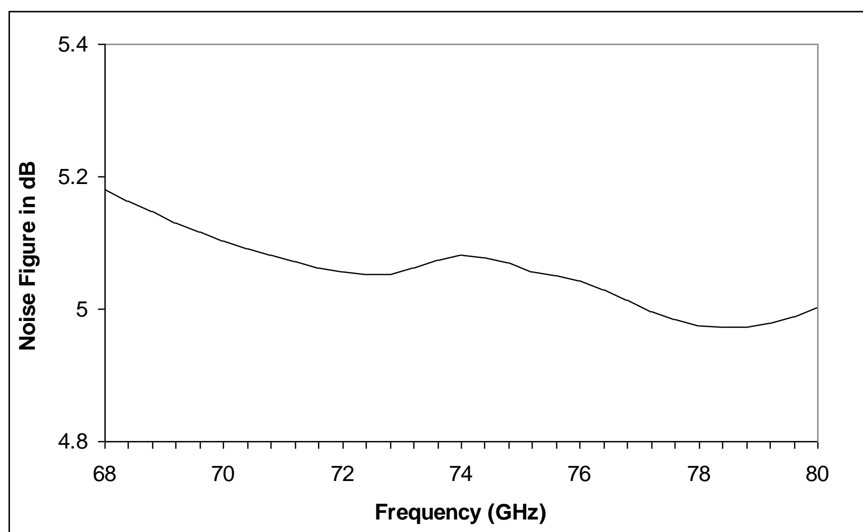


Fig.5.17.Noise figure of the designed amplifier

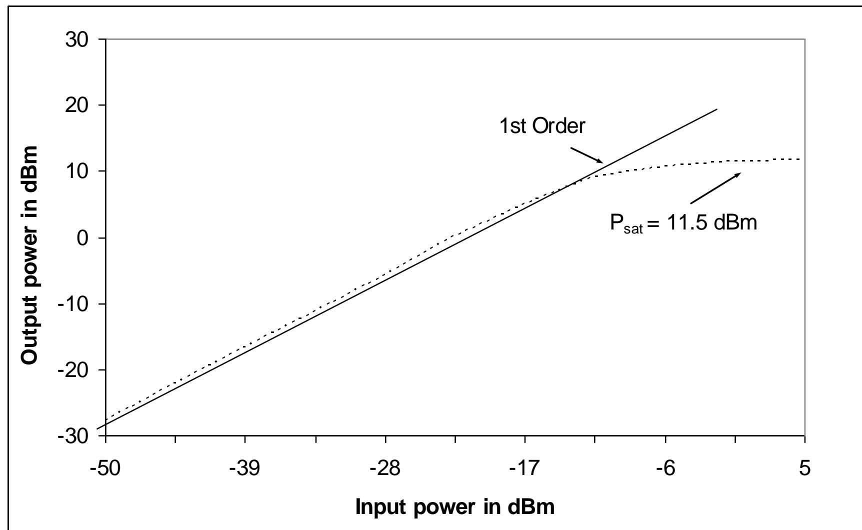


Fig. 5.18 Simulated P_{1dB} at 74 GHz

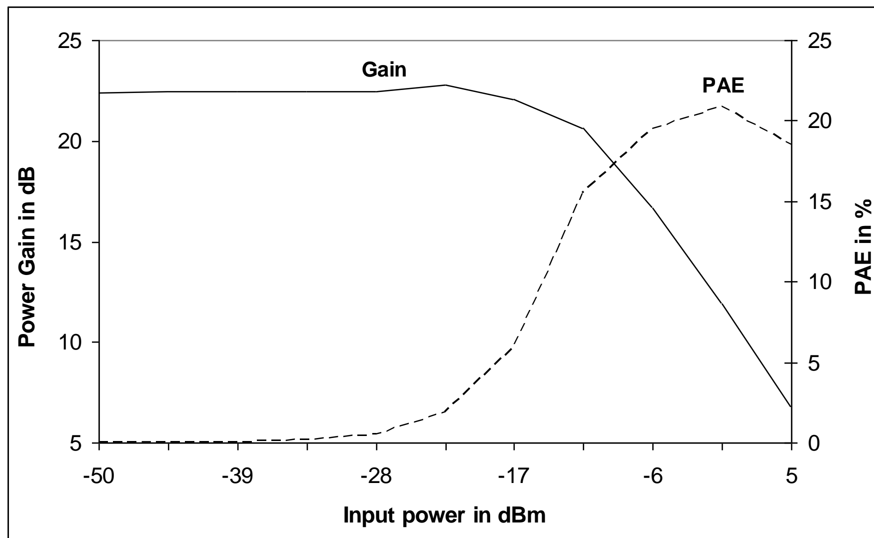


Fig.5.19.Simulated gain and PAE at 74 GHz

Table 5.2. Power Amplifier Performance

Frequency Range	71-76 GHz
Saturated Output Power (@Vcc=1.5 V, Ids = 33mA)	11.5 dBm
PAE	20 %
Gain @ 74GHz	17.02 dB
Output-referred 1dB Compression Pt	9 dBm
Supply Range	1.2 to 1.5 V
Noise figure	5 dB
3-dB Bandwidth	5 GHz

Table.5.3. Millimeter-Wave Power Amplifier Performance: Comparative Table.

Freq	Device	P_{1dB},out (dBm)	PAE_{max} (%)	Gain (dB)	P_{sat} (dBm)
** 60 GHz **[2]**	90nm CMOS	6.4	7.4	5.2	9.3
* 77GHz **[3]**	.12µm SiGe	11.6	6.5	6.1	13.5
** 61 GHz **[4]**	.12µm SiGe	-	4.3	10.8	16.2
* 85GHz **[6]**	.12µm SiGe	-	4.5	8	21
74 GHz (this work)	**90nm CMOS**	**7.2**	**20**	**17**	**11.5**

** Simulation   * Measurements

5.8 Conclusion

The linear and nonlinear proposed model is particularly suited to millimeter-wave circuits. Since it is a CAD-oriented model, it can be easily used in commercial simulators. In order to show the accuracy of the model, the linear proposed model was first implemented in the commercial circuit simulator Agilent-ADS to design a low noise amplifier in UWB band. Then, it was fabricated and its performance successfully compared to measured data.

Furthermore, to demonstrate the capability of the nonlinear model to characterize and optimize microwave circuits in millimeter-wave frequencies, a 74-GHz class-A power amplifier with 20% maximum PAE was implemented in the 90-nm CMOS technology using

the commercial circuit simulator Cadence. The designed millimeter-wave power amplifier shows high performance compared to those already published in such frequency band.

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Chapter 6 Conclusion

6.1 Summary

In the context of this thesis, a new approach for analyzing microwave field effect transistors has been presented. This new method can accurately consider the effect of wave propagation along the device electrodes. The derived equation was solved using the FDTD technique. The results show that by increasing the frequency up to the mm-wave range, a difference appears between the proposed model and the lumped model. This is due to the wave propagation and phase cancellation effects. We also highlighted the impedance skin effect of the FET electrode conductors in a transistor behavior. Such effect is often neglected in the analysis of FETs, leading to non accurate models in high frequencies

Also, the nonlinear active multiconductor transmission line equations have been introduced using distributed proposed model based on a three-line structure. This modeling approach was applied to an FET and the results, for example the voltage and current waveforms were compared with those of the lumped model. At low frequencies, the results of the proposed model have a good agreement with those of the lumped model. However, by increasing the frequency, a fractional difference exists between the two models. But in high-frequency applications, the use of the proposed model is recommended

A new modeling approach for noise analysis of high frequency transistors was presented. This method can accurately take into account the effect of wave propagation along the device electrodes. The promising model can be applied to solve issues related to simultaneous signal and noise analysis, as well as in modeling traveling wave FETs in which the gate width is much higher than that of a usual FET.

Finally, Three-stage distributed power amplifier based on our proposed FET model was designed and analyzed in time domain. The measured circuit performance was successfully compared to the simulated values and the desired. The capability and the usefulness of our distributed model in terms of characterizing and optimizing microwave circuits are then demonstrated.

6.2 Future Work

Several directions can be highlighted based on the present work:

1. The large-signal model can be applied to other technologies especially to the promising GaN transistors, which usually do not have specific large signal models available in the market.
2. The small- and large-signal modeling approaches can be also applied to other structures such as to Dual-gate transistors, which have important applications in mixers. Developing temperature dependent large-signal models for dual-gate MESFETs can be also quite attractive in power applications.
3. Noise analysis of FET in this thesis has been investigated based on small-signal excitations. However, applications in which nonlinear behaviors are present can be targeted in terms of noise performance.
4. In the present work, all linear and nonlinear equations were solved using the well-known FDTD time-domain method. However, we can consider other methods for full-wave modeling of high-frequency semiconductor devices. The model could contain the semiconductor equations in conjunction with the Maxwell's equations, which describe the complete behavior of high-frequency active devices. Using other approaches like ADI approach could lead to a significant reduction of the full-wave simulation time.
5. The three active coupled transmission lines we used in this thesis have been assumed to be uniform, but an efficient numerical method for transient analysis of lossy non-uniform transmission lines cloud be investigated.