THRESHOLD LOGIC GATE SYNTHESIS
USING OPERATIONAL AMPLIFIERS

by

John W. Gaffney

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ABSTRACT

The theory of threshold logic has been well developed and the applications exist, but the synthesis of threshold logic gates still needs improvement. The problems of realizing these devices are numerous but today's advancing technology is presenting solutions.

One example of this technology is the integrated circuit and, more specifically, the operational amplifier. It is proposed in this thesis to investigate the feasibility of using operational amplifiers to realize threshold logic gates. It is required that the realization be dependable, have good sensitivity, and be easily manufacturable at a reasonable cost.

The findings of this work bear out the proposal. Operational amplifiers, used in pairs to form a summer and comparator, will realize threshold gates. Modern technology permits the ready fabrication in the popular integrated form of packaging.

ACKNOWLEDGEMENTS

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CHAPTER I : INTRODUCTION

1. THE STATE OF THE ART

Before any statement of purpose is made in this presentation, it is necessary to present a brief resume of the development of threshold logic, both in theory and in practise. Most of this work has been carried out just in the last decade or so and although the theory has advanced rapidly, circuit design and applications have some catching-up to do.

A threshold gate is an electronic building block for circuits to realize logic (or switching) functions such as appear in the control, register, and processing portions of an electronic digital computer. Inputs and outputs take on values we call "0" and "1". At present, "Boolean"[*] gates (AND, OR, NOT, and thier complements)[‡] are used almost exclusively, but these gates perform an identification function only. An AND gate, for example, determines whether or not a certain pattern of inputs is present. Boolean switching theory is well developed and provides a good basis for logic design using Boolean gates.

In the late 1950's several variations of a new type of circuit were developed. This type of circuit performs the more sophisticated function of determining the "majority" signal among its inputs. For example, a 5-input gate has an output of 1 only when three or more (majority) of its inputs are 1's. The obvious generalization of such a gate is the threshold gate, where, in effect, inputs are allowed different (possibly even negative) "weights" in the voting process; instead of a simple majority being determined, an arbitrary "Threshold" is specified for the gate. The output then indicates whether or not the weighted sum of inputs attains the given threshold.

[*‡] The term "Boolean gate" is used to refer to the conventional Boolean algebra type gates; e.g., AND, OR, NAND, NOR, etc.

Since its decision process is much more sophisticated than that of the Boolean gate, the threshold gate is logically more powerful, and fewer are needed to realize a given switching function.

Secondly, threshold gates can be modified conveniently (by variations of the weights), making them particularly suitable for adjustable networks. In these applications there may be tens or even hundreds of inputs to each gate, and circuit errors can be tolerated because of the intrinsically statistical environment. However, greater reliability is often required, and so more accurate methods of circuit realization must be found. This point will be expanded further in this thesis.

2. STATEMENT OF PURPOSE

Threshold gate circuit design has been difficult owing to such constraints as tolerances, cost, simplicity, and ease of use in logic design. Several methods of realization have been devised using active and inactive elements alike. In this age of micro-miniaturization when the integrated circuit is becoming so prominent, it seems likely that this building block should hold some promise for the solution of the problem of threshold gate realization. Some designs have already been produced, these being particular circuits designed solely as threshold gates. It will be the purpose of this thesis to explore the possibility of using an already generally-known device, namely the operational amplifier, to realize threshold gate circuits. It is hoped that such a design will be comparable and even superior to conventional gates for tolerances, noise immunity, simplicity, and cost of production and interconnection.

To realize the basic notion of a threshold gate, i.e., summation and comparison, requires the construction of a two-part circuit, namely a summer and a comparator. The weighting operation does not require any active elements and so is not considered as a separate part.

Summers and comparators may be built using such standard circuit elements as resistors, diodes and transistors. Problems arise however in the form of limited fan-in and fan-out, poor noise immunity, poor sensitivity. These may be dealt with individually in individually-designed circuits but it is difficult to overcome all of them at one time. This thesis proposes the operational amplifier as a solution to these multiple problems.

As is known from the use of operational amplifiers in analog computers, they are ideal for realizing a current or voltage type summer. Due to their extremely high input resistance, they draw very little (and ideally zero) input current. Therefore, there is practically no restraint on the fan-in to these devices. Fan-out capabilities will vary depending on the particular amplifier in use as will other characteristics such as output level, input voltage offset and bias current, common mode parameters, etc. However, it is not too difficult to choose a suitable amplifier from the many packages available.

CHAPTER II : THRESHOLD LOGIC

1. PHILOSOPHY

During the past few years there have been many active research programs concerned with threshold logic. Properties of threshold functions have been determined and realization procedures have been developed.

The threshold gate as a basic logic element has, in principle, powerful logic capabilities. It is now well known that an arbitrary function can be realized by a network of such components and that there are many examples where the number of gates required is considerably less than are needed when conventional gates are used. In contrast, however, there are functions where there are no savings.

With regard to actual implementations, a factor of particular significance is that threshold gates are more sensitive than conventional gates to component and signal fluctuations. There are inherent sensitivities independent of the particular implementing circuit configuration. In fact, some of the factors which give the gate its greater logic capability are ones that increase its sensitivity. The characteristics of threshold gates that can actually be implemented, therefore, depend upon the amount of signal and component fluctuations that can be tolerated. These in turn determine the component savings that are obtained in the realization of a particular function.

The intent, then, of threshold logic is to provide a simpler realization procedure for arbitrary logic functions and at the same time maintain or improve the accuracy and dependability beyond that of the conventional gates.

2. THEORY

This discussion of threshold logic theory is divided into four parts: (A) a basic system of properties possessed by all threshold functions, (B) test synthesis; i.e., the determination of whether or not a given switching function is a threshold function, and if it is, what weights and threshold realize it, (C) synthesis of networks of interconnected gates to calculate specified switching functions, and (D) classification and enumeration of threshold functions, with statistics and estimates of various factors such as the number of threshold functions, the size of the weights, and the number of threshold gates likely to be needed in a network. It should be noted that several variations of this basic threshold logic are being developed, notable non-linear threshold logic (Ataka)[5], a 3-valued threshold logic (Varshavsky-Ovsievich)[29], a multiple -threshold threshold logic (Haring-Diephus)[19], and a theory of partially separable functions.

A. Properties of Threshold Functions

There are many simple but important properties of threshold functions that follow directly from the definitions; these have been discussed in several earlier (circa 1960) papers and books on threshold logic functions. Some of the principal properties are:

(a) 1-realizability: the capability of a Boolean function to be realized by a single threshold logic element.

(b) Positivity: a switching function, F, is positive in a variable x_i iff F has an irredundant normal form in which no term has $\bar{x}_i$ as a factor. F is negative in x_i if no term has x_i as a factor.

(c) Unateness: a switching function, F, is unate in x_i iff F is either positive or negative in x_i. F of n variables is unate iff it is unate in each of its variables.

(d) Comparability: two functions, F_1, F_2 are comparable iff either $F_1 \subset F_2$ or $F_1 \supset F_2$.

(e) Monotonicity: a switching function, F, of n variables is 1-monotonic iff the reduced function of F expanded along any one variable x_i, i.e., F_{x_i} and $F_{\bar{x}_i}$ are comparable.

F is k-monotonic iff the reduced functions expanded along any i variables, $1 \leq i \leq k$, are comparable. Completely monotonic = n-monotonic.

There are other properties but these are the more important ones and are sufficient for the purposes of this brief survey. More detailed discussions can be found in Gabelman,[15] Lewis and Coates,[22] Sheng[28] and others.

E.F. Moore has shown that the monotonicity properties do not characterize threshold functions, and for this reason generalizations to stronger conditions have been and are still being explored. The adequacy of monotonicity for limited value of n (the number of arguments) has been determined as $n \leq 8$, and Gabelman[15] has shown the inadequacy for n = 9.

Chow[7] has defined a set of n+1 easily calculated numerical parameters which, among other uses, provide a theoretical characterization of threshold functions. These "Chow" parameters provide a fertile area for further work on basic properties of threshold functions.

B. Test Synthesis

The problem of identifying and realizing threshold functions (finding weights and threshold when they exist) has unfortunately produced a large number of varied papers. For small n, no more than 6, say, the problem is trivial — most functions are not threshold functions and can be so recognized immediately, especially in any reasonable geometric representation, by the i-monotonicity test. For those near-threshold functions which pass this test, a calculation of Chow parameters and a table-look-up in tables that exist for n = 7 immediately provide the "best" realization, if one exists, or an indication that it does not.

For partially specified functions, or for large n, there is no practical method known other than the solution of a system of linear inequalities generated by the definition of a threshold function. This system must first be reduced to reasonable size by elimination of redundant inequalities, which amounts to determining the signs and relative magnitudes of the weights. Then it can be solved in a variety of fashions -- by linear programming or game theory, by algebraic determination of all solutions, or by various specialized iterative methods. The dual-simplex method of Muroga-Toda-Takasu[24] is easily carried out by hand for n up to 12 and higher, is easily programmed for a computer, and gives (by definition) the best possible realization.

Other fairly limited methods of identification and realization have been proposed, but the subject has been well covered and further work in test synthesis would seem to be unnecessary.

C. Networks

Methods to synthesize networks of threshold gates divide into four classes: (a) synthesis with majority gates of three or five inputs, (b) synthesis of symmetric functions, (c) general combinational synthesis, and (d) sequential machine synthesis.

When the basic gate is constrained to be a three-input majority gate, it is easily possible to realize arbitrary functions for small n (up to 5 or 6) by using geometric representations. For larger n, truth table representations can be used in computer programs to produce heuristically good networks. But there is much theoretical interest in using an algebraic approach, analogous to the Boolean algebra used for Boolean gates. This theory has been developed in a variety of papers which propose rules for manipulating the algebraic expressions, often suggesting a particular form that always gives realizations, but not necessarily the best ones.

Methods of synthesis of symmetric functions have been developed to the point where the theoretical problem is much better solved then the technological problem of increasing the number of gate inputs, upon which the theory depends.

Methods for realizing arbitrary functions are a little more difficult and consequently have developed more slowly. Several algorithms and many different approaches have been suggested but there appears to be no "blanket" solution to the problem. Sequential machine realization has been studied only generally and may hold more promising possibilities. The use of computers to combine man's intuition with the machines clerical abilities is likely to prove the best approach to logic design using threshold gates.

D. Classification, Enumeration and Bounds

There are several proposed methods of classification and enumeration of threshold functions, too numerous and complex to go into here. Another point of much contention among authors on the subject is the value of the upper bound, the number of threshold gates required to realize an arbitrary function. All the results so far produced are purely academic, since they assume gates with an unlimited number of inputs.

In summary, the theory is well developed, but important new ideas are to be expected in the difficult area of network synthesis, and there will probably be continuing progress in the unification and completion of the basic theory of the nature of threshold functions.

3. CIRCUIT DESIGN

Threshold gate circuits can be broadly divided into two classes — (a) those that sum directly the input signal representations, and (b) those that do not. In either case, there is eventually a summation, and two methods have been widely used — magnetic flux summation and resistor current or voltage summation.

The threshold gate responsible for most of the earliest interest in threshold logic was simple and elegant, consisting of several input windings on a ferrite core and an output winding. Signals could be represented by the direction of a unit pulse of current in each input; algebraic summation of fluxes takes place in the core, except that the flux saturates in one direction or the other at the equivalent of one unit pulse of current in the output winding. Magnitude and sign of input weighting were determined by the number of turns and the direction of each input winding. There were many variations of this basic theme; elaborations were necessary for speed, tolerance and other engineering reasons. A typical magnetic threshold gate system operated in a multi-phase system — "waves" of power supply activation washed through the system to impress a directionality on otherwise bilateral signal propagation. Furthermore, it was typically necessary to add a transistor or other such active device to provide (a) gain, and/or (b) a sharper threshold discrimination, and/or (c) better standardization and driving capability in the output signal. Several computers have been built using such magnetic threshold gates, e.g., Ferranti's ORION.

Once an active element was introduced, it was natural to use a simple Kirchoff resistor summation of the inputs, with the active device used to restore proper levels. Important such devices used were the phase-locked-oscillator, and the tunnel-diode balanced pair. These examples represented phased ac and phased dc power supplies respectively. Although some success was achieved, tolerance, speed, and power supply distribution problems remained severe.

Resistor summation and transistor discrimination/ restandardization represented the most important threshold gate circuit for several years (Chao[6], Coates-Lewis[9], Akers-Rutter[2]). (Earlier, vacuum tube threshold gates were used in some computers.) These circuits had two related difficulties: (a) close tolerances were required on the summing resistors and the threshold supply, and (b) noise appearing on the different input signals was combined additively at the critical summation point. These effects combined to limit the gates to reasonable fan-in (i.e., number of equivalent majority-gate inputs) with poor noise immunity, or reasonable noise immunity with poor fan-in. And this is typical with 1% uniformity resistors.

Integrated circuit technology has permitted a solution to this dual problem. First , the relative uniformity of a cluster of resistors manufactured at the same time is very high -- 2% uniformity is standard and better uniformity is possible by increasing geometric dimensions. Second, it is now possible to provide a separate current switch for each input, the outputs of which are used in the summation process. This isolates the decision process from the possibly noisy inputs -- all that is required of the inputs is that they lie at least 100 mV from the reference level that separates 1's from 0's. Integrated gates of this sort are the first threshold gates that, compared with contemporary Boolean gates, are (a) competitive in cost (approximately 25% more costly in exactly the same fabrication technology), (b) compatible in all voltage levels and so usable as subsystems in conventional systems, (c) compatible in speed (initial experimental gates operate with 12 nanoseconds state delays, fully loaded, as compared with 8 nanoseconds for comparable OR/NOR gates), and (d) have better noise immunity. The gates actually fabricated (Amodei-Hampel-Mayhew-Winder[4]) have five inputs weighted respectively 2,2,1,1, and 1, withthreshold 4, and provide both true and complemented outputs. This gate was combined with a 3-input majority gate in a 14-pin package to provide a versatile building block. Higher fan-ins are possible, but then only one gate per package is feasible with this technology.

Threshold gate circuits are also being developed for the new large-scale integration (LSI) technologies. These circuits compared with the high-speed, high-power threshold gates discussed above are simpler, somewhat slower, and on a local level often have much less noise immunity. They are designed to behave virtually independently of temperature variations and those power supply drops that show up symmetrically on the two power-supply lines. These particular circuits allow incorporation of very simple OR functions at inputs and outputs; they are most tolerant to component variations when their thresholds are highest. These properties seem likely to generate a new generation of logic design problems and corresponding switching theory.

In summary, threshold gate circuit technology has taken a long step forward and is roughly on a par with the theory of threshold gates. In both areas, threshold gates are now competitive with Boolean gates. It is now essential to consider the application of each to the real problems of logic design in computer-like systems.

4. LOGIC DESIGN

Practical logic design with threshold gates is found in the phased power supply system (Muroga-Takashima)[25] and in Ferranti's ORION data-processing computer. However, detailed information on these efforts is not available and, moreover, the requirement for multiple phases places special constraints on the logic design that do not apply in the integrated circuit technology. The known logic designs, are, for the most part, realizations of computer subsystems, such as adders, parity checkers, registers and counters.

A complete full adder accepting three inputs and delivering a sum and a carry as outputs, can be realized using two threshold gates (Amodei-Hampel-Mayhew-Winder[4]). This realization typifies the advantages of using threshold gates: (a) one-third as many gates are needed as in the most sophisticated Boolean-gate adder (in fact, one of the 14-pin packages mentioned earlier constitutes one entire adder stage), (b) interconnection is simpler, and (c) only the true input signal representations are needed (saving a factor of two in the number of input connections to the adder).

Many other adder designs are known. For examples, only three 3-input majority gates are required per stage (Curry[12]-Harel[18]-Cohn-Lindaman[11]). Binary/decimal adder/subtractors are easily realized (Fischler-Poe[13]). Carry look-ahead is very natural in threshold logic (Coates-Lewis[10]); a 64-bit adder can be built that uses 189 of the (2,2,1,1,1) gates mentioned earlier and operates in just six stage delays (Winder).

A fast, two-level, approximately n/2-gate n-bit parity checker is discussed by Minnick[23]. Kautz[20] gives a slower, less expensive design using $\log_2 n$ of gates (this network also gives a complete binary count of the number of one's present among the inputs). Since both these designs require tolerances equivalent to a (2n+1)-input majority gate, probably the best solution is a $\log_2 n$-level tree network of approximately n 2-gate, 3-input full adders of the sort described above.

Sequential networks of threshold gates offer very interesting possibilities. In Gustafson-Haring-Susskind-Wills-Sandford[16], the realization of counters is investigated, assuming a collection of identical delay lines as in the standard synchronous sequential machine model, but then doing the next-stage logic with one threshold gate per output. Of more practical interest are the ring counters developed (for $m \geq 3$) in Price[26], which require one majority gate per full count and no capacitive interconnection. Counters of this type are very simple (either all or all but one of the gates can be 5-input majority gates) and can operate at very high speeds — one lightly-loaded stage delay per transition of the clocking pulse. Binary counters can be constructed using three gates per stage.

The Boolean idea of realizing a flip-flop or register by cross-connected NOR gates becomes, in threshold logic, a pair of minority gates. However, the same effect can be realized with a single threshold gate. Furthermore, the need for an isolating AND gate between the sampled input signal and register stage is eliminated; control signals ("reset" and "gate in data") can be applied directly to the gate (Winder).

Many other logic designs have been published; among them are comparators, a decoding system using 3-input majority gates, pattern recognition systems, a multi-purpose accumulator and a multipurpose logic array, methods of realizing large fan-in majority gates using low fan-in gates, and methods of improving reliability by suitable redundancy, an application for which threshold gates are especially appropriate.

Two important principles should be mentioned here. First, because of pin limitations, an asymmetric basic building block (such as the 2,2,1,1,1 gate) is preferable to a majority gate; the full generality of the 7-input majority gate is rarely needed, and the saving of two pins is quite important. As an example of this, consider the full adder stage and the register stage with an AND gate for output isolation, each of which can be realized using one package of the type described earlier. Second, the functions of storage and logic can be combined in one threshold gate by using suitable feedback of the output; this, of course, is not true with a Boolean gate. The simplest example is the register stage, but much more sophisticated applications are possible. In particular, realization of control logic by chains (or trees) of one-gate flip-flops (an asynchronous digital version of delay lines) is an attractive scheme for reasons of economy, simplicity

In Coates-Lewis (DONUT)[9] a careful comparison was made in equivalent designs of a complete small computer using threshold gates and NOR gates. A reduction in gate count from 2:1 to 4:1 was reported depending on the fan-in of the threshold gate assumed. Similarly, on subsystems such as those discussed above, using the integrated threshold gate has produced an average reduction of from 2:1 to 3:1. Equally significant -- since the cost of printed circuit plug-ins, platters and racks can exceed the cost of the integrated circuit packages themselves -- an average reduction of about 2:1 in the number of interconnections can be obtained. These statistics, taken together with the 25% per package cost increase for threshold gates, result in a total main-frame cost reduction of about 50%.

CHAPTER III : OPERATIONAL AMPLIFIERS

1. DEVELOPMENT OF THE OPERATIONAL AMPLIFIER

The first operational amplifiers were manufactured using transistors. This solid-state device was an improvement over vacuum-tube devices providing such notable advantages as small size, low power consumption, reliability and ruggedness. Previous to this break-through, operational amplifiers were relegated almost entirely to the laboratory being too costly and bulky for feasible commercial application. Now they are being used in a wide variety of applications in signal processing and control with foreseeable uses in other fields such as threshold logic.

There are still problems with the transistor-type operational amplifier arising from the temperature-dependency of some transistor characteristics. Solutions have been found in a number of ways. Carefully matched input transistors employed in a differential input configuration (Figure 1) will reduce the temperature sensitivity as well as providing greater versatility since there are now two available inputs. This method does not completely eliminate the temperature problem and so another configuration was developed — the chopper stabilized amplifier. This configuration provides two amplifying channels: one

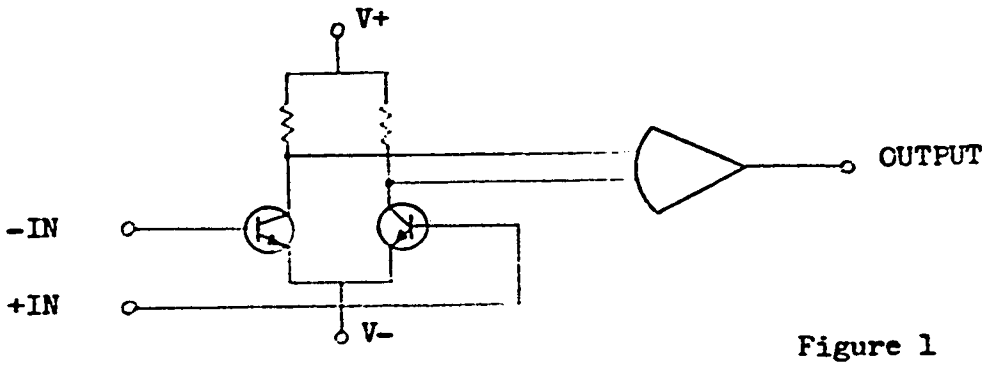


Figure 1

for AC and one for DC. The latter effectively provides amplification in the order of 1000 while minimizing temperature sensitivity and virtually eliminating DC offsets or drift. Field effect transistors (FET'S) have also been used in place of the bipolar ones of Figure 1 to increase input impedance.

Finally, monolithic integrated circuits have produced devices which operate about on a par with discrete devices of four or five years ago.

A comparison of the afore-mentioned devices shows that bipolar-type amplifiers are now comparable to the chopper-stabilized type of three years ago but that the present chopper-stabilized type has improved tenfold in that period. FET's are closing the price-performance gap but monolithic amplifiers have a long way to go to match the discrete component and hybrid devices.

2. APPLICATIONS

(a) Monolithic IC amplifiers with bipolar transistor inputs are generally most useful in low-impedance circuits such as low-gain amplifiers.

(b) FET input stages make the amplifier preferable in high impedance and memory circuits.

(c) Chopper-stabilized amplifiers are best for low levels and where long-term stability is required.

3. FUNDAMENTAL CIRCUIT THEORY

Although a powerful and versatile circuit element, the operational amplifier's operation can be simply explained by the consideration of a few simple restraints. The operational amplifier shown in Figure 1 can be more simply modeled as in Figure 2.

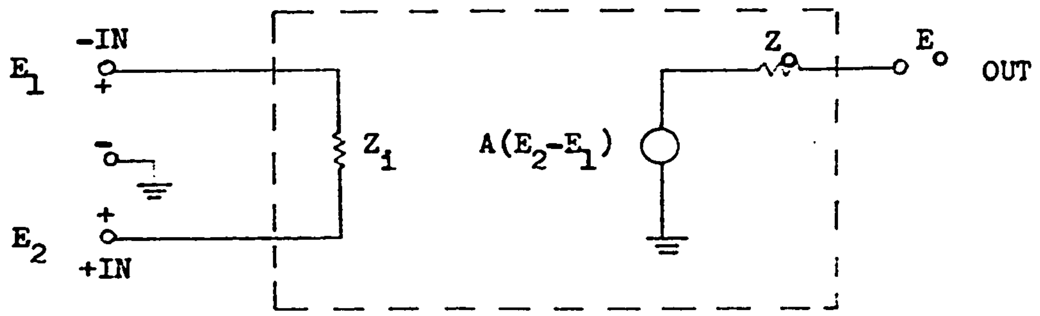


Figure 2

There are two inputs. The inverting input (-IN) provides negative amplification, -A, while the non-inverting input (+IN) provides a positive amplification, A, where A is the amplifier gain and is very large. Certain assumptions are made to produce an idealized model which is easier to handle. They are:

(a) Gain = ∞ $(A \rightarrow \infty)$.
(b) $E_o = 0$ when $E_1 = E_2$.
(c) Input impedance = ∞ $(Z_i \rightarrow \infty)$.
(d) Output impedance = 0 $(Z_o \rightarrow 0)$.
(e) Bandwidth = ∞ (response time = 0) .

These ideal characteristics will be used to develop the equations which control the operation of the amplifier.

<u>Inverting Circuits</u>

The non-inverting input is grounded and the input is supplied through -IN. A feedback loop is connected from the output to -IN. Since Z_i is assumed to be infinite, then no current enters the amplifier so that the input and feedback resistors, R_i and R_f respectively, carry equal currents. Referring to Figure 3, the following equations may be written.

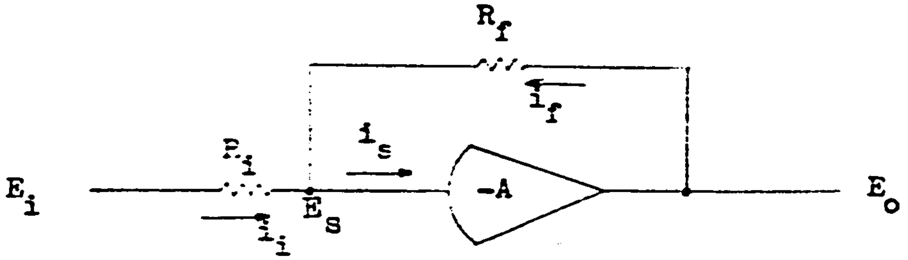


Figure 3

$$i_s = i_i + i_f = 0$$

Therefore, $$\frac{E_i - E_s}{R_i} + \frac{E_o - E_s}{R_f} = 0 ,$$

and since $$E_s = \frac{-E_o}{A} \rightarrow 0 \text{ as } A \rightarrow \infty ,$$

then $$\frac{E_i}{R_i} = - \frac{E_o}{R_f} ,$$

and $$E_o = - \frac{R_f}{R_i} \cdot E_i .$$

The gain can be controlled by the ratio of the external resistors R_i and R_f and as $A \rightarrow \infty$ the summing point potential E_s becomes a virtual ground. This condition, along with the condition that no current flows into the amplifier holds not only for resistive feedback but also for any other complex feedback and input networks.

Extending the general idea of the operational amplifier to incorporate multiple inputs produces a summing amplifier or "summer". There remains only one feedback element but the gains on the various inputs will vary with the value of the particular input resistance. Thus for n inputs the output of the summer is expressed as

$$E_o = -\left[\frac{R_f}{R_1}E_1 + \frac{R_f}{R_2}E_2 + \dots + \frac{R_f}{R_n}E_n\right].$$

There are practical limits on the number of such inputs, but these will be discussed at a later time.

There are other basic inverting circuits such as the integrator and the differentiator. These will not be discussed here as they bear no direct relationship to threshold logic applications. Details are available from such publications as the Burr-Brown Handbook and Catalogue of Operational Amplifiers.

Non-Inverting Circuits

Unlike inverting circuits which may be realized using either single-ended or differential input, the non-inverting circuit realization requires a differential input. The simplest non-inverting circuit is the voltage follower. The input is applied at +IN and the output is fed back to -IN. Algebraically,

$$E_o = A(E_i - E_o)$$

$$E_o = \frac{E_i}{1 + 1/A}.$$

As $A \rightarrow \infty$, $E_o \rightarrow E_i$.

Such a non-inverting, unity-gain amplifier can be used as a buffer element to isolate circuits or devices from one another.

When the feedback is through a voltage divider network, the result is a non-inverting amplifier with gain greater than unity and regulated by the feedback resistors.

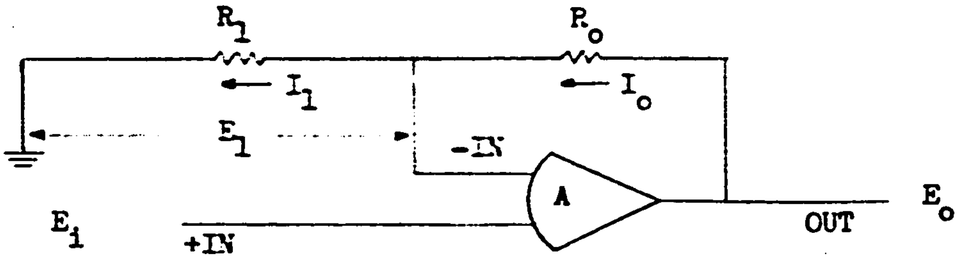


Figure 4

$$E_1 = I_1 R_1 = \left(\frac{E_o}{R_1 + R_o} \right) R_1$$

$$E_o = A\,(E_i - E_1)$$

Combining these equations yields

$$E_i = \frac{E_o}{A} + E_o \left(\frac{R_1}{R_1 + R_o} \right)$$

and as A → ∞

$$E_i = E_o \left(\frac{R_1}{R_1 + R_o} \right)$$

or

$$E_o = \left(\frac{R_1 + R_o}{R_1} \right) E_i \quad .$$

An extension of this result to the feedback differential amplifier which has inputs to both the inverting and non-inverting inputs and feedback from the output to the inverting input produces the relationship

$$E_o = \frac{R_o}{R_1} \left(E_2 - E_1 \right)$$

where E_1 and E_2 are the inverting and non-inverting inputs respectively and R_o and R_1 are the elements of the voltage divider networks for the non-inverting input and the feedback loop.

4. ELECTRICAL SPECIFICATIONS

The theory so far discussed was based on the assumption of idealized operational amplifier characteristics. Introducing a real operational amplifier will cause variations from the predicted ideal operation. These variations can be predicted from knowledge of the electrical characteristics of the amplifier. Discussion on this subject will be limited to the parameters considered most important for threshold logic application. Complete specifications and their meanings are available from the literature.

Rated Output

The output voltage which an operational amplifier is capable of supplying must be known and considered in any application. Over-driving the amplifier can cause at least temporary upsets while the device returns to normal levels if not permanent damage. The limit on the output voltage swing is called the saturation level.

Open Loop Gain

Higher gain yields operation closer to that of the ideal operational amplifier. Ideally, the gain, A, is infinite. Practically it is from 10^4 to 10^8, still quite large. However, since the gain is not infinite, there is a certain error introduced, $= 1/A$, giving

$$\text{Actual Open Loop Gain} = G_c = \frac{\text{Idealized Open Loop Gain}}{1 + 1/A}$$

where A = Open Loop Gain

$$= \text{Feedback Ratio} = \frac{R_i}{R_i + R_f} .$$

If R_i and R_f are perfectly matched the gain error is $1/A$. The A term is called loop gain and can be expressed :

Loop Gain (db) = Open Loop Gain (db) - Closed Loop Gain (db).

Loop gain limits the closed loop accuracy. If feedback is adjusted the finite open loop gain can be compensated leaving only temperature stability to deal with.

Some other useful definitions are:

(a) Slew Rate: maximum rate of output voltage change or rate of swing.

(b) Settling Time : time required to achieve steady state operation after input change.

(c) Voltage Offset : result from unequal base-emitter voltages in the input pair of transistors and is minimized by careful matching; temperature and power supply variations produce drift which can usually be dealt with by external means.

(d) Bias Current : can affect output voltage and cause input offset unless compensated by external circuitry.

(e) Noise : is amplified by closed loop gain; in non-inverting applications it is best to use low feedback impedance to minimize the effects of noise; the bipolar input gives lowest output noise for low values of source and feedback impedance (less than 10K).

(f) Common Mode Voltage -- Common Mode Rejection : In circuits making use of differential input operational amplifiers, consideration of the Common Mode Voltage (CMV) and/or the Common Mode Rejection Ratio (CMRR) is important. Ideally, when the two inputs are equal (CMV), the output is zero, but since the inverting and non-inverting gains are not usually equal, an output voltage will be generated. This is known as Common Mode Gain (CMG).

$$\text{CMG} = \frac{\text{Output Voltage}}{\text{Input CMV}} \quad \text{(where the inputs are tied together)}$$

Another expression of this characteristic is the Common Mode Rejection Ratio :

$$\text{CMRR} = \frac{\text{Open-Loop Gain}}{\text{CMG}} = \frac{A}{\text{CMG}} \ .$$

The non-inverting amplifier is most affected by CMRR which adds another error term to the output. Since the CMV goes to zero whenever either input is grounded, those circuits using both inputs or the differential input type are affected by CMRR.

5. APPLICATION OF OPERATIONAL AMPLIFIERS TO THRESHOLD LOGIC

Basically the function of a threshold gate is to accept a number of weighted inputs, sum them and compare the sum to a previously-selected threshold value. Operational amplifiers lend themselves very nicely to such applications as the preceding discussion of summers and the following discussion of comparator circuits show.

Comparators

A comparator is a simple two-state device whose output reflects the value of the input as compared to a previously-established level. Another way of expressing its operation is that the output indicates the relative polarity of its inputs. Usually, the inputs consist of one reference voltage and one or more variable voltages. The variables may represent physical quantities such as temperature, pressure, etc., or may have no physical connotations at all. Thus, a comparator can effectively perform the operation of a threshold gate by accepting variable weighted inputs and comparing their sum to a reference or threshold value.

There are many different types of comparator circuits with varying degrees of suitability to threshold logic. As more detailed discussion and comparison will be presented in the next chapter, details will be omitted here. Suffice it to say that operational amplifiers can be used to fabricate threshold logic gates. With what degree of succes will be seen later.

Actually there are many difficulties to be overcome in the realization of threshold gates, not the least important of which is the sensitivity requirement. Since, in physical realization, input values and weights are represented by physical quantities, naturally they have variations. When the overall variation exceeds the gap length, g, the output of a threshold logic element will be in error. The overall variation increases with the number of input variables and the size of the weights. Thus, practically, there is a limit to the number of input variables and the sizes of the weights.

The restriction on the weight is rather obvious in the case of resistive inputs. Consider the percentage fluctuation in the nominal value of any given resistor and we realize that larger values will yield larger deviations; e.g., a 1-ohm, 1% resistor may vary between 0.9 and 1.1 ohms, whereas a 100-ohm, 1% resistor may have values between 99 and 100 ohms, a difference of two ohms as opposed to 0.2 ohms for the smaller resistor. Thus, sensitivities will decrease with large-valued weights. The problem that this thesis will deal with , then , is to produce a threshold gate design that employs operational amplifiers and will reduce if not eliminate the constraints on size and number of input weights.

CHAPTER IV : TEST RESULTS AND ANALYSIS

In order to ascertain whether or not operational amplifiers could be successfully used in the fabrication of threshold gates it was necessary to do some laboratory testing and comparison of this type of circuit to the more conventional transistor and diode gates. The following, then, are the results of those tests.

1. THE TEST CIRCUIT

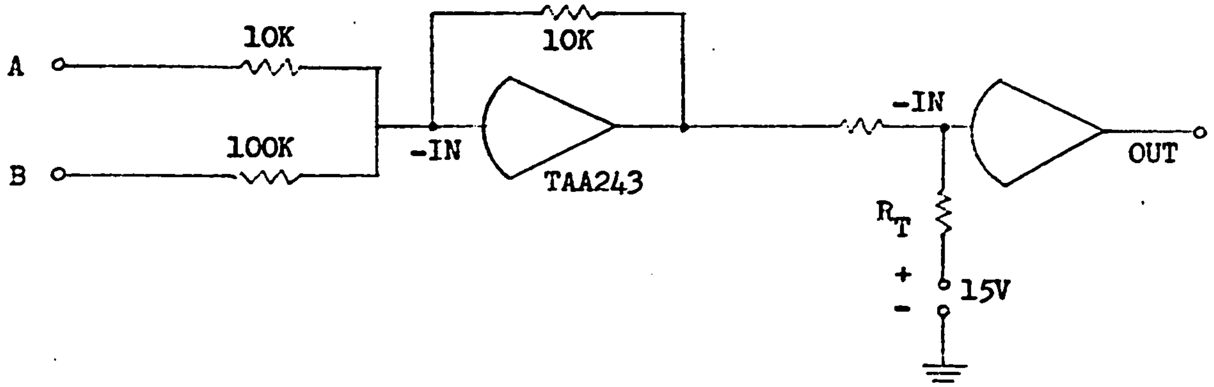
The preliminary tests were performed using a Philips type TAA243 operational amplifier. This is an inexpensive type and does not perform with a high degree of accuracy but was sufficient to establish that the basic idea of using operational amplifiers to fabricate threshold gates was sound. Table 1 shows the particularly relevant data for the TAA243.

Table 1. Reference Data : Philips TAA243 Operational Amplifier

Characteristics at $T_{amb} = 25^{\circ}C$

Voltage gain	G_v	typ.	2300
Common mode rejection ratio	CMRR	typ.	80 dB
Differential input resistance	R_i	typ.	20 kΩ
Output resistance	R_o	typ.	200 Ω
Common mode voltage	V_i	typ.	-6 to 1.5 V
Input offset voltage	V_{io}	typ.	7 mV

Using this operational amplifier in a comparator circuit with a second operational amplifier to sum the inputs produced the circuit and data given in Figure 5.



T = 4.32 V

A	1.68	2.28	2.63	3.03	3.39	4.09	4.29
B	27.16	20.46	16.81	12.27	8.74	0.91	0.00

Figure 5

The first amplifier is used as a summer in the configuration discussed in Chapter III, Section 3, Figure 3. The A input has a gain factor of one since the feedback/input resistor ratio is 10:10 or unity, while the B input has a gain factor of one-tenth since the ratio is 10:100. Thus, in considering the data presented along with Figure 5, the summing process is carried out on the A values taken at face value and the B values taken at one-tenth of face value. What is accomplished by this process is a demonstration of "weighting" of the input variables.

Since the first operational amplifier produces an inversion of the sum of the inputs (i.e., positive to negative), the threshold voltage is established at a positive level. When the sum exceeds the threshold in a negative sense, the second operational amplifier changes output states. This configuration uses positive weights and threshold. If negative values of these variables are desired, appropriate inverters can be introduced to yield the required polarities.

Before continuing to analyse the data we must consider the established threshold level. This level may be varied by adjusting the resistor R_T or the power supply. For the case in point, the threshold was established at 4.32 volts with the upper and lower threshold levels being, respectively, $T_u = 4.37$ and $T_l = 4.27$ volts. It should be pointed out here that these were convenient values for the experiment and are not necessarily convenient values for actual threshold logic use. In the latter case it is preferred to have integral values for the threshold and gap length when integral weights are also being used. Note, however, that it is not hard to effect the desired adjustments to make T itself an integral value. Additionally, since greater sensitivity is afforded when the threshold level is very low, the experimental level was kept reasonably low and could, as explained earlier, be made lower. The constraints here, of course, lie in the ability of the power supply to produce a steady, low-level voltage (say several hundreds of millivolts) and the successful neutralization of input offsets that could introduce large-scale errors.

Let's now consider the recorded data to see how well it confirms the premise that operational amplifiers are really useful for threshold gate realization.

Table 2 : Sample Calculations

Input		Weight		Weighted Input		Sum	Output
A	B	A	B	A	B		
1.68	26.16	1	1/10	1.68	2.616	4.296	HI
2.28	20.46	1	1/10	2.28	2.046	4.326	HI
2.63	16.81	1	1/10	2.63	1.681	4.311	HI
3.03	12.27	1	1/10	3.03	1.227	4.257	LO
3.39	8.74	1	1/10	3.39	0.874	4.264	LO
4.09	0.91	1	1/10	4.09	0.091	4.181	LO
4.29	0.00	1	1/10	4.29	0.000	4. 29	HI

In the cases where the sum of the weighted inputs fell within the gap

($4.27 < T \leq 4.37$) the output was HI (or 1). In the remainder of the cases, where this sum was less than T_1, the output was LO (or 0). Since the problem of negative weights inposes some peculiar effects we restricted ourselves to positive values.

This threshold gate realization seems to provide a very sensitive test of the threshold level. As mentioned earlier, the maximum variation in T was 4.37 - 4.27 = 0.1 volt. Thus the sensitivity value for T of 4.32 volts is

$$S_T = \frac{0.1}{4.32} .$$

Obviously this will improve if the threshold level is lowered and as has been discussed, this is easily possible.

To see further how the threshold can be changed and how this will affect the operation of the gate the following data was gathered and plotted as shown in Tble 3.

Table 2 : Threshold Level Variation

$R_1(K\Omega)$	$R_2(K\Omega)$	$E_{ref}(V)$	$E_t(V)$	$E_i(V)$	E_o
1	1	1	1	1	HI
1	1	1.5	1.5	1.5	HI
1	1	2	2	2	HI
1	1	3	3	3	HI
1	.5	.5	1	1.02	HI
1	.5	1	2	2.02	HI
1	.5	1.5	3	3.02	HI
1	.5	2	4	4.02	HI
.5	1	2	1	1.01	HI
.5	1	4	2	2.01	HI
.5	1	6	3	3.01	HI
.5	1	8	4	4.01	HI

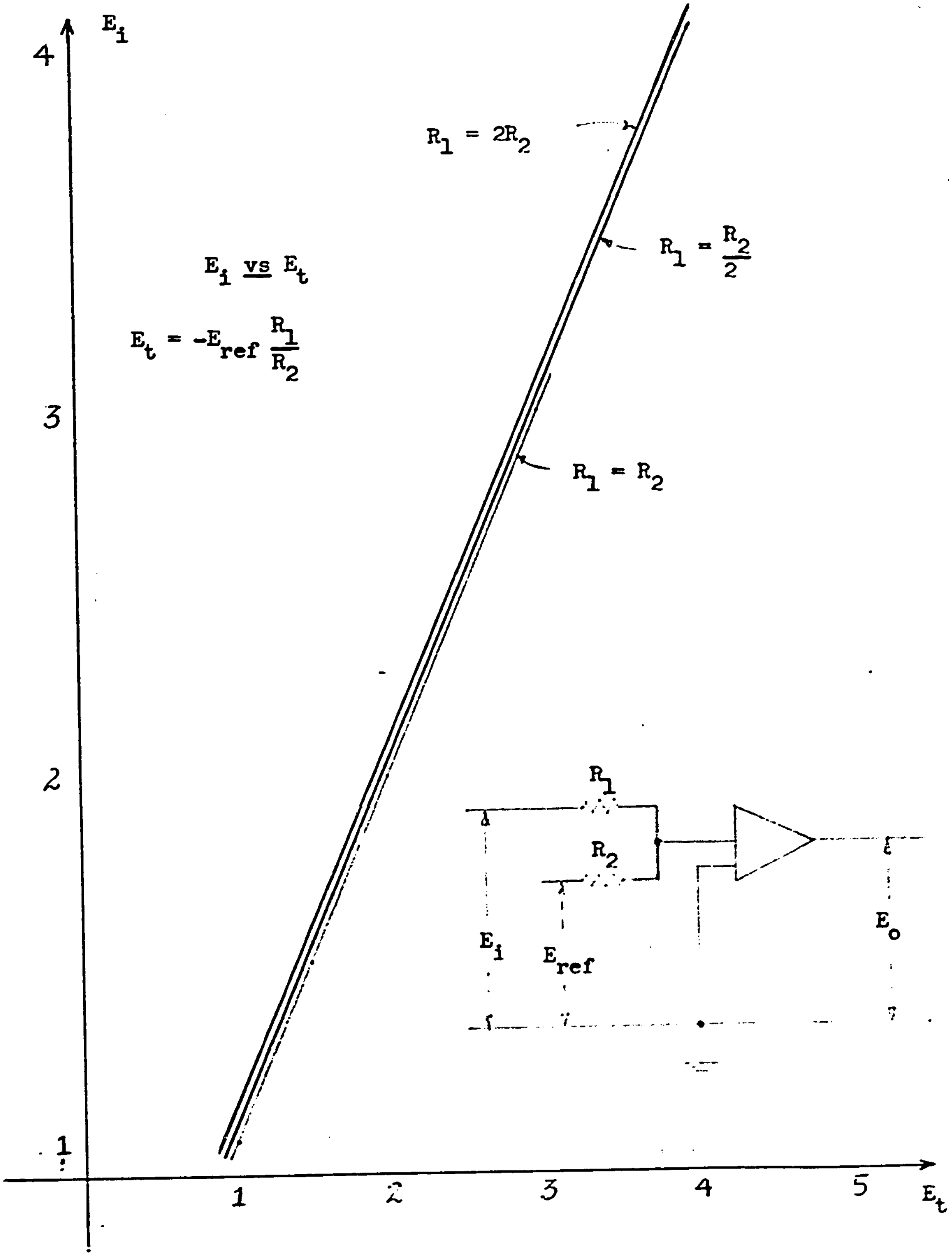

E_i
4
3
2
1
E_i vs E_t
$E_t = -E_{ref} \frac{R_1}{R_2}$
$R_1 = 2R_2$
$R_1 = \frac{R_2}{2}$
$R_1 = R_2$
1
2
3
4
5
E_t
R_1
R_2
E_i
E_{ref}
E_o

Figure 6

The circuit shown in Figure 6 is just the second part of the circuit of Figure 5. The threshold level, E_t , is a function of the reference voltage, E_{ref} , and the input resistors R_1 and R_2. Obviously, then, great latitude is available for the adjustment of the threshold level as R_1, R_2, and/or E_{ref} may be varied. The data in Table 3 was gathered by making just such variations.

The values listed under the heading "E_t" are the calculated values of E_t using the equation and the values under E_i (input) are the minimum inputs required to trigger the operational amplifier into the other output state. As the data and graphs indicate, the gate functions very consistantly even as E_t is varied and the external circuitry is varied. The sensitivity remains very good.

The weight sensitivity can be controlled by the accuracy of the resistors. Since the sensitivity is directly proportional to the allowable variation in the nominal value of the resistor, it is beneficial to use resistors produced in the same batch of high quality resistors to assure as far as possible a uniformity in value.

The threshold sensitivity of the gate is subject to yet another constraint, that being the offset voltage of the amplifier. However, this value is usually constant and is specified by the manufacturer (Table 1). Therefore, establishment of a threshold value is dependent only on correct biasing and hence on the resistors used in the feedback loop.

From these preliminary results it can be seen that operational amplifers can be quite successfully used to realize threshold logic gates. However, to return to the sensitivity problem, we must take a closer look to see if it is satisfactorily handled by this realization. In order to better understand the problem first consider the following threshold logic gate constructed simply of Diodes, resistors, and transistors.

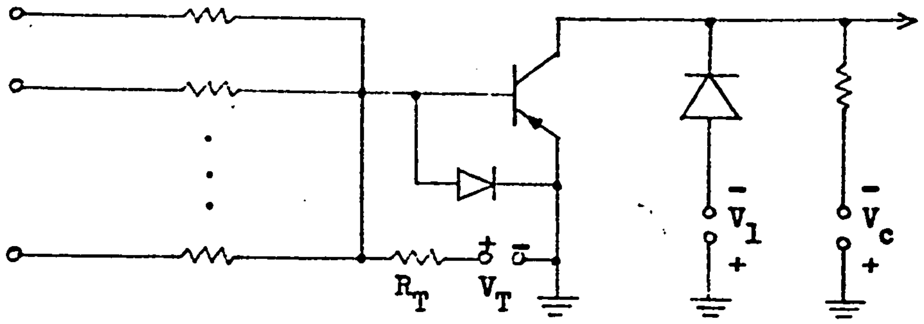


Figure 7

This is a low fan-in gate circuit with a fan-in range of about one to ten. To obtain high fan-in circuits, it is necessary to offset the decrease in efficiency of the normal resistance adder that high fan-in causes. This is the purpose of the diodes in the input leads and the resistor R_B (Figure 8) . For such circuits the efficiency is independent of fan-in and depends only on gap position; therefore, the fan-in is practically unlimited.

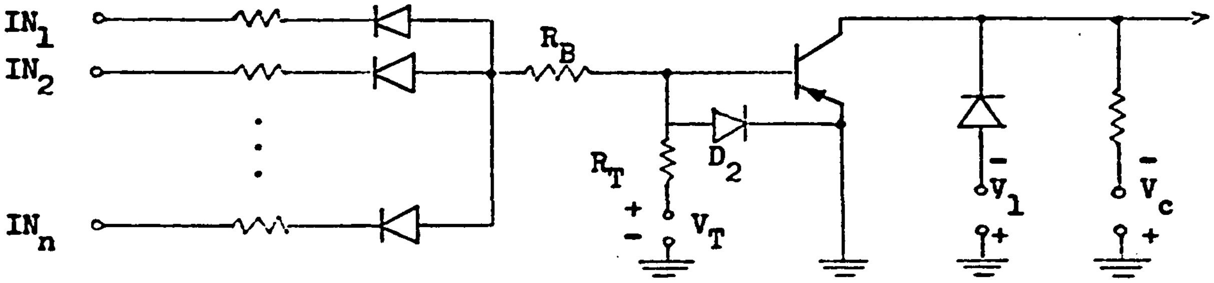


Figure 8

The gates such as that shown in Figure 8 are constructed from readily-available components and operate over a fan-in range of one to fifteen (although, as explained, thay need not be so limited) and a fan-out of one to ten (one to fifty when an emmitter-follower is included). The range of the gap T_u:T_1 is from 1:0 to 5:4.

The voltage corresponding to logical "1" is determined by the clamp supply V_1, and the clamp diode voltage V_D. The logical "0" voltage is determined by the collector-emmitter saturation voltage of the transistor. The input circuit is the standard resistance-type adder that includes the threshold , as determined by R_T and V_T, as one of the inputs. The input circuit includes a second clamp diode, D_2, to prevent the transistor base from becoming excessively positive with respect to the emitter.

If it is desired to construct threshold gates with high gap locations (e.g., 9:8), then high logic levels are required and consequently tolerances must be strictly controlled. (As noted previously, sensitivity is higher for lower gap locations.) Such tolerances are fairly easily obtained in individual or discrete components. For example, resistors with tolerances of plus or minus one percent of nominal are available and power supplies reliable within 0.05 percent also exist as off-the-shelf items. It is obvious, then, that the more discrete components (transistors, diodes, resistors, etc.) that are used, the more sources there are to introduce error. Use of operational amplifiers to replace discrete components will help to reduce the number of error sources and produce a more reliable threshold gate.

2. ADDITIONAL CIRCUITS

The test circuit previously described is only a representative scheme for threshold gate realization. A few other circuit designs using ordinary operational amplifiers and specially designed threshold or level detectors will now be discussed.

A threshold detector (Figure 9) may be built using an operational amplifier producing a circuit similar to a Schmitt Trigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier ouput is in either the positive or negative saturated state, the positive feedback network provides a voltage at the non-inverting input which is determined by the attenuation of the feedback loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must change polarity by an amount larger than the amplifier input offset voltage. When this occurs, the amplifier saturates in the oposite direction and remains in that state until the voltage at its input again reverses.

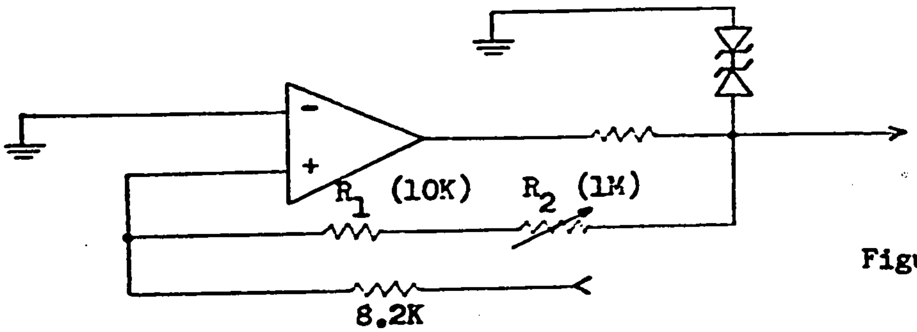


Figure 9

The zener diodes clamp the detector to make it independent of temperature and supply voltage. The detector may be compensated if power supply impedance causes oscillation during its transition time.

The circuit shown in Figur 10 uses an operational amplifier in an open-loop configuration to supply the comparator function. The very high open-loop gain means that only a very small differential input signal is needed to cause the amplifier output to make a transition between saturated states. In such a comparator circuit the input threshold voltage is equal to E_{ref}. This E_{ref} must not exceed the maximum common-mode-voltage for the particular operational amplifier in use. If desired, the input and reference voltages may be interchanged thus changing the polarity of the output transition.

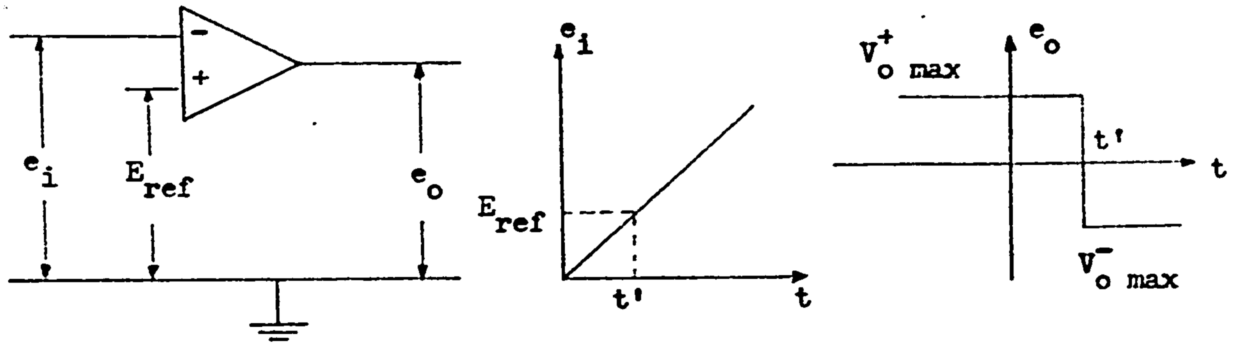


Figure 10

If only one input is used (as in Figure 6), then the reference and input voltages are applied to the same input terminal of the operational amplifier through appropriate resistors. The other input terminal of the amplifier is earthed and consequently no common-mode limitations exist. E_{ref} may be any convenient voltage opposite in polarity to the signal voltage. The threshold voltage is set by a choice of input resistors.

In both of these comparators the input voltage must swing past the threshold voltage by an amount

$$\frac{V^+_{o\,max} - V^-_{o\,max}}{A_{VOL}}$$

for the full output transition to take place. In the case of rapidly changing input signals the output transition time is dependent on amplifier characteristics, but when the input voltage varies comparatively slowly the time is dependent on the rate of change of input voltage. In the latter case it is often advantageous to speed up the output transition time by using some form of regenerative comparator. In this arrangement (Figure 11) positive feedback is applied between output and input via resistors R_2 and R_1, and when e_i reaches the threshold voltage the amplifier switches regeneratively between saturated states, the output transition time being made virtually independent of the rate of change of input voltage.

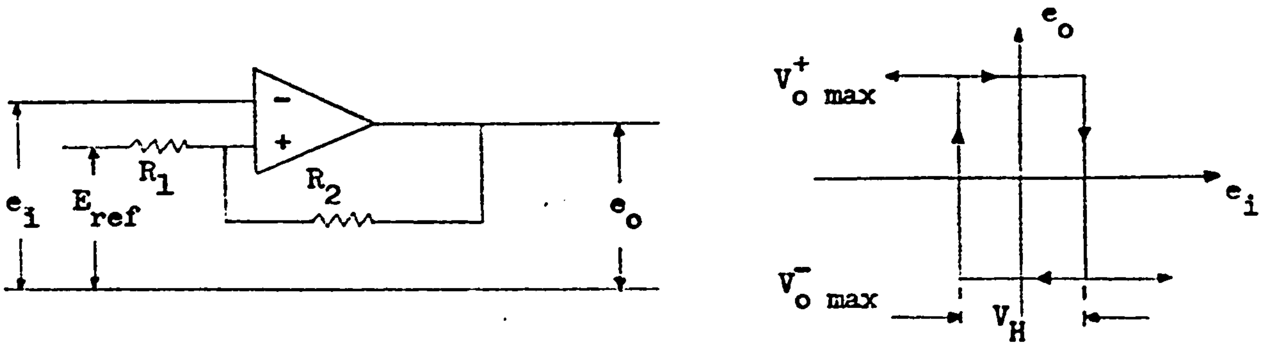


Figure 11

The circuit exhibits hysteresis, i.e., the transition takes place for different values of e_i dependent on whether e_i is increasing or decreasing towards E_{ref}. The transfer curve for the comparator is illustrated for a value of E_{ref} equal to zero. The input threshold voltage at which the transition takes place has a value of approximately

$$V_{o\,max} \frac{R_1}{R_1 + R_2}$$

and with $V_{o\,max}$ having its positive and negative saturation values, the amount of hysteresis is thus

$$V_H = (V_{o\,max}^{+} - V_{o\,max}^{-}) \frac{R_1}{R_1 + R_2} \quad .$$

In all comparators outputs may be clamped to desired values rather than using saturation limiting and it is important that care be taken to ensure that reference and input voltages do not exceed allowable limits for common mode and differential input signals.

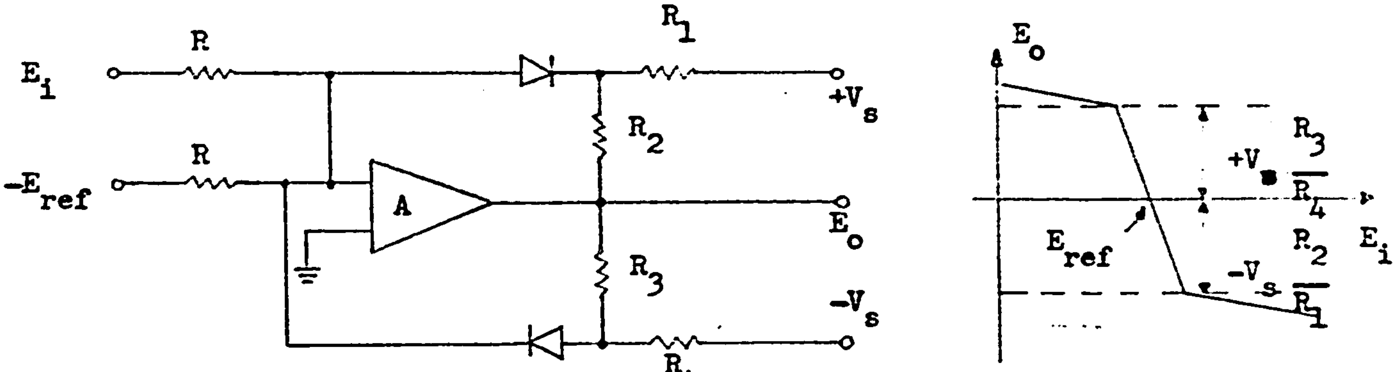
Also available from manufacturers in pre-packaged forms are threshold detectors of different sorts. However, as this discussion deals only with threshold devices employing operational amplifiers, these other devices will not be considered further at this time.

3. PERFORMANCE ANALYSIS

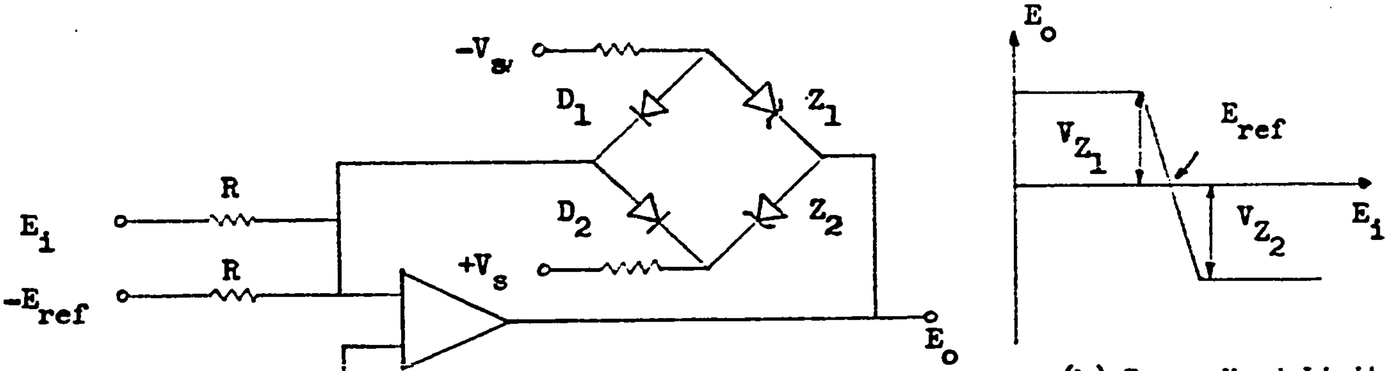
Several comparator circuits have been shown in this and the last chapter. It is now necessary to consider the advantages and disadvantages of each with respect to application to the realization of a threshold gate.

In Chapter III, Section 5, comparator circuits with different limiting circuits were mentioned. These are shown in Figure 12. All of these use a single input configuration which results in a relatively slow switching time from state to state but has the advantage that there is no common-mode limitation on the reference and input voltages. This latter may be useful where relatively high voltages are in use in the threshold network. The choice of output limiting technique can be made to coincide with the requirements of the circuit. For example, if it is not important that the output voltage maintain a steady state value above and below the reference level then the simple "soft limit" will suffice. If the output must remain steady then either the zener or transistor "hard" limiting can be employed. The transistor technique affords an easier way of adjusting the output limiting levels by simply adjusting the resistor divider network. The zener circuit would require a change in the value of the zener diodes in the bridge network. All three circuits provide about the same output transfer, that is, the slope of the transfer curve is approximately the same in each case.

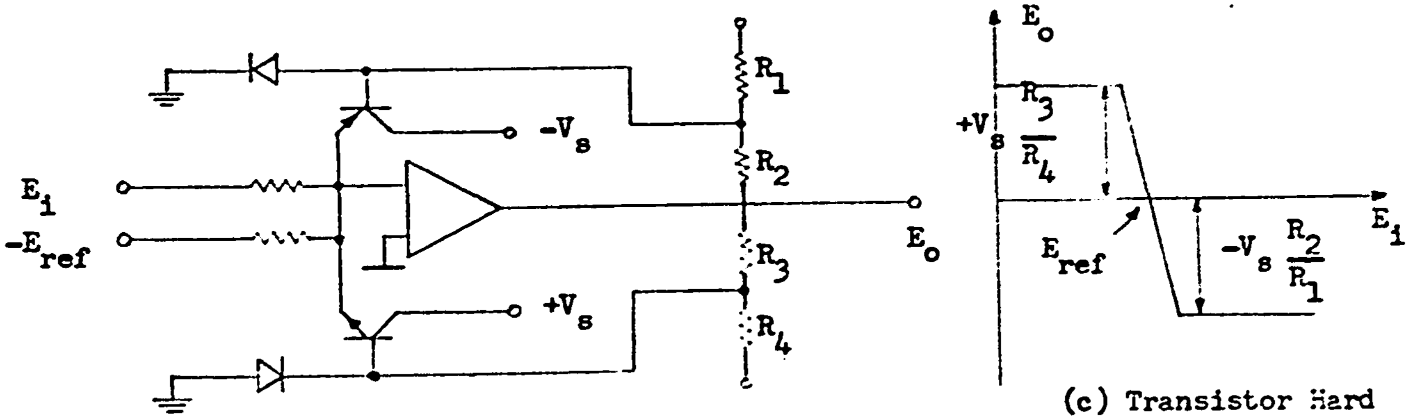
For a faster response to an input voltage change which exceeds or drops below the threshold or reference level the differential input configuration is used. However, as was noted earlier, there is a restriction on this configuration. The value of the threshold voltage must not exceed the maximum CMV for



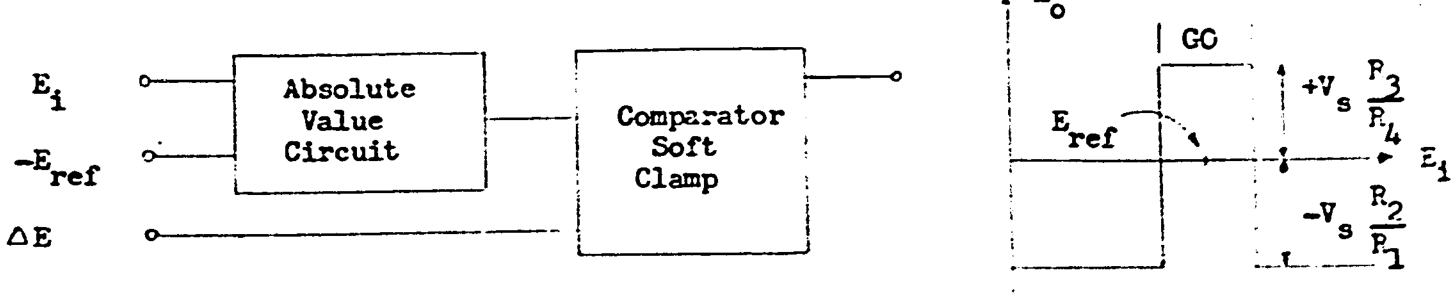
(a) Soft Clamp



(b) Zener Hard Limit



(c) Transistor Hard Limit



(d) Window Comparator

Figure 12

the particular amplifier in use. For most logic circuit applications this will pose no particular problem. In fact, in threshold function realization it is advantageous from a sensitivity point of view to keep the threshold value low (see Sheng, Chapter 9, Section 9-6).

Figure 10 shows the transfer curves for a typical differential input comparator. The slope of the output voltage curve at time t' (when the input voltage reaches the reference level) is infinite; i.e., the voltage swing is instantaneous. Figure 11 shows positive feedback techniques which also provide a steep (slope $= \infty$) transfer curve at the $V_{in} = V_{ref}$ point. However, these circuits also introduce hysteresis which provides noise immunity but sacrifices comparison-point accuracy. The width of the hysteresis loop is easily controlled by the ration of the feedback resistors though, and so can be adjusted to an acceptable amount to satisfy sensitivity requirements and still gain the advantage of noise immunity.

The circuit shown in Figure 9 is similar to that of Figure 11. It was designed for use in a constant amplitude triangular wave generator and consequently the resistive values are specified for that application. They are adjustable to be compatible with any circuit use. This circuit exhibits a very rapid response but is restricted in that the input cannot exceed the differential mode voltage of the amplifier. Also, since the amplifier changes state only when the input voltage changes polarity by an amount greater than the input offset voltage then such a comparator would be of no use in a logic circuit employing only positive logic levels. However, it could be very useful in circuits using positive and negative logic levels, again taking into consideration the hysteresis affect of the positive feedback.

The "window" comparator shown in Figure 12(d) could be used in threshold logic but only in specially restricted applications. Since the output is positive only when the input falls within a previously-established range then some restriction must be put on the input so that it will not exceed the threshold value by more than a specified amount. The gap length can easily be regulated by adjusting ΔE. Under these restrictions the comparator is useful. However, it is unlikely that the input voltage can be controlled so closely so as not to exceed the threshold level by more than ΔE. In other words, for threshold logic applications the window comparator circuit is not very feasible.

It would appear then, that either the single or differential input configurations will satisfy the requirements of a threshold gate, the choice being based on speed and input requirements. The output limiting and hysteresis features can also be selected to conform to particular application requirements. Clearly, though, the operational amplifier will function as a threshold gate.

4. FABRICATION TECHNIQUES

It has now been seen that the operational amplifier will fulfill the requirements for realization of a threshold logic gate. The question which remains to be answered is whether an operational amplifier can be incorporated along with the necessary external circuitry into a simple single package containing one or more threshold gates.

A recent development by Motorola Semiconductors Products Div., a single chip containing six internally-compensated, high performance operational amplifiers, is one possible answer to the problem. If each threshold gate was implemented using a pair of operational amplifiers then such a chip could be used to fabricate three gates. The external circuitry, the resistors which are needed to weight the inputs to the first operational amplifier (the summer) and those needed to provide threshold level adjustment on the second operational amplifier (the comparator) could be manufactured separately by thin film deposit techniques and the appropriate connections made to produce a single package. In fact, Bell-Northern Laboratories use a process of this nature in production of circuitry for the "touch tone" telephone dialing system.

At present, integrated circuit technology does not produce highly accurate individual resistors on silicon chips. The "pinch" resistor, which can be made with values of from 2 ohms to about 10 K-ohms, has at best a tolerance of about two percent nominal. However, very accurate resistor ratios can be produced on silicon chips and as resistor ratios play a very important part in the circuits which have been discussed, this technology can be made use of in the proposed threshold gate fabrication.

Thus, the technology exists today to produce a single package incorporating operational amplifiers to realize threshold logic gates.

CHAPTER V : CONCLUSIONS

In Chapters III and IV several comparator circuits were presented and discussed. The relative merits and demerits of each will render them useful or impractical in certain circumstances, but in general it was shown that an operational amplifier realization is indeed very feasible and quite desirable.

Also available now from the manufacturers are pre-packaged circuits which are actual threshold detectors in themselves. These were not considered in detail as this thesis meant only to deal with operational amplifier circuits. However, these devices should receive some mention here as further investigation could prove them to be equal or superior to any other method. For example, Philips Electron Devices produce special integrated circuits for comparators for use with core memories where speed is more important than sensitivity. They also have the TAA560 Level Detector, the data for which will be found in the appendices. General Electric also produces a level detector, the PA494. Again, the data will be found in the appendices.

It has been noted variously throughout this writing that ultimate accuracy depends not on one or even two but a number of contributing factors. It is generally accepted that operational amplifiers, as products of today's advanced technology, are capable of highly accurate performance. Thus the basic summing and comparing operations which comprise the proposed threshold gate realization method can be performed accurately given that the external devices used in conjunction with the operational amplifier also are of a controlled accuracy. Here again, today's knowledge and production techniques can assure high tolerances in such items as resistors and power supplies which are really the only components needed to complement the operational amplifier integrated circuit. All these items are available off-the-shelf and so do not invlove additional special-order costs.

This concludes this discussion of the realization of threshold logic gates using operational amplifiers, at least as far as the feasibility of such a plan is concerned. It has been shown that such configurations can come up to any desired requirements and do so in a simple and economic way. A detailed discussion of costs was deliberatley avoided as the price range of operational amplifiers is so wide reaching (from several dollars to several hundreds of dollars) and constantly changing as production techniques improve, that such a discussion would have little meaning. Suffice it to say that quality varies with cost and that the user's budget will dictate the quality he can demand.

This thesis has not presented the ultimate solution perhaps for the realization of threshold logic gates, but its proposal is certainly workable and has offered yet another approach through the pre-packaged threshold devices that are now available.

APPENDICES

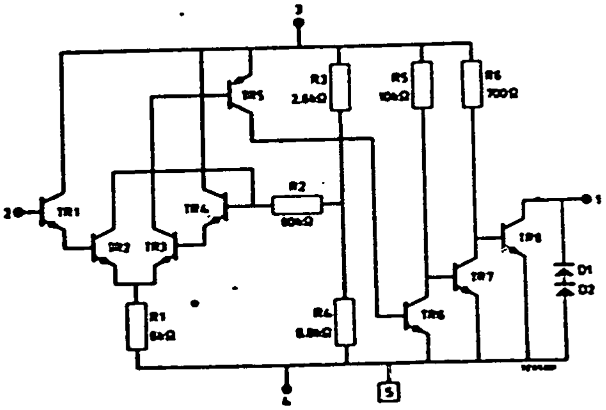
APPENDIX A: Philips TAA560 Level Detector

The TAA560 is a silicon monolithic integrated level detector in a metal envelope. A Darlington input circuit forms a Schmitt-trigger that operates at a low current level. Due to the three-stage current amplifier an output current of maximum 50 mA can be delivered. It is primarily intended for battery fed timing circuits, such as in camera shutter control.

Characteristics

Threshold Voltage		
Switching to OFF-state	Supply at 2.5 V	typ. 1.5 V
	Supply at 4.5 V	typ. 2.9 V
Switching to ON-state	Supply at 2.5 V	typ. 1.2 V
	Supply at 4.5 V	typ. 1.4 V
Input Voltage		max. 4.5 V
Output Voltage		max.12.5 V
Output Current		max. 50 mA

Circuit Diagram



APPENDIX B : General Electric PA494 Precision Threshold Detector with Hysteresis

The PA494 is a monolithic integrated circuit threshold detector with 10% hysteresis and is intended for application requiring the logic function of a Schmitt-trigger but with superior voltage and temperature stability. With input sensitivity below 100 nanoamperes and its own voltage reference (0.6 of supply voltage), this IC provides an ideal interface with high impedance resistor dividers or voltage inputs as well as threshold detection of approximately one time constant for resistor-capacitor networks. The wide range of power supply voltages and output characteristics also makes the PA494 directly compatible with many other types of quasi-linear or digital circuits as well as with discrete resistive or inductive loads.

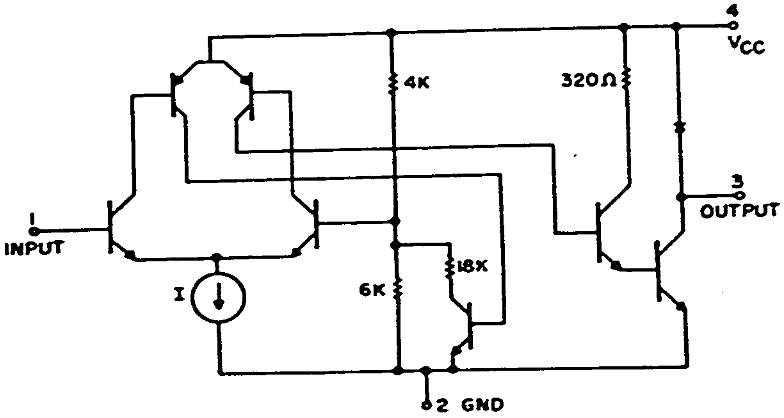
Maximum Ratings

V_{cc}	+9 V (min. 2.3 V)
V_{output}	+9 V
I_{output}	250 mA
V_{input}	+9 V

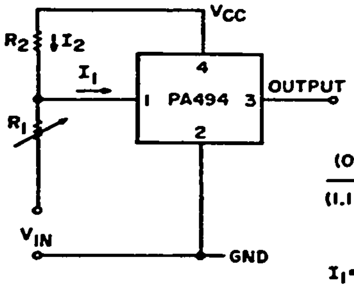
Electrical Characteristics

L_{OFF} Switching Level (V_{in}/ V_{cc})	typ. 0.61
L_{ON} Switching Level (V_{in}/ V_{cc})	typ. 0.54

Circuit Diagram



Voltage Threshold Detction Circuits



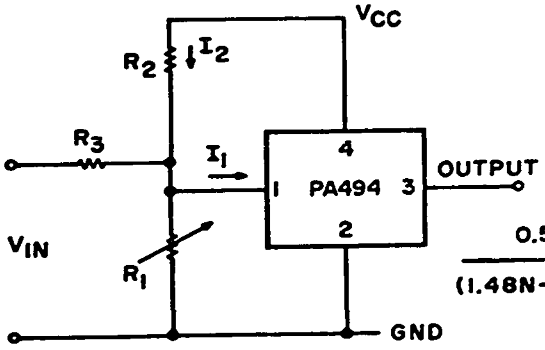
$$R_2 = \frac{0.4V_{CC}}{N(1 \times 10^{-7})}\ \Omega$$

$$\frac{(0.54V_{CC}-V_{IN})}{(1.15N-1)(1 \times 10^{-7})}\ \Omega < R_1 < \frac{(0.66V_{CC}-V_{IN})}{(0.85N-1)(1 \times 10^{-7})}\ \Omega$$

$I_1 = 1 \times 10^{-7}$ AMP (MAX)

N = RATIO OF RESISTOR BIAS CURRENT TO $I_1 = I_2/I_1$

Figure (a) Voltage Level Detection for $V_{IN} < 0.4V_{CC}$



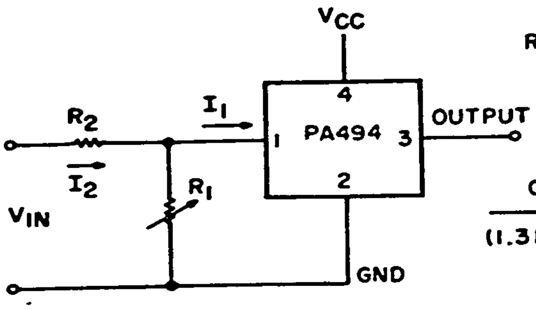
$$R_2 = \frac{0.4V_{CC}}{N(1 \times 10^{-7})}\ \Omega$$

$R_3 = 2\ R_2$

$$\frac{0.54V_{CC}}{(1.48N-1)(1 \times 10^{-7})}\ \Omega < R_1 < \frac{0.66V_{CC}}{(0.52N-1)(1 \times 10^{-7})}\ \Omega$$

$N = I_2/I_1$

Figure (b) Voltage Level Detection for $0.4V_{CC} < V_{IN} < 0.8V_{CC}$



$$R_2 = \frac{V_{IN}-0.6V_{CC}}{N(1 \times 10^{-7})}\ \Omega$$

$$\frac{0.54V_{CC}}{(1.3N-1)(1 \times 10^{-7})}\ \Omega < R_1 < \frac{0.66V_{CC}}{(0.7N-1)(1 \times 10^{-7})}\ \Omega$$

$N = I_2/I_1$

Figure (c) Voltage Level Detection for $V_{IN} > 0.8V_{CC}$

APPENDIX C : Large Scale Integration

Motorola Semiconductor Products Inc. has developed two methods of fabricating complex circuits on a single chip or board. The first is sort of a pseudo-Large-Scale-Integration (LSI) technique involving more conventional Medium Scale Integration (MSI) chips and compact multi-layer interconection packaging. The second is "MCS Polycell LSI", a new process capable of producing complex custom-designed integrated circuits.

The development of large area, high density MOS chip fabrication technology makes LSI possible today. The Motorola Polycell LSI System provides the design capability that makes LSI practical as well. The ability to quickly and economically reduce custom circuit requirements to working chips is the key to LSI. This is the roll of the Polycell System. The heart of this system is a library of MOS P-channel logic cells, self contained units for performing logic functions. The electrical performance of each cell, consisting of a number of interconnected components, has been characterized. The fact that these cells are handled as units greatly expedites the entire design procedure.

Many circuit realizations are possible using the present cell designs. However, some circuits may require the development of new cell designs. This is possible but may be rather costly at the present time. As the technology advances these costs will be reduced proportionately.

The other method mentioned above is shown in the accompanying diagrams. This is an example of a 3-Bit A/D Converter, but other circuits could be realized using a similar procedure. The key to effective design lies in the multilayer board. These guidelines commonly used with 1 nanosecond digital logic are: 1) minimum line length, 2) matched transmission lines, 3) ground plane environment, and 4) coaxial input/output signal paths.

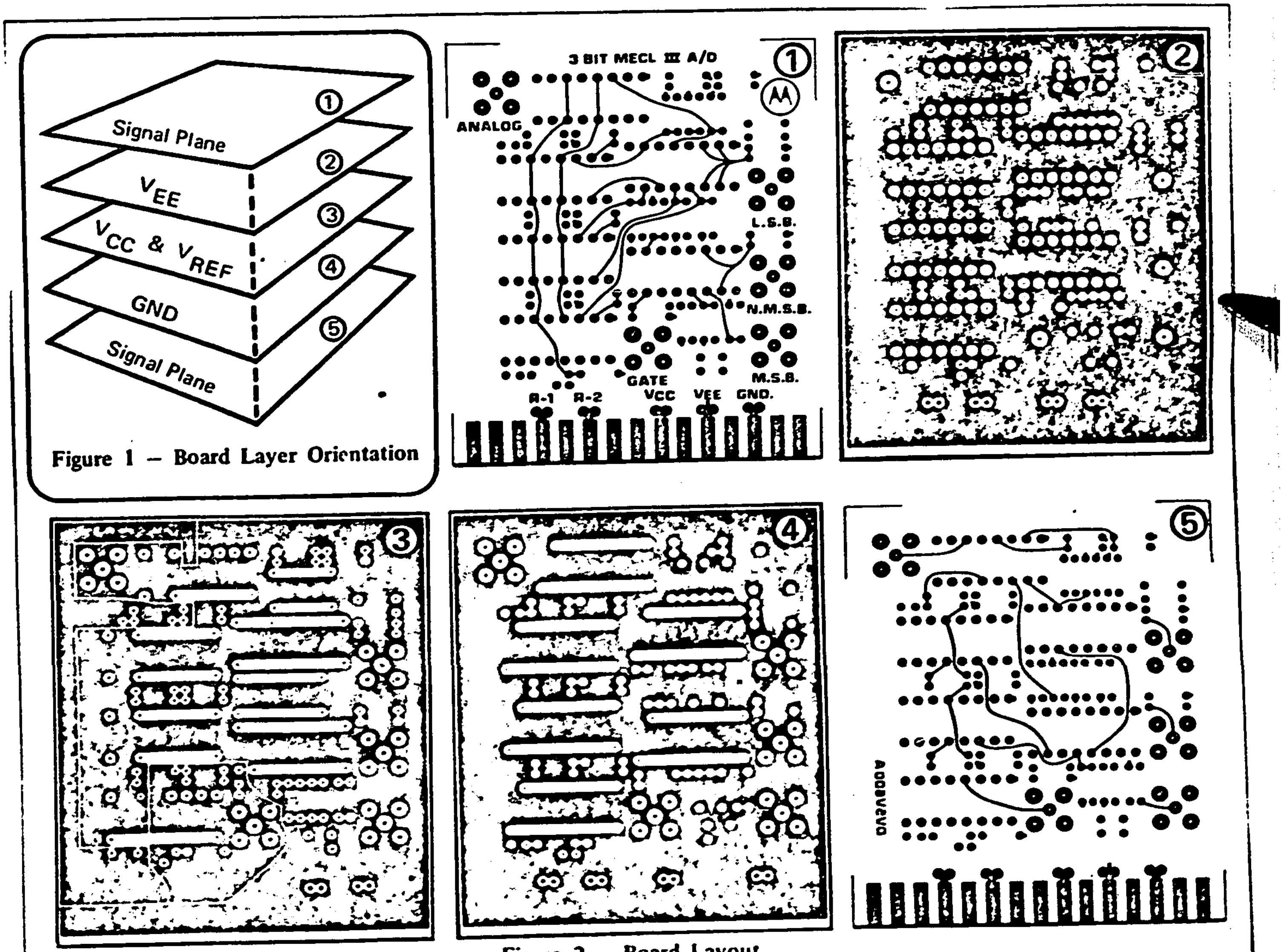


Figure 1 – Board Layer Orientation

Figure 2 – Board Layout

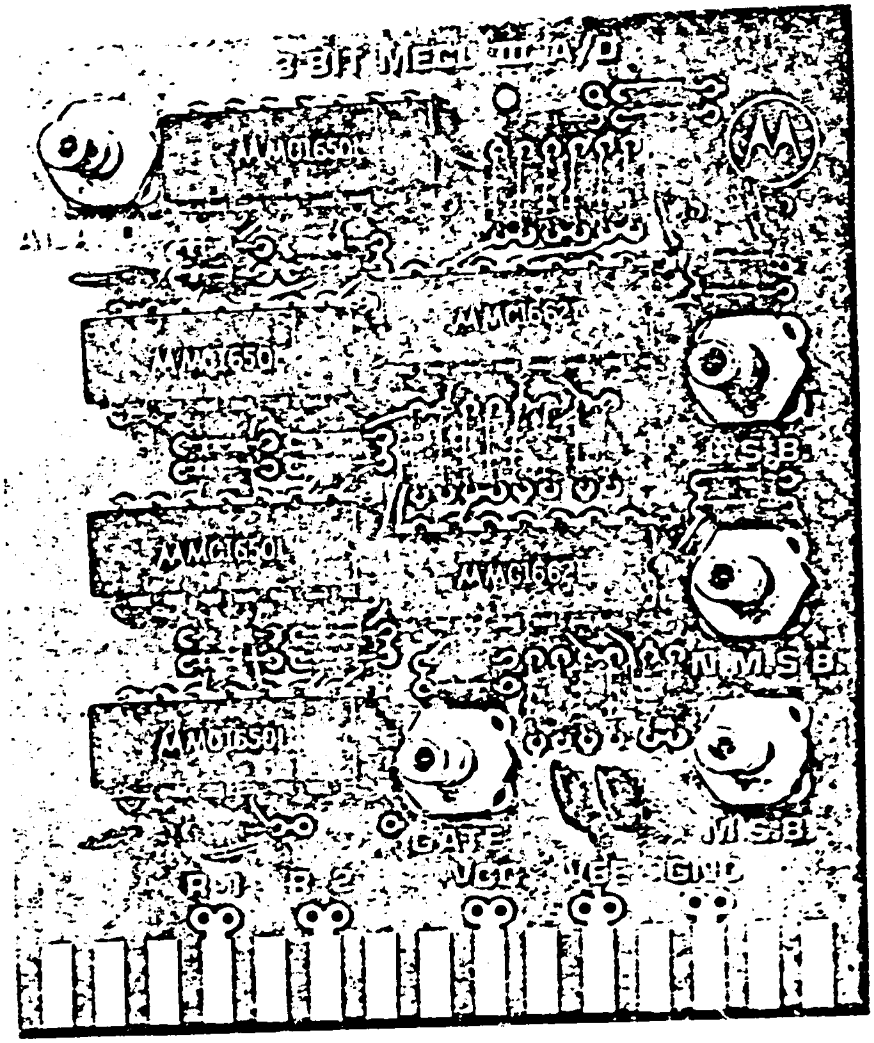


Figure 3 A Completed Board

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