Design and Implementation of an Integrated Energy-Harvesting Non-Coherent Control Architecture for Beam-Steering Systems

Mohamad Al Sabbagh



uOttawa

Thesis submitted to the University of Ottawa

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical and Computer Engineering

Ottawa–Carleton Institute for Electrical and Computer Engineering

School of Electrical Engineering and Computer Sciences

University of Ottawa

© Mohamad Al Sabbagh, Ottawa, Canada, 2026

Abstract

Scaling phased–array beam–steering systems increases the complexity of distributing power, clock, and control signals to a large number of beam–steering elements. This thesis presents a wirelessly powered control architecture for phased–array beam–steering that combines Wireless Power Transfer (WPT) with non–coherent Amplitude–Shift Keying with Pulse–Width Modulation (ASK–PWM) communication to reduce the need for conventional wired power, clock, and control distribution.

The proposed architecture uses a single–input interface to wirelessly deliver power and control information to distributed beam–steering control blocks. WPT is used to energize the control circuitry, while ASK–PWM enables recovery of data and clock signals from the same received signal without phase–locked loops or conventional SPI interfaces. A synthesizable digital frame router is developed to decode and distribute the received control information to multiple beam–steering elements. To support the proposed architecture, this work further develops an energy–harvesting ASK–PWM receiver, RF isolation and leakage–mitigation techniques for energy–harvesting circuits, a PCB–feasible skewed buffer for PWM decoding, and a slewed–comparator–based DAC architecture for control–voltage generation.

The proposed architecture is implemented and experimentally evaluated through FR–4 PCB prototypes and a custom 130–nm CMOS integrated circuit. These hardware implementations demonstrated the operation and integration of the wireless power, communication, and beam–steering control functions. The resulting system is integrated with a phased–array antenna to experimentally demonstrate beam–steering.

The experimental results demonstrated the feasibility of combining wireless power transfer and non–coherent ASK–PWM communication for distributed beam–steering control thus, reducing the dependence on conventional wired power, clock, and SPI control distribution.

Acknowledgments

*First and foremost, I would like to thank **Almighty Allah** for granting me the strength, knowledge, health, patience, and opportunity to pursue and complete this research. I pray that **Allah** blesses this work and accepts it among my good deeds.*

*I would like to express my sincere gratitude to my co–supervisor, **Professor Rony Amaya**, for his continuous guidance and support throughout this research. I am especially thankful for the weekly meetings and discussions, which greatly contributed to my development as a researcher. His advice, insight, and constructive challenges constantly pushed me to think deeper and improve my work. Despite his busy schedule, he always made time to help, including during evenings and weekends when needed. I truly appreciate his dedication, mentorship, and the valuable lessons I learned from working with him.*

*I would also like to sincerely thank my supervisor, **Professor Mustapha Yagoub**, for his support, expertise, and guidance throughout this work. His deep knowledge and experience in the field were invaluable during the course of this research. I greatly appreciate his thoughtful advice and his ability to propose practical and effective solutions to research challenges. In addition, his careful review and revision of my writing significantly improved the quality of this thesis. Beyond his academic support, I am thankful for his kindness, encouragement, and approachable personality.*

*I would also like to thank **Dr. Maryam Hasheminasab** for her contributions to the reflective phase shifter and beamformer layouts, **Dr. Kam Kedze** for designing the patch antenna used in this work, and **Dr. Abdullah Al Mohaimeed** for his valuable advice and guidance on wireless power transfer. Their support and contributions are greatly appreciated.*

*I would also like to thank the technical staff and engineers whose support was invaluable throughout this research. In particular, I sincerely thank **D!** for his PCB and FPGA expertise, **Nagui Mikhail** for equipment support and system interface guidance, and **Jean–Noël Nugu** for assistance with the anechoic chamber and equipment coordination. I also greatly appreciate **Scott Bruce** for restoring my damaged design files at a critical moment.*

*I would also like to express my deepest gratitude to my parents, **Bassam** and **Muna**, for their endless love, sacrifices, and unwavering support throughout my life and academic journey. They sacrificed so much to help me reach where I am today, and for that I will be forever grateful. Thank you for your constant encouragement, life advice, wisdom, and belief in me through every challenge and success. I would also like to thank my sister, **Ghalia**, and my brother–in–law, **Wael**, for their constant support, encouragement, and for always checking up on me throughout this journey.*

*I would also like to thank my friends **Dr. Mohannad Al Bezreh**, **Abdullah Al Bezreh**, **Khalid Ali**, **Dr. Mohamad Adghim**, **Dina Adghim**, **Ahmed Al Nasser**, and **Qusai Mansour** for their constant support throughout this journey. Thank you for listening to me endlessly talk and complain about the PhD without ever getting tired of it. Your friendship, encouragement, and the moments we shared made this journey much lighter and more enjoyable.*

*Finally, I would like to thank the **University of Ottawa** and **Carleton University** for providing the opportunity and resources necessary to conduct this research. I would also like to acknowledge the support of **CMC Microsystems** for facilitating the integrated circuit design and fabrication aspects of this work.*

Table of Content

Chapter 1: Introduction 1
1.1 Research Motivation 1
1.2 Problem Statement and Research Question 2
1.3 Research Objectives 4
1.4 Proposed Research Solutions 6
1.5 Research Contributions 8
1.6 Research Publications 11
1.7 Thesis Outline 11
Chapter 2: State–of–the–Art Literature Review 13
2.1 Power and Information Routing Issues in Phased Array Systems 13
2.2 Synchronous Data Transfer in Phased Array Systems 19
2.3 Issues Prototyping WPT with ASK–PWM Receiver on PCB 23
2.4 Conclusion 26
Chapter 3: Related Theory 27
3.1 Beamforming and Beam–steering 28
3.1.1 An introduction to scanned array systems 28
3.1.2 The antenna 31
3.1.3 Phased arrays 36
3.1.4 Beam–steering circuits 40
3.1.4.1 RF switches 40
3.1.4.2 RF attenuators 41
3.1.4.3 RF phase shifters 41
3.2 Wireless Power Transfer (WPT) 42
3.2.1 Introduction to WPT 43
3.2.2 Classifications of WPT 44

3.2.2.1 Inductive coupling WPT 45
3.2.2.2 Resonance coupling WPT 46
3.2.2.3 Microwave Power Transfer (MPT) 46
3.2.2.4 Ambient Energy Harvesting (AEH) 47
3.2.3 Block diagram of MPT system 48
3.2.3.1 Transmit and receive antennas 48
3.2.3.2 RF rectifier 49
3.2.3.3 Matching network 51
3.2.3.4 Power conditioner 51
3.3 Communication Architectures and Protocols 53
3.3.1 Communication schemes 54
3.3.1.1 Common digital modulation schemes 54
3.3.1.2 ASK–PWM communication scheme 58
3.3.2 Multiple access techniques 61
3.3.2.1 Time Division Multiple Access (TDMA) 62
3.3.2.2 Frequency Division Multiple Access (FDMA) 62
3.3.2.3 Code Division Multiple Access (CDMA) 63
3.3.3 Data transfer protocols 64
3.3.3.1 Serial Peripheral Interface (SPI) 64
3.3.3.2 Universal Asynchronous Receiver–Transmitter (UART) 67
3.3.3.3 Inter–Integrated Circuit (I^2C) 68
3.3.3.4 ASK–PWM data transfer solution 69
3.4 Conclusion 70
Chapter 4: Control System Architecture and Simulink Modeling 73
4.1 Control System Overview 73
4.2 Control System Block Diagram 76
4.2.1 RF rectifier and PMU 78

4.2.2 ASK–PWM demodulator and decoder block 79
4.2.3 Digital frame router and DACs....81
4.3 Timing Analysis Example....86
4.4 Simulink Model and Simulations....90
4.5 Conclusion 95
Chapter 5: Synthesized Digital Control and ASK–PWM PCB Prototype....98
5.1 2×2 Subarray Digital Control Validation 99
5.2 ID–Based Control Validation in a 4×4 Array....108
5.3 ASK–PWM PCB Control and Beam–steering Demonstration....112
5.3.1 Communicating antenna characterization....114
5.3.2 ASK–PWM circuit design 117
5.3.3 Reflective phase shifter characterization 122
5.3.4 Beam–steerer characterization 128
5.3.5 Beam–steerer control system experimental results....138
5.4 Conclusion 146
Chapter 6: PCB Prototype of a Wirelessly Powered ASK–PWM Receiver 148
6.1 Wirelessly Powered ASK–PWM Receiver Specifications 149
6.2 RF Energy Rectifier Schematic Design 151
6.3 Parasitic Inductance Impact and Reduction....153
6.4 Interfacing Harvesting and Communication Rectifiers 161
6.5 Wirelessly Powered ASK–PWM Receiver Experimental Work....170
6.6 Conclusion 177
Chapter 7: Integrated Circuit Implementation of the Control Block 179
7.1 IC Specifications....180
7.2 RF Rectifier and Power Conditioning....183
7.2.1 RF rectifier design....184
7.2.2 Bandgap references....193

7.2.3 Voltage regulators 202
7.3 Communication and Digital Frame Router Blocks.....209
7.4 Low–Power Level–Shifting DAC Design 213
7.5 Sub–IC Interface Simulations.....218
7.5.1 Power management with ASK demodulator interface.....220
7.5.2 Communication with digital control interface 222
7.6 IC Testing and Debugging 224
7.6.1 Bandgap references and voltage regulators testing.....229
7.6.2 ASK demodulator testing.....232
7.6.3 PWM decoder, digital frame router and DACs testing.....236
7.6.4 RF rectifier and ASK demodulator interface testing.....239
7.6.5 IC samples testing and summary 241
7.7 Conclusion 243
Chapter 8: System–Level Validation and Proof of Concept 246
8.1 System–Level Architecture and Specifications 247
8.2 System–Level Proof–of–Concept Demonstration 251
8.3 Conclusion 264
Chapter 9: Summary of Thesis and Future Work.....266
9.1 Summary of Thesis Achievements.....266
9.2 Future Research Directions.....269
References.....271
Appendix: List of Commercial Components used in Thesis 284

List of Figures

2.1 Phased array modules from state–of–the–art literature showing the back and front panels, and the PCB layers from: (a) [47], (b) [31], (c) [33], and (d) [35]. 17
3.1 Scanned array systems showing the different techniques of: (a) mechanically scanned array and (b) AESA [10]..... 30
3.2 Block diagram of a TRM [77]..... 31
3.3 Radiation pattern of antenna array showing the difference in directivity of: (a) single antenna element, (b) two, and (c) multiple antenna elements [82]..... 37
3.4 A conceptual plot showing how linear phase progression of antenna elements can change the direction of the main lobe [83]..... 39
3.5 Plots of phased array pattern showing sidelobes tapering by changing the weighting of current excitation at each antenna element of a 5x1 array [84]. 39
3.6 Block diagram of an MPT [95]. 48
3.7 Common RF rectifier topologies: (a) series, (b) shunt, (c) voltage doubler, and (d) full–wave rectifier [95]. 50
3.8 Voltage regulator circuits: (a) linear, (b) switch–mode boost converter, and (c) switch–mode buck converter [95]..... 52
3.9 Common modulation schemes: (a) ASK, (b) OOK, (c) FSK, and (d) PSK [23]. . 55
3.10 ASK–PWM waveforms showing: (a) the modulating signal, and (b) the modulated signal [23]. 60
3.11 A basic block diagram of ASK–PWM transmitter and receiver [21]–[23]..... 61
3.12 Multiple access techniques: (a) TDMA, (b) FDMA, and (c) CDMA. 61
3.13 Typical configuration of SPI leader and multiple SPI followers [24]..... 65
3.14 Typical block diagram of an SPI [103]. 66
4.1 Proposed control system approach using wirelessly powered non–coherent ASK–PWM control system..... 74
4.2 Block diagram of the control system: (a) transmitter, and (b) the two receivers.. 77
4.3 Block diagram of the RF rectifier with power conditioners. 78
4.4 Block diagram of ASK–PWM demodulator and decoder [22]. 79

4.5 A conceptual plot of the waveforms of the ASK–PWM demodulator and decoder. 79
4.6 Digital frame router and DACs block diagram. 81
4.7 Data pattern used for decoding the control information. 83
4.8 Block diagram of the data director. 86
4.9 A conceptual plot of the waveform of the shift register. 87
4.10 Waveforms of subsequent blocks of the shift register. 88
4.11 Simulink implementation of the transmitter and ASK–PWM demodulator and decoder. 91
4.12 Waveform simulations of Simulink model of the transmitter and ASK–PWM demodulator and decoder. 93
4.13 Simulink model of the digital frame router and DACs. 94
4.14 Simulink testbench of the control system. 94
4.15 Simulink testbench simulation waveforms showing: (a) *CLK*, (b) *DATA*, (c) *ACK*, (d) *BL_ID*, (e) *CELL* outputs, and (f) DAC outputs. 96
5.1 Block diagram of the 2x2 subarray prototype. 100
5.2 Logic gate implementation of the digital PWM decoder used for the first two experimental phases. 101
5.3 Illustrative plot of the operation of the digital PWM decoder. 101
5.4 PCB for prototyping an emulated 2x2 subarray. 103
5.5 Varactor capacitance measurements using LCR meter showing: (a) test setup, and (b) testing schematic. 104
5.6 Varistor resistance measurements using Ampere meter showing: (a) test setup, and (b) testing schematic. 105
5.7 Test setup for measuring the transient waveforms of the control PCB. 105
5.8 Comparison between measurement and datasheet values in a 2x2 emulated subarray of: (a) varactors, and (b) varistors. 106
5.9 Waveform signals for the 2x2 emulated subarray prototype showing: (a) FPGA GPIO pins, and (b) varactors and varistors control voltages and their annotated controlled values. 107
5.10 Block diagram of the 4x4 array prototype. 109

5.11 PCB for prototyping an emulated 4x4 array. 110
5.12 Comparison between measured and datasheet varactor values in a 4x4 emulated array. 110
5.13 Waveform signals for the 4x4 emulated array prototype showing: (a) FPGA GPIO pins, and (b) varactors control voltages and their annotated controlled values. ..111
5.14 Block diagram of the test setup for validating wirelessly controlled ASK–PWM phased array system. 113
5.15 Panel antenna characterization setup. 115
5.16 Measured $|S_{11}|$ for TX (red) and RX (blue) panel antennas. 116
5.17 ASK demodulator circuit schematic. 117
5.18 ASK demodulator simulations showing voltage waveforms of: (a) V_{rx}, (b) V_{env} (red) and V_{avg} (blue), (c) V_{dig}, and (d) Voltage difference between V_{env} & V_{avg} during idle mode. 119
5.19 PWM decoder circuit schematic. 120
5.20 PWM decoder simulations showing voltage waveforms of: (a) V_{dig}, (b) V_{skew} (red) and V_{ref} (blue), and (c) *PRE_DATA*. 122
5.21 Schematic of reflective phase shifter [91]. 123
5.22 PCB prototype of the reflective phase shifter [Designed by Dr. Maryam Hasheminasab; experimentally validated by the author]. 124
5.23 Experimental setup of the reflective phase shifter characterization. 126
5.24 Measured $|S_{11}|$ of the reflective phase shifter across control voltages, showing individual responses (light red) and their average (dark red). 126
5.25 Measured S_{21} phase showing: (a) absolute phase, and (b) relative phase. 127
5.26 Top and Side View of a 2x4 patch antenna array [Designed by Dr. Kam Kedze]. 129
5.27 Gain simulation of the 2x4 patch array design [Courtesy of Dr. Kam Kedze]. .. 130
5.28 Radiation pattern simulations of the 2x4 patch antenna array for different phase shift configurations: $S0 \rightarrow 0°$ (red), $S1 \rightarrow 10°$ (blue), and $S2 \rightarrow 15°$ (green). .. 131
5.29 Fabricated PCB of the 2x4 beam–steerer showing: (a) top panel, and (b) bottom panel [Designed by Dr. Maryam Hasheminasab; experimentally validated by the author]. 132

5.30 Test setup of the 2x4 beam–steerer. 133
5.31 Beam–steerer measurement results showing measured $|S_{11}|$ per test state (light red), and average $|S_{11}|$ (dark red). 133
5.32 Control–room view of the anechoic chamber measurement setup: (a) overall setup including the VNA and DC bias supplies, and (b) close–up of the RJ–45 (Ethernet) bias distribution interface ("Ethernet bridge"). 135
5.33 Anechoic chamber setup showing the transmitting horn antenna, phased–array under test, and Ethernet–based DC control distribution. Insets provide detailed views of the array and bias connections. 136
5.34 Direct–DC bias beam–steering measurement results showing radiation patterns for *S0* (red), *S1* (blue), and *S2* (green) progressive phase shift states at beam–forming frequencies of: (a) 3.0 GHz, (b) 3.1 GHz, (c) 3.2 GHz, (d) 3.3 GHz, (e) 3.4 GHz, and (f) 3.5 GHz. 137
5.35 Comparison between direct DC bias control (solid) and simulation (dashed) of the 2x4 beam–steerer for different steering angle states: (a) *S0*, (b) *S1*, and (c) *S2*. 138
5.36 ASK–PWM control PCB prototype. 140
5.37 Measurement setup of the ASK–PWM control side for the beamforming experiment: (a) complete hardware setup, and (b) zoomed view of the communication–control circuitry and its interconnections. 142
5.38 Measurement waveforms of proposed ASK–PWM control system: (a) V_{env} (red) and V_{avg} (blue), (b) *CLK*, (c) V_{skew} (red) and V_{ref} (blue), (d) *PRE_DATA*, (e) control block 1 DAC outputs, and (f) control block 2 DAC outputs. 143
5.39 Comparison between measured radiation pattern of ASK–PWM control system approach (solid) and direct DC bias (dashed) of the 2x4 beam–steerer for different steering angle states: (a) *S0*, (b) *S1*, and (c) *S2*. 144
6.1 System architecture of the wirelessly powered ASK–PWM receiver for beam–steering control. 150
6.2 Voltage doubler circuit schematic. 152
6.3 Simulated S_{11} on a Smith chart using LSSP analysis, showing swept L_M for different values of C_M. 152

6.4 Simulated PCE (red) and V_{EH} (blue) as a function of P_{in} for the designed voltage doubler. 153
6.5 Output smoothness and RF feedthrough rejection of the schematic voltage doubler showing: (a) transient response, and (b) frequency response. 154
6.6 Initial PCB layout of the voltage doubler. 154
6.7 Output smoothness and RF feedthrough rejection of the voltage doubler layout in Figure 6.6 showing: (a) transient response, and (b) frequency response. 155
6.8 Modified rectifier and output filter model including parasitic inductance L_P and the segmented output capacitances. 156
6.9 PCB layout of the voltage doubler decomposing C_2 into multiple parallel branches. 157
6.10 Output smoothness and RF feedthrough rejection of the modified voltage doubler layout in Figure 6.9 showing: (a) transient response, and (b) frequency response. 157
6.11 RF output ripple $V_{RF\,OUT}$ as a function of number of shunt capacitors N (blue dashes show ripple reduction differences for two consecutive N). 158
6.12 Experimental validation of reduced inductive effects via shunt capacitive branching showing: (a) PCB implementation, and (b) Measurement setup used for characterization. 159
6.13 Comparison between co–simulated (blue dashed lines) and measured (red solid lines) rectifier performance versus input power showing: (a) V_{EH}, and (b) PCE. 159
6.14 Measured output voltage waveform (blue) of the proposed voltage doubler. 160
6.15 Interface between harvester and communication paths. 161
6.16 Simulations showing the impact of changing R_{eq} on: (a) V_{COMM}, and (b) PCE of harvesting path. 162
6.17 Proposed modified harvesting–communication interface circuit to improve isolation by adding R_M. 163
6.18 Simulations showing the impact of adding R_M while sweeping R_{eq} on: (a) V_{COMM}, and (b) PCE of harvesting path. 164
6.19 Communication rectifier included with the detailed ASK filter. 165
6.20 AC frequency response of the communication path for different values of C_3. .. 167

6.21 Transient response of the harvesting–communication interface circuit for: (a) C_3 =10 pF and (b) C_3=1000 pF. 167
6.22 PCB prototype of the harvesting–communication interface circuit. 168
6.23 Co–simulated (dashed lines) and measured (solid lines) performance of the harvesting–communication interface PCB prototype showing: (a) V_{EH} (red) and V_{COMM} (blue) vs. P_{in}, and (b) PCE as a function of P_{in}. 169
6.24 Transient response of the prototyped harvesting–communication interface PCB showing V_{EH} (yellow) and V_{COMM} (blue). 170
6.25 Circuit schematic of the proposed wirelessly powered ASK–PWM Receiver. .. 171
6.26 Wirelessly powered ASK–PWM experimental work showing: (a) printed circuit, and (b) measurement setup. 173
6.27 Waveform measurements obtained from oscilloscope showing: (a) V_{EH} (red) and V_{DDH} (blue), (b) V_{COMM}, (c) V_{ENV} (red) and V_{CM} (blue), (d) V_{SK} (red) and V_{REF} (blue), (e) V_D (red) and CLK (blue), and (f) measured distance validation. 175
7.1 Circuit schematic of the voltage doubler using diode–connected transistors. 184
7.2 Simulated PCE vs. L_M for various transistor widths W. 188
7.3 Schematic simulations of the designed diode–connected RF rectifier showing PCE (red) and V_{EH} (blue) as functions of input power P_{in}. 189
7.4 Post–layout simulations of MIM capacitors vs. frequency for different capacitance values. 190
7.5 Impact of inductor's finite on–chip Q on PCE of RF rectifier. 191
7.6 Post–layout simulations of the voltage doubler showing: (a) PCE (red) and V_{EH} (blue), and (b) $|S_{11}|$ matching simulations. 192
7.7 A CMOS only high–voltage bandgap reference. 195
7.8 A CMOS only low–voltage bandgap reference. 196
7.9 Performance of the two designed bandgap references showing: (a) temperature dependence, (b) supply dependence, (c) start–up verification, and (d) $PSRR^{-1}$ simulation. 201
7.10 Designed boosted voltage regulators: (a) high–voltage, and (b) low–voltage regulator. 206

7.11 Post–layout performance simulations of both voltage regulator designs: (a) open–loop gain and phase, (b) supply dependence, (c) start–up performance, and (d) $PSRR^{-1}$ simulations. 208
7.12 IC realization of the PWM decoder. 211
7.13 Typical schematic of a current–mode converter [25]. 214
7.14 Modified folded–resistor string 6–bit DAC. 216
7.15 Simulation comparison between typical and modified folded resistor string DACs showing: (a) V_{out} of typical design, (b) I_{DDH} of typical design, (c) V_{out} of modified design, (d) I_{DDL} (red) and I_{DDH} (blue) of modified design. 219
7.16 Output voltage of the modified folded–resistor string DAC for different switch implementations: standard (red), low threshold (green), and native (blue) transistors. 220
7.17 Testbench of the power management unit with the ASK demodulator. 221
7.18 Waveform simulations of the testbench in Figure 7.17. 223
7.19 Testbench of the communication and control blocks. 224
7.20 Waveform simulations of the testbench in Figure 7.19. 225
7.21 Micrograph of the fabricated IC in TSMC 130 nm CMOS technology, highlighting the integrated subblocks. 226
7.22 IC packaging and test boards showing: (a) the 40–lead, 6×6 mm open–cavity QFN–packaged die, (b) the test platform for power management, ASK demodulator, and PWM decoder with digital frame router and DACs, and (c) the RF test platform for rectifier and ASK demodulator characterization. 227
7.23 Experimental setup for bandgap references and voltage regulators characterization. 230
7.24 Measured (solid) and simulated (dash) PMU output voltages V_{DDH} (red), V_{DDL} (blue), and V_{COMP1} (green) as a function of input supply voltage. 230
7.25 Measured startup transient of the PMU, showing V_{DDH} and V_{DDL} as the input supply ramps to its steady–state value. 232
7.26 Experimental setup for standalone characterization of the ASK demodulator. .. 233

7.27 Waveform results of intermediate nodes in the ASK demodulator showing: (a) Measured V_{ENV} (red) and V_{CM} (blue), and (b) Simulated post–layout V_{ENV} (green) and V_{CM} (orange). 233

7.28 Comparator output CLK measurement (solid red) vs. post–layout simulation (dashed blue) at: (a) 100 kHz with improper probe loading, (b) 1 kHz with improper probe loading, (c) 100 kHz with reduced probe loading and equivalent capacitive–load model simulation, and (d) 1 kHz with reduced probe loading and equivalent capacitive–load model simulation. 235

7.29 Experimental setup for testing the PWM decoder, digital frame router, and DACs. 237

7.30 Measurement results of the PWM decoder, digital frame router, DACs showing: (a) input PWM signal applied to the IC, (b) measured DAC outputs for each phase shifter's cell, and (c) measured DAC outputs for each attenuator's cell. 238

7.31 Experimental setup for evaluating the RF rectifier and its interface with the ASK demodulator. 240

7.32 Measured rectifier output voltage under RF excitation 240

8.1 Initial system–level architecture of the proposed wirelessly powered beam–steering platform. 247

8.2 Updated proof–of–concept system architecture incorporating the practical modifications required after IC and phase shifter characterization. 249

8.3 Photograph of the fabricated proof–of–concept harvesting and control PCB panel. 252

8.4 Experimental validation setup of the proposed wirelessly powered beam–steering control system showing: (a) measurement setup, and (b) zoomed–in view of the fabricated harvesting and control PCB module during measurement. 257

8.5 Measured wireless power harvesting and regulated supply voltages of the proposed beam–steering platform showing: (a) V_{EH} (red) and V_{EHUH} (blue), and (b) measured regulated outputs showing V_{DDH} (red), V_{DDL} (blue), V_{COMP1} (green), and V_{DDUH} (orange). 259

8.6 Measured ASK–PWM envelope detection and recovered digital waveform under wireless powering conditions showing: (a) V_{ENV} (red) and V_{AVG} (blue), and (b) V_{dig}. 260

8.7 Measured transient response of the phase shifter control voltages for one row of the antenna array during wireless powering and ASK–PWM beam–steering operation, highlighting important regions. 262

8.8 Comparison between measured radiation pattern of the wirelessly powered control approach (solid) and direct DC bias (dashed) of the 2x4 beam–steerer for different steering angle states: (a) *S0*, (b) *S1*, and (c) *S2*. 263

List of Tables

3.1 Antenna specifications of common antenna types (*: Typical values) [15], [79]–[81]. 36

5.1 Comparison of control and synchronization approaches in related works 145

6.1 Comparison between conducted work and literature on wirelessly powered ASK–PWM receiver (*: receiver efficiency with regulator included). 176

7.1 Summary of measured functionality across five fabricated IC prototypes for the main subblocks (✓: fully functional, ⚠: partially functional with degraded performance, and ✗: not functional)..... 242

A.1 Commercial off–the–shelf components used throughout the thesis. 284

List of Symbols

("[X]" indicates a number)

A	Area
A_{0H}	Bit "0" Maximum amplitude level
A_{0L}	Bit "0" Minimum amplitude level
A_{1H}	Bit "1" Maximum amplitude level
A_{1L}	Bit "1" Minimum amplitude level
ACK	Acknowledgment signal
$B[X]$	Shift Register bit [X]
BER	Bit Error Rate
$BL1$	Control Block ID bit 1
$BL2$	Control Block ID bit 2
BL_ID	Cell identifier trigger bit
$BL\_ID\_S\_1$	Block ID select bit 1
$BL\_ID\_S\_2$	Block ID select bit 2
C	Count
$c(t)$	Carrier signal
C_1	Decoupling capacitor of voltage doubler
C_2	Load capacitor of voltage doubler
C_3	Decoupling capacitor of communication voltage doubler
C_4	Load capacitor of communication voltage doubler

$C_5 - C_{10}$	Filtering capacitors in three–stage voltage doubler
C_{cm}, C_{CM}	Average (common) mode capacitance
C_D	FPGA interface capacitance
C_f	Bandgap filtering capacitor
C_L	Load capacitor
C_M	Matching capacitor
C_o	Output capacitor
C_{ox}	Oxide capacitance
C_{skew}, C_{SK}	Skewing capacitor
C_v	Phase shifter varactor
$CE1$	Cell ID bit 1
$CE2$	Cell ID bit 2
$CELL[X]$	Cell [X] activation bit
$CELL[X]\_PS$	Analog control voltage for phase shifter's cell [X]
CLK	Extracted clock
D	Directivity
d	Largest antenna dimension
D_1	Series diode of voltage doubler
D_2	Shunt diode of voltage doubler
D_3	Series diode of communication voltage doubler
D_4	Shunt diode of communication voltage doubler
$D_5 - D_{10}$	Diodes in three–stage voltage doubler

$d_{[X]}$	Digital control bit [X] for current–steering DAC
D_c	Duty cycle
d_c	Duty cycle parameter
$DATA$	Extracted PWM data after synchronization
dl	Segment length
$EIRP$	Effective Isotropic Radiated Power
f	Frequency
f_0	Resonance frequency
f_b	Bit rate
f_c	Carrier frequency
$G_{d,max}$	Maximum directive gain
G_r	Receive antenna gain
G_t	Transmit antenna gain
$I_{D[X]}$	Drain current of transistor [X]
I_0	Antenna element current
I_{DDH}	2.6 V supply voltage DAC current
I_{DDL}	0.75 V supply voltage DAC current
I_L	Load current
I_s	Process–dependent current
K	Integrator gain
k	Summation index

$K_{[X]}$	Device transconductance parameter of transistor [X]
k_b	Boltzmann constant
$L(s)$	Loop–gain
$L_{[X]}$	Length of transistor [X]
L_M, L_{in}	Matching inductor
L_p	Parasitic inductor
L_s	Phase shifter resonance inductor
$m_0(t)$	Bit ”0” modulation
$m_1(t)$	Bit “1” modulation
$M_{[X]}, Q_{[X]}$	Transistor [X]
N	Number of shunt capacitive elements
P_{dyn}	Dynamic power consumption
P_{in}	Input power
P_r	Received power
P_{rad}	Radiated power
P_t	Transmitter power
PCE	Power Conversion Efficiency
PLL_CLK	FPGA’s divided PLL clock
PRE_DATA, V_D	Extracted PWM data before synchronization
$PS[X]$	Phase shifter control bit [X]
$PSRR$	Power Supply Rejection Ratio

Q	Quality factor
q	Electron charge
r	Separation distance between elements
$R_{H[X]}$	Voltage divider resistor [X] for high–voltage regulator
$R_{L[X]}$	Voltage divider resistors [X] for low–voltage regulator
R_0	Source resistance
R_1	First part of voltage doubler resistive divider
R_2	Second part of voltage doubler resistive divider
R_{cm}, R_{CM}	Second part of dynamic reference generator resistive divider
R_{div}, R_{DIV}	First part of dynamic reference generator resistive divider
R_{eq}	Load resistance of communication voltage doubler
R_f	Bandgap filtering resistor
R_L	Load resistance
R_M	Isolating resistor
R_{on}	On–channel resistance
R_p	Phase shifter resistor
R_{rad}	Radiated resistance
R_{ref}	Reference resistance
R_{skew}, R_{SK}	Skewing resistor
RCD	Record signal
RCD_D	Delayed record signal

RST	Reset signal
s	Complex frequency
$S0$	Progressive phase configuration of 0° steering angle
$S1$	Progressive phase configuration of 10° steering angle
$S2$	Progressive phase configuration of 15° steering angle
S_{11}	Input reflection coefficient
S_{21}	Forward transmission coefficient
S_{22}	Output reflection coefficient
SER	Sample Error Rate
SNR	Signal–to–Noise Ratio
T	Absolute temperature
V_{DDH}	Regulated high supply voltage
V_{DDL}	Regulated low supply voltage
$V_{GS[X]}$	Gate–to–source voltage of transistor [X]
$V_{RF\ OUT}$	Output RF ripple voltage
V_{avg}, V_{CM}	Average of envelope (common–mode) voltage
V_{BE}	Base–Emitter voltage
V_{COMM}	Communication voltage
V_{COMP1}	0.5 V comparator reference voltage
V_{COMP2}	0.3 V comparator reference voltage
V_{DD}	Supply voltage

V_{DDUH}	Regulated ultra–high supply voltage
V_{dig}, V_{DIG}	Digital pulse signal
V_{EH}	Harvested voltage
V_{EHUH}	Ultra–high harvested voltage
V_{env}, V_{ENV}	Envelope voltage
V_{IN}	ASK demodulator input
V_{out}	DAC output voltage
V_{ref}, V_{REF}	Reference voltage
V_{REFH}	High–reference output voltage
V_{REFL}	Low–reference output voltage
V_{REG}	Regulated voltage
V_{RS}	Resonance voltage node
V_{rx}, V_{RX}	Received modulated RF voltage
V_{skew}, V_{SK}	Skewed voltage
V_T	Thermal voltage
V_{TH}	Transistor's threshold voltage
V_{TH0}	Transistor's threshold voltage extrapolated to 0 K
$VSWR$	Voltage Standing Wave Ratio
W	Transistor's width
$W_{[X]}$	Width of transistor [X]
W_f	Transistor's finger width

$y(t)$	ASK–PWM modulated signal
$\left\vert \vec{u} \cdot \vec{v} \right\vert$	Polarization factor product
α	Multipath propagation factor
η	Subthreshold slope factor
η_r	Receive radiation efficiency
η_t	Transmit radiation efficiency
λ	Wavelength
μ_n	Electron mobility
τ_1	Voltage doubler high–pass time constant
τ_2	Voltage doubler low–pass time constant
τ_3	Dynamic reference generator time constant
τ_4	Skewing time constant

List of Abbreviations

("[X]" indicates a number)

5G	Fifth Generation
6G	Sixth Generation
AC	Alternating Current
ADC	Analog–to–Digital Converter
ADS	Advanced Design System
AEH	Ambient energy harvesting
AESA	Active Electronically Scanned Array
Amp	Differential Amplifier
ASK	Amplitude–Shift Keying
ASK–PWM	Amplitude–Shift Keying with Pulse–Width Modulation
AT	Attenuator
BiCMOS	Bipolar Complementary Metal–Oxide–Semiconductor
BJT	Bipolar Junction Transistor
CAD	Computer–Aided Design
CDMA	Code Division Multiple Access
CMOS	Complementary Metal–Oxide–Semiconductor
Comp	Comparator
$COMP_{[X]}$	Comparator [X]
CS	Chip Select
CTS	Clear–to–send

DAC	Digital–to–Analog Converter
DC	Direct Current
DDS	Direct Digital Synthesis
DPSK	Differential Phase–Shift Keying
E–field	Electrical Field
EM	Electromagnetic
FCC	Federal Communications Commission
FDMA	Frequency Division Multiple Access
FET	Field–Effect Transistor
FMCW	Frequency–Modulated Continuous Wave
FPGA	Field Programmable Gate Array
FR–4	Flame Retardant Type–4
FSK	Frequency–Shift Keying
FSM	Finite State Machine
FSS	Frequency–Selective Surfaces
Ge	Germanium
GFSK	Gaussian–Filtered Frequency–Shift Keying
GND	Ground
GPIO	General–Purpose Input/Output
HDL	Hardware Description Language
H–field	Magnetic Field
HV	High–Voltage

I/Q	In–band/Quadrature
I^2C	Inter–Integrated Circuit
IC	Integrated Circuit
ICMR	Input Common–Mode Range
ID	Identifier, Identification
IF	Intermediate Frequency
IMU	Inertial Measurement Unit
IPTAT	Inverse proportional to absolute temperature
ISM	Industrial, Scientific, and Medical
KVL	Kirchhoff's Voltage Law
LC	Inductor–Capacitor
LCR	Inductor–Capacitor–Resistor
LDO	Low–dropout
LNA	Low Noise Amplifier
LO	Local Oscillator
LSSP	Large–Signal S–Parameter
LV	Low–Voltage
LVT	Low–Voltage–Threshold
MCU	Micro–Controller Unit
MIM	Metal–Insulator–Metal
MISO	Master–In Slave–Out
MOSI	Master–Out Slave–In

MPT	Microwave Power Transfer
MSB	Most significant bit
n^+	Heavily n–doped
NI	National Instruments
NMOS	N–doped Metal–Oxide–Semiconductor
NRZ	Non–return–to–zero
OFDMA	Orthogonal Frequency Division Multiple Access
OOK	ON–OFF Keying
Op Amp	Operational Amplifier
p^+	Heavily p–doped
PA	Power Amplifier
PCB	Printed Circuit Board
PIN	P–doped–Insulator–N–doped
PLL	Phase–Locked Loop
PMOS	P–doped Metal–Oxide–Semiconductor
PMU	Power Management Unit
PNA	Performance Network Analyzer
PNP	P–N–P–doped
PS	Phase Shifter
PSK	Phase–Shift Keying
PSS	Periodic Steady–State
PTAT	Proportional to absolute temperature

PVT	Process, Voltage, Temperature
PWM	Pulse–Width Modulation
QFN	Quad Flat No–leads
Radar	Radio Detection and Ranging
RC	Resistor–Capacitor
Rectenna	Rectifying antenna
REG	Regulator
RF	Radio Frequency
RHCP	Right–hand circularly polarized
ROM	Read–only memory
RTS	Request–to–send
Rx	Receive, Receiver
RZ	Return–to–zero
SCK	Serial Clock
SCL	Serial Clock Line
SCMA	Sparse Code Multiple Access
SDA	Serial Data Line
SDR	Software Defined Radio
SiGe	Silicon Germanium
SMA	SubMiniature version A
SMD	Surface Mount Device
SoC	System–on–Chip

SOT	Short–Open–Thru
S–parameters	Scattered parameters
SPDT	Single–Pole Double–Throw
SPI	Serial Peripheral Interface
SPST	Single–Pole Single–Throw
SRAM	Static Random–Access–Memory
SRF	Self–Resonance Frequency
SWIPT	Simultaneous Wireless Information and Power Transfer
TDMA	Time Division Multiple Access
TRM	Transmit/Receive Module
TSMC	Taiwan Semiconductor Manufacturing Company
Tx	Transmit, Transmitter
UART	Universal Asynchronous Receiver–Transmitter
USB	Universal Serial Bus
USRP	Universal Software Radio Peripheral
VGA	Variable Gain Amplifier
VHDL	VHSIC Hardware Description Language
VHSIC	Very High–Speed Integrated Circuit
VNA	Vector Network Analyzer
VWF	Vector Waveform File
WPT	Wireless Power Transfer
WSN	Wireless Sensor Node

Chapter 1: Introduction

1.1 Research Motivation

Beamforming and beam–steering are fundamental techniques in modern communication systems, with widespread applications in satellite and wireless communications, radar, sonar, military, and space systems [1]–[9]. Beamforming primarily concerns the architectural arrangement of radiating antenna elements and their associated control blocks, whereas beam–steering refers to the circuitry responsible for controlling the direction of the radiated beam [10]. In these applications, a beamforming system must generate a high–signal–strength beam suitable for long–distance transmission and reception, while enabling precise control of the main beam direction and minimizing sidelobe levels [10], [11].

Beam formation is achieved by exciting antenna elements with Radio Frequency (RF) signals, while beam–steering can be realized either mechanically or electronically. Electronic beam–steering is commonly implemented using RF beam–steering circuits such as RF switches, RF attenuators, and RF phase shifters [11], [12]. Meeting demanding beamforming requirements such as high gain, high directivity, low sidelobes, and high signal–to–noise ratio is fundamentally infeasible with a single antenna element. As a result, antenna arrays are employed to enhance achievable gain and directivity [11], [13].

In phased–array systems, beam direction is controlled by introducing phase shifts in the RF signals applied to individual antenna elements [10]. Additionally, RF attenuators may be incorporated at each element to taper sidelobes and improve radiation pattern characteristics [10]. The control of beam–steering circuitry can be broadly classified into uniform and non–uniform schemes. In uniform control, identical or near–identical control voltages are applied across most or all elements, simplifying the control architecture at the expense of reduced flexibility and performance. In contrast, non–uniform control assigns independent control voltages to each beam–steering element, enabling superior system performance but at the cost of increased routing complexity and a larger number of control signals [14]. Furthermore, control architectures may be implemented globally, where a

single control system manages the entire array, or in a segmented manner, where multiple control blocks independently manage subsets of the beam–steering circuitry.

To keep pace with the increasing performance demands of these applications, phased–array systems must achieve higher gain and directivity, both of which can be obtained by increasing the number of antenna elements in the array [15]. However, as more elements are integrated within a physically constrained area, the available space for power and clock distribution, and control–signal routing associated with the beam–steering circuitry is significantly reduced. Moreover, the routing of additional power, clock, and control lines consumes increasing area as the array scales in size. These constraints make it increasingly difficult to scale phased arrays to achieve the desired performance.

One possible mitigation is the use of uniform control schemes, as previously discussed; however, this approach severely limits array flexibility and overall performance, while failing to fundamentally address the challenges of power distribution and control routing. Although adding additional routing layers could provide more routing area, this solution is often cost–prohibitive and results in increased physical size. Furthermore, the added interconnect complexity introduces parasitic and propagation effects that can degrade radiation performance and limit the maximum operating frequency of the system [16]–[18].

1.2 Problem Statement and Research Question

Large–scale phased–array beamforming systems require dense networks of power and control interconnects: wired power rails, clock–distribution networks, possible on–chip Phase–Locked Loops (PLLs), and high–density digital buses using Serial Peripheral Interface (SPI) to configure individual element control blocks [11], [18]–[20]. These wired infrastructures create severe practical problems as array size grows: complex multi–layer routing, many power–feeding and I/O pins, increased parasitic coupling, and layout and/or Printed Circuit Board (PCB) cost that limit achievable element density and modular scalability [11], [18]–[20].

The central technical gap is the lack of a simultaneously combined power, clock and control transfer that can achieve the following:

(a) removing wired power feeds and on–board batteries,

(b) eliminating the need for distributed clock/PLL/SPI infrastructure at the receiver,

(c) enabling independent, addressable configuration of control blocks.

This leads to the following research question:

*Can a **completely wireless** beam–steering control architecture be designed to replace conventional **wired** power, clock, and control distribution networks while preserving the accuracy, latency, and robustness required for practical phased–array systems?*

This research question advocates a fundamental transition from the conventional wired distribution of power, clock, and control signals toward a wireless alternative for beam–steering control architectures. Such a wireless distribution approach offers several compelling advantages. By eliminating dedicated power routing networks and external feeding pins through Wireless Power Transfer (WPT), power can be locally generated at each control block using integrated miniaturized antennas. This distributed harvesting approach significantly reduces metal congestion, routing overhead, and power delivery constraints across the array.

Similarly, wirelessly delivered control information removes the need for long wired buses and serial interfaces, thereby reducing routing complexity, parasitic loading, and electromagnetic coupling between packed interconnects and antenna elements. In addition, enabling local clock recovery within each control block without explicit clock routing or PLLs eliminates distributed clock lines for the control blocks. This allows each control block to operate independently, removing the need for centralized SPI–style communication and simplifying synchronization across the array.

Collectively, transitioning from wired to wireless distribution has the potential to eliminate dedicated power, clock, and control routing networks as well as their associated feeding pins. This substantially simplifies the physical design of large–scale phased arrays while improving modularity, scalability, and integration flexibility.

1.3 Research Objectives

While the transition from wired to wireless distribution addresses many of the structural limitations of conventional beam–steering control architectures, it also introduces a new set of objectives that must be carefully addressed, which are discussed below.

- **Ultra–Low–Power System and IC Architecture for Simultaneous Wireless Power and Control:** Develop a compact, low–power control Integrated Circuit (IC) incorporating energy harvesting, communication demodulation, data decoding, digital frame routing, and local control to support dense phased–array integration while eliminating conventional power, data, clock, and feeding connections. The architecture should provide a low–cost and scalable solution for large arrays, while addressing the reduced RF WPT efficiency associated with the lossy silicon substrate of Complementary Metal–Oxide–Semiconductor (CMOS) technologies.
- **Single–Pad RF Interface for Power, Data & Clock:** Develop a single RF input that simultaneously provides wireless power, clock recovery, and control–data transfer while minimizing interconnects, power, and area. The approach requires co–design of WPT and communication while addressing their interaction and interference [21], [22], non–coherent clock–recovery limitations [23], and the additional connections required by conventional SPI interfaces [24].
- **Output Pad Count Reduction:** Reduce the output pad count between each control IC and its corresponding attenuator or phase shifter by locally converting the parallel digital control word into a single analog signal using an ultra–low–power Digital–to–Analog Converter (DAC). This approach must maintain the WPT power budget while supporting a low–cost, scalable beam–steering implementation with adequate phase resolution, linearity, and loss performance.
- **Low–Voltage Digital to High–Voltage Control Interface**: Address the voltage–domain mismatch between sub–1 V digital logic and the higher control voltages required by RF phase shifters. Efficient level shifting and/or voltage–

boosting techniques must therefore be developed to generate the required analog control voltage while maintaining low power consumption compatible with WPT constraints.

- **Ultra–Low–Power and On–Chip Voltage References and Regulations:** Develop compact, ultra–low–power voltage references and regulators to support the multiple voltage domains required within the WPT–powered IC. CMOS–only reference architectures must be investigated as conventional CMOS Bipolar Junction Transistors (BJTs) can exhibit lower current gain, higher resistance, poorer matching, and greater process dependence than vertical BJTs [25], [26]. In addition, suitable regulation strategies must balance efficiency, area, dropout, Power Supply Rejection Ratio (*PSRR*), load regulation, and stability under strict power and area constraints [27]. Achieving stable, low–dropout, regulation across multiple voltage domains under strict power and area constraints constitutes a critical system–level design challenge.
- **Synthesizable Digital Frame Routing for Non–Coherent Demodulation:** Develop a synthesizable digital frame router capable of reliably decoding and synchronizing the non–coherent data and recovered clock signals. The design must address timing variations such as jitter, duty–cycle distortion, and data–dependent timing while maintaining reliable synchronization and well–defined clock–domain operation within a standard digital design flow.
- **PCB–Level Prototyping and Validation:** Develop and validate a PCB implementation of the proposed wireless control architecture while addressing the RF non–idealities introduced by FR–4 substrates, including dielectric loss, impedance mismatch, and reduced WPT efficiency. The implementation must also mitigate RF leakage between the harvesting and communication paths and demonstrate practical decoding of the proposed dual–modulation non–coherent scheme at the PCB level.

1.4 Proposed Research Solutions

To address the limitations of conventional wired beam–steering control architectures, a fully wireless system approach is proposed and realized. The central idea is to unify WPT with a dual–modulation non–coherent Amplitude–Shift Keying with Pulse–Width Modulation (ASK–PWM) scheme to simultaneously deliver power, control data, and timing information to distributed control ICs embedded within a phased–array module. By radiating both energy, clock, and control information, the proposed architecture eliminates the need for wired power distribution, external supply rails, clock routing networks, and SPI–based digital control buses.

In this approach, each control unit operates as an independently addressable wireless node. RF energy received through a single antenna interface is rectified and regulated on–chip to power the entire control circuitry. Concurrently, the superimposed ASK–PWM modulation enables asynchronous extraction of control data and timing information without requiring a local oscillator or an on–chip PLL for clock recovery. Eliminating the need for a receiver PLL reduces on–chip circuitry and power overhead. Separately, because control frames are decoded asynchronously and include per–cell addressing, there is no reliance on a shared synchronous bus (e.g., SPI), removing the need for external clock/data lines, shared digital buses, and the associated board–level routing and feed pins. Embedded control–block and Cell–Identification (ID) logic lets each IC independently determine whether a received frame is intended for one of its attenuators and phase shifters, further obviating wired SPI interfaces.

To physically realize the proposed architecture, a compact control IC was designed, fabricated, and experimentally validated in a 130 nm Taiwan Semiconductor Manufacturing Company (TSMC) CMOS process. The design emphasizes low cost, ultra–low power operation, and small form–factor to enable dense integration within phased–array antenna modules. The IC integrates an RF rectifier, a Power Management Unit (PMU), a non–coherent ASK–PWM demodulator and decoder, a synthesizable digital frame router, and ultra–low–power DACs for attenuator and phase shifter control. All circuit blocks were co–optimized to operate under strict WPT constraints.

Special attention was given to minimizing power consumption across both analog and digital domains. A CMOS–only bandgap reference consuming less than 30 μW was implemented to provide stable biasing without external components. A low–dropout regulator utilizing native N–doped MOS (NMOS) devices ensures efficient voltage regulation under low–voltage operation. Within the DAC architecture, a slewed comparator interface was introduced between the low–voltage digital logic and the switchable resistive network generating the higher–voltage analog control signal. This approach reduces dynamic switching losses while maintaining the voltage control range required by the phase shifters.

To reduce output pad count and simplify array integration, a 6–bit ultra–low–power DAC architecture was adopted, enabling a single analog control line per beam–steering circuit. The selected analog phase shifter topology is a reflective architecture based on hybrid couplers, which can be implemented cost–effectively on FR–4 substrates. This choice supports low–cost scalability while preserving beam–steering functionality.

Because the proposed ASK–PWM scheme is non–coherent and asynchronous, careful synchronization strategies were required. A synthesizable delay–buffer cascade was developed to generate the necessary timing alignment for digital frame routing and PWM decoding. During Field Programmable Gate Array (FPGA) prototyping, synthesis constraints were applied to preserve these delay elements from optimization, enabling practical validation of the timing scheme.

System–level feasibility was further validated through PCB prototypes. Several practical challenges were addressed to ensure co–existence of WPT and ASK–PWM. RF leakage was mitigated by appropriately shunting rectifier load capacitors, while a controlled lossy resistor was introduced in the communication branch to isolate the harvesting path and preserve rectifier Power Conversion Efficiency (PCE). A configurable PWM decoding scheme was implemented at the PCB level to allow timing skew adjustment.

Collectively, the proposed architecture demonstrates that radiated power and asynchronous dual–modulation control can replace conventional wired power, clock, and digital interfaces in phased–array beam–steering systems. By eliminating power routing

networks, clock distribution trees, PLLs, and SPI buses, the architecture significantly reduces interconnect density, feed–pin count, and routing congestion. This simplification enhances scalability for large arrays while enabling compact, independently addressable control ICs suitable for dense antenna integration.

1.5 Research Contributions

This work designs, implements, and validates a wirelessly powered, non–coherent ASK–PWM control architecture that provides independent analog control to eight RF phase shifters in a 2 × 4 phased–array antenna. The contributions of this thesis address the key architectural, circuit–level, implementation, and integration challenges associated with replacing conventional wired power and control distribution with a wireless interface. The original contributions of the thesis are:

- **Unified Wirelessly–Powered Control Architecture for Phased Arrays:** A wireless control architecture was developed that combines WPT with non–coherent ASK–PWM communication to simultaneously provide power, timing, and control information to distributed beam–steering control blocks. The contribution lies in the integration of these functions within a common wireless interface, enabling distributed control nodes to operate without dedicated wired power, clock, and SPI connections. This provides a system–level approach to reducing interconnect complexity and potentially increasing the scalability of phased–array control.
- **Single–Pad RF Interface and Addressing Scheme:** A single–input RF interface was developed to allow each control node to receive the wireless power and ASK–PWM control signal through a common input. Per–chip and per–cell identification mechanisms have been incorporated to enable independent addressing of distributed beam–steering elements without relying on a shared SPI–based control bus. The combination of a single–input interface and local addressing enables distributed control nodes to operate independently while maintaining a minimal external interface.

- **Practical PCB Demonstration of a Wirelessly Powered ASK–PWM Receiver on FR–4 Substrate:** A practical FR–4 PCB implementation of the wirelessly powered ASK–PWM receiver was developed and experimentally validated. This work demonstrated that the proposed dual–function wireless link can be implemented outside of an idealized or fully integrated IC environment, where PCB substrate loss, parasitic coupling, RF leakage, and limited component integration introduce significant nonidealities. The implementation therefore provides practical validation of the proposed architecture and establishes the circuit and layout considerations required for its realization at the PCB level.
- **RF Isolation and Leakage Mitigation Techniques for Coexisting WPT and ASK–PWM:** Circuit and PCB–level techniques were developed to enable simultaneous wireless power transfer and ASK–PWM communication while limiting interference between the harvesting and communication paths. These techniques include parallel shunting of rectifier load capacitors to reduce RF leakage at the rectifier output and the use of a controlled lossy series resistance in the communication branch to isolate the two paths.
- **PCB–Feasible Skewed Buffer Design for PWM Decoding:** A skewed–buffer architecture was developed to provide the controlled timing skew required for PWM decoding in the proposed non–coherent receiver. In conventional IC implementations, the buffer skew can be adjusted through transistor sizing, providing direct control over the relative propagation delays. This flexibility is not available in a PCB implementation, where discrete devices have fixed characteristics. This work therefore developed a practical PCB–compatible approach for realizing and adjusting the required buffer skew, enabling reliable PWM decoding without relying on transistor–level sizing.
- **Synthesizable, PLL–Free Synchronization and Frame Routing Enabling the ASK–PWM Interface:** A low–overhead synchronization and frame–routing architecture was developed to support non–coherent ASK–PWM communication without an on–chip PLL or a globally distributed clock. Cascaded delay buffers have been used to establish the required timing

relationship for PWM decoding and frame synchronization, while the digital frame router performs address recognition and control–data routing.

- **IC Realization and Validation of the Control Node in TSMC 130 nm CMOS–on–Silicon:** A compact control IC was designed and fabricated in a 130–nm CMOS process, integrating the major functions required by the proposed wirelessly powered control node, including power management, non–coherent ASK–PWM demodulation and decoding, digital frame routing, and DAC–based analog control. The contribution lies in translating the proposed system architecture and supporting circuit techniques into an integrated implementation under strict power, voltage, and area constraints.
- **Slewed–Comparator–Based DAC Architecture for Low–Power Analog Phase Control:** A 6–bit DAC architecture was developed to convert the low–voltage digital control information generated by the frame router into the higher–voltage analog control signal required by the RF phase shifters. Slewed comparators have been used as the interface between the low–voltage digital domain and the higher–voltage analog output stage, providing voltage translation while reducing dynamic power consumption.

Collectively, these contributions establish a practical and scalable framework for wirelessly powered and asynchronously controlled phased–array systems. By unifying WPT, non–coherent ASK–PWM signaling, synthesizable digital frame routing, and low–power analog control within a compact IC platform, this work demonstrated that conventional wired power, clock, and SPI infrastructures can be fundamentally restructured. The proposed architecture reduces routing density, feed–pin count, and PCB complexity while preserving precise analog beam–steering capability. The multi–level validation, spanning circuit design, FPGA prototyping, PCB demonstration, and IC realization, confirmed both feasibility and practical implementation. This foundation enables scalable control segmentation for larger arrays and opens a pathway toward highly integrated, low–cost beam–steering modules.

In this work, the primary focus is placed on the development and validation of the proposed circuitry and integrated system architecture. However, due to the

multidisciplinary scope of the beam–steering platform, collaboration was required for the realization of the complete system. Dr. Maryam Hasheminasab contributed to the layout design of the phase shifter and beam–steering subsystems, while Dr. Kam Kedze contributed to the patch antenna layout design. Dr. Abdullah Al Mohaimeed provided valuable advice and guidance on the wireless power transfer aspects of the system. Their contributions supported the integration and evaluation of the overall beam–steering platform.

1.6 Research Publications

[1] M. Al Sabbagh, R. E. Amaya, M. C. E. Yagoub, and A. M. Almohaimeed, "Overcoming printed circuit board limitations in an energy harvester with amplitude shift keying and pulse width modulation communication decoder using practical design solutions," *Electronics*, vol. 14, no. 3, Art. no. 485, Jan. 2025, doi: 10.3390/electronics14030485.

[2] M. Al Sabbagh, M. Hasheminasab, K. Kedze, A. M. Almohaimeed, M. C. E. Yagoub, and R. E. Amaya, "A wireless non–coherent ASK–PWM decoded beam–steering control system using hybrid PCB/FPGA implementation," *J. of Electr. and Comput. Eng.*, manuscript submitted for publication, Jul. 2026.

[3] M. Al Sabbagh, M. Hasheminasab, K. Kedze, A. M. Almohaimeed, M. C. E. Yagoub, and R. E. Amaya, "A one–input–pin wireless interface using WPT and ASK–PWM for simultaneous power, clock, and data delivery in phased–array control," manuscript to be submitted.

1.7 Thesis Outline

This thesis is organized into nine chapters. Chapter 2 presents a review of the state of the art in phased–array beam–steering control, wireless power transfer, and non–coherent communication, identifying the limitations of existing approaches and motivating the proposed architecture.

Chapter 3 presents the theoretical and technical background relevant to the proposed system, including phased–array beamforming and beam–steering, wireless power transfer, and communication techniques.

Chapter 4 introduces the proposed wirelessly powered ASK–PWM beam–steering control architecture and describes its system–level operation, including the wireless power, communication, addressing, and digital control mechanisms.

Chapter 5 presents the initial hardware validation of the proposed architecture through PCB and FPGA implementations, focusing on the digital control framework and ASK–PWM communication prior to the integration of WPT. The validated control system is then integrated with the phased–array beam–steering system to demonstrate its operation.

Chapter 6 focuses on the integration of WPT and ASK–PWM communication at the PCB level. The design and experimental validation of the self–powered receiver are presented, including techniques developed to enable their co–existence.

Chapter 7 presents the design, fabrication, and characterization of the proposed 130–nm CMOS control IC, including the integrated power management, communication, digital control, and DAC circuitry.

Chapter 8 presents the system–level proof–of–concept implementation of the proposed wirelessly powered beam–steering architecture. The chapter describes the practical integration of the developed circuitry and presents experimental results demonstrating wireless power delivery, ASK–PWM communication, beam–steering control, and phased–array beam–steering.

Chapter 9 concludes the thesis by summarizing the major findings and contributions and discussing directions for future research.

Chapter 2: State–of–the–Art Literature Review

Given the multidisciplinary nature of the proposed architecture, the literature review is organized into three focused sections. The first section examines the routing and feeding challenges in large–scale phased arrays, with emphasis on power distribution, clock generation and routing, and serial data interconnects. These wired infrastructures introduce metal congestion, parasitic loading, electromagnetic coupling, and a large number of feeding pins, all of which fundamentally limit scalability and dense integration.

The second section reviews existing phased–array control architectures and highlights the absence of the dual–modulated non–coherent ASK–PWM scheme for beam–steering control. While conventional systems rely on SPI–based data and clock transfer, the use of an ASK–PWM for distributed control has not been explored for phased array systems.

The third section investigates prior work on WPT and ASK–PWM based systems, demonstrating that ASK–PWM receiver–based WPT combined with control decoding has not previously been prototyped on PCB for phased–array applications. This gap further motivates the experimental validation presented later in this thesis.

2.1 Power and Information Routing Issues in Phased Array Systems

One of the most critical challenges in the realization of phased–array systems is the extensive routing required for supply, digital control, and SPI interconnects [11], [18]–[20]. As the number of antenna elements increases, the associated power, bias, and control lines grow proportionally, leading to significant routing congestion. In addition to on–board interconnect complexity, the implementation of feeding terminals for supply, clock, and digital control signals further occupies a considerable portion of the phased–array module area, thereby limiting scalability and integration density.

The work in [18] highlights that phased–array performance is not only determined by RF circuitry, but is also strongly influenced by the feeding networks for bias and supply lines, as well as by the parasitic effects of interconnects. It further emphasizes the need for improved integration between antenna elements and their associated electronic circuitry to

meet the stringent requirements of emerging Sixth Generation (6G) systems. Several reported phased–array implementations demonstrate that digital signal and power routing can consume a substantial fraction of the PCB area and even contribute significantly to module thickness.

A review of the state–of–the–art reveals that most phased–array architectures segment the control system into multiple ICs responsible for beamforming control. However, these architectures still rely on conventional wired distribution of power, clock, and digital control signals, resulting in non–uniform control complexity and persistent routing overhead. In this section, recent phased–array implementations are examined to illustrate the limitations of classical power and data routing and feeding approaches. The discussion motivates the use of WPT with ASK–PWM as a potential solution to mitigate routing congestion, reduce feeding terminals, and enable more scalable and densely integrated phased–array systems.

Starting with the work in [28], a phased–array architecture implemented in Silicon Germanium (SiGe) Bipolar CMOS (BiCMOS) technology was presented. The array size was 4×8, where each chip controlled a 2×2 subarray. Out of four PCB layers, two were dedicated to control and bias distribution. The feed connector was located at the corner of the back panel and consisted of 14 pins, occupying valuable board area.

In [29], 64–element and 128–element phased arrays were demonstrated using multilayer PCBs and multiple SiGe chips, each controlling 2×2 subarrays. Space was reserved for Direct Current (DC) and RF routing as well as chip placement. SPI was again used to control the phase of each channel. Digital signal and power routing required three PCB layers.

A multiband phased–array design for Fifth Generation (5G) applications was reported in [30]. The array consisted of eight elements, where each SiGe BiCMOS chip controlled a 4×1 subarray. Similar to previous designs, an 8×2 connector was mounted on the panel for bias and SPI connections, consuming additional area.

In [31], a 256–element phased–array receiver was presented. The system employed 64 SiGe BiCMOS receiver chips, each controlling a 2×2 subarray. The implementation used

a 12–layer PCB, with five layers dedicated to RF, DC, and SPI routing. Due to the large number of elements, the feeding–pin count was substantial: 68 pins were required to provide control, supply, and SPI clocks.

The work in [19] demonstrated a 16–element phased–array beamformer capable of generating two beams. The digital control system comprised 226 digital lines, 32 analog lines, and 98 power lines. The authors described the routing as complex and challenging, necessitating the use of a multilayer PCB. Furthermore, control and power were provided by an external PCB, which was noted as impractical for the intended space applications.

In [32], a 40×40 phased–array module utilized SiGe chips to control each 2×2 subarray. A photograph of the brick–style module showed two DC and digital connectors positioned near the center of the board, with a total pin count of 80.

The papers in [20], [33] presented a 24–29.5 GHz, 256–element phased–array controlled by 2×2 beamforming chips in SiGe BiCMOS technology. A 12–layer PCB was used, with three layers dedicated to power and control routing. On the back panel, 92 pins were used for digital and supply connectivity. The authors emphasized that a sufficient number of PCB layers is essential for reliable IC interconnection.

A tile–based phased array for smart–skin applications was developed in [34], where 2×2 chips controlled 8–element subarrays, resulting in a total of 32 elements. To enable flexible implementation, only a single PCB layer was used. However, each 2×2 chip required seven pads at each PCB corner for supply and SPI connections, amounting to 28 pads per chip. Consequently, for 32 elements, a total of 112 connection pads were required, in addition to the associated supply and digital routing complexity.

Another design with fewer PCB layers was reported in [35]. In the proposed 64–element phased array, chips controlling 2×2 subarrays were used for beamforming and beam–steering. Only four PCB layers were implemented, three of which were dedicated to digital, SPI, and supply routing. Nevertheless, routing had to be implemented around both the antennas and the chips due to the large number of required connections. The design also used 20 pins for supply and digital feeds.

Similar approaches are reported in [17], [36]–[47], where empty areas were left along the PCB edges to accommodate SPI pins on the back panel. These designs relied on multiple layers for supply, digital, and SPI clock routing, utilized large header pins for connectivity, and allocated a significant portion of the PCB area to routing infrastructure.

Figure 2.1 illustrates four of the discussed phased–array modules, showing both the front and back panels as well as the PCB layer stacks. Blue rectangles are drawn to highlight key areas. The highlights on the back panels indicate the large number of feeding pins used for digital, supply, and SPI connections, while the highlights on the PCB stack–ups show the layers dedicated to digital, supply, and SPI routing.

Several key observations can be drawn from this comprehensive state–of–the–art review. First, supply and SPI routing occupy a substantial portion of phased–array modules. In most reported implementations, between three and five PCB layers are dedicated to power and control routing, significantly increasing fabrication complexity and manufacturing cost.

Although some designs reduced the number of PCB layers, as shown in [34], [35], a considerable portion of the routing was instead relocated to the front and back panels of the phased–array module. While this approach reduces stack–up complexity, it consumes valuable surface area, increases susceptibility to digital switching noise coupling into RF paths, and limits the available space for array scalability. This effect is clearly illustrated in **Figure 2.1**(d), where routing traces are visibly distributed across both panels of the module.

In all reviewed works, feeding pins were required to deliver supply voltages and digital/SPI signals. The number of these pins scales with the number of array elements, thereby consuming increasing board area as the array grows. Supply pins are required to power the control and beamforming chips, while digital pins are necessary for transmitting control data. Furthermore, SPI communication requires four signal lines per interface due to its synchronous data transfer nature. As the array size increases, the number of SPI interfaces and associated pins increases accordingly [24], [28], [41], [48], [49]. In addition, each control chip typically operates as an SPI follower controlled by a leader device, further increasing routing density and interconnect overhead [24], [28], [41], [48], [49].

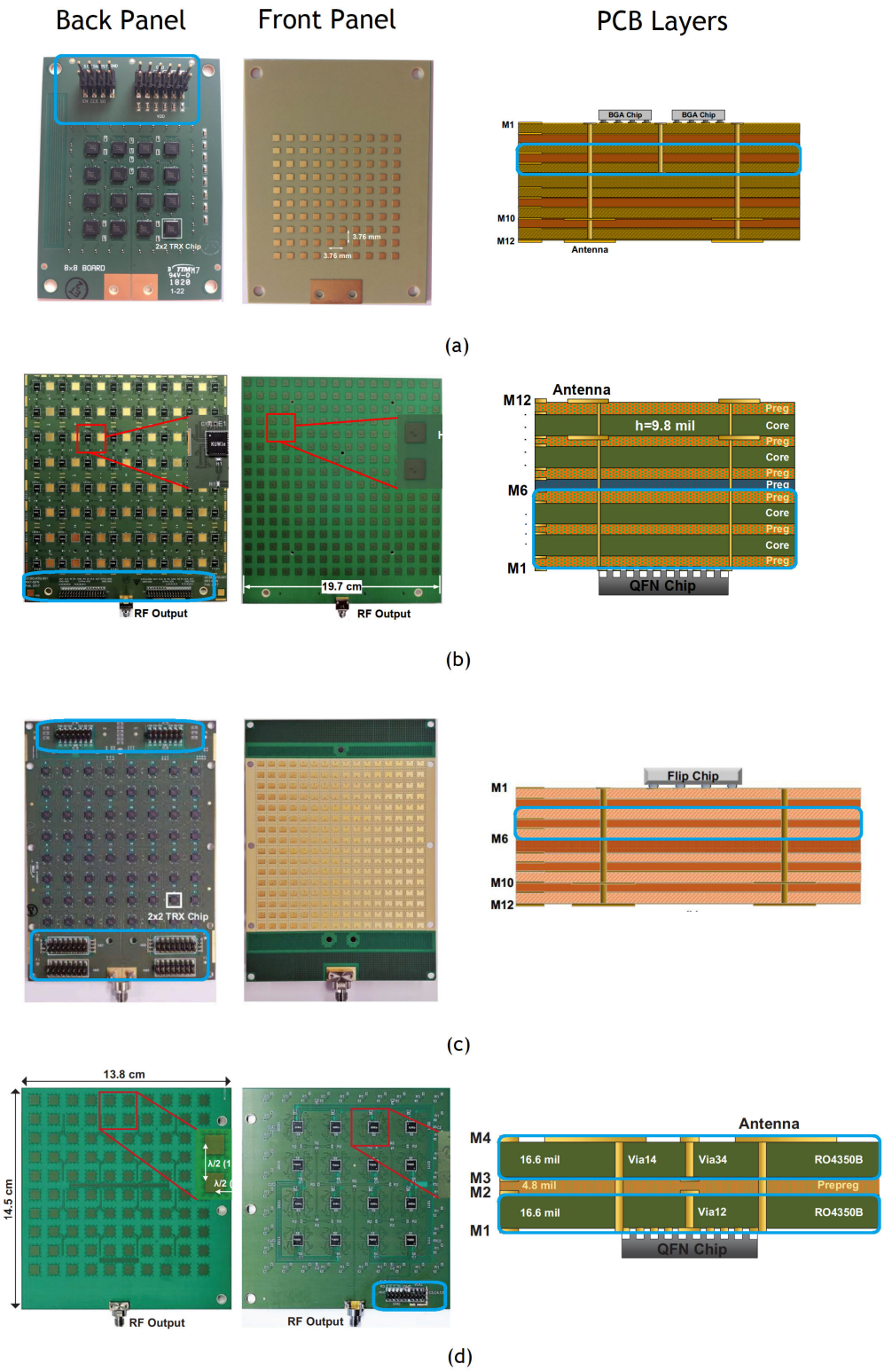


Figure 2.1 Phased array modules from state–of–the–art literature showing the back and front panels, and the PCB layers from: (a) [47], (b) [31], (c) [33], and (d) [35].

Another important observation is that most published designs adopt a segmented control architecture, where each control chip manages a 2×2 subarray [20], [28], [29], [31]–[35], [47]. Even when different segmentation strategies are employed, distributed control across multiple chips remains a common architectural choice in all cited works. While segmentation improves modularity, it proportionally increases the number of required supply, digital, and SPI interconnects.

Finally, many reported phased–array implementations rely on SiGe or SiGe BiCMOS technologies [20], [28]–[33], [47], to achieve high RF performance. However, these technologies introduce additional fabrication complexity due to the incorporation of Germanium (Ge) layers and BJTs, leading to higher manufacturing cost. In contrast, a CMOS–only implementation on a silicon substrate would significantly reduce fabrication cost by avoiding additional process steps, making it more attractive for large–scale and cost–sensitive phased–array systems.

Building on the literature review, we propose combining WPT with non–coherent ASK–PWM to realize a compact, one–pin solution that simultaneously provides power, clock/timing, and control data to each control chip via a miniaturized on–chip antenna. In this approach, WPT supplies the energy required to power the control node, while ASK–PWM carries control information and encodes timing non–coherently (so no local PLL or distributed clock tree is required). The result is a dramatic reduction in supply and digital routing: power feeds and many digital lines are eliminated, PCB layer count and back–panel feed pins are greatly reduced, and the large header pins and empty edge areas seen across the surveyed designs disappear.

Beyond routing savings, the combined WPT & ASK–PWM solution enables architectural simplifications that directly address the problems identified in the literature. Replacing SPI with an asynchronous, non–coherent ASK–PWM receiver removes the need for a wired SPI leader and SPI followers, reducing both pin count and protocol complexity. Local clock recovery from ASK–PWM removes distributed clock distribution and PLL area/power overheads. Implementing the WPT receiver and ASK–PWM demodulator and decoder in a low–cost CMOS process further supports scalable, large–area phased arrays by avoiding the added fabrication cost of SiGe/BiCMOS approaches.

These advantages align with the thesis objectives and contributions discussed earlier: design and silicon realization of a compact, ultra–low–power control IC that integrates a WPT RF rectifier, ASK–PWM demodulator and decoder, digital frame router for data directivity (included with chip and cell identification features), and low–power DACs, all optimized for operation from wirelessly received power. Collectively, WPT & ASK–PWM offers a practical path to remove conventional power, clock, and control pins, reduce PCB complexity, and enable denser, lower–cost phased–array implementations.

2.2 Synchronous Data Transfer in Phased Array Systems

Synchronous data transfer architectures constitute the dominant approach for control distribution in modern phased–array systems. In such architectures, control information is transmitted alongside a global clock reference, typically through SPI, shift–register chains, and parallel clocked buses that program phase shifters and associated RF front–end circuitry [50]–[52]. This section reviews the state–of–the–art synchronous data transfer architectures employed in phased–array control systems.

Several works in the literature have employed synchronous data–transfer protocols to implement digital control and data directivity in phased–array systems.

In [50], a phase–control architecture based on Direct Digital Synthesis (DDS), a PLL, and a fourth subharmonic mixer was introduced. The DDS required a reference clock signal, making the overall system inherently dependent on synchronous clock distribution.

A digital control system utilizing SPI was reported in [51], The architecture employed a central control logic implemented as a Moore Finite State Machine (FSM), with the SPI interface triggered by an external clock to program attenuators and phase shifters.

In [52], a digital phased–array control system was implemented using the core of a DW8051 single–chip microcomputer embedded within a Static Random Access Memory (SRAM)–based FPGA. This solution also relied on the FPGA’s clock for system synchronization and control–data processing.

The work in [53] presented a phased–array control system based on an SPI architecture comprising a leader and multiple followers controlled by a microcontroller. The system managed a bank of sixteen 8–bit registers clocked by a ring oscillator. The SPI leader directed configuration data to the appropriate chip, while the SPI followers routed the received data to the corresponding phase shifters.

A combined software–hardware control architecture for phased arrays was proposed in [54]. The control logic was implemented using Artix–7 and ZYNQ–7000 FPGAs, leveraging the built–in SPI modules of these platforms for data routing and device programming.

A true time–delay control system for phased arrays was discussed in [55]. In this work, digital control signals were applied to phase tuners and were generated using circuitry synchronized to a reference clock. The system also incorporated a PLL for clock generation and timing stability.

In [56], a highly integrated 24–GHz 4–Transmit (Tx)/4–Receive (Rx) Frequency–Modulated Continuous Wave (FMCW) phased–array radar transceiver fabricated in 65–nm CMOS was presented. The system employed reconfigurable beam scanning and frequency sweep generators to enable automatic beam–steering and fast chirp generation. Control and configuration were performed through an SPI interface communicating with external microcontroller units, thus relying on synchronous data transfer.

In [57], a 10–GHz quad–element phased–array transmitter implemented in 28–nm CMOS was presented, based on a Local Oscillator (LO) phase–shifting architecture. Each element incorporated a digital PLL with direct phase control, enabling inherently linear and high–resolution phase shifting. Programming of the phase control word and other configuration settings was performed through an SPI interface, relying on synchronous communication.

In [58], the authors demonstrated a self–adaptive S–band conformal phased array that compensates for deformation–induced beam distortions using a single six–axis Inertial Measurement Unit (IMU) mounted per element and an algorithm that fuses accelerations, angular velocities, and element phases. Continuous phase control is realized with

microwave vector multipliers driven by a 16–channel DAC. A Micro–Controller Unit (MCU) communicates with the IMU and DAC over SPI.

In [59], the authors presented a D–band (134–141 GHz) scalable 2–D CMOS tiled phased–array transmitter using a traveling–wave LO/IF (Intermediate Frequency) distribution and precise half–wavelength antenna spacing, demonstrated as 4×4 and 8×8 arrays. The implementation used SPI for control within a synchronous control framework.

In [60], a 16–element 140–160 GHz phased–array transceiver fabricated in 55–nm SiGe BiCMOS was reported, comprising separate 4–channel Tx and Rx chips along with in–band/Quadrature (I/Q) up– and down–converters and LO multiplication stages. The complete system, assembled on a commercial PCB with cavity–backed patch antennas. Beam–steering control and configuration were implemented using SPI, where the SPI followers were managed by a Beagle Bone Black single–board computer, reflecting a synchronous control architecture.

In [61], Gaydos *et al.* demonstrated a low–cost digital–beamforming testbed built from four National Instruments (NI) Universal Software Radio Peripheral (USRP–2922) software–defined radios, using adaptive algorithms to perform interference cancellation. The Software Defined Radio (SDR) array is synchronized with a CDA–2990 clock module to align RF and sample clocks, and each device is controlled from a central computer.

In [62], a distributed beam–steering architecture uses an SPI leader–follower structure to deliver control data and clocks to phase shifters and attenuators, guided by lookup tables. An FPGA–based Digilent Nexys2 board with a MicroBlaze processor manages SPI communication and angular control data.

In [63], a 4–element passive beamforming continuous–time ΔΣ Analog–to–Digital Converter (ADC) implemented in 40–nm CMOS was presented for high dynamic–range automotive radar applications. The architecture integrates an R–2R based resistive beamforming network within a 4th–order inverter–based ΔΣ loop. The beamformer setup is rather complex, employing both synchronous and asynchronous clock generators.

In [64], a fully integrated 220–260 GHz four–element phased–array transmitter and receiver chipset fabricated in 130–nm SiGe BiCMOS was presented for high–data–rate

wireless links. In the reported implementation, system configuration and control were performed via a Universal Serial Bus (USB) interface; although the authors mention SPI as a potential future option for DAC control, it was not employed in the current realization.

Importantly, none of the surveyed works integrate WPT with the phased–array control system or discuss the system–level advantages WPT would enable. Instead, the literature is dominated by synchronous control paradigms such as SPI leader/follower networks, FPGA/MCU clocked controllers, DDS/PLL–based clocking, and external clock–generators, which impose substantial routing and pin–count overhead and generally require centralized or local clock generation (often via power–hungry PLLs that introduce area, power, cost, and jitter penalties [65], [66]. In particular, many implementations rely on a single–leader, multiple–followers SPI topology to direct data to chips and antenna cells; this approach does not only increase interconnect complexity and feeding–pin requirements but also enforces strict synchronization between the SPI leader and followers (e.g., to control a 4×4 array one typically needs one SPI leader and four SPI followers for each 2x2 subarray) [24], [28], [41], [48], [49], [53], [67]. A few systems use alternative host interfaces or dedicated clock hardware (e.g., SDR clock modules), but these do not remove the fundamental dependence on synchronous timing. Collectively, the review exposes a clear gap: scalable, low–power control architectures that avoid PLL clock generation and leader–follower SPI topologies are needed to enable practical WPT–powered, one–pad–per–control IC phased arrays.

To address the aforementioned limitations, an asynchronous ASK–PWM decoded control architecture is proposed for controlling analog RF attenuators and phase shifters in active phased–array systems. Owing to its asynchronous nature, the proposed scheme does not require an externally distributed clock or a local PLL, unlike synchronous modulation approaches such as Frequency–Shift Keying (FSK) and Phase–Shift Keying (PSK). Eliminating clock–generation and PLL circuitry significantly reduces area and power consumption, which is essential for scalable arrays and WPT operation. Although ASK–PWM entails trade–offs including higher bit–error rate, reduced spectral efficiency, and lower average transmitted power compared to FSK [21]–[23]. These limitations are acceptable for low–data–rate beam–steering control.

In the proposed architecture, the clock information is internally recovered from the ASK envelope, while the transmitted data bits are extracted using PWM decoding of the same input waveform. This dual–modulation strategy enables simultaneous clock and data recovery with a simple, low–power receiver structure [23], [68]. Moreover, ASK–PWM is well suited for integration with WPT if its modulation index can be kept within approximately 10% of the carrier amplitude, thereby minimally impacting WPT efficiency [21], [22].

Because each control node operates asynchronously, the conventional wired single–leader/multiple–follower SPI topology becomes unnecessary. Instead, SPI can be replaced with a simple shift–register–based interface, substantially simplifying internal communication. Each control block incorporates a self–identification mechanism that compares incoming parallel data with a locally stored chip ID, accepting only the intended configuration word and discarding others. This removes the need for a wired centralized data–directing unit and enhances scalability.

Overall, the proposed control system enables a compact, low–power, and cost–effective on–chip implementation by eliminating clock distribution networks, PLLs, and SPI–based synchronization. In combination with WPT, this approach reduces digital and power routing, lowers feeding–pin count, and potentially decreases PCB layer requirements, thereby facilitating highly scalable phased arrays, programmable antennas, and frequency–selective surfaces (FSS).

2.3 Issues Prototyping WPT with ASK–PWM Receiver on PCB

Wireless power and data transfer using ASK–PWM has been explored extensively at the IC level, particularly for biomedical and implantable applications. These IC implementations have demonstrated that ASK–PWM is a viable single–link technique for Simultaneous Wireless Information and Power Transfer (SWIPT), enabling extremely compact receiver architectures and high integration density suited to severe size and power constraints.

Building on this general concept, a substantial body of earlier literature has focused on IC–level realizations of ASK–PWM SWIPT for biomedical systems, emphasizing ultra–low power consumption and reliable short–range links.

In [21], an implantable device capable of locomotion in a fluid medium was fabricated in 65 nm CMOS; it received 500 μW from a 2 W transmitter at 1.86 GHz over a 5 cm distance, supporting ASK–PWM data rates from 2.5 to 25 Mbps.

In [22], an 11 μW transceiver fabricated in a 65 nm CMOS process was reported for powering and communicating with implantable devices. The system employed ASK–PWM with a reconfigurable data rate between 4 and 20 Mbps along an RF carrier of 1.32 GHz. The IC was attached to an off–chip antenna and separated by 3.5 cm from a 125 mW transmitter.

In [69], a 13.56 MHz inductively coupled WPT system implemented in a hybrid organic/metal–oxide process achieved a data rate of 75 bits/s using ASK–PWM, targeting organic biomedical platforms with a form factor of 11×11 cm.

A 4.5 μW, three–channel wireless intra–cardiac acquisition system was presented in [70], realized in a 180 nm CMOS process using a 13.56 MHz inductive link and supporting an 88.3 kbps data rate.

A System–on–Chip (SoC) implementation based on magnetic induction and incorporating ASK–PWM with a flexible dithering feature was introduced in [71] Fabricated in 180 nm CMOS, it reported a power consumption of 50 mW.

In [72], a comparator–less ASK–PWM architecture for inductively coupled WPT was demonstrated in 180 nm CMOS. The design integrated a frequency divider, frequency multiplier, and data sampler to recover clock and data from the ASK–PWM signal at a data rate of 2 Mbps.

A cochlear implant stimulation system employing an 8–channel inductive link with ASK–PWM was described in [73], where a custom receiver chip achieved 120 kbps data rate at a total current consumption of 105 mA.

In [74], a 900 MHz inductively coupled ASK–PWM link operating at a data rate of 10 Mbps was proposed for brain implant applications, consisting of 32 ICs fabricated in 65 nm CMOS.

Finally, [75] reported a 180 nm SoC realization, implementing a near–field resonant inductive link at 40.68 MHz using ASK–PWM, supporting up to 16 implantable stimulators at an 8 cm separation, achieving 10 kbps while consuming 27 μW from a 2 W transmitter.

Collectively, these works validate the practicality of ASK–PWM based SWIPT at the IC level, particularly for implantable and biomedical platforms where compactness, low power consumption, and short–range operation are paramount.

Despite the strong body of IC–level work demonstrating ASK–PWM as a compact SWIPT solution for implants and other size–constrained systems, there remains a clear gap for rapid, low–cost hardware exploration. IC fabrication is expensive, slow, and inflexible for early–stage design exploration, while discrete PCB prototyping is fast and accessible but has not been demonstrated (nor documented in detail) for a wirelessly–powered ASK–PWM receiver using off–the–shelf components.

Attempting a fully discrete realization revealed practical problems that are absent in IC implementations. The three that proved most significant were (i) parasitic inductances at the harvesting rectifier's output filter that allow the input RF to leak into the DC output, (ii) power leaking into the communication path from the harvesting path that results in PCE reduction, and (iii) the incapability of tuning transistor geometries in a discrete skewed buffer stage, making it difficult to produce the skewing needed for robust PWM decoding.

This work closes these gaps by presenting a practical, fully discrete wirelessly–powered ASK–PWM receiver design, included with a reproducible design methodology based on commercially available components. At a high level, it addresses the problems with a combination of circuit– and layout–level mitigations to suppress parasitics, topology and load–decoupling techniques that preserve PCE while adding flexibility in communication filter design, and discrete–logic design strategy that enables robust PWM decoding without custom IC devices. These contributions provide a clear, practical path for

rapid prototyping and system–level experimentation of ASK–PWM SWIPT outside the IC foundry flow.

2.4 Conclusion

This chapter surveyed the state–of–the–art across three complementary areas: power and information routing challenges in large–scale phased arrays, synchronous control architectures for beam–steering, and the lack of work on discrete wirelessly–powered ASK–PWM receivers on PCB. The literature shows that conventional designs allocate a significant portion of board area and fabrication complexity to supply, clock, and SPI routing, as well as the associated back–panel feed pins. At the same time, most control solutions rely on synchronous, leader–follower SPI topologies, which may require local clock generation (PLL) which introduces additional area, power, and timing overhead. Finally, although ASK–PWM SWIPT is well established at the IC level for implants and other size–constrained systems, there is no documented approach for realizing a complete wirelessly–powered ASK–PWM receiver using discrete, off–the–shelf components on PCB.

To address these gaps, we proposed an alternative control paradigm based on combining WPT with an asynchronous, non–coherent ASK–PWM receiver. This one–pad–per–control IC approach supplies power, timing, and control data simultaneously, removing the need for large power/SPI routing, distributed clock trees, and leader/follower SPI topologies. We also identified three practical obstacles that arise when moving from ICs to PCB–level prototypes: parasitic RF leakage at the harvesting rectifier output, power leakage between harvesting and communicating rectifiers, and limited transistor–geometry control in discrete logic. We outlined high–level mitigation strategies (circuit/layout fixes, load–decoupling topologies, and discrete skewing techniques) that enable a reproducible, fully discrete implementation.

In the next chapter we develop the theoretical foundations necessary to design and analyze beamforming and beam–steering systems, the WPT front end and the ASK–PWM communication scheme that make the proposed architecture feasible.

Chapter 3: Related Theory

In this chapter, the theoretical and technical foundations required for the development of the proposed beam–steering control architecture are presented. The discussion covers the fundamental principles underlying phased–array beamforming and beam–steering, the adopted WPT strategy, and the selected communication scheme, access technique, and data–transfer protocol.

The chapter begins with a review of phased–array systems, revisiting the core concepts of beamforming and beam–steering that form the basis of electronically controlled radiation patterns. This establishes the framework within which the proposed wireless control architecture operates.

Subsequently, the theory of WPT is introduced, with emphasis on high–frequency long–range WPT, commonly referred to as Microwave Power Transfer (MPT). The discussion focuses on the principles governing RF energy propagation, rectification, and PCE, as these directly influence the feasibility of wirelessly powering distributed control ICs.

Following this, communication schemes suitable for simultaneous power and control delivery are reviewed, with particular attention given to the non–coherent ASK–PWM technique. Its operational principles, advantages, and relevance to low–power distributed control systems are examined.

Finally, multiple–access techniques and digital data–transfer protocols are discussed, including conventional SPI systems, to establish a comparative baseline and motivate the architectural decisions adopted in this work.

The purpose of this chapter is not only to summarize the relevant theoretical background, but also to justify the key design choices underlying the proposed system–level architecture, including the control strategy, WPT implementation, communication scheme, access method, and data protocol.

3.1 Beamforming and Beam–steering

In this section, the fundamental principles of beamforming and beam–steering are introduced, along with the essential elements required to realize electronically steerable antenna systems.

We begin with a general overview of scanned–array architectures, introducing the concept of the Active Electronically Scanned Array (AESA) and outlining the key subsystems required to enable dynamic beam control. This provides a system–level perspective of how electronically controlled radiation patterns are achieved.

Next, the discussion turns to the most fundamental building block of any phased–array system: the antenna element. Its radiation characteristics, impedance behavior, and role within an array environment are reviewed, as these directly influence overall array performance.

Following this, the concept of antenna arrays is presented. By combining multiple radiating elements in a controlled spatial configuration, arrays enable constructive and destructive interference, allowing enhanced directivity, beam shaping, and electronic beam–steering compared to a single antenna element.

Finally, the RF beam–steering components responsible for controlling amplitude and phase are discussed, including RF switches, phase shifters, and attenuators. These elements form the core of the control architecture and enable precise manipulation of the array radiation pattern.

3.1.1 An introduction to scanned array systems

The best way to describe the idea of a scanned array is to directly present its most fundamental application: The radar. Radar stands for **ra**dio **d**etection **a**nd **r**anging. As the term states, radar is a system that is used mainly for the detection of objects in its range while identifying the distance to the object [15].

The operating principle of a radar system can be described as follows. A transmitting antenna radiates a short–duration electromagnetic pulse in a specified direction. When this

pulse encounters an object within its propagation path, a portion of the incident energy is reflected back toward the radar system. Immediately after transmission, the system switches from transmit mode to receive mode in order to capture the returned echo signal [15].

By measuring the time interval between the emission of the pulse and the reception of its echo, the radar system determines the round–trip propagation delay. This delay is then used to calculate the distance to the target, since the electromagnetic wave travels at the speed of light [15].

In addition to range estimation, radar systems possess directional control capability. By steering the transmitted and received beam across a defined angular sector, the radar can scan multiple directions within its coverage range, enabling the detection and localization of objects throughout the scanned region [10].

From the preceding discussion on radar operation, the essential components required to implement such a system can be identified. At a minimum, a radar system requires an RF power source, a radiating antenna or array of antennas, and a Transmit/Receive Module (TRM) responsible for signal generation, amplification, and reception [10].

In addition to these core elements, an effective radar system must incorporate a mechanism for beam–steering to enable spatial scanning. Early implementations achieved this by mechanically rotating the antenna structure, typically a parabolic dish. While functional, mechanical scanning suffers from significant drawbacks, including large size, high weight, increased power consumption, limited scanning speed, and susceptibility to mechanical wear and failure [76].

Modern systems instead adopt the AESA architecture, which enables beam–steering through electronic control rather than physical movement. In an AESA system, beam direction is manipulated using RF control components such as RF phase shifters, attenuators, and switches [10]. By adjusting the relative phase and amplitude of the signals feeding each antenna element, the overall radiation pattern can be steered electronically. Furthermore, in AESA architecture, each antenna element is typically equipped with its own dedicated TRM, allowing independent control and improved system flexibility.

Figure 3.1 illustrates the structural and operational differences between mechanically scanned arrays and AESA systems.

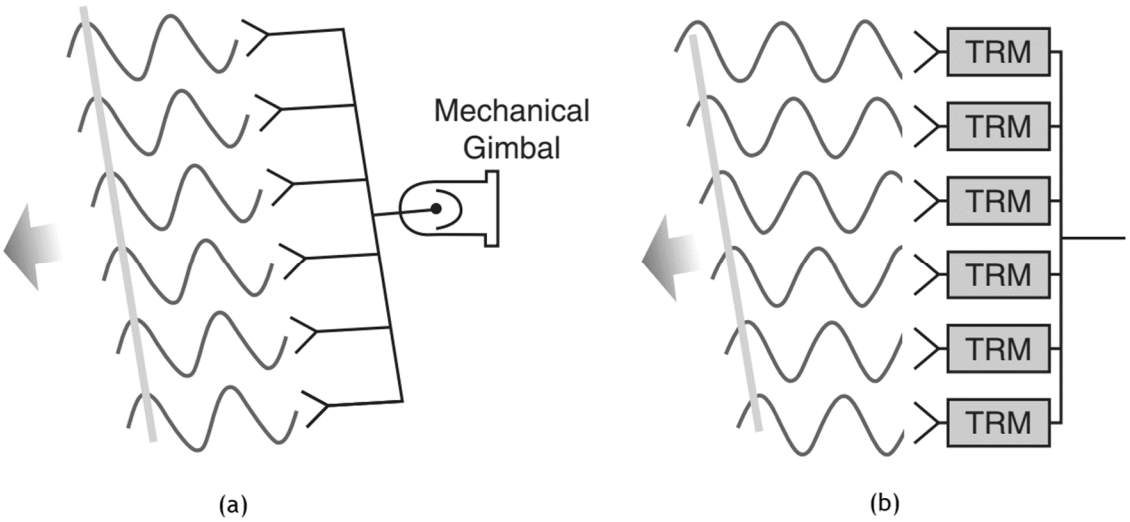


Figure 3.1 Scanned array systems showing the different techniques of: (a) mechanically scanned array and (b) AESA [10].

A central building block of the phased–array architecture is the TRM. The primary objective of the TRM on the transmit path is to condition and control the RF signal prior to radiation. This includes providing sufficient power amplification through a Power Amplifier (PA), thereby relaxing the requirements on the preceding RF signal generation stage. The TRM also incorporates a voltage–controlled Phase Shifter (PS), which adjusts the phase of the RF signal to enable beam–steering, and a voltage–controlled Attenuator (AT), which allows deterministic amplitude control. Amplitude tapering across the array elements is particularly important for sidelobe suppression and radiation pattern shaping [10], [77].

On the receive path, the TRM includes a Low Noise Amplifier (LNA) to amplify the incoming signal while minimizing the added noise contribution. Similar to the transmit path, phase shifters and attenuators are employed to ensure coherent signal combining and amplitude control during reception. Additionally, the TRM must incorporate an RF switch to alternate between transmit and receive modes, enabling time–division operation of the radar system.

Figure 3.2 presents a representative block diagram of a typical TRM in a phased–array system. Also shown is the associated control block, which governs the phase shifters and attenuators, through analog, digital, or hybrid control signals, depending on the specific circuit implementation, while the RF switches are typically digitally controlled. In some architectures, a Variable Gain Amplifier (VGA) is included to maintain a consistent output signal level suitable for subsequent processing stages, regardless of input signal variations [78].

Further details on beam–steering circuitry and control implementations are discussed in Subsection 3.1.4.

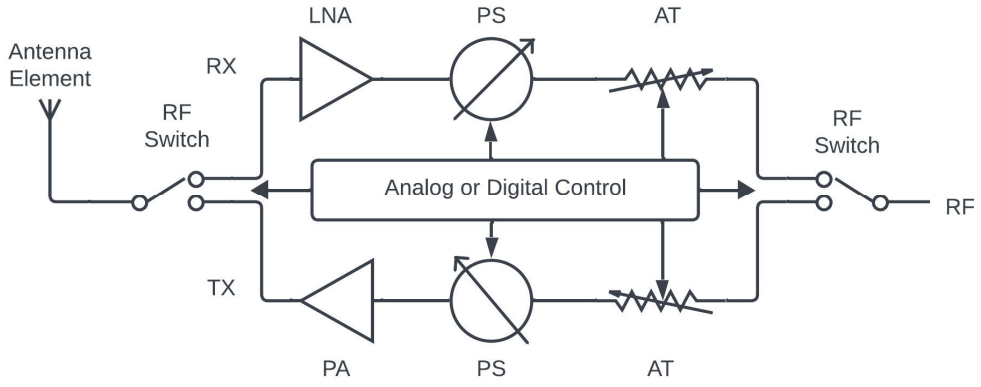


Figure 3.2 Block diagram of a TRM [77].

3.1.2 The antenna

Since antenna elements constitute the fundamental radiating units of any beamforming system, a brief overview of their operation and characteristics is essential.

An antenna may be interpreted from two complementary perspectives. First, it can be viewed as a transducer that converts guided electromagnetic (EM) waves into radiated waves during transmission, and vice versa during reception. Second, it may be regarded as an impedance–transforming interface between a transmission line or waveguide and free space [15]. From this viewpoint, the antenna must not only radiate efficiently but also provide proper impedance matching to minimize reflections and maximize power transfer.

Antennas can be broadly categorized based on their physical structure and operating principle. Wire antennas, for example, are constructed from conducting elements and include dipoles, monopoles, loops, and helical antennas. These are commonly used due to their relatively simple structure and well–understood radiation characteristics. Another category includes aperture antennas, which are typically larger and operate by guiding energy through an opening that transitions smoothly into free space. These structures, such as pyramidal horn antennas and parabolic reflector dishes, often provide high directivity and improved impedance matching between the waveguide and the surrounding medium [15].

The rigorous EM analysis of antennas and their radiation mechanisms involves advanced mathematical formulations derived from Maxwell's equations and boundary conditions. However, for the purpose of this work, the focus will be placed on key performance parameters and radiation characteristics of representative antenna types. These results provide practical insight into the specifications required for antenna elements within a phased–array beamforming system.

We begin the discussion with the Hertzian dipole, an idealized infinitesimal current element that does not physically exist in practice. Despite its hypothetical nature, the analytical solutions derived from its EM radiation provide valuable insight that can be extended to practical antenna designs.

One of the key insights obtained from the Hertzian dipole analysis concerns the spatial behavior of the electric field (E–field) and magnetic field (H–field) as a function of distance from the source. The resulting expressions reveal that the radiated fields exhibit different characteristics depending on the observation distance, leading to the classification of EM regions into reactive (inductive), radiating near–field, and far–field regions [15]. Since this distinction is particularly important in the context of WPT, a more detailed discussion will be deferred to Section 3.2.

Another important insight derived from the Hertzian dipole model relates to the radiated power P_{rad}, and the concept of radiation resistance R_{rad}, These quantities quantify how efficiently a current element converts electrical power into radiated EM energy.

The corresponding expressions can be written as follows [15]:

$$P_{rad} = \frac{1}{2} {I_0}^2 R_{rad}, \tag{3.1}$$

$$R_{rad} = 80\pi^2 \left[\frac{dl}{\lambda}\right]^2, \tag{3.2}$$

where I_0 is the current flowing through the antenna element, dl the segment length, and λ is the wavelength.

From these relations, it can be observed that the radiated power is directly proportional to R_{rad}. Therefore, for a given current amplitude, achieving higher radiated power requires a larger radiation resistance. Since R_{rad} scales with $(dl/\lambda)^2$ electrically small antenna elements exhibit very low radiation resistance and consequently radiate inefficiently.

In addition to reduced radiation efficiency, electrically small elements present impedance–matching challenges. A very short dipole has a small real–part input impedance, making it difficult to match to a standard 50 Ω transmission line without additional matching networks. For instance, if $dl = \lambda/20$, the radiation resistance is approximately $R_{rad} \approx 2\ \Omega$, which represents a severe impedance mismatch relative to a 50 Ω system. This mismatch leads to significant reflections and reduced power transfer unless impedance transformation techniques are employed.

The analysis of the Hertzian dipole can be extended to physically realizable antenna structures. However, once the antenna length becomes comparable to the wavelength, the assumption of uniform current is no longer valid. Instead, an appropriate current distribution must be assumed that satisfies the excitation conditions at the feed point as well as current continuity along the radiating element and its boundary conditions [15].

This extended analysis leads to practical and widely used antenna configurations, most notably the half–wave dipole and the quarter–wave monopole.

For a half–wave dipole antenna ($\lambda/2$), the radiation resistance is approximately $R_{rad} \approx 73\ \Omega$, representing a substantial increase compared to electrically small dipoles.

According to (3.1), this higher radiation resistance translates into significantly improved radiation efficiency for a given current amplitude.

For a quarter–wave monopole antenna ($\lambda/4$) mounted over a ground plane, the radiation resistance is approximately $R_{rad} \approx 36.5\ \Omega$, which is roughly half that of the half–wave dipole. This reduction arises because the monopole effectively represents half of a dipole, with the ground plane acting as an image conductor.

Interestingly, the geometric mean of 73 Ω and 36.5 Ω is very close to 50 Ω, indicating that both antennas can be reasonably matched to a standard 50 Ω transmission line. In practice, this results in a Voltage Standing Wave Ratio ($VSWR$) typically below 2, allowing efficient power transfer with minimal matching complexity.

It is worth noting that the half–wave dipole is particularly significant, as it forms the conceptual basis for many practical antenna structures, including microstrip (patch) antennas. Patch antennas, which can be easily fabricated on PCBs, are widely used in array implementations due to their low profile, ease of integration, and compatibility with planar technologies [13].

We conclude the discussion on wire antennas with the small–loop antenna. A small–loop antenna is characterized by a loop radius that is much smaller than the operating wavelength, meaning it is electrically small (radius $\ll \lambda$) [15]. Due to this property, small–loop antennas offer compact and flexible physical implementations, making them attractive in applications where space is limited.

However, similar to electrically short dipoles, the radiation characteristics of small loops differ significantly from those of resonant–length antennas. In particular, their radiation resistance is typically very small, which impacts their radiation efficiency. The radiation resistance of a small–loop antenna can be expressed as:

$$R_{rad} = \frac{320\pi^4 A^2}{\lambda^4}, \tag{3.3}$$

where A represents the physical area enclosed by the loop. From (3.3), it is evident that the R_{rad} increases with the square of the loop area. Therefore, increasing the loop area

enhances the radiated power for a given current amplitude, provided the loop remains electrically small (typically with circumference or radius much smaller than the wavelength).

This observation highlights an important design trade–off. On one hand, increasing the antenna area improves radiation resistance and thus radiation efficiency. On the other hand, as the loop dimensions approach a significant fraction of the wavelength, the electrically small assumption is no longer valid. The current distribution is no longer approximately uniform, and the simple small–loop model no longer accurately describes the antenna behavior.

A fundamental parameter used to characterize antenna performance is the Directivity D, defined as the ratio of the maximum radiation intensity to the average radiation intensity over all directions [15]. Directivity quantifies how effectively an antenna concentrates radiated power in a particular direction compared to an isotropic radiator. It is sometimes referred to as the maximum directive gain $G_{d,max}$, particularly when losses are neglected. As such, directivity serves as an important metric for comparing different antenna designs in terms of their spatial energy focusing capability.

Table 3.1 summarizes the key characteristics of the antenna types discussed. From the table, it can be observed that the maximum directive gains of the half–wave dipole, quarter–wave monopole, and small–loop antennas are typically below 2 dBi (approximately 1.5–1.8 dBi depending on implementation) [15], [79]. Microstrip (patch) antennas offer improved performance, with maximum directive gains generally ranging between 4 dBi and 8 dBi [80].

Although patch antennas provide higher directivity than simple wire antennas, the achievable gain of a single antenna element is typically limited to below 10 dBi. This limitation restricts the maximum power density that can be concentrated in a given direction when using a single radiator. For applications requiring highly directive beams such as radar systems and long–range wireless links, this constraint becomes significant.

The solution to this limitation lies in the use of antenna arrays, where multiple radiating elements are combined to achieve substantially higher directivity and controlled beam–

steering. The concept and theory of antenna arrays are discussed in the following subsection.

Table 3.1 Antenna specifications of common antenna types (*: Typical values) [15], [79]–[81].

Antenna Type	Radiation Resistance (Ω)	Maximum Directive Gain (dBi)
Half–wave Dipole	73	1.64
Quarter–wave Monopole	36.5	1.5
Loop	1–100*	1.5*
Patch	70–360*	4–8*

3.1.3 Phased arrays

As discussed in the previous subsection, the maximum directive gain of a single antenna element is inherently limited, typically remaining below 10 dBi. In many practical applications, particularly in radar systems, it is desirable to concentrate EM energy into a highly focused beam directed toward a specific angle. Achieving higher spatial power density and improved angular resolution therefore requires an approach beyond the use of a single radiating element.

This requirement leads to the concept of the antenna or phased array. A phased array consists of multiple individual radiating elements arranged in a defined geometric configuration and excited with controlled amplitudes and phases to produce a desired overall radiation pattern [15]. By exploiting constructive and destructive interference between the fields radiated by each element, the array can significantly enhance directivity and enable electronic beam–steering.

In most practical implementations, the array elements are chosen to be identical. This simplifies fabrication, analysis, and control, while ensuring predictable radiation characteristics across the array [15].

Figure 3.3 illustrates how increasing the number of elements within an array enables greater beam focusing and higher directivity, demonstrating the fundamental advantage of array–based radiation over single–element antennas.

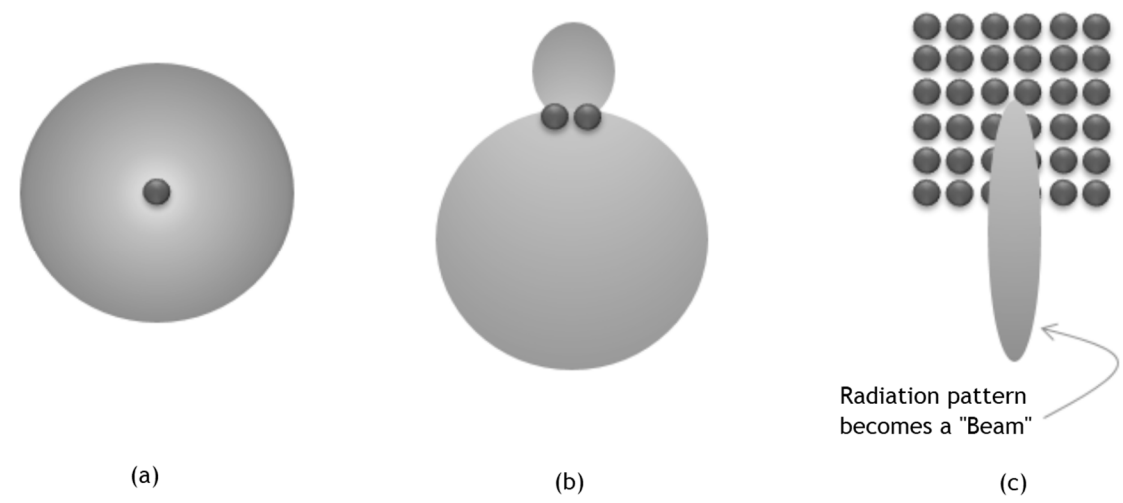


Figure 3.3 Radiation pattern of antenna array showing the difference in directivity of: (a) single antenna element, (b) two, and (c) multiple antenna elements [82].

It is important to recognize that, in the far–field region, the radiated waves from individual antenna elements combine through the principle of superposition. Depending on the relative element spacing, number of elements, individual element radiation pattern, array factor, and the excitation phase and amplitude applied to each element, the resulting fields may interfere constructively, destructively, or partially in different spatial directions [13], [15].

Constructive interference occurs when the radiated waves from the array elements arrive in phase along a particular direction, reinforcing one another and producing a strong, highly directive beam. The dominant beam is referred to as the main lobe, while additional strong maxima that may appear, often due to improper element spacing, are known as grating lobes.

Partial constructive interference results in smaller radiation peaks called sidelobes, which represent undesired radiation away from the intended beam direction. In contrast, when the fields from the array elements combine out of phase such that they cancel completely, nulls are formed in the radiation pattern.

Although multiple factors influence the characteristics of the main lobe and sidelobes, the most critical controllable parameter in an antenna array is the excitation current at each

element, specifically, its amplitude and phase [15]. By appropriately adjusting these quantities, the overall radiation pattern of the array can be shaped and steered.

Beam–steering is primarily achieved through phase control. By introducing a progressive phase shift between adjacent antenna elements, constructive interference can be forced to occur in a desired direction, thereby steering the main lobe without physically moving the antenna structure. This electronically controlled configuration is known as a phased array, and it forms the basis of modern electronically scanned radar systems [10], [11]. **Figure 3.4** illustrates how applying a linear phase progression across a linear array shifts the direction of the main beam [83].

In contrast, amplitude control is mainly used for sidelobe management. By applying non–uniform amplitude weights across the array elements, which is a process commonly referred to as amplitude tapering, sidelobe levels can be reduced, thereby improving radiation pattern quality and minimizing unwanted radiation in off–axis directions [10], [11]. **Figure 3.5** presents radiation patterns of a 5×1 phased array under different amplitude weighting schemes, demonstrating how sidelobes can be shaped through controlled excitation [84].

An important observation is that aggressive sidelobe suppression often comes at the expense of main lobe performance. For example, binomial weighting can eliminate sidelobes entirely; however, this results in a significant reduction in directivity and beam sharpness. Consequently, practical phased–array designs rely on optimization techniques to achieve a balanced trade–off, reducing sidelobe levels while preserving as much main lobe gain and beamwidth performance as possible.

As for grating lobes, these are undesired radiation maxima that appear at directions different from the intended main lobe and may approach, or even equal, its magnitude [85]. Unlike ordinary sidelobes, grating lobes represent strong constructive interference in unintended directions and can severely degrade array performance.

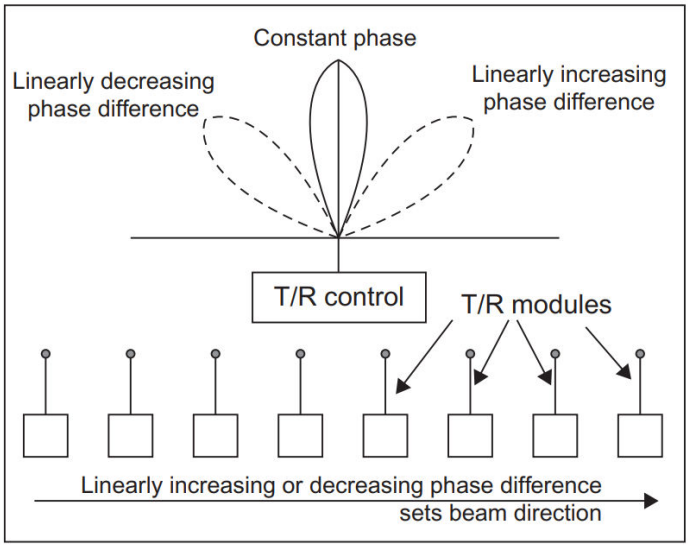


Figure 3.4 A conceptual plot showing how linear phase progression of antenna elements can change the direction of the main lobe [83].

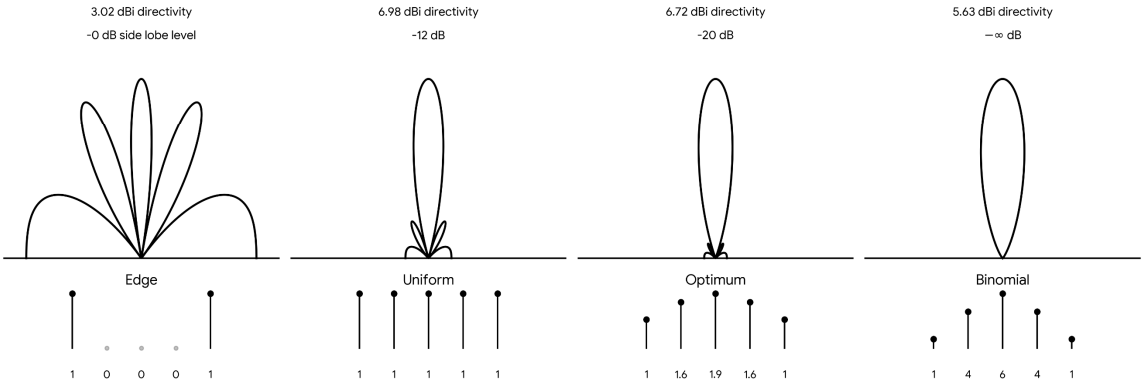


Figure 3.5 Plots of phased array pattern showing sidelobes tapering by changing the weighting of current excitation at each antenna element of a 5x1 array [84].

Grating lobes occur when the spacing between adjacent antenna elements exceeds approximately half a wavelength ($> \lambda/2$). Under this condition, the spatial sampling of the radiated wavefront becomes insufficient, allowing constructive interference to occur at multiple angular directions in addition to the desired beam direction [85].

Consequently, to avoid the formation of grating lobes over the intended scan range, array element spacing is typically limited to $\lambda/2$ or less. This constraint has important practical implications: as the operating frequency increases and the wavelength decreases,

the permissible spacing between elements becomes smaller. As a result, high–frequency phased arrays require increasingly compact layouts, which significantly impacts integration density and system–level design complexity.

3.1.4 Beam-steering circuits

As discussed in the previous subsection, steering the main lobe and controlling sidelobe levels in a phased array require independent control of the phase and amplitude of the excitation current at each antenna element. This electrical control is realized through dedicated RF circuitry integrated within the TRM.

The circuit responsible for introducing a controlled phase shift to the RF signal is the RF phase shifter, while amplitude control is achieved using an RF attenuator. By adjusting the phase across elements, the direction of the main beam can be electronically steered. Similarly, by adjusting the amplitude distribution, sidelobe levels can be shaped through tapering techniques.

As illustrated earlier in **Figure 3.2**, the TRM incorporates not only phase shifters and attenuators but also RF switches. These switches serve two primary purposes: they are fundamental building blocks within many phase shifter and attenuator topologies, and they enable switching between transmit and receive modes in time–division radar systems.

In the following discussion, key operational principles and design considerations of these RF beam–steering circuits are reviewed, with emphasis on their role within phased–array implementations.

3.1.4.1 RF switches

RF switches are fundamental components in beam–steering architectures and play a critical role in TRM implementations [10]. Two common switch configurations used in phased–array systems are the Single–Pole Single–Throw (SPST) and the Single–Pole Double–Throw (SPDT) switches. An SPST switch functions as a simple on/off element, connecting or disconnecting a signal path. In contrast, an SPDT switch routes a common input to one of two output paths.

SPDT switches are essential in TRMs to enable switching between transmit and receive modes in time–division systems such as radar [10]. Both SPST and SPDT configurations are extensively employed within RF phase shifter and attenuator topologies, where controlled signal routing is required to achieve discrete phase or amplitude states [86], [87].

Two widely adopted technologies for implementing RF switches are the P–doped–Insulator–N–doped (PIN) diode and the Field–Effect Transistor (FET). PIN diodes are traditionally used in RF switching applications due to their fast–switching speed and ability to handle relatively high RF power levels [68]. However, in IC implementations, FET–based switches are often preferred. The intrinsic gate–to–channel isolation in FET devices provides high input impedance and good control over the conduction state, enabling compact integration, and compatibility with CMOS processes [86].

3.1.4.2 RF attenuators

The objective of the RF attenuator is to provide gain control through the path of the RF current [10]. This is needed for two reasons, the first is to reduce the gain in case the overall gain of the path is above the expected level, the second is to taper the current's amplitude in every antenna element to reduce the sidelobes [10]. RF attenuators can be controlled via analog or digital means depending on the design requirements. Typically, RF attenuators are constructed either from a π–resistive network or T–resistive one [86], [88]. These resistors can be passive which would result in a fixed attenuator or digitally controlled one or can be an active analog one by utilizing the nonlinear resistance of an FET [89].

3.1.4.3 RF phase shifters

An ideal RF phase shifter is capable of adjusting the phase of an input RF signal to a desired value without altering its amplitude or introducing additional loss [86]. In practice, however, phase shifters exhibit insertion loss, phase error, and amplitude variation that must be carefully managed.

RF phase shifters may be implemented as analog (continuous–control) devices, where the phase shift varies smoothly with a control voltage, or as digital (discrete–step) devices,

where predefined phase states are selected using switching elements [86]. In phased–array systems, the primary objective of the phase shifter is to impose the required phase progression across antenna elements to steer the main lobe electronically.

Several phase shifter topologies are commonly employed in beam–steering applications, including reflective phase shifters, loaded–line phase shifters, switched–delay–line phase shifters, and switched–filter phase shifters [86], [90], [91].

A reflective phase shifter typically consists of a 90° hybrid coupler with reflective terminations connected at its output ports. By controlling the reflection coefficient (often using varactors), the reflected signal acquires a controllable phase shift, which is then recombined at the input port to produce the desired output phase variation [90], [91].

Loaded–line phase shifters achieve phase control by introducing a variable shunt susceptance along a transmission line. Adjusting this reactive loading alters the effective electrical length of the line and therefore the phase shift [90].

Switched–delay–line phase shifters are digitally controlled implementations that employ two or more transmission lines of different electrical lengths. An SPDT switch selects between these paths, resulting in discrete phase states determined by the length difference [90].

Finally, switched–filter phase shifters utilize SPDT switches to alternate between different filter networks, such as high–pass and low–pass configurations. Since these filters exhibit distinct phase responses, switching between them enables discrete phase control [86].

3.2 Wireless Power Transfer (WPT)

Since the proposed architecture relies on wirelessly powering the control blocks of the phased–array system, a foundational overview of WPT and its underlying principles is essential. This section introduces the theoretical background and system–level considerations relevant to the proposed implementation.

We begin by presenting the fundamental concept of WPT, outlining its operating principle, motivation, and the technological need for contactless energy delivery in distributed electronic systems. Various WPT technologies are then briefly reviewed to provide context for the selected approach in this work.

Next, WPT techniques are classified according to the transmission distance relative to the wavelength and radiating structure. This classification highlights the distinction between near–field and far–field energy transfer mechanisms, which is particularly relevant for high–frequency implementations.

Finally, a representative block diagram of an MPT system is presented. The essential system components including the RF power source, transmitting antenna, propagation channel, receiving antenna, rectifier, and power management circuitry are discussed with emphasis on their relevance to compact, distributed control nodes.

3.2.1 Introduction to WPT

The fundamental objective of WPT is to deliver electrical power from a source to a load without the use of physical wired connections. In a typical WPT system, a transmitter converts electrical power into a time–varying electromagnetic field, which propagates through space and transfers energy to a remote receiver via a wireless link [92]. The receiving unit then captures the electromagnetic energy and converts it back into usable electrical power to supply the load.

WPT offers several important advantages. It enhances system mobility and flexibility by eliminating wired interconnections, reduces mechanical wear associated with connectors, and enables power delivery in environments where wired connections are impractical, hazardous, or physically inaccessible [92], [93]. Additionally, WPT can provide environmental and economic benefits by simplifying system deployment and reducing maintenance requirements [94].

WPT technologies can be broadly classified based on operating frequency and the distance between the transmitter and receiver [95]. Three principal categories can be identified:

1. **Low–frequency, short–range WPT**, typically based on capacitive coupling, inductive coupling, or magnetic resonance coupling.
2. **High–frequency, short–range WPT**, which employs electrically small antennas for near–field energy transfer.
3. **High–frequency, long–range WPT**, which includes MPT and Ambient Energy Harvesting (AEH), where power is transmitted and received through radiative far–field mechanism.

In the following subsection, WPT will be further classified according to the separation distance between the transmitting and receiving radiating elements.

3.2.2 Classifications of WPT

The analysis of the Hertzian dipole in Subsection 3.1.2 provides valuable insight into how EM field characteristics evolve with distance from a radiating source. This spatial variation naturally leads to a classification of WPT technologies according to the dominant field mechanism.

At extremely short distances from the radiating element, the EM fields are predominantly reactive and resemble the electrostatic field of a dipole. In this regime, energy transfer occurs mainly through electric–field coupling, making capacitive WPT suitable for operation in this region [15].

At slightly larger, yet still electrically short distances, the magnetic (inductive) component of the reactive field becomes dominant. In this region, inductive coupling is the primary mechanism for power transfer, forming the basis of inductively coupled WPT systems [15]. Both capacitive and inductive coupling operate within what is commonly referred to as the near–field region. This region is typically defined by distances r

satisfying $r \ll 2d^2/\lambda$ where d represents the largest physical dimension of the antenna [15].

For distances exceeding approximately $2d^2/\lambda$, the EM fields transition into radiative behavior, and the wavefronts approximate plane waves. In this far–field region, energy transfer occurs through propagating electromagnetic waves, which forms the basis of MPT and AEH technologies [15].

Between the reactive near–field and the radiative far–field lies the radiating near–field (Fresnel region), where the fields exhibit a spherical wavefront structure and cannot be approximated purely as reactive or fully planar. In this intermediate region, electrically small antennas are often employed, and system behavior depends on both geometric and wavelength considerations.

A similar field–based classification can also be derived using loop antennas instead of Hertzian dipoles, as discussed in [95].

The various classes of WPT are now examined in detail in the following subsubsections.

3.2.2.1 Inductive coupling WPT

Inductive coupling WPT operates in the near–field region and is typically used for very short–range power transfer, where the H–field is the dominant energy–carrying component [96]. In such systems, coils are employed at both the transmitter and receiver to generate and capture the alternating H–field. Power transfer occurs through magnetic flux linkage between the coupled coils.

Despite its high efficiency at close proximity, inductive coupling WPT is fundamentally limited by its short operational range. Efficient energy transfer requires the transmit and receive coils to be placed in close alignment and at small separation distances, typically much smaller than the wavelength [95]. As the separation increases, the mutual inductance decreases rapidly, leading to a sharp reduction in transferred power.

3.2.2.2 Resonance coupling WPT

The effective transfer distance in inductive coupling WPT can be extended by introducing capacitors in series or parallel with the coils to form resonant LC tanks [95]. This approach, known as resonant inductive coupling or magnetic resonance coupling, enhances energy transfer by tuning both the transmitter and receiver coils to resonate at the same operating frequency. At resonance, the reactive energy stored in the inductors and capacitors oscillates efficiently, resulting in improved coupling and increased power transfer over larger distances compared to non–resonant inductive systems [95].

Using resonance, the achievable transfer distance can be extended to approximately 4–10 times the coil diameter, depending on alignment and quality factor (Q) [95]. However, resonant coupling introduces its own limitations. The system typically achieves maximum efficiency at a specific separation distance between the transmitter and receiver [97]. As the distance increases, the mutual coupling coefficient decreases, leading to reduced efficiency.

Conversely, when the separation distance becomes smaller than the designed optimum, the system may enter the strong–coupling regime. In this case, the single resonance peak splits into two distinct frequency peaks that shift away from the original resonance frequency, resulting in reduced efficiency at the intended operating frequency [97].

To maintain high efficiency over varying distances, adaptive tuning circuits are often incorporated at the transmitter and/or receiver. These circuits dynamically adjust the resonance condition to compensate for changes in coupling and alignment [97].

3.2.2.3 Microwave Power Transfer (MPT)

When longer transmission distances are required, MPT becomes the preferred approach. In MPT systems, power is transmitted through high–frequency electromagnetic waves that propagate in the far–field region. Directional antennas or beamforming structures are typically employed at the transmitter to concentrate RF energy toward the receiving unit, thereby increasing the received power density.

At the receiver, a rectenna, which consists of an antenna followed by an RF rectifier, captures the incident RF power and converts it into usable DC power [85]. The rectifier stage may be implemented as a simple single–diode rectifier or as a multi–stage voltage multiplier, depending on the required output voltage and the available input power level.

A key challenge in MPT systems is the variability of the incident RF power. The received power level is sensitive to changes in separation distance, antenna alignment, obstacles in the propagation path, and environmental conditions [95]. These variations directly affect rectifier efficiency and output voltage.

To maintain efficient power conversion across varying input conditions, reconfigurable rectifier architectures are often employed. Such designs dynamically adjust the rectification topology or the number of active stages to adapt to changes in received RF power [95].

A more detailed discussion of MPT is presented in the following subsection.

3.2.2.4 Ambient Energy Harvesting (AEH)

AEH shares fundamental similarities with MPT, as both rely on converting incident RF energy into usable DC power. The key distinction, however, lies in the source of the RF energy. In AEH systems, there is no dedicated transmitter intentionally delivering power. Instead, energy is scavenged from ambient electromagnetic radiation present in the environment [98].

This ambient energy originates from various sources, including mobile communication systems, wireless local area networks, broadcast radio and television transmitters, and other RF–emitting infrastructure [98], [99]. Unlike MPT, where power levels can be engineered and directed, the available ambient RF power density is typically very low and highly variable.

Due to these low power levels, AEH is generally suitable for ultra–low–power applications, such as wireless sensor nodes (WSNs) and low–duty–cycle monitoring systems. Efficient rectifier design and power management are therefore critical in AEH systems to maximize the usable DC output under weak input conditions.

3.2.3 Block diagram of MPT system

Since MPT is selected in this work due to its ability to support larger separation distances between the transmitter and receiver, a more detailed discussion of its system architecture is warranted. In particular, it is important to examine the functional blocks that constitute a typical MPT system and understand the role of each stage in enabling efficient wireless power delivery.

Figure 3.6 presents a representative block diagram of an MPT system. The key components of this architecture are described in the following subsubsections, with emphasis on the features most relevant to the proposed implementation.

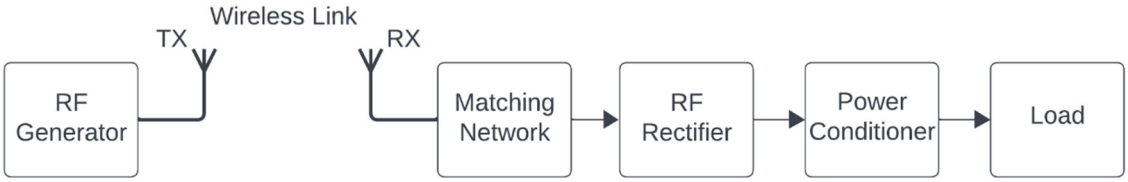


Figure 3.6 Block diagram of an MPT [95].

3.2.3.1 Transmit and receive antennas

To determine the specifications required for the transmit and receive antennas in an MPT system, the non–ideal Friis transmission equation must be considered [95]:

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi r}\right)^2 \eta_t \eta_r (1 - S_{11})(1 - S_{22}) \left|\vec{u} \cdot \vec{v}\right| \alpha, \tag{3.4}$$

where P_r is the received power at the rectenna, P_t is the transmitted power, G_t and G_r are the gains of the transmit and receive antennas, respectively, and r is the separation distance between them. The terms η_t and η_r represent the radiation efficiencies of the transmit and receive antennas. The reflection coefficients S_{11} and S_{22} account for impedance mismatch at the transmit and receive antennas, respectively. The factor $\left|\vec{u} \cdot \vec{v}\right|$ models polarization mismatch between the two antennas, while α accounts for multipath propagation effects.

From (3.4), it is evident that maximizing the received power P_r requires increasing the transmitted power P_t, enhancing the antenna gains G_t and G_r, ensuring high antenna efficiencies, achieving proper impedance matching, and maintaining polarization alignment between the transmitter and receiver.

Assuming that impedance matching, antenna efficiency, and polarization conditions are optimized, the received power becomes primarily dependent on the product $P_t G_t$ (often referred to as the Effective Isotropic Radiated Power, $EIRP$) and the receive antenna gain G_r. While $P_t G_t$ can be increased by raising transmit power or improving transmit antenna gain, regulatory constraints such as those imposed by the Federal Communications Commission (FCC) limit the maximum allowable $EIRP$ [95]. Consequently, MPT system design often involves setting $P_t G_t$ within regulatory limits while optimizing the receive antenna gain G_r to maximize harvested power [99].

Common antenna types used in rectenna designs include dipole antennas, linearly polarized patch antennas, and loop antennas [95], each offering trade–offs in gain, size, polarization characteristics, and integration complexity, as was discussed in subsection 3.1.2.

3.2.3.2 RF rectifier

The primary objective of an RF rectifier is to convert an RF input voltage into a usable DC output voltage. A typical RF rectifier consists of three main components: an input matching and filtering network, a nonlinear rectifying device (typically a diode or diode–connected transistor network), and an output filter that smooths the rectified waveform into a DC voltage [95].

Several RF rectifier topologies are commonly employed, as illustrated in **Figure 3.7**.

The simplest configuration is the series–mounted diode rectifier (**Figure 3.7**(a)). In this half–wave topology, the diode is placed in series with the signal path. During the positive half–cycle of the RF input, the diode conducts and charges the output filter (usually a shunt rectification capacitor); during the negative half–cycle, it blocks current flow [95].

Another half–wave configuration is the shunt–mounted diode rectifier (**Figure 3.7**(b)), where the diode is connected in parallel with the load. This topology operates on a similar principle but differs in current flow path and impedance characteristics [95].

By combining series– and shunt–mounted diodes, a voltage doubler configuration can be realized (**Figure 3.7**(c)). This topology increases the DC output voltage by stacking charge contributions from alternating half–cycles, making it particularly useful in low–input–power scenarios [95].

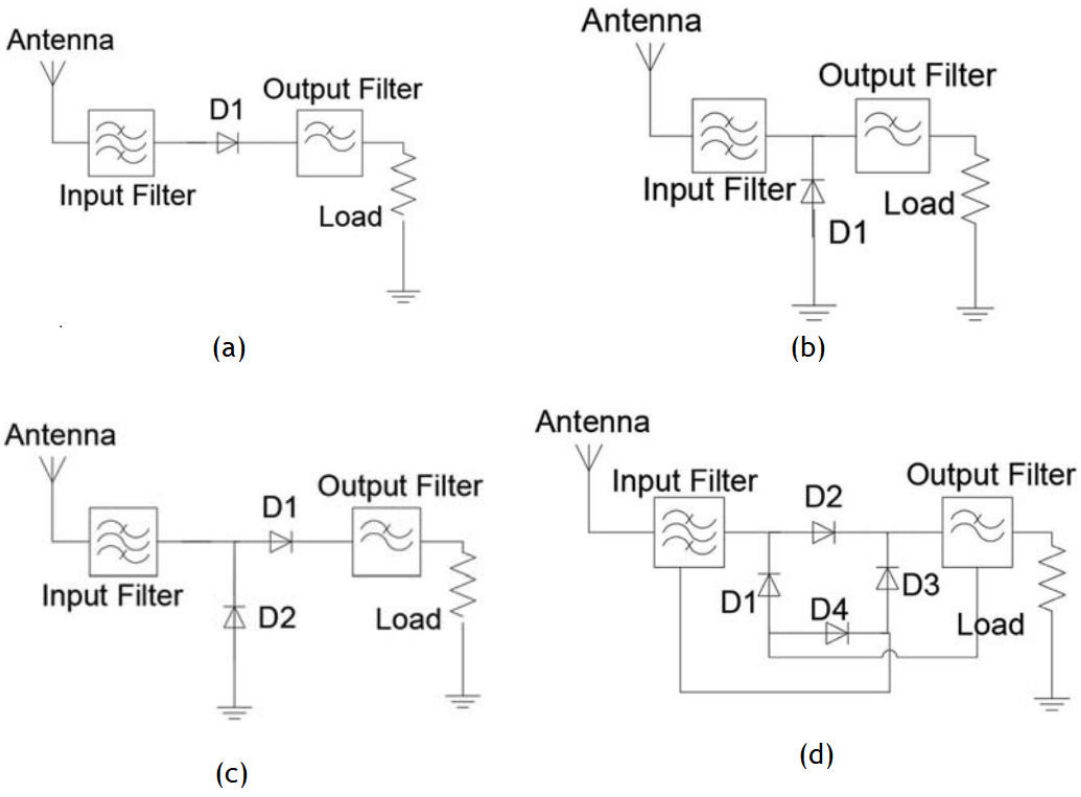


Figure 3.7 Common RF rectifier topologies: (a) series, (b) shunt, (c) voltage doubler, and (d) full–wave rectifier [95].

Finally, the full–wave rectifier (**Figure 3.7**(d)) utilizes multiple diodes to rectify both half–cycles of the RF input signal. This results in reduced output ripple and improved power handling capability. However, because two diodes are typically in the conduction path during each half–cycle, the effective threshold voltage increases, reducing sensitivity, especially under low–input–power conditions.

3.2.3.3 Matching network

Impedance matching between the receiving antenna and the RF rectifier is a critical consideration in rectenna design. Unlike linear RF loads, the rectifier is inherently a nonlinear device; therefore, its input impedance depends on the input power level and operating point. As a result, large–signal simulations (e.g., harmonic balance analysis) are required to accurately determine the optimal input impedance for maximum power transfer, since this impedance varies with incident RF power [95].

This nonlinear behavior makes the design of the matching network particularly challenging. The matching condition that maximizes efficiency at one input power level may not be optimal at another. Consequently, the rectifier and matching network must be co–designed to ensure acceptable performance across the expected input power range.

Moreover, the topology of the matching network can significantly influence rectifier sensitivity. For instance, incorporating a resonant inductor at the input can boost the RF voltage across the rectifying device, effectively lowering the minimum input power required for diode turn–on. This approach shifts the peak PCE toward lower input power levels, making the rectifier more suitable for weak–signal operation [85].

3.2.3.4 Power conditioner

In many rectenna systems, the rectified DC voltage at the load is not directly suitable for powering subsequent circuitry. Therefore, a power conditioning stage is typically required to regulate and stabilize the output voltage [95]. This stage is commonly referred to as a voltage regulator, and it can be broadly classified into two categories: linear regulators and switch–mode regulators, as illustrated in **Figure 3.8**.

Linear voltage regulators maintain a constant output voltage by operating an active device as a voltage–controlled current source. A feedback control loop continuously monitors the output voltage and adjusts the conduction of the pass device to maintain regulation. This control loop typically employs active components such as BJTs or FETs, with an operational amplifier (Op Amp) serving as the error amplifier in the feedback path [95].

Three main types of linear regulators are commonly used: standard regulators, low–dropout (LDO) regulators, and quasi low–dropout regulators, as shown in **Figure 3.8**(a) [95]. Standard linear regulators often use a Darlington pair as the pass element to achieve high current gain suitable for driving heavier loads. However, this configuration introduces a relatively large voltage drop (approximately 1.4 V) between the input and output due to the two base–emitter voltage drops. To reduce this dropout voltage, a single common–emitter stage can be used instead of a Darlington pair, resulting in a quasi–LDO structure. Further reduction in dropout voltage can be achieved by removing the additional amplification stage entirely and using a single pass transistor configuration, forming a true LDO regulator.

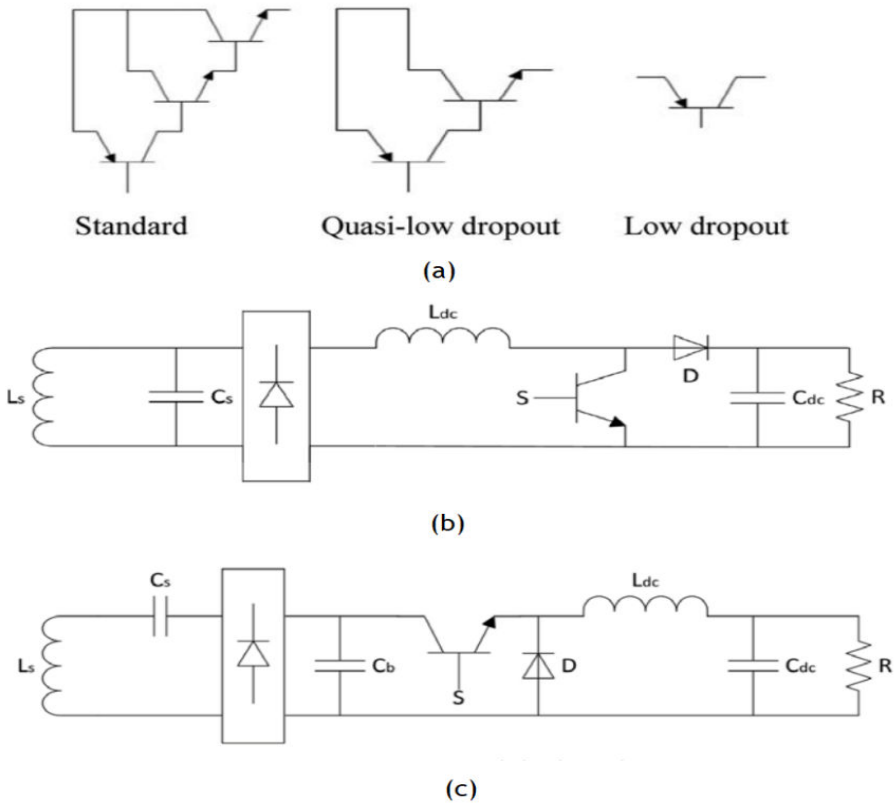


Figure 3.8 Voltage regulator circuits: (a) linear, (b) switch–mode boost converter, and (c) switch–mode buck converter [95].

Switch–mode regulators, in contrast, regulate the output voltage by rapidly switching energy between storage elements such as inductors and capacitors [95]. The two primary topologies are buck and boost converters, shown in **Figure 3.8**(b) and (c). A buck converter steps the input voltage down to a lower regulated output, while a boost converter increases the input voltage to a higher level.

Boost converters, however, present a dynamic and sometimes reactive load to the preceding stage, which can disturb impedance matching conditions at the rectifier output. Buck converters generally exhibit more stable input behavior but can encounter startup challenges, particularly in low–power harvesting systems where the initial input voltage may be insufficient to activate control circuitry [95].

In addition to these operational considerations, both buck and boost converters rely on inductive energy storage elements. These inductors are typically bulky and occupy significant physical area, which complicates compact implementation. In IC realizations, on–chip inductors consume large silicon area and often exhibit limited Q, while off–chip inductors increase system size, reduce integration density, and require additional IC package leads. Consequently, switch–mode regulators may be less attractive for highly integrated and miniaturized wirelessly powered ICs.

3.3 Communication Architectures and Protocols

In this section, the communication strategies relevant to the proposed wireless control architecture are reviewed and analyzed. The discussion begins with an overview of common digital modulation techniques, highlighting their operating principles and examining their compatibility with WPT systems. Particular emphasis is placed on how modulation choices affect power transfer efficiency, spectral efficiency, receiver complexity, and synchronization requirements.

Following this general review, the non–coherent ASK–PWM scheme is examined in detail. Its structure, operational principles, and suitability for simultaneous power and control delivery are discussed, with emphasis on its advantages in low–power distributed control systems.

Since the proposed architecture involves controlling multiple distributed ICs from a centralized transmitter, the section then reviews common multiple–access techniques, including Time Division Multiple Access (TDMA), Frequency Division Multiple Access (FDMA), Orthogonal Frequency Division Multiple Access (OFDMA), and Code Division Multiple Access (CDMA). Their complexity, scalability, synchronization requirements, and suitability for compact phased–array control are compared.

Finally, digital data transfer protocols are examined, including SPI, Universal Asynchronous Receiver–Transmitter (UART), and Inter–Integrated Circuit (I^2C). Particular attention is given to their clock distribution requirements, synchronization mechanisms, leader–follower structures, and the resulting routing overhead. These aspects are critical in dense phased–array implementations, where additional clock trees and dedicated communication lines significantly increase layout complexity.

This structured review establishes the rationale behind the communication architecture adopted in this work.

3.3.1 Communication schemes

In wireless architectures where power and data share the same transmission link, the choice of modulation scheme must be evaluated not only in terms of communication performance but also in terms of its impact on WPT. In this subsection, common digital modulation techniques including ASK, ON–OFF Keying (OOK), FSK, and PSK are briefly reviewed, with emphasis on the question of suitability for simultaneous power and data delivery. The ASK–PWM scheme is then examined in greater detail due to its favorable integration with WPT–based control systems.

3.3.1.1 Common digital modulation schemes

To enable wireless data transmission, the baseband information must be modulated onto a high–frequency carrier. Several common digital modulation schemes are widely used for this purpose, including ASK, OOK, FSK, and PSK. These techniques differ in the carrier parameter they vary (amplitude, frequency, or phase) to encode information. The corresponding signal representations are illustrated in **Figure 3.9**.

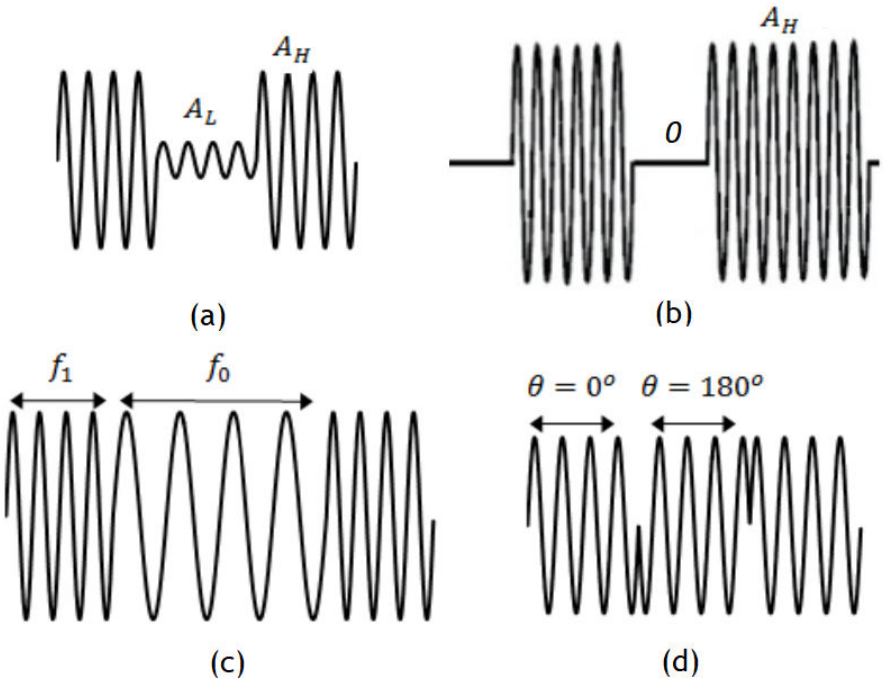


Figure 3.9 Common modulation schemes: (a) ASK, (b) OOK, (c) FSK, and (d) PSK [23].

In ASK, the amplitude of the carrier is varied between discrete levels according to the input data sequence. Two main detection approaches exist: coherent and non–coherent. Coherent ASK relies on a locally generated carrier that is phase–synchronized with the received signal for demodulation [23]. This approach requires additional circuitry for carrier recovery, typically involving clock–generation blocks and a PLL, which increases system complexity and power consumption.

Non–coherent ASK, on the other hand, operates asynchronously and does not require carrier phase synchronization. Demodulation is typically performed using an envelope detector followed by low–pass filtering, eliminating the need for phase detection and significantly reducing receiver complexity and power requirements [23].

While ASK offers implementation simplicity and favorable integration with rectifier–based receivers, its achievable data rates are generally lower compared to more spectrally efficient modulation schemes [23].

In OOK, the carrier is switched on and off according to the input data sequence. A logical “1” is typically represented by the presence of the carrier, while a logical “0”

corresponds to its absence. Implementing OOK requires an RF source capable of fast switching to ensure accurate symbol transitions.

OOK can be viewed as a special case of ASK with a 100% modulation index. Because of this full–depth modulation, OOK generally exhibits higher immunity to noise and interference compared to low–modulation–index ASK schemes. In general, increasing the modulation index in amplitude–based schemes improves noise robustness [23].

However, in WPT–integrated systems, OOK presents a significant challenge. Since power delivery depends on continuous RF energy transmission, turning the carrier off during the transmission of logical “0” symbols interrupts power transfer. If a long sequence of zeros is transmitted, the RF power delivered to the receiver drops to zero, potentially causing voltage collapse at the rectifier output and disrupting the operation of the powered circuitry. This makes conventional OOK less suitable for simultaneous power and data delivery applications [23].

In FSK, the frequency of the RF carrier is shifted between discrete values according to the input data sequence. One of the key advantages of FSK is its high immunity to noise and interference. Moreover, since the carrier amplitude remains constant, FSK is inherently compatible with WPT systems, as it does not introduce envelope fluctuations that could significantly disturb rectifier operation [23].

However, FSK demodulation typically requires frequency discrimination or phase–locked techniques, which increase receiver complexity and power consumption compared to simple envelope–based schemes [23]. Additionally, because information is encoded through discrete frequency shifts, spectral efficiency is limited, and achievable data rates are generally lower than those of higher–order modulation schemes [23].

A common variation is Gaussian–filtered FSK (GFSK), in which a Gaussian filter is applied to the baseband signal prior to modulation. This reduces spectral sidelobes and narrows the occupied bandwidth, thereby improving spectral efficiency and reducing adjacent–channel interference [23].

In PSK, information is encoded by varying the phase of the carrier while maintaining constant amplitude and frequency. Because the carrier envelope remains constant, PSK

offers good power efficiency and improved noise performance. Compared to ASK and FSK, PSK generally achieves a lower Bit Error Rate (BER) under similar Signal–to–Noise ratios (SNRs) [23]. Moreover, higher–order PSK schemes can support increased data rates by transmitting multiple bits per symbol.

However, PSK requires coherent detection, meaning that the receiver must recover a phase reference synchronized with the incoming carrier. This necessitates carrier recovery circuits, often involving PLL–based architectures, which increase receiver complexity and power consumption [23]. Such requirements may be undesirable in ultra–low–power or wirelessly powered systems.

PSK can also be implemented in differential form (DPSK), where information is encoded in the phase difference between consecutive symbols rather than the absolute phase. Differential encoding simplifies the receiver by relaxing strict carrier phase synchronization requirements and improves robustness to certain phase disturbances and interference [23]. Regardless, its implementation still introduces additional complexity and area overhead compared to envelope–based modulation.

From the preceding discussion, it may appear that FSK and PSK are naturally well suited for WPT–based systems due to their constant–envelope characteristics, which maintain continuous RF power delivery. However, the receiver architectures required for these schemes are relatively complex, often requiring carrier recovery or frequency discrimination circuitry. This increases power consumption, silicon area, and overall implementation complexity, factors that are undesirable in low–power, wirelessly powered control nodes.

Asynchronous ASK, in contrast, offers a significantly simpler receiver architecture based on envelope detection. It eliminates the need for carrier synchronization and PLL circuitry, resulting in lower power consumption and reduced area utilization. The main drawback of ASK, however, is that its amplitude variations inherently modulate the transmitted power. These envelope fluctuations can disturb the steady power flow required for reliable WPT operation.

One possible mitigation strategy is to reduce the modulation index so that amplitude variations are small. However, excessively lowering the modulation index reduces the distinguishability of logic levels at the receiver, increasing susceptibility to noise and interference and potentially degrading BER performance. Encouragingly, prior work has demonstrated that maintaining a modest ASK modulation index of approximately 10% preserves the simplicity and low–power advantages of ASK while having minimal impact on WPT efficiency [21]–[23].

3.3.1.2 ASK-PWM communication scheme

Although ASK has been shown to be suitable for WPT–integrated systems, additional advantages can be achieved by adopting a dual–modulation approach. By combining ASK with Pulse–Width Modulation (PWM), the resulting ASK–PWM scheme enables simultaneous power delivery, data transmission, and clock extraction using a single RF carrier [21]–[23].

In ASK–PWM, the amplitude variations associated with ASK are used to generate an envelope that can be exploited for asynchronous clock recovery, while the pulse–width variations introduced by PWM encode the data bits. In other words, the envelope detector extracts the ASK component to provide a timing reference, and the PWM structure is subsequently decoded to recover the transmitted information.

This architecture preserves the simplicity and low–power benefits of non–coherent ASK reception while eliminating the need for dedicated clock–generation circuitry and PLL–based synchronization in the digital control block [21]–[23]. As a result, ASK–PWM is particularly attractive for distributed, wirelessly powered control nodes where minimizing power consumption, circuit area, and routing complexity is essential.

The ASK–PWM modulated waveform can be mathematically described by the following expressions [23]:

$$m_0(t) = A_{0L} + \left(A_{0H} - A_{0L} \sum_{k=0}^{\infty} \frac{sin\left[2\pi(2k-1)\frac{f_b}{2}t\right]}{2k-1} \right), \tag{3.5}$$

$$\begin{aligned} m_1(t) &= A_{1L} + \cdots \\ &\left(\frac{A_{1H} - A_{1L}}{2} \sum_{k=0}^{\infty} \frac{sin\left[2\pi(2k-1)\frac{f_b}{2}t\right]}{2k-1} \right) + \ldots \\ &\left(\frac{A_{1H} - A_{1L}}{2} \sum_{k=0}^{\infty} \frac{sin\left[2\pi(2k-1)\frac{f_b}{2}(t+d_c)\right]}{2k-1} \right), \end{aligned} \tag{3.6}$$

$$d_c = \frac{(1 - D_c)}{f_b}. \tag{3.7}$$

$m_0(t)$ represents the modulation corresponding to bit “0”, while $m_1(t)$ represents the modulation corresponding to bit “1”. The parameters A_{0L} and A_{0H} denote the minimum and maximum amplitude levels associated with bit “0”, respectively. Similarly, A_{1L} and A_{1H} represent the minimum and maximum amplitude levels corresponding to bit “1”. The factor k is a summation index, f_b is the bit rate, and d_c is a parameter related to the duty cycle D_c, as defined in (3.7).

From (3.5), the modulating signal can be interpreted as a square waveform expressed as a Fourier series consisting of the sum of sinusoidal components at odd harmonics of $f_b/2$, with a DC offset of A_{0L}. (3.6) introduces an additional term associated with the pulse–width variation for bit “1”, where the duty cycle is governed by (3.7).

Combining (3.5)–(3.7), the resulting ASK–PWM envelope exhibits two distinct pulse–width characteristics: a narrow high–level pulse representing bit “0” and a wider high–level pulse representing bit “1”, as illustrated in **Figure 3.10**(a).

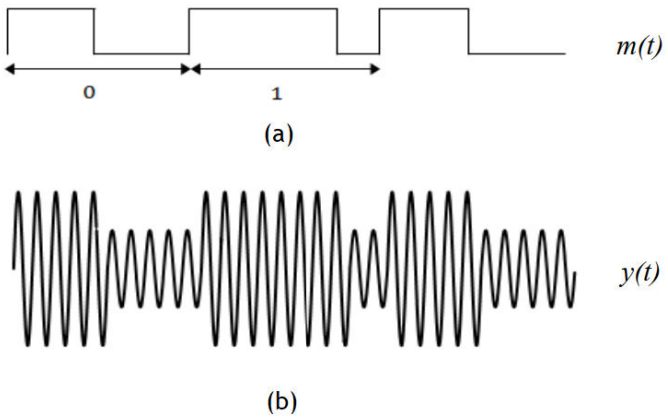


Figure 3.10 ASK–PWM waveforms showing: (a) the modulating signal, and (b) the modulated signal [23].

The carrier signal $c(t)$ and the resulting ASK–PWM modulated signal $y(t)$ can be expressed as follows [23]:

$$c(t) = sin(\,2\pi f_c t), \tag{3.8}$$

$$y(t) = m(t)c(t), \tag{3.9}$$

where f_c is the carrier frequency. The resulting ASK–PWM modulated waveform is illustrated in **Figure 3.10**(b).

A simplified block diagram of the ASK–PWM transmitter and receiver is shown in **Figure 3.11**. On the transmitter side, the architecture consists of a bit generator, an RF source that generates the carrier signal, and a mixer that combines the carrier with the ASK–PWM envelope. The resulting modulated signal is then amplified by a switch–mode PA to provide sufficient power for radiation through the transmit antenna [23].

On the receiver side, the architecture begins with a receive antenna that captures the incoming RF signal. The signal is then processed through a bandpass filter followed by an envelope detector to recover the ASK envelope. A return–to–zero (RZ) converter extracts the timing information, generating the asynchronous clock signal from the ASK

component. In parallel, a skewed buffer and comparator are employed to decode the PWM variations, thereby recovering the transmitted data bits [21]–[23].

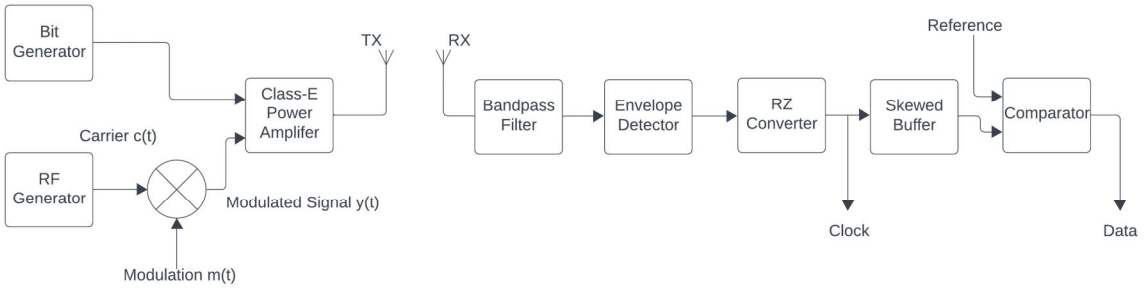


Figure 3.11 A basic block diagram of ASK–PWM transmitter and receiver [21]–[23].

More information about this block diagram and its implementation in Simulink and IC will be presented in Chapters 4 and 7, respectively.

3.3.2 Multiple access techniques

Since the proposed architecture involves wirelessly controlling multiple distributed ICs from a dedicated transmitter, an appropriate multiple–access strategy must be considered. The communication framework must ensure that control information is delivered reliably to the intended IC while avoiding interference among neighboring nodes. This raises the fundamental question of how shared transmission resources (time, frequency, or code space) are allocated among multiple receivers. **Figure 3.12** shows illustrative plots of typical multiple access techniques

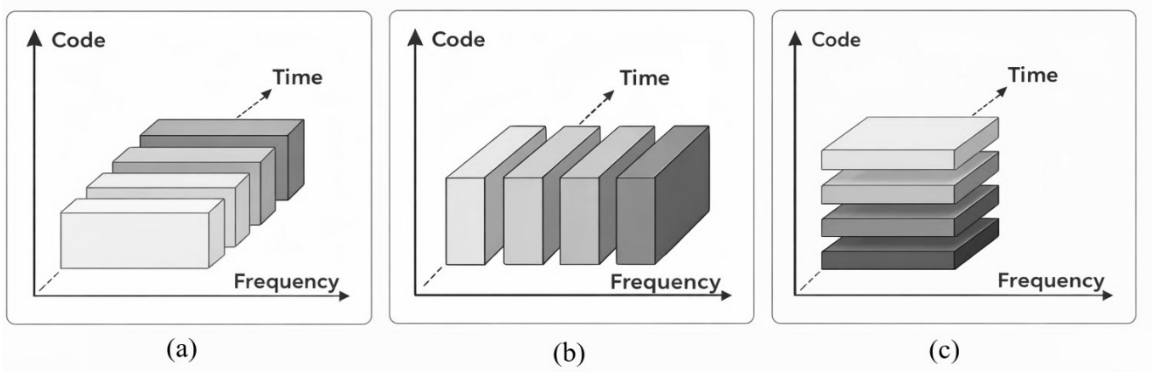


Figure 3.12 Multiple access techniques: (a) TDMA, (b) FDMA, and (c) CDMA.

3.3.2.1 Time Division Multiple Access (TDMA)

TDMA is a multiple–access technique in which multiple devices share the same frequency band by dividing the transmission time into different, non–overlapping time slots. Each time slot is assigned exclusively to a single device, thereby preventing collisions on the shared channel. Since transmissions occur in well–defined and predictable intervals, TDMA is particularly suitable for deterministic and real–time communication systems [100].

In practical implementations, TDMA requires timing coordination among participating nodes. At a minimum, symbol–level synchronization must be maintained so that each device transmits or receives within its allocated slot. In downlink scenarios, synchronization can typically be established by a central transmitter. In uplink scenarios, however, additional coordination is necessary to ensure that devices remain sufficiently time–aligned to avoid overlap between adjacent slots [100].

In the context of the proposed architecture, TDMA offers a straightforward mechanism for addressing multiple distributed ICs using a single RF carrier. Since the system operates in a downlink–only configuration (with a dedicated transmitter and receiving ICs) complex multi–node synchronization is not required. Each IC continuously monitors the received downlink stream, decodes the transmitted data, and extracts the corresponding control block ID and cell ID fields. Upon identifying its assigned address, the IC updates its local phase shifters and attenuators accordingly. The overall control process would be therefore implemented in a time–division manner, where configuration commands intended for different ICs are transmitted sequentially within dedicated time intervals.

3.3.2.2 Frequency Division Multiple Access (FDMA)

In FDMA, the available bandwidth is divided into multiple frequency channels, and each device is assigned a dedicated sub–band for communication. Unlike TDMA, where users are separated in time, FDMA separates users in the frequency domain. Each IC would therefore receive and process a distinct carrier frequency allocated to it [101].

A more advanced implementation of FDMA is OFDMA, where subcarriers are made orthogonal to each other. This allows multiple users to transmit simultaneously without inter–carrier interference. Such techniques are widely used in broadband wireless systems because they are robust to multipath fading and allow flexible allocation of spectral resources [101].

However, FDMA–based schemes require accurate frequency synchronization between transmitter and receiver. Each receiver must be tuned precisely to its assigned carrier frequency, which typically requires local oscillators and PLLs [101].

For the proposed WPT–based control architecture, FDMA is not well suited. The need for frequency synchronization and PLL–based carrier recovery increases power consumption and circuit area, which contradicts the objective of low–power, wirelessly powered control nodes. Furthermore, allocating separate frequency channels for multiple ICs increases spectral complexity without providing significant benefit in a purely downlink, low–data–rate control system.

3.3.2.3 Code Division Multiple Access (CDMA)

CDMA enables multiple users to share the same time and frequency resources by assigning each user a unique spreading sequence. All users transmit simultaneously over the same bandwidth, and signal separation is achieved through code–domain processing at the receiver [100].

In conventional CDMA, the baseband data is multiplied by a high–rate spreading sequence, producing a wideband signal. The effectiveness of the scheme depends on the autocorrelation and cross–correlation properties of the spreading codes, as these determine resistance to self–interference and multiuser interference. Orthogonal or semi–orthogonal codebooks are typically employed to control interference levels [100].

At the receiver, separation of the combined signals requires correlation–based detection or multiuser detection techniques, which involve significant signal processing complexity. Even more advanced schemes, such as Sparse Code Multiple Access (SCMA), rely on structured codebooks and iterative decoding algorithms to separate users [100].

For the proposed WPT–based phased–array control system, CDMA presents several disadvantages. The need for high–rate spreading code generation, correlation–based detection, and potentially multiuser interference suppression increases circuit complexity, silicon area, and power consumption. Furthermore, accurate timing alignment between spreading sequences is typically required to maintain orthogonality, which reintroduces synchronization overhead. Given that the objective of the proposed architecture is to maintain low–power, non–coherent reception without PLLs or complex digital processing, CDMA is not well aligned with the system constraints.

3.3.3 Data transfer protocols

Since the proposed architecture involves communicating with multiple distributed ICs, an appropriate data transfer protocol must be considered. The selected protocol must not only support reliable multi–node communication but also remain compatible with the constraints imposed by the wirelessly powered control architecture, particularly low power consumption, minimal routing complexity, and reduced clock–distribution requirements. In this subsection, commonly used wired protocols such as SPI, UART, and I²C protocols are reviewed and evaluated in the context of large–scale phased–array control systems. Their architectural requirements and limitations are discussed, after which the ASK–PWM–based approach is revisited to demonstrate how it overcomes many of these constraints in the wirelessly powered control architecture.

3.3.3.1 Serial Peripheral Interface (SPI)

The SPI is a widely used digital communication protocol that enables data exchange between two or more devices [48]. SPI is a full–duplex, synchronous, serial communication interface in which one device operates as the leader (controller) and one or more devices operate as followers (peripherals) [48].

A standard SPI interface consists of four signal lines [102]:

- Serial Clock (SCK): Generated by the leader, this signal synchronizes data transfer and controls the timing of bit shifting.
- Master–Out Slave–In (MOSI): Carries data from the leader to the followers.

- Master–In Slave–Out (MISO): Carries data from the selected follower back to the leader. Only the active follower is allowed to drive this line to avoid bus contention.
- Chip Select (CS): Used by the leader to select a specific follower for communication. Non–selected followers place their MISO outputs in a high–impedance state.

Typically, the SCK, MOSI, and MISO lines are shared in parallel among all follower devices, while each follower is assigned an individual CS line, as illustrated in **Figure 3.13** [102].

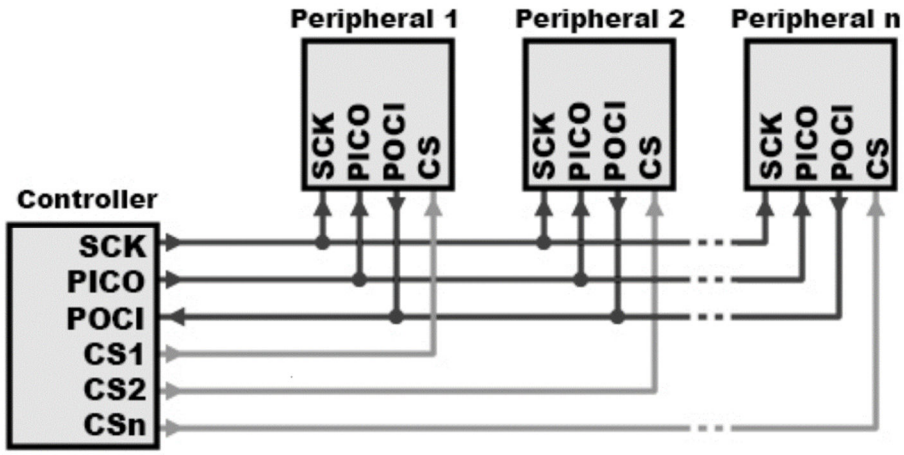


Figure 3.13 Typical configuration of SPI leader and multiple SPI followers [24].

SPI communication proceeds as follows: the leader initiates a transaction by pulling the CS line of the desired follower low. The leader then generates clock pulses on the SCK line. With each clock edge, data bits are shifted out on MOSI and simultaneously shifted in on MISO, enabling full–duplex communication. Once the desired number of bits has been transferred, the leader de–asserts the CS line, terminating the transaction [24].

A typical SPI controller architecture, shown in **Figure 3.14**, includes data and status registers, shift registers for serial–to–parallel and parallel–to–serial conversion, a baud–rate generator derived from a system clock, leader/follower control logic, and port interface circuitry [103].

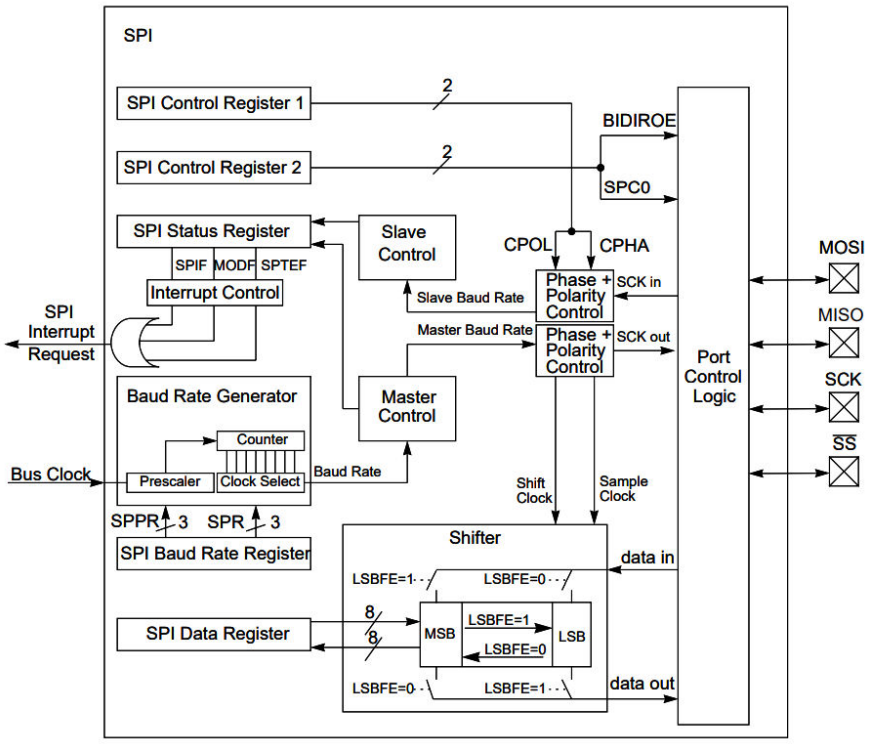


Figure 3.14 Typical block diagram of an SPI [103].

As discussed in the Sections 2.1 and 2.2, SPI is widely adopted for the digital control of phased–array systems. However, several disadvantages arise when SPI is used in large–scale, distributed control architectures.

First, SPI is a synchronous protocol and therefore requires clock generation and distribution. The presence of a high–speed clock line increases circuit complexity, power consumption, and silicon area in each node. In dense phased arrays, distributing the clock signal across multiple ICs introduces additional routing overhead and clock–tree design challenges.

Second, SPI inherently relies on a wired leader–follower structure. A central leader must continuously manage communication, which limits architectural flexibility and creates a single point of control. Moreover, for each additional follower device, a dedicated chip–select line is required. As illustrated in **Figure 3.13**, this results in a linear increase in routing lines as the number of controlled ICs grows, significantly complicating PCB layout, number of PCB layers, and hence increased costs in large arrays.

Third, the internal architecture of an SPI controller, shown in **Figure 3.14**, consists of multiple functional blocks, including shift registers, control logic, baud–rate generators, and interface circuitry. While these blocks provide flexibility and full–duplex capability, they increase silicon area and power consumption. In a wirelessly powered system where each control IC must operate under strict energy constraints, adopting SPI across all nodes would substantially increase the harvested power requirement.

Consequently, although SPI is effective for board–level digital communication, its clock dependency, routing overhead, and internal hardware complexity make it less suitable for a distributed, WPT–integrated phased–array control architecture.

3.3.3.2 Universal Asynchronous Receiver-Transmitter (UART)

The UART is a widely used serial communication protocol that enables point–to–point data exchange between two devices [104]. Unlike synchronous protocols, UART does not require a separate clock line; instead, it relies on predefined baud rates agreed upon by both transmitter and receiver [104]. A basic UART interface consists of two primary signal pins: Tx and Rx. In addition, a common ground reference is required. Optional hardware flow–control signals such as Request–to–Send (RTS) and Clear–to–Send (CTS) may also be included in more advanced implementations. UART transmits data in frames that typically consist of one start bit, data bits, optional parity bit, and one or two stop bits [104].

Because UART is asynchronous, synchronization between transmitter and receiver is achieved using the start bit. Upon detecting the falling edge of the start bit, the receiver begins sampling the incoming signal according to its locally generated baud–rate clock. Therefore, although UART does not require an external clock line, it still requires an internal clock generator to produce the baud rate [104].

In systems where multiple control ICs must be addressed, UART presents scalability limitations. Standard UART communication is inherently point–to–point, meaning each transmitter communicates with only one receiver. To control multiple ICs, additional hardware such as multiplexers, tri–state buffers, or multi–drop bus configurations must be introduced. In such shared–bus arrangements, address decoding logic is required within each node to determine whether the incoming data is intended for that device.

Furthermore, even though UART eliminates the need for an explicit clock distribution line, each receiving IC must maintain a stable local oscillator to generate the sampling clock. In low–power, wirelessly powered control nodes, implementing accurate baud–rate generation circuitry increases power consumption and area utilization.

For the proposed wirelessly powered phased–array control architecture, these requirements reduce the attractiveness of UART. While it simplifies wiring compared to synchronous protocols such as SPI, it still depends on local clock generation and does not inherently provide efficient multi–node addressing without added overhead.

3.3.3.3 Inter-Integrated Circuit (I^2C)

The I^2C protocol is a synchronous, multi–device serial communication interface widely used for short–distance communication between integrated circuits on the same board. Unlike UART, I^2C is a synchronous protocol and therefore requires a shared clock signal [105].

A standard I^2C interface consists of two bidirectional lines: Serial Data Line (SDA) and Serial Clock Line (SCL). Both lines are open–drain and require pull–up resistors. Communication is controlled by a leading device, which generates the clock on SCL and initiates all transactions. Following devices respond only when their unique address is detected on the bus [105].

Data transmission begins with a start condition, followed by bits dedicated for follower address and a read/write bit. After address acknowledgment, data bytes are transferred sequentially, each followed by an acknowledgment bit. Communication ends with a stop condition [105].

Because I^2C is inherently multi–drop, it naturally supports multiple following devices on the same bus. Each control IC can be assigned a unique address, allowing a single leader to communicate with many nodes over only two wires. This makes I^2C more scalable than UART in wired systems, while having less routing compared to SPI.

However, several limitations arise when considering low–power, wirelessly powered control nodes. I^2C requires a shared clock distributed to all following devices, which

introduces routing overhead and increases interconnect density in large phased–array systems. Additionally, each follower must remain synchronized to the leader clock, hence requires clock input buffering and digital timing circuitry in every node. Furthermore, since I²C uses open–drain signaling, pull-up resistors are required. These introduce static current consumption during logic–low states, which is undesirable in WPT systems. Finally, bus capacitance increases with the number of connected ICs and trace length, reducing achievable data rates and increasing rise and fall times. In dense arrays, this becomes a significant constraint.

In the context of the proposed WPT–based phased–array control system, I²C offers the advantage of built–in addressing and multi–IC support. However, the requirement for a distributed clock line, continuous leader control, and wired interconnects conflicts with the objective of eliminating clock trees and minimizing routing complexity. Additionally, each follower must remain clock–synchronized, increasing local digital circuitry and power consumption.

3.3.3.4 ASK-PWM data transfer solution

The limitations of SPI, UART, and I²C in large–scale, wirelessly powered phased–array systems motivate the adoption of an alternative communication architecture. This is where wireless transmission of ASK–PWM provides a compelling solution. By employing a wirelessly–transmitted, non–coherent modulation scheme, the receiver architecture is significantly simplified, eliminating the need for carrier recovery circuits, clock–generating blocks, and PLLs. The asynchronous clock extracted directly from the ASK envelope enables local timing without requiring a distributed clock tree.

Because timing information is embedded within the received wireless waveform, conventional synchronous protocols such as SPI are no longer required at each control node. Instead, the digital control logic can be reduced to a simple shift–register–based structure for serial data conversion, where each control block achieves internal synchronization through carefully designed delay cells between the extracted clock and data. This substantially reduces circuit area, routing complexity, and power consumption, all of which are critical constraints in WPT–powered ICs.

Admittedly, ASK–PWM introduces certain trade–offs. Compared to constant–envelope schemes such as FSK, it exhibits higher BER, reduced spectral efficiency, and slightly lower transmitted average power [23]. However, in the context of low–data–rate phased–array control, these disadvantages are acceptable. The simplicity of the receiver and elimination of clock and data distribution on board outweigh the performance penalties, particularly when integration with WPT is a primary objective.

Therefore, the combination of ASK–PWM demodulation and lightweight digital decoding provide a communication framework that is inherently aligned with the requirements of distributed, wirelessly powered control ICs.

3.4 Conclusion

This chapter assembled the theoretical and technical foundation needed for the proposed wirelessly powered beam–steering control architecture. We began with phased–array fundamentals showing why single antenna elements are limited in directivity and how combining many elements into an array enables high directivity and electronic beam–steering. The TRM was identified as the core hardware cell: it conditions and amplifies the RF signal, provides phase control via phase shifters to steer the main beam, and provides amplitude control via attenuators to manage sidelobes.

Because the architecture depends on removing wired power feeds to many control nodes, we reviewed WPT in detail and adopted the far–field, radiative approach MPT as the practical means to deliver energy across the larger separation distances of interest. The complete MPT chain was examined, with particular attention given to factors that directly affect harvested power, such as antenna gain, efficiency, polarization alignment, and impedance matching. On the receiver side, rectifier topology selection was shown to influence sensitivity, ripple, and achievable output voltage, while its nonlinear input impedance requires careful large–signal matching that varies with input power level. Finally, voltage regulation was assessed under integration constraints: switch–mode converters improve efficiency but add inductive complexity, while linear/LDO regulators

provide compact, low–power solutions more suitable for wirelessly powered ICs. These considerations shaped the chosen architecture.

On the communications side we surveyed common digital modulations (ASK/OOK/FSK/PSK). Constant–envelope schemes (FSK/PSK) are friendly to continuous power transfer but impose complex, power–hungry receiver front ends (PLL/carrier recovery). Non–coherent ASK provides an extremely simple, low–power receiver (envelope detection) but modulates the transmitted envelope. Combining ASK with PWM (ASK–PWM) yields a practical compromise: the envelope (ASK) is used for asynchronous clock extraction while the PWM encodes data bits. ASK–PWM preserves carrier continuity (so power keeps flowing), removes the need for PLLs and distributed clock trees, and enables very lightweight digital front ends in each node.

We evaluated multiple–access and protocol alternatives in the context of wirelessly powered, downlink–only control nodes. TDMA is a natural fit for downlink control because the central transmitter can time–multiplex configuration frames and the receivers only need to parse their assigned intervals. In our non–coherent ASK–PWM architecture, this requires no global clock distribution or uplink synchronization. FDMA/OFDMA and CDMA were found less suitable because they demand precise frequency or code synchronization, PLLs, and more complex receivers, increasing area and power that are scarce in wirelessly powered nodes. Similarly, standard wired data protocols (SPI, UART, I²C) were reviewed and shown to introduce unwanted clock distribution, chip–select routing, or local baud–rate generators that conflict with the goal of ultra–compact, low–power control ICs.

Taken together, these choices lead to the system–level decision adopted in this work: use MPT to supply power and ASK–PWM to deliver clock and data, with time–division framing to address individual control blocks. This combination minimizes receiver complexity (no PLLs, no externally distributed clocks), reduces PCB routing and pin count (no per–node CS or clock trees), and allows each control block to implement a minimal digital interface, which is a small serial shift register with internal synchronization achieved with delay cells between the recovered clock and data. The trade–offs (higher BER and reduced spectral efficiency compared with coherent schemes) are acceptable given the low

data–rate, control–centric application and the large system gains in integration, area, and power.

Having established the theoretical principles and justified the key architectural choices, the next chapter transitions from theory to system–level realization. The proposed wireless power and control framework will be analyzed and validated at the system level, forming the basis for subsequent circuit implementation and experimental demonstration.

Chapter 4: Control System Architecture and Simulink Modeling

In this chapter, the architecture of the proposed wirelessly powered control system for beam–steering is presented and validated at the system level. An overview of the control system and its role within the overall beam–steering architecture will be presented, including the 2×4 (8–cell) phased array example used throughout the chapter.

Next, we present the control–system block diagram and describe how each subsystem (RF rectifier, power conditioning, the ASK–PWM demodulator/decoder, and the digital frame router with DACs) contributes to power harvesting, clock/data recovery, frame–routing, and analog control signal assertion.

Afterwards, we provide a timing–analysis example that demonstrates how serial ASK–PWM frames are decoded, converted to parallel control bits, and applied to the phase shifter DACs; this timing study also motivates the use of deliberate delay elements and explains how TDMA addressing coordinates multiple control blocks.

Finally, the last section introduces the Simulink model used for preliminary verification and presents waveform results that confirm correct clock recovery, data decoding, and frame routing. Together, these sections establish the functional feasibility of the wirelessly powered ASK–PWM control scheme showing how embedding clock and data in the power link removes the need for global clock trees and SPI wiring, reduces routing and feed–pin requirements, and enables a scalable TDMA–based control strategy prior to FPGA and IC implementation in later chapters.

4.1 Control System Overview

The main concept of the proposed wirelessly powered control system is illustrated in **Figure 4.1**. In this architecture, a power transmitter utilizes a transmit antenna to deliver modulated RF power to the phased array module at a frequency significantly lower than the beamforming frequency to reduce EM interference between the WPT carrier and the beamforming carrier. Each control block or IC receives this modulated RF power and harvests its energy using a rectenna (Subsection 3.2.3). The modulation present on the same

transmitted RF signal is then used to demodulate and decode the ASK–PWM waveform, enabling the recovery of both clock and data signals as described in Subsubsection 3.3.1.2.

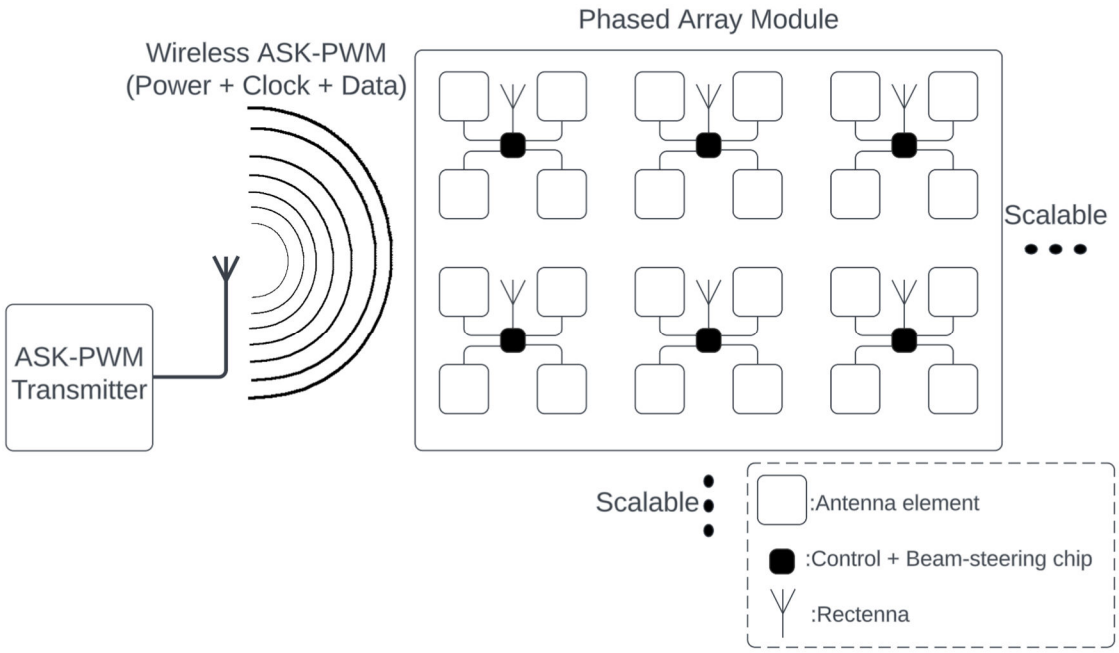


Figure 4.1 Proposed control system approach using wirelessly powered non–coherent ASK–PWM control system.

Within each control block, the received serial data are converted into parallel data using a shift register with manually introduced delay cells to achieve internal synchronization between the received data and clock, rather than relying on an SPI interface as discussed in Subsubsection 3.3.3.1.

The resulting parallel data are used for acknowledgment, control block identification, and cell identification. The acknowledgment mechanism verifies correct data reception through a predefined bit pattern, while each control block performs self–identification to determine whether the received command is intended for that specific control block. If the control block identification matches, the command is accepted; otherwise, it is discarded.

Communication among the control blocks is performed in a TDMA manner, as discussed in Subsubsection 3.3.2.1, where configuration commands are sequentially addressed to each IC. In this architecture, TDMA enables simple addressing of multiple

control blocks over a single RF link, without requiring complex synchronization due to the downlink–only operation.

Each control block is designed to manage four antenna elements. Accordingly, each control block continuously monitors the received downlink stream, decodes the received ASK–PWM signal, and extracts the corresponding control block ID and cell ID fields. Upon identifying its assigned address, the IC updates the control signals of phase shifters and/or attenuators of the corresponding antenna element through DACs.

The integration of non–coherent ASK–PWM with WPT enables a unified, fully wireless architecture that simultaneously delivers power, control data, and timing information through a single RF link. By harvesting power, power distribution networks, external supply rails, and connection feeding pins on the phased array module are eliminated. Additionally, by embedding clock in amplitude (ASK) and data in pulse width (PWM), the same received signal can be used to locally extract both clock and control data without requiring coherent demodulation or phase synchronization. This additionally eliminates the clock trees, PLLs, and SPI–based communication buses, allowing each control node to operate from a single RF input pad and antenna. As a result, system complexity, I/O count, and pad requirements are significantly reduced, while low–power operation is maintained due to the avoidance of power–hungry clock recovery and synchronization circuits.

Furthermore, the proposed ASK–PWM with WPT framework enables a distributed and modular control architecture in which each node independently harvests energy, recovers timing, and decodes its assigned data using embedded addressing schemes. This removes the need for shared communication buses and centralized wired control, allowing scalable expansion to large phased–array systems without increasing routing complexity. By eliminating extensive interconnects, the architecture reduces metal congestion, parasitic effects, and electromagnetic coupling, thereby potentially improving RF performance and enabling higher integration density. The resulting reduction in routing layers, interconnect overhead, and supporting circuitry lowers overall system cost and facilitates compact implementations suitable for dense antenna arrays.

For simplicity, the control system is presented for the case of a 2x4 (8–cell) phased array, although the architecture is scalable and can be extended to larger arrays. Each 1x4 subarray is associated with a single control block. From this point forward, an antenna element in the phased array will be referred to as a cell for simplicity.

4.2 Control System Block Diagram

This section presents the block diagram of the proposed wirelessly powered control system and describes the functionality of its main building blocks. The system architecture consists of a transmitter that generates the ASK–PWM modulated signal and multiple receivers that harvest the transmitted power while simultaneously recovering the clock and data signals. Each receiver contains three primary subsystems: the RF rectifier and power conditioning circuitry, the ASK–PWM demodulator and decoder, and the digital control back–end responsible for data routing and DAC control.

In this work, the control system consists of one transmitter and two receivers. The transmitter is composed of a data generator, an RF generator, a mixer, a PA, and a transmit antenna, as shown in **Figure 4.2**(a). The data generator produces a level–shifted digital PWM signal in which the high–level pulse width is quantized depending on the transmitted bit. Specifically, narrow and wide pulses represent the transmission of “0” and “1” bits, respectively.

The RF generator produces a carrier signal that is combined with the PWM signal using a mixer to generate an ASK–PWM modulated waveform. This modulated signal is then amplified by the PA before being transmitted wirelessly through the transmit antenna.

The two receivers are identical in design, with their respective chip IDs defined externally. As illustrated in **Figure 4.2**(b), each receiver is composed of three main functional blocks. The first block consists of the RF rectifier and PMU circuitry responsible for harvesting and regulating the received wireless power into multiple outputs. The second block is the ASK–PWM demodulator and decoder, which extracts the clock and data signals from the received modulated waveform. The third block is the receiver back–end, which contains the digital frame router and the DACs used to generate the analog control

signals for the beam–steering circuitry. Further details of these blocks are provided in the following subsections.

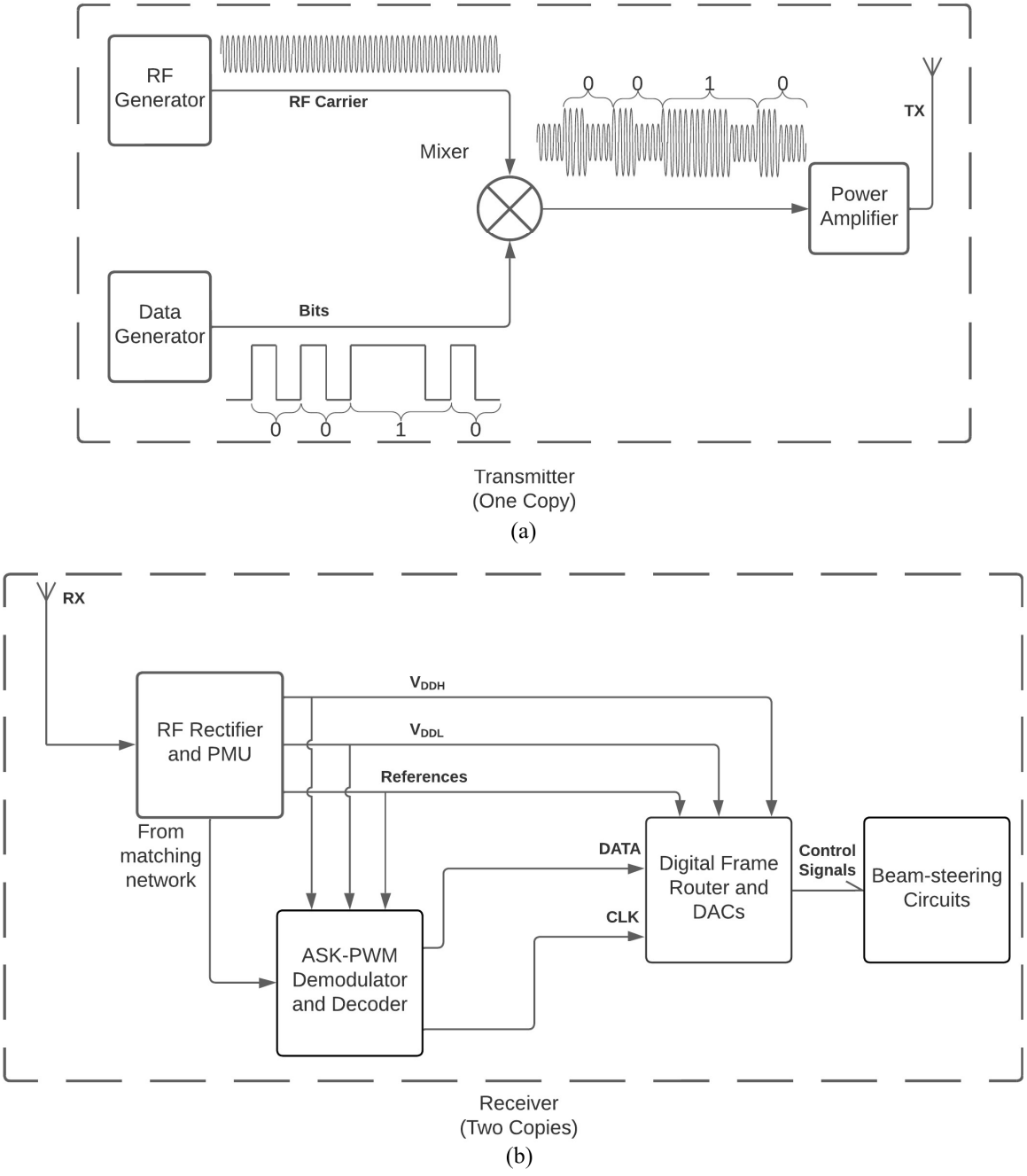


Figure 4.2 Block diagram of the control system: (a) transmitter, and (b) the two receivers.

4.2.1 RF rectifier and PMU

The purpose of this block is to harvest the required energy to power both the ASK–PWM demodulator and decoder block as well as the digital frame router and DACs. **Figure 4.3** shows the block diagram of the RF rectifier and power conditioning modules. The receiving antenna is connected to a matching network, whose output feeds both the ASK–PWM demodulator and decoder block and the RF rectifier.

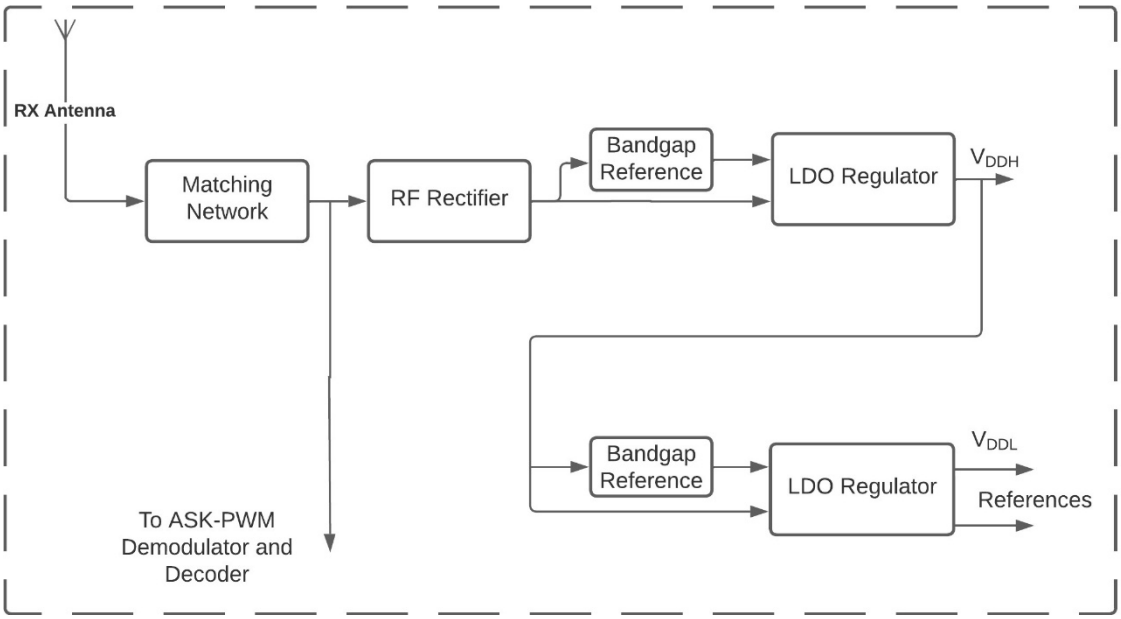


Figure 4.3 Block diagram of the RF rectifier with power conditioners.

The RF rectifier converts the received RF power into DC power, as was described in Subsubsection 3.2.3.2. A bandgap reference is used to generate a stable reference voltage, which is then regulated by an LDO regulator to produce a stable supply voltage (V_{DDH}) suitable for the analog circuitry (Subsubsection 3.2.3.4). This regulator also drives an additional bandgap reference used by a second LDO regulator to generate a lower supply voltage suitable for the digital switching circuits (V_{DDL}). In addition, this LDO provides multiple stabilized reference voltages that are used by the comparator circuits.

Further details of this power conditioning architecture will be presented in Chapter 7, where the IC implementation is described.

4.2.2 ASK-PWM demodulator and decoder block

The ASK–PWM demodulator and decoder block from Subsubsection 3.3.1.2 is shown in **Figure 4.4**. It consists of an envelope detector, a dynamic reference generator, comparators, a skewed buffer, a clock buffer, and a delay unit. The annotated voltages in **Figure 4.4** are illustrated in **Figure 4.5** for the case of an input pattern of "0010", where "0" corresponds to a narrow high pulse and "1" corresponds to a wide high pulse.

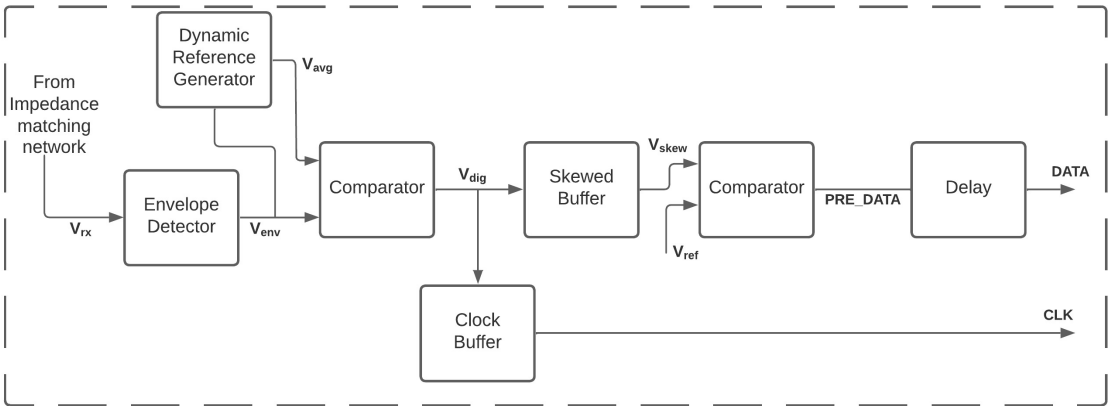


Figure 4.4 Block diagram of ASK–PWM demodulator and decoder [22].

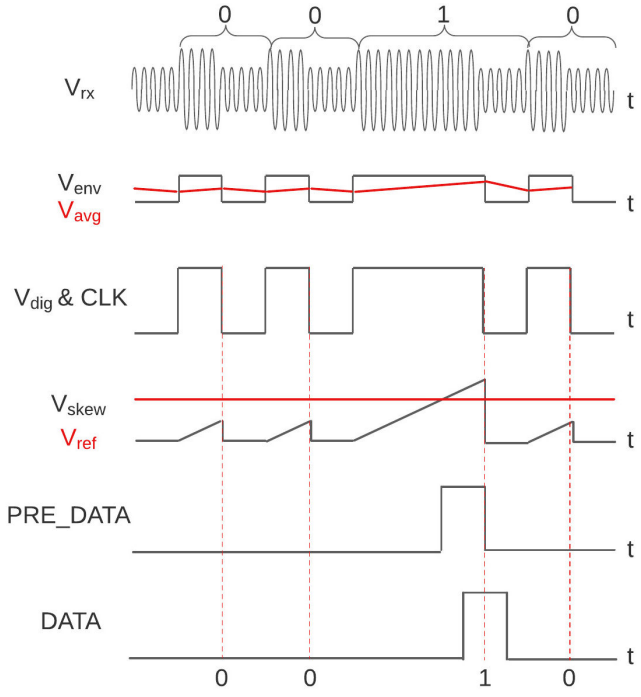


Figure 4.5 A conceptual plot of the waveforms of the ASK–PWM demodulator and decoder.

The received modulated RF voltage, V_{rx}, is obtained from the output of the matching network and passed to the envelope detector, which extracts the envelope of the modulated signal, producing V_{env}. The dynamic reference generator then tracks the envelope's upper and lower peaks and outputs their average as V_{avg}. Because V_{env} is a Non–return–to–zero (NRZ) signal, it must be converted into an RZ signal for proper decoding. This conversion is achieved using a comparator that receives both V_{env} and V_{avg} as inputs, generating the digital pulse signal V_{dig}. This signal, serving as the recovered clock, is buffered to form the final clock output CLK. Up to this stage, the ASK modulation has been successfully demodulated into digital pulses. Notably, the clock is extracted directly from the received signal without requiring additional clock generation circuitry such as PLLs.

Next, V_{dig} passes through a skewed buffer. For low–to–high input transitions, the buffer introduces a high skew producing a slow, nearly linear voltage rise, while for high–to–low transitions it exhibits a rapid, almost instantaneous voltage transition. The resulting output, V_{skew}, represents a "0" for a narrow–high input pulse and a "1" for a wide–high input pulse. This signal is then fed into another comparator that compares V_{skew} with a fixed reference voltage V_{ref}, positioned midway between the levels corresponding to short and long skews.

At this point, both the ASK and PWM components of the received signal have been demodulated and decoded, producing the PRE_DATA signal that contains the transmitted information. Visually from **Figure 4.5**, it can be observed that the ASK modulation encodes amplitude variations used to recover the CLK signal, while the PWM modulation encodes pulse–width variations that define the transmitted bit values.

It is essential to ensure proper synchronization between the CLK and PRE_DATA signals. As observed in the waveform of PRE_DATA in **Figure 4.5**, its falling edge coincides with the falling edge of the CLK signal. Since the subsequent stage will be a negative–edge–triggered shift register, PRE_DATA must be delayed relative to CLK so that the falling edge of CLK occurs approximately at the midpoint of the delayed PRE_DATA pulse (referred to as $DATA$) as illustrated by the third dashed red line from the left in **Figure 4.5**. With this timing adjustment, each falling edge of CLK triggers the shift register to capture the corresponding $DATA$ bit in its flip–flops. In **Figure 4.5**, four negative clock

edges are visible, and their alignment with the $DATA$ waveform enables correct detection of the transmitted bit sequence "0010," matching the received sample.

It is worth noting the advantage of this self–synchronizing approach, which reduces both circuit complexity and area by eliminating the need for additional clock–generation circuitry such as PLLs. Furthermore, it removes the requirement for global synchronization among control blocks, unlike the SPI–based protocol approach.

4.2.3 Digital frame router and DACs

The digital frame router and DACs, shown in **Figure 4.6**, consist of a shift register, an acknowledgment block, an acknowledgment reset block, a control block identifier, an ID selector, a cell identifier, delay blocks, a data holder, a data director, and DACs. The $DATA$ and CLK signals used by this block are generated by the ASK–PWM demodulator and decoder described in the previous subsection. Here, the DAC resolution will be defined as 4–bits and the RF attenuators will be omitted due to FPGA General–Purpose Input/Output (GPIO) pin count limitations as will be discussed in next chapter.

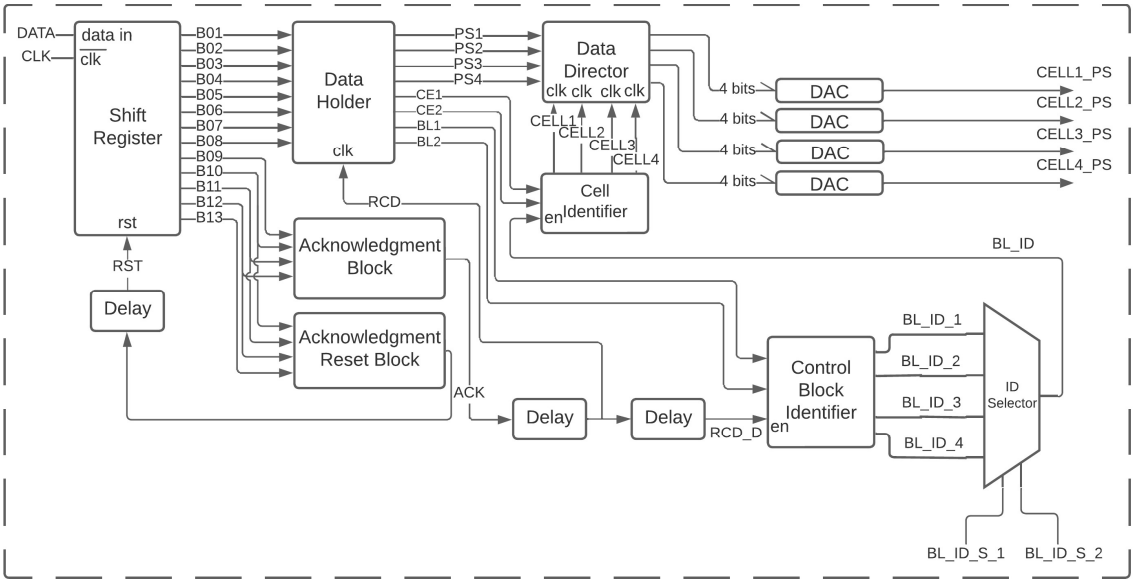


Figure 4.6 Digital frame router and DACs block diagram.

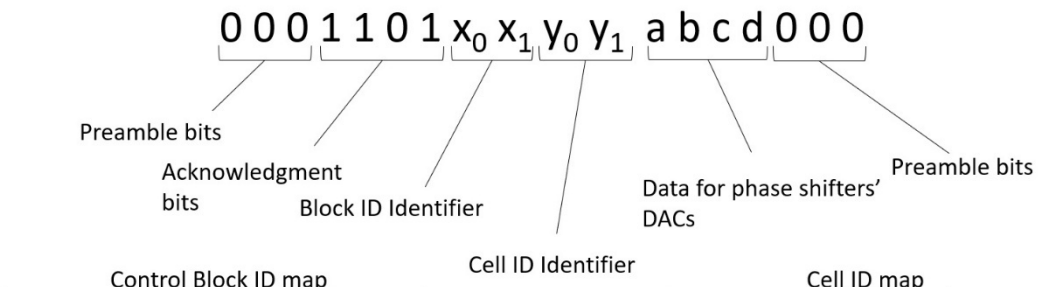
The shift register is implemented using cascaded negative–edge–triggered D flip–flops, where the Q output of each flip–flop is connected to the D input of the subsequent stage. A common reset signal is applied to all flip–flops (rst pin) except the final stage, which does not include a reset input for the purpose of defining a reset timing via a bit word, as will be discussed. The length of the shift register is determined by the control system functionality and is therefore configured to contain 13 flip–flops.

The outputs of the shift register correspond to the received data frame. Bits $B01 - B04$ (**Figure 4.6**) are used to control the phase shifter. Bits $B05 - B06$ are assigned for cell identification, indicating which antenna cell's phase shifter is to be controlled. Bits $B07 - B08$ serve as the control block identifier, determining whether the control block should accept the incoming data. Bits $B09 - B12$ form the acknowledgment field, which confirms that a valid data sample is being received, while bits $B10 - B13$ are allocated to the acknowledgment reset block used to clear the shift register contents.

The corresponding bit frame for a data sample is shown in **Figure 4.7**. The acknowledgment field is defined as "1101", the control block identifier bits are represented as "x_1x_0", while the cell identifier bits are "y_1y_0". The data bits applied to the DAC that controls the phase shifter are "abcd", where "a" represents the most significant bit (MSB).

Additionally, the control block ID and cell ID truth tables are used to identify the target control block and antenna cell for data routing. A spacing bit stream of "000" is inserted between consecutive samples to initiate the reset phase.

There are two main reasons for selecting "1101" as the acknowledgment bit pattern. First, the placement of the '0' bit ensures that the acknowledgment cannot be unintentionally retriggered. After a subsequent clock event, the '1' bit shifts into the position previously occupied by the '0', forcing the acknowledgment signal to return to a low state.



Control Block ID map

Block	x_0	x_1
Block 1	0	0
Block 2	0	1
Block 3*	1	0
Block 4*	1	1

*Not used in this work

Cell ID map

Cell	y_0	y_1
Cell 1	0	0
Cell 2	0	1
Cell 3	1	0
Cell 4	1	1

Figure 4.7 Data pattern used for decoding the control information.

Second, the same bit pattern is reused to reset the shift register. Using a uniform reset pattern such as all ‘1’s or all ‘0’s could lead to a latched reset condition during system start–up. By employing a nonuniform code such as “1101”, the proposed approach mitigates the risk of the system entering a persistent reset state during initialization.

One may question the need for a multi–bit reset word instead of a single clearing bit (e.g., logic ‘1’). A single–bit reset signal would be susceptible to spurious occurrences of that bit during normal operation, potentially resetting the shift register even when a meaningful data word is being received. Such behavior could interrupt valid data acquisition. In contrast, requiring a specific multi–bit reset sequence ensures that the reset operation is triggered only intentionally, thereby enabling reliable delivery of control data without unintended resets.

At the output of the shift register shown in **Figure 4.6**, bits $B01 - B08$, which include the DAC data, cell ID, and control–block ID fields, are captured by the data holder block. The data holder consists of positive–edge–triggered flip–flops connected in a configuration similar to the shift register but without reset functionality. Its purpose is to retain valid data for subsequent processing by the cell identifier, control–block identifier, and data director blocks.

The acknowledgment and acknowledgment reset blocks are identical and implemented using combinational logic. Each block generates a high ACK or RST output, respectively, only when the keyword "1101" is detected. The inputs to these two blocks are offset by one bit, such that the ACK signal is triggered prior to the RST signal.

The acknowledgment output is then passed through two delay stages. The first delay stage ensures that the data stream at the shift–register outputs has stabilized before being captured by the data holder. The output of this stage, referred to as RCD (record), triggers the data holder to store the received data. The second delay stage produces the signal RCD_D, which serves as the enable input to the control–block identifier. This additional delay guarantees that the data holder has successfully latched the data before the control–block identification logic is activated. Consequently, both the control–block ID and cell ID checks are performed only after valid data have been recorded, ensuring correct delivery of control data to the DACs.

The inclusion of the data holder serves two primary purposes. First, it enables precise identification of the end of a valid data sample through the delayed acknowledgment signal, allowing meaningful data from the shift register to be reliably captured and stored for processing. Second, since the shift register continuously processes incoming samples without interruption, the data holder allows previously received data to be analyzed while the shift register simultaneously acquires the next sample.

It is important to note that both the acknowledgment and acknowledgment reset blocks operate directly on the continuously updating outputs of the shift register. If these blocks were instead driven by the data holder, their inputs would no longer reflect real–time data, which could cause the logic to latch and prevent correct system operation.

All control blocks are architecturally identical and differ only in their assigned identifiers. Two approaches can be used to implement these identifiers. In the first approach, each control block incorporates a unique combinational logic circuit to distinguish it from the others. While functionally effective, this method increases design complexity, raises fabrication costs, and limits the scalability of the array.

The second approach, adopted in this thesis work, maintains a common control–block architecture while allowing the control block ID to be defined externally. Specifically, each control block contains all possible ID values internally, and an internal multiplexer (ID selector) selects the active ID based on external control bits ($BL\_ID\_S\_1$ and $BL\_ID\_S\_2$), as shown in **Figure 4.6**. This external ID assignment can be implemented using a read–only memory (ROM) programmed after IC fabrication or through dedicated external connections driven by on–chip reference signals (to avoid off–chip select pins as in SPI interface).

By defining the control block IDs externally, all chips remain identical at the design and fabrication levels while still supporting unique identifiers at the system level. This approach significantly reduces integration costs and improves scalability for large phased–array systems.

Once the control block ID has been assigned, each control block uses its identifier to determine whether incoming data should be accepted or rejected through the control block identifier. The control block identifier is implemented as a 2–to–4 decoder with an enable input, receiving the two bits $BL1$ and $BL2$ from the data holder.

The cell identifier is implemented as a 2–to–4 decoder with an enable input as well. As shown in **Figure 4.6**, the enable input is driven by the output of the control block identifier through the multiplexer (BL_ID). Consequently, once the control ID output is asserted, the cell identifier becomes active and produces a high output at one of the decoder outputs corresponding to the selected antenna cell. The two outputs from the data holder, $CE1$ and $CE2$, serve as the inputs to the decoder.

The outputs of the cell identifier are connected to the clock inputs of the data director block. The data director consists of four internal 4–bit data holders, as shown in **Figure 4.8**. The data inputs of these internal holders are connected to the outputs of the outer data holder ($PS1 - PS4$), while their clock signals are individually controlled by the outputs of the cell identifier.

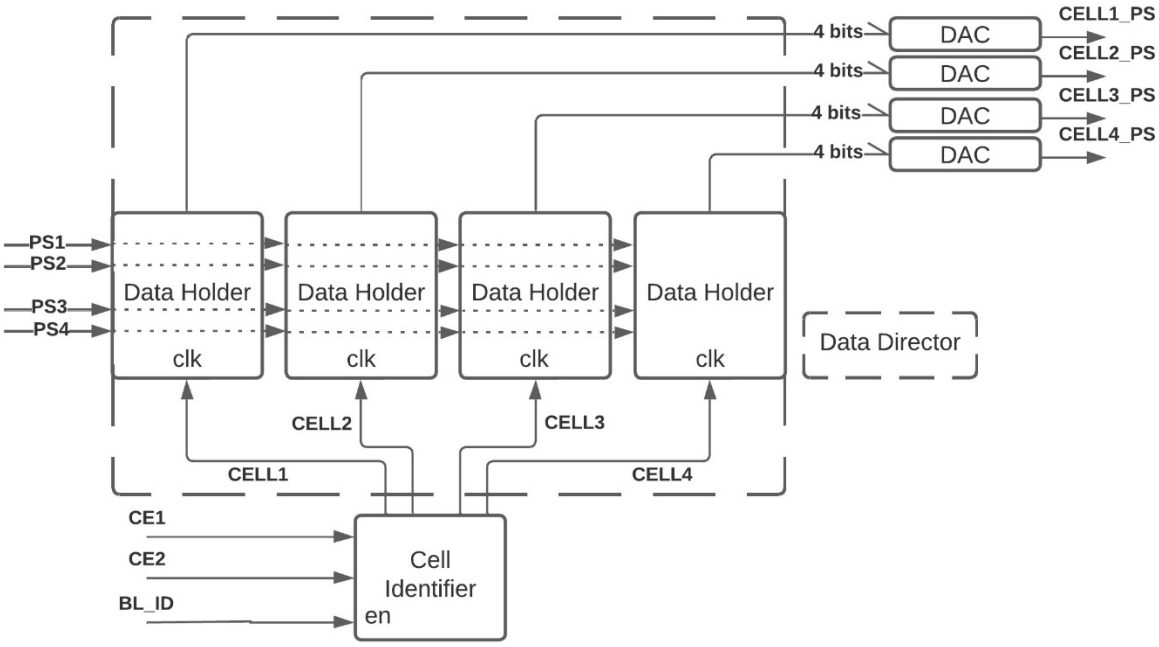


Figure 4.8 Block diagram of the data director.

For example, when $CELL1$ is selected, the corresponding internal data holder in the data director is triggered on the positive clock edge in **Figure 4.8**. This action routes the DAC control bits ($PS1 - PS4$) to the phase shifter associated with cell 1, producing the analog control $CELL1\_PS$ signal.

4.3 Timing Analysis Example

To further illustrate the operation of the control system, the following example is considered. The objective is to transmit the data word "1001" to the phase shifter of cell 1 on control block 1, both of which are assigned the identifier "00". Based on the bit sequence defined in **Figure 4.7**, this control frame is encoded into the serialized data pattern "110100001001000".

The timing analysis of the shift–register terminals is shown in **Figure 4.9**, which illustrates the input clock signal along with all output bits of the shift register. As observed in the figure, the waveforms exhibit the expected behavior of a conventional shift register. The discussion here focuses on the regions highlighted in red.

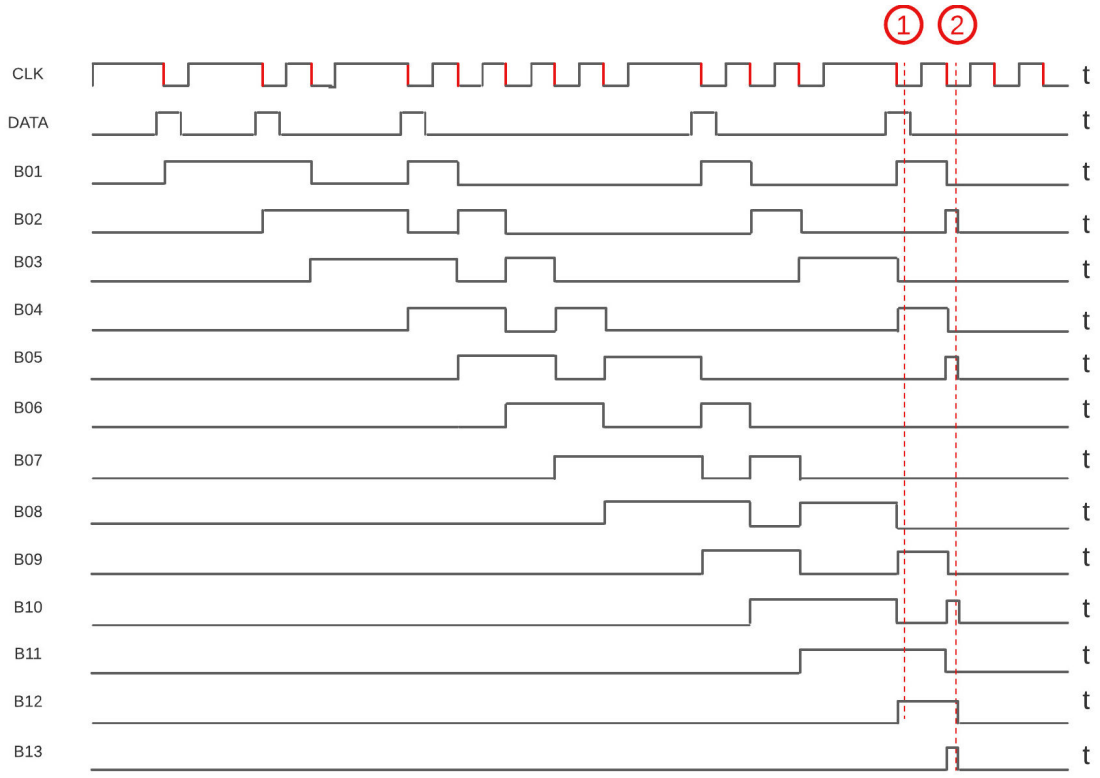


Figure 4.9 A conceptual plot of the waveform of the shift register.

At each negative edge of the CLK signal, a bit is generated based on the pulse width of CLK, and the data are shifted to the subsequent flip–flop, consistent with negative–edge–triggered shift–register operation. After 12 negative clock edges, flip–flops 9–12 contain the correct acknowledgment pattern. Following a short delay, this pattern produces a logic–high RCD signal (see **Figure 4.6**), thereby enabling the data to be captured by the data holder. This event occurs at the dashed line labeled ① in **Figure 4.9**. At this instant, the data bits are precisely aligned, highlighting the necessity of the intentional delay following acknowledgment detection.

After one additional negative–edge CLK transition, the acknowledgment pattern propagates to the acknowledgment–reset block. Following another short delay, the reset signal is asserted, clearing the shift register and preparing it to accept new control data. This delayed reset event is indicated by the dashed line labeled ② in **Figure 4.9**.

While the timing analysis of the shift register is critical, the timing behavior of the subsequent blocks must also be carefully examined. Continuing with the same example, additional key timing regions between the dashed lines ① and ② in **Figure 4.9** are highlighted in **Figure 4.10**.

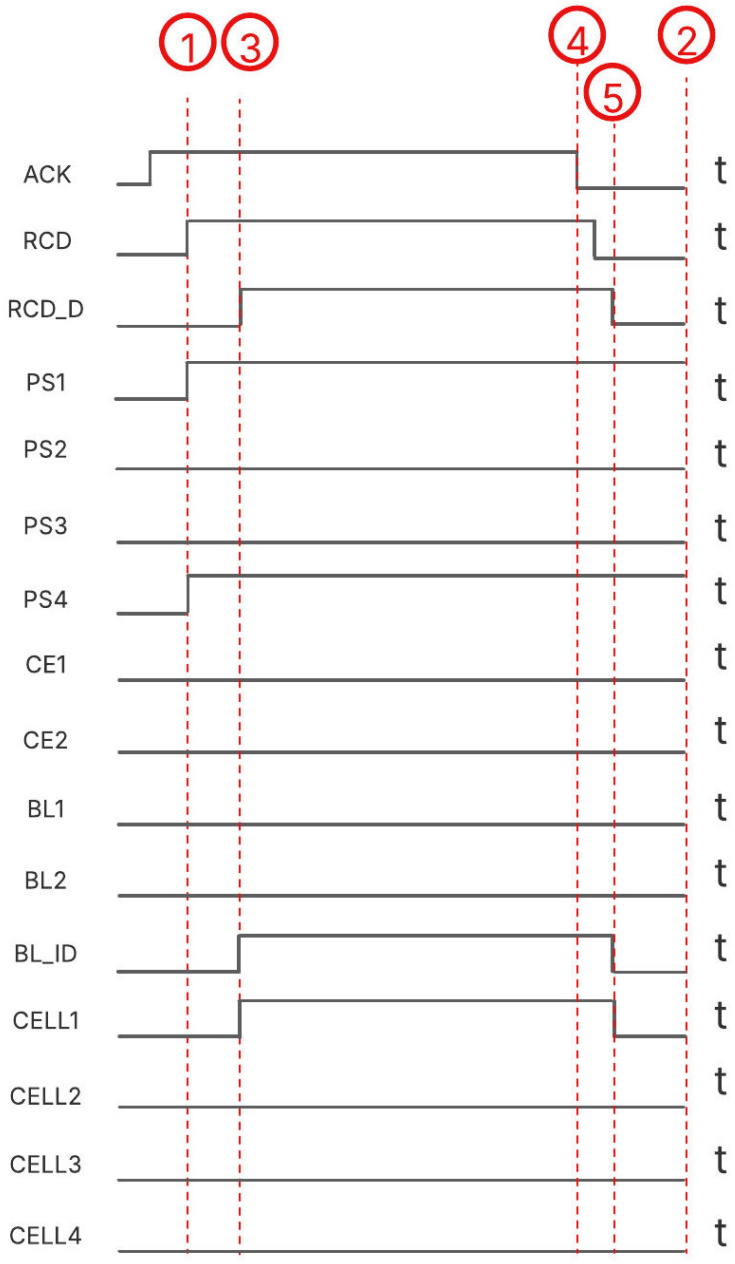


Figure 4.10 Waveforms of subsequent blocks of the shift register.

As shown in **Figure 4.10**, marker ① corresponds to the triggering of the RCD signal. At this instant, all data present at the output of the shift register are latched into the data holder. By aligning the shift–register outputs (**Figure 4.6**) with the data–holder inputs at the dashed line ①, it can be observed that the signals $PS1$, $PS2$, $PS3$, $PS4$, $CE1$, $CE2$, $BL1$, and $BL2$ are updated according to the received data pattern.

Specifically, both $BL1$ and $BL2$ are set to "0", consistent with the transmitted data. Likewise, $CE1$ and $CE2$ are both "0", indicating communication with control block 1 and cell 1, as intended in this example. The signals $PS1$ and $PS4$ transition to a high state, while $PS2$ and $PS3$ remain low, resulting in the correctly decoded phase shifter control word "1001".

Once the correct data have been stored, the next step is to route the data to the appropriate cell within the targeted control block. This operation occurs after an additional delay following the trigger of RCD, indicated by the dashed line ③ in **Figure 4.10**, corresponding to the RCD_D signal. At this point, the control–block identifier logic in all control blocks is enabled, allowing each block to evaluate the received ID data. In this example, only control block 1 accepts the data, while the other control block rejects it.

After control block 1 is selected, its control–block identifier produces a high output that enables the cell identifier logic. Consequently, only $CELL1$ is asserted high according to the selected cell ID, while the remaining cell signals remain low. This action routes the decoded data to the correct DAC of the phase shifter associated with cell 1.

After a certain period, the ACK signal returns to a low state, as indicated by the dashed line ④. Consequently, both RCD and RCD_D also return to low after their respective delays. At the falling edge of the RCD_D signal, highlighted by ⑤ in **Figure 4.10**, all control–block and cell–identifier signals are disabled. As a result, any errors originating from the shift register such as output glitches caused by the reset event at the dashed line ②, or subsequent changes in the shift–register outputs do not affect the data holder until a new valid acknowledgment sequence is detected.

This timing behavior ensures that the stored data remain intact and significantly improves the robustness of the system against transient errors.

4.4 Simulink Model and Simulations

This section presents the Simulink model developed to verify the operation of the proposed control system at the system level. The model includes the main functional components of the architecture, namely the transmitter, the wireless channel, the ASK–PWM demodulator and decoder, the digital frame router, and the DACs. Through this model, the end–to–end communication process from data generation and modulation at the transmitter to data decoding, routing, and DAC control at the receiver can be evaluated to confirm the correct functionality of the proposed control scheme.

The purpose of these simulations is to provide a preliminary verification of the control architecture and the data communication protocol before circuit–level implementation. It should be noted that the RF rectifier and PMU subsystems are not included in this Simulink model. The performance of the RF rectifier and power conditioning circuitry depends strongly on the target technology and the power consumption of the control block. Therefore, the design and analysis of the MPT circuitry will be addressed separately in Chapters 6 and 7 as part of the PCB and IC implementations, respectively.

Figure 4.11 shows the Simulink implementation of the transmitter and the ASK–PWM demodulator and decoder. Starting from the transmitter side, a Signal Generator block is used to generate the RF carrier at 1 GHz. The input bit sequence is generated using a Repeating Sequence Stair block. In this implementation, a narrow pulse representing a logical “0” has a period of 1 μs with a 50% duty cycle, while a wide pulse representing a logical “1” has a period of 3 μs with an 83.33% duty cycle.

The RF carrier and the generated bit sequence are then mixed to produce the ASK–PWM modulated signal, which is received by the first stage of the receiver front–end, namely the envelope detector. The envelope detection process is implemented using a squaring and low–pass filtering technique. In this approach, the received signal is first squared, then multiplied by a gain of 2 to restore the original signal energy. The signal is subsequently down–sampled and passed through a low–pass filter to remove high–frequency components. Finally, a square–root operation is applied to compensate for the amplitude scaling introduced by the squaring process.

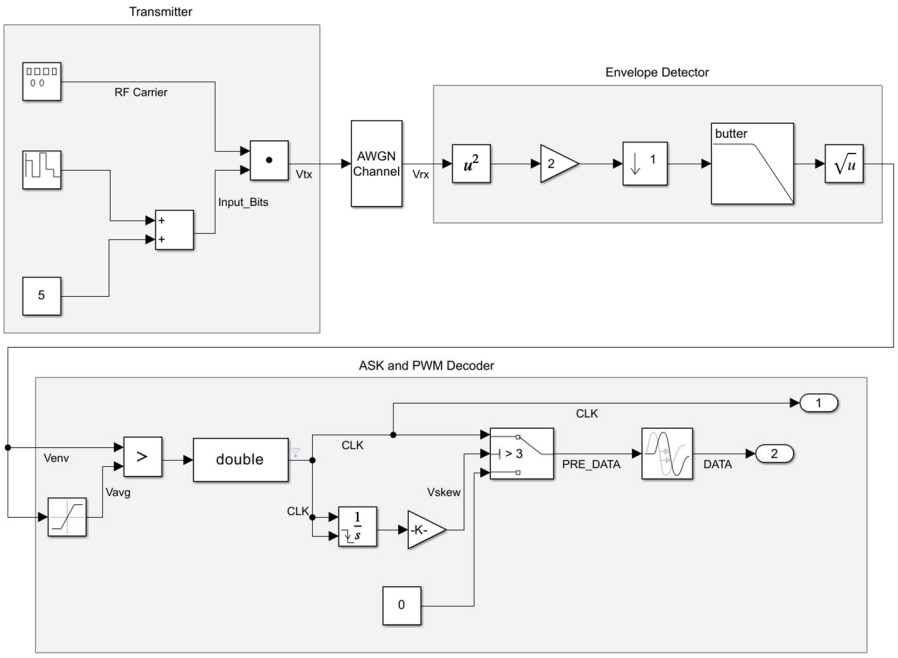


Figure 4.11 Simulink implementation of the transmitter and ASK–PWM demodulator and decoder.

The envelope signal V_{env} obtained from the envelope detector is first compared with a dynamically generated reference voltage V_{avg}. This comparison is performed using a relational operator block, which produces a digital pulse whenever V_{env} exceeds V_{avg}. The resulting signal represents the recovered ASK waveform (CLK).

To extract the PWM information embedded in the pulse width of the clock signal, the recovered CLK is processed through an integrator with reset, configured to reset on the negative edge of the clock. The integrator gain K is set to 2×10^6 to produce the desired slope for the integration process. This structure emulates the behavior of the skewed buffer described in Subsection 4.2.2, generating the signal V_{skew}, whose amplitude increases proportionally with the pulse width of the input signal.

The V_{skew} signal is then applied to a switching block that compares it against a predefined threshold value (greater than 3 in this model). Based on this comparison, the block produces the signal PRE_DATA, which represents the decoded data before synchronization. Finally, a delay block synchronizes PRE_DATA to generate the final $DATA$ signal, ensuring proper alignment between the clock and the decoded data bits.

This Simulink implementation therefore reproduces the functional behavior of the ASK demodulator and PWM decoder, enabling verification of the clock recovery and data decoding processes prior to hardware implementation.

The resulting waveform simulations obtained from the Simulink model in **Figure 4.11** are presented in **Figure 4.12**. The results verify the correct operation of the ASK–PWM transmitter and receiver. As illustrated by the green thin lines, the negative–edge transitions of the CLK signal represent the sampling instants, where narrow high pulses are interpreted as bit "0" and wide high pulses as bit "1."

Figure 4.13 shows the nine primary blocks of the frame router implemented in Simulink: the shift register, acknowledgment block, acknowledgment reset block, control block identifier, ID selector, cell identifier, data holder, data director, and DACs. The structure follows the same architecture described previously for the digital control system in Subsection 4.2.3.

It should be noted that the delay elements used in this Simulink model are implemented as time–defined delays to emulate the required timing relationships between signals. In practical hardware implementations, these delay elements will be realized differently depending on the design stage. Specifically, the synthesized digital implementation described in Chapter 5 and the IC realization presented in Chapter 7 will employ technology–dependent delay structures suitable for their respective platforms.

Figure 4.14 shows the Simulink implementation of the testbench used for control system verification, modeling two digital frame routers with different control block IDs. To create a comprehensive test setup, an ASK–PWM modulator and a pair of ASK–PWM demodulators and decoders were included in the simulation. In addition, each digital frame router contains four 4–bit DACs that generate the control outputs $PS1 - PS4$ for each control block. In this setup, the $BL\_ID\_S\_1$ and $BL\_ID\_S\_2$ bits are set to "00" for control block 1 and '01' for control block 2 using the ID selector as shown in **Figure 4.14**.

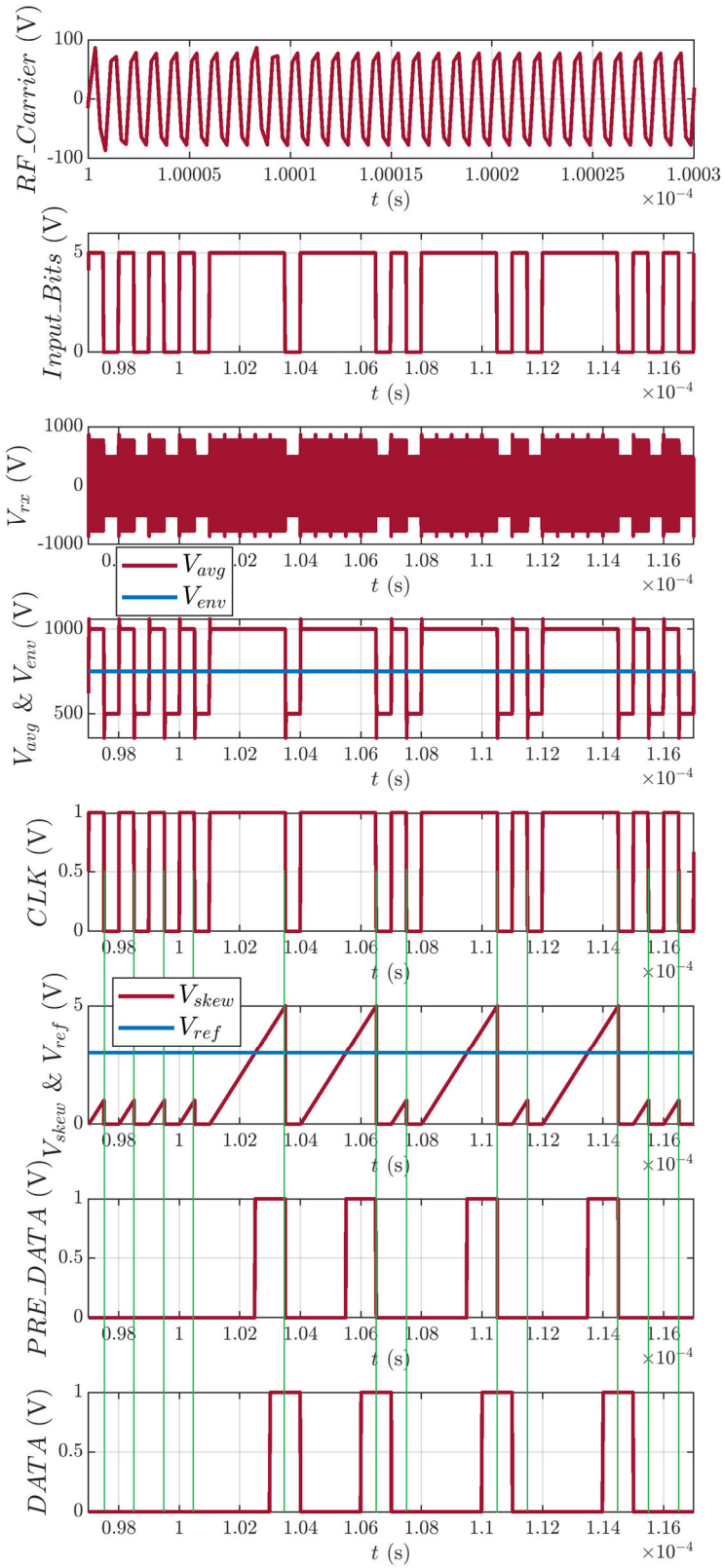


Figure 4.12 Waveform simulations of Simulink model of the transmitter and ASK–PWM demodulator and decoder.

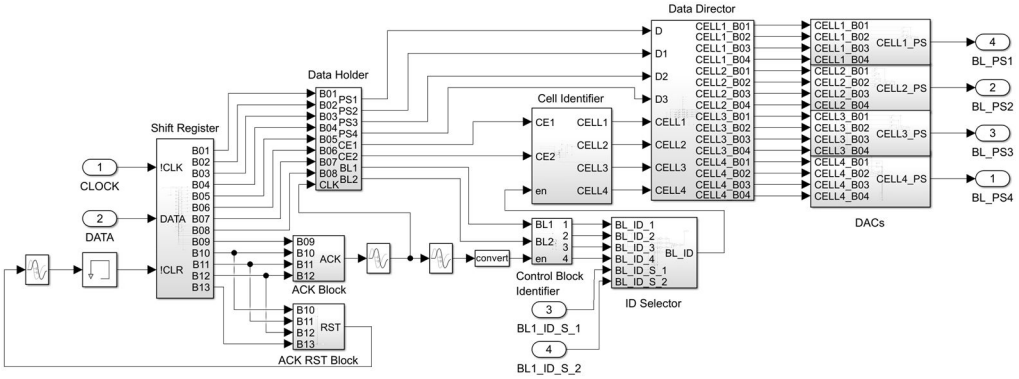


Figure 4.13 Simulink model of the digital frame router and DACs.

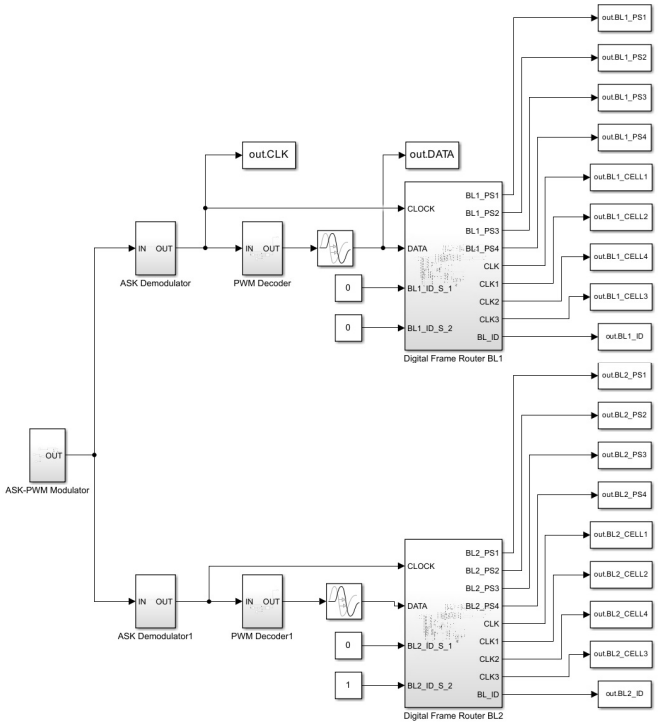


Figure 4.14 Simulink testbench of the control system.

To demonstrate the full capabilities of the control system, a data pattern was generated that first updates the DACs output voltages of the four cells (in numerical order) of control block 1, followed by the four cells (again in order) of control block 2. The data patterns consist of a variety of bit values to validate correct digital frame router operation under different pulse–width conditions, since the total frame duration varies depending on the number of logic “1” bits.

Figure 4.15 presents the simulated waveforms of the digital frame routers, highlighting the key system signals. The inputs to the routers are the recovered CLK and $DATA$ signals shown in **Figure 4.15**(a) and (b), respectively. **Figure 4.15**(c) shows the acknowledgment signal (ACK) being triggered eight times, corresponding to the eight control samples transmitted to control blocks 1 and 2, after which an ID check is performed. **Figure 4.15**(d) shows that the first four BL_ID outputs are asserted for control block 1, enabling its cell identifier block, followed by the assertion of the remaining four BL_ID outputs for control block 2, activating its corresponding cell identifier.

Figure 4.15(e) shows the cell identifier outputs for both control blocks. As observed, the cells are triggered sequentially with order of control blocks as intended, correctly routing the incoming data to the appropriate DACs. The resulting DAC control voltages are shown in **Figure 4.15**(f). These two digital frame routers will subsequently be synthesized on an FPGA for measurement–based validation, as will be presented in Chapter 5.

The simulation results demonstrate the correct operation of the proposed control architecture. Through the developed Simulink model, the ASK–PWM transmitter and receiver were successfully implemented and verified, confirming proper clock and data recovery. In addition, the operation of the digital frame routers was validated, demonstrating correct data routing to the intended control blocks and antenna cells, as well as proper generation of the DACs control signals. These system–level simulations provide an important preliminary validation of the proposed architecture prior to hardware implementation.

4.5 Conclusion

This chapter presented and validated the system–level architecture of the proposed wirelessly powered ASK–PWM control system for phased–array beam–steering. The transmitter and receiver architectures were described in detail, including the RF rectifier and power conditioning circuitry, the ASK–PWM demodulator and decoder, and the digital frame router responsible for data routing and DAC control. A timing–analysis example

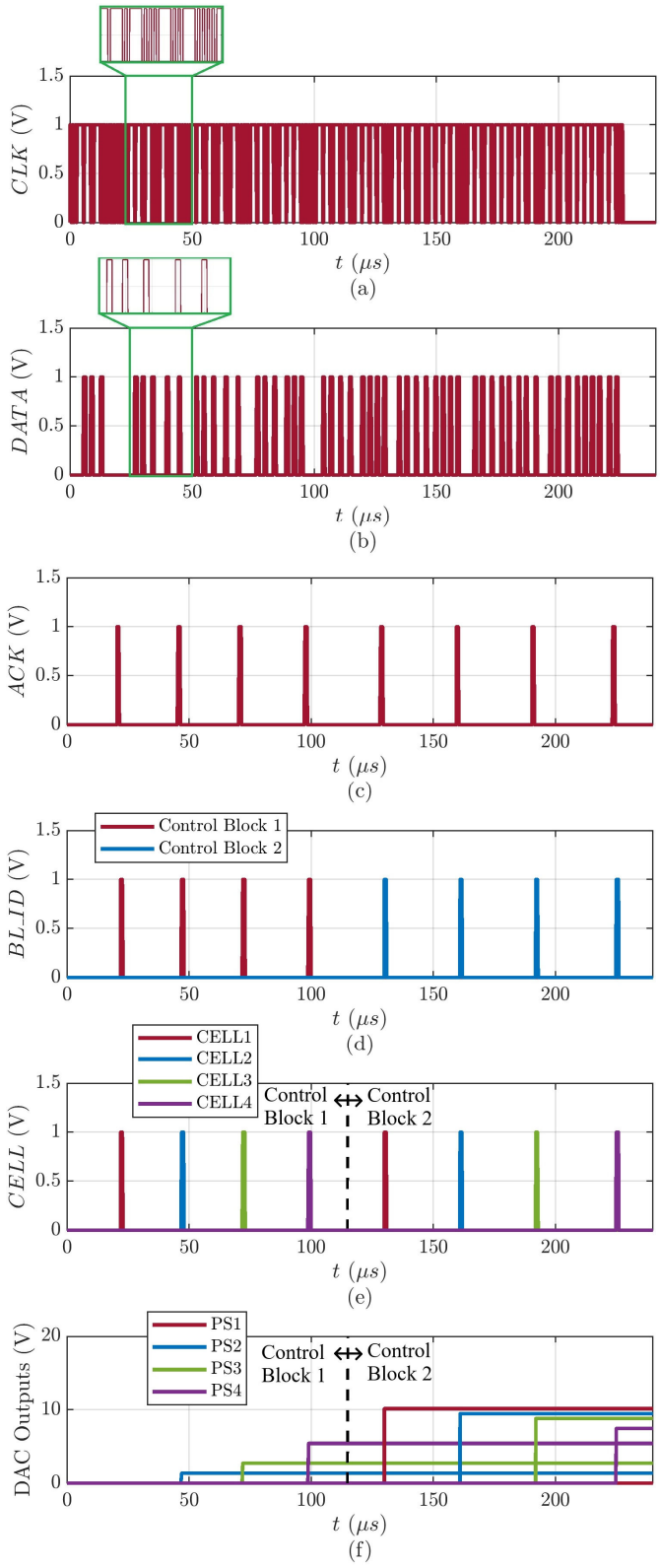


Figure 4.15 Simulink testbench simulation waveforms showing: (a) *CLK*, (b) *DATA*, (c) *ACK*, (d) *BL_ID*, (e) *CELL* outputs, and (f) DAC outputs.

illustrated how serial ASK–PWM frames are decoded, synchronized, and converted into parallel control signals that are routed to appropriate control blocks and antenna cells.

System–level verification was performed using a comprehensive Simulink model that included the transmitter, wireless channel, ASK–PWM demodulator and decoder, digital frame router, and DAC blocks. The simulation results confirmed correct clock recovery from the ASK envelope, accurate PWM decoding of narrow and wide pulses to recover the data, reliable frame recognition, and proper routing of DAC control data through the TDMA–based addressing scheme. These results validate the feasibility of the proposed architecture prior to hardware implementation.

More importantly, the proposed wirelessly powered ASK–PWM control system highlights the key advantages proposed in this thesis. By utilizing WPT, wired power sources, power distribution networks, and power feeding pins can be eliminated on board. By embedding both the clock and data within the transmitted WPT carrier, the system eliminates the need for dedicated clock–tree distribution and conventional SPI–based communication interfaces, allowing for one–input–pin–per control block approach. This significantly reduces routing complexity, minimizes the number of feeding pins and PCB layers, and simplifies interconnections within phased–array modules while enabling scalable control of multiple distributed control blocks using TDMA–based control strategy.

With the functional feasibility of the proposed architecture established, this chapter paves the way for the remainder of the thesis. Chapter 5 presents the PCB implementation of the ASK–PWM receiver, along with the synthesized digital frame router implemented on an FPGA to demonstrate beam–steering capabilities through DAC–controlled phase shifters. Chapter 6 investigates the practical realization of the wirelessly powered ASK–PWM receiver on PCB, where the RF rectifier and associated circuits are prototyped and the challenges associated with implementing WPT on a PCB platform are addressed. Chapter 7 then presents the IC realization of the proposed architecture, with particular emphasis on the RF rectifier, PMU, the communication block, and digital control blocks. Finally, Chapter 8 demonstrates the complete proof–of–concept system by utilizing the ICs to operate a beamformer, validating the effectiveness of the proposed approach in a practical beam–steering application.

Chapter 5: Synthesized Digital Control and ASK–PWM PCB Prototype

This chapter presents the experimental validation of the proposed control architecture through the synthesis and hardware prototyping of the digital frame router, the ASK–PWM interface, and the DACs. The digital frame routing is implemented using an FPGA–based synthesis together with multiple PCB prototypes fabricated on FR–4 substrates. The objective of these experiments is to demonstrate the practical feasibility of the proposed control scheme and to verify its ability to control beam–steering elements in phased array systems.

To progressively validate the different components of the architecture, three experimental prototypes were developed. The first two testing phases focus primarily on validating the synthesized digital frame router while simplifying the communication interface by using a digitally decoded PWM signal rather than the analog ASK–PWM signal. In these phases, the FPGA internal clock is used as the system clock and the ASK modulation and demodulation stages are omitted. This approach allows the digital frame routing architecture to be evaluated independently while assuming that the ASK envelope has already been demodulated. The synthesized system therefore consists of a digital PWM decoder and a frame router, while the DACs are implemented on PCB. The analog loads are modeled using variable capacitors (varactors) and variable resistors (varistors) to emulate RF phase shifters and attenuators. The third experimental phase then combines the ASK–PWM demodulator and decoder to the synthesized digital frame router to demonstrate the control system's operation in a beamforming experiment.

The first experimental phase evaluates a 2×2 control sub–block, representing a subarray. The prototype includes an FPGA implementing the synthesized digital PWM decoder and frame routing logic, and then four varactors are used to emulate tunable RF phase shifters, and four varistors are used to emulate RF attenuators. The analog control voltages are generated using R–2R ladder DACs implemented on PCB. This experiment serves two purposes. First, it demonstrates the functionality of a single control block capable of tuning beam–steering components. Second, it illustrates the versatility of the control system by showing that the same architecture can control different RF tuning elements, including both phase shifters and attenuators.

The second experimental phase validates the ID–based addressing mechanism used by the digital frame router to direct control data to the correct control block. In this setup, a 4×4 element array is emulated, where each 2×2 group represents a subarray with a unique ID. The prototype therefore contains sixteen varactors corresponding to sixteen controllable elements. Each element is driven by a 2–bit R–2R ladder DAC. Due to the limited number of FPGA GPIO pins, the attenuator emulation using varistors was removed in this phase. The purpose of this experiment is to verify correct frame decoding, address recognition, and selective routing of control data to multiple subarrays.

Finally, the third experimental phase demonstrates the complete control system including the ASK–PWM interface. In this prototype, an ASK–PWM receiver implemented on PCB is used to recover the clock and data signals required by the FPGA control logic. This removes the need for the FPGA's internal clock and the digitally synthesized PWM decoding used in the previous prototypes, thereby validating the intended wireless non–coherent control architecture. In addition, a 2×4 phased–array system is implemented to experimentally verify beam–steering capability. The RF carrier carrying the ASK–PWM modulation is transmitted wirelessly using a signal generator, while the resulting beam patterns are measured in an anechoic chamber.

5.1 2×2 Subarray Digital Control Validation

The block diagram of the first experimental setup is shown in **Figure 5.1**. In this implementation, a PWM signal is generated by the Altera FPGA board to encode the transmitted data, where a narrow high pulse represents bit "0" and a wide high pulse represents bit "1". The clock signal is also provided by the Altera board and is synchronized with the PWM signal in a manner similar to the ASK–PWM receiver architecture presented in Subsection 4.2.2. Each cell contains both a varactor and a varistor. The varactors are used to emulate the behavior of RF phase shifters in preparation for the beamforming experiment presented in the third phase of the experimental work in this chapter. The varistors are used to emulate RF attenuators. The DAC resolution was chosen to be 4–bits,

which represents a compromise between control resolution and the limited number of GPIO pins available on the Altera FPGA board.

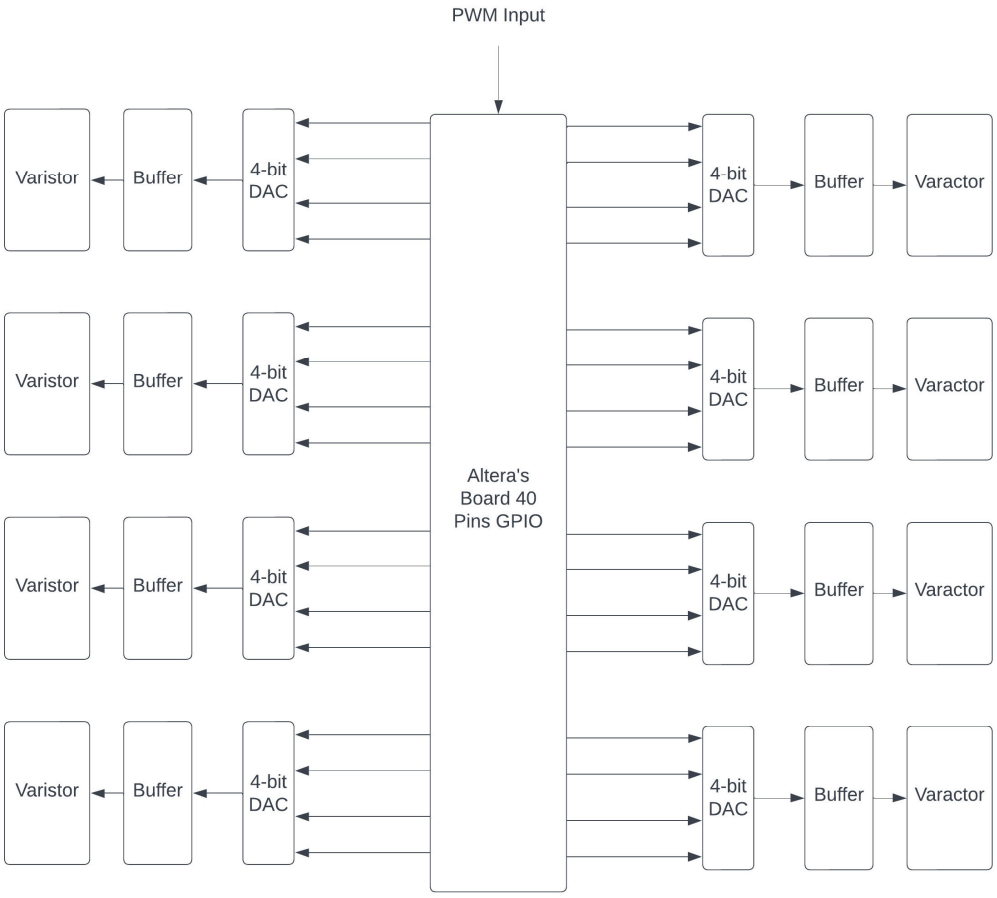


Figure 5.1 Block diagram of the 2x2 subarray prototype.

The PWM decoding in this prototype is implemented using digital logic, rather than the analog skewed–buffer approach presented in Subsection 4.2.2 and Section 4.4. This transition to a digital PWM decoder is intentionally adopted for the first two experimental phases in this chapter to simplify the communication subsystem and enable independent testing and validation of the digital frame router. Specifically, a 3–bit ripple counter is used to distinguish between narrow and wide pulses, as illustrated in **Figure 5.2**.

The digital frame router used in this experiment is largely similar to the architecture presented in Subsection 4.2.3. However, the delay cells are implemented using FPGA clocked flip–flops, which introduce controlled delays synchronized with the FPGA clock.

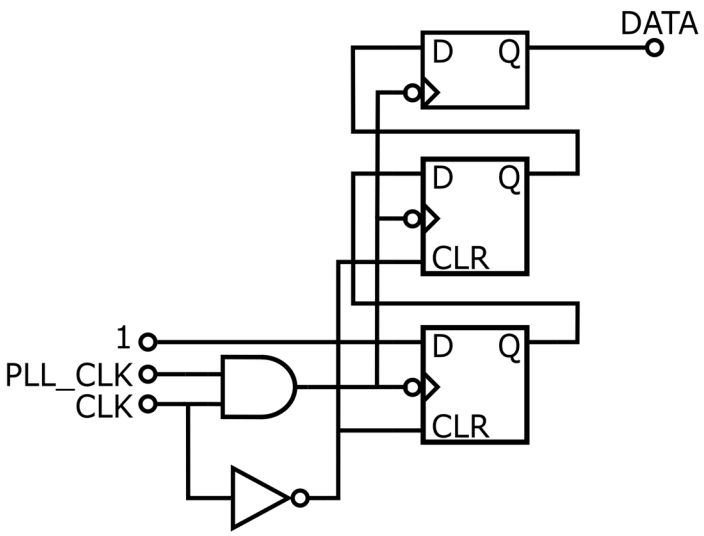


Figure 5.2 Logic gate implementation of the digital PWM decoder used for the first two experimental phases.

Figure 5.3 illustrates the operating principle of the digital PWM decoder through an example waveform. The decoder counts the negative edges of the divided FPGA's PLL (PLL_CLK) clock signal to determine whether a narrow pulse (bit "0") or a wide pulse (bit "1") has been received. As shown in the waveform, the clock is counted three times ($C = 3$) when a wide pulse is detected, resulting in the generation of a data bit "1". In contrast, when a narrow pulse is received, the clock is counted only once ($C = 1$), corresponding to data bit "0". The two bottom flip–flops shown in **Figure 5.3** are reset whenever CLK returns to a low level, ensuring that the internal counter is cleared and the $DATA$ signal is correctly captured.

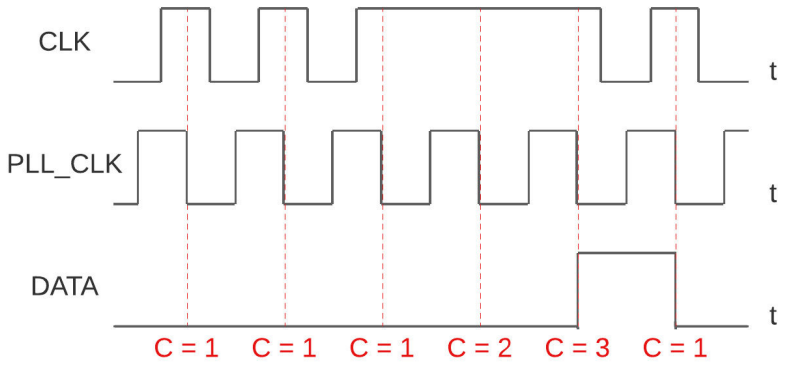


Figure 5.3 Illustrative plot of the operation of the digital PWM decoder.

In this implementation, the decoded $DATA$ signal is applied to the input of the frame router shift register (**Figure 4.6**), while CLK is used as the clock input for the shift register. This architecture requires the PLL_CLK and CLK signals to remain synchronized, which necessitates the use of the FPGA's PLL. Furthermore, the delay elements used in the frame routing logic must also be synchronized with the FPGA clock through the PLL. While this approach is suitable for this simplified prototype, it becomes problematic in larger systems containing multiple control blocks, as each block may require its own PLL for synchronization. This requirement increases routing complexity, power consumption, and area utilization which is a part of the limitations discussed in Chapters 1 and 2. Hence, a drive towards non–coherent control is necessary, as will be shown in phase 3 of the experimental work in this chapter.

Prior to hardware implementation, the operation of the control system was verified through simulations using Vector Waveform Files (VWFs). This approach enabled both functional simulations, used to verify the logical operation of the digital frame router, and timing simulations, which account for propagation delays within the FPGA. Both simulations confirmed correct operation of the digital frame routing. The DACs used in the prototype were implemented using R–2R resistor ladder networks followed by unity–gain buffer amplifiers, providing the required digital–to–analog conversion for controlling the varactors and varistors.

The test circuit was implemented on a generic FR–4 PCB, as shown in **Figure 5.4**. The functional blocks corresponding to each control cell are highlighted in red to clearly illustrate the architecture. The resistors used in the R–2R ladder DACs were implemented using 0805 surface–mount resistors with values of 10 kΩ and 20 kΩ. In addition, a 10 kΩ resistor was placed at the output of the buffer amplifier to decouple the Alternating Current (AC) excitation signal from the Inductor–Capacitor–Resistor (LCR) meter from the DC bias applied to the varactors. A resistive voltage divider was also included to scale the control voltage to a suitable range for the varistors.

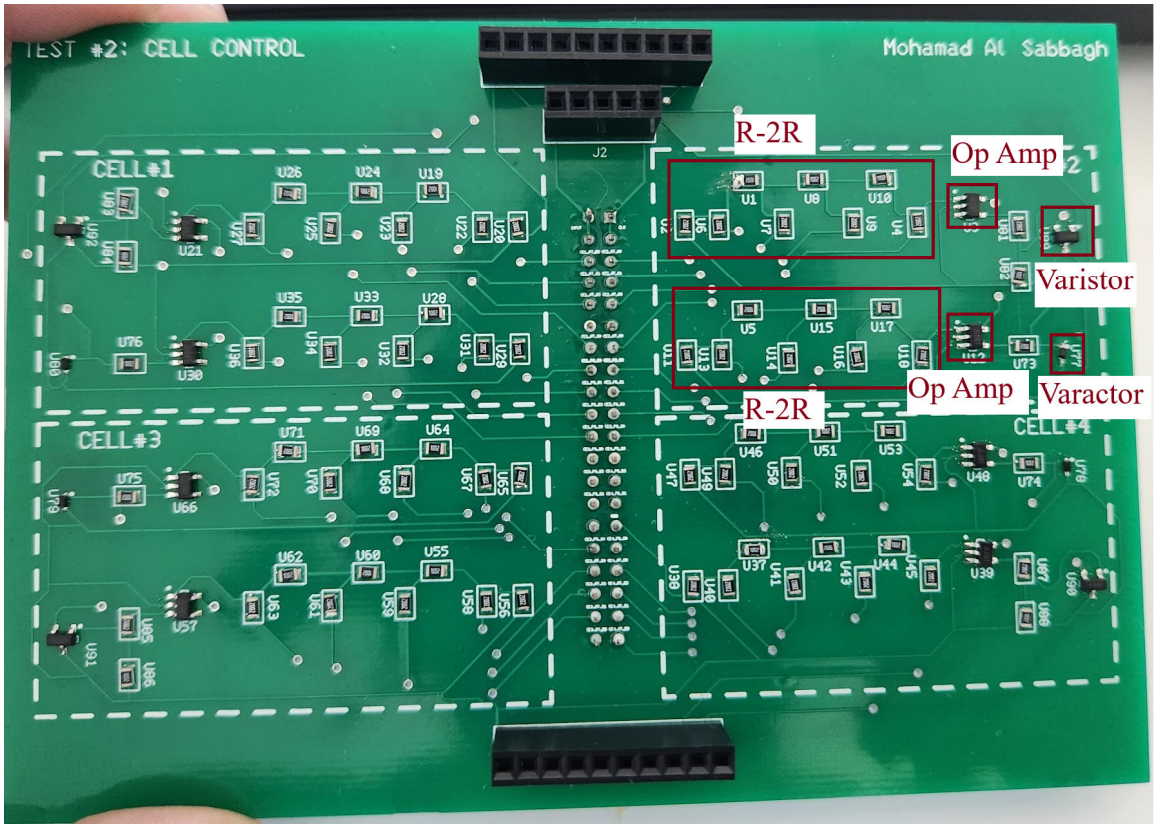


Figure 5.4 PCB for prototyping an emulated 2x2 subarray.

For the varactor implementation, the SMV1249–079LF component was selected, which provides a capacitance tuning range from approximately 37 pF down to 3 pF for control voltages between 0 V and 3.3 V. To emulate the attenuator element, a high–R_{on} transistor, namely LND150K1–G, was used as a voltage–controlled resistor. This device provides a resistance range of approximately 6 kΩ down to 2 kΩ for gate voltages between 0 V and 1 V.

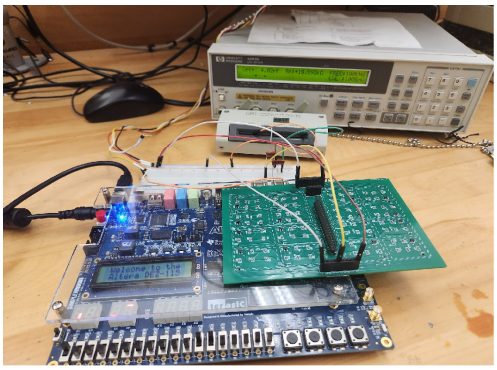
The buffer amplifier used in the DAC output stage is the AS321KTR–G1, a single–supply operational amplifier with a gain–bandwidth product of 700 kHz and an input common–mode range (ICMR) extending from 0 V to $V_{DD} - 1.5$ V.

To interface the PCB with the FPGA, a 2×20 extended expansion header was included. Additionally, two 1×10 headers were placed at the top and bottom edges of the PCB to provide V_{DD} and ground (GND) connections, as well as convenient access to measurement

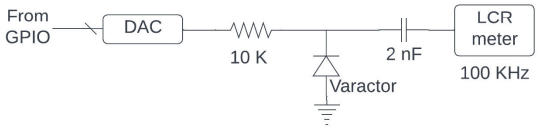
test points. Finally, a 5×1 header was added to allow monitoring of the input PWM and clock signals during testing.

The key parameters required for the experimental validation of the control system are now discussed. These measurements include the capacitance of the varactors, the resistance of the varistors, and the transient voltages observed at the FPGA GPIO pins and DAC outputs.

Figure 5.5 shows the measurement setup used to characterize the capacitance of the varactors. An HP 4263B LCR meter was used to perform the measurements, providing an AC excitation signal at 100 kHz. A 2 nF coupling capacitor was inserted between the varactor and the LCR meter to decouple the AC measurement signal from the DC bias voltage applied by the DAC. In addition, as described previously, a 10 kΩ resistor was included to provide isolation between the LCR meter and the DAC circuitry. The 2x2 emulated subarray PCB was mounted on the DE2–115 Development Kit, on which the digital PWM decoder and frame router were synthesized on the FPGA.



(a)



(b)

Figure 5.5 Varactor capacitance measurements using LCR meter showing: (a) test setup, and (b) testing schematic.

To measure the resistance of the varistors, a DM3058E digital multimeter was used to measure the current flowing through the device, as illustrated in **Figure 5.6**. The resistance value was then calculated using Ohm's law.

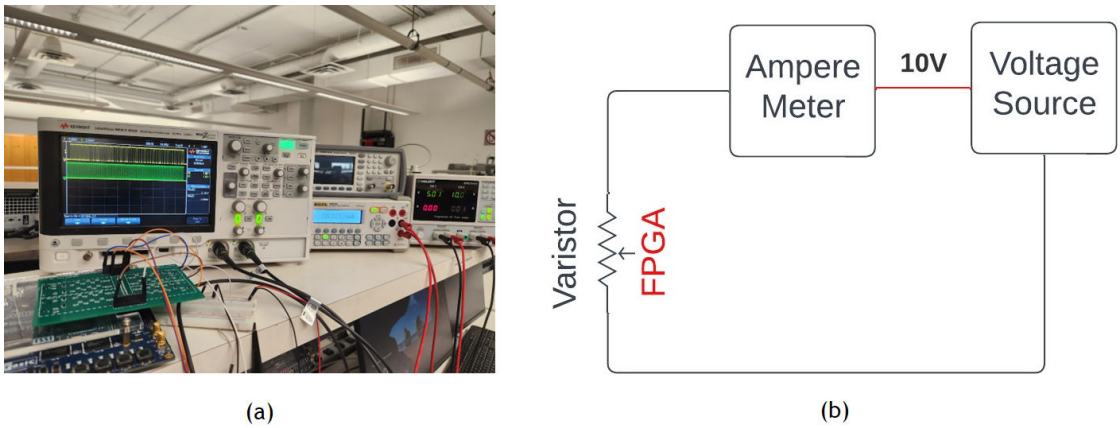


Figure 5.6 Varistor resistance measurements using Ampere meter showing: (a) test setup, and (b) testing schematic.

Finally, transient voltage measurements were performed to observe the input PWM signal (CLK), the PLL_CLK signal, the FPGA GPIO outputs, and the DAC output voltages. These measurements were carried out using an MSO–X 2012A oscilloscope, together with a laboratory power supply and Keysight DSOX2M08 eight–channel digital probe cables, as shown in **Figure 5.7**. The measurement results obtained from these experiments will now be presented.

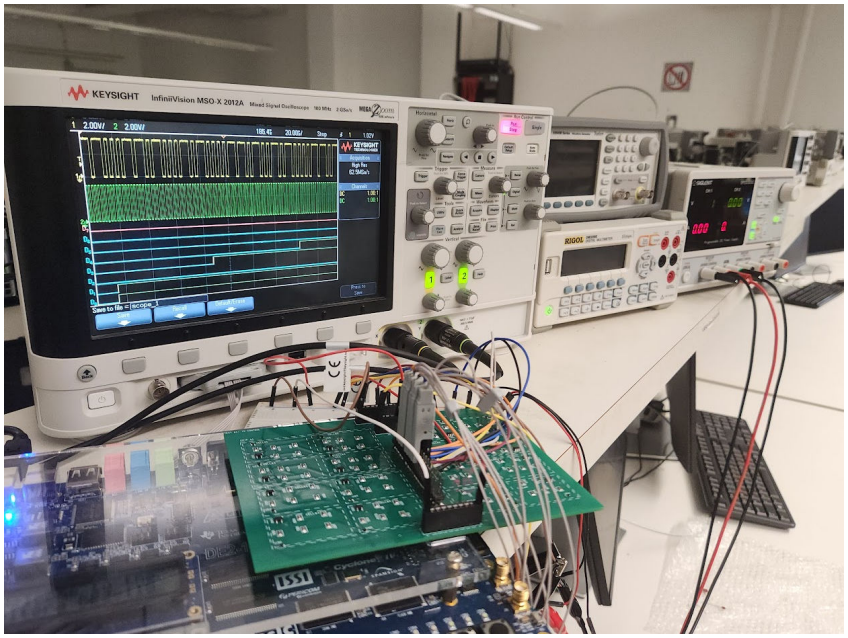


Figure 5.7 Test setup for measuring the transient waveforms of the control PCB.

Figure 5.8 presents a comparison between the measured values and the datasheet specifications of the tested varactors and varistors at various control voltages. **Figure 5.8**(a) shows the average measured capacitance of all varactors used in the 2×2 emulated subarray prototype. The results demonstrate very good agreement between the averaged measurements and the values reported in the datasheet.

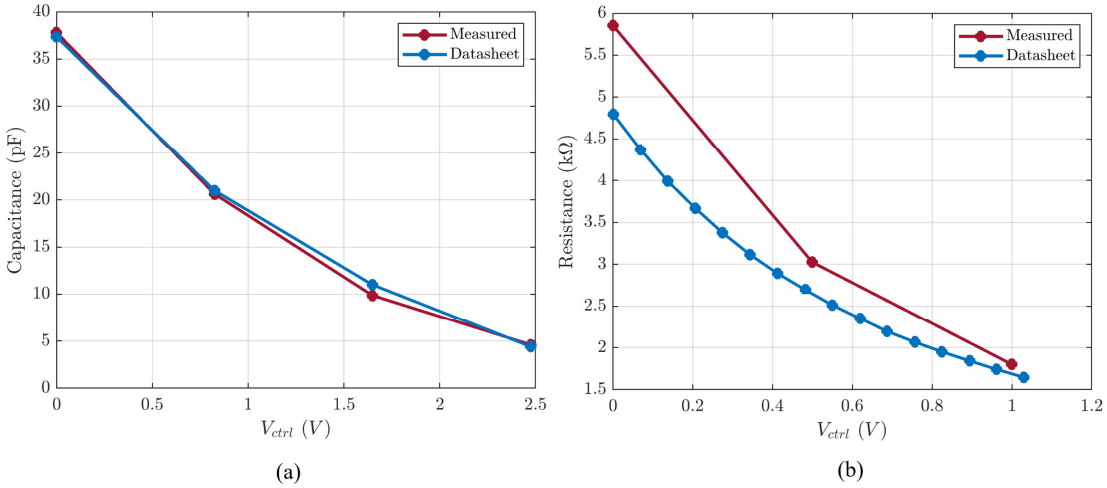


Figure 5.8 Comparison between measurement and datasheet values in a 2x2 emulated subarray of: (a) varactors, and (b) varistors.

Figure 5.8(b) compares the averaged measured resistances of the varistors with the corresponding datasheet values. A certain discrepancy between the measured and datasheet results can be observed. This difference can be attributed to the variation in testing conditions, as the datasheet values are obtained using pulsed measurements, which minimize the impact of non–ideal effects such as device self–heating. Despite this discrepancy, the overall trend of the measured resistance closely follows the trend indicated in the datasheet.

Waveform measurements of the GPIO pins for the 2x2 emulated subarray are presented in **Figure 5.9**(a). The measured signals include the CLK signal (shown in blue) and the divided FPGA clock PLL_CLK (shown in magenta). The bit rate was selected such that the transmitted square pulses remain well defined and free of significant distortion; experimentally, this condition was satisfied at a rate of 500 kbps. The red waveforms

correspond to the digital control signals generated at the FPGA GPIO pins, which are produced according to the PWM input coding scheme described in **Figure 4.7**.

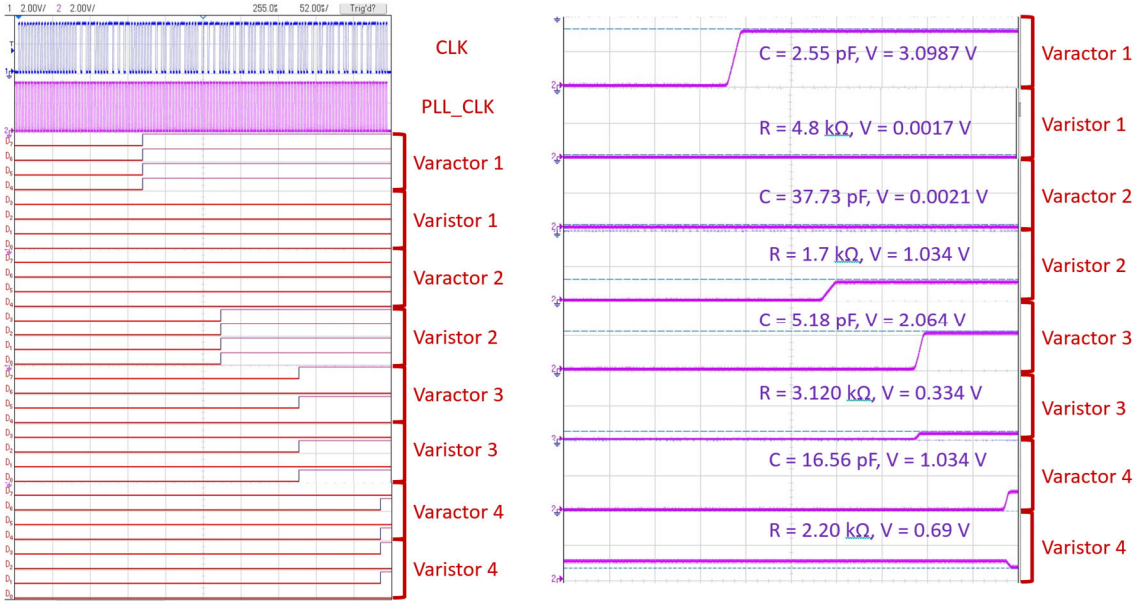


Figure 5.9 Waveform signals for the 2x2 emulated subarray prototype showing: (a) FPGA GPIO pins, and (b) varactors and varistors control voltages and their annotated controlled values.

As observed in **Figure 5.9**(a), the GPIO outputs update after each control sample, and the corresponding control pins associated with the selected varactor or varistor are modified accordingly. **Figure 5.9**(b) presents the analog voltages generated by the DAC outputs for the 2×2 prototype. These voltages follow the digital control signals and are applied to the corresponding devices. As shown in the figure, the DAC outputs can be adjusted to produce the required bias voltages, thereby modifying the capacitance of the varactors or the resistance of the varistors, as annotated in **Figure 5.9**(b).

Overall, the measured waveforms confirm the correct operation of the digital frame router and DAC interface for the 2×2 subarray prototype. The results demonstrate that the control system successfully decodes the PWM signal, updates the appropriate GPIO outputs, and generates the corresponding analog control voltages. These observations validate the expected functionality of a single control block and confirm the potential feasibility of extending the architecture to larger array configurations. Building on this

validation, the next experiment extends the system to a larger configuration in order to verify the ID–based frame routing mechanism across multiple control blocks in a 4×4 emulated array.

5.2 ID-Based Control Validation in a 4×4 Array

Following the successful validation of the single control block in the 2×2 prototype, the next experimental phase focuses on evaluating the scalability of the proposed control architecture. In particular, this experiment aims to verify the ID–based frame routing mechanism, which is responsible for directing control data to the appropriate control block in a larger array configuration.

To accomplish this, a 4×4 array prototype was implemented, where each group of 2×2 elements represents a subarray controlled by a single digital control block. Each subarray is assigned a unique ID, allowing the frame router to selectively update the control parameters of the targeted subarray while leaving the remaining elements unchanged. This setup emulates the operation of a larger phased–array system where multiple subarrays must be independently addressed through a shared communication link.

In this experiment, the FPGA again generates the PWM control frames and performs the frame routing according to the assigned subarray IDs. The overall architecture of the 4×4 prototype is illustrated in **Figure 5.10**, where the FPGA GPIO interface distributes the control signals to four independent subarray blocks, each corresponding to a 2×2 subarray. The analog loads are implemented using sixteen varactors, each driven by a 2–bit R–2R ladder DAC, allowing the capacitance of each element to be adjusted through the digital control signals. As shown in the figure, each DAC output is buffered before being applied to the corresponding varactor. Due to the limited number of available FPGA GPIO pins, the attenuator emulation using varistors was omitted in this phase. Nevertheless, the varactors provide a sufficient platform to validate the correct routing of control signals and the independent tuning of each array element.

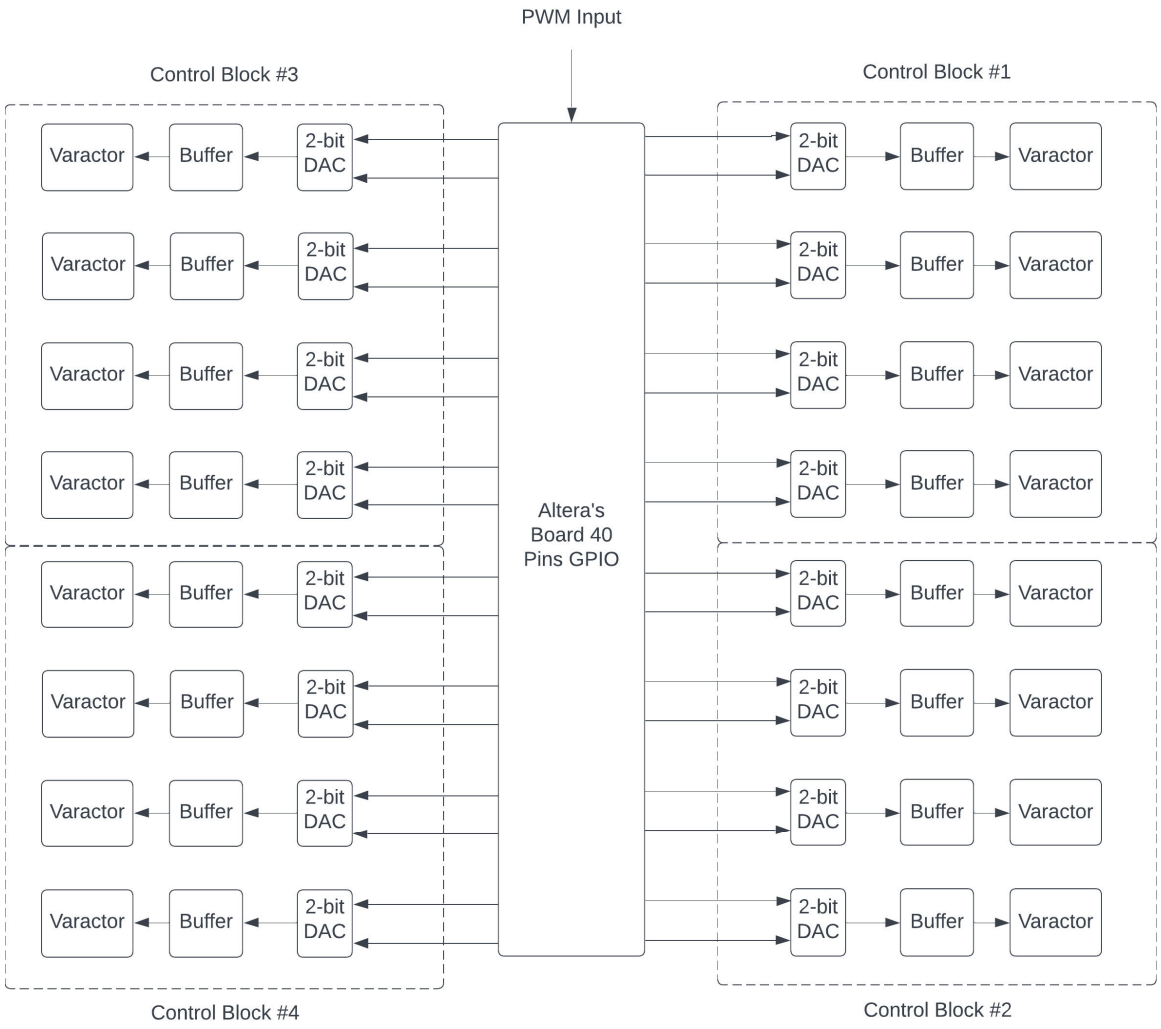


Figure 5.10 Block diagram of the 4x4 array prototype.

The fabricated 4×4 array prototype PCB used for the ID–based control experiment is shown in **Figure 5.11**. The board contains sixteen identical control cells arranged in four 2×2 subarray blocks, each controlled by a control block described in the system architecture. Every cell consists of a 2–bit R–2R ladder DAC, followed by a buffering op amp and a varactor, which emulates the tunable element of a phase shifter. The components used in this prototype are identical to those presented in the previous section, including the same R–2R resistor values, varactor devices, and operational amplifiers, ensuring consistent behavior between the 2×2 and 4×4 experiments. As illustrated in the figure, the PCB also includes headers used to interface the board with the FPGA GPIO pins, which provide the digital control signals required to control the DACs of each cell.

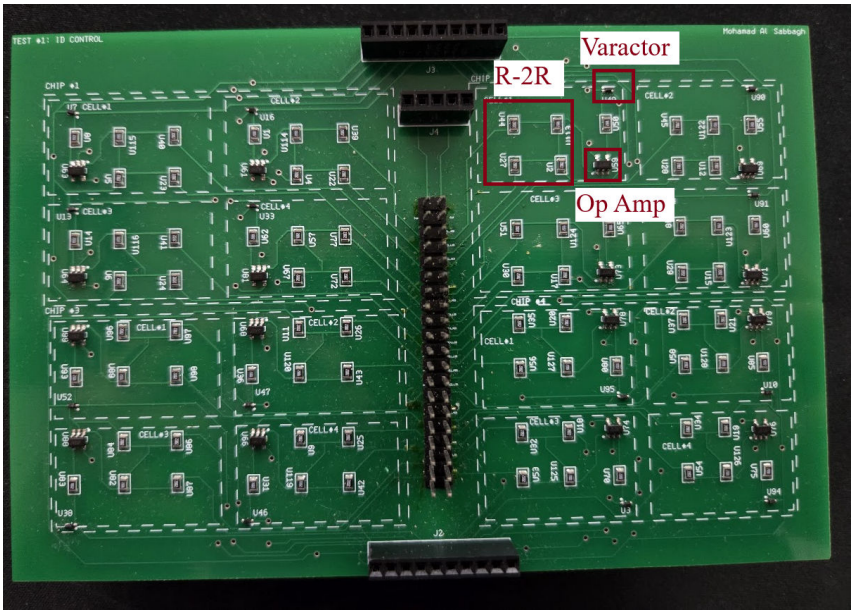


Figure 5.11 PCB for prototyping an emulated 4x4 array.

The measured capacitance characteristics of the varactors used in the 4×4 array prototype are presented in **Figure 5.12**, together with the corresponding datasheet values for comparison. The plot shows the average measured capacitance as a function of the control voltage applied by the DAC outputs. The measured results exhibit a similar trend to the datasheet curve across the entire control voltage range.

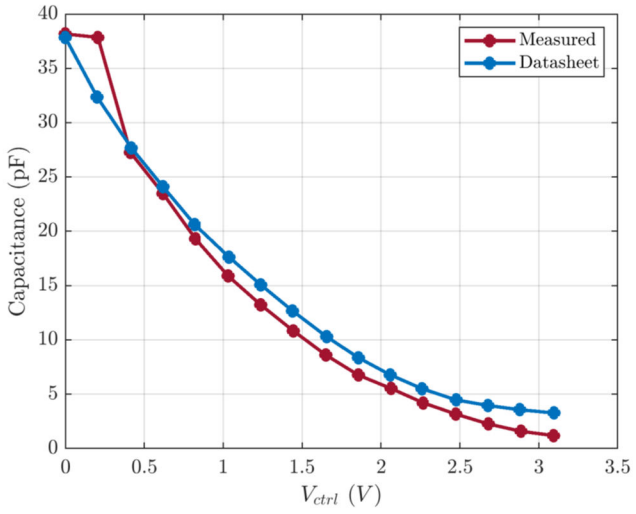


Figure 5.12 Comparison between measured and datasheet varactor values in a 4x4 emulated array.

Waveform measurements of the GPIO pins for the 4×4 prototype are presented in **Figure 5.13**. The measurements illustrate the operation of the ID–based addressing mechanism, where the GPIO outputs update according to the received control frames. As shown in **Figure 5.13**, the digital control signals change after each control sample based on the decoded control block ID and cell ID, ensuring that only the targeted control block and corresponding element are updated.

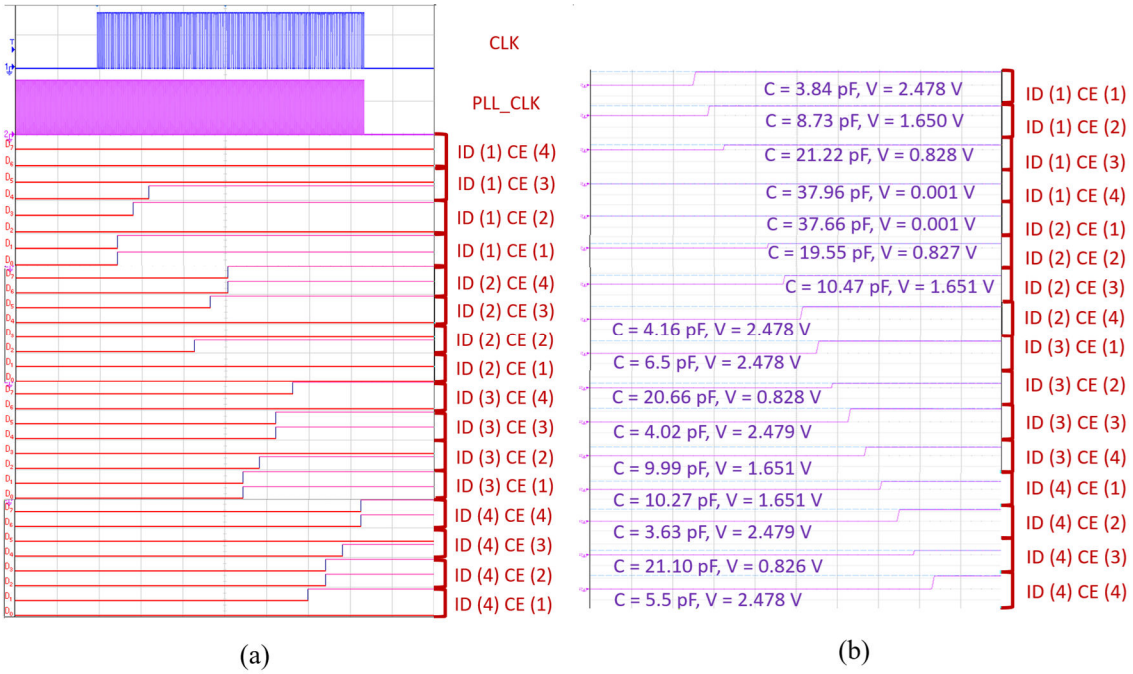


Figure 5.13 Waveform signals for the 4x4 emulated array prototype showing: (a) FPGA GPIO pins, and (b) varactors control voltages and their annotated controlled values.

The experimental results provide a proof–of–concept demonstration of data directivity, where control information can be selectively routed to a particular control block while other control blocks remain unaffected. The annotated control voltages and corresponding varactor measurements further confirm the correct operation of the addressing and control scheme.

Overall, these measurements validate the correct operation of the ID–based frame routing architecture in the 4×4 prototype. The results demonstrate that the control system can selectively address individual control blocks and cells, generating the required analog

bias voltages, thereby confirming the scalability of the proposed control approach for larger phased–array configurations. Having verified both the functionality of a single control block and the scalability of the addressing scheme, the next phase of the experimental work combines the ASK–PWM communication interface with the synthesized digital frame router with a phased–array antenna prototype for beamforming validation.

5.3 ASK–PWM PCB Control and Beam–steering Demonstration

The final phase of the experimental work combines the complete ASK–PWM wireless control system with a beamforming antenna array in order to validate the proposed architecture under realistic operating conditions. The objective is to demonstrate that digital beam–steering commands can be transmitted wirelessly, recovered locally, and used to dynamically control the phase of multiple antenna elements, without the need for clock distribution trees or conventional SPI–based control protocols. This significantly reduces routing complexity, the required number of PCB layers, and the number of feeding pins on the phased–array module. The overall test arrangement is illustrated in **Figure 5.14**.

The control communication path begins with an ASK–PWM transmitter feeding a transmitting panel antenna. The ASK–PWM modulated signal is radiated through the wireless channel and captured by the receiving panel antenna. The received RF signal is first conditioned by a matching network and then passed to an ASK demodulator, which extracts both the envelope and its average voltage. These signals are processed by a comparator to generate the recovered clock CLK, which is then used by the PWM decoder to reconstruct the PRE_DATA signal. The recovered CLK and PRE_DATA are subsequently applied to the FPGA GPIO for frame routing and distribution to the DACs.

Unlike the two earlier validation phases, where a digitally synthesized PWM decoder ran inside the FPGA for convenience, the present experiment performs PWM decoding in the ASK–PWM receiver hardware, so the FPGA receives already recovered CLK and PRE_DATA and is therefore dedicated to frame routing and addressing. This approach is in accordance with the PLL–less objective of this thesis, as the clock is directly recovered from the received ASK–PWM signal without requiring any external clock generation or

complex synchronization circuitry. In this setup, we intentionally use one receive antenna and a single FPGA as a practical simplification to emulate two control blocks. The single FPGA models the behavior of two separate control blocks by handling distinct address ranges, allowing us to validate control block addressing and routing without requiring duplicate receiver hardware.

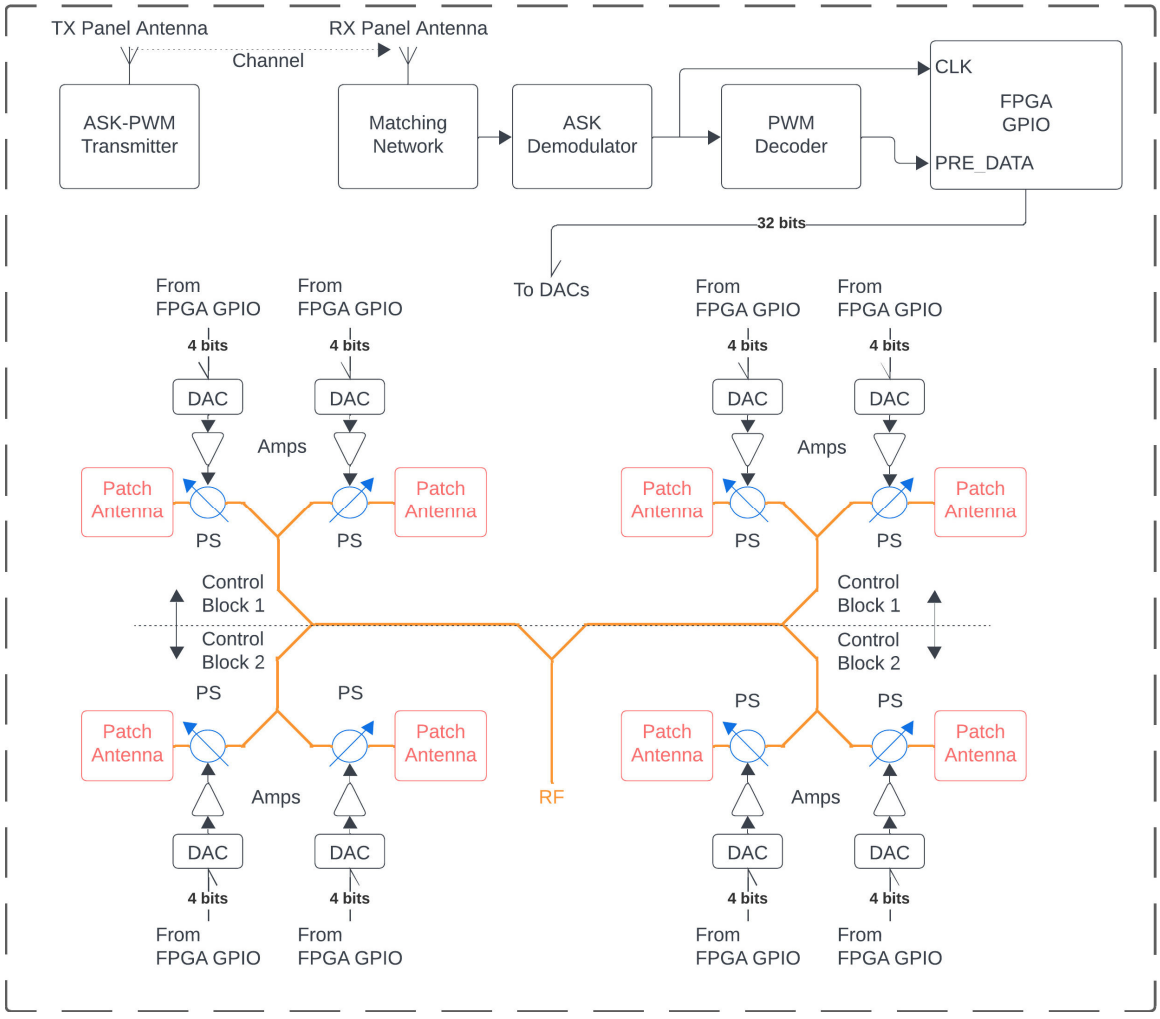


Figure 5.14 Block diagram of the test setup for validating wirelessly controlled ASK–PWM phased array system.

Once routed, the decoded control frames are converted to analog bias voltages by multiple DAC channels. Each DAC output is amplified and applied to a reflective PS associated with a particular antenna element. The RF beamforming path (orange) routes

the carrier through a feed network into branches containing the reflective PS units; by changing the bias voltages, the relative phase at each patch element is altered, producing steerable radiation patterns from the 2×4 planar patch array.

To support the addressing scheme used in the experiment, the array is partitioned into two subarrays: the top half (1x4) is controlled by the emulated control block 1 and the bottom half is controlled by control block 2 (annotated in the diagram). The FPGA's frame router therefore targets the top or bottom subarray depending on the received control block ID. This arrangement provides a clear proof–of–concept of data directivity and ID–based control in a near–real scenario.

The selected bit rate, ASK–PWM carrier frequency, and beamforming frequency, are determined based on the requirements of a low–power control system intended for WPT applications. Accordingly, a relatively low bit rate of 15 kbps is chosen, as control signaling in such systems typically requires only low throughput while benefiting from reduced circuit complexity and improved energy efficiency. The ASK–PWM carrier frequency is selected within the Industrial, Scientific, and Medical (ISM) band, with a frequency of 935 MHz used in this design, consistent with the panel antenna characterization presented in the next subsection. The beamforming frequency is chosen to be between the third and fourth harmonic of the ASK–PWM carrier frequency to mitigate harmonic EM interference. Hence, a beamforming frequency of 3.5 GHz was chosen.

The following subsections examine each element in detail: communicating antenna characterization, ASK–PWM circuit implementation, phase shifter characterization, the 2×4 array performance, and the final beamforming measurements.

5.3.1 Communicating antenna characterization

Since the primary focus of this work is to design and experimentally validate the wireless control blocks, commercially available antennas were adopted to simplify system integration and evaluation. The used antennas are the 8 dBi HG908PCR right–hand circularly polarized (RHCP) panel antennas. These antennas were selected to provide reliable wireless transmission of the ASK–PWM control signal between the transmitter and

receiver modules. Prior to integration into the system, the antennas were characterized to verify their impedance matching and operating frequency.

The measurement setup used for the characterization is shown in **Figure 5.15**. The antenna reflection coefficient was measured using an Agilent E8363B Performance Network Analyzer (PNA), which is a high–performance network analyzer commonly used for RF device characterization, and can run scattering parameters (S–parameters) measurements up to 40 GHz. Before performing the measurements, the PNA was calibrated using the Short–Open–Thru (SOT) calibration approach in order to remove systematic measurement errors associated with cables and connectors. The calibration process resulted in a measurement dynamic range of approximately -75 dB in $|S_{11}|$, ensuring high accuracy in the subsequent antenna characterization.

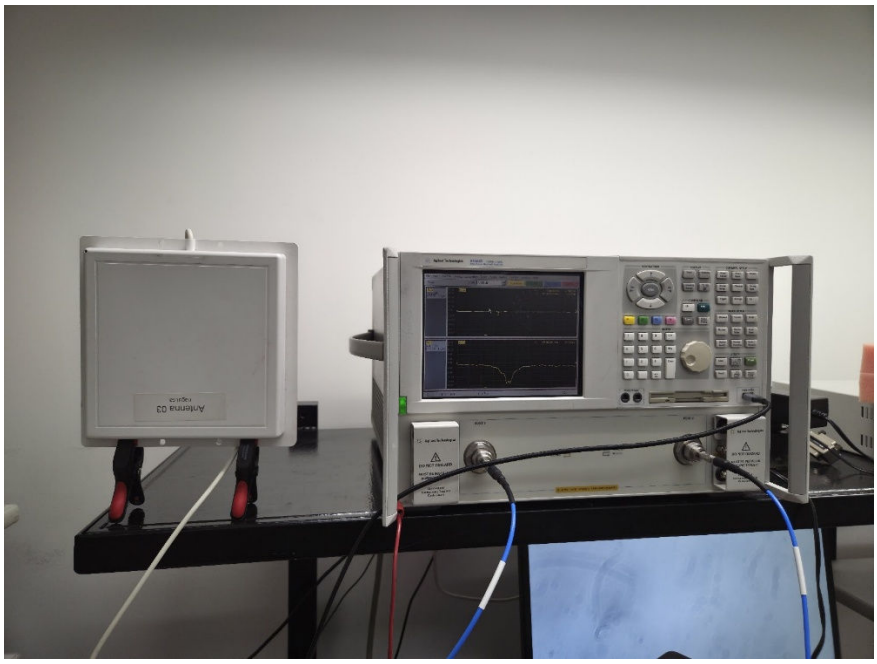


Figure 5.15 Panel antenna characterization setup.

Following calibration, the antenna under test was connected directly to the PNA port through a coaxial cable, and the $|S_{11}|$ parameter was measured across the frequency band of interest. The measured reflection coefficients of the transmitting and receiving panel antennas are presented in **Figure 5.16**. The results show that both antennas exhibit very

similar impedance characteristics across the measured frequency range, with a pronounced resonance occurring near 935 MHz. This frequency was therefore selected as the carrier frequency for the wireless ASK–PWM communication link, as it provides a good compromise between the matching conditions of both antennas.

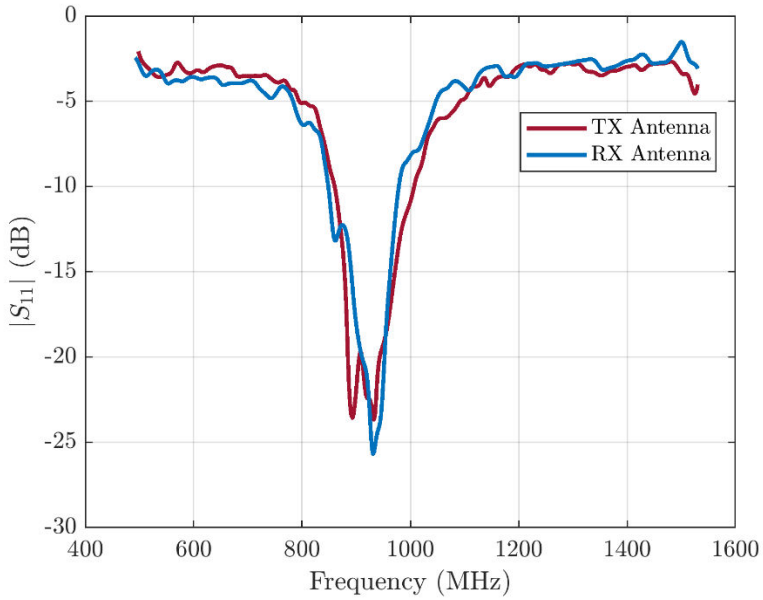


Figure 5.16 Measured $|S_{11}|$ for TX (red) and RX (blue) panel antennas.

At the resonant frequency, both antennas demonstrate strong impedance matching, with the transmit antenna exhibiting an impedance of approximately 44.45 Ω and the receive antenna exhibiting an impedance of approximately 54.81 Ω. These values are reasonably close to the standard 50 Ω system impedance, indicating good matching performance and minimal reflection losses at the operating frequency.

The measured –10 dB impedance bandwidth spans approximately 848 MHz to 980 MHz, providing a bandwidth of roughly 132 MHz. This bandwidth ensures stable operation of the wireless link under small frequency deviations or environmental variations. The similarity between the transmit and receive antenna responses further confirms that the two commercially available panel antennas exhibit consistent performance, making them suitable for reliable wireless transmission and reception of the ASK–PWM control signal.

5.3.2 ASK-PWM circuit design

In this subsection, the circuit design of the ASK–PWM demodulator and decoder is presented. This design stage is necessary to validate correct circuit–level operation, including voltage levels, frequency response, and timing behavior, prior to hardware implementation.

The ASK demodulator, shown in **Figure 5.17**, consists of three main blocks: an envelope detector, a dynamic reference generator, and a comparator. The envelope detector is implemented as a voltage doubler composed of components C_1, D_1, D_2, C_2, R_1, and R_2. The dynamic reference generator is implemented using the components R_{div}, R_{cm}, and C_{cm}. Finally, the comparator stage consists of a differential amplifier (Amp) followed by a comparator (Comp), which generates the RZ output signal V_{dig}. A matching inductor L_{in} is used for power matching purposes.

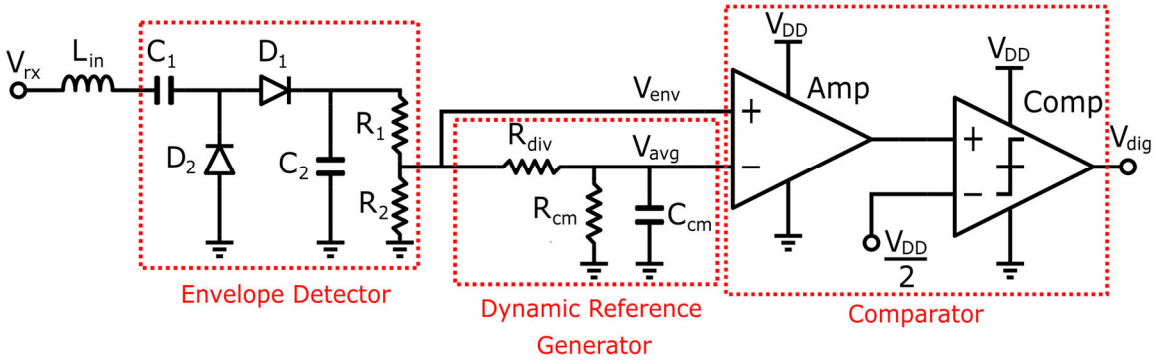


Figure 5.17 ASK demodulator circuit schematic.

For proper operation of the envelope detector, the carrier frequency must be sufficiently attenuated while preserving the ASK modulation. This requirement leads to the design of two critical time constants:

$$\tau_1 \approx C_1 (R_1 + R_2), \tag{5.1}$$

$$\tau_2 \approx C_2 (R_1 + R_2). \tag{5.2}$$

These expressions assume that R_{cm} is in the MΩ range. Here, τ_1 represents the input high–pass time constant of the detector, while τ_2 corresponds to the output low–pass time constant. To ensure correct demodulation, τ_1 must be at least 10× to 20× larger than the ASK modulation time constant, allowing the 15 kHz modulation to pass without significant attenuation. In contrast, τ_2 must be sufficiently large to suppress the carrier frequency, while remaining small enough to accurately track the envelope of the ASK signal (e.g., on the order of 10× or 20× smaller than the ASK modulation time constant).

Based on these considerations, and for an ASK modulation frequency of 15 kHz (corresponding to a time constant of approximately 10 μs), the component values $C_1 = 1\,\text{nF}$, $C_2 = 6\,\text{pF}$, and $(R_1 + R_2) = 150\,\text{k}\Omega$ were selected. This results in $\tau_1 = 150\,\mu\text{s}$, corresponding to a high–pass cutoff frequency of approximately 1.06 kHz, and $\tau_2 = 900$ ns, corresponding to a low–pass cutoff frequency of approximately 176.8 kHz. These values provide an appropriate passband for the 15 kHz ASK signal while effectively rejecting the 935 MHz carrier. The resistors R_1 and R_2 are chosen to be equal (75 kΩ each) to center the output voltage of the voltage doubler within the ICMR of the Amp.

A third time constant, τ_3, associated with the dynamic reference generation used to bias Amp, is given by

$$\tau_3 \approx C_{cm}\,(R_{div} + R_2). \tag{5.3}$$

This time constant is designed to be approximately two orders of magnitude larger than τ_2 in order to effectively filter the ASK modulation and produce a smooth, quasi–static common–mode reference voltage representing the average of the envelope voltage. Accordingly, $C_{cm} = 600$ pF and $R_{div} = 100$ kΩ are selected, resulting in $\tau_3 \approx 105\,\mu$s and a corresponding low–pass cutoff frequency of approximately 1.51 kHz. The voltage divider formed by R_{div} and R_{cm} ensures that, under no–modulation conditions, the envelope voltage V_{env} and the average voltage V_{avg} differ by approximately 1–2%, thereby preventing spurious switching at the comparator output. Based on this requirement, R_{cm} is selected to be 8 MΩ.

The proposed circuit was simulated using Keysight Advanced Design System (ADS), and the corresponding results are shown in **Figure 5.18**. The envelope detector employs SMS3922–079LF Schottky diodes (Skyworks, USA), for which an SPICE model is available in the datasheet, enabling accurate nonlinear device modeling in simulation. **Figure 5.18**(a) shows the received signal generated by the ASK generator (PWM is omitted here for simulation simplifications). The corresponding envelope V_{env} and its averaged value V_{avg} are illustrated in **Figure 5.18**(b). **Figure 5.18**(c) presents the output of the differential amplifier followed by a comparator to produce the digital signal V_{dig}, which acts as the CLK signal after buffering. Finally, **Figure 5.18**(d) illustrates the circuit behavior under no modulation, demonstrating that R_{div} and R_{cm} produce two distinct voltage levels, enabling stable and spurious–free operation.

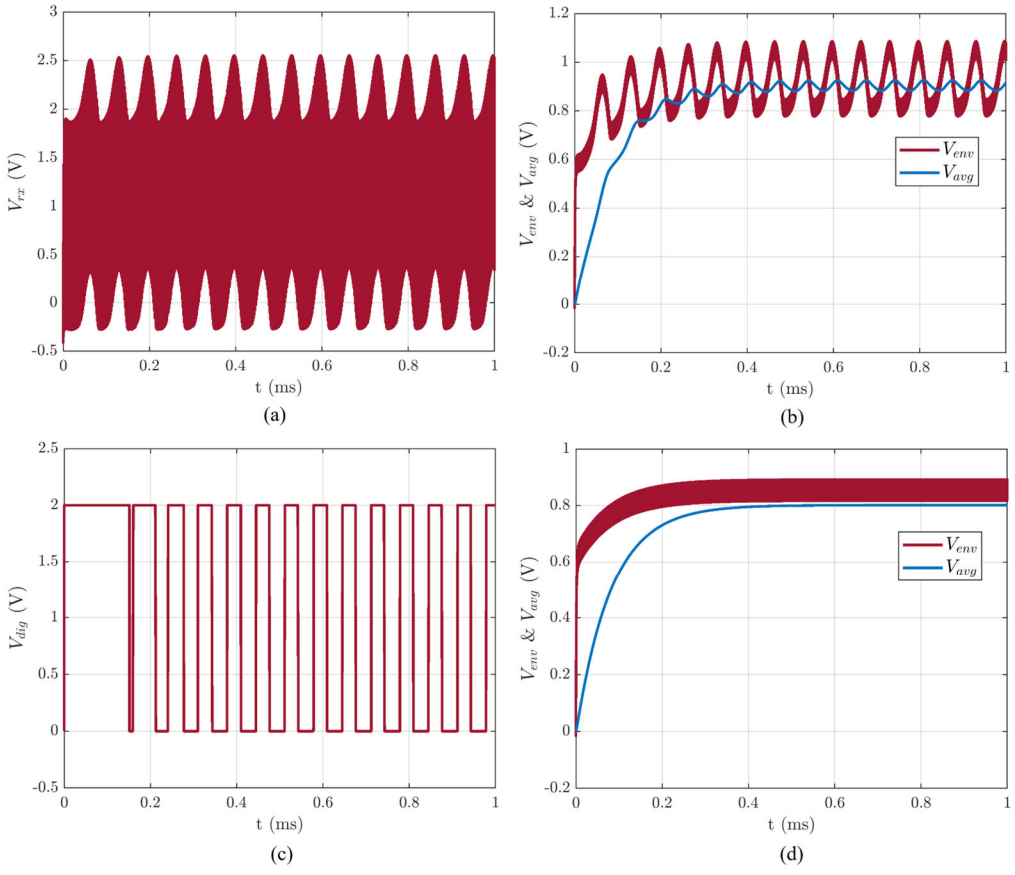


Figure 5.18 ASK demodulator simulations showing voltage waveforms of: (a) V_{rx}, (b) V_{env} (red) and V_{avg} (blue), (c) V_{dig}, and (d) Voltage difference between V_{env} & V_{avg} during idle mode.

As discussed in Subsubsection 3.3.1.2 and Subsection 4.2.2, PWM decoding requires a skewing operation to discriminate between different pulse widths. Traditionally, this skewing is implemented in a CMOS inverter by increasing the channel length of the pull–up transistor, which increases the Resistor–Capacitor (RC) charging time constant, while maximizing the aspect ratio of the pull–down transistor to maintain a fast discharge path. Although this approach is straightforward in IC implementations, where transistor dimensions can be freely adjusted, it becomes impractical in a discrete PCB implementation due to limited flexibility in modifying transistor geometry.

To address this limitation, the skewing inverter on PCB employs an alternative approach. A skewing resistor is inserted between the drain of the pull–up transistor and the inverter output, increasing the resistance of the charging path and thereby enlarging the charging time constant without affecting the discharge path. In addition, a capacitor is connected at the output of the skewing inverter to further support the desired time–constant increase.

The complete PWM decoder circuit, illustrated in **Figure 5.19**, consists of a skewed buffer followed by a comparator. The skewed buffer interfaces directly with the output of the ASK demodulator and is composed of a CMOS inverter (M_1 and M_2) followed by the skewed inverter implemented using transistors M_3 and M_4 together with R_{skew} and C_{skew}. The resulting skewed signal is then applied to a comparator, whose output is buffered by transistors M_5, M_6, M_7, and M_8 to generate the PRE_DATA signal.

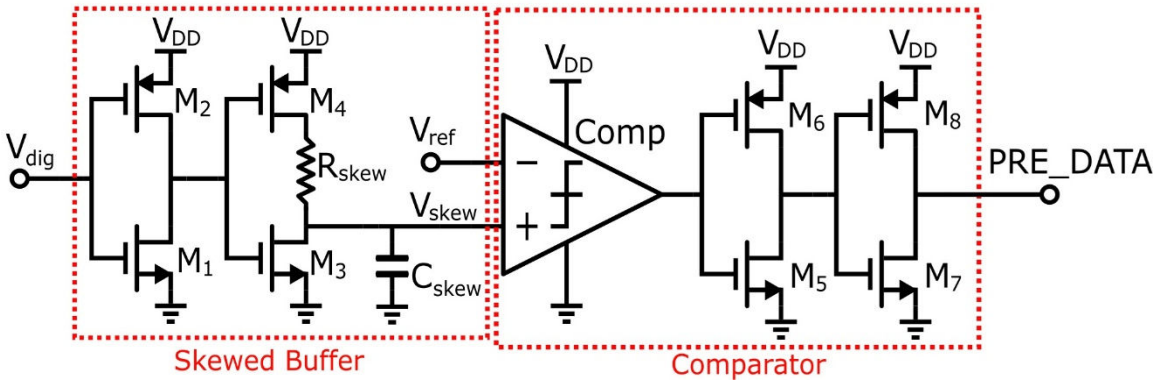


Figure 5.19 PWM decoder circuit schematic.

The resistor R_{skew} intentionally slows the low–to–high transition while preserving a sharp high–to–low transition, producing asymmetric switching behavior. This asymmetry enables discrimination between logic "0" and "1" based on pulse width. The charging dynamics of the skewed inverter output are characterized by the time constant τ_4, which can be approximated as

$$\tau_4 \approx R_{skew} C_{skew}. \tag{5.4}$$

The value of τ_4 must be carefully selected to ensure a clear voltage difference between the peaks generated by wide and narrow pulses, enabling reliable PWM data decoding.

For the PWM encoding scheme, the low–level pulse width for both logic "0" and logic "1" is fixed at 33 µs. The high–level pulse width, however, differs between the two symbols. For bit "0", the high–level duration remains 33 µs (corresponding to a data rate of 15 kbps), whereas for bit "1", the high–level duration is extended to 99 µs. The time constant τ_4 is therefore chosen such that the output voltage of the skewed inverter exceeds a reference voltage V_{ref} only for the wider 99 µs pulse, ensuring reliable detection of bit "1", while remaining below V_{ref} for the narrower 33 µs pulse corresponding to bit "0".

Assuming a supply voltage $V_{DD} = 2$ V, which is suitable for FPGA interfacing, and selecting an initial value of $\tau_4 = 50\,\mu$s, a first–order RC approximation predicts peak output voltages of approximately 1.72 V for the wide pulse and 0.96 V for the narrow pulse. These values provide sufficient voltage margin for reliable bit discrimination using a reference voltage of $V_{ref} = 1.5$ V. However, circuit–level simulations revealed undershoot effects primarily caused by transistor parasitic capacitances. To mitigate this effect and improve robustness, the time constant τ_4 was reduced to $25\,\mu$s through Computer–Aided Design (CAD) assisted optimization.

Accordingly, the final design selects $R_{skew} = 250\,k\Omega$ and $C_{skew} = 100$ pF, yielding the desired time constant and ensuring reliable PWM decoding. The simulation results of the PWM decoder are presented in **Figure 5.20**, illustrating the pulse–width–based data recovery process. **Figure 5.20**(a) shows the digital output of the ASK demodulator (V_{dig}), **Figure 5.20**(b) shows the output of the skewed buffer (red) and the chosen reference

voltage (blue) for data discrimination, and **Figure 5.20**(c) shows the recovered PRE_DATA signal. These results demonstrate correct PWM decoding, where logic "1" is generated for wide pulses and logic "0" for narrow pulses.

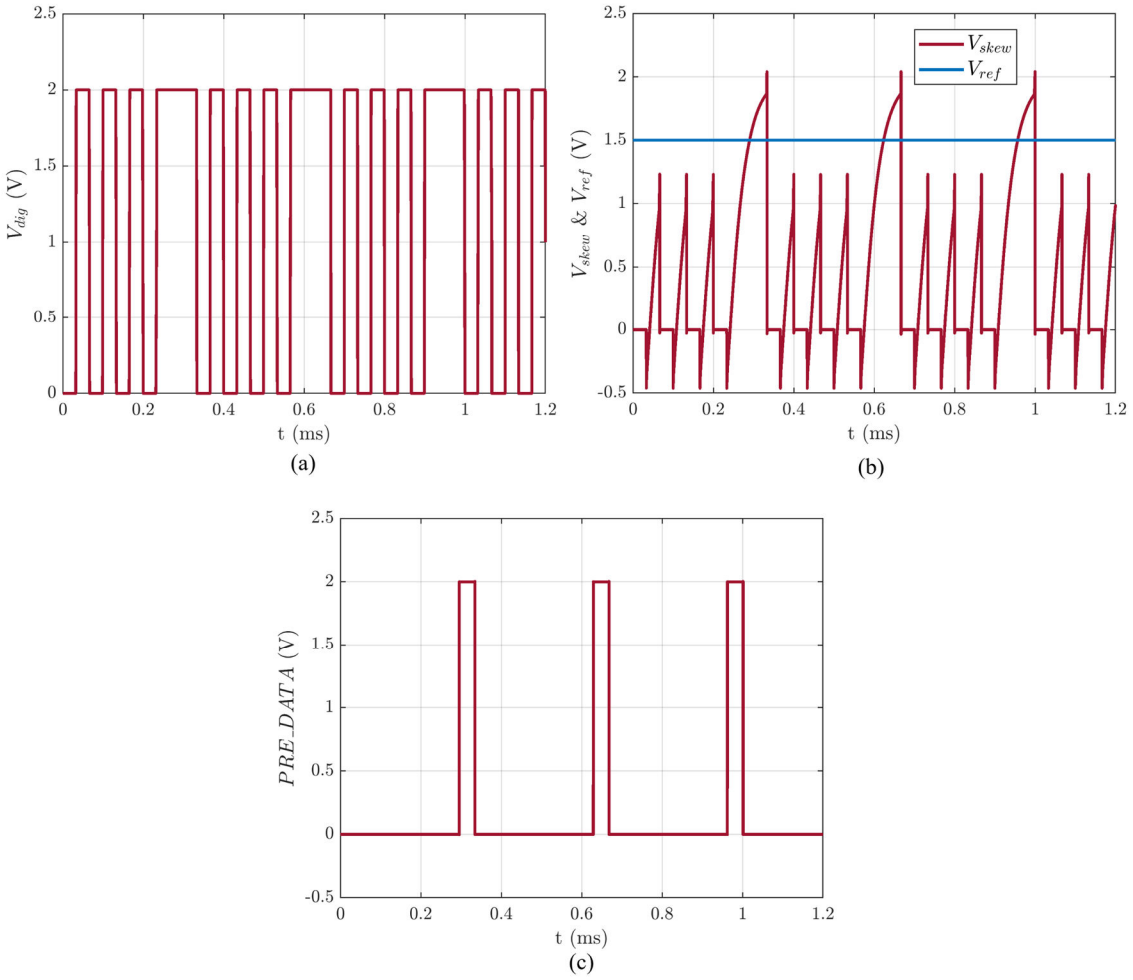


Figure 5.20 PWM decoder simulations showing voltage waveforms of: (a) V_{dig}, (b) V_{skew} (red) and V_{ref} (blue), and (c) PRE_DATA.

5.3.3 Reflective phase shifter characterization

The implemented phase shifter is based on a reflection–type architecture (Subsubsection 3.1.4.3) using a 3–dB impedance–transforming branch–line coupler, as shown in **Figure 5.21**. The input signal applied at port 1 is equally divided by the quadrature coupler and directed toward ports 3 and 4, which are terminated by identical

reflective loads. Each load consists of a series–resonated network formed by an inductor L_s and a varactor C_v, together with a shunt resistor R_p. The reflected signals from these two loads are recombined by the coupler and delivered to the output port. Since the phase of the reflected signal depends on the reactance of the load, tuning the capacitance of the varactor through a control voltage changes the reflection phase, thereby producing a controllable phase shift between the input and output signals [91].

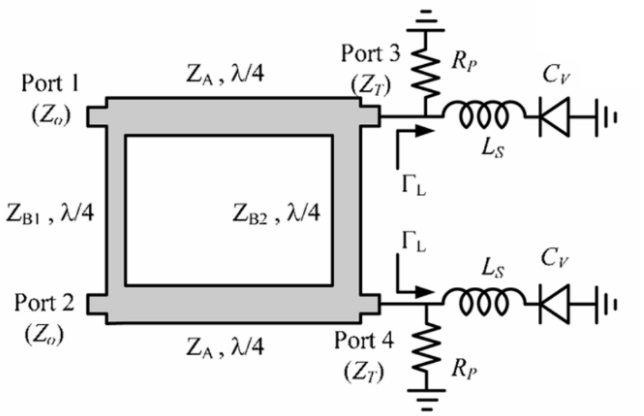


Figure 5.21 Schematic of reflective phase shifter [91].

The series inductor L_s is used to form a series–resonant circuit with the varactor, which effectively expands the achievable reactance variation for a given varactor capacitance range. This allows a significantly larger phase–shift range than what would be achievable with the varactor alone. However, practical varactors exhibit parasitic series resistance, which causes insertion loss to vary as the capacitance is tuned. To mitigate this effect, a shunt equalization resistor R_p is introduced in the reflective load. This resistor helps maintain a nearly constant reflection magnitude while the phase changes, thereby reducing insertion–loss variation across the tuning range and preventing amplitude imbalance in phased–array applications [91].

This topology was selected because it provides large phase tuning capability while remaining compatible with a low–cost PCB implementation on FR–4. The branch–line coupler simultaneously performs quadrature signal splitting and impedance transformation, which increases the achievable phase shift for a given varactor capacitance

range and eliminates the need for additional matching networks. As a result, the circuit remains compact and suitable for discrete implementation using Surface Mount Device (SMD) components. The reflective phase shifter therefore offers a practical solution for low–cost phased–array beamforming systems while maintaining good return loss and nearly constant insertion loss over the tuning range.

The fabricated prototype of the 3.5 GHz reflective phase shifter is shown in **Figure 5.22**. The circuit was implemented on a low–cost 0.6 mm FR–4 substrate to demonstrate the feasibility of realizing phased–array beamforming hardware using inexpensive PCB technology. The reflective loads of the phase shifter are implemented using SMV1430–040LF varactor diodes, whose capacitance is controlled through a bias voltage ranging from 0 to 10 V. According to the manufacturer datasheet, the varactor capacitance varies approximately from 1.24 pF at 0 V to 0.44 pF at 10 V, providing the tunable reactance required for phase control.

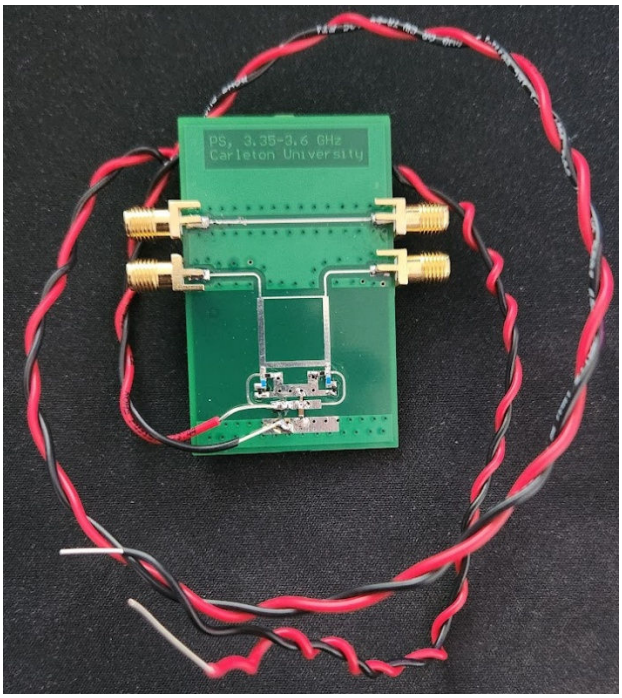


Figure 5.22 PCB prototype of the reflective phase shifter [Designed by Dr. Maryam Hasheminasab; experimentally validated by the author].

Each varactor is connected in series with a 1.8 nH inductor (0603HP-1N8XJRW) to form a series–resonant network that enhances the effective reactance tuning range. Microstrip transmission lines are used to implement the impedance–transforming branch–line coupler in the reflective phase shifter. The phase shifter is interfaced via SubMiniature version A (SMA) connectors to facilitate RF measurements.

In the original phase shifter design, the shunt equalization resistor R_p was included across the reflective load using a 777 Ω resistor (RT0603BRD07777RL). An issue arises when scaling the system to eight phase shifters in the beamforming network, for which the presence of these resistors resulted in unnecessary static current consumption, which is undesirable for a system powered through WPT. To improve power efficiency, the R_p resistors were removed in the final implementation. This modification eliminates continuous power dissipation in the reflective loads at the cost of slightly increased insertion–loss variation along the phase shifter tuning range, representing a practical trade–off between RF performance and power consumption in the WPT–powered beamforming system.

The measurement setup used to characterize the fabricated phase shifter is shown in **Figure 5.23**. The phase shifter PCB is connected between the two ports of the PNA using coaxial cables and SMA connectors to measure its S–parameters. A DC power supply (Siglent SPD3303X series) is used to generate the control voltage required for tuning the varactor diodes. The bias voltage is applied to the varactor bias pads through external wires connected to the PCB.

The measured input reflection coefficient $|S_{11}|$ of the fabricated phase shifter from 1 to 5 GHz is shown in **Figure 5.24**. The light red traces correspond to individual measurements obtained at different varactor control voltages ranging from 0 V to 10 V, while the dark red curve represents the average response across all bias conditions. As expected for a reflective phase shifter, the impedance seen at the input varies with the varactor capacitance, which causes small variations in the reflection response across the tuning range.

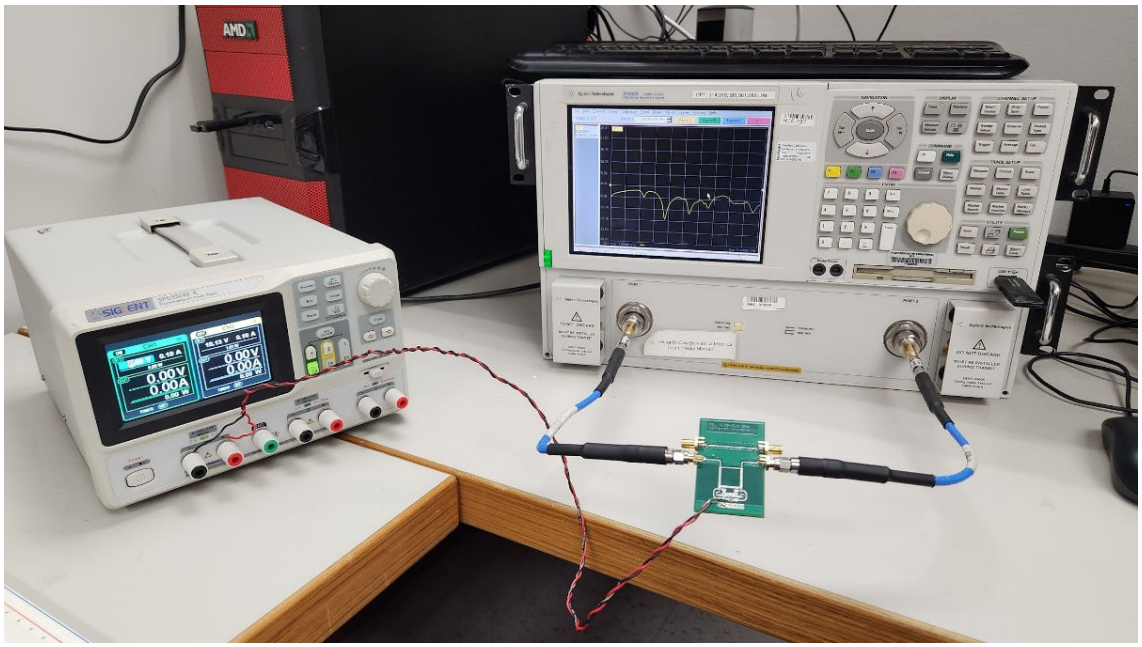


Figure 5.23 Experimental setup of the reflective phase shifter characterization.

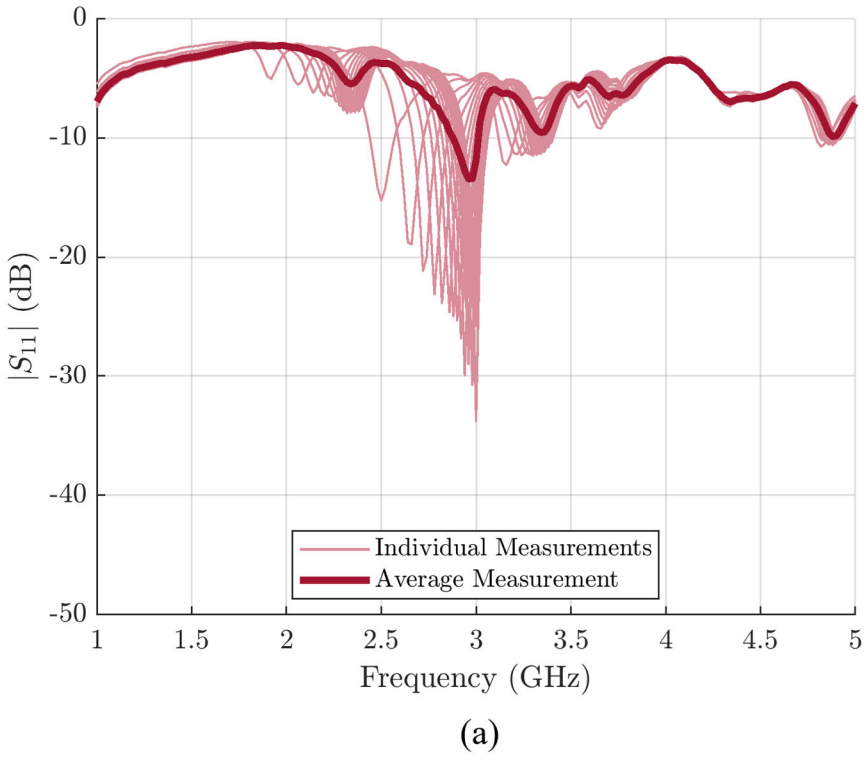


Figure 5.24 Measured $|S_{11}|$ of the reflective phase shifter across control voltages, showing individual responses (light red) and their average (dark red).

The measurements indicate that the minimum reflection point occurs around 3 GHz, whereas the original design targeted an operating frequency of 3.5 GHz. This frequency shift is primarily attributed to stack–up differences between the substrate parameters assumed during design and those of the manufactured FR–4 board. Regardless, considering a –5 dB reflection bandwidth, the phase shifter exhibits an operational range approximately between 2.75 GHz and 3.5 GHz, which is suitable for the beamforming experiments conducted in this work. Additionally, the phase shifter bandwidth is within the gap between third and fourth harmonics of the 935 MHz used for data carrier, which helps reduce potential interference.

For this work, the exact operating frequency of the phase shifter is not critical; rather, the primary requirement is achieving controllable phase tuning to enable beam directivity in the antenna array. Hence, the frequency shift can be corrected in subsequent manufacturing runs.

The measured phase response of the fabricated reflective phase shifter as a function of the varactor control voltage is shown in **Figure 5.25**. **Figure 5.25**(a) presents the absolute transmission phase $\angle S_{21}$, while **Figure 5.25**(b) shows the relative phase shift obtained by referencing the phase to the value at 0 V control voltage.

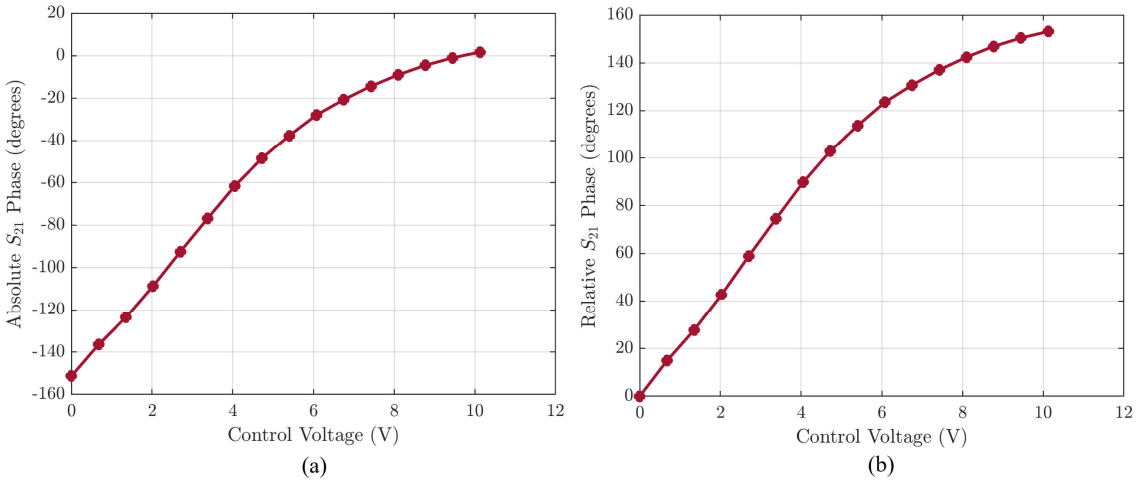


Figure 5.25 Measured S_{21} phase showing: (a) absolute phase, and (b) relative phase.

The measurements indicate a monotonic phase variation with increasing control voltage. From **Figure 5.25**(a), the absolute transmission phase varies from approximately -155° to 0°, while the relative phase response in **Figure 5.25**(b) shows a total achievable phase tuning range of approximately 155°. This continuous phase variation confirms the proper operation of the reflective phase shifter architecture and demonstrates that the varactor–based tuning mechanism effectively controls the phase of the RF signal.

The available 155° phase tuning range is sufficient to generate different discrete phase states required for the beam–steering operation of the antenna array presented in the following section. By selecting appropriate control voltages corresponding to different phase values, a few phase states can be defined and applied across the elements of the antenna array to steer the radiation beam in desired directions. In the next section, these measured phase responses are used to establish the phase–state mapping required for beam–steering.

5.3.4 Beam-steerer characterization

Having established the operation of the reflective phase shifter in the previous subsection, we now turn to the designed antenna array, from which the beam–steering system is realized. The phase shifters developed earlier are integrated with the array elements to enable controlled phase distribution across the aperture, forming the basis of the beamformer. In this subsection, the antenna array is first characterized in terms of its operating frequency range, followed by an evaluation of its radiation patterns under different phase configurations. The measured results are then compared with simulations to validate the performance of the phased array part.

The designed antenna array used for beam–steering is shown in **Figure 5.26** and consists of a 2×4 microstrip patch array implemented on an FR–4 substrate for operation around 3.5 GHz. As discussed in Subsection 3.1.2, microstrip patch antennas were selected due to their planar structure, ease of integration with PCB technology, and relatively high gain compared to other low–profile antennas.

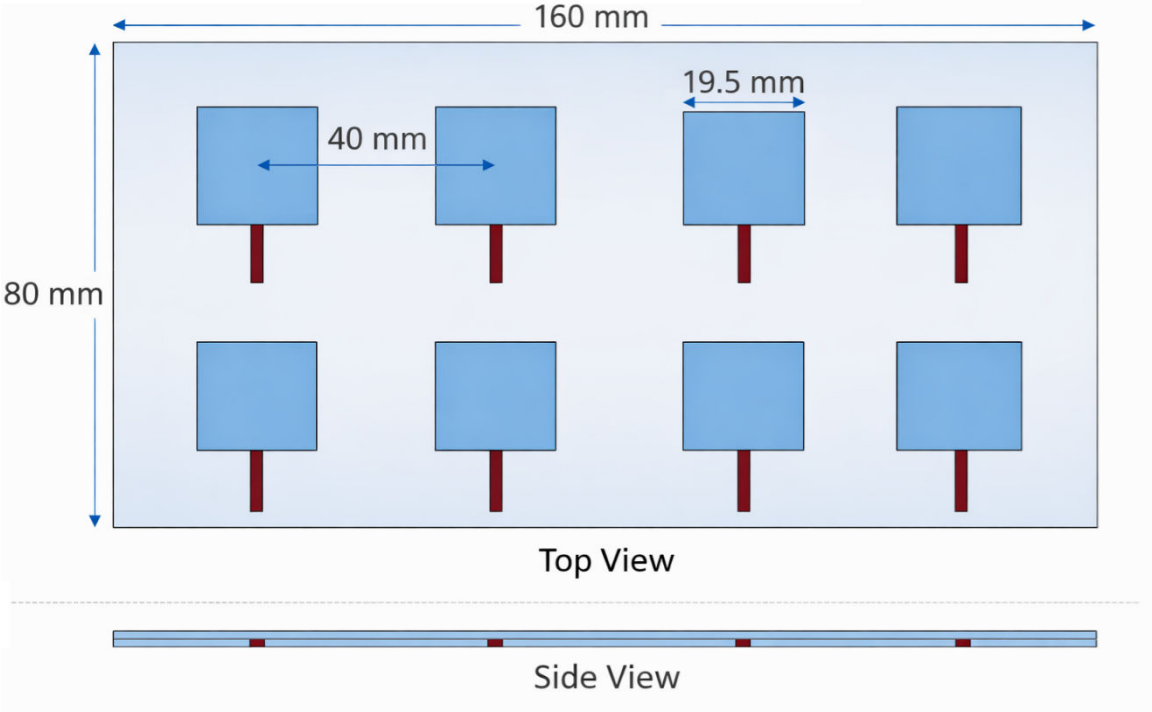


Figure 5.26 Top and Side View of a 2x4 patch antenna array [Designed by Dr. Kam Kedze].

At 3.5 GHz, the free–space wavelength is approximately $\lambda \approx 85.7$ mm. The chosen inter–element spacing of 40 mm corresponds to approximately 0.47λ, which is close to the conventional $\lambda/2$ spacing used in phased arrays. This spacing is selected to avoid grating lobes while maintaining good beam–steering capability, as mentioned in Subsection 3.1.3. Each patch has a width of approximately 19.5 mm, while the overall array dimensions are 160 mm × 80 mm.

The array employs a proximity–coupled feeding technique, where the feed lines are located beneath the radiating patches and electromagnetically couple to them. The proximity–coupled structure is well–suited for multilayer PCB implementations and allows the feeding network to be integrated cleanly with the phase shifters.

The antenna array was simulated using ANSYS HFSS, where it achieved a gain of approximately 10.3 dBi at 3.5 GHz, as shown in **Figure 5.27**, confirming the expected gain enhancement compared to a single patch element (**Table 3.1**).

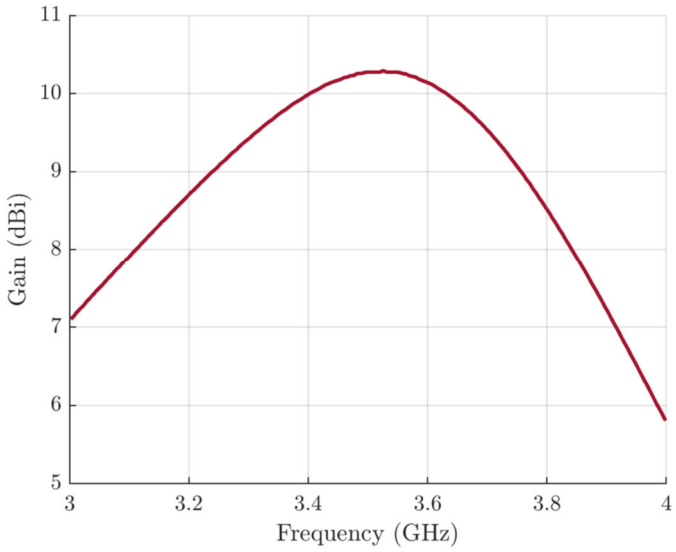


Figure 5.27 Gain simulation of the 2x4 patch array design [Courtesy of Dr. Kam Kedze].

Based on the measured performance of the reflective phase shifter presented in the previous subsection, a maximum continuous phase tuning range of approximately 155° is attained. This phase range enables the implementation of progressive phase excitation across the array elements to achieve beam–steering. Full–wave simulations indicate that by applying a progressive phase shift of 46.59° between adjacent elements along each row, the main beam can be steered up to approximately 15° from broadside. Similarly, a smaller progressive phase shift of 31.26° results in a beam–steering angle of approximately 10°. These results demonstrate that the available phase tuning range of the designed phase shifter is sufficient to achieve practical beam–steering in the proposed array configuration, as illustrated in **Figure 5.28** for different steering states ($S0 \rightarrow 0°$, $S1 \rightarrow 10°$, and $S2 \rightarrow 15°$).

The fabricated phased–array PCB is shown in **Figure 5.29**. The array is implemented on a four–layer 2 mm FR–4 substrate to maintain low fabrication cost while enabling the integration of both the radiating elements and the RF phase shifters within a compact structure. The top layer consists of the 2×4 patch antenna array, which forms the radiating aperture of the system. The second layer is dedicated to the feeding network, where microstrip lines are used to distribute the RF signal to each antenna element using a proximity–coupled configuration. The third layer serves as a continuous ground plane,

providing isolation between the radiating elements and the underlying phase shifters, while also stabilizing the electromagnetic performance of the array. The fourth (bottom) layer integrates the eight reflective phase shifters along with the power divider network, which distributes the input RF signal from a single SMA connector to all antenna elements.

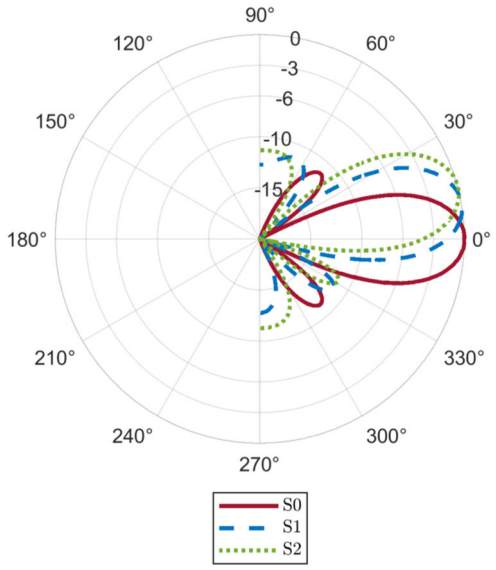


Figure 5.28 Radiation pattern simulations of the 2x4 patch antenna array for different phase shift configurations: $S0 \rightarrow 0°$ (red), $S1 \rightarrow 10°$ (blue), and $S2 \rightarrow 15°$ (green).

Each phase shifter is connected to an antenna element, enabling independent phase control across the array. The biasing and control signals for the phase shifters are routed to a 2×5 header connector, where eight pins are used to control the individual phase shifters, and the remaining two center pins are allocated for ground connections.

The measurement setup used to characterize the fabricated phased array is shown in **Figure 5.30**. The array is connected to the PNA through an SMA interface, while the bias voltages controlling the eight phase shifters are supplied through a breadboard interface, allowing independent control of each element. The objective of this measurement is to evaluate the $|S_{11}|$ of the overall array under different phase–control states and to assess the impedance response across various beamforming configurations.

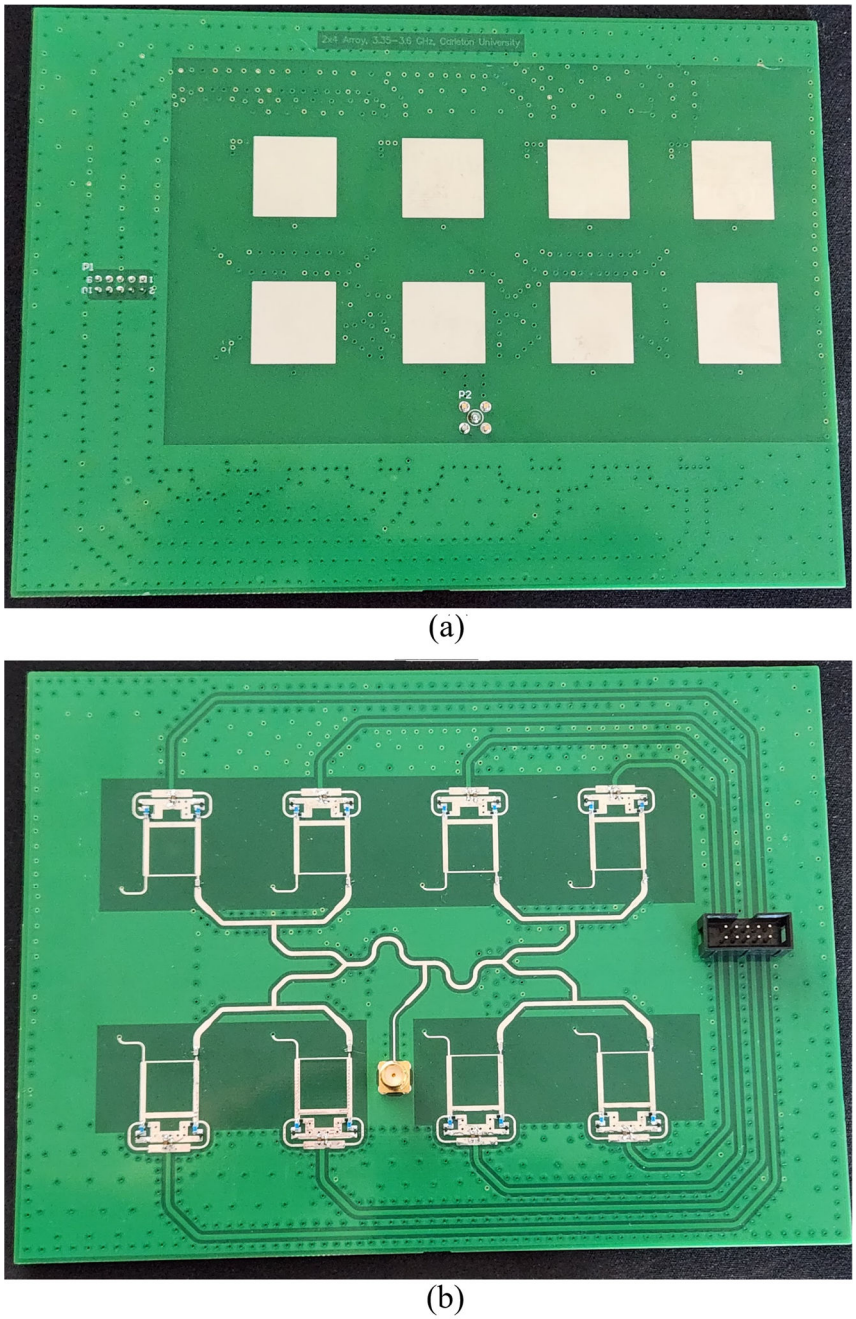


Figure 5.29 Fabricated PCB of the 2x4 beam–steerer showing: (a) top panel, and (b) bottom panel [Designed by Dr. Maryam Hasheminasab; experimentally validated by the author].

The measured $|S_{11}|$ of the phased array for multiple phase–control states is shown in **Figure 5.31**. The light red curves represent the individual measurements corresponding to different test states described below, while the thick dark red curve represents the averaged value across all tested states.

The first test corresponds to a uniform excitation test, where all phase shifters are set to the same control voltage. Three cases were evaluated: 0 V, mid–range control voltage (≈ 5 V), and maximum control voltage (10 V). The measured $|S_{11}|$ responses for these cases were found to be nearly identical indicating that the array maintains a consistent input impedance regardless of the uniform phase state.

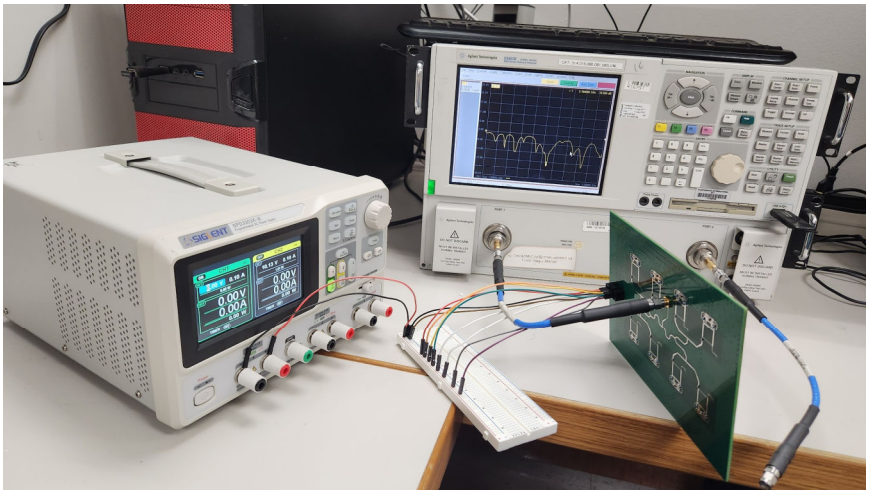


Figure 5.30 Test setup of the 2x4 beam–steerer.

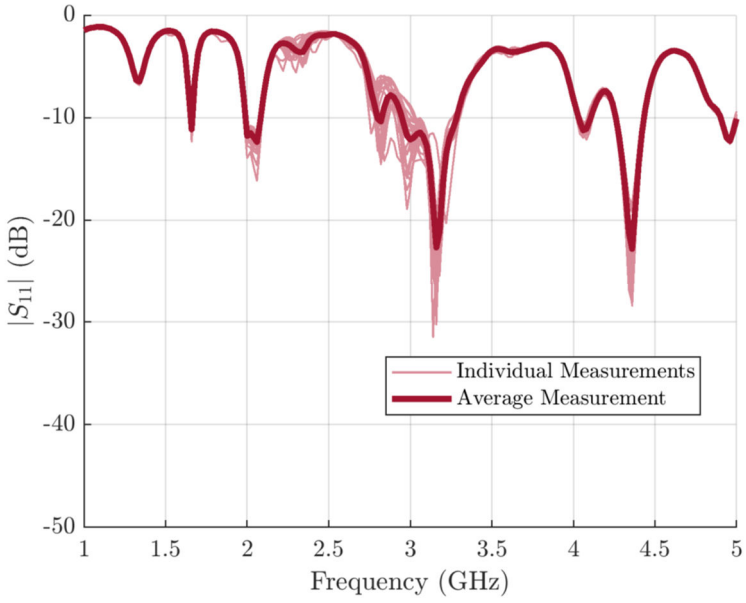


Figure 5.31 Beam–steerer measurement results showing measured $|S_{11}|$ per test state (light red), and average $|S_{11}|$ (dark red).

The second test involves a single–element variation test, where one phase shifter at a time is adjusted to mid–range and maximum control voltages while the remaining elements are kept fixed. Although slight shifts in $|S_{11}|$ were observed due to local impedance perturbations, the overall responses remained very similar across all elements, demonstrating good robustness of the array to individual phase variations.

Next, a symmetry test was performed by applying identical control voltages to symmetric groups of elements, including outer elements, inner elements, and corresponding top and bottom pairs. The resulting $|S_{11}|$ responses showed minimal variation, confirming that the array preserves impedance symmetry under balanced excitation conditions. This was followed by diagonal and anti–diagonal excitation tests, where four different configurations were evaluated. Again, the measured responses were highly consistent, further validating the stability of the array input matching under non–uniform phase distributions.

Finally, a progressive phase excitation test was conducted to emulate beam–steering conditions. In this case, the control voltage was incrementally varied across the array elements, first along one row, then the other, and finally across all elements, using steps of approximately one–third of the full control range. Despite the introduction of phase gradients, the measured $|S_{11}|$ remained consistent, indicating that the phased array maintains good impedance matching even under beam–steering operation.

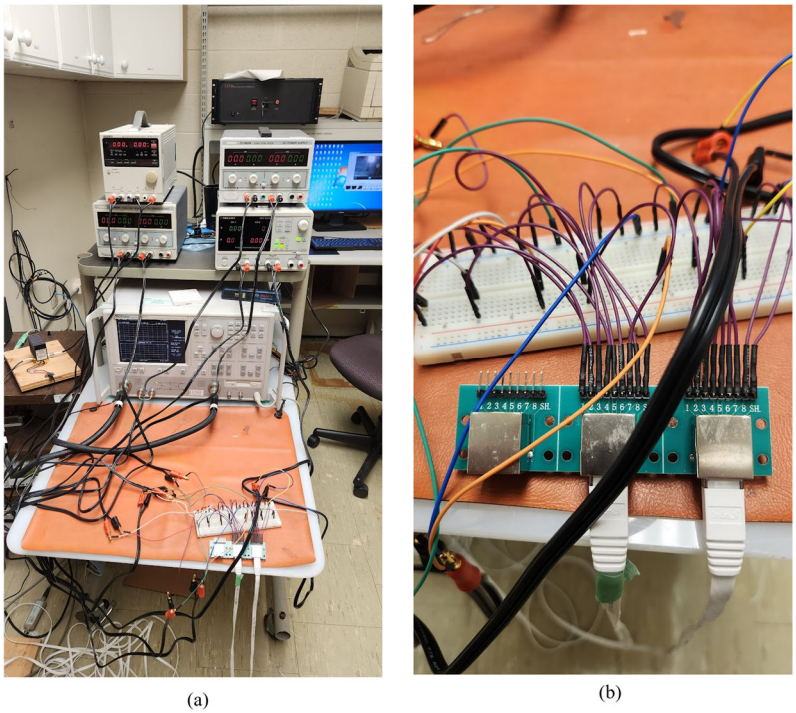
The close agreement between the individual traces indicates that the array maintains a relatively stable input impedance regardless of the applied phase distribution.

It can be observed that the resonance is shifted from the intended 3.5 GHz design frequency to approximately 3.15 GHz. This frequency shift is again attributed to stack–up discrepancies between the assumed substrate parameters during design and the actual manufactured FR–4 substrate.

Despite this shift, the array still exhibits a suitable operating bandwidth. Considering a –5 dB reflection coefficient criterion, the bandwidth extends approximately from 2.75 GHz to 3.4 GHz, which remains adequate for the intended beamforming operation. Moreover,

the consistency of $|S_{11}|$ across different phase states confirms that the phased array preserves good impedance matching under beam–steering conditions.

Now, the phased–array radiation pattern will be measured in an anechoic chamber using the previously defined phase states ($S0$, $S1$, and $S2$) to validate the beam–steering accuracy. **Figure 5.32** shows the control–room side of the measurement system. It includes an Anritsu 37397C Vector Network Analyzer (VNA) and four DC power supplies; each supply provides two independent outputs, giving a total of eight bias channels to control the eight reflective phase shifters. The DC bias leads from the supplies are gathered on a small breadboard and routed to a compact RJ–45/Ethernet breakout (an "Ethernet bridge"). The Ethernet cables are used as a convenient, shielded multi–conductor feedthrough to carry the eight bias lines (plus ground return) through the chamber port to the array inside the anechoic chamber. To further improve signal integrity and reduce interference between control lines, the Ethernet pins were arranged in an alternating RF–GND–RF–GND configuration.



(a) (b)

Figure 5.32 Control–room view of the anechoic chamber measurement setup: (a) overall setup including the VNA and DC bias supplies, and (b) close–up of the RJ–45 (Ethernet) bias distribution interface ("Ethernet bridge").

Figure 5.33 shows the anechoic chamber. The measurement setup consists of a transmitting horn antenna and the phased–array under test, both mounted–on positioners and surrounded by RF–absorbing foam to suppress reflections. The array is held on a low–scattering support structure, with its backside accessible for DC biasing. The Ethernet cables entering the chamber are split out into individual conductors and connected to a 2×5 header on the array PCB, where the two center pins are connected to ground. Close–up views show the array aperture, the rear control network, and the Ethernet–based bias distribution interface used to control the reflective phase shifters during radiation pattern measurements.

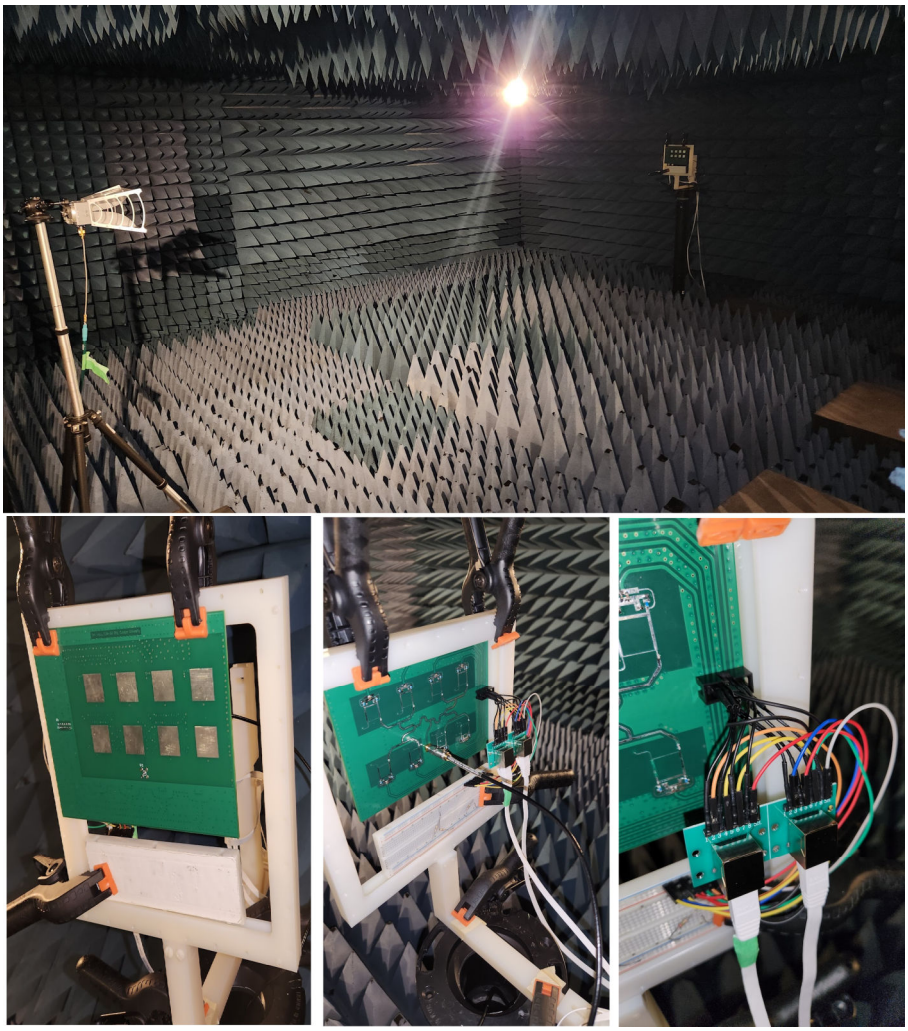


Figure 5.33 Anechoic chamber setup showing the transmitting horn antenna, phased–array under test, and Ethernet–based DC control distribution. Insets provide detailed views of the array and bias connections.

Figure 5.34 presents the measured radiation patterns of the phased array for frequencies ranging from 3.0 GHz to 3.5 GHz in steps of 0.1 GHz, where each subfigure corresponds to a different beamforming frequency. For each case, progressive phase shifts were applied across the array elements according to the phase–steering strategy discussed previously. The results demonstrate that the array is capable of achieving beam–steering, as evidenced by the shift in the main lobe direction for different phase states ($S0$, $S1$, and $S2$).

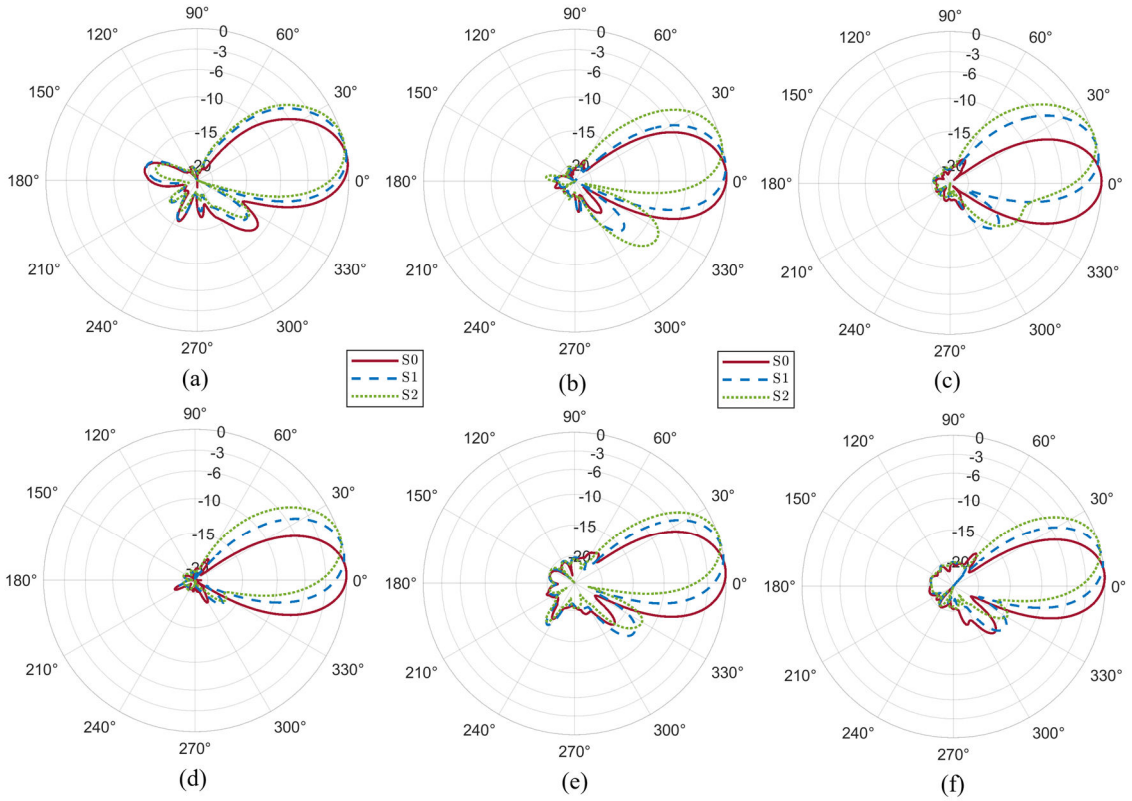


Figure 5.34 Direct–DC bias beam–steering measurement results showing radiation patterns for *S0* (red), *S1* (blue), and *S2* (green) progressive phase shift states at beam–forming frequencies of: (a) 3.0 GHz, (b) 3.1 GHz, (c) 3.2 GHz, (d) 3.3 GHz, (e) 3.4 GHz, and (f) 3.5 GHz.

It can be observed that the beam–steering performance varies with frequency. Among all measured cases, the radiation pattern at 3.3 GHz exhibits the closest agreement with the expected steering behavior. In this case, the main beam is well–defined, the steering angle progression is consistent with the applied phase shifts, and the radiation pattern shows the lowest sidelobe levels compared to other frequencies.

Figure 5.35 presents a comparison between the measured and simulated radiation patterns of the phased array for the three steering states at 3.3 GHz. The solid lines correspond to the measurements, while the dashed lines represent the simulation results. Overall, a good agreement between simulation and measurement is observed, confirming the validity of the design and the effectiveness of the implemented phase–shifting network.

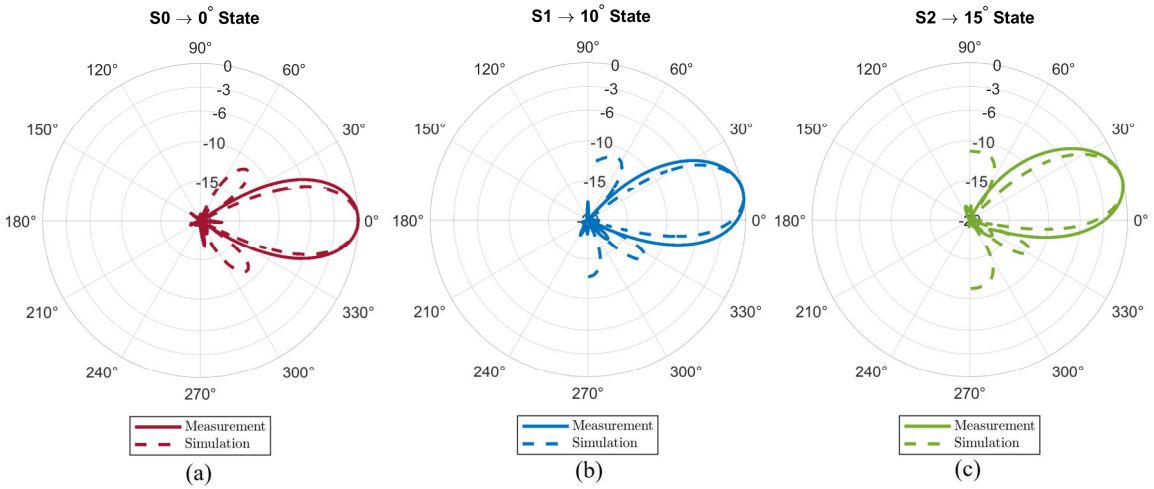


Figure 5.35 Comparison between direct DC bias control (solid) and simulation (dashed) of the 2x4 beam–steerer for different steering angle states: (a) *S0*, (b) *S1*, and (c) *S2*.

From the measurements, the initial steering angles were observed to be approximately 2°, 12°, and 17° for states $S0$, $S1$, and $S2$, respectively. The small offset in the first state is attributed to minor systematic measurement misalignment from antenna positioning and fixture orientation within the anechoic chamber. After accounting for this offset, the corrected steering angles become approximately 0°, 10°, and 15°, which match the simulated steering angles predicted during the design phase. The results clearly demonstrate that the proposed phased array successfully achieves the intended beam–steering functionality with performance closely aligned to simulation.

5.3.5 Beam-steerer control system experimental results

This subsection brings together the complete system from **Figure 5.14** by integrating all previously developed and tested components into a unified experimental setup. The focus is to validate the end–to–end operation of the proposed ASK–PWM control

architecture, combining both the control and beamforming functionalities. We begin by presenting the ASK–PWM demodulator and decoder PCB, including its interface with the FPGA and the implemented DACs used to generate the control voltages for the phase shifters. This control subsystem enables wireless transfer and reconstruction of phase information, which is then applied to the beamforming network. Subsequently, the full beamformer is assembled by connecting the control PCB with its communicating antennas with the phased–array antenna and phase shifter network. Finally, the complete system is experimentally evaluated to demonstrate wireless control and beam–steering, thereby validating the feasibility of the proposed architecture for phased–array applications

The fabricated control PCB, shown in **Figure 5.36**, implements a discrete–component realization of the ASK demodulator and PWM decoder, based on the design presented in Subsection 5.3.2 and realized on a 0.6 mm FR–4 low–cost substrate. These analog front–end circuits are located on the left side of the board and would interface the communicating antenna via an SMA connector. With the exception of passive components, the demodulation stage employs SMS3922–079LF Schottky diodes (Skyworks, USA), selected for their low turn–on voltage, low series resistance, and low junction capacitance, enabling envelope detection. The comparators used in both the ASK demodulator and PWM decoder are BU5265HFV–TR devices (Rohm Semiconductor, Japan), which provide rail–to–rail output swing, operate from a low 2 V supply, and support operating frequencies up to approximately 14 MHz. Their CMOS–based implementation ensures minimal loading on the preceding analog stages. The PWM decoding stage further utilizes BSH103BK NMOS and BSH205G2 PMOS transistors (Nexperia, USA), whose low threshold voltages (below 1 V) and high switching speeds (up to 33 MHz) make them well–suited for low–voltage and low–speed requirements.

Extension headers are located on the top side of the PCB, enabling direct integration with the external digital control system (FPGA–based). To generate the required analog control voltages for the phase shifters, the digital signals are converted using R–2R ladder 4–bit DACs implemented on the right side of the board. The resulting analog voltages are then amplified using operational amplifier stages to extend the output range from the

FPGA's 1.8 V logic level to a maximum of 10 V, which is required for proper tuning of the varactor–based reflective phase shifters.

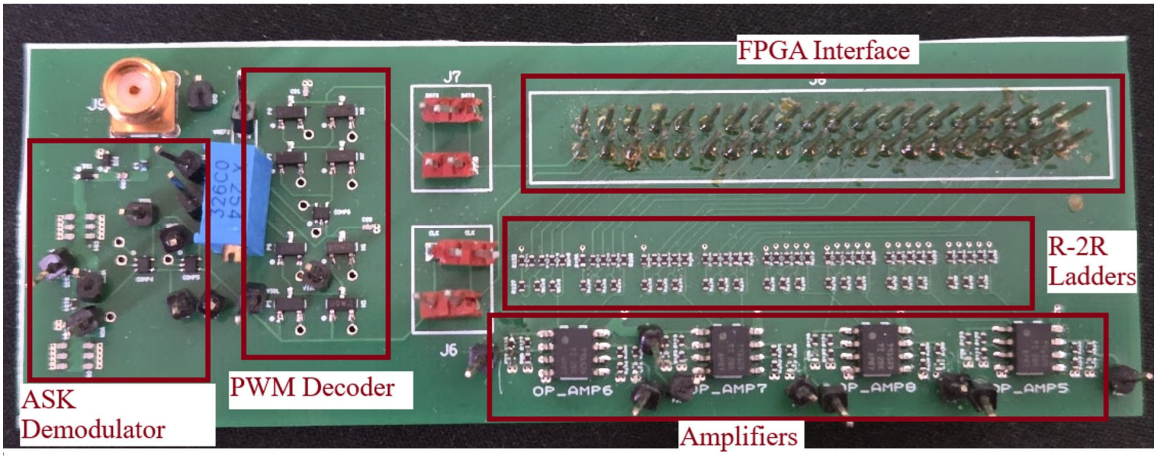


Figure 5.36 ASK–PWM control PCB prototype.

The Simulink model described in Section 4.4, specifically, the two digital frame router blocks, was translated into Very High–Speed Integrated Circuit (VHSIC) Hardware Description Language (HDL) or VHDL code and synthesized on the FPGA of the DE2–115 Development and Education Kit. The delay cells illustrated in **Figure 4.6** were manually implemented using 500 cascaded synthesized inverters, which were explicitly preserved from logic merging and timing optimization by the synthesis tool. The DE2–115 GPIO interface was used to provide the digital control signals. In total, 32 GPIO pins were configured as outputs, corresponding to 4 control bits per phase shifter, with 4 phase shifters per one control block of the two used. Additionally, two GPIO pins were configured as inputs to receive the CLK and PRE_DATA signals from the implemented ASK demodulator and PWM decoder, respectively.

The R–2R ladders were realized using 10–20 kΩ resistors. The non–inverting amplifier provides a gain of 6, implemented using a 5 MΩ feedback resistor and a 1 MΩ grounded resistor, where the use of megaohm–range resistances minimizes power consumption from the 12 V supply. The 12 V supply was chosen to allow for sufficient DAC range up to the needed 10 V output control voltage. The operational amplifier used is the TLV9152IDR from Texas Instruments, which supports supply voltages up to 16 V and provides a

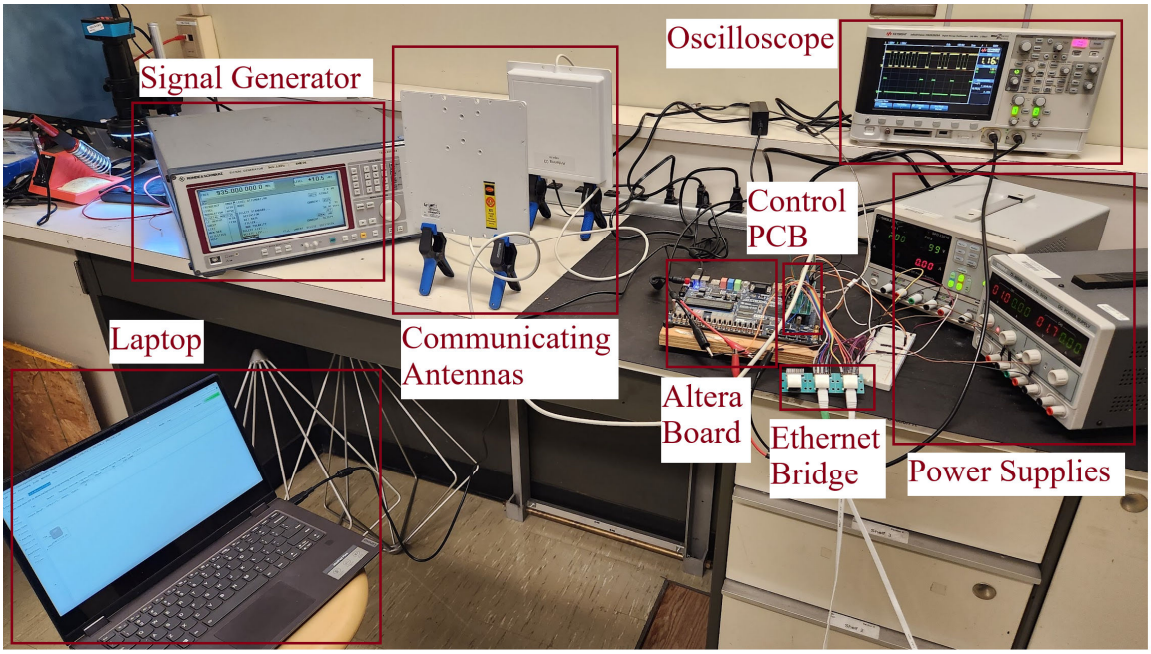
common–mode range from -0.1V to 13 V at a 12 V supply. Its 4.5 MHz gain–bandwidth product and 20 V/μs slew rate are sufficient for the DAC update rate of 582–842 samples/s.

The complete measurement setup is shown in **Figure 5.37**, where **Figure 5.37**(a) illustrates the control–side configuration and **Figure 5.37**(b) shows the FPGA–PCB interface. In the control setup, an SME06 signal generator (Rohde & Schwarz) was used to generate a 935 MHz carrier, which was modulated using the proposed ASK–PWM scheme. Since the signal generator does not natively support ASK modulation, its internal digital attenuator was programmed to emulate ASK–PWM modulation. The transmitted signal was radiated using communicating antennas characterized in Subsection 5.3.1. For simplicity, only a single receive antenna was used in this work, which was connected to the SMA input of the ASK–PWM control PCB mounted on the DE2–115 board.

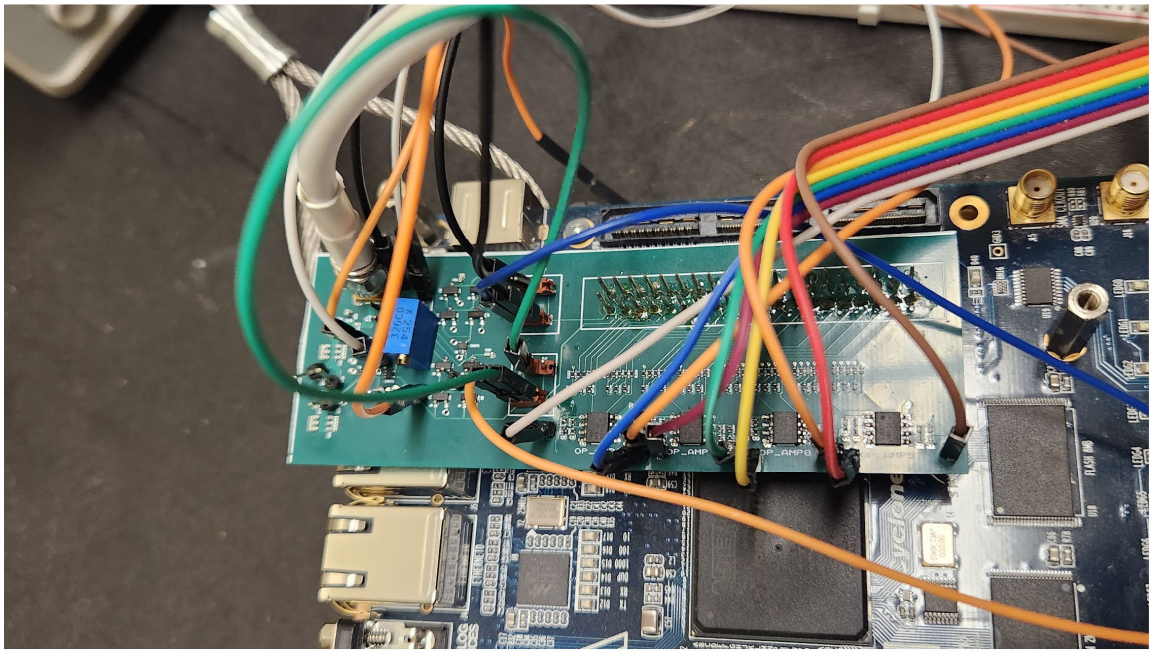
Two external power supplies were used to bias the system: a 2 V supply for the comparators and reference circuits, and a 12 V supply for the DAC amplification stages. A DSOX3024T oscilloscope (Keysight Technologies) was used to monitor waveform signals at designated test points on the PCB. The generated analog control voltages were routed through Ethernet–compatible connectors and transmitted to the anechoic chamber using RJ–45 cables. Inside the chamber, these signals were converted back to standard header connections and interfaced with the control inputs of the beamformer PCB.

The measured waveforms obtained from the proposed experimental setup are shown in **Figure 5.38**, validating the end–to–end operation of the ASK–PWM control system.

The ASK demodulation process is illustrated in **Figure 5.38**(a), validating the correct operation of the envelope detector and the dynamic reference generator implemented on the PCB. The output of the ASK demodulator (CLK) is shown in **Figure 5.38**(b). **Figure 5.38**(c) demonstrates the operation of the PWM decoder, validating the functionality of the skewed buffer stage. The output of the PWM decoder (PRE_DATA) is shown in **Figure 5.38**(d), confirming correct data recovery based on the pulse width of the extracted *CLK* signal.



(a)



(b)

Figure 5.37 Measurement setup of the ASK–PWM control side for the beamforming experiment: (a) complete hardware setup, and (b) zoomed view of the communication–control circuitry and its interconnections.

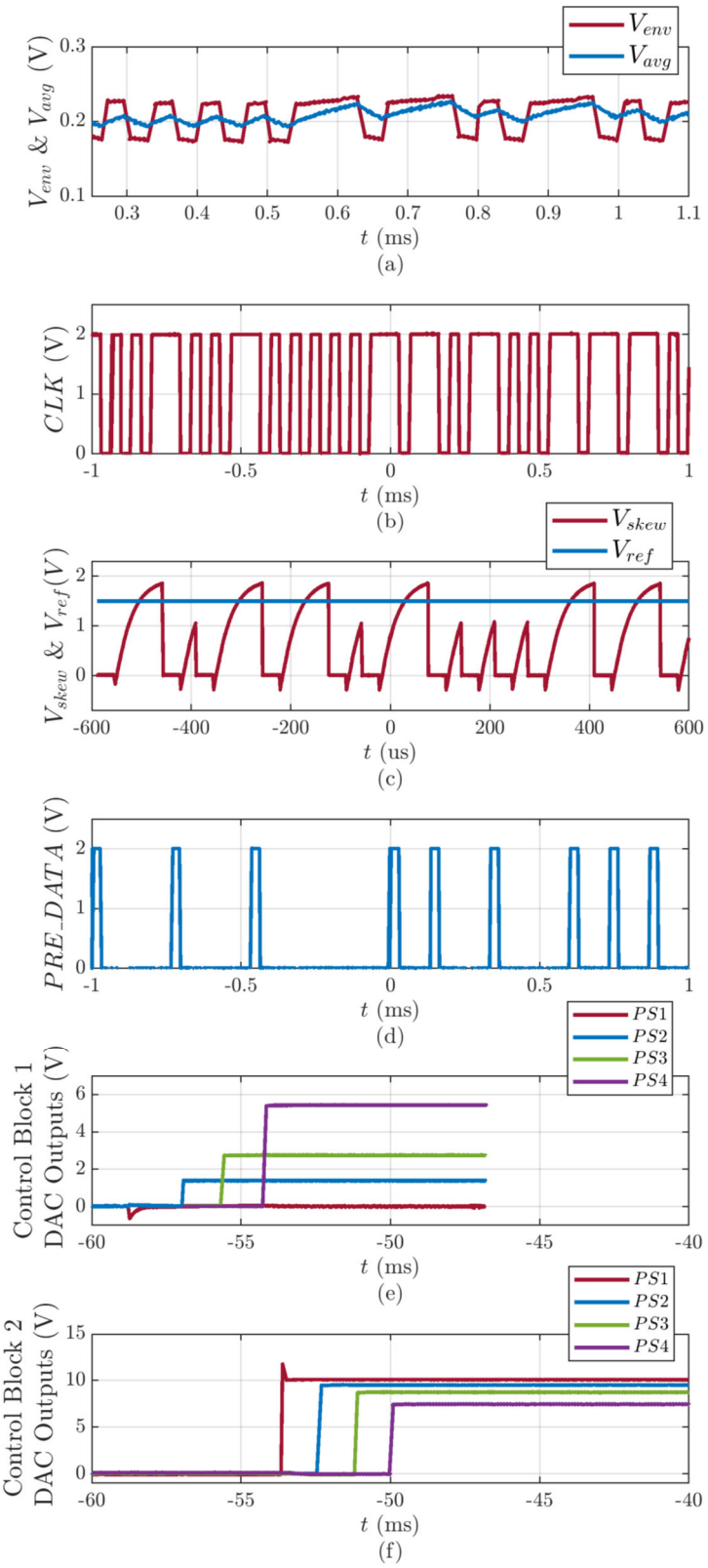


Figure 5.38 Measurement waveforms of proposed ASK–PWM control system: (a) V_{env} (red) and V_{avg} (blue), (b) *CLK*, (c) V_{skew} (red) and V_{ref} (blue), (d) *PRE_DATA*, (e) control block 1 DAC outputs, and (f) control block 2 DAC outputs.

The outputs of the DACs used for phase shifter control are shown in **Figure 5.38**(e) for control block 1 and **Figure 5.38**(f) for control block 2. The transmitted ASK–PWM pattern in this experiment matches the simulated pattern shown in **Figure 4.15**(a) in Section 4.4; accordingly, the DAC outputs on the PCB correctly reproduce the expected control voltages, confirming that the complete chain: from wireless ASK–PWM transmission to ASK–PWM demodulation and decoding, FPGA processing, and analog voltage control operates as intended. The pattern was repeatedly transmitted over 60 seconds, comprising 37,500 samples, of which 4 were received in error, resulting in a Sample Error Rate (SER) of $\approx 10^{-4}$.

The measured radiation patterns obtained using the proposed control system are shown for each steering state in **Figure 5.39**. The resulting beam directions correspond to measured steering angles of approximately 1°, 9°, and 14°, respectively, demonstrating successful beam–steering and validating the overall ASK–PWM–based control approach. These results are also compared with the radiation patterns obtained using direct DC bias control, as presented in the previous subsection. A close agreement between the two sets of measurements is observed, confirming that the proposed wireless ASK–PWM control system is capable of accurately reproducing the phase states required for beam–steering without the need for wired DC control.

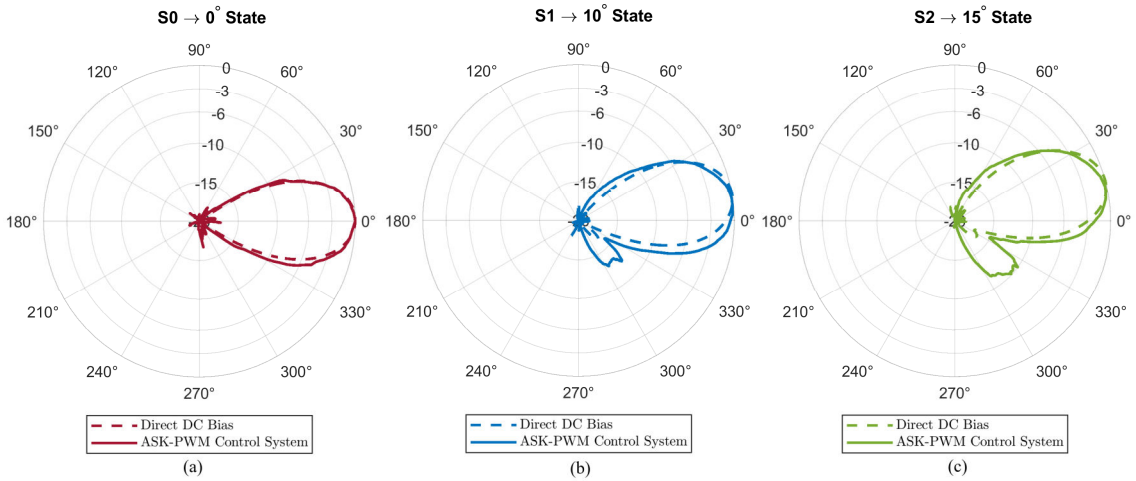


Figure 5.39 Comparison between measured radiation pattern of ASK–PWM control system approach (solid) and direct DC bias (dashed) of the 2x4 beam–steerer for different steering angle states: (a) *S0*, (b) *S1*, and (c) *S2*.

With reference to literature review done in Section 2.2, **Table 5.1** compares existing control and synchronization approaches for phased–array and beam–steering systems with the proposed work. Most prior works rely on SPI–based wired control and coherent architectures, which increase routing complexity and system overhead. In contrast, the proposed approach eliminates the need for wired data transfer, SPI, PLLs, and coherent control, thereby reducing complexity and improving scalability. This architecture represents a clear shift toward fully non–coherent, wireless, and low–overhead control, making it particularly well suited for large–scale and highly integrated array systems.

Table 5.1 Comparison of control and synchronization approaches in related works

Reference	Non–SPI	Non–Coherent	Wireless Link
This work	✓	✓	✓
[50]	✓	✗	✗
[51]	✗	✗	✗
[52]	✗	✗	✗
[53]	✗	✗	✗
[54]	✗	✗	✗
[55]	✓	✗	✗
[56]	✗	✗	✗
[57]	✗	✗	✗
[58]	✗	✗	✗
[59]	✗	✗	✗
[60]	✗	✗	✗
[61]	✓	✗	✗
[62]	✗	✗	✗
[63]	✓	✗	✗
[64]	✗	✗	✗

The intended objective of demonstrating a complete wirelessly controlled beam–steering system has been successfully achieved. The proposed ASK–PWM communication scheme was experimentally validated, enabling reliable extraction of clock and data signals from the received RF waveform without the need for conventional synchronization circuitry. Measurements confirmed that the system is capable of producing controlled beam directions that closely match both simulation and direct DC bias results, thereby validating the effectiveness of the proposed approach.

5.4 Conclusion

In this chapter, the proposed wireless control architecture was experimentally validated through a staged prototyping strategy that progressively built from digital control verification to complete beam–steering demonstration. The main objective of this chapter was to demonstrate that the subblocks developed earlier in the thesis can be realized in hardware using low–cost PCB implementations and FPGA–based control, while still providing the functionality required for practical phased–array operation. Furthermore, the proposed approach was benchmarked against existing wired and coherent control architectures, highlighting its reduced complexity and potentially improved scalability.

The first stage of experimentation demonstrated the correctness of the proposed digital control architecture. A 2x2 control subarray was implemented to verify the basic operation of the synthesized PWM decoder, frame router, and DAC interface. This prototype confirmed that the FPGA could correctly decode the control information, route the digital frames, and generate the corresponding analog voltages required to control the emulated RF beam–steering elements. The second stage extended this concept to a 4x4 emulated array, where the ID–based addressing mechanism was validated. The results showed that the control data could be selectively routed to specific subarrays, confirming the scalability of the proposed architecture and its suitability for larger phased–array implementations. These experiments were important because they established that the digital control framework works correctly before introducing the additional complexity of the ASK–PWM wireless interface.

Prior to hardware implementation, circuit–level simulations of the ASK–PWM demodulator and decoder verified correct signal recovery, timing behavior, and reliable pulse–width discrimination, ensuring correct operation of the wireless control link. The fabricated phase shifter and antenna array were also characterized experimentally, and the results showed that the array maintained good impedance matching under multiple phase–control states and was able to produce measurable beam–steering.

The chapter then moved to the PCB implementation of the complete ASK–PWM receiver integrated with the synthesized digital frame router and DAC subsystems. The analog front–end, including the ASK demodulator and PWM decoder, was realized using discrete components, and its operation was verified experimentally. The measured waveforms confirmed reliable envelope detection, dynamic reference generation, clock recovery, and PWM decoding. The complete wireless control link operated at 935 MHz with a data rate of 15 kbps, supporting effective sample transmission rates between 582–842 samples/s with an SER of 10^{-4}. The decoded digital signals were then interfaced and routed with the FPGA and converted into analog control voltages through the implemented R–2R DACs and amplifier stages. This part of the work demonstrated that the received wireless control signal could be translated into consistent, usable control voltages suitable for the phase shifters. Beam–steering was experimentally demonstrated using a 2x4 array at 3.3 GHz, and the measured radiation patterns agreed well with simulation and with the direct DC bias case, confirming that the proposed wireless control link can accurately reproduce the required phase states. In other words, the chapter validated not only the wireless reception of the ASK–PWM signal, but also the complete system required to transform that signal into practical control voltages for beam–steering.

Overall, the results demonstrated the feasibility of a compact, low–cost, and scalable wirelessly controlled beam–steering platform. Compared to conventional SPI–based and coherent control approaches, the proposed architecture eliminates extensive routing, synchronization overhead, and clock distribution. The chapter shows that wireless control, signal processing, and phased–array beamforming can be integrated successfully on PCB hardware. In the next chapter, this work is extended by combining WPT with the ASK–PWM receiver on PCB, moving toward a fully wireless and self–powered control platform.

Chapter 6: PCB Prototype of a Wirelessly Powered ASK–PWM Receiver

This chapter extends the work presented in the previous chapter by focusing on the system's power delivery mechanism. While the prior implementation demonstrated system–level functionality using an ASK–PWM demodulator and decoder, an FPGA, and DACs for beam–forming control, it relied on external power supplies. In this chapter, a wirelessly powered solution is introduced through the integration of WPT with the ASK–PWM receiver, eliminating the need for wired power while maintaining reliable communication. To emulate the expected loading of the digital control and DAC blocks, the receiver is interfaced with an equivalent resistive load representative of low–power operation.

The proposed system is realized through a PCB prototype, translating the design into a fully functional discrete implementation while addressing practical non–idealities. Particular emphasis is placed on the co–design of the WPT and ASK–PWM communication paths to ensure efficient WPT and robust data recovery.

The chapter begins with the definition of the wirelessly powered ASK–PWM receiver design specifications. These include achieving high PCE while generating a sufficient DC voltage level to reliably power low–power circuitry, such as low–power DACs, and the associated control blocks. These specifications guide the design choices of the RF energy rectifier and subsequent circuit stages.

Following this, the design and optimization of the RF energy rectifier are presented. Key aspects such as impedance matching, component selection, and large–signal behavior are discussed. The impact of PCB–induced inductive effects from vias and traces is then analyzed, showing how they alter the output filter response and degrade RF rejection. Mitigation techniques, including capacitor segmentation and layout–aware modeling, are proposed.

Next, the integration of the energy harvesting and communication paths is examined. Through impedance isolation, simultaneous power delivery and data transmission are achieved while preserving efficiency. This approach also enables flexible tuning of communication path time constants without affecting the harvesting path.

Finally, the complete wirelessly powered ASK–PWM receiver PCB prototype and its experimental setup are presented. Measurements including harvested voltage, PCE, and communication waveforms are provided to assess system performance and demonstrate its suitability for wirelessly powered beam–steering applications.

6.1 Wirelessly Powered ASK–PWM Receiver Specifications

To realize the wirelessly powered ASK–PWM receiver described in this chapter, the overall system architecture is first established, highlighting the integration of WPT and communication paths as well as the resulting power distribution within the receiver. In parallel, the key design specifications are defined, including achieving high PCE while generating a sufficient DC voltage level to reliably power low–power circuitry. These specifications guide the design choices of the RF energy rectifier and subsequent circuit stages.

Figure 6.1 illustrates the overall system architecture implemented in this chapter. The same transmitting and receiving antennas characterized in Subsection 5.3.1 are reused to enable both WPT and ASK–PWM communication over the shared RF channel. At the receiver side, the incoming RF signal is first passed by a matching network and then split into two paths: a harvesting path and a communication path. The harvesting path consists of an RF rectifier followed by a voltage regulator, which generates a high stable supply rail V_{DDH} for the receiver circuitry. In parallel, the communication path is made out of an ASK demodulator and a PWM decoder, followed by the digital frame router and DACs, ultimately controlling the phase shifters through amplifiers.

The circuits requiring a regulated high–voltage supply include the ASK demodulator, PWM decoder, digital frame router, and DACs. To ensure compatibility with the previously implemented FPGA–based system from Subsection 5.3.5, which operates at 1.8 V, a regulated supply of 2 V is selected for V_{DDH} in this chapter to provide sufficient margin while maintaining proper interfacing. Consequently, the harvested voltage must be sufficiently higher than the regulated level to ensure reliable operation. While a nominal harvested voltage of approximately 3 V would be sufficient under constant–envelope

conditions and LDO regulation, the use of ASK–PWM modulation introduces amplitude variations. Therefore, a higher target harvested voltage is adopted (4 V) to account for these fluctuations and maintain regulation under all operating conditions.

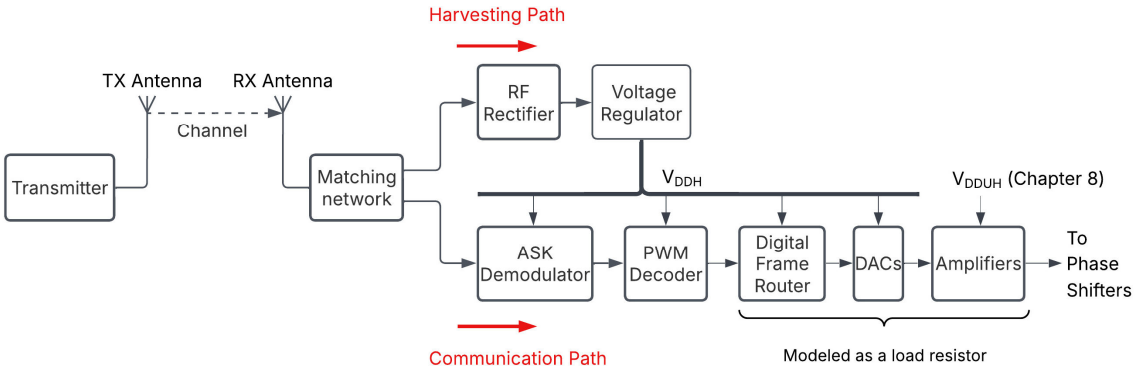


Figure 6.1 System architecture of the wirelessly powered ASK–PWM receiver for beam–steering control.

The amplifier stage, which interfaces with the phase shifters, requires a higher supply voltage up to 12 V to allow for the 10 V control range requirements of the phase shifter identified in Subsection 5.3.3. This ultra–high–voltage domain (V_{DDUH}) is addressed separately and will be discussed in detail in Chapter 8.

From a power consumption perspective, the ASK–PWM demodulator and decoder utilize multiple comparators, contributing tens of microamperes of bias current. The DACs are assumed to operate in a micro–watt regime, requiring on the order of 100–200 µA each, with four DACs per control block. Based on these estimates, the total current drawn from V_{DDH} is approximated to be on the order of 1 mA. Accordingly, the receiver load is modeled as a 1 mA equivalent load for design and validation purposes.

The system operates at an RF frequency range of 900–935 MHz, consistent with the antenna characteristics established in Subsection 5.3.1. The RF energy harvester is designed to achieve a PCE exceeding 50% while delivering sufficient DC voltage to sustain system operation. The communication bitrate is maintained at 15 kbps, as previously selected in Chapter 5, to minimize dynamic power consumption while ensuring reliable data transfer.

6.2 RF Energy Rectifier Schematic Design

The design of the RF energy rectifier is a critical step in enabling efficient WPT, as it directly determines the achievable DC voltage and PCE. Several rectifier topologies can be considered, as was discussed in Subsubsection 3.2.3.2, each offering different trade–offs in terms of output DC voltage, efficiency, and sensitivity under low–input–power conditions.

Among these topologies, the voltage doubler is selected in this work due to its ability to provide a higher DC output voltage at the targeted power level. For a harvested voltage of 4 V across a 1 mA load, the required output power is 4 mW (≈ 6 dBm). According to [95], voltage doubler topologies exhibit improved performance at input power levels above –6 dBm, making them well suited for this operating regime. The sensitivity of the rectifier is further enhanced through the use of a series inductor, as described in [85], which improves impedance matching and boosts the effective RF voltage at the rectifier input.

Figure 6.2 shows the schematic of the voltage doubler implemented in ADS. The RF source with series resistance R_0 models the harvesting antenna, feeding power (P_{in}) through a matching network composed of L_M and C_M, which is used to transform the input impedance of the rectifier to 50 Ω. The RF signal then passes through the voltage doubler formed by the series capacitor C_1, the diodes D_1 and D_2, along with the output capacitor C_2 and load R_L. The rectified voltage is developed across R_L, producing the harvested output voltage V_{EH}.

The capacitance C_1 is chosen as 10 pF to ensure that the input reactance is primarily dominated by D_1 and D_2, allowing efficient RF power transfer into the rectifier without attenuation. The output capacitor C_2 is implemented as a single large capacitance 600 pF to minimize voltage ripple at the harvested output node. The load resistance R_L is selected as 4 kΩ such that a harvested voltage of 4 V corresponds to a delivered power of 4 mW.

The rectifying elements are the same SMS3922–079LF Schottky diodes that were used for envelope detectors in Subsections 5.3.2 and 5.3.5. These diodes were selected for their low turn–on voltage, low series resistance, and suitable junction capacitance. Their SPICE models are obtained from the manufacturer datasheet and used for large–signal simulation.

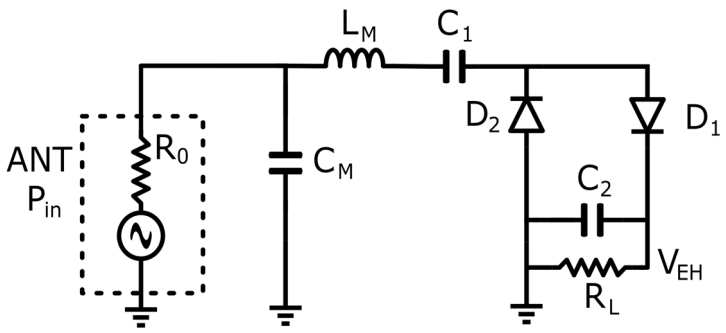


Figure 6.2 Voltage doubler circuit schematic.

The matching network is optimized by sweeping L_M from 1 nH to 100 nH while parametrically varying C_M. **Figure 6.3** presents the S_{11} plotted on a Smith chart using Large–Signal S–Parameter (LSSP) simulation. Each contour corresponds to a different value of C_M across the swept range of L_M. Based on this analysis, optimal values of $L_M = 33.68$ nH and $C_M = 2$ pF are selected to achieve input matching to 50 Ω, noting that these values may be further adjusted during PCB layout implementation.

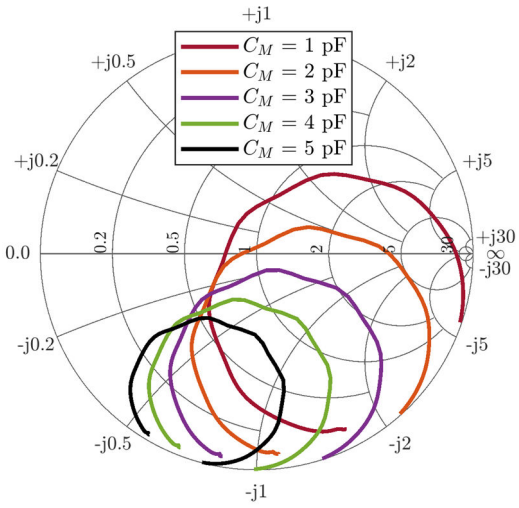


Figure 6.3 Simulated S_{11} on a Smith chart using LSSP analysis, showing swept L_M for different values of C_M.

Figure 6.4 shows the simulated DC harvested voltage and PCE. At an input power of 8 dBm, the rectifier achieves an output voltage of 4.2 V with a PCE of 71.0%, demonstrating its suitability for the targeted WPT application.

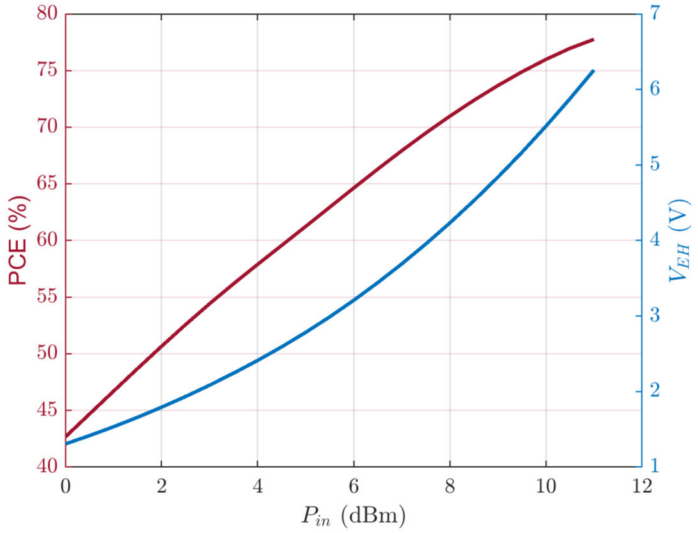


Figure 6.4 Simulated *PCE* (red) and V_{EH} (blue) as a function of P_{in} for the designed voltage doubler.

6.3 Parasitic Inductance Impact and Reduction

To verify the performance of the output filter in rejecting RF feedthrough and producing a smooth DC output, both transient and frequency response simulations were performed on the circuit in **Figure 6.2**. The results are presented in **Figure 6.5**. The transient response in **Figure 6.5**(a) shows that the output voltage settles to a steady DC value with negligible ripple and no observable RF variations, indicating effective suppression of the RF signal and its harmonics. The frequency response of the output filter, shown in **Figure 6.5**(b), exhibits a low–pass characteristic, providing strong attenuation of 44.6 dB at a frequency of 900 MHz. This confirms that the filter effectively rejects RF components while preserving the DC output.

An initial PCB layout was implemented using an FR–4 substrate with a thickness of 0.6 mm to enable more realistic simulation conditions, as shown in **Figure 6.6**. A transient co–simulation was then performed to evaluate the harvested DC output voltage, with the results presented in **Figure 6.7**(a). As observed, a significant amount of RF content appears at the output, which is not mitigated by increasing the value of C_2.

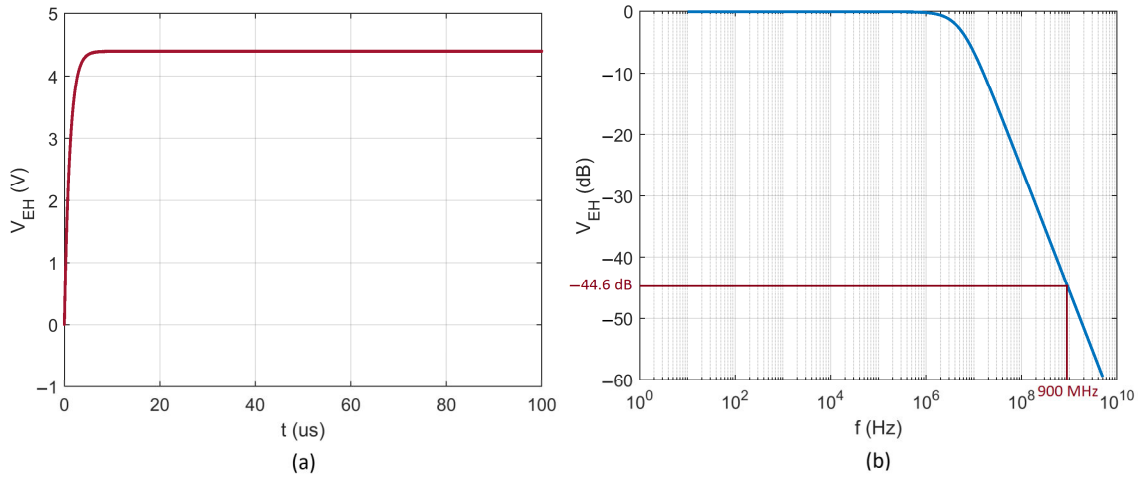


Figure 6.5 Output smoothness and RF feedthrough rejection of the schematic voltage doubler showing: (a) transient response, and (b) frequency response.

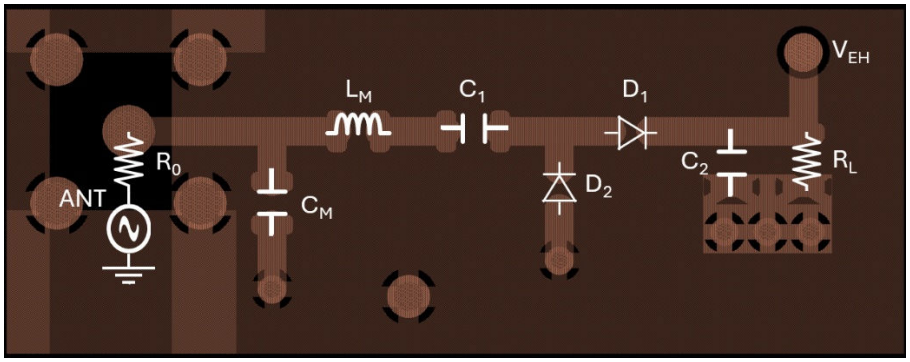


Figure 6.6 Initial PCB layout of the voltage doubler.

To further investigate this behavior, the frequency response of the output filter is examined in **Figure 6.7**(b). Unlike the schematic case, the response now exhibits a notch characteristic rather than a low–pass behavior, with a rejection of 17 dB at 900 MHz. This deviation is attributed to the parasitic inductive path introduced by the traces and vias connecting the rectification filter to the ground plane.

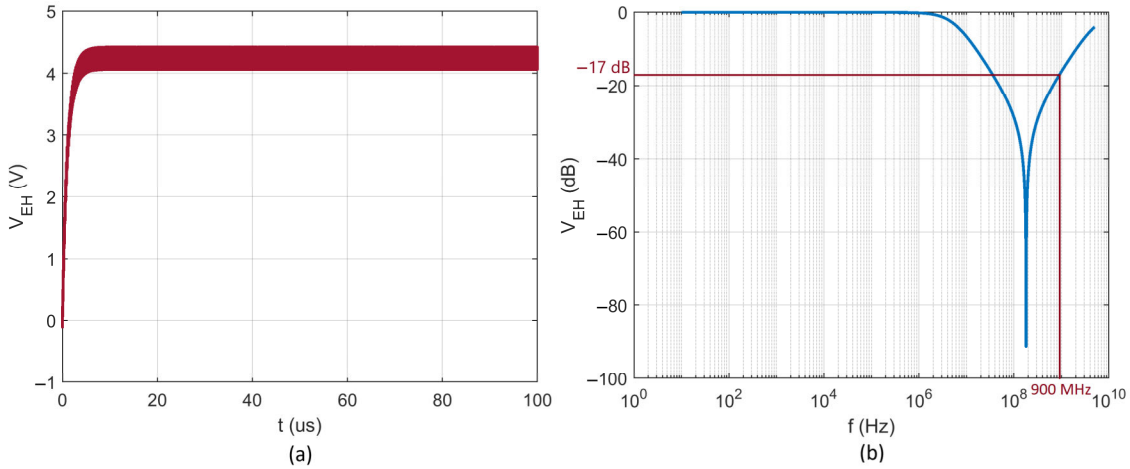


Figure 6.7 Output smoothness and RF feedthrough rejection of the voltage doubler layout in **Figure 6.6** showing: (a) transient response, and (b) frequency response.

To capture this effect, the ideal schematic in **Figure 6.2** is modified by introducing a parasitic inductance $L_p = 1.2$ nH in series with the output capacitance. To mitigate the impact of L_p, the output capacitor C_2 is split into multiple shunt capacitors connected in parallel. This approach reduces the effective parasitic inductance while maintaining the same total capacitance. The modified load is therefore modeled as N parallel branches, each of value C_2/N, such that the total capacitance remains unchanged. These modifications are shown in **Figure 6.8**. Around the notch frequency, where the capacitive impedance of C_2 becomes small, the output filter response can be approximated as follows:

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{R_L}{R_0 + R_L} \frac{s^2 + \dfrac{N}{L_p C_2}}{s^2 + s\left(\dfrac{R_0 R_L}{R_0 + R_L}\dfrac{N}{L_p}\right) + \dfrac{N}{L_p C_2}}, \tag{6.1}$$

where s is the complex frequency. (6.1) confirms the output filter response as a notch filter, which has a resonance frequency f_0 at:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{N}{L_p C_2}}. \tag{6.2}$$

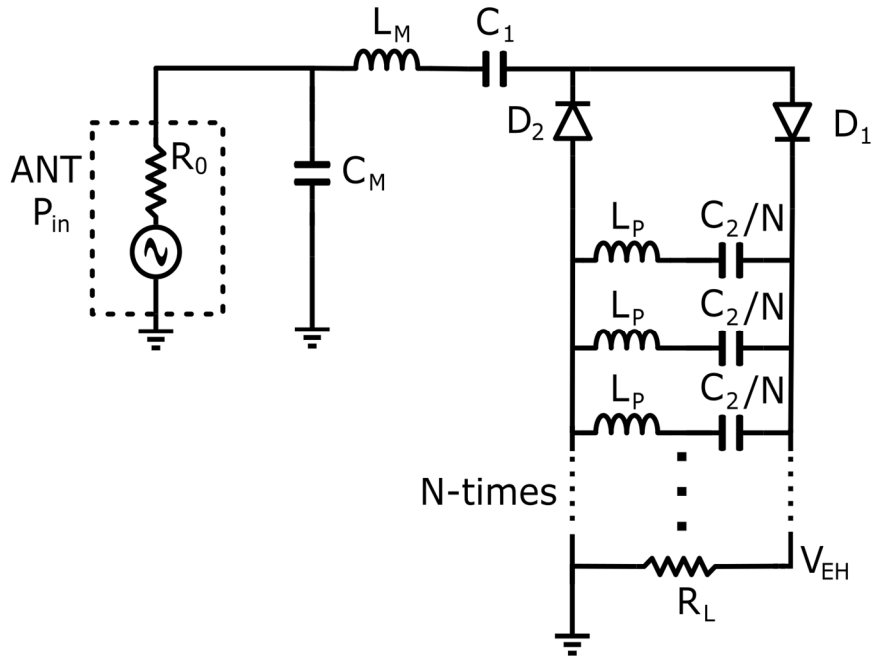


Figure 6.8 Modified rectifier and output filter model including parasitic inductance L_P and the segmented output capacitances.

From (6.2), it can be observed that increasing N (the number of parallel capacitive branches while keeping the total capacitance constant) effectively reduces the impact of the parasitic inductance. As a result, the resonance frequency f_0 increases, which in turn shifts the 3–dB cutoff frequencies and improves RF rejection at 900 MHz.

Based on this analysis, the 600 pF capacitor is implemented as six parallel 100 pF capacitors, as shown in the modified layout in **Figure 6.9**. The corresponding transient co–simulation demonstrates a significant reduction in RF leakage at the output, as shown in **Figure 6.10**(a). This improvement is attributed to the reduction in effective parasitic inductance, as multiple shunt paths divide the inductive contribution of the traces and vias approximately by the number of branches.

The frequency response in **Figure 6.10**(b) further confirms this behavior, where the increase in f_0 leads to enhanced RF attenuation, improving rejection at 900 MHz from 17 dB in **Figure 6.7**(b) to 35 dB in **Figure 6.10**(b). Although a similar increase in f_0 could be achieved by reducing C_2, doing so would increase output voltage ripple, which is undesirable. Therefore, reducing the effective parasitic inductance while maintaining a

large capacitance provides a more favorable trade–off, simultaneously minimizing both RF leakage and voltage ripple. This approach is applied throughout the design to suppress RF leakage at critical nodes.

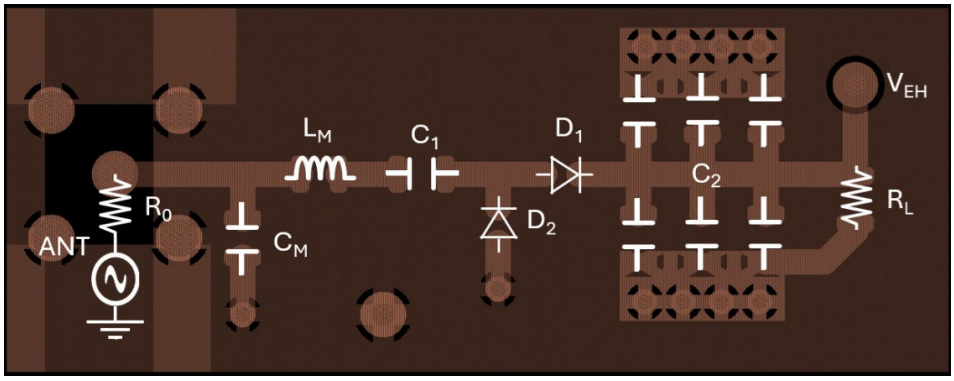


Figure 6.9 PCB layout of the voltage doubler decomposing C_2 into multiple parallel branches.

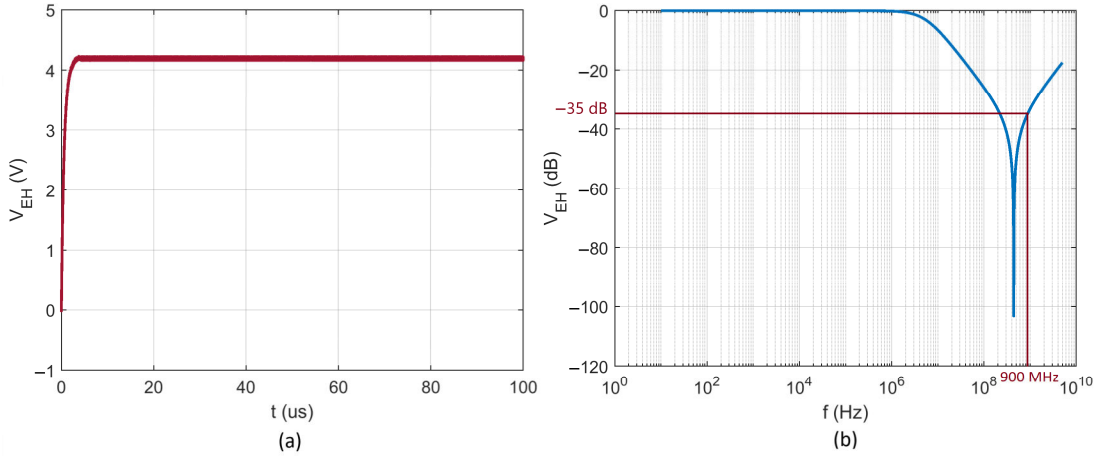


Figure 6.10 Output smoothness and RF feedthrough rejection of the modified voltage doubler layout in **Figure 6.9** showing: (a) transient response, and (b) frequency response.

Figure 6.11 illustrates the relationship between the number of parallel capacitive branches and RF leakage at the rectifier output $V_{RF\ OUT}$. As expected, increasing N reduces RF leakage; however, the improvement diminishes with each additional branch, indicating diminishing returns (blue dashed lines show significant reduced improvement as N increases beyond six). Based on this trade–off, six parallel capacitors are selected as an

optimal choice, providing effective RF suppression while maintaining compact PCB implementation.

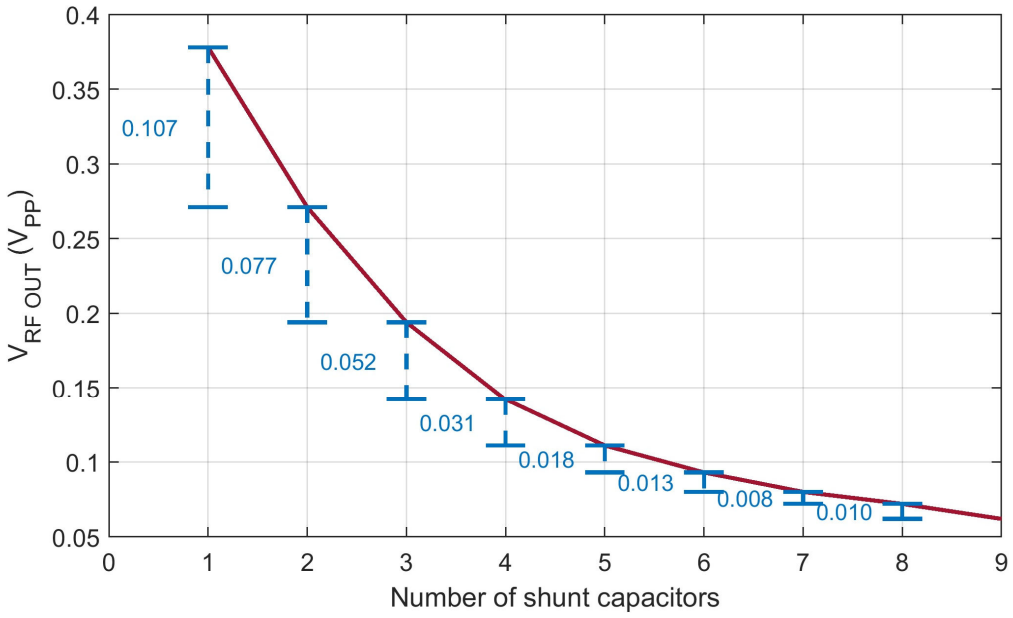
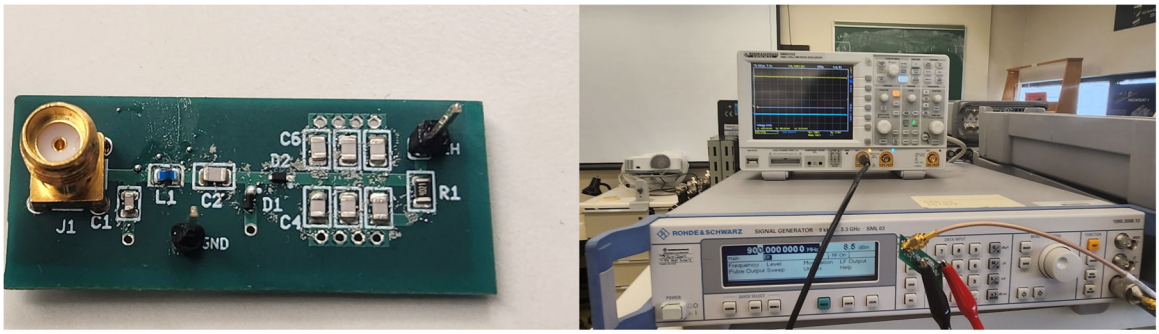


Figure 6.11 RF output ripple $V_{RF\,OUT}$ as a function of number of shunt capacitors N (blue dashes show ripple reduction differences for two consecutive N).

To validate the reduction of RF leakage achieved by the proposed capacitor segmentation technique, a PCB prototype of the rectifier was fabricated and experimentally characterized. The PCB shown in **Figure 6.12**(a) corresponds to the layout presented in **Figure 6.9** and is implemented on an FR–4 substrate with a thickness of 0.6 mm. An SMA connector is used for RF input, allowing direct connection to measurement equipment. The matching inductor and capacitor values were adjusted to 17 nH and 4.5 pF, respectively, to account for PCB parasitics and layout–induced effects.

The measurement setup is shown in **Figure 6.12**(b). An RF signal generator (Rohde & Schwarz SML03) is used to provide a continuous–wave input signal at 900 MHz with controlled power levels. The output of the PCB is monitored using a digital oscilloscope (Rohde & Schwarz HMO3000 series), which captures the transient voltage waveform and enables observation of any residual RF content at the output node.



(a) (b)

Figure 6.12 Experimental validation of reduced inductive effects via shunt capacitive branching showing: (a) PCB implementation, and (b) Measurement setup used for characterization.

Figure 6.13 compares the co–simulated and measured performance of the RF rectifier in terms of V_{EH} and PCE as a function of input power. Overall, a good agreement is observed between co–simulation and measurement, validating the design methodology.

From **Figure 6.13**(a), the measured V_{EH} closely follows the co–simulated trend across the input power range, with a slightly higher turn–on threshold for the diodes observed in measurements. As a result, the same output voltage of 4.2 V is achieved at an input power of 9 dBm, compared to 8 dBm in ideal schematic simulation of **Figure 6.4**.

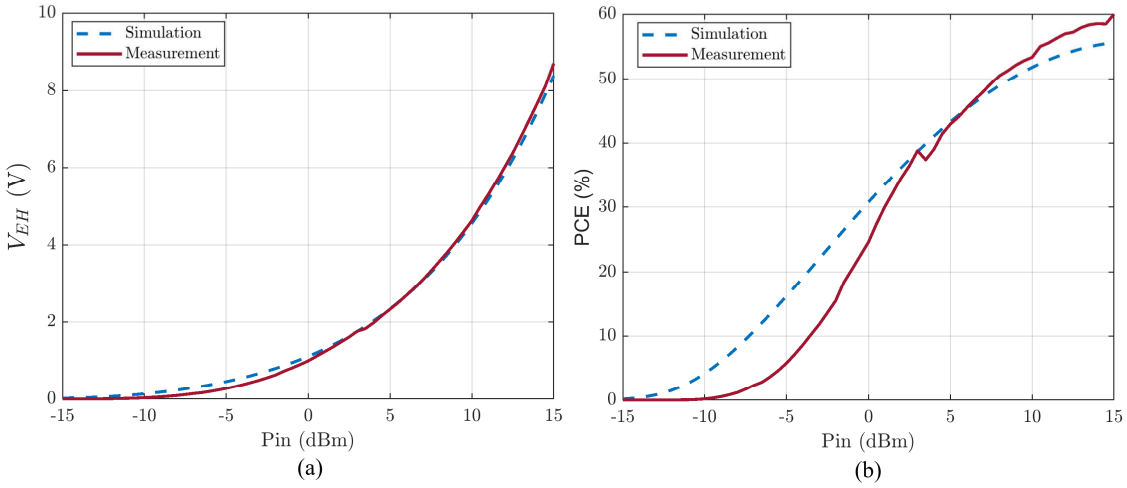


Figure 6.13 Comparison between co–simulated (blue dashed lines) and measured (red solid lines) rectifier performance versus input power showing: (a) V_{EH}, and (b) *PCE*.

Figure 6.13(b) presents the corresponding PCE comparison. In the ideal schematic simulations of **Figure 6.4**, a peak PCE of 71% is achieved at a harvested voltage of 4.2 V. However, when PCB substrate effects and coaxial cable losses are included through co–simulation, the predicted PCE decreases to approximately 51% for the same harvested voltage. The measured result shows a PCE of 53%, which matches the co–simulation.

Figure 6.14 shows the measured transient output voltage of the proposed rectifier at 10 dBm input power. The blue trace represents the harvested DC voltage, which is centered around approximately 4.6 V. A small residual RF ripple is observed, with a peak–to–peak variation of approximately 0.06 V, indicating effective suppression of RF leakage at the output node.

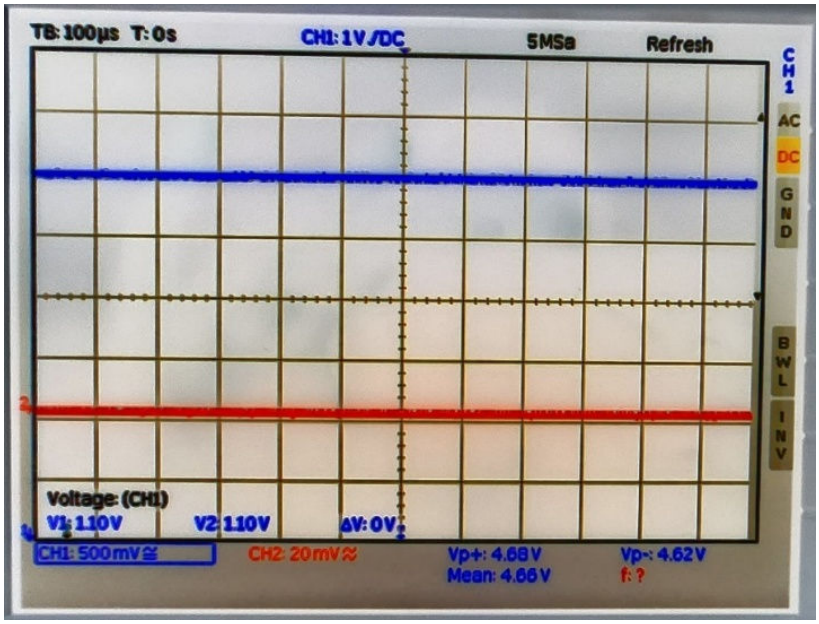


Figure 6.14 Measured output voltage waveform (blue) of the proposed voltage doubler.

This result is in close agreement with the simulations of **Figure 6.11**, where a peak–to–peak ripple of approximately 0.09 V was predicted when using six parallel shunt capacitors. The slightly lower ripple observed in measurements is primarily attributed to the limited bandwidth of the oscilloscope, which restricts its ability to fully capture high–frequency components around 900 MHz.

Overall, the strong agreement between simulations and measurements confirms the effectiveness of the proposed capacitor segmentation technique in minimizing RF leakage while maintaining a stable DC output.

6.4 Interfacing Harvesting and Communication Rectifiers

To enable simultaneous WPT and communication, the RF energy rectifier is interfaced with a dedicated communication rectifier, as shown in **Figure 6.15**. The design objectives of this interface are threefold: to preserve the PCE of the energy harvesting path, to generate a communication signal (V_{COMM}) compatible with the ICMR of the subsequent differential amplifier for NRZ ASK recovery, and to allow flexible design of the communication path time constants without impacting the harvesting performance.

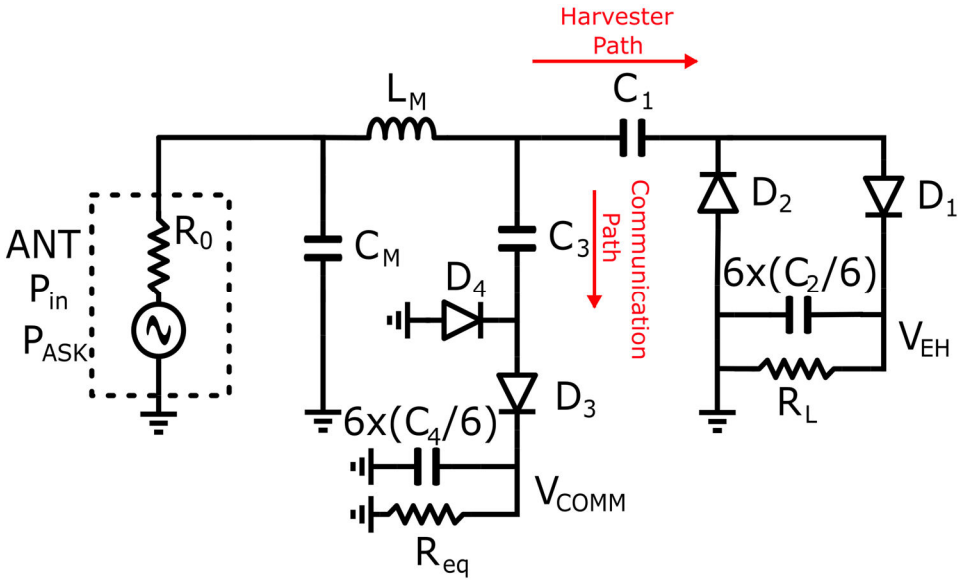


Figure 6.15 Interface between harvester and communication paths.

As illustrated in the figure, the incoming RF signal is first processed by the matching network (L_M, C_M), then split into two paths. The primary path, referred to as the harvester path, was discussed in the previous section.

In parallel, a secondary branch is introduced for communication (envelope detection), forming a rectification path composed of C_3, diodes D_3 and D_4, decomposed C_4, and the load R_{eq}. R_{eq} approximates the series combination of R_1 and R_2 from **Figure 5.17** in Subsection 5.3.2.

A key limitation of this topology arises from the interaction between the communication path and the harvesting path loadings. To preserve a high PCE in the harvester path, the current drawn by the communication branch must be kept at minimal. This requires a large R_{eq} relative to R_L , which effectively reduces loading on the harvesting rectifier. However, increasing R_{eq} results in a higher V_{COMM}, which may exceed the ICMR of the subsequent differential amplifier, making it unsuitable for reliable operation.

These trade–offs are illustrated in **Figure 6.16**. The x–axis represents the swept matching inductance L_M, which alters the input matching conditions as the effective load changes with different values of R_{eq}. **Figure 6.16**(a) shows that as R_{eq} decreases (i.e., increased loading), the resulting V_{COMM} is reduced, but at the cost of increased loading on the rectifier. Conversely, larger values of R_{eq} yield higher V_{COMM}, potentially exceeding acceptable voltage levels.

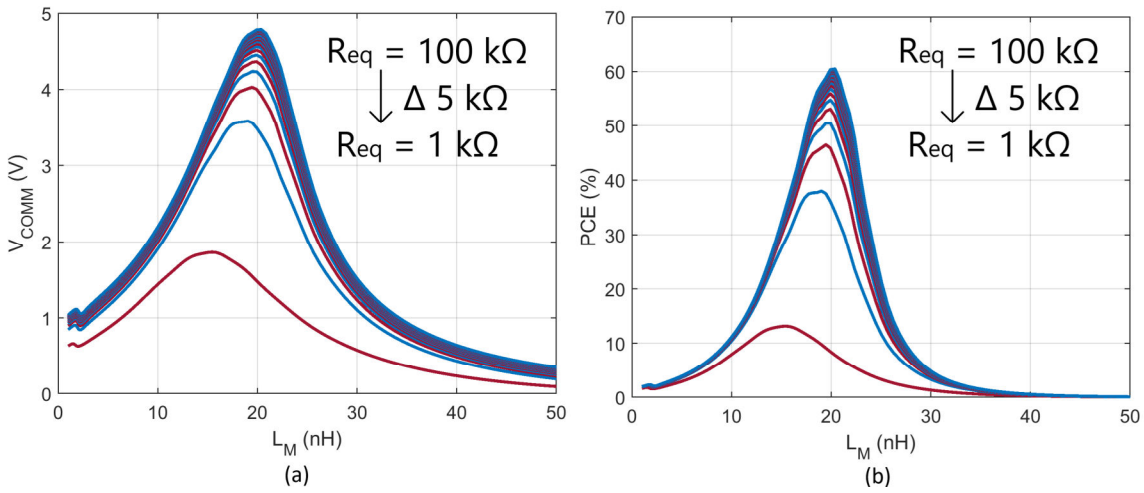


Figure 6.16 Simulations showing the impact of changing R_{eq} on: (a) V_{COMM}, and (b) PCE of harvesting path.

Figure 6.16(b) shows the corresponding PCE behavior of the harvesting path. It can be observed that smaller R_{eq} values significantly degrade the PCE due to increased loading of the communication path, while larger R_{eq} values preserve higher efficiency. This clearly highlights the trade–off between maintaining high PCE and achieving a suitable V_{COMM} level.

Additionally, R_{eq} (through R_1 and R_2) directly influences the time constants of the communication path (5.1)–(5.3). Adjusting R_{eq} to meet both PCE and V_{COMM} constraints reduces the available design flexibility in setting the desired time constants, thereby complicating the optimization of the ASK demodulator design.

Overall, R_{eq} cannot be independently optimized without affecting both the energy harvesting efficiency and the communication signal characteristics, motivating the need for improved isolation between the two paths.

To address the limitations observed in the previous topology, the modified circuit shown in **Figure 6.17** introduces a series resistance R_M in the communication path, placed in series with D_3. The purpose of R_M is to limit the current flowing through the communication branch, thereby improving the isolation between the communication and energy harvesting paths.

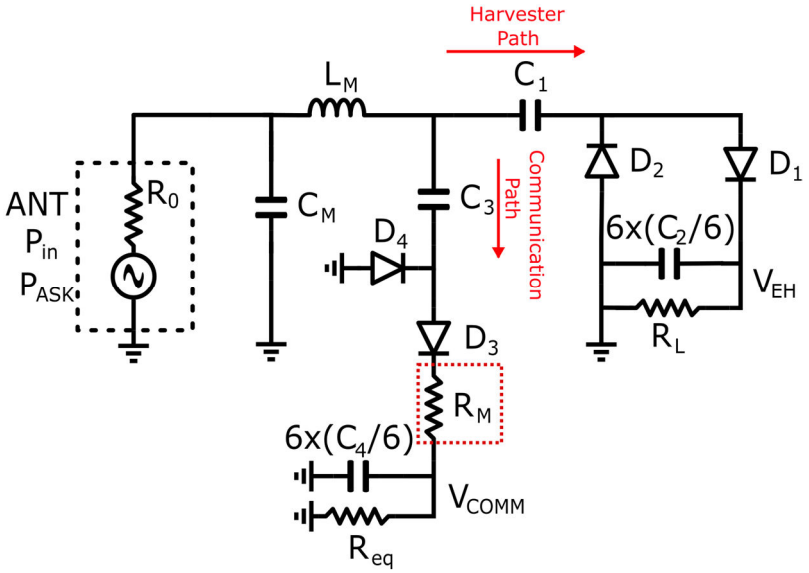


Figure 6.17 Proposed modified harvesting–communication interface circuit to improve isolation by adding R_M.

This modification effectively reduces the loading effect of the communication path on the harvesting rectifier, allowing the harvester path to maintain a high PCE for a wide range of R_{eq}. As a result, the strong dependency between communication loading and harvesting efficiency observed in the previous design is significantly mitigated.

The impact of this improvement is illustrated in **Figure 6.18**. Compared to the previous results (**Figure 6.16**), the PCE in **Figure 6.18**(b) remains nearly unchanged across different values of R_{eq}, confirming that the introduction of R_M successfully preserves the efficiency of the energy harvesting path.

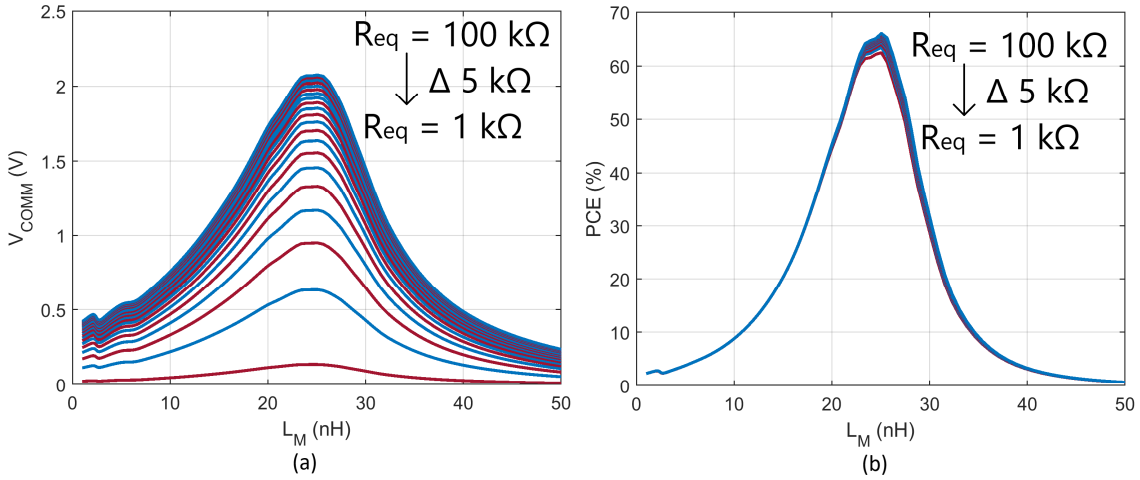


Figure 6.18 Simulations showing the impact of adding R_M while sweeping R_{eq} on: (a) V_{COMM}, and (b) PCE of harvesting path.

In addition, **Figure 6.18**(a) shows that V_{COMM} varies more smoothly with changes in R_{eq}. This contrasts with the nonlinear behavior observed in **Figure 6.16**(a) without the isolating resistor, where abrupt changes were caused by the strong nonlinear conduction of diode D_3. The presence of R_M effectively linearizes the current through D_3, resulting in a more gradual and predictable variation of V_{COMM}.

As for the component value of R_M, its selection must satisfy two key objectives. First, it should provide sufficient isolation between the harvester and communication paths such that variations in R_{eq} do not affect the PCE of the harvester. Second, it should reduce

V_{COMM} to an appropriate level, ideally to allow the envelope voltage to be centered within the ICMR of the differential amplifier.

Since the design procedure is closely tied to the time constants of the communication rectifier and ASK filtering stages, **Figure 6.17** is redrawn to include the more detailed ASK filter circuitry from Subsection 5.3.2, as shown in **Figure 6.19**. The time constants from (5.1)–(5.3) are re–mapped to the circuit parameters of **Figure 6.19** and rewritten as:

$$\tau_1 \approx C_3 (R_M + R_{eq}), \tag{6.3}$$

$$\tau_2 \approx C_4 R_{eq}, \tag{6.4}$$

$$\tau_3 \approx C_{CM} (R_{DIV} + R_2). \tag{6.5}$$

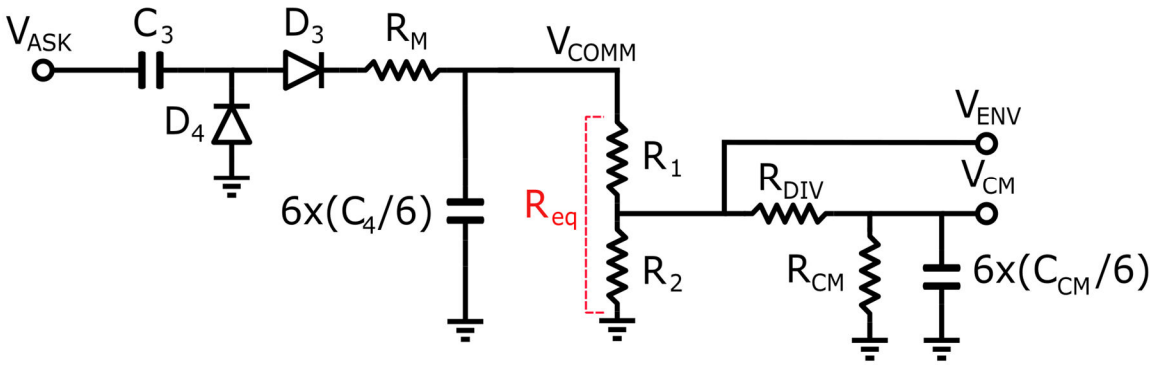


Figure 6.19 Communication rectifier included with the detailed ASK filter.

The design procedure begins by selecting R_{eq} to set the time constant τ_2 with C_4, with the objective of attenuating the carrier frequency, while allowing ASK modulation to pass (10– to 20–times smaller than the ASK modulation time constant). Next, R_2 is chosen to define τ_3 with C_{CM} and R_{DIV}, ensuring that τ_3 is approximately two orders of magnitude larger than τ_2 to generate the average of the envelope signal V_{CM} (equivalent to V_{avg} in Chapters 4 and 5), as discussed in Subsection 5.3.2. The resistor R_1 is then obtained from $R_{eq} - R_2$.

Subsequently, R_M is gradually increased through simulation until the PCE of the harvester is maximized while ensuring that V_{ENV} remains centered within the ICMR of the differential amplifier. Finally, C_3 is selected to set τ_1 about 10– or 20–times larger than the ASK modulation time constant, allowing the ASK modulation to pass effectively to the output of the communication rectifier. It is important to note that C_3 still needs to be maintained larger than the intrinsic capacitances of D_3 and D_4 for proper de–coupling.

From the design procedure, R_{eq} is selected as 150 kΩ and C_4 as 6 pF, resulting in a time constant $\tau_2 = 900$ ns, which corresponds to a low–pass cutoff frequency of 176.84 kHz. This ensures sufficient attenuation of the 900 MHz RF carrier while allowing the 15 kHz ASK modulation to pass.

Next, R_2 is chosen as 75 kΩ, with $C_{CM} = 600$ pF and $R_{DIV} = 100$ kΩ (from the previous chapter), yielding a common–mode time constant of $\tau_3 = 105$ µs which is approximately two orders of magnitude larger than τ_2. Accordingly, R_1 is set to 75 kΩ.

From CAD simulations, selecting $R_M = 15$ kΩ results in $V_{COMM} \approx 2$ V and a good PCE isolation. After the voltage division by R_1 and R_2, the resulting envelope voltage is centered around 1 V, which is suitable for the ICMR of the differential amplifier operating at a 2 V supply.

The time constant τ_1 is chosen to be at 160 µs (≈ 1 kHz). Solving (6.3) yields $C_3 \approx$ 1000 pF.

Figure 6.20 presents the AC simulation results, confirming that the selected value of $C_3 = 1000$ pF enables effective transmission of the 15 kHz ASK signal while attenuating lower–frequency components. **Figure 6.21** illustrates the transient response for $C_3 = 10$ pF (a) and 1000 pF (b). As observed, the modulation is correctly recovered for the optimized capacitor value, in agreement with the predicted frequency response and prior calculations.

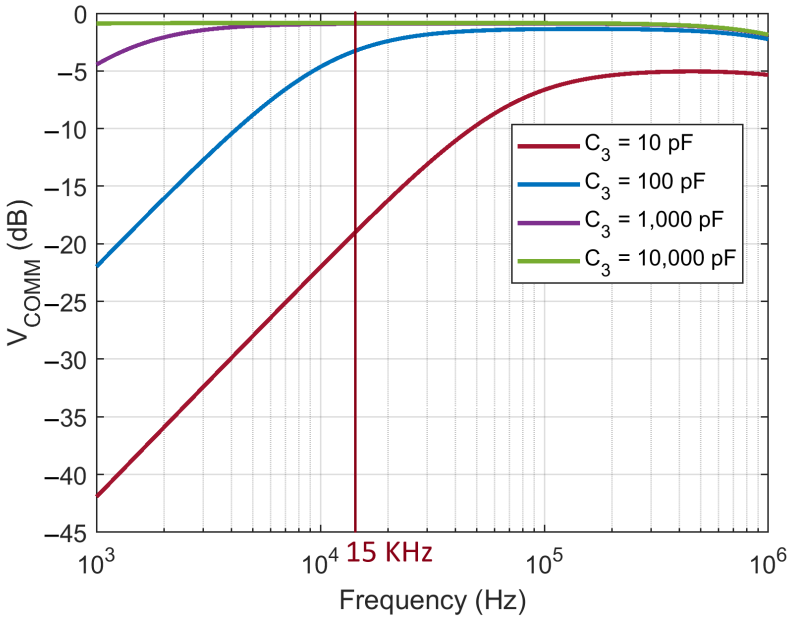


Figure 6.20 AC frequency response of the communication path for different values of C_3.

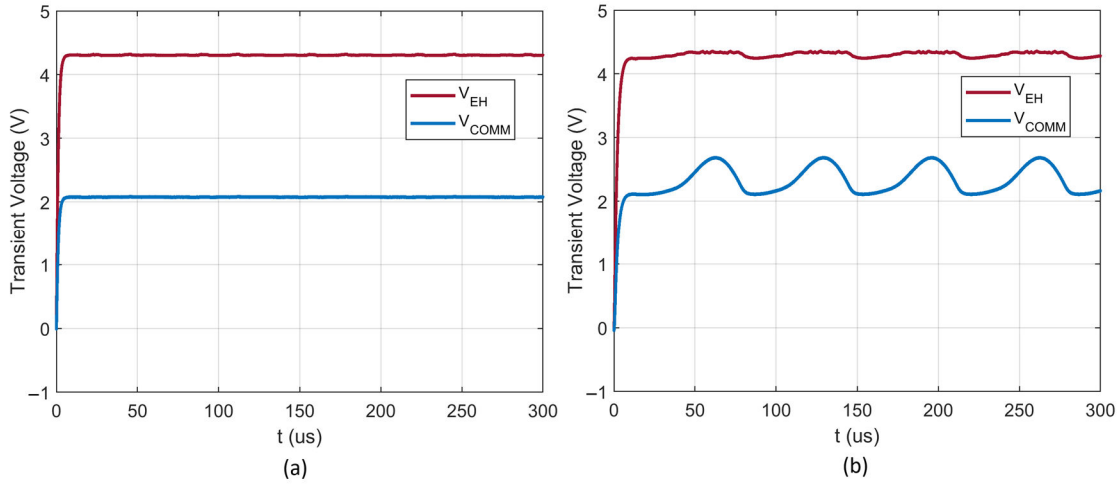


Figure 6.21 Transient response of the harvesting–communication interface circuit for: (a) C_3 =10 pF and (b) C_3=1000 pF.

The circuit shown in **Figure 6.17** is implemented as a PCB prototype, as depicted in **Figure 6.22**. The board is fabricated on an FR–4 substrate with a thickness of 0.6 mm, consistent with the previous prototypes to ensure comparable parasitic conditions.

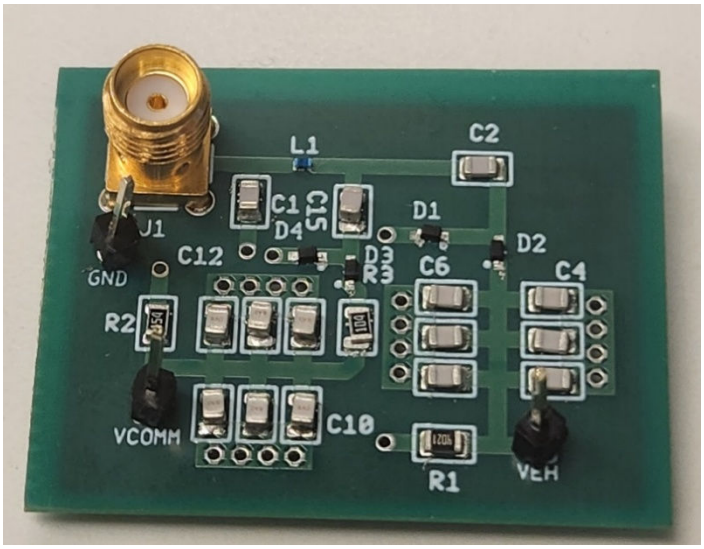


Figure 6.22 PCB prototype of the harvesting–communication interface circuit.

The PCB integrates both the energy harvesting and communication paths within a single layout. The RF input is applied through an SMA connector, followed by the impedance matching network, which consists of a 6.7 nH inductor and a 9 pF capacitor. To mitigate parasitic effects, the layout incorporates multiple parallel capacitors and short grounding paths, in accordance with the findings of Section 6.3. Test points are managed at key nodes, including V_{EH} and V_{COMM}, enabling convenient measurement and validation of both the harvested DC voltage and the communication signal performance.

Figure 6.23 presents the co–simulated (post–layout) and measured performance of the proposed circuit. **Figure 6.23**(a) shows V_{EH} and V_{COMM} as a function of the input power, while **Figure 6.23**(b) presents the harvesting PCE.

Following post–layout simulations, the value of R_M was increased from 15 kΩ (used in schematic design) to 100 kΩ to maintain performance comparable to the ideal case. This adjustment compensates for additional parasitic effects introduced by the layout.

From **Figure 6.23**(a), the measured V_{EH} reaches approximately 4 V at an input power of 10 dBm, compared to 4 V at 9 dBm in co–simulation. Similarly, the measured V_{COMM} is approximately 1.8 V at 10 dBm, whereas the co–simulated value is around 2.5 V. The discrepancy in voltage levels is primarily attributed to the sensitivity of R_M to diode variations. Since R_M linearizes the current through diode D_3, whose I–V characteristic

exhibits strong exponential dependence, small variations in diode parameters can lead to noticeable differences in the resulting voltage.

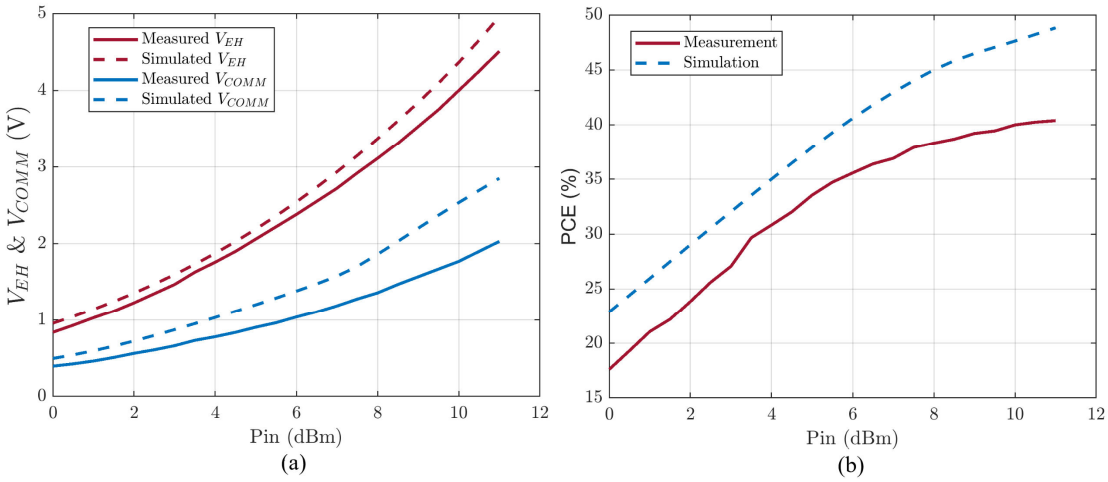


Figure 6.23 Co–simulated (dashed lines) and measured (solid lines) performance of the harvesting–communication interface PCB prototype showing: (a) V_{EH} (red) and V_{COMM} (blue) vs. P_{in}, and (b) PCE as a function of P_{in}.

Despite these variations, the achieved voltage levels remain suitable for the intended simultaneous harvesting and telemetry operation. The harvested voltage supports a 4 mW output power target, while the communication voltage remains within a usable range for the ICMR of the differential amplifier.

Figure 6.23(b) shows the PCE comparison. The ideal schematic design (**Figure 6.18**(b)) achieved a peak PCE of approximately 65% at 10 dBm. This value decreases to 47.5% in post–layout co–simulation due to substrate losses, parasitics, and interconnect effects. The measured PCE further reduces to approximately 40%, which is consistent with additional practical losses and component tolerances. Nevertheless, the agreement between co–simulation and measurement validates the effectiveness of the isolation resistor in maintaining a good PCE while adding flexibility in communication filter design.

Figure 6.24 shows the measured transient waveforms of V_{EH} and V_{COMM} at an input power of 10 dBm with an ASK modulation frequency of 15 kHz. As expected, V_{COMM} exhibits clear variations corresponding to the ASK modulation. The same ASK modulation

is observed in the measured waveform of V_{EH}, which is undesirable. However, despite these variations, the impact on system operation is minimal. In the subsequent stage, a voltage regulator is employed to provide a stable 2 V DC supply for the receiver circuitry, effectively suppressing any residual fluctuations in V_{EH}. Therefore, the observed behavior does not compromise the overall system performance.

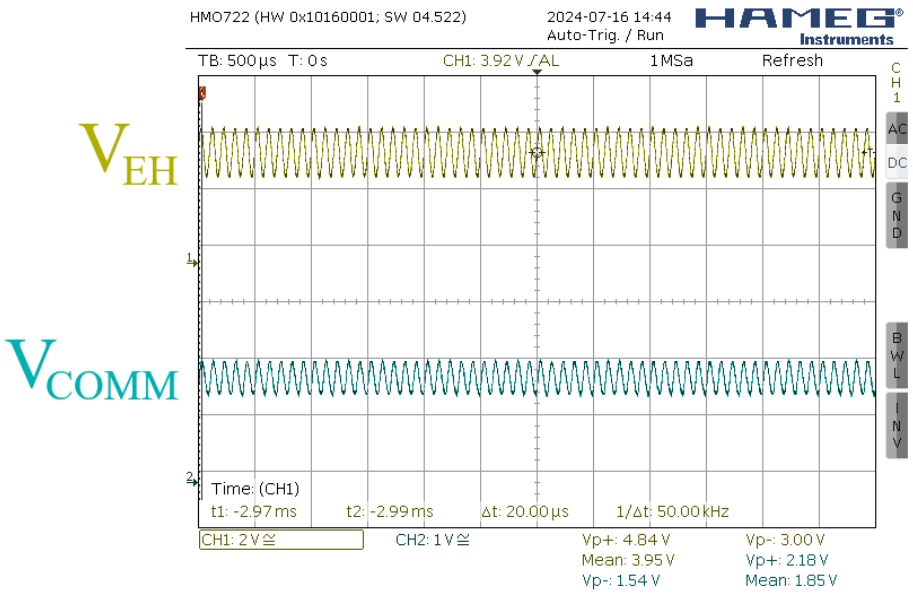


Figure 6.24 Transient response of the prototyped harvesting–communication interface PCB showing V_{EH} (yellow) and V_{COMM} (blue).

6.5 Wirelessly Powered ASK-PWM Receiver Experimental Work

With the PCB–related challenges addressed, specifically, reducing RF feedthrough into the harvesting path through capacitive segmentation to mitigate inductive parasitics, and isolating the communication path from the harvester using a lossy resistor to preserve PCE, the design is now ready for full front–end receiver implementation.

The complete system implementation of the wirelessly powered ASK–PWM receiver is shown in **Figure 6.25**. The circuit integrates the solutions developed in the two preceding sections and comprises four main blocks: the receiving antenna, the matching network, the energy harvesting path, and the communication path.

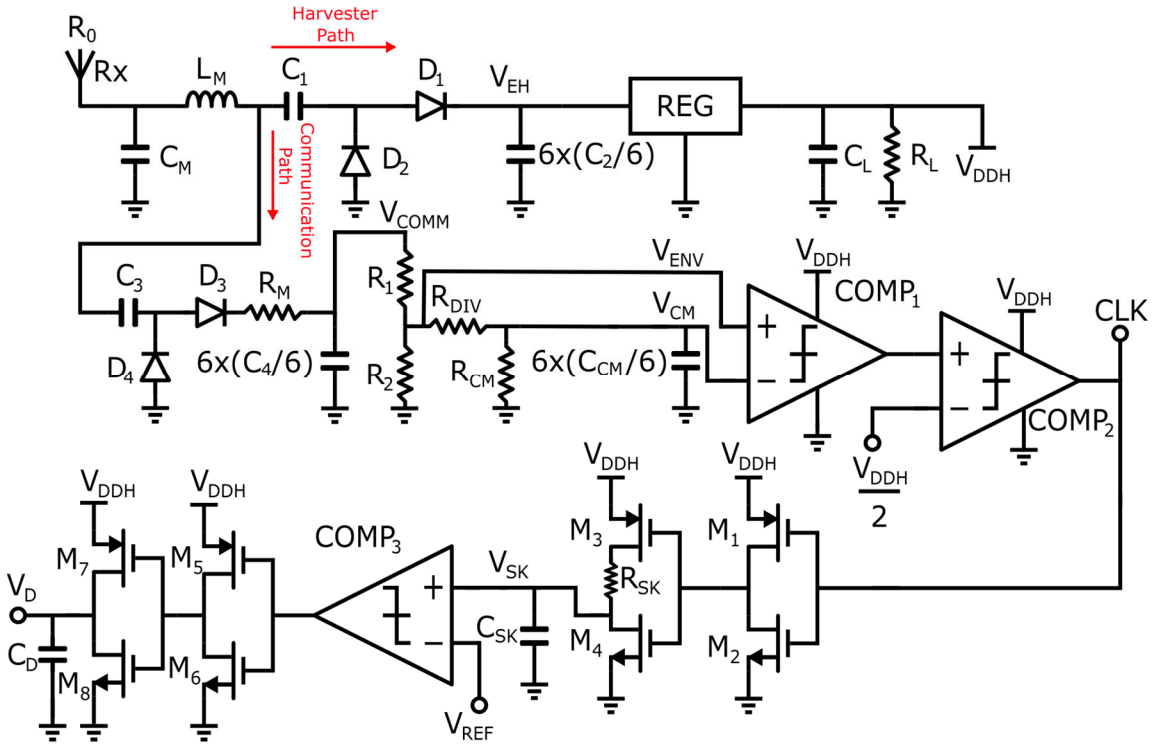


Figure 6.25 Circuit schematic of the proposed wirelessly powered ASK–PWM Receiver.

The receiving antenna captures both the RF power and the ASK–PWM modulated signal and is modeled by its source resistance R_0. The matching network is designed to provide impedance matching without disturbing the low–frequency ASK–PWM content.

The harvesting path consists of the voltage doubler designed in Section 6.3 followed by a voltage regulator (REG), load capacitor C_L, and load resistor R_L. The regulator provides a stable supply voltage originating from V_{EH}, isolating the downstream circuitry from variations in V_{EH} and from switching noise. This regulated voltage powers the load R_L as well as the comparators and inverters used in the receiver as was shown in **Figure 6.1** and **Figure 6.25**.

The communication path comprises an ASK–PWM demodulator and decoder. It includes the communication rectifier and ASK filter developed in Section 6.4. To complete the ASK–PWM receiver, as described in Subsection 5.3.2, the differential amplifier (realized here as a comparator $COMP_1$) and the RZ comparator ($COMP_2$), along with the PWM decoder, are incorporated. The decoder consists of an inverter (M_1, M_2), a skewing

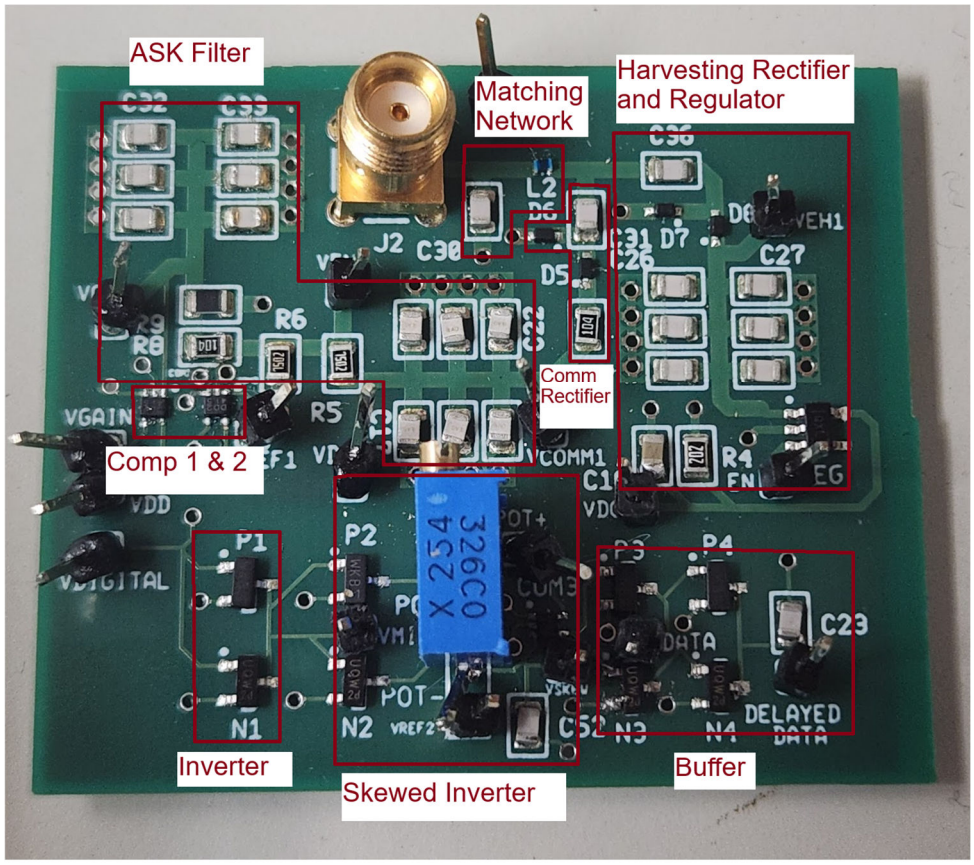
inverter (M_3, M_4, R_{SK}, C_{SK}), a comparator ($COMP_3$), and a CMOS buffer (M_5–M_8, C_D). R_{SK}, C_{SK}, and V_{SK} are equivalent to R_{skew}, C_{skew}, and V_{skew} in Chapters 4 and 5, while C_D represents the capacitive loading of the digital frame router.

The communication rectifier generates the signal V_{COMM}, which is subsequently processed by the ASK filter to produce V_{ENV} and the common–mode reference V_{CM}. The envelope is amplified by $COMP_1$ stage while V_{CM} serves as its bias. The output of $COMP_1$ is then converted to an RZ signal by $COMP_2$, using a $V_{DDH}/2$ reference to recover the clock signal CLK. Finally, the PWM decoder processes the recovered clock, following the design described in Subsection 5.3.2. The inverter pair first inverts CLK, after which the skewing inverter and $COMP_3$ detect the pulse–width difference between logic states. A narrow high pulse is decoded as bit "0," whereas a wide high pulse is decoded as bit "1." The output of $COMP_3$ is then buffered by the buffer stage, producing the recovered data signal V_D (equivalent to PRE_DATA in Chapters 4 and 5).

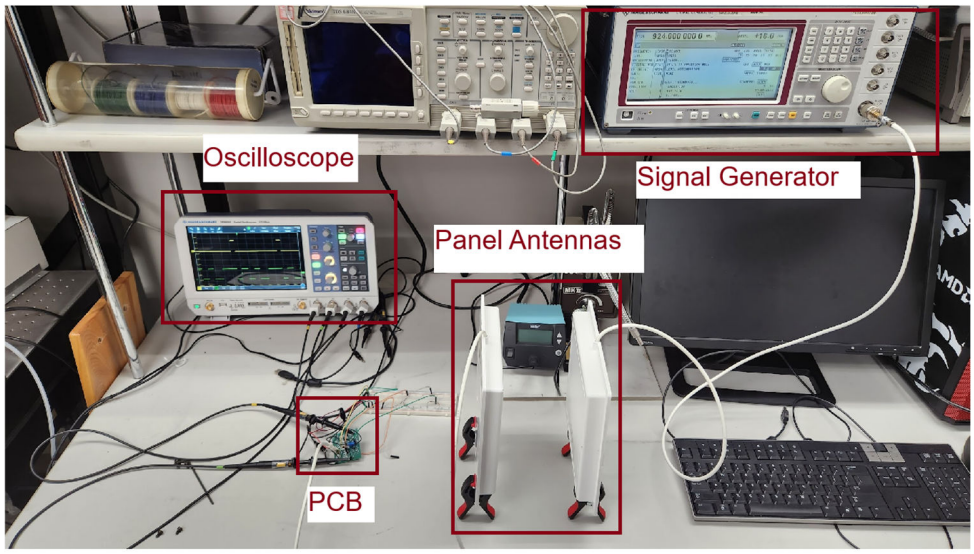
To validate the proposed system in a discrete implementation, the complete ASK–PWM receiver with WPT was realized on a two–layer FR–4 PCB with dimensions of 5 cm × 4 cm × 0.6 mm. The top layer contains all components and interconnects, while the bottom layer serves as a continuous ground plane. The fabricated PCB is shown in **Figure 6.26**(a), where the main circuit blocks are annotated.

The RF matching network employs a 5.2 nH inductor and a 9 pF capacitor. Voltage regulation is provided by the TLV70220PDBVR from Texas Instruments, which delivers a stable 2 V output while maintaining a low quiescent current of 35 µA and a $PSRR$ of 68 dB at 1 kHz. Stability is ensured using $C_L = 100$ nF in conjunction with the decomposed 600 pF C_2.

The communication and control circuitry employ the same comparators and transistors described in Subsection 5.3.5, which are suitable for 2 V, low–power, and moderate–speed operation. The combined power consumption of the ASK demodulator and PWM decoder is approximately 355 µW, representing only a fraction of the actual load. A potentiometer is used for R_{SK} to enable tuning of the skewing time constant, ensuring reliable bit discrimination under various manufacturing conditions.



(a)



(b)

Figure 6.26 Wirelessly powered ASK–PWM experimental work showing: (a) printed circuit, and (b) measurement setup.

The measurement setup is shown in **Figure 6.26**(b). An SME06 signal generator (Rohde & Schwarz) is used to generate a 924 MHz RF signal. Since direct ASK modulation is not supported, a digitally controlled attenuator is driven by a bit pattern to synthesize ASK–PWM modulation at a switching rate of 30 kHz. Bit "1" is represented by a 99 μs high pulse followed by a 33 μs low pulse, while bit "0" consists of a 33 μs high pulse followed by a 33 μs low pulse. The RF signal is transmitted and received using the same antennas in Subsection 5.3.1, with the receiving antenna connected to the PCB. The separation distance between antennas was set to 8 cm, with reliable operation observed between 6 cm and 12 cm.

The PCB includes multiple test points connected to an R&S RTB2004 oscilloscope for waveform observation. The system operates fully self–powered, with the regulator supplying all comparators and logic circuits. The regulator enable pin is connected to V_{EH}, requiring it to remain above 2 V for proper operation.

Figure 6.27 presents key measurement results. **Figure 6.27**(a) shows the harvested voltage V_{EH} and regulated voltage V_{DDH}. Under a repeating "100" bit pattern, V_{EH} varies between 2.9 V and 5.2 V, centered around 4.2 V, while remaining above the regulator threshold. The regulated output remains stable at 2 V, delivering 1 mA to the load, corresponding to a total system efficiency of 12.5%.

Figure 6.27(b) shows V_{COMM}, which is reduced by R_M to approximately 2.31 V, with variations between 1.32 V and 3 V. After division by R_1 and R_2, the envelope V_{ENV} ranges from 0.73 V to 1.5 V, remaining within the ICMR of $COMP_1$, as shown in **Figure 6.27**(c), alongside the reference V_{CM}. **Figure 6.27**(d) illustrates the skewing inverter output and reference used for pulse–width discrimination. **Figure 6.27**(e) confirms correct data recovery, where wide pulses are decoded as "1" and narrow pulses as "0", while the clock signal is simultaneously recovered from the envelope detection path.

Finally, **Figure 6.27**(f) evaluates system performance versus antenna separation distance. Three regions are observed: optimal operation near 8 cm, reduced performance beyond 12 cm due to insufficient V_{EH}, and complete failure beyond 18 cm as the regulator ceases operation. The system reliably delivers 1 mA within a range of 6–12 cm.

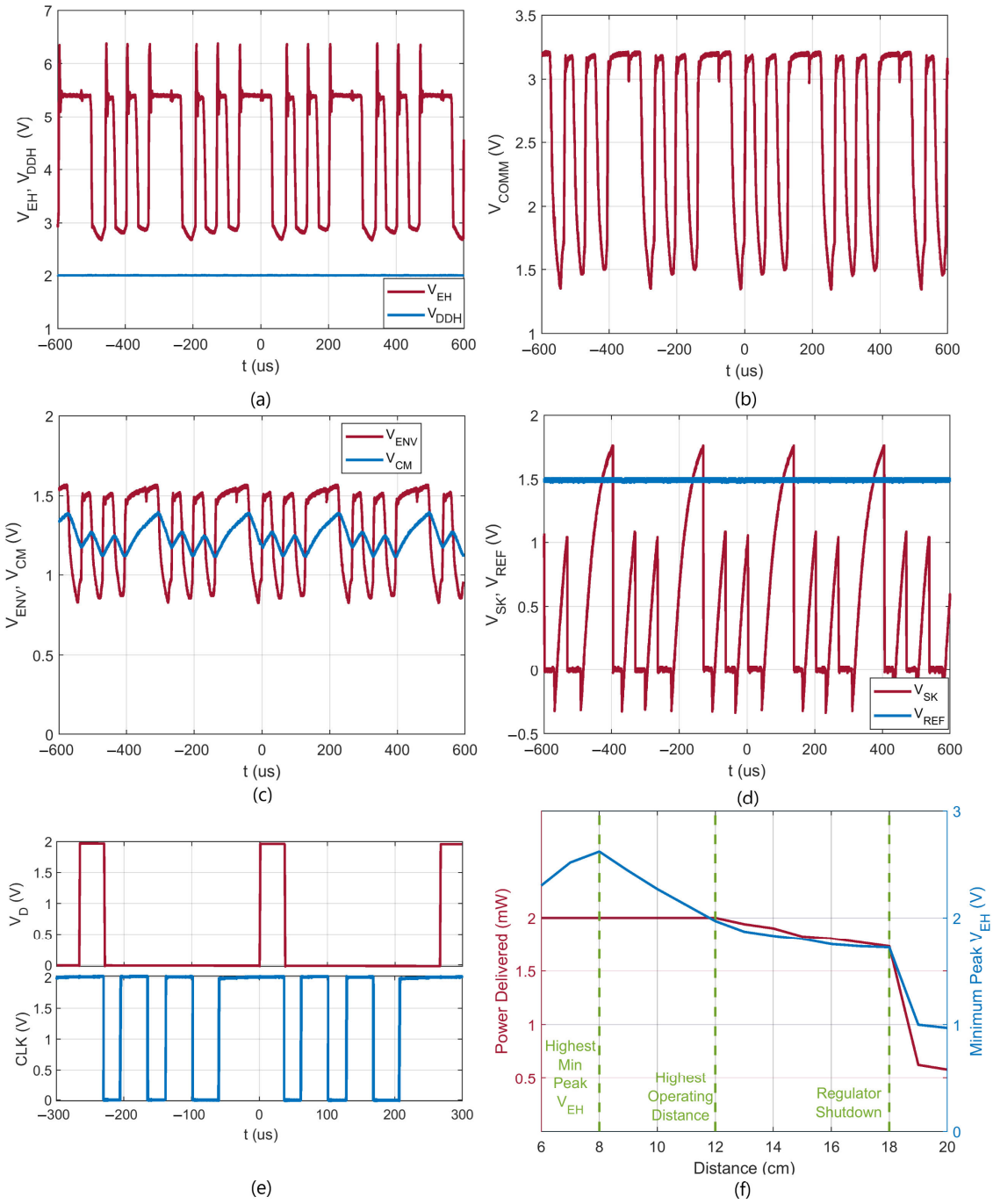


Figure 6.27 Waveform measurements obtained from oscilloscope showing: (a) V_{EH} (red) and V_{DDH} (blue), (b) V_{COMM}, (c) V_{ENV} (red) and V_{CM} (blue), (d) V_{SK} (red) and V_{REF} (blue), (e) V_D (red) and CLK (blue), and (f) measured distance validation.

Based on the literature review in Section 2.3, a comparison between this work and prior works is presented in **Table 6.1**. This work is the only implementation of an ASK–PWM harvesting system realized on an FR–4 substrate using exclusively discrete components. In addition, it achieves the largest reported separation distance, reaching up to 12 cm.

Table 6.1 Comparison between conducted work and literature on wirelessly powered ASK–PWM receiver (*: receiver efficiency with regulator included).

Reference	Harvesting Frequency	Bitrate	*PCE*	Power Consumption	Separation Distance	Harvesting Technology	Manufacturing Technology
This Work	924 MHz	15 kbps	42.12% (12.5%)*	355 µW	6–12 cm	Radiative Field	FR–4 PCB
[21]	1.86 GHz	25 Mbps	55%	7 µW	5 cm	Radiative Field	65 nm
[22]	1.32 GHz	20 Mbps	N/A	11 µW	3.5 cm	Radiative Field	65 nm
[69]	13.56 MHz	75 bps	N/A	800 µW	N/A	N/A	Hybrid CMOS
[70]	13.56 MHz	88.3 kbps	N/A	4.5 µW	2 mm	Inductive Coupling	180 nm SoC
[71]	N/A	N/A	N/A	50 mW	N/A	Inductive Coupling	180 nm BCD
[72]	N/A	2 Mbps	N/A	129 µW	N/A	Inductive Coupling	180 nm
[74]	900 MHz	10 Mbps	N/A	N/A	1 cm	Inductive Coupling	65 nm
[75]	40.68 MHz	10 kbps	55%	27 µW	80 mm	Inductive Coupling	180 nm

The experimental results of the wirelessly powered ASK–PWM receiver confirm the feasibility of integrating WPT with an ASK–PWM demodulator and decoder for distributed beam–steering systems, thereby eliminating the need for wired power while maintaining a simple discrete–component implementation. This is enabled by the combined use of capacitor segmentation to mitigate parasitic effects and effective isolation between the communication and harvesting paths, enabling full receiver realization on a PCB using discrete components and supporting initial phase design and validation.

6.6 Conclusion

This chapter presented the design, implementation, and experimental validation of a wirelessly powered ASK–PWM receiver, extending the digital control system presented in the previous chapter by eliminating the need for external power supplies through the integration of WPT. By co–designing the energy harvesting and communication paths, key challenges associated with PCB parasitics and path interaction were addressed, enabling efficient power delivery alongside robust data recovery.

Specifically, the impact of PCB–induced parasitic inductance on the rectifier output filter was analyzed, revealing a degradation in RF rejection and the emergence of unwanted RF feedthrough. To address this, a capacitor segmentation technique was introduced, where the output capacitance was distributed across multiple parallel branches to reduce the effective parasitic inductance. This approach significantly improved RF suppression and restored the desired behavior, which was validated through both simulation and measurement.

Next, the interaction between the harvesting and communication paths was investigated, highlighting a fundamental trade–off between PCE, communication rectifier voltage level, and time constants design flexibility. To overcome this limitation, a resistive isolation strategy was proposed, introducing a series resistor in the communication path to decouple the two branches. This modification preserved the PCE of the harvesting path while maintaining the envelope signal within the required operating range of the receiver and enabling flexible tuning of the communication path time constants.

The proposed wirelessly powered ASK–PWM receiver was realized as a discrete FR–4 PCB prototype and experimentally validated. Measurements demonstrated a harvested voltage centered around 4.2 V, while maintaining a regulated 2 V supply capable of delivering 1 mA to the load. A peak PCE of approximately 40% was achieved for the harvesting path, with reliable ASK–PWM data recovery at a bitrate of 15 kbps. The system operated successfully over a wireless distance of 6–12 cm, supporting initial phase design and validation for wirelessly powered distributed beam–steering systems.

Looking back at Chapter 5, the effectiveness of beam–steering control using ASK–PWM demodulation and decoding was demonstrated through a synthesized implementation of the digital frame router. With the successful realization of a wirelessly powered ASK–PWM receiver in this chapter, the next step is to integrate these functionalities, along with the DACs, into a unified IC. Accordingly, in the next chapter, these building blocks will be combined into a fully integrated circuit implementation, enabling a compact, scalable, and fully wireless solution for distributed beam–steering control.

Chapter 7: Integrated Circuit Implementation of the Control Block

As the system evolves from a discrete PCB prototype toward a scalable beamforming architecture, the transition to an IC implementation becomes a necessary step rather than an optional improvement. While the PCB implementation presented in the previous chapter successfully demonstrated the feasibility of simultaneous WPT and ASK–PWM–based communication, it inherently suffers from limitations in size, parasitic effects, and scalability. These limitations become increasingly critical when targeting large–scale phased–array systems, where a high density of control nodes must be deployed in a compact and power–efficient manner.

As discussed in Chapter 4, the proposed architecture distributes control across compact IC–based nodes, each responsible for a 1×4 sub–array control. By leveraging non–coherent ASK–PWM signaling, conventional wired interfaces such as SPI are eliminated, thereby reducing interconnect complexity, routing congestion, and synchronization overhead. In addition, WPT removes the need for batteries, on–module power routing, and dedicated supply feeding pins. Consequently, each IC operates under a single–input paradigm, where power, clock, and data are simultaneously delivered through a single pad. This represents a fundamental shift from traditional control architectures and is particularly well suited for large–scale, distributed beamforming systems.

The single–input architecture is a key enabler for IC–level integration, as it significantly reduces interconnect density and simplifies system–level design. Furthermore, integrating the RF rectifier, power management circuitry, communication blocks, and digital frame routing on–chip provides several important advantages, including improved power efficiency through subblock–level optimization, reduced interconnect losses, and minimized parasitic effects compared to discrete implementations. This high level of integration also enables a substantial reduction in overall system footprint, while facilitating scalable deployment to large–scale arrays.

This chapter presents the design, implementation, and experimental validation of the proposed control IC fabricated in a 130 nm CMOS on silicon substrate technology. The IC integrates all key building blocks required for wireless control, including the RF rectifier,

bandgap references, voltage regulators, ASK demodulator, PWM decoder, digital frame router, and DACs. To facilitate first–pass silicon validation and debugging, a modular design approach is adopted, allowing individual subsystems to be tested independently.

The chapter begins with the definition of system–level specifications and design constraints, followed by detailed descriptions of the RF rectifier and power conditioning circuitry. The communication blocks, including the ASK demodulator and PWM decoder, are then presented, along with the digital frame router and DAC architecture. Post–layout simulation results are provided to verify control block functionality. Finally, measurement results from the fabricated IC are discussed, highlighting both successful operation of key subsystems and important limitations observed in silicon, which provide valuable insights for future design iterations.

7.1 IC Specifications

To guide the circuit design of the control IC, several key specifications must be established, driven by both system–level requirements and the constraints imposed by WPT operation.

The system requirements impose a single–input pad per IC, through which power, clock, and data are simultaneously delivered in order to minimize routing complexity and feeding pin overhead. This is achieved by combining WPT with ASK–PWM signaling. In addition, one output pin is required per beam–steering control path, which is realized using on–chip DACs. It should be noted that both the DAC resolution and the number of DAC channels differ from those presented in Subsection 4.2.3. In the previous implementation, the resolution was limited to 4 bits due to the GPIO constraints of the DE2–115 platform; in this work, it is increased to 6 bits to enable finer control. Furthermore, the number of DACs is expanded from four to eight to support RF attenuators for sidelobe tapering. These modifications are introduced to enhance flexibility and establish a more general–purpose IC architecture suitable for a wider range of beamforming applications. Additionally, to enable integration with a compact miniaturized antenna, the harvesting frequency selected in the previous chapter is increased from 900 MHz to 2.4 GHz.

As for the per–IC specifications, power consumption is the most critical design constraint, as the IC is entirely powered through wireless energy harvesting. The available power is limited; therefore, both static and dynamic power consumption must be minimized. Based on the initial IC schematic design, the total current consumption of the control IC is expected not to exceed 1 mA, which is used as a reference for estimating the overall system power budget.

To guide circuit–level design under this constraint, it is useful to consider the dominant contributors to power consumption. In digital circuits, power is primarily dominated by switching activity, resulting in dynamic power consumption given by:

$$P_{\text{dyn}} = C_L V_{DDL}^2 f, \tag{7.1}$$

where f is the frequency.

From this relation, it is evident that reducing the supply voltage has the most significant impact due to its quadratic dependence. Therefore, the digital circuitry is designed to operate at a low supply voltage of $V_{DDL} = 0.75$ V. The selected supply voltage also provides sufficient overdrive relative to the threshold voltages of the CMOS devices (on the order of 0.3 V), ensuring reliable switching while maintaining low power operation. However, operating at such low voltage introduces challenges in terms of noise margins, process variations, and maximum operating speed.

In addition to voltage scaling, the operating data rate also directly impacts dynamic power consumption. Based on initial system–level simulations, a data rate of 100 kbps was selected as a suitable trade–off, providing reliable communication while maintaining low dynamic power consumption within the constraints of WPT operation.

As for static power consumption, it is minimized by biasing most analog building blocks such as comparators, operational amplifiers, and reference circuits, in the weak inversion (subthreshold) region. While this approach significantly reduces DC current consumption, it introduces trade–offs in bandwidth and noise performance that must be carefully managed.

The next issue is the dual–supply requirement and voltage domain translations. A key challenge in this design is the coexistence of two voltage domains: a low–voltage domain $V_{DDL} = 0.75\,\text{V}$ for digital logic, and a high–voltage domain $V_{DDH} = 2.6\,\text{V}$ for analog DAC outputs.

The higher voltage domain was initially selected to interface with commercial phase shifters capable of achieving up to $200°$ phase shift using 2 V control range. However, due to component obsolescence and cost constraints, the system transitioned to in–house designed reflective phase shifters requiring a $10\,\text{V}$ control range with approximately $155°$ phase shift, as was presented in Subsection 5.3.3. In this chapter, the IC is designed assuming a $2.6\,\text{V}$ DAC output range, while the extension to $10\,\text{V}$ control using amplification stages is addressed in the following chapter.

The level translation between the 0.75 V digital domain and the 2.6 V analog domain presents a non–trivial design challenge. Conventional level shifters either consume excessive power or suffer from reliability issues at ultra–low voltages. To address this, a low–power slewed comparator–based approach is introduced within the DAC architecture, enabling efficient and reliable voltage domain interfacing without significantly increasing power consumption. In addition, the slewing behavior inherently limits the charging and discharging currents at the output, thereby reducing the dynamic power consumption of the DAC.

Furthermore, since the IC is powered through WPT, the on–chip RF rectifier must generate both voltage domains from the received RF signal. In particular, it must efficiently convert RF power into DC, provide a sufficiently high output voltage, and maintain high PCE under low input power conditions. Due to the requirement of a regulated $V_{DDH} \approx 2.6\,\text{V}$, as well as voltage drops, modulation–induced variations from ASK–PWM signaling, and necessary design margins, the rectifier is required to generate at least 4 V at its output. This requirement tightly couples the rectifier design with the overall system power budget and dictates the need for highly efficient rectification and power management circuits.

Finally, the IC area must be minimized to enable dense integration of multiple control ICs on a single PCB. Since each IC controls only a 1x4 sub–array, a large number of ICs

are required for practical beamforming systems. Area constraints impact several design choices, including minimizing passive component sizes, reducing capacitor usage where possible, and simplifying circuit topologies. However, certain passive elements remain unavoidable, particularly in power management and analog signal conditioning blocks, requiring careful trade–offs between area and performance.

7.2 RF Rectifier and Power Conditioning

In this section, the design methodologies and trade–offs associated with the RF rectifier and power conditioning circuitry are presented. These blocks form the front–end of the IC and are critical to enabling fully wireless harvesting operation, as they are responsible for converting the received RF energy into stable DC supplies and reference signals required by the rest of the system.

As was shown in **Figure 4.3** (Subsection 4.2.1) and discussed in Subsubsection 3.2.3.3, the RF rectifier must be carefully impedance–matched to the harvesting antenna to maximize PCE. Given the limited available input power in WPT systems (typically in the range of -10 dBm to 0 dBm at the receiver), even small impedance mismatches can significantly degrade the harvested power. Therefore, the design of rectifier input impedance network is essential to achieve high PCE.

From a system perspective, the rectifier is required to generate a DC output voltage of at least 4 V. This requirement arises from several constraints, which are the need to reliably regulate a high supply voltage of $V_{DDH} \approx 2.6\,\text{V}$, take into account the voltage drops across regulation stages, and allow for amplitude variations introduced by the ASK–PWM modulation scheme. Ensuring sufficient voltage headroom is therefore critical for stable operation under varying input power conditions.

The generated DC voltage is then processed by the power conditioning circuitry to produce two regulated supply domains: a high–voltage rail ($V_{DDH} = 2.6\,\text{V}$) used by the DACs and analog interface blocks, and a low–voltage rail ($V_{DDL} = 0.75\,\text{V}$) used by the digital control logic to minimize dynamic power consumption.

In addition to voltage regulation, the power conditioning block is responsible for generating stable reference voltages required by key analog components, including comparators, operational amplifiers, and DACs. These references must exhibit low sensitivity to supply variations and process mismatches, despite operating under tight power constraints.

Another important function of this front–end is to provide a signal path for communication. Since the same RF signal carries both power and ASK–PWM modulated data, the rectifier input must be appropriately interfaced with the demodulation and decoding circuitry. This requires careful design to ensure that the envelope variations used for data transmission are preserved and can be reliably extracted, while still maintaining stable DC supply generation.

7.2.1 RF rectifier design

The RF rectifier consists of an input matching network (L_M), diode–connected transistors (M_1, and M_2), and rectification capacitors (C_1, and C_2). A voltage doubler topology, shown in **Figure 7.1**, is adopted due to its ability to generate higher DC output voltages under low input power conditions, consistent with the RF rectifier designed in the previous chapter.

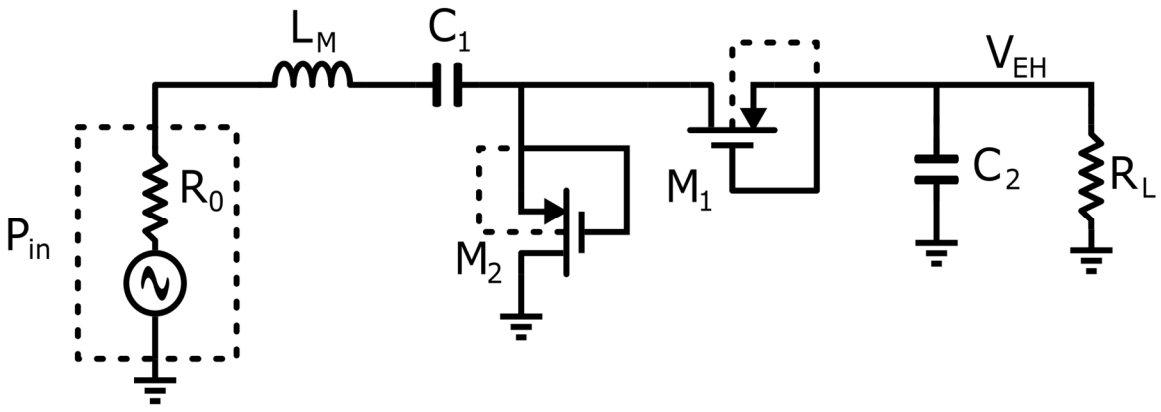


Figure 7.1 Circuit schematic of the voltage doubler using diode–connected transistors.

A key component of the design is the input resonating inductor L_M, which serves two critical roles. First, it provides impedance matching between the antenna and the rectifier to maximize power transfer. Second, it forms a series resonance with the effective capacitance at the input node, resulting in voltage amplification at the input of the voltage doubler. This resonant voltage boosting is particularly important, as it enables the diode–connected P–doped Metal–Oxide–Semiconductor (PMOS) device to turn on even at low input power levels, thereby improving sensitivity and overall PCE, as was discussed in Section 6.2. The value of the resonating inductor directly impacts the resonance condition and thus determines the input power level at which peak efficiency occurs.

The choice of PMOS over NMOS for the diode–connected devices is driven by process considerations. The utilized technology is based on a p–type silicon substrate, which is grounded to ensure proper reverse biasing of parasitic junctions. Using NMOS devices in this configuration would introduce body effect due to the voltage difference between the source and substrate, degrading efficiency and sensitivity. However, deep n–well option for RF transistors for PMOS are capable of mitigating this issue. As a result, PMOS devices allow the body (n–well) to be tied directly to the source, effectively eliminating body effect and improving rectifier performance. To ensure proper operation and isolation, the n–well is robustly connected to the source using heavily n–doped (n^+) guard rings, while adjacent devices are isolated using heavily p–doped (p^+) guard rings tied to ground.

The design of the RF rectifier is inherently challenging due to the nonlinear behavior of the diode–connected transistors and the wide range of input power levels. For higher input power operation, larger transistor widths are required to deliver sufficient current to the load. This results in increased parasitic capacitances, which, in turn, necessitates smaller resonating inductances to maintain the desired resonance frequency. Additionally, higher load currents imply lower optimal load resistance values for maximum power transfer.

Conversely, for low input power operation, smaller transistor sizes, larger inductances, and higher load resistances are preferred to improve PCE and sensitivity. Therefore, the selection of transistor width, resonating inductance, and load resistance is tightly coupled

and must be co–optimized to achieve high PCE at the desired input power level. This trade−off ultimately determines the operating point and efficiency profile of the rectifier.

It is necessary to first determine the required DC output voltage V_{EH} and the required load current I_L. As will be detailed later in this chapter, the power conditioning circuitry is capable of generating a regulated high supply of $V_{DDH} = 2.6\,\mathrm{V}$, provided that its input supply is at least 3 V. Consequently, the RF rectifier must deliver a minimum DC output voltage of 3 V to ensure proper regulation.

However, due to the use of ASK–PWM modulation for simultaneous power and data transfer, the rectified voltage is subject to envelope variations. To guarantee reliable operation under modulation, additional voltage headroom is required. A target DC output voltage of approximately 4 V is therefore selected, which provides sufficient margin to accommodate amplitude variations while ensuring that the regulator input remains above its minimum required voltage.

In terms of load current I_L, the overall system consumption is estimated to be less than 1 mA based on initial schematic work. Based on this requirement, an initial estimate of the load resistance R_L can be obtained using:

$$R_L = \frac{V_{EH}}{I_L}. \tag{7.2}$$

Substituting $V_{EH} = 4\,\mathrm{V}$ and $I_L = 1\,\mathrm{mA}$ yields an estimated $R_L = 4\,\mathrm{k\Omega}$. However, this value will be reduced after DC–to–DC conversion, which lowers the harvested voltage and results in an effective load resistance of 2 kΩ.

The output capacitance C_2 must be chosen to balance ripple suppression and transient performance. A sufficiently large capacitance increases the output time constant, reducing voltage ripple due to rectification and providing the instantaneous current required by switching circuits. However, excessively large capacitance increases area and slows transient response. Therefore, C_2 is selected based on transient simulations to ensure stable DC output under dynamic loading conditions.

To systematically design the rectifier, a design methodology based on Periodic Steady–State (PSS) simulations in Cadence Virtuoso is adopted:

1. Determine the required I_L and V_{EH} based on system specifications and estimate the load resistance R_L using (7.2).
2. Select an input power P_{in} assuming a PCE of approximately 50% to establish a starting design point.
3. Perform a sweep of the resonating inductance L_M while parametrically sweeping the transistor width W, ensuring resonance at the target operating frequency.
4. Identify the optimal combination of L_M and W that maximizes PCE at the chosen input power level.
5. Verify the achieved DC output voltage; if the required voltage level is not met, increase the rectifier order (e.g., add an additional voltage doubler stage) and repeat the design process until the desired output voltage is achieved.

This design methodology was applied to the rectifier operating at 2.4 GHz with a load resistance of 4 kΩ. **Figure 7.2** illustrates the PCE as a function of the matching inductance L_M for different transistor widths W, ranging from $20\,\mu$m to $200\,\mu$m. Based on the methodology outlined previously, where the input power is selected assuming an initial PCE of 50%, an input power of approximately 9 dBm was chosen to meet the target of delivering around 4 mW of DC power.

An important trend is observed: as the transistor width increases, the peak PCE shifts toward lower inductance values. This behavior is attributed to the increased parasitic capacitance associated with larger device widths, which necessitates smaller inductance values to maintain resonance at the operating frequency. Conversely, smaller transistor widths exhibit peak efficiency at larger inductance values. The maximum peak PCE is achieved at $L_M = 12.5$ nH and $W = 160\,\mu$m, corresponding to proper input impedance matching while simultaneously satisfying the output load matching condition.

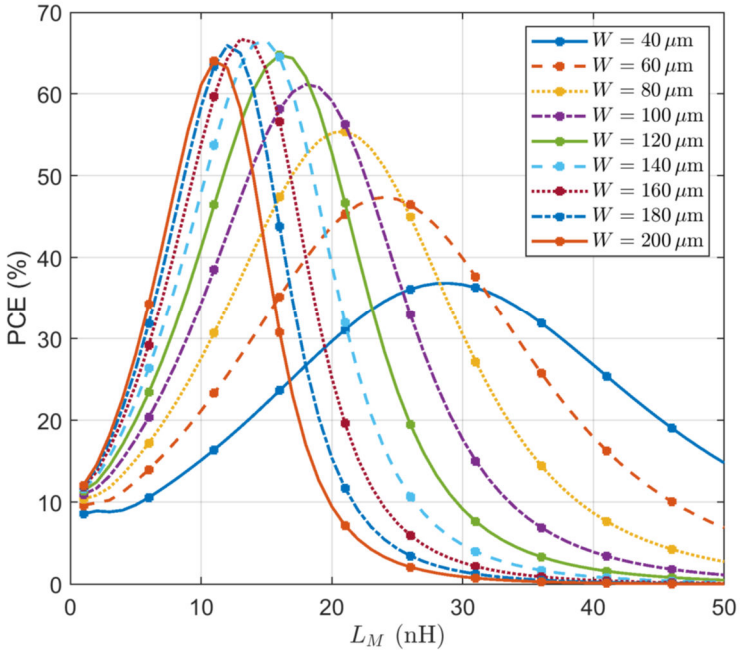


Figure 7.2 Simulated *PCE* vs. L_M for various transistor widths *W*.

Figure 7.3 presents the simulation results of the designed RF rectifier. The results correspond to the design using $L_M = 12.5$ nH, transistor finger width $W_f = 8\,\mu$m, number of fingers $= 20$ (resulting in a total width $W = 160\,\mu$m), $C_1 = 10$ pF, $C_2 = 100$ pF, $R_0 = 50\,\Omega$, and $R_L = 4$ kΩ.

As observed, the PCE initially increases with input power, reaching a peak value of approximately 69%, before gradually decreasing at higher input levels due to device breakdown. Meanwhile, the output voltage V_{EH} increases monotonically with input power as more RF energy is converted into DC.

A key observation from this plot is that the rectifier achieves an output voltage slightly above 4 V at an input power of approximately 8.2 dBm. This is lower than the 9 dBm estimated using the presented design methodology. The difference arises from the conservative assumption of 50% PCE used during the design phase. In simulation, the rectifier exhibits a higher efficiency of about 65%, allowing the required DC output power and voltage to be achieved at a reduced input power level.

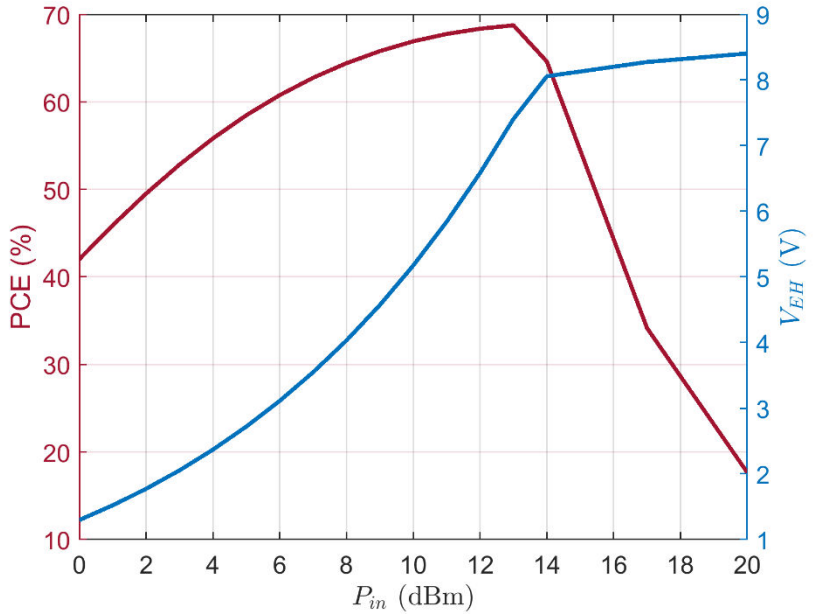


Figure 7.3 Schematic simulations of the designed diode–connected RF rectifier showing *PCE* (red) and V_{EH} (blue) as functions of input power P_{in}.

The implementation of passive components on–chip has a significant impact on both the PCE and the quality of the rectification process. In particular, large integrated capacitors exhibit reduced self–resonant frequencies (SRFs), which limits their effective use at RF frequencies such as 2.4 GHz. At the same time, sufficiently large capacitance values are required at the rectifier output to suppress voltage ripple and ensure stable DC operation.

Figure 7.4 presents post–layout simulations of Metal–Insulator–Metal (MIM) capacitors with values of 10 pF, 50 pF, and 100 pF, across frequency. As observed, the 10 pF capacitor maintains its nominal capacitance up to higher frequencies (approximately 20–30 GHz), making it suitable for input matching and resonance tuning of the RF rectifier. In contrast, the 50 pF and 100 pF capacitors begin to deviate significantly from their nominal values around 1 GHz due to parasitic effects, indicating that they are not suitable for direct use in RF signal paths or resonance networks.

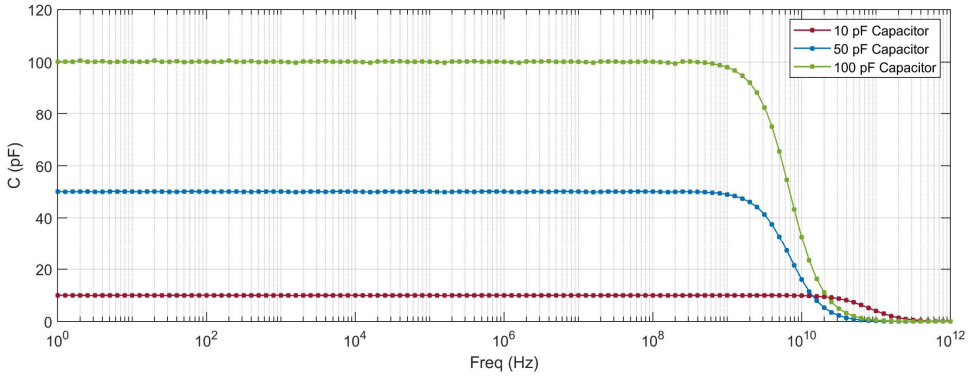


Figure 7.4 Post–layout simulations of MIM capacitors vs. frequency for different capacitance values.

However, at the rectifier output, the circuit behaves as a low–pass network, effectively attenuating high–frequency RF components. As a result, large capacitors at this node primarily operate under near–DC conditions and act as effective charge storage elements, despite their degraded high–frequency characteristics. This mitigates the impact of their limited SRF on overall rectifier performance.

Based on this trade–off, both 50 pF and 100 pF capacitors were evaluated. The 50 pF capacitor was ultimately selected for the load rectification stage, as it provides sufficient ripple reduction while occupying less silicon area compared to the 100 pF option, achieving a balanced compromise between performance and integration cost.

While large on–chip MIM capacitors exhibit Q degradation at high frequencies, the performance of on–chip inductors is even more severely limited and therefore requires careful consideration. **Figure 7.5** illustrates the operating regions of the RF rectifier as a function of the inductor's Q and the input power P_{in}, for a load resistance of 4 kΩ. The plot is divided into two regions based on the rectified output voltage V_{EH}: the red region corresponds to $V_{EH} < 4\,\mathrm{V}$, where the system cannot reliably sustain regulation and amplitude modulation, while the blue region represents $V_{EH} \geq 4\,\mathrm{V}$, indicating successful energy harvesting sufficient for downstream circuitry. The black curve denotes the boundary corresponding to $V_{EH} = 4\,\mathrm{V}$, effectively defining the minimum required input power for a given inductor quality factor.

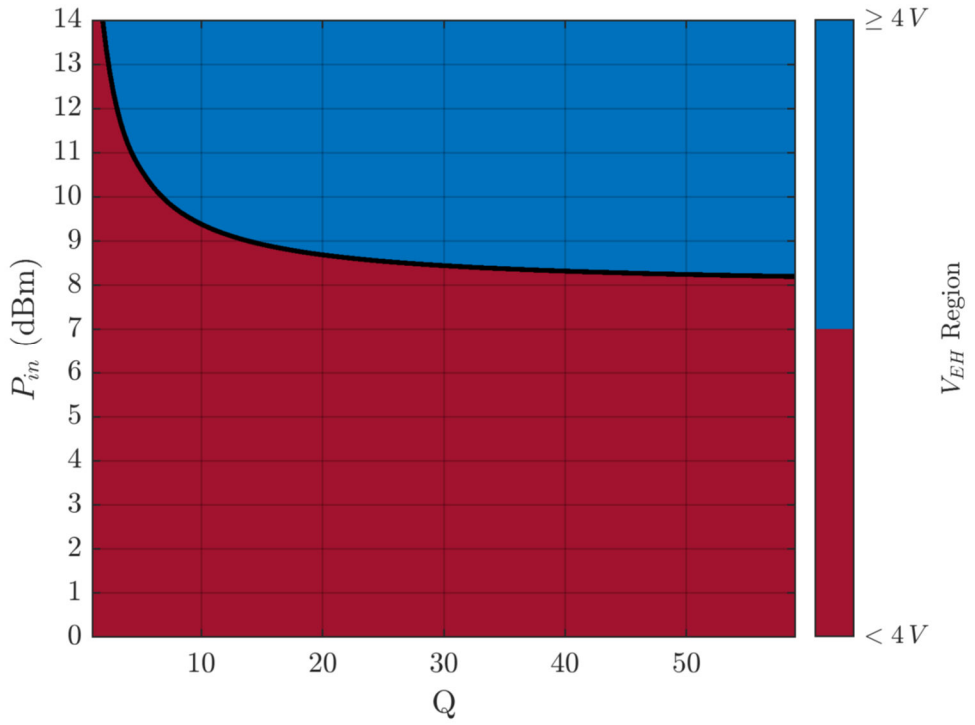


Figure 7.5 Impact of inductor's finite on–chip Q on PCE of RF rectifier.

Several important observations can be made from this figure. First, for high–quality inductors ($Q > 50$), which are typically achievable using off–chip components, the required input power to reach the target output voltage is approximately 8.2 dBm as was discussed. This represents the ideal operating scenario, where minimal losses in the matching network allow efficient RF–to–DC conversion.

However, as the inductor quality factor decreases, the required input power increases to recover the specified minimum harvested voltage. In practical IC implementations, on–chip inductors suffer from limited quality factors due to substrate losses, metal resistance, and parasitic effects. For inductance values above approximately 8 nH, the achievable Q is typically constrained to the range of 10–12. In this regime, the plot shows that the required input power shifts to approximately above 9 dBm to achieve the same 4 V output level.

This trend highlights the significant impact of inductor losses on rectifier performance. Lower Q values reduce the rectified output voltage, thereby degrading the overall PCE, which requires an increase in the necessary input power. Consequently, when accounting

for realistic on−chip inductor performance, as well as additional layout parasitics and losses in the energy harvesting path, the required input power is expected to increase further, reaching approximately 10 dBm.

Next, the layout−level implementation of the RF rectifier was simulated to evaluate the impact of parasitics and packaging effects. As expected, a noticeable degradation in performance was encountered compared to the schematic–level design. As a result, the matching network has been refined. The modified post–layout performance of the RF rectifier is shown in **Figure 7.6**. As shown in **Figure 7.6**(a), the required input power to achieve the target output voltage of 4 V increases to approximately 11.5 dBm, compared to the 8.2 dBm simulated at the schematic level.

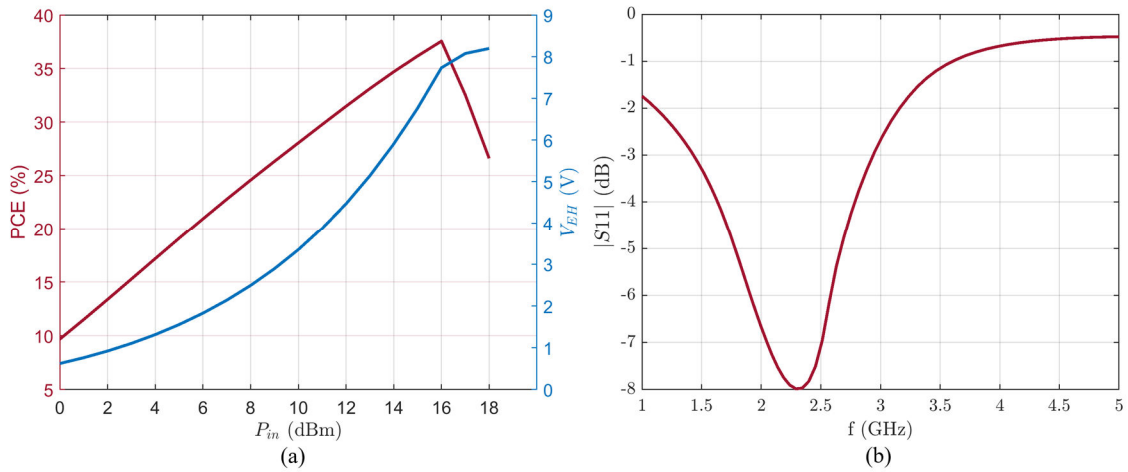


Figure 7.6 Post–layout simulations of the voltage doubler showing: (a) PCE (red) and V_{EH} (blue), and (b) $|S_{11}|$ matching simulations.

Furthermore, the PCE is reduced to approximately 30%, compared to the estimated 65% at the schematic level. This reduction is attributed to the increased resistive and reactive losses introduced by parasitic elements and degraded matching conditions, as seen in the plot of $|S_{11}|$ in **Figure 7.6**(b). Additionally, the inclusion of metal density filling layers introduces significant parasitic capacitance due to their large spatial distribution. As a result, the optimal value of the matching inductor had to be reduced to re–establish resonance at the operating frequency.

Furthermore, the effect of bondwire inductance was incorporated into the simulation. Based on the selected package, a bondwire inductance of approximately 1 nH/mm was assumed, corresponding to a total inductance of about 2 nH for a 2 mm wire. This required the on–chip matching inductor to be reduced to 5 nH in order to compensate for the external inductive contribution.

Despite this degradation, the rectifier maintains a sufficient output voltage dynamic range around $P_{in} \approx 11.5$ dBm. The output voltage exhibits adequate sensitivity to input amplitude variations, making it suitable for the intended ASK–PWM modulation scheme.

7.2.2 Bandgap references

Based on the discussion in Subsubsection 3.2.3.4, linear regulators are preferred for this work due to their compatibility with low–power operation and ease of integration without bulky inductive components. In particular, an LDO regulator is selected to efficiently regulate the rectified voltage under limited headroom conditions typical of RF energy harvesting systems. Consequently, a bandgap reference circuit is needed to provide a stable, process–independent reference voltage for regulation.

Bandgap references are fundamental analog building blocks in power conditioning systems, as they provide stable reference voltages that are ideally independent of temperature and supply variations. These references are widely used in various circuits, including operational amplifiers, comparators, ADCs, and DACs, where precise and stable biasing is required.

The operating principle of a bandgap reference relies on combining two voltage components with opposite temperature coefficients. Specifically, a voltage with a negative temperature coefficient (typically the base–emitter voltage of a bipolar junction transistor, V_{BE}) is combined with a voltage that is proportional to absolute temperature (PTAT). The PTAT voltage is commonly generated from the difference between two base–emitter voltages operating at different current densities. By properly scaling and summing these two components, a temperature–independent reference voltage can be achieved.

Bandgap reference circuits can be broadly classified into two categories: high–voltage and low–voltage references. High–voltage bandgap references typically generate an output voltage close to or greater than the silicon bandgap voltage ($\approx 1.24\,\mathrm{V}$). These are commonly realized by directly summing a PTAT voltage with an inverse PTAT (IPTAT) voltage in series, resulting in a relatively high output voltage.

In contrast, low–voltage bandgap references are designed to operate below the silicon bandgap voltage. In these architectures, the PTAT and IPTAT devices are first converted into currents, which are then summed and translated back into a voltage through a resistive element. This approach enables operation at lower supply voltages and is particularly suitable for low–power systems.

In this work, the focus is placed on low–voltage bandgap references. This choice is motivated by the stringent power constraints imposed by WPT, where minimizing dynamic power consumption is critical. Operating the digital circuitry at a reduced supply voltage significantly lowers switching power, and a low–voltage reference naturally supports this requirement. Furthermore, when higher voltage levels are required for analog blocks, the reference can be subsequently amplified.

In conventional bandgap reference implementations, bipolar transistors and high–value resistors are commonly employed to achieve low temperature dependence and low power consumption [106]. As a result, low–power bandgap operation generally requires very small bias currents, which in turn necessitates the use of large–valued resistors, often in the range of hundreds of kΩ, to generate the required voltage reference. Implementing such large resistances on–chip leads to significant area overhead and can introduce further variability and noise concerns.

In CMOS technologies, these bipolar devices are typically realized using parasitic vertical P–N–P–doped (PNP) transistors, where the n–well serves as the base. However, such devices exhibit limited performance due to the relatively high resistance of the n–well [25], [26].

To address these limitations, a design approach that avoids both vertical bipolar transistors and large passive resistors is desirable. In this work, a fully CMOS–based

bandgap reference architecture is adopted, inspired by the ultra–low–power design reported in [107], which achieves a power consumption on the order of 300 nW. The proposed implementation leverages MOS devices operating in subthreshold to generate the required temperature–dependent components, thereby eliminating the need for parasitic BJTs and large resistors.

Based on this approach, two bandgap reference circuits were designed to meet the requirements of the proposed control system: a high–voltage reference generator, shown in **Figure 7.7**, and a low–voltage reference generator, shown in **Figure 7.8**. These two references provide flexibility in supporting both low–power digital operation and higher–voltage analog interfaces within the IC.

In **Figure 7.7**, transistors M_1–M_6 generate a PTAT voltage through the difference of their gate–to–source voltages when operating in the subthreshold region. Transistor M_7, on the other hand, produces an IPTAT voltage. Together, these components are combined to form a temperature–stable reference. Transistors M_8-M_{10} and M_{21}–M_{24} form a cascoded PMOS supply–independent bias network used to bias the cascoded PMOS current sources M_{13}–M_{20}. The cascode structure improves bias stability and reduces sensitivity to supply variations. Transistor M_8 operates in the triode region and provides a well–defined current reference for the current mirror network

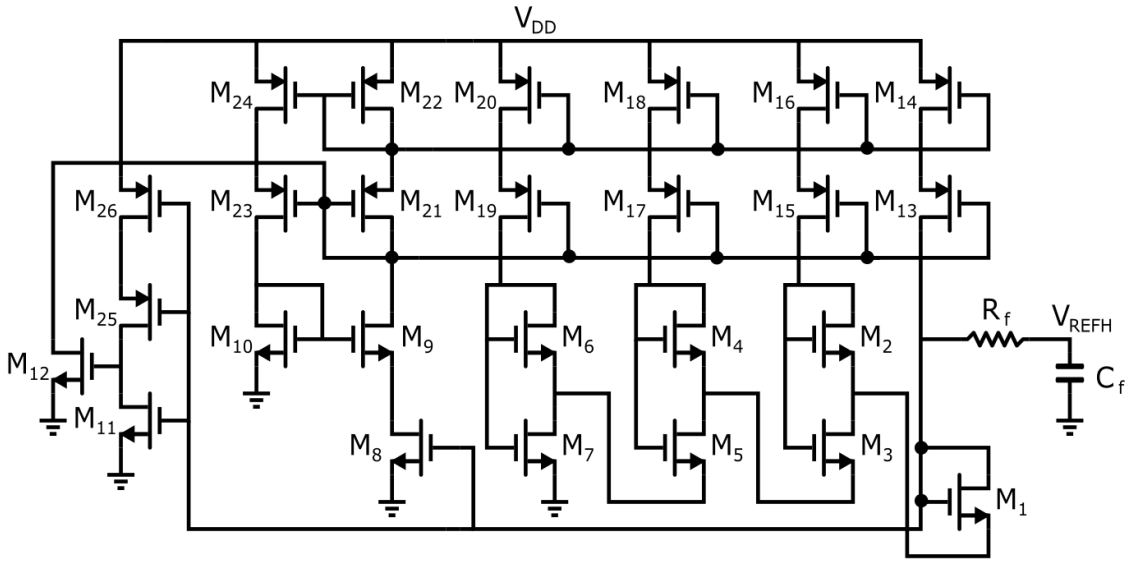


Figure 7.7 A CMOS only high–voltage bandgap reference.

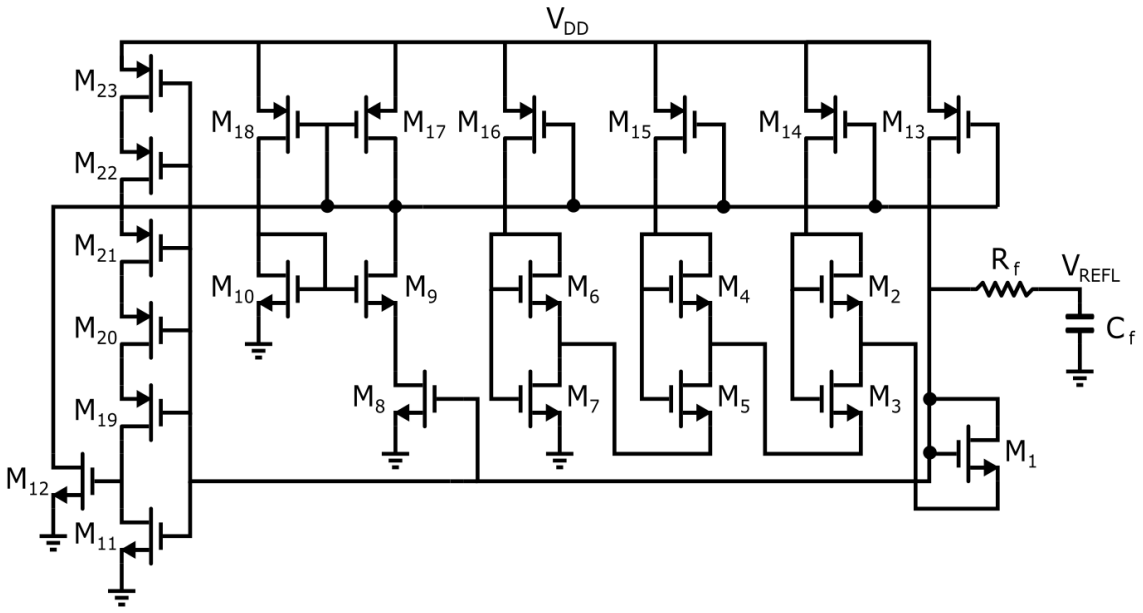


Figure 7.8 A CMOS only low–voltage bandgap reference.

Additionally, transistors M_{11}, M_{12}, M_{25}, and M_{26} implement an inverter–based start–up circuit to guarantee proper circuit initialization and to prevent the undesired zero–current operating point. Finally, R_f and C_f are included to suppress high–frequency noise coupling from the supply to the reference output.

Applying Kirchhoff's Voltage Law (KVL) from the high–reference output voltage (V_{REFH}) to ground yields:

$$V_{REFH} = V_{GS7} - V_{GS6} + V_{GS5} - V_{GS4} + V_{GS3} - V_{GS2} + V_{GS1}. \tag{7.3}$$

Since all transistors operate in the subthreshold region to emulate BJT–like exponential behavior and minimize power consumption, the gate–to–source voltage V_{GS} of each transistor can be expressed as:

$$V_{GS[X]} = \eta V_T \, ln\left(\frac{I_{D[X]}}{K_{[X]} I_s}\right) + V_{TH}, \tag{7.4}$$

where η is the subthreshold slope factor, $V_T = \frac{k_b T}{q}$ is the thermal voltage, k_b is the Boltzmann constant, T is the absolute temperature, q is the electron charge, $I_{D[X]}$ is the drain current of transistor $M_{[X]}$, $K_{[X]} = \mu_n C_{ox} \frac{W_{[X]}}{L_{[X]}}$ is the device transconductance parameter, μ_n is the mobility of electrons, C_{ox} is the oxide capacitance, $W_{[X]}$ is the width of transistor $M_{[X]}$, $L_{[X]}$ is the length of transistor $M_{[X]}$, I_s is the process–dependent current, and V_{TH} is the transistor's threshold voltage.

Substituting (7.4) into (7.3) and simplifying, the reference voltage can be re–expressed as [107]:

$$V_{REFH} = V_{TH} + \eta V_T \, ln\left(\frac{I_{D7}}{K_7 I_S}\right) + \eta V_T \, ln\left(\frac{K_2 K_4 K_6}{K_1 K_3 K_5}\right). \tag{7.5}$$

From (7.5), it can be observed that the reference voltage consists of a temperature–dependent term (IPTAT contribution from M_7) and a PTAT component arising from the geometric ratios of transistors M_1–M_6. By carefully selecting the transistor sizing ratios, the PTAT and IPTAT terms can be made to cancel each other, resulting in a temperature–independent reference voltage.

By differentiating (7.5) with respect to temperature, it can be shown that an appropriate choice of transistor dimensions allows the reference voltage to converge to [107]:

$$V_{REFH} \approx V_{TH0}, \tag{7.6}$$

where V_{TH0} is the threshold voltage extrapolated to 0 K.

It is noteworthy that, unlike conventional BJT–based bandgap references, where a PTAT voltage is added to a base–emitter voltage to produce a reference near the silicon bandgap ($\sim$ 1.24 V), this CMOS–based architecture achieves a low–voltage reference of V_{TH0} by combining PTAT and IPTAT components directly. This enables operation below the bandgap voltage, making the design particularly suitable for low–voltage, low–power applications.

The same operating principle applies to the low–voltage bandgap reference shown in **Figure 7.8**.

Compared to the original configuration presented in [107], several modifications were introduced to adapt the bandgap reference to the requirements of the proposed wirelessly powered control system. These modifications are summarized as follows:

- **Improved $PSRR$ through cascoding:** Cascoded PMOS transistors were incorporated into the high–voltage bandgap reference (**Figure 7.7**) to enhance $PSRR$, which quantifies the sensitivity of the reference voltage to supply variations. The original design in [107] exhibits relatively low PSRR compared to conventional bandgap implementations. By introducing cascoding, the output resistance of the bias network is increased, thereby improving supply isolation and stabilizing the reference voltage. It is important to note that this modification is feasible in the present design since the supply voltage is derived from the RF rectifier output (approximately 4 V), providing sufficient headroom to accommodate the additional voltage drop introduced by the cascoded structure.
- **Mixed–voltage device utilization:** Most transistors in the design are implemented using 3.3 V devices to ensure reliable operation under higher voltage conditions. However, transistors M_9 and M_{10} are realized using 1 V devices to enable operation at lower harvested voltages due to their lower threshold voltages.
- **High–frequency noise filtering and $PSRR$ enhancement:** A passive RC network (R_f and C_f) is added to suppress high–frequency supply noise and improve $PSRR$ at higher frequencies. This is particularly important in the present system, where the supply originates from an RF rectifier operating at 2.4 GHz. The added capacitance C_f helps attenuate residual RF ripple and prevents its coupling into the reference output. Additionally, C_f provides local charge storage, which supports transient current demands from the digital switching circuitry.

The low–voltage bandgap reference shown in **Figure 7.8** follows the same fundamental operating principle as the high–voltage implementation in **Figure 7.7**. However, it is specifically designed to generate a reduced reference voltage suitable for low–voltage digital switching circuitry.

In this design, the cascoded PMOS transistors used in **Figure 7.7** are intentionally omitted. This decision is motivated by two key considerations. First, the low–voltage bandgap is supplied through a regulated voltage derived from the high–voltage bandgap (as shown in **Figure 4.3** in Subsection 4.2.1), which already provides significant power supply rejection. As a result, the additional $PSRR$ improvement obtained from cascoding becomes less critical at this stage. Second, the available supply voltage for the low–voltage bandgap is lower than the harvested 4 V, leaving insufficient voltage headroom to accommodate cascoded devices while maintaining proper transistor operation. Removing the cascoded PMOS structure therefore ensures correct biasing and reliable operation under reduced supply conditions.

To further improve robustness, additional PMOS transistors (M_{21}–M_{23}) are incorporated into the start–up circuitry. Although these devices remain off during normal operation, their inclusion serves two important purposes. First, by stacking multiple PMOS transistors in series, the effective turn–on voltage of the start–up path is increased. This introduces a controlled voltage drop from V_{DD} toward the internal nodes, ensuring that the start–up circuitry does not interfere with steady–state operation unless sufficiently high supply conditions are met. This effectively expands the allowable range of V_{DD} without degrading the temperature stability of the reference voltage.

Second, the stacked configuration improves the overall $PSRR$ of the circuit. In this design, the start–up network represents a dominant leakage path through which supply variations can couple into the reference node. Increasing the effective resistance of this path through transistor stacking reduces this coupling, thereby enhancing supply rejection.

It is worth noting that such modifications were not required in the high–voltage bandgap (**Figure 7.7**), where the higher output reference voltage naturally ensures that the start–up circuitry remains inactive during normal operation.

Finally, all transistors in **Figure 7.8** are implemented using 1 V devices. Given the lower supply voltage of this stage, these devices provide sufficient overdrive to maintain proper operation while enabling reduced power consumption and improved compatibility with low–voltage digital circuitry.

Both bandgap references were designed and fully laid out, and their post–layout simulation results are presented in **Figure 7.9**.

Figure 7.9(a) shows the reference voltage of both designs as a function of temperature. The high–voltage bandgap reference V_{REFH} generates a stable output of approximately 1.44 V with a temperature coefficient of 24 ppm/°C over the range of 0°C to 100°C. The low–voltage bandgap reference V_{REFL} produces a reference of approximately 0.68 V with a temperature coefficient of 167.97 ppm/°C over the same temperature range. Although the temperature dependence of the low–voltage reference is higher, it remains sufficiently stable for digital switching applications, where absolute precision is less critical than in analog blocks.

Figure 7.9(b) illustrates the line regulation performance of both bandgap references. For the high–voltage bandgap, the supply voltage V_{DD} corresponds to the output of the RF rectifier V_{EH} and is expected to vary between approximately 3.5 V and 4.5 V due to amplitude modulation. As shown in the figure, the reference voltage remains effectively constant at 1.44 V across this range, demonstrating good line regulation. For the low–voltage bandgap, the supply is provided by the regulated analog rail ($V_{DDH} \approx 2.6$ V). The simulation confirms that the reference voltage remains stable up to this supply level, indicating proper operation within the intended voltage domain.

The start–up behavior of both bandgap references is verified in **Figure 7.9**(c), where a ramped supply voltage is applied. In the absence of the start–up circuitry, the bandgap references remain stuck in the zero–current state and fail to initialize. With the inclusion of the start–up circuits, both designs successfully converge to their intended operating points, producing the expected reference voltages.

The $PSRR$ is a critical metric in this system due to multiple potential sources of supply disturbance. These include: (i) high–frequency ripple originating from the RF rectifier

operating at 2.4 GHz, (ii) low–frequency variations due to ASK–PWM amplitude modulation at approximately 100 kHz, and (iii) additional noise coupled through supply routing.

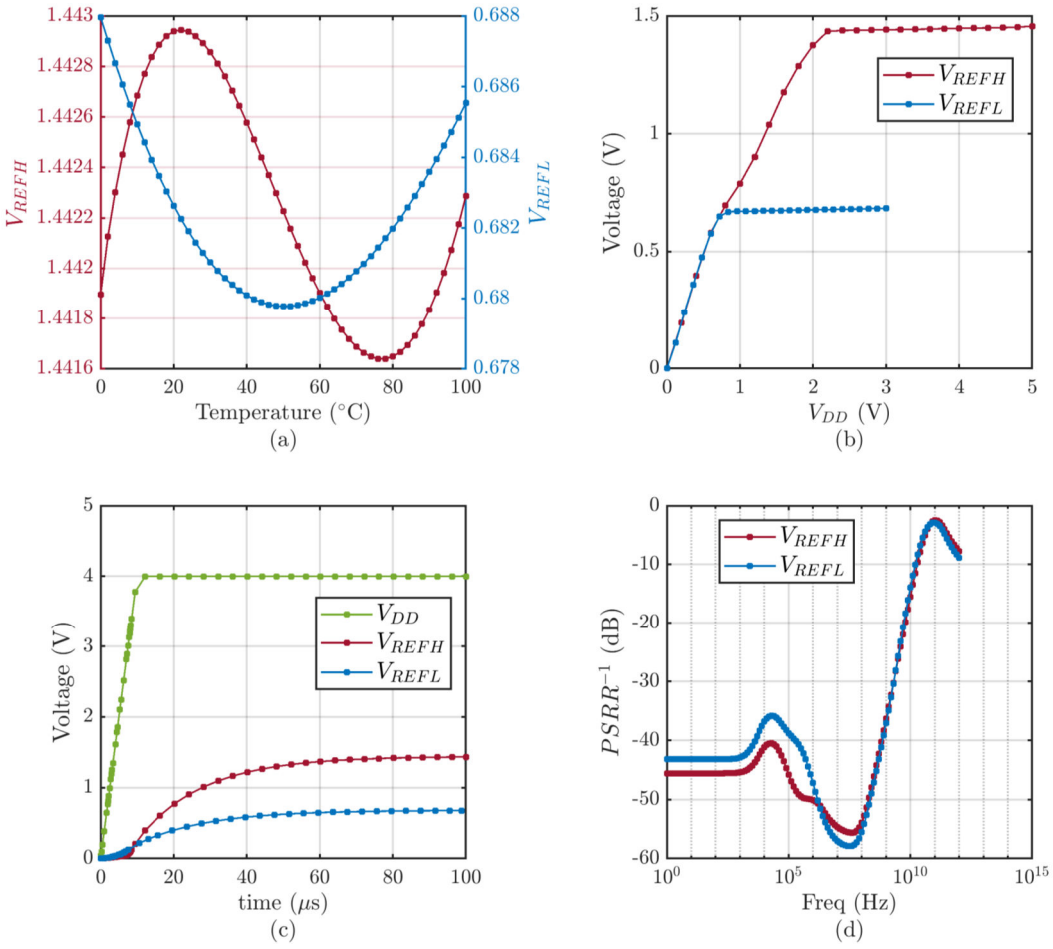


Figure 7.9 Performance of the two designed bandgap references showing: (a) temperature dependence, (b) supply dependence, (c) start–up verification, and (d) $PSRR^{-1}$ simulation.

Figure 7.9(d) presents the simulated $PSRR^{-1}$ of both bandgap references. At low frequencies (DC), the $PSRR^{-1}$ is approximately –40 to –45 dB. In the frequency range between 100 kHz and 1 GHz, the effect of the on–chip filtering network becomes evident. The R_f–C_f filter, designed with a cutoff frequency below the modulation frequency, effectively suppresses supply variations, maintaining the $PSRR^{-1}$ below –40 dB across this band. Without this filtering network, the $PSRR^{-1}$ in this range degrades to approximately –10 dB, which would be undesirable.

At higher frequencies, a resonance peak is observed around 100 GHz, associated with the self–resonant frequency of the 10 pF MIM capacitor used for C_f. This observation is consistent with the analysis presented in **Figure 7.4**. However, this resonance is not of practical concern, as it lies far beyond the frequency content of the system, including the RF carrier, modulation frequencies, and beamforming signals.

Finally, the total power consumption of the high–voltage and low–voltage bandgap references is 22.75 μW and 13.67 μW, respectively. These low power levels make the designs well–suited for integration in wirelessly powered systems with stringent energy constraints.

7.2.3 Voltage regulators

Voltage regulators are essential components for maintaining a stable supply voltage in the presence of load and supply variations. In particular, the regulator must provide the required current to the load while ensuring that the output voltage remains constant, even as the load conditions change. To achieve this, the regulator continuously monitors the output and adjusts its operation through a feedback mechanism.

In this work, the voltage regulator consists of three main building blocks: a bandgap reference that provides a stable reference voltage, an operational amplifier (Op Amp) configured in a negative feedback loop to regulate the output, and a pass transistor that delivers the required current to the load. The Op Amp compares the output voltage to the reference and adjusts the gate voltage of the pass device accordingly, thereby maintaining a constant output voltage.

The design of the voltage regulator involves several critical considerations, including the Op Amp design, the choice of the pass transistor, loop stability, and voltage headroom constraints.

A key requirement for the Op Amp is a high DC gain (on the order of 80 dB). A higher gain improves the accuracy of the regulation by enforcing a stronger virtual short between the Op Amp inputs, ensuring that the output voltage closely tracks the reference voltage.

The regulated voltage V_{REG} can be related to supply variations through the regulator loop gain as:

$$PSRR^{-1}(s) = \frac{\frac{V_{REG}}{V_{DD}}(s)}{1 + L(s)}, \tag{7.7}$$

where $L(s)$ is the loop gain of the regulator. The numerator represents the direct coupling from the supply to the output, which depends on the choice of pass transistor, while the denominator reflects the suppression provided by the feedback loop.

Since $L(s)$ is large at low frequencies, the regulator achieves good power supply rejection in this region. However, as frequency increases and the loop gain decreases, the $PSRR$ degrades. Therefore, achieving both high DC gain and sufficient bandwidth in the Op Amp is crucial for maintaining strong $PSRR$ across a wide frequency range, particularly in the presence of supply ripple from the RF rectifier and modulation signals.

Three main Op Amp architectures were considered: The first is a single–stage differential amplifier**.** This architecture consists of a differential pair with active loads and typically achieves moderate gain (40–60 dB) with relatively high bandwidth. Its simplicity and single dominant pole make it inherently stable, but the limited gain may not be sufficient for accurate voltage regulation.

The second is a two–stage amplifier. This topology combines a differential input stage with a common–source gain stage, enabling high gain (80–90 dB). However, the presence of two high–impedance nodes introduces two low–frequency poles, which can lead to significant phase shift (approaching $180°$) and potential instability. Compensation techniques, such as Miller compensation, are required to improve phase margin. While effective, these techniques reduce bandwidth due to the Miller effect, which in turn degrades high–frequency $PSRR$. As a result, the regulator may exhibit peaking and even amplify supply noise beyond the dominant pole frequency.

The last option is a telescopic (cascoded) amplifier. This architecture achieves high gain with improved bandwidth compared to the two–stage design, as it avoids the need for

compensation. However, it suffers from limited voltage headroom due to stacked transistors, which restricts the ICMR. This is particularly problematic in low–voltage designs, where the allowable signal swing is already constrained.

To determine the most suitable Op Amp architecture, the design must be considered jointly with the choice of the pass transistor, as the overall loop dynamics and voltage headroom are strongly influenced by the pass device configuration.

The choice of the pass transistor is a critical design decision in voltage regulator architectures. Three common configurations are typically considered: a PMOS pass device in a common–source configuration, an NMOS pass device in a source–follower (common–drain) configuration, and a native NMOS source–follower.

The PMOS pass transistor offers a key advantage in terms of dropout voltage. Specifically, the voltage drop between V_{DD} and the regulated output is limited to approximately one overdrive voltage, typically in the range of 200–$500\,\mathrm{mV}$. This makes PMOS–based regulators well–suited for applications requiring low dropout operation. In the context of this work, this is particularly advantageous, as it enables the regulator to produce an output voltage close to the harvested voltage, thereby maximizing the usable energy from the RF rectifier.

In such configurations, the pass transistor itself contributes significant gain, effectively acting as an additional amplification stage. As a result, the Op Amp can be implemented as a single–stage amplifier, and the overall regulator behaves as a two–stage system. This simplifies the Op Amp design while still achieving sufficient loop gain for regulation.

However, the use of a PMOS pass device introduces several drawbacks. First, the small–signal path from the supply to the output exhibits a non–negligible gain, as the PMOS operates similarly to a common–gate stage for supply perturbations. Consequently, variations in V_{DD} can be directly coupled to the output, leading to degraded *PSRR* particularly at higher frequencies.

Second, the presence of two gain stages, the Op Amp and the pass device, introduces additional poles in the loop transfer function. This reduces the overall bandwidth and complicates stability. As discussed previously, a reduction in loop bandwidth leads to a

faster degradation of $PSRR$ with frequency as indicated by (7.7) and may result in peaking in the $PSRR$ response beyond the dominant pole. This effect is further exacerbated by the intrinsic gain of the pass device, which amplifies supply noise at higher frequencies.

The limitations associated with the PMOS pass transistor can be mitigated by employing an NMOS pass device. In this configuration, the pass transistor behaves as a source–follower, which significantly improves the $PSRR$. In particular, supply variations at V_{DD} are attenuated at the output due to the inherent source–follower behavior, resulting in reduced coupling of supply noise to the regulated voltage.

In addition, the use of an NMOS pass device eliminates the additional gain stage introduced by a PMOS pass transistor. Consequently, the overall loop gain is determined primarily by the Op Amp itself. When combined with a single–stage Op Amp architecture, this results in improved bandwidth and enhanced high–frequency $PSRR$ performance.

However, NMOS pass transistors suffer from a major drawback: a larger dropout voltage. Specifically, the output voltage is limited by the gate–to–source voltage required to keep the device in conduction, resulting in a significant voltage drop between V_{DD} and the regulated output. In the context of a boosted regulator, this leads to an output voltage that is substantially lower than the available harvested voltage, reducing overall efficiency.

To alleviate this issue, native NMOS devices can be employed. These transistors exhibit very low threshold voltages (typically below 100 mV), which significantly reduces the required V_{GS} and, consequently, the dropout voltage. This enables the regulator to achieve higher output voltages while retaining the advantages of improved $PSRR$ and bandwidth.

In this work, two voltage regulator designs were implemented, as shown in **Figure 7.10**. The first design, shown in **Figure 7.10**(a), is a boosted regulator that utilizes the high–voltage bandgap reference (1.44 V) to generate a regulated output of 2.6 V (2.58 V Simulated), suitable for analog building blocks such as control DACs. The second design, shown in **Figure 7.10**(b), uses the low–voltage bandgap reference (0.68 V) to generate a regulated output of approximately 0.75 V, suitable for digital switching circuitry. Additionally, this regulator provides auxiliary reference voltages (e.g., 0.5 V and 0.3 V) for use in comparator–based communication and control circuits.

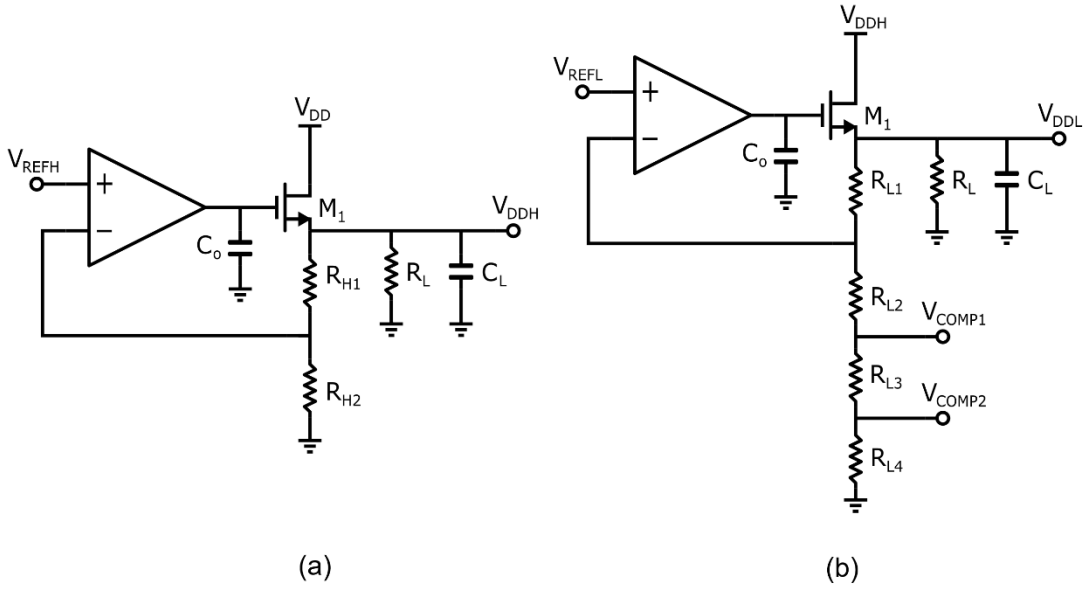


Figure 7.10 Designed boosted voltage regulators: (a) high–voltage, and (b) low–voltage regulator.

For both designs, the Op Amp is implemented as a single–stage differential amplifier with current mirror active loads. NMOS transistors are used for the input differential pair to provide an $ICMR$ that extends closer to V_{DD}, which is beneficial when interfacing with higher reference voltages. All transistors in the Op Amp are biased in the subthreshold region to minimize power consumption. The device sizing is carefully optimized to achieve a suitable trade–off between bandwidth and power efficiency, which is critical for wirelessly powered operation.

The Op Amp biasing is realized using a supply–independent bias network, where an on–chip resistor defines the bias current. An output capacitor C_o is included at the Op Amp output to shift its dominant pole and separate it from the pole associated with the regulator output node. The value of C_o is optimized to ensure adequate bandwidth and phase margin.

In addition, a load capacitor $C_L = 50$ pF is placed at the regulator output to smooth the DC voltage and reduce $PSRR$ peaking. The pass transistor M_1 is implemented using a native NMOS device to minimize dropout voltage and maximize the achievable output voltage. To support load currents corresponding to resistances as low as $500\ \Omega$, the pass

device is realized as five parallel transistors, each with dimensions of $100\,\mu$m width, providing sufficient current–driving capability.

The post–layout performances of both voltage regulators are presented in **Figure 7.11**. **Figure 7.11**(a) shows the open–loop gain and phase responses of the two regulator designs. The observed gain corresponds to the combined effect of the Op Amp gain and the attenuation introduced by the NMOS source–follower pass transistor. The DC gain is approximately 50–55 dB for both regulators. The dominant pole is located around 1 kHz, primarily set by the bandwidth of the Op Amp, while a second pole appears near 10 MHz, associated with the output load time constant of the regulator.

The phase margin is designed to be approximately 80°, ensuring it remains above 75° under all operating conditions. This provides a stable response with minimal overshoot and prevents ringing in the time domain.

Figure 7.11(b) presents the line regulation performance of both regulators. The high–voltage regulator produces $V_{DDH} = 2.6$ V, which is a boosted version of the high–voltage bandgap reference V_{REFH}, and is suitable for analog blocks such as DACs. Since the input supply to this regulator is the harvested voltage from the RF rectifier V_{EH} (**Figure 4.3**), it is expected to vary between approximately 3.5 V and 4.5 V due to amplitude modulation. As shown in the figure, the regulator maintains a constant 2.6 V Output across this range.

The low–voltage regulator is supplied by V_{DDH} and generates $V_{DDL} = 0.75$ V, suitable for digital switching circuitry. To account for process, voltage, and temperature (PVT) variations, the supply was swept up to 3 V, and the regulator maintains a stable output over this range. In addition, the regulator provides auxiliary reference voltages of 0.5 V and 0.3 V, which are used for comparator–based circuits in the communication and control blocks.

Figure 7.11(c) verifies the start–up behavior of all regulator outputs. With the inclusion of start–up circuitry in both the main regulator loop and the op amp biasing network, all voltages converge correctly to their intended steady–state values.

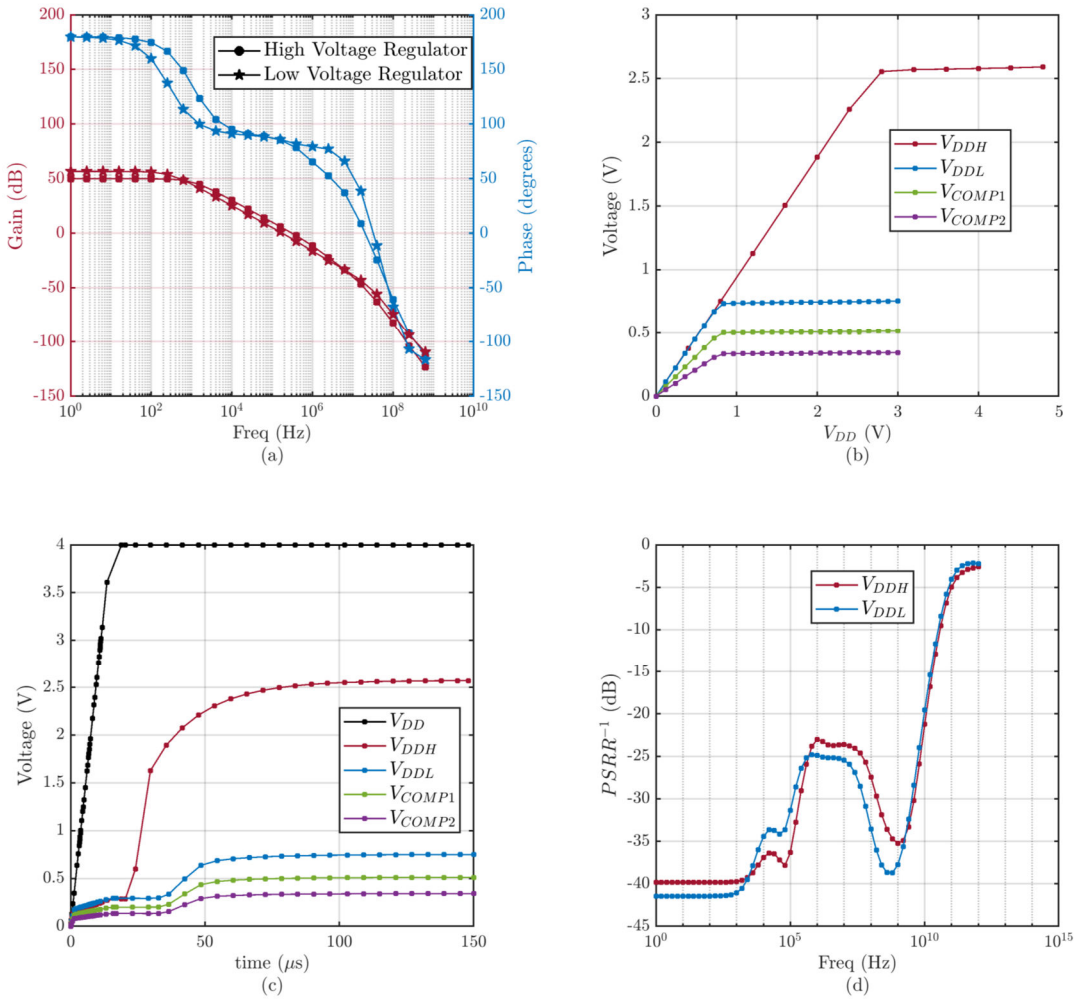


Figure 7.11 Post–layout performance simulations of both voltage regulator designs: (a) open–loop gain and phase, (b) supply dependence, (c) start–up performance, and (d) *PSRR -1* simulations.

Figure 7.11(d) shows the simulated $PSRR^{-1}$ of both regulators. At low frequencies, the $PSRR^{-1}$ is approximately –40 dB, which is consistent with the $PSRR$ of the bandgap reference (**Figure 7.9**(d)). This is because the high–voltage bandgap and the regulator are effectively connected in parallel from a supply noise perspective (**Figure 4.3**), and the overall $PSRR$ is limited by the weakest (lowest impedance) path from V_{DD} to the output. In this case, the bandgap reference dominates and sets the $PSRR$ limit.

This observation is further confirmed by increasing the Op Amp gain to approximately 90 dB using a two–stage architecture. Despite the higher gain, the low–frequency $PSRR^{-1}$

remains close to –40 dB, indicating that improving regulator gain alone does not enhance $PSRR$ when the bandgap reference is the limiting factor.

As frequency increases, the $PSRR$ begins to degrade at a rate of approximately 20 dB/decade, starting at the dominant pole of the Op Amp (≈1 kHz). This behavior is consistent with the reduction of loop gain beyond the bandwidth of the amplifier.

Two important design insights can be drawn from this result. First, increasing the Op Amp bandwidth would push the $PSRR$ degradation to higher frequencies, improving noise rejection over a wider range. However, this requires higher bias currents, which conflicts with the stringent power constraints of WPT systems. Second, increasing the Op Amp gain without improving bandwidth can be detrimental. In the case of a two–stage amplifier, the higher gain extends the region over which $PSRR$ degrades, potentially leading to peaking and amplification of supply noise at intermediate frequencies (e.g., around 1 MHz). This highlights the importance of co–optimizing gain and bandwidth rather than maximizing gain alone.

At higher frequencies, the effect of the output capacitor ($C_L = 50\,\text{pF}$) becomes apparent, introducing resonance behavior similar to that observed in the bandgap reference filtering network (**Figure 7.9**(d)). However, this occurs well beyond the frequency range of interest for the system.

7.3 Communication and Digital Frame Router Blocks

With the RF rectifier and power conditioning circuitry now established, attention is directed to the ASK–PWM demodulator and decoder, as well as the digital frame router. The implementations of these blocks closely follow those presented in Subsections 5.3.2 and 4.2.3, respectively. Therefore, this section focuses on the key differences between the IC realization and the PCB/synthesized implementations.

The ASK demodulator was previously presented in **Figure 5.17** (Subsection 5.3.2). The same design methodology used for the PCB implementation is adopted for the IC realization, with several key modifications outlined below.

First, the matching inductor L_{in} is omitted, as the harvesting rectifier inductor L_M in **Figure 7.1** provides impedance matching for both the harvesting and communication rectifiers, as demonstrated in **Figure 4.2**(b) and **Figure 6.15**. The addition of the communication rectifier on–chip introduces only minimal capacitive and resistive loading and therefore does not require retuning of L_M.

Second, diodes D_1 and D_2 in **Figure 5.17** are replaced with diode–connected PMOS transistors, implemented using a schematic similar to that of the harvesting rectifier shown in **Figure 7.1**. Section 6.4 showed that a lossy resistor R_M is required in the PCB implementation to limit current leakage into the communication rectifier and preserve the PCE of the harvesting path. In the IC implementation, this is no longer necessary, as device sizing of D_1 and D_2 can be reduced to limit the current in the communication path, thereby maintaining both matching and PCE.

Third, the data rate in this implementation is increased to 100 kbps, compared to 15 kbps as discussed in Section 7.1. Consequently, the time constants in (5.1)–(5.3), and thus the associated resistor and capacitor values, are adjusted to allow the 100 kbps modulation to pass while still attenuating the 2.4 GHz carrier.

Fourth, the amplifier is implemented as an uncompensated two–stage topology to achieve high gain and wide bandwidth under open–loop operation. To extend the ICMR, the amplifier is powered from V_{DDH}, enabling it to accommodate variations in both the envelope amplitude and its average level.

Finally, the comparator is powered from the low–voltage supply V_{DDL} and compares the amplified signal against the reference voltage V_{COMP1} generated by the low–voltage regulator. This stage produces the digital output V_{dig} at a reduced supply voltage, thereby lowering the dynamic power consumption of the subsequent digital circuitry.

Similarly to the ASK demodulator described in this section, the PWM decoder design is based on the implementation presented for PCB realization in **Figure 5.19** of Subsection 5.3.2. **Figure 7.12** shows the modified PWM decoder suitable for IC realization, with the major differences outlined below.

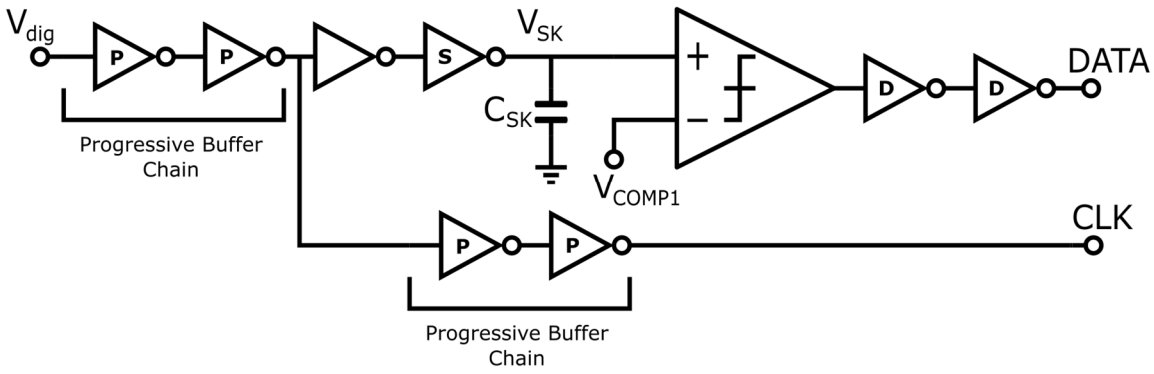


Figure 7.12 IC realization of the PWM decoder.

First, to improve the driving capability of the ASK demodulator comparator, a progressive buffer chain (labeled "P" in the figure) is introduced to drive the capacitive load of the subsequent stage. A similar progressive buffer chain is also added in the CLK path to drive the large capacitive load of the shift register in the frame router.

Next, unlike the skewed inverter in **Figure 5.19**, where a skewing resistor R_{skew} was required for PCB implementation, this component is no longer necessary in the IC realization. Instead, the skewing operation is achieved through transistor sizing. The skewed inverter (denoted as "S" in **Figure 5.19**) is intentionally designed with asymmetric device dimensions: the PMOS transistor has a width of 200 nm and a length of 20 μm, while the NMOS transistor has a width of 20 μm and a length of 130 nm. This sizing produces a fast high–to–low transition, driven by the strong NMOS device, and a slow, nearly linear low–to–high transition due to the long–channel PMOS device. The comparator used for PWM decoding is identical to that used for ASK demodulation.

Furthermore, a delay buffer (denoted as "D" in **Figure 5.19**) is inserted at the comparator output. This delay stage is implemented using minimum–width NMOS and PMOS devices with extended channel lengths (20 μm) to introduce the required propagation delay. Careful PVT analysis is required to ensure that this delay remains within acceptable bounds, thereby maintaining reliable synchronization between CLK and $DATA$ in the shift register.

Finally, due to the increase in data rate from 15 kbps to 100 kbps, the timing constant in (5.4) associated with the skewing operation has been redesigned. The PWM decoder is

now capable of decoding a logic “0” represented by a 10 μs high–pulse at 50% duty cycle, and a logic “1” represented by a 25 μs high–pulse at 71.4% duty cycle.

As for the digital frame router, although a fully synthesized design was presented in Chapter 5 (capable of serial–to–parallel conversion, acknowledgment check, ID verification, data storage, and data routing), the IC implementation could not follow the same approach due to digital design licensing constraints. Consequently, both the schematic and layout were implemented manually. The overall architecture remains similar to that shown in **Figure 4.6** of Subsection 4.2.3. However, key modifications were introduced. In particular, the delay cells are realized using an analog approach based on long–channel inverters, similar to the “D” inverter employed in the PWM decoder, rather than using cascaded synthesized inverter cells.

Furthermore, as discussed in Section 7.1, the system requirements were expanded to accommodate additional RF attenuators and increased resolution. As a result, the number of DACs was doubled, and their resolution was increased by 2 bits. Correspondingly, the shift register length was increased from 13 bits to 21 bits, the data holder from 8 bits to 16 bits, and the data director from 4 bits to 12 bits. A block diagram of the modified digital control block will be presented in Section 7.5, along with the IC simulation results.

Referring to the data format shown in **Figure 4.7**, where each frame packet previously consisted of 15 bits, the enhanced system functionality increases the packet length to 23 bits. The updated frame structure comprises 4 acknowledgment bits, 2 control block ID bits, 2 cell ID bits, 6 AT data bits, 6 PS data bits, and 3 preamble bits.

The increase in packet length would, in principle, reduce the achievable frame (sample) rate compared to the implementation in Chapters 4 and 5, where a rate of 582–842 samples/s was reported. However, this reduction is more than compensated by the higher data rate, which has been increased from 15 kbps to 100 kbps. As a result, the effective frame rate improves to approximately 1785–3636 samples/s, depending on the proportion of transmitted logic “1” bits, which directly affects the average bit duration under the adopted PWM scheme.

7.4 Low–Power Level–Shifting DAC Design

We now turn our attention to the design of the DACs. To reduce the number of digital output pins from the control system, and consequently minimize beamformer module routing complexity, it is desirable to convert multiple digital control bits into a single analog control voltage using DACs. Controlling four RF phase shifters and four RF attenuators requires $6\ \text{bits} \times 8$ beam–steering elements, resulting in 48 digital output traces, which is impractical. By employing eight 6–bit DACs, the number of required control traces is reduced from 48 to 8, significantly simplifying routing and improving system integration.

Several key requirements must be satisfied by the DACs within each control block. First, both static and dynamic power consumption must be minimized to ensure compatibility with WPT operation. Second, the DACs must provide a sufficiently large output voltage range to achieve the required control span for the RF beam–steering circuitry, despite being driven by low–voltage digital input levels. Third, the speed requirement is relatively modest (on the order of 4 kilo samples per second), allowing slower conversion speeds to be traded for reduced power consumption. Finally, the DAC area must be minimized to enable a compact implementation of the control blocks.

From an architectural perspective, DACs reported in the literature can generally be classified into two main categories: current–mode DACs and resistor–based (decoder–based) DACs. Current–mode DACs rely on digitally controlled current sources that are summed and converted to a voltage across a load, whereas decoder–based DACs employ switchable resistor networks to translate digital inputs into an analog voltage.

A representative current–mode DAC architecture is shown in **Figure 7.13** [25]. In this implementation, an Op Amp with negative feedback establishes a stable reference voltage, generating a bias current of V_{ref}/R_{ref} through transistor Q_4. This current is then mirrored into multiple branches corresponding to the input bits. When a control bit (e.g., d_1) is low, transistor Q_1 turns on, diverting the branch current to ground. Conversely, when d_1 is high, Q_1 turns off, allowing a cascoded current source formed by Q_2 and Q_3 to mirror the reference current into the load resistance.

However, this architecture presents several drawbacks. First, the digital control signals $(d_1, d_2, ...)$ must swing close to V_{DDH} to fully turn off the PMOS devices (e.g., Q_1). This requirement forces the digital circuitry to operate at a high supply voltage, resulting in increased dynamic power consumption. Second, for a 6–bit implementation, a total of $6 + 1$ current branches remain continuously active, leading to significant static power dissipation due to the persistent bias currents in the cascoded structures.

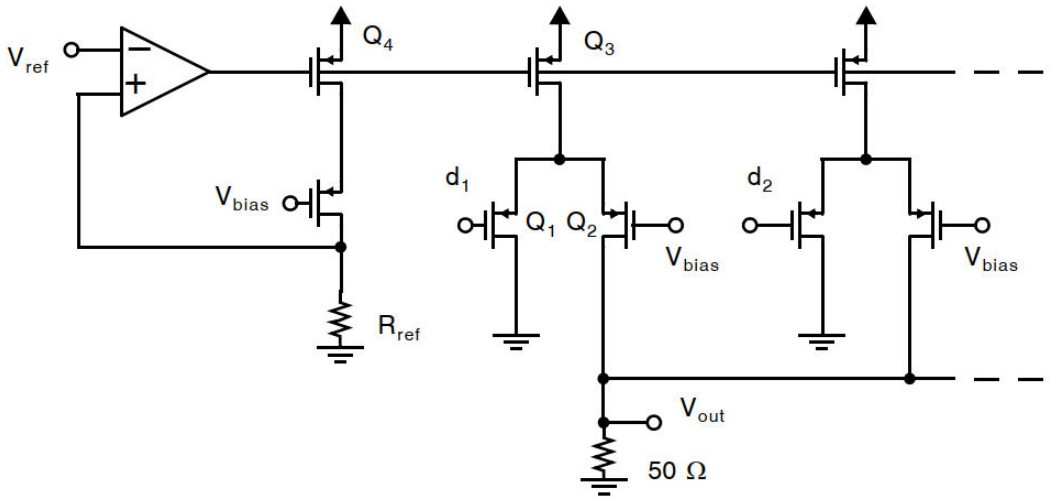


Figure 7.13 Typical schematic of a current–mode converter [25].

Decoder–based DACs can be broadly classified into four main architectures: the resistor–string tree–like decoder, the resistor–string with digital decoder, the folded resistor–string decoder, and the multiple resistor–string decoder [25].

The resistor–string tree–like decoder requires $2^6 = 64$ resistors to generate the voltage division necessary for a 6–bit DAC. In addition, it relies on a large number of switches to route the selected voltage to the output. A key drawback of this approach is that multiple switches are often placed in series along the signal path, which increases both resistive losses and parasitic capacitances, thereby degrading accuracy and speed.

The resistor–string with digital decoder maintains the same number of resistors but reduces losses and improves speed by minimizing the number of series switches. However, this benefit comes at the expense of increased digital complexity, as it requires a 6–to–64

decoder implemented with a large number of logic gates. This significantly increases both area and dynamic power consumption.

To address this limitation, the folded resistor–string architecture can be employed. This approach replaces the large 6–to–64 decoder with two smaller 3–to–8 decoders, thereby substantially reducing both area and dynamic power. This makes it particularly attractive for low–power applications.

Another alternative is the multiple resistor–string architecture, which reduces the number of required resistors by approximately half. While this improves area efficiency and can enhance resolution, it typically requires high–speed Op Amps to combine outputs from multiple strings, leading to increased power consumption. Furthermore, in the context of the proposed design, additional comparators are introduced to enable simultaneous operation at a low supply (V_{DDL}) while maintaining a high reference voltage (V_{DDH}). Incorporating these comparators into a multiple resistor–string architecture would lead to a significant increase in their number due to the cascaded structure, resulting in excessive area and power consumption.

To balance area, power efficiency, and architectural flexibility, including the integration of slewed comparators, a modified folded resistor–string DAC is adopted, as shown in **Figure 7.14**. In a typical implementation, this architecture employs 64 switches arranged in a matrix–like structure, analogous to memory arrays. The lower 3–to–8 decoder selects the bit lines, while the left 3–to–8 decoder selects the word lines. For a given digital input, one word line activates a row of switches, while a single bit–line switch connects the appropriate tap of the resistor string to the output. Finally, a buffer is placed at the output to provide isolation and drive capability.

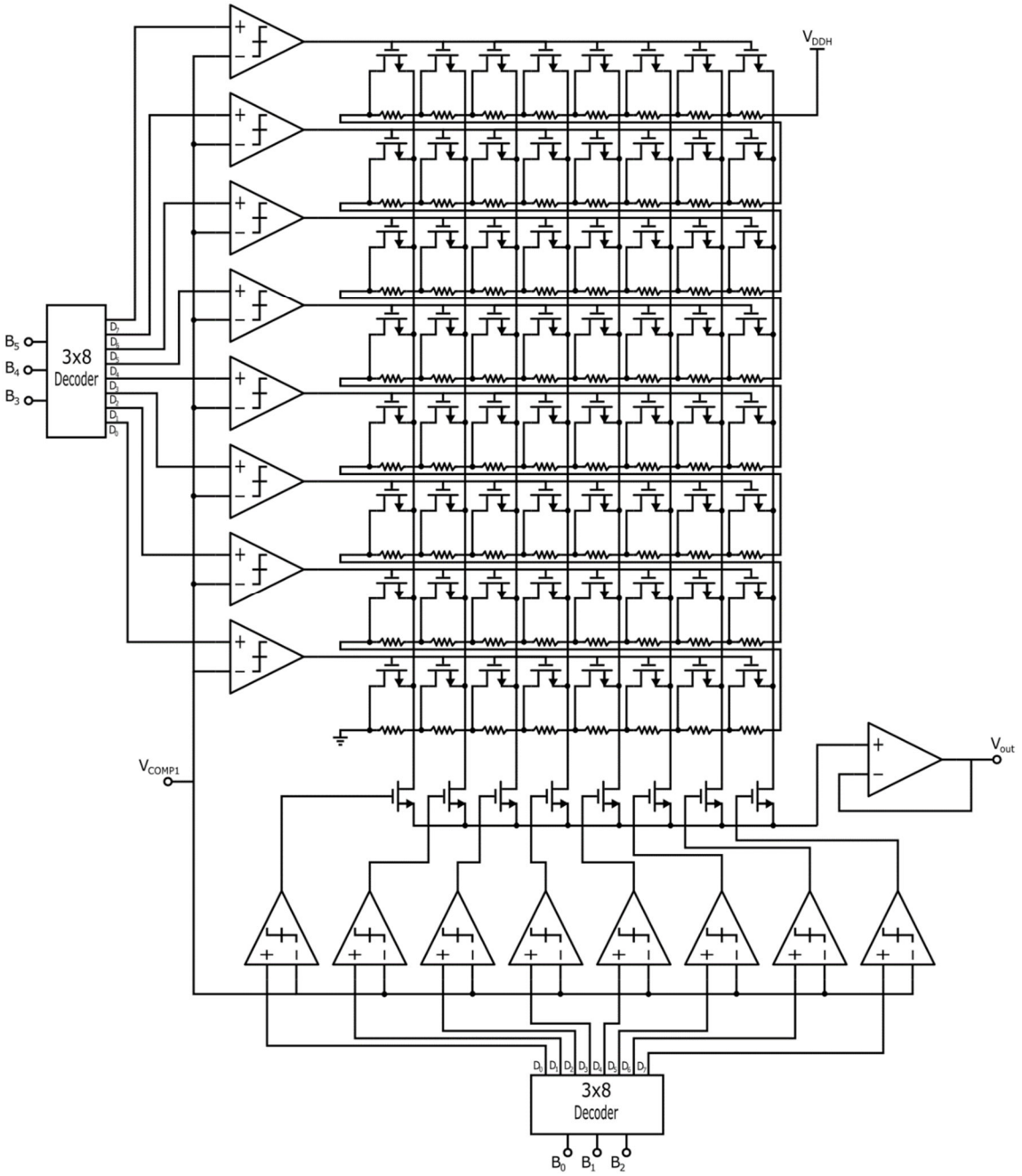


Figure 7.14 Modified folded–resistor string 6–bit DAC.

To optimize both performance and dynamic power consumption, the conventional folded resistor–string DAC architecture was modified. In the proposed design, the reference voltage of the resistor string is connected to V_{DDH} to maximize the output control

range for the RF beam–steering circuits. Meanwhile, the 3–to–8 decoders are powered from V_{DDL} to reduce dynamic power consumption.

However, initial simulations of this configuration revealed incorrect DAC operation. Specifically, the decoder output levels, limited by V_{DDL}, were insufficient to properly drive the switches connected to the resistor string, which operate at the higher voltage V_{DDH}. As a result, some switches failed to turn on reliably. To address this, a level conversion stage was required between the decoders and the switch network.

A first attempt employed two cascaded inverters powered from V_{DDH} to perform level shifting. This approach, however, introduced two major issues. First, the dynamic power consumption increased significantly due to the quadratic dependence on supply voltage, effectively negating the benefits of operating the decoders at V_{DDL}. Second, the switching threshold of the inverters shifted to approximately $V_{DDH}/2$, which exceeded the decoder output levels and prevented proper switching. Attempts to redesign the inverters to lower their switching threshold resulted in impractically large device sizes, which excessively loaded the decoder outputs and degraded signal integrity.

To overcome these limitations, low–power comparators were introduced, as shown in **Figure 7.14**. These comparators are powered from V_{DDH} and serve as level converters, producing rail–to–rail control signals suitable for driving the switches. They are designed with a wide ICMR, allowing operation with low input voltages (below V_{DDL}) and enabling the use of a reference voltage V_{COMP1} generated from the low–voltage regulator. During switching events, the comparators operate in a slew–limited regime, restricting the current used to charge and discharge parasitic capacitances at the switch nodes. This behavior significantly reduces dynamic power consumption while maintaining correct functionality.

A simulation comparison between the conventional and proposed design is presented in **Figure 7.15**. In the conventional implementation, both the resistor string and decoders are powered from V_{DDH}, and no comparators are used. In contrast, the proposed design powers the resistor string and comparators from V_{DDH}, while the decoders operate at V_{DDL}. As shown in **Figure 7.15**(a) and (c), both designs produce correct DAC outputs under full switching activity at 4 kilo samples per second. However, the conventional design exhibits

a peak current of approximately 6 mA per conversion, which is prohibitively high for WPT applications. In comparison, the proposed design requires only about 180 μA from V_{DDH} and 50–80 μA from V_{DDL}, demonstrating a substantial reduction in dynamic power consumption. Although the inclusion of comparators increases the static current to approximately 200 μA, the overall power savings are dominated by the significant reduction in dynamic consumption.

Finally, the design of the switching elements was investigated. Four options were considered: standard NMOS, low–voltage–threshold (LVT) NMOS, native NMOS, and transmission–gate–based switches. The transmission–gate option was excluded due to the requirement of complementary control signals, which would necessitate an additional inverter per switch (64 inverters per DAC), leading to excessive dynamic power consumption.

The remaining three options were evaluated, and their output characteristics are shown in **Figure 7.16**. All three exhibit similar performance across most input codes; however, differences become apparent at higher output levels. Standard NMOS switches suffer from increased voltage drop due to their relatively high threshold voltage, limiting the achievable output range. Both LVT and native devices improve this behavior due to their lower threshold voltages. While native transistors achieve the highest output voltage, they exhibit poor robustness under PVT variations, with threshold voltages dropping to approximately 2 mV under high–temperature (100 °C) and fast–corner conditions, significantly degrading DAC performance.

For this reason, LVT NMOS devices were selected as the switching elements, providing an optimal trade–off between output range, robustness, and reliable operation across PVT variations.

7.5 Sub–IC Interface Simulations

Having described the key building blocks of the IC, we now proceed to their integration and system–level validation through post–layout simulations. This step is essential to verify the proper interaction between subsystems under realistic operating conditions.

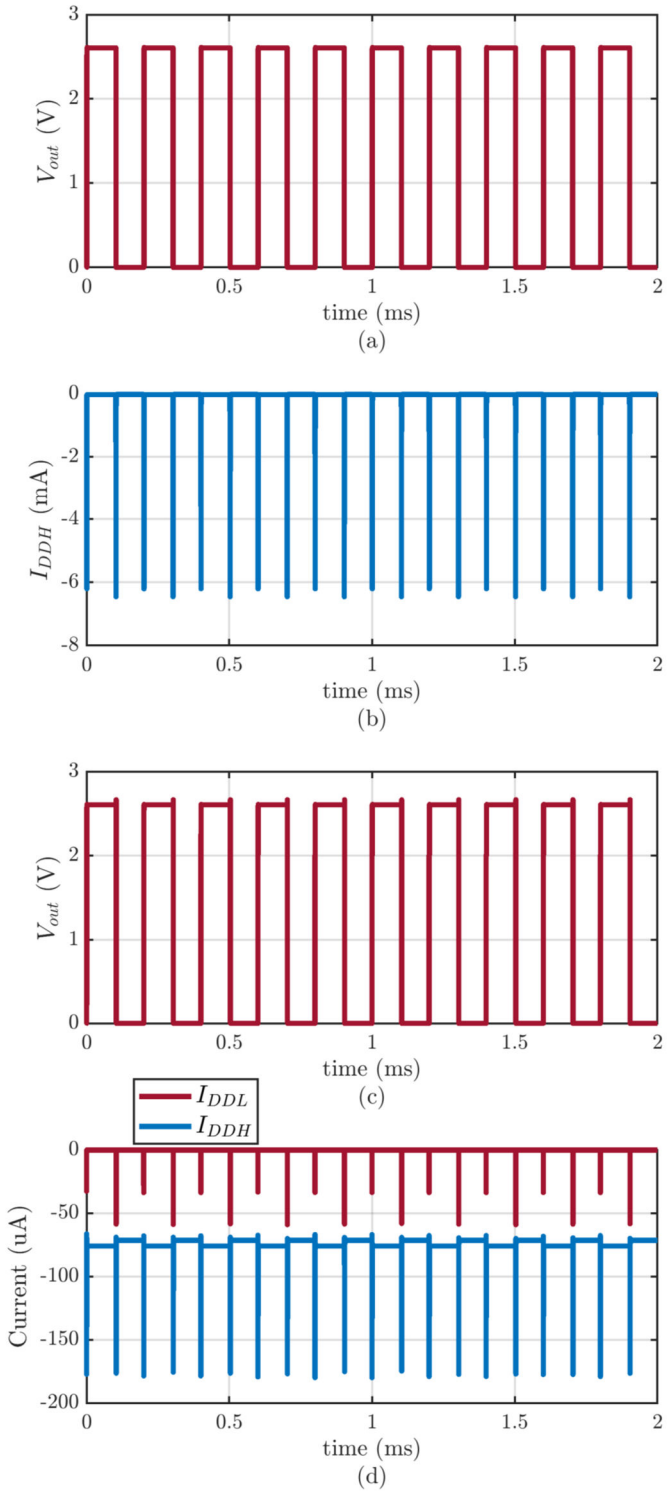


Figure 7.15 Simulation comparison between typical and modified folded resistor string DACs showing: (a) V_{out} of typical design, (b) I_{DDH} of typical design, (c) V_{out} of modified design, (d) I_{DDL} (red) and I_{DDH} (blue) of modified design.

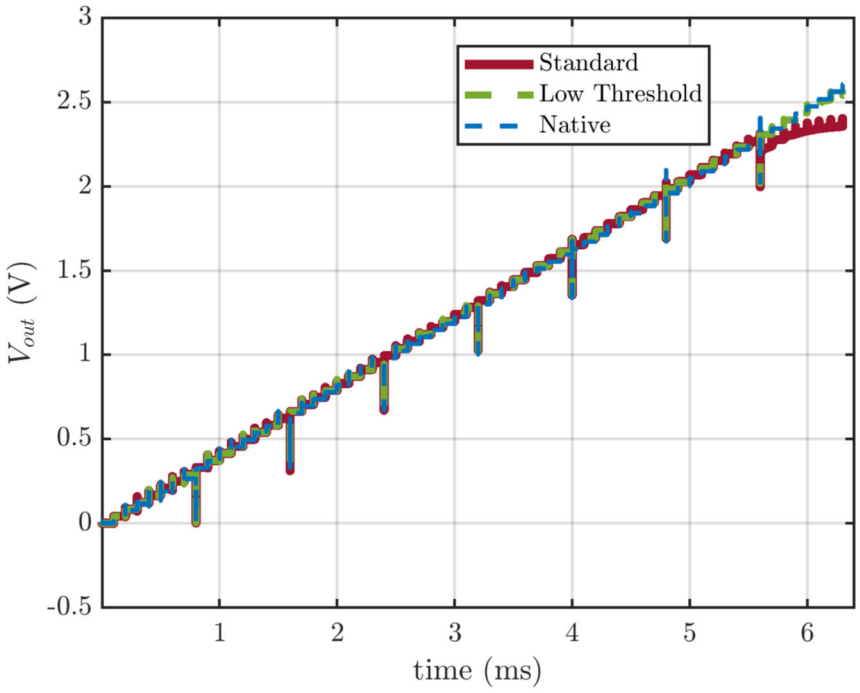


Figure 7.16 Output voltage of the modified folded–resistor string DAC for different switch implementations: standard (red), low threshold (green), and native (blue) transistors.

We begin by examining the integration of the RF rectifier and power conditioning circuitry with the ASK demodulator. This simulation validates the ability to reliably power up the control block and support data demodulation. Subsequently, the integration of the communication block with the digital control circuitry is presented, validating correct demodulation, decoding, digital frame routing, and control functionality at the IC level.

7.5.1 Power management with ASK demodulator interface

A testbench demonstrating the integration of the RF rectifier, bandgap references, voltage regulators, and the ASK demodulator is shown in **Figure 7.17**. A 2 nH series inductance is included at the RF input to model the bond–wire inductance. This value is based on an estimated inductance of approximately 1 nH/mm and a bond–wire length of about 2 mm for a 40–pin package.

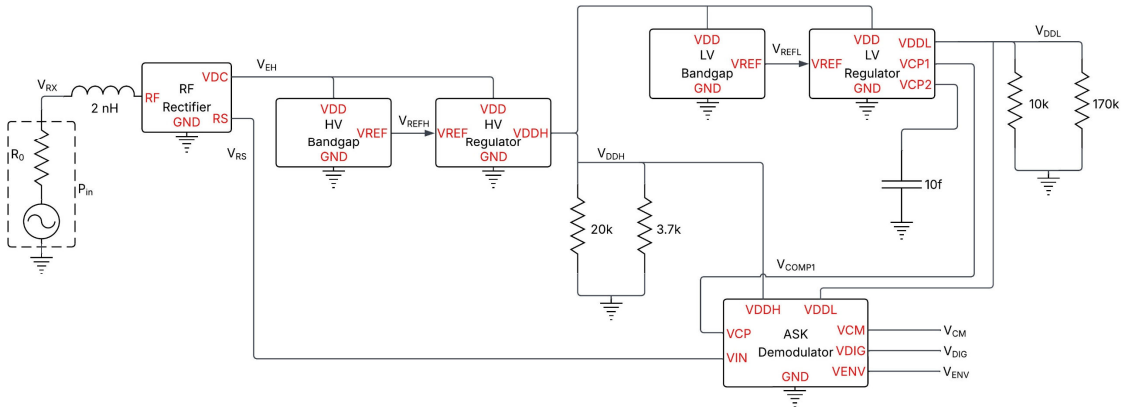


Figure 7.17 Testbench of the power management unit with the ASK demodulator.

The RF rectifier converts the incoming RF signal into a harvested DC voltage V_{EH}, which supplies the high–voltage (HV) bandgap and regulator blocks. The RS node of the rectifier provides access to the resonant RF voltage, which is used as the input V_{IN} to the ASK demodulator.

The HV regulator generates V_{DDH}, which in turn powers the low–voltage (LV) bandgap and regulator to produce V_{DDL}. To emulate realistic loading conditions, the analog block current consumption is modeled using a 3.7 kΩ resistive load connected to V_{DDH}. Additionally, a 20 kΩ resistor is included in parallel as a start–up load to facilitate proper regulator initialization and ensure reliable voltage convergence during the transient phase of the RF rectifier. Similarly, for the LV domain, a 170 kΩ resistive load is used to model the digital block consumption. A 10 kΩ shunt resistor is added to improve start–up behavior.

The ASK demodulator is powered by dual supply domains, where V_{DDH} is used to supply the Op Amp, while V_{DDL} supplies the comparator. V_{COMP1} is generated through a resistive divider from V_{DDL} to establish the comparison threshold for the comparator. The demodulator provides access to the internal nodes V_{ENV}, V_{CM}, and V_{DIG}, which are used to verify the envelope detection, common–mode or average envelope level, and recovered digital data of the ASK signal, respectively.

The simulated waveforms corresponding to this testbench are shown in **Figure 7.18**. V_{RX} represents the received RF voltage, which is delivered to the rectifier and, after passing

through L_M, produces the resonant voltage V_{RS}. The rectifier converts this signal into the harvested voltage V_{EH}, which exhibits amplitude modulation due to the ASK signal and therefore does not provide a stable supply. This harvested voltage is then regulated to generate V_{DDH} and V_{DDL}, both of which remain well stabilized, confirming the effectiveness of the power management circuitry. In parallel, V_{RS} is processed by the ASK demodulator to generate the envelope V_{ENV}. Furthermore, V_{CM} accurately tracks the average of V_{ENV}, enabling reliable thresholding and generation of the digital output V_{DIG} through the referenced comparator.

7.5.2 Communication with digital control interface

To validate the integration of the communication circuitry with the digital frame router and DACs, a dedicated testbench is developed, as shown in **Figure 7.19**. The testbench includes an ASK–PWM generator that provides the modulated input signal, followed by an ASK demodulator that recovers the clock, and a PWM decoder that extracts the data stream. These signals are then processed by the modified digital frame router, which incorporates increased bit resolution and attenuator control functionality, and interfaces with the DAC blocks to generate the corresponding analog control signals. The corresponding transient simulation results are presented in **Figure 7.20**, demonstrating the complete signal flow from ASK–PWM demodulation and decoding to analog control generation.

To validate functionality, four distinct control samples were transmitted and successfully acknowledged, as indicated by the ACK signal. The RCD signal marks the temporary storage of incoming data within the data holder, while the RST signal clears the shift register once the data has been latched. In this simulation, the transmitted control samples sequentially address all cells of control block 1.

Finally, the resulting analog control voltages generated by the DACs are shown in the figure, confirming correct decoding, routing, and digital–to–analog conversion across all control channels.

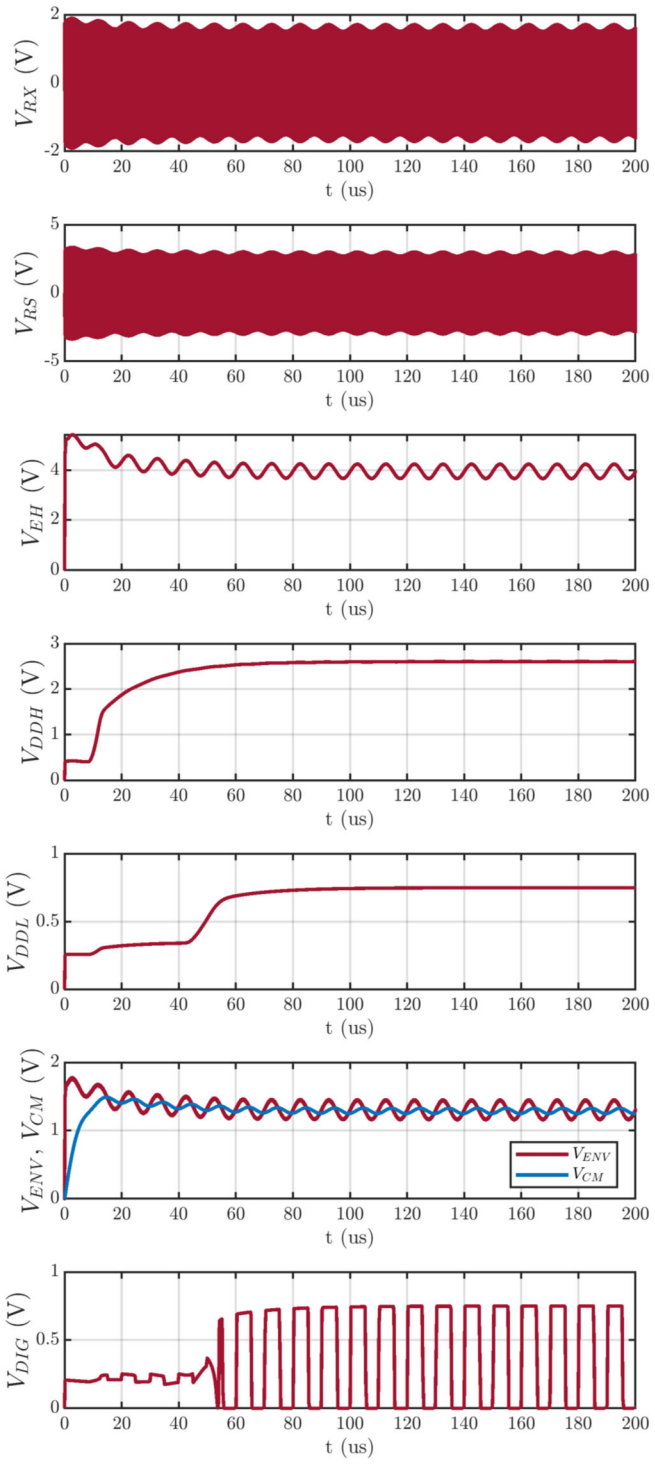


Figure 7.18 Waveform simulations of the testbench in **Figure 7.17**.

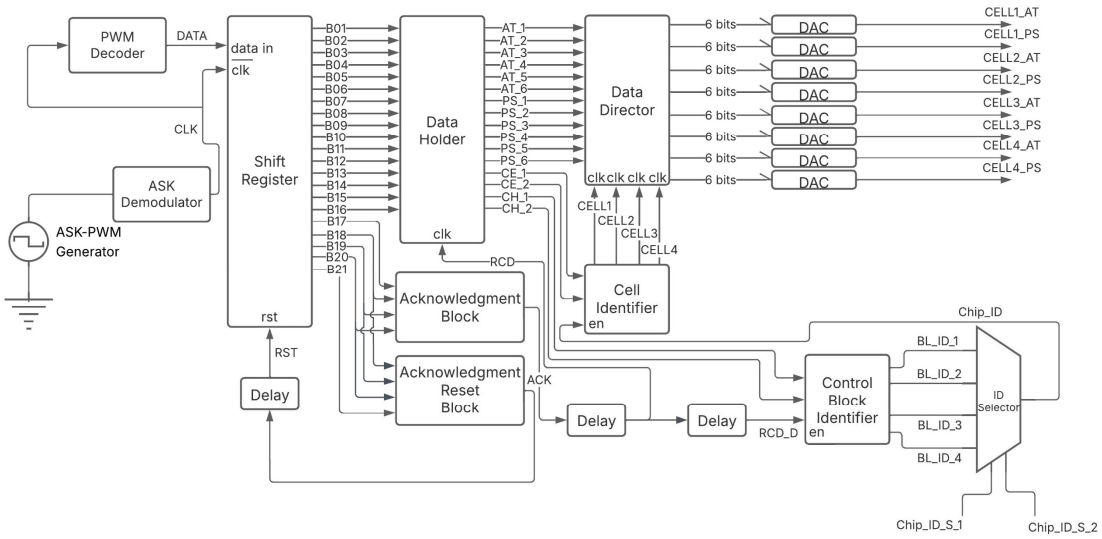


Figure 7.19 Testbench of the communication and control blocks.

The operation of the control block ID selector and the corresponding ID encoding within the control samples was also verified. The results confirm that the generated control voltages are routed to the intended control block only when the ID bits embedded in the transmitted sample match those of the ID selector. In cases of mismatch, the received data are ignored, ensuring that control signals are applied exclusively to the targeted IC.

7.6 IC Testing and Debugging

The presented subblocks, namely the RF rectifier, power management circuitry (including the bandgap references and voltage regulators), ASK demodulator, PWM decoder, digital frame router, and DACs, have been integrated and taped out in a single IC, as shown in **Figure 7.21**. The chip was implemented in TSMC 130 nm general–purpose CMOS technology and occupies an area of 2 mm × 1.8 mm.

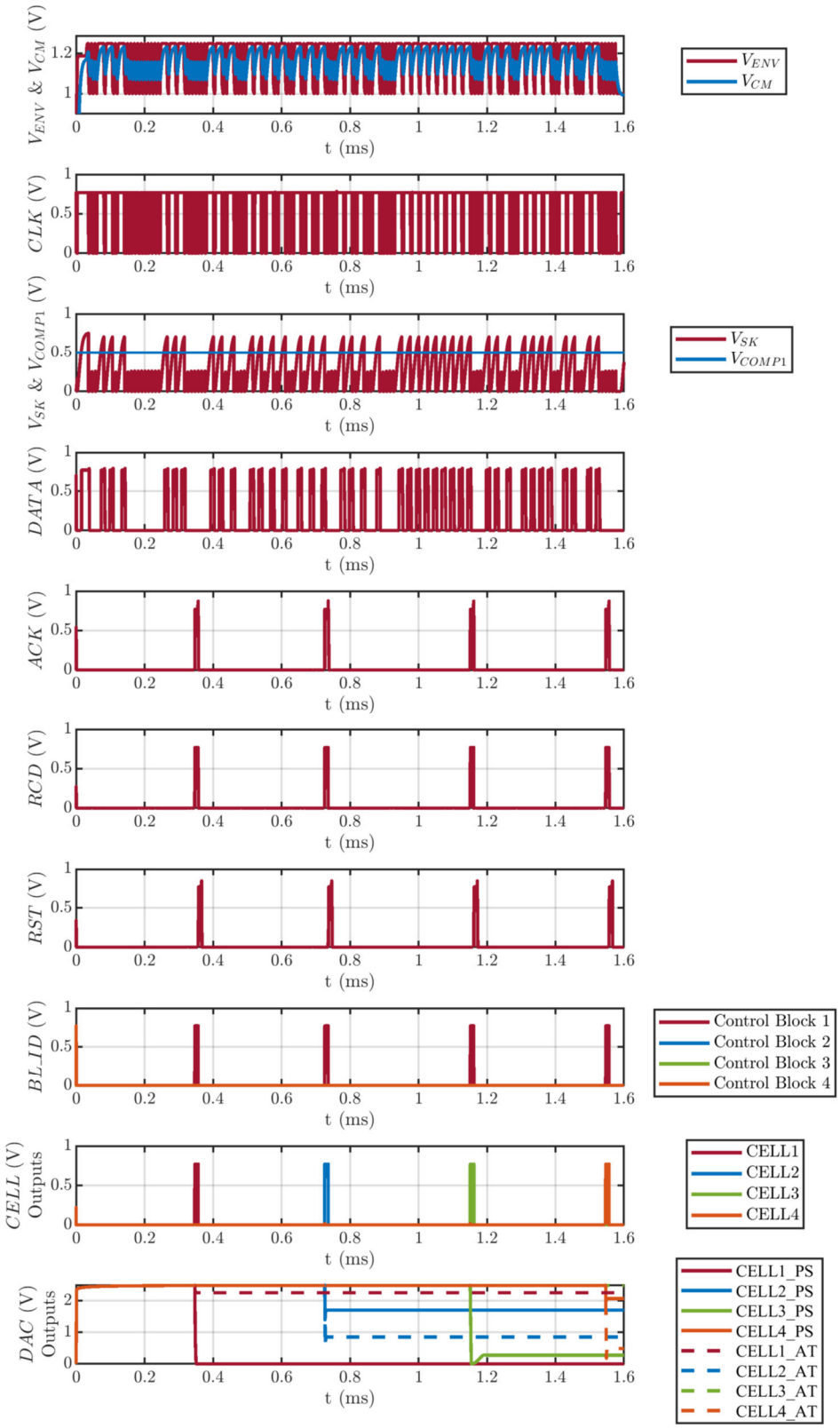


Figure 7.20 Waveform simulations of the testbench in **Figure 7.19**.

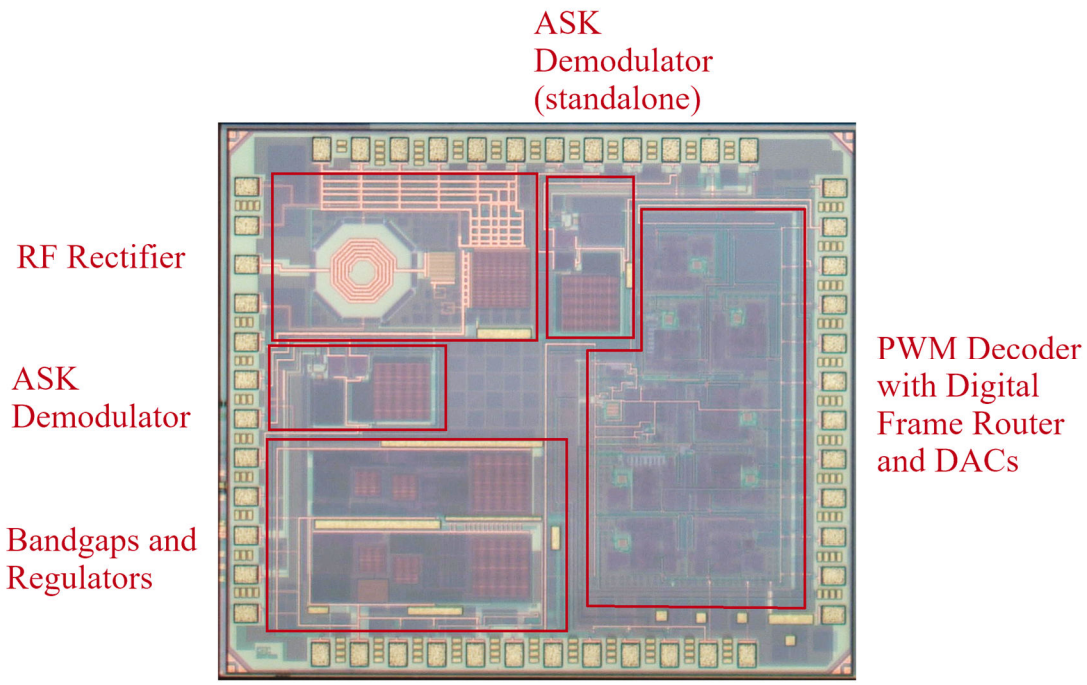


Figure 7.21 Micrograph of the fabricated IC in TSMC 130 nm CMOS technology, highlighting the integrated subblocks.

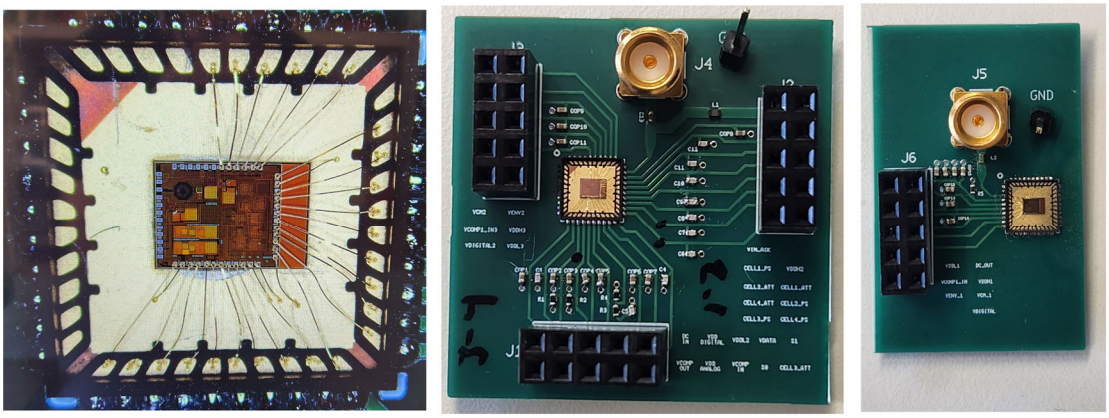
The overall system is conceptually intended to operate as a single–input–pad solution, where RF power, data and clock are received through a unified interface. However, to improve measurement flexibility and reduce debugging complexity in this first tapeout, a modular testing approach was adopted. As a result, the critical functional blocks are partially decoupled and made accessible through a 48–pad padframe, enabling standalone characterization and validation of individual subsystems before full system integration.

The RF rectifier and ASK demodulator are located in the upper–left region of the die and are directly interconnected to enable evaluation of the interface between harvesting and communication paths. In addition, a standalone ASK demodulator is implemented at the top side of the IC, allowing independent characterization and validation without the influence of the harvesting rectifier stage. This redundancy is particularly useful for isolating performance limitations during measurements.

The bandgap references and voltage regulators are placed in the lower–left portion of the die, providing stable biasing and supply voltages for analog, digital, and mixed–signal blocks. Their standalone accessibility enables direct verification of regulation performance under controlled conditions.

On the right–hand side, the IC integrates the PWM decoder and digital frame router, along with the associated DACs. This digital subsystem is physically separated from sensitive analog blocks to minimize coupling and interference, while also allowing independent functional testing through dedicated pads.

The fabricated ICs were packaged in a 40–lead, 6×6 mm open–cavity Quad Flat No–leads (QFN) package with castellated leads, as shown in **Figure 7.22**(a). The exposed leadframe paddle (die attach pad) is connected to a conductive backplane and serves as the primary ground reference. The die was attached to the paddle using silver epoxy, while gold wire bonds were used to connect all non–ground pads to the corresponding package leads. Grounding was achieved by directly bonding the IC ground pads to the exposed paddle.



(a) (b) (c)

Figure 7.22 IC packaging and test boards showing: (a) the 40–lead, 6×6 mm open–cavity QFN–packaged die, (b) the test platform for power management, ASK demodulator, and PWM decoder with digital frame router and DACs, and (c) the RF test platform for rectifier and ASK demodulator characterization.

To accommodate the limited number of package pins and enable flexible debugging, two distinct wire bonding configurations were implemented, resulting in two dedicated test boards.

The first test platform, shown in **Figure 7.22**(b), is designed to evaluate the bandgap references and voltage regulators, the PWM decoder and digital frame router with DACs, and the ASK demodulator.

All supply nodes are decoupled using 100 pF capacitors to suppress supply noise. Larger decoupling capacitors were avoided to prevent degradation of the phase margin and stability of the LDO regulators. For load emulation, a 3 kΩ resistor is connected to V_{DDH}, while a 100 kΩ resistor is used for V_{DDL}. The input to the PWM decoder is driven from an FPGA and scaled using a resistive voltage divider (10 kΩ / 10 kΩ) to reduce the 1.5 V logic level to 0.75 V, matching the V_{DDL} domain. In addition, a 1 pF capacitor is placed at the input to mitigate transient current spikes during switching.

Each DAC output is loaded with a 1 pF capacitor, representing a light capacitive load while approximating the expected loading from varactors (< 2 pF for the reflective phase shifters in Subsection 5.3.3). An SMA connector is used to feed the ASK demodulator input with a 2.4 GHz RF signal modulated at 100 kHz.

To support flexible biasing for the ASK demodulator, a 15 μH inductor and a 100 nF capacitor are included for optional bias decoupling. The demodulator's intermediate outputs, V_{ENV} and V_{CM}, are intentionally left unloaded to avoid capacitive loading. All supply pins associated with the ASK demodulator, PWM decoder, frame router, and DACs are decoupled with 100 pF capacitors.

The second test platform, shown in **Figure 7.22**(c), is dedicated to RF rectifier characterization and its interface with the ASK demodulator.

An SMA connector is used to inject a 2.4 GHz RF signal at 11.5 dBm, modulated with a 100 kHz ASK waveform. The rectifier output is loaded with a 4 kΩ resistor to maintain consistent loading conditions. To minimize supply noise and ripple during measurement, five parallel 100 pF decoupling capacitors are employed.

Similarly, all supply lines associated with the ASK demodulator are decoupled using 100 pF capacitors to ensure stable operation and reduce measurement noise.

Both test boards were fabricated on FR–4 substrates with a thickness of 0.6 mm. All RF traces were carefully designed to achieve 50 Ω characteristic impedance and are exclusively interfaced using SMA connectors to maintain signal integrity at GHz frequencies. Multiple pin headers are distributed across the boards to provide flexible access for power supply connections, digital signal injection (e.g., FPGA interface), and probed measurement of internal nodes.

7.6.1 Bandgap references and voltage regulators testing

Figure 7.23 shows the experimental setup used to characterize the bandgap references and voltage regulators. A DC power supply is used to emulate the harvested input voltage V_{EH}, while a digital multimeter monitors the regulated outputs. The IC test board is interfaced through a breadboard to allow flexible probing. Care was taken to ensure stable measurements by using short connections and proper grounding. The regulated outputs V_{DDH}, V_{DDL}, and the comparator reference voltage V_{COMP1} were measured across a range of input supply voltages. Due to limited packaging pads, the secondary comparator reference V_{COMP2} was not accessible during testing, and V_{COMP1} was used for characterization and voltage referencing.

Figure 7.24 presents the measured and simulated outputs of the power management circuitry as a function of the input supply voltage. Overall, a strong agreement between simulation and measurement is observed, validating the bandgaps, and regulators design.

At low input voltages ($<$0.6 V), all outputs remain near zero, indicating that the circuits are below their startup threshold. As the supply voltage increases, the bandgap reference begins to function properly, enabling the regulators to turn on. Around 0.7 V, a sharp transition is observed where all regulated outputs rise rapidly toward their nominal values.

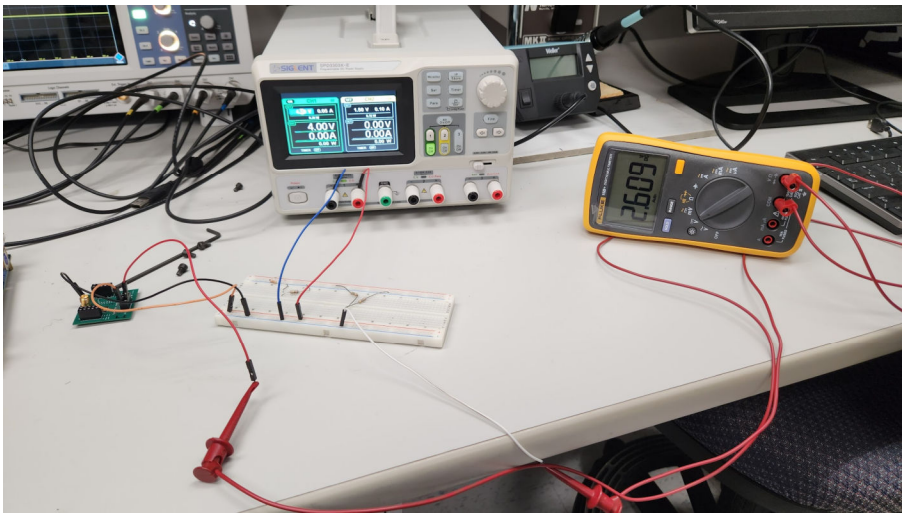


Figure 7.23 Experimental setup for bandgap references and voltage regulators characterization.

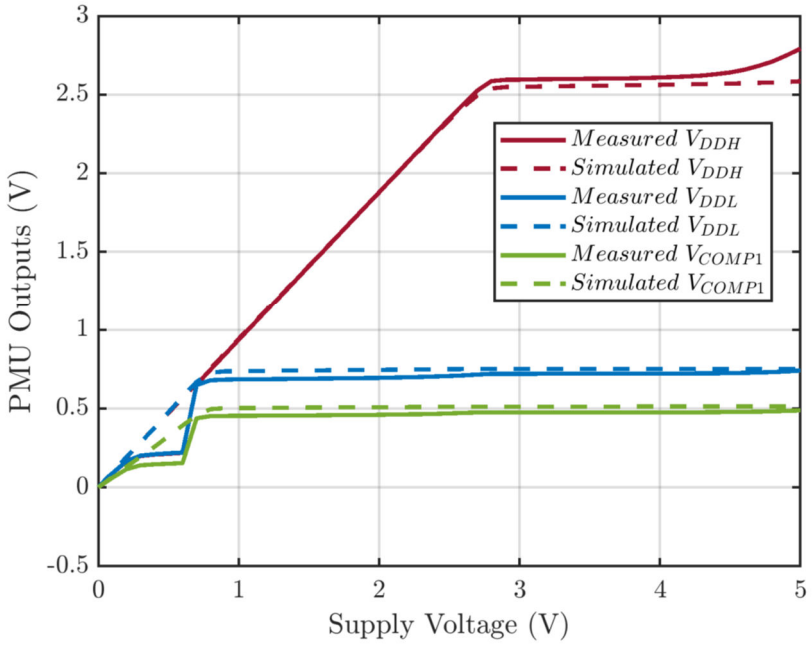


Figure 7.24 Measured (solid) and simulated (dash) PMU output voltages V_{DDH} (red), V_{DDL} (blue), and V_{COMP1} (green) as a function of input supply voltage.

The low–voltage regulator output V_{DDL} stabilizes around 0.7–0.75 V, closely matching the simulated value of 0.75 V. Similarly, the comparator reference voltage V_{COMP1} settles in the range of 0.45–0.49 V, with minimal deviation from the expected value of 0.5 V. These

results confirm proper operation of the low–voltage bandgap reference, voltage regulator and their derived reference network.

The high–voltage regulator output V_{DDH} increases with the supply voltage until it reaches a regulated plateau around 2.6 V. Beyond this point, a slight upward slope is observed in the measured curve, which can be attributed to transistor's breakdown, rather than ideal voltage clamping.

Since the target operating condition corresponds to $V_{EH} \approx 4$ V, this region is of primary interest. At this input voltage:

- $V_{DDH} = 2.609$ V (vs. 2.58 V simulated)
- $V_{DDL} = 0.722$ V (vs. 0.75 V simulated)
- $V_{COMP1} = 0.47$ V (vs. 0.513 V simulated)

These values closely match the simulated results, confirming that the PMU provides stable and predictable biasing conditions for the rest of the system under nominal operation.

Figure 7.25 shows the startup behavior of the PMU as the input supply voltage is ramped over time. Initially, all outputs remain near zero until the supply voltage reaches approximately 0.6–0.7 V, at which point the bandgap reference activates and enables the regulation stages.

Following startup, both regulated outputs rise rapidly:

- V_{DDL} settles to approximately 0.72 V
- V_{DDH} settles to approximately 2.6 V

The outputs exhibit a fast–settling time with no overshoot or oscillation, indicating stable loop behavior. Once the supply reaches its final value (4 V), both regulated outputs remain stable with negligible variation.

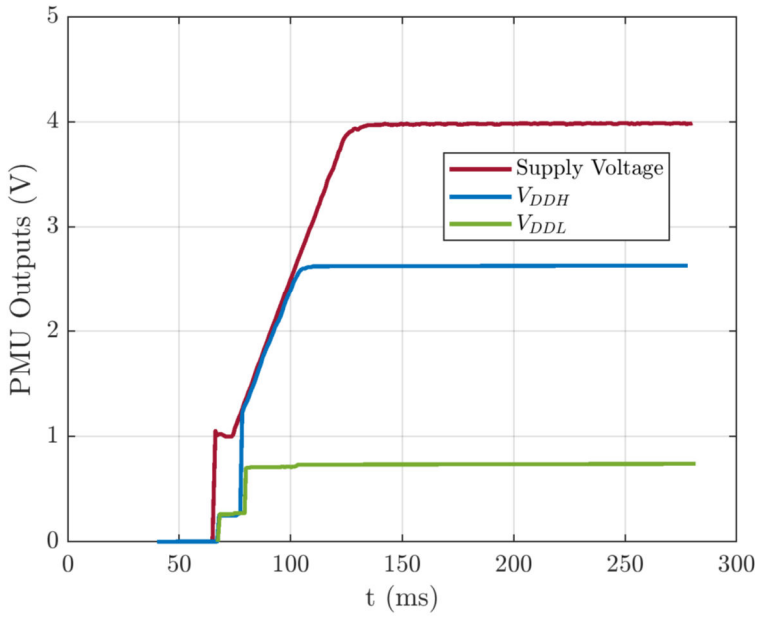


Figure 7.25 Measured startup transient of the PMU, showing V_{DDH} and V_{DDL} as the input supply ramps to its steady–state value.

7.6.2 ASK demodulator testing

We now move to the standalone characterization and debugging of the ASK demodulator, as shown in **Figure 7.26**. An RF signal generator, specifically the Rohde & Schwarz SME 06 signal generator (top right), was used to generate the input signal. A 10 dBm carrier at 2.4 GHz with 100 kHz amplitude modulation was applied to emulate the ASK component of the ASK–PWM scheme.

The demodulator was biased using external DC supplies. A supply of 2.6 V was applied to V_{DDH} for the differential amplifier following the envelope detector and dynamic reference generator, while 0.75 V was used for V_{DDL} to power the comparator stage. In addition, a 0.42 V reference voltage was provided to the comparator to establish the detection threshold.

The output signals of the ASK demodulator were monitored using a digital oscilloscope, namely the Keysight InfiniiVision Oscilloscope (bottom left). This enabled real–time observation of the recovered envelope, generated common–mode and digital output signals, allowing verification of correct ASK demodulation.

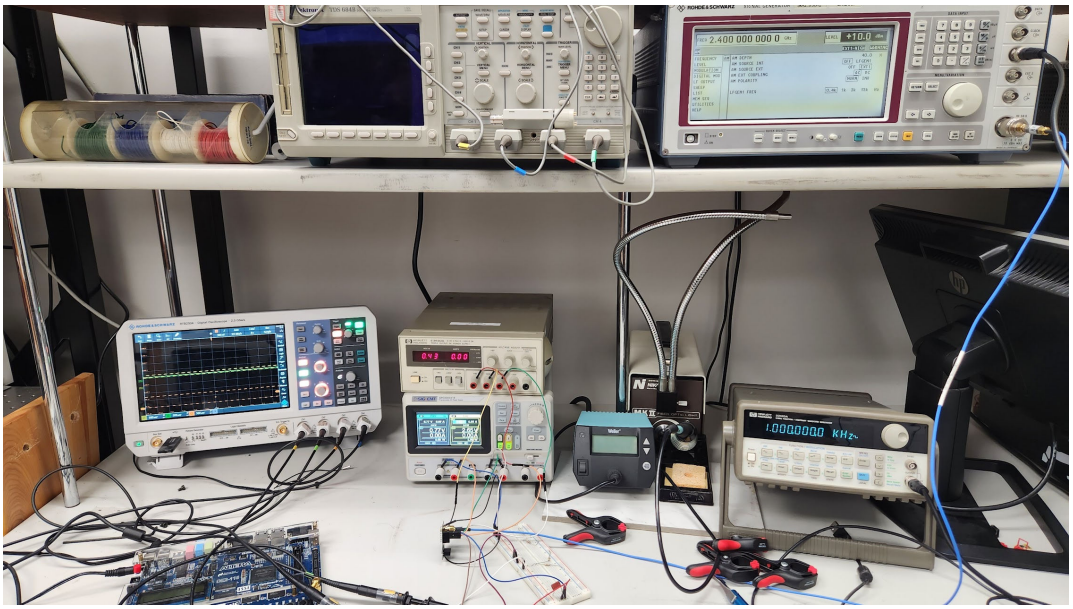


Figure 7.26 Experimental setup for standalone characterization of the ASK demodulator.

Figure 7.27 shows the extracted envelope voltage V_{ENV} and common–mode voltage V_{CM} of the ASK demodulator. The measured results are presented in **Figure 7.27**(a), while the corresponding post–layout simulation results are shown in **Figure 7.27**(b).

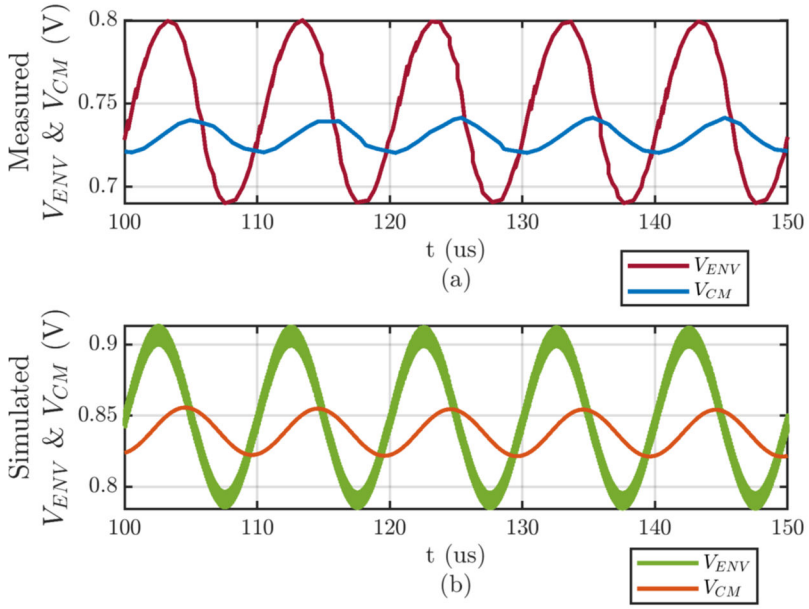


Figure 7.27 Waveform results of intermediate nodes in the ASK demodulator showing: (a) Measured V_{ENV} (red) and V_{CM} (blue), and (b) Simulated post–layout V_{ENV} (green) and V_{CM} (orange).

A strong agreement between measurement and simulation is observed. The envelope signal V_{ENV} clearly follows the applied 100 kHz modulation, demonstrating correct operation of the envelope detection stage. The waveform shape, amplitude, and frequency closely match the simulated response, confirming that the demodulator accurately recovers the baseband signal from the RF input.

The common–mode voltage V_{CM} also exhibits the expected behavior, tracking a relatively stable bias level with small signal variation. In the measured results, V_{CM} is slightly lower than in simulation. This discrepancy is attributed to loading effects from the oscilloscope probe, which introduces additional capacitance and slightly perturbs the bias point.

Figure 7.28(a) shows the measured output of the comparator (solid red) compared to the expected simulated response (dashed blue). Ideally, the comparator output should exhibit a clean square waveform. However, the measured signal appears as an attenuated and smoothed version of the envelope signal V_{ENV}, indicating degraded switching behavior.

To investigate this discrepancy, the modulation frequency was reduced from 100 kHz to 1 kHz, as shown in **Figure 7.28**(b). Under these conditions, the measured output more closely resembles the expected square waveform, suggesting that the issue is frequency–dependent and likely related to bandwidth or drive limitations.

Initially, this behavior was suspected to be caused by measurement loading. The first oscilloscope used (the InfiniiVision oscilloscope) presents an input capacitance on the order of 10 pF, which can significantly load low–power analog nodes. To mitigate this effect, measurements were repeated using a higher–performance oscilloscope, namely the Tektronix TDS 684B, which provides reduced effective loading, resulting in improved waveform fidelity at 100 kHz, as illustrated in the solid red waveform in **Figure 7.28(**c).

Despite this improvement, the output still exhibits noticeable slew asymmetry and skew, particularly during the discharge phase. To further understand this behavior, additional post–layout simulations were performed, incorporating 2 pF of capacitive loading (accounting for probe capacitance and parasitics), along with adjusted common–mode bias conditions to reflect measurement observations. These simulations successfully

reproduced the measured waveform characteristics, as shown in the dashed blue lines in **Figure 7.28**(c), confirming that the observed distortion is not a measurement artifact alone, but a circuit–level limitation.

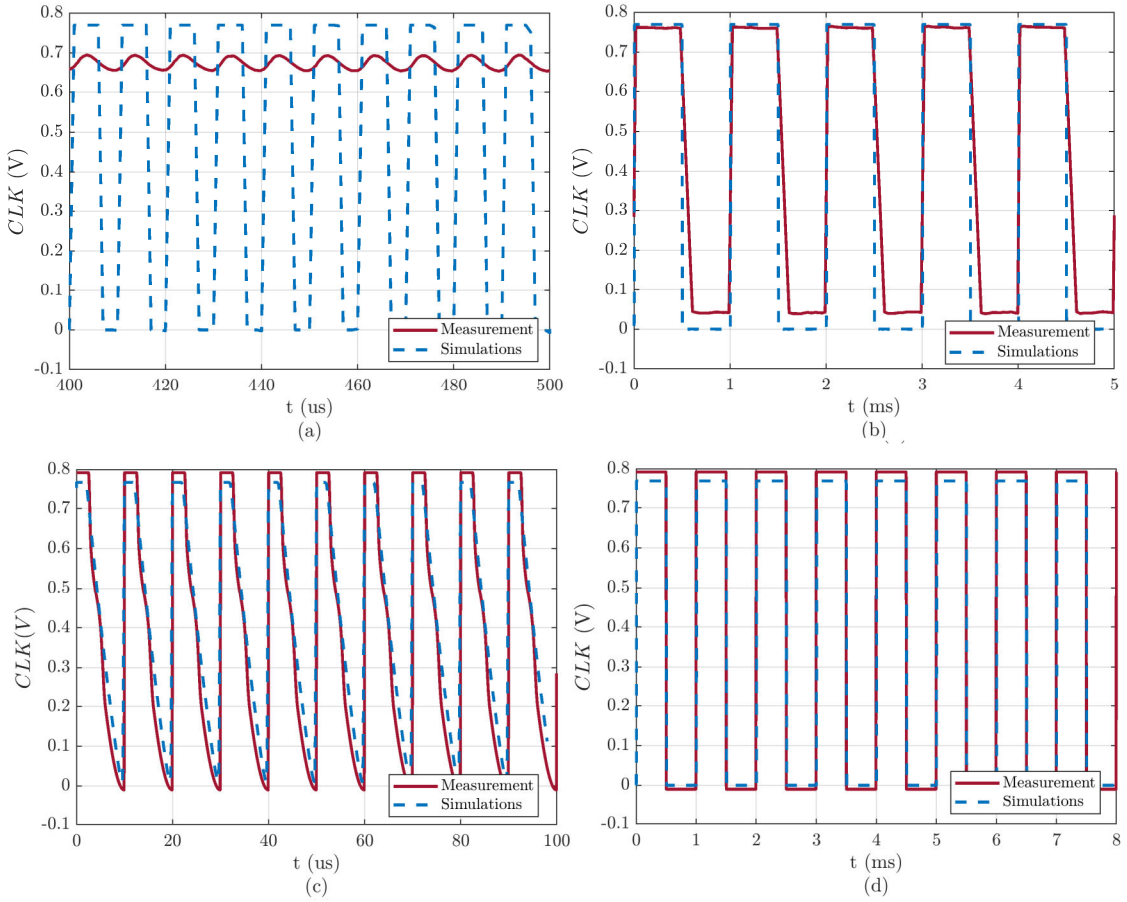


Figure 7.28 Comparator output *CLK* measurement (solid red) vs. post–layout simulation (dashed blue) at: (a) 100 kHz with improper probe loading, (b) 1 kHz with improper probe loading, (c) 100 kHz with reduced probe loading and equivalent capacitive–load model simulation, and (d) 1 kHz with reduced probe loading and equivalent capacitive–load model simulation.

The root cause is attributed to the limited drive strength and bandwidth of the comparator, which was intentionally designed for low–power operation in energy harvesting applications. The simulated 3–dB bandwidth of the comparator is approximately 112 kHz, which is marginal for processing a 100 kHz square–like signal, whose higher–order harmonics extend well beyond this frequency. As a result, the comparator effectively filters these harmonics, leading to rounded transitions and loss of sharp edges.

Additionally, the relatively weak discharge path contributes to the observed asymmetry, causing slower falling edges and further distortion, as seen in **Figure 7.28**(c).

To validate this conclusion, the system was again tested at 1 kHz modulation, as shown in **Figure 7.28**(d), where excellent agreement between measurement and simulation is achieved. This confirms that the comparator operates correctly within its bandwidth limitations.

These results indicate that the comparator is not sufficiently designed for high–speed switching at 100 kHz under the given loading conditions. While adequate for low–frequency operation, its limited bandwidth and drive capability restrict performance at higher data rates.

This limitation may also impact the operation of subsequent blocks, such as the PWM decoder and digital frame router, which rely on the same comparator architecture. The impact will be described in the next chapter. This issue can be addressed in future tape outs by increasing transistor sizing to improve drive strength and optimizing output stage design for better load driving capability.

7.6.3 PWM decoder, digital frame router and DACs testing

To experimentally validate the digital backend, **Figure 7.29** illustrates the setup used to evaluate the PWM decoder, digital frame router, and DACs. The PWM input pattern was generated using an FPGA development board, identical to the one used in IC simulations, enabling a direct comparison between simulated and measured results.

The IC was biased using external supplies: V_{DDH} for the DACs and their associated comparators, V_{DDL} for the PWM decoder and digital frame router, and a 0.67 V reference for the PWM decoder comparator. The outputs of the DAC channels were monitored using the digital oscilloscope.

Figure 7.30(a) shows the input PWM signal applied to the IC, consisting of a sequence of pulses encoding the data bits. A zoomed–in view highlights the pulse–width variations used for data representation. The signal matches that used in **Figure 7.20** (Subsection 7.5.2), enabling direct comparison.

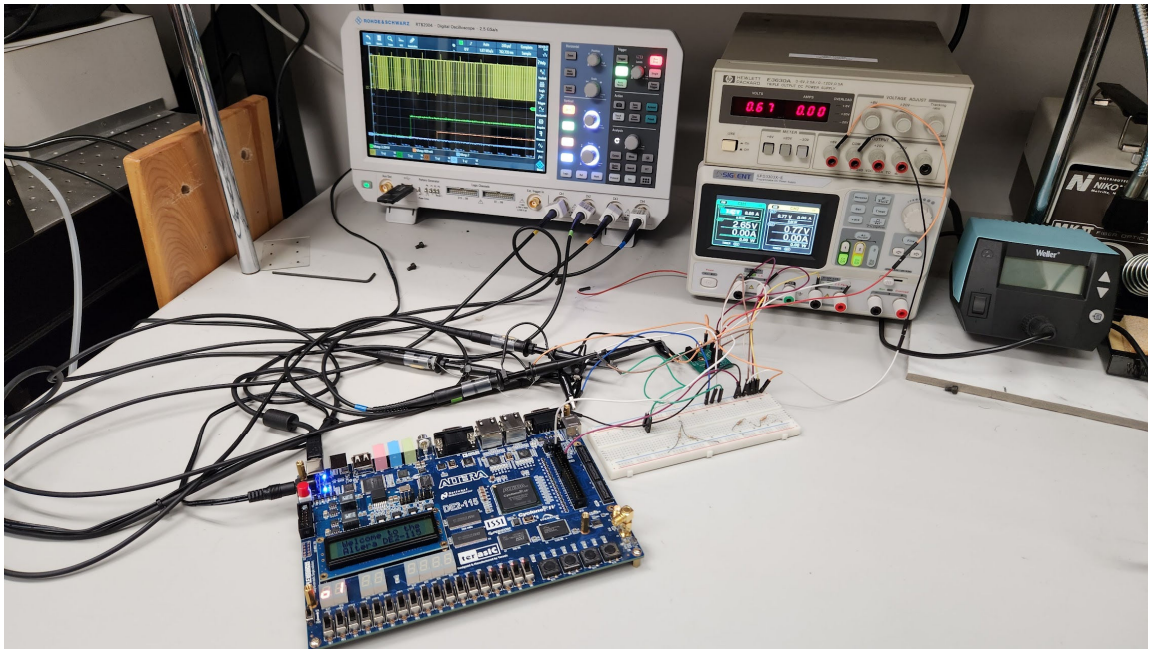


Figure 7.29 Experimental setup for testing the PWM decoder, digital frame router, and DACs.

Figure 7.30(b) and (c) present the outputs of the DACs responsible for phase shifter control (PS1–PS4) and attenuator control (AT1–AT4), respectively, as routed by the digital frame router. The measured signals confirm correct decoding of the input PWM stream, with each control activating at the appropriate time instance. The voltage levels and timing alignment are, for the most part, in close agreement with simulation results, validating the functionality of the PWM decoder and routing logic. Specifically, one exception is observed in AT3, which remains at 0 V instead of toggling as expected. This discrepancy is likely due to a pad–level issue (e.g., faulty or damaged ESD structure) or a soldering/interconnect issue on the test board.

Since the remaining channels operate correctly and match simulation results, the issue is considered localized rather than systemic. The results confirm that the PWM decoding, frame routing, and DAC functionality operate as intended under measured conditions.

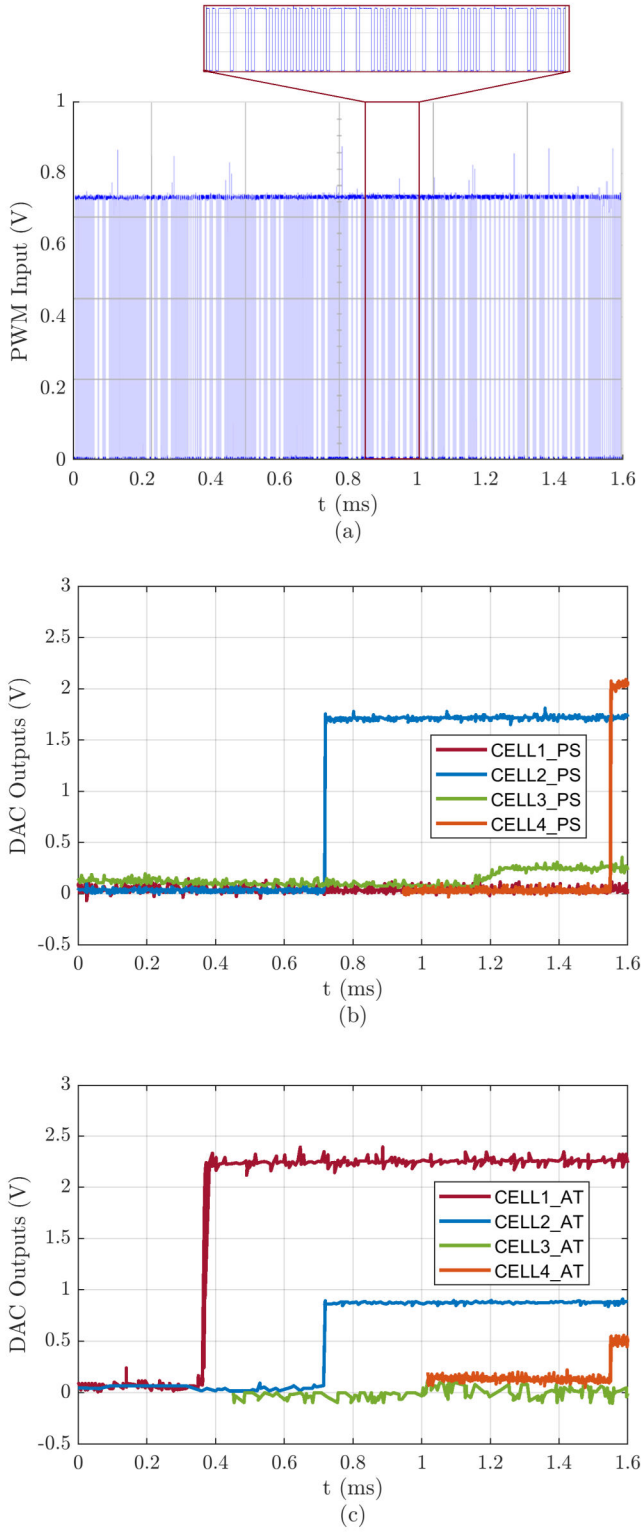


Figure 7.30 Measurement results of the PWM decoder, digital frame router, DACs showing: (a) input PWM signal applied to the IC, (b) measured DAC outputs for each phase shifter's cell, and (c) measured DAC outputs for each attenuator's cell.

It is important to note that five IC samples were tested for the digital frame router, and only one exhibited fully functional operation (more details are provided in Subsection 7.6.5). This behavior is attributed to the comparator design limitations discussed in the previous subsection, particularly its insufficient bandwidth and drive capability. As was shown, the comparator struggles to reliably process the 100 kHz ASK–PWM signal, resulting in degraded or incorrect switching behavior in most samples.

The single functional IC likely represents a favorable process variation case, where device parameters (e.g., threshold voltage, transconductance) enabled the comparator to operate closer to the required performance margin. In contrast, the remaining samples did not meet the necessary speed and drive requirements, resulting in improper decoding.

7.6.4 RF rectifier and ASK demodulator interface testing

Finally, the interface between the harvesting and communication paths on the IC is experimentally evaluated. **Figure 7.31** illustrates the setup used to characterize the RF rectifier and its interaction with the ASK demodulator. The RF input signal is generated using the signal generator and applied to the IC via an SMA connection, while the rectifier output is monitored using a digital oscilloscope.

The input signal was configured to operate near the intended 2.4 GHz carrier frequency, with power levels swept up to 19 dBm to evaluate the rectifier performance under strong excitation conditions. The goal of this measurement was to verify the ability of the rectifier to generate a sufficiently high DC voltage V_{EH} to power the subsequent blocks.

The measured rectifier output is shown in **Figure 7.32**. Contrary to expectations, the harvested DC voltage was limited to approximately 0.42 V at an input power of 19 dBm, which is significantly lower than the expected 4 V at 11.5 dBm predicted by simulations. This indicates a substantial degradation in rectifier performance.

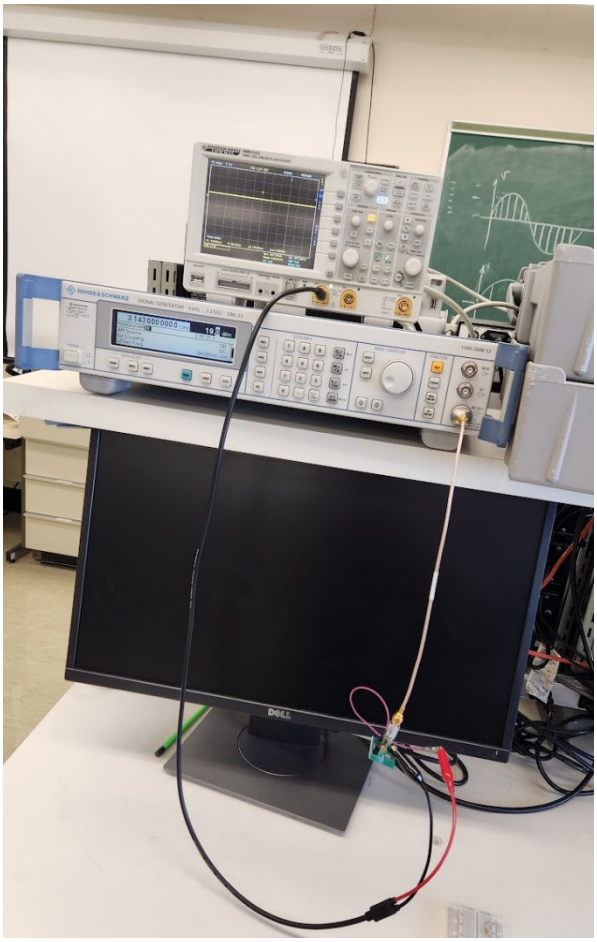


Figure 7.31 Experimental setup for evaluating the RF rectifier and its interface with the ASK demodulator.

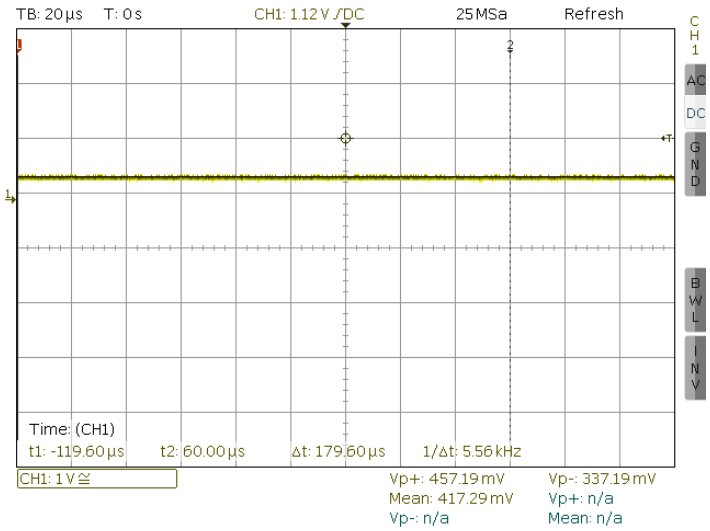


Figure 7.32 Measured rectifier output voltage under RF excitation.

Additionally, the input matching network exhibited a resonance around 3.14 GHz, rather than the intended 2.4 GHz, suggesting a shift in the effective impedance environment or parasitic effects not fully captured during design.

Further investigation revealed a critical design issue in the ASK demodulator PMOS devices. Specifically, the transistors were implemented without a proper deep n–well (or triple–well) isolation structure, preventing independent body biasing. As a result, the PMOS body became unintentionally coupled to the substrate.

This led to parasitic diode conduction paths between the source/drain and the substrate, causing unwanted current leakage. Consequently, A portion of the harvested RF energy was dissipated through the substrate, causing the rectified voltage to significantly reduce, hence degrading its efficiency.

This unintended current path likely contributed to both the reduced output voltage and the shift in resonance frequency, as the rectifier no longer operated under its intended loading conditions.

These results indicate that the failure of the RF rectifier is not due to the rectifier topology itself, but rather due to layout–level device isolation issues in the interfaced ASK demodulator. This issue can be addressed in future tape outs by implementing deep n–well (triple–well) structures for PMOS devices requiring isolation.

7.6.5 IC samples testing and summary

To evaluate the overall performance and integration of the fabricated system, a comprehensive experimental characterization of multiple IC prototypes is carried out. In this work, a total of five samples were evaluated, as summarized in **Table 7.1**. The measurements assess the functionality of the key subblocks across different samples.

Overall, the PMU demonstrated the most reliable performance across the tested samples, consistently providing stable regulated outputs in close agreement with simulation results. An exception was observed in IC prototype 1, where the V_{DDL} pad is believed to have been damaged, resulting in the loss of the corresponding regulated output. Despite this isolated issue, the PMU functionality is considered validated.

Table 7.1 Summary of measured functionality across five fabricated IC prototypes for the main subblocks (✓: fully functional, ⚠: partially functional with degraded performance, and ✗: not functional)

IC prototype	PMU	ASK demodulator	PWM decoder, digital frame router, and DACs	RF rectifier with ASK demodulator
1	⚠	⚠	✓	⚠
2	✓	⚠	✗	⚠
3	✓	⚠	✗	⚠
4	✓	⚠	✗	⚠
5	✓	⚠	✗	⚠

The ASK demodulator was found to be functional; however, its performance is limited by the insufficient drive strength and bandwidth of the comparator stage. While correct operation can be achieved at lower modulation frequencies (e.g., 1 kHz), the demodulator exhibits degraded switching behavior at the target 100 kHz operating frequency. This limitation directly impacts subsequent blocks that rely on the same comparator architecture.

Similarly, the PWM decoder is constrained by the same comparator limitations and can only reliably operate at reduced frequencies. As a result, correct decoding of the 100 kHz ASK–PWM signal is not consistently achieved across all samples.

The digital frame router and DACs were successfully demonstrated on a single IC prototype, where correct decoding and routing of the control signals were observed, with outputs matching simulation results. However, the remaining ICs failed to exhibit proper operation due to the aforementioned comparator limitations in the PWM decoder. Consequently, only one IC prototype provides a fully functional digital backend suitable for system–level validation.

The RF rectifier and its interface with the ASK demodulator exhibited significantly degraded performance. Although rectification was observed, the output voltage was

substantially lower than expected, rendering the block unsuitable for practical operation. This degradation is attributed to layout–level issues in the ASK demodulator, specifically the lack of proper device isolation, which introduced parasitic conduction paths and reduced rectification efficiency.

Based on these results, only one IC prototype is available for demonstrating the digital frame routing functionality in the proof–of–concept system presented in the next chapter. As a result, advanced features such as ID–based addressing cannot be experimentally validated at the IC level within this work.

To enable full system demonstration, a hybrid approach is adopted. One IC prototype is used for the PMU, while the functional digital IC is used for PWM decoding, digital frame routing, and DAC control. Due to the poor performance of the on–chip RF rectifier and ASK demodulator, these blocks are excluded from the IC–level implementation and are instead realized on a PCB, following the approach previously demonstrated in Chapter 6.

7.7 Conclusion

This chapter presented the design, implementation, and experimental validation of a fully integrated control IC for wirelessly powered beam–steering applications. Fabricated in 130 nm CMOS technology, the proposed IC integrates all major subsystems required for single–input operation, including the RF rectifier, PMU, ASK demodulator, PWM decoder, digital frame router, and DACs.

Several key architectural and circuit–level modifications were introduced in the IC implementation to enable low–power operation, improve integration, and support scalability. In the RF rectifier, a voltage–doubler topology using diode–connected PMOS devices was adopted, with co–design of the matching network to operate at 2.4 GHz. The power management circuitry was redesigned using fully CMOS–based bandgap references operating in subthreshold, eliminating the need for BJTs and large resistors, and enabling ultra–low power operation. Two voltage domains were generated ($V_{DDH} \approx 2.6$ V, $V_{DDL} \approx$

0.75 V) using NMOS–based regulators with improved $PSRR$ and low dropout characteristics.

In the communication path, the ASK demodulator was adapted from the PCB implementation by replacing diodes with diode–connected PMOS devices and integrating a two–stage amplifier to increase gain and bandwidth. The PWM decoder was redesigned using transistor–level skewing instead of passive components, along with delay elements and buffer chains to improve signal timing and drive capability. The digital frame router was manually implemented at the transistor level due to synthesis constraints, with expanded functionality including increased bit resolution, additional DAC channels, and longer frame length to support both phase and amplitude control.

The DAC architecture was significantly modified to reduce power consumption. A folded resistor–string topology was combined with low–power skewing comparators to perform level shifting between the low–voltage digital domain and high–voltage analog domain. This approach eliminated the need for power–hungry level shifters and reduced dynamic current consumption from the milliampere range to approximately 180 µA from V_{DDH} and 50–80 µA from V_{DDL}, with a static current of 200 µA.

From measurement results, the PMU demonstrated the most reliable performance, achieving regulated outputs of $V_{DDH} \approx 2.6$ V, $V_{DDL} \approx 0.72$ V, and $V_{COMP1} \approx 0.47$ V, in close agreement with simulations.

The ASK demodulator was functionally validated; however, its performance is limited by the comparator, which exhibits a bandwidth of approximately 112 kHz. As a result, reliable operation is only achieved at reduced frequencies (e.g., 1 kHz), while significant distortion and attenuation is observed at the target 100 kHz data rate. This limitation propagates to the PWM decoder and digital frame router, which rely on the same comparator architecture.

Although correct decoding and routing were demonstrated, this was only achieved in one out of five tested IC samples, indicating sensitivity to process variations and insufficient design margin. When functional, the digital backend successfully demonstrated proper frame decoding, routing, and DAC control, validating the proposed architecture.

The RF rectifier and its interface with the ASK demodulator exhibited significant performance degradation. The measured rectified voltage reached only approximately 0.42 V at 19 dBm input power, far below the expected 4 V at 11.5 dBm. This behavior was traced to layout–level device isolation issues in the ASK demodulator, which introduced parasitic conduction paths and degraded rectifier efficiency.

Overall, this first tapeout successfully validates key aspects of the proposed system. At the same time, it highlights critical limitations, particularly in comparator design and layout–level isolation, which must be addressed in future iterations.

Given these constraints, a hybrid system approach is adopted in the next chapter for complete proof of concept. The validated PMU and the single functional digital IC are combined to demonstrate system–level operation, while the RF rectifier and ASK demodulator are implemented off–chip using a PCB–based solution. This enables a complete proof of concept validation of the proposed wirelessly powered beam–steering control system while preserving the core contributions of this work.

Chapter 8: System–Level Validation and Proof of Concept

This chapter presents the system–level implementation, integration, and experimental proof–of–concept validation of the proposed wirelessly powered beam–steering architecture developed throughout this thesis. Building upon the individual circuit blocks and subsystem characterizations presented in previous chapters, the complete platform is experimentally demonstrated using simultaneous WPT, ASK–PWM clock and data recovery, digital frame routing, DAC–based analog control generation, and RF beam–steering through a single RF interface.

The chapter first discusses the originally intended fully integrated architecture and the practical modifications required after characterization of the fabricated ICs and reflective phase shifters. Due to partial subsystem functionality observed during IC testing, together with the high control voltage requirement of the reflective phase shifters, the final proof–of–concept platform required redistribution of functionality across multiple IC samples as well as the addition of several low–power external support circuits. The chapter further provides detailed discussion of these architectural modifications, highlighting the differences between the originally intended implementation and the final proof–of–concept platform, together with the newly designed external harvesting, regulation, demodulation, and amplification blocks required to achieve complete system–level validation.

The implemented harvesting and control platform is experimentally validated through measurements of harvested and regulated voltages, ASK–PWM envelope recovery, digital frame routing, phase shifter control verification, and final beamformer radiation patterns. The measured beam–steering results are compared against previously characterized directly biased beamforming states to evaluate the accuracy and feasibility of the proposed wireless control methodology.

8.1 System-Level Architecture and Specifications

This section presents the system–level implementation and integration of the proposed wirelessly powered beam–steering platform, including the modifications required after experimental characterization of the fabricated ICs and RF beam–steering circuitry. The original architecture targeted a fully integrated solution capable of wireless power harvesting, clock and data recovery, digital control routing, and analog beam–steering control using a single RF interface. However, the measurement results discussed in Chapter 7, together with the high control voltage requirement of the reflective phase shifters in Chapter 5, revealed several practical limitations that necessitated redistribution of functionality between multiple IC samples and the introduction of external support circuitry, while still maintaining the proposed one–input system concept.

Figure 8.1 illustrates the initial system–level architecture envisioned for the beam–steering platform prior to the IC limitations identified during experimental validation and phase shifter constraints. At the transmitter side, a single RF source broadcasts a modulated signal carrying both wireless power and control information. This signal is wirelessly received by two ICs, each connected to an RF receiving antenna and assigned a unique control block ID.

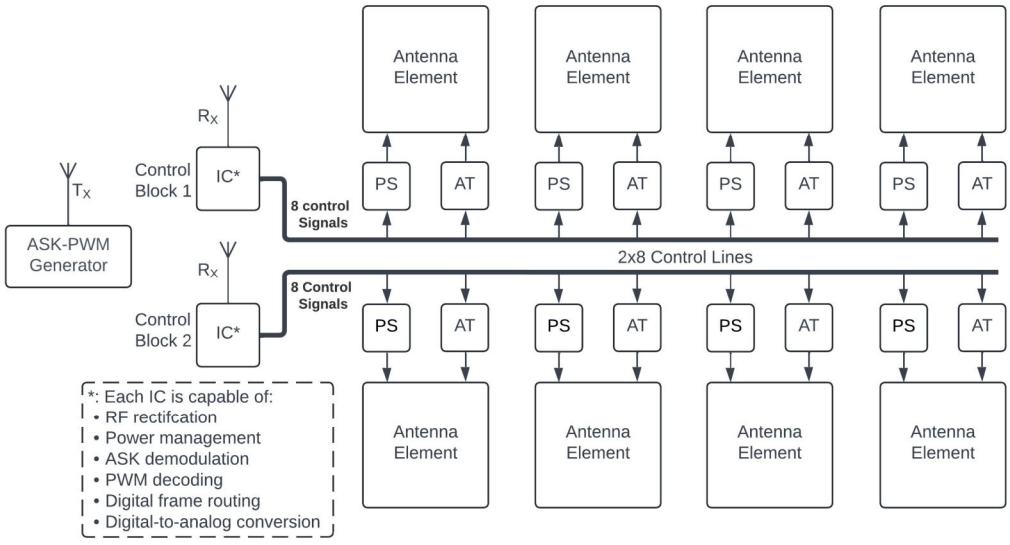


Figure 8.1 Initial system–level architecture of the proposed wirelessly powered beam–steering platform.

Each IC was originally intended to provide the complete functionality of the proposed beam–steering control block, including RF rectification for energy harvesting, power management for on–chip supply generation, ASK demodulation and PWM decoding for simultaneous clock and data recovery, digital frame routing for destination selection, and digital–to–analog conversion for generating the required analog control voltages. The recovered control signals would then be distributed to the attenuators and phase shifters associated with the antenna elements.

Similar to the architecture presented in **Figure 5.14** of Section 5.3, the upper row of attenuators, phase shifters, and antenna subarray elements would be managed by the IC labeled as control block 1, while the lower row would be managed by control block 2. Within each row, the RF control circuitry associated with each antenna element could be individually addressed through a dedicated cell ID.

The purpose of this initial architecture was to demonstrate the proof of concept of the core contribution of this thesis: a single–input wireless interface capable of simultaneously delivering power, clock, and control data to an integrated circuit that performs energy harvesting, data and clock recovery, digital frame routing, control block and cell identification, and digital–to–analog conversion for wireless beam–steering, without the need for dedicated wired supply, clock, data routing, or external feeding pins.

Unfortunately, the experimental limitations discussed in Chapter 7 necessitated several architectural modifications. As shown in Subsection 7.6.5, the limited drive capability of the comparator degraded the operation of the PWM decoder, resulting in only one IC sample with a fully functional frame router. In addition, the damaged regulator pad on that same IC prevented its use for power management, requiring a second IC sample to provide the regulated supply voltages. Furthermore, the reflective phase shifter presented in Subsection 5.3.3 requires a high control voltage. Since the fabricated DAC provides a maximum output voltage of only 2.6 V, as it was originally intended to interface with low–voltage commercial phase shifters, external low–power amplifiers are required to increase the control voltage to approximately 10 V for proper phase shifter operation. Consequently, an additional ultra–high–voltage rectifier and regulation stage is also required to supply these amplifiers.

The updated system architecture, shown in **Figure 8.2**, reflects the practical limitations observed during IC testing and the corresponding modifications required to achieve complete system–level validation. While the original design targeted a fully integrated solution, the experimental results necessitated a redistribution of functionality and the introduction of several external support circuits.

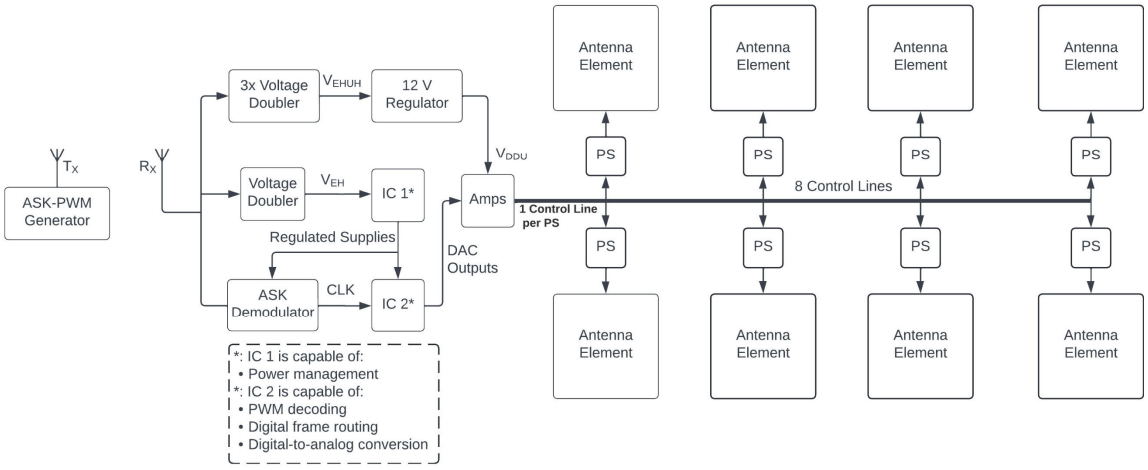


Figure 8.2 Updated proof–of–concept system architecture incorporating the practical modifications required after IC and phase shifter characterization.

Due to the partial functionality of the fabricated IC samples, the intended operations are distributed across two identical chips. In this configuration, IC 1 is dedicated to power management and voltage regulation, providing V_{DDH} (2.6 V) and V_{DDL} (0.75 V) while IC 2 performs PWM decoding, digital frame routing, and digital–to–analog conversion. Together, the two ICs emulate the behavior of a single, almost fully functional control IC. Specifically, IC 1 generates the regulated supply rails required for system operation, whereas IC 2 is responsible for digital processing and the generation of analog beam–steering control signals.

Based on the results presented in Subsections 7.6.4 and 7.6.5, the on–chip RF rectifier and ASK demodulator did not meet the required performance targets and are therefore implemented externally on the PCB. To simplify the implementation, the system employs the panel antenna characterized in Subsection 5.3.1, which operates near the 900 MHz ISM

band. Consequently, the wireless power harvesting circuitry follows the 900 MHz design approach presented in Chapter 6 rather than the 2.4 GHz implementation discussed in Chapter 7. The voltage doubler from Section 6.3 is used to perform RF–to–DC conversion and generate the harvested voltage V_{EH} of approximately 4 V, while an external ASK demodulator, modified from the design in Subsection 5.3.2 to support a 100 kbps data rate, extracts the clock signal from the incoming RF waveform. The harvested voltage is supplied to IC 1 for regulation, whereas the recovered clock signal is provided to IC 2 for PWM decoding and subsequent digital processing. All external support circuits are designed for low power consumption to maintain compatibility with WPT operation while ensuring reliable demodulation of the 100 kHz ASK signal.

Since only one fabricated IC sample contains a fully functional frame router, the control block ID functionality cannot be experimentally validated in this chapter using the originally intended multi–IC architecture. As a result, IC 2 is configured to simultaneously control both antenna subarrays. A single IC is capable of generating eight analog control outputs corresponding to four phase shifters and four attenuators, each implemented using a 6–bit DAC, as was presented in the previous chapter. However, the beam–steering array presented in Subsection 5.3.4 requires control of eight phase shifters. Therefore, the four attenuator control paths are omitted in this proof–of–concept implementation, allowing all eight DAC outputs of IC 2 to be dedicated exclusively to phase shifter control. Nevertheless, this modification does not invalidate the proposed IC control architecture, since the control block identification concept was already validated independently in Chapters 4, 5, and 7.

Another important modification arises from the replacement of obsolete commercial phase shifters with the reflective phase shifter introduced in Subsection 5.3.3, which requires a control voltage of approximately 10 V. To satisfy this requirement, a three–stage voltage doubler is employed to boost the harvested DC voltage, producing V_{EHUH}, followed by an off–chip 12 V regulator that provides a stable ultra–high–voltage supply V_{DDUH}. This supply supports the analog beam–steering control path by enabling amplification of the maximum 2.6 V DAC outputs to approximately 10 V for proper operation of the reflective phase shifters. The three–stage voltage doubler follows the same concept presented in

Section 6.4, where the matching network is designed to provide good impedance matching for both the harvesting path and the additional ultra–high–voltage rectification path while isolating the communication path through the use of a series lossy resistor.

The following section presents the experimental validation and proof–of–concept demonstration of the overall system.

8.2 System-Level Proof-of-Concept Demonstration

The harvesting and control subsystem shown in **Figure 8.2** was implemented on a dedicated proof–of–concept PCB platform, shown in **Figure 8.3**, to experimentally validate the complete wireless powering and beam–steering control architecture. The harvesting–control panel was fabricated on a 0.6 mm FR–4 PCB, where the top layer was used for component placement and signal routing, while the bottom layer served as a continuous ground plane to provide a low–impedance return path and improved noise isolation.

To preserve the integrity of the fabricated ICs and avoid potential damage associated with repeated desoldering and reassembly, the previously developed characterization boards from **Figure 7.22**(b) were directly integrated into the proof–of–concept platform. The IC2 test board, containing the PWM decoder, digital frame router, and DAC circuitry, was mounted on the bottom–left side of the panel, while the IC1 test board, containing the power management circuitry for V_{DDH}, V_{DDL}, and V_{COMP1}, was mounted on the bottom–right side. This modular integration approach enabled reuse of the validated test platforms while still maintaining access to measurement nodes and debugging interfaces through the expansion headers available on each board.

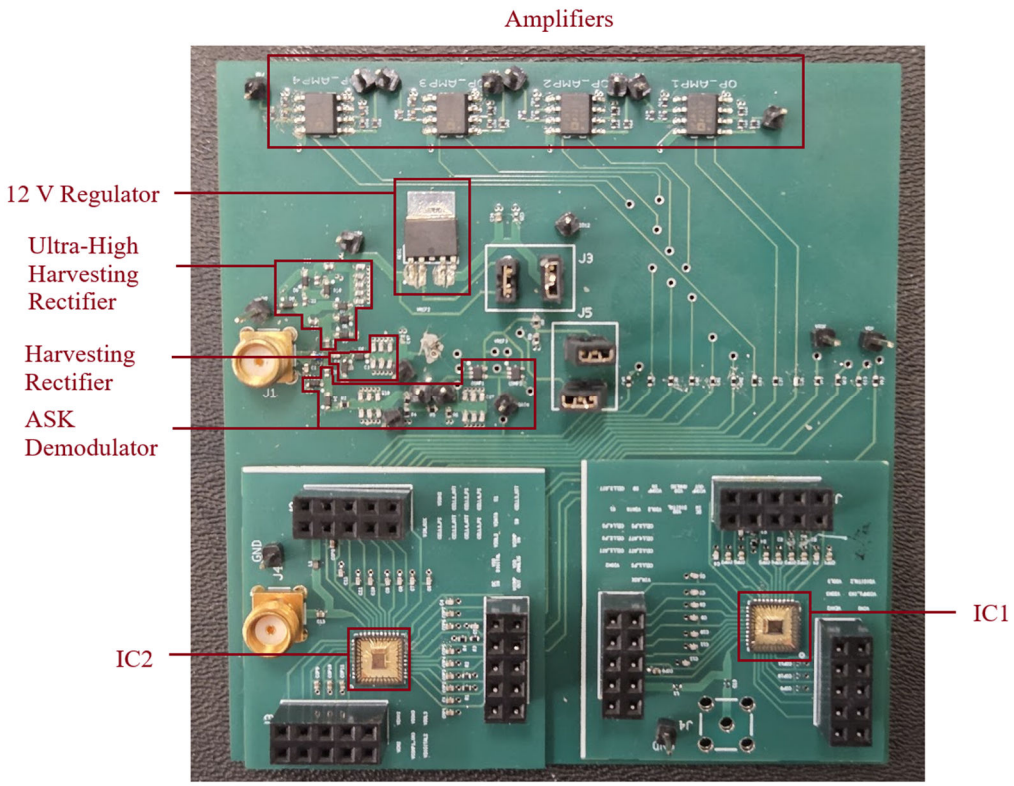


Figure 8.3 Photograph of the fabricated proof–of–concept harvesting and control PCB panel.

In addition to the mounted IC test platforms, several supporting circuits were implemented directly on the main PCB panel. These included the harvesting rectifier, ultra–high harvesting rectifier, 12 V regulator, ASK demodulator, and external amplifier stages required to interface the DAC outputs with the reflective phase shifters. The resulting platform therefore combines the previously characterized IC subsystems with the additional off–chip support circuitry required for full system–level operation and experimental validation.

The harvesting and communication section implemented on the left side of the PCB panel is redrawn in schematic form in **Figure 8.4** for clarity. The architecture and circuit partitioning of the harvesting and communication paths follow the design considerations discussed in the previous section, where separate power and communication branches were introduced to simultaneously support wireless powering, ASK–PWM demodulation and decoding, and high–voltage phase shifter control.

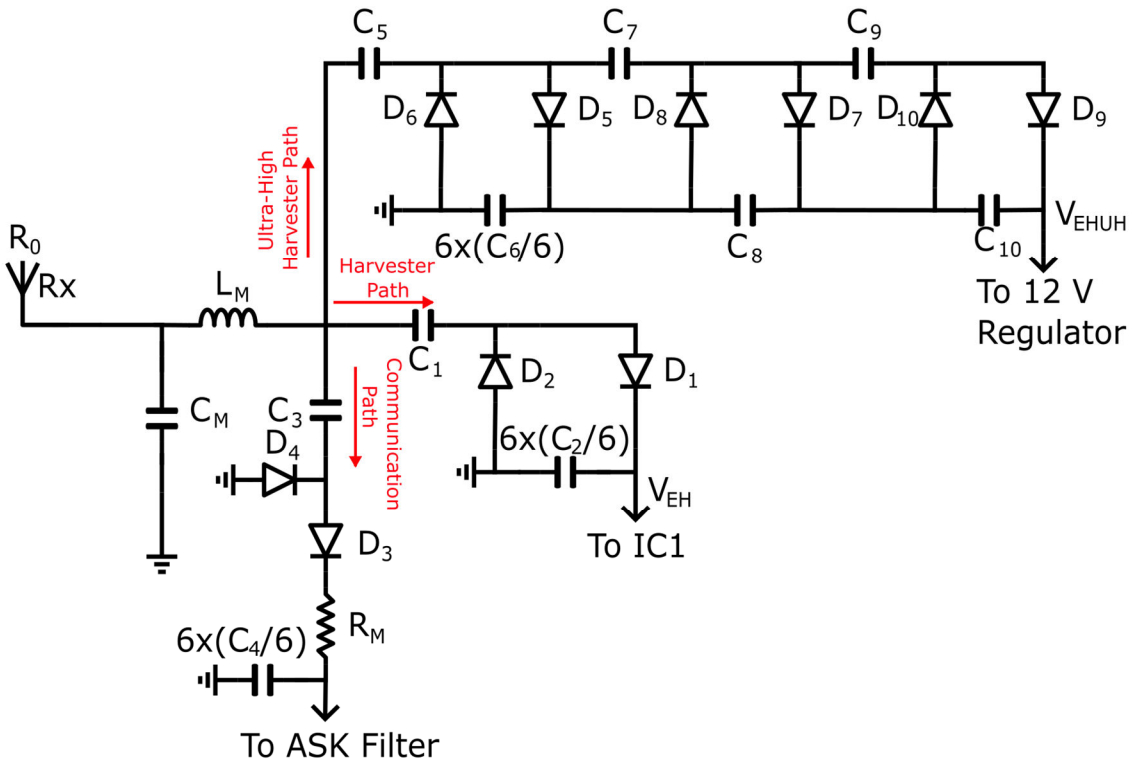


Figure 8.4 Simplified schematic of the harvesting and communication section implemented on the proof–of–concept PCB platform.

The main harvesting path forms a single–stage voltage doubler that generates V_{EH} used by the IC power management circuitry (IC1). In parallel, the communication path extracts the ASK–PWM modulation envelope for subsequent demodulation and clock/data recovery. The ultra–high harvesting path consists of capacitors $C_5 - C_{10}$, together with diodes $D_5 - D_{10}$, forming a three–stage voltage doubler. This path generates the ultra–high harvested supply V_{EHUH}, which is subsequently regulated to 12 V through the external regulator shown previously in **Figure 8.2**. The regulated 12 V supply is required to support the maximum amplified DAC output voltage of approximately 10 V needed by the reflective phase shifters.

A two–stage voltage doubler implementation was also investigated during simulation; however, it produced a harvested voltage of only approximately 13 V under nominal conditions. Considering the expected degradation due to parasitics, loading, and measurement losses in the fabricated prototype, this voltage margin was insufficient to reliably sustain 12 V regulation. Consequently, the three–stage implementation was

selected to provide additional voltage headroom and improved robustness during experimental operation. The same SMS3922–079 Schottky diodes used throughout Chapter 6 were employed in both the harvesting and communication paths to maintain consistency with the previously characterized rectifier and detector implementations.

Post–layout simulations, including the expected loading conditions of the harvesting branches, demonstrated simultaneous generation of approximately 20 V for V_{EHUH}, 4 V for V_{EH}, and 2 V for V_{COMM} at an RF input power of 10 dBm, satisfying the supply requirements of the overall system. The input matching network was implemented using an inductance L_M of 4.3 nH in post–layout simulations together with a matching capacitance C_M of 16 pF. During experimental measurements, the inductance value was reduced to 3.0 nH to compensate for practical parasitic effects and improve matching performance.

The capacitors used in the three–stage voltage doubler were selected as 1000 pF components to provide sufficient filtering and supply decoupling, while the capacitor values used in the harvesting and communication paths follow the design methodology presented in Sections 6.2, 6.3, and 6.4. Additionally, the shunt–capacitor techniques introduced in Section 6.3 were again applied at critical RF nodes to suppress parasitic inductive effects and reduce RF feedthrough into the harvesting and communication paths.

As for the 12 V regulator, the S–19213BC0A–V5T2U7 LDO regulator from ABLIC Inc., Tokyo, Japan, was selected for the implementation. This regulator provides a fixed 12 V output while supporting input voltages up to 36 V, making it suitable for the V_{EHUH} harvested level of approximately 20 V generated by the three–stage voltage doubler. The V_{EHUH} node was also directly connected to the enable pin of the regulator to automatically activate the 12 V supply once sufficient harvested voltage becomes available. The regulator features a very low quiescent current of approximately 5 μA, making it well suited for the low–power operation targeted in this work. A 100 nF output capacitor was added to ensure loop stability and suppress output voltage fluctuations. Additionally, a dummy 150 kΩ resistor was connected at the regulator output, drawing approximately 80 μA, to assist WPT startup operation and stabilize the loading conditions seen by the ultra–high harvesting path.

The regulated 12 V supply powers the amplifier stages located on the top side of the PCB panel shown previously in **Figure 8.3**. The amplifier selection was particularly challenging because the design simultaneously required operation from a 12 V supply, extremely low current consumption compatible with WPT operation, and sufficient bandwidth to support the DAC update rate of approximately 4 kilo samples per second. As a result, the OP281GSZ dual operational amplifier from Analog Devices Inc., Wilmington, Massachusetts, USA, was selected. The OP281GSZ integrates two operational amplifiers within a single package, consumes approximately 4 μA per amplifier, and supports supply voltages up to 12 V, making it compatible with the selected regulator. The amplifier provides a gain–bandwidth product of approximately 105 kHz and a slew rate of 25 V/ms, which is sufficient for the targeted DAC update rate.

The amplifiers were configured using the same non–inverting gain topology introduced previously in Subsection 5.3.5. A closed–loop voltage gain of 5 was implemented using a 5 MΩ feedback resistor together with a 1 MΩ resistor connected to ground. Large resistance values were intentionally selected to minimize the current drawn from the 12 V supply, since this supply is generated entirely through wireless harvesting. With a gain–bandwidth product of approximately 105 kHz, the resulting closed–loop bandwidth is approximately 20 kHz, which is sufficient for the approximately 4 kilo samples per second DAC update rate used in the beam–steering system. Assuming a measured DAC output voltage close to 2.5 V, the amplified output can ideally reach approximately 12.5 V, which comfortably covers the required 10 V control range of the reflective phase shifters. A 10 kΩ isolation resistor was added at the output of each amplifier to provide bias isolation between the control circuitry and the reflective phase shifters.

From a power consumption perspective, the 12 V regulator supplies approximately 150 μA in total, including the amplifier stages and startup resistor. This corresponds to an equivalent loading resistance of approximately 135 kΩ seen by the V_{EHUH} node, which was included during the design and optimization of the three–stage voltage doubler.

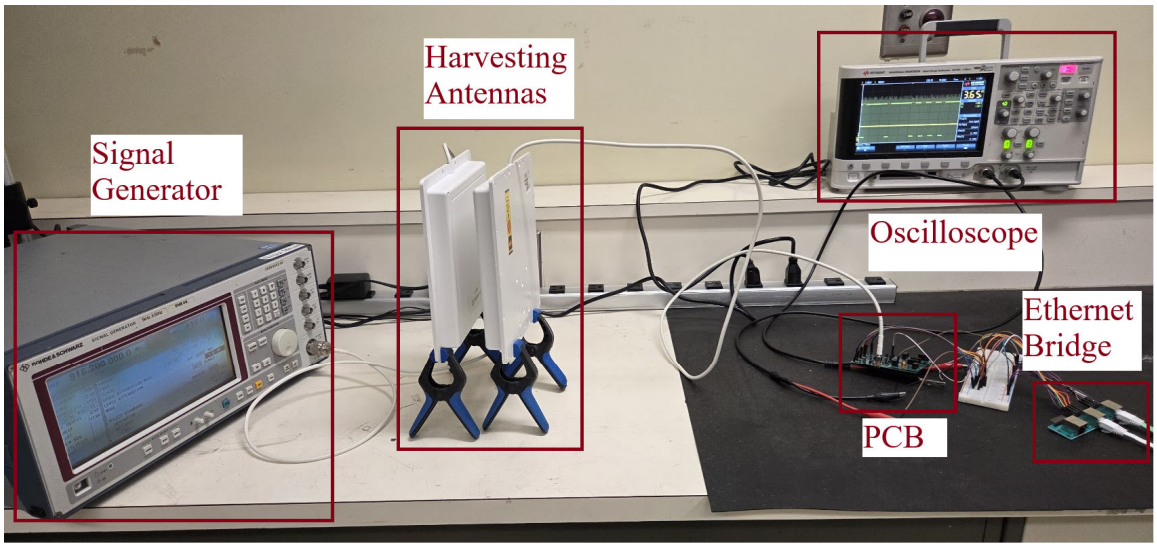
Figure 8.4(a) shows the experimental setup used to validate the proposed wirelessly powered beam–steering control architecture. A 100 kHz ASK–PWM signal on a 916 MHz RF carrier was generated using the Rohde & Schwarz SME06 signal generator and

transmitted through the harvesting antenna pair introduced in Subsection 5.3.1. The RF signal simultaneously carries wireless power, clock information, and digital control data. Due to the integration of two harvesting paths, the overall matching conditions were narrow, making the link sensitive to mistuning during measurement. The resulting power loss limited the harvested energy, requiring a reduced antenna separation to ensure sufficient received power. Consequently, the final proof–of–concept operated in the short–range regime, with the receiving antenna delivering the RF signal to the harvesting and control PCB shown in **Figure 8.3**.

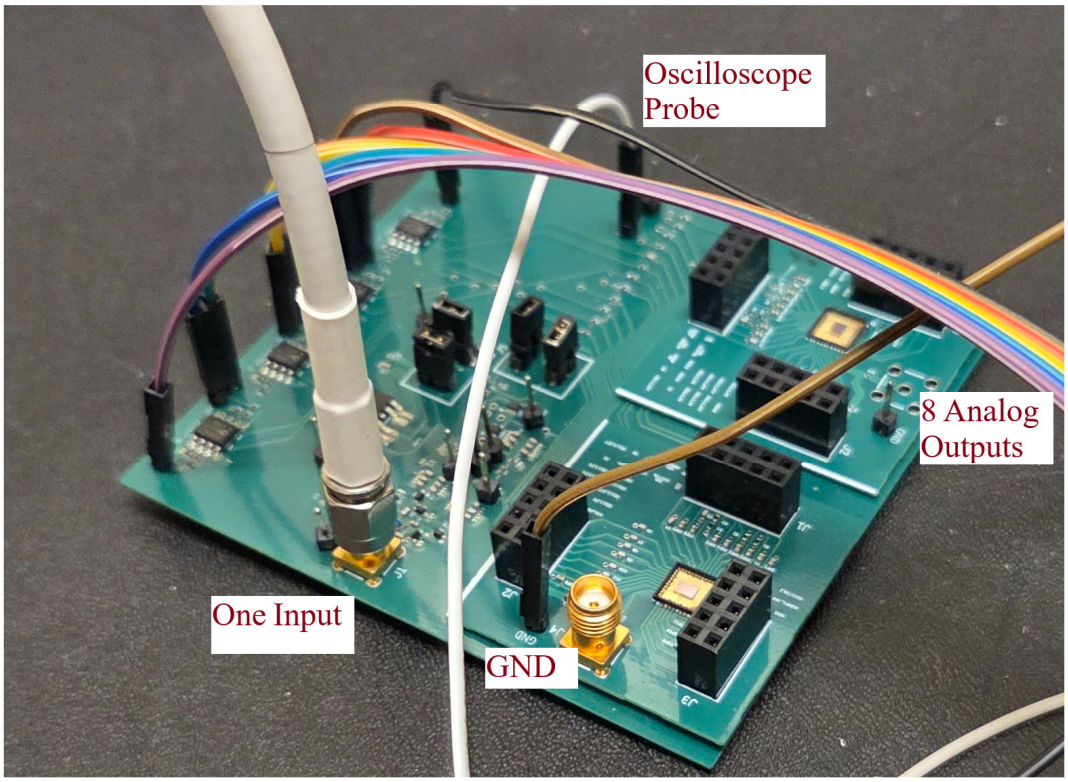
A key feature of this experimental demonstration is that no external DC power supplies were used to operate the control platform. All required system supplies, including the IC supply voltages, data and clock recovery circuitry, digital control logic, DAC operation, and amplified phase shifter bias voltages, were generated exclusively through the received wireless RF signal. This experimentally demonstrates the capability of the proposed architecture to simultaneously deliver wireless power and control signaling through a single RF interface.

The recovered digital control data are converted into amplified analog control signals, which are then routed from the PCB control module through an Ethernet bridge interface toward the reflective phase shifters and antenna array presented in Subsection 5.3.4. The resulting RF beam–steering operation of the antenna array was experimentally characterized inside an anechoic chamber at 3.3 GHz. An oscilloscope was additionally connected to the harvesting–control PCB panel to monitor critical signals during operation, including harvested and regulated supply voltages, recovered clock and control waveforms, and amplified DAC phase shifter control voltages.

Figure 8.4(b) provides a zoomed–in view of the fabricated PCB panel during measurements. One of the key highlights of this implementation is that the entire system operates using only a single RF input connection, through which WPT, clock recovery, and control data transmission are simultaneously achieved, consistent with the primary objective of this work. The figure also shows that only eight analog control outputs are required from the control module to bias the reflective phase shifters of the antenna array.



(a)



(b)

Figure 8.4 Experimental validation setup of the proposed wirelessly powered beam–steering control system showing: (a) measurement setup, and (b) zoomed–in view of the fabricated harvesting and control PCB module during measurement.

As for the data pattern setup, the signal generator was configured to produce ASK–PWM control patterns that adjust the phase shifters in a progressive manner, similar to the beam–forming states described in Subsections 5.3.4 and 5.3.5. Accordingly, three control states were programmed: S0, corresponding to 0° beam–steering, S1, corresponding to a progressive phase shift for 10° steering, and $S2$, corresponding to 15° steering.

The ASK–PWM data pattern was encoded such that a logic '0' consisted of a 5 μs low pulse followed by a 5 μs high pulse, corresponding to a duty cycle of 50% at a bit rate of 100 kbps. In contrast, a logic '1' maintained the same 5 μs low pulse width but used an extended 20 μs high pulse width.

The transmission was performed using a TDMA–based approach, where cell 1 was programmed first using a 12–bit control word. Since each phase shifter DAC requires 6 bits, this allowed independent control of the first two phase shifters. The same procedure was then sequentially applied to cell 2, cell 3, and cell 4 to realize the desired progressive phase–shift distribution across the antenna array.

Figure 8.5(a) shows the measured harvested voltages for both energy harvesting paths. To maximize the harvested voltage levels and compensate for propagation path loss and impedance mismatches, the RF signal generator output power was increased up to 16 dBm, while the transmitting and receiving antennas were positioned in close proximity. The high–voltage harvesting path, V_{EHUH}, reached approximately 18 V, which is lower than the expected 20 V. Similarly, the low–voltage harvesting path, V_{EH}, measured approximately 3 V instead of the targeted 4 V. These reductions are mainly attributed to the additional RF power loss introduced by the wireless link between the transmitting and receiving antennas. Furthermore, the input matching network was difficult to optimize on the PCB since the system simultaneously performs power matching for two separate harvesting paths operating under different loading conditions.

Despite the reduced harvested voltage levels, the measured V_{EH} of approximately 3 V remained sufficient to sustain regulation of the 2.6 V supply, as previously demonstrated in **Fig. 7.11**(b). However, reliable regulation required reducing the ASK modulation index

to a relatively small value in order to minimize large fluctuations on V_{EH}, which could otherwise cause temporary regulator dropout during data transmission.

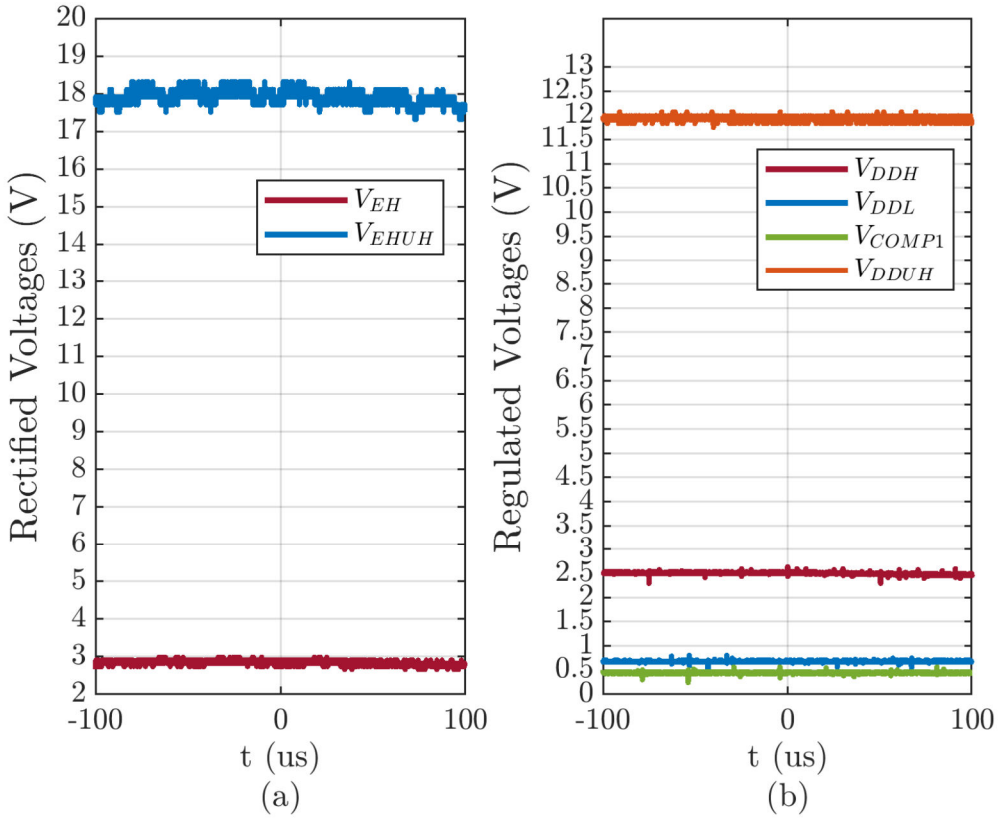


Figure 8.5 Measured wireless power harvesting and regulated supply voltages of the proposed beam–steering platform showing: (a) V_{EH} (red) and V_{EHUH} (blue), and (b) measured regulated outputs showing V_{DDH} (red), V_{DDL} (blue), V_{COMP1} (green), and V_{DDUH} (orange).

Figure 8.5(b) presents the measured regulated supply voltages generated from the harvested inputs. The regulated outputs remain stable with relatively small ripple and variation despite the reduced harvested voltage levels and wireless transmission losses. Specifically, V_{DDH} is regulated near 2.6 V, while V_{DDUH} remains close to 12 V. In addition, the low–voltage digital supply V_{DDL} and comparator reference voltage V_{COMP1} remain stable at approximately 0.75 V and 0.5 V, respectively, throughout the measurement interval. These results confirm that the proposed regulation and power distribution architecture can maintain stable operation under practical wireless powering conditions,

enabling reliable operation of the subsequent ASK–PWM demodulation and beam–steering control circuitry.

Figure 8.6(a) shows the measured envelope detector output, V_{ENV}, together with the extracted average voltage, V_{AVG}, under wireless powering and ASK–PWM data transmission conditions. Compared to the measurements presented in **Figure 7.27**(a) of Subsection 7.6.2, the envelope swing observed here is significantly smaller. This reduction is mainly due to the lower available harvested voltage and the intentionally reduced ASK modulation index required to maintain stable regulator operation. By limiting the modulation depth, large variations on the harvested supply were avoided, preventing temporary dropout of the regulated outputs during data transmission.

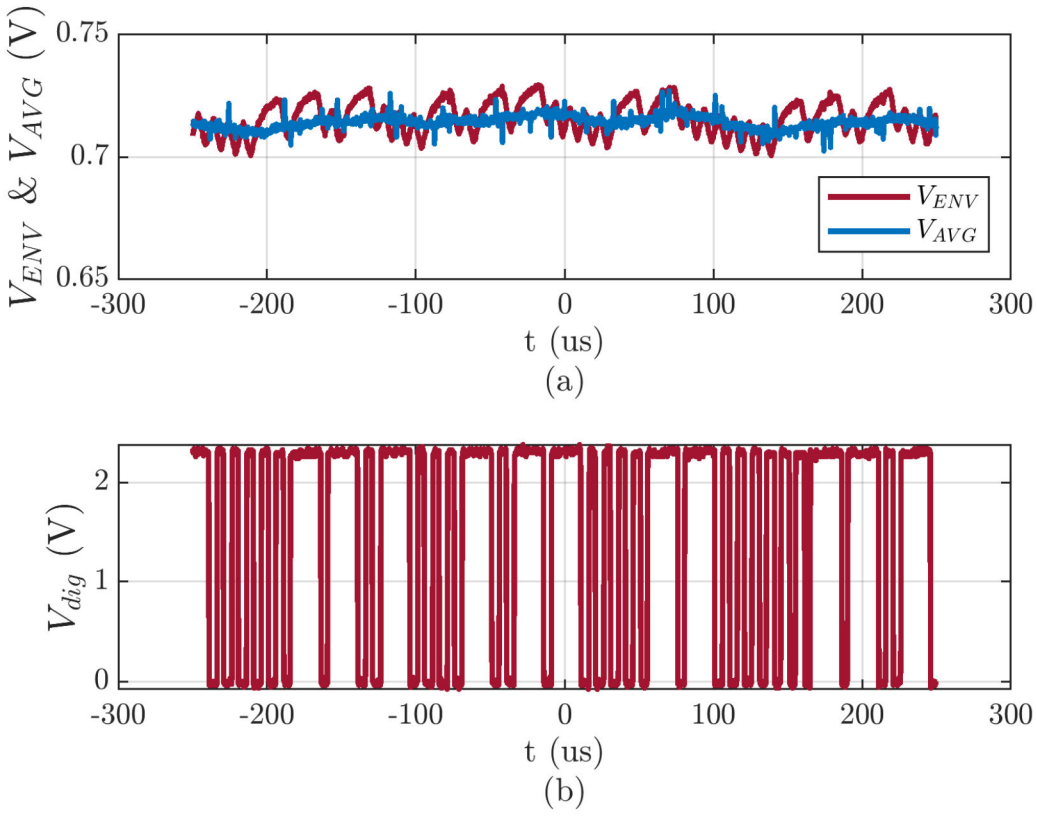


Figure 8.6 Measured ASK–PWM envelope detection and recovered digital waveform under wireless powering conditions showing: (a) V_{ENV} (red) and V_{AVG} (blue), and (b) V_{dig}.

Despite the smaller envelope amplitude, the average tracking voltage V_{AVG} continues to follow the envelope variations with sufficient separation between the two signals to enable reliable clock and data extraction. The extracted digital waveform shown in **Figure 8.6**(b) confirms that the ASK demodulation circuitry remains fully operational, successfully recovering the transmitted clock even under reduced modulation conditions.

Figure 8.7 presents the measured transient response of the phase shifter control voltages for one row of the antenna array during wireless powering, startup, and ASK–PWM beam–steering operation. Only one row of phase shifters is shown since the second row follows the same progressive phase–shift behavior and therefore exhibits nearly identical operation.

As discussed previously in Subsection 7.6.3, one output pin of the fabricated IC was not functioning correctly, likely due to pin damage during handling or test board integration. Consequently, this output was replaced with a ground connection during the PCB implementation. This modification does not affect the beam–steering operation since the first antenna element in the progressive phase–shift configuration is intentionally maintained at approximately 0 V and serves as the phase reference for the remaining elements.

The measured waveforms clearly illustrate four distinct operating regions. Initially, each phase shifter maintains its previous control state before wireless powering is interrupted. Once the harvested energy is removed, the control voltages enter a switch–off state where the stored charge on the phase shifter control nodes gradually decays. During the subsequent harvester startup and energy buildup phase, the harvested supplies recover and the control circuitry begins restoring operation, resulting in transient fluctuations and overshoot behavior as the regulators, DACs, and control loops stabilize. Finally, the control system converges toward the recovered beam–steering state corresponding to the transmitted ASK–PWM control pattern.

The final steady–state control voltages demonstrate the successful recovery of the intended progressive phase distribution across the phase shifter network. Despite the reduced harvested power conditions, the proposed wireless power and ASK–PWM control architecture successfully restores the desired beam–steering control states after startup.

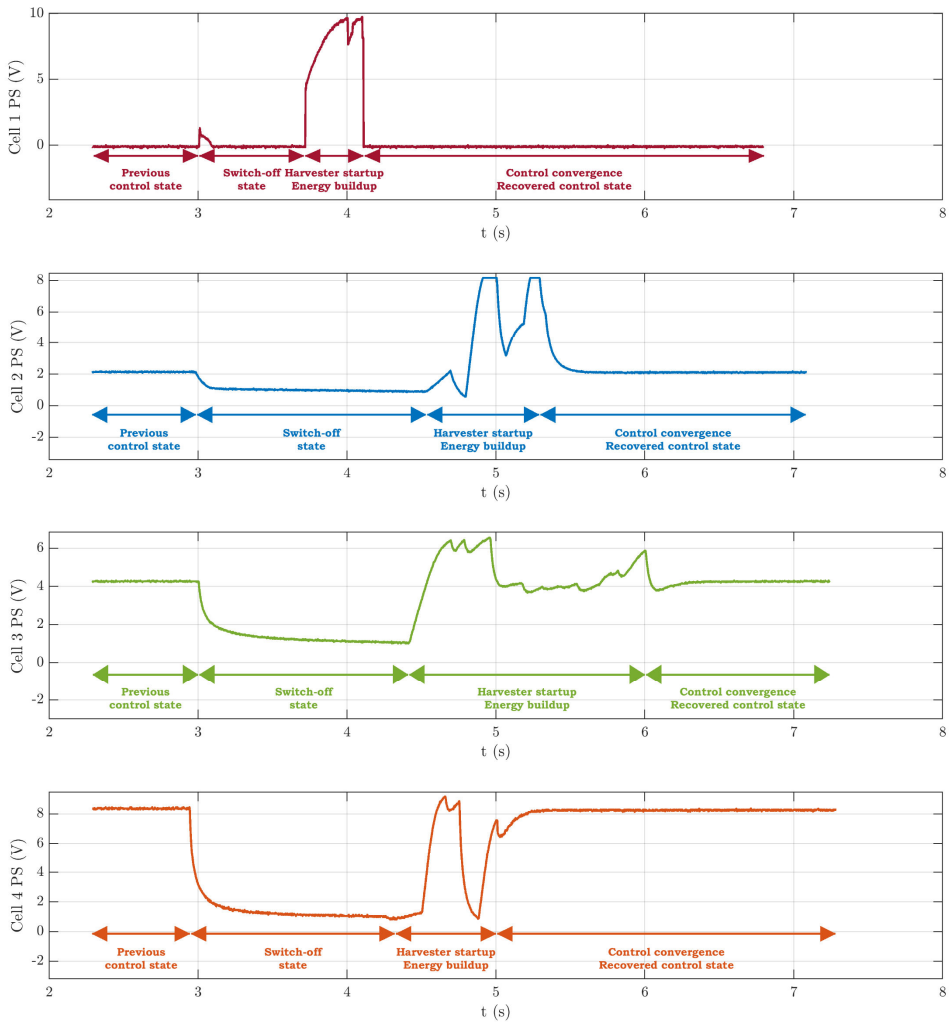


Figure 8.7 Measured transient response of the phase shifter control voltages for one row of the antenna array during wireless powering and ASK–PWM beam–steering operation, highlighting important regions.

Figure 8.8 presents the measured radiation patterns of the wirelessly powered beam–steering platform for the three transmitted beam states $S0$, $S1$, and $S2$, measured at a beamforming frequency of 3.3 GHz. The overall experimental setup, including the routing of the recovered control signals from the wireless control system through the Ethernet bridge interface toward the reflective beam–steering network, was implemented in the same manner as described previously in Subsections 5.3.4 and 5.3.5. In this experiment, however, the beam–steering control voltages were generated entirely through the proposed wireless power harvesting and ASK–PWM control architecture rather than through direct wired biasing.

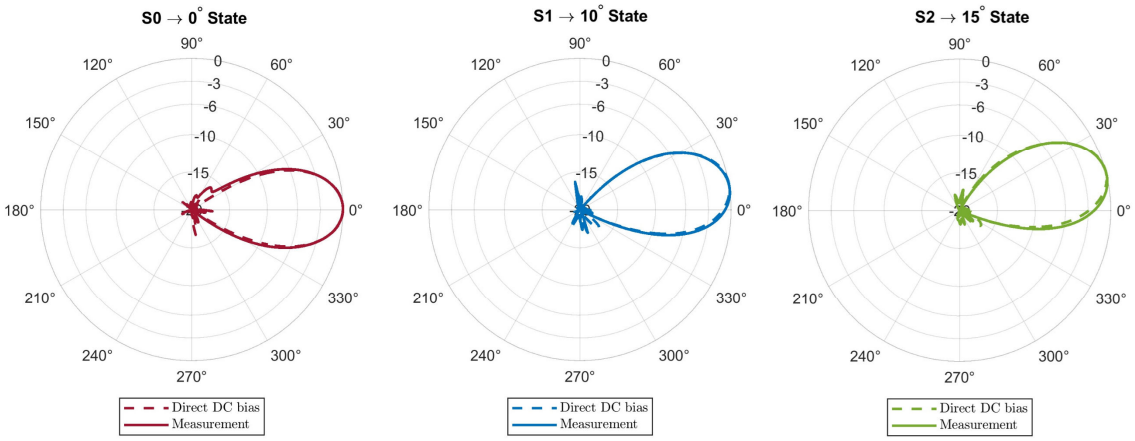


Figure 8.8 Comparison between measured radiation pattern of the wirelessly powered control approach (solid) and direct DC bias (dashed) of the 2x4 beam–steerer for different steering angle states: (a) *S0*, (b) *S1*, and (c) *S2*.

The measured radiation patterns are compared against the previously measured direct DC bias reference beam states from Subsection 5.3.4. For the three transmitted steering states, the measured beam directions were approximately 1°, 10°, and 15°. After accounting for the small systematic angular offset observed during measurement calibration, the corrected steering angles become approximately 0°, 9°, and 14°, respectively. These corrected beam directions closely match the directly biased beamforming results obtained previously, demonstrating that the proposed wireless control platform successfully reproduces the intended progressive phase–shift distribution across the antenna array.

These results experimentally validate the complete end–to–end operation of the proposed system, including wireless power harvesting, regulated supply generation, ASK–PWM clock and data recovery, TDMA–based control routing, DAC–based phase shifter bias generation, and RF beam–steering. The successful recovery and reproduction of the intended antenna beam states confirm the feasibility of the proposed wirelessly powered beam–steering architecture and demonstrates the first proof–of–concept realization of the integrated system presented throughout this thesis.

8.3 Conclusion

This chapter experimentally demonstrated the complete proof–of–concept implementation of the proposed wirelessly powered beam–steering architecture. The developed system successfully achieved simultaneous WPT, ASK–PWM clock and data recovery, digital routing, DAC–based analog control generation, and RF beam–steering through a single RF interface. Despite the practical limitations encountered during fabricated IC characterization, including partial subsystem functionality and the high control voltage requirement of the reflective phase shifters, the modified proof–of–concept platform successfully preserved the intended system operation and experimentally validated the core concept proposed in this thesis.

Experimental measurements confirmed stable wireless harvesting and regulation of multiple supply rails required for system operation. Under wireless excitation at 916 MHz with an RF input power up to 16 dBm, the proposed harvesting platform generated close to the required harvested voltages. These voltages were successfully regulated, enabling simultaneous operation of the low–voltage digital circuitry and the amplified reflective phase shifter control path. Reliable ASK–PWM envelope detection, clock recovery, and digital data extraction were demonstrated at a data rate of 100 kbps, while the DAC and amplified phase shifter control path successfully supported update rates of approximately 4 kilo samples per second. These operations were achieved even under reduced modulation depth conditions required to maintain nominal regulator performance during wireless operation. In addition, transient measurements of the phase shifter control voltages verified successful startup recovery and convergence of the intended progressive beam–steering states following wireless power interruption and restoration.

Most importantly, the final measured antenna radiation patterns demonstrated successful beam–steering at approximately 0°, 9°, and 14° after calibration correction, closely matching the previously measured directly biased beamforming reference states. The measurements were performed at a beamforming frequency of 3.3 GHz, where the proposed wireless control architecture successfully reproduced the intended progressive phase distribution across the 2×4 beam–steering array. These results experimentally validate the feasibility of the proposed wireless control architecture and demonstrate the

first complete end–to–end realization of the integrated system presented throughout this thesis.

The next and final chapter summarizes the major contributions and findings of this work, revisits the overall system achievements, and discusses potential future research directions and improvements toward fully integrated and scalable wirelessly powered beam–steering systems.

Chapter 9: Summary of Thesis and Future Work

Conventional phased–array beamforming systems introduce significant physical and architectural challenges as array dimensions continue to scale. Traditional beam–steering implementations rely heavily on wired infrastructures for power delivery, clock distribution, and digital control routing. As the number of antenna elements increases, these interconnect networks consume substantial routing area, increase PCB complexity, introduce parasitic coupling and electromagnetic interference, and ultimately limit achievable array density, modularity, and scalability.

The motivation behind this thesis was therefore driven by the need to fundamentally rethink how beam–steering control systems distribute power, timing, and control information across large–phased arrays. Instead of relying on conventional wired infrastructures, this work explored the feasibility of a wireless alternative capable of reducing routing congestion, simplifying integration, and enabling scalable distributed beam–steering architectures.

To address these challenges, this thesis proposed and experimentally demonstrated a wirelessly powered beam–steering control architecture based on the combination of WPT and non–coherent ASK–PWM. The proposed architecture enables simultaneous wireless delivery of power, timing information, and control data through a unified RF interface.

To validate the feasibility of the proposed approach, the system was implemented and experimentally evaluated through multiple levels of validation including PCB prototyping, FPGA verification, RF subsystem characterization, and integrated circuit realization in a 130 nm CMOS process.

9.1 Summary of Thesis Achievements

This thesis presented and validated a system–level architecture for a wirelessly powered ASK–PWM beam–steering control platform capable of simultaneously delivering wireless power, clock information, and control data through a unified RF interface. The developed receiver architecture incorporated the RF rectifier and power conditioning

circuitry, ASK–PWM demodulator and decoder, digital frame router, and DAC control interface required for distributed beam–steering operation. Furthermore, a wireless TDMA addressing strategy enabled independent routing of control data toward distributed control blocks and antenna cells.

System–level feasibility of the proposed architecture was verified through a comprehensive Simulink implementation. Simulation results demonstrated successful clock recovery from the ASK envelope, reliable decoding of narrow and wide PWM pulses for data extraction, accurate frame recognition, and proper TDMA–based routing of DAC control signals toward the intended control blocks. These results confirmed the functional feasibility of the proposed non–coherent wireless control framework.

Also, this thesis experimentally validated the proposed non–coherent wireless control framework through a staged FPGA and PCB prototyping strategy that progressively evolved from digital control verification toward phased–array beam–steering demonstration. The complete ASK–PWM receiver, including the synthesized digital frame router and DAC subsystems, was subsequently implemented and experimentally validated on PCB. Reliable asynchronous clock recovery and PWM decoding were successfully demonstrated, and the recovered control data were routed through the FPGA–implemented frame router before being converted into analog beam–steering control voltages using DAC and amplification stages. The proposed framework was further validated through wireless beam–steering operation of a 2×4 phased array, confirming reliable reproduction of the intended beam–steering phase states using the proposed non–coherent ASK–PWM architecture.

Next, this thesis extended the validated ASK–PWM digital control framework toward a fully wirelessly powered implementation through the design, realization, and experimental validation of a wirelessly powered ASK–PWM receiver. This directly addressed the challenge of simultaneously delivering wireless power, clock information, and control data while eliminating conventional wired power distribution, external supply rails, PLLs, and SPI communication infrastructures. The complete receiver was experimentally validated on an FR–4 PCB platform, demonstrating stable simultaneous wireless power harvesting and communication. To enable reliable operation, techniques

were introduced to mitigate PCB parasitic effects and reduce interaction between the harvesting and communication paths, thereby preserving both harvesting efficiency and communication robustness. These results validated the practical feasibility of the proposed wireless harvesting and communication architecture for distributed beam–steering control applications.

This thesis also presented the design, fabrication, and experimental validation of a 130 nm CMOS wirelessly powered control IC for beam–steering applications. The proposed IC integrated key subsystems required for single–input wireless operation, including wireless power harvesting, ASK demodulation, PWM decoding, digital frame routing, and DAC–based analog control generation. Experimental results successfully validated several core architectural concepts, particularly the PMU, communication chain, and distributed control functionality. However, comparator bandwidth limitations and layout–related rectifier isolation issues reduced overall communication robustness and standalone IC performance, preventing full functionality across all fabricated samples. Despite these limitations, the first tapeout successfully demonstrated the feasibility of the proposed architecture and validated its core system–level operation.

Finally, this thesis experimentally demonstrated the proof–of–concept realization of a wirelessly powered beam–steering architecture using a hybrid implementation combining fabricated IC subsystems with PCB–based wireless front–end circuitry. The system successfully validated simultaneous wireless power delivery, asynchronous clock recovery, digital data extraction, local routing, and analog beam–steering control generation through a single–input RF interface. Final antenna radiation measurements further confirmed accurate RF beam–steering operation and successful generation of the required progressive phase distribution across the implemented 2×4 phased array, thereby validating the core architectural concepts proposed throughout this thesis despite practical IC and phase shifter limitations. This final demonstration directly addressed the central research question regarding whether conventional wired power, clock, and control infrastructures in phased–array systems could be replaced by a fully wireless alternative while preserving practical beam–steering functionality, synchronization capability, and distributed control operation.

Ultimately, the proposed architecture enables a pathway toward compact, scalable, and modular beam–steering systems with substantially reduced routing density, feed–pin count, PCB complexity, and synchronization overhead. Such capabilities are particularly attractive for future large–scale phased arrays, reconfigurable intelligent surfaces, distributed antenna systems, low–cost electronically steerable antennas, space–constrained RF front–ends, satellite communications, radar systems, sensing platforms, and next–generation wireless communication systems where dense integration, scalability, and routing simplification become increasingly critical.

9.2 Future Research Directions

A major direction for future work involves the comprehensive optimization of the wireless power–transfer link between the external transmitter and the distributed beam–steering control ICs. While this thesis primarily focused on validating the IC architecture and subsystem functionality, large–scale deployment will require each control IC to operate using its own integrated or miniaturized receive antenna. Achieving such a distributed wireless powering network introduces several challenges, including limited gain and reduced power–harvesting capability of small antennas. Future work should therefore investigate the scalability limits of simultaneously powering large numbers of distributed receivers from a single source. In addition, alternative transmitter architectures, such as distributed transmit subarrays servicing localized groups of control ICs, should be explored as potential solutions for improving power uniformity and enhancing scalability for large beam–steering surfaces. In addition, since the beam–steering panel and control panel were implemented as physically separate subsystems in this work, future research should explore their full integration onto the same panel and quantitatively investigate the interaction between the WPT network and the beamforming operation.

Another important direction for future work is the development of a more scalable and manufacturing–efficient control block identification methodology. In this thesis, control block IDs were configured externally using dedicated ID–selection pins; however, this approach becomes increasingly impractical as array size grows due to limited IC pad

availability. Future systems containing hundreds or thousands of beam–steering elements will therefore require alternative identification techniques that improve scalability while minimizing routing overhead. A promising approach is the implementation of self–generated random identification circuits that exploit controlled process–variation behavior to generate unique IDs for each fabricated IC [108]. By intentionally designing circuit structures to produce statistically separable binary states, stable random bit generation may be achieved without external programming or additional routing. Such a technique could significantly improve scalability, simplify manufacturing, and reduce system complexity while allowing all ICs to remain physically identical.

Another important direction for future work involves the beam–steering phase shifter architecture. The implemented phase shifter required a relatively large control voltage approaching 10 V to achieve sufficient phase tuning, which presents significant integration challenges in modern small feature–size CMOS technologies due to device breakdown limitations and reduced voltage tolerance. Consequently, generating and distributing such voltages on–chip increases circuit complexity, power management overhead, and reliability concerns. Future research should therefore explore alternative passive low–power phase shifter topologies capable of achieving wide phase–tuning ranges while operating at substantially lower control voltages.

A further important direction for future work involves improving the timing robustness and jitter tolerance of the digital frame router presented in Chapters 4 and 5. Experimental measurements indicated that a small portion of the recovered data experienced transmission errors due to timing jitter and synchronization uncertainties within the recovered clock and routing network. Future work should therefore investigate improved timing optimization techniques to further reduce the SER and enhance overall communication reliability.

Future work may also focus on further optimization and refinement of the IC itself in terms of power consumption, operating speed, silicon area, robustness, and subsystem performance. Although the proposed IC successfully demonstrated the core proof–of–concept operation of the architecture, several areas for improvement were identified throughout the design and experimental validation stages.

References

[1] P. K. Bailleul, “A New Era in Elemental Digital Beamforming for Spaceborne Communications Phased Arrays,” *Proc. of the IEEE*, vol. 104, no. 3, pp. 623–632, 2016, doi: 10.1109/JPROC.2015.2511661.

[2] L. Rao *et al*., “5G beamforming techniques for the coverage of intended directions in modern wireless communication: In-depth review,” *Int. J. of Microw. and Wireless Technol.*, vol. 13, no. 10, pp. 1039–1062, 2020, doi: 10.1017/S1759078720001622.

[3] B. Ning *et al.*, “Beamforming Technologies for Ultra-Massive MIMO in Terahertz Communications,” *IEEE Open J. of the Commun. Soc.*, vol. 4, pp. 614–658, 2023, doi: 10.1109/OJCOMS.2023.3245669.

[4] Z. Xiao *et al.*, “A Survey on Millimeter-Wave Beamforming Enabled UAV Communications and Networking,” *IEEE Commun. Surv. and Tutor.*, vol. 24, no. 1, pp. 557–610, 2022, doi: 10.1109/COMST.2021.3124512.

[5] F. I. Urzaiz *et al*., “Digital Beamforming on Receive Array Calibration: Application to a Persistent X-Band Surface Surveillance Radar,” *IEEE Sens. J.*, vol. 21, no. 5, pp. 6752–6760, 2021, doi: 10.1109/JSEN.2020.3037781.

[6] K. F. Warnick *et al*., “High-Sensitivity Phased Array Receivers for Radio Astronomy,” *Proc. of the IEEE*, vol. 104, no. 3, pp. 607–622, 2016, doi: 10.1109/JPROC.2015.2491886.

[7] B. Yin and J. Chen, “Application of adaptive beamforming technology in underwater acoustic,” in *2023 3rd Int. Conf. on Neural Netw., Inf. and Commun. Eng. (NNICE)*, Guangzhou, China: IEEE, 2023, pp. 219–223. doi: 10.1109/NNICE58320.2023.10105792.

[8] A. Bansal, C. J. Panagamuwa, and W. G. Whittow, “State-of-the-Art Millimeter-Wave Beam Steering Antennas for Beyond 5G and 6G Networks: A comprehensive review,” 2024. doi: 10.1109/MAP.2024.3441378.

[9] T. Saeidi and S. Karamzadeh, “Enhancing CubeSat Communication Through Beam-Steering Antennas: A Review of Technologies and Challenges,” 2025. doi: 10.3390/electronics14040754.

[10] A. Brown, *Active Electronically Scanned Arrays: Fundamentals and Applications*. WILEY, 2022.

[11] K. Benson, “Phased Array Beamforming ICs Simplify Antenna Design,” Analog Dialogue. Accessed: May 15, 2026. [Online]. Available: https://api.semanticscholar.org/CorpusID:153316567.

[12] S. Kausar *et al*., “Comparative Analysis of Smart Beam-Steering Antennas for mm-Wave Communication Systems & 5G,” *Prog. In Electromagn. Res. B*, vol. 98, pp. 147–164, 2023, doi: 10.2528/PIERB22112301.

[13] C. A. Balanis, *Antenna Theory: Analysis and Design*, 2nd ed. WILEY, 1997.

[14] N. Javanbakht, “Analysis and Design of Low-Profile Reconfigurable Leaky- Wave Antennas Based on Substrate Integrated Waveguide for 5G Millimeter-Wave Applications,” Carleton University, 2021.

[15] Matthew N.O. Sadiku, *Elements of Electromagnetics*, 7th ed. Oxford University Press, 2018.

[16] S. Patel, “Effectively Overcoming RF PCB Antenna Design Issues.” Accessed: May 15, 2026. [Online]. Available: https://www.mwrf.com/technologies/components/article/21249767/mer-mar-electronics-effectively-overcoming-rf-pcb-antenna-design-issues.

[17] J. Pang *et al.*, “A 28-GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR,” *IEEE J. of Solid-State Circuits*, vol. 55, no. 9, pp. 2371–2386, 2020, doi: 10.1109/JSSC.2020.2995039.

[18] G. Federico *et al*., “A Review of Antenna Array Technologies for Point-to-Point and Point-to-Multipoint Wireless Communications at Millimeter-Wave Frequencies,” *Int. J. of Antennas and Propag.*, vol. 2021, no. 1, 2021, doi: 10.1155/2021/5559765.

[19] B. Kieniewicz, “Development of an Analogue Phased Array Beamformer for Wide Ku / K Band Applications Quick Beam-Forming Recap.” Accessed: May 15, 2026. [Online]. Available: https://engineeringconsultancy.eu/wp-content/uploads/2020/12/Ben-Kieniewicz-ARMMS-Nov-2019.pdf.

[20] X. Gu, D. Liu, and B. Sadhu, “Packaging and Antenna Integration for Silicon-Based Millimeter-Wave Phased Arrays: 5G and Beyond,” *IEEE J. of Microw.*, vol. 1, no. 1, pp. 123–134, 2021, doi: 10.1109/jmw.2020.3032891.

[21] D. Pivonka *et al*., “A mm-sized wirelessly powered and remotely controlled locomotive implant,” *IEEE Trans. on Biomed. Circuits and Syst.*, vol. 6, no. 6, pp. 523–532, 2012, doi: 10.1109/TBCAS.2012.2232665.

[22] A. Yakovlev, J. H. Jang, and D. Pivonka, “An 11 μw Sub-pJ/bit Reconfigurable Transceiver for mm-Sized Wireless Implants,” *IEEE Trans. on Biomed. Circuits and Syst.*, vol. 10, no. 1, pp. 175–185, 2016, doi: 10.1109/TBCAS.2014.2371031.

[23] A. I. Al-Kalbani, M. R. Yuce, and J. M. Redouté, “Performance of a biomedical implant communication system using PWM coded ASK,” in *2012 Int. Symp. on Commun. and Inf. Technol. (ISCIT)*, Gold Coast, QLD, Australia, 2012, pp. 133–138. doi: 10.1109/ISCIT.2012.6380877.

[24] “Serial Peripheral Interface (SPI).” Accessed: May 15, 2026. [Online]. Available: https://learn.sparkfun.com/tutorials/serial-peripheral-interface-spi/all.

[25] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed. WILEY, 2011. doi: 10.1142/9781848164079_0004.

[26] A. Ribeiro *et al*., “A Bandgap Voltage Reference With Only MOS Transistors.” Accessed: May 15, 2026. [Online]. Available: https://api.semanticscholar.org/CorpusID:12492968.

[27] A. Ciprut and E. G. Friedman, “Stability of on-chip power delivery systems with multiple low-dropout regulators,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 8, pp. 1779–1789, Aug. 2019, doi: 10.1109/TVLSI.2019.2914395.

[28] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, “A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a Beamformer Flip-Chip Unit Cell,” *IEEE J. of Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, 2018, doi: 10.1109/JSSC.2018.2791481.

[29] B. Rupakula, S. Zihir, and G. M. Rebeiz, “Low Complexity 54 – 63-GHz Transmit / Receive on Multilayer Organic Substrates With 64-QAM 30-Gbps Data Rates,” *IEEE Trans. on Microw. Theory and Tech.*, vol. 67, no. 12, pp. 5268–5281, 2019.

[30] A. Alhamed, G. Gultepe, and G. M. Rebeiz, “A Multi-Band 16–52-GHz Transmit Phased Array Employing 4 × 1 Beamforming IC With 14–15.4-dBm Psat for 5G NR FR2 Operation,” *IEEE J. of Solid-State Circuits*, vol. 57, no. 5, pp. 1280–1290, 2022.

[31] A. H. Aljuhani *et al*., “A Scalable Dual-Polarized 256-Element Ku-Band Phased-Array SATCOM Receiver with ±70° Beam Scanning,” in *2018 IEEE/MTT-S Int. Microw. Symp. - IMS*, Philadelphia, PA, USA, 2018, pp. 1203–1206. doi: 10.1109/MWSYM.2018.8439257.

[32] P. Uhlig *et al*., “Brick or tile? evaluation of integration concepts for microwave phased array antennas,” in *2020 IEEE 8th Electron. Syst.-Integr. Technol. Conf. (ESTC)*, Tønsberg, Norway, 2020, pp. 1–5. doi: 10.1109/ESTC48849.2020.9229703.

[33] Y. Yin *et al*., “A 24-29.5 GHz 256-Element 5G Phased-Array with 65.5 dBm Peak EIRP and 256-QAM Modulation,” in *2020 IEEE/MTT-S Int. Microw. Symp. (IMS)*, Los Angeles, CA, USA, 2020, pp. 687–690.

[34] X. He, Y. Cui, and M. M. Tentzeris, “Tile-based massively scalable MIMO and phased arrays for 5G/B5G-enabled smart skins and reconfigurable intelligent surfaces,” *Sci. Reports*, vol. 12, no. 1, pp. 1–10, 2022, doi: 10.1038/s41598-022-06096-9.

[35] A. H. Aljuhani *et al*., “Ultra-Low Cost Ku-Band Dual-Polarized Transmit and Receive Phased-Arrays for SATCOM and Point-to-Point Applications with

Bandwidths up to 750 MHz," in *2019 IEEE Int. Symp. on Phased Array Syst. and Technol. (PAST)*, Waltham, MA, USA, 2019. doi: 10.1109/PAST43306.2019.9021008.

[36] R. Valkonen, "Compact 28-GHz phased array antenna for 5G access," in *2018 IEEE/MTT-S Int. Microw. Symp. - IMS*, Philadelphia, PA, USA, 2018, pp. 1334–1337. doi: 10.1109/MWSYM.2018.8439223.

[37] Y. B. Kim, S. Lim, and H. L. Lee, "Electrically conformal antenna array with planar multipole structure for 2-D wide angle beam steering," *IEEE Access*, vol. 8, pp. 157261–157269, 2020, doi: 10.1109/ACCESS.2020.3019498.

[38] J. Pang *et al*., "A 28-GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation," in *2020 IEEE Symp. on VLSI Circuits*, Honolulu, HI, USA, 2020, pp. 3–4. doi: 10.1109/VLSICircuits18222.2020.9162882.

[39] T. Hoffmann, M. Livadaru, and D. Jensen, "IMPACT common module and S-band planar array beamforming measurements," in *2018 IEEE Radar Conf. (RadarConf 2018)*, Oklahoma City, OK, USA, 2018, pp. 588–592. doi: 10.1109/RADAR.2018.8378625.

[40] H.-T. Kim *et al.*, "A 28-GHz CMOS Direct Conversion Transceiver With Packaged 2×4 Antenna Array for 5G Cellular System," *IEEE J. of Solid-State Circuits*, vol. 53, no. 5, pp. 1245–1259, 2018, doi: 10.1109/jssc.2018.2817606.

[41] J. C. S. Chieh *et al*., "Dual Polarized Ku-Band Phased Array on ROHACELL utilizing Silicon Beamforming Chipsets," in *2019 IEEE Int. Symp. on Phased Array Syst. and Technol. (PAST)*, Waltham, MA, USA, 2019, pp. 1–5. doi: 10.1109/PAST43306.2019.9020845.

[42] S. Zheng *et al.*, "A 94-GHz 16T1R Hybrid Integrated Phased Array With ±50◦ Scanning Range for High-Date-Rate Communication," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 2, pp. 948–961, Feb. 2024, doi: 10.1109/TCSI.2023.3335324.

[43] Z. Hu *et al*., “A 16-Channel 3.1-25.5-GHz Phased-Array Receive Beamformer IC with Two Simultaneous Beams and 2.0-2.4-dB NF for C/X/Ku/Ka-Band SATCOM,” *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 5, pp. 2773–2785, May 2024, doi: 10.1109/TMTT.2024.3349518.

[44] C. Weston *et al*., “A 64 Element 28GHz Digital Beamformer Based on Tileable Synchronized Distributed Beamforming Chiplets,” *IEEE Open J. Solid-State Circuits Soc.*, vol. 5, pp. 424–436, 2025, doi: 10.1109/OJSSCS.2025.3625891.

[45] X. Lei *et al*., “A 4×4 5-6GHz CMOS Wi-Fi Transceiver Front-End for Fiber-to-the-Room with Analog Beamforming Achieving 27dBm 1024 QAM MCS11 EIRP and -45dB EVM Floor,” in *2024 Proc. Custom Integr. Circuits Conf.*, Denver, CO, USA, 2024, pp. 1–2. doi: 10.1109/CICC60959.2024.10529059.

[46] N. Li *et al*., “A Ka-Band 64-Element Four-Beam Phased Array Receiver With Inter-Beam Interference Cancellation,” *IEEE Trans. Microw. Theory Techn.*, vol. 73, pp. 221–233, 2025, doi: 10.1109/LMWT.2023.3265022.

[47] Y. Yin *et al*., “A 37-42 GHz 8x8 Phased-Array for 5G Communication Systems with 48-50 dBm EIRP,” in *2019 IEEE MTT-S Int. Microw. Symp. (IMS)*, Boston, MA, USA, 2019, pp. 480–483. doi: 10.1109/mwsym.2019.8700867.

[48] C. Unsalan and B. Tar, *Digital System Design with FPGA: Implementation Using Verilog and VHDL*, 1st ed. McGraw-Hill Education, 2017.

[49] J. Chen and S. Huang, “Analysis and Comparison of UART, SPI and I2C,” in *2023 IEEE 2nd Int. Conf. on Elect. Eng., Big Data and Algorithms (EEBDA)*, Changchun, China, 2023, pp. 272–276. doi: 10.1109/EEBDA56825.2023.10090677.

[50] Y. H. Zhang *et al*., “DDS-PLL Phased Source for Ka-Band Beam Control Phased Array Receiver,” in *2018 Proc. 12th Int. Symp. Antennas Propag. EM Theory (ISAPE)*, Hangzhou, China, 2018, pp. 1–4. doi: 10.1109/ISAPE.2018.8634073.

[51] D. Li and D. Zhao, “A Low-Power Digital Control Core with High-Speed SPI Slave for Phased Array Application in 40nm CMOS,” in *2019 IEEE Int. Conf. on Int.*

Circuits, Technol. and Appl. (ICTA), Chengdu, China, 2019, pp. 67–68. doi: 10.1109/ICTA48799.2019.9012878.

[52] X. Li *et al*., "Design of micro-phased array antenna control system," in *2021 2nd China Int. SAR Symp. (CISS)*, Shanghai, China, 2021, pp. 1–5. doi: 10.23919/CISS51089.2021.9652222.

[53] D. Del Rio *et al*., "Design of Integrated Control Circuits for mm-Wave Phased Arrays in 55-nm BiCMOS," in *2019 XXXIV Conf. on Des. of Circuits and Integr. Syst. (DCIS)*, Bilbao, Spain, 2019, pp. 1–5. doi: 10.1109/DCIS201949030.2019.8959897.

[54] H. G. Garakani *et al*., "Digital Implementation of a Beam Control Scheme in Phased Array for Satellite Communications," in *2018 18th Int. Symp. on Antenna Technol. and Appl. Electromagn. (ANTEM)*, 2018, pp. 1–3. doi: 10.1109/ANTEM.2018.8572875.

[55] M. Y. W. Chia *et al*., "Electronic Beam-Steering Design for UWB Phased Array," *IEEE Trans. on Microw. Theory and Tech.*, vol. 54, no. 6, pp. 2431–2438, 2006, doi: 10.1109/TMTT.2006.875300.

[56] G. H. Ko *et al*., "24-GHz 4TX-4RX Phased Array Transceiver with Automatic Beam Steering Mode for FMCW Radar Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 5, pp. 3065–3075, May 2024, doi: 10.1109/TMTT.2023.3320741.

[57] F. Tesolin *et al*., "A 10-GHz Localized-LO-Phase-Shifting Phased-Array Transmitter," in *2025 IEEE MTT-S Int. Microw. Symp. Dig.*, 2025, pp. 386–389. doi: 10.1109/IMS40360.2025.11103785.

[58] X. Zhi *et al*., "A Self-Adaptive Phased Array Conformed on a Highly Flexible Aperture," *IEEE Trans. Microw. Theory Techn.*, vol. 73, no. 3, pp. 1821–1836, 2025, doi: 10.1109/TMTT.2024.3458018.

[59] B. Dai *et al.*, “D-Band, 2-D Scalable CMOS Planar Phased Array Transmitters With λ/2-Spaced Integrated Antenna,” *IEEE Trans. Microw. Theory Techn.*, vol. 73, no. 11, pp. 9534–9549, 2025, doi: 10.1109/TMTT.2025.3595454.

[60] D. Del Rio *et al.*, “A D-Band 16-Element Phased-Array Transceiver in 55-nm BiCMOS,” *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 2, pp. 854–869, 2023, doi: 10.1109/TMTT.2022.3203709.

[61] D. C. Gaydos, P. Nayeri, and R. L. Haupt, “Adaptive Beamforming With Software-Defined-Radio Arrays,” *IEEE Access*, vol. 10, pp. 11669–11678, 2022, doi: 10.1109/ACCESS.2022.3144959.

[62] A. Manco and V. Ugo, “Beam Steering Controller Architectures for an Active Electrically Scanned Array Antenna: Comparison and a Cost Effective Implementation,” *Int. J. of Comput. Appl.*, vol. 179, no. 52, pp. 1–8, 2018, doi: 10.5120/ijca2018917091.

[63] R. Schalk *et al.*, “A 4-Element Passive-Beamforming CT- ΔΣ ADC for Spatial Selectivity in Automotive Radar,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 72, no. 9, pp. 4431–4441, 2025, doi: 10.1109/TCSI.2025.3561950.

[64] M. H. Eissa *et al.*, “A Fully Integrated Modular 2×4 220–260 GHz Beam-Forming Transmitter and Receiver With 50 Gbps Wireless Transmission in SiGe:C BiCMOS,” *IEEE Trans. THz Sci. Technol.*, vol. 15, no. 5, pp. 805–820, 2025, doi: 10.1109/TTHZ.2025.3573157.

[65] B. Bailey, “The Problem With Clocks.” Accessed: May 15, 2026. [Online]. Available: https://semiengineering.com/the-problem-with-clocks/.

[66] “Phase-Lock Loop-Based (PLL) Clock Driver: A Critical Look at Benefits Versus Costs.” Accessed: May 15, 2026. [Online]. Available: https://www.ti.com/lit/pdf/scaa033a.

[67] T. Liu and Y. Wang, “IP design of universal multiple devices SPI interface,” in *2011 Proc. IEEE Int. Conf. Anti-Counterfeiting, Security Identification*, Xiamen, China, 2011, pp. 169–172. doi: 10.1109/ASID.2011.5967443.

[68] F. Yuan, “Design techniques for ASK demodulators of passive wireless microsystems: A state-of-the-art review,” *Analog Integr. Circuits and Signal Process.*, vol. 63, no. 1, pp. 33–45, 2010, doi: 10.1007/s10470-009-9379-6.

[69] V. Fiore *et al*., “A 13.56MHz RFID Tag with Active Envelope Detection in an Organic Complementary TFT Technology,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Francisco, CA, USA, 2014, pp. 492–493. doi: 10.1109/ISSCC.2014.6757526.

[70] Y. Rezaeiyan *et al.*, “A 4.5 μW Miniaturized 3-Channel Wireless Intra-Cardiac Acquisition System,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 17, no. 5, pp. 1097–1110, 2023, doi: 10.1109/TBCAS.2023.3294560.

[71] X. Zhong and C.-W. Sham, “An SoC for Qi-compliant Wireless Power Transmitter With Enhanced EMI Performance,” in *2019 Proc. 6th Int. Conf. Syst. Informat. (ICSAI)*, Shanghai, China, 2019, pp. 725–728. doi: 10.1109/ICSAI48974.2019.9010208.

[72] A. Barakat, M. K. Bin Zulkalnain, and R. Pokharel, “Comparator-less ASK-PWM CDR Circuit for Forward Data Communication Over A Single Channel Wireless Power and Data Transfer System,” in *2023 Proc. IEEE Wireless Power Technol. Conf. Expo (WPTCE)*, San Diego, CA, USA, 2023, pp. 1–4. doi: 10.1109/WPTCE56855.2023.10215978.

[73] S. K. An *et al.*, “Design for a simplified cochlear implant system,” *IEEE Trans. Biomed. Eng.*, vol. 54, no. 6, pp. 973–982, Jun. 2007, doi: 10.1109/TBME.2007.895372.

[74] V. W. Leung *et al*., “Distributed Microscale Brain Implants with Wireless Power Transfer and Mbps Bi-directional Networked Communications,” in *2019 Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Austin, TX, USA, 2019, pp. 1–4. doi: 10.1109/CICC.2019.8780289.

[75] I. Habibagahi, J. Jang, and A. Babakhani, “Miniaturized Wirelessly Powered and Controlled Implants for Vagus Nerve Stimulation,” in *2022 IEEE RFIC Symp. Dig. Papers*, 2022, pp. 51–54. doi: 10.1109/RFIC54546.2022.9863172.

[76] J. D. Myers *et al*., “Refractive waveguide non-mechanical beam steering (NMBS) in the MWIR,” in *Photonic Instrum. Eng. V*, San Francisco, CA, United States, 2018, pp. 1–7. doi: 10.1117/12.2290379.

[77] T. Cooney *et al*., “Transmit/receive module for L-band phased array synthetic aperture radar with polarisation control,” in *2013 Int. Conf. on Radar*, Adelaide, SA, Australia, 2013, pp. 167–172. doi: 10.1109/RADAR.2013.6651979.

[78] D. Mitra, P. Roy, and D. Dawn, “A Variable Gain CMOS Phased Shifter for Phased Array Antenna Applications,” *Microw. and Opti. Technol. Lett.*, vol. 59, no. 2, pp. 324–328, 2017, doi: 10.1002/mop.

[79] S. Magierowski, “Small Loop Antenna Calculations.” [Online]. Available: https://wiki.eecs.yorku.ca/lab/emil/_media/technotes:loopantcalcs1.pdf.

[80] T. A. Milligan, *Modern Antenna Design*, 2nd ed. WILEY, 2005. doi: 10.1002/0471720615.

[81] K. Y. Yazdandoost and K. Sato, “Radiation resistance of rectangular microstrip antenna,” in *2001 Asia-Pacific Microw. Conf. (APMC)*, Taipei, Taiwan, 2001, pp. 1159–1162. doi: 10.1109/apmc.2001.985338.

[82] “5G/NR - Beam Management.” Accessed: May 15, 2026. [Online]. Available: https://www.sharetechnote.com/html/5G/5G_Phy_BeamManagement.bak.

[83] A. Bole, A. Wall, and A. Norris, *Radar and ARPA Manual: Radar, AIS and Target Tracking for Marine Radar Users*, 3rd ed. ELSEVIER, 2013.

[84] R. T. D, S. K. C. Korada, and S. K. Kotamraju, “An improved peak side lobe reduction method for linear array antenna for military applications,” *Int. J. of Intell. Comput. and Cybern.*, vol. 14, no. 2, pp. 186–198, 2021, doi: https://doi.org/10.1108/IJICC-09-2020-0127.

[85] N. Shinohara, *Wireless Power Transfer via Radiowaves*. WILEY, 2014. doi: 10.1002/9781118863008.

[86] S. Marsh, *Practical MMIC Design*. ARTECH HOUSE, 2006.

[87] K. Datta *et al*., "PSO optimized concurrent dual-band LNA with RF switch for better inter-band isolation," in *2010 5th Eur. Conf. on Circuits and Syst. for Commun. (ECCSC)*, Belgrade, Serbia, 2010, pp. 59–62.

[88] B. H. Ku and S. Hong, "6-bit CMOS digital attenuators with low phase variations for X-band phased-array systems," *IEEE Trans. on Microw. Theory and Tech.*, vol. 58, no. 7, pp. 1651–1663, 2010, doi: 10.1109/TMTT.2010.2049691.

[89] Y. Y. Huang *et al*., "Highly linear RF CMOS variable attenuators with adaptive body biasing," *IEEE J. of Solid-State Circuits*, vol. 46, no. 5, pp. 1023–1033, 2011, doi: 10.1109/JSSC.2011.2117530.

[90] D. M. Pozar, *Microwave Engineering*, 4th ed. WILEY, 2011.

[91] C. S. Lin *et al*., "Design of a reflection-type phase shifter with wide relative phase shift and constant insertion loss," *IEEE Trans. on Microw. Theory and Tech.*, vol. 55, no. 9, pp. 1862–1868, 2007, doi: 10.1109/TMTT.2007.903346.

[92] S. Soni and S. Gupta, "WPT Techniques based Power Transmission: A State-of-Art Review," in *2022 13th Int. Conf. on Comput. Commun. and Netw. Technol. (ICCCNT)*, Kharagpur, India, 2022, pp. 1–6. doi: 10.1109/ICCCNT54827.2022.9984606.

[93] A. Azad *et al*., "A Smart Autonomous WPT System for Electric Wheelchair Applications with Free-Positioning Charging Feature," *IEEE J. of Emerging and Selected Topics in Power Electron.*, vol. 8, no. 4, pp. 3516–3532, 2020, doi: 10.1109/JESTPE.2018.2884887.

[94] F. N. Ibrahim, N. A. M. Jamail, and N. A. Othman, "Development of wireless electricity transmission through resonant coupling," in *4th IET Clean Energy and Technol. Conf. (CEAT)*, Kuala Lumpur, Malaysia, 2016, pp. 1–5. doi: 10.1049/cp.2016.1290.

[95] J. I. Agbinya, *Wireless Power Transfer*, 2nd ed. River Publishers, 2016.

[96] S. Valtchev, E. Baikova, and L. Jorge, “Electromagnetic field as the wireless transporter of energy,” *Facta universitatis - series: Electron. and Energetics*, vol. 25, no. 3, pp. 171–181, 2012, doi: 10.2298/fuee1203171v.

[97] H. Hoang and F. Bie, “Maximizing Efficiency of Electromagnetic Resonance Wireless Power Transmission Systems with Adaptive Circuits,” in *Wireless Power Transfer - Principles and Engineering Explorations*, InTech, 2012, ch. 11, pp. 207–226. doi: 10.5772/28922.

[98] S. Beeby and N. M. White, *Energy Harvesting for Autonomous Systems*. ARTECH HOUSE, 2010. doi: 10.1109/mie.2012.2182863.

[99] S. Nikoletseas, Y. Yang, and A. Georgiadis, *Wireless power transfer algorithms, technologies and applications in ad Hoc communication networks*. Springer, 2016. doi: 10.1007/978-3-319-46810-5.

[100] E. A. Jorswieck, “Next-Generation Multiple Access: From Basic Principles to Modern Architectures,” *Proc. IEEE*, vol. 112, no. 9, pp. 1149–1178, 2024, doi: 10.1109/JPROC.2024.3412423.

[101] A. F. M. S. Shah *et al*., “Survey and performance evaluation of multiple access schemes for next-generation wireless communication systems,” *IEEE Access*, vol. 9, pp. 113428–113442, 2021, doi: 10.1109/ACCESS.2021.3104509.

[102] K. Arshak *et al*., “Modelling and simulation of wireless sensor system for health monitoring using HDL and Simulink® mixed environment,” *IET Comput. and Digital Tech.*, vol. 1, no. 5, pp. 508–518, 2007, doi: 10.1049/iet-cdt:20050206.

[103] “SPI Block Guide,” OpenCores. Accessed: May 15, 2026. [Online]. Available: https://opencores.org/usercontent/doc/1499360489.

[104] A. K. Gupta *et al*., “Design and Implementation of High-Speed Universal Asynchronous Receiver and Transmitter (UART),” in *2020 Proc. 7th Int. Conf. Signal Process. Integr. Netw. (SPIN)*, Noida, India, 2020, pp. 295–300. doi: 10.1109/SPIN48934.2020.9070856.

[105] Y. Li, T. Jin, and W. Tang, “Design and Implementation of I2C Bus Controller Based on FPGA,” in *2025 Proc. IEEE 8th Adv. Inf. Technol., Electron. Autom. Control Conf. (IAEAC)*, Guiyang, China, 2025, pp. 1344–1347. doi: 10.1109/IAEAC65194.2025.11166419.

[106] E. Barteselli *et al*., “Design Techniques for Low-Power and Low-Voltage Bandgaps †,” *Electricity*, vol. 2, no. 3, pp. 271–284, Sep. 2021, doi: 10.3390/electricity2030016.

[107] K. Ueno *et al*., “A 300 nW, 15 ppm/∘C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs,” *IEEE J. of Solid-State Circuits*, vol. 44, no. 7, pp. 2047–2054, 2009, doi: 10.1109/JSSC.2009.2021922.

[108] J. H. Mitchell-Moreno and G. E. Flores-Verdad, “A Low Bit Instability CMOS PUF Based on Current Mirrors and WTA Cells,” *J. Electron. Testing Theory Appl.*, vol. 39, no. 5–6, pp. 611–620, Dec. 2023, doi: 10.1007/s10836-023-06085-4.

Appendix: List of Commercial Components used in Thesis

Table A.1 Commercial off-the-shelf components used throughout the thesis.

Component	Manufacturing Company	Location	Datasheet Website Link
AS321KTR–G1	Diodes Incorporated	Plano, TX, USA	https://www.diodes.com/assets/Datasheets/AS321.pdf
BSH103BK	Nexperia	Nijmegen, Netherlands	https://assets.nexperia.com/documents/data-sheet/BSH103BK.pdf
BSH205G2	Nexperia	Nijmegen, Netherlands	https://assets.nexperia.com/documents/data-sheet/BSH205G2.pdf
BU5265HFV–TR	ROHM Semiconductor	Kyoto, Japan	https://www.rohm.com/datasheet?p=BU5265HFV&dist=Digi-key&media=referral&source=digi-key.com&campaign=Digi-key
HG908PCR	L–Com	North Andover, MA, USA	https://www.l-com.com/Images/Downloadables/Datasheets/ds_HG908PCX-XX.pdf?srsltid=AfmBOornTs2-pYaVsR6I8he6s6kTk1xVYlVIqPlxo79QFAW61QHVdKgI
LND150K1–G	Microchip Technology	Chandler, AZ, USA	https://ww1.microchip.com/downloads/aemDocuments/documents/OTH/ProductDocuments/DataSheets/LND150-LND250-N-Channel-Depletion-Mode-DMOS-FETs-Data-Sheet-20005454A.pdf
OP281GSZ	Analog Devices	Wilmington, MA, USA	https://www.analog.com/media/en/technical-documentation/data-sheets/OP281_OP481.pdf
S–19213BC0A–V5T2U7	ABLIC Inc.	Tokyo, Japan	https://mm.digikey.com/Volume0/opasdata/d220001/medias/docus/7159/S19213_E.pdf
SMS3922–079LF	Skyworks Solutions, Inc.	Irvine, CA, USA	https://www.skyworksinc.com/-/media/774A119F8939424F801CA8A44572D829.pdf
SMV1249–079LF	Skyworks Solutions, Inc.	Irvine, CA, USA	https://www.skyworksinc.com/Products/Diodes/SMV1249-Series
SMV1430–040LF	Skyworks Solutions, Inc.	Irvine, CA, USA	https://www.skyworksinc.com/-/media/5586FCB47A2640488FB7FE939CD86306.pdf
TLV70220PDBVR	Texas Instruments	Dallas, TX, USA	https://www.ti.com/general/docs/suppproductinfo.tsp?distId=10&gotoUrl=https%3A%2F%2Fwww.ti.com%2Flit%2Fgpn%2Ftlv702
TLV9152IDR	Texas Instruments	Dallas, TX, USA	https://www.ti.com/lit/ds/symlink/tlv9151.pdf