A Clock Multiplier Based on an Injection Locked Ring Oscillator

by

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To my one of a kind mother and in the memory of my ever inspiring father.

Abstract

Clock multipliers are among the most critical elements in high speed digital circuits. Power consumption, area, jitter and wide tuning range are key design metrics in these circuits. To provide a wide range of clock frequencies, Digitally Controlled Ring Oscillators (DCROs), whose frequencies are discretely tuned using a Frequency Code Word (FCW), have been investigated in recent studies. They have several advantages over LC-based Voltage Controlled Oscillators (VCO) including simplicity of design, small die area (i.e. no large inductors), better compatibility with deep submicron CMOS processes, ability to offer multiple output phases, and wider tuning range.

A compact differential Injection Locked Clock Multiplier (ILCM) based on an injection locked DCRO is implemented in this thesis. As the transistor features continuously shrink and the supply voltage is reduced, ILCMs are becoming more prone to issues such as increased effect of random mismatch, increased device noise, susceptibility of the design to noise coupling and vulnerability to Process Voltage and Temperature (PVT) variations. Furthermore, ILCMs in recent System on a Chip (SoCs) have stringent design requirements including accurate frequency tuning, fine fractional resolution, high levels of integration and better amenability to technology scaling. In the proposed ILCM, multiple techniques were used to address deep submicron CMOS design challenges, as well as modern applications' requirements. The design is fully digital, synthesizable and automatically placed and routed. All circuit blocks were implemented using digital design flow and designed using a Hardware Description Language (HDL). This allows the design to be more easily ported to deep submicron processes. Online or offline PVT calibration can be performed using a replica oscillator and high speed digital counters to track frequency drifts with PVT variations. A DCRO based on a matrix structure has been utilized to reduce period variations due to random mismatch. The DCRO is built

up from pseudo differential delay cells to enhance design immunity to noise coupling. The key thesis contributions are implementing a new DCRO structure using fully synthesizable differential structure, utilizing a novel PVT calibrator that can compensate for frequency mismatch between the main DCRO and its replica, and using a low complexity fractional ILCM technique that achieves a fine fractional resolution with few number of ring oscillator stages.

Designed in a TSMC 65 nm GP CMOS process with no analog or RF enhancements, the proposed ILCM frequency ranges from 1.0 to 1.8 GHz and occupies $124.5\mu m \times 170\mu m$ of chip area. The ILCM can operate in integer or fractional mode for multiplication ratios up to 9. At 1.7 GHz and 1.1 V, the measured integrated RMS jitter (1 kHz to 30 MHz) for the 3^{rd} and 9^{th} multiplication factors are 197 fs and 381 fs, respectively. The ILCM consumes 13.25 mW of power and has a fraction resolution of $f_{ref}/32$. Furthermore, it achieves a jitter-power FOM of -241 dB, when measured at room temperature and 1.1 V. When tested in the presence of switching noise, it provides up to 7 dB improvement in phase noise when compared to a single ended version of the ILCM. In the presence of voltage variations (from 0.9 V to 1.1 V) and temperature variations (from $30°C$ to $70°C$), the maximum integrated RMS jitter variation observed was 50 fs.

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List of Abbreviations

A/D	Analog to Digital
ADPLL	All-Digital Phase Locked Loop
AMOS	Accumulation-mode Metal Oxide Semiconductor
CDR	Clock Data Recovery
CPU	Central Processing Unit
CM	Clock Multiplier
D2D	Die to Die
DCO	Digitally Controlled Oscillator
DCRO	Digitally Controlled Ring Oscillator
DPLL	Digital Phase Locked Loop
DSP	Digital Signal Processing
DTC	Digital-to-Time Converter
FCW	Frequency Code Word
FLL	Frequency Locked Loop
FPGA	Field Programmable Gate Array
FTL	Frequency Tracking Loop
GPIB	General Purpose Interface Bus
HDL	Hardware Description Language
I/O	Input Output
IC	Integrated Circuit
IDAC	Current Digital to Analog Converter
ILCM	Injection Locking Clock Multiplier
IMOS	Inversion-mode Metal Oxide Semiconductor

IoT	Internet of Things
LDO	Low Drop Out
MDLL	Multiplying Delay Locked Loop
MIM	Metal Insulator Metal
MOS	Metal Oxide Semiconductor
NBW	Noise-suppression Bandwidth
OTW	Oscillator Tuning Word
P&R	Place and Route
PCB	Printed Circuit Board
PLL	Phase Looked Loop
PN	Phase Noise
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PVT	Process, Voltage and Temperature
RO	Ring Oscillator
RMS	Root Mean Square
RTL	Register Transfer Level
SMA	Sub-Miniature version A
SNR	Signal to Noise Ratio
SSB	Single Side Band
SoC	System on a Chip
TDC	Time to Digital Converter
VCDL	Voltage Controlled Delay Line
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integrated-systems
VT	Voltage and Temperature
WID	With In Die

List of Symbols

α	Relative frequency error
β	Current factor
ε	Error between interploteed DCRO1 frequency and the operating frequency
κ	Realignment factor
γ_N	NMOS fraction of the gate length
γ_P	PMOS fraction of the gate length
$\Delta\Sigma$	Delta-Sigma
ΔC	Capacitance difference
Δt	Time delay
Δw	Offset frequency
δ	Rise/fall time of non-ideal square wave
ζ	Pulse width of non-ideal square wave
τ_d	Time delay of an inverter
τ_{dN}	NMOS propagation delay
τ_{dP}	PMOS propagation delay
θ	Phase difference between I_{inj} and I_{osc}
$\theta_e[n]$	Phase error between free running and reference instances
$\theta_{INJ-RO}(z)$	Phase error function at the RO output under injection in z-domain
$\theta_{inst-RO}[nT_{ref}^{-}]$	Free-running phase shift
$\theta_{out}[n]$	Phase shift due to jitter
$\theta_{RO}(z)$	RO free-running phase shit function in z-domain
$\theta_{ref}[nT_{ref}]$	Reference phase
$\theta_{ref}(z)$	Reference phase error function in z-domain

σ_{β}^2	Random variations in current factor
σ_{τ}	Jitter
σ_{τ}^2	Jitter variance
$\sigma_{\tau_d}^2$	Variance in time delay
$\sigma_{\tau_{dN}}^2$	Variance in an NMOS propagation delay
$\sigma_{\tau_{dP}}^2$	Variance in a PMOS propagation delay
σ_{T}^2	Variance in DCRO period
$\sigma_{V_t}^2$	Random variations in threshold voltage
$\mathcal{L}(\Delta f)_{free}$	Free-running one-sided phase noise
$\mathcal{L}(\Delta f)_{injection}$	Injection locked one-sided phase noise
$\mathcal{L}(\Delta f)_{total}$	Total SSB output phase noise
$\mathcal{L}(\Delta f)_{REF}$	Input reference signal phase noise
$\mathcal{L}(\Delta f)_{REF_{out}}$	Refernece phase noise at the ILCM output
$\mathcal{L}(\Delta w)$	SSB phase noise
$A(s)$	Voltage gain transfer function per stage
A	Voltage gain per stage
A_{β}	Current factor technology parameter
A_{Vt}	Threshold voltage technology parameter
C	Capacitor
C_{ox}	Oxide capacitor
$Diff_{init,i}$	Initial difference between DCRO1 and DCRO2 frequencies
$Diff_{intp}$	Interpolated difference between DCRO1 and DCRO2 frequencies
$F(s)$	Feedback transfer function
f_{ERR}	Frequency error
f_L	One-sided frequency lock range
$f_{hi1,init,i}$	Initial DCRO1 free running frequency
$f_{hi1,intp}$	Interpolated DCRO1 free running frequency
$f_{hi2,i}$	DCRO2 free running frequency

$f_{hi2,init,i}$	Initial DCRO2 free running frequency
f_{max}	Maximum output frequency of the oscillator
f_{out}	RO output frequency
f_{osc}	Oscillating frequency
f_{ref}	Reference frequency
G_m	Transistor transconductance
$G(s)$	Feedback gain
$H(s)$	Open-loop gain
$H_{rl}(z)$	Phase realignment transfer function
$H_{up}(z)$	Up converted reference transfer function
I_C	Capacitor current
I_{osc}	Oscillator current
I_{inj}	Injector current
I_N	NMOS drain current
I_P	PMOS drain current
j	Number of consecutive injections per stage
K	Multiplication factor
K_{DCO}	Digital controlled oscillator gain
K_{fN}	NMOS empirical coefficient
K_{fP}	PMOS empirical coefficient
K_{VCO}	Voltage controlled oscillator gain
k	Boltzmann constant
L	Inductor
L_N	NMOS channel length
L_P	PMOS channel length
M	Fractional multiplication factor
M_{hi2}	Mean of frequencies of DCRO2 in calibration phase II
$M_{hi2,init}$	Mean of frequencies of DCRO2 in calibration phase I

N	Integer multiplication factor
N_{osc}	Number of stages
n	Number of counter bits
P_{noise}	Noise power
PH_{av}	Average phase shift per reference cycle
Q	Quality factor
R	Resistance
r	Ratio between I_{ref} and I_{osc}
$S_{iN}^{1/f}(f)$	NMOS flicker noise current spectral density
$S_{iP}^{1/f}(f)$	PMOS flicker noise current spectral density
$S_{vN}^{1/f}(f)$	NMOS flicker noise PSD
T	Temperature
U	Number of parallel transistors
V_{cont}	Control voltage
V_{DD}	Supply voltage
V_f	Feedback voltage
V_i	Input voltage
V_o	Output voltage
V_m	Switching voltage
V_t	Threshold voltage
V_{tN}	NMOS threshold voltage
V_{tP}	PMOS threshold voltage
W_N	NMOS channel width
W_P	PMOS channel width
w_L	One-sided angular frequency lock range
w_{max}	Maximum reference frequency
w_{min}	Minimum reference frequency
w_o	Angular frequency at $V_{cont} = 0$

w_{out}	Angular output frequency
w_{osc}	Angular oscillating frequency
w_p	Pole angular frequency
w_{ref}	Reference angular frequency

1

Introduction

1.1 Motivation

In this 21^{st} century, in the face of an ever-increasing demand for faster data transfer, the need for high-speed Clock Multipliers (CMs) has increased considerably. High data-rate systems require CMs that can operate at high frequencies while maintaining low area, low power, low cost and high level of integration. In these systems, CMs play an essential role in the overall system performance by providing precise low noise clock signals that can be used in clock generation, clock data recovery, data conversion and frequency synthesis [1][2][3][4]. Uncertainty in a clock edge position (jitter) can cause errors and deteriorate the system's performance. For instance, in microprocessors and Digital Signal Processing (DSP) units, clock jitter specifications affect the system's net speed, as more conservative timing margins are required for correct operation. Another example

is in frequency synthesizers, where noisy clock signals can degrade a transceiver's Signal-to-Noise Ratio (SNR). To enhance clock signal purity, an injection locking technique was first investigated in [5]. In this technique, a low noise periodic reference signal, typically a sinusoidal or square wave, is introduced to correct the oscillator output transitions to be aligned with those of the reference in the time domain. The reference frequency or one of its harmonics needs to be close to the oscillation frequency of the oscillator so that the oscillator frequency tracks its frequency, hence the jitter is reduced. The range of frequency over which the oscillation frequency can be locked into the reference or one of its harmonics is called the locking bandwidth. Within the locking bandwidth, the noise of an oscillator is suppressed significantly [6]. With technology scaling, oscillator flicker noise corner frequency has increased to tens of MHz [7]. As a result, designing a CM with wide Noise suppression Bandwidth (NBW) is crucial in advanced process nodes. A CM based on a typical type II Digital Phase Locked Loop (DPLL) has a limited NBW of $f_{ref}/10$, where f_{ref} is the reference signal frequency and suffers from conflicting NBW requirements between the Time to Digital Converter (TDC) and oscillator [8]. On the other hand, Injection Locked Clock Multipliers (ILCMs) have a wider NBW of $f_{ref}/6$ [3] and eliminate the need for a power-hungry high resolution TDCs to achieve low jitter. For these reasons, ILCMs have gained attention recently in deep submicron CMOS designs [1][9][10][11].

Compact ILCMs are desirable in modern electronic devices. This is due to several reasons: the manufacturing cost of a design depends on the silicon area occupied, small design area allows mass-production deployment of CM in portable devices and also helps achieving high levels of integration into a single chip [12]. Therefore, ILCMs based on Ring Oscillators (RO) have been investigated intensively in state-of-the-art publications [6][13][14][15][16]. Their advantages of low area, wide frequency tuning range and multiphase outputs make them an attractive choice for various applications [17]. They are excellent candidates for applications that require multiple clock sources for different modules such as System on a Chip (SoC), modern multicore processors, Field Programmable

Gate Array (FPGA) and Input Output (I/O) interfaces [7][9][18][19][20]. They are also used as frequency synthesizers in Internet of Things (IoT) medical applications [21][22] and GPS receivers [23]. Compared to LC-based oscillators, ROs have poorer phase noise (PN). Thanks to the injection locking technique, ILCMs based on ROs can achieve comparable PN performance to LC-oscillators for frequencies below 10 GHz [7]. Furthermore, the low integration levels of LC-oscillators and custom digital CMs are bottlenecks when migrating designs to new processes. Another advantage of ILCMs based on RO is that they can be all digital and fully synthesizable which make them easily ported to advanced technologies with shorter design times [24][25][26]. In addition, all digital designs have many benefits including the use of a standard digital design flow, better noise immunity, fast design turnaround time and improved scalability and portability [12][26][27]. Fully synthesizable designs are described in HDL language then its blocks are mapped to standard cells by the aid of a synthesis tool and finally the layout is automatically generated by the aid of CAD tools without the need for custom layout enhancements. Consequently, this work proposes an all digital and fully synthesizable ILCM.

With increasing chip size, design complexity and switching interference from high-speed circuits, ILCMs require improved power supply and substrate noise rejection [28]. Digital switching noise degrades the phase noise and jitter performance of ILCMs [29]. Additionally, Process Voltage Temperature (PVT) variations also affect the ILCM performance. These two factors cause the free-running frequency to drift from the target frequency resulting in large levels of reference spur and increase jitter. According to [30] and [31], a reference spur as high as -20 dBc can be caused by 1% frequency deviation, when the multiplication factor is 10. Therefore, calibration is crucial to achieve the intended performance. Calibration using conventional Phase Locked Loops (PLLs) has potential drawbacks including poor free-running frequency tracking under locking conditions and stability problem due to PLL calibration while injection locking [2][24][32]. Therefore, this work investigates the use of a differential RO structure in the proposed ILCM and the implementation of a Frequency Lock Loop (FLL) based PVT calibrator to reduce the

effects of switching noise, as well as PVT variations. Another factor that can contribute to large reference spurs in the ILCM is the phase offset between the oscillator output and the reference signal due to errors in the PVT calibrator caused by random mismatch [14]. This problem is addressed in this work as random mismatch is reduced because of the use of a delay matrix rather than a single delay row as found in previous designs [3][24].

1.2 Research objectives

In order to achieve high performance and fulfill design requirements with the aid of low complexity digital circuits, this thesis main research objectives are:

- Designing a compact fully synthesizable RO that can be digitally tuned with an accurate frequency step size.
- Reducing RO jitter by using a pulse injection locking technique.
- Achieving fractional frequency resolution with low complexity circuits and reduced power overhead.
- Implementing an FLL based PVT calibration technique to make the ILCM robust to PVT variations.
- Implementing design techniques to reduce ILCM sensitivity to on-chip noise coupling.

1.3 Research contributions

An ILCM based on a pseudo differential Digitally Controlled Ring Oscillator (DCRO) structure has been implemented. It operates in both integer mode and fractional mode. From that, original contributions have been made as follows:

- First, this is the first implementation of a fully synthesizable ILCM using a differential DCRO that achieves phase noise performance comparable to fully customized

ILCMs. Being fully synthesizable, the design is more generic compared to other existing designs [33][34] and eliminates the need for special isolation and layout techniques to obtain the desired RO performance. Hence, the proposed design achieves comparable results while maintaining low area and complexity. To date, previous fully synthesizable designs are single ended and noise coupling problem is not addressed [25][26][35][36]. The proposed design addresses this problem by using a pseudo differential ILCM structure. Another advantage of the designed structure is lower frequency variations due to With In Die (WID) mismatch, which is becoming increasingly important with technology scaling [37][38]. Reducing WID variations in the ILCM results in reduced jitter and spurious level, more efficient PVT calibration and more accurate frequency tuning.

- Second, a novel calibration algorithm using a replica DCRO and high-speed counters is employed to overcome PVT variations in background fashion. The proposed calibration algorithm is capable of providing improved performance over temperature and power supply variations with minimal impact on power consumption. The calibration technique is less complex than other Frequency Tracking Loop (FTL) based calibration techniques [34][39]. Also, it does not cause additional in-band spurs or time mismatch problems as in prior techniques found in [40][41] and [42][43]. Different from previous PVT techniques that use replica oscillator as in [12][25][44], the proposed PVT calibration is able to compensate for the frequency mismatch between main and replica oscillators after initial calibration. Consequently, it can better track PVT variations.

- Third, the fractional mode utilizes low complexity sequential injection technique and achieves a resolution of $f_{ref}/32$ using only a four stages RO. Compared to traditional sequential injection techniques [32][45], the proposed design achieves finer fractional resolution by a factor of 8 compared to [45] and 4 compared to [32]. This indicates that the proposed design has a fine fractional resolution without the need

to increase the number of ring oscillator stages. Increasing the number of oscillator stages results in reduced oscillating frequency and injection locking bandwidth, and increased jitter [45]. Moreover, in the proposed design, the injection method does not rely directly on the accuracy of pulse width of the injection signal, which is PVT dependent, as in [6][18][24], where the outputs of the oscillator are shorted every injection cycle for the pulse duration. However, the injection method used here uses the injection pulse as a window for injection, where the reference signal overrides the oscillator outputs.

1.4 Related publications and awards

To date the outcomes of the thesis are as follows:

a. Nahla T. Abou-El-Kheir, Ralph D. Mason, Mingze Li, and Mustapha C.E. Yagoub," A Sub-harmonic Injection Locking Clock Multiplier with FLL PVT Calibrator," Microelectronics Journal, vol. 98, no. 1, Apr. 2020.

b. Nahla T. Abou-El-Kheir, Ralph D. Mason, Mingze Li, and Mustapha C.E. Yagoub, "A High-Performance Low Complexity All-Digital Fractional Clock Multiplier," IEEE Asian Solid-State Circuits Conference, Macau, Nov. 2019.

c. Nahla T. Abou-El-Kheir, Ralph D. Mason, and Mustapha C.E. Yagoub, "Fully Synthesizable Clock Multiplier Based on an Injection Ring Oscillator," CMC TEXPO competition, Toronto, Canada, Oct. 2018. Winner of the Micro-Nanosystems Design Award TEXPO competition (worth 3,000$) by CMC Microsystems and Huawei. This award recognizes novel use or development of Computer Aided Design (CAD) tools or design methods leading to the improved manufacture and application of sophisticated micro-nanosystem prototypes relevant to Canadian industry.

d. Nahla T. Abou-El-Kheir, Ralph D. Mason, and Mustapha C.E. Yagoub," A -243dB FOM Fully Synthesizable Injection Locked Clock Multiplier," University of Ottawa Faculty of Engineering 10^{th} Poster Competition, Ottawa, Canada, Mar. 2018. Winner of WIE best presenter.

e. Nahla T. Abou-El-Kheir, Ralph D. Mason, Mingze Li, and Mustapha C.E. Yagoub, "A 65 nm Compact High Performance Fully Synthesizable Clock Multiplier Based on an Injection Locked Ring Oscillator," IEEE International Symposium on Circuits and Systems, Florence, Italy, May 2018.

f. Mingze Li, Ralph D. Mason, and Nahla T. Abou-El-Kheir, "A Fully Synthesized Injection Locked Ring Oscillator Based on a Pulse Injection Locking Technique," IEEE Asia-Pacific Microwave Conference, Kuala Lumpur, Malaysia, Nov. 2017.

1.5 Thesis organization

The remainder of this thesis is divided into five chapters. Chapter 2 introduces the oscillation theory and fundamentals. Next, important performance specifications of clock multiplier based ring oscillators are pointed out. Then, the injection locking technique is described and different ILCM trade-offs are discussed. In Chapter 3, ILCM design challenges due to technology scaling are elaborated upon, including accurate tuning, efficient injection, PVT calibration, and noise immunity. Following this, related works that address these concerns are reviewed and different tuning, injection, PVT calibration and noise immunity methods are explored. Then, existing research gaps in literature are examined. In Chapter 4, system level architecture of the proposed ILCM is presented. The details of its building blocks are discussed, and operating principle of individual blocks and oscillator tuning method are depicted in this chapter as well. Then, Integer and fractional injection multiplication factors formulas are deduced. Furthermore, a formula for relative variations in DCRO period is derived and the advantages of the matrix based ILCM structure are highlighted. At the end of this chapter, the proposed design summary is provided and design solutions to exiting research gaps are explained. Chapter 5 shows simulation and measurement results of the proposed ILCM. Then, its performance is reported and compared to state-of-the-art works. Finally, conclusions and recommended future work are drawn in Chapter 6.

2

Background and related concepts

This chapter introduces oscillator background theory, as well as, ring oscillator advantages and disadvantages compared to other oscillator types. Following that, ring oscillator design aspects, possible applications, classifications, tuning methods, oscillation conditions and oscillating frequency are described. Next, clock multipliers based on ring oscillator specifications are explained including: output frequency, output amplitude, tuning range, frequency resolution, power dissipation, signal spurs, multiplication factor, portability, phase noise, and jitter. Then, phase noise and jitter equations are derived for a ring oscillator, as well as their relationship. Finally, injection locking fundamental design metrics and their relationships are presented.

2.1 Theory of oscillators

Oscillators are key components in modern electronic systems. They provide systems with a clock signal that can be used in digital circuits, DSP units, and communications systems. By definition, they are autonomous circuits that generate a periodic waveform whether sinusoidal, pulsed or other signal types. Typically, sinusoidal waveforms are used in analog circuitry, whereas pulsed waveforms are used in digital systems' clocks. Two fundamental characteristics of an oscillation are startup condition of oscillation (Barkhausen criterion) and oscillation frequency [46]. To study these characteristics, a first order model can be developed to analyze the behavior of an oscillator. In this section, we focus on linear analysis while other parameters, such as spectrum spurious levels and Phase Noise (PN) will be discussed later in the chapter.

2.1.1 Barkhausen criterion

The oscillator can be modeled as a positive feedback system as seen in Figure 1. In this model, $H(s)$ is the transfer function of an amplifier, also called open-loop gain, and $G(s)$ is the transfer function of the feedback network. The feedback network samples the signal output (V_o) and feeds it back to its input, hence the output of the feedback (V_f) is added to the input signal (V_i) for oscillation to take place [47]. From Figure 1 we get:

$$V_o = H(s)V_d \tag{1}$$

$$V_f = G(s)V_o \tag{2}$$

and

$$V_d = V_i + V_f \tag{3}$$

Thus from Equations (1) to (3) the closed loop transfer function $F(s)$ is given by:

$$F(s) = \frac{V_o}{V_i} = \frac{H(s)}{1 - G(s)H(s)} \tag{4}$$

Oscillation starts at a certain frequency w_{osc} when $F(s)$ denominator approaches zero. That is, when

$$G(s)H(s) = 1 \tag{5}$$

Replacing $s = jw_{osc}$ for oscillation at w_{osc} frequency, gives

$$G(jw_{osc})H(jw_{osc}) = 1 \tag{6}$$

The above Equation is known as Barkhausen criterion, and it establishes the initial conditions of oscillation. It can be expressed in polar form as:

$$|G(jw_{osc})H(jw_{osc})| = 1 \tag{7}$$

$$\angle G(jw_{osc})H(jw_{osc}) = \pm 2\pi n \qquad \text{where } n = 0, 1, 2, 3, ... \tag{8}$$

The Barkhausen criterion is a necessary condition for stable oscillation. Electronic noise, typically thermal noise, alters the oscillator initially. The feedback network filters the noise at the output at w_{osc} which then is added and amplified in the loop to generate a periodic waveform at w_{osc} fundamental frequency.

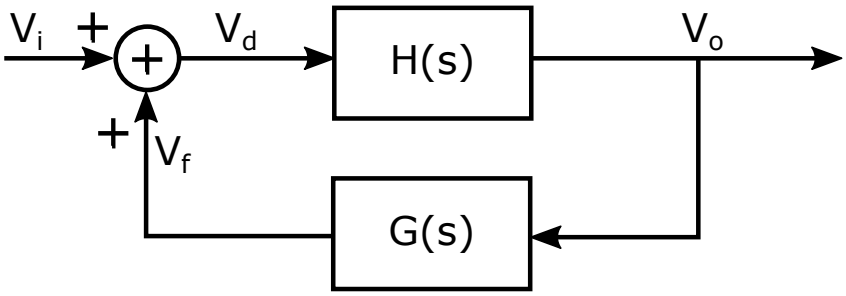


Figure 1: Feedback network

2.1.2 Types of oscillators

Oscillators can be classified into different types based on their structures and characteristics. In modern electronic circuits, three types are used extensively namely, LC, crystal, and ring oscillators.

2.1.2.1 LC-oscillators

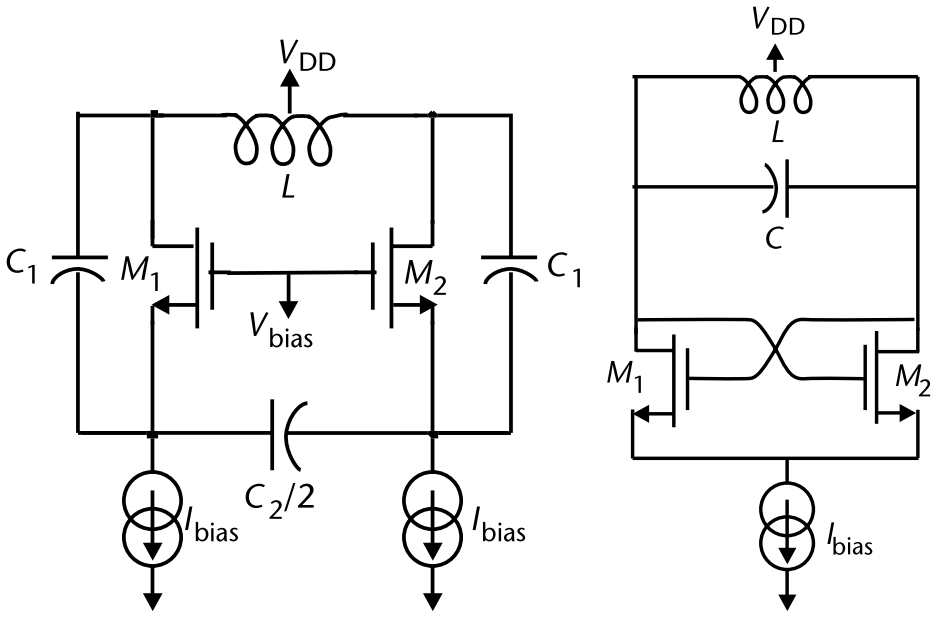
LC-oscillators are widely used in RF applications and they are characterized by their high quality factor (Q) due to the presence of the inductor. They use a resonator composed of an LC-tank to resonate at a fundamental frequency, where the tank parallel resistance approaches infinity. The oscillating frequency can be expressed by:

$$w_{osc} = \sqrt{\frac{1}{LC}} \tag{9}$$

The feedback network of an LC-oscillator results in a negative resistance which helps the oscillator amplitude to grow until the loop gain reaches 1, according to the Barkhausen criterion, then stable oscillation is maintained [48]. A Colpitts oscillator in Figure 2a and a $-G_m$ oscillator in Figure 2b are two common examples of LC-oscillators [48]. In reality, losses exit in the tank's components. On-chip inductors are usually spiral inductors. As they occupy large area, their quality factor will decrease, thereby increasing the tank's losses. The oscillator frequency can be tuned by varying one of the oscillator elements, usually the capacitance (e.g. a voltage controlled capacitance is used such as a varactor).

2.1.2.2 Crystal oscillators

In these oscillators, a piezoelectric crystal, typically a quartz crystal, is used to generate a periodic waveform and resonate at a certain w_{osc} as in an LC-oscillators. When the crystal is subjected to an electric field, mechanical deformation happens and the crystal will resonate at a certain frequency to restore its shape. They are characterized by their high Q, small size, and low power [48]. They are used to provide stable clocks for digital systems and can be used as stable reference clocks in PLLs. However, they are costly and limited in speed; their frequency range can typically only go up to a few hundreds of MHz. Depending on their physical structure, their resonant frequencies and Q factors are determined. Figure 3 shows a single-ended Colpitts-based crystal oscillator using MOS transistors [48].



(a) Colpitts oscillator (b) -Gm oscillator

Figure 2: Examples of LC-oscillators

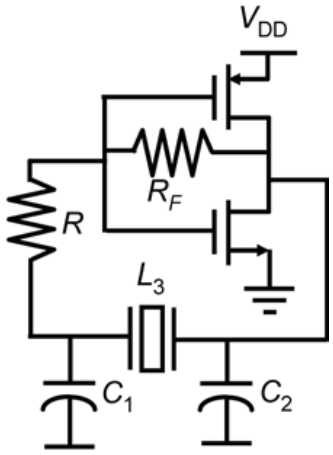


Figure 3: Crystal oscillator

2.1.2.3 Ring oscillator

A RO is composed of a chain of identical elements; these elements can be inverters or delay cells. Ring oscillators do not have a high Q tank as in the case of LC and crystal oscillators. They are widely used in Integrated Circuit (IC) design because of their

increased levels of integration, as they are implemented without capacitors, inductors, or resistors; only transistors are used. According to [49], the RO is one of the most widely manufactured integrated circuits. Foundries use ROs on semiconductor wafers to monitor gate delay and speed-power product of fabricated inverters [50]. Wafers are then selected based on automated measurements of the RO frequency. Figure 4 shows the simplest form of a RO, which is composed of 3 identical inverters. Each stage inverts the input signal throughout the chain, then the output is fed back to the first inverter and the loop continues. The frequency of oscillation depends on the number of elements in the chain and the delay of each one of them as will be derived in the next section. Noise components in a RO disturb each node voltage at X, Y and Z. With time, oscillation starts up and the waveform grows until it reaches rail-to-rail swing [46].

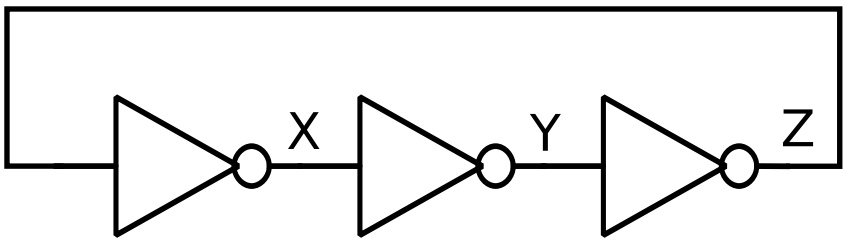


Figure 4: 3-stage ring oscillator

2.2 Ring oscillator classifications

ROs have been used extensively in ICs in the last few decades. More specifically, Clock Multipliers (CMs) based on ROs have drawn a lot of interest lately. This is because they scale well with technology, occupy small die area, offer multiphase outputs and provide a wide tuning range [11][51]. While clock multipliers based on LC-oscillators generally suffer from large area and limited tuning range [52][53], they typically have superior PN and jitter performance compared to RO-based clock multipliers, as they have higher Q factors [54]. For fully integrated IC designs, using off-chip tank elements or crystal is not desirable. In LC-oscillators operating at low frequencies (100MHz to 1GHz), the inductor value typically requires large amount of die area. Hence, integrated

inductors are practical in the GHz frequency range and above with typical Q factors of order 10 or lower due to resistive and substrate losses [55]. Furthermore, even at high frequencies their die area depends on the available metal layers in a given process. Therefore, for fully integrated compact oscillators in 100 MHz to 10 GHz range, RO-based clock multipliers are preferred. RO-based clock multipliers can be used to generate, synchronize, or recover clock signals in Very Large Scale Integrated (VLSI) systems, oversampling Analog to Digital (A/D) converters, Central Processing Units (CPU), and wired/wireless transceivers [17][53][56][57].

As illustrated in Figure 4, the RO, in its simplest form, is built of cascaded stages of inverters placed in a feedback loop, where the number of stages (N_{osc}) is at least 3. According to the Barkhausen criterion, to achieve a total of 2π phase shift, the total phase shift of each of the cascaded inverters is π/N_{osc} as can be illustrated in Figure 5. A linear model is developed for the RO as shown in Figure 6, where R and C are, respectively, the output equivalent resistance and capacitance of an inverter stage assuming identical inverters and G_m the transconductance of the transistor. Hence, the one stage voltage gain transfer function can be written as [46]:

$$A(s) = \frac{-G_m R}{1 + sCR} = \frac{A}{1 + sCR} \tag{10}$$

where $-G_m R$ is the voltage gain per stage (A). Therefore the open-loop gain of a three stage RO is given by:

$$H(s) = \left(\frac{A}{1 + sCR}\right)^3 \tag{11}$$

Hence, the system has three poles located at w_p, given by:

$$w_p = \frac{1}{RC} \tag{12}$$

To achieve 180^o phase shift in a three stage RO, each stage should have a phase shift of 60^o at the oscillation frequency w_{osc}, hence:

$$\angle A(s) = \arctan(\frac{w_{osc}}{w_p}) = 60^o \tag{13}$$

Therefore, the oscillation frequency can be written as:

$$w_{osc} = \sqrt{3} w_p \tag{14}$$

More generally, the oscillation frequency for any given number of stages can be expressed as:

$$w_{osc} = \frac{tan(\theta)}{RC} \tag{15}$$

where θ is the phase shift per stage. To meet the loop gain criterion, Equation (11) can be rewritten as:

$$|H(w_{osc})| = \frac{A^3}{\left(\sqrt{1 + \left(\frac{w_{osc}}{w_p}\right)^2}\right)^3} = 1 \tag{16}$$

By substituting Equation (14) to Equation (16), we can see that each stage should have $A = 2$ for steady state oscillation. If $A < 2$, the circuit will fail to oscillate, and if $A > 2$, theoretically the oscillation amplitude will grow to infinity, although practically the amplitude is limited due to circuit non-linearities and saturation of stages [46]. An alternative method to express the oscillating frequency is by the time delay in each inverter (τ_d). The frequency of oscillation can be also be written as:

$$f_{osc} = \frac{1}{2 N_{osc} \tau_d} \tag{17}$$

Ring oscillators are classified by signal type and tuning methods as discussed in the following subsections.

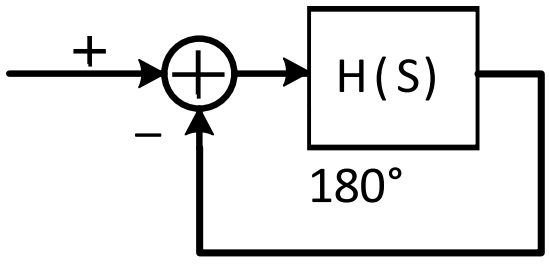


Figure 5: Unity feedback system

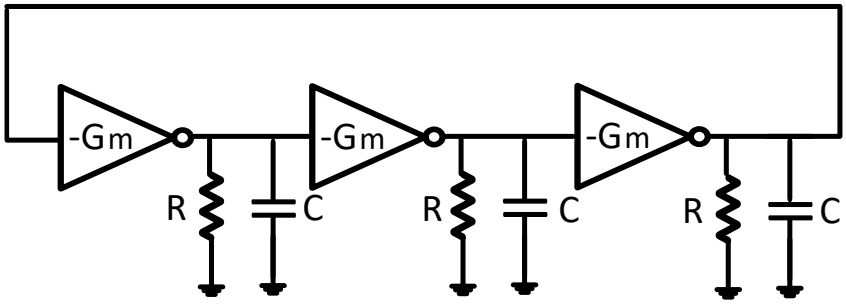


Figure 6: Ring oscillator linear model

2.2.1 Signal Type

Like any other type of oscillators, a RO output signal type affects its performance. RO structures can be categorized into three main categories based on signal type: single ended, true differential, and pseudo differential; each of these structures will be further discussed in the following subsections.

2.2.1.1 Single-ended

The single-ended RO structure can be seen in Figure 7, and the transfer characteristics of a single inverter are shown in Figure 8, where V_m is the ideal switching point of the inverter. An odd number of inverters is used for oscillation to occur as illustrated in Section 2.1.1. Inverter number and transistor sizes can be chosen based on the desired oscillation frequency, as transistor sizes will affect the stage delay. Different inverter structures can be utilized depending on the application [58][59]. A single-ended RO has more than one advantage. First, it consumes less power, as ideally it only draws current when there is a signal transition (*i.e.* no short circuit path) and also it is built of fewer circuit components. Whereas, in a true differential structure, current is drawn from the supply whether there is a signal transition or not, and in a pseudo differential structure circuit, components are doubled compared to single-ended structure. Second, it has rail-to-rail swing, which helps to reduce jitter [55]. Disadvantages of this topology include its susceptibility to variations from the supply and substrate voltages (because

of variations in the inverters' switching points), which negatively affects jitter, and the fact that the number of inverters is limited to an odd number, which is undesirable in some applications, like those that require quadrature outputs [60][61].

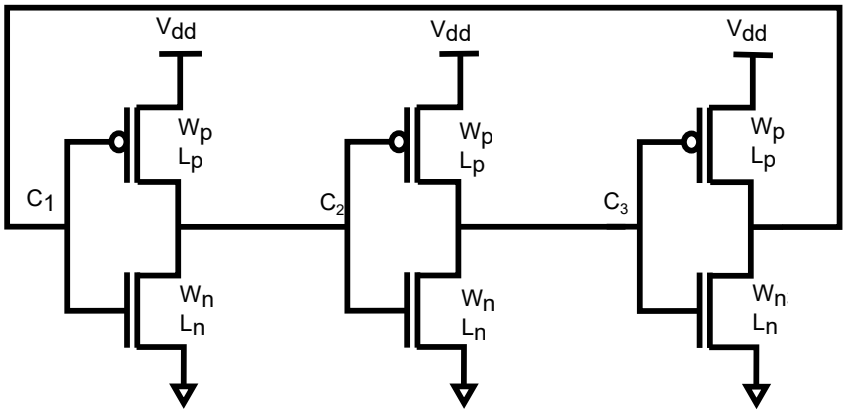


Figure 7: Single-ended RO

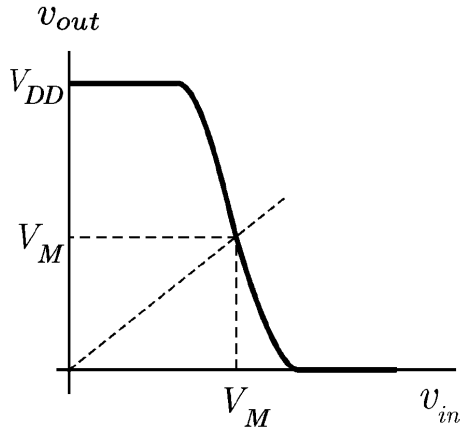


Figure 8: Transfer characteristics of an inverter

2.2.1.2 True differential

A true differential cell consists of a differential pair with a resistive load and a tail current source as can be seen in Figure 9. The input and output signals are differential, so the +ve output signal of one stage is connected to the –ve input of the next stage and vice versa, and then at the last stage the wires are switched as can be seen in Figure 10 [48]. As a result, quadrature outputs can be obtained with even/odd numbers of stages.

Another advantage is that it provides good common mode rejection, hence it is better at rejecting supply and substrate variations. However, this topology suffers from reduced voltage headroom to keep the transistors in saturation region, therefore the voltage swing is not rail-to-rail, thus increasing the sensitivity to jitter [55].

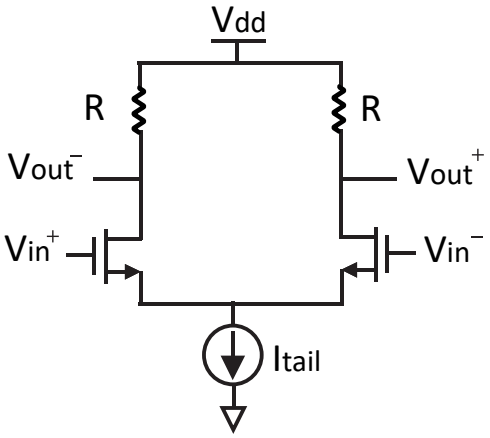
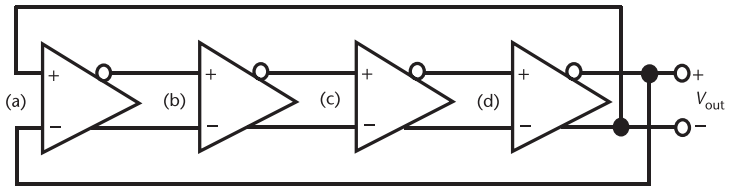


Figure 9: True differential circuit



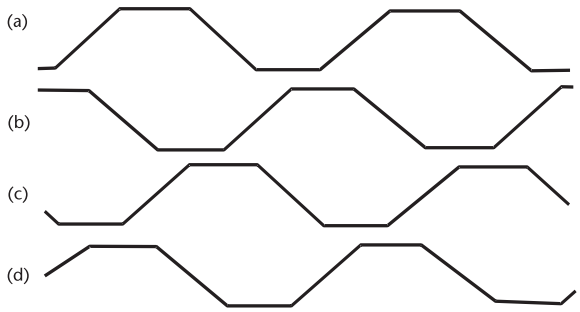


Figure 10: Quadrature waveforms

2.2.1.3 Pseudo differential

In a pseudo differential structure, two inverters and a pair of cross coupled inverters can be used as seen in Figure 11. The cross coupled inverters are sized smaller than the main two inverters. The cross coupled inverters accelerate the output transiting hence reduce sensitivity to jitter [34]. This topology, similar to the true differential topology, can be implemented using even or odd numbers of delay cells and it can produce quadrature outputs if an even number of stages is used. In addition, signals have rail-to-rail swing, which decreases jitter.

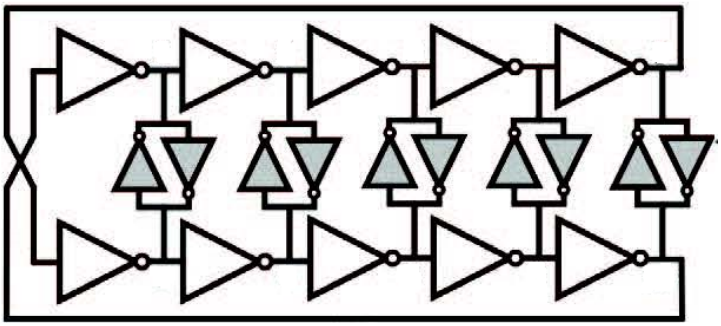


Figure 11: Pseudo differential structure

2.2.2 Frequency tuning

In many applications, oscillators are required to be tunable *i.e.* their output frequency varies with a control input. For example, if the oscillator is used as a local oscillator, the oscillation frequency must be tunable over the receiver or transmitter range. The oscillation frequency can be varied continuously using a Voltage Controlled Oscillator (VCO) or discretely using a Digitally Controlled Oscillator (DCO). In the following subsections, differences between them will be examined. Different tuning structures will be covered in the next chapter.

2.2.2.1 Voltage Controlled Oscillator

In this tuning technique, the oscillating frequency is tuned using an input voltage signal V_{cont}. The output frequency is a nonlinear function of the input voltage. However, within a limited range of operation, the VCO's output frequency can be approximated as a linear transfer function of its voltage control signal, as can be seen in Figure 12 and expressed as [46]:

$$w_{osc} = w_o + K_{VCO}\, V_{cont} \tag{18}$$

where w_o represents the intercept corresponding to $V_{cont} = 0$, K_{VCO} is the VCO gain, also called tuning sensitivity, and V_{cont} is the control voltage. Furthermore, from Figure 12, the achievable tuning range can be defined as $w_2 - w_1$. The VCO gain can be written as:

$$K_{VCO} = \frac{\partial w_{osc}}{\partial V_{cont}} \tag{19}$$

VCOs can provide a fine resolution, as they are controlled by an analog signal. They are mainly used in PLLs to map a control voltage coming from a frequency phase detector and lowpass filter to an output frequency, thereby tracking changes in the control voltage. In cases where the VCO control line that adjusts oscillator frequency (for example by tuning the oscillator's varactor) is implemented as single ended, it is then susceptible to common mode noise. This noise is upconverted to the VCO output, hence deteriorates the VCO's PN performance [46][48]. This issue becomes more critical with the use of low supply voltages in advanced CMOS processes. This issue has been addressed in [62] and [63], by tuning the VCO differentially at the expense of area and power consumption.

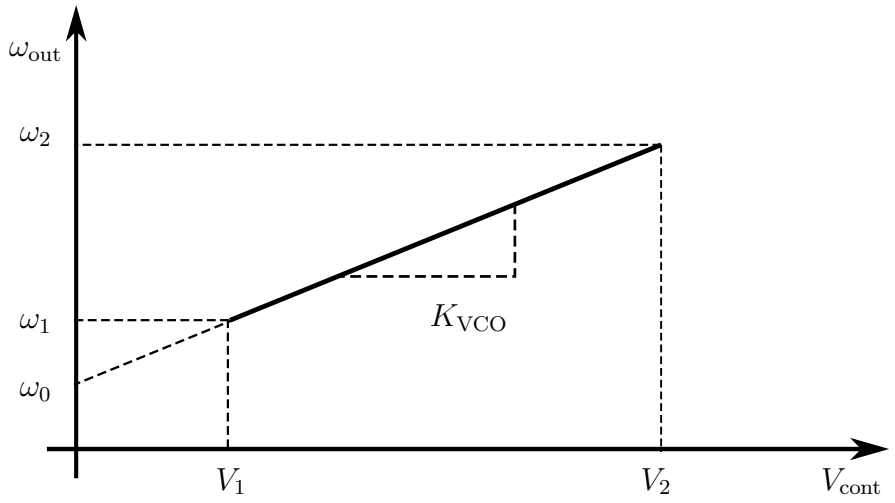


Figure 12: VCO transfer function

2.2.2.2 Digitally Controlled Oscillator

Unlike VCOs, the oscillating frequency in a DCO is tuned using a digital Oscillator Tuning Word (OTW), also called a Frequency Code Word (FCW). Similar to VCOs, the output frequency is a nonlinear function of OTW and linear only within a certain range of frequencies, tuning range, as can be seen in Figure 13, can be expressed as [12]:

$$w_{osc} = w_o + K_{DCO}\, OTW \tag{20}$$

where K_{DCO} is the DCO gain and it is defined as:

$$K_{DCO} = \frac{\Delta\, w_{osc}}{\Delta\, OTW} \tag{21}$$

DCOs are considered the core of All-Digital Phase Locked Loops (ADPLLs). It determines ADPLL jitter, phase noise, tuning range, power consumption, and area [12]. They perform digital-to-frequency conversion by controlling the output frequency by one of various code forms such as thermometer, binary, and one-hot codes to provide a variety of different frequency resolutions [64][65]. In some applications, where fine frequency resolution and wide tuning rang are required, the RO employs a combination of both a DCO and a VCO. In these cases, the DCO is used to provide wide operating range and

flexibility of control, and the VCO is used to obtain small step size [33].

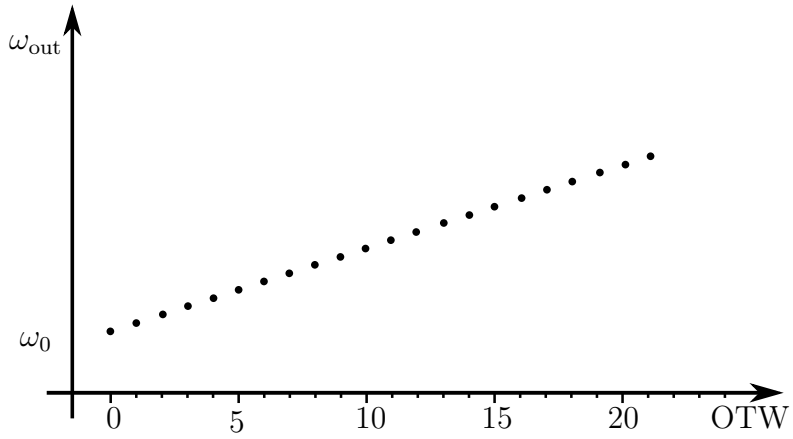


Figure 13: DCO transfer function

2.3 Clock multiplier specifications

In many electronic systems, a CM provides a low jitter clock signal whose spectral purity highly impacts the overall system's performance. Given a reference frequency clock, a CM generates an output signal that is an integer or a fractional multiple of a low-frequency reference. The following specifications are key parameters to evaluate a CM performance:

- **Output frequency:** It is determined by application requirements. A typical RO-based CM operating frequency is up to 10 GHz [34]. The operating frequency is a trade-off with the frequency step-size and power dissipation. A higher output frequency can help reducing jitter in a RO-based CM. In addition, a programmable output frequency is important for some applications.

- **Output amplitude:** To make the output waveform less sensitive to noise, it is desirable to have high output amplitude with fast switching times. Furthermore, high output amplitude helps to achieve low jitter performance [46][55].

- **Tuning range:** The required tuning range in a design is dictated by three param-

eters: (1) the variation of the oscillator center frequency with PVT, (2) the frequency range necessary for the application, and (3) the overlap between frequency bands or tuning methods as will be elaborated in the next chapter. The center frequency of some CMOS oscillators may vary considerably with PVT conditions, thus mandating a sufficiently wide tuning range to guarantee that the oscillator output frequency can be adjusted to the desired value [12][24]. Also, a wide tuning range is essential for applications that incorporate clock frequencies required to vary by one to two orders of magnitude. For example, a frequency synthesizer needs to cover all frequencies necessary to demodulate/modulate all frequency channels. Moreover, when switching between two tuning banks, typically each bank should allow an overlap range to keep monotonic frequency change even at the bank's boundaries [33].

- **Power dissipation:** Reduced power consumption is preferable in CMs, especially in battery-operated portable devices, to extend battery life and reduce costs. Generally, ROs suffer from a trade-off between power dissipation and noise.

- **Output signal spurs:** A CM output spectrum is desired to be free of spurious tones, which are frequency components other than the desired frequency. Spurs appear at the oscillator output spectrum due to periodic timing error coming from systematic timing fluctuations in the output period [12]. Spurs are usually measured with respect to the fundamental frequency in dBc by subtracting the spur power in dBm from the fundamental tone power in dBm.

- **Multiplication factor:** It is the ratio between the output frequency and input reference frequency. The multiplication factor (K) affects the output frequency value, PN, spur level and NBW, as will be discussed in details in Section 2.4.

- **Frequency resolution:** It is determined by the application and also called frequency step-size. For instance, in a frequency synthesizer, the frequency step-size must be no more than the channel spacing. A fine frequency resolution might come

at the expense of power consumption as multiple frequency tuning stages are used to achieve the required resolution [33][44], as will be discussed in the next chapter. Also in some designs, delta-sigma dithering is utilized to further enhance the step size, which increases the power consumption. This is because the dithering frequency is typically higher than the reference frequency [12]. As the frequency resolution becomes finer, the reference spurs level decreases and also the multiplication factor can be increased.

- **Portability:** It is the ability to transfer a design from one technology node to the next. In the past few decades, portability has become increasingly important, as portable designs help shorten product time-to-market. Designs described in a Hardware Description Language (HDL) are typically easier to port than a full custom analog design.

- **Phase noise:** An ideal RO will have most of its power concentrated at the fundamental frequency w_{osc}. However, in practice, internal noise in the oscillator causes its spectrum to spread into nearby frequencies around w_{osc}, forming skirts (phase noise) as shown in Figure 14. These skits result from phase error in time domain, and they are undesirable. For example, if the RO is used as a local oscillator, these skirts will cause interference between channels. Single sided phase noise is usually calculated with respect to the carrier power (signal power at the fundamental frequency w_{osc}) in a 1-Hz unit bandwidth at a Δw frequency offset from w_{osc} in dBc/Hz as [12] :

$$\mathcal{L}(\Delta w)|_{dBc/Hz} = 10 \times log_{10} \frac{P_{noise} \text{ in a 1-Hz BW at frequency } w_{osc} + \Delta w}{\text{carrier power}} \quad (22)$$

where, P_{noise} is the noise power. The phase noise spectrum as a function of Δw of a non-ideal oscillator can be illustrated in Figure 15 in log scale. Region 1 is due to flicker noise of electronic devices when it gets up-converted to $1/w^3$ region. Region 2, due to thermal noise, is shaped by the oscillator's transfer function and gets up-converted to $1/w^2$ region. Region 3 is due to thermal noise outside the RO

filtering bandwidth [66].

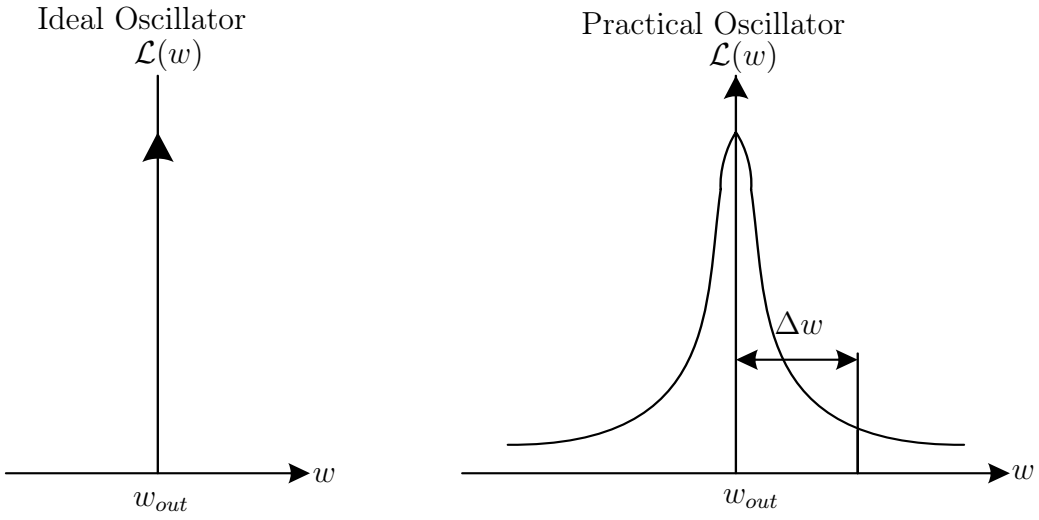


Figure 14: Oscillator spectrum

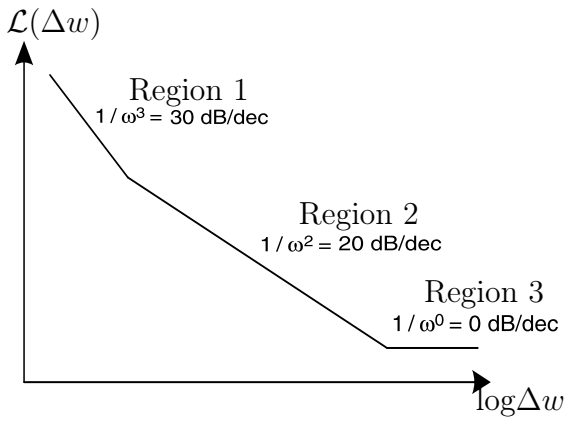


Figure 15: Phase noise of an oscillator

- **Jitter:** It is defined as instantaneous variations in the phase of a signal that causes its deviation from its ideal position as can be seen in Figure 16. Typically, a signal position can be defined by its zero-crossing. Jitter can result from intrinsic sources as device's thermal and flicker noise or extrinsic sources such as supply and substrate noise or noise coming from the reference clock in case of PLLs/ILCMs [67][68]. Jitter (σ_τ) can be expressed in different ways. Absolute jitter, period jitter, and cycle-to-cycle jitter are common ways to measure an oscillator jitter.

Absolute jitter is deviation of each positive or negative transition from it ideal value. Period jitter is defined as the deviation of each cycle period from its nominal value. Cycle-to-cycle jitter can be calculated by measuring the difference between two consecutive cycles of the waveform [46]. Jitter variance (σ_τ^2) is a function of the PN, hence the Single Side Band (SSB) phase noise due to thermal noise can be expressed as [49]:

$$\mathcal{L}(\Delta w) = \sigma_\tau^2 \frac{w_{osc}^3}{2 \times \pi \times \Delta w^2} \tag{23}$$

where σ_τ is the RMS period jitter.

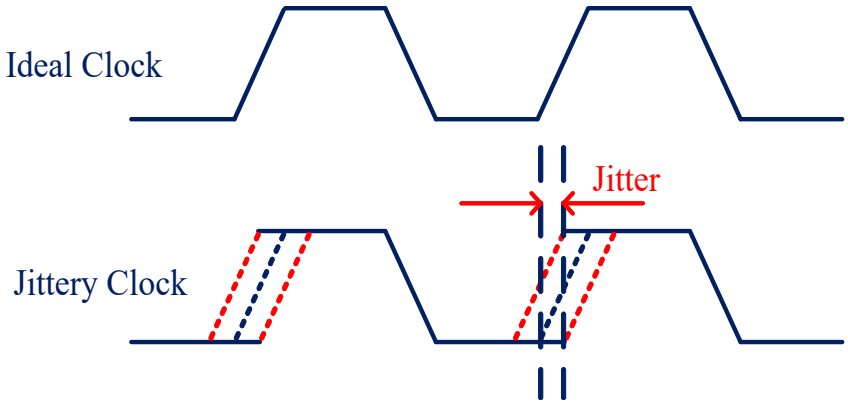


Figure 16: Jitter in RO

2.3.1 Phase noise and jitter analysis of a ring oscillator

Phase noise and jitter due to thermal and flicker noise will be analyzed in this subsection, considering a RO composed of N_{osc} inverter stages as can be seen in Figure 17.

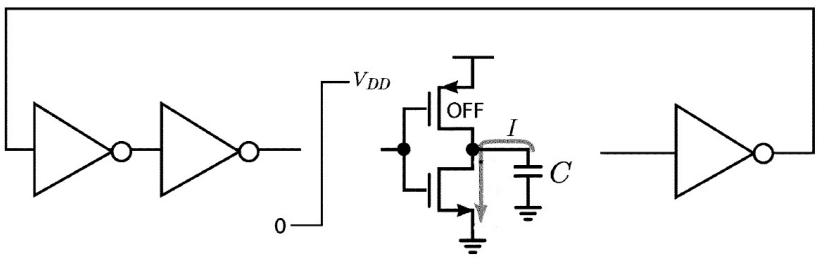


Figure 17: Inverter stage while switching

- **Ring oscillator phase noise due to thermal noise**

  In an inverter circuit, transistor current noise and channel resistance noise are the two main contributors of thermal noise. Given that these two sources, are uncorrelated the total uncertainty in propagation delay of an inverter stage (assuming equal pull-up and pull-down currents $I_N = I_P = I$) can be written as [49]:

$$\sigma^2_{\tau_{dN}} = \frac{4kT\gamma_N\tau_{dN}}{I(V_{DD} - V_{tN})} + \frac{kTC}{I^2} \tag{24}$$

  where k is the Boltzman constant, T the temperature, γ_N the fraction of the gate length, τ_{dN} the NMOS propagation delay, τ_{dP} the PMOS propagation delay, I_N the NMOS drain current, I_P the PMOS drain current, V_{DD} the supply voltage, V_{tN} NMOS threshold voltage , and C the load capacitance. The frequency of oscillation of a RO can be written as:

$$\begin{aligned} f_{osc} &= \frac{1}{N_{osc}(\tau_{dN} + \tau_{dP})} \\ &\simeq \frac{2}{N_{osc}CV_{DD}}\left(\frac{1}{I_N} + \frac{1}{I_P}\right)^{-1} \\ &\simeq \frac{I/C}{N_{osc}V_{DD}} \end{aligned} \tag{25}$$

  Every propagation delay is jittered by noise in the pull-up or pull-down processes. Given that these noise events are uncorrelated, the variance of period jitter is:

$$\sigma^2_\tau = N_{osc}(\sigma^2_{\tau_{dN}} + \sigma^2_{\tau_{dP}}) \tag{26}$$

  where $\sigma^2_{\tau_{dN}}$ and $\sigma^2_{\tau_{dP}}$ are variance in NMOS and PMOS propagation delays respectively. Using Equations (24) and (25) and assuming equal NMOS and PMOS threshold voltages ($V_{tN} = V_{tP} = V_t$) for simplicity, the variance in period jitter can be rewritten as:

$$\sigma^2_\tau = \frac{kT}{If_{osc}}\left(\frac{2(\gamma_N + \gamma_P)}{V_{DD} - V_t} + \frac{2}{V_{DD}}\right) \tag{27}$$

  where γ_P is the fraction of the PMOS gate length. From Equation (23), SSB PN due to thermal noise can be expressed as:

$$\mathcal{L}(\Delta w) = \frac{2kT}{I}\left(\frac{(\gamma_N + \gamma_P)}{V_{DD} - V_t} + \frac{1}{V_{DD}}\right)\left(\frac{w_{osc}}{\Delta w}\right)^2 \tag{28}$$

  Thus, phase noise-power trade-off can be noticed in the above Equation.

- **Ring oscillator phase noise due to flicker noise**

  Pull-up and pull-down currents contain flicker $(1/f)$ noise that varies slowly over many output transitions and the noise arising from every transistor is uncorrelated [49]. From Equation (25), the sensitivity of f_{osc} to I_N of an NMOS transistor can be written as:

$$\frac{\partial f_{osc}}{\partial I_N} = \frac{2}{N_{osc} C V_{DD}} \left(\frac{1}{I_N} + \frac{1}{I_p} \right)^{-2} \frac{1}{I_N^2} = \frac{f_{osc}}{2 N_{osc} I} \tag{29}$$

  Therefore, the SSB PN per stage due to flicker noise in pull down current of current spectral density $(S_{iN}^{1/f}(f))$ is [49]:

$$\mathcal{L}(\Delta w) = \frac{1}{4\Delta w^2} \left(\frac{w_{osc}}{2 N_{osc} I} \right)^2 S_{iN}^{1/f}(f) \tag{30}$$

  Hence, SSB PN in a N_{osc} stage RO is:

$$\begin{aligned} \mathcal{L}(\Delta w) &= \frac{1}{4\Delta w^2} \left(\frac{w_{osc}}{2 N_{osc} I} \right)^2 \times N_{osc} \left(S_{iN}^{1/f}(f) + S_{iP}^{1/f}(f) \right) \\ &= \frac{1}{16 N_{osc} I^2} \left(S_{iN}^{1/f}(f) + S_{iP}^{1/f}(f) \right) \left(\frac{w_{osc}}{\Delta w} \right)^2 \end{aligned} \tag{31}$$

  where $S_{iP}^{1/f}(f)$ is the current spectral density due to flicker noise in the pull up current. The relation between flicker noise current spectral density of an NMOS $S_{iN}^{1/f}(f)$ and flicker noise Power Spectral Density (PSD) of an NMOS $S_{vN}^{1/f}(f)$ is:

$$S_{iN}^{1/f}(f) = g_m^2 S_{vN}^{1/f}(f) \tag{32}$$

  Given that $S_{v_n}^{1/f}$ is equal to [49]:

$$S_{v_n}^{1/f} \simeq \frac{K_{fN}}{W L C_{ox} f} \tag{33}$$

  where g_m is transistor transconductance, K_{fN} is NMOS empirical coefficient dependent on circuit bias and technology and C_{ox} is the oxide capacitance. Therefore, the total SSB PN induced by NMOS and PMOS flicker noise using Equation (31) is [49]:

$$\mathcal{L}(\Delta w) = \frac{2\pi}{4 N_{osc} (V_{DD} - V_t)^2} \left(\frac{K_{fN}}{W_N L_N} + \frac{K_{fP}}{W_P L_P} \right) \times \frac{w_{osc}^2}{\Delta w^3} \tag{34}$$

where K_{fP} is PMOS empirical coefficient, W_N and W_P are the channel widths of NMOS and PNMOS respectively, and L_N and L_P are NMOS and PMOS channel lengths. From Equation (34), we can see that the bigger transistor's size the smaller flicker noise it will contribute. Furthermore, it can be noted that the PN can be suppressed at the expense of power, similar to thermal noise case. Equations (28) and (34) describe PN and Δw relationship as found in Figure 15.

2.4 Injection locking

The phenomenon of injection locking was first recorded by Christian Huygens in the 17^{th} century. He was observing the pendulums of two clocks on the wall, where they were hung close to each other, when he noticed that the two pendulums moved in unison, and over time, they eventually moved at the same frequency with a 180^o phase shift. He predicted that the vibrations coupled through the wall drove the clocks into synchronization [69]. Early studies on injection locking in oscillators can be found in [5][70]. Ever since injection locking has been used in various applications such as frequency division [71][72], quadrature signal generation [73][74], and clock multiplication in oscillators and PLLs [75][76]. Furthermore, Injection locked ROs' multiphase outputs property make them a popular choice for state-of-the-art multistandard I/O interfaces in high speed serial links, where they are combined with a phase interpolator to provide the transmitter and receiver with quadrature clock and data signals [9][19][77][78].

The focus in this thesis is on the sub-harmonic injection locked clock multipliers. Sub-harmonic injection locking technique has been utilized in oscillators to achieve low PN frequency multiplication by locking the oscillator frequency to one of the reference harmonics. Jitter accumulates in a RO due to its poor Q factor as can be seen in Figure 18. Consequently, this phenomenon deteriorates the RO PN performance. To address this issue, sub-harmonic injection locking techniques have been adopted to help suppress the free-running RO phase noise [24][34]. In these techniques, the free-running RO is locked onto the K^{th} harmonic of a low-noise reference signal. This is accomplished by injecting

the reference signal edge into the RO every K output cycles as shown in Figure 19. When the reference signal is injected, it inserts an additional phase shift into the RO feedback loop, hence the RO no longer oscillates at the free-runnig frequency, since the total phase shift at this frequency deviates from 2π as discussed in Section 2.1.1. The RO overcomes this additional phase shift by oscillating at the injection frequency and then it is said to be injection locked, given that the amplitude and frequency of the injection signal are selected according to design considerations discussed later in this section [69]. The multiplication factor is determined by choosing the reference harmonic order that the RO will lock onto. This factor can be either an integer [25][31][79] or a fraction [32][40][45][80] depending on the application. ILCMs have four main characteristics, which are injection locking bandwidth, realignment factor, PN, and reference spurs. These characteristics are detailed below.

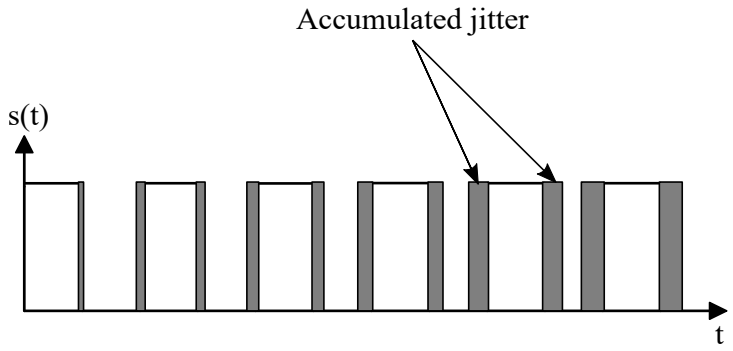


Figure 18: Jitter accumulation in RO

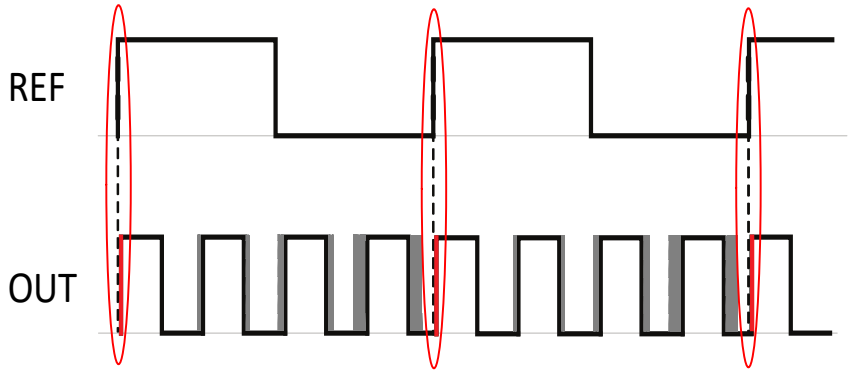


Figure 19: Injection locking

2.4.1 Injection locking bandwidth

The oscillator injection locking range can be defined as the frequency range over which injection locking holds and outside of which the free-running oscillator PN dominates. In Figure 20, the PN of the free-running oscillator ($\mathcal{L}(\Delta f)_{free}$) and injection locked oscillator ($\mathcal{L}(\Delta f)_{injection}$) can be seen. From Figure 20, we can see that injection locking technique suppresses the free-running PN within a certain locking bandwidth after which the oscillator's PN follows the free-running PN profile. The locking BW is determined by oscillator circuit parameters, Q factor, and the reference signal power. If a reference signal is injected into a RO and the difference between the free-running frequency and the reference frequency (or one of its harmonics frequencies) is within the locking BW, the oscillator is said to be injection locked. The reference signal can be a sine or pulsed signal. A typical ILCM has a locking bandwidth of $f_{ref}/6$ [3], where f_{ref} is the reference frequency.

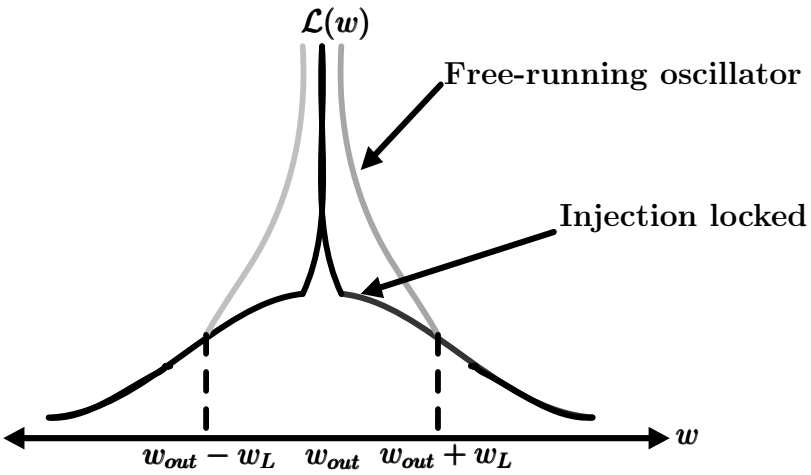


Figure 20: Injection locking range

Locking BW analysis for ROs can be found in [76] and [81]. For simplicity, we assume a sine reference signal with injection current of amplitude I_{ref} and θ phase difference with respect to the oscillator current I_{osc} as can be seen in Figure 21. In this analysis, we

consider the case where injection occurs at a single stage. I_{osc} can be written as [76]:

$$I_{osc} = \frac{I_C}{sin(\frac{\pi}{N_{osc}})} \tag{35}$$

where I_C is the current flowing onto the capacitor. The overall lock range around w_{osc} is $w_L^{\pm}$, where w_L is the one-sided lock range, w_L^+ is equal to $w_{max} - w_{osc}$ and w_L^- is equal to $w_{osc} - w_{min}$. From the analysis in [76], we get the maximum and minimum w_{ref} values ($w_{max/min}$) for the case of $I_{ref} \leqslant I_{osc}$ as:

$$w_{max/min} = \frac{1}{RC} \times \tan\left(\frac{\pi \pm \sin^{-1}(r)}{N_{osc}}\right) \tag{36}$$

where r is the ratio between I_{ref} and I_{osc}. Since the value of resistance R may not be apparent in some topologies, the fractional lock range is used, It is given by:

$$\frac{w_L^{\pm}}{w_{osc}} = \frac{\tan\left(\frac{\pi \pm \sin^{-1}(r)}{N_{osc}}\right) - \tan\left(\frac{\pi}{N_{osc}}\right)}{\tan\left(\frac{\pi}{N_{osc}}\right)} \tag{37}$$

Thus, for small injection, where $I_{ref} \ll I_{osc}$, small angle approximation gives:

$$\frac{w_L^{\pm}}{w_{osc}} \approx \pm \frac{2}{N_{osc} \times \sin(\frac{2\pi}{N_{osc}})} \times \frac{I_{ref}}{I_{osc}} \tag{38}$$

From Equations (37) and (38), we can notice that as the injection current increases *i.e.* injection signal power increases, the locking BW increases. Furthermore, we can observe that the locking BW will decrease as the number of stages increases. It is worth mentioning that multi-phase injection techniques have been proposed in [82][83] to further enhance the RO locking BW by a factor of N_{osc} [76]. In addition, techniques to extend the noise suppression BW by dual injection have been suggested in [84][85] and by frequency doubler in [3][86]. These techniques trade noise suppression BW with signal purity as $2 \times f_{ref}$ spurs are introduced to the output signal spectrum.

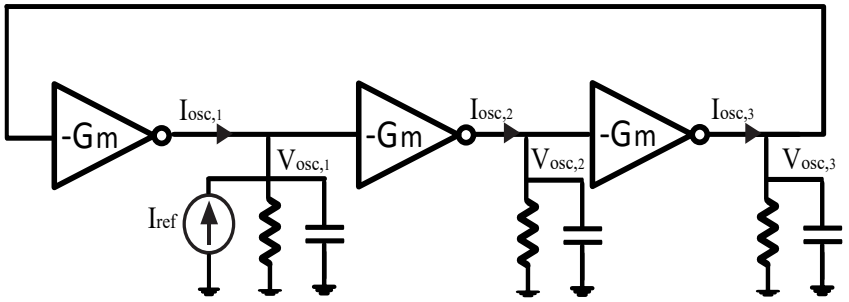


Figure 21: Injection locking RO model

2.4.2 Realignment factor

Injecting a reference signal into the RO output at every reference period helps to realign the RO output to its correct edge position as illustrated in Figure 19. If the oscillator and reference were both noiseless, the RO output edge would line up with the reference edge at every reference period. Practically, the jitter in the RO output and reference signal causes their edges to occur at different times. Hence, when injection takes place, the RO output edge is pulled towards the reference edge; this realignment effect perturbs the RO. These perturbations affect both the amplitude and phase of the RO. Although the amplitude fluctuations fade within several RO cycles, phase fluctuations do not disappear [87]. As can be seen in Figure 22, the RO output is dragged towards the reference edge and a phase shift ($\theta_{out}[n]$) in the RO output happens due to the instantaneous input phase error between the free-running RO edge and the reference signal edge ($\theta_e[n]$). The output phase shift can be approximated as a linear function of the phase error and can be expressed as $-\kappa\theta_e[n]$, where κ is called the realignment factor, which describes the strength of the injection process and it ranges from 0 to 1. Cycle-to-cycle variations in $\theta_e[n]$ are mainly caused by the free-running RO PN. $\theta_e[n]$ can be expressed as [87]:

$$\theta_e[n] = \theta_{inst-RO}[nT_{ref}^{-}] - K\theta_{ref}[nT_{ref}] \tag{39}$$

where $\theta_{inst-RO}[nT_{ref}^{-}]$ is the free-running phase just after the n^{th} reference edge and $\theta_{ref}[nT_{ref}]$ is the reference phase of the K^{th} harmonic. Hence, the phase error at the RO output under injection can be written as a function of the RO free-running phase error

$(\theta_{RO}(z))$ and the reference phase error $(\theta_{ref}(z))$ as [41][87]:

$$\theta_{INJ-RO}(z) = \theta_{RO}(z)H_{rl}(z) + \theta_{ref}(z))H_{up}(z) \tag{40}$$

where

$$H_{rl}(z) = 1 - \frac{\kappa z^{-1}}{1-(1-\kappa)z^{-1}} \tag{41}$$

and

$$H_{up}(z) = \frac{K \times \kappa}{1-(1-\kappa)z^{-1}} \tag{42}$$

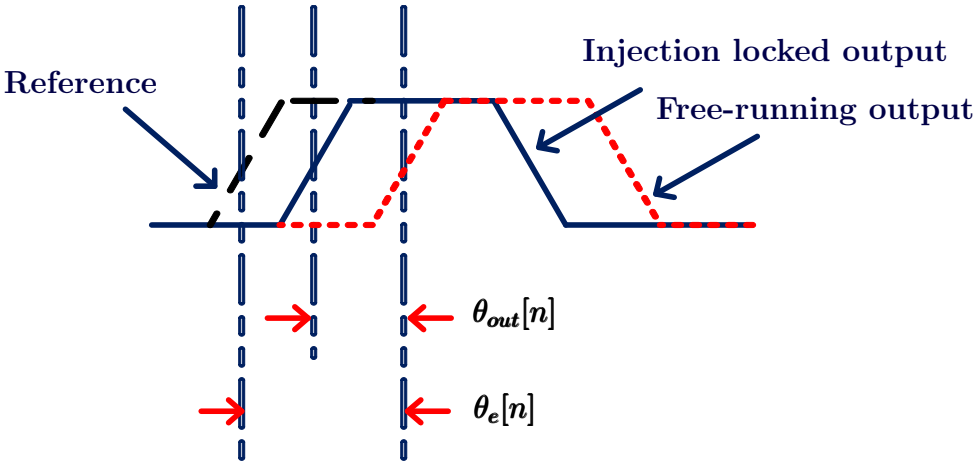


Figure 22: Phase realignment

The transfer functions $H_{rl}(z)$ and $H_{up}(z)$ represent the effect of phase realignment and the up conversion of the reference noise to the RO output, respectively. The free-running phase error $\theta_{RO}(z)$ is high pass filtered and the reference phase error is low pass filtered $\theta_{ref}(z)$ at the injection locked output. It can be noted from the above equations that the higher the κ factor is, the lower the injection locked RO phase noise will be. Furthermore, the up conversion reference transfer function is directly proportional to the multiplication factor K.

2.4.3 Injection locking phase noise and spurs

As discussed in Section 2.3.1, noise in a RO causes phase fluctuations, which results in errors in the zero crossing times (*i.e.* jitter). As the zero-crossing error at each stage adds

to the previous zero-crossing errors, these fluctuations build up over time causing jitter to accumulate as shown in Figure 18. In the frequency domain, this effect is equivalent to multiplying the jitter PSD by a transfer function proportional to $1/f^2$ resulting in RO output PN. As shown in Figure 19, injection locking pulls the RO edge to its correct position, hence refreshes the RO output and suppresses the memory of past errors. In the frequency domain, noise suppression attenuates the $1/f^2$ transfer function, thereby reduces the RO PN as can be seen in Figure 23.

Different analyses of injection locked oscillator PN in the frequency domain can be found in [88][89][90]. The small-signal PN analysis in [89] was one of the first papers to consider the effect of the realignment factor on the injection locked oscillator PN. From the analysis in [89] and assuming that the free-running PN profile is dominated by thermal noise, we can conclude that the SSB injection locked PN is:

$$\mathcal{L}(\Delta f)_{injection} \approx \pi^2 \times \Delta f^2 \times \frac{K^2}{f_{osc}^2} \times \left[\left(\frac{2}{\kappa} - 1\right)^2 + \frac{1}{3}\right] \times \mathcal{L}(\Delta f)_{free} \tag{43}$$

where $\mathcal{L}(\Delta f)_{free}$ is the free-running PN of an oscillator. The above equation only describes the oscillator output PN under injection locking due to phase realignment at frequency offsets lower than the locking bandwidth (f_L) and assumes that the reference noise will not dominate the output PN. Furthermore, it is based on the assumption that $f_{osc} = K \times f_{ref}$, which is not necessarily true with PVT variations. According to [88], the input reference signal PN ($\mathcal{L}(\Delta f)_{REF}$) increases by $20log(K)$ at the output as:

$$\mathcal{L}(\Delta f)_{REF_{out}} \approx K^2 \times \mathcal{L}(\Delta f)_{REF} \tag{44}$$

By adding Equations (43) and (44), we get the total SSB output PN, assuming that the reference and oscillator intrinsic noise are uncorrelated:

$$\mathcal{L}(\Delta f)_{total} = \mathcal{L}(\Delta f)_{injection} + \mathcal{L}(\Delta f)_{REF_{out}} \tag{45}$$

It is worth mentioning that the quality of the reference clock should be chosen carefully in ILCMs. The input reference PN must be at least $20log(K)$ below the injection locked PN, so that it does not dominate the total PN at the output [88]. The total output PN

and the free-running PN are plotted in Figure 23. We can note that within the locking BW, the free-running PN is reduced, while outside the locking BW, the injection locked PN is 3 dB higher than the free-running PN as demonstrated for high offset frequencies (higher than f_L) in [89][88][90].

Due to PVT variations, the free-running frequency (f_{osc}) deviates from f_{out}, where f_{out} is equal to Kf_{ref}. In this case, the oscillator runs for $(K-1)$ cycles at f_{osc} and at each K^{th} injection cycle, the realignment effect causes the oscillator to change its period, so that the average frequency is equal to Kf_{ref}. In other words, phase error accumulated for $(K-1)$ cycles is compensated by injection by $2\pi Kf_{ERR}/f_{osc}$ phase shift, where f_{ERR} is equal to $Kf_{ref} - f_{osc}$ [41]. The relative frequency error (α) is given by f_{ERR}/Kf_{ref}. Due to this pulling effect at the RO output every reference period, a reference spur appears at the RO output spectrum at f_{ref} offset from the oscillating frequency, as well as deterministic jitter, which is proportional to α. The reference spur can be expressed in dBc as [24]:

$$Spur = 20 \times log_{10}(K\alpha) \tag{46}$$

From the above equation, we can see that as K increases, the reference spur, as well as deterministic jitter, increase. This rise in deterministic jitter can also be seen in frequency domain, as the injection locked PN increases due to the reduced filtering BW, as shown in Figure 24 [8]. Reference spurs levels in ILCMs typically range from -40 to -65 dBc [31]. It is worth mentioning that higher κ factors cause higher spur levels [6][44].

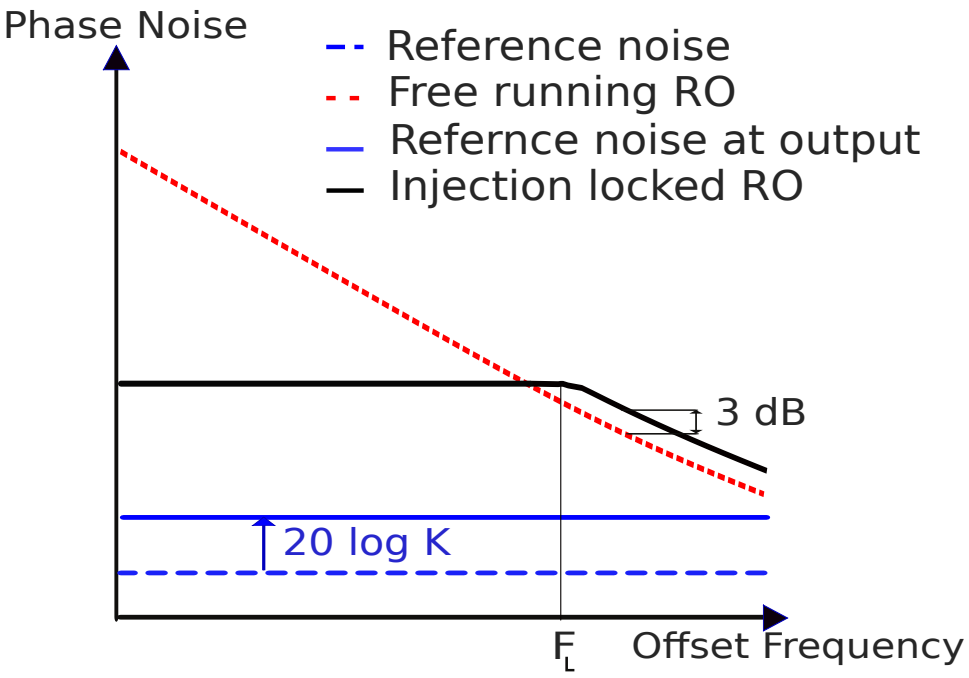


Figure 23: Injection locking phase noise

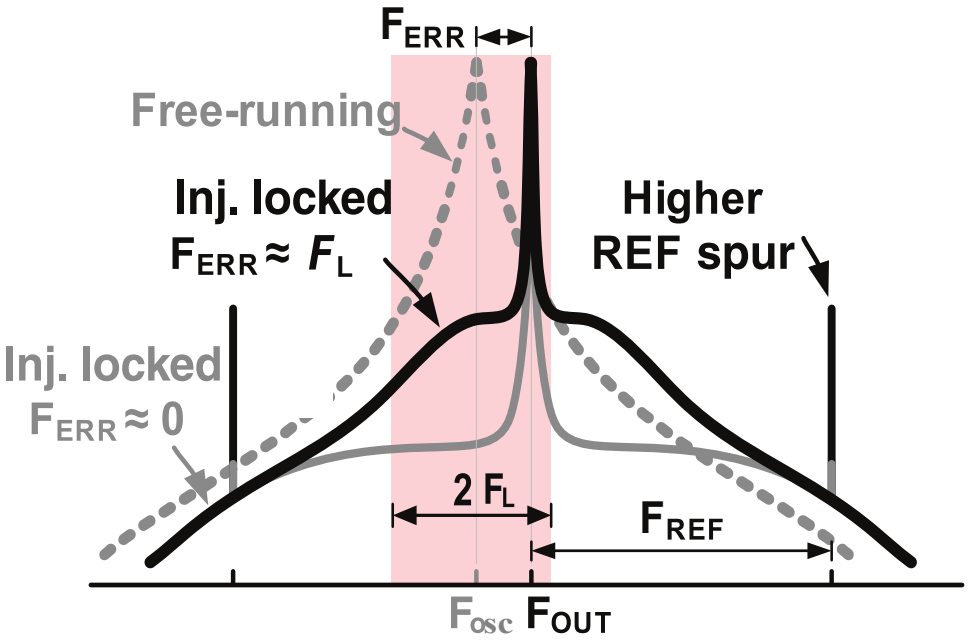


Figure 24: Injection locking PN in the presence of frequency error

2.5 Conclusion

Concepts related to the proposed ILCM design were presented in this chapter. First, background information about oscillator design criteria was covered. Second, RO theory and classifications were briefly explained. Clock multiplier design considerations, metrics, and trade-offs were summarized. Finally, injection locking was presented and its key parameters were reviewed. In the next chapter, ILCMs design challenges in deep sub-micron CMOS technologies will be elaborated and state-of-the-art studies will be discussed.

3

Clock multipliers challenges

ILCMs based on DCRO is an active research area. However, designing low-jitter ILCMs in deep submicron CMOS processes comes with several challenges. In this chapter, these challenges will be discussed. Frequency tuning, efficient injection methodology, PVT calibration, and noise immunity are critical design considerations to achieve high performance. Some design techniques have been investigated in recent studies to meet these requirements, so state-of-the-art ILCMs will be reviewed in this chapter and research gaps will be pointed out.

3.1 DCRO frequency tuning

Accurate frequency tuning is essential when designing a DCRO-based ILCM. The DCRO free-running frequency needs to be tuned to be within the locking BW of a reference harmonic for successful sub-harmonic injection locking. As the order of the reference har-

monic increases, *i.e.* higher output frequency is required, the injection signal becomes weaker, and the locking BW will be narrower as discussed in Section 2.4.1. Therefore, the frequency step size should be fine enough so that the ILCM does not lose lock at high K factors. In addition, the frequency resolution will affect the ILCM reference spur and jitter. If the frequency resolution is coarse, the frequency error (f_{ERR}) between the reference and the free-running frequency will increase, leading to high reference spur and deterministic jitter as pointed out in Section 2.4.3. Other important aspects of DCRO tuning are: linearity, which demands careful matching between elements, operating frequency, which is determined by application, and tuning range, which may require coarse and fine stages. Different DCRO structures were designed to achieve accurate frequency tuning as will be detailed in the coming subsections.

3.1.1 Current digital to analog converter

This technique has been used intensively in ILCM design due to its low power consumption, wide tuning range, and high operating frequency compared to other techniques [3][8][24][25][41]. In this technique a Current Digital to Analog Converter (IDAC) is utilized to change the RO's drain/source current, hence changing the oscillation frequency as highlighted in the previous chapter in Equation (25). An IDAC, in its simplest form, is composed of parallel current sources that can be turned on or off using a FCW as shown in Figure 25 [24]. It can be used for coarse and fine tuning as in Figure 26 [3]. The fine tuning is thermometer coded and implemented using unit-weighted current sources, and the coarse tuning is binary coded and implemented using binary weighted current sources to achieve wide tuning range. The DAC resolution must be chosen carefully as it affects the power consumption, area, and spurious level. This technique has two prospective drawbacks: (1) poor supply noise rejection and (2) dependency of the DCRO voltage on the tuning code, which requires a level shifter and duty cycle corrector, which adds additional analog components and complexity to the design.

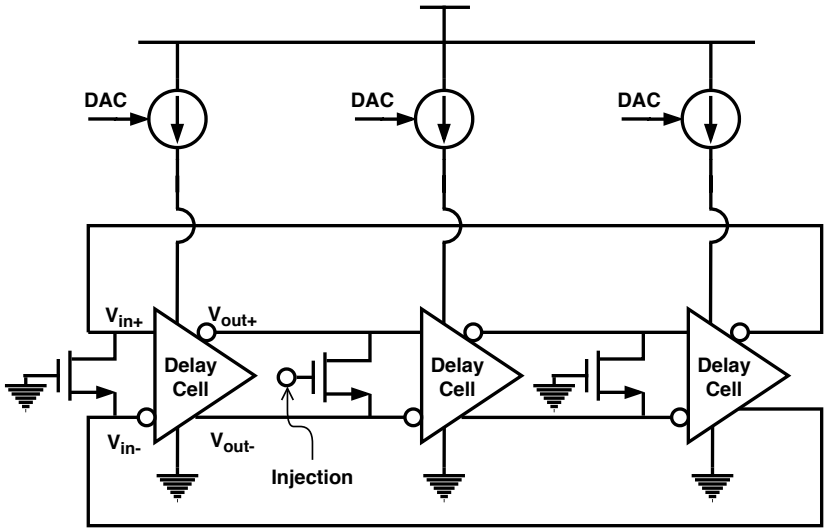


Figure 25: IDAC based ILCM

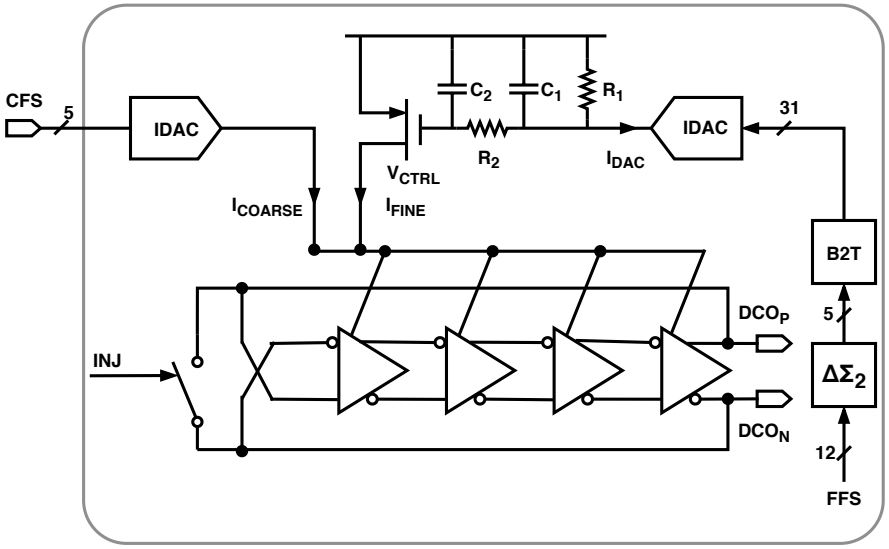


Figure 26: Coarse and fine IDAC

3.1.2 Digitally controlled resistors

In this technique [16][79], an array of resistors, composed of logic gates and transistors, are digitally controlled to change the DCRO supply voltage based on the tuning code, hence controlling the DCRO frequency. It can be used for fine or coarse tuning as shown

in Figure 27 [16]. It has the advantage of wide tuning range at the expense of high power consumption. Similar to the previous technique, it suffers from reduced supply noise rejection and needs a level shift and duty cycle corrector.

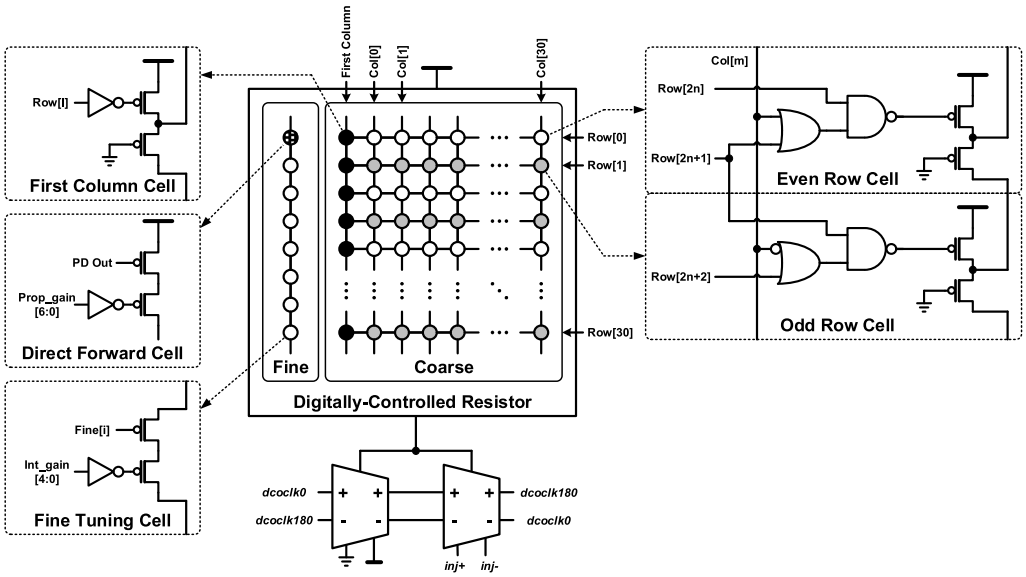


Figure 27: Digitally controlled resistors array

3.1.3 Programmable inverter array

In this technique [36][91][92][93], inverters in an array are turned on or off to increase or decrease the current of an inverter, therefore increasing or decreasing the oscillation frequency. In [36][91], each unit weighted inverter in the array can be enabled or disabled as shown in Figure 28, while in [92][93] binary weighted rows of inverters are selected one at a time for coarse tuning as shown in Figure 29. The step-size of this technique can be further enhanced by using half and quarter unity cells as found in [91] to achieve sub-gate delay resolution. This technique has a wide tuning range and it can be fully synthesizable, as it is built from standard cell inverters, although it suffers from reduced supply noise rejection, as well as a trade-off between the oscillating frequency and step-size.

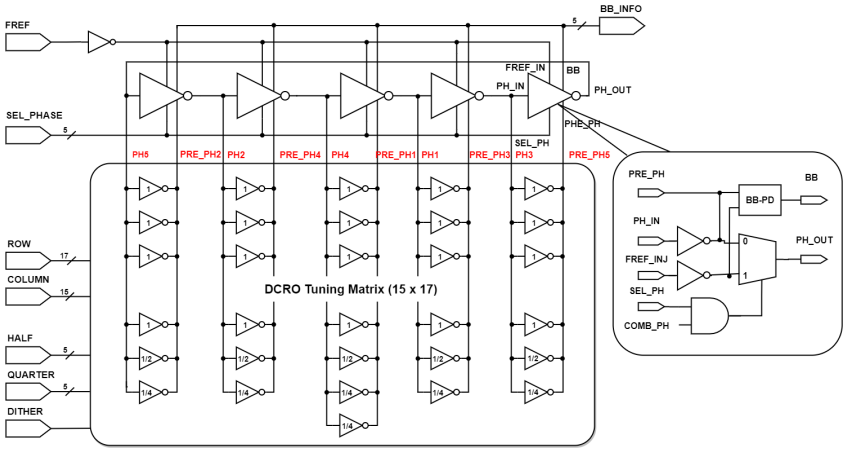


Figure 28: Programmable inverter array

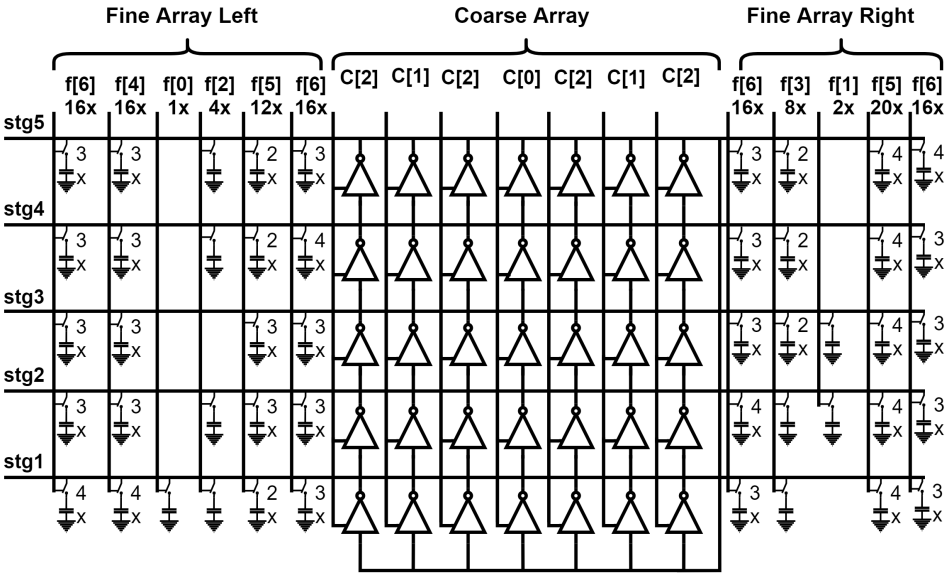


Figure 29: Programmable binary weighted inverter array

3.1.4 Switched capacitor

Switched capacitor tuning has been widely used for coarse and fine tuning in ILCMs. Examples of switched capacitor-based tuning are investigated in [12][25][29][33][44][64][65][92][93]. Metal Oxide Semiconductor (MOS) or Metal Insulator Metal (MIM) capacitors are used as building blocks to digitally tune the RO load capacitance as illustrated in Figure 30. As shown in Equation (25), the oscillation frequency decreases as the RO load capac-

itor increases. This technique is characterized by its fine step-size and wide tuning range at the expense of reduced operating frequency. Additionally, MOS capacitors suffer from poor supply noise rejection. In [12], the author uses the capacitance difference (ΔC) between depletion and inversion region of an Inversion-mode Metal Oxide Semiconductor (IMOS) to control the capacitor value by the gate voltage, where the depletion region resembles the on-state capacitor and the inversion region resembles the off-state capacitor. In [25][44], the authors use the miller capacitor difference in a NAND gate by changing one of its inputs from 0 to 1. In [64], authors use one-hot code to achieve a very fine step size of 5 kHz by using different sized transistors to achieve small ΔC. In [65][29], authors use complementary varactor pair which changes the load capacitance by the capacitance difference between differently sized MOS capacitors. This method reduces supply noise sensitivity of MOS capacitors. In [92][94], authors use the drain junction capacitance and a transmission gate switch to enable/disable the capacitor. It is worth mentioning that in an N-well process, PMOS capacitors are preferable due to the well isolation that makes it less sensitive to switching noise from the surrounding circuits, as well as, PMOS transistors reduce flicker noise compared to NMOS transistors.

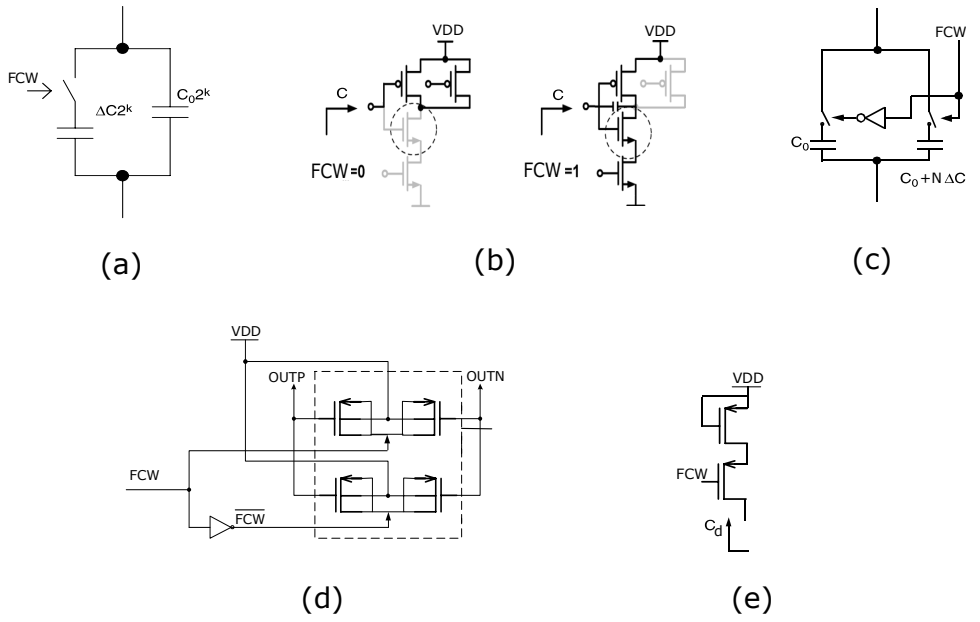


Figure 30: Switched capacitors configurations (a) IMOS switched capacitor (b) Miller switch capacitor (c) One-hot coded switched capacitor (d) Complementary varactor pair (e) Drain junction capacitance

3.1.5 Varactors

This technique has been used in [33][34]. Similar to the previous technique, the frequency is dependent of the load capacitance value, where typically Accumulation-mode Metal Oxide Semiconductor (AMOS) or IMOS varactors are utilized as load capacitors. In this technique, the capacitance value is controlled digitally, although the signal is converted to an analog signal by the aid of a DAC as shown in Figure 31 [33]. Thus, the linear region in the capacitance-voltage transfer function is used, which causes its tuning range to be limited as the linear region is shrinking with technology scaling [12]. This technique is characterized by its fine step-size, low power, and high operating frequency. However, due its analog tuning nature, it is susceptible to power supply noise.

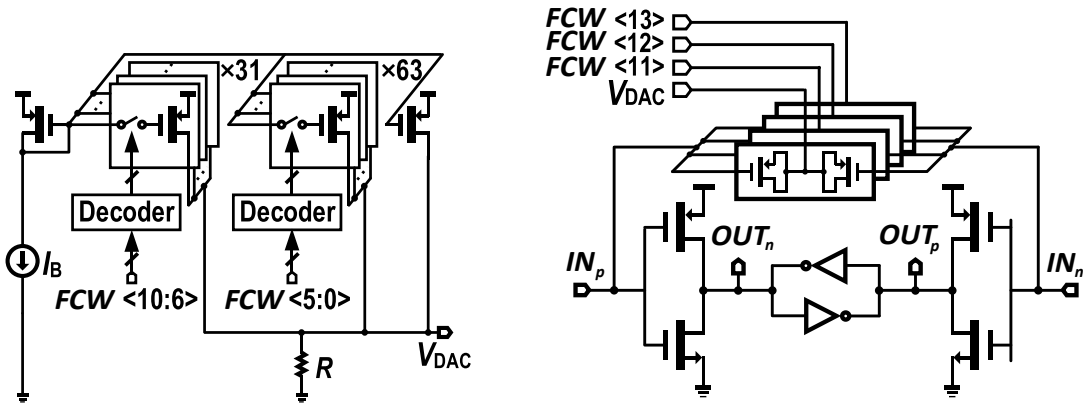


Figure 31: Varactor based tuning

At the end of this section, it is worth mentioning that different combinations of the above techniques have been used to achieve fine resolution and wide tuning range. Nevertheless, this requires band-switching algorithm to ensure linear step-size in the presence of PVT, which adds complexity to the design [33].

3.2 Injection methods

In an ILCM, the injection method affects the output reference spur and PN, as it determines the realignment factor (κ) as discussed in Section 2.4.2. Similar to ILCMs, Multiplying Delay Locked Loops (MDLLs) are commonly used to reduce jitter in RO [33][86][93]. In this method, the noisy clock edge is replaced by a clean reference edge periodically with the aid of a MUX. Unlike ILCMs, they have selection logic that controls the RO edge replacement. MDLLs use a divider and other extra digital logic for selection, which limits their frequency and consume relatively high power [1][18][95]. MDLLs are often compared to ILCMs techniques because of their similar nature. Injection techniques are divided into integer or fractional, where K is an integer in the former and a fraction in the latter. More details about integer and fractional techniques are provided in the following sub-sections.

3.2.1 Integer injection locking

Various methods have been used to implement integer injection locking in RO:

- RO outputs shorting is one common method to implement integer injection locking as described in [8][24][34][41]. In this method, a pass transistor shorts the RO output of a certain stage every injection period using a narrow input signal as shown in Figure 25. Although it is composed of a simple injection circuit with low power consumption, it needs PVT calibration to guarantee pulse width accuracy. As the use of extensively narrow pulse width causes oscillator locking to fail and the wide pulse width causes deterministic jiiter [25].

- The pulse injection window method was first introduced in [45]. In this method, the reference is injected to the RO outputs to override their value and realign them as shown in Figure 32. This method has better PVT immunity but consumes higher power consumption compared to the previous method.

- MUX based injection window was proposed in [91], where one of the RO outputs is replaced by the reference signal every injection cycle using a MUX as shown in Figure 29. It has improved PVT performance as it is independent of the pulse width; however, it suffers from high reference spurs, as well as high power consumption.

- Switched capacitors injection was investigated in [75] as shown in Figure 33. It has the advantage of PVT immunity and insensitivity to the pulse width. Nevertheless, mismatches in injection switches can cause increased spur levels.

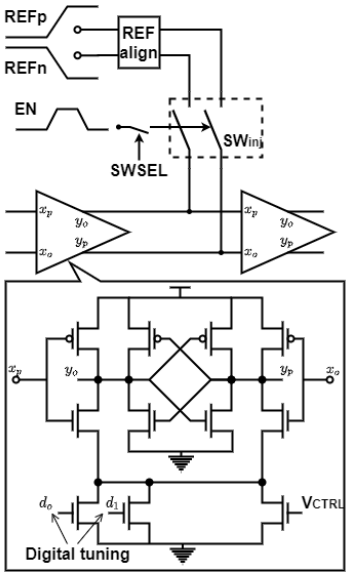


Figure 32: Pulse window injection

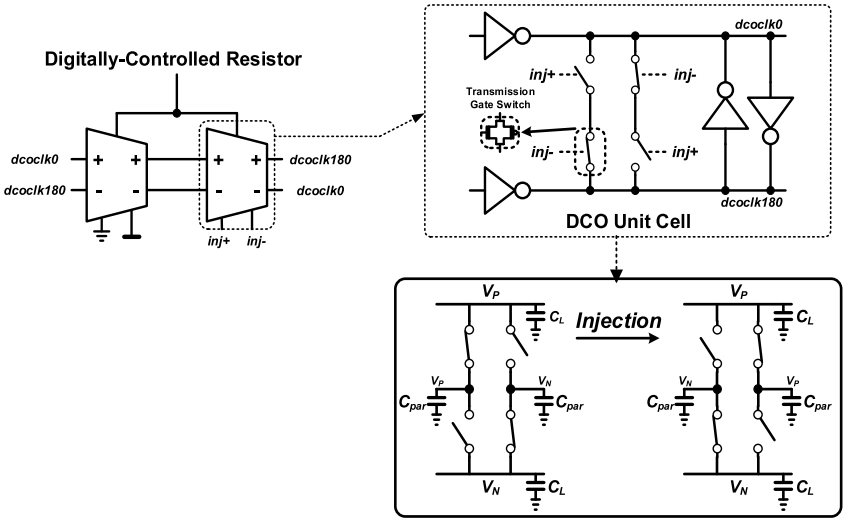


Figure 33: Switched capacitor injection

3.2.2 Fractional injection locking

To date, several methods have been used to realize fractional multiplication as resolution/phase noise trade-off found in integer clock multipliers limits their applications. The sequential injection method, which makes use of the multiphase output of the RO [32][45], is generally less complex; however, the frequency resolution is limited compared

to other approaches. In the Digital-to-Time Converter (DTC) based methods, the reference signal is shifted in time to be aligned with the oscillator output transition. It can provide improved frequency resolution but at the expense of higher complexity [40] [96]. A soft injection method, in which the injection amplitude controls the RO phase adjustment [44], can also provide improved resolution and low spur levels using two PLLs stages to overcome degraded injection efficiency.

3.3 PVT variations

With technology scaling, DCRO frequency deviation due to PVT variations has become more significant. Changes in temperature and voltage happen over time and can be caused by device heating, low Power Supply Rejection Ratio (PSRR) and external factors [97]. Conversely, global changes in process are more static by nature, and they happen as result of parameter fluctuation during fabrication, especially in deep submicron CMOS processes. Process variations can happen between Wafer to Wafer (W2W), Die to Die (D2D) and Within Die (WID); in all cases their effect increases with technology scaling [37][98].

PVT variations negativity affect the ILCM reference spur and jitter as pointed out in Section 2.4.3. Therefore, PVT calibration is crucial to maintain a locked state with the intended performance. In Figure 34, the locking bandwidth relation with DCRO output frequency and jitter is illustrated. The FCW controls the free-running frequency f_{osc}, as the FCW increases f_{osc} increases. When the DCRO is injected locked, the DCRO output frequency (f_{out}) is locked to the reference harmonic frequency Nf_{ref}, when f_{osc} is within the locking bandwidth. When f_{osc} is exactly equal to Nf_{ref}, the lowest jitter is achieved. While, as f_{osc} drifts with PVT variations, f_{osc} is no more equal to Nf_{ref}, hence jitter increases. Significant increased deterministic jitter and high reference spur level are found at the edges of the locking bandwidth due to sever periodic pulling of the RO edges. If the difference between Nf_{ref} and f_{osc} (f_{ERR}) increases beyond the one sided locking bandwidth (f_L), the DCRO loses lock [24][69].

Time diagram in Figure 35 shows $f_{osc} \neq N f_{ref}$ case, when $|f_{ERR}|$ is less than f_L. Within the locking bandwidth, changing the FCW does not affect f_{out}, as f_{out} is the average output frequency of the DCRO over N cycles, where the RO oscillates at f_{osc} for N-1 cycles until the injection signal resets its timing. However, the FCW changes f_{osc} internally, hence it changes the time delay (Δt) within the injection locked DCRO. It is worth mentioning that the locking bandwidth is typically in tens of MHz range and it depends on the multiplication factor, oscillator Q factor, and the number of oscillator stages, as discussed in the previous chapter.

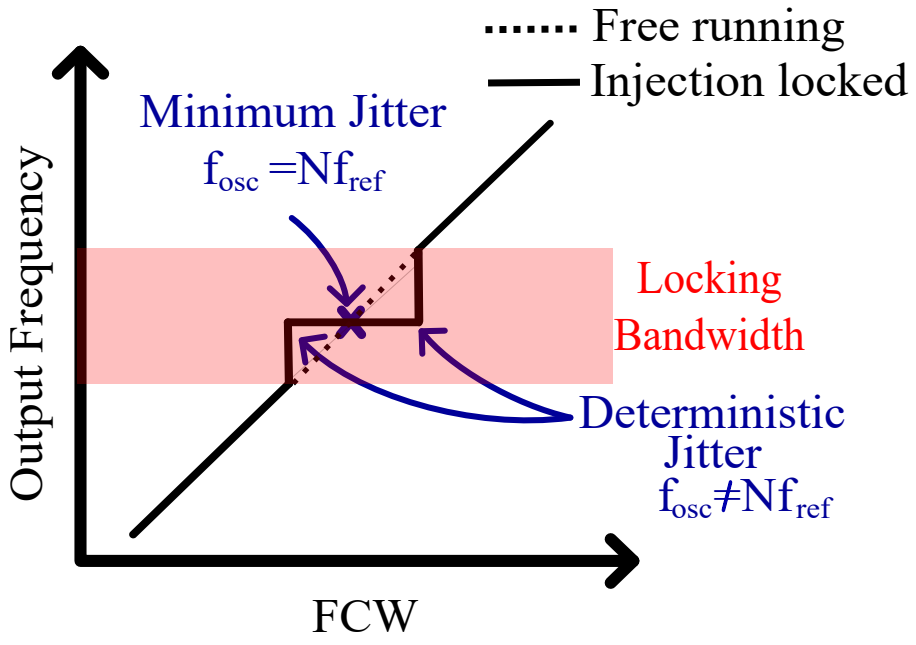


Figure 34: RO frequency under injection locking

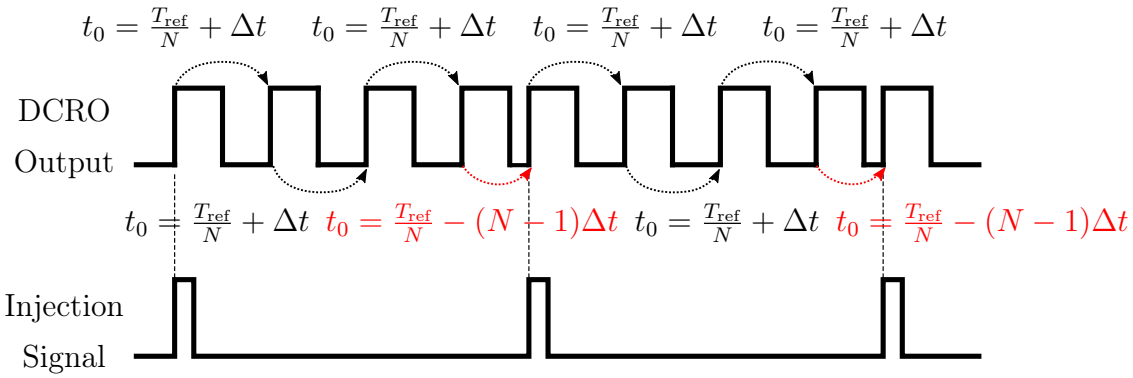


Figure 35: RO output in time domain when $f_{osc} \neq N f_{ref}$

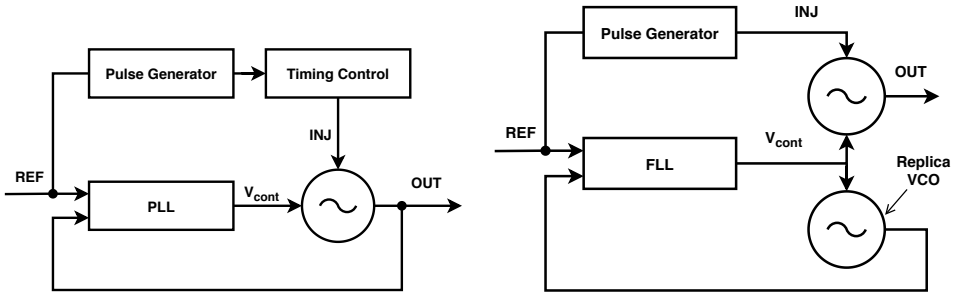
Several PVT calibration techniques have been implemented in literature:

- PVT Calibration using conventional PLLs has been proposed in [42][43][45][87]. The ILCM is put in a PLL to track frequency deviations as shown in Figure 36a. This approach has potential drawbacks including poor free-running frequency tracking under locking conditions and timing mismatch between the injection and PLL paths [2][16][95].

- Alternative calibration methods, which use a FLL with the aid of a replica oscillator, have been introduced in [24][44]. As illustrated in Figure 36b, the replica oscillator detects the free-runnig frequency and corrects the DCRO frequency. In this approach, frequencies of the main and replica oscillators do not change equally with temperature and voltage variations. Furthermore, the replica oscillator increases the design area.

- Injection skipping technique was first proposed in [40][41]. In this technique, injection cycles are skipped to measure the free-running frequency for calibration as shown in Figure 37 [41]. Possible disadvantages of this technique are additional accumulated jitter due to skipped injection cycles and additional in-band spurs at the injection skipping rate.

- Phase control FTL, as shown in Figure 38, was used in [34][39][99]. This technique tracks PVT variations by detecting DCRO phase information, hence it provides better noise suppression at low frequencies [7]. Since it only detects instantaneous phase shift in a DCRO, it has limited acquisition range and needs additional frequency acquisition circuit like PLL or FLL, as well as a lock-loss detector that switches from frequency acquisition mode to phase control mode. Consequently, these circuits add complexity to the design.



(a) Conventional PLL (b) Replica FLL

Figure 36: PVT calibration techniques

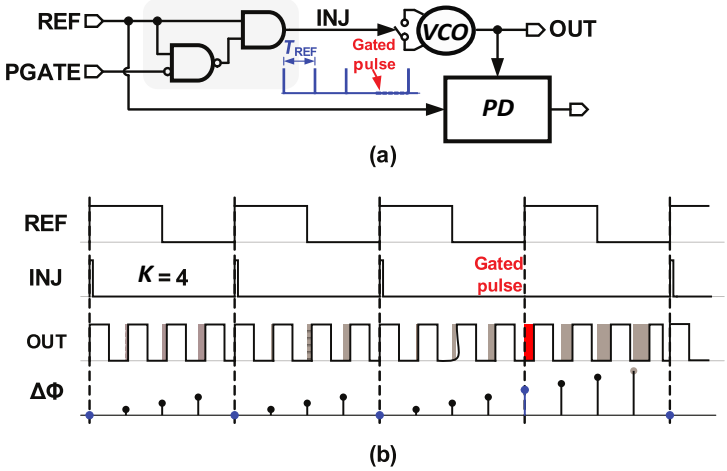


Figure 37: Injection skipping technique (a) Structure (b) Timing diagram

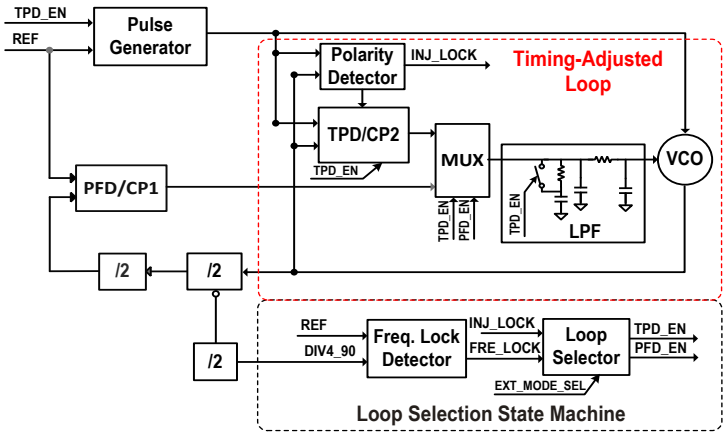


Figure 38: Phase controlled FTL

3.4 Noise coupling

Designing a noise insensitive DCRO has become more and more challenging with technology scaling due to reduced voltage supplies. Low supply voltage reduces the signal dynamic range, thus causing severe degradation in SNR [97]. In addition, with higher levels of integration and design complexity, switching noise couples through the supply voltage and substrate.

Switching noise results from circuits transients thus, causing ripples on the supply voltage by two mechanisms. First, significant voltage drop can occur when long wire traces are used due to parasitic resistance. Not only does this effect cause supply ripples, but also it causes the DCRO voltage supply to be lower by the IR drop than the external power supply. Second, parasitic inductance found in broad traces, package traces and bond wires causes supply/ground bouncing at high frequencies by $L\frac{di}{dt}$.

Substrate noise coupling takes place due to the resistive and capacitive nature of the substrate [97]. Switching noise affects circuits on the same chip that share the same substrate and supply. All these effects result in variations in the RO waveform that will appear as jitter and increased spurious levels [12][97]. It is worth mentioning that switching noise has a significant impact on analog circuit performance, hence analog circuits with high PSRR are preferable. This, on the other hand, increases design complexity.

Different techniques can be utilized to minimize noise coupling effects. First, reducing the use of analog components in a design generally lowers design's susceptibility to noise and/or the need to have special design and layout techniques. Second, differential DCRO structures help reducing noise sensitivity as discussed in Sections 2.2.1.2 and 2.2.1.3. Third, decoupling capacitors are placed between supply and ground to filter out the noise and minimize the supply ripple magnitude. Fourth, voltage regulators can be used to suppress low frequency noise by filtering any current spikes on the power supply. Low Drop Out (LDO) voltage regulators are commonly used in ILCMs and PLLs. They can be implemented using a comparator, pass transistor and capacitor as shown in Figure

39. Different LDO structures have been used in ILCMs in [8][27][100][101].

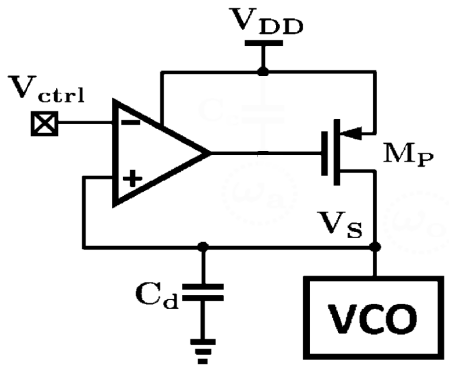


Figure 39: LDO structure

3.5 Existing gap

Designing an ILCM in deep submicron CMOS technology raises several issues [2][16][33] [34][93][95][100]. First, custom analog/digital ILCM designs are not easy to port to new CMOS processes. Second, analog designs are, by nature, more prone to noise coupling than digital designs. Third, single-ended ILCM designs suffer from noise coupling and typical true differential structures suffer from reduced voltage headroom. Fourth, PVT calibration technique that can fully compensate for PVT variations are critical to overcome temperature and voltage variations over time, as well as WID variations that can result in frequency offset. Fifth, an injection technique that is PVT immune is indispensable to achieve high performance. We can note that these effects are becoming more significant with technology scaling. To tackle these issues, a fully synthesizable DCRO based ILCM with a PVT calibrator will be proposed and further detailed in the next chapter. The proposed design aim is to meet the following state-of-the-art research gaps that need to be addressed:

- Array based DCRO structures have been used in several ILCMs as they offer linear frequency steps. In [26][27][36][91], authors used this structure and implemented it with the aid of single ended delay cells. As a result, these designs are prone to noise coupling, which negatively affects the phase noise, jitter and spurs. Therefore, an

array based DCRO structure built of pseudo differential delay cells will be proposed in this work to reduce noise coupling.

- PVT calibration methods using replica oscillator have been introduced in [24][25][32] [44]. With VT variations, the main and replica oscillators frequencies change differently, which is a challenge with this technique. In [32], a Voltage Controlled Delay Line (VCDL) used replica delay cells to calibrate the main VCO. A problem with this technique is that any mismatch in the delay cells and routing between the VCDL and VCO is not accounted for, which results in different frequency ratios between the VCDL and VCO over temperatures and voltages. Authors of [24], [44] and [25] stated that their techniques do not compensate for frequency mismatch between main and replica DCROs after initial calibration. Consequently, there is a need for a replica based calibration technique that can calibrate for the frequency differences between main and replica oscillators as will be investigated in the proposed PVT calibrator.

- In traditional sequential injection techniques found in previous designs [32][45], the fractional resolution is limited to the inverse of the number of ring oscillator stages or double the number of ring oscillator stages in the case where negative edge phases are also used (*i.e.* $f_{res} = f_{ref}/N_{osc}$ in [45] and $f_{res} = f_{ref}/2N_{osc}$ in [32]). Hence, for better resolution, the number of stages has to be increased; consequently, this reduces the oscillating frequency of the ring oscillator, increases power consumption at a given frequency, increases jitter due to delay cell mismatch, and reduces the locking bandwidth [32][76]. Thus, a new method that can provide fine fractional resolution without increasing N_{osc} will be explored in this design.

3.6 Conclusion

In this chapter, design considerations of ILCMs were elaborated and different design techniques in prior works were discussed. After reviewing the literature, several ILCM design issues in deep-submicron CMOS technology were pointed out. Then, different techniques employed in the proposed design to address these issues were discussed. Afterwards, research gaps in literature were illustrated. In the next chapter, the proposed ILCM structure will be presented, sub-harmonic integer and fractional modes of operation will be examined, online and offline PVT techniques will be elaborated and WID variations effect on the DCRO frequency will be deduced. Additionally, advances of the proposed design compared to prior works and its novelty will be highlighted.

4

Proposed design

The design techniques we propose to address current ILCM challenges will be discussed in this chapter. A detailed description of the proposed ILCM structure will be provided. The building blocks including DCRO matrix, injector, and control logic will be elaborated. Next, the sub-harmonic injection locking technique will be presented and its integer and rotational fractional injection modes will be detailed. Afterwards, the proposed PVT technique will be explored, where online and offline calibration modes will be discussed. Then, random mismatch variations' effects on ILCM performance will be explained and a formula for relative variations in DCRO period will be derived. Finally, advantages of the proposed design will be discussed.

4.1 ILCM structure

The proposed ILCM architecture is shown in Figure 40. It consists of main and replica DCROs (DCRO1 and DCRO2, respectively). The replica DCRO and the digital counters are used for calibration purposes as will be illustrated in Section 4.3. Each DCRO is controlled by a FCW, which is provided to it by the control logic. Serial data are input to the ILCM, then shift registers in the control logic change the data from serial to parallel. The control logic stores the FCW, enables/disables the DCROs and counters, selects integer/fractional operation modes, and selects the injection sequence as will be discussed in Section 4.2. The binary encoded FCW is fed into an 8-bit thermometer decoder that provides monotonic frequency tuning of the DCROs by enabling multiple delay cells in the DCRO using 256 control lines ($EN[0:255]$). Each $EN[i]$ signal is connected to the enable of a delay cell. Hence, when the FCW increases, more delay cells are enabled sequentially. Injector and select signals are only provided to DCRO1, as DCRO2 operates in free-running mode when calibration is required. The square-wave reference signal (REF) is input to the injector, which generates the injection pulse ($Pulse$) and differential reference signals (REF_n and REF_p). Select signals include SEL_{sign} (used to switch REF_n and REF_p polarity), SEL_{cell} (selects which column of delay cells is used for injection in fractional mode at each reference clock) and $SEL[0:3]$ (decoded version of the binary encoded SEL_{cell} signal). The next subsections will discuss different building blocks of the ILCM.

4.1.1 DCRO matrix

The proposed DCRO is implemented using an array structure to achieve uniform frequency steps and reduce the effect of random mismatch between delay cells. The main and replica DCROs are each composed of a 4×64 matrix of delay cells as shown in Figure 41, where only 4×63 cells can be tuned on or off as the first row is always enabled unless the oscillator is turned off. Each column's output is connected in parallel to the outputs

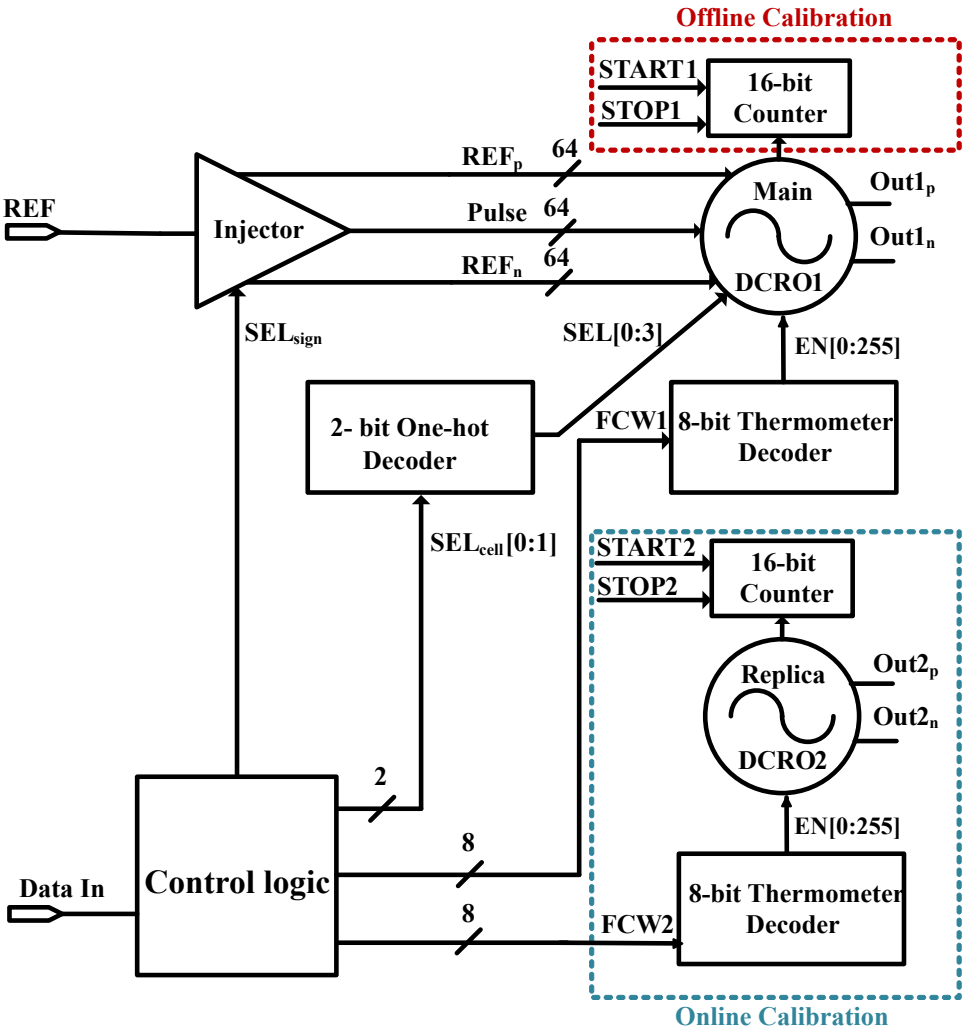


Figure 40: ILCM structure

of the same column. The last column outputs are cross connected to the first column inputs for oscillation to occur. Thus, the DCRO produces 8 quadrature outputs. The rest of delay cells are enabled one after the other to increase the drive current charging the load capacitance at each node in the matrix, thereby increasing the frequency as shown in Equation (25). The maximum frequency is obtained when all delay cells are enabled. In other words, the DCRO tunes the frequency in a discrete fashion with a non-constant frequency resolution across the frequency tuning range, due to the small intrinsic capacitance each delay cell adds when enabled. As mentioned in Chapter 2, the frequency tuning resolution determines the multiplication factor. In this design, it

depends mainly on the number of delay cells in parallel. Consequently, as the number of matrix elements increases, the frequency tuning resolution improves at the expense of power consumption and silicon area. Improved frequency resolution would also result in lower spurious levels as discussed in Chapter 3. Each DCRO delay cell has 5 input signals besides the differential inputs coming from the previous stage. These input signals are: $EN[i]$ that enables or disables the delay cell, $SEL[i]$ that selects the delay cells for injection, and $Pulse$, REF_n and REF_p in case the delay cell was selected for injection.

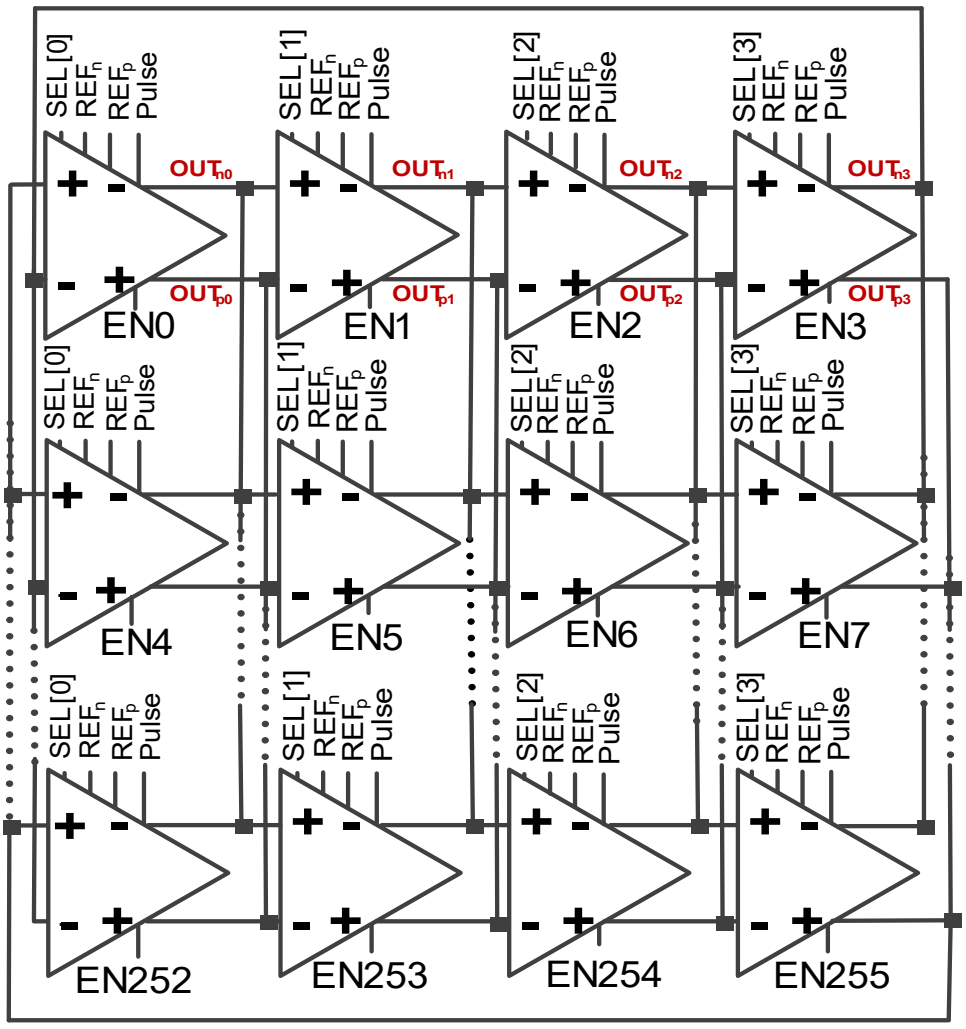


Figure 41: DCRO matrix

Each delay cell consists of delay logic (implemented using two tristate drivers and a cross

coupled inverter latch) and injection logic for forcing the internal delay cell signals to align with the differential reference clock signals (implemented using two tristate buffers and an AND gate) as shown in Figure 42. The two tristate inverters are sized larger than the cross coupled pair by a factor of 4 (using INVTD4 and INVTD1 logic gates). Furthermore, the two tristate injection buffers are sized smaller than the tristate inverters by a factor of 1.7 and implemented using BUFTD2 gate, and the injector AND gate is implemented using CKND2 gate from the standard cell library.

For DCRO2, the injection logic is included so that both DCROs will have similar free-running frequencies; however, the logic is disabled by connecting the injection logic inputs to logic 0. Each column of the matrix is connected to the same select signal ($SEL[i]$). As a result, all the cells in the column are injected at the same time in injection mode. This provides a strong injection signal to overcome the internal nodes of the delay cells. Pseudo differential delay cells are used in the delay logic for their superior noise rejection and rail-to-rail signal swing.

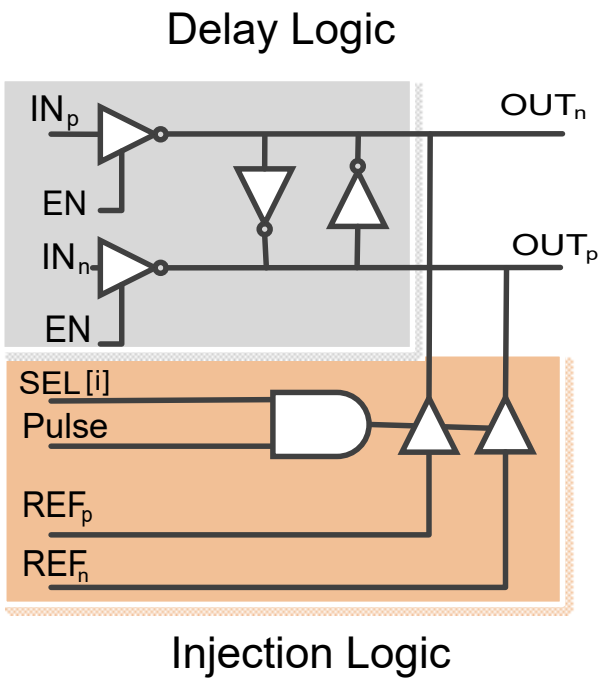


Figure 42: Delay cell circuit

4.1.2 Injector

The injector structure is shown in Figure 43. The reference signal typically comes from a signal source generator and gets converted to a square wave with the aid of an on-chip input buffer. The injector is implemented using four main blocks. First, a pulse generator is used to generate the injection pulse signal for DCRO1 when in injection mode. The REF signal is fed into an AND gate and a chain of inverters to provide a narrow $Pulse$ signal at the output of the AND gate. Second, a Single-To-Differential (STD) signal converter is used to provide REF_n and REF_p using two XOR gates and cross coupled inverters to generate symmetric signals. Third, an edge selection block swaps the differential reference signals when SEL_{sign} is high. Fourth, a symmetric clock tree to distribute $Pulse$, REF_n and REF_p signals among the delay cells with minimum clock skew, so that injection occurs at the same time for all delay cells in the selected column (*i.e.* whichever column of cells has its $SEL[i]$ signal high). Each of the clock tree output signals is composed of 64 bits, each bit goes to one row of the DCRO matrix. As shown in Figure 44, the clock tree is composed of two inverter stages, where each inverter drives four other inverters of the same size. The 64 output signals drive four parallel buffers (one row) of smaller sized logic gates in the injection logic. Thus, the $Pulse$, REF_n and REF_p signals arrive at the DCRO injection logic with very small time differences in order to achieve high performance.

The chain of inverters is implemented using minimum sized inverters (CKND0) and CKAND8 is selected for the injector AND gate. CKXORD4 and CKND1 are used to implement the STD. The edge selection block is built from two parallel MUXs (CKMUXD4) whose select is connected to SEL_{sign}. All of the clock tree inverters use CKND16 gates to be able to drive two rows and each has CKAND2 gate for its injection logic. It is worth mentioning that clock standard cells (CKXXX) are used in the injector to achieve symmetric rise and fall times.

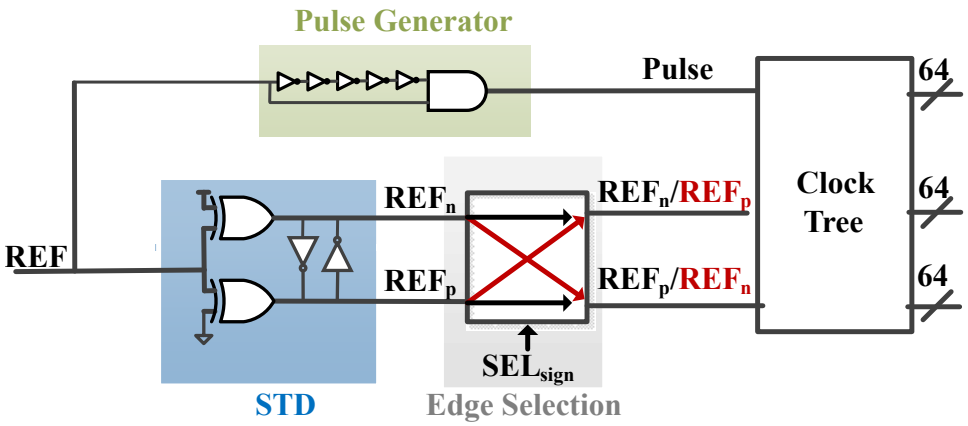


Figure 43: Injector circuit

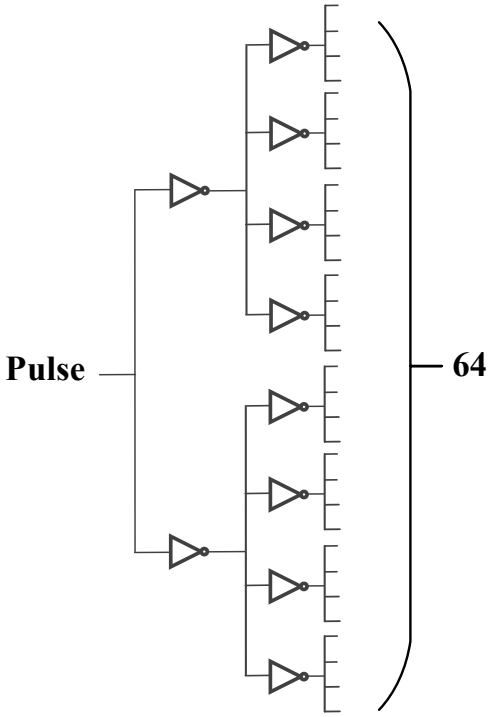


Figure 44: Clock tree

4.2 Pulse injection locking technique

The reference signal is injected periodically every N cycles to continuously realign the RO transitions, hence, the RO is said to be locked to the N^{th} harmonic of the reference. As long as the difference between the reference harmonic frequency $N \times f_{ref}$ and

the free-running frequency f_{osc} is within the locking bandwidth, the RO will maintain a locked condition and the RO output frequency f_{out} will be equal to the reference harmonic frequency [69]. The best phase noise and jitter performance is achieved when the difference between $N \times f_{ref}$ and f_{osc} is minimized as discussed in Chapter 3.

During injection, the differential reference signals REF_n and REF_p ideally intersect at 50% of the supply voltage in the middle of the injection pulse, as shown in Figure 45. When $Pulse$ and $SEL[i]$ are high, REF_n and REF_p are injected into the OUT_p and OUT_n nodes of the delay cells to force their transitions to occur at the same time relative to REF_n and REF_p at each reference clock cycle [45]. Only one column can be selected for injection on each reference clock cycle based on the values of the $SEL[0:3]$ signals. This injection technique does not require a precise pulse signal generator since injection occurs within the pulse window and is not controlled by the pulse directly. This overcomes the challenges of generating a precise pulse signal at high frequencies. The following subsections describe integer and fraction injection modes of operation.

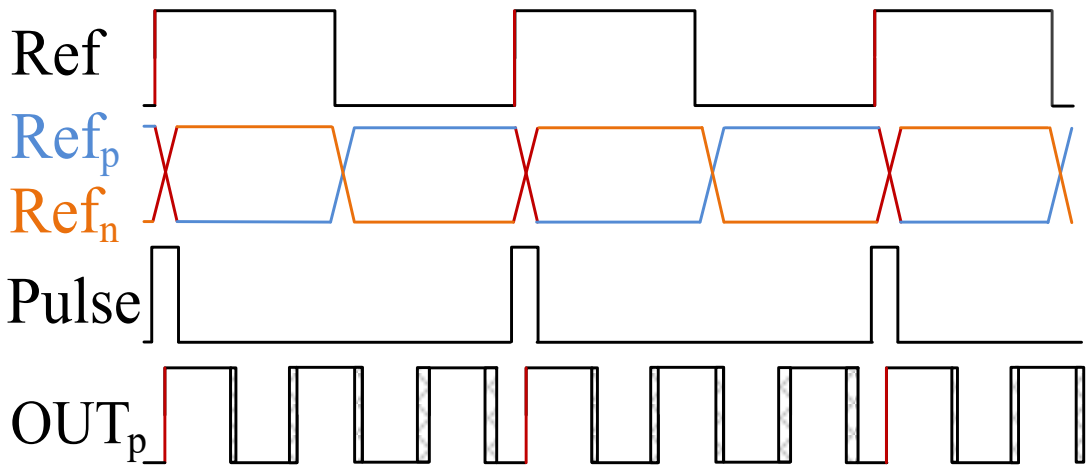


Figure 45: Sub-harmonic injection locking

4.2.1 Integer mode of operation

In integer mode, the reference signal is injected into the same DCRO1 output every N output cycles, where N is 3 in Figure 45 (i.e., the oscillator is locked to an integer harmonic of the reference signal). A square wave $Pulse$ signal, generated from the

reference signal, is fed into DCRO1. From the Fourier series expansion, a non-ideal square wave, which has finite rise/fall times, is a summation of weighted sine and cosine waves of reference frequency harmonics. As the order of the harmonics increases, the amplitude of Fourier harmonic coefficient decreases, as can be seen in Equation (47) [29], where ζ is the pulse width and δ is the rise/fall time of the square wave. Therefore, the injection power is higher at low order harmonics meaning that the phase noise and locking bandwidth will improve at these harmonics as discussed in Chapter 2.

$$C_{n_{real}} = \frac{\zeta}{T_{osc}} \times \cos(-n\pi\frac{\delta+\zeta}{T_{osc}}) \times sinc(\frac{n\pi\delta}{T_{osc}}) \times sinc(\frac{n\pi\zeta}{T_{osc}}) \tag{47}$$

In this work, harmonics from 1^{st} to 9^{th} were investigated. This range of harmonics provides good phase noise performance, as well as a locking bandwidth approximately three times the frequency tuning steps to provide reliable injection locking, as will be further discussed in the next chapter. If harmonics higher than the 9^{th} are used, the locking bandwidth and tuning range will decrease. Only one of the $SEL[i]$ signals is enabled in this mode of operation and therefore only one column of delay cells is injected every N reference cycles. The DCRO1 frequency can be written as:

$$f_{osc} = Nf_{ref} \tag{48}$$

4.2.2 Fractional mode of operation

In the fractional mode, the rising edge of the reference signal is injected into different delay cells in a rotational sequence to achieve a fractional injection ratio. As can be seen in Figure 40, the $SEL[i]$ signals are responsible for selecting different columns of delay cells that are to be injected at the next reference edge. Whereas, the SEL_{sign} determines whether the positive or negative edge of the delay cell outputs (OUT_n and OUT_p) will be injected by swapping the REF_p and REF_n signals, as shown in Figure 43. This feature further enhances the frequency resolution. FCW1 controls the integer multiplication (N), while $SEL[i]$ and SEL_{sign} control the fractional multiplication (M) of DCRO1. Hence, the output frequency is a fractional multiple (K) of the reference signal frequency. Figure

46 shows the timing diagram for the REF, $SEL[i]$ and $Pulse$ signals with $N = 3$ and $M = 1/8$. It can be noted that the $SEL[i]$ and SEL_{sign} signals change on the negative edge of REF to allow the signals to settle before the next injection pulse and minimize switching noise. Moreover, they are stored in a fractional selector composed of 3×128 shift register that provides a programmable fractional frequency multiplication factor K with a frequency resolution of $1/32 \times f_{ref}$, as shown in Figure 47. First, $SEL[i]$ and SEL_{sign} values are loaded to the shift register by the aid of the control logic. Then when fractional injection mode is enabled, these signals are fed to DCRO1 every reference cycle.

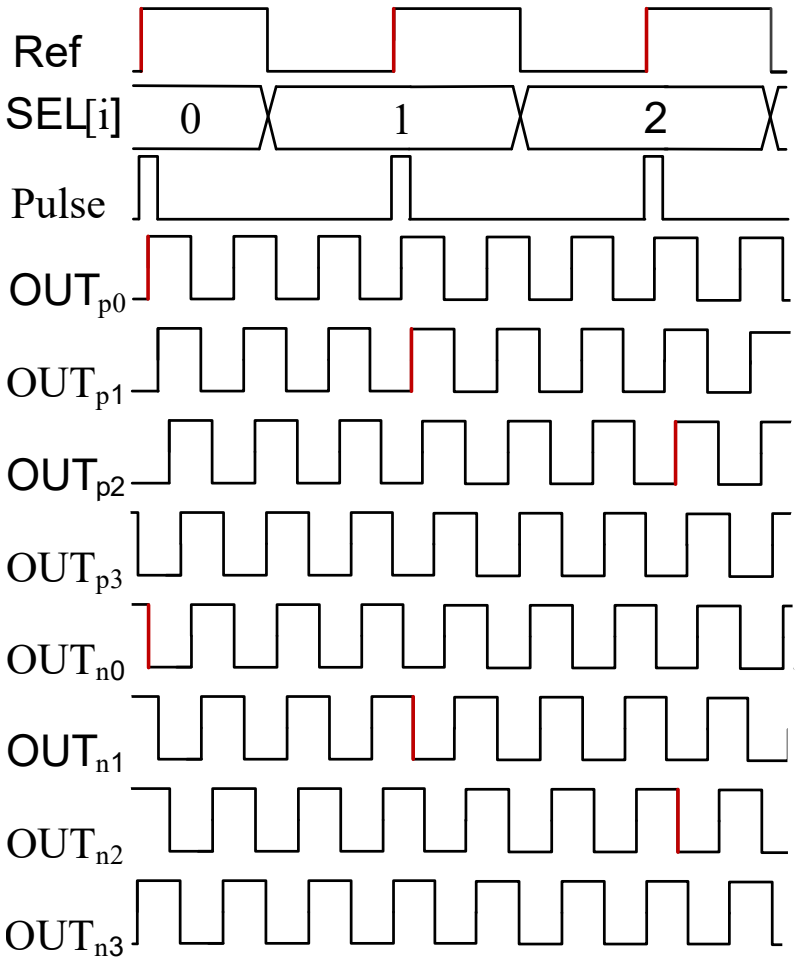


Figure 46: Fractional injection locking

The fractional frequency can be expressed as:

$$f_{osc} = Kf_{ref} = (N + M)f_{ref} \tag{49}$$

and M is given by:

$$M = \frac{PH_{av}}{2 \times N_{osc} \times j} \tag{50}$$

where j is the number of consecutive injections per stage and PH_{av} is the average phase shift per reference cycle, which depends on SEL_{sign} and the number of delay cells that are skipped per reference cycle. As an example, if 9/16 fraction is chosen, j is set to 1 (because the fraction is greater than 1/8) and PH_{av} must be set to 4.5 to achieve the required fraction. Figure 48 shows a phase diagram that explains how the RO output edges occur at different phases with phase differences of $2\pi/8$. Points 0 to 7 are injection points that are selected by $SEL[i]$ and SEL_{sign}. PH_{av} can be set to 4.5 by choosing the injection points to rotate each reference cycle as $0 \longrightarrow 5 \longrightarrow 1 \longrightarrow 6 \longrightarrow 2 \longrightarrow 7 \longrightarrow 3$ and so on. Parameter j is set to 1 by injecting each of these points once.

We can note that by being able to inject the same matrix column consecutively more than once, by setting j to be more than 1, we can achieve fractional resolution below $f_{ref}\ /2N_{osc}$

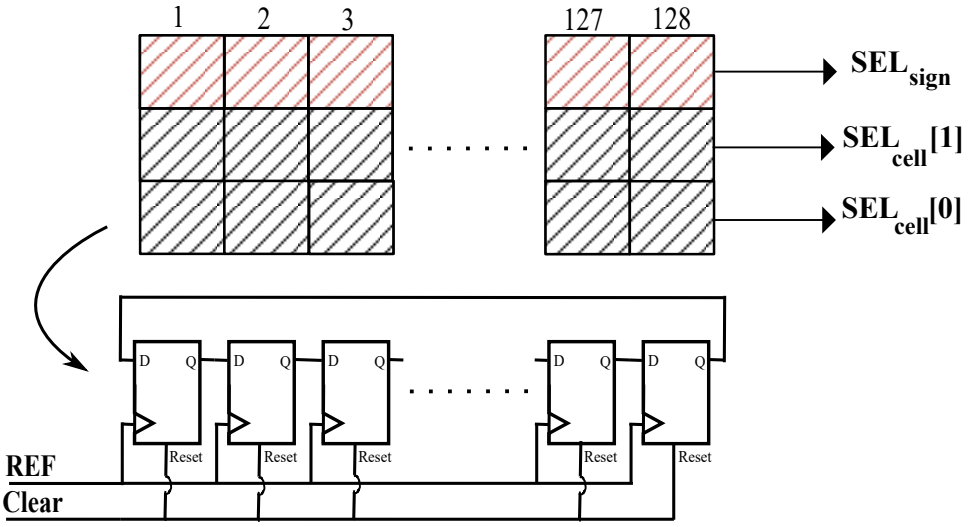


Figure 47: Fractional selector

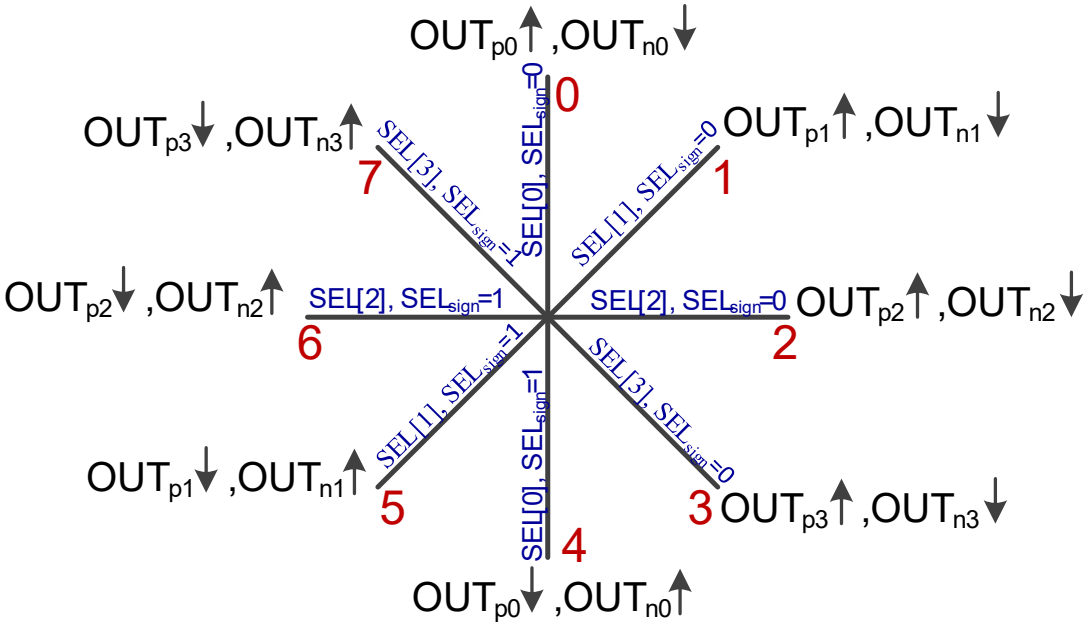


Figure 48: Phasor diagram of fractional operation

4.3 PVT Calibration

ILCMs are sensitive to PVT variations as discussed in the previous chapters. This work investigates two techniques for PVT calibration namely, online and offline calibration as shown in Figure 40, where the control logic selects between the two calibrations techniques. In the online calibration method, DCRO2 and a high-speed counter are used to track real time PVT variations. The counter acts as a frequency-to-digital converter to calibrate DCRO1 using the frequency reading obtained from DCRO2 in real time. Figure 49 shows the three calibration phases: initial calibration, calibration, and sleep. During the first phase of calibration, the DCRO1 and DCRO2 free-running frequencies ($f_{hi1,init,i}$ and $f_{hi2,init,i}$) are measured at a given initial supply voltage and temperature. In the second phase, the reference signal is then injected into DCRO1 while DCRO2 is free-running and counter 1 is disabled. Knowing DCRO1 and DCRO2 free-running frequencies from the first phase of calibration and DCRO2 free-running frequency at any given supply voltage and temperature, we can estimate the required FCW1 for DCRO1 to obtain a free-running frequency in the center of the locking bandwidth for best phase

noise and jitter performance. Furthermore, DCRO2 and its associated counter can be disabled after a calibration cycle to reduce power consumption in the third phase.

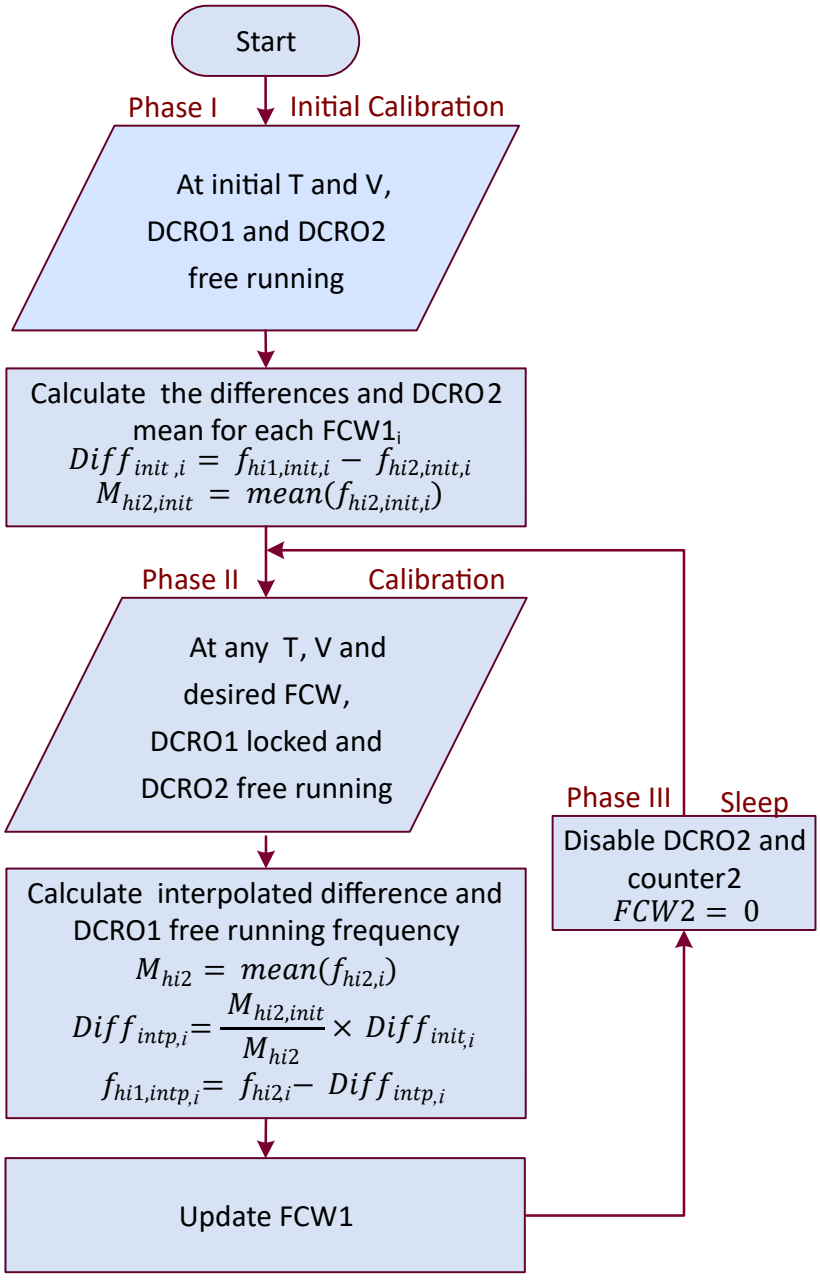


Figure 49: PVT online calibration flow chart

As shown in Figure 49, the interpolated free-running value of DCRO1 ($f_{hi1,intp}$) is calculated in phase II from: (1) the mean of frequencies of DCRO2 in phase I ($M_{hi2,init}$), (2) the difference between DCRO1 and DCRO2 frequencies in phase I ($Diff_{init,i}$), (3) DCRO2

free-running frequencies in phase II ($f_{hi2,i}$), and (4) the mean of frequencies of DCRO2 in phase II (M_{hi2}). The timing diagram of the proposed online calibration method is shown in Figure 50. In phase I, DCRO1 and DCRO2 are operated sequentially to obtain the tuning curves from which the DCRO2 mean frequency and frequency differences between DCRO1 and DCRO2 are calculated. The frequency tuning curves are discrete and DCROs' frequency readings are not exactly the same due to automated $P\&R$. In phase II, the DCRO2 tuning curve is obtained and FCW1 is updated, this phase takes less than 200 μs. In phase III, the calibration is paused and DCRO2 is turned off for a programmable period of time (typically longer than the phase II duration). Phase II and phase III are repeated at some regular update intervals. It is worth mentioning that DCRO1 free-running frequency is estimated from DCRO2 updated frequency readings in every calibration phase at a voltage and temperature different from those of the initial calibration phase. This indicates that the proposed calibration technique can calibrate for frequency differences between the two DCROs at different VT conditions.

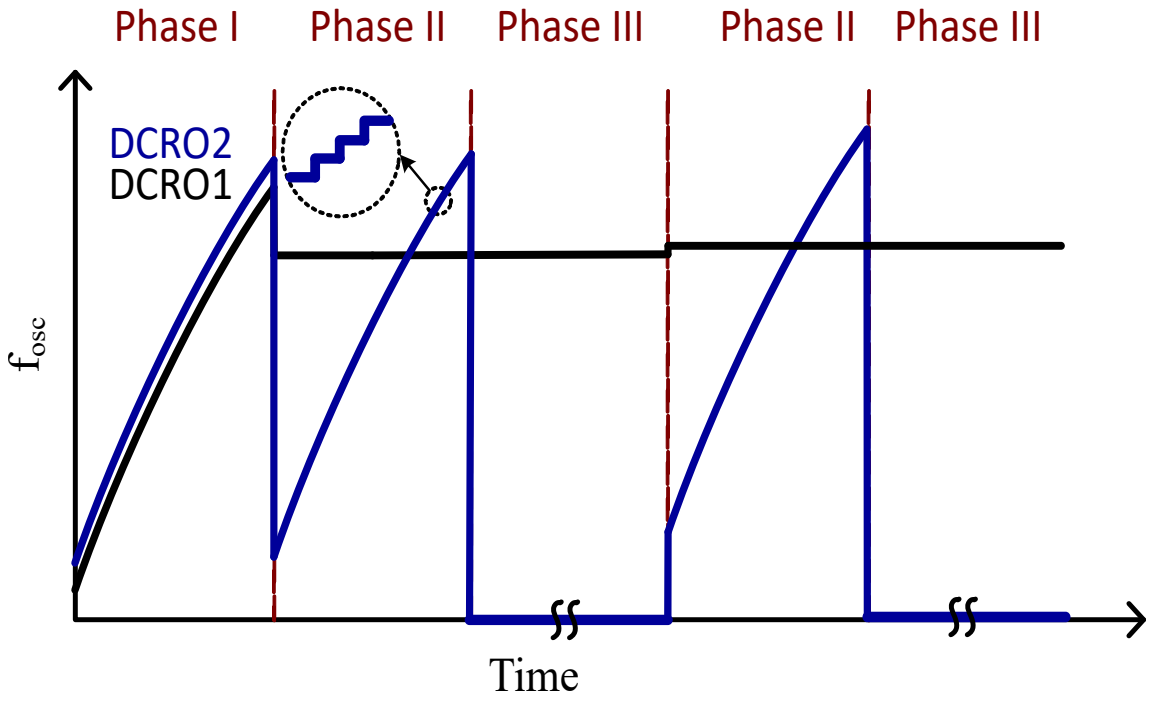


Figure 50: PVT online calibration time diagram

The second technique, offline calibration, utilizes only DCRO1 and its associated counter while DCRO2 and its associated counter are disabled at all times. Unlike online calibration, the calibration takes place when the main DRCO is free-running. The main counter reading is then used to tune the main DCRO1's FCW1 before injection (*i.e.* whenever calibration is required, the injector is disabled and the DCRO1 output frequency is not injection locked).

The calibration counters use asynchronous 16-bit ripple counters for high accuracy and low power consumption as shown in Figure 51. The counter resolution is $f_{max}/2^n$, where f_{max} is the maximum output frequency of the oscillator and n is the number of counter bits. The counter resolution (27 kHz) is significantly lower than the smallest step size (5 MHz). The control logic provides START and STOP signals to control the counters' operation. The START signal resets the counters and triggers them to start counting; then a precisely timed STOP signal is set high to stop the counting process and store the readings. A small delay between the STOP signal and storing the readings allows the asynchronous ripple counter bits to settle. The time difference between the two signals and the counter reading are used to calculate the DCRO frequency. Since asynchronous ripple counters are simple to implement (only D flip-flops are used), they show superior performance in terms of power, operating frequency and area. It is worth mentioning that the accuracy of START and STOP signals is important to obtain an accurate frequency reading. To further enhance their accuracy on-chip crystal oscillators based circuits can be implemented to provide these two signals.

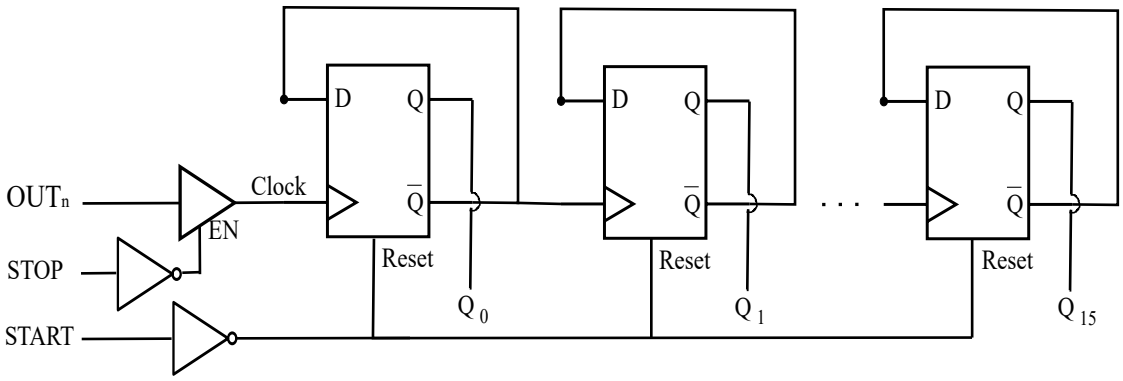


Figure 51: Asynchronous counter

4.4 Random Mismatch

Keeping f_{osc} as close as possible to $K \times f_{ref}$ can be achieved by reducing PVT effects using calibration, as well as, reducing WID variations in the DCRO. With technology scaling, WID variations are becoming as large as D2D variations [37]. D2D variations are mainly due to systematic variations caused by imperfect manufacturing, whereas WID variations are due to random device mismatch caused by effects such as channel dopant, oxide charges, local mobility fluctuations, etc.[38][102]. As reported in [38], frequency variation due to WID and D2D variations in a 5-stage RO is about 3% (30 MHz). Such deviation from the free-running frequency will affect the ILCM jitter and reference spurious level negatively, as f_{osc} will be offset from $K \times f_{ref}$, and may cause the ILCM to lose lock at high harmonics. The proposed design aims to reduce such variations to obtain lower jitter and spurious level. Threshold voltage (V_t) and current factor (β) WID variations are two of the main contributors to performance variation in MOSFETs [98][102]. Variations in V_t and β are considered random variables with Gaussian distributions. Random variations in V_t and β for two identical devices, assuming they are closely separated, are given by:

$$\sigma_{Vt}^2 = \frac{A_{V_t}^2}{WL} \text{ and } \frac{\sigma_\beta^2}{\beta^2} = \frac{A_\beta^2}{WL} \tag{51}$$

where A_{V_t} [mV$\times\mu m$] and A_β [%$\times\mu m$] are technology parameters obtained experimentally. The effective Length (L) and Width (W) of a transistor are the drawn length and width subtracted by channel length and width reduction parameters. These effects happen due to lateral diffusion of source and drain diffusions and encroachment of field oxide into the channel [87]. For simplicity, we assumed that the effective L and W are approximately equal to the drawn L and W. It can be shown in Equation (51) that WID variations averages out as the area increases due to its random nature.

In order to examine the effect of V_t and β variations on the proposed DCRO relative period mismatch ($\frac{\sigma_T}{T}$), we first assume that an NMOS transistor is operating in the saturation region with drain current (I_N) approximately equals to Equation (52) and time delay (τ_d) equals to Equation (53), where ΔV is the voltage swing and C is the total load capacitance.

$$I_N \simeq \frac{\beta}{2}\left(V_{GS} - V_t\right)^2 \tag{52}$$

$$\tau_d = \frac{\Delta V \times C}{I_N} \tag{53}$$

By substituting Equation (52) into Equation (53), we get the time delay as follows:

$$\tau_d \simeq \frac{2 \times \Delta V \times C}{\beta\left(V_{GS} - V_t\right)^2} \tag{54}$$

The variance of the delay can be expressed as Equation (55), assuming uncorrelated V_t and β variations. Substituting Equation (54) into Equation (55) gives the delay variance shown in Equation (56) and hence, the relative mismatch variance in the delay can be approximated as in Equation (57).

$$\sigma^2_{\tau_d} \simeq \left(\frac{\partial \tau_d}{\partial \beta}\right)^2 \times \sigma^2_\beta + \left(\frac{\partial \tau_d}{\partial V_t}\right)^2 \times \sigma^2_{V_t} \tag{55}$$

$$\sigma^2_{\tau_d} \simeq \left(\frac{-2 \times \Delta V \times C}{\beta^2 \times \left(V_{GS} - V_t\right)^2}\right)^2 \times \sigma^2_{\beta}. + \left(\frac{4 \times \Delta V \times C}{\beta \times \left(V_{GS} - V_t\right)^3}\right)^2 \times \sigma^2_{V_t} \tag{56}$$

$$\frac{\sigma^2_{\tau_d}}{\tau^2_d} \simeq \sigma^2_\beta + \frac{4 \times \sigma^2_{V_t}}{\left(V_{GS} - V_t\right)^2} \tag{57}$$

Assuming identical transistors, we can express the RO period as Equation (58) and assuming statistically independent variations of single gate delays, we get Equation (59). Therefore, the relative variations in a DRCO period is found as Equation (60) and similar expressions can be obtained for the PMOS transistors.

$$T = 2 \times N_{osc} \times \tau_d \tag{58}$$

$$\sigma_T^2 = 4 \times N_{osc}^2 \times \sigma_{\tau_d}^2 \tag{59}$$

$$\frac{\sigma_T^2}{T^2} \simeq \sigma_\beta^2 + \frac{4 \times \sigma_{V_t}^2}{(V_{GS} - V_t)^2} \tag{60}$$

In the proposed structure, parallel inverters increase the transistor width by U, where U is the number of parallel transistors rows. The frequency increase as U increases. Hence, the relative variations in the proposed DCRO period can be expressed as:

$$\frac{\sigma_T^2}{T^2} \simeq \frac{1}{U \times W \times L} \left(A_\beta^2 \times \beta^2 + \frac{4 \times A_{V_t}^2}{(V_{GS} - V_t)^2} \right) \tag{61}$$

This equation illustrates how the proposed design further decreases the relative variation in DCRO period by U compared to a single row RO. For the selected frequency range U is greater than 27, which greatly reduces delay cell and frequency step size variations, as well as, mismatch variations between the main and replica oscillators. Consequently, the proposed structure has the following advantages: 1) it has reduced jitter and spurious levels, 2) it can efficiently calibrate for PVT changes as the main and replica oscillators can better track each other and 3) it has an accurate tuning mechanism because frequency step size variations are decreased within the tuning range. It is worth mentioning that adding excessive rows to reduce mismatch will come at the expense of power consumption.

4.5 Design Summary

The proposed design goals are to reduce jitter and spurs level in an ILCM, meet deep-submicron CMOS design requirements, as well as tackle research gaps mentioned in the previous chapter. This is achieved using multiple techniques:

- The proposed design is all digital and fully synthesizable. All cells in the proposed design come from vendor supplied standard cell libraries. Standard CAD tools were utilized for synthesis and automatic Place and Route ($P\&R$). Fully synthesizable designs can be more easily ported to new technology nodes with shorter design times and reduced implementation costs [24][25][26].

- An array DCRO based on pseudo differential delay cells is utilized for frequency tuning for its advantages. First, unlike previous array based DRCO designs, pseudo differential delay cells are employed to reduce the effects of substrate and power supply switching noise coming from other digital circuits on the same chip. Moreover, the differential rail-to-rail signal swing provides increased output power, which further reduces the effects of external noise sources. Second, the proposed frequency tuning mechanism enables one delay cell at a time to change the frequency, which results in small and uniform step sizes. Third, the array structure helps reducing WID variations between delay cells, as they average out due to their random nature. It is worth mentioning that this is the first implementation of a fully synthesizable injection locked differential DCRO.

- The proposed design addresses the need for a replica calibration technique that compensates for main and replica frequency mismatch even after initial calibration. A novel online replica DCRO calibration algorithm has been adopted in this design to continuously calibrate the main DCRO. Unlike previous works, the algorithm periodically measures all the replica tuning codes to recalibrate the delta frequencies between the main and replica DCROs. Hence, the proposed design achieves superior jitter and PN performance compared to previous papers. In addition, an offline calibration mode is provided that could be used without a replica DCRO to reduce silicon area for applications that do not require 100 % availability of the clock signal.

- The proposed design uses a novel sequential injection approach to achieve a fine

fractional resolution of $f_{ref}/8N_{osc}$. Therefore, the proposed design has the advantage of reducing the fractional resolution by at least 4 times the traditional sequential fractional designs in [32][45] without reducing the oscillating frequency or sacrificing the jitter, and without using dithering, which can increase the power consumption. Furthermore, unlike injection methods, which short the outputs when injecting the reference [24][34], reference injection in the proposed technique is not directly controlled by a pulse signal. Consequently, the proposed design eliminates the need for generating a narrow pulse for injection that is PVT dependent.

4.6 Conclusion

In this chapter, the proposed ILCM design was detailed. The utilized DCRO matrix and delay cell structure were provided, as well as the injector circuit. Integer and fractional sub-harmonic injection methods were explained. Integer and fractional multiplication factors formulas were concluded. Afterwards, online PVT calibration calculations and calibration phases were elaborated and their associated counter structure was presented. Then, the effects of threshold voltage and current factor random variations on the DCRO period were elaborated and advantages of the proposed DCRO matrix structure were highlighted. At last, a design summary of the proposed ILCM was detailed and compared to previous works. In the following chapter, simulation and measurement results of the proposed design will be presented.

5

Simulation and measurement results

The proposed ILCM design was simulated using Virtuoso Cadence to obtain the ILCM tuning curve, frequency step size, locking BW, and PN performance. Afterwards, the proposed ILCM was fabricated in 65 nm process. Measurement results for integer and fractional modes including tuning curves, frequency step size, locking BW, PN, jitter, reference spur and fractional spur will be presented in this chapter. They include the test of the ILCM performance in the presence of switching noise and VT variations. Finally, the measurement results will be compared to previous works.

5.1 Simulation results

The proposed design was implemented with the aid of commercially available CAD tools using a standard cell digital design flow, as shown in Figure 52. A syntheziable design means that it is described in HDL code then a synthesis tool is used to generate the gate

netlist from the code, finally the design is automatically placed and routed to generate the design layout (i.e no custom layout is required). For this design, gate level verilog was used to describe the two DCROs and injector using gates from the standard cell library, while the remainder of the logic was described in Register Transfer Level (RTL) verilog. The RTL verilog was synthesized using Synopsys Design Vision to generate the gate level netlist. The two netlists from Gate level and RTL verilog were combined and Cadence Encounter was used for standard cell $P\&R$ to generate the layout. Mentor Graphics Calibre was used for parasitics extraction and finally the post-layout verification was completed using Cadence AMS. The design flow was repeated several times until the design met the required specifications.

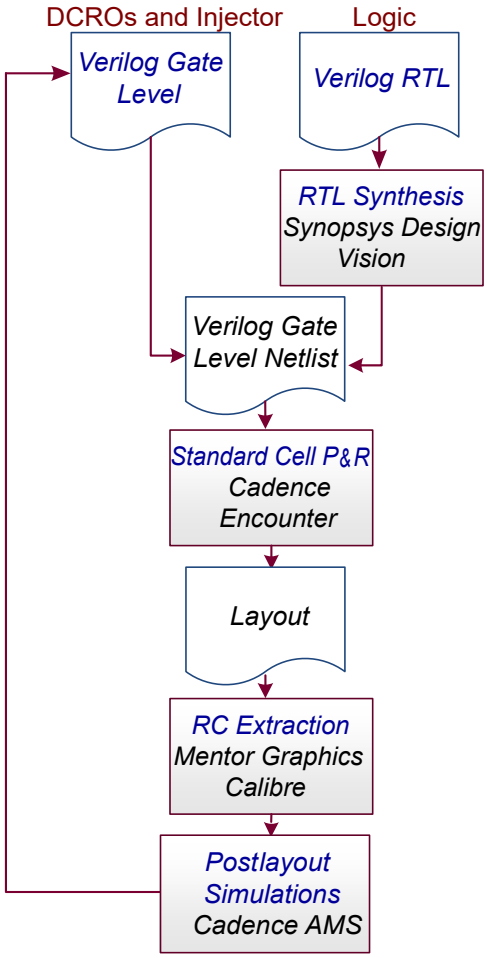


Figure 52: Digital design flow

The delay cell was implemented as shown in Figure 42 in the previous chapter. The delay cell driver to latch logic ratio is 4 : 1. Furthermore, the injector buffer in the injection logic to delay cell driver in delay logic ratio is 1.7 : 1, which resulted in a realignment factor (κ) of 0.75 at 1.1 V and room temperature [87]. Tuning curves were obtained using the simulation testbench shown in Figure 53. An ocean script, as well as Verilog-A codes, were used in the Cadence AMS environment to automate post-layout frequency calculations. Tuning curves at 0.9 V, 1 V, and 1.1 V vs FCW (up to code 255) are shown in Figure 54. The step size decreases as the FCW increases (i.e as more delay elements in the matrix are enabled). The average frequency step sizes over the whole FCW range at 0.9 V, 1 V, and 1.1 V were 7.6 MHz, 8.8 MHz, and 9.8 MHz, respectively.

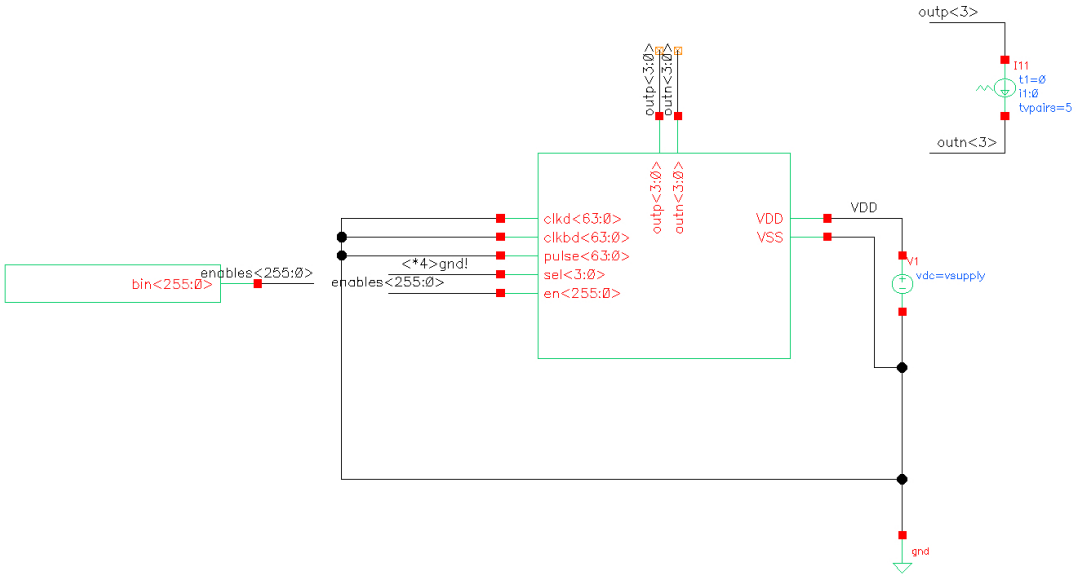


Figure 53: Tuning curve testbench

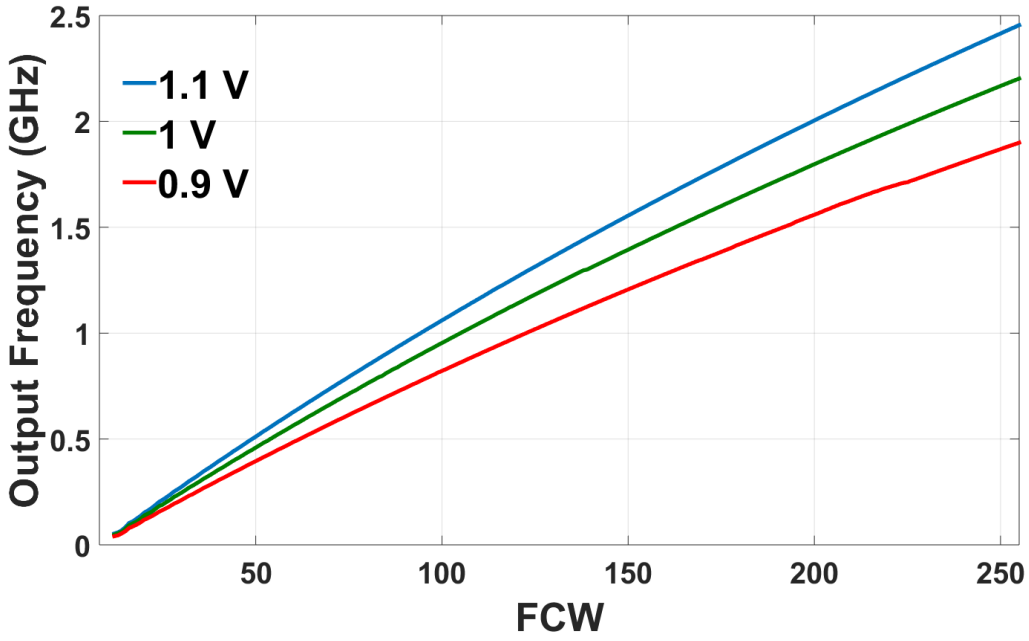


Figure 54: Simulated tuning curves at 0.9 V, 1 V, and 1.1 V

Injection simulation signals of the 3^{rd} harmonic can be seen in Figure 55. REF_p and REF_n override the delay cell outputs OUT_n and OUT_p every 3 cycles, when the Pulse signal is high at 1.1 V and room temperature. OUT_p and OUT_n of the first column are selected by setting binary signal $SEl[3:0]$ bits to 0001. The pulse signal width is 110 ps and REF_p and REF_n intersect approximately in the middle of the pulse. In the lock state, f_{osc} is equal to $3 \times f_{ref}$. The simulated locking BW is estimated using the testbench seen in Figure 56. Figure 57 shows the locking BW at the 3^{rd} harmonic and frequency step size vs FCW at 1.1 V and room temperature. The highest locking BW is 130 MHz and the lowest is 4.5 MHz. The DCRO tuning range was chosen so that the locking BW is approximately three times the frequency tuning resolution to provide extra locking margin. As previously shown in Equation (37), as the frequency increases, the locking BW increases. Moreover, as detailed in the previous chapter and shown in Figure 57, as the number of delay cells in parallel increases (i.e the DCRO frequency increases), the frequency step size decreases. Consequently, only the upper range of FCWs is used. It can also be noted that the frequency range of operation depends on the maximum

multiplication factor used.

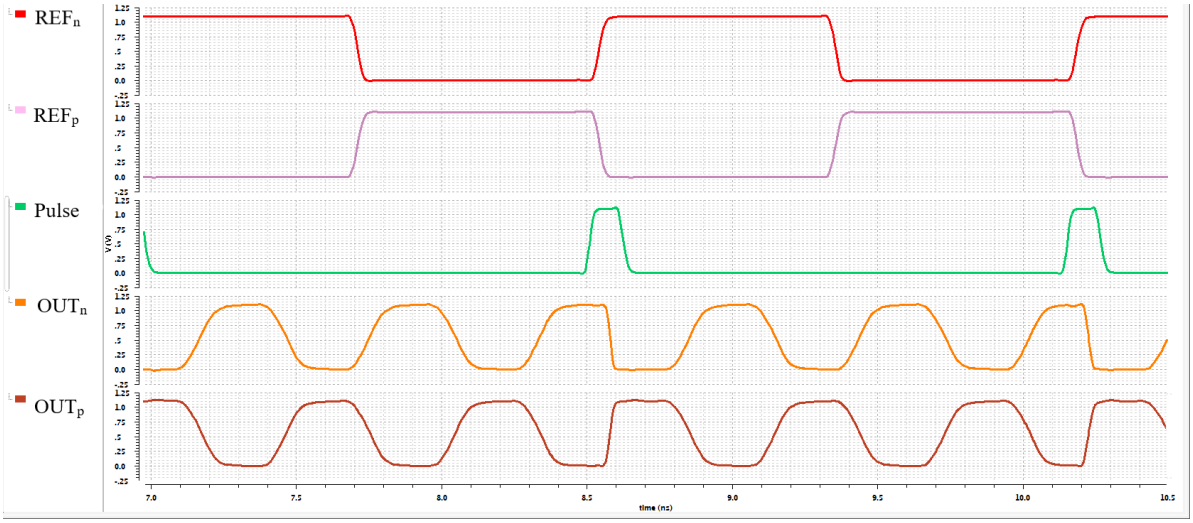


Figure 55: 3^{rd} harmonic injection locking

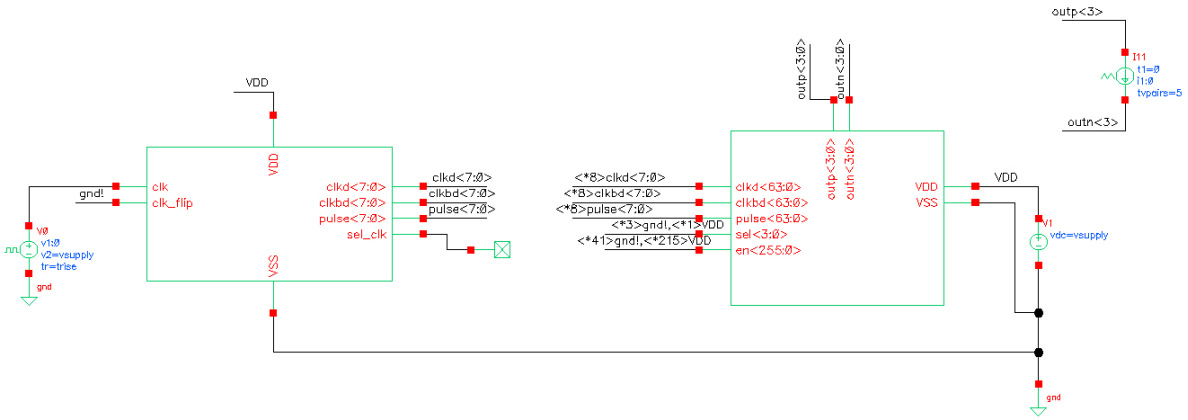


Figure 56: Locking BW testbench

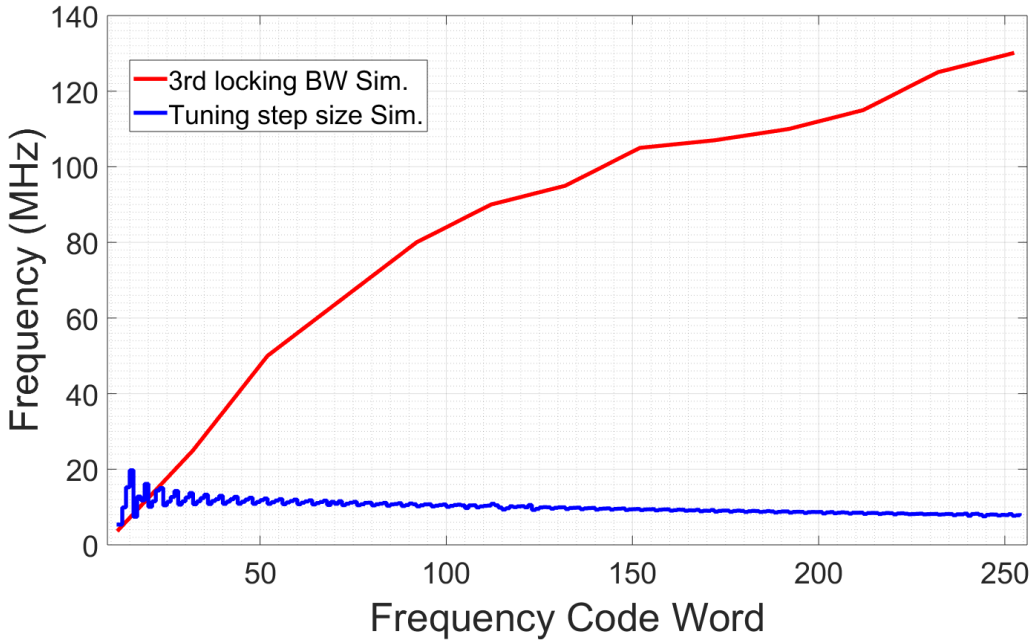


Figure 57: Locking BW and frequency step size vs frequency code word

The online PVT calibration technique, as described in Chapter 4, is simulated at different PVT conditions. The maximum absolute calibration error is evaluated for ss, tt and ff process corners, temperatures from 30 $°C$ to 70 $°C$ and voltages from 0.9 V to 1.1 V as shown in Figure 58 to Figure 60.

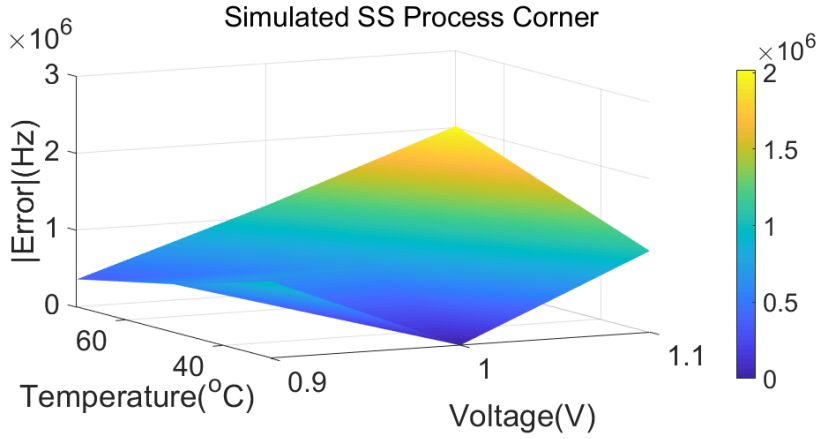


Figure 58: Maximum absolute calibration error at ss process corner

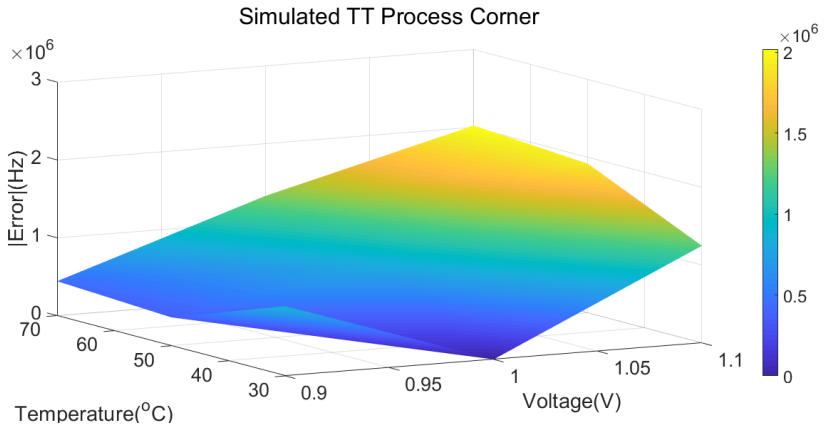


Figure 59: Maximum absolute calibration error at tt process corner

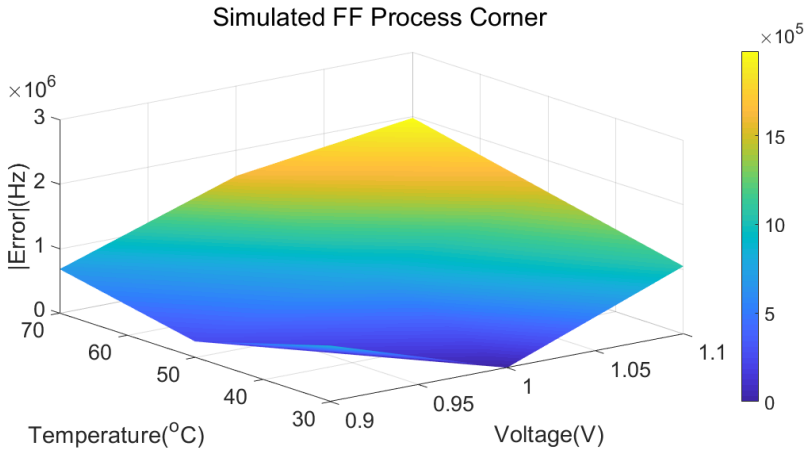


Figure 60: Maximum absolute calibration error at ff process corner

5.2 Measurement results

The proposed design was fabricated in TSMC 65 nm generic CMOS technology. The die micrograph is shown in Figure 61. The ILCM, including replica DCRO, control logic, injector, decoders, fractional selector, and counters, has a total die area of 124.5μm by 170μm. The chip was packaged in a 24-pin ceramic package and mounted on a custom Printed Circuit Board (PCB) for testing, as shown in Figure 62. LDOs are placed on the PCB along with potentiometers to adjust the test board supply voltages. Furthermore, a 3.3 V to 1 V level shifter has been used for the interface between the 8 bits coming from

the pattern generator and the chip input pins. In addition, decoupling capacitors were placed on board close to the chip, whose differential outputs were routed symmetrically to the PCB Sub-Miniature version A (SMA) output headers. The reference signal is injected through an input SMA header placed on the PCB.

Figures 63 and 64 show the PCB connections and measurement setup, respectively. The measurements were performed using: 1) a PCB with the packaged chip mounted on it, 2) a source meter to supply the chip with DC voltage, 3) a laptop to run matlab scripts to control the equipment using General Purpose Interface Bus (GPIB) protocol, 4) a pattern generator to load in data to program the chip using the control logic on-chip, 5) a signal source to provide the chip with the reference clock, and 6) a signal source analyzer to obtain the output spectrum and calculate PN and jitter.

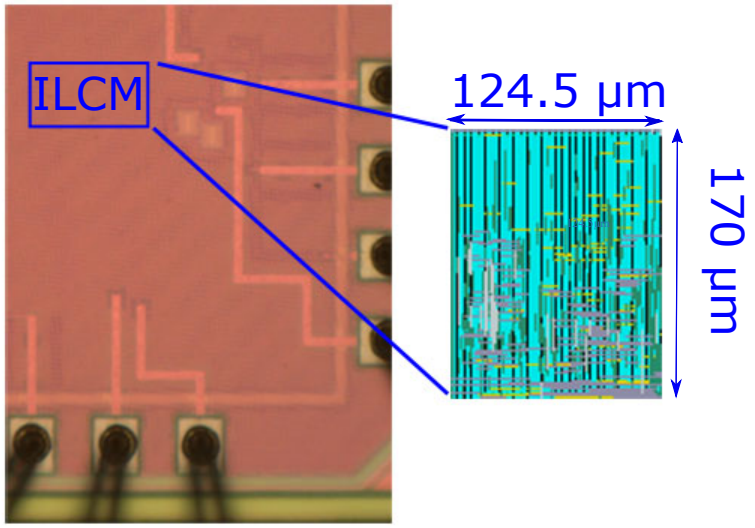


Figure 61: Die microphotograph of ILCM

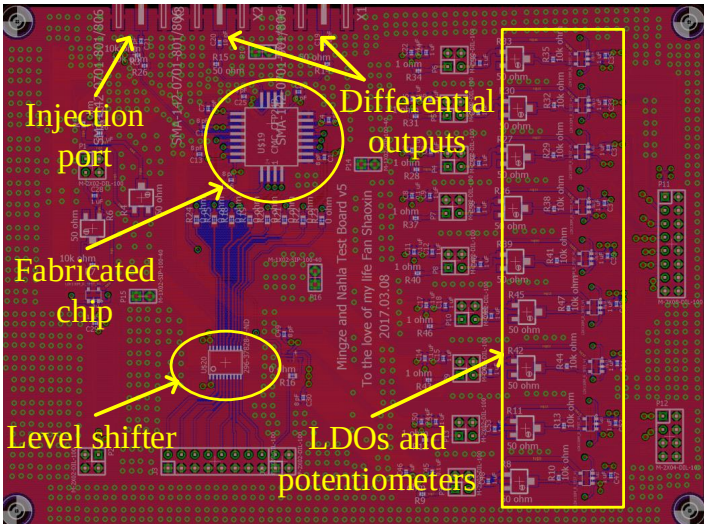


Figure 62: PCB layout

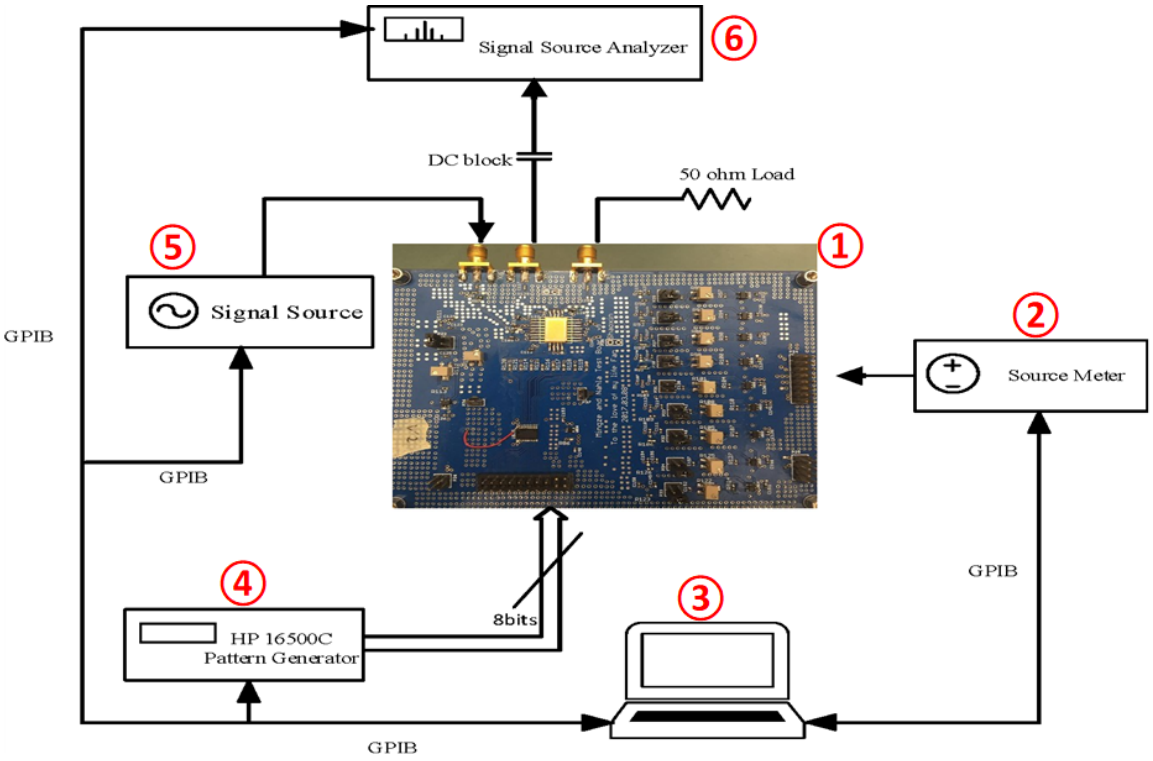


Figure 63: PCB connections

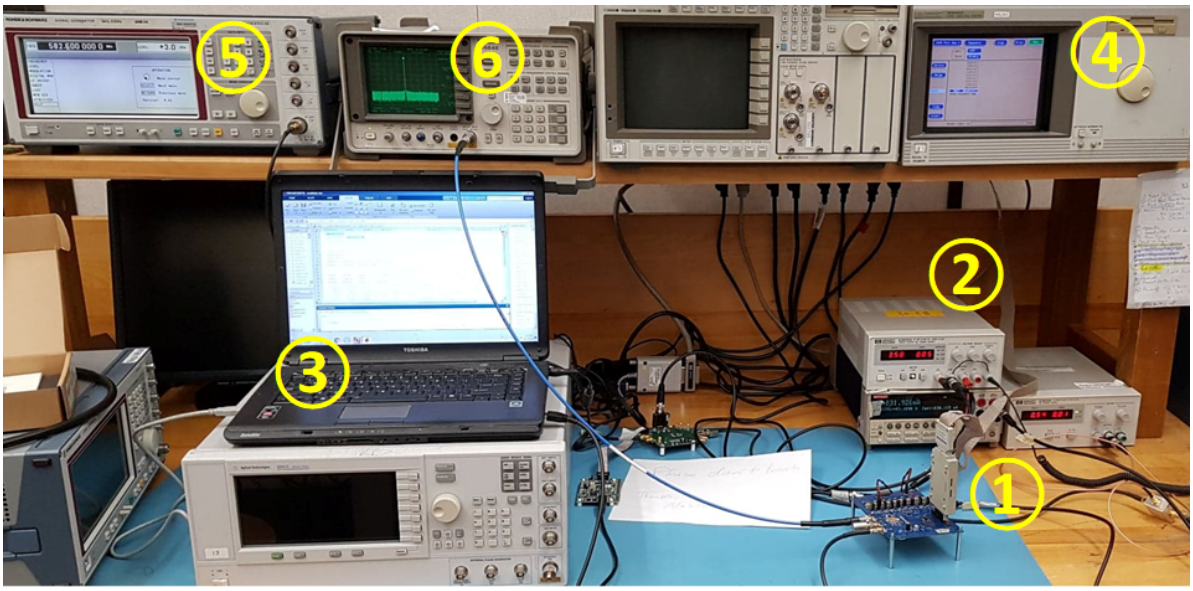


Figure 64: Measurement testbench

Figure 65 shows the primary and replica DCROs free running tuning curves at 1.1 V. It can be noted that their frequencies are non-identical. In addition, the frequency step size can also be seen in Figure 65. Non-linear capacitor behaviour at each node in the DCRO matrix results in non-constant step size across the entire frequency range. It can also be seen that the step size decreases as the FCW increases, as observed in the simulation results. The DCRO lowest usable output frequency is 1 GHz and the highest usable output frequency is 1.8 GHz. The worst case frequency tuning resolution within this range is 8 MHz at 1.1 V and the resolution at 1.7 GHz is 5 MHz. The DCRO tuning range is chosen so that the 9^{th} harmonic locking bandwidth is approximately three times the frequency tuning resolution. In Figure 66, the 3^{rd} and 9^{th} harmonic locking bandwidths, as well as the frequency step size, are plotted over the DCRO operating frequency range. The 3^{rd} harmonic locking BW at 1.7 GHz is 86 MHz. It can be noted that the measured output frequencies at 1.1 V are lower than the simulation values and locking BW is lower than the simulation results at 1.1 V due to extra routing parasitics. Furthermore, the frequency step sizes within the tuning range are finer than those from simulations at 1.1 V due to extra parasitic routing capacitance, as the absolute value of

frequency resolution is inversely proportional to the total capacitance at each node.

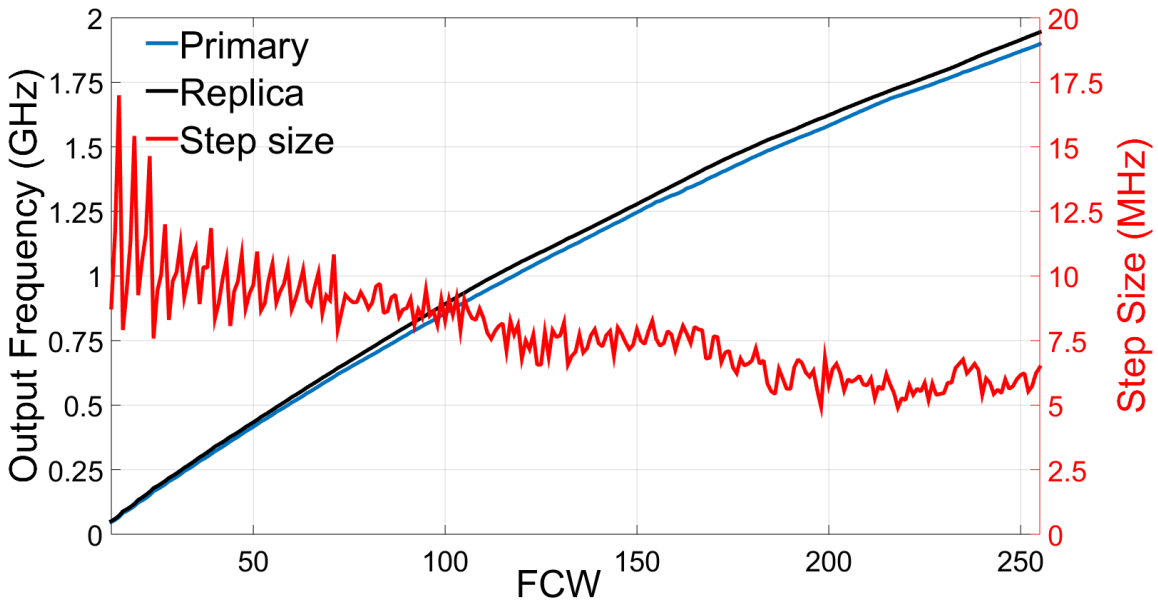


Figure 65: Frequency tuning and step size curves

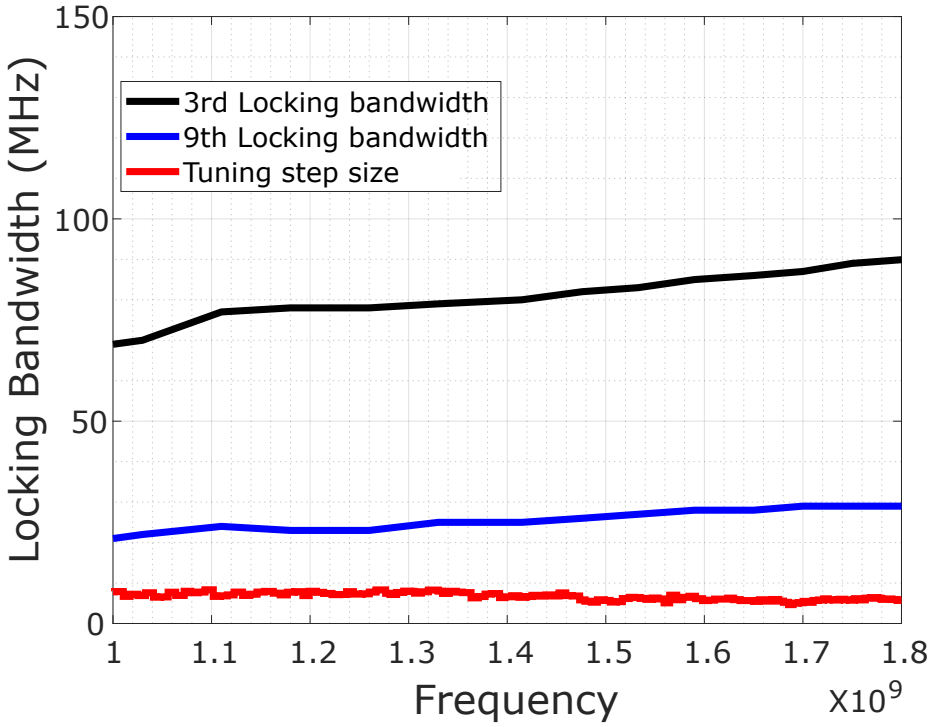


Figure 66: Locking bandwidth

At 1.1 V and 1.7 GHz, the PN performance of the primary DCRO was simulated and measured. The measured PN performance vs the simulated PN for free running and 3^{rd} harmonic injection ILCM (K=3) is shown in Figure 68. A clean square wave reference signal was generated using a Rohde & Schwarz SMA100B signal source, and Rohde & Schwarz FSWP were used for measuring the phase noise and jitter. In addition, the measured vs theory PN is plotted in Figure 67 for K=9 at 1.7 GHz and 1.1 V. The theory PN was obtained from Equation (45) in Chapter 2 at $\kappa = 0.75$. We can see from the figure that the difference between theory and measured PN is less than 4 dB. Furthermore, in Figure 69 and Figure 70, the measured phase noise and jitter are shown for the 3^{rd} and 9^{th} harmonics with 56 fs (f= 566.7 MHz) and 296 fs (f= 188.9 MHz) input references, respectively. The 3^{rd} and 9^{th} harmonics' integrated RMS jitters (1 kHz to 30 MHz) are 197 fs and 381 fs, respectively. The 3^{rd} and 9^{th} harmonics PN at 1 MHz offset are respectively -128 dBc/Hz and -121.6 dBc/Hz compared to -94 dBc/Hz for the free running ILCM. Additionally, the reference spur is -47 dBc at K=3, as can be seen in Figure 71. From Equation (46) in Chapter 2, for the 3^{rd} harmonic injection at 1.7 GHz and a 5 MHz step size, the calculated spur level is -46.8 dBc, which is close to the measured value. The power consumption is 11.77 mW in integer mode. Table 1 compares this work to recent integer designs that also used ring oscillators.

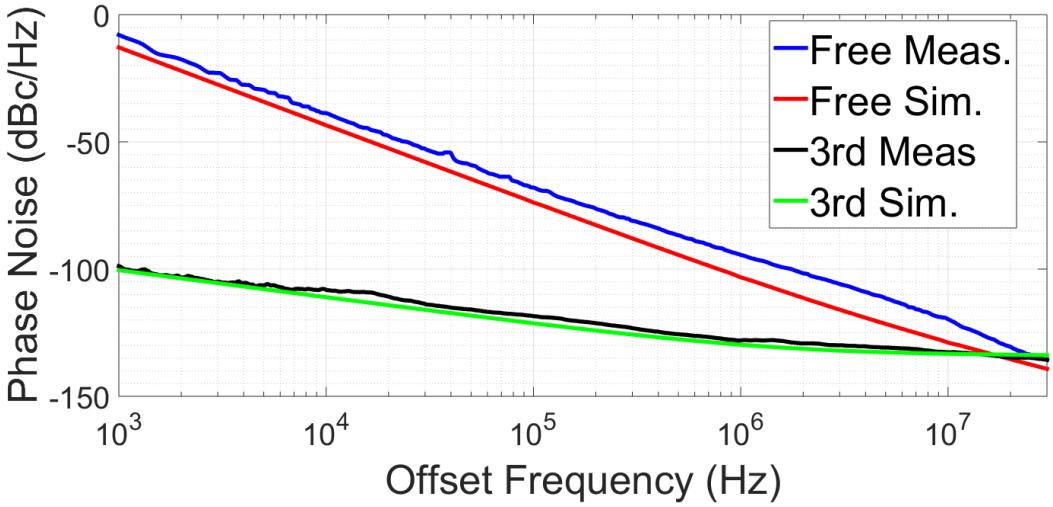


Figure 67: Measured vs simulated PN at 1.7 GHz

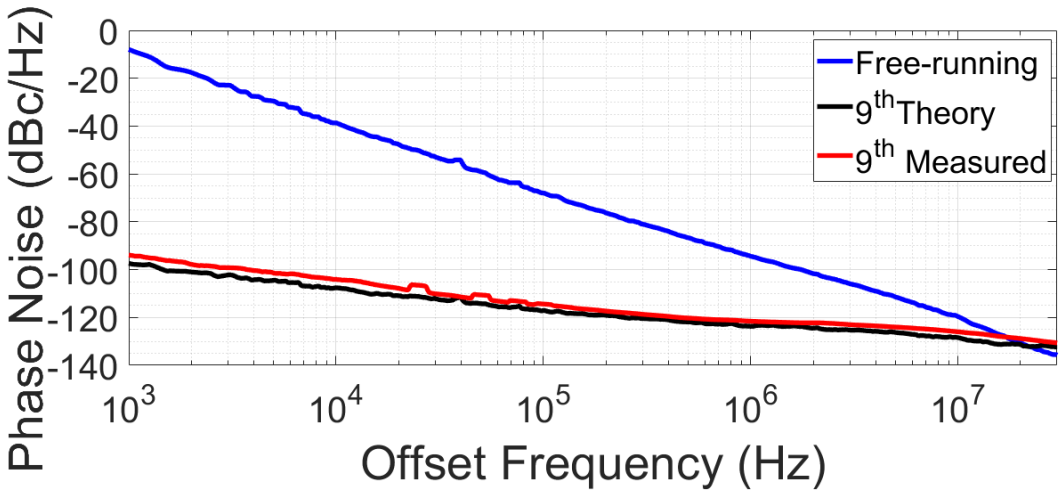


Figure 68: Measured vs theory PN at 1.7 GHz

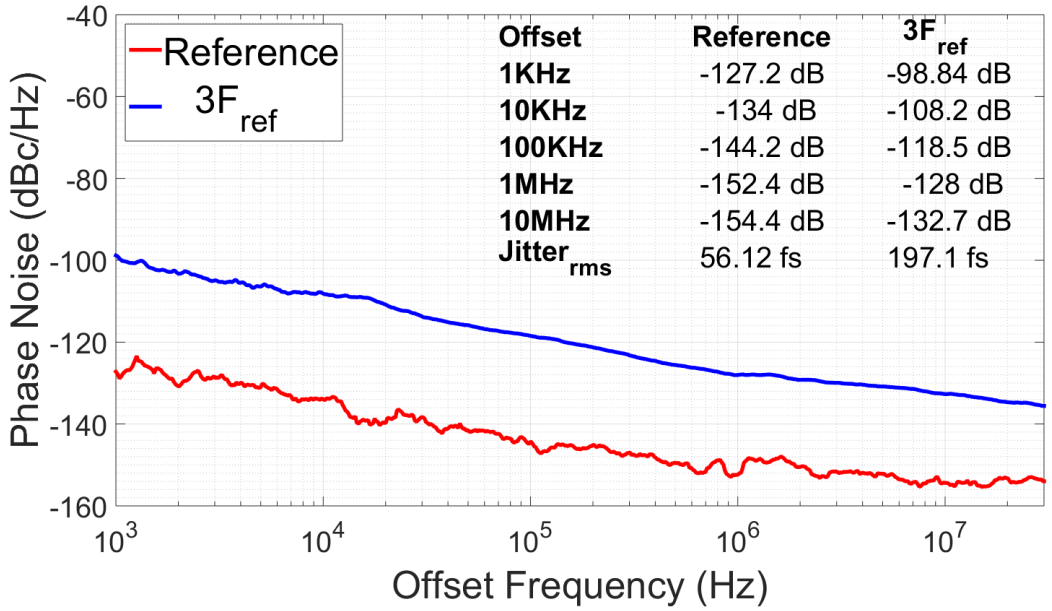


Figure 69: Measured PN for K=3 at 1.7 GHz and 1.1 V

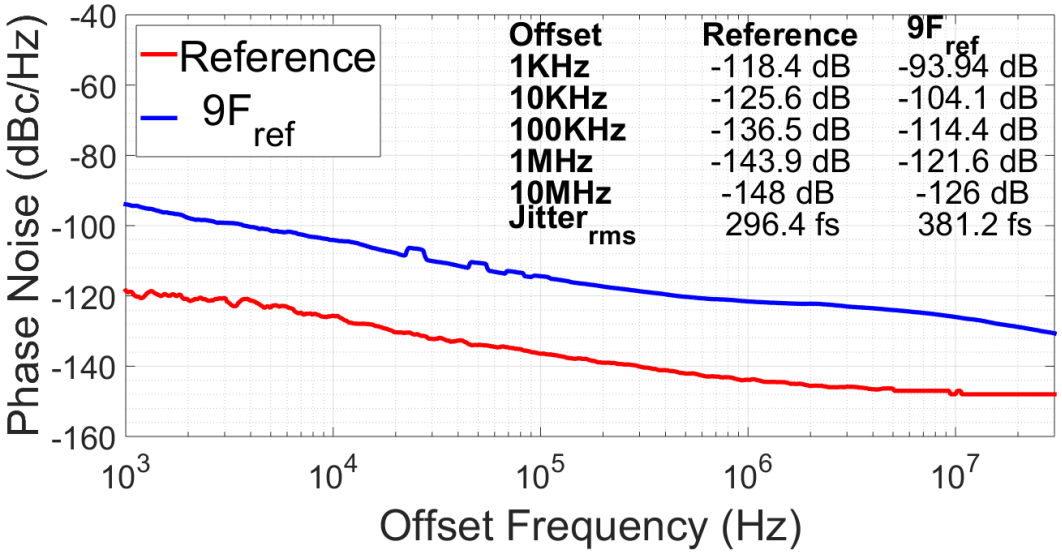


Figure 70: Measured PN for K=9 at 1.7 GHz and 1.1 V

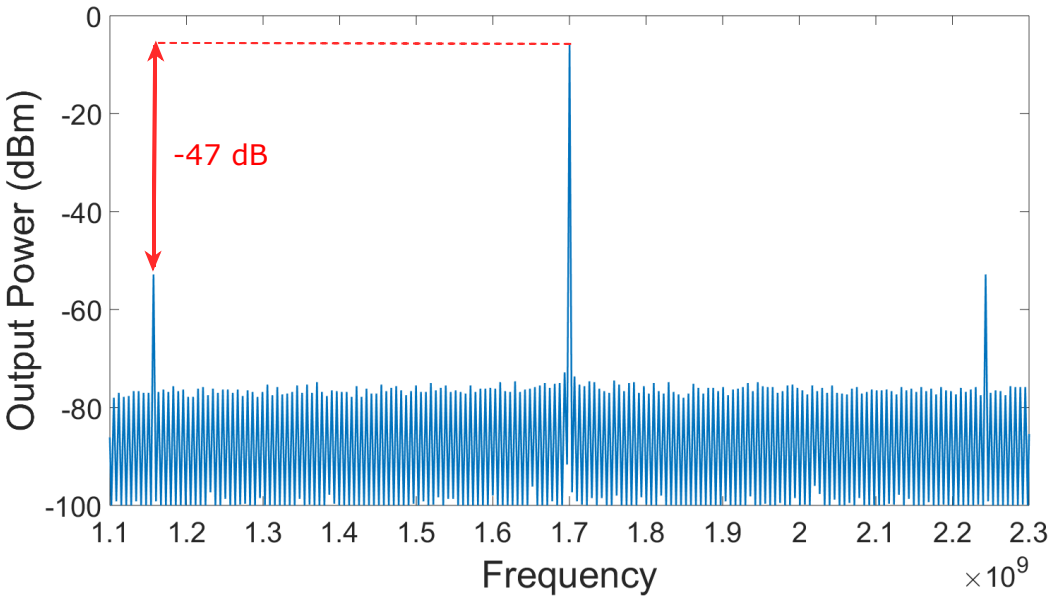


Figure 71: Measured reference spur for K=3 at 1.7 GHz and 1.1 V

Table 1: Comparison with previous integer ILCM works

	JSSC'14 [1]	**JSSC'15 [2]**	**CICC'17 [3]**	**VLSI'16 [4]**	**This work**
Frequency (GHz)	0.5-1.6	0.4-1.4	0.8-1.3	1.44	1-1.8
RMS jitter (fs)	700	1700	513	450	**197**
PN at 1 MHz (dBc/Hz)	-127 @ 1.2 GHz	-118 @ 0.9 GHz	-121 @ 1.1 GHz	-123@ 1.4 GHz	**-128 @ 1.7 GHz**
Locking bandwidth (MHz)	NA	NA	NA	NA	86
Reference Spur (dBc)	-57	-42	-63	-59	-47
Power (mW)	0.97	0.78	13.5	2.8	11.77
Area (mm^2)	0.022	0.0066	0.1225	0.061	0.017
Topology	Differential ILPLL-DCRO	Single-ended ILPLL-DCRO	Differential ILPLL-VCRO	Differential IL-VCRO	Differential IL-DCRO
Technology(nm)	65	65	130	40	65
FOM_a (dB)	-243.2	-236	-234	-242	**-243.4**
$\lvert FOM_a \rvert$/Area (dB/mm^2)	11045	35829	1914	3975	14317
FOM_b (dB)@ 1MHz	-189	-178	-170	-181	-182
Fully Synthesizable?	No	Yes	No	No	Yes

$$FOM_a = 20 \times log(\tau/1s) + 10log(P/1mW)$$

$$FOM_b = \mathcal{L}(\Delta f) - 20 \times log(f_{osc}/\Delta f) + 10 \times log(P/1mW)$$

The measured phase noise and jitter performance of integer mode and fractional mode at K=3, K=3.125, and K=3.0625, are shown in Figure 72. It can be seen that at 1.1 V and 1.7 GHz, the phase noise at 1 MHz offset and RMS jitter from 1 kHz to 30 MHz for the above respective K values are -128, -126, and -125 dBc/Hz and 197, 251, and 253 fs, respectively. Figure 73 shows the RMS integrated jitter from 1 kHz-30 MHz (including spurs if in band) and fractional spurs for fractions (M) from 1/32 up to 16/32, when $N = 3$. The lowest and highest fractional spurs were -55 dBc and -44 dBc, and the minimum and maximum jitter values were 251 fs and 1.4 ps. The frequency spectrum for K = 3.125 can be seen in Figure 74, where the largest and closest fractional spur (68 MHz offset) is at -48 dBc, measured with a different spectrum analyzer resolution bandwidth than the reference spur. The fractional spurs would contribute 517 fs of jitter if found in band according to the following Equation [103]:

$$Jitter_{spur} = \frac{1}{\sqrt{2}\,\pi \times f_{osc}} \times 10^{\frac{Spur(dBc)}{20}}$$

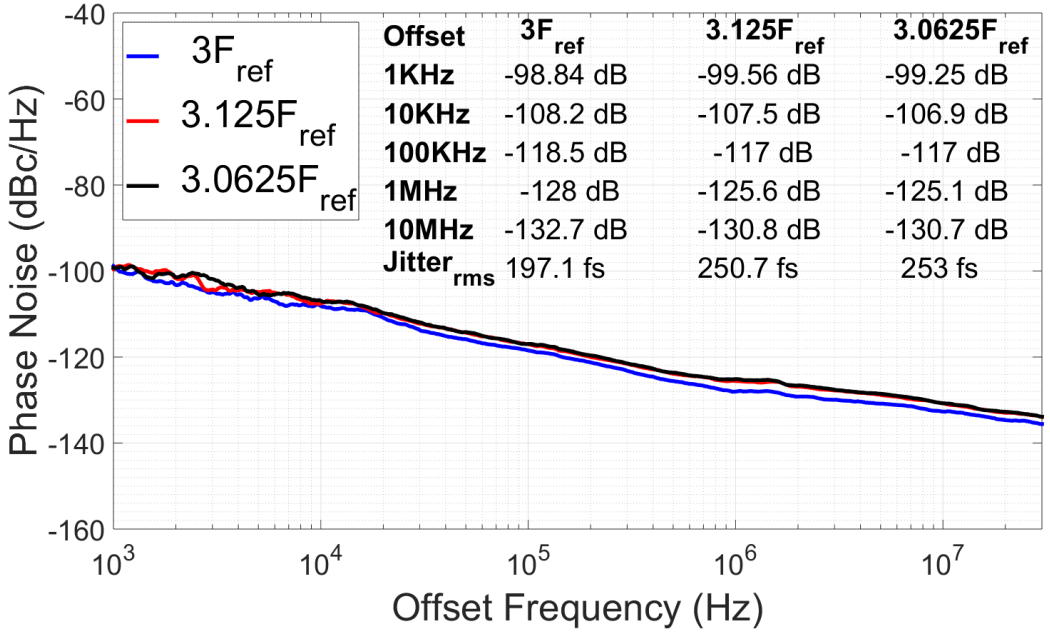


Figure 72: Measured PN for K=3, K=3.125 and K=3.0625 at 1.7 GHz

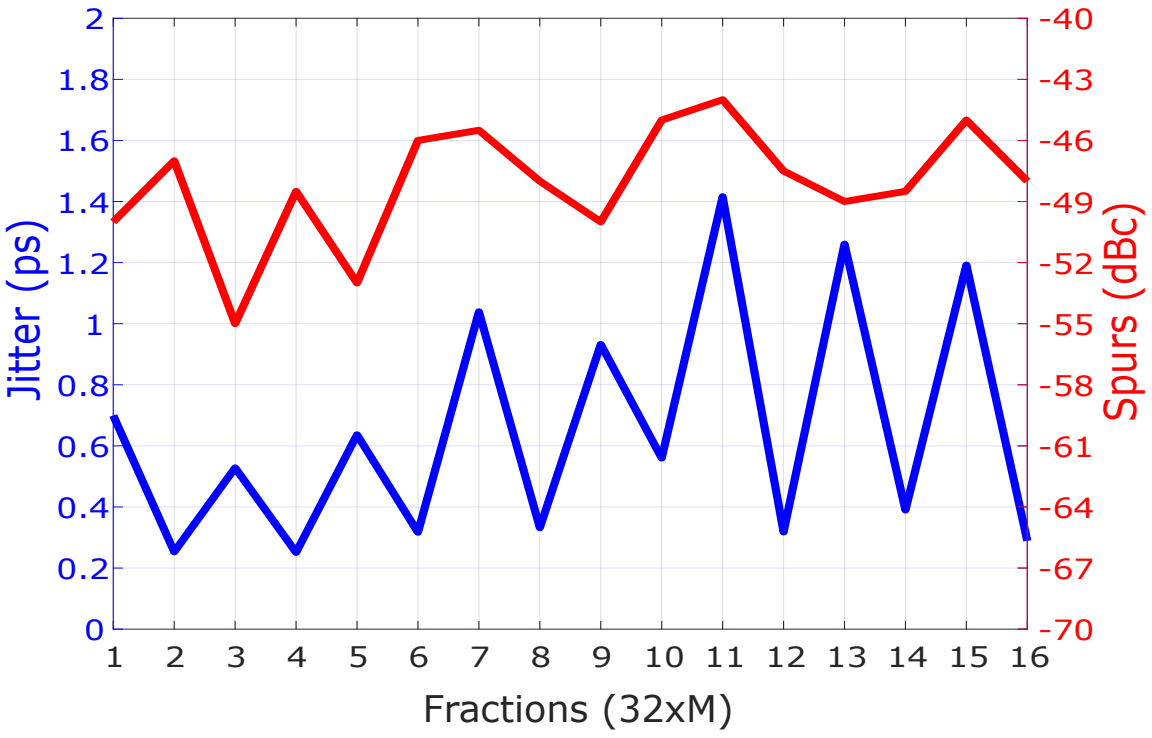


Figure 73: Jitter and fractional spurs for M from 1/32 to 16/32

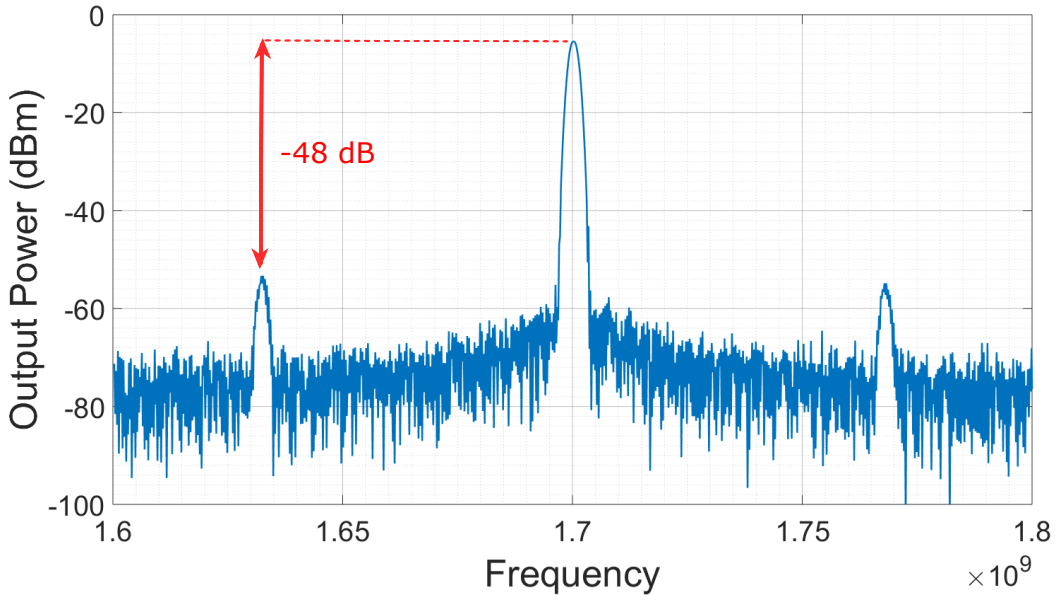


Figure 74: Measured frequency spectrum for K=3.125 at 1.7 GHz and 1.1 V

Table 2: Comparison with previous fractional ILCM works

	ISSCC'12 [5]	**JSSC'16 [6]**	**ISSCC'14 [7]**	**ISSCC'15 [8]**	**This work**
Frequency (GHz)	1.2-2	0.58	1.6-1.9	0.8-1.7	1-1.8
RMS jitter (ps)	0.461/NA	2.42*/8.05*	1.15*/1.4*	3.6*/NA	**0.251/1.4***
(min/max)	1k-30MHz	100- 40MHz	30k-30MHz	1k-100MHz	**1k-30MHz**
PN at 1 MHz (dBc/Hz)	-122.9 @ 1.6 GHz	-113 @ 0.58 GHz	-115 @ 1.6 GHz	-114 @ 1.5 GHz	**-126 @ 1.7 GHz**
Fractional Spur (dBc)	-43	NA	-47	NA	**-48**
Reference Spur (dBc)	NA	NA	-47	NA	-47
Frac. Resolution	$f_{ref}/10$	$f_{ref}/32$	$f_{ref}/2^{18}$	f_{ref} /172	f_{ref} /32
Power (mW)	3.6	10.5	3	3	13.25
Area(mm^2)	0.032	0.158	0.4	0.048	**0.021**
Topology	Single-ended IL-DLL	Differential IL-PLL	Differential MDLL	Single-ended Soft IL-PLL	Differential ILCM
Technology	65 nm	65 nm	65 nm	65 nm	65 nm
$FOM_a(dB)$	-241	-222	-234	-224	**-241**
$FOM_b(dB)@1MHz$	-181	-158	-174	-173	-179
Fully Synthesizable?	No	No	No	Yes	Yes

*Jitter including fractional spurs in band

The ILCM fractional mode performance is listed in Table 2 and compared to prior fractional injection designs. This work shows good performance in terms of jitter, phase noise, area, FOM_a and FOM_b.

The power consumption in the fractional mode at 1.7 GHz and 1.1 V is 13.25 mW. Figure 75 shows the power breakdown of the ILCM. DCRO1 consumes 72% of the total power. The calibration added power depends on whether online or offline calibration is chosen. For offline calibration, only the power consumption of counter1 will be added at some small duty cycle (e.g. once every 20 ms), which is 0.001 mW. For online calibration, DCRO2 and counter2 power will be added. Assuming a 20 ms phase III calibration period and 200 μs phase II calibration period, the added power will be 0.09mW.

The proposed differential ILCM phase noise performance was tested in the presence of digital switching noise and compared to a single ended ILCM that was implemented on the same substrate. The switching noise was generated using 6,000 flip flops randomly

toggling at 500 MHz placed approximately two times closer to the differential ILCM as shown in Figure 76. Additionally, the noise source shares the same ground and supply with the differential ILCM, while the single ended ILCM has a separate supply and ground. As shown in Figure 77, the differential ILCM is less sensitive to switching noise compared to the single ended ILCM and provides up to 7 dB improvement in phase noise even with higher supply and substrate noise coupling. This result shows the importance of the use of a differential structure.

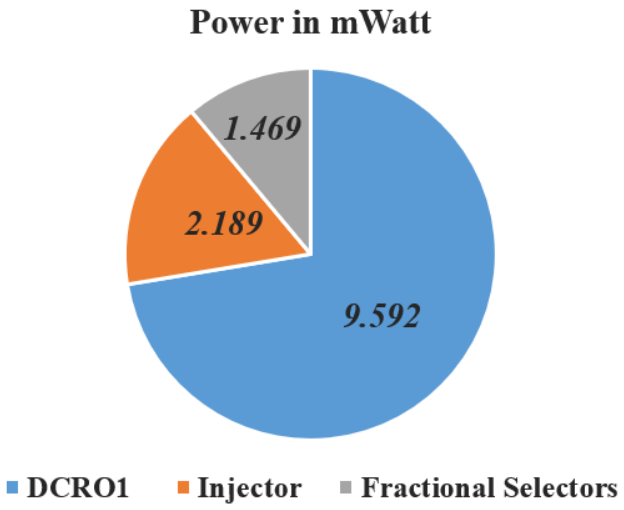


Figure 75: Power breakdown

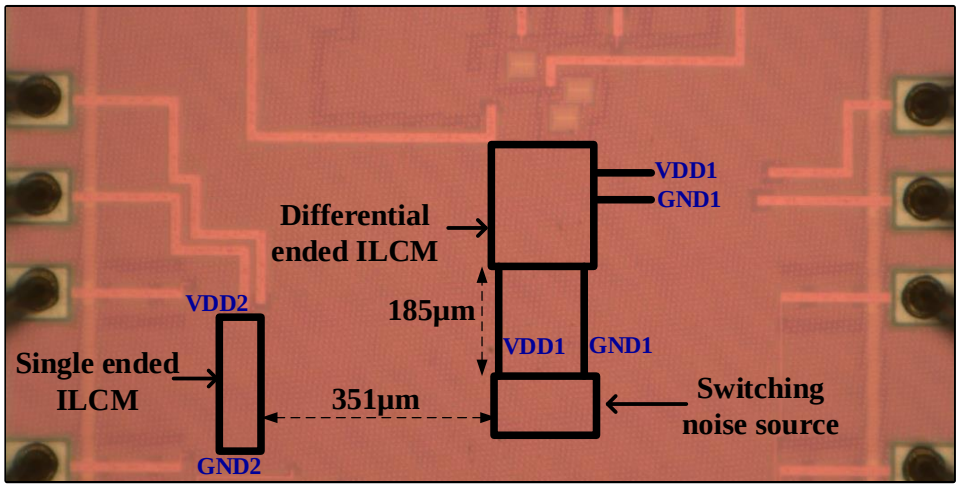


Figure 76: Differential and single ended ILCM micrograph

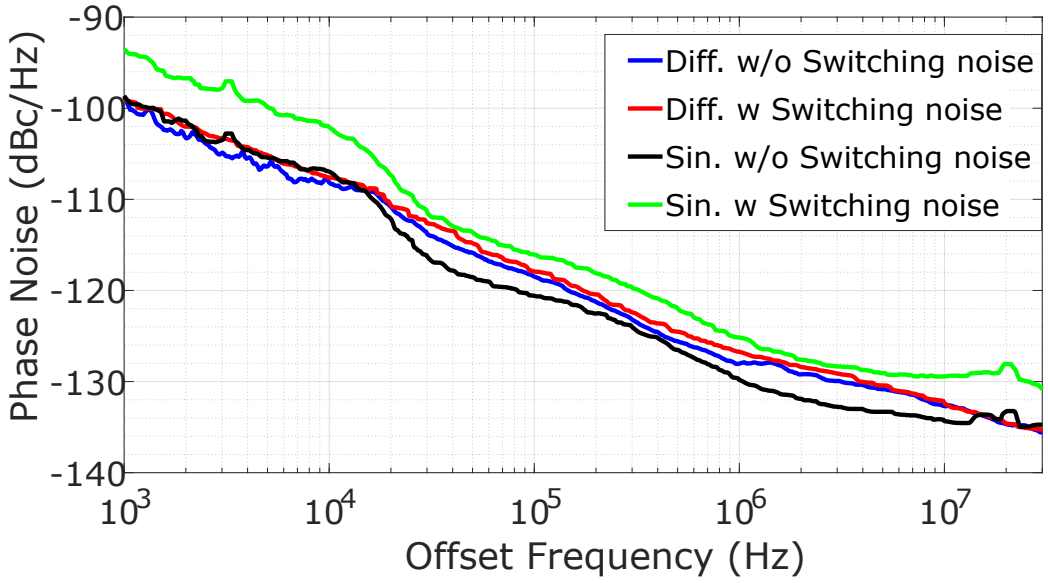


Figure 77: Measured differential vs single ended ILCM PN performance in the presence of switching noise for K=3 at 1.7 GHz and 1.1 V

The online PVT technique was applied following the coming steps. First, in the initial phase different FCWs of DCRO1 and DCRO2 are loaded from the pattern generator to the chip, then using the on-chip counters the tuning curves of DCRO1 and DCRO2 are read from the chip and stored in matlab. Second, in the calibration phase only the DCRO2 FCWs are loaded to the chip and counter 2 frequency values are read and stored in matlab. Third, estimated DCRO1 tuning curve is estimated from the data previously stored in matlab using the algorithm mentioned in Chapter 4. Fourth, a new FCW1 that generates the closet frequency value to Kf_{ref} is selected and loaded through the pattern generator.

The ILCM performance was tested over different temperatures (from 30 to 70°C) and supply voltages (from 0.9 to 1.1 V). Figure 78 displays the jitter variation as a function of temperature, showing that the maximum jitter variation percentage is 13.7% at the highest temperature and voltage (70°C and 1.1 V). It can also be seen that the phase noise at 1 MHz offset changes less than 0.7 dB over different voltages and temperatures. These results show that the proposed on-line calibration scheme helps maintaining the

ILCM performance efficiently over PVT variations. In addition, integrated RMS jitter (1 kHz to 30 MHz), phase noise (1 MHz offset) and power consumption over the tuning range are shown in Figure 79 for K=3 at 1.1 V and room temperature. As shown in this figure, there is less than 4.7 dB change in phase noise and less than 66 fs change in jitter over a 800 MHz frequency range.

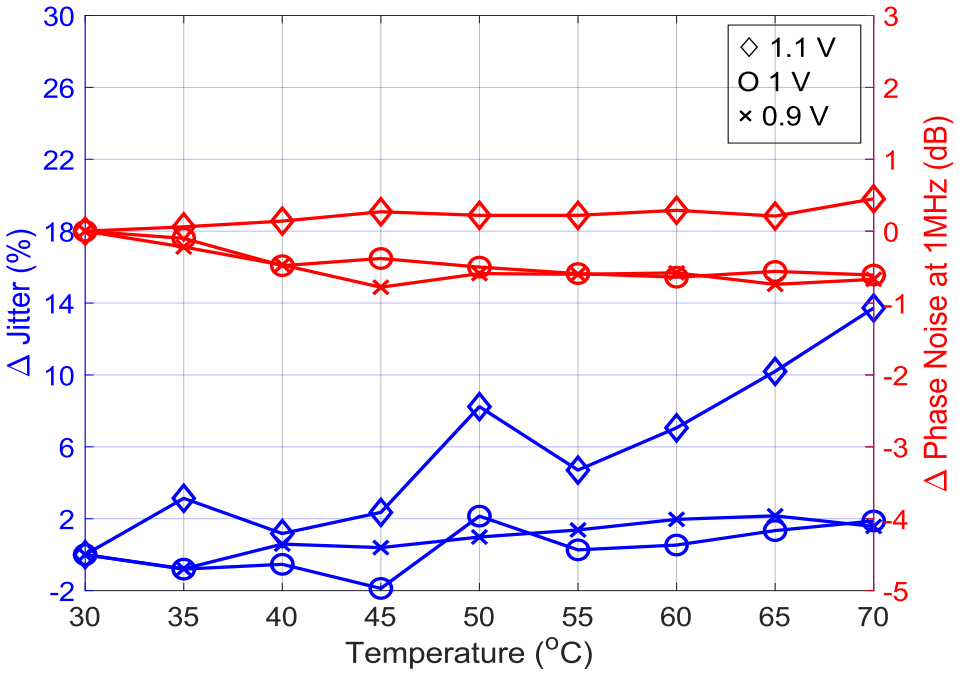


Figure 78: Jitter and PN for K=3 vs Temperature

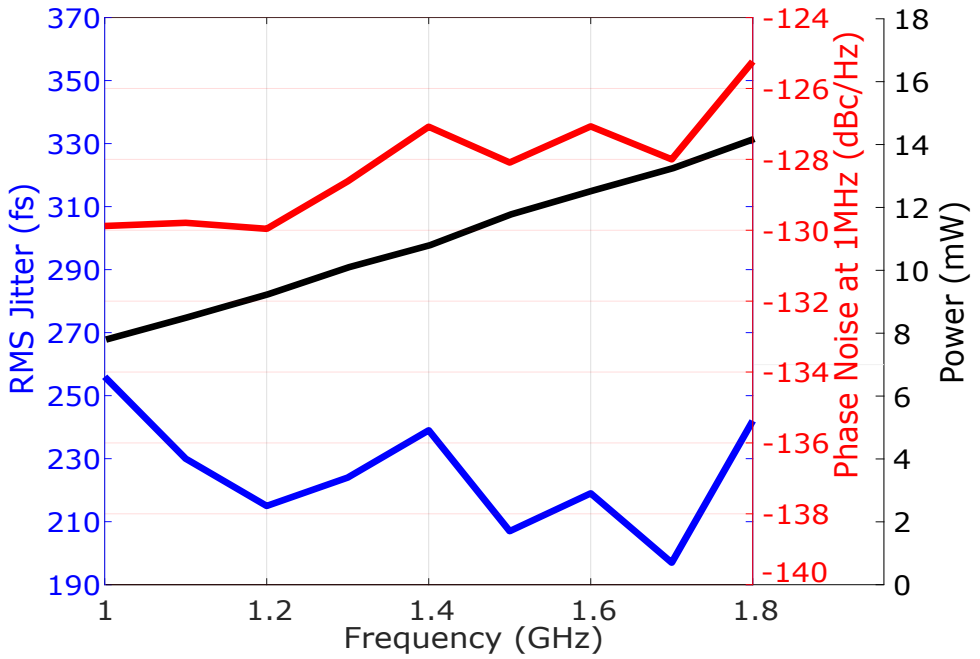


Figure 79: Jitter, phase noise and power vs frequency for K=3 at 1.1 V and room temperature

Figure 80 shows the maximum absolute frequency error between interpolated free running values of DCRO1 $f_{hi1,intp}$ and its free running frequency values, across all frequencies, using the online calibration algorithm as discussed in Chapter 4. The initial calibration was done at 1 V and 30 $°C$ then the voltage was swept by 10% and the temperature was increased to 50 $°C$ and 70 $°C$ (due to temperature chamber limitations the temperature couldn't be decreased below 30$°C$). The worst-case error across all frequencies was 4.3 MHz (0.25%), which is less than the smallest step size (5 MHz). This indicates that the calibration technique used in this work is capable of estimating DCRO1 free running frequency effectively under VT variations. In Figure 81, the measured FCW1 and FCW2 are shown in online calibration phase (phase II) at 1.7 GHz, 1.1 V and different temperatures. DCRO2 is free running at that phase and its FCW2 at 1.7 GHz increases as temperature increases. FCW1 is chosen by selecting the closest $f_{hi1,intp}$ to 1.7 GHz at each temperature. Furthermore, the error between $f_{hi1,intp}$ and the operating frequency

(ε) is 0.27 MHz, 0.32 MHz and -1.2 MHz at 30 $^{\circ}C$, 50 $^{\circ}C$ and 70 $^{\circ}C$, respectively, as can be seen in Figure 81.

On the whole, this work compares well to other designs in terms of jitter, phase noise, area, and FOMs as shown in Table 1 and Table 2, especially considering the use of generic standard cells and $P\&R$ for the entire design. Furthermore, this is one of the smallest areas reported in integer/fractional ILCMs. It is worth mentioning that the matrix structure reduces WID variations at the expense of power consumption. In addition, the use of differential structure to reduce noise coupling added extra power and area to the ILCM.

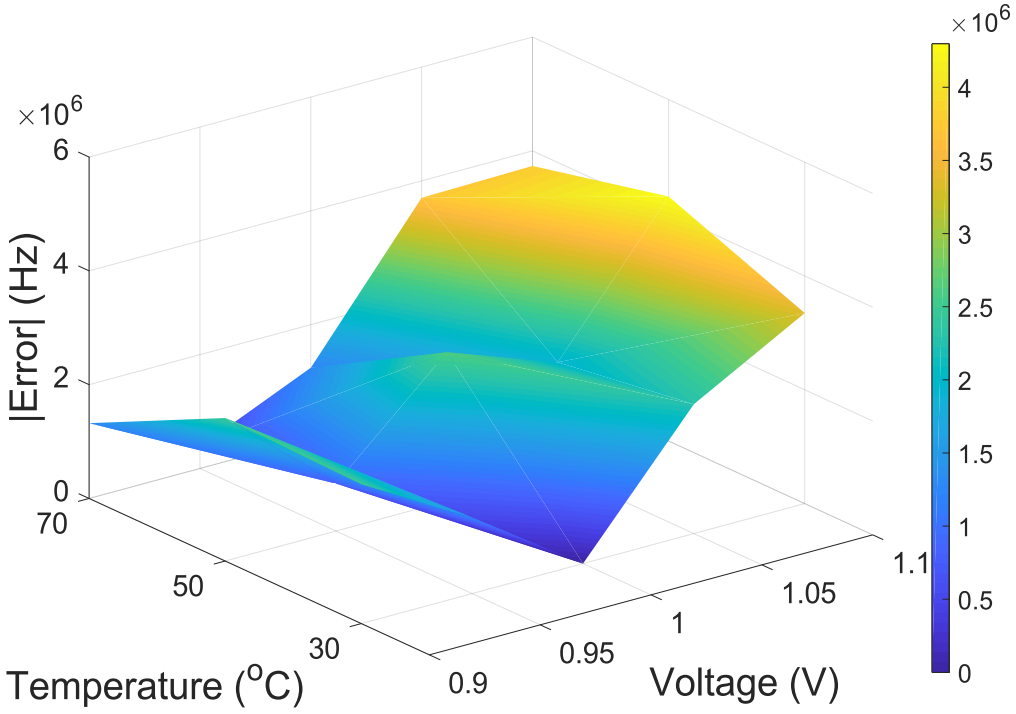


Figure 80: Maximum absolute frequency error between estimated and free running DCRO1 frequencies

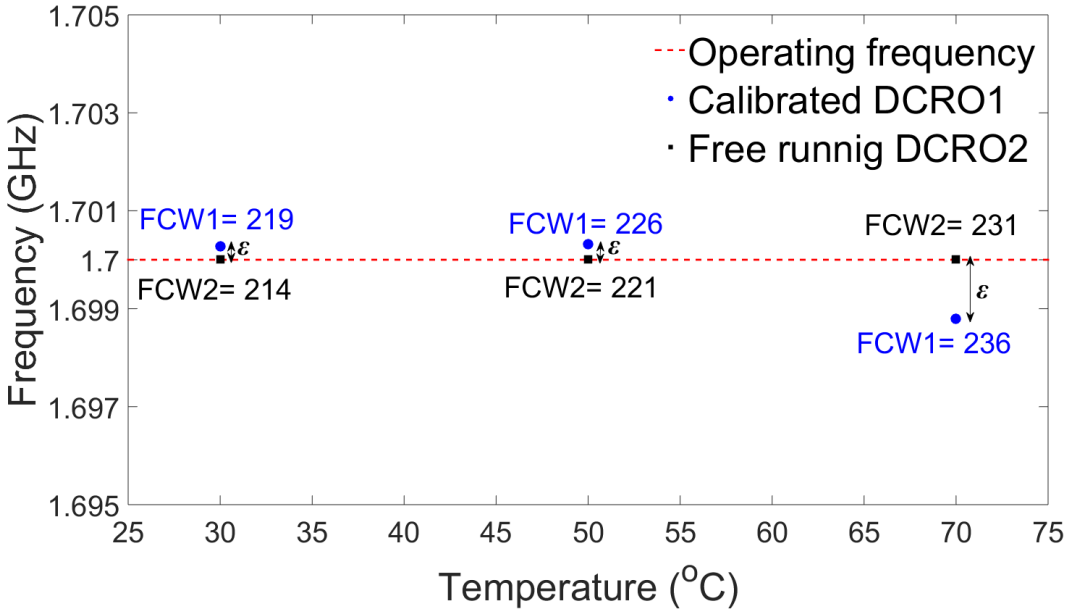


Figure 81: Online calibration at 1.1 V and 1.7 GHz operating frequency

5.3 Conclusion

This chapter described the digital design flow used to implement the proposed design. The design was first simulated and critical design parameters such as realignment factor, tuning curves, PN performance, locking BW and frequency step size were obtained. Afterwards, the fabricated design parameters were tested. Moreover, the ILCM performance was tested when varying the voltage supply by 10% and temperature from 30°C to 70°C, showing a maximum of 50 fs jitter variation. In addition, the maximum error between the free running and the interpolated frequency values, obtained from calibration phase II, was less than the frequency step size showing that the calibration technique used provides accurate results. The measurement results for integer and fractional operations were compared to recent works. The proposed ILCM, fully synthesizable, shows superior performance in terms of jitter and jitter-power FOM when compared to other custom designs. In the next chapter, a conclusion of this research will be provided and future work will be detailed.

6

Conclusion and Future Work

6.1 Conclusion

This thesis has focused on designing a high performance CM that meets modern CMOS technology demands. These demands include designing a CM whose locking bandwidth can go up to tens of MHz and employing a PVT calibrator and noise rejection techniques. Furthermore, with the continuous trend of smaller devices and lower voltage supply scaling, traditional analog designs have become increasingly difficult to design and port to new technologies. Thus, building an all digital CM that can be scaled down with finer geometry CMOS processes is becoming increasingly important. Therefore, the proposed design offered solutions to these design challenges using digital circuits .

All mentioned research objectives indicated in Chapter 1 have been achieved. To further illustrate how this was addressed in this work, each objective and its corresponding design

achievement will be detailed as follows:

The first design objective was to design a compact fully synthesizable RO that can be digitally tuned with an accurate frequency step size. This was achieved by implementing an all digital DCRO that is composed of a matrix structure. The DCRO was digitally tuned using FCW that enables one delay cell at a time to accomplish an accurate frequency step size. Furthermore, it achieved a high level of design integration and small die area, only 0.021 mm^2, by utilizing digital cells that come from vendor supplied standard cell libraries. Moreover, it was implemented using digital design flow with the aid of standard CAD tools for synthesis and automatic $P\&R$.

The second design objective was to reduce RO jitter by using a pulse injection locking technique. It was used in the proposed design as a pulse signal window is applied for injecting the differential reference signals to the DCRO differential outputs every K cycles, where K ranged from 1 to 9. This technique realigned the DCRO outputs and reduced jitter and PN significantly within the locking bandwidth of the ILCM, which was reported as 86 MHz and 30 MHz when measured at 1.7 GHz and 1.1 V for $K = 3$ and $K = 9$, respectively. The realignment factor was set to 0.75 with the goal of achieving low jitter. Measurement results showed a 34 dB reduction in the PN level of the free-running DCRO at 1 MHz, when injected locked to the 3^{rd} harmonic of the reference at 1.7 GHz. In addition, the jitter was further reduced by the use of the parallel delay cells. This is because random mismatch between single row DCRO elements cause variations in the DRCO period. This possibly leads to inaccuracy in f_{osc}. The parallel DCRO structure helped decrease period variations resulting from WID variations by more than a factor of 27 compared to a single row DCRO leading to lower jitter and reference spur level.

The third design objective was to achieve fractional frequency resolution with low complexity circuits and reduced power overhead. A novel sequential fractional injection method was used to obtain fractional resolution as fine as $f_{ref}/32$. This fine resolution was attained without having to increase the number of RO stages, as in previous

traditional sequential injection designs that can increase power consumption at a given operating frequency. The fractional rotational technique was implemented utilizing low complexity digital circuits that included an array of shift registers, decoder and edge selection logic. These circuits only increase the total power of the ILCM by 11%. Jitter of fractions from $f_{ref}/32$ to $f_{ref}/16$ were measured at 1.7 GHz and 1.1 V. The maximum and minimum integrated RMS jitter were found to be 251 fs and 1.4 ps, respectively.

The fourth design objective was to implement an FLL based PVT calibration technique to make the ILCM robust to PVT variations. A novel replica based FLL PVT calibration technique was realized to estimate the free-running frequency of the DCRO while it is under injection. This is the first time a calibration technique has been used to calibrate for the differences between the main and replica oscillators at different VT conditions after initial calibration. The PVT calibration task in ILCMs is to minimize the difference between f_{osc} and Kf_{ref} to ensure locking condition, achieve reduced jitter and lower the reference spur level. The calibration technique performance was measured and assessed over voltage variations from 0.9 V to 1.1 V and temperature variations from 30 $^{\circ}C$ to 70 $^{\circ}C$. The maximum absolute calibration error between the estimated and actual free-running DCRO frequencies was 4.3 MHz, which is less than the DCRO frequency step size, showing that the estimated FCW1 led to the the minimum frequency error. Moreover, under the same VT conditions, the maximum measured integrated RMS jitter variation was 50 fs at 70$^{\circ}C$ and 1.1 V and the measured PN value changed by a maximum of 0.7 dB over the entire range of voltages and temperatures.

The fifth design objective was to implement design techniques to reduce ILCM sensitivity to on-chip noise coupling. This was accomplished with the aid of decoupling capacitors, as well as the use of pseudo differential logic in the delay cells. It should be highlighted that, to our knowledge, this is the first fully synthesizable differential DCRO. To evaluate the PN performance of the ILCM under switching noise, a switching noise source, that shared the same supply voltage with the ILCM, was placed on the same chip 185 μm

apart from it. When the measured PN of the proposed pseudo differential ILCM was compared to a single-ended version of it, it showed superior PN performance with up to 7 dB improvement.

6.2 Future Work

This thesis presented a compact highly integrated low jitter clock multiplier that can be improved in various ways. Design metrics like frequency resolution, locking bandwidth, jitter, reference spur and power consumption can be further enhanced.

First, the frequency resolution of the proposed DCRO limited the ILCM performance in several ways. In ILCMs, the tuning range is chosen based on the step size and largest K factor, since the step size was more than 8 MHz for frequencies lower than 1 GHz, the operating tuning range was only 800 MHz to be able to lock to the 9^{th} harmonic. Furthermore, for a given tuning range, the step size limits the K factor because the locking bandwidth at high harmonics is relatively narrow. Moreover, it negatively affected the reference spur and jitter, even in the presence of PVT calibration, as the difference between f_{osc} and Kf_{ref} could be as large as the step size. More than one technique can be used to achieve a finer frequency resolution including the use of fine and coarse tuning banks, where capacitors can be used for fine tuning [33] or a Delta-Sigma modulator ($\Delta\Sigma$) IDAC [40].

Second, the DCRO locking bandwidth of only $f_{ref}/6$ restricted the maximum K factor that can be used in the ILCM. Additionally, at a given K factor, the PN suppression bandwidth is limited at high harmonics causing increased jitter. Frequency doublers with a PVT calibrator can be used to double the reference frequency and increase the ILCM locking bandwidth to approximately $f_{ref}/3$, hence, K can be increased [18]. Another solution is to use a multiple pulse injection technique, where more than one RO stage can be injected at the same time. This helps widening the locking bandwidth by a factor of N_{osc} [76]. Finally, an MDLL with locking bandwidth of $f_{ref}/4$ can be implemented

[3].

Third, to further enhance the jitter, various techniques can be realized. Variable pulse width controller can be added to the ILCM [29] and injection strength controller can be used to adjust the realignment factor [44]. Furthermore, dual injection technique with a duty cycle corrector can be used to inject the DCRO output at both the positive and negative edges of the reference as suggested in [16]. Moreover, effects like DCRO output slope modulation due to periodic injection can be calibrated to achieve low jitter and reference spur level [14].

Fourth, to further suppress noise coupling effects, an on-chip LDO regulator can be used to supply the DCRO with a more stable supply voltage (if a separate supply voltage can not be provided to it). In addition, layout techniques like guard rings and shielding can be implemented.

Fifth, the power consumption of the proposed DCRO can possibly limit its applications. Consequently, an alternative low power tuning method can be explored as switched capacitors or IDAC tuning. Additionally, a low power calibration technique can be investigated by using a replica delay cell instead of the replica DCRO [95].

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Appendix

Sample verilog codes

Delay cell circuit

```
/*********************************************
/* diff_one_cell_inj_V4.sv
*********************************************/

/**
* Module: diff_one_cell_inj_V4
*
*/
module diff_one_cell_inj_V4(inp, inn, clkp, clkn,
 sel, pulse, en, outp, outn);

input inp, inn, clkp, clkn, sel, pulse, en;
inout outp, outn;
wire  selANDen, enb, outn2, outp2, outn3, outp3;
```

```
INVTD4 g1 ( .A3(inp), .ZN(outn2), .A2(en), .A1(enb) );
INVTD4 g2 ( .A3(inn), .ZN(outp2), .A2(en), .A1(enb) );
INVTD1 g3 ( .A3(outn), .ZN(outp3), .A2(en), .A1(enb) );
INVTD1 g4 ( .A3(outp), .ZN(outn3), .A2(en), .A1(enb) );
INVD0 g5 ( .I(en), .ZN(enb) );
CKAN2D2 g6 ( .A1(sel), .A2(pulse), .Z(selANDen) );
BUFTD2 g7 ( .I(clkp), .Z(outn), .OE(selANDen) );
BUFTD2 g8 ( .I(clkn), .Z(outp), .OE(selANDen) );

endmodule
```

Clock tree circuit

```
/*********************************************
* inv16x8_clk.sv
*********************************************/

module inv16x8_clk ( clkinput, clkbinput, clk, clkb );
input clkinput, clkbinput;
output [7:0] clk;
output [7:0] clkb;
wire   [1:0] clkint;
wire   [1:0] clkbint;

CKND16 g1 ( .I(clkinput), .ZN(clkint[0]) );
CKND16 g2 ( .I(clkinput), .ZN(clkint[1]) );
CKND16 g3 ( .I(clkbinput), .ZN(clkbint[0]) );
```

```
CKND16 g4 ( .I(clkbinput), .ZN(clkbint[1]) );
CKND16 g5 ( .I(clkint[0]), .ZN(clk[0]) );
CKND16 g6 ( .I(clkint[0]), .ZN(clk[1]) );
CKND16 g7 ( .I(clkint[0]), .ZN(clk[2]) );
CKND16 g8 ( .I(clkint[0]), .ZN(clk[3]) );
CKND16 g9 ( .I(clkint[1]), .ZN(clk[4]) );
CKND16 g10 ( .I(clkint[1]), .ZN(clk[5]) );
CKND16 g11 ( .I(clkint[1]), .ZN(clk[6]) );
CKND16 g12 ( .I(clkint[1]), .ZN(clk[7]) );
CKND16 g13 ( .I(clkbint[0]), .ZN(clkb[0]) );
CKND16 g14 ( .I(clkbint[0]), .ZN(clkb[1]) );
CKND16 g15 ( .I(clkbint[0]), .ZN(clkb[2]) );
CKND16 g16 ( .I(clkbint[0]), .ZN(clkb[3]) );
CKND16 g17 ( .I(clkbint[1]), .ZN(clkb[4]) );
CKND16 g18 ( .I(clkbint[1]), .ZN(clkb[5]) );
CKND16 g19 ( .I(clkbint[1]), .ZN(clkb[6]) );
CKND16 g20 ( .I(clkbint[1]), .ZN(clkb[7]) );
CKND4 g21 ( .I(clkint[0]), .ZN(clkbint[0]) );
CKND4 g22 ( .I(clkbint[0]), .ZN(clkint[0]) );
CKND4 g23 ( .I(clkint[1]), .ZN(clkbint[1]) );
CKND4 g24 ( .I(clkbint[1]), .ZN(clkint[1]) );
CKND4 g25 ( .I(clk[0]), .ZN(clkb[0]) );
CKND4 g26 ( .I(clkb[0]), .ZN(clk[0]) );
CKND4 g27 ( .I(clk[1]), .ZN(clkb[1]) );
CKND4 g28 ( .I(clkb[1]), .ZN(clk[1]) );
CKND4 g29 ( .I(clk[2]), .ZN(clkb[2]) );
CKND4 g30 ( .I(clkb[2]), .ZN(clk[2]) );
CKND4 g31 ( .I(clk[3]), .ZN(clkb[3]) );
```

```
CKND4 g32 ( .I(clkb[3]), .ZN(clk[3]) );
CKND4 g33 ( .I(clk[4]), .ZN(clkb[4]) );
CKND4 g34 ( .I(clkb[4]), .ZN(clk[4]) );
CKND4 g35 ( .I(clk[5]), .ZN(clkb[5]) );
CKND4 g36 ( .I(clkb[5]), .ZN(clk[5]) );
CKND4 g37 ( .I(clk[6]), .ZN(clkb[6]) );
CKND4 g38 ( .I(clkb[6]), .ZN(clk[6]) );
CKND4 g39 ( .I(clk[7]), .ZN(clkb[7]) );
CKND4 g40 ( .I(clkb[7]), .ZN(clk[7]) );

endmodule
```