

CCD TRANSVERSAL FILTERS

by

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A thesis submitted to the School of Graduate Studies in
partial fulfillment of the requirements for the degree of
Master of Applied Science

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University of Ottawa
Ottawa, Canada
April 1975

ABSTRACT

The design and implementation of transversal filters using charge coupled devices is described. Results are presented for frequency selective filter designs using two different CCD implementations. The first method discussed is a flexible technique using the voltage sensing CCD and an external weighting and summing network. The second method discussed is a fixed coefficient technique using the split electrode CCD which performs the weighting and summing operations on chip. An analysis is presented to calculate the effective filter coefficient values based on the positions of the electrode gaps and on the capacitive loading associated with the rest of the electrode structure.

ACKNOWLEDGEMENTS

The author wishes to thank Dr. W. Steenaart for his supervision and helpful advice throughout this project.

The author is also deeply indebted to the Silicon Devices Group at Bell Northern Research for their support of this work by supplying the devices and facilities necessary to perform the experimental portions of the research. Special thanks are extended to Dr. Ali Ibrahim and Mr. Lester Sellars for their interest and assistance in this project.

The financial support of the National Research Council of Canada in the form of a 1967 Science Scholarship is gratefully acknowledged.

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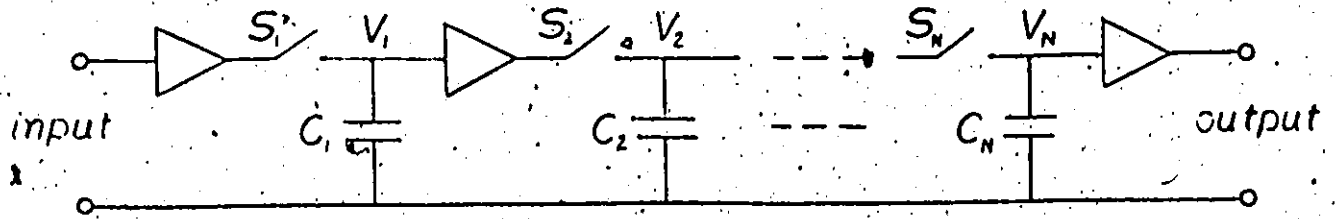
INTRODUCTION

The charge coupled device (CCD) is a silicon integrated circuit capable of providing storage and delay of sampled analog signals. The basic CCD consists of a linear array of closely spaced MOS capacitors on a common substrate. The signal samples are stored as mobile charge carriers and moved along the silicon surface by pulsing the capacitor electrodes with appropriate clock waveforms.

The concept of storing signal samples and clocking them along an array of capacitors is not new. It was proposed in 1952 by Janssen[1] as an alternative to LC delay lines in low frequency applications. Figure 1.1a shows the circuit in which the inductor of an LC delay line section has been replaced by a switch and a unity gain buffer amplifier. The signal samples V_1 to V_N are stored as voltages on the array of storage capacitors C_1 to C_N .

The operation of this circuit is shown in figure 1.1b. The odd numbered switches are closed momentarily at intervals T seconds apart, sampling the input and transferring the samples to the odd numbered capacitors. Between these events, also at T second intervals, the even numbered switches are closed momentarily to transfer the samples to the even numbered capacitors. This cycle is repeated and the signal is propagated down the delay line.

a. DELAY CIRCUIT



b. CIRCUIT OPERATION

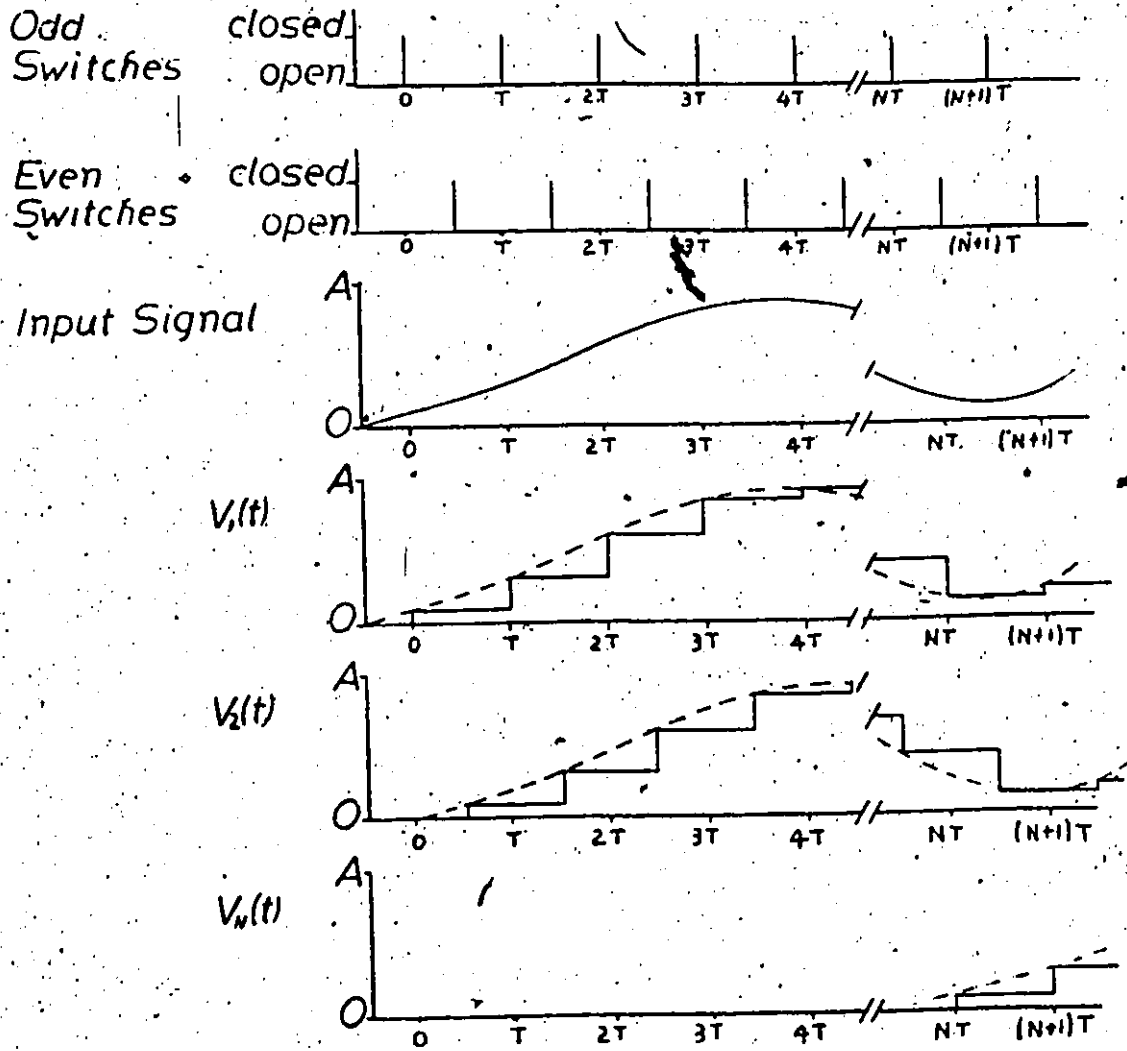
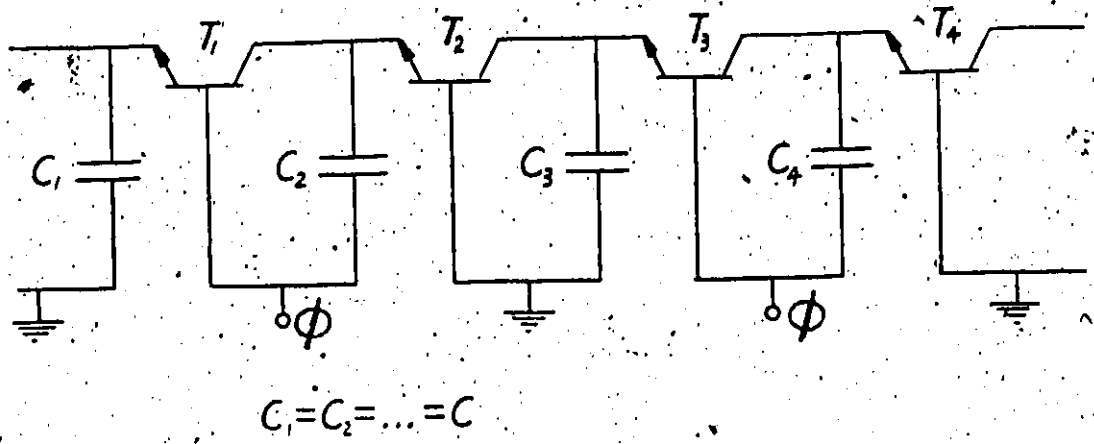


Figure 1.1 Janssen's Discontinuous Low Frequency Delay Line With Continuously Variable Delay[1]

The two-phase mode of operation as described above is required since only one-half of storage capacitors carry signal information at any given time. The other half of the array remains in a state ready to receive information during the next transfer operation. This sequence of operations parallels that of a two-phase CCD, except that the latter has no switches or buffer amplifiers between the storage capacitors.

The discontinuous delay line did not receive too much attention since it could not be implemented in a practical manner. With the technology available at that time the switches and amplifiers would have been more bulky and troublesome than the inductors which they were to replace. It was not until 1968 that an acceptable method of implementation was found when Sangster and Teer[2] built their integrated bucket brigade device (IBBD). Their circuit using bipolar technology is shown in figure 1.2a. It was almost a direct solid state implementation of the discontinuous delay line circuit with the switch and buffer amplifier of each stage realized by a single transistor. It also used two-phase clocking in its operation. The clocking waveform ϕ with negative and positive excursions is equivalent to two non-overlapping phases applied alternately to the device stages. The signal in this case was represented as a charge deficit as illustrated in figure 1.3. The integrated form of the bipolar bucket brigade

a. BUCKET BRIGADE CIRCUIT



b. SINGLE STAGE IMPLEMENTATION (BIFOLAR)

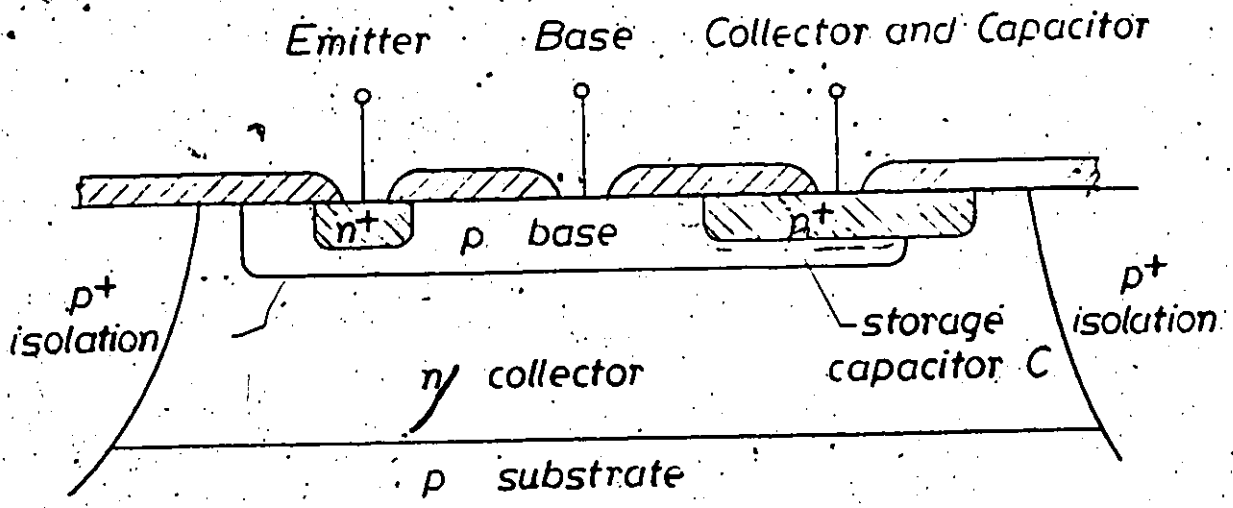


Figure 1.2 Sangster and Teer's Bucket Brigade Circuit[2.]

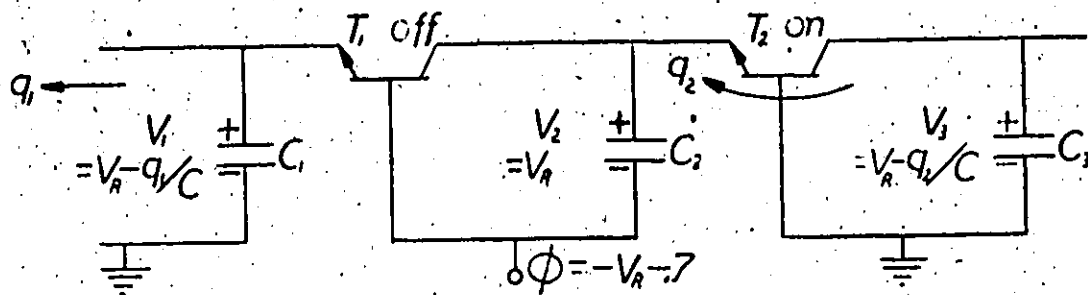
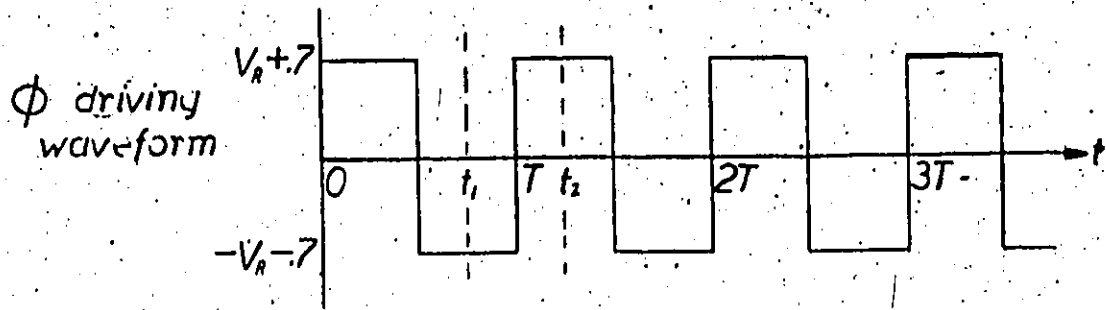
circuit was quite simple and compact as shown in figure 1.2b. The storage capacitor was implemented by overlapping the n^+ collector contact over the base diffusion.

The number of stages possible in the bipolar BBD's was limited by the common base current gain (α) of the transistors. Since a small fraction of the emitter current recombines in the base of each transistor the signal is attenuated over k transfers by a factor Λ :

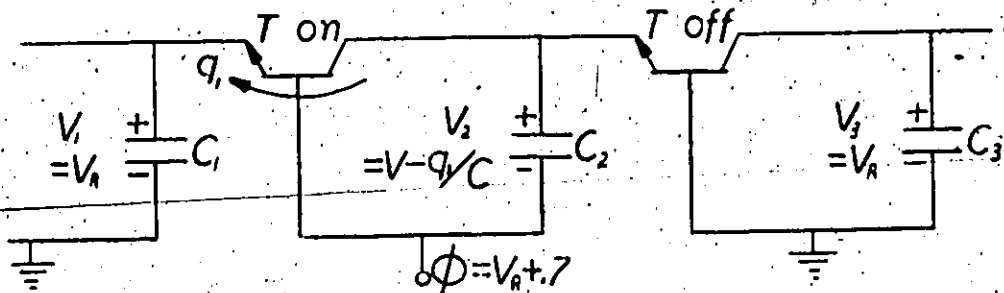
$$\Lambda = (\alpha)^k \quad 1.1$$

In later BBD's the bipolar transistors were replaced by MOS transistors to produce devices showing much less charge loss. The main limitation of MOS BBD's was not the charge lost completely but rather the charge left behind on the previous stage after transfer. Practical devices are able to transfer about .999 of the stored signal charge to the next stage in each clock cycle.

In 1970 another degree of simplification was achieved in charge transfer devices by Boyle and Smith[3] with the introduction of the charge coupled device. As shown in figure 1.4a the CCD consists of an array of closely spaced MOS capacitors. The device is not readily broken down into an equivalent circuit of transistors and capacitors like the BBD, but must be considered in terms of charge storage and manipulation. In operation the CCD stores minority carriers in potential wells created at the surface of the silicon



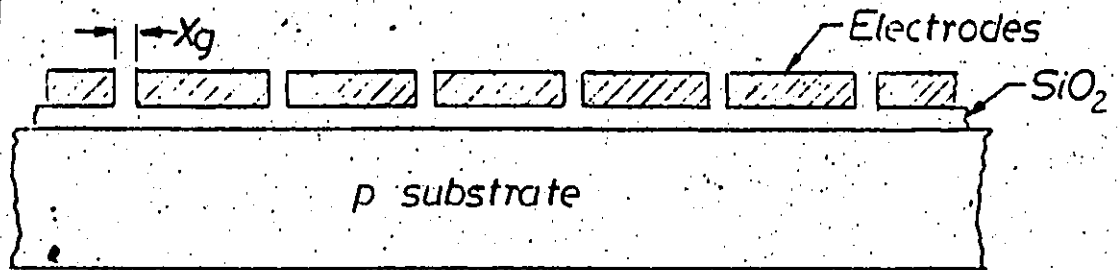
$t = t_1$, Signal on C_1 , represented by voltage deficit q_1/C below reference voltage V_R



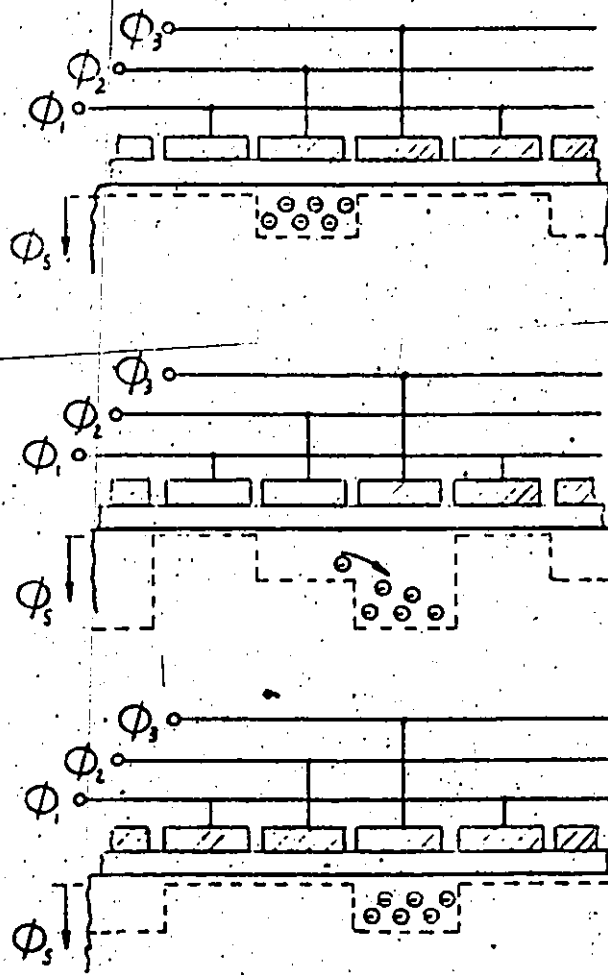
$t = t_2$, ϕ changes polarity turning T_1 on and T_2 off
 Signal transferred from C_1 to C_2 by charge deficit q_1 (ie charge q_1 transfers from C_2 to C_1)
 Similarly q_2 transfers from C_4 to C_3 as signal goes from C_3 to C_4

Figure 1.3 BBD Operation

a. CROSS SECTION



b. THREE PHASE OPERATION



1) Storage Mode $\Phi_2 > \Phi_1, \Phi_3$
 Charge stored in potential well under Φ_2 electrode

2) Transfer Mode $\Phi_3 > \Phi_2 > \Phi_1$
 Charge moves to potential minimum under Φ_3 electrode.
 $\Phi_1 < \Phi_2$ to prevent charge from transferring backwards

3) Storage Mode $\Phi_3 > \Phi_2, \Phi_1$
 Charge remains under Φ_3 electrode ready for next transfer

Figure 1.4 Single Level Charge Coupled Device (n channel)

substrate. Charge transport is achieved by controlling the magnitude and position of these potential wells along the silicon surface as shown in figure 1.4b.

The CCD has no equivalent component to the switch as shown in figure 1.1a for the discontinuous delay line, so that some other method is required to define the direction of charge transfer within the device. In the first CCD's this was accomplished by using a three-phase clocking scheme. The third phase allows the charge to transfer in one direction only, as shown in figures 1.4b1 to 1.4b3. Since the original publication of the CCD using the three-phase single level structure, many other structures and clocking schemes have been introduced.[4,5,6]. In many of these devices the direction of charge transfer is determined by asymmetries in the CCD construction, so that only two clock phases are required for operation.

The following chapters of this work describe the implementation of transversal filters using CCD's. Chapter two describes the two-phase, two-level polysilicon gate CCD which was used in all of the examples presented in this study. Chapter three reviews the operation of sampled data transversal filters and describes different methods of signal reconstruction which are compatible with CCD's. In chapter four the effects of cumulative charge loss and incomplete transfer are discussed in terms of their influence on the CCD filter transfer function.

Chapter five describes flexible filter implementation using the voltage sensing CCD and an external summing network. Results are presented for a 24-tap lowpass filter and a 32-tap bandpass filter.

Chapter six describes fixed filter implementation using the split electrode CCD. Results are obtained for a 24-tap lowpass filter. An analysis is presented on the loading effects of the electrode capacitances on the output signal. Suggestions are made as to how the split electrode filters could be directly cascaded to produce higher order filters with less sensitivity to coefficient error.

Chapter seven contains the conclusions obtained from this study.

TWO-LEVEL POLYSILICON GATE CCD

2.1 GENERAL

The two-level polysilicon gate CCD [7,8,9] is shown in figure 2.1. The purpose of the two-level gate structure is to produce an asymmetric potential well under the upper and lower electrodes with the application of a common clock pulse. ~~With this design the direction of charge transfer is defined by the asymmetry of the device.~~ As a result only two clock phases are required for operation.

The two-level CCD also maintains more efficient control of the surface potential within the channel region. In the three-phase structure discussed previously, device operation is highly dependent on the inter-electrode gap X_g (figure 1.4). It must be very narrow (2-3 microns) to maintain a controlled field under the gap region. This places a rather narrow tolerance on the etching process during fabrication and can result in reduced yield. In the two-level structure, the lower electrodes (storage electrodes) are well spaced and the channel regions between them are controlled by the upper electrodes (transfer electrodes). No gaps exist in this structure since the two gate levels overlap slightly.

Operation of this CCD is achieved using two-phase push clocks. As shown in figure 2.2, the two clock waveforms ϕ_1

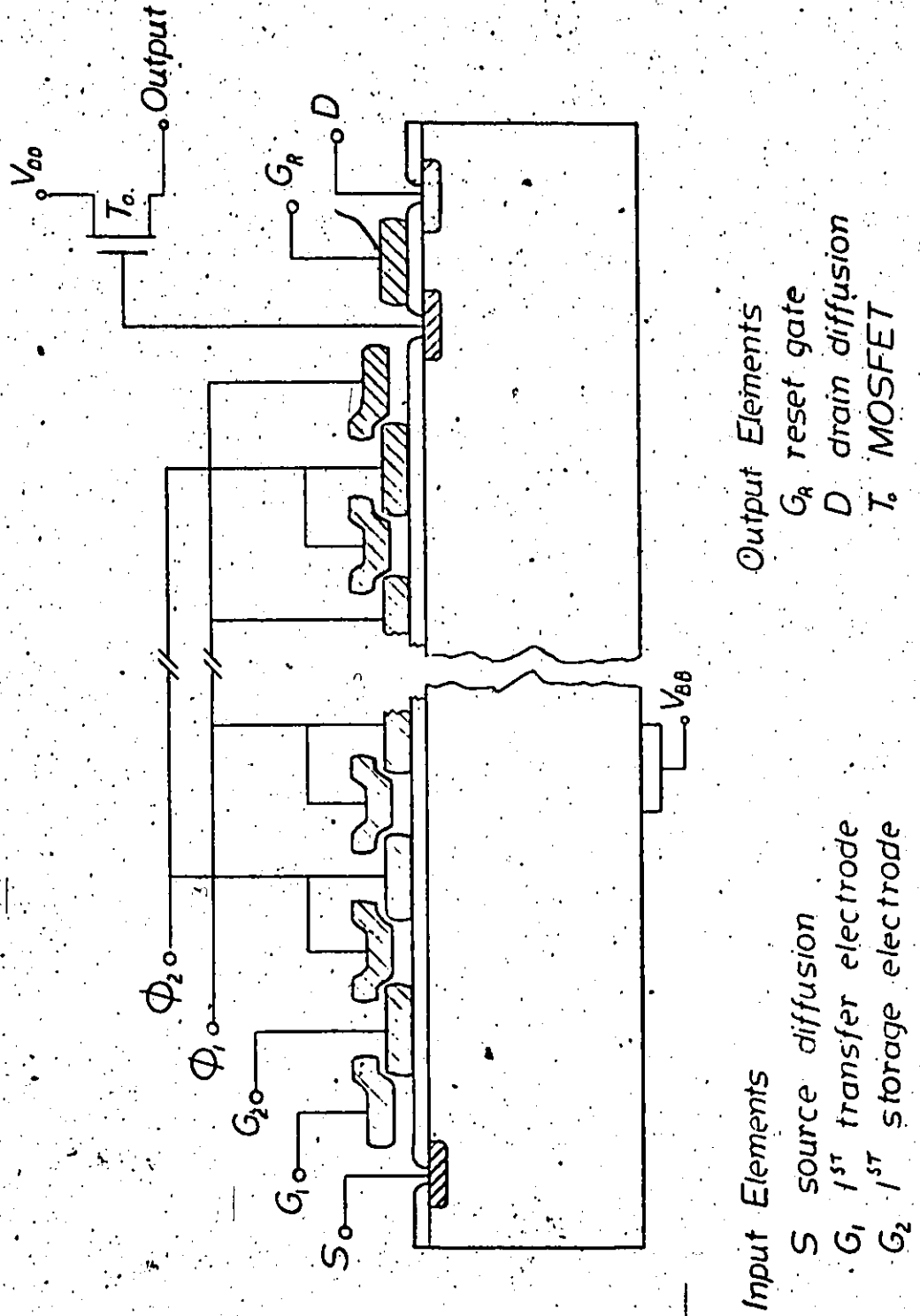
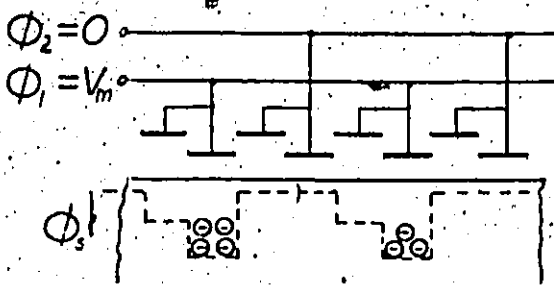
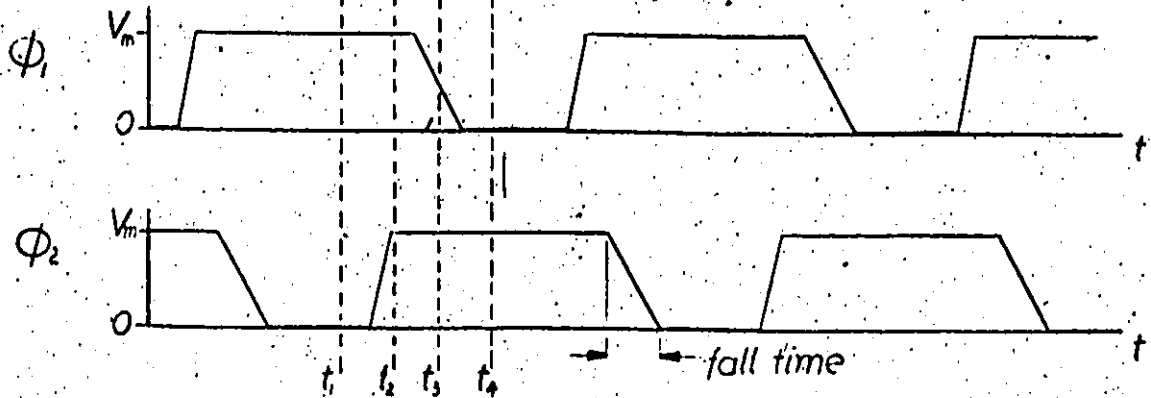
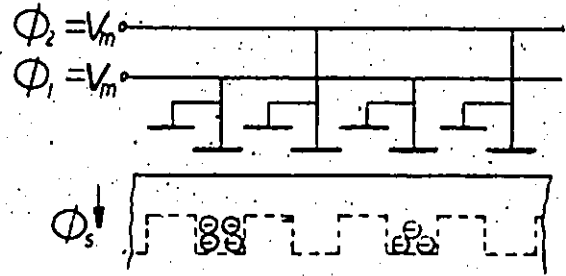


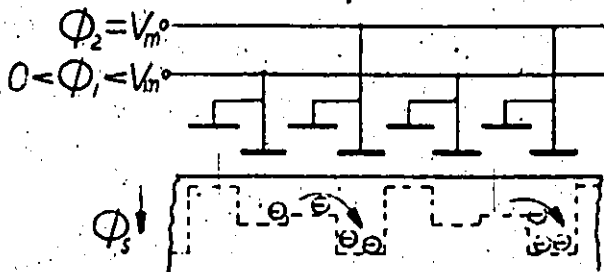
Figure 2.1 Two Level Polysilicon Gate CCD



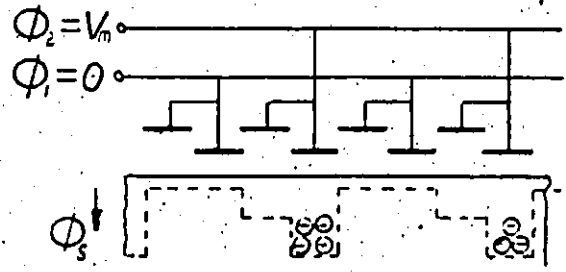
$t = t_1$ Charge stored under ϕ_1 storage electrodes



$t = t_2$ Potential wells formed under ϕ_2 electrodes ready to receive charge



$t = t_3$ Charge transfer occurs during fall time of ϕ_1



$t = t_4$ Transfer complete Charge stored under ϕ_2 storage electrodes

Figure 2.2 Two Phase Push Clock Operation

and ϕ_2 have a finite overlap to ensure control of the surface potential over the entire clock cycle. With ϕ_1 high and ϕ_2 low, the signal samples are stored under the ϕ_1 storage electrodes. When ϕ_2 goes high during the overlap period the charge remains under ϕ_1 but ϕ_2 produces a potential well ready to accept the charge carriers. As ϕ_1 goes low the potential minima disappear from this phase and the charge is "pushed" out of the ϕ_1 wells and into the ϕ_2 wells. It is apparent then that the transfer operation occurs only during the fall time of the clocks. The purpose of the clock overlap is to ensure that the one phase is in the correct state to receive mobile carriers as the other phase voltage falls. The fall time of the clocking waveforms must be slow enough to allow charge to transfer as completely as possible under the electrodes of the next phase. This is of the order of ten's of nanoseconds for the normal surface CCD.

The maximum charge which can be stored using the push clock operation is determined by the difference potential in the substrate due to the difference in oxide thickness under the upper and lower electrodes (the difference bucket).

2.2 INPUT METHODS

The method of charge input into the CCD is very

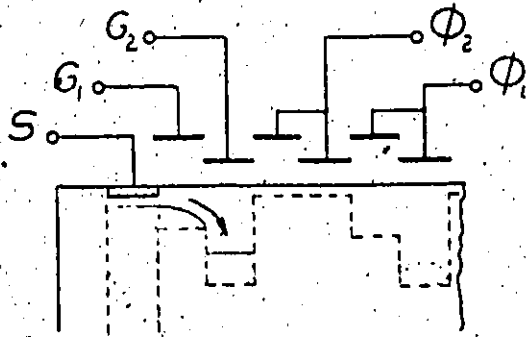
important in terms of maintaining the maximum linearity and dynamic range of device operation. Several possible input methods for the two-level CCD structure are shown in figure 2.3. In each case the charge injection is controlled by the following three elements:

- 1) input source diffusion
- 2) first transfer electrode
- 3) first storage electrode

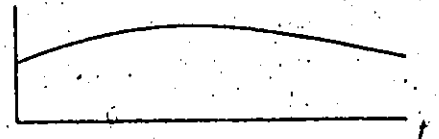
One of the simplest methods is the dynamic injection input [10] shown in figure 2.3a. The transfer gate (G_1) is held at a low dc potential and the input is applied to the source diffusion. The amount of charge injected into the storage well is dependent on the applied signal voltage during the time that the storage electrode is on. This injection, however is somewhat nonlinear and is affected by the channel conductance under G_1 as well as the length of the clock pulse applied to G_2 . The total charge injected varies in a dynamic (i.e. tends to integrate the signal over the period of ϕ_1) and nonlinear manner and this method is not suitable for most analog applications.

The other four methods shown in the figure are not dynamic in operation. The injected charge is determined by the input signal level during a very short sampling interval. These methods represent improvements over the dynamic injection method and can be compared using a simplified one-dimensional analysis. The voltage applied to

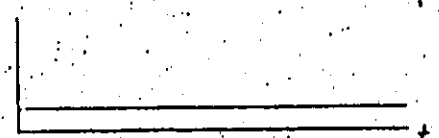
a DYNAMIC INJECTION



$S = \text{input}$



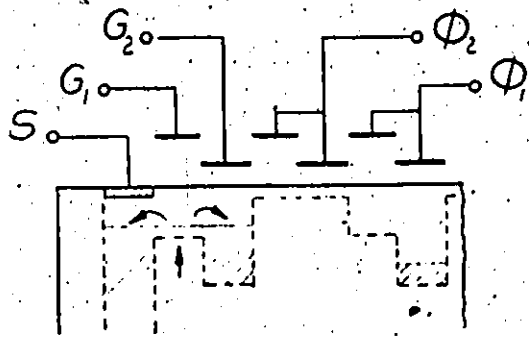
$G_1 = \text{small dc bias}$



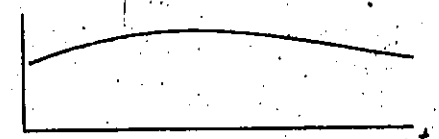
$G_2 = \Phi_1$



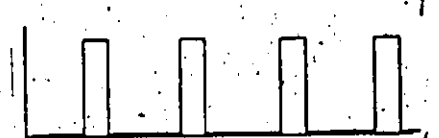
b DIODE CUTOFF



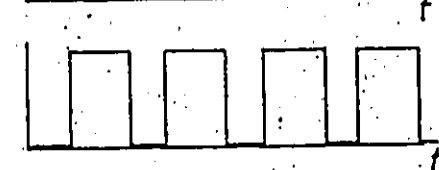
$S = \text{input}$



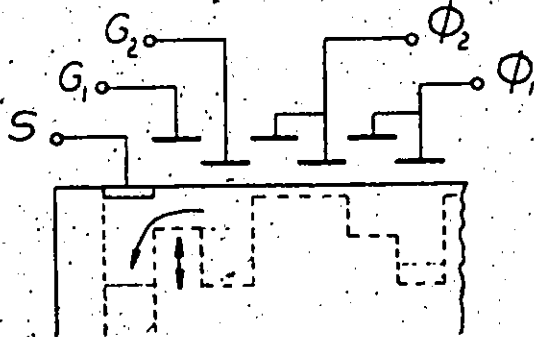
$G_1 = \text{strobe}$



$G_2 = \Phi_1$



c POTENTIAL EQUILIBRIUM I



$S = \text{trim pulse}$



$G_1 = \text{input + pulldown}$



$G_2 = \Phi_1$

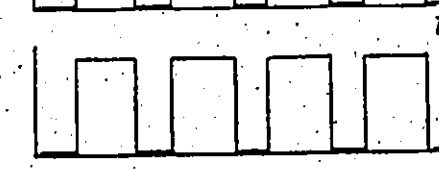
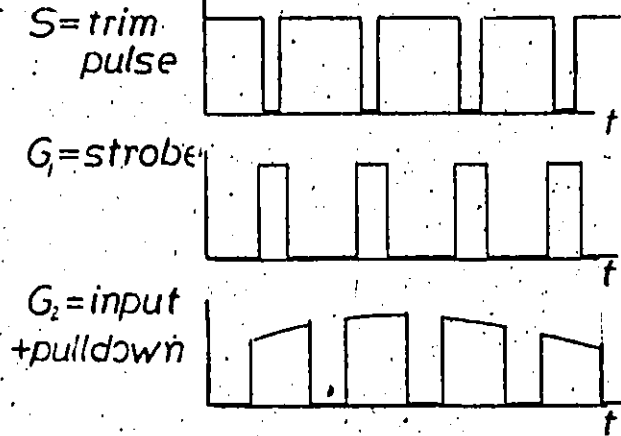
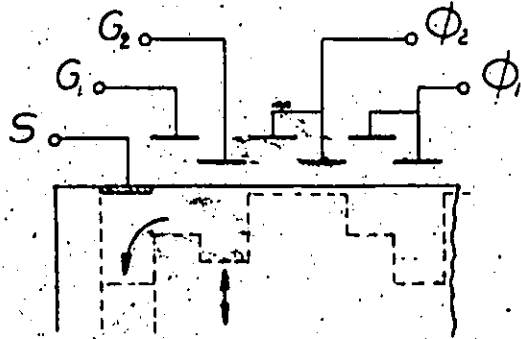


Figure 2.3 Input Methods for the Two Level CCD

d POTENTIAL EQUILIBRIUM II



e STROBED INPUT

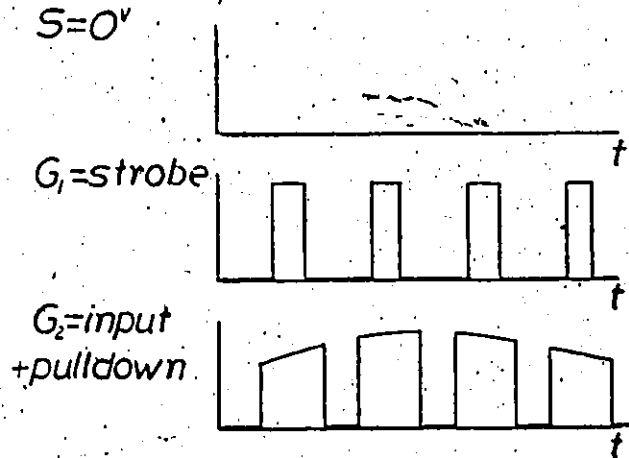
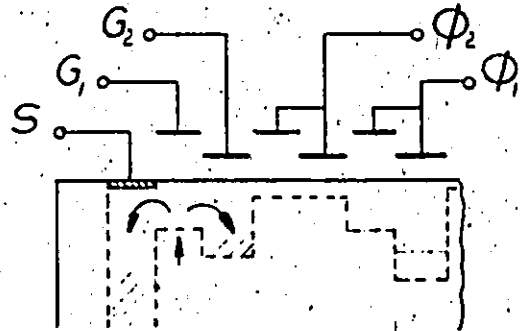


Figure 2.3 (continued) Input Methods for the Two Level CCD

the CCD electrode can be related to the surface potential, substrate bias, and device parameters in the following manner [11,12]:

with no mobile charge at the surface

$$V_G = V_{FB} + \phi_0 + 1/C_{ox} [2e_s q N_A (\phi_0 - V_{BB})]^{1/2} \quad 2.1$$

with mobile charge at the surface

$$V_G = V_{FB} + \phi + 1/C_{ox} [2e_s q N_A (\phi - V_{BB})]^{1/2} + q_n / C_{ox} \quad 2.2$$

where ϕ = surface potential under electrode

ϕ_0 = surface potential under electrode with no mobile charge at surface

V_{FB} = flatband voltage

C_{ox} = oxide capacitance/unit area

V_{BB} = substrate bias (negative for n channel device)

V_G = applied gate voltage

q_n = mobile surface charge density

In the diode cutoff method, shown in figure 2.3b, the biased input signal is applied to the input diffusion and holds the surface potential to the input voltage level. When the transfer and storage electrodes are both on, charge is injected from the source diffusion until the surface potential under the two gates is reduced to the value $V_{in} + 2\phi_F$ (using the onset of strong inversion as the criteria for holding the channel open). Substituting this value of the surface potential into (2.2) and solving for the mobile

charge density gives

$$q_n / (C_{ox})_{ST} = V_{G_2} - V_{in} - 2\phi_F + (V_{FB})_{G_2} - 1 / (C_{ox})_{ST} \{ 2\epsilon_s q N_A (V_{in} + 2\phi_F - V_{BB}) \}^{1/2} \quad 2.3$$

where $V_{BB} < V_{in} < (\phi_o)_{TR} - 2\phi_F$

subscript TR refers to transfer electrode

subscript ST refers to storage electrode

From (2.3), it is seen that the injected charge is a nonlinear function of the input voltage. This nonlinearity is introduced from the dependence of the depletion layer charge upon the surface potential. There is also a certain ambiguity in the partitioning of the charge stored under G_1 during the next transfer operation. Some of this charge will be transferred forward and some will be returned back to the source diffusion, contributing further to the nonlinearity of this input method.

Figure 2.3c shows another input technique, the potential equilibrium method. Here the input is applied to the transfer electrode (G_1) while the storage electrode is held on by the ϕ_1 clock pulse. Then the input diode is strongly reverse biased to collect charge back into the source diffusion. Charge stored under the transfer and storage electrodes is swept back to the source until all of the charge has been removed from under G_1 . The surface potential under G_1 with no mobile charge present is found implicitly from equation 2.1 to give

$$(\phi_0)_{G_1} = V_{in} - (V_{FB})_{G_1} - 1/(C_{ox})_{TR} \{2e_s q \eta A [(\phi_0)_{G_1} - V_{BB}]\}^{1/2} \quad 2.4$$

This potential represents a barrier to any further flow of carriers back to the source region and prevents the potential under G_2 from dropping below this level. Substituting the value of the surface potential into (2.2) for the case of a storage electrode gives

$$q_n / (C_{ox})_{G_2} = -V_{in} + V_{G_2} + (V_{FB})_{G_1} - (V_{FB})_{G_2} + [1/(C_{ox})_{G_1} - 1/(C_{ox})_{G_2}] \{2e_s q \eta A [(\phi_0)_{G_1} - V_{BB}]\}^{1/2} \quad 2.5$$

where $(\phi_0)_{G_1}$ = function of V_{in}

This shows that the injected charge is a linear function of the input voltage for the case of a single level structure only. In the two-level CCD, the oxide capacitance is different for the transfer and the storage electrodes, and introduces a surface potential dependence on the charge injection (last term in equation 2.5). There is also a direct dependence on the voltage applied to G_2 so that any noise in the clock driving circuitry enters the input directly via the storage gate.

The linearity of the potential equilibrium method is improved by reversing the connections to G_1 and G_2 . The input signal is now applied to G_2 and G_1 is connected to the ϕ_1 clock. The input can be isolated from the driving circuitry by connecting G_1 to a separately generated strobe

pulse as shown in figure 2.3d. As in the previous technique the input diode is reverse biased so that charge is collected back to the source diffusion until no mobile carriers are left under G_1 . However, in this case, since the transfer gate is connected to a constant amplitude clock pulse, the final surface potential is always set to the same value independent of the input signal level. From equation 2.5, with the connections to G_1 and G_2 reversed, the input charge can be expressed as

$$q_n / (C_{ox})_{G_2} = -V_{G_1} + V_{in} + (V_{FB})_{G_1} - (V_{FB})_{G_2} + [1/(C_{ox})_{G_1} - 1/(C_{ox})_{G_2}] \{2\epsilon_s q N_A [(\phi_o)_{G_1} - V_{BB}]\}^{1/2} \quad 2.6$$

where $(\phi_o)_{G_1} = \text{constant}$

From the above equation based on a one-dimensional analysis, this version of the potential equilibrium method injects a charge which is a linear function of the applied signal voltage. Also, since the surface potential is set to the same value during each sampling interval, the two-dimensional effects and surface potential dependent terms have a minimum influence on the input linearity. Note that it is critical in this method that the clock pulse applied to G_1 be of constant amplitude so that noise is not added to the input signal.

The input method which has been used in this work is shown in figure 2.3e. It is identical to the second version of the potential equilibrium technique, except that the

source is not pulsed into reverse bias but is held at ground for the entire clock cycle. When the storage and transfer electrodes are both on, charge is injected below these gates until the surface potential drops to the value $2\phi_F$. Substituting this surface potential into equation 2.2 gives

$$q_n / (C_{ox})_{G_2} = V_{in} - 2\phi_F - (V_{FB})_{G_2} - 1 / (C_{ox})_{G_2} \{ 2e_s q N_A (2\phi_F - V_{BB}) \}^{1/2} \quad 2.7$$

The injected charge is seen to be a linear function of the input voltage. The main source of nonlinearity, not shown explicitly in equation 2.7, is the partitioning of the charge under G_1 , as in the diode cutoff method. This can be minimized by making the active area under G_1 as small as possible. Note that with this technique the strobe pulse amplitude on G_1 is not critical since it does not set the final surface potential as in the previous two methods. As long as the source diffusion is held at a constant dc level, there is no direct coupling of clock noise to the input signal. Also there is one less clock waveform required since the source diffusion is not pulsed.

2.3 OUTPUT METHODS

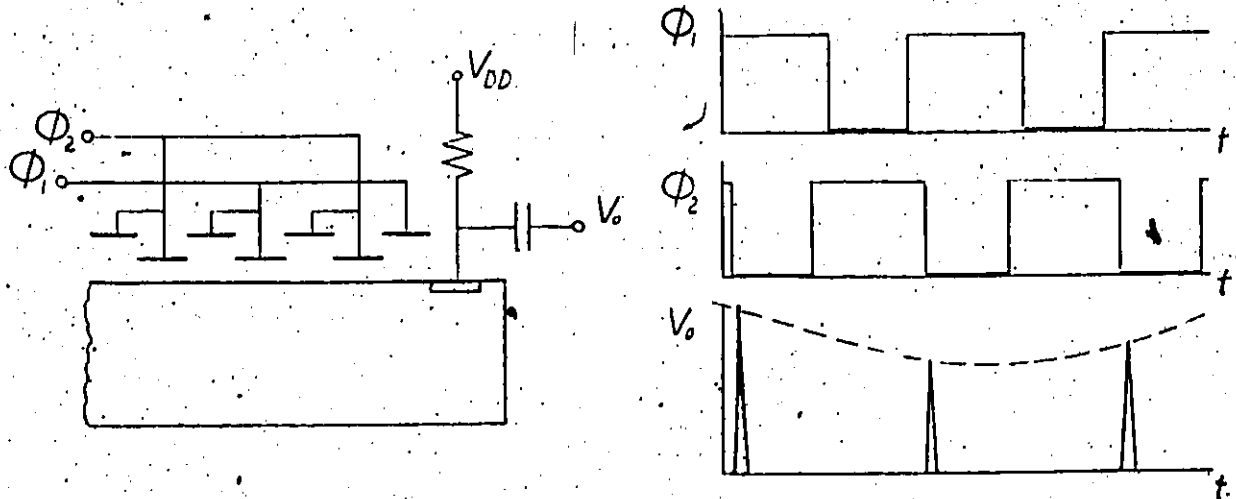
The sensing mechanism used to detect the CCD signal charge is equally important as the input in maintaining overall linearity in the device performance. The final

output must also be a charge sink and remove the carriers from the end of the CCD channel. Intermediate outputs, on the other hand, must remove as little charge as possible during the detection process in order to maintain the high transfer efficiency inherent to the devices.

The simplest method of output is a reverse biased diode as shown in figure 2.4a. This is suitable as a final output since all of the charge is collected at the reverse biased junction. The signal can be sensed using a dc blocking capacitor as shown in the figure. The output will appear as a narrow spike of current, such that the integral of the current is equal to the charge sample in the last stage of the CCD.

Another technique which is also used as a final output is the reset floating diffusion shown in figure 2.4b. It consists of a floating diffusion, reset gate, reset drain, and an output MOST. The drain is held reverse biased so that when the reset gate is turned on, the sensing diffusion is reset to V_{DD} and mobile charge carriers are removed. Then the reset gate is turned off and the n+ diffusion is left floating at a raised potential. When charge is transferred from the last stage of the CCD it is attracted by the potential of the floating diffusion. The mobile carriers are collected at the diffusion, causing the potential to drop by some amount proportional to the transferred charge. The sensing diffusion also controls the gate of an MOST source

a. REVERSE BIASED DIODE



b. FLOATING DIFFUSION WITH RESET

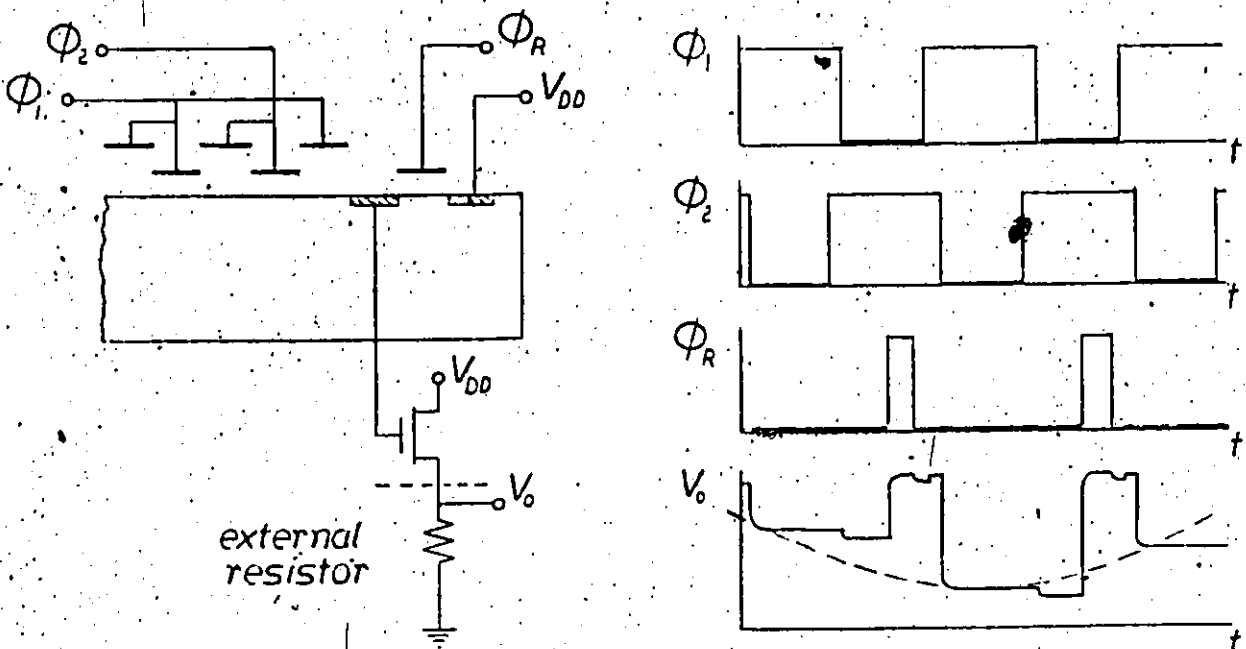


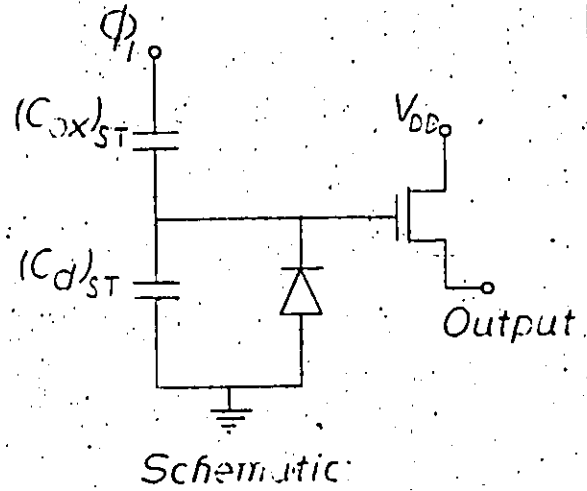
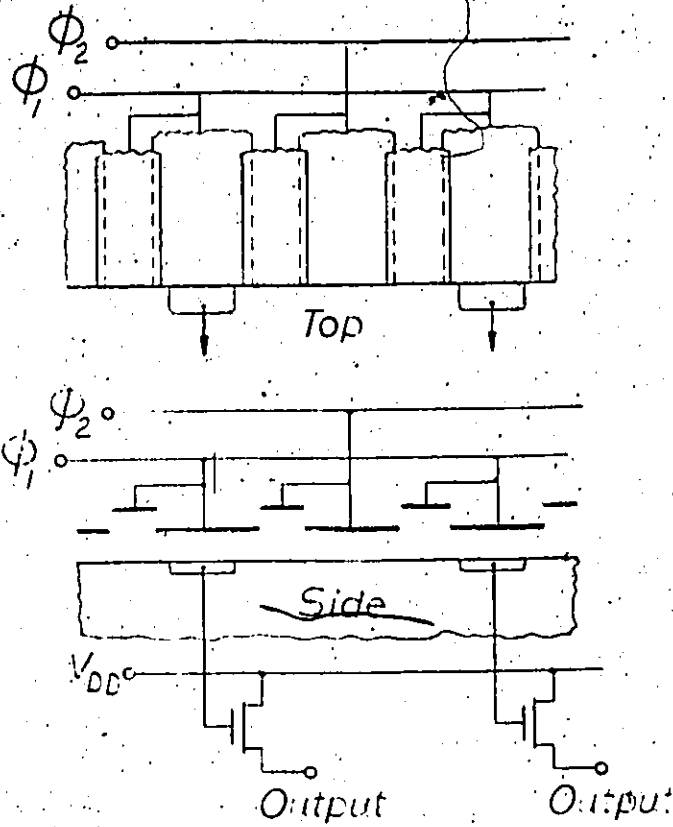
Figure 2.4 Final Output Methods for the Two-Level CCD

follower to provide an output voltage proportional to the detected signal. The voltage level of the floating diffusion remains essentially constant until the mobile carriers are removed upon application of the next reset pulse ϕ_R . Note that the diffusion is also affected by ϕ_1 through capacitive coupling from the adjacent transfer electrode. This is shown on the sketch of the output waveform in figure 2.4b.

A technique similar to the one above can be used in sensing intermediate stages of the CCD. This is the voltage sensing method shown in figure 2.5a. It consists of a small n^+ sensing diffusion and an output MOST. The diffusion is located at the side of a ϕ_1 storage electrode and connected to the input of an MOS transistor to provide a minimum of loading on the device stage. When the ϕ_1 phase turns on, the n^+ diffusion assumes the same potential as the substrate under the ϕ_1 electrode and controls the output voltage level of the source follower. When the ϕ_1 phase goes low, the sensing diffusion is left reverse biased and mobile charge carriers cannot return to the diffusion. This charge deficit will influence the next charge sample transferred along the device and thus represents a signal dependent distortion in the sensing mechanism. The effect is minimized by making the total capacitance of the sensing diffusion and MOST input gate as small as possible relative to the storage electrode capacitance.

An improvement in the above technique is shown in

a. SENSING DIFFUSION



b. SENSING DIFFUSION WITH RESET

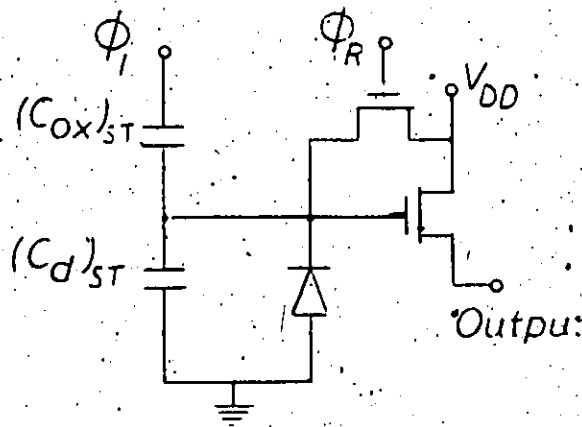


Figure 2.5 Voltage Sensing Techniques

figure 2.5b. Here a reset transistor has been added to reset the sensing diffusion to the same potential after each sensing operation. This will cause some attenuation along the line, but will lessen the distortion effect produced by charge sharing between adjacent stages of the device. As in the previous method, this attenuation can be minimized by making the sensing diffusion and input gate of the output MOS² as small as possible.

TRANSVERSAL FILTER

3.1 INTRODUCTION

The direct form of an Nth order sampled data filter is shown in figure 3.1. The input signal V is considered only at a set of points in time, but can take on a continuum of amplitude values. The filter produces a second sampled data signal at the output which is the desired transformation of the input signal. If the signal levels were quantized then the diagram of figure 6 would represent a digital filter and the operations indicated within the boxes would be implemented using memory, adders, and other digital hardware. This similarity can be important in terms of using the well established digital filter design techniques [13,14,15] available for calculating the required filter coefficients.

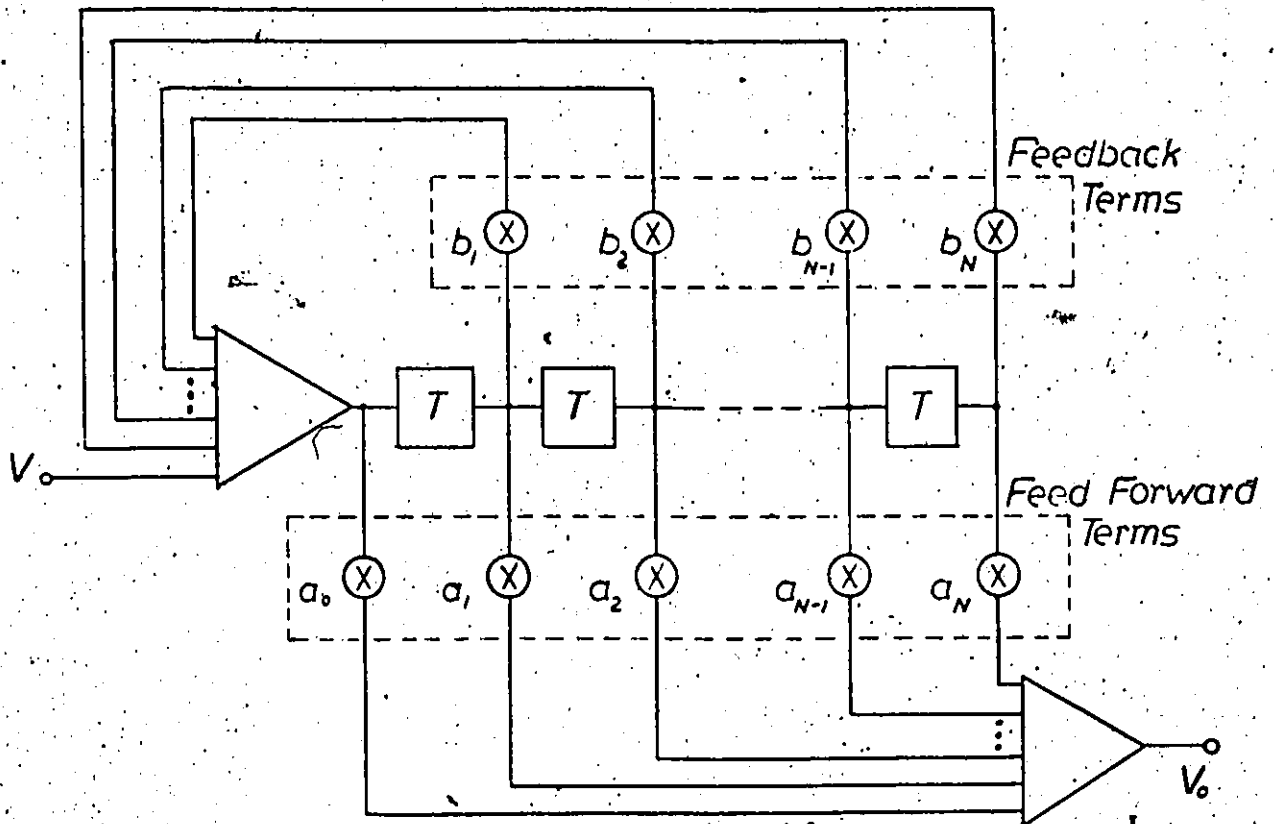
The direct filter form shown in the diagram has the transfer function

$$H(z) = \frac{\sum_{i=0}^N a_i z^{-i}}{\sum_{i=1}^N b_i z^{-i}} \quad 3.1$$

where N=number of delay stages.

a_i =gain of ith feed forward coefficient

b_i =gain of ith feedback coefficient



$$V_o(nT_c) = \sum_{k=0}^N a_k V((n-k)T_c) + \sum_{k=0}^N b_k V_o((n-k)T_c)$$

Figure 3.1 Nth Order Sampled Data Filter

z^{-1} = unit delay operator

This filter will realize any function which can be expressed as the ratio of two polynomials in z . The feed forward terms (a's) realize the zeros of the filter transfer function and the feedback terms (b's) realize the filter poles. A potential problem exists with this structure in that any inaccuracies in the feedback terms may cause the filter poles to shift to positions of instability. This would cause the filter to oscillate making it ineffective as a signal processing unit.

By eliminating the feedback terms (b's) the general structure shown reduces to that of a transversal filter [16]. This is an all zero filter and has no potential problems of instability. It can be designed to give a linear phase (constant delay) characteristic. The shape of the filter response curve depends on the ratio of the coefficient values only and not on their absolute values as in the feedback case. A further advantage of the transversal filter is that only one summing operation is required at the final output.

With the elimination of the feedback terms, the N-stage filter is no longer of Nth order. To obtain the same transfer function that was realized by the direct method, the denominator of the transfer function must be eliminated.

$$\frac{\sum_{j=0}^N a_j z^{-j}}{\sum_{j=1}^N b_j z^{-j}} = \sum_{i=0}^{\infty} h_i z^{-i} \quad 3.2$$

where h_i = gain of i th transversal filter coefficient

In general, division of two polynomials will lead to a polynomial of infinite degree. In practice, this result must be truncated after a finite number of terms to yield a finite length structure. It is also possible to optimize these terms to give a better approximation to the desired filter transfer function than could be obtained by simple truncation of the infinite series.

3.2 SENSITIVITY AND RESPONSE ERROR

A major consideration in filter design is the sensitivity of the transfer function to errors in the coefficient values. This can be derived from the standard definition of sensitivity.

$$S_{h_i} = \frac{H(z)}{h_i} \frac{\partial H(z)}{\partial h_i} \cdot \frac{h_i}{H(z)} \quad 3.3$$

Substituting the expression for the transversal filter (equation 3.2) into the above sensitivity formula gives

$$\frac{S}{h_i} = \frac{h_i z^{-i}}{H(z)} \quad 3.4$$

The magnitude of this sensitivity function is then

$$\left| \frac{S}{h_i} \right| = \frac{h_i}{|H(z)|} \quad 3.5$$

This result shows that the transversal filter transfer function is most sensitive to errors in the largest coefficients, and that the region of highest sensitivity is in the filter stopband where the magnitude of $H(z)$ is small. This can be seen intuitively by considering that in the stopband regions the filter is producing a very small output signal from the sum of many larger values.

The above expression is somewhat restrictive since it represents the sensitivity of the transfer function to only a single coefficient (i.e. the local sensitivity). When all of the coefficients contain errors, the effect on the filter transfer function is more complicated and must be considered in a statistical manner.

Puckette et al [17] have studied the problem of coefficient error in terms of the variance of the filter response error. The i th coefficient can be modelled as the sum of a nominal value plus an error term.

$$h_i = h_{i, \text{nom}} + e_i \quad 3.6$$

In most cases of interest the error term e_i can be

represented by one of the following two models.

$$\#1 \quad e_i = h_i \cdot X \quad 3.7$$

$$\#2 \quad e_i = \max\{h_i\} \cdot X \quad 3.8$$

where X = a random variable with distribution representative of the coefficient error

$\max\{h_i\}$ = magnitude of the largest coefficient

In the first model, (3.7), the coefficient errors are expressed as a fraction of the nominal value. This case would arise in using components with tolerances equal to some percentage of their indicated values. In the second model, (3.8), the coefficient errors are expressed as a fraction of the largest coefficient value. The errors are expressed as absolute rather than relative quantities as in the first model.

If the mean error can be assumed to be zero, then the variance of the filter response error can be calculated for the above two models in the following manner.

$$\#1 \quad \mathcal{E}\{|E(f)|^2\} = \mathcal{E}\{X^2\} \cdot \sum_{i=1}^N h_i^2 \quad 3.9$$

$$\#2 \quad \mathcal{E}\{|E(f)|^2\} = \mathcal{E}\{X^2\} \cdot N \cdot (\max\{h_i\})^2 \quad 3.10$$

The simplest case to consider is a uniform error distribution in the range defined by the tolerance of the coefficient values. The variance of the response error is then

$$\#1 \quad \mathcal{E}\{|E(f)|^2\} = (\text{tolerance})^2 / 3 \cdot \sum_{i=1}^N h_i^2 \quad 3.11$$

$$\#2 \quad \mathcal{E}\{|E(f)|^2\} = (\text{tolerance})^2 / 3 \cdot N \cdot (\max\{h_i\})^2 \quad 3.12$$

The response error will affect mainly the stopband of the filter as determined from the sensitivity results (equation 3.5). Thus the standard deviation of the response error should be smaller than the signal output in the stopband if the designed attenuation levels are to be achieved. The required tolerance for the case of a uniformly distributed error within the coefficient tolerance range is then

$$\#1 \quad \text{tolerance} < \frac{\sqrt{3} \cdot (\text{passband gain})}{\sqrt{\sum_{i=1}^N h_i^2}} \cdot 10^{-A_{dB}/20} \quad 3.13$$

$$\#2 \quad \text{tolerance} < \frac{\sqrt{3} \cdot (\text{passband gain})}{\sqrt{N \cdot \max\{h_i\}}} \cdot 10^{-A_{dB}/20} \quad 3.14$$

where A_{dB} = designed stopband attenuation measured in dB

The above two equations give an approximate upper bound on the tolerance required to achieve a given stopband attenuation.

3.3 IMPLEMENTATION

For the applications considered in this work the sampled data delay section (idealized CCD) can take the form as shown in figure 3.2a. It consists of M stages, each with a delay of T/M seconds to yield an overall delay of T seconds. To be compatible with the signal storage, the sampler must operate at a rate of M/T samples per second. Since sampling and delay are both linear operations, the above delay section can be represented by the equivalent structure shown in figure 3.2b. This is a continuous delay T followed by a sampler running at the rate M/T samples per second. The output from the single delay section is

$$V_o(t) = \sum_{n=-\infty}^{\infty} V(nT/M - T) \delta(t - nT/M) \quad 3.15$$

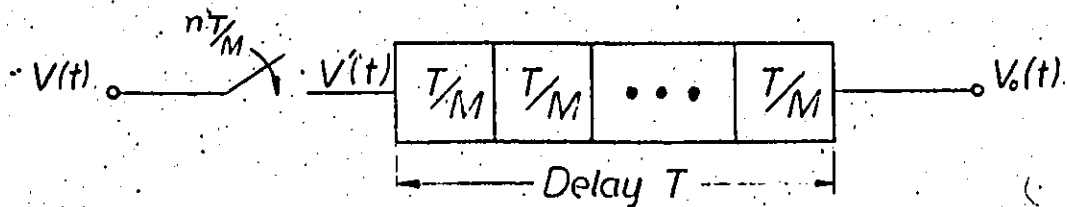
where $V(t)$ = input signal

$\delta(t)$ = unit impulse function

By connecting N of these delay sections in cascade and weighting the output of each, a transversal filter can be assembled as shown in figure 3.3a. As in the case of a single delay section, the filter can be represented as a continuous structure with the output sampled at the rate M/T samples per second. This equivalent filter shown in figure 3.3b has the same output as the actual sampled data filter.

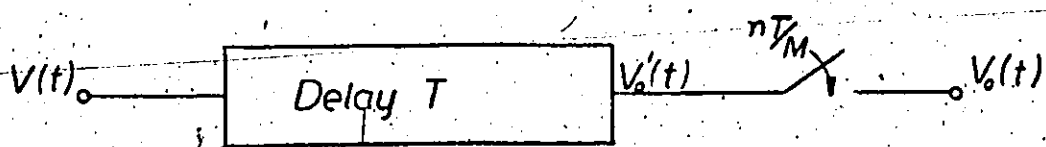
$$V_o(t) = \sum_{i=1}^N \sum_{n=-\infty}^{\infty} h_i V(nT/M - iT) \delta(t - nT/M) \quad 3.16$$

a SAMPLED DATA DELAY SECTION



$$\begin{aligned}
 V_o(t) &= V'(t-T) = \sum_{n=-\infty}^{\infty} V(t-T) \delta(t-nT/M-T) \\
 &= \sum_{n=-\infty}^{\infty} V(t-T) \delta(t-nT/M)
 \end{aligned}$$

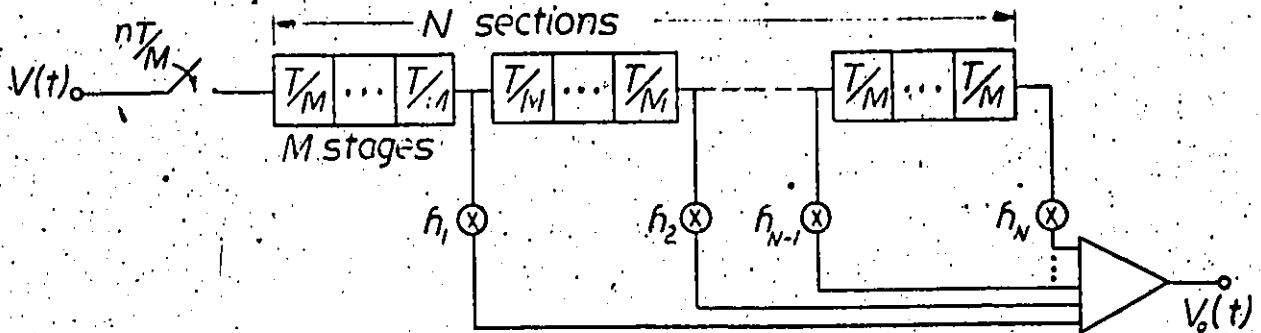
b EQUIVALENT DELAY SECTION



$$\begin{aligned}
 V_o(t) &= \sum_{n=-\infty}^{\infty} V'_o(t) \delta(t-nT/M) \\
 &= \sum_{n=-\infty}^{\infty} V(t-T) \delta(t-nT/M)
 \end{aligned}$$

Figure 3.2 Sampled Data Delay Section

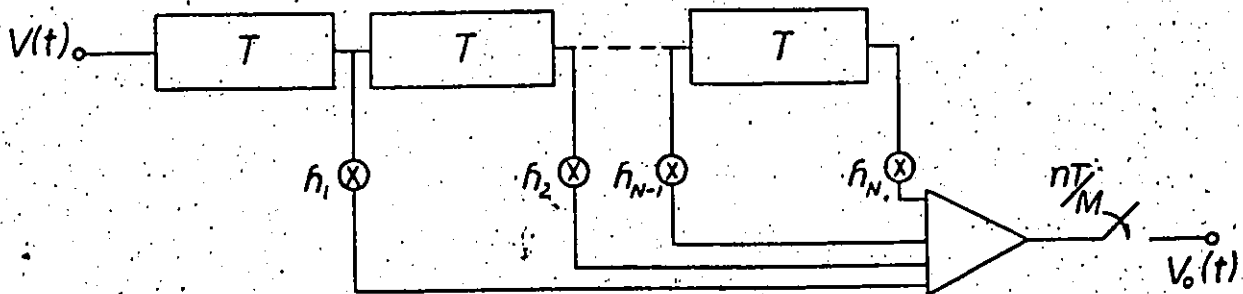
a. SAMPLED DATA TRANSVERSAL FILTER



$$V_o(t) = \sum_{i=1}^N h_i \sum_{n=-\infty}^{\infty} V(t-iT) \delta(t-nT/M)$$

$$= \sum_{i=1}^N \sum_{n=-\infty}^{\infty} h_i V(t-iT) \delta(t-nT/M)$$

b. EQUIVALENT FILTER STRUCTURE



$$V_o(t) = \sum_{n=-\infty}^{\infty} \delta(t-nT/M) \sum_{i=1}^N h_i V(t-iT)$$

$$= \sum_{i=1}^N \sum_{n=-\infty}^{\infty} h_i V(t-iT) \delta(t-nT/M)$$

Figure 3.3 N-Stage Sampled Data Transversal Filter

A representation of the waveforms associated with the sampled data transversal filter is shown in figure 3.4. It is seen that the delay T determines the frequency scaling and periodicity of the transfer function while the number of stages per delay section (M) determines the positions of the frequency translated baseband spectra.

Using higher values of M does not change the bandwidth restrictions on the input signal. The spectrum of the filter transfer function is repeated every $1/T$ interval in the frequency domain. Thus in the general case the input signal should be bandlimited to $1/2T$. The main advantage in using higher values of M is in signal reconstruction at the output as explained in the next section.

3.4 SIGNAL RECONSTRUCTION

The signal output from the sampled data transversal filter, as described in the previous section, is a series of weighted impulses spaced T/M seconds apart. This impulse train represents the sampled output signal as determined by the input signal and filter coefficients. In the CCD structure, the output can take different forms depending on the method used to sense the charge samples. The simplest method, outlined in section 2.3 is the reverse biased diode.

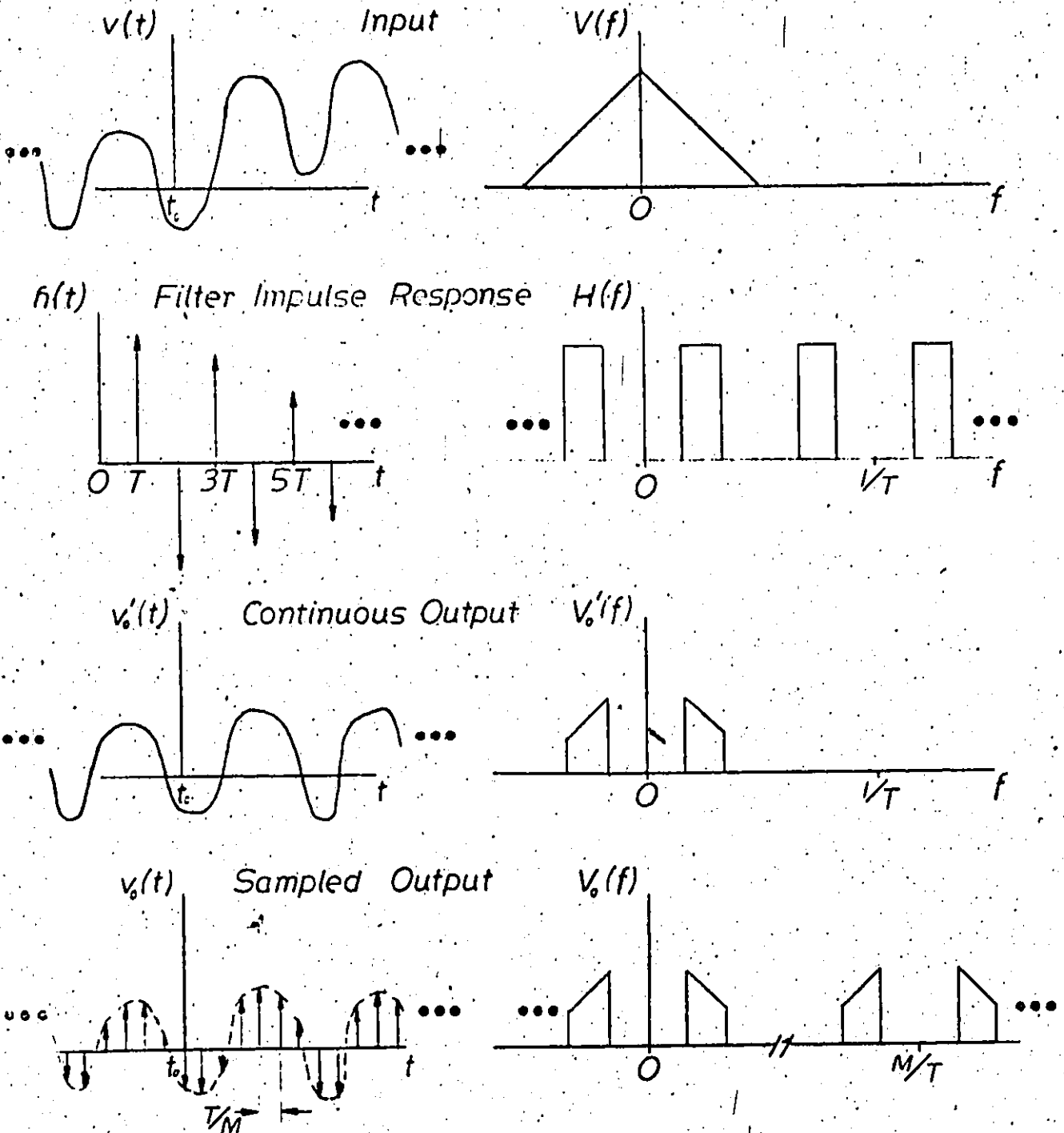


Figure 3.4 Sampled Data Filter Output Waveforms

This produces a spike of current during each clock period which approximates the output of an ideal sampler. The integral of the current in each spike is proportional to the charge transferred from the previous stage. However, this method cannot be used for sensing the intermediate stages since all of the charge is removed from the CCD during the sampling operation.

A more practical method is the floating diffusion, described in section 2.3. It can be used as a final output (with reset circuitry) or as an intermediate output. In either case the signal produced is a voltage proportional to the stored charge sample, and is held at a constant level for the duration of the ϕ_1 clock pulse. By controlling the relative widths of the clock pulses ϕ_1 and ϕ_2 it is possible to vary the fraction of the clock period for which the signal level is held.

The operation of holding the signal at a constant level can be expressed as a convolution of the ideal sampled output signal with a pulse $P_\tau(t)$ as shown in figure 3.5. The output signal $S(t)$ can then be expressed as

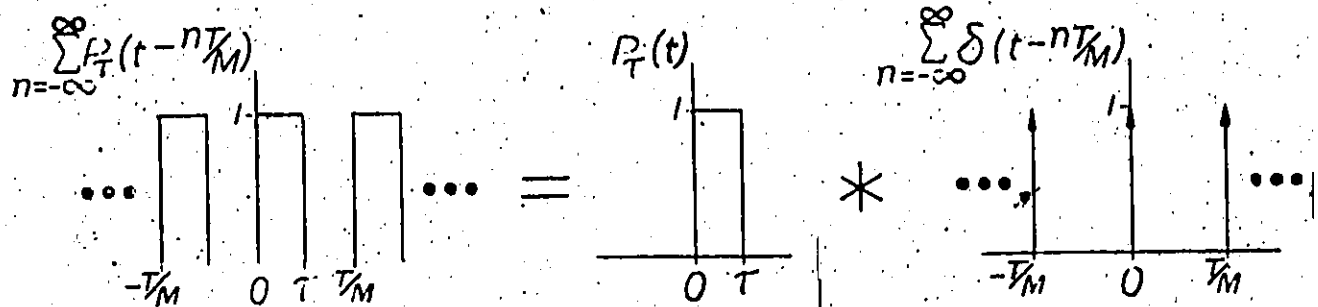
$$S(t) = V_o(t) * P_\tau(t) \quad 3.17$$

where $V_o(t)$ = output of sampled data filter

$$P_\tau(t) = \begin{cases} 1, & 0 < t < \tau \\ 0, & \text{for all other values of } t \end{cases}$$

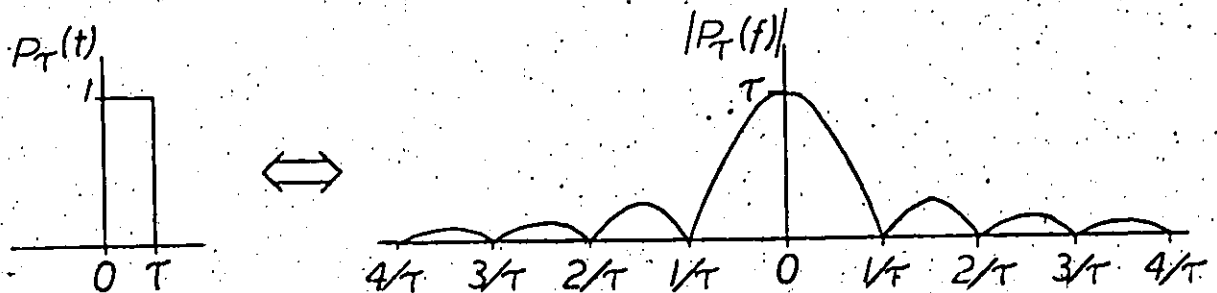
Substituting the output voltage of the sampled data filter

a DECOMPOSITION OF PULSE TRAIN



$$P_T(t) * \sum_{n=-\infty}^{\infty} \delta(t - nT/M) = \sum_{n=-\infty}^{\infty} \int_{-\infty}^{\infty} P_T(t-t') \delta(t' - nT/M) dt'$$

$$= \sum_{n=-\infty}^{\infty} P_T(t - nT/M)$$

b FOURIER TRANSFORM OF $P_T(t)$ 

$$P_T(t) \Leftrightarrow T \operatorname{sinc}(fT) \exp(-j\pi fT)$$

$$|P_T(f)| = |T \operatorname{sinc}(fT)|$$

Figure 3.5 Sample and Hold Output

(equation 3.16) into (3.17) gives

$$S(t) = \sum_{i=1}^N \sum_{n=-\infty}^{\infty} h_i V(nT/M - iT) \delta(t - nT/M) * P_T(t)$$

$$= \sum_{i=1}^N \sum_{n=-\infty}^{\infty} h_i V(nT/M - iT) P_T(t - nT/M) \quad 3.18$$

The frequency domain representation of (3.18) gives for the magnitude of the output signal:

$$|S(f)| = |V_0(f)| \cdot |\text{sinc}(fT)| \quad 3.19$$

where $\text{sinc}(x) = [\sin(\pi x)]/\pi x$

Thus the effect of the holding circuit is to cause the ideal filter magnitude function to be multiplied by a sinc function. This is shown in figure 3.6 for different values of the hold time. The sinc function suppresses the higher frequency harmonics of the input signal but also causes a certain rolloff in the baseband signal itself. The value of M can be chosen to improve both rolloff and higher band suppression at the expense of more stages per delay section as shown in figure 3.7.

The ideal method of signal reconstruction would be the use of a sinc pulse generator, in which each sinc pulse was weighted by an output sample from the transversal filter. The result of this technique would be perfect reconstruction of the output signal, provided that the input was bandlimited to one half of the system sampling frequency. This result comes from the sampling theorem

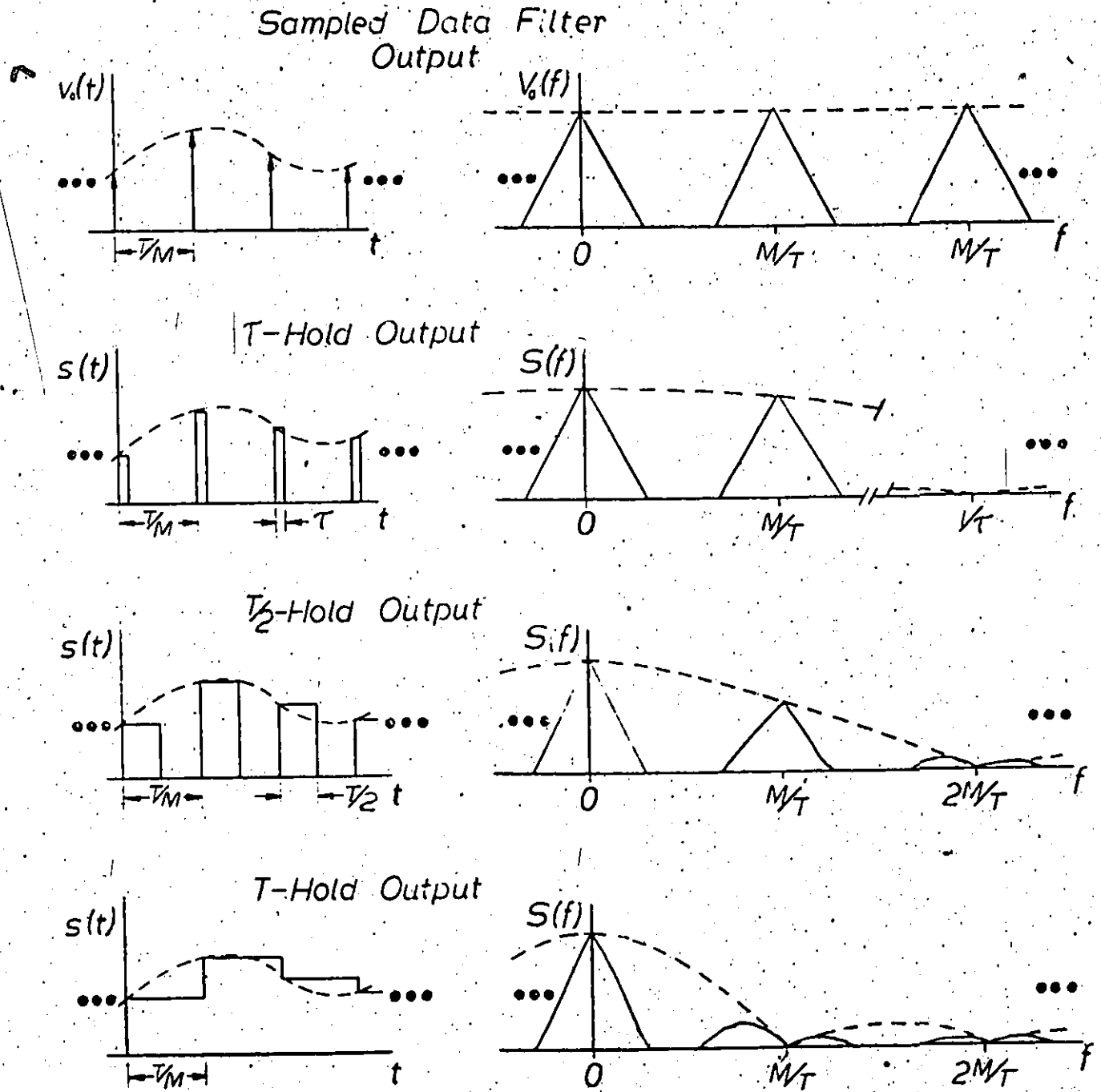
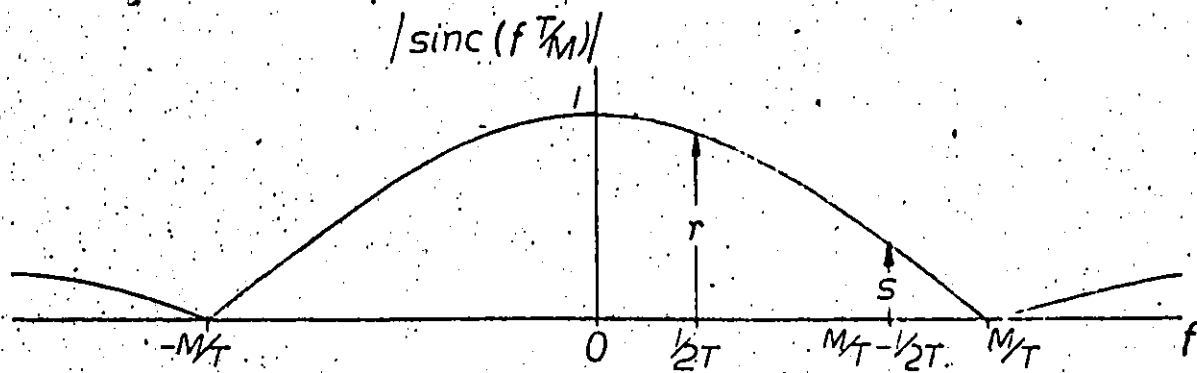


Figure 3.6 Output Signal Reconstruction



r = baseband rolloff at folding frequency $1/2T$
 s = maximum gain of out-of-band components
 (assuming input bandlimited to $1/2T$)

M	r	r (dB)	s	s (dB)
1	.6366	-3.922	.6366	-3.922
2	.9003	-0.912	.3001	-10.455
3	.9550	-0.401	.1910	-14.380
4	.9750	-0.224	.1392	-17.126
5	.9836	-0.144	.1093	-19.228
6	.9886	-0.899	.0899	-20.927
7	.9916	-0.073	.0763	-22.352
8	.9936	-0.056	.0662	-23.578

Figure 3.7 Effect of M (Number of Stages per Delay Section)

$$x(t) = \sum_{n=-\infty}^{\infty} x(nT) \text{sinc}(t/T - n) \quad 3.20$$

The sinc function is physically unrealizable but can be approximated by a delayed, truncated version of the sinc waveform. This approximation introduces a delay in the reconstructed waveform and causes some degree of amplitude distortion. The latter effect shows up as ripple in the frequency domain representation of the signal.

To make use of the sampled data structure available, the sinc function approximation can be implemented as a sampled-waveform, introducing translated baseband signals in the output spectrum. However, the sampling frequency of the output sinc pulse can be higher than (i.e. some multiple of) the clock frequency of the transversal filter so that the translated basebands are much farther removed from the desired baseband signal.

The problem of signal reconstruction can also be considered in the frequency domain in terms of lowpass filter design. What is required is a lowpass filter which passes only the baseband signal and attenuates all higher frequency bands of the output signal. It is necessary then to cascade another sampled data transversal filter as a final stage to the previously defined filter. This final stage can be an optimized lowpass design with clocking frequency at some multiple (K) of the previous sections (i.e. KM/T). Furthermore a sample and hold circuit can be implemented at

the output so that the higher order frequencies are attenuated as discussed previously. The overall effect of this final lowpass filter stage with sample and hold output is illustrated in figure 3.8.

If the input signal is bandlimited to $1/2T$, then the baseband rolloff and higher band suppression can be found from the table in figure 3.7 by replacing the value M with the product KM . A large amount of flexibility is available in choosing the values of K and M to suit particular design requirements.

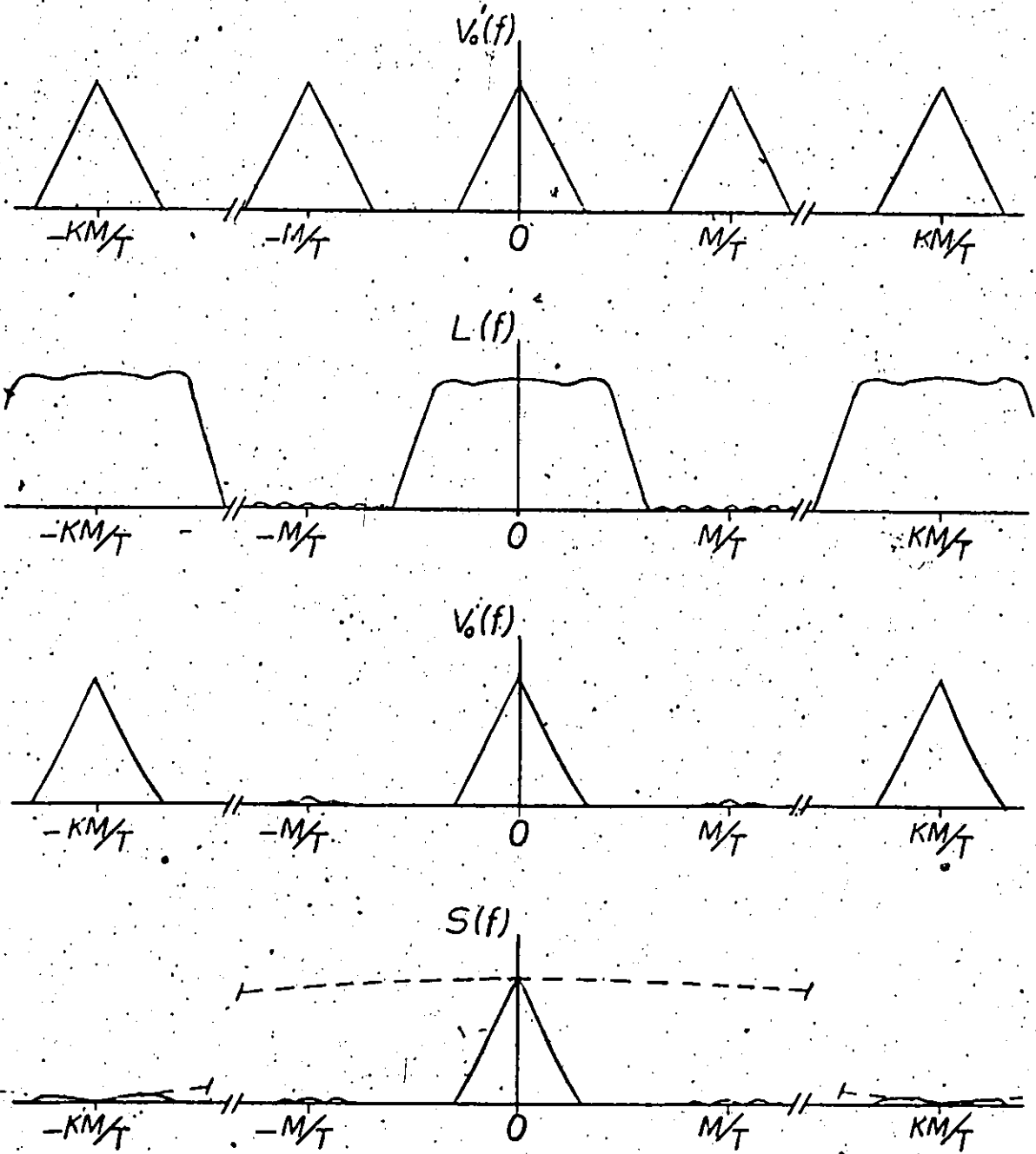
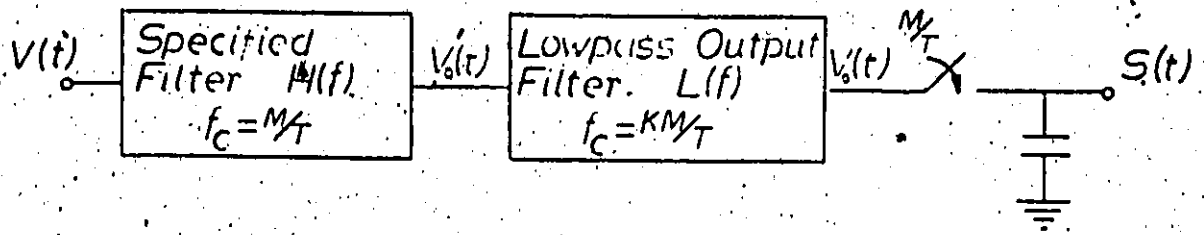


Figure 3.8 Effect of a Lowpass Filter Output Stage

NON IDEAL CHARGE TRANSFER

4.1 GENERAL

The performance of charge coupled devices as sampled data delay lines is limited by the effects of charge loss and incomplete transfer [18,19,20]. The interstage transfer in the devices can be better than 99.99% efficient such that the small fraction of charge lost or left behind is barely detectable. However, the effects of charge loss and incomplete transfer are cumulative over all stages, resulting in significant amplitude and phase distortion over a large number of transfers. These effects must be considered in filter design, especially if the proposed filter has a large number of delay stages. It may be necessary to offset the effects of non-ideal transfer by modifying the values of the tap weights.

4.2 CHARGE LOSS

The simplest effect which contributes to non-ideal operation of the CCD is charge loss during transfer (i.e. lost completely from the surface and not left behind on the previous stage). This effect can be characterized by the

total charge lost during transfer over one stage of the device.

$$\gamma = \frac{\text{charge lost from } i\text{th stage}}{\text{initial charge in } i\text{th stage}} \quad 4.1$$

The amount of charge in any given stage will be determined by the fraction of charge transferred from the previous stage.

$$q_i(nT) = (1-\gamma) q_{i-1}((n-1)T) \quad 4.2$$

If the input is such that the charge samples are proportional to the input voltage, then the voltage of the i th output can be expressed as

$$V_i(nT) = (1-\gamma)^i V((n-i)T) \quad 4.3$$

From this equation the net effect of charge loss is a frequency independent attenuation along the CCD delay line. In filter implementation this can be compensated for by adjusting the gain of each coefficient to make up for the signal attenuation at each point along the device. Normally CCD's do not show charge loss, as described above, since this effect is masked by the more dominant effect of incomplete charge transfer. However, one case where simple charge loss has been made dominant is the sensing diffusion output with reset, shown in figure 2.5b. Here the diffusion is reset to a constant voltage level after each sensing

operation so that any charge left behind is removed before it can influence the next charge sample to be sensed.

4.3 INCOMPLETE CHARGE TRANSFER

The dominant problem in CCD operation is that of incomplete charge transfer. In this case a fixed fraction of the charge sample is left behind after each transfer where it affects subsequent charge samples. This effect can be characterized by the transfer inefficiency

$$\epsilon = \frac{\text{amount of charge left behind on } i\text{th stage}}{\text{initial amount of charge on } i\text{th stage}} \quad 4.4$$

The amount of charge at any given stage of the device will then be determined by the fraction $(1-\epsilon)$ transferred from the previous stage plus the fraction (ϵ) left behind from the previous transfer.

$$q_i(nT) = (1-\epsilon)q_{i-1}((n-1)T) + \epsilon q_i((n-1)T) \quad 4.5$$

Taking the Z-transform of this equation

$$Q_i(z) = (1-\epsilon)z^{-1}Q_{i-1}(z) + \epsilon z^{-1}Q_i(z) \quad 4.6$$

Then solving for $Q_i(z)$

$$Q_i(z) = \left(\frac{1-\epsilon}{1-\epsilon z^{-1}} \right) z^{-1} Q_{i-1}(z) \quad 4.7$$

Assuming that the stored charge is proportional to the input voltage, $V(z)$, then the i th output can be expressed as

$$V_i(z) = \left(\frac{1-\epsilon}{1-\epsilon z^{-1}} \right)^i z^{-i} V(z) \quad 4.8$$

The transfer function for the output of a simple CCD delay line with k stages is then

$$\frac{V_k(z)}{V(z)} = \left(\frac{1-\epsilon}{1-\epsilon z^{-1}} \right)^k z^{-k} \quad 4.9$$

This is known as the modulation transfer function (MTF) of the CCD. In the ideal case $\epsilon=0$ and the MTF is z^{-k} (i.e. a pure delay of kT seconds). The effect of ϵ on the MTF is shown in figure 4.1. The transfer inefficiency is shown to affect both the magnitude and the phase of the delayed signal. For small values of ϵ as are characteristic of the CCD, the MTF of an n -stage CCD is a function of the product $n\epsilon$.

If this device is used as an N -stage transversal filter, then the output can be expressed as

$$V_o(z) = \sum_{i=1}^N h_i \left(\frac{1-\epsilon}{1-\epsilon z^{-1}} \right)^i z^{-i} V(z) \quad 4.10$$

The transfer function of this non-ideal filter can then be expressed in terms of modified filter coefficients as

$$H'(z) = \sum_{i=1}^N h_i' z^{-i} \quad 4.11$$

$$\text{where } h_i' = \left(\frac{1-\epsilon}{1-\epsilon z^{-1}} \right)^i h_i$$

It is possible to compensate for the dispersion due to

$$MTF(f) = \left(\frac{1-\epsilon}{1-\epsilon z} \right)^k z^{-k} \Big|_{z=e^{j2\pi f/f_c}} = M e^{-j\theta} e^{-j2\pi k f/f_c}$$

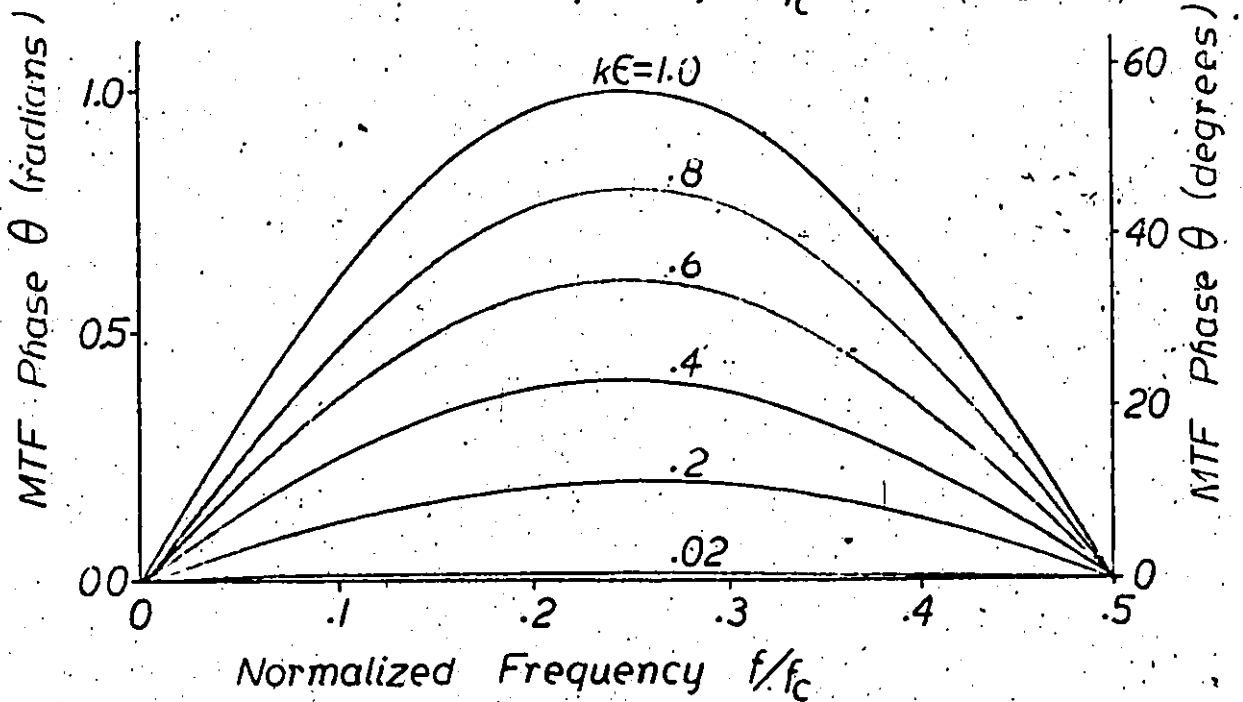
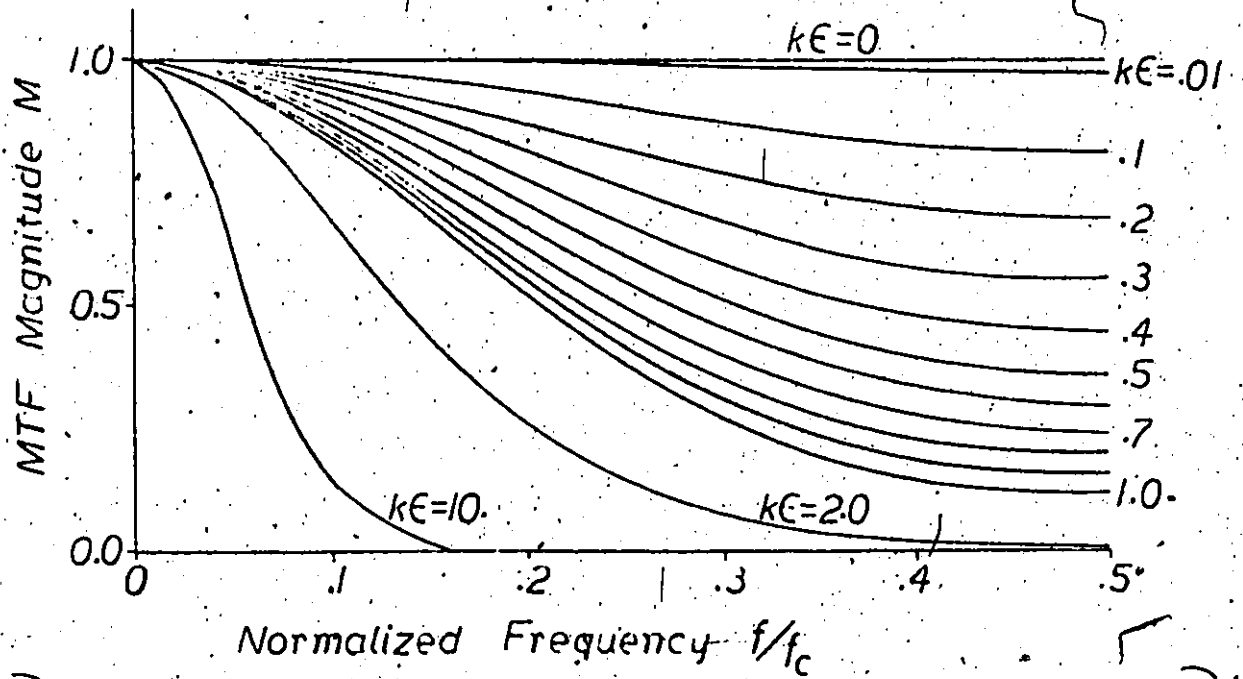


Figure 4.1 OCD Modulation Transfer Function (valid for small ϵ)

transfer inefficiency by altering the filter coefficients [21]. Expanding (4.11) for the case of an infinite number of coefficients gives

$$H'(z) = \sum_{i=1}^{\infty} \left[\sum_{m=0}^{i-1} h_{i-m} \binom{i-1}{m} e^m (1-e)^{i-m} \right] z^{-i} \quad 4.12$$

Equating the terms in the square brackets to the desired coefficient values gives

$$h_i = \frac{h_i - \sum_{m=1}^{i-1} h_{i-m} \binom{i-1}{m} e^m (1-e)^{i-m}}{(1-e)^i} \quad 4.13$$

This is an iterative formula for determining the corrected coefficients necessary to realize the desired filter transfer function. It generates an infinite number of coefficients, which can be truncated after approximately the same number of terms as the original filter design, since the remaining terms are very small.

The usefulness of this compensation technique is limited by the accuracy and consistency with which the transfer inefficiency ϵ can be predicted. Deviations from the predicted value will lead to errors in the compensated filter transfer function. The sensitivity of $H(z)$ to the transfer inefficiency ϵ can be calculated from

$$\frac{S}{e} = \frac{z^{-1} - 1}{(1-e)(1-ez^{-1})} \cdot \frac{e}{H'(z)} \cdot \sum_{i=1}^N i \left(\frac{1-e}{1-ez^{-1}} \right)^i h_i z^{-i}$$

$$\tilde{z} \frac{e(z^{-1}-1)}{H'(z)} = \sum_{i=1}^N ih_i z^{-i} \quad 4.14$$

This function is dependent on the particular filter design being implemented. The factor ih_i in the summation suggests that the sensitivity will increase with an increase in the number of delay stages.

CCD TRANSVERSAL FILTER (EXTERNAL WEIGHTING)

5.1 GENERAL

A direct method of constructing a CCD transversal filter is to provide an output at every Mth stage of the device. The signals from these outputs can then be weighted and summed appropriately to produce the required transfer function. In this first method of filter implementation to be presented, a 32-stage CCD with an external output available at each stage (i.e. $M=1$) was used. The outputs were provided using the voltage sensing technique explained in section 2.3 and illustrated in figure 2.5b. The device was enclosed in a 40-pin package to provide external pins to each of the 32 CCD outputs.

5.2 EXTERNAL SUMMING NETWORK

The external summing network used to implement the transversal filter coefficients is shown in figure 5.1. It consists of a resistive weighting network, two op amp summers, and an op amp difference amplifier. The resistors R_1 to R_{32} are all source resistors for the MOS source followers which are integrated on the CCD chip. The two

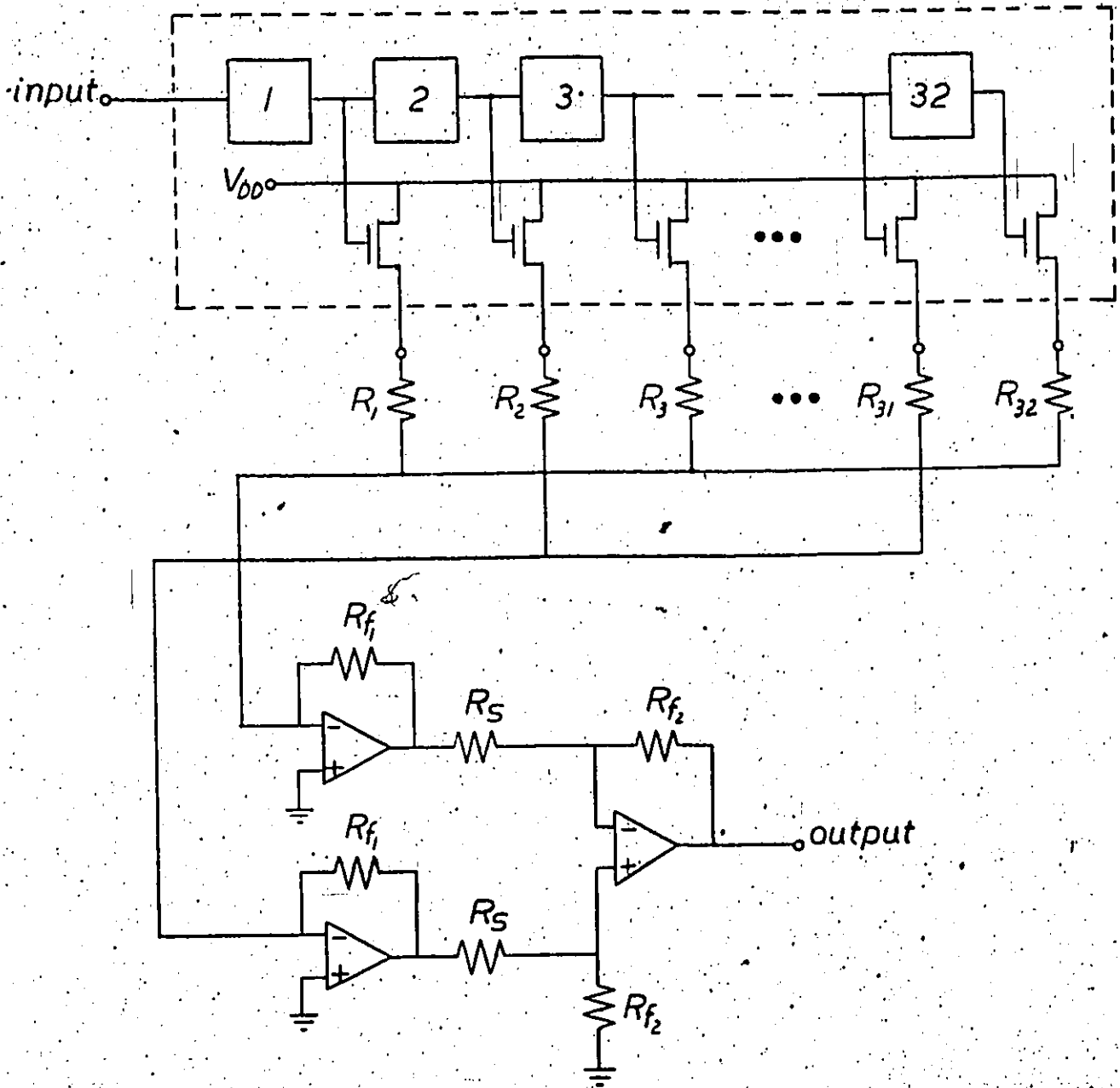


Figure 5.1 External Summing Network

summing amplifiers ensure that all of the above resistors are terminated at a virtual ground. In this way the current from each tap is inversely proportional to the combined resistance of the source resistor and the output impedance of the MOS transistor. One op amp summer is provided for the positive coefficients and the other is for summing the negative coefficients. The third op amp is connected in a difference amplifier configuration to produce the difference between the sum of the positive coefficients and the sum of the negative coefficients as well as to provide any final gain required.

A sample and hold amplifier can be added to the circuit to aid in filtering the signal. However, the effect of the sample and hold amplifier can be closely approximated by using asymmetrical driving clocks such that the width of ϕ_1 is much greater than the width of ϕ_2 . This effect was illustrated in figure 3-5.

The range of coefficient values possible with the resistive network is limited by a number of factors. First, the minimum resistance possible is determined by the amount of nonlinearity tolerable from the MOS source followers. Also the current through the transistors must be limited to a safe value to prevent overheating. In low frequency applications the minimum current which the op amp can detect will limit the maximum resistance used in the summing network. In higher frequency applications the resistance

values will be limited by the RC time constant of the CCD output. If R is too large in this case it will cause unwanted rolloff of the filtered signal. Further restrictions, based on power dissipation and area limitations would be in effect if the resistances were integrated onto the CCD chip.

The resistive network used in this work consisted of thirty-two potentiometers to achieve a range in resistance of from 1K to 500K.

5.3 RESULTS

The first design to be implemented was a 24-tap linear-phase lowpass filter taken from the published work by McClellan et al [22]. It is an optimized design with low passband ripple and a minimum stopband attenuation of 38dB. The coefficients were adjusted individually by monitoring the output signal amplitude of each tap with a constant amplitude sinusoidal signal at the input. The potentiometers were set in each case to produce the proper tap gain as determined by the filter design. This method of tap adjustment includes the output impedance of the MOS transistors. It also partially compensates for the effects of transfer inefficiency in that the attenuation along the line is accounted for in setting the tap gains. There is,

however, no compensation for the phase distortion introduced and this will affect the filter performance to some degree.

The output response of this lowpass filter is shown in figure 5.2. The measured response is seen to be in good agreement with the ideal response curve. The experimental results show a somewhat better attenuation in the stopband as the frequency approaches the folding frequency. This effect is however due to the sample and hold output, resulting in a sinc function rolloff in the frequency domain. For this filter with one stage per delay section, the sample and hold output gives an attenuation at the folding frequency of about 4dB as found on the table in figure 3.7.

A 32-tap bandpass filter[22] has been implemented in the same way as described above. The filter was designed to give an attenuation in the stopband of 56dB. The designed output characteristic along with a number of measured responses are shown in figure 5.3. Each curve in the figure was obtained after readjusting all of the potentiometers, attempting to get coefficient gains as accurate as possible. The measured curves all show excellent agreement with the theoretical curve in the passband region, but deviate noticeably in the stopband. This agrees with the results of section 3.2, that the transversal filter sensitivity is greatest in the stopband region.

The accuracy of the coefficients implemented with the

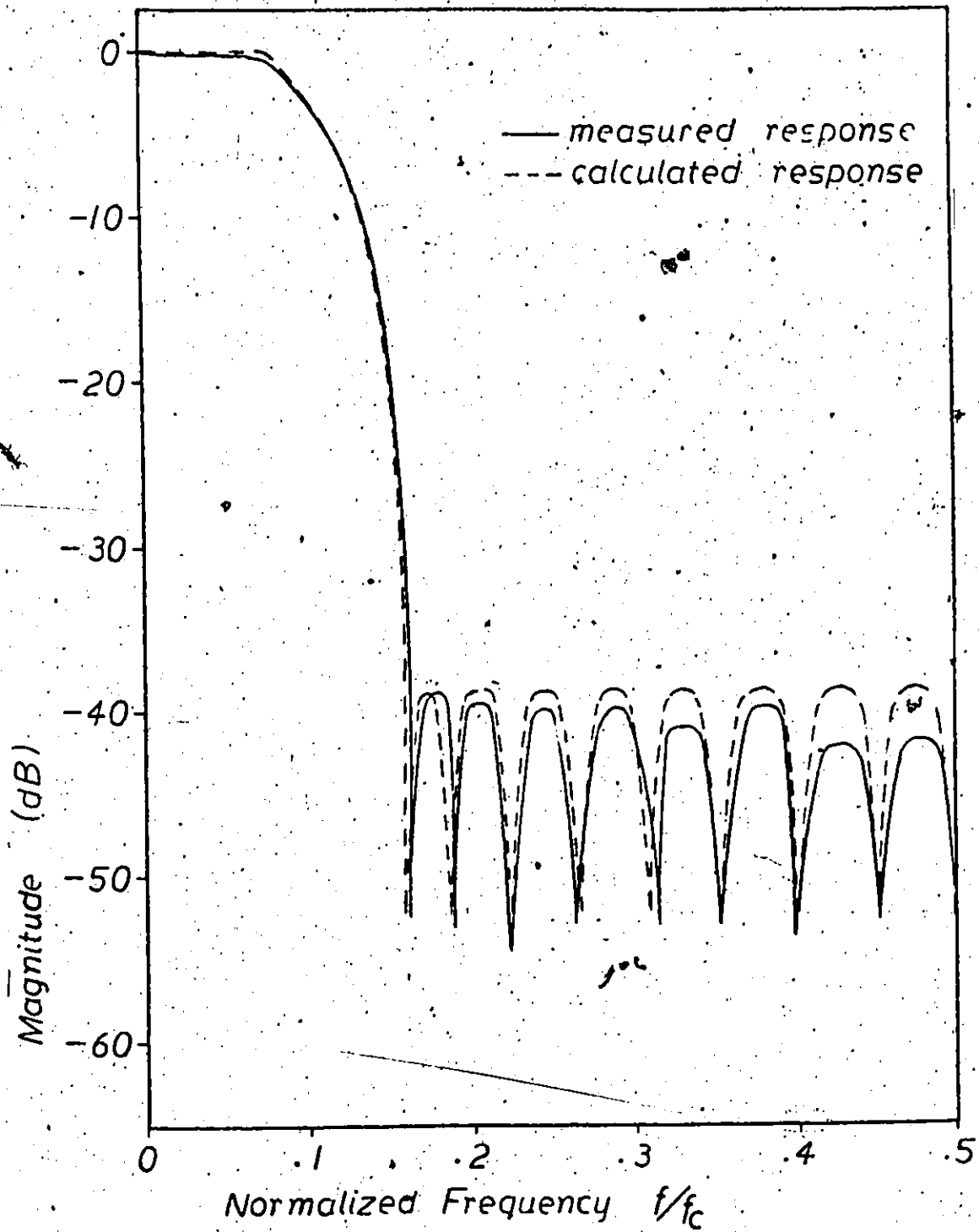


Figure 5.2 Output Response- 24-Tap Lowpass Filter

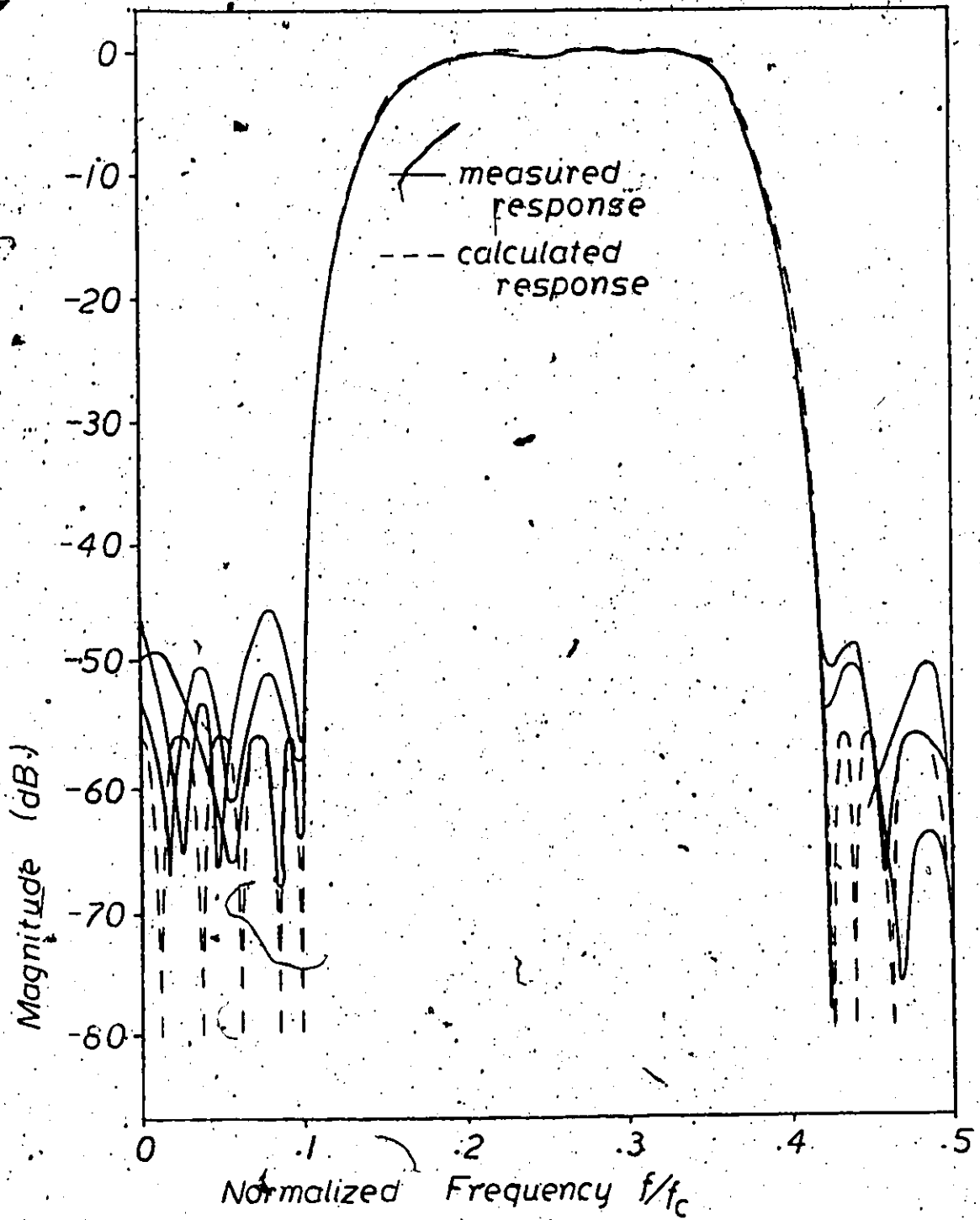


Figure 5.3 Output Response- 32-Tap Bandpass Filter

external weighting method was determined by the accuracy of the calibration instruments and the resolution available from the potentiometers. The coefficient error is best represented by the first model discussed in section 3.2 (equation 3.7). From (3.13) the tolerance required to achieve 38dB attenuation in the stopband of the lowpass filter design is calculated to be 4.5%. For the bandpass filter with a stopband attenuation of 56dB, the same calculation shows a tolerance requirement of 0.4%. In the experimental setup used the coefficient accuracy was estimated to be about 1%. From the above calculations this is sufficiently accurate to meet the lowpass filter specifications, but not to meet those of the bandpass filter. The measured results of figures 5.2 and 5.3 show agreement with the above predictions based on the simple uniformly distributed error model of section 3.2.

An MTF magnitude measurement was made on the last stage of the CCD to determine the transfer efficiency of the device. The results are shown in figure 5.4. The device gain at the folding frequency was .92, indicating a transfer efficiency of .9995 (from figure 4.1).

The harmonic distortion introduced by the voltage sensing CCD was examined using a spectrum analyzer. Figure 5.5 shows the spectral content of the output signal from the last tap of the CCD for three different input levels. In each case the output has been normalized to show 0 dB at the

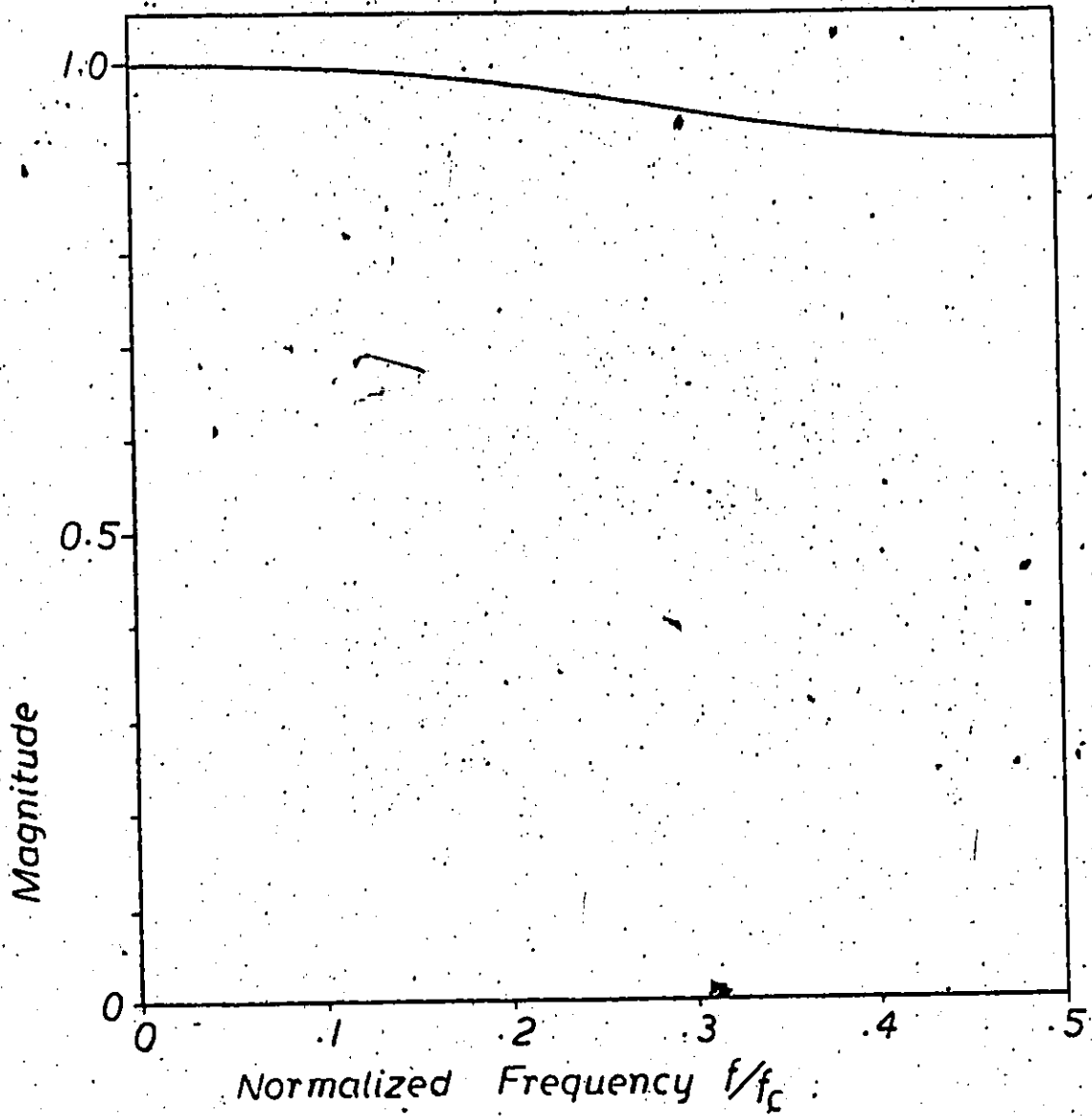


Figure 5.4 MTF Magnitude of Final Stage of 32-Tap CCD

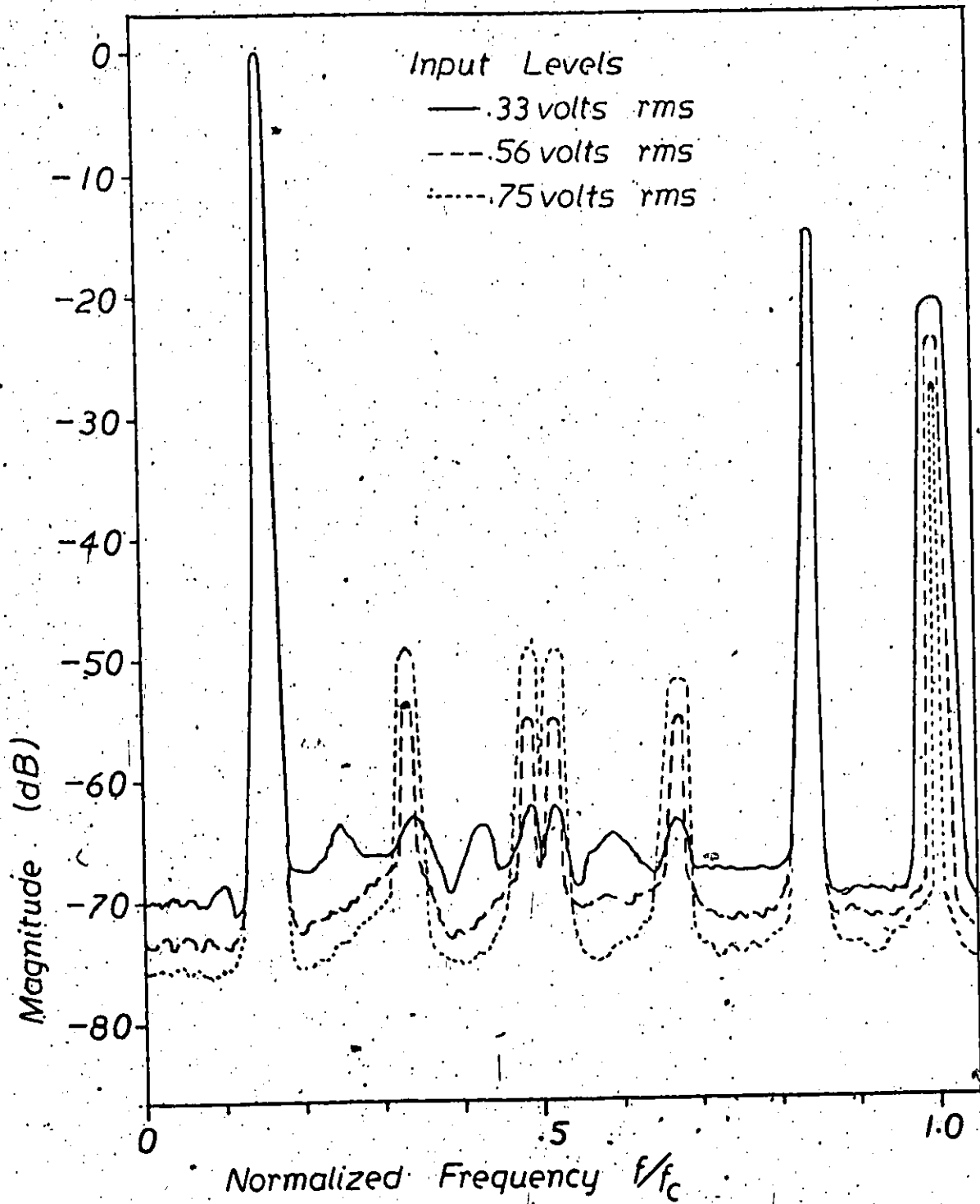


Figure 5.5 CCD Output Spectrum for Three Input Levels

fundamental frequency of the signal (2.45 KHz). With the input level at 0.33 volts rms. the harmonics are all more than 60 dB below the fundamental. Increasing the input signal level to .75 volts rms. causes greater signal distortion so that the harmonics are only about 47 dB below the magnitude of the fundamental as shown. In any given application the maximum input level will be determined by the amount of harmonic distortion tolerable.

Figure 5.5 also shows how the output spectrum of the CCD is reflected about the folding frequency ($0.5f_c$). The reflected harmonic and fundamental components are seen to be increasingly attenuated from the baseband levels because of the sample and hold output as discussed in section 3.4. There is a significant output component at the clock frequency ($f_c = 14$ KHz). This can be eliminated by making the hold time of the output exactly equal to the clock period ($T = 1/f_c$). In the case shown, the output was held only for the duration of ϕ_1 , which was 90% of the clock period.

The minimum detectable input signal to the CCD is limited by the noise level of the device. The output noise level of the 32-tap bandpass filter is shown in figure 5.6. This is a sketch of the output spectrum obtained with only the dc offset level applied to the input. The graph has been normalized so that 0 dB represents the magnitude of the filtered signal with the input signal in the passband at an amplitude of .33 volts rms. The results show that the

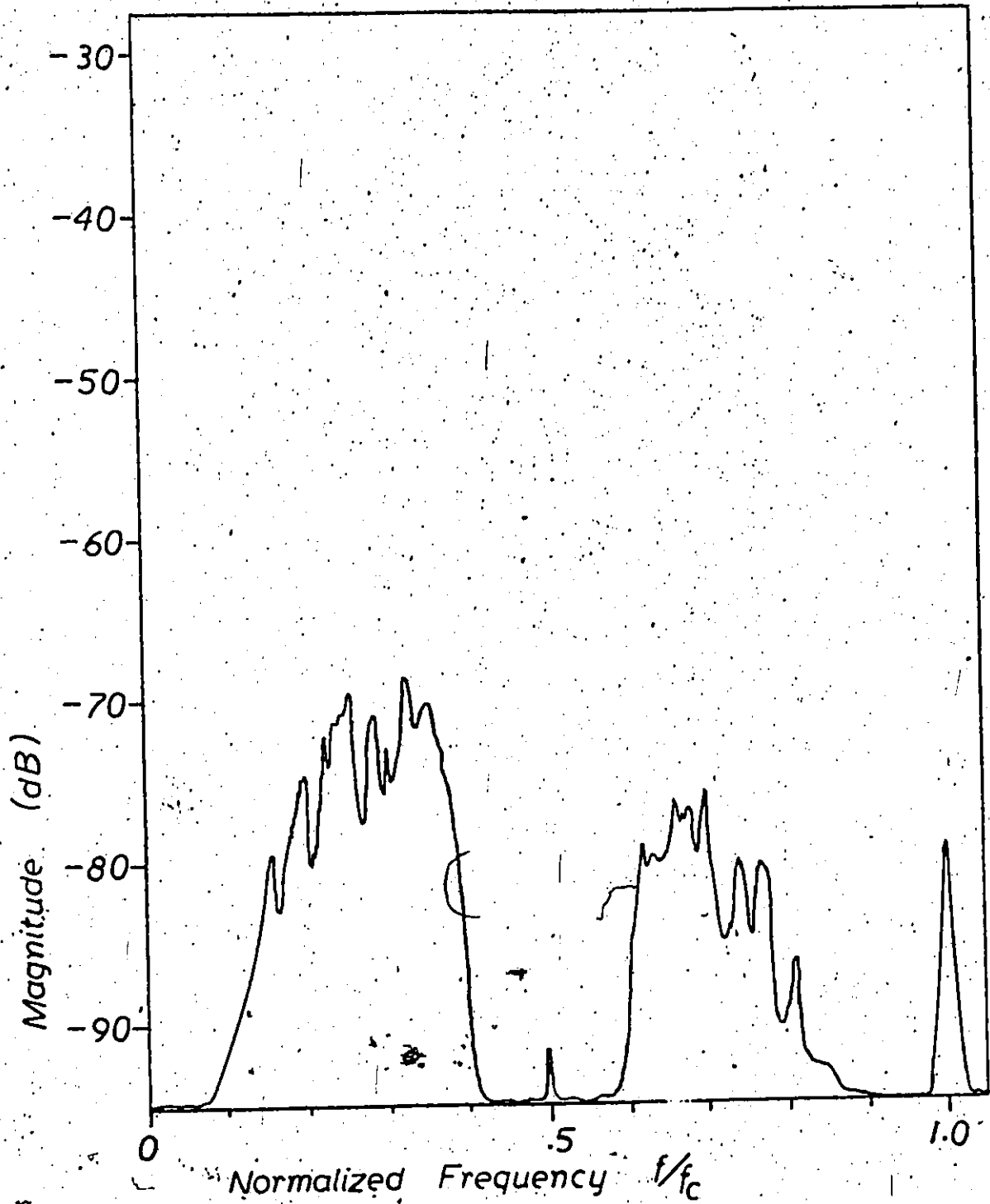


Figure 5.6 Bandpass Filter Output Noise Spectrum

dynamic range available from this filter is 70 dB, under the above conditions. If greater harmonic distortion is tolerable for a given application then the dynamic range can be increased accordingly.

The output noise spectrum has the same shape as the output response of the bandpass filter. This suggests that the major source of noise was introduced at the device input, since the noise spectrum is being filtered in the same manner as an input signal. The most likely origin of this noise was through the ground connection to the input source diffusion of the CCD.

The output component at the clock frequency, shown in figure 5.5 for the CCD output, has been suppressed considerably in the filter output, shown in figure 5.6. This will always be the case for filter designs which do not pass dc, since the clock frequency lies in the stopband region of all such filters.

CCD TRANSVERSAL FILTER (SPLIT ELECTRODE WEIGHTING)

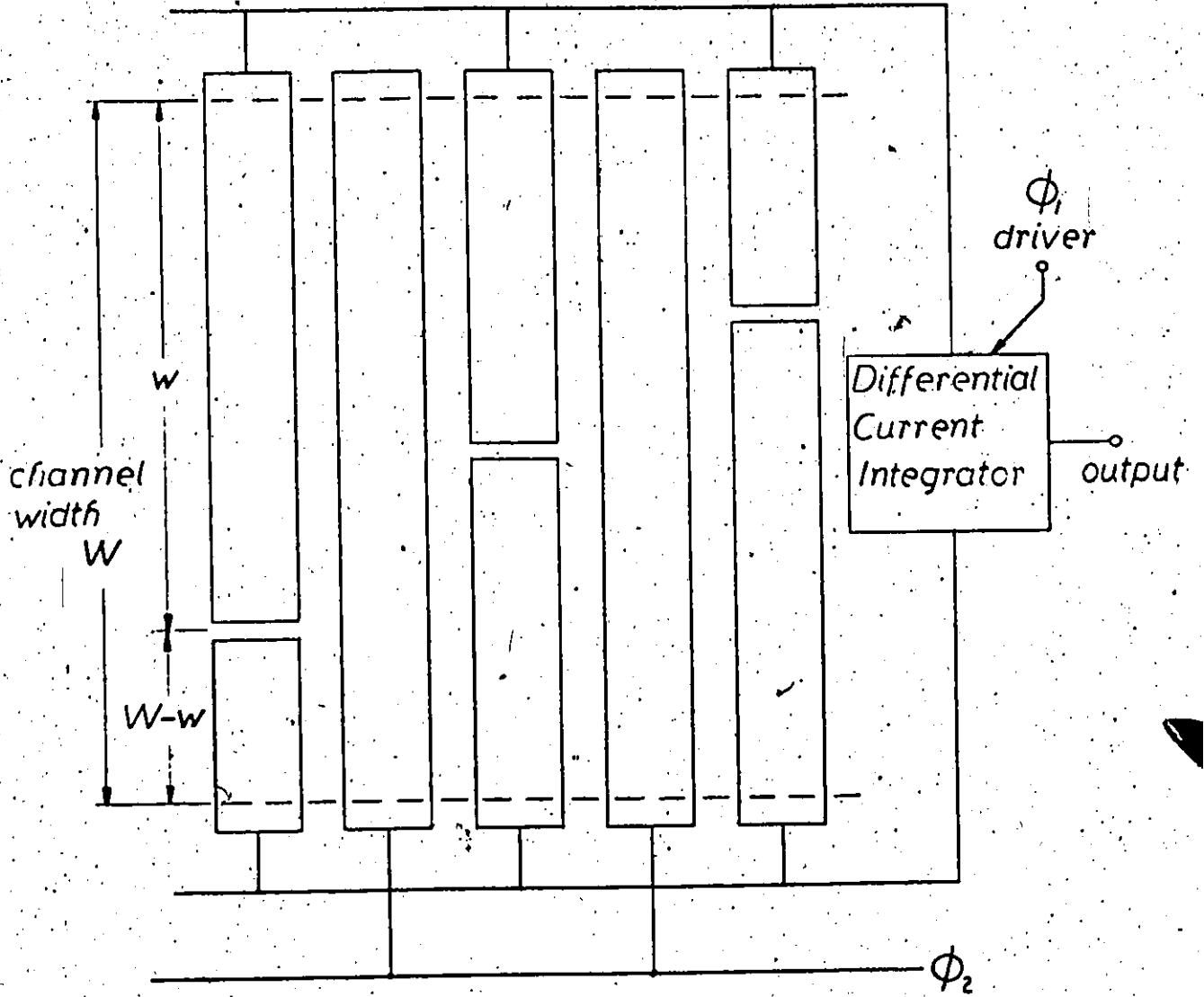
6.1 GENERAL

The split electrode technique is a method of implementing filter design with fixed coefficient values. It was introduced by D.R. Collins et al [23] using a three-phase CCD. The transfer function of the filter is determined on chip by the position of gaps in the CCD electrodes.

6.2 OPERATION

The split electrode structure is shown schematically in figure 6.1. For simplicity, only the storage electrodes are shown in the figure. The ϕ_1 phase is used for the sensing operation. Since the storage electrode, oxide, and silicon surface form a parallel plate capacitor, the amount of charge on the electrode is proportional to the amount of charge (representing the signal sample) stored in the substrate below. If the electrode is split, then a weighted value of the signal charge proportional to the area partitioned by the gap position is obtained. By finding the difference in charge on each side of the gap, it is possible to also have negatively weighted coefficients. If the i th

7



Note:
Transfer electrodes
not shown

Figure 6.1 Schematic of the Split Electrode Technique

electrode is split at a position w along its width, then the value of the i th coefficient will be proportional to the fraction of the electrode area from 0 to w , minus the fraction of the area from w to W as shown in figure 6.1.

$$h_i = w_i / W - (W - w_i) / W = 2k_i - 1 \quad 6.1$$

where W = channel width

$$k_i = w_i / W$$

Thus the values of h_i can range from -1 to $+1$ as the value of k_i ranges from 0 to 1. A gap in the middle of the electrode represents a coefficient value of 0. The storage electrodes of the ϕ_1 phase are tied to two common lines $\phi_1(+ve)$ and $\phi_1(-ve)$. These two buses are connected to a differential current meter/integrator to determine the difference in charge flowing into the two ϕ_1 clock lines and produce the required filtered signal.

The advantage of this technique is that all of the weighting and most of the summing operations are conveniently performed on the CCD chip. All that is required externally is a single integrator-difference amplifier to produce the required output. However, there are few practical methods which can be used to measure and integrate the current flowing in the CCD clock lines. Charge transfer occurs only during the fall time of the driving clock pulses so that the bulk of the current flow occurs only for a very short duration (a few nanoseconds). Furthermore the

magnitude of this current is very small so that an accurate integration and differencing amplifier would be difficult to implement. One method which has been used [23,24] is the following. Two identical driving capacitors are connected to $\phi_1(+ve)$ and $\phi_1(-ve)$ and precharged to equal levels. After the charge transfer has been completed the difference in the two capacitor voltages is proportional to the difference in charge on the two sides of the ϕ_1 storage electrodes. A high input impedance difference amplifier is then required to produce the voltage difference representing the filtered output signal.

The devices employed in this study used a similar method, floating gate sensing [25], to produce a voltage change on the storage electrode proportional to the charge transferred to that stage. Since all of the ϕ_1 storage electrodes are connected to the two common lines $\phi_1(+ve)$ and $\phi_1(-ve)$, the contribution of all of the electrodes can be summed simultaneously by using these lines. This implementation is shown in figure 6.2a. The change in output voltage due to any one of the split electrode stages will depend partially on the loading due to the other electrodes plus any other associated capacitances. This loading must be examined carefully to determine its effects on the values of the filter coefficients. The capacitances associated with the $\phi_1(+ve)$ side of the storage electrodes are shown in figure 6.2b.

Initially, only the charge flowing in the i th stage is considered in order to determine its influence on the output, based on the loading from the other $(N-1)$ stages and the load capacitance. This is a linear model with the depletion capacitance represented by its average value.

When a charge $k_i q_i$ is transferred under the $\phi_1(+ve)$ side of the storage electrode it causes a voltage change at the surface

$$\Delta V = -k_i q_i / C_{T_i}^+ \quad 6.2$$

$$\text{where } C_{T_i}^+ = \frac{(C_{E_i}^+ + C_L^+) k_i C_{ox}^+}{C_{E_i}^+ + C_L^+ + k_i C_{ox}^+} + k_i C_d$$

= total capacitance seen by charge $k_i q_i$

$$C_E^+ = \frac{C_{ox} C_d}{C_{ox} + C_d} \sum_{i=1}^N k_i$$

= total capacitance of $\phi_1(+ve)$ electrodes

$$C_{E_i}^+ = C_E^+ - k_i \frac{C_{ox} C_d}{C_{ox} + C_d}$$

= loading capacitance on i th stage from remaining $(N-1)$ electrodes

C_{ox} = oxide capacitance of one storage electrode of area = WL

C_d = depletion capacitance of one storage electrode

C_L^+ = load capacitance

k_i = w_i / W
= fraction of i th ϕ_1 storage electrode connected to $\phi_1(+ve)$

The resulting voltage change on the storage electrode is obtained by considering the voltage division on the circuit capacitances

$$\Delta V_i^+ = \frac{1/(C_{E_i}^+ + C_L^+) \Delta V}{1/(C_{E_i}^+ + C_L^+) + 1/k_i C_{ox}} = \frac{k_i q_i C_{ox}}{(C_{E_i}^+ + C_L^+) (C_{ox} + C_d) + k_i C_{ox} C_d} \quad 6.3$$

substituting for $C_{E_i}^+$

$$\Delta V_i^+ = \frac{k_i q_i C_{ox}}{(C_E^+ + C_L^+) (C_{ox} + C_d)} \quad 6.4$$

The same analysis applies to $\phi 1$ (-ve), except that k_i is replaced by $(1-k_i)$ and C_E^+ and C_L^+ are replaced by C_E^- and C_L^- . This yields

$$\Delta V_i^- = \frac{(1-k_i) q_i C_{ox}}{(C_E^- + C_L^-) (C_{ox} + C_d)} \quad 6.5$$

The output obtained from the voltage difference $\phi 1$ (+ve) - $\phi 1$ (-ve) is then

$$V_o = \frac{C_{ox}}{C_{ox} + C_d} \left(\frac{\sum_{i=1}^N k_i q_i}{(C_E^+ + C_L^+)} - \frac{\sum_{i=1}^N (1-k_i) q_i}{(C_E^- + C_L^-)} \right) \quad * \quad 6.6$$

Since $h_i = 2k_i - 1$, the correct transfer function is obtained only when $(C_E^+ + C_L^+) = (C_E^- + C_L^-)$. The two load capacitances C_L^+ and C_L^- will normally be equal if similar output MOST's are used on each side. However, the electrode

* Note: The dynamic range of this output will be limited by the non-linearity of C_d and C_E . V_o can be linearized by making C_L the dominant capacitance.

capacitances C_E^+ and C_E^- are not necessarily identical since their values depend on the coefficients of the designed filter. A special case arises for any filter $H(\omega)$ such that $H(\omega)|_{\omega=0} = 0$ (i.e. bandpass filter, high pass filter, differentiator, Hilbert transformer, etc.). For this class of filters $\sum_{i=1}^N h_i e^{j0} = \sum_{i=1}^N h_i = 0$ so that

$$C_E^+ = C_E^- = \frac{C_{ox} C_d}{C_{ox} + C_d} \quad 6.7$$

Thus the loading on each side of the ϕ_1 electrodes will be equal and the filter transfer function can be implemented directly. For filters that pass dc (i.e. lowpass filter) it will be necessary to readjust the k_i values or else add extra capacitance to one of the two C_L 's until the terms $(C_E^+ + C_L^-)$ and $(C_E^- + C_L^+)$ are equal.

6.3 RESULTS

The split electrode technique with floating gate sensing was used to implement a 24-tap lowpass filter [22], the same design used with the external weighting method described in section 5.3. The output response for this filter is shown in figure 6.3. The measured results show excellent agreement with the calculated response in the passband region with some differences showing up in the

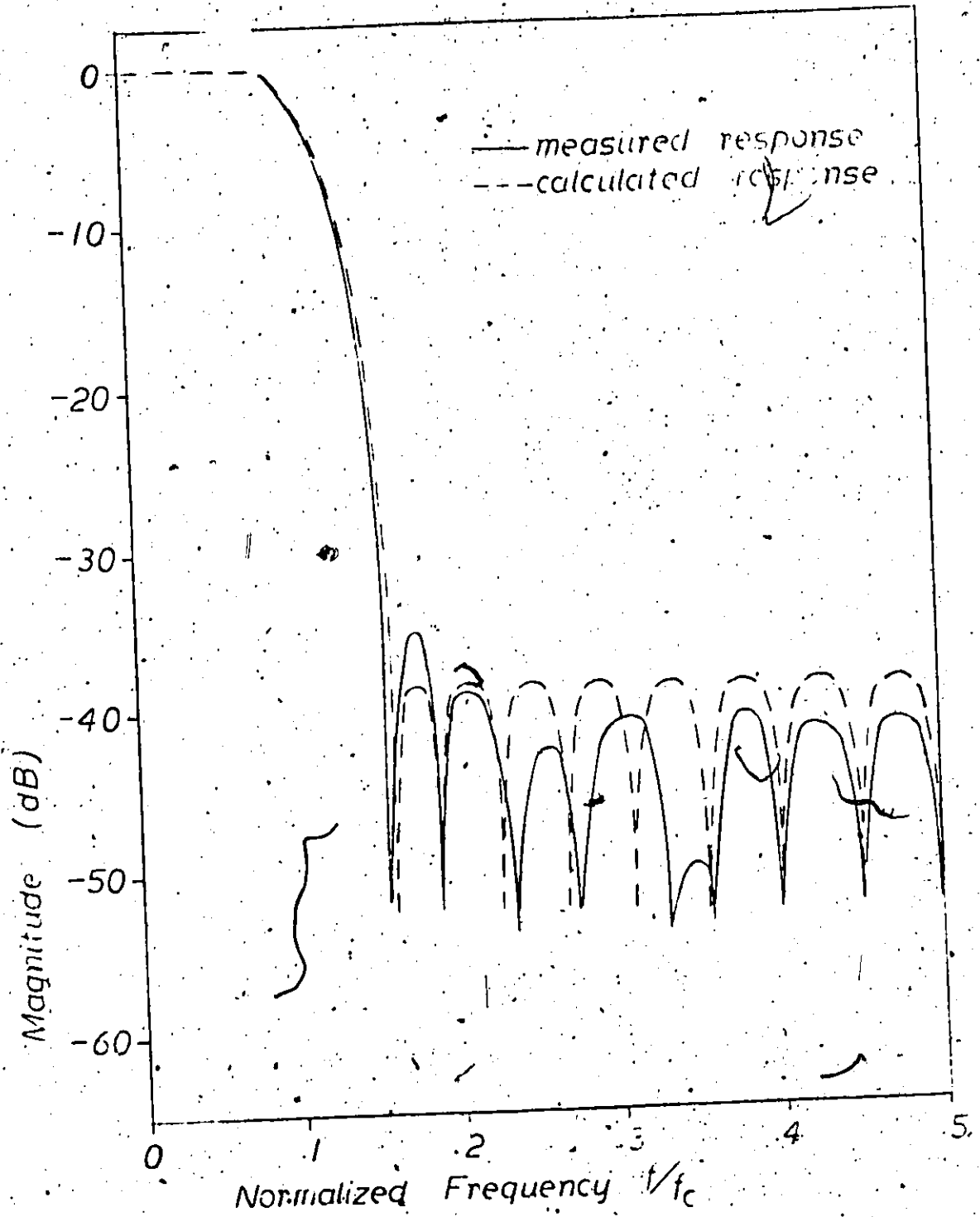


Figure 6.3 Output Response- 24-Tap Lowpass Filter

stopband. This particular filter was designed for use with the current sensing technique and was not optimized in any way for the floating gate sensing. Also since it was a lowpass design, the loading on each side of the $\phi 1$ storage electrodes was not equal and had to be compensated externally by applying more gain to the $\phi 1(+ve)$ side of the output. Furthermore the coefficients were not modified in any way to compensate for the transfer inefficiency of the device. It is thus very difficult to comment on the practical limits imposed by this technique. The results obtained for the 2nd-tap lowpass filter were very encouraging. It is contemplated that a much more difficult filter design could be implemented by taking the above factors into account.

6.4 CASCADING SECTIONS

It is known from the results of digital filter work that a given filter design is less sensitive to coefficient errors when implemented as a series of cascaded lower order filters, rather than as a single transversal filter. This is directly applicable to CCD filters. If a single filter structure is limited to some value of stopband attenuation (x dB) due to coefficient inaccuracies, then a filter implemented with n sections should be able to achieve a

stopband attenuation of n dB. The number of coefficients required in any one stage will be determined by the passband ripple and rolloff requirements of the overall filter specifications.

It would then be very useful to be able to cascade filter sections directly without the use of external amplifiers between stages. The split electrode method with floating gate sensing produces two output levels whose difference represents the desired filtered signal. If external circuitry is to be eliminated between sections then an analog subtractor must be implemented which is compatible with the CCD structure. A simple method of finding the difference signal at the input of the next filter stage is shown in figure 6.4. It is essentially the same as the potential equilibrium methods discussed in section 2.2, except that first gate G_1 is connected to $\phi 1(-ve)$ and the second gate G_2 is connected to $\phi 1(+ve)$. Note that if these two inputs are equal then charge is still injected into the first stage, depending on the difference in threshold voltages of the first two gates. This is necessary since the CCD signal input must be offset to accommodate inputs with both positive and negative excursions. The final surface potential during each sampling interval is determined by the voltage on G_1 as discussed in section 2.2. Since in this case the gate G_1 is controlled by a varying input signal and not a constant amplitude pulse, this simple input method

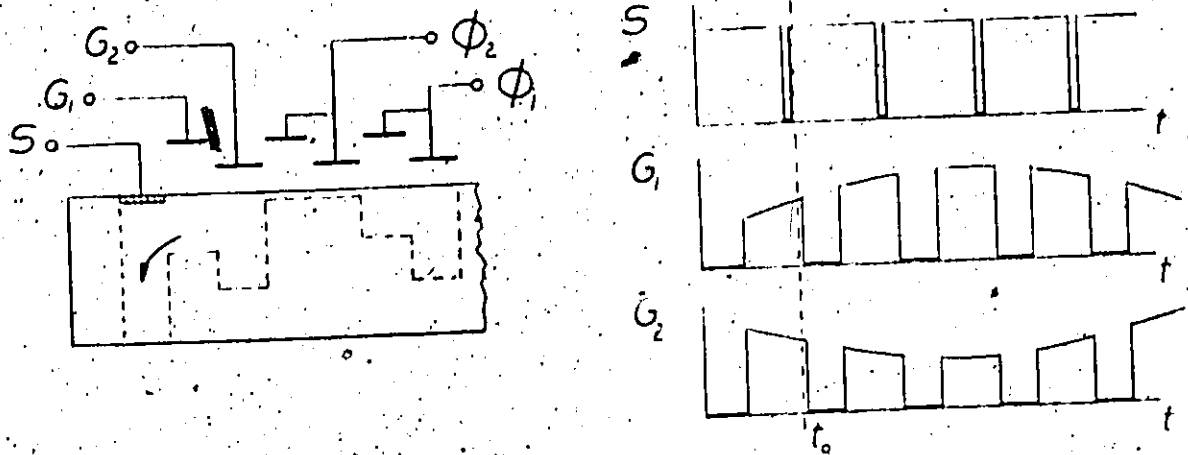


Figure 6: " Difference Signal Input

will not be completely linear. This will limit the dynamic range available to the succeeding filter stage.

A more suitable method can be implemented by fabricating both input gates on the same level. This improves the linearity of the input (see equation 2.5). More circuitry is then required to add the fat zero and signal offset required to accommodate both positive and negative excursions of the input signal.

CONCLUSIONS

The implementation of transversal filters using charge coupled devices has been described in the preceding chapters. The concepts of CCD operation and of sampled data transversal filters have been introduced to provide the necessary background in the two diverse fields of silicon device technology and signal processing. Results from two different methods of CCD implementation have been presented. The relative merits of these two approaches, as well as CCD filtering in general will now be discussed.

The two-phase polysilicon gate technology has been shown to be a valid method of implementing CCD filters. It was adapted to both the voltage sensing technique and to the split electrode method. The two-phase driving clock required for these CCD's is simpler to generate than the three-phase clock required for the single level structure. The experimental devices were found to have a useful dynamic range in excess of 70dB, adequate for the filter designs tested. Further improvement in dynamic range can be achieved by optimizing the input gate structure to improve the linearity of the charge injection (section 2.2) and by limiting the introduction of noise. The latter can be accomplished by isolating the input elements from the rest of the system (section 5.3).

The design of sampled data transversal filters, outlined in chapter 3, involves choosing a number of parameters such as clock frequency (f_c), and the number of stages per delay section (M). To avoid aliasing in the system, the folding frequency of the filter response ($1/2T$) must be at least as great as the highest frequency component of the input signal. As the folding frequency is further increased, the filter design tends to become more complex and more sensitive to coefficient error. [26]. However the translated basebands of the sampled data system become more removed from the desired baseband signal spectrum and reconstruction of the output signal is simplified. By keeping the delay (T) constant and increasing M , the filter response is unaltered, but the sampling rate is increased. This simplifies signal reconstruction without increasing the sensitivity of the filter design. This was illustrated in figure 3.7 for the case of a sample and hold output where the baseband rolloff, and higher band suppression were both improved by increasing the value of M . It must be emphasized that the folding frequency of the filter response remains at $1/2T$ regardless of the value of M . It is therefore necessary that the input signal be bandlimited to $1/2T$ to prevent the inclusion of out of band signals in the output.

The addition of a cascaded output filter was discussed as a further improvement to signal reconstruction. By clocking this unit at some multiple (K) of the main filter

clock frequency, it is possible to increase the separation of the unwanted upper bands from the desired baseband signal. The designer can choose values of f_c , M , and N (chapter 3) to provide the best compromise in filter order, sensitivity, CCD length, and ease of signal reconstruction for any given application.

The length of the CCD used is limited by the transfer efficiency of the device. When the value of the product of the number of stages and the transfer inefficiency ($k\epsilon$) exceeds 2, the MTF magnitude of the k th output is decreased to almost zero as was shown in figure 4.1. If the attenuation is not too severe, it is possible to invert the dispersive effects of transfer inefficiency by modifying the coefficients according to equation 4.13, provided that the value of ϵ can be predicted with sufficient accuracy. The product ih_i in the summation of equation 4.14 suggests that the sensitivity of the transfer function to ϵ can be reduced by having the large coefficients at the beginning of the filter. It would thus appear advantageous to use minimum phase rather than linear phase designs since the former tends to have the large coefficients at the beginning of the filter whereas the latter is a symmetrical filter with the large coefficients near the middle of the structure.

The first filter implementation presented was the voltage sensing technique. This is a flexible method since it can be used to implement any kind of transversal filter

by connecting the appropriate external summing network. An external output is available at each stage of the device making it possible to monitor the CCD signal at each delay interval. This facility made it very useful as a test device.

As a practical method of filter implementation the voltage sensing CCD has several disadvantages. It requires a large package to accommodate all of the outputs, and extensive external circuitry to perform the required summation of the delayed signals. The output signal levels are dependent to some extent on substrate bias and signal voltage offset, thus limiting the accuracy which can be maintained in realizing the filter coefficients. It was suggested that the sensitivity of the filter to coefficient variations could be reduced by cascading lower order sections. This can be done with the voltage sensing CCD, but requires an external summing network and amplifiers for each section making the overall implementation more involved.

The voltage sensing technique would be used in applications which require the flexibility available with this method such that the cost of implementation can be justified. One possible application would be a programmable filter used as an adaptive channel equalizer. In this case the tap values would be set dynamically while data is being received to minimize intersymbol interference. Since the taps are set using a feedback configuration the sensitivity

of the filter. to the operating parameters of the CCD would not be a problem as in the case of an open loop system.

The second filter implementation presented was the split electrode technique. This is a fixed filter method since the transfer function obtained cannot be changed without altering the electrode structure of the CCD. This approach is well suited to the production of large quantities of fixed filter designs. A large initial investment is required for the mask design which can be offset by large volume production. The resulting filters using the split electrode technique require a comparatively small amount of external circuitry since all of the summing is done on chip. The filters are also less susceptible to variations in operating voltages of the CCD since such parameter variations affect both sides of the electrode structure equally.

The coefficient accuracy available is limited by the precision with which the position of the gaps in the electrode structure can be determined. This places an absolute tolerance on the coefficient accuracy such that the second model, (3.8), discussed in section 3.2 is applicable. Equation 3.14 can be used to obtain an estimate of the coefficient tolerance required to achieve a given attenuation level. If the accuracy proves unsuitable for a particular filter design the filter can be redesigned using cascaded lower order sections. The split electrode CCD is

better suited to cascading sections than the voltage sensing device since no external connections are required. This was outlined in section 6.5.

More work is required in developing the split electrode method. More data must be obtained from other filter designs to determine the available accuracy of the coefficient values which can be realized with this technique. The methods of cascading sections must be analyzed in terms of device operating voltages so that a CCD can be designed which has compatible input and output signal levels.

APPENDIX

CCD TEST SET

A test set [27] was constructed to facilitate testing of the CCD filter circuits. The set produces the two-phase overlapping clock waveforms ($\phi 1$ and $\phi 2$) required to drive the two-level CCD's used. Separate controls are available for the $\phi 1$ clock width (T1), $\phi 2$ clock width (T2), $\phi 1$ overlap (L1), and $\phi 2$ overlap (L2). In addition, a number of extra waveforms are generated for use as stroke pulses, reset pulses, etc.

The three auxiliary pulses (ϕx , ϕy , ϕz) are each provided with separate delay and pulse width controls. They can be triggered by the leading edge of $\phi 1$ or of $\phi 2$.

The circuit diagram for this test set is shown in figure A1. It uses TTL logic for the pulse generation and output drivers (NS MH026) are used to provide the voltage levels required for the CCD circuits. Two monostable multivibrators, 74121-1 and 74121-2, are connected as a free running oscillator and control the pulse widths of $\phi 1$ and $\phi 2$. The \bar{Q} outputs from these units trigger two other monostable multivibrators, 74121-3 and 74121-4, which control the overlap times of $\phi 1$ and $\phi 2$. The Q outputs from 74121-1 and 74121-2 are used to trigger the auxiliary pulses ϕx , ϕy and ϕz . A two-position origin switch is used to enable one of the two Q signals to the trigger input of each

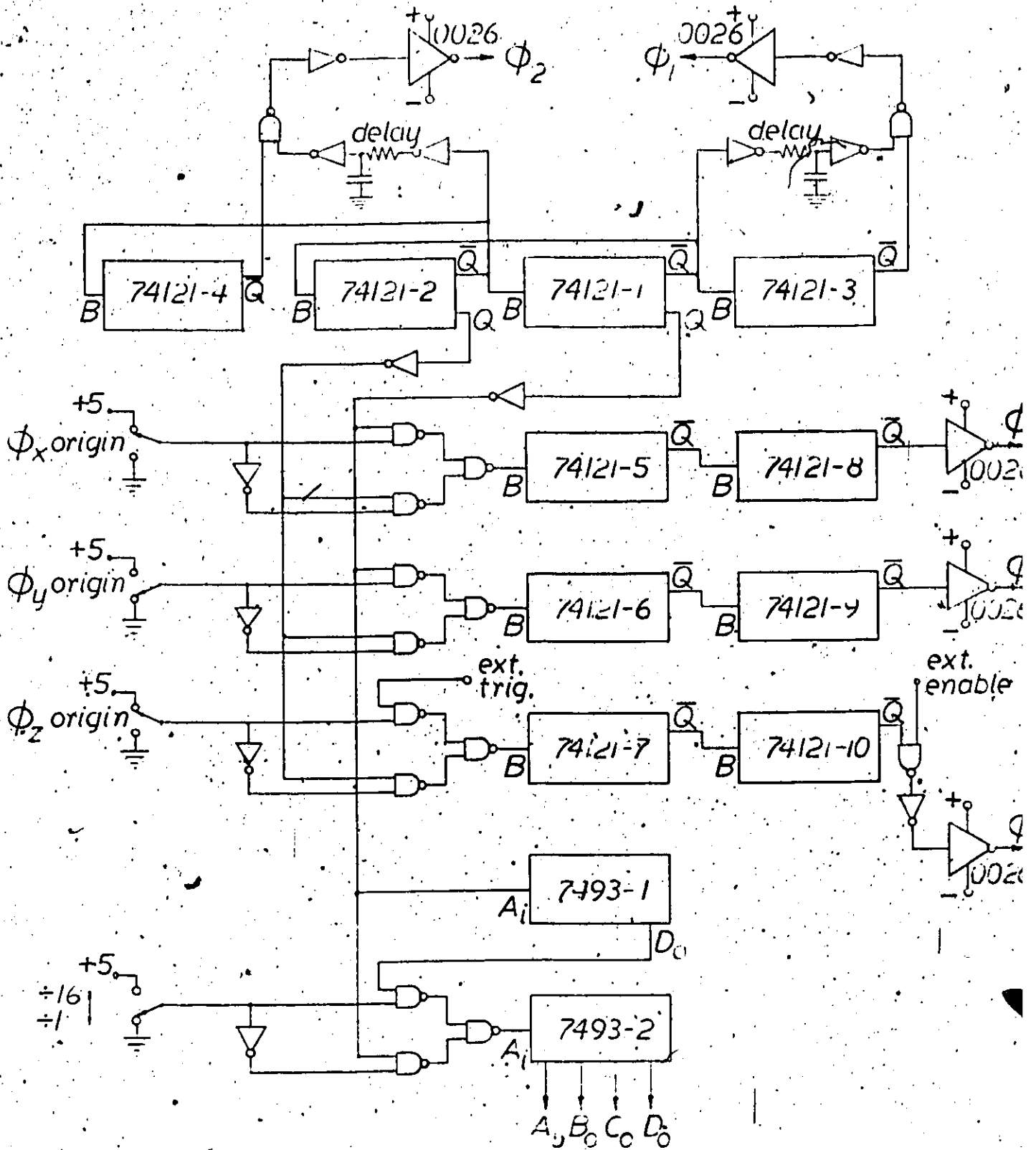


Figure A1 CCD Test Set Circuit

auxiliary pulse. Monostable multivibrators are used again to provide a controllable delay (74121-5 to 74121-7) and also a controllable pulse width (74121-8 to 74121-10) for each auxiliary pulse. The waveform ϕz has externally available trigger and enable inputs which can be used in conjunction with other waveforms produced by the test set, to provide some form of word generation for testing purposes. Two counters, 7493-1 and 7493-2 provide TTL level waveforms which can be used for scope triggering or with ϕz for bit pattern generation. The timing diagram for this test set is shown in figure A2.

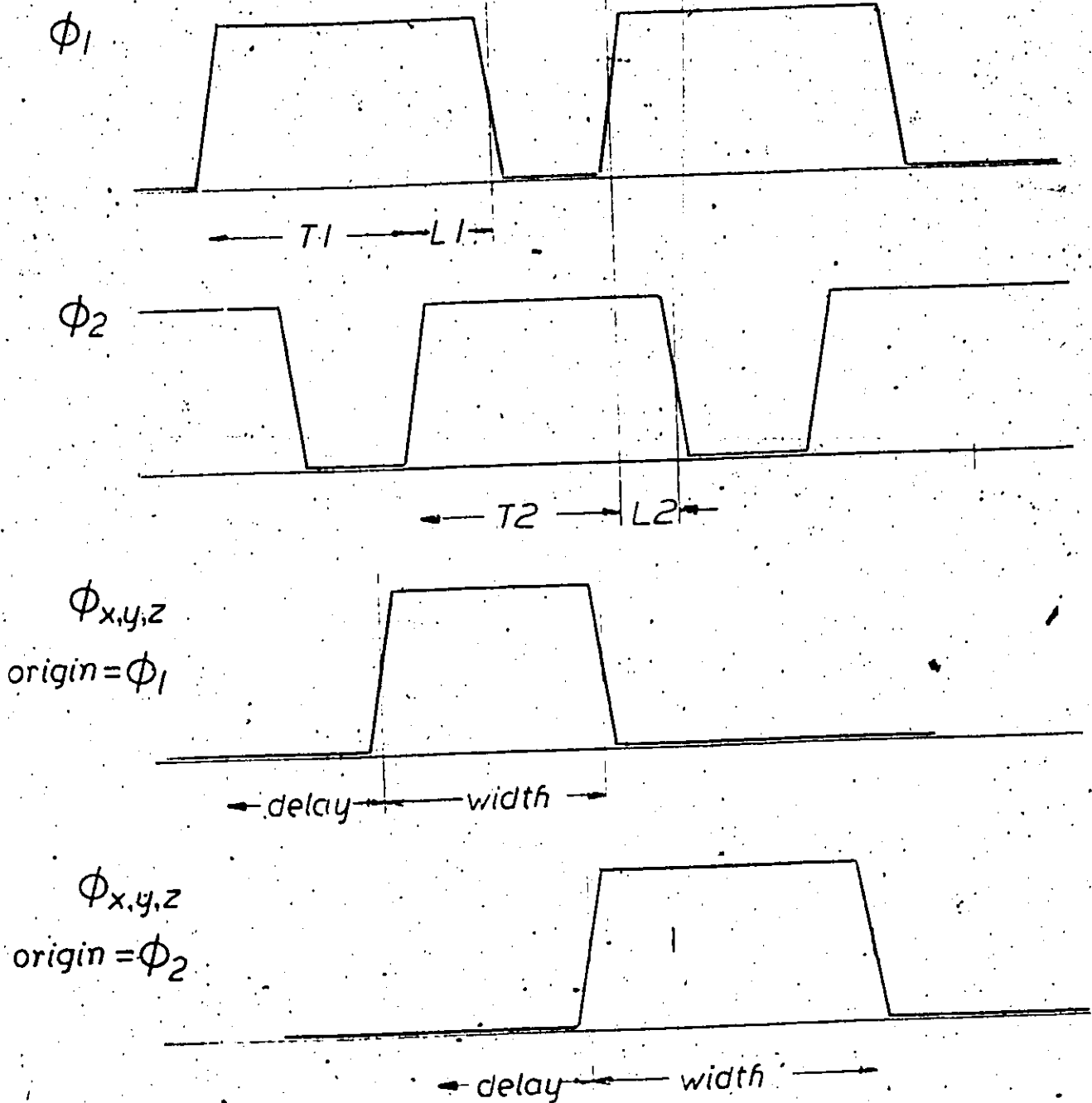


Figure A2 CCD Test Set Timing Diagram

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