ACTIVE TUNING ELEMENTS FOR INTEGRATED BROADCAST FREQUENCY RECEIVERS

by

C. S. Yap

Submitted in partial fulfillment of the requirements
for the degree of Master of Science

Department of Electrical Engineering,
Faculty of Pure and Applied Science,
The University of Ottawa,
Ottawa, Canada

ACTIVE TUNING ELEMENTS FOR INTEGRATED BROADCAST FREQUENCY RECEIVERS

ABSTRACT

Recent developments in phase-locked loop systems have permitted the complete integration of broadcast receivers, except for antenna tuning. This thesis investigates techniques, for tuning the antenna, which are compatible with integrated circuit technology. In particular, forms of immittance converter are studied and their performance evaluated in relation to the above application. It is concluded that a new current-amplifier form of positive immittance converter provides a reasonable compromise between the requirements of the tuning system and the integrated circuit technology.

ACKNOWLEDGEMENT

The author wishes to express his sincere thanks to his thesis supervisor Professor P. M. Thompson for his patient guidance and encouragement in the preparation of this thesis, Mr. W. Peil of the General Electric Company, Advanced Research Laboratory, Syracuse, N.Y. for the formulation of the problem investigated and Mr. J. G. Mlacak of Bell Northern Research for encouragement in completing the thesis while the author was employed by his company.

LIST OF SYMBOLS

A	one amplifier immittance amplifier feedback factor
B	total loop gain of an immittance converter
D_p, D_n	diffussion constants for holes and electrons respectively
f_o, ω_o	resonant frequency of a total tuning system
g	conductance
g_{11}, g_{22} g_{21}, g_{12}	are g parameters of a two port network
G_I	current amplifier gain
G_V	voltage amplifier gain
i_1	small signal input current
i_o	small signal output current
I_1	input current at port 1 etc.
I_B	transistor base current
I_C	transistor collector current
I_o'	diode saturation current
k	1.38×10^{-23} joule/°K, Boltzmann's constant
K	a constant equals to $\frac{kT}{q}$
L	inductance
L_n	diffussion length of electrons in P-region
L_p	diffussion length of holes in N-region
M	gain of current attenuator
n_{po}	donor carrier density in the P-region
p_{no}	acceptor carrier density in the N-region

q	1.6×10^{-19} coulomb, electron charge
Q	Q-factor of a tuned circuit
r	resistance
r_1	input resistance of amplifier
r_L	series loss of antenna
r_o	output resistance of amplifier
r_p	total resistance at the shunt port of an immittance converter
r_{se}	total resistance at the series port of an immittance converter
t_d	time delay in a complete feedback loop of an immittance converter
v_1	small signal input voltage
v_o	small signal output voltage
V_1	input voltage at port 1 etc
Y_1	admittance measured at port 1 etc
Y_L	load admittance
Y_o	output admittance
Y_{11}, Y_{12} Y_{21}, Y_{22}	are admittance parameters for a two port network
y_{11}, y_{12} y_{21}, y_{22}	modulus of the respective Y parameters
Z_1	impedance measured at port 1 etc
Z_L	load impedance
Z_o	output impedance etc.
α	current gain of a transistor in the common base connection
β	current gain of a transistor in the common emitter connection

τ_β minority carrier life time in the base of a transistor

τ_η minority carrier transit time through the base of a transistor

θ phase delay angle in a complete feedback loop of an immittance converter

TABLE OF CONTENTS

LIST OF FIGURES

Page

LIST OF TABLES

INTRODUCTION

The development of integrated circuit technology is having a profound effect on the design of integrated receiving systems. The conventional tuning systems of discrete component receivers are being replaced by systems where the overall bandwidth is determined at the detector (ref. 0.1, 0.2, 0.3). However, amplification is found to be desirable between the antenna system and the detector and intermodulation distortion can be introduced if large interfering signals are present. This interference can be reduced by antenna tuning and this thesis is concerned with integrated circuit methods for its implementation.

Several forms of antenna systems are suitable for broadcast receivers, but the tuned ferrite rod is presently the most economical. The antenna must always be tuned to the same frequency as the detection system, so tracking is an important consideration in the choice of a tuning system. Because integrated receiver systems must contain amplifiers, they are also a good choice for the tuning system. Thus the thesis will consider the design of active circuit tuning systems for ferrite rod antennas, within the constraints of integrated circuit batch of fabrication technology.

Active circuit tuning systems contain amplifiers which change the immittance of one element of a tuned circuit

as presented to another. The amplifiers are connected in a feedback configuration and because the batch fabrication implies that they are not compensated, system stability is an important design consideration. For this reason, the thesis will depart from the more conventional active network synthesis approach, in favour of one more related to control theory. All elements will be treated as imperfect transducers in a feedback loop and the immittances at input ports derived on this basis.

Chapter 1 presents the theory of immittance converter in two approaches. The first approach uses the classical network theory. The second uses an approach based on control philosophy. Using the second approach several forms of immittance converter are developed. Chapter 2 presents receiving systems with active tuning elements using phase locked-loop techniques and shows possible ways of tracking the antenna with the local oscillator. Chapter 3 deals with the circuit realizations of the immittance converters. Chapter 4 presents the results and performance characteristics of immittance converter employed to tune antennas. The thesis concludes with the results achieved and an indication of which forms of immittance converter are most promising for antenna tuning systems.

CHAPTER 1

THEORY OF IMMITTANCE CONVERTERS

1.0 Introduction

In this chapter immittance converters are considered, using two separate approaches. First, it is treated as a two port network using classical active network theory (ref. 1.1 - 1.9). This treatment develops a description of the port characteristics of a converter without reference to the practical realization. However, the converter is realized as a feedback circuit and the second treatment approaches immittance converters more from the point of view of control theory. The converter is considered as a system of transducers and an immittance is a voltage to current, or current to voltage transducer, with the input and output at the same port. Then the introduction of amplifiers into the system can change the magnitude and sign of the immittance as measured at the input-output port.

1.1 Classical Active Network Theory Approach

In classical network theory, the immittance converter is considered as a two port linear active network as shown in Fig. 1.1, together with the positive sign and direction for the voltages and currents at the two ports. For an ideal immittance converter, the

immittance measured at one port is equal to the immittance at the other port multiplied by a constant which may be positive or negative.

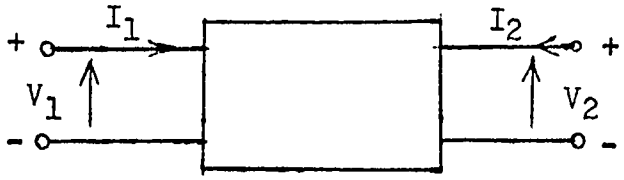


Fig. 1.1 A general two port network

For a general treatment, the voltages and currents at the two ports may be conveniently related by the g parameters method (1.10).

The hybrid g equivalent circuit is shown in Fig. 1.2.

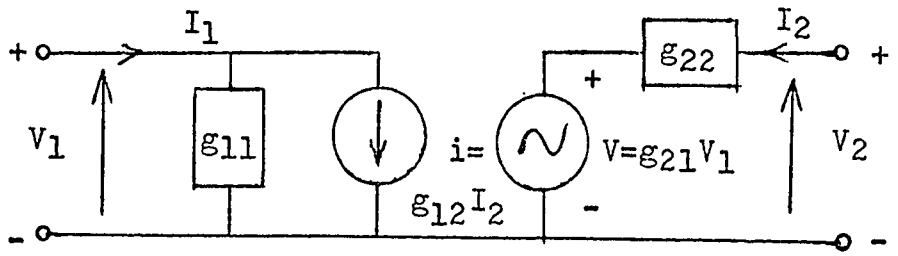


Fig. 1.2 Hybrid g equivalent circuit for a two port network

$g_{12}I_2$ is a current controlled source at port 1 and $g_{21}V_1$ is a voltage controlled source at port 2. The two ports are defined by

$$I_1 = g_{11} V_1 + g_{12} I_2 \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.1)$$

$$V_2 = g_{21} V_1 + g_{22} I_2 \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.2)$$

where the g parameters are defined by

$$g_{11} = \left.\frac{I_1}{V_1}\right|_{I_2=0} ; \quad g_{12} = \left.\frac{I_1}{I_2}\right|_{V_1=0}$$

$$g_{21} = \left.\frac{V_2}{V_1}\right|_{I_2=0} \& \quad g_{22} = \left.\frac{V_2}{I_2}\right|_{V_1=0}$$

g_{12} and g_{21} are dimensionless current and voltage ratios, and g_{11} has the dimension admittance and g_{22} of impedance. If port 2 is terminated with a passive load Z_L, according to the sign defined in Fig. 1.2.

$$Z_L = -\frac{V_2}{I_2} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.3)$$

Solving 1.1, 1.2 and 1.3, the admittance measured at port 1

$$Y_1 = \frac{I_1}{V_1} = g_{11} - \frac{g_{12}\, g_{21}}{Z_2 + g_{22}} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.4)$$

If $g_{11} = 0, \quad g_{22} = 0 \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.5)$

$$Y_1 = -\frac{g_{12}\, g_{21}}{Z_2} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.6)$$

or $$Z_1 = -\frac{Z_L}{g_{12}\, g_{21}} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.7)$$

1.5 states the necessary and sufficient conditions for the two ports to be an ideal impedance converter.

If port 1 is terminated with an impedance Z_L, it

can be shown that the input impedance at port 2

$$Z_2 = g_{22} - \frac{g_{12} \cdot g_{21}}{g_{11} + 1/Z_L} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.8)$$

and $$Z_2 = - g_{12} \cdot g_{21} Z_L \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.9)$$

if the conditions for 1.5 are satisfied.

1.1.1 Immittance Converters

If $g_{11} = 0$, $g_{22} = 0$, g_{21} is positive and g_{12} is negative, the above becomes a positive immittance converter. These conditions are shown in Fig. 1.3. There is no inversion in voltage across or current through the load with respect to the voltage or current at port 1.

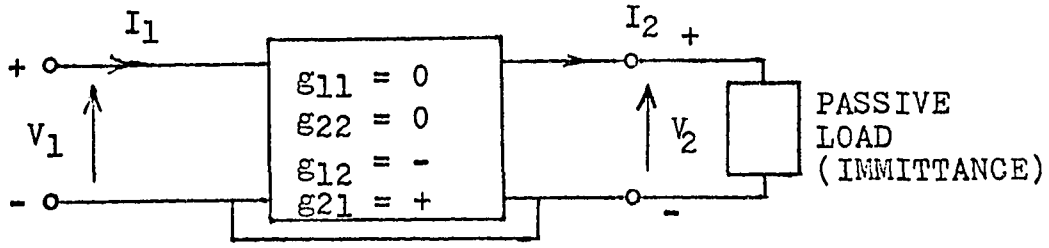


Fig. 1.3 An ideal positive immittance converter

1.1.2 Voltage Inversion Negative Immittance Converters

If $g_{11} = 0$, $g_{22} = 0$, g_{12} and g_{21} are negative, the above becomes a voltage inversion negative immittance converter. These conditions are shown in Fig. 1.4. There is no current inversion at either port but the voltage at port 2 is inverted with respect to that at port 1.

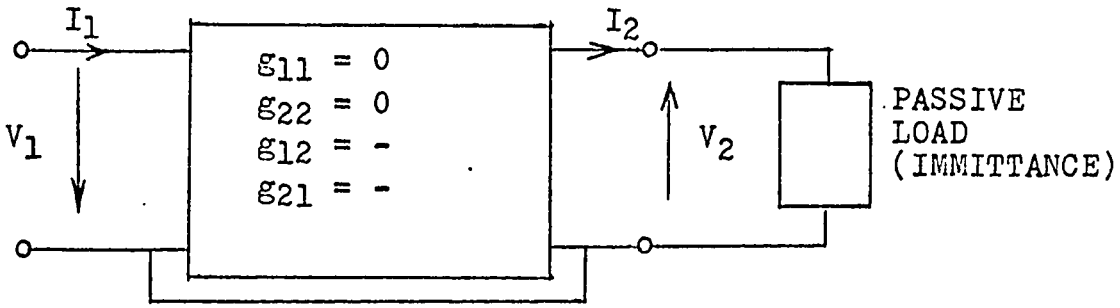


Fig. 1.4 An ideal voltage inversion negative immittance converter

1.1.3 Current Inversion Negative Immittance Converters

If $g_{11} = 0$, $g_{22} = 0$, g_{12} and g_{21} are positive, the above becomes a current inversion negative immittance converter. These conditions are shown in Fig. 1.5. There is no voltage inversion at either port, but the direction for the current I_2 through the load is opposite to that of I_1,

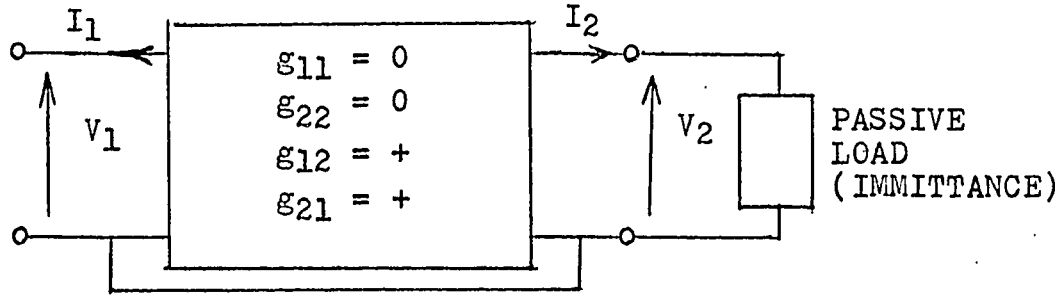


Fig. 1.5 An ideal current inversion negative immittance converter

In the above treatment, it is assumed that $g_{11} = g_{22} = 0$. In practical realizations, g_{11} and g_{22} are finite and their effects on Z_1 and Z_2 are seen from 1.4.

and 1.8. However, their values can be made zero at a single frequency by network compensation techniques.

1.1.4 Effect of Time Delay in High Pass Form

The amplifiers are imperfect i.e. g_{11} and g_{22} are finite, and all amplifiers introduce a time delay. Now consider the effect of g_{11}, g_{22} and the time delay on the overall system when the positive immittance converter is used to tune the ferrite rod antenna. High pass form (Fig. 1.6) is first considered in which port 2 is terminated with a capacitance C, and port 1 with an inductance L. Thus $Z_L = \frac{1}{j\omega c}$.

Because of delay $g_{12}{}^{\bullet}g_{21}$ can be written as

$$g_{12}{}^{\bullet}g_{21} = (g_{12}' - jx_{12})(g_{21}' - jx_{21})$$

$$= G_{12}e^{-j\theta_{12}} \; G_{21}e^{-j\theta_{21}}$$

$$= Be^{-j\theta} \quad \text{where} \quad B = G_{12}{}^{\bullet}G_{21}$$

$$\theta = \theta_{12} + \theta_{21} = \omega t_{d1} + \omega t_{d2}$$

t_{d1}, t_{d2} are time delays in the amplifiers.

$$g_{12}{}^{\bullet}g_{21} = B(1-j\theta) \text{ if } \theta \text{ is small} \quad \ldots\ldots\ldots\ldots\ldots \quad (1.10)$$

Substituting Z_L and 1.10 in 1.4

$$Y_1 = g_{11} + \frac{B(1-j\theta)}{1/j\omega c + g_{22}}$$

on normalizing the denominator and expanding

$$Y_1 = g_{11} + \frac{B(\omega C\,\theta + \omega^2 C^2 g_{22} + j\omega C - j\omega^2 C^2\,\theta\, g_{22})}{1 + (g_{22}\,\omega C)^2}$$

$$= g_{11} + \frac{B\omega C\,\theta}{1 + (g_{22}\,\omega C)^2} + \frac{B\omega^2 C^2 g_{22}}{1 + (g_{22}\,\omega C)^2}$$

$$+ \frac{j\omega CB}{1 + (g_{22}\,\omega C)^2} - \frac{j\omega^2 C^2 \theta g_{22}}{1 + (g_{22}\,\omega C)^2} \quad \ldots\ldots \quad (1.11)$$

$\frac{j\,\omega^2 C^2 \theta\, g_{22}}{1 + (g_{22}\,\omega C)^2}$ can be neglected. As $(g_{22}\,\omega C)^2 << 1$, 1.11 can be approximated as

$$Y_1 \simeq g_{11} + B\omega^2 C^2 g_{22} + B\omega C\,\theta + jB\omega C \quad \ldots\ldots\ldots\ldots \quad (1.12)$$

The first, second and third term of 1.12 represents the losses due to g_{11}, g_{22} and the delay respectively. None introduces a negative admittance, so the system is inherently stable. These losses merely reduces the system Q.

Let the total loss

$$g_t = g_L + g_{11} + B\omega C\theta + B\omega^2 C^2 g_{22} \quad \ldots\ldots\ldots \quad (1.13)$$

where $g_L = \frac{r_L}{w^2 L^2}$ the loss of the antenna. Fig. 1.7 is the equivalent circuit for Fig. 1.6.

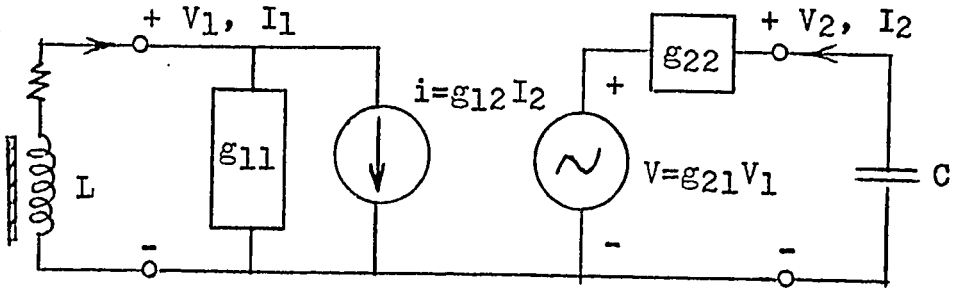


Fig. 1.6 An immittance converter used to tune a ferrite rod antenna (high pass form)

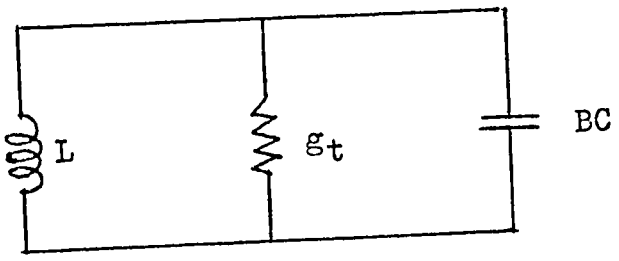


Fig. 1.7 Equivalent circuit of Fig. 1.6

The overall Q of the system

$$Q = \frac{1}{\omega L g_1} = \frac{\omega BC}{g_1} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.14)$$

and the resonant frequency

$$f_o = \frac{1}{2\pi\sqrt{LCB}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.15)$$

1.1.5 Effect of Time Delay in Low Pass Form

We will now examine the low pass form in which port 2 is terminated with the antenna L whose series loss is R_L. By the similar procedure as before

$$Y_1 = g_{11} + \frac{B(g_{22}+R_L)}{(R_L+g_{22})^2+\omega^2L^2} - \frac{B\omega L\theta}{(R_L+g_{22})^2+\omega^2L^2}$$

$$- \frac{j\omega LB}{(R_L+g_{22})^2+\omega^2L^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.16)$$

as $\omega^2L^2 >> (R_L+g_{22})^2$, 1.16 can be approximated as

$$Y_1 = g_{11} + \frac{B(g_{22}+R_L)}{\omega^2L^2} - \frac{B\theta}{\omega_L} - \frac{jB}{\omega_L} \quad \ldots\ldots\ldots\ldots \quad (1.17)$$

17 shows that the delay θ ($\theta = \omega t_d$) introduces a negative admittance $\frac{B\theta}{\omega L}$ which causes the system to be unstable.

1.2 Control Theory Approach

The voltage controlled source $g_{21}V_1$ and the current controlled source $g_{12}I_2$ in the Hybrid equivalent circuit of Fig. 1.2 can be partitioned as shown in Fig. 1.8 using a voltage amplifier and a current amplifier. This method of partitioning the controlled sources into voltage and current amplifiers leads to a convenient means of circuit realization.

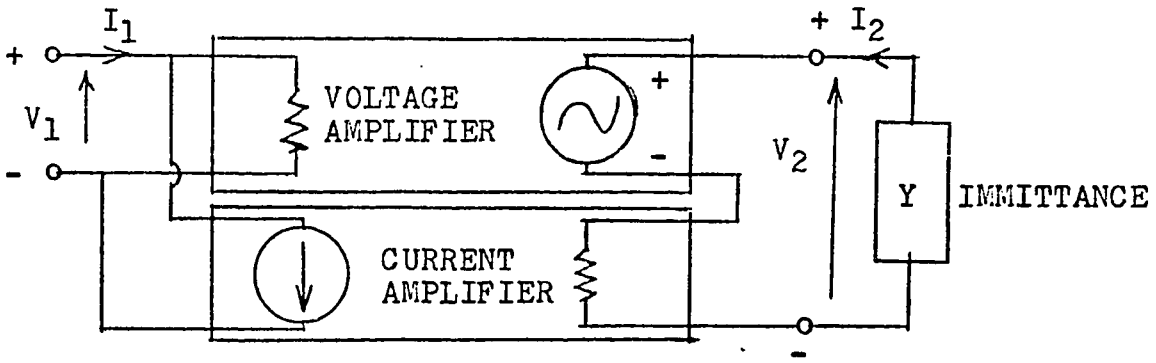


Fig. 1.8 An equivalent circuit of Fig. 1.2 when partitioned into a voltage and current amplifier

A feedback loop is formed if the two ports are terminated with immittances. Voltage applied at port 1 is amplified and becomes V_2 at port 2. The immittance terminated at port 2 will transform V_2 into a current I_2, which will be amplified and becomes I_1 at port 1, thus completing the feedback loop. Because of the existence of this feedback loop, control theory can be applied to advantage to determine its

terminal characteristics and system stability (ref. 1.11, 1.12, 1.13).

Every element within the loop is considered as a transducer. The immittances are considered as voltage to current or current to voltage transducers with the input and output at the same port. The following example will help to illustrate this point. A voltage controlled current source, such as a field effect transistor has a transfer admittance, which can be expressed as $\frac{i_2}{v_1}$. When the output port is connected in parallel with the input port, so that feedback is negative, as shown in Fig. 1.9, the input has the characteristic of an admittance $\frac{i_2}{v_1}$ as shown in Fig. 1.10. The input

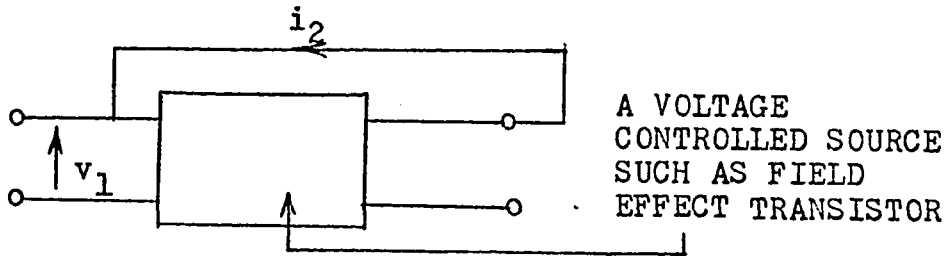


Fig. 1.9 A two port network arranged to have an input admittance

immittance is reciprocal, that is, for an input current there is a corresponding voltage and vice versa. Thus, it is

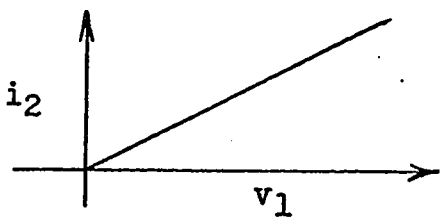


Fig. 1.10 Reciprocal relationship of I_2 and v_1

impossible to deduce, from input immittance measurements, whether the two port of Fig. 1.9 has a transfer admittance or a transfer impedance, or whether the device is voltage or current controlled. However, if the feedback were positive and the input immittance becomes negative, the voltage and current relationship is no longer reciprocal and it is possible to deduce whether the device has a transfer admittance or impedance from the input immittance measurements. If it is a voltage controlled negative admittance Y_2, the system will be stable if it is driven by a voltage source but unstable if driven by a current source. The condition of stability is

$$\left| Y_1 + Y_o \right| > 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.18)$$

where Y_o is the output admittance of the driving source.

If the input is a current controlled negative impedance Z_1, the condition of stability is

$$\left| Z_1 + Z_o \right| > 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.19)$$

where Z_o is the output impedance of the driving source.

The foregoing discussion is concerned with the stability criteria for an immittance converter at a single operating frequency. However, a practical converter must be stable at all frequencies and must meet the general stability criteria of e.g. Bode (ref. 1.14) and Nyquist (ref. 1.15). Thus, in order to perform a complete design, an approach more oriented to control theory and suitable for determining both the overall stability criteria and the

terminal characteristics will prove convenient.

1.2.1 Two Amplifier Immittance Converters

The immittance converter in Fig. 1.8 can be drawn in control form as shown in Fig. 1.11, which is a single loop feedback system. All the circuit elements in the system are treated as transducers. The system contains a voltage amplifier, a current amplifier and a transfer conductance G_y. The voltage amplifier is the voltage controlled voltage source of figure 1.8 which has a gain $G_V = \frac{V_2}{V_1}\Big|_{I_2 = 0}$, the current amplifier is the current controlled current source which has a gain $G_I = \frac{I_1}{I_2}\Big|_{V_1 = 0}$ and the transfer admittance G_y is the terminating admittance Y. Note that a one-port immittance G_y is now treated as a two-port transducer. This is possible because it is placed in a zero impedance loop and its input and output are different quantities.

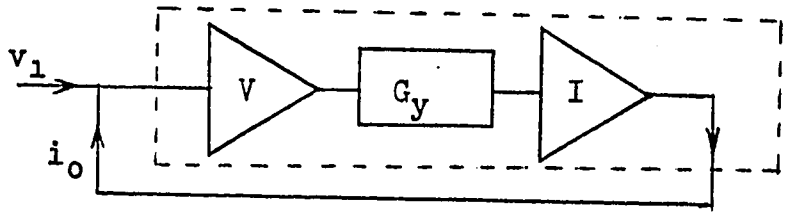


Fig. 1.11 A control form representation of the immittance converter of Fig. 1.8

Because the transfer function of the voltage and current amplifiers are pure numbers, being in series with G_y, they do not change the dimension of G_y, but modify its

magnitude by the product of their transfer functions $G_I G_V$. Thus the dotted box in Fig. 1.11 is a transfer conductance $G_I G_V G_y$.

With the output feedback to the input, they are at the same port and the system becomes an admittance.

$$Y_1 = - G_V G_I G_y \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.20)$$

Alternatively the V and I relationship at the input may be stated in terms of a transfer resistance G_z as shown in Fig. 1.12.

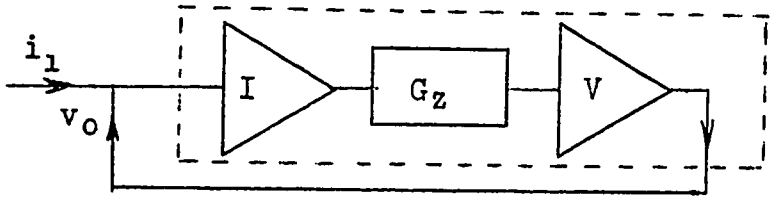


Fig. 1.12 Another control form representation of the immittance converter of Fig. 1.8

$$Z_1 = G_V G_I G_z \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1.21)$$

The following two points are noted for the above two configurations:

(1) In both cases the transfer conductance or resistance is placed between the two controlled sources. So that it is isolated from the input of the system.

(2) The sign of Y_I or Z_I depends on the sense of the feedback. Y_I or Z_I is positive if the feedback is negative and negative if the feedback is positive.

1.2.2 One Amplifier Immittance Converters

As the transfer function of the voltage and current amplifiers are pure numbers, removing a voltage or a current amplifier does not affect the dimensions of the transfer function of the series chain in Fig. 1.11 and Fig. 1.12, but reduces it by a factor equal to the gain of the amplifier removed. By doing so, four different forms of immittance converter are formed. Fig. 1.13 and Fig. 1.14 are formed respectively by removing a current and a voltage amplifier from Fig. 1.11, and Fig. 1.15 and Fig. 1.16 are similarly formed from Fig. 1.12.

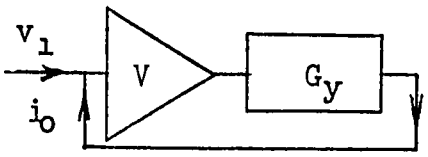


Fig. 1.13 An immittance converter formed from Fig. 1.11 by removing the current amplifier

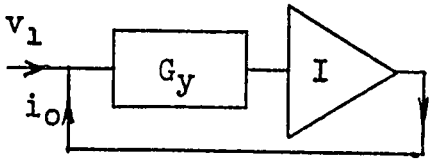


Fig. 1.14 An immittance converter formed from Fig. 1.11 by removing the voltage amplifier

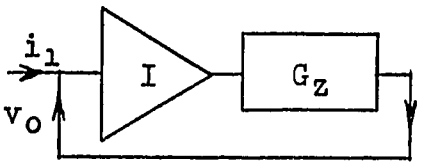


Fig. 1.15 An immittance converter formed from Fig. 1.12 by removing the voltage amplifier

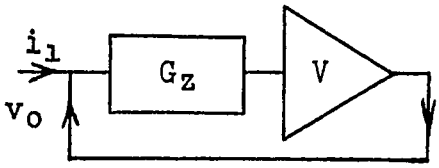


Fig. 1.16 An immittance converter formed from Fig. 1.12 by removing the voltage amplifier

The input immittance of Fig. 1.13, 1.14, 1.15, 1.16 are

respectively

$Y_1 = G_y(1+G_V)$, $Y_1 = G_y(1+G_I)$, $Z_1 = G_z(1+G_I)$, $Z_1 = G_z(1+G_V)$, i.e., as an amplifier is removed, the original transfer immittance G_y or G_z is seen directly by the input. Thus the input immittance can be partitioned into two components: one is G_y or G_z, the other is a converted immittance introduced by the amplifier. For the configuration shown in Fig. 1.13, with negative feedback (i.e., the amplifier gain G_V is negative), thus

$$Y_1 = \frac{i_o}{V_1} = G_y - (G_V G_y)$$
$$= G_y + G_V G_y \quad \ldots\ldots\ldots\ldots \quad (1.22)$$

Eq. 1.22 can be represented by Fig. 1.17 where G_y and $G_V G_y$ are in parallel,

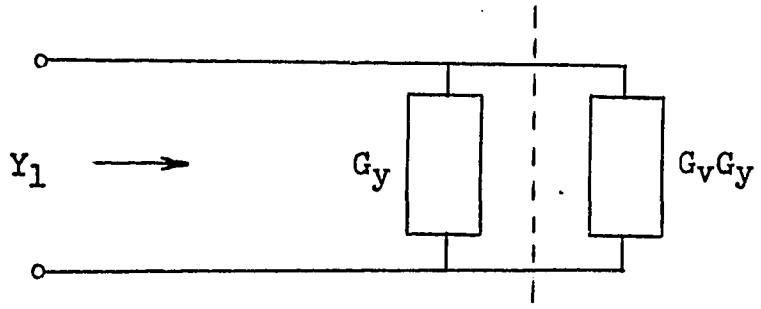


Fig. 1.17 Y_1 represented by G_y and $G_V G_y$ in parallel

with positive feedback (G_V is positive), thus

$$Y_1 = G_y - (G_V G_y) = G_y - G_V G_y \quad \ldots\ldots\ldots\ldots \quad (1.23)$$

Eq. 1.23 can be represented by Fig. 1.18 where G_y and $-G_V G_y$ are in parallel.

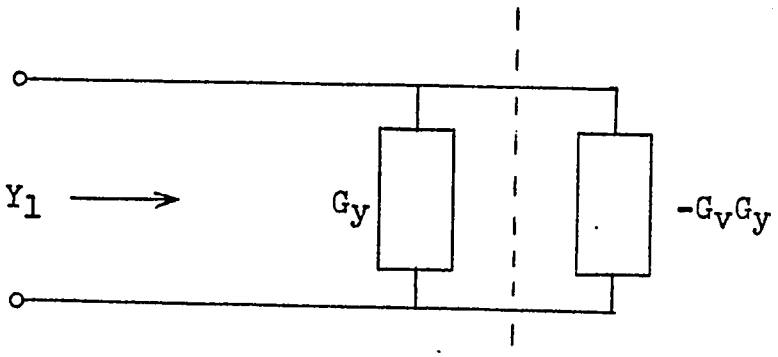


Fig. 1.18 Y_1 represented by G_y and $-G_vG_y$ in parallel

For the configuration shown in Fig. 1.14 with negative feedback (the current amplifier is inverted or G_I is positive), thus

$$Y_1 = G_y + (G_1G_y) = G_y + G_IG_y \quad \ldots\ldots\ldots\ldots\ldots \quad (1.24)$$

With positive feedback (the current amplifier is non-inverted or G_I is negative), thus

$$Y_1 = G_y + (G_1G_y) = G_y - G_1G_y \quad \ldots\ldots\ldots\ldots\ldots \quad (1.25)$$

Eq.1.24 &1.25 can be similarly represented as shown in Fig. 1.17 and Fig. 1.18 respectively.

For Fig. 1.15, with negative feedback (G_I is positive), thus

$$Z_1 = G_z + (G_1G_z) = G_z + G_1G_z \quad \ldots\ldots\ldots\ldots\ldots \quad (1.26)$$

Eq.1.26 can be represented by Fig. 1.19 where G_z and G_IG_z are in series.

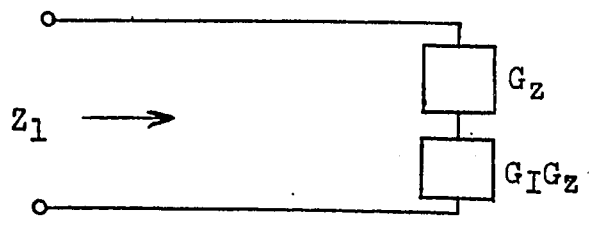


Fig. 1.19 Z_1 represented by G_z and G_IG_z in series

With positive feedback (G_I is negative), thus

$$Z_1 = G_z + (G_1 G_z) = G_z - G_1 G_z \quad \ldots\ldots\ldots\ldots\ldots \quad (1.27)$$

Eq. 1.27 can be represented by Fig. 1.20 where G_z and $-G_I G_z$ are in series.

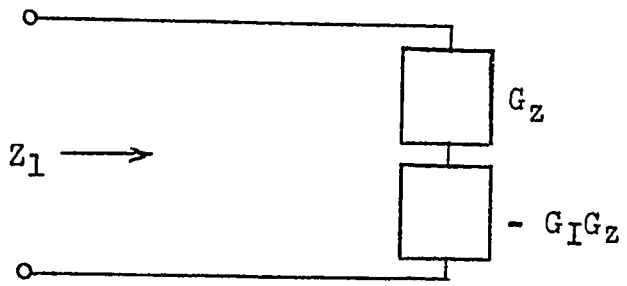


Fig. 1.20 Z_1 represented by G_z and $-G_I G_z$ in series

For Fig. 1.16 with negative feedback (G_v is positive), $G_v G_z$ is positive, thus

$$Z_1 = G_z + (G_v G_z) = G_z + G_v G_z \quad \ldots\ldots\ldots\ldots\ldots \quad (1.28)$$

With positive feedback (G_v is negative), thus

$$Z_1 = G_z + (G_v G_z) = G_z - G_v G_z \quad \ldots\ldots\ldots\ldots\ldots \quad (1.29)$$

Eq. 1.28 and 1.29 can be similarly represented by Fig. 1.19 and 1.20 respectively.

The trivial case of a simple passive immittance is treated as a single transfer immittance G_y or G_z with the output and input connected to the same port, as shown in Fig. 1.21 (a) & (b).

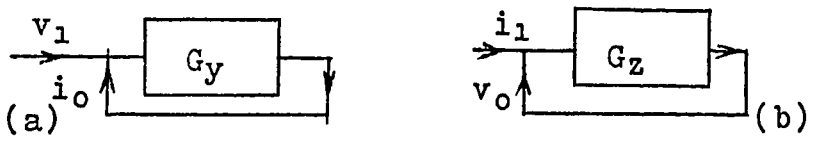


Fig. 1.21 A simple passive immittance treated as a single transfer immittance

The sense of the feedback is always taken to be negative.

The circuit configuration for the one amplifier immittance converter in Fig. 1.13 to 1.16 are shown respectively in Fig. 1.22 to 1.25.

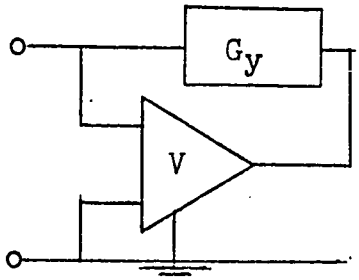


Fig. 1.22

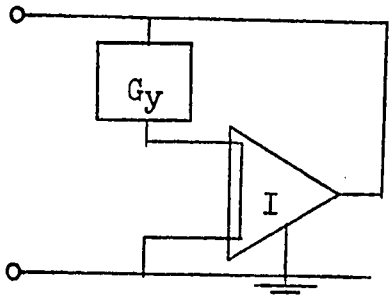


Fig. 1.23

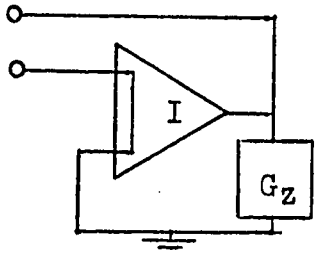


Fig. 1.24

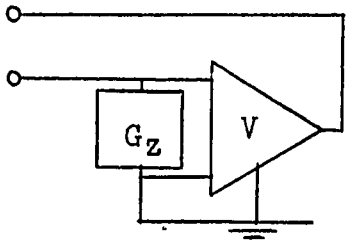


Fig. 1.25

Figs. 1.22, 1.23, 1.24 and 1.25 are the circuit configurations of Figs. 1.13, 1.14, 1.15 and 1.16 respectively.

1.2.3 Effect of Time Delay in One Amplifier Immittance Converters

Since all amplifiers introduce a time delay t_d, the current gain G_I is complex and can be expressed as

$$G_I = G_I' - jX_I$$

$$= B_I e^{-j\theta_I}$$

$$= B_I(1-j\theta_I) \quad \ldots\ldots\ldots\ldots\ldots \quad (1.30)$$

If θ_I IS small,

$$\text{where} \quad B_I = \sqrt{G_1'^2 + X_I^2}$$

$$\text{and} \quad \theta_I = t_{an} \frac{-1X_I}{G_1'}$$

$$= \omega t_d$$

Similarly, the voltage gain

$$G_V = B_V e^{-j\theta_V}$$

$$= B_V(1-j\theta_V) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.31)$$

Substituting eq. 1.30 & 1.31 in eq. 1.23, 1.25, 1.27 & 1.29. (assuming positive feedback in all cases), we obtain respectively

$$Y_1 = G_y - G_y\left[B_V(1-j\theta_V)\right] = G_y - G_yB_V + j\,G_yB_V\,\theta_V \,. \quad (1.32)$$

$$Y_1 = G_y - G_y\left[B_1(1-j\,\theta_1)\right] = G_y - G_yB_I + j\,G_yB_I\,\theta_1 \,. \quad (1.33)$$

$$Z_1 = G_z - G_z\left[B_1(1-j\,\theta_1)\right] = G_z - G_zB_I + j\,G_zB_1\,\theta_1 \,. \quad (1.34)$$

$$Z_1 = G_z - G_z\left[B_V(1-j\,\theta_V)\right] = G_z - G_zB_V + j\,G_zB_V\,\theta_V \,. \quad (1.35)$$

The immittances due to the time delay for the above four configurations employed to tune a ferrite rod antenna are tabulated in Table 1.1. If the feedback is negative, the sign is changed. An alternative approach to account for the time delay is given in section 1.4.2.

A general comment on system stability can now be made. As in the two amplifier immittance converters, in the cases where the time delay introduces positive immittances, the system is inherently stable but it lowers the system Q

	G_y	Equivalent Conductance Due to Time Delay		G_z	Equivalent resistance Due to Time Delay
Eq. 1.32	$j\omega C$	$-\omega C \theta_V B_V$	Eq. 1.34	$\frac{1}{j\omega C}$	$+\frac{\theta_I B_I}{\omega C}$
Fig. 1.13	$\frac{1}{j\omega L}$	$+\frac{\theta_V B_V}{\omega L}$	Fig. 1.15	$j\omega L$	$-\omega C \theta_I B_I$
Eq. 1.33	$j\omega C$	$-\omega C \theta_I B_I$	Eq. 1.35	$\frac{1}{j\omega C}$	$+\frac{\theta_V B_V}{\omega C}$
Fig. 1.14	$\frac{1}{j\omega L}$	$+\frac{\theta_I B_V}{\omega L}$	Fig. 1.16	$j\omega L$	$-\omega L \theta_V B_V$

Table 1.1 The immittances due to time delay for the above four configurations employed to tune an antenna

whereas in the cases where the time delay introduces negative immittance, the system Q is increased as it approaches instability.

1.3.0 Stability Considerations

The basis of a closed loop system stability is determined by the roots of the characteristic equations of the closed loop response. The Nyquist Criterion and Bode Criteria (ref. 1.14 and 1.15) are convenient criteria which can yield system stability information from the characteristic equations.

For a system whose open loop gain is G(S) and feedback factor H(S) the closed loop response can be stated as

$$\frac{\text{output}}{\text{input}} = \frac{G(S)}{1 + G(S)H(S)} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.36)$$

and the characteristic equation is

$$1 + G(S)\,H(S) = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.37)$$

The roots of the characteristic equation are the poles of 1.36, thus the relation of the roots and the system response (stability) can be stated as:

(1) If all the roots are in the left half of the S-plane, the transient will die out and the system is stable.

(2) If more than one pair of roots are on the imaginary axis the response is undamped sinusoidal oscillations and the system is considered unstable.

(3) If one or more roots are in the right half of the S-plane, the response will increase with time and the system

is unstable.

Physically all linear systems have a limit of linearity. Once they become unstable, they saturate and the loop gain G(S) H(S) is reduced to unity.

1.3.1 Nyquist Criterion

Nyquist criterion is a convenient technique to discover if the characteristic equations has any roots in the right half of the S-plane. Following the Nyquist path in the clockwise direction, the magnitude and angle of G(S) H(S) are plotted in the G(S) H(S) plane, a Nyquist diagram is obtained. The Nyquist locus will make N = Z - P encirclements of the critical point (-1,0), where

Z = number of zeros of the characterisitc equation in the right half plane.

P = number of poles of H(S) G(S) in the right half of the S-plane

The encirclement of (-1,0) is clockwise if $(Z-P) > 0$ and anti-clockwise if $(Z-P) < 0$.

For most systems G(S) and H(S) are stable functions, i.e. P = 0. For a stable system N must be zero. Thus, assuming P = 0, Fig. 1.26 shows the Nyquist locus for a stable system as it does not encircle the critical point in an clockwise direction; Fig. 1.27 shows the Nyquist locus for an unstable system which makes an clockwise encirclement of the critical point and Fig. 1.28 shows the Nyquist locus for a conditional stable system.

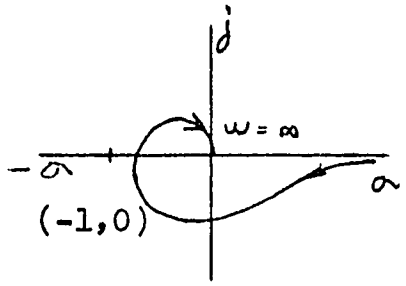


Fig. 1.26 Nyquist locus of a stable system

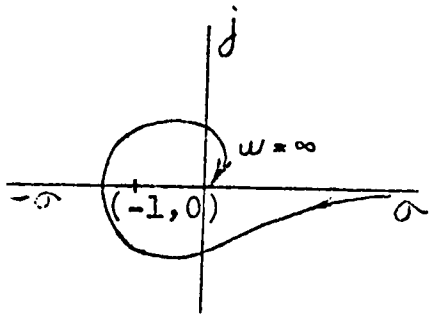


Fig. 1.27 Nyquist locus of an unstable system

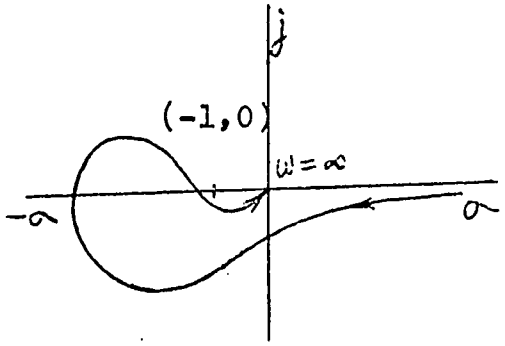


Fig. 1.28 Nyquist locus of a conditionally stable system

A conditionally stable system is undesirable in practice, because once oscillation starts, the system saturates and reduces the loop gain G(S) H(S) to $1 \angle -180^\circ$ and oscillations persist.

1.3.2 Bode Criterion

If the transfer function is a minimum phase function, which is defined as one which does not have any poles or zeros in the right half of the S-plane, or the relationship between the magnitude and phase is unique, Bode criterion can be applied to determine the system closed loop stability.

In general, G(S) H(S) can be stated as

$$G(S)\,H(S) = \frac{K'\,(S+z_1)(S+z_2)\text{ ------- }(S+z_m)}{S^{\ell}\,(S+p_1)(S+p_2)\text{ ------- }(S+p_n)} \quad \ldots\ldots \quad (1.38)$$

where K' is a constant and ℓ is a positive integer. The z's and p's may be zero, real or complex conjugate. Under sinusoidal conditions, $S = j\omega$, Eq. 1.38 can be written as

$$G(S)\,H(S) = \frac{K\,(1+\frac{j\omega}{z_1})(1+\frac{j\omega}{z_2})\text{ ---- }(1+\frac{j\omega}{z_m})}{(j\omega)^{\ell}(1+\frac{j\omega}{p_1})(1+\frac{j\omega}{p_2})\ (1+\frac{j\omega}{p_n})} \quad \ldots\ldots \quad (1.39)$$

where $K = K' \prod_{i=1}^{m} z_i \Big/ \prod_{i}^{n} p_i$

The magnitude is given by

$$20\log_{10}\left[G(j\omega)H(j\omega)\right] = 20\log_{10} K + 20\log_{10}\left[1+\frac{j\omega}{z_i}\right] + \text{- - -}$$

$$\text{----} + 20\log_{10}\left[1+\frac{j\omega}{z_m}\right] - 20\log_{10}\ (j\omega)^{\ell} - 20\log_{10}(1+\frac{j\omega}{p_1}) —$$

$$\text{-----} —20\log_{10}\left[1+\frac{j\omega}{p_1}\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1.40)$$

and the phase is given by

$$\arg\left[G(j\omega)\,H(j\omega)\right] = \arg K + \arg\left[1+\frac{j\omega}{z_1}\right] + \text{-----}$$

$$+\arg\left[1+\frac{j\omega}{z_m}\right] - \arg\,(j\omega)^{\ell} - \arg\,(1+\frac{j\omega}{p_1})\ \text{------}$$

$$-\arg\left[1+\frac{j\omega}{p_n}\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1.41)$$

A pair of complex zeros in 1.38 consists of two terms in 1.40 & 1.41 which can be replaced respectively by

$$20\log_{10}\left[1-(\frac{\omega}{\omega_z})^2 + j2\zeta\frac{\omega}{\omega_z}\right]$$

and $\arg \left[1 - \left(\frac{\omega}{\omega_z}\right)^2 + 2j\zeta \frac{\omega}{\omega_z} \right]$

A pair of complex poles in 1.38 consists of two terms in 1.40 &1.41 which can be replaced respectively by

$$20 \log_{10} \left[\frac{1}{1-\left(\frac{\omega}{\omega_p}\right)^2 + 2j\zeta \frac{\omega}{\omega_p}} \right]$$

and $\arg \left[\frac{1}{1-\left(\frac{\omega}{\omega_p}\right)^2 + 2j\zeta \frac{\omega}{\omega_p}} \right]$.

Plotting 1.40 in db. and 1.41 in degrees vs logω separately form the Bode plot, e.g. as shown in Fig. 1.29. For most practical purposes, straight line approximations are adequate.

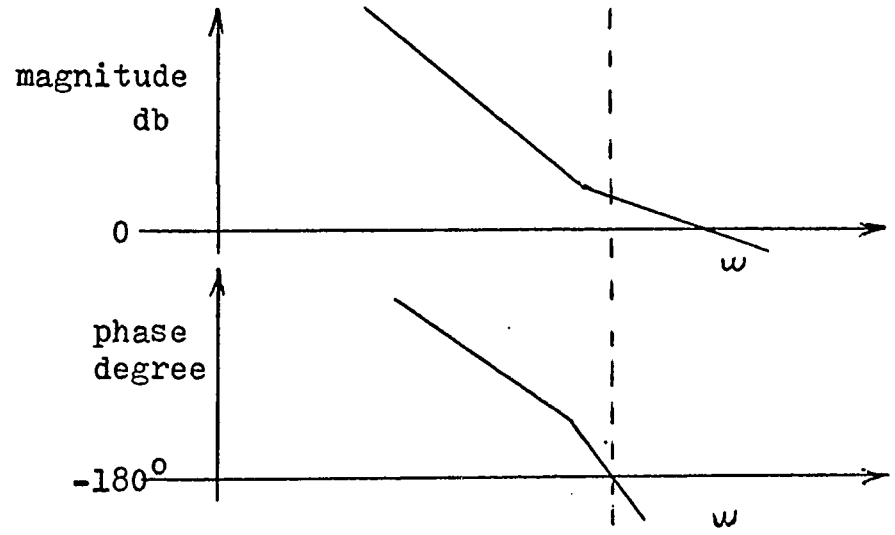


Fig. 1.29 Straight line approximation in Bode plot

The closed loop system is unstable if the magnitude is greater than zero db. when the phase is -180°. This corresponds to the Nyquist locus encirles the critical point

(- 1, 0). In order to be stable, the magnitude must be less than zero db. when the phase is -180°.

1.3.3 Bode & Nyquist Criteria Applied to Two Amplifier Immittance Converters.

An immittance converter can be used to tune a ferrite rod antenna in two possible forms, the high pass and the low pass form as shown respectively in Fig. 1.30 (a) and (b). They are similar with the interchange of the L and C and the two forms will be considered in detail below.

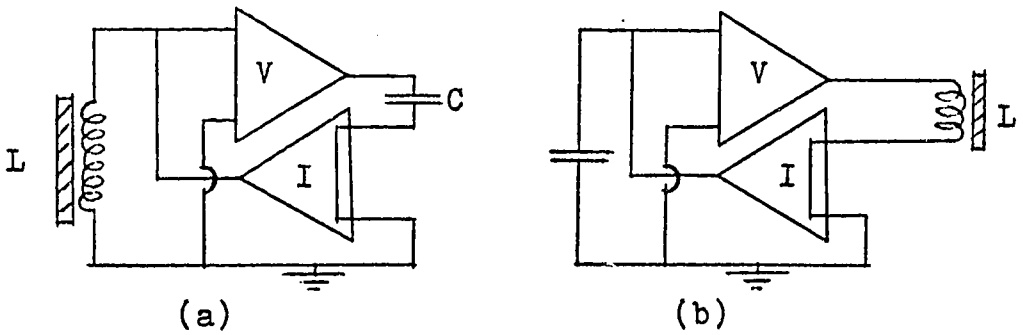


Fig. 1.30 An immittance converter arranged to tune an antenna in (a) High pass form (b) low pass form

(a) First consider immittance converter systems employing practical inductances and capacitances and ideal voltage and current amplifiers, i.e., the voltage amplifier has infinite input impedance and zero output impedance and has no delay and the current amplifier has zero input impedance and infinite output impedance and there is no delay.

Then the L and C separately introduces a phase shift of almost 90° at the tuned frequency. In the high pass case the

phase shift is leading and in the low pass case the phase shift is lagging. The Bode magnitude plot for the above two cases are shown in Fig. 1.31 and Fig. 1.32 respectively.

The slope is 12 db/oct. in both cases. It is positive for the high pass case and negative for the low pass case. AB is the operating region. As the slope is rising at 12 db/oct. in the high pass case, in order not to violate the Bode

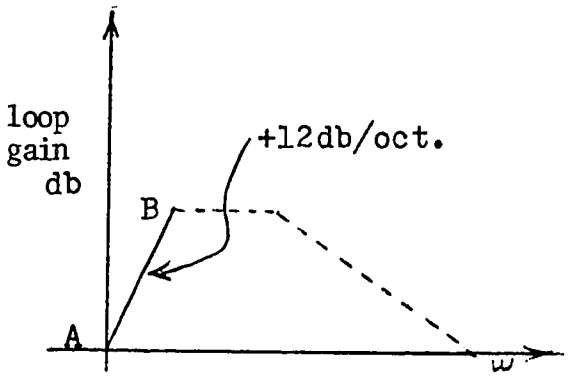


Fig. 1.31 Bode Magnitude plot for the high pass form

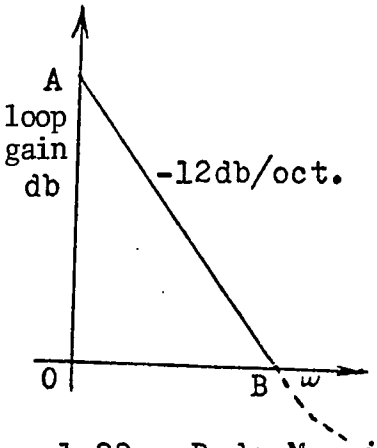


Fig. 1.32 Bode Magnitude plot for the low pass form

Criterion of stability the magnitude must decrease to zero db. when the phase is -180^{o}. This problem does not exist in the low pass case as the L and C cause the magnitude to fall at a rate of -12 db/oct. right to zero db. satisfying the Bode Criteria of stability.

(b) Systems employing practical amplifiers

Practical amplifiers have finite input and output impedances, which introduce a loss into the system as will be discussed later, and a time delay t_d which adds a lagging phase angle $\theta = \omega t_d$ radians to the loop. The time delay

modifies the Nyquist locus for the two forms as shown dotted in Fig. 1.33 & Fig. 1.34 respectively.

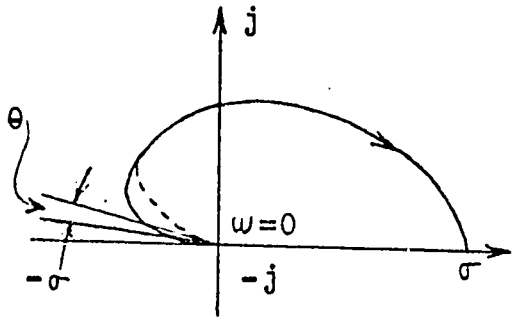


Fig. 1.33 Nyquist locus for the high pass form

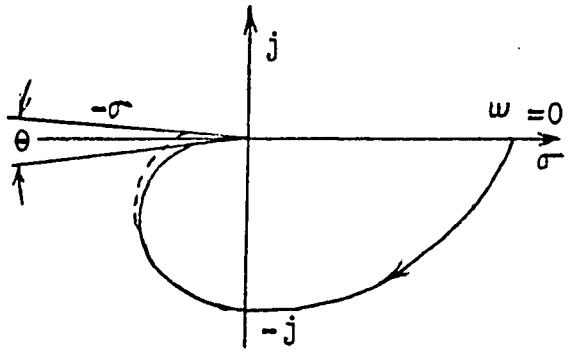


Fig. 1.34 Nyquist locus for the low pass form

It is seen that the time delay renders the low pass form potentially unstable as the Nyquist locus will exceed -180^{o} phase shift, but increases the system stability in the high pass case. Equivalently it can be said that the time delay introduces a loss to the high pass form and a gain (negative immittance) to the low pass form (refer to section 1.1.4 and 1.1.5).

1.4 Circuit Analysis for the Complete Antenna Tuning System Using Two Practical Amplifier Immittance Converters

(I) Effect of Time Delay as a Loss Factor

At any frequency ω, the time delay t_d through the circuit can be represented by an equivalent resistance $r_T = \omega^2 L t_d$ or $r_T = \frac{\theta}{\omega c}$ in series with the inductance L of the antenna or the capacitance C. As shown in Fig. 1.35,

θ is the phase angle due to the delay t_d. As

$$Q = \frac{\omega L}{r_T} = \frac{1}{\omega C r_T} = \frac{1}{\tan \theta} \simeq \frac{1}{\theta}$$

The approximation is valid if

$$\theta < \frac{\pi}{36} \text{ rad or } 5^\circ, \quad \therefore r_T = \omega L \theta = \omega^2 L t_d$$

as $\theta = \omega t_d$

$$\text{or } r_T = \frac{\theta}{\omega C} = \frac{\omega t_d}{\omega C} = \frac{t_d}{C} \quad \ldots\ldots\ldots\ldots \quad (1.42)$$

which is positive in the high pass form and negative in the low pass form.

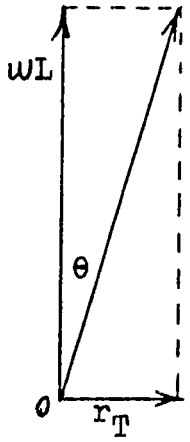


Fig. 1.35 Vector diagram to illustrate the effect of phase delay

(II) Equivalent Circuits

As the immittance converter is used to synthesize a variable capacitor to tune the antenna with an inductance L, it is convenient to draw the equivalent circuit for the system with the immittance and converter losses all referred to the port in which the antenna is terminated. There are two convenient methods to handle these losses and by these methods they can be partitioned as explained below. Because

at the shunt port, the input of the voltage amplifier is in parallel with the output of the current amplifier, and at the series port the input of the current amplifier is in series with output of the voltage amplifier, it is convenient to express the input immittance at the above two ports as $y_1 = \frac{i_o}{V_1}$ and $Z_1 = \frac{V_o}{i_1}$ respectively. Thus it is also convenient to represent the losses in the high pass form by a conductance g shunting the tuned system as shown in Fig. 1.36 (a) while in the low pass form by a resistance r in series with the tuned system as shown in Fig. 1.36(b). g and r can be expressed respectively by Eq. 1.43 and 1.44 as the sum of the losses.

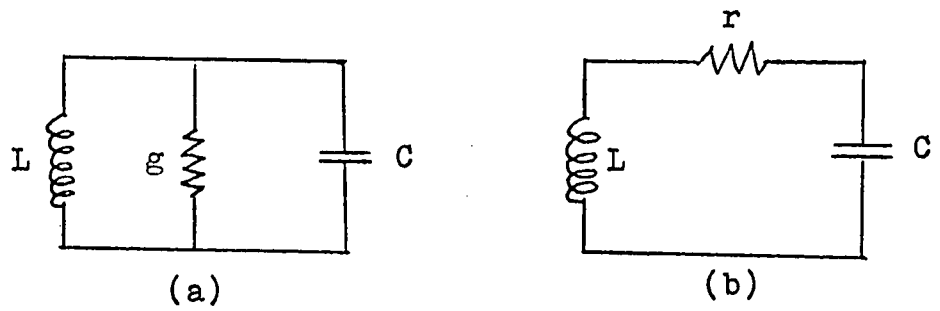


Fig. 1.36 (a) Equivalent circuit for the high pass form
(b) Equivalent circuit for the low pass form

$$g = g_1 + g_2 + \text{-------} + g_n \quad \text{.....} \quad (1.43)$$

$$r = r_1 + r_2 + \text{-------} + r_n \quad \text{.....} \quad (1.44)$$

where g_1, ... g_n; r_1 .... r_n are the various losses in the amplifiers referred to the shunt port and the series port respectively.

The equivalent circuit for the high pass form is shown in Fig. 1.37 (a) in which the admittances and losses are all

referred to the shunt port. The admittance transformation ratio from the series to shunt port is B (eq. 1.20, $B = G_V G_I$). The equivalent circuit for the low pass form is shown in Fig. 1.37 (c) in which the impedances and losses are all referred to the series port. The impedance transformation ratios from the shunt port to the series port is B (eq. 1.21) Fig. 1.37 (a) and (c) can be simplified to Fig. 1.37 (b) and (d) respectively, where g and r are given by Eq. 1.43 and 1.44

n = 5 as only five losses due to the imperfections of the amplifiers are considered important.

g_1, r_1 - Equivalent shunt conductive and series resistive loss of the antenna respectively

g_2, r_2 - Equivalent shunt conductive and series resistive loss due to time delay

g_3, r_3 - Equivalent shunt conductive and series resistive loss at the shunt port

g_4, r_4 - Equivalent shunt conductive and series resistive loss due to output resistance (in series) with the series port

g_5, r_5 - Equivalent shunt conductive and series resistive loss due to the loss shunting the series port

Their values are tabulated in Table 1.2. The corresponding Q and the tuned frequency for the two forms are respectively,

$$Q_{HP} = \frac{1}{\omega L g}, \quad f_{HP} = \frac{1}{2\pi\sqrt{LCB}} \quad \ldots\ldots\ldots\ldots\ldots \quad (1.45)$$

and $$Q_{LP} = \frac{\omega L}{r}, \quad f_{LP} = \frac{1}{2\pi\sqrt{LC/B}} \quad \ldots\ldots\ldots\ldots\ldots \quad (1.46)$$

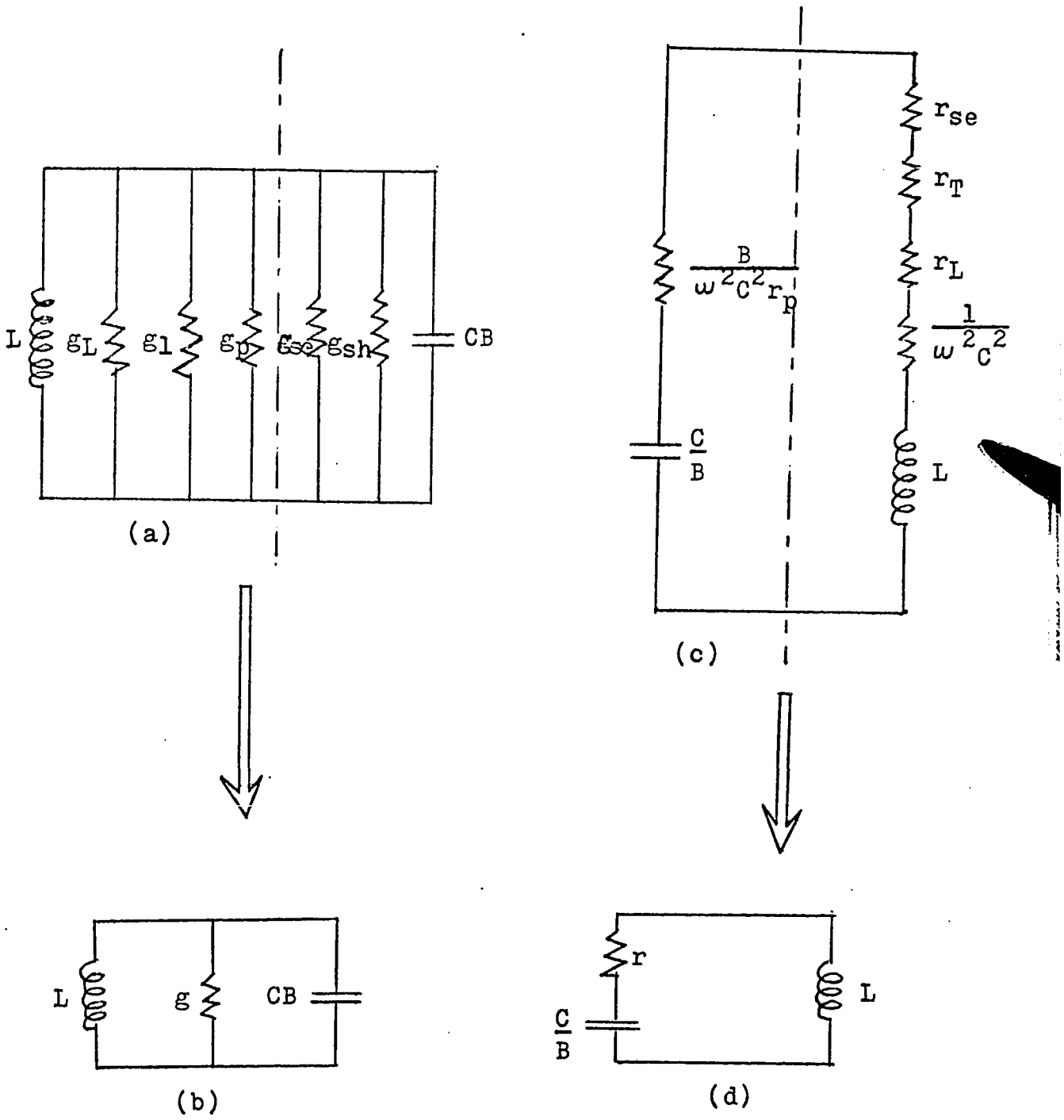


Fig. 1.37 (a) Equivalent circuit for the high pass form which can be simplified into (b)

(c) Equivalent circuit for the low pass form which can be simplified into (d)

Admittance Transformed From Series Port to Shunt Port	Impedance Transformed From Shunt Port to Series Port	
$g_1 = g_L = \frac{r_L}{(\omega L)^2}$	$r_1 = r_L$	r_L is the series loss of L
$g_2 = g_T = \frac{\omega^2 L t_d}{(\omega L)^2} = \frac{t_d}{L}$	$r_2 = -\omega^2 L t_d = r_T$	t_d is the loop delay time
$g_3 = g_p = \frac{1}{r_p}$	$r_3 = \frac{B}{\omega^2 C^2 r_p}$	r_p is the total resistance at the shunt port
$g_4 = g_{se} = \omega^2 C^2 B\, r_{se}$	$r_4 = r_{se}$	r_{se} is the total output series resistance at the the series port
$g_5 = g_{sh} = \frac{B}{r_{sh}}$	$r_5 = \frac{BL}{Cr_{sh}}$	r_{sh} is the total resistance shunting the series port

Table 1.2 Losses of the High Pass Form and Low Pass Form Referred to the Shunt Port and Series Port Respectively

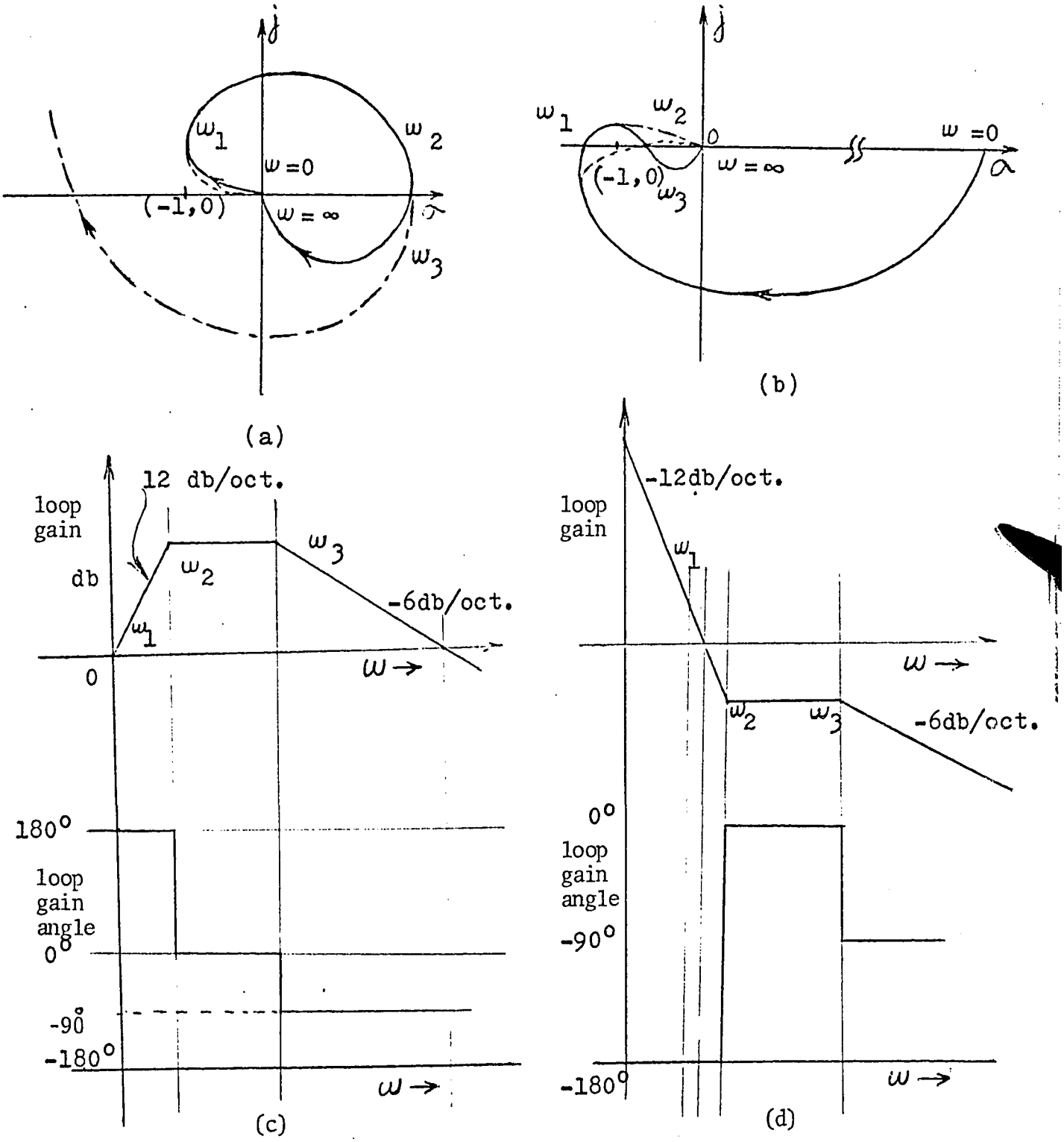


Fig. 1.38 (a)and(b) are respectively the Nyquist locus for the complete antenna tuning system using immittance converter arranged in the high pass form and low pass form. Fig. 1.38 (c)and(d) are the Bode curves for the two forms respectively

(III) Using Bode and Nyquist Criteria to Examine Their Stabilities

Due to L and C, the phase shift of the loop at low frequency is almost 180° leading in the high pass form and 180° lagging in the low pass form, owing to the series resistive losss in L and the losses at the shunt and series port of the converter, while the magnitude increases at 12db/oct in the high pass form and decreases at -12 db/oct in the low pass form. As the frequency increases and, if there is no time delay, the Nyquist loci for the two forms are as shown dotted in Fig. 1.38 (a) & (b). Because of the time delay introducing a phase lag angle $\theta = \omega t_d$, the actual Nyquist locus for the high pass form deviates from the negative real axis at $\omega = \omega_1$, while that for the low pass form will cross the negative real axis, causing the system to be conditionally stable. As the frequency increases, the magnitude and phase angle of the Nyquist loci for the two forms continue to change as mentioned above until $\omega = \omega_2$ the stray capacitance C_s across L comes into effect, which reduces the Nyquist locus magnitude by 6 db/oct in the high pass form and increases it by 6 db/oct in the low pass form and C_s also adds 90° phase lag in the high pass form and 90° phase lead in the low pass form. The amplifiers roll off at 6 db/oct at the high frequency end. Thus the Nyquist locus for the two forms are as shown in the figures. Without C_s, the Nyquist locus for the two forms are shown dashed in the figures. It is seen that C_s

restores the stability in the high pass form. The corresponding Bode Curves for the two forms are shown in Fig. 1.38 (c) & (d) respectively.

1.4.1 Circuit Analysis for the Complete Antenna Tuning System Using One Amplifier Negative Immittance Converter

The one amplifier voltage controlled negative immittance converter employed to tune an antenna is shown in Fig. 1.39. (The reason for the choice is given in section 3.2).

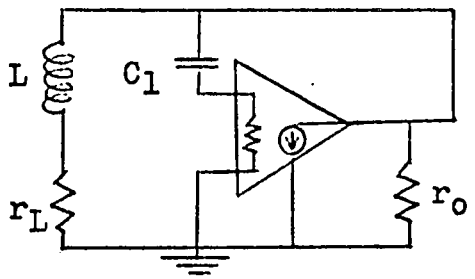


Fig. 1.39 One amplifier voltage controlled negative immittance converter (with losses) employed to tune an antenna

The imperfections of the current amplifiers are

r_1 - input resistance of the amplifier

r_o - output resistance of the amplifier

t_d - time delay in the amplifier

The equivalent circuit for Fig. 1.39 is shown in Fig. 1.40, where

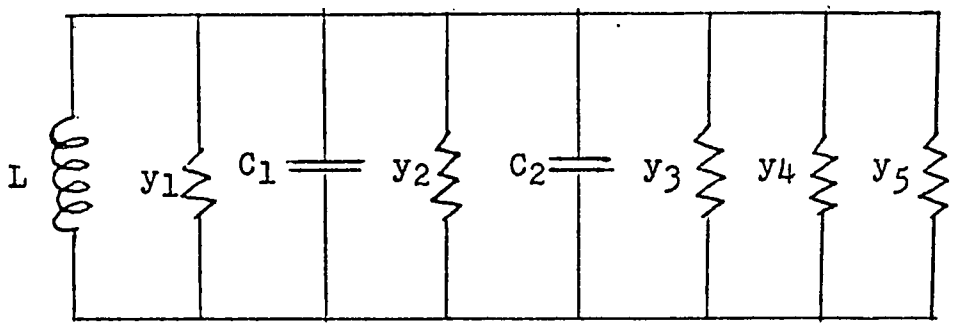


Fig. 1.40 Equivalent circuit of Fig. 1.39

the losses can be represented by

$$y = y_1 + y_2 + \ldots\ldots\ldots y_n \quad \ldots\ldots\ldots\ldots \quad (1.47)$$

n is the number of losses and in this case n = 5 as only five losses are considered important and where

y_1 - equivalent shunt admittance of the antenna

y_2 - equivalent shunt admittance of the input of the amplifier

y_3 - converted value of y_2

y_4 - equivalent shunt admittance of the output of the amplifier

y_5 - equivalent shunt admittance due to time delay

C_2 - converted value of $C_1 = - A\ C_1$

The above losses are tabulated in Table 1.3

$y_1 = \frac{r_L}{(\omega L)^2}$	r_L is the series loss of L
$y_2 = \frac{1}{(\omega C)^2 r_1}$	r_1 is the input resistance of the amplifier
$y_3 = -A\ y_1$	- A is the gain of the amplifier or the feedback factor
$y_4 = y_o = \frac{1}{y_o}$	r_o is the output resistance of the amplifier
$y_5 = y_T = -\frac{C}{t_d} \cdot A$	t_d is the amplifier delay time

Table 1.3 Losses of the one amplifier negative immittance converter employed to tune an antenna

Fig. 1.40 can be simplified to Fig. 1.41 and the condition for the system stability is

$$y \geqslant 0$$

$$\text{i.e., } (y_1 + y_2 + y_3 + y_4 + y_5) \geqslant 0$$

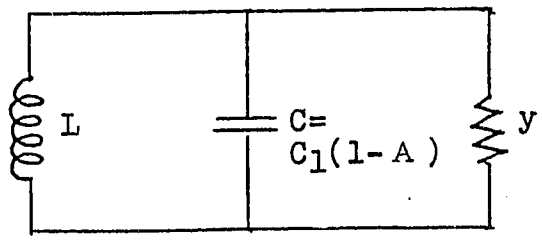


Fig. 1.41 Simplified equivalent circuit of Fig. 1.40

The Nyquist locus for the one amplifier voltage controlled negative immittance converter used to tune a

ferrite rod antenna is shown in Fig. 1.42. Curve a is the Nyquist locus if the losses in the antenna and the input and out impedance of the current amplifier are considered. Curve b is the Nyquist locus if the time delay in the amplifier

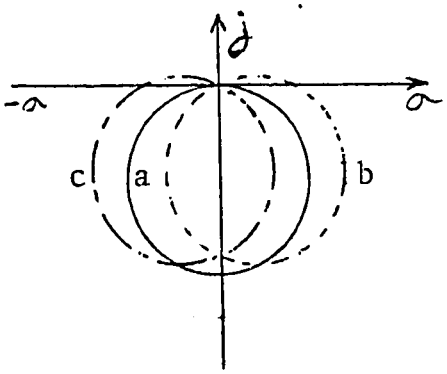


Fig. 1.42 Nyquist locus for the one amplifier voltage controlled negative immittance converter

is also considered but with negative feedback; it is seen that this will reduce the system Q. As G_1 increases, it is tilted more to the right. Curve C is the Nyquist locus if time delay in the amplifier is considered but with positive feedback. As G_1 increases it is tilted to the left. It is seen that the system Q is increased as it goes towards unstability.

1.5 Gyrators

An ideal gyrator is an active 2 port linear element and its transmission matrix has been defined (ref. 1.16) by

$$\left[Agy\right] = \begin{bmatrix} 0 & +\frac{1}{G} \\ +G & 0 \end{bmatrix} \quad \ldots\ldots\ldots\ldots\ldots \quad (1.48)$$

where G is the gyration conductance. The symbol has been used for a gyrator is shown in Fig. 1.43.

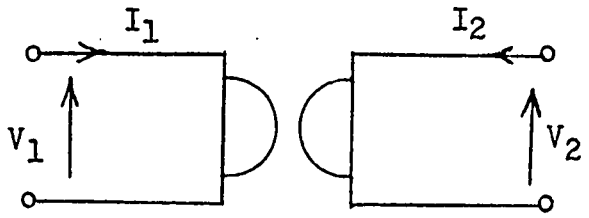


Fig. 1.43 Symbol for a gyrator

The equation for the two ports can be written in matrix form as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{G} \\ G & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.49)$$

Eq. 1.49 can be split into two equations:

$$\left.\begin{aligned} I_1 &= GV_2 \\ I_2 &= -GV_1 \end{aligned}\right\} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.50)$$

The input impedance at port 1 is

$$Z_1 = \frac{V_1}{I_1} = \frac{-I_2/G}{GV_2} = \frac{1}{G^2} \cdot \frac{1}{\frac{-V_2}{I_2}} = \frac{1}{G^2 Z_2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.51)$$

Eq. 1.51 shows the well known impedance inversion characteristics of a gyrator.

1.5.1 Gyrator formed by cascading an NIC with an NII

It is of interest that impedance inversion can also

be obtained by cascading a negative immittance converter (NIC) with a negative immittance inverter (NII) (ref. 1.17, 1.18, 1.19) as shown in Fig. 1.44. i.e.,

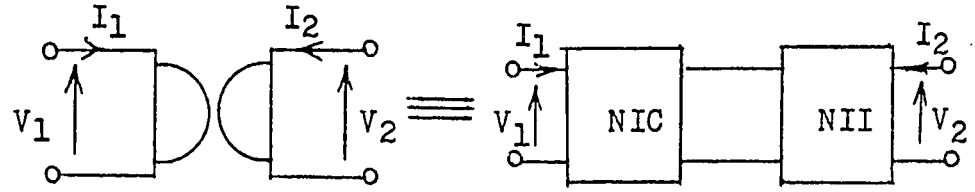


Fig. 1.44 A gyrator formed by cascading an NIC with an NII

This is shown below by manipulating the transmission matrix $[A]$. For an NII with impedance inversion ratio $1/H$, the equation for the two ports expressed in matrix form is

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & \pm\frac{1}{\sqrt{H}} \\ \mp\sqrt{H} & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad \ldots\ldots\ldots\ldots \quad (1.52)$$

where the transmission matrix

$$\begin{bmatrix} A_{NII} \end{bmatrix} = \begin{bmatrix} 0 & \pm\frac{1}{\sqrt{H}} \\ \mp\sqrt{H} & 0 \end{bmatrix} \quad \ldots\ldots\ldots\ldots \quad (1.53)$$

The transmission matrix for an NIC with convertion ratio K is given by

$$\begin{bmatrix} A_{NIC} \end{bmatrix} = \begin{bmatrix} \pm\sqrt{K} & 0 \\ 0 & \mp\frac{1}{\sqrt{K}} \end{bmatrix} \quad \ldots\ldots\ldots\ldots \quad (1.54)$$

When cascading an NIC with an NII, their transmission matrixes multiply, thus

$$\left[A_{NIC}\right]\left[A_{NII}\right] = \begin{bmatrix} \pm\sqrt{K} & 0 \\ 0 & \mp\sqrt{K} \end{bmatrix} \begin{bmatrix} 0 & \pm\frac{1}{\sqrt{H}} \\ \mp\sqrt{H} & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & +\sqrt{\frac{K}{H}} \\ +\sqrt{\frac{H}{K}} & 0 \end{bmatrix} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1.55)$$

The right hand side of eq. 1.55 is the transmission matrix of a gyrator of gyration conductance $G = \sqrt{\frac{H}{K}}$. However, this is not an economical way to realize a gyrator.

1.5.2 Transconductance gyrator and transresistance gyrator

As with immittance converters there are two types of gyrator (ref. 1.20):

Transconductance gyrator

As indicated by eq. 1.50, a transconductance gyrator can be formed by two voltage controlled current sources (ref. 1.21, 1.22) or two transconductances connected back to beck as shown in Fig. 1.45 one with no phase inversion and one with phase inversion.

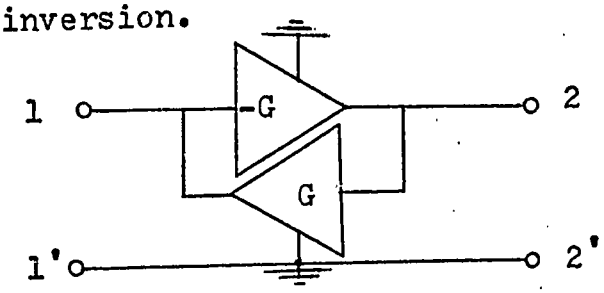


Fig. 1.45 A transconductance gyrator formed by two voltage controlled current sources

A voltage controlled current source can be decomposed into a voltage amplifier and a current amplifier with a passive conductance g between them as shown in Fig. 1.46.

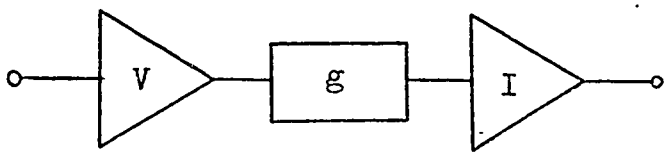


Fig. 1.46 A voltage controlled current source decomposed into a voltage and a current amplifier with a passive conductance between them.

The transconductance

$$G = G_V \, g \, G_I$$

where G_V and G_I are the gain of the voltage and current amplifier respectively. Thus if the two passive conductances are brought out of the gyrator and each forms a port, the original two port device becomes a four port device (ref. 1.20) as shown in Fig. 1.47. The transconductance gyrator is formed by port 1 and port 3 when port 2 and port 4 are terminated by passive conductances. The transfer resistance gyrator is formed by port 2 and port 4 when port 1 and port 3 are terminated with resistances as will be discussed in the next section.

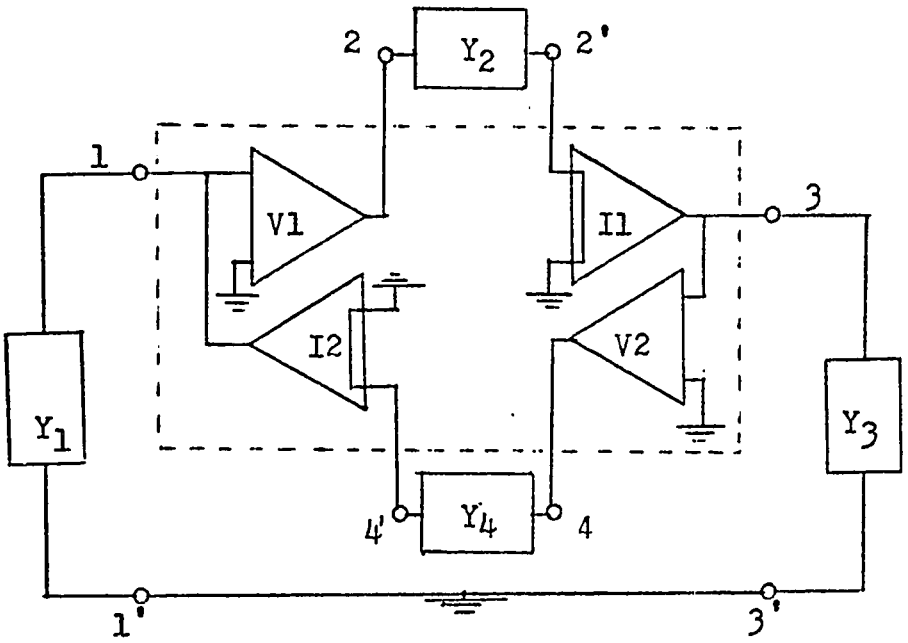


Fig. 1.47 Four port configuration of a gyrator formed by two voltage and two current amplifiers

For the transconductance gyrator, the input admittance at port I is given by

$$Y_1 = Y_2\, Y_4 \cdot G_{V1}\, G_{V2} \cdot G_{I1}\, G_{I2} \cdot \frac{1}{Y_3} \quad \ldots\ldots\ldots \quad (1.57)$$

$$Y_1 = G^2 \frac{1}{Y_3} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1.58)$$

Assuming $Y_2 = Y_4 = g$ and $G = Y_2\, G_{V1}\, G_{I1} = Y_4\, G_{V2}\, G_{I2}$, where G_{V1}, G_{V2}, G_{I1} & G_{I2} are the gain of the voltage amplifiers V_1, V_2 and current amplifiers I_1 and I_2 respectively. Eq. 1.58 shows that it has the characteristic of admittance inversion.

Eq. 1.57 indicates that:

(1) If Y_3 and Y_4 are conductances, port 1 and port 2 become an admittance converter.

(2) If Y_3 and Y_2 are conductances, port 1 and port 4 become an admittance converter.

Transresistance gyrator

If port 1 and port 3 of Fig. 1.47 are terminated with resistances, then port 2 and port 4 form a transfer resistance gyrator because it now consists of two current controlled voltage sources. The input impedance at port 2, when port 4 is terminated with Z_4, is given by

$$Z_2 = \frac{Z_1 Z_3}{Z_4} G_{V1} G_{V2} G_{I1} G_{I2} \quad \ldots\ldots\ldots\ldots \quad (1.59)$$

$$Z_2 = \frac{R^2}{Z4} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1.60)$$

if $Z_1 = Z_3 = r$ and $Z = Z_1 G_{v1} G_{I2} = Z_3 G_{v2} G_{I1}$.

Eq. 1.59 indicates that:

(1) If Z_4 and Z_3 are resistance, then port 1 and port 2 become an impedance converter.

(2) If Z_4 and Z_1 are resistance, then port 2 and port 3 become an impedance converter.

1.5.3 Stability Considerations for Gyrators

A gyrator can be terminated with two capacitors to form a resonant circuit. In the transconductance gyrator, the two capacitors will introduce a 180° phase lag while in the transfer resistance gyrator 180° phase lead. The Nyquist plots for the above two cases are shown in Fig. 1.48. The time delay t_d in the four amplifiers will introduce a phase lag angle θ ($\theta = \omega t_d$), which will bring the Nyquist curve of

the transconductance gyrator across the negative real axis and brings that of the transresistance gyrator away from the axis, as shown dotted in the figure. According to the Nyquist stability criterion, the transfer conductance gyrator employed in this way is unstable.

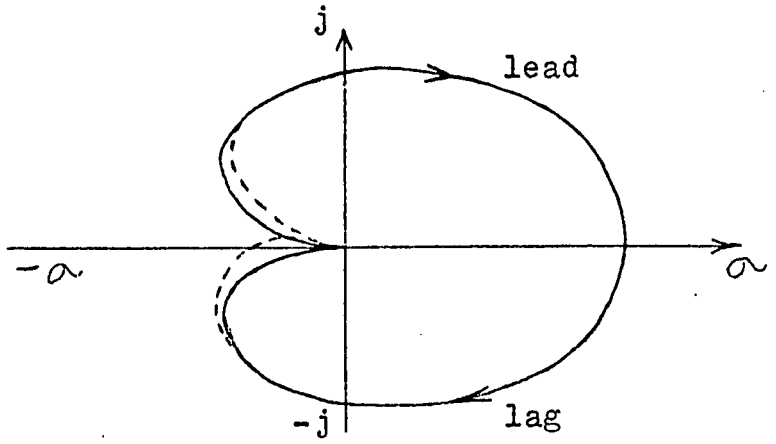


Fig. 1.48 Nyquist locus for the transresistance gyrator and transconductance gyrator when terminated with two capacitors.

1.5.4 Effect of Time Delay in Gyrators

The immittances due to the time delay t_d in the transresistance gyrator and transconductance gyrator will be deduced below.

Let Y_{12} and Y_{21} be the transfer admittance for the transconductance gyrator and Z_{12} and Z_{21} be the transfer impedance for the transresistance gyrator. They can also be written as

$$\begin{aligned} Y_{12} &= y_{21}\, e^{-j\theta_{12}} \\ Y_{21} &= y_{21}\, e^{-j\theta_{21}} \\ Z_{12} &= z_{12}\, e^{-j\theta_{12}} \\ Z_{21} &= z_{21}\, e^{-j\theta_{21}} \end{aligned} \qquad \text{..... (1.61)}$$

where y_{12}, y_{21}, z_{12} and z_{21} are the modulus of the Y_{12}, Y_{21}, Z_{12} and Z_{21} respectively and θ_{ij} is the phase shift from point i to j in the circuit.

Consider the input admittance Y_1 (eq. 1.58) of a transconductance gyrator when loaded with a capacitor C.

$$Y_1 = \frac{y_{12}\, e^{-j\theta_{12}}\, y_{21}\, e^{-j\theta_{21}}}{j\omega C}$$

$$= \frac{y_{12}\, y_{21}}{j\omega C}\, e^{-j(\theta_{12}+\theta_{21})}$$

Let $\theta_{12}+\theta_{21} = \theta = \omega t_d$

$$= \frac{y_{12}\, y_{21}}{j\omega C}\, e^{-j\theta} = \frac{y_{12}\, y_{21}}{j\omega C}(1-j\theta) \text{ if } \theta \text{ is small}$$

$$= \frac{y_{12}\, y_{21}}{j\omega C} - \frac{y_{12}\, y_{21}\, \theta}{\omega C}$$

$$= \frac{y_{12}\, y_{21}}{j\omega C} - \frac{y_{12}\, y_{21}\, t_d}{C} \quad \ldots\ldots\ldots\ldots \quad (1.62)$$

The first term on the R. H. S. of eq. 1.62 is the simulated inductance and the second is a negative conductance due to the time delay t_d, which will cause instability.

Similarly, for the transfer resistance gyrator, by using eq. 1.60, it can be shown that

$$Z_1 = \frac{z_{12}\, z_{21}\, e^{-j\theta}}{Z_3}$$

$$Z_1 = z_{12}\, z_{21}\, j\omega C + z_{12}\, z_{21}\, \omega C\theta \quad \ldots \quad (1.63)$$

Eq. 1.63 shows that the time delay introduces a positive resistance $z_{12}\, z_{21}\, \omega\, C\theta$. The Q of the simulated inductance is

$$Q = \frac{z_{12}\, z_{21}\, \omega C}{z_{12}\, z_{21}\, \omega C\theta} = \frac{1}{\theta} \quad , \quad \theta \text{ in radian/sec.}$$

which is inversely proportional to the phase delay θ .

1.5.5 Remarks

In both types of gyrators, the two reactances placed at the input and output port tune each other because each will gyrate an inductance (or capacitance) from the capacitor (or inductor) terminated at the output port to tune the capacitor (or inductor) terminated at the input port. Meanwhile, the gyrator will also gyrate the inverse of the reactance placed at the input port to tune the reactance terminated at the output port. Although both types of the gyrator perform the same gyration function, they have different properties. In the transconductance gyrator, time delay will introduce a negative conductance when both ports are terminated with capacitors and thus they may be unstable; but thetime delay will introduce a positive resistance when both ports are terminated with inductors. For the transfer resistance gyrator the situation is reversed.

A summary of the configurations for one amplifier immittance converters, two amplifier immittance converters and the gyrators is given in Table 1.4.

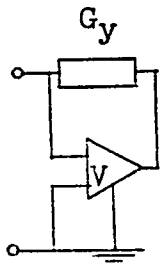
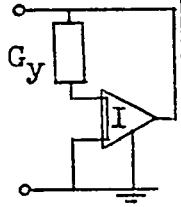
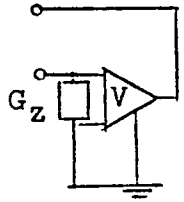
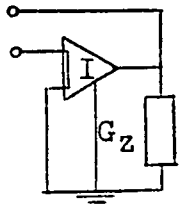
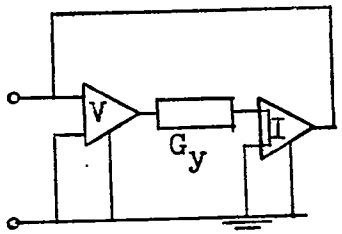
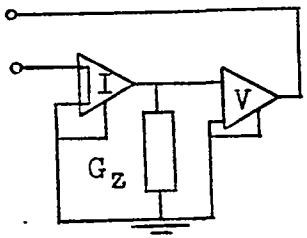
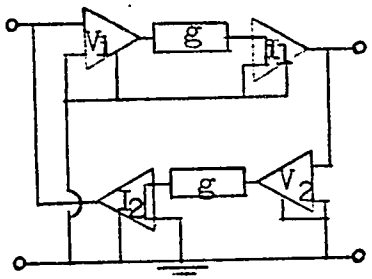
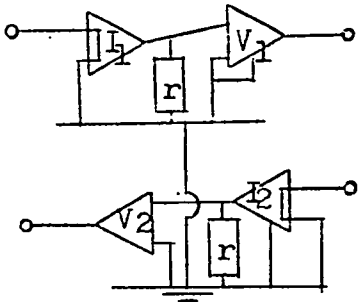
	Single Passive Immittance		Single Amplifier Immittance Converter							
Type of Input Immittance	Y	Z	Y				Z			
Condition of Stability			$(\text{Real}Y_2+\text{Real}Y_1)>0$				$(\text{Real}Z_L+\text{Real}Z_I)>0$			
Controlled	V	I	V				I			
Loop Gain			-	+	-	+	-	+	-	+
Input Immittance Due to Active Component			+	-	+	-	+	-	+	-
Amplifiers			V		I		V		I	
Block Diagrams										
Input Immittance	Y	Z	$Y_1 = G_Y(1+G_V)$		$Y_1 = G_Y(1+G_I)$		$Z_1 = G_Z(1+G_V)$		$Z_1 = G_Z(1+G_I)$	

Table 1.4 Summary of the configurations for one amplifier immittance converters, two amplifier immittance converters and immittance gyrators.

Two Amplifier Immittance Converter				Immittance Gyrator			
Y		Z		Y		Z	
$(RealY_L+RealY_I)>0$		$(RealZ_L+RealZ_I)>0$		$(RealY_L+RealY_I)>0$		$(RealZ_L+RealZ_I)>0$	
V		I		V		I	
-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-
V + I		V + I		2(V + I)		2(V + I)	
							
$Y_1 = G_V\ G_I\ G_Y$		$Z_1 = G_V\ G_I\ G_Z$		$Y_1 = \frac{G^2}{Y_3}$ $G = G_{V1}\ g\ G_{I1}$ $= G_{V2}\ g\ G_{I2}$		$Z_1 = \frac{R^2}{Z_3}$ $R = G_{I1}\ r\ G_{V1}$ $= G_{I2}\ r\ G_{V2}$	

CHAPTER 2

RECEIVING SYSTEMS WITH ACTIVE TUNING ELEMENTS

2.1 Introduction

The introduction to the thesis gives reasons why synchronous detection systems and phase-locked-loops will be used in integrated broadcast receivers and why active tuning will be desirable for the antenna systems. Since the active circuit tuning systems which are the subject of the thesis will be used with phase-locked receiver systems, this chapter will be concerned with these systems.

The above mentioned phase-locked systems may take many forms, but they all have the general form shown in Fig. 2.1, i.e., the system provides a signal which tunes the local oscillator to the correct frequency and the same signal may be used to tune the antenna system. If the receiver is a

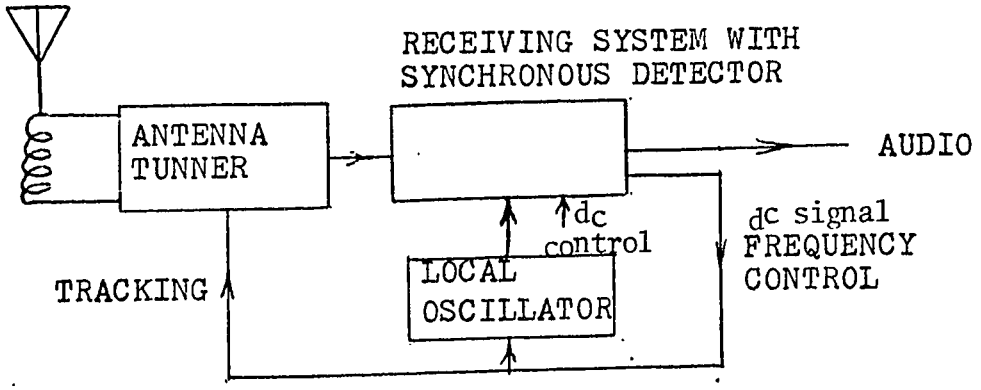


Fig. 2.1 A general form of phase-locked systems.

tuned-radio-frequency system, the local oscillator is tuned to the same frequency, as is the antenna.

This chapter will open with the general theory of phase-locked-loop systems. Then a particular system will be used as an example and finally possible tuning systems which appear to meet the requirements of the receiver system will be discussed (ref. 2.1).

An important requirement is that the antenna must be automatically tuned to the local oscillator frequency, that is, the local oscillator must track the antenna and this can be obtained by active tuning elements such as immittance converters and gyrators.

2.1.1 Phase-locked-loop

A block diagram of phase-locked-loop system is shown in Fig. 2.2 (ref. 2.2). Phase-locked loop techniques have been well developed in the literature (ref. 2.3, 2.4, 2.5, 2.6). The principle of operation is briefly as follows. The phase comparator compares the instantaneous phase of the

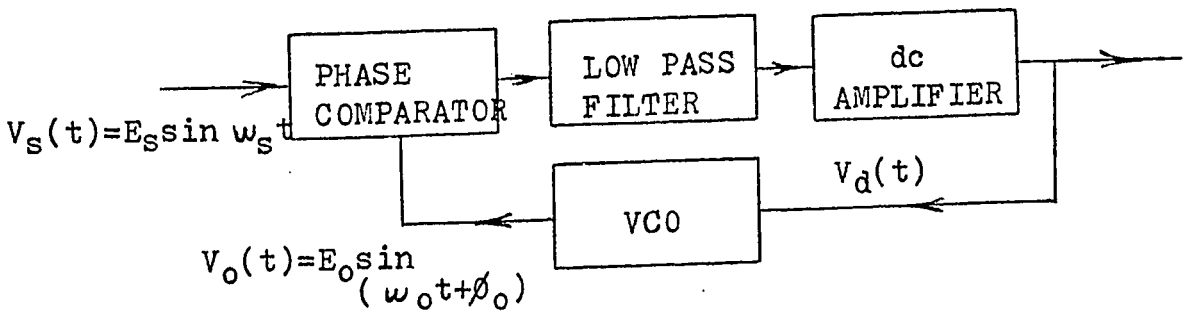


Fig. 2.2 A block diagram of phase-locked loop system

incoming signal with that of the voltage controlled oscillator (VCO) output and produces an error voltage proportional to the phase difference of the two input signals. The error voltage is filtered to reduce noise and high frequency components and then amplified. The amplifier output is used to control the VCO forming a corrective feedback loop so that the VCO varies in such a direction to reduce the phase difference between the incoming signal and its output frequency until they are locked or synchronized, if the input signal is close to the free-running frequency of the VCO or it is within its capture range. This brings out the following two significant features which make the phase-locked loop techniques compatible with the integrated circuit technology.

(a) Since the VCO automatically tunes to the carrier signal, the system does not demand high accuracy and high stability of component values which can be accomplished by integrated circuit without difficulty.

(b) Since the centre frequency f_o of the synchronization detector is equal to the carrier signal, the frequency conversion is directly from radio frequency to audio and no intermediate frequency stage is needed. The bandwidth of the radio frequency signal is determined by the low pass or audio filter.

2.1.2 A Synchronous AM Detecting System

A basic synchronous AM detecting system (ref. 2.7) is shown in Fig. 2.3. The received signal $V_s(t)$ and the synchronous local oscillator output $V_o(t)$ are mixed in the mixer, producing the desired output $V_m(t)$ which is filtered and then amplified to the desired level. The above process can be expressed mathematically as follows:

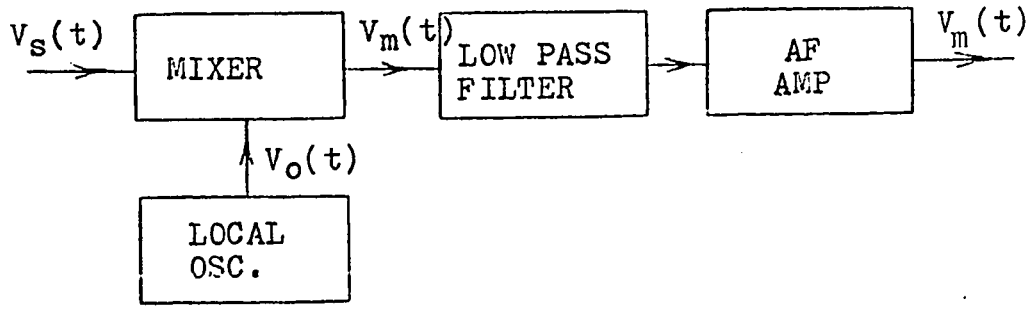


Fig. 2.3 A basic synchronous detecting system

$$\text{Let} \quad V_s(t) = A_c\left[1+S(t)\right]\cos(\omega_c t+\theta_c)$$

$$V_o(t) = A_o\cos(\omega_o t+\theta_o) \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.1)$$

The mixer output is given by

$$V_m(t) = A_cA_o\left[1+S(t)\right]\cos(\omega_c t+\theta_c)\cos(\omega_o t+\theta_o)$$

$$= \tfrac{1}{2}A_cA_o\left[1+S(t)\right]\left\{\cos\left[(\omega_c+\omega_o)t+\theta_c+\theta_o\right]\right.$$

$$\left.+\cos\left[(\omega_c-\omega_o)t+\theta_c-\theta_o\right]\right\} \ldots\ldots\ldots\ldots (2.2)$$

Because of synchronization $\omega_o = \omega_c$

$$V_m(t) = \tfrac{1}{2}A_cA_o\left[1+S(t)\right]\cos(2\omega_c t+\theta_c+\theta_o)$$

$$+\tfrac{1}{2}A_cA_o\cos(\theta_c-\theta_o)+\tfrac{1}{2}A_cA_oS(t)\cos(\theta_c-\theta_o)$$

$$\ldots\ldots\ldots\ldots (2.3)$$

After filtering, the output is

$$V_m(t) = \tfrac{1}{2}A_cA_oS(t)\cos(\theta_c-\theta_o)$$
$$= CS(t)\cos\theta_f \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2.4)$$

where $C = \frac{1}{2}A_cA_o$ and $\theta_f = \theta_c-\theta_o$. θ_f is the phase difference between the received carrier and the local oscillator frequency. $V_m(t)$ is maximum when $\theta_f = 0$ and zero when $\theta_f = 90^o$. Thus to obtain the maximum output not only the oscillator frequency must be equal to the carrier frequency but also the phase angle of the oscillator frequency must be equal to that of the carrier frequency. Fig. 2.4 is a complete AM synchronous detecting system which meets the requirements. It is a two phase synchronous detection system: the in-phase and the quadrature-phase.

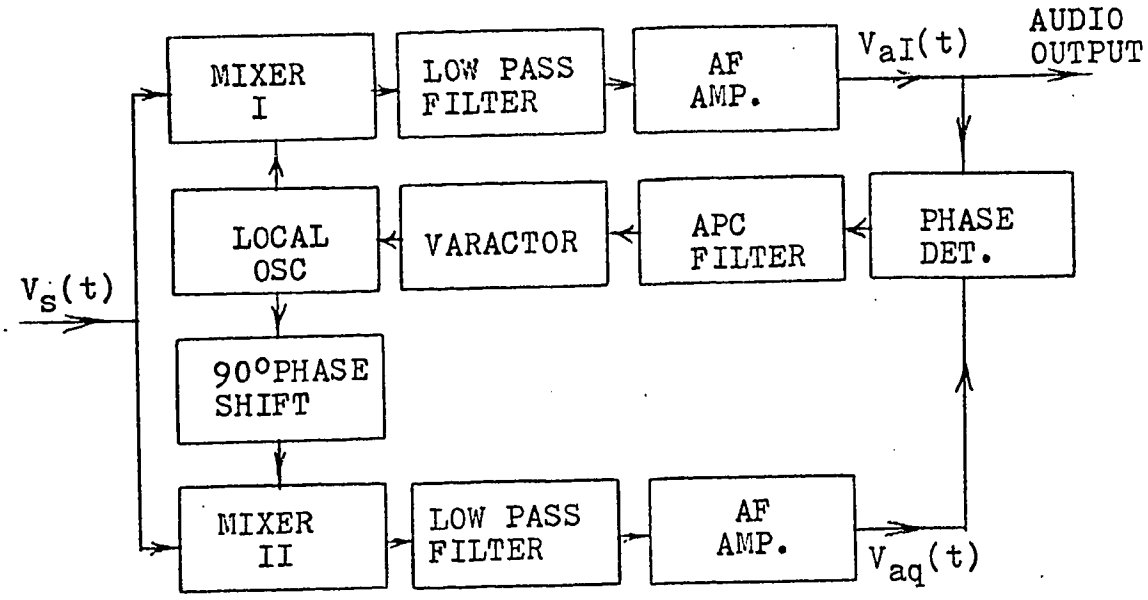


Fig. 2.4 A complete synchronous AM detector

If there is no frequency and phase difference between the received carrier and the local oscillator, the in-phase channel will give maximum audio output while the quadrature-phase channel give zero output due to the 90^{o} phase shift in it. The phase detector will produce no phase-correcting voltage. If there is a phase error in the local oscillator output, the audio output in the in-phase channel is reduced while some will present in the quadrature phase channel. The phase detector will produce a dc phase correcting voltage whose magnitude depends on the phase error and whose sign depends on the sign of the phase error. After passing through the automatic phase control (APC) filter, the dc voltage is applied to the varactor thereby correcting the phase angle of the local oscillator frequency. Such a phase control loop will not only control the local oscillator phase angle but also correct its frequency over a few KHz in AM broadcast band.

2.1.3 Tracking the Antenna with the Local Oscillator

Active tuning elements such as immittance converters which can change the magnitude of the immittance of one element of a tuned circuit can be used to tune the antenna or the local oscillator. Gyrator is another form of active tuning element which can change the inverted magnitude of an immittance, which is one element of a tuned circuit, can also be used to tune the antenna or the local oscillator. However, it is easier to track two similar active tuning elements fabricated on a silicon ship than if they are of different kind.

Thus with two similar active tuning elements on a chip, one is used for the antenna tuner and one for the local oscillator, the tracking problem will be solved. There are three feasible sets of active tuning elements listed in Table 2.1 that could be used for this tracking purposes.

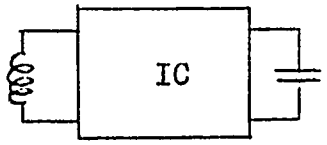
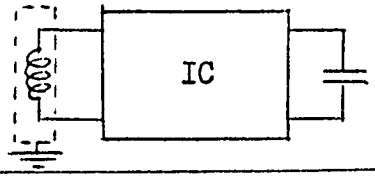
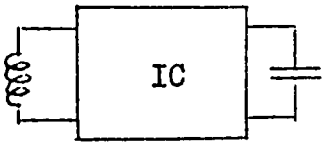
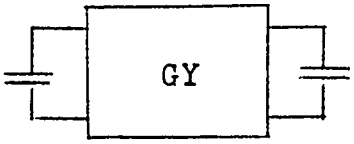
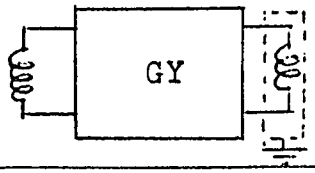
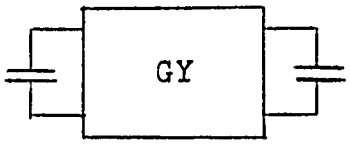
CASE	ANTENNA	LOCAL OSCILLATOR
1		
2		
3		

Table 2.1 Three feasible sets of active tuning elements

Case I Employs two identical immittance converters as the active tuning elements and two identical pairs of passive elements L and C. Due to fabrication discrepancies, final tracking adjustments can be made by trimming the trimmer across C or adjusting the inductance in the local oscillator. Good screening for this inductance is essential.

Case II An immittance converter is used to tune the antenna and a gyrator is used for the local oscillator. This scheme replaces one inductor with a capacitor and thus has the following advantages:

(1) Capacitors can be made in integrated circuits but inductors cannot

(2) Inductors are generally more expensive than capacitors.

(3) It eliminates the screening problem for the inductor. The screening problem for the capacitor is not difficult. Because of the very small distance between its two plates, its stray capacitance associated with the nearby objects is small compared with its original value and screening can be done by proper arrangement of the two plates and earthing one of them, thus eliminating the external electrostatic effects. But inductors will extract and store electromagnetic energy from the space and also have mutual coupling with its nearby objects and thus it needs careful screening by housing it properly in an earthed high conductivity metal can. However, as this scheme employs two different active elements, it is not so easy for them to track as for one with two similar active elements.

Case III Two identical gyrators are employed, one for the antenna tuner and one for the oscillator. Both inductors are on the antenna tuner. One of them may be screened or both unscreened (thus eliminating the screening problem)

and placed 90° to each other in order to produce a better receiving field pattern. Final tracking adjustments can be made by trimming the trimmers added across the two capacitors.

CHAPTER 3

CIRCUIT REALIZATION

3.1 Introduction

This chapter will consider the circuit realization of the immittance converters and gyrators treated in Chapter 1. The immittance converters and gyrators are partitioned into voltage and current amplifiers which are the basic building blocks. In addition, constant current sources and current gain control are employed in all the circuit realizations. They are also considered as basic building blocks. Thus, it is most convenient to realize these blocks first and then employ them to realize the separate immittance converters and gyrators. The capacitors and inductors terminated at the series and shunt ports are conventional passive elements and need no further description.

It was shown in Chapter I that there are two possible forms to employ the immittance converter to tune the antenna, i.e., the high pass form and the low pass form. It was shown that the time delay in the high pass form introduces a loss factor whereas in the low pass form a negative parasitic impedance. Thus for reasons of stability the high pass form is preferred and chosen for realizations.

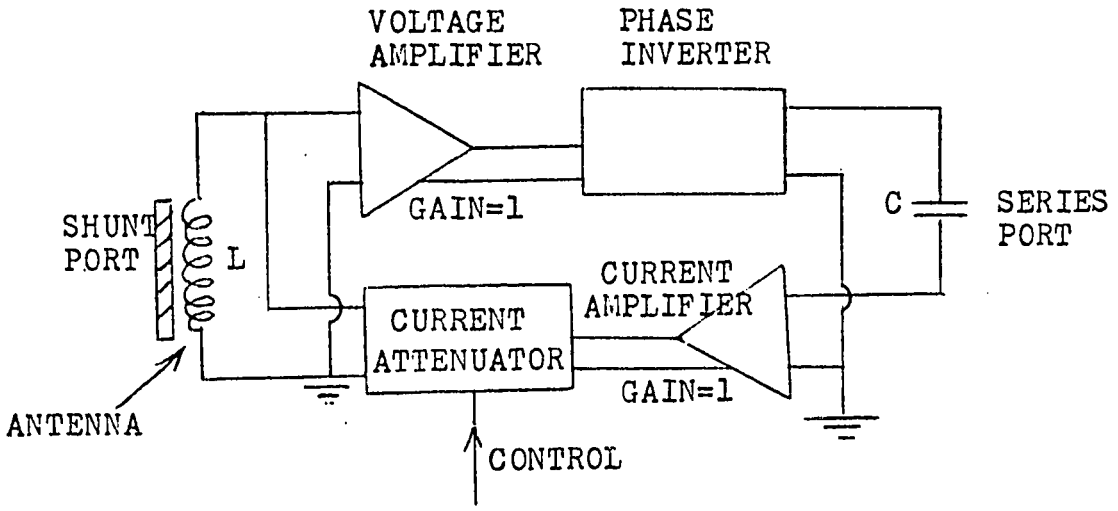


Fig. 3.1 A system diagram for the immittance converter in the high pass form to tune the antenna

3.1.1 Realizations of the High Pass Form Two Amplifier Immittance Converter

A block diagram of a convenient two amplifier immittance converter system is shown in Fig. 3.1. It consists of a unity gain voltage amplifier, unity gain current amplifier, current gain control, constant current sources, voltage level shifting and phase inversion for overall negative feedback.

3.1.2 Voltage Amplifier

The block diagram of a unity gain voltage amplifier is shown in Fig. 3.2 and its ideal characterisitcs are input impedance $Z_1 = \infty$, output impedance $Z_o = 0$ and time delay $t_d = 0$. Because $Z_1 = \infty$ and $Z_o = 0$, its current gain and

power gain are infinite.

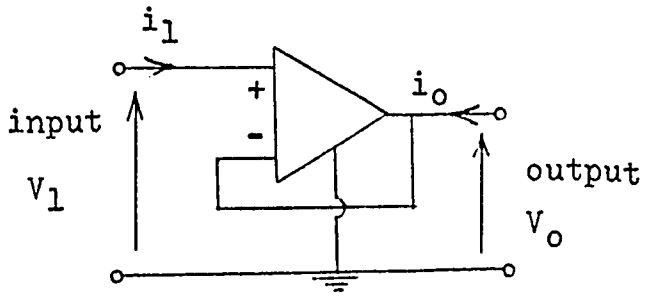


Fig. 3.2 A unity gain voltage amplifier

Unity gain (ref. 3.1) is employed, because it is easy to obtain by using a differential amplifier with a feedback factor $\mu = -1$ (obtained by returning the output to one of the inputs as shown in Fig. 3.2). For example, if the voltage gain $G_V = 10^6$, the amplifier gain G_{Vo} with feedback factor $\mu = -1$ is

$$G_{Vo} = \frac{G_V}{1-\mu G_V} = \frac{10^6}{1+10^6} = .999999$$

which is accurate to 0.0001%. If $G_V = \infty$, $G_{Vo} = 1$. Component variations due to temperature changes or aging may cause considerable changes in G_V but negligible changes in G_{Vo}, i.e. the unity gain is insensitive to component variations. This is an important characteristic as the immittance conversion ratio depends on the amplifier gain.

As the current gain A_i of a voltage amplifier is

closely related to the performance of an active tuning circuit, the following will consider

(1) the relation of A_i of the voltage amplifier, its input impedance Z_1 and output impedance Z_o, and

(2) the relation of A_i and the Q of a L C tuned circuit, when they are incorporated in an active tuning loop.

(1) Since the current gain A_i remains unchanged with or without the series voltage negative feedback, the feedback will increase Z_1 by the same factor that Z_o is reduced. Thus, when $G_{vo} = 1$

$$\frac{i_o}{i_1} = A_{io} = A_i$$

But $$\frac{i_o}{i_1} = \frac{Z_1}{Z_o}$$

Thus $$A_{io} = A_i = \frac{Z_1}{Z_o} \quad \text{.....} \quad (3.1)$$

(2) If the amplifier is used in active tuning and assuming a lossless LC circuit, Z_o will be in series with the LC circuit and Z_1 in shunt with it as shown in Fig. 3.3. The final Q of the circuit is given by

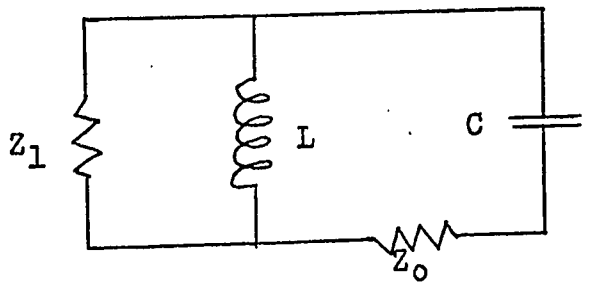


Fig. 3.3 Effect of amplifier loss on LC circuit

$$Q = \frac{\omega L}{\frac{(\omega L)^2}{Z_1} + Z_o} \qquad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.2)$$

$$\text{if } Z_1 >> \omega L$$

As seen from eq. 3.1, a large current gain is required for high Q. Field effect transistors have an extremely high A_i ($A_i = 10^6$, say). However, they are not generally compatible with integrated circuits. Thus bipolar transistors will be considered, but because of their small current gain ($A_i \approx 10^2$), three cascaded stages will be required to have the same order of current gain as that of a single field effect transistor. The increased number of stages will increase the time delay t_d. As shown in sections 1.1.4, 1.2.3 and 1.5.4, t_d can introduce a positive or negative immittances. Thus extra losses or instability may be introduced. So a compromise has to be sought between A_i and t_d. The circuit diagram is shown in Fig. 3.4. A simple

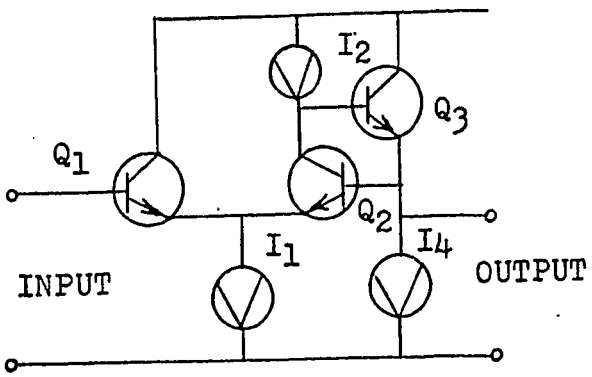


Fig. 3.4 A circuit diagram of a unity gain voltage amplifier

differential amplifier is employed to avoid time delay. As a large ratio of Z_1/Z_o is required for high Q, a large current gain A_i is needed. High Z_1 is obtained by adding an emitter follower Q_4 to the input of the differential pair and also by returning the Q_4 collector to that of Q_2 as shown dotted in Fig. 3.5 so that the negative feedback will eliminate the effect of C_{bc} of Q_4 on Z_1. Assuming the output is terminated in a low impedance (Ref. 3.5)

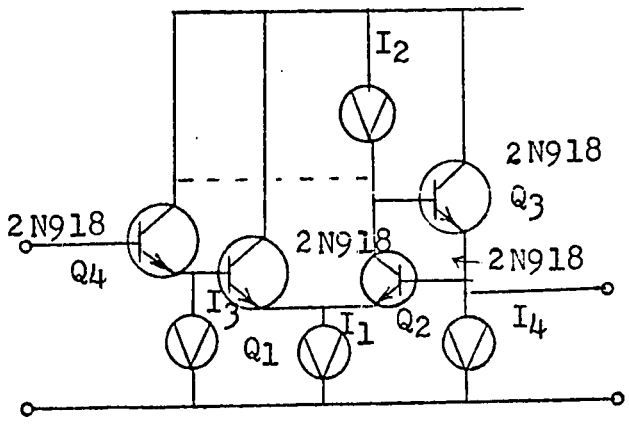


Fig. 3.5 A unity gain voltage amplifier with high input impedance

$$Z_{1V} \approx 2\beta\, r_e\, (\beta)$$
$$= 2\beta^2 r_e \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.3)$$

where $r_e = \dfrac{26}{I_E(\text{ma})}$

β = current gain of Q_1, Q_2, Q_3 and Q_4 (assumed equal)

It is noted that in Fig. 3.4 and 3.5 all resistors are replaced by constant current sources. To provide bias currents I_1, I_2, and I_3 ordinary constant current sources shown in Fig. 3.10 (a) and (b) will suffice, but to bias I_4 a constant current source with a 10×10^6 output resistance will be required so that its shunting effect across the series port will be negligible. As constant current sources will be required in the rest of the realizations, we will discuss them in the following section. As the output impedance of the voltage amplifier Z_o is the same as the input impedance Z_1 of the current amplifier, it is considered in section 3.1.4.

3.1.3 Constant Current Sources

The function of a constant current source (ref. 3.2) is to provide a constant bias current for a circuit. Its circuit symbol is shown in Fig. 3.6. Its ideal practical characteristics (shown in Fig. 3.7) are

(1) Its ac output impedance $R_o = \dfrac{\Delta V_o}{\Delta I_o} = \infty$ over the operating range.

(2) Its dc resistance $R_{dc} = \dfrac{V_o}{I_o}$ should be small.

(3) The lowest operating voltage V_o should be small.

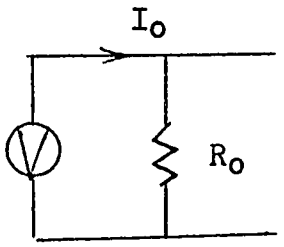


Fig. 3.6 A constant current source

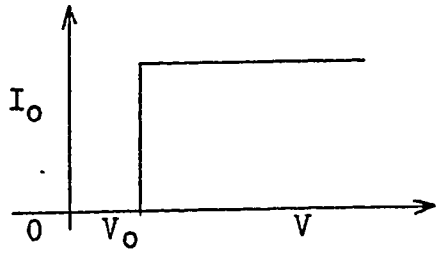


Fig. 3.7 Characteristic of an ideal practical constant current source

The above mentioned characteristics for a constant current source are not obtainable but may be approximated in practice. Non-ideal constant current sources are realized by

(1) A resistor and a DC power supply

(2) The collector of a transistor

The second method gives much superior characteristics than the former.

(I) Constant current source formed by a resistor and a DC power supply

In this method $R_o = R_{dc}$. In order to have a constant current of 1 mA and R_o = 1 MΩ, a DC power supply of $1 \times 10^{-3} \times 10^{6} = 10^{3}$ volts is required. This example illustrates the drawback of this method.

(II) Constant current source formed by the collector of a transistor

A. By the collector of a common base transistor

The output characteristics of a common base transistor is shown in Fig. 3.8. In the active region (emitter base foreward biased, collector base reverse biased), the output resistance of the collector is given by

$$R_o = r_b + r_c - \frac{r_b\,(r_b + \alpha r_c)}{R_s + r_e + r_b} \quad \ldots\ldots\ldots\ldots \quad (3.4)$$

where r_b = the base resistance

r_c = the collector resistance

r_e = the emitter resistance

and R_s = the input source resistance

R_o is of the order of megohms and provides a

good constant current source which needs a dc supply voltage of the order of one volt only. The small slope of the output characteristics in the active region is due to the following:

(a) As $I_c = \alpha I_E$, the decrease of the base width (because the space charge in the collector base junction increases towards the base as V_{CB} increases) reduces the chance of carriers recombination in the base and thus increases the α as V_{CB} increases.

(b) The decrease in base width, as V_{CB} increases, increases the charge gradient in the base and thus increases the minority carriers I_E injected across the emitter junction.

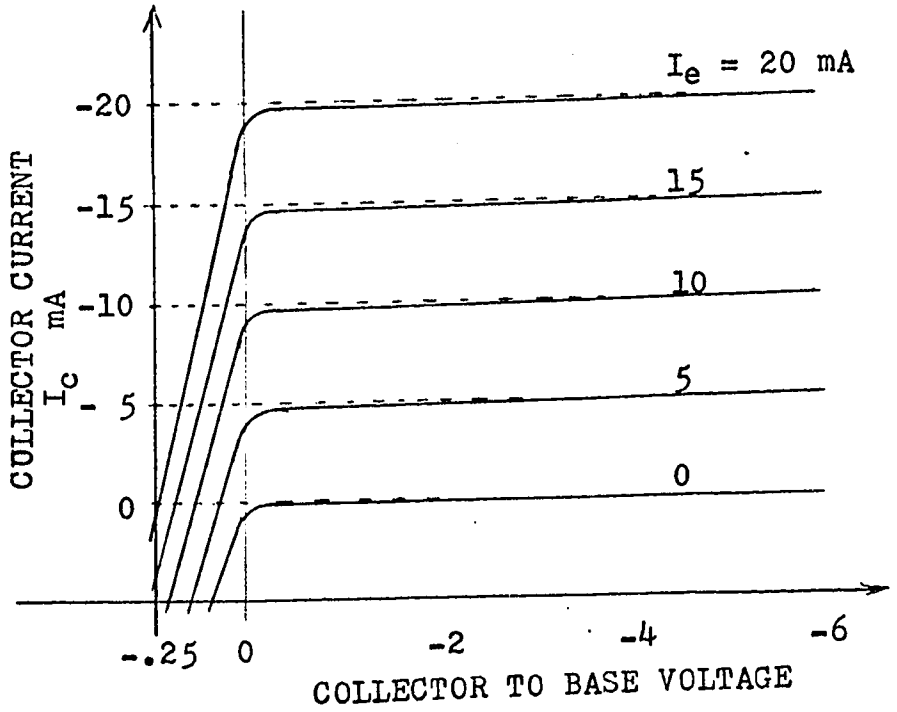


Fig. 3.8 Output characteristic of a common base transistor

B. By the collector of a common emitter transistor

The output characteristics of a common emitter of a transistor is shown in Fig. 3.9. The active region, which is beyond the knee of the curves, can be used as a constant current source with an output impedance

$$r_o = r_c(1 - \alpha) + r_e \frac{R_s + r_b + \alpha r_c}{R_s + r_b + r_e}$$

In this region, the slope of the curves is larger than those in the common base configuration because the base width modulation effect on I_c by V_{BC} mentioned above is more serious in this case. Because $I_c = \beta I_B$, assuming $\alpha = 0.98$, 0.5% change in α will cause 34% change in β.

Although common base configuration provides higher source impedance, the common emitter configuration is preferred as this form is conveniently fabricated in integrated circuit. However, stablizing circuits can be employed to improve the output impedance.

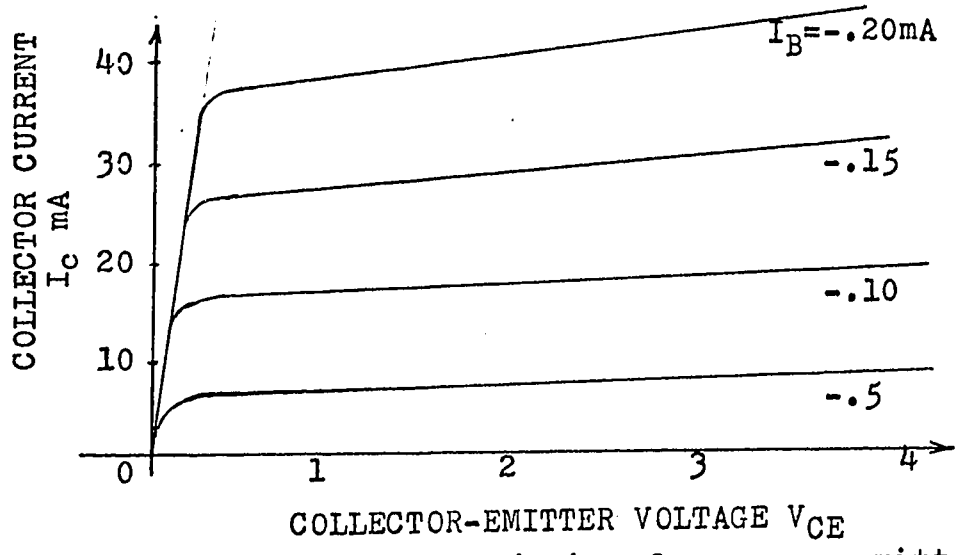


Fig. 3.9 Output characteristic of a common emitter transistor

Three constant current sources (ref. 3.2) are shown in Fig. 3.10. In Fig. 3.10 (a), R_3 stabilizes the emitter current of Q_1, it is a good constant current source but not economical in integrated form as it employs three resistors. Fig. 3.10 (b) shows a practical constant curreent source, the emitter current of Q_2 is stabilized by that of Q_1 which is connected as a diode. If Q_1 and Q_2 are identical, $i \approx \frac{V_a+V_b}{R}$ Fig. 3.10 (c) is a cascode form constant current source whose output impedance is more than 10 MΩ because of the following:

(1) The collector of Q_5 is employed as the emitter load for Q6 which stabilizes the emitter current of Q_6 extremely well.

(2) The Darlinton pair Q6 and Q_7 increases the current gain of the composite transistor. The higher the current gain the less effect of I_B on R_o. If $\beta = \infty$, $I_B = 0$ then $I_C = I_E$, the output characteristics are horizontal and $R_o = \infty$.

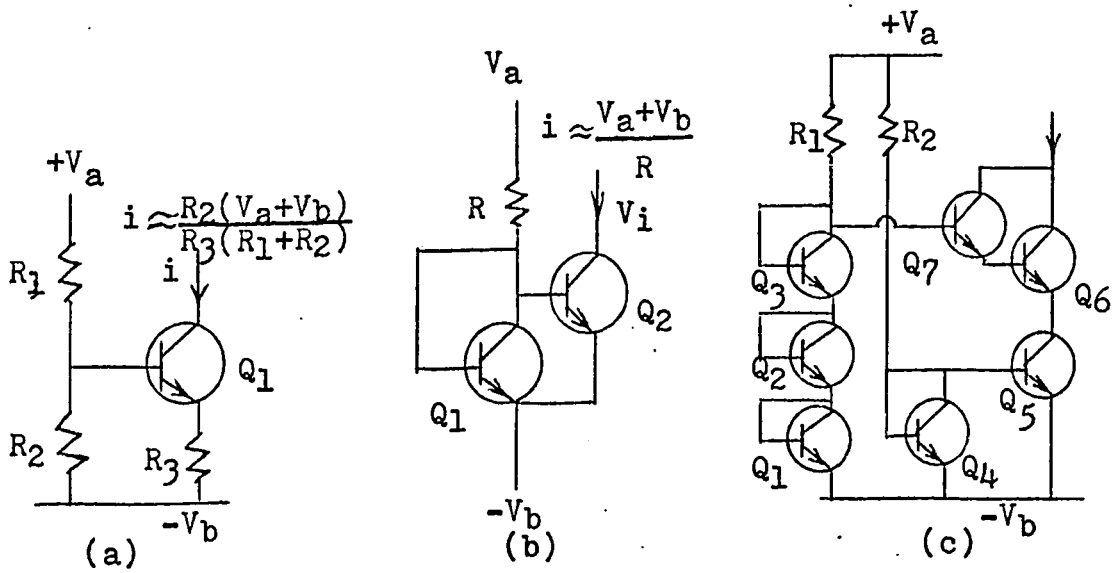


Fig. 3.10 Constant current sources

3.1.4 Unity Gain Current Amplifier

The ideal characteristics of a unity gain current amplifier are $Z_1 = 0$, $Z_o = \infty$ and $t_d = 0$. In practice, this means a low value of Z_1, a high value of Z_o, a small time delay t_d and a gain close to unity. These appear to match the characteristics of a common base transistor amplifier. However, the common base amplifier alone does not provide the required high Z_o and low Z_1. Other circuit techniques such as negative feedback are employed to reduce Z_1 and cascode form output to increase Z_o. Fig. 3.11 shows the circuit diagram of the current amplifier. The large time delay is avoided by the short feedback loop and the high α cut-off frequency of the common base configuration.

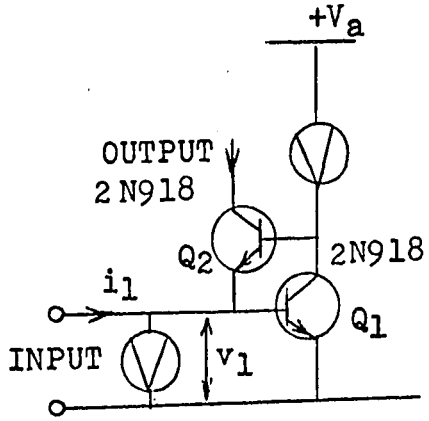


Fig. 3.11 A unity gain current amplifier

Q_1 is a voltage amplifier whose output is fed back to the base of the common base amplifier Q_2 in order to obtain low Z_1. Bias is provided by the constant current sources.

An approximate treatment is given below.

$Z_1 = \frac{V_1}{i_1}$ where V_1 is the input voltage and i_1 the input current.

But $v_1 \approx i_{c1} r_{e1}$, thus $Z_1 \approx \frac{i_{c1} r_{e1}}{i_1}$

But $i_{c1} \approx \frac{i_{e2}}{\beta_2}$ thus $Z_1 \approx \frac{i_{e2}}{\beta_2} \cdot \frac{r_{e1}}{i_1}$

But $i_{e2} \approx i_1$, thus $Z_1 \approx \frac{r_{e1}}{\beta_2}$ ..... (3.5)

Experimentally Z_1 given by eq. 3.5 is valid at low frequencies, but increases at high frequencies (see Fig. 4.1) and reduces the Q to an unacceptable value. This is unexplainable by the well known relation $\beta = \frac{f_\alpha}{f_\beta}$ (where β is the common emitter current gain at low frequency, f_α is the 3 db α cut off frequency and f_β is the 3 db β cut off frequency).

As f_α = 600 MHz for transistors 2N918 and β = 100, then f_β = 6 MHz. But experimentally f_β = 1.3 MHz. Evidently, the parasitic effects due to the stray capacitances C_{be1} and C_{be2} at the emitter base of Q_1 and Q_2 at high frequencies must be considered. C_{be2} has a larger shunting effect on Z_1 as its capacitance is magnified by the voltage gain G_v of Q_1. Thus the total stray admittance shunting the input is

$$Y_{Sh} = j\omega C_{be1} + j\omega C_{be2} (1+G_v) \quad \ldots\ldots\ldots\ldots \quad (3.6)$$

In future work, accurate circuit analysis and redesign the amplifier for low Z_1 throughout the operating frequency range are required.

3.1.5 Current Gain Attenuator

A method used to control the current gain is shown in Fig. 3.12. This is a conventional method which is used by integrated circuit manufacturers (ref. 3.3) eg., in receiver automatic gain control systems.

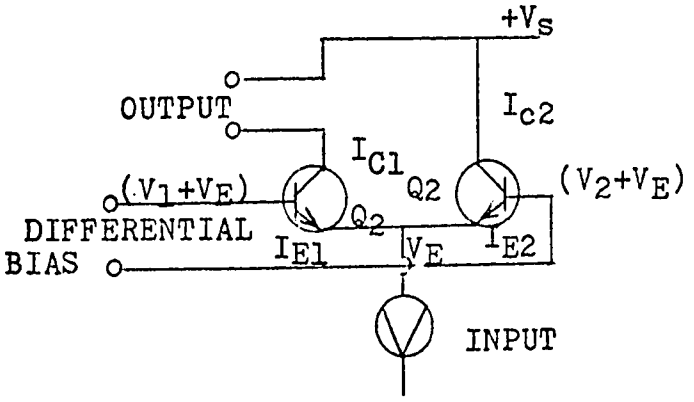


Fig. 3.12 A current gain attenuator

The current gain M is defined by

$$M \approx \frac{I_{c1}}{I_{c1}+I_{c2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.7)$$

where $I_{c1} + I_{c2} \approx I_{E1} + I_{E2} = I_{dc}$ is supplied by the constant current source and $1 \geq M \geq 0$.

The ratio of the collector currents $\frac{I_{c1}}{I_{c2}}$ can be controlled by a differential bias voltage (V_1-V_2) at the bases of Q_1 and Q_2; the relation between the bias and the current gain is developed below.

It is well known that the dc voltage current relation (Fig. 3.13) for an ideal pn junction is given by

$$I = I_o^{'1} (e^{qV/kT} - 1) \quad \ldots\ldots\ldots\ldots \quad (3.8)$$

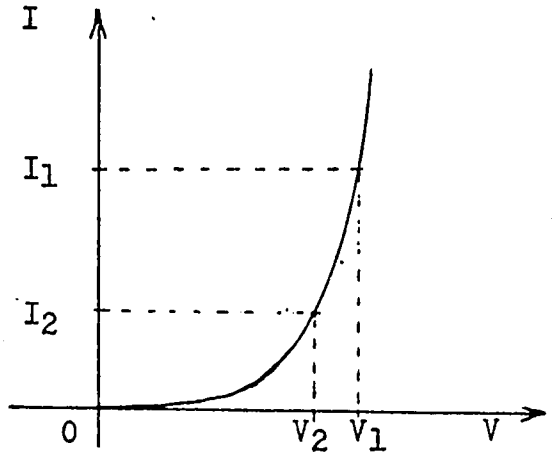


Fig. 3.13 dc voltage and current relation of an ideal pn junction

where $q = 1.6 \times 10^{-19}$ Coulomb, the electron charge

V = the applied voltage across the pn junction

$k = 1.38 \times 10^{-23}$ joule/°K, Boltzmann's constant

$$I_o' = A' q \left(\frac{p_{no} D_p}{L_p} + \frac{n_{po} D_n}{L_n}\right)$$ the saturation current

where A' = area of the junction in cm^3

p_{no} = acceptor carrier density (cm^{-3}) in the N region

n_{po} = donor carrier density (cm^{-3}) in the P region

D_p & D_n = diffusion constants for holes and electrons respectively

L_p = diffusion length of holes in the N region in cm

L_n = diffusion length of electron carriers in the P region in cm

For the same type of npn transistors and assuming uniformity of the emitter base junction, the collector

currents of Q_1 and Q_2 are respectively,

$$I_{c1} = \beta_1 I_{B1} = \frac{\tau_{B1}}{\tau_{\eta 1}} I'_{o1} \left(e^{\frac{qV_1}{kT_1}} - 1\right)$$

$$= \frac{\tau_{B1}}{\tau_{\eta 1}} A'_1 q \left(\frac{p_{no}D_p}{L_{p1}} + \frac{n_{po}D_n}{L_{n1}}\right) \left(e^{\frac{qV_1}{kT_1}} - 1\right) \quad \ldots \quad (3.9)$$

And $$I_{c2} = \beta_2 I_{B2} = \frac{\tau_{B2}}{\tau_{\eta 2}} \cdot I'_{o2} \left(e^{\frac{qV_2}{kT_2}} - 1\right)$$

$$= \frac{\tau_{B2}}{\tau_{\eta 2}} A'_2 q \left(\frac{p_{no}D_p}{L_{p2}} + \frac{n_{po2}D_n}{L_{n2}}\right) \left(e^{\frac{qV_2}{kT_2}} - 1\right) \quad \ldots \quad (3.10)$$

where τ_{B1}, τ_{B2} electron carrier life time in the base of Q_1 and Q_2 respectively

$\tau_{\eta 1}$, $\tau_{\eta 2}$ electron carrier transit time through the base of Q_1 and Q_2 respectively

From eq. 3.9 and 3.10

$$\frac{I_{c1}}{I_{c2}} = \frac{\frac{\tau_{B1}}{\tau_{\eta 1}} A'_1 q \left(\frac{p_{no1}D_p}{L_{p1}} + \frac{n_{po1}D_n}{L_{n1}}\right) \left(e^{\frac{qV_1}{kT_1}} - 1\right)}{\frac{\tau_{B2}}{\tau_{\eta 2}} A'_2 q \left(\frac{p_{no1}D_p}{L_{p2}} + \frac{n_{po2}D_n}{L_{p1}}\right) \left(e^{\frac{qV_2}{kT_2}} - 1\right)}$$

$$\log_e \frac{Ic1}{Ic2} = \log_e \frac{\frac{\tau_{B1}}{\tau_{\eta 1}} A'_1 q \left(\frac{p_{no1}D_p}{L_{p1}} + \frac{n_{po1}D_n}{L_{n1}}\right)}{\frac{\tau_{B2}}{\tau_{\eta 2}} A'_2 q \left(\frac{p_{no2}D_p}{L_{p2}} + \frac{n_{po2}D_n}{L_{n2}}\right)}$$

$$+ \frac{q}{k} \left(\frac{V_1}{T_1} - \frac{V_2}{T_2}\right) \quad \ldots \ldots \ldots \ldots \ldots \quad (3.11)$$

In integrated circuit Q_1 and Q_2 are fabricated on a silicon chip. Since they are made under the same diffusion and doping conditions, then the following equalities hold within a reasonable degree of accuracy, certainly better than 1%.

$$\begin{aligned} \tau_{B1} &= \tau_{B2} \\ \tau_{\eta 1} &= \tau_{\eta 2} \\ p_{no1} &= p_{n02} \\ n_{po1} &= n_{po2} \\ L_{p1} &= L_{p2} \\ L_{n1} &= L_{n2} \end{aligned} \qquad \ldots\ldots\ldots\ldots \quad (3.12)$$

Also $T_1 = T_2 = T$

since both the junctions are on the same chip. However, because of the limitations of the photolithography, the equality $A_1' = A_2'$ may not hold to the same degree of accuracy.

Using eq. 3.12, eq. 3.11 becomes

$$\log_e \frac{I_{c1}}{I_{c2}} = \log \frac{A_1'}{A_2'} + \frac{q}{kT}(V_1 - V_2)$$

$$\log_e \frac{I_{c1}A_2'}{I_{c2}A_1'} = K'(V_1 - V_2) \qquad \ldots\ldots\ldots\ldots \quad (3.13)$$

where $\frac{q}{kT} = K'$, a constant. Eq. 3.13 shows that the dc collector current I_{c1} and I_{c2} divides in such a way that the

logarithm of the ratio $\frac{I_{c1}A_2'}{I_{c2}A_1'}$ is proportional to the dc differential bias $(V_1 - V_2)$. If ac signal currents are superimposed on I_{c1} and I_{c2}, it is shown below that they will divide in the same ratio as that of I_{c1} and I_{c2}. From eq. 3.8, the small signal resistance of the diode is

$$r = \frac{dV}{dI} = \frac{kT}{q} \cdot \frac{1}{I}$$

Thus the small signal resistance of the emitter and base of Q_1 is

$$r_1 = \frac{dV_1}{dI_{E1}} = \frac{kT}{q} \cdot \frac{1}{I_{E1}} = \frac{K}{I_{E1}}$$

where $K = \frac{kT}{q}$

Similarly,

$$r_2 = \frac{K}{I_{E2}}$$

$$\therefore \frac{r_1}{r_2} = \frac{I_{E2}}{I_{E1}} \approx \frac{I_{c2}}{I_{c1}} \quad \text{.....} \quad (3.14)$$

If a signal voltage v_1 is applied at the emitter of Q_1 and Q_2

$$i_1 = \frac{v_1}{r_1} \text{ and } i_2 = \frac{v_1}{r_2}$$

Thus $$\frac{i_1}{i_2} = \frac{r_2}{r_1} \quad \text{.....} \quad (3.15)$$

Using 3.13, 3.14 and 3.15,

$$\log_e \frac{i_1}{i_2} = \log_e \frac{I_{c1}}{I_{c2}} = \log_e \frac{A_1'}{A_2'} + K(V_1-V_2),$$

$$\log_e \frac{i_1 A_2'}{i_2 A_1'} = \log_e \frac{I_{c1} A_2'}{I_{c2} A_1'} = K(V_1-V_2) \quad \ldots\ldots\ldots\ldots \quad (3.16)$$

Eq. 3.16 (see also eq. 3.9 and 3.10) is used to determine the current gain M which is defined by eq. 3.7. Thus when $V_2 = 0$, $I_{c2} = 0$, then $M \approx 1$. Also when V_2 increases, I_{c2} increases and M decreases.

Two emitter coupled pairs fabricated on a chip and with a common bias arrangement as shown in Fig. 3.14, one pair can be used for example, the current gain control on the antenna tuning system (sect. 2.1.4) and the other pair for the current gain control in the local oscillator.

Using eq. 3.16

$$\log_e \frac{I_{c1}}{I_{c2}} \cdot \frac{A_2'}{A_1'} = \log_e \frac{I_{c3} A_4'}{I_{c4} A_3'} = K(V_1-V_2) \quad \ldots\ldots\ldots \quad (3.17)$$

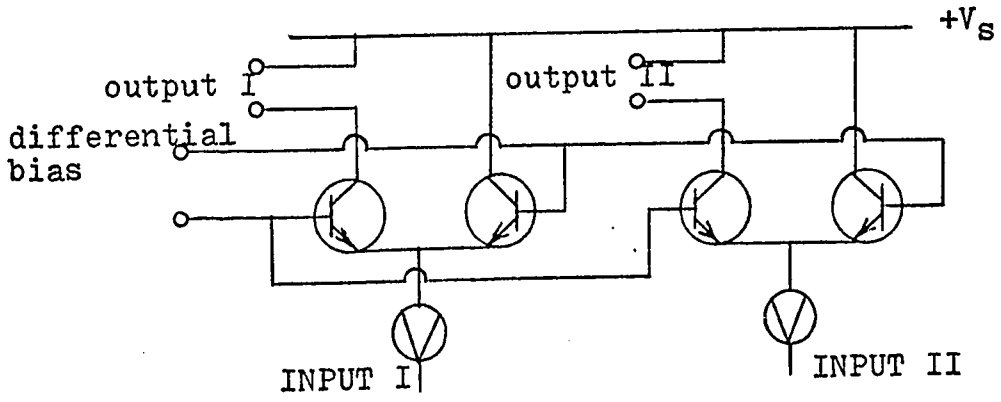


Fig. 3.14 Two emitter coupled pairs on a chip with a common bias arrangement

Providing $\frac{A_2'}{A_1'} = \frac{A_3'}{A_4'}$ then $\frac{I_{c1}}{I_{c2}} = \frac{I_{c3}}{I_{c4}}$ perfect tracking can be obtained. But because of the resolution limiations of the photolithography (usually $A_1' \approx A_2' \approx A_3' \approx A_4'$) trimer capacitors may have to be added to the fixed capacitors in the immittance converters (see table 2.1) to obtain satisfactory tracking between the antenna and the oscillator.

Cascode output to increase output impedance

Because of the small input resistance r_e at the emitters of Q_1 and Q_2, the collector output impedance of Q_1

$$r_o = r_c (1-\alpha) + r_e \cdot \frac{R_S + r_b + \alpha_{rc}}{R_S + r_p + r_e}$$

is not high enough to meet the requirements. A cascode (ref. 3.4) form output is shown in Fig. 3.15. The collector output impedance r_o of Q_1, is employed as the emitter load,

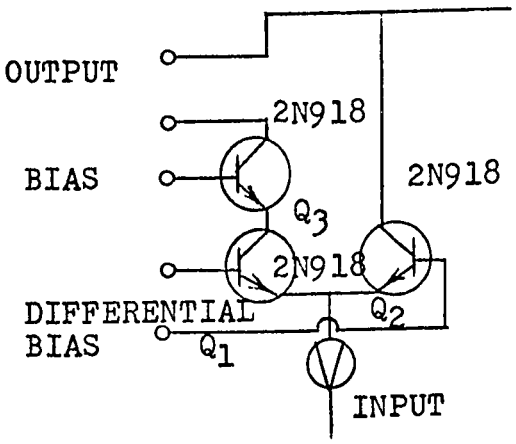


Fig. 3.15 A current gain attenuator with cascode output

r_e of Q_3, thus obtaining the high output impedance. Alterna-

tively, the tracking mentioned above may be obtained by a feedback technique which will force the ratio $\frac{I_{c3}}{I_{c4}}$ to equal $\frac{I_{c1}}{I_{c2}}$. By this method the stringent requirement on the similarity of the four PN junctions is eliminated.

3.1.6 Current Amplifier with a Gain Greater Than Unity

The ideal port characteristics of this amplifier are the same as those of the unity gain current amplifier discussed in the previous section, except that it has a gain greater than unity. Its block diagram is shown in Fig. 3.16. Because a low input resistance is required, the input is a unity gain amplifier and is followed by a stage with a gain greater than unity. A circuit diagram is shown in Fig. 3.17. The current gain G_I is determined primarily by R_1 and R_2, providing the conditions stated below are met.

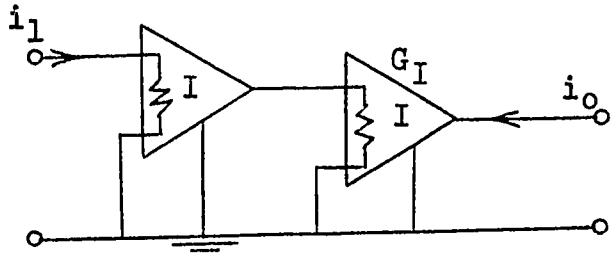


Fig. 3.16 A current amplifier with a gain greater than unity

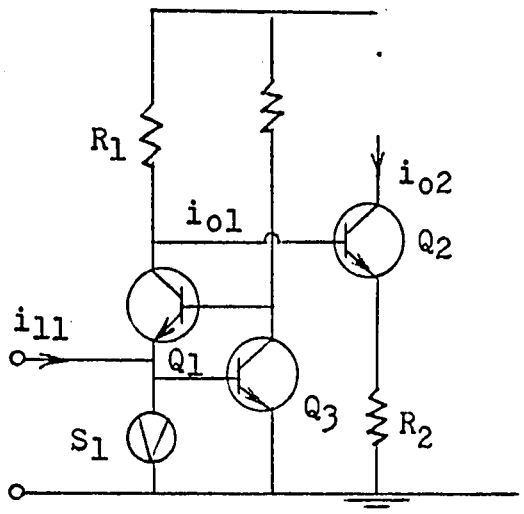


Fig. 3.17 Circuit diagram of a current amplifier with a gain greater than unity

The input resistance at the base of Q_2 is given by

$$r_{i2} = \beta\,(r_e + R_2)$$ neglecting parasitic effects associated with the base of Q_2

The current gain of the complete amplifier is given by

$$G_I \approx \frac{i_{o2}}{i_{11}}$$

$$\approx \beta_2 \cdot \frac{R_1}{\beta_2(r_e+R_2)+R_1}$$ assuming Q_1 has a unity gain

$$\approx \frac{R_1}{R_2} \text{ if } R_2 \gg r_e \;\&\; \beta_2 R_2 \gg R_1 \quad \ldots\ldots \quad (3.18)$$

Note that by using more devices to increase the current gain, the time delay is also increased. The input resistance is similar to that of the unity gain current amplifier.

3.2 Realization for the One Amplifier Immittance Converters

Eight different kinds of one amplifier immittance converter were developed in Chapter 1. A single amplifier is used to modify the value of the capacitor to tune the antenna from the broadcast band frequency of about 0.5 MHz to 1.5 MHz, and a 10:1 ratio in the change of the capacitor value is required if the stray capacitance of the antenna is considered. The characteristics of the amplifiers suitable for the eight configurations are tabulated in Table 3.1. In the integrated circuit form, bipolar transistors will be used. From Table 3.1, the voltage controlled negative immittance converter and the current controlled negative immittance converter appear to match the characteristics of a common base bipolar transistor. It is noted that in the configurations, it is possible to realize the current gain required with very small phase delay. As shown in section 1.1.4, 1.2.3, 1.3.3 and 1.5.4, time delay can introduce parasitic immittances. From Table 1.1, for voltage controlled negative immittance converter if $G_y = j\omega C$ (Fig. 3.18), the time delay t_d introduces a negative conductance $-\omega C\theta_I B_I$ ($\theta_I = t_d\omega$); if $G_y = \frac{1}{j\omega L}$, a positive conductance $\frac{\theta_I B_I}{\omega L}$. For the current controlled negative immittance converter, when $G_z = \frac{1}{j\omega C}$ (Fig. 3.19), the time delay introduces a positive resistance $\frac{\theta_1 B_1}{\omega C}$; when $G_z = j\omega L$, a negative resistance $-\omega L\theta_I B_I$.

	Voltage Controlled				Current Controlled			
Sense of Feedback	-	+	-	+	-	+	-	+
Type	+	-	+	-	+	-	+	-
Amplifier Employed	V	V	I	I	I	I	V	V
Amplifier Gain for 10:1 change in the Capacitor Value	0 to -9	0 to +0.9	0 to +9	0 to -0.9	0 to +9	0 to -0.9	0 to -9	0 to +0.9
Preferred Amplifier Input Impedance	∞	∞	0	0	0	0	∞	∞
Preferred Amplifier Output Impedance	0	0	∞	∞	∞	∞	0	0
Preferred Amplifier Time Delay	0	0	0	0	0	0	0	0

Table 3.1 Preferred Amplifier Characteristics for One Amplifier Immittance Converter

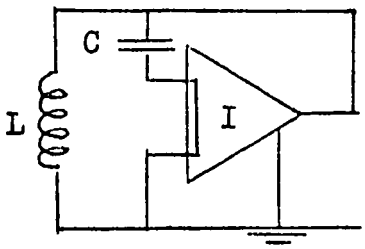


Fig. 3.18 A voltage controlled negative immittace converter

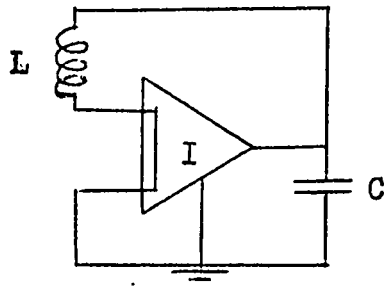


Fig. 3. 19 A current controlled negative immittance converter

Note that the magnitude of the immittances due to the time delay t_d are proportional to the product of the phase delay $\theta(\theta = \omega t_d)$ and the amplifier gain B_I. Thus t_d must be reduced so that it does not cause system instability where it introduces negative immittances; and causes minimum circuit losses, required by high Q, where it introduces positive immittances.

Alternatively, the effect of time delay t_d can be shown by a vector diagram. For example, for the voltage controlled negative immittance converter (Fig. 3.18), if the amplifier has no delay, Fig. 3.20 (a) shows its vector diagram. C is the passive capacitance and G is the circuit losses represented as a conductance in parallel with C. OP is the input current to a different scale. Because of positive feedback, the current amplifier introduces a current OP' (OP' = A x OP, A is the feedback factor) in opposite phase to OP, a negative capaci-

tance -AC and a negative conductance -AG. The equivalent input admittance is shown in Fig. 3.20(b). t_d will cause a phase lagging angle θ_1 as shown in Fig. 3.21 (a). OP is the input current and OP", the current feedback by the amplifier, is displaced θ_1 from its initial position OP' and it introduces a negative conductance $-G_t$. The equivalent input admittance is shown in Fig. 3.21 (b).

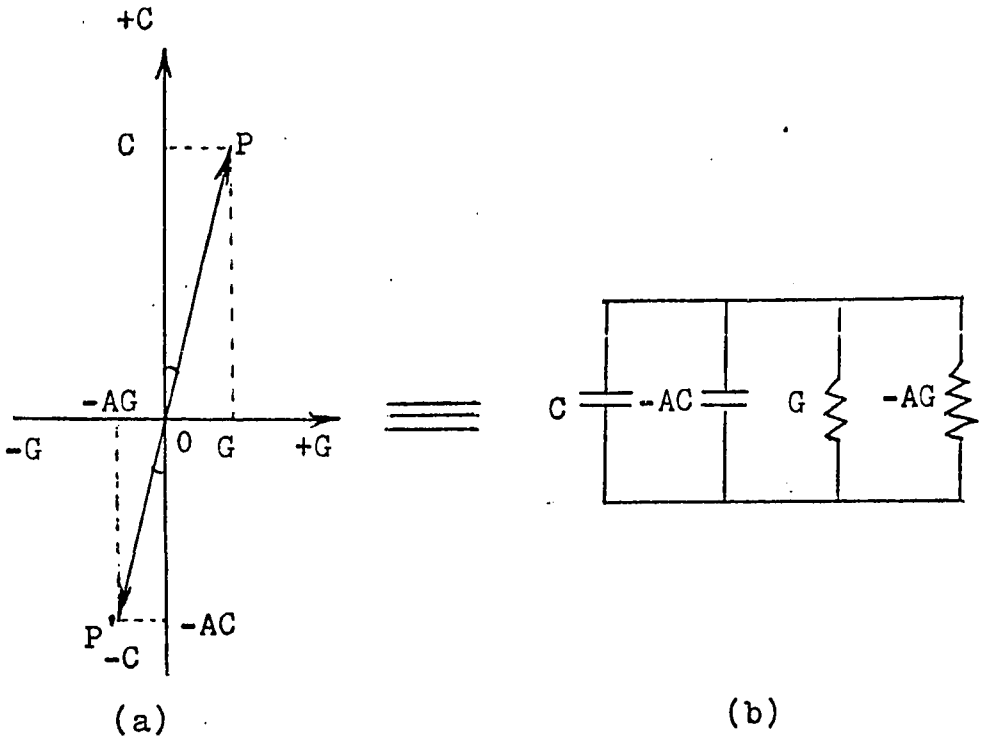


Fig. 3.20 (a) Vector diagram for a voltage controlled negative immittance converter
(b) Equivalent input admittance for (a)

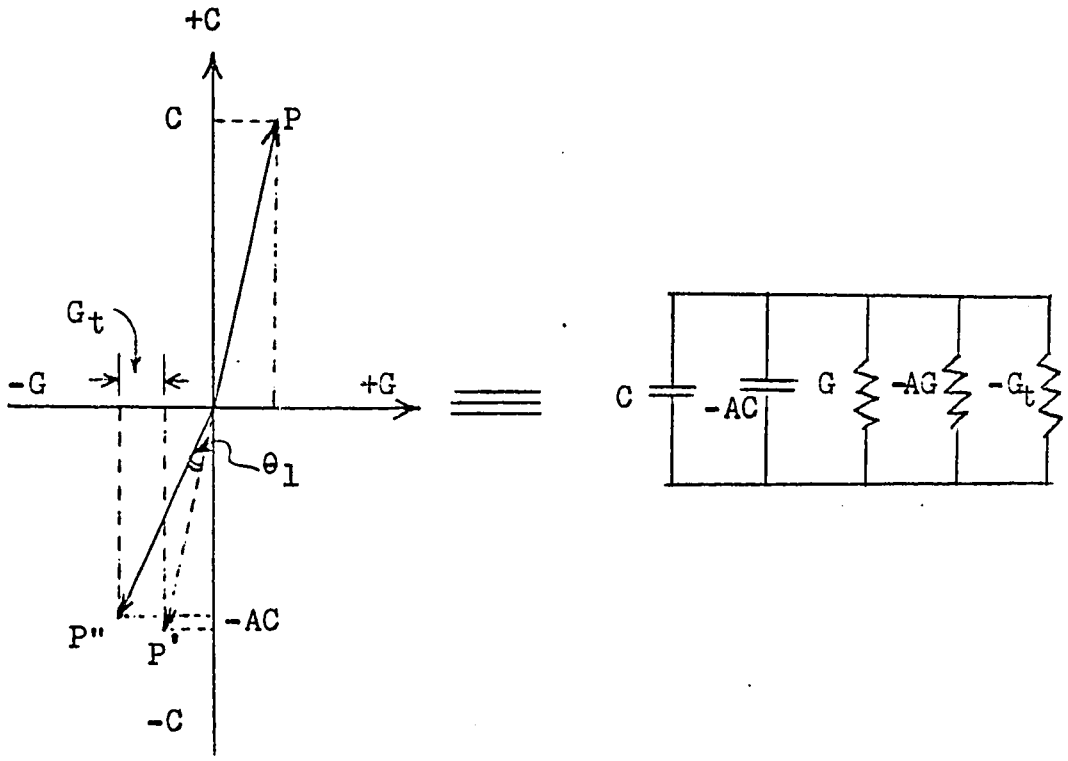


Fig. 3.21 (a) Vector diagram for a voltage controlled negative immittance converter with a phase delay angle θ_1
(b) Equivalent input admittance for (a)

Methods of finding the overall circuit Q

There are two methods of finding the overall Q of one amplifier immittance converter used in active tuning.

Method I:

Each circuit loss can be represented as a resistance in series with the tuned circuit or as a conductance in shunt with the tuned circuit as in Fig. 3.21 (b), where the overall circuit Q can be expressed as

$$Q = \frac{\omega C}{G_{total}}$$

where G_{total} is the sum of the shunt conductances.

Method II

Each circuit loss can be expressed as an angle. If the sum of the angles $\theta_{total} \leq \frac{\pi}{36}$ rad. the overall circuit $Q \approx \frac{1}{\theta_{total}}$. θ_{total} can be easily found by drawing a vector diagram. E.g., for Fig. 3.21 (a), the vector diagram is shown in Fig. 3.22, where θ_1 is the angle due to the input resistance r_1 of the current amplifier and the antenna loss. θ_t is due to the time delay. OP is the input current vector and OP" is the output current vector. Because of positive feedback, the resultant is OR. If $\theta_2 \leq \frac{\pi}{36}$ rad. $Q \approx \frac{1}{\theta_2}$

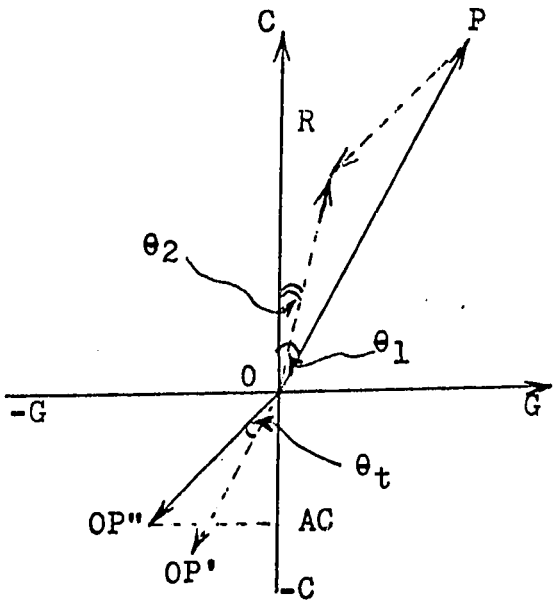


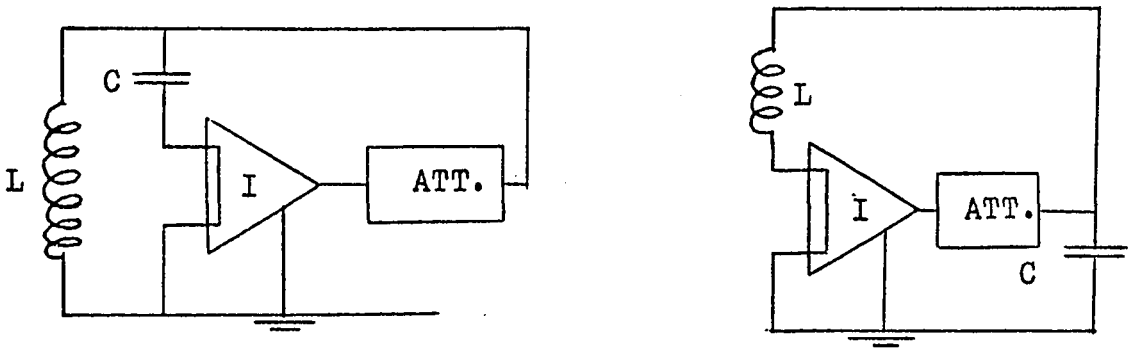
Fig. 3.22 Vector diagram to find the circuit Q of Fig. 3.21 (a)

3.3.1 A Complete Circuit for the One Current Amplifier Negative Immittance Converter

The system diagram for the voltage controlled negative immittance converter and current controlled negative immittance converter employed to tune the antenna are shown

in Fig. 3.23 (a) and (b) respectively. They consist of a current amplifier and a current attenuator.

Note that in Fig. 3.23 (a), L is in parallel with the attenuator output and C is in series with the amplifier input while in Fig. 3.23 (b), C is in parallel with the attenuator output and L in series with the amplifier input. In Fig. 3.23 (a) L has one end grounded, but in Fig. 3.23 (b), C has one end grounded. The time delay introduces a negative conductance $-\omega C\theta_I B_I$ in Fig. 3.23 (a) and a positive resistance $\frac{\theta_1 B_1}{\omega C}$ in Fig. 3.23 (b). Interchanging the positions for L and C in Fig. 3.23 (a), Fig. 3.23 (b) results and vice versa.



(a) (b)

Fig. 3.23 A system diagram for the one amplifier negative immittance converter to tune the antenna.
(a) Voltage controlled
(b) Current controlled

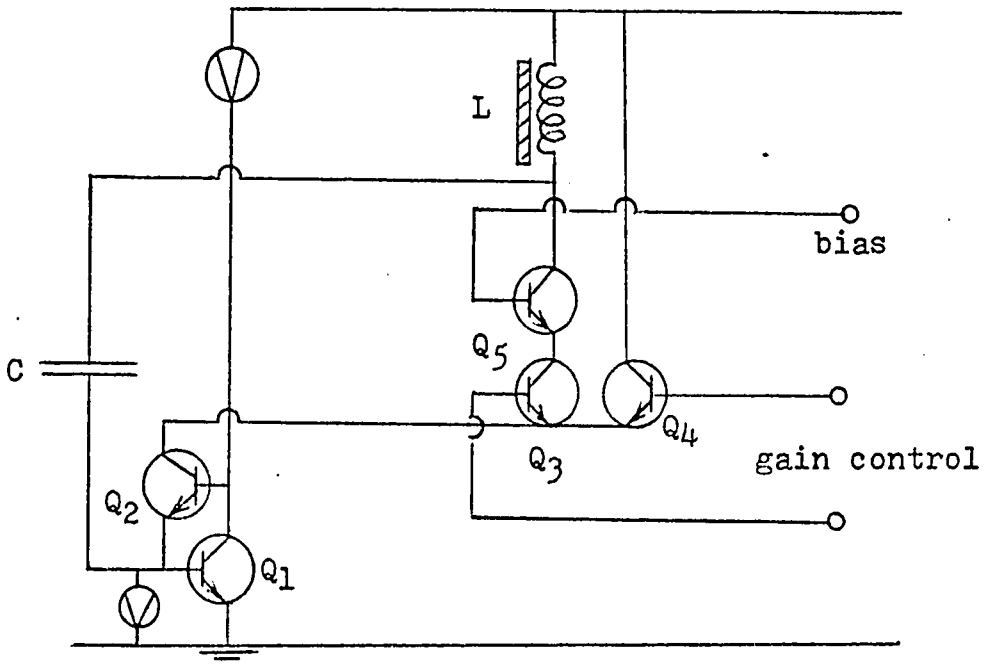


Fig. 3.24 A complete circuit for the one amplifier negative immittance converter

The circuit realization for the voltage controlled negative immittance converter of Fig. 3.23 (a) is shown in Fig. 3.24. Interchanging the positions of L and C results the realization for Fig. 3.23 (b). Thus an additional good constant current source in parallel with C is needed to bias the collector current of Q_5 in this latter case; also an additional dc blocking capacitor in series with L is required. Thus the realization shown in Fig. 3.24 is preferred.

3.2.2 A Circuit for the One Current Amplifier Positive Immittance Converter

A block diagram for a one current amplifier positive immittance converter to tune a ferrite rod antenna is shown

in Fig. 3.25. It consists of the current amplifier of Fig. 3.16 and the current attenuator of Fig. 3.15 to control the

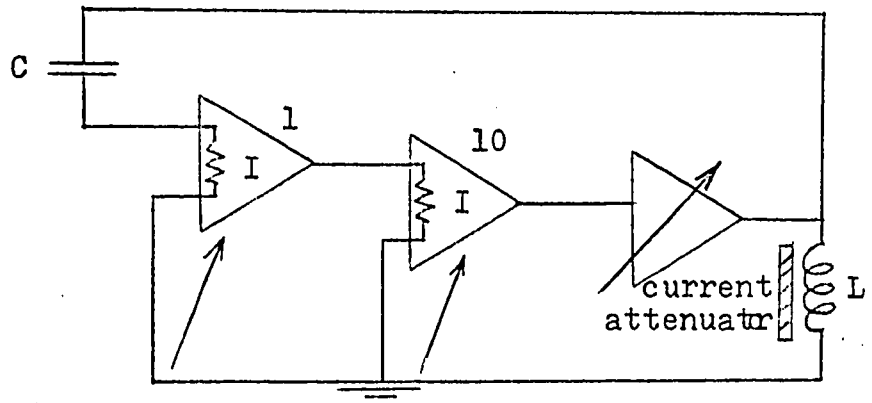


Fig. 3.25 A block diagram of a one current amplifier positive immittance converter to tune an antenna

resonant frequency. A typical circuit diagram is shown in Fig. 3.26. A block diagram and an equivalent circuit are shown in Fig. 3.27. Note that the value of C (≈20 pf) used in this circuit is much smaller than for the negative immittance converter and that it may be possible to integrate it.

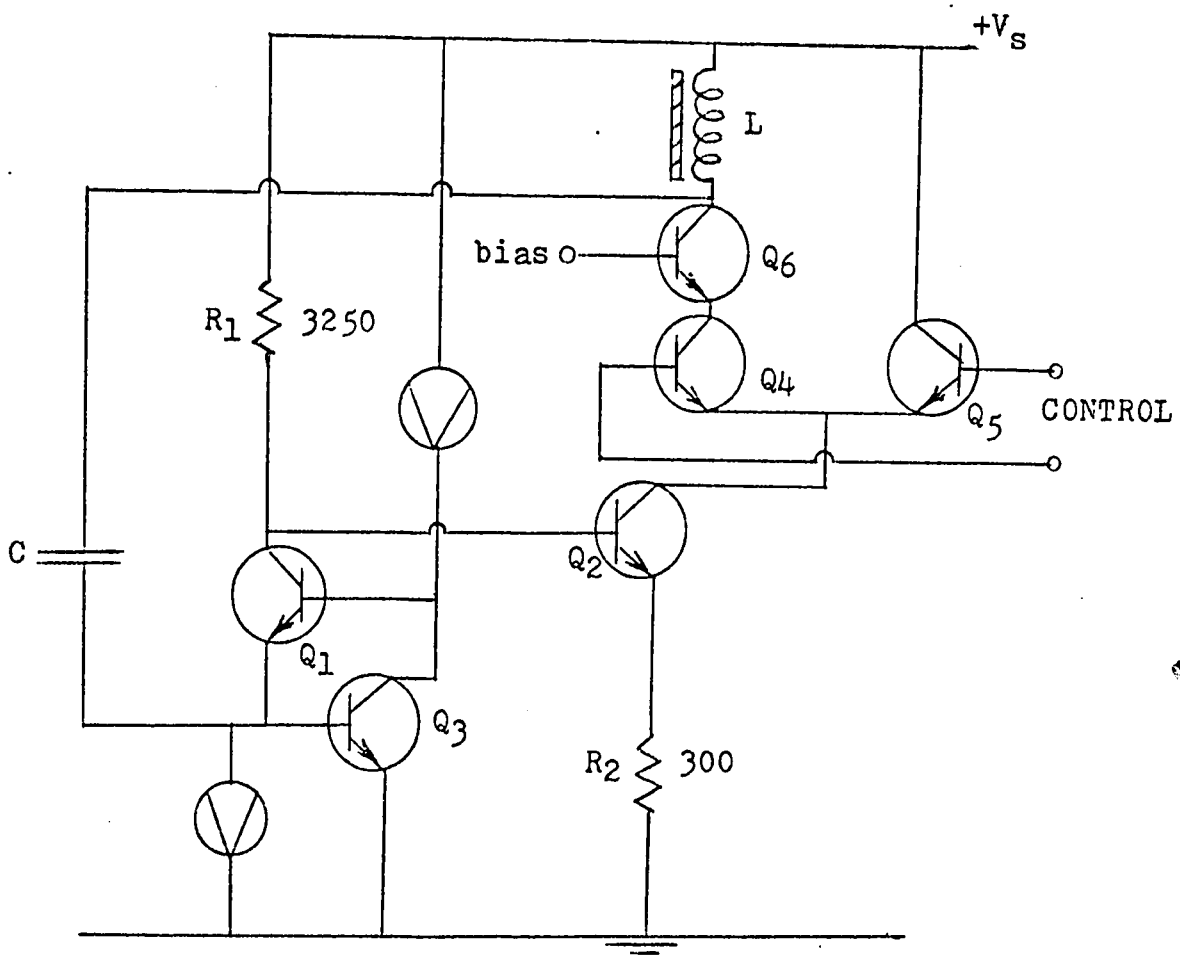


Fig. 3.26 A typical circuit for a one current amplifier positive immittance converter employed to tune an antenna

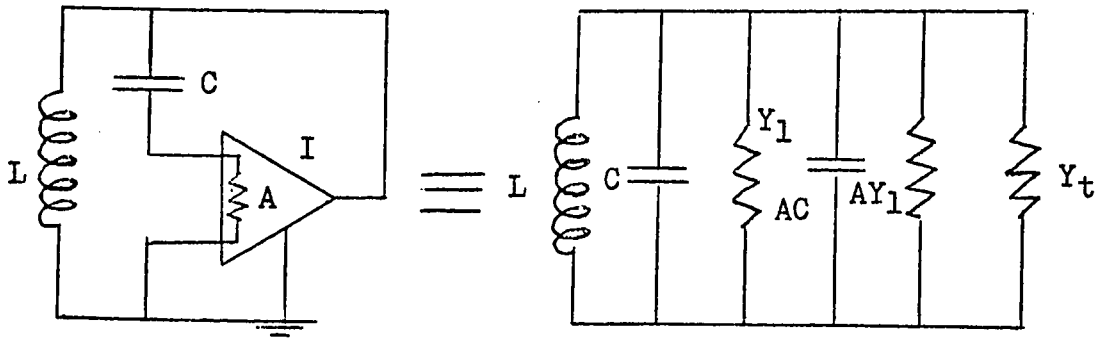


Fig. 3.27 Equivalent circuits for Fig. 3.26

The overall Q of the circuit is found by the vector diagram shown in Fig.3.28. OP is the input current vector, θ_1 is due to the amplifier input resistance and the antenna loss, OP′ is the output current vector with no delay and OP″ is the output current vector with a phase delay angle θ_t. The resultant input current vector OR is the vector sum of OP and OP″. If $\theta_2 \leqslant \frac{\pi}{36}$ rad, the overall tuned circuit $Q \simeq \frac{1}{\theta_2}$

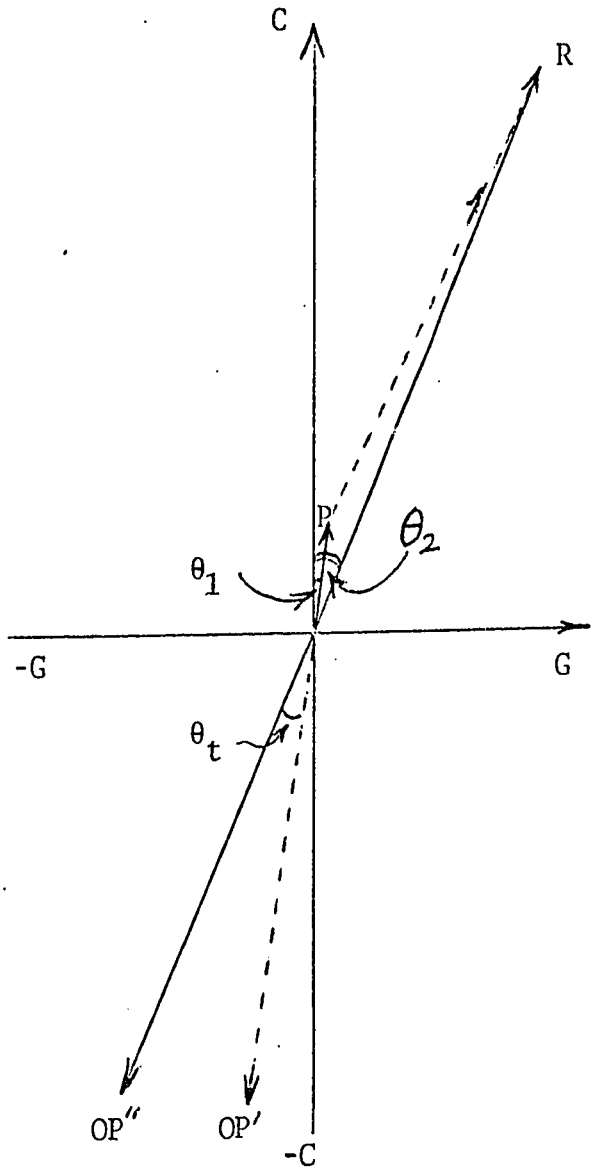


Fig. 3.28. Vector diagram to find the circuit Q of Fig. 3.26

3.3 Circuit Realization for the Gyrator

As shown in Fig. 1.47, a gyrator can be formed by two voltage and two current amplifiers. The block diagram of the transconductance gyrator to tune the antenna of inductance L_1 is shown in Fig. 3.29.

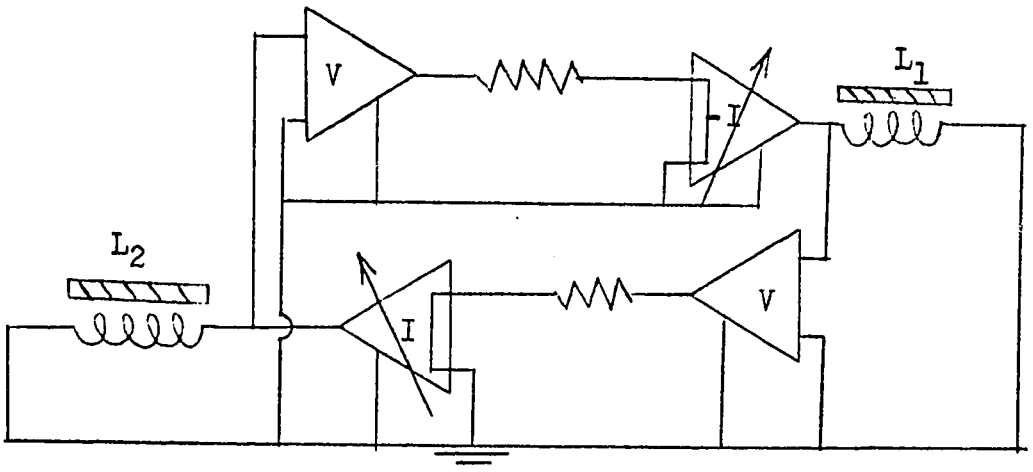


Fig. 3.29 A block diagram of the transconductance gyrator to tune the antenna of inductance L_1

It is now shown that the effect of the input conductance g_{11}, the output conductance g_{22}, and the phase delay θ on the Q-factor of the circuit shown in Fig. 3.29. For simplicity, parasitic immittances are neglected. Thus

$$Y_{12} \cdot Y_{21} = y_{12}\, y_{21}\, e^{-j\theta}$$
$$= y^2 (1 - j\theta) \quad \ldots\ldots\ldots\ldots\ldots \quad (3.19)$$

where $y = y_{12} = y_{21}$ and $e^{-j\theta} = 1 - j\theta$ for small θ.

Thus the equivalent circuit for Fig. 3.29 is as shown in Fig. 3.30 whose input admittance is

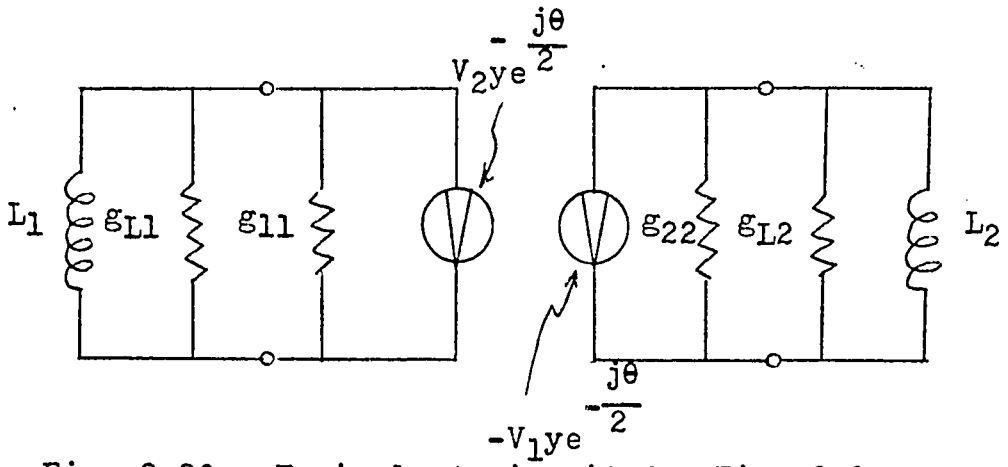


Fig. 3.30 Equivalent circuit for Fig. 3.29

$$Y_1 = Y_{11} - \frac{Y_{21}\, Y_{12}}{Y_{22} + Y_L}$$

$$= g_{11} + \frac{y^2\,(1-j\theta)}{g_{22} + g_{L2} + \frac{1}{j\omega L_2}}$$

After normalizing the denominator,

$$Y_1 = g_{11} + \frac{y^2\,\omega\, L_2\,[\omega L_2\,(g_{22}+g_{L2})]}{1 + \omega^2\, L_2^2\,(g_{22}+g_{L2})} + \frac{y^2\,\omega L_2\,\theta}{1 + \omega^2 L_2^2\,(g_{22}+g_{L2})}$$

$$+ \frac{j\omega y^2 L_2\,[1-\omega L_2\theta(g_{22}+g_{L2})]}{1 + \omega^2\, L_2^2\,(g_{22}+g_{L2})} \quad \ldots\ldots\ldots\ldots \quad (3.20)$$

The third term on the R.H.S. of eq. 3.20 is the conductance due to the phase delay θ ($\theta = \omega t_d$) and the last term is the gyrated conductance.

Eq. 3.20 can be written as

$$Y_1 = Y_{eq} + j\omega C_{eq} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.21)$$

where

$$Y_{eq} = g_{11} + \frac{y^2 \omega L_2 \left[\omega L_2(g_{22}+g_{L2})+\theta\right]}{1 + \omega^2 L_2^2 (g_{22}+g_{L2})^2}$$

and $$C_{eq} = \frac{y^2 L_2 \left[1 - \omega L_2 \theta (g_{22}+g_{L2})\right]}{1 + \omega^2 L_2^2 (g_{22}+g_{L2})^2} \quad \ldots\ldots\ldots\ldots \quad (3.22)$$

Thus Fig. 3.30 can be further reduced to Fig. 3.31, where the total conductance

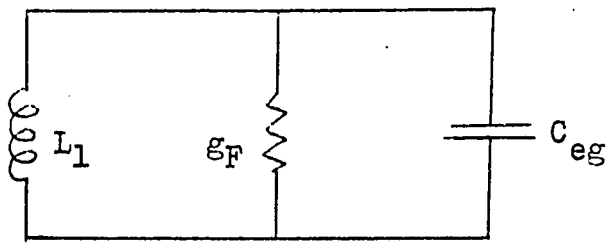


Fig. 3.31 Final equivalent circuit for Fig. 3.29

$$g_F = g_{L1} + g_{11} + \frac{y^2 \omega L_2 \left[\omega L_2(g_{22}+g_{L2})+\theta\right]}{1 + \omega^2 L_2^2 (g_{22}+g_{L2})^2} \quad \ldots\ldots \quad (3.23)$$

as g_F is positive for all ω, the circuit is stable.

The overall Q of the circuit is

$$Q = \frac{\omega C_{eq}}{g_F} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.24)$$

as the gyrated capacitance C_{eq} decreases as ω increases, due to g_{11}, g_{22} and θ (see eq. 3.21), the overall Q of the circuit

is expected to fall as ω increases. When the frequency increases to such a value that C_{eq} vanishes and thereafter becomes negative, the device no longer functions as a gyrator.

CHAPTER 4

RESULTS AND CONCLUSION

4.1 Introduction

The purpose of this chapter is to explore the range of practical results that might be expected when tuning systems using the immittance converters discussed in the previous chapter are realized as integrated circuits. The first section deals with the results that have been obtained from practical realization of the basic building blocks of the immittance converters. The second section shows how the overall performance of the tuning system using immittance converters to tune a ferrite rod antenna is governed by the performance of the building blocks. Finally, some conclusions are drawn about the most suitable form of immittance converter for tuning broadcast band receivers.

4.1.1 Circuit Parameters

The circuit parameters of several practical realization of the building blocks have been measured. The input resistance, output resistance and time delay, where applicable, of the unity gain voltage amplifier, current amplifier, cascode form current attenuator and constant current source are tabulated in Table 4.1. Note that the input resistance r_1 of

Table 4.1 Measured parameters of typical practical realization of Fig. 3.5, Fig. 3.10c, Fig. 3.11, Fig. 3.15, Fig. 3.24 and Fig. 3.26

Item	Parameters	Measured Value	Remarks
1	input resistance of the unity gain voltage amplifier (Fig. 3.5)	3MΩ	measured at 1 KHz
2	input resistance of the unity gain current amplifier (Fig. 3.11); the output resistance of the voltage amplifier (Fig. 3.5)	.25Ω	dc value, for frequency characteristic see Fig. 4.1
3	output resistance of the cascode form constant attenuator (Fig. 3.15)	≈10MΩ	measured at low frequency
4	output resistance of the cascode form constant current source (Fig. 3.10 c)	≈10MΩ	measured at low frequency
5	unloaded Q of the ferrite rod antenna	≈150	measured at 1 MHz, for frequency characteristic see Fig. 4.2
6	time delay of the unity gain voltage amplifier (Fig. 3.5)		3 nS ± 25%
7	time delay of the unity gain current amplifier (Fig. 3.11)		2 nS ± 25%
8	time delay of the current attnuator (Fig. 3.15)		2 nS ± 25%
9	time delay of the antenna tuning system using a two amplifier immittance converter (Fig. 3.1)		6 nS ± 25%
10	time delay of the antenna tuning system using one amplifier negative immittance converter (Fig. 3.24)		4 nS ± 25%
11	time delay of the antenna tuning system using one amplifier positive immittance converter (Fig. 3.26)		4 nS

the current amplifier ($I_{C1} \approx 1$ mA Fig. 3.11) is approximately 0.26 Ω from zero H_z to 40 KH_z and then rises to 4 Ω at 400 KH_z and 28 Ω at 1.6 MH_z. At low frequency from 0-40 KH_z, the measured results agree closely with the calculated value (sect. 3.1.4), but above 40 KH_z they do not.
Assuming $r_1 \propto \frac{1}{I_{C1}}$, then r_1 between 1 Ω and 40 Ω at 400 KH_z and between 7 Ω and 280 Ω at 1.6 MH_z can be obtained by varying I_C from 0.10 mA to 4 mA. The time delay of the voltage amplifier, current amplifier and current attenuator are respectively 3 nS, 2 nS & 2 nS. They are subject to variations from about 0.2 nS upwards depending on the β cut-off frequency and wiring (the integrated circuit will reduce the wiring delay drastically). Thus it is expected that the time delay for an antenna tuning system using a one amplifier immittance converter can be reduced to less than $\frac{1}{2}$ nS

4.1.2 Performance Curves for One Amplifier Immittance Converters

It has been shown that it is possible to achieve in wide range input impedance, output impedance and time delay for practical immittance converters. e.g. the input impedance may be in the order of 30 Ω if no special precautions are taken to reduce it. If special precautions are taken input impedances considerably lower than 1 Ω can be achieved. The parameters of the final circuit may thus be chosen on the basis of the design compromises and the degree of complication acceptable.

This section will study the effect of the important parameters of the immittance converter on the final circuit Q and its stability.

(I) One Amplifier Negative Immittance Converter (Fig. 3.24)

Fig. 4.3 shows the effect of time delay t_d, input resistance r_1 of the current amplifieer and the antenna loss (see Fig. 4.2) on the overall Q of the circuit. As t_d changes from $\frac{1}{2}$ nS to 1 nS and 2nS, it has a predominant effect on the circuit Q. Because a capacitance range of 10:1 is required to cover the frequency range from 0.4 MH_z to 1.6 MH_z, the feedback factor A increases from a small fraction to close unity. As shown by the vector diagram of Fig. 3.22, the circuit Q is very sensitive to time delay when A is close to unity. The circuit Q increases as time delay increases and it runs into oscillations when OR crosses the 90° axis. e.g., for t_d = 2 nS, $Q \approx 1000$ at 1.2 MH_z and the circuit tends to oscillate.

Fig. 4.4 and Fig. 4.5 indicate that for a one amplifier negative immittance converter to have the required circuit Q shown in the figures, the input resistance r_1 must have the characteristic shown, i.e. increasing from 17 Ω to 69 Ω (Fig. 4.4) and from 45 Ω to 615 Ω (Fig. 4.5) as the frequency in increased from 400 KH_z to 1.6 MH_z. The ripple of r_1 is due to the combined effect of time delay and antenna loss.

(II) One Amplifier Positive Immittance Converter (Fig. 3.26)

Fig. 4.6 shows the effect of time delay t_d, the input resistance r_1 of the current amplifier and the antenna loss (Fig. 4.2) on the overall circuit Q of the one amplifier positive immittance converter used to tune the antenna. As time delay introduces a loss factor, the maximum Q is always less than the Q of the antenna loaded by r_1, which is shown by the dotted curve in the Figure. The sag in the middle of the curve is due to the effect of time delay (see Fig. 3.28). As the feedback factor A decreases from 14.6 at 400 KH_z to zero at 1.6 MH_z (i.e. the time delay has no effect on the circuit Q at 1.6 MH_z and all curves meet at one point at 1.6 MH_z.)

4.2 Concluding Remarks

From the foregoing sections, it is noted that there are commonalities between the two new forms of immittance converter, the current amplifier negative immittance converter and the current amplifier positive immittance converter, when used to tune an antenna, as follows:

1. Both use amplifiers whose port characteristics are similar to those of a common base bipolar transistor.

2. It is possible to obtain the overall circuit Q required, with normal value of input resistance of the amplifier and in many cases no special precautions are needed to reduce it to a very low value.

3. Since the antenna signal is circulated by the amplifier system, no other amplifiers need be connected to the antenna. The signal can be taken directly from the immittance converter amplifier. This applies to all immittance converters treated in this thesis.

In addition, the current amplifier negative immittance converter has the following attraction. The inductance L provides a path for the direct current of Q_5 (see Fig. 3.24) and C blocks the dc supply voltage from reaching Q_2 emitter, in addition of being resonanting elemtnes. As a result, the integrated form of it becomes a simple and elegant circuit.

However, it has the following major disadvantage. Only a limited capacitance range can be obtained depending on the operating frequency and the circuit parameters. Because a large capacitance range needs a feedback factor A close to unity, the circuit Q becomes sensitive to the time delay (see Fig. 3.22 and Sect. 4.1.2) and other circuit parameters. Thus, as A approaches unity, Q may rise to infinity (depending on circuit parameters) and the circuit may oscillate. The useful capacitance range is limited by the circuit stability and sensitivity.

The above disadvantage of the negative immittance converter does not apply to the current amplifier positive immittance converter which has the following advantages:

1. It is a stable circuit because time delay introduces only a Q loss and it can have a larger stable capacitance

range than that of the negative immittance converter.

2. The normal input resistance of the current amplifier without impedance reducing tricks can be used.

However, it has the following problems associated with it, although they are not serious, they must be overcome to obtain satisfactory system performance:

1. The current amplifier must have a fixed stable gain of approximately 10 to provide the required capacitance range. e.g., in the circuit of Fig. 3.26, any changes in R_1, R_2 or r_e of Q_2 will change the fixed gain and thus its resonanting frequency. Any change in gain will interfere with the tracking (see sect. 2.1.4).

2. Since the amplifier gain is higher than in the previous case, the time delay through the circuit is also greater.

The thesis has shown that the current forms of immittance converter appear to meet the requirements of a tuning system for fully integrated circuit broadcast receivers. However, the detailed design of the amplifiers and the noise problems the system may introduce have not been studied and further work in this direction is required before these immittance converters can be applied to practical integrated broadcast receivers.

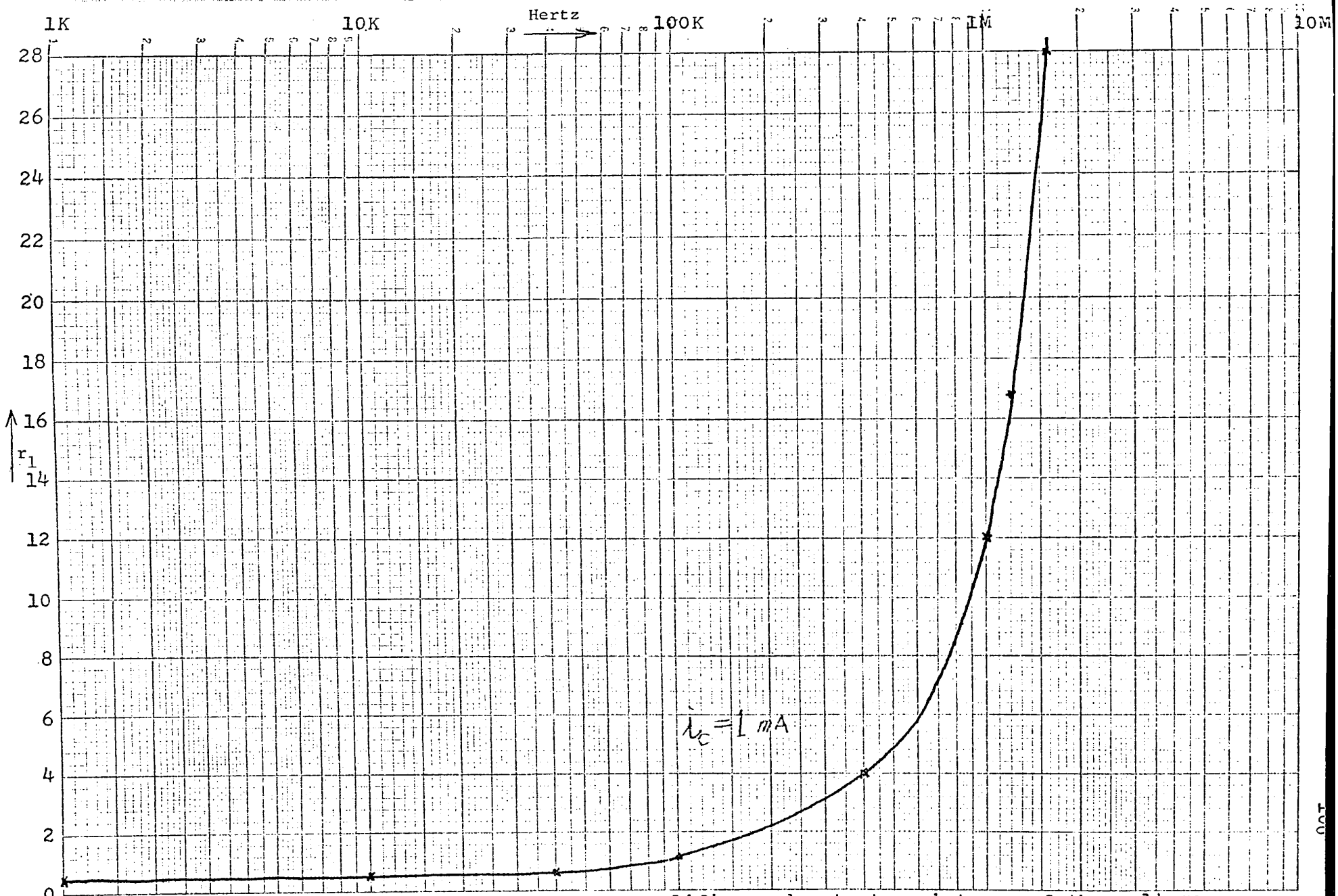


Fig. 4.1 Input resistance of the current amplifier and output resistance of the voltage amplifier against frequency

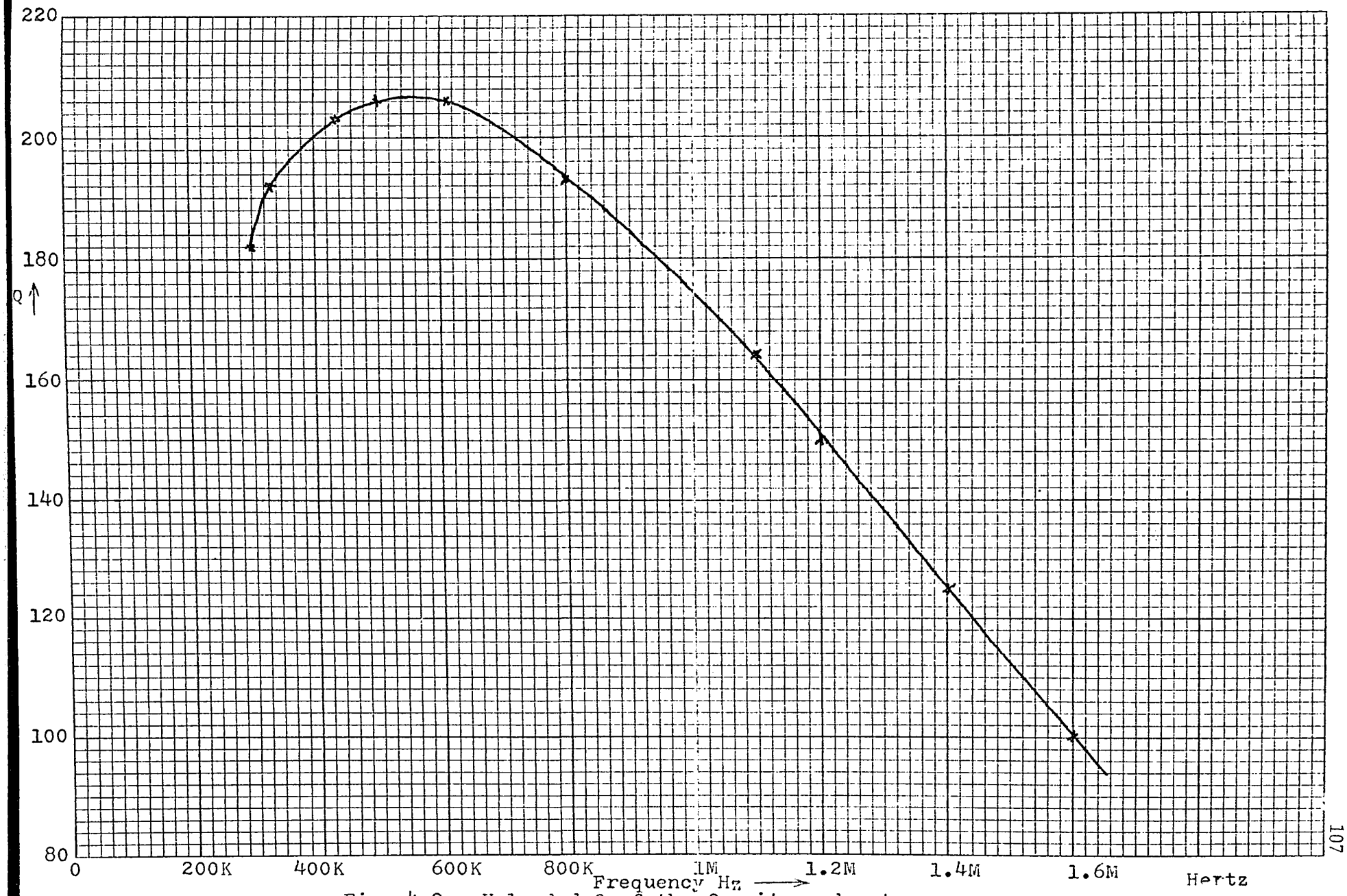


Fig. 4.2 Unloaded Q of the ferrite rod antenna

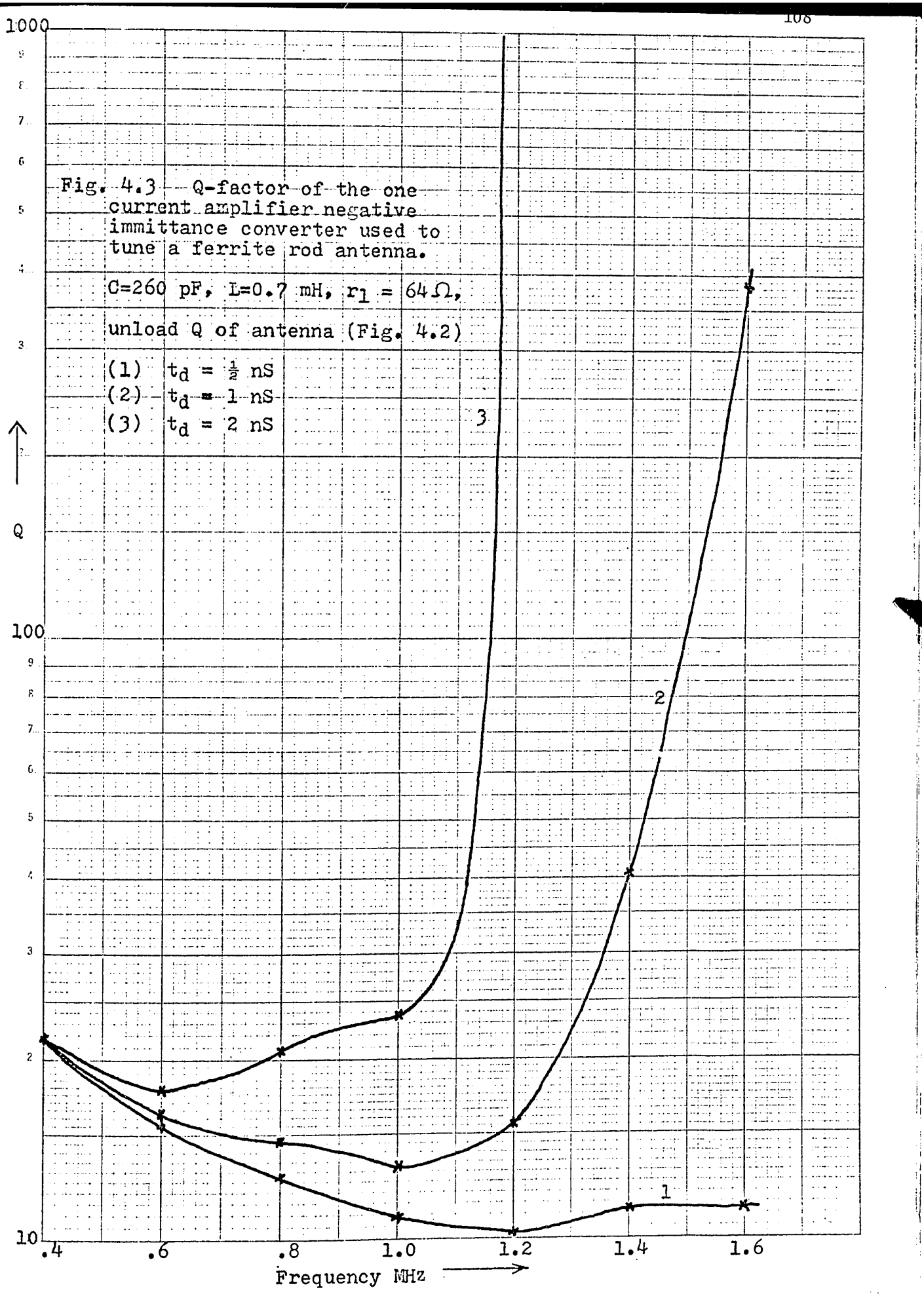


Fig. 4.3 Q-factor of the one current amplifier negative immittance converter used to tune a ferrite rod antenna.

C=260 pF, L=0.7 mH, $r_1 = 64\,\Omega$,

unload Q of antenna (Fig. 4.2)

(1) $t_d = \frac{1}{2}$ nS
(2) $t_d = 1$ nS
(3) $t_d = 2$ nS

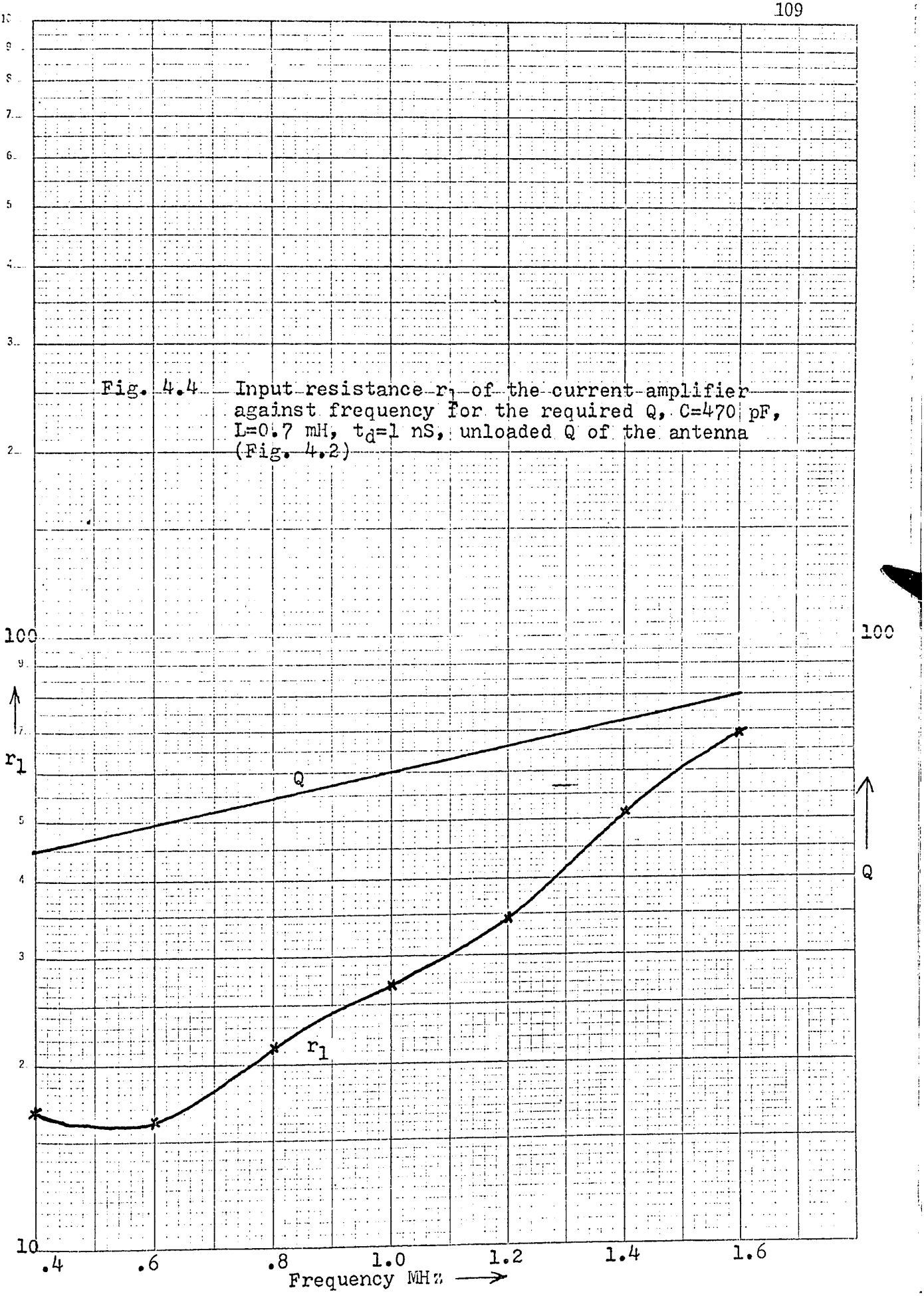


Fig. 4.4 Input resistance r_1 of the current amplifier against frequency for the required Q, C=470 pF, L=0.7 mH, t_d=1 nS, unloaded Q of the antenna (Fig. 4.2)

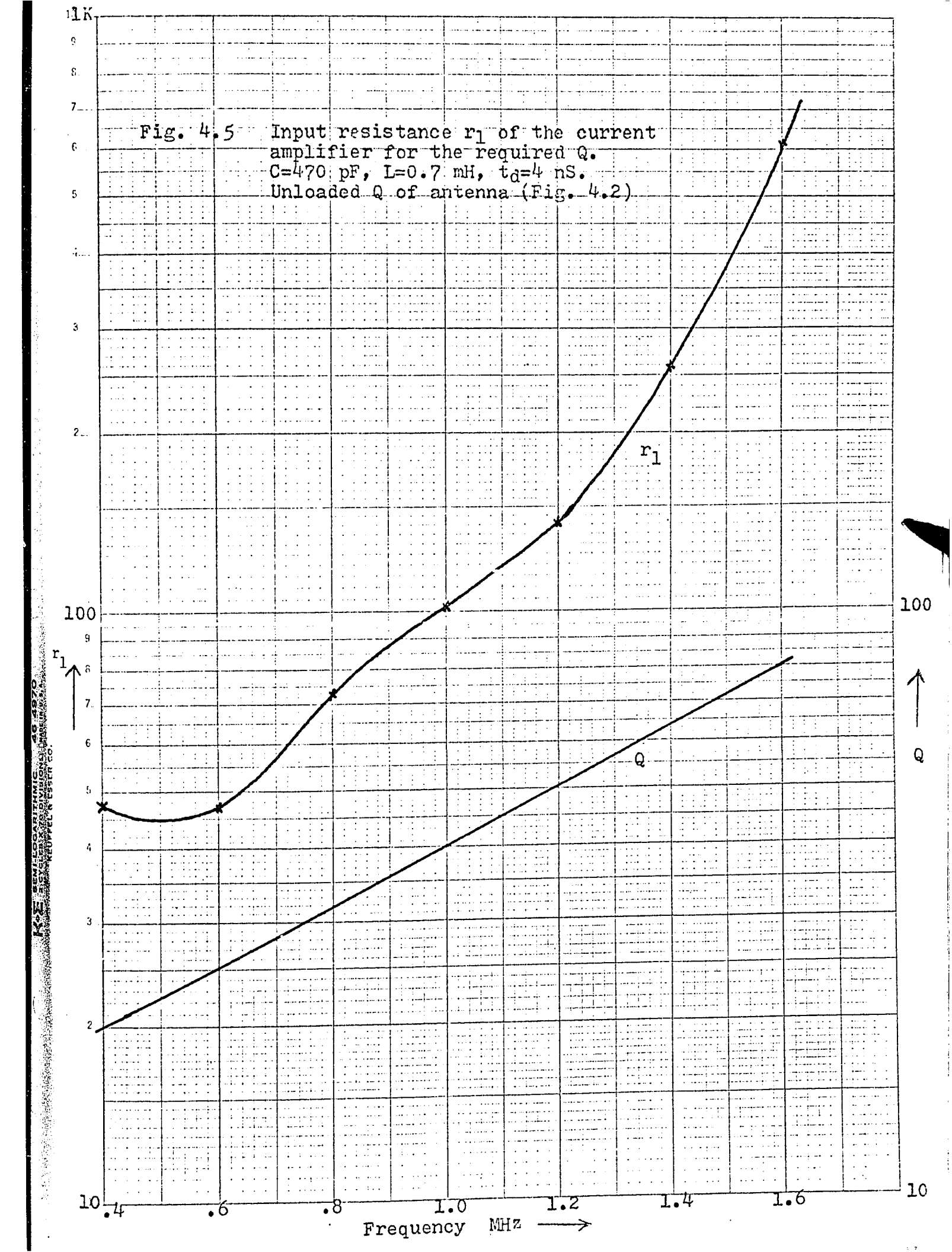


Fig. 4.5 Input resistance r_1 of the current amplifier for the required Q. C=470 pF, L=0.7 mH, t_d=4 nS. Unloaded Q of antenna (Fig. 4.2)

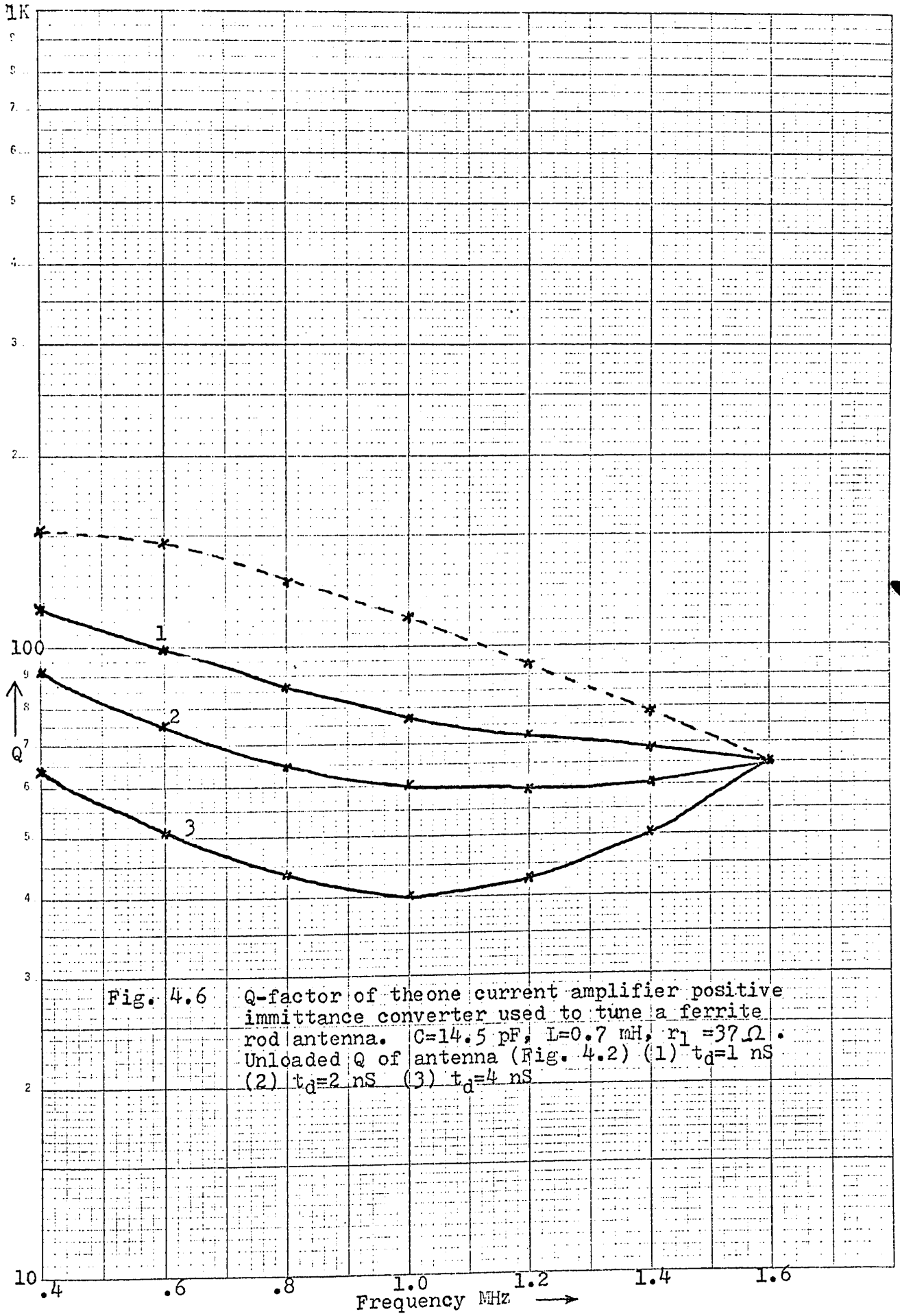


Fig. 4.6 Q-factor of theone current amplifier positive immittance converter used to tune a ferrite rod antenna. C=14.5 pF, L=0.7 mH, r_1 =37 Ω. Unloaded Q of antenna (Fig. 4.2) (1) t_d=1 nS (2) t_d=2 nS (3) t_d=4 nS

REFERENCES

0.1 Chu, L. P., "A Phase-Locked AM Radio Receiver", IEEE Journal on Radio & TV Broadcast Receivers, p. p. 300-308, Oct., 1969

0.2 Grebene, A. B., "A Monolithic Phase-Locked Filter/Demodulator", a technical report of signetics, California. (Signetic Part No. E-5021)

0.3 Grabene, A. B., "Frequency-Selective Integrated Circuits Using Phase-Lock Techniques", IEEE Journal of Solid-State Circuits, Vol. Sc-4, No. 4, pp. 216-225, August 1969

Chapter 1

1.1 Merrill, J. L., "Theory of the Negative Impedance Converters", The Bell System Journal, pp. 89-109, January 1951

1.2 Linvill, J. G., "Transistor Negative-Impedance Converters", Proceedings of IRE, pp. 725-730, June 1953

1.3 Linvill, J. G., "RC Active Filter", Proceeding IRE, Vol. 42 pp. 301-340, March 1954

1.4 Lundry, W. R., "Negative Impedance Circuits - Some Basic Relations and Limitations", IRE Trans. on Circuit Theory, pp. 132-139, September 1957

1.5 Yanagisawa, T., "RC Active Networks Using Current Inversion Type Negative Impedance Converters", IRE Trans. on Circuit Theory, pp. 140-144, September 1957

1.6 Sypress, J. M., "Synthesis of Active RC Networks", IRE Trans. on Circuit Theory, pp. 260-269, September 1961

1.7 Huelsman, L. P., "Theory and Design of Active RC Circuits", McGraw-Hill, 1968, pp. 112-154

1.8 Kuo, F. F., "Network Analysis and Synthesis", p. p. 254-270, John Wiley, 1966

1.9 Rohrer, K., "Theory of Linear Active Network", pp. 217-251, Holden-Day, 1967

1.10 Larky, A. I., "Negative-Impedance Converters", IRE Trans. on Circuit Theory, pp. 124-131, September 1957

1.11 Mason, S. J., "Feedback Theory - Some Properties of Signal-flow Graphs", Proc. IRE 41, pp. 1144-1156, September 1953

1.12 Mason, S. J., "Feedback Theroy - Further Properties of Signal-flow Graphs", Proc. IRE, 44, pp. 920-926, July, 1956

1.13 Huggins, H. W., Entwisle, D. R., "Introductory Systems and Design", pp. 49-134, Blaisdell Publishing Co. 1968

1.14 Bode, H. W., "Network Analysis and Feedback Amplifier Design", D. Van Nostrand Company, Inc., New York, N. Y. pp. 66-103, 1945

1.15 Nyquist, H. "Regeneration Theory", Bell System Tech. Bell System Techn. Journal, Vol. 11, pp. 126-147, 1932

1.16 Tellegen, B. D. H., "The Gyrator, a New Electric Network Element", Phillips Research Reports, 3, 81, 1948

1.17 Su, K. L., "Active Network Synthesis", pp. 25-52, McGraw-Hill, 1965

1.18 Haykin, S. S., "Active Network Theory", Addison-Weilay, 1970, pp. 176-190

1.19 Antoniou, A., "The Realization of RC-active Filters Using Operational Amplifier", IEEE Proceeding, pp. 1838-1850, December 1969

1.20 Daniels, R. W., "Gyrators, Negative Impedance Converters and Related Circuits", IEEE Trans. on Circuit Theory, pp. 261-262, May 1969

1.21 Holt, A. G. H., Linggard, R., "A New Multiport Antireciprocal Device and its Use in Network Design", presented at the N.T.G. Meeting, Munich, April 1967

1.22 Rao, I. N. & Newcomb, R. W., "Direct-coupled Gyrator Suitable for Integrated Circuits and Time Variations", Electronics Letters, July 1966, Vol. 2, No. 1, pp. 250-251

Chapter 2

2.1 Thompson, P. M., Yap, C. S., Peil, W., "Impedance Converters for Tuning Ferrite Rod Antenna", IEEE International Solid-State Circuits Conference, Pennsylvania, 1970

2.2 Gardner, F. M., "Phaselock Techniques", New York, Wiley 1966, pp. 35-37

2.3 Gruen, W. J., "Theory of AFC Synchronization", Proceedings of IRE, August 1953, pp. 1043-48

2.4 Costas, J. P., "Synchronous Communications", Proceedings of IRE, Dec. 1956, pp. 1713-1718

2.5 Moschytz, G. S., "Miniaturized RC Filters Using Phase-Locked Loop", The Bell System Journal, May 1965, pp. 823-870

2.6 Gilchriest, C. E., "Application of Phase-Locked Loop as a Discriminator or Tracking Filter", IRE Trans. Telemetry and Remote Control, Vol. TRC-4, pp. 20-35, June 1958

2.7 Chu, L. P., "A Phase-Locked AM Radio Receiver", IEEE Journal on Radio & TV Broadcast Receivers, pp. 300-308, Oct., 1969

Chapter 3

3.1 Zai, Y. F., "RC-active Filters Using Unity Gain Amplifier", Electronics Letters, pp. 461-462

3.2 Widlar, R. J., "Some Circuit Techniques for Linear Integrated Circuits", IEEE Transaction on Circuit Theory, Vol. CT-12, No. 4, Dec. 1965, pp. 586-594

3.3 "RCA Linear Integrated Circuit", Circuits Technical Series IC-41, pp. 135-142

3.4 Lynn, D. K., Meyer, C. S., Hamilton, D. J., "Analysis and Design of Integrated Circuits", McGraw-Hill, pp. 418-422, 1967

3.5 C. L. Searle, A. R. Boothroyd, "Elementary Circuit Properties of Transistors", pp. 193-194, John Wiley, 1966

VITA

NAME: Cho-Sing Yap

BORN: Bahau, N.S., Malaysia

August 3, 1937

EDUCATION: Primary - Chi Wen Public Primary School
Bahau, N.S., Malaysia

Secondary - The Singapore Chinese High School,
Singapore

University - Graduate of the Institution of
Electronic and Radio Engineers,
England, 1966

University of Ottawa, Ontario,
Canada

Course - Electrical Engineering
Degree - B.A.Sc., 1968

PUBLICATION :

P.M. Thompson; C.S. Yap; W. Peil, "Impedance Converters for Tuning Ferrite Rod Antenna", I.E.E.E. International Solid-State Circuits Conference, Pennsylvania, 1970.