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SCFL VLSI Circuits for Improved Yield

By

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A dissertation submitted to the
School of Graduate Studies and Research,
in partial fulfillment of the requirements
for the degree of

Master of Applied Science

Ottawa-Carleton Institute for Electrical Engineering
Department of Electrical Engineering
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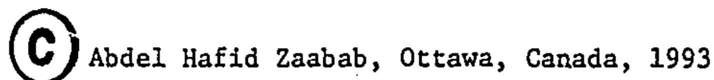

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Abstract

In this thesis an improvement to the Gallium Arsenide source coupled FET logic ECL output cell is presented. Because of parameter variations from site-to-site in the wafer, ECL compatibility of source coupled FET logic circuits, in terms of voltage levels and clock duty cycle, was very poor and therefore the electrical yield was very low. A source coupled FET logic buffer driver was designed to make the Gallium Arsenide ECL cell more resistant to parameter variations and consequently, the yield is highly improved. Furthermore, multi-site circuits are now possible with a high output electrical yield.

The circuit complexity is limited by the latency problem which occurs when using both high and low frequency signals to drive the gate. In this research, the latency time period is reduced by over 75% and hence either the operating frequency or the complexity can be increased six times.

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Je dédie cette thèse à toute ma famille en Algerie, à ma femme Laâtra et à tout le peuple Algerien qui combat pour une vie meilleur.

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Symbols and Abbreviations

GaAs	Gallium Arsenide
SCFL	Source Coupled FET Logic
DCFL	Direct Coupled FET Logic
MESFET	Metal Semiconductor FET
FET	Field Effect Transistor
ECL	Emitter Coupled Logic
CML	Current Mode Logic
VLSI	Very Large Scale Integration
LSI	Large Scale Integration
IC	Integrated Circuit
CMRR	Common Mode Rejection Ratio
NM	Noise Margin
V_{to}	Threshold voltage
V_{OH}	Output Voltage High
V_{OL}	Output Voltage Low
β	Transconductance parameter
λ	Channel length modulation parameter
α	Saturation voltage parameter
R_G	Gate ohmic resistance
R_S	Drain ohmic resistance
R_S	Source ohmic resistance

γ_{DS}	Drain voltage, induced threshold voltage lowering coefficient
U_{crit}	Critical field for mobility degradation
I_S	Gate junction saturation current
n	Gate junction ideality factor
C_{GS}	Zero bias GS junction capacitance
C_{GD}	Zero bias GD junction capacitance
C_{DS}	Drain to source parasitic capacitance
V_{BI}	Gate diode built-in voltage

Chapter 1

Introduction

From about 1980, there has been a growing effort to develop digital ICs based upon Gallium Arsenide technology. Many of the advances in high-speed digital communications and high-resolution radar systems at frequencies beyond a few gigahertz (GHz) have been possible only with Gallium Arsenide devices. And, as advances in fabrication and packaging techniques are made, the operating speed will further increase and the cost of production will reach a point where large scale application of Gallium Arsenide circuits will be economical in these and other systems where speed is of primary importance [1], [3].

1.1 Advantages of Gallium Arsenide

Basically Gallium Arsenide transistors have two distinct advantages over Silicon transistors: speed and power [2]. At the same speed, the power in a Gallium Arsenide circuit is usually lower, and for the same power dissipation, a Gallium Arsenide circuit is usually faster than Silicon. Table 1.1 summarizes the material and electronic properties of Gallium Arsenide and Silicon for comparison. Some of the properties that have let Gallium Arsenide to establish a foothold in high speed electronics can be inferred from table 1.1 as follows [2]-[8]:

- Gallium Arsenide has higher electron mobility than Silicon. Knowing that logic circuit propagation delay is directly proportional to carrier velocity, the net result

Properties	GaAs	Silicon
Bandgap	Direct; 1.42 eV	Indirect; 1.12 eV
Low-field electron drift mobility	5000 $cm^2/(V \cdot s)$ at $N_D = 10^{17}/cm^{-3}$	800 $cm^2/(V \cdot s)$ at $N_D = 10^{17}/cm^{-3}$
Low-field hole mobility	250 $cm^2/(V \cdot s)$ at $N_A = 10^{17}/cm^{-3}$	300 $cm^2/(V \cdot s)$ at $N_A = 10^{17}/cm^{-3}$
Substrate resistivity	10^6 to $10^8 \Omega \cdot cm$	Low
Native oxide	Several reactive and unstable compounds of Ga and As	SiO_2; very stable

Table 1.1: Electronic properties of GaAs and Si [7].

at the circuit level is that Gallium Arsenide logic circuits are faster than Silicon circuits for the same minimum feature size.

- Gallium Arsenide devices have greater immunity to radiation effects because of their larger band gap and the absence of critical gate oxide or isolating oxides as used in Silicon devices. This is an important consideration for space and military applications.

- Pure Gallium Arsenide is semi-insulating with very high resistivity so that no special measures need to be taken to provide isolation between devices on the chip. This further reduces parasitic capacitances and yields a better performance at high temperatures.

- The inter-electrode capacitance is much smaller in a Gallium Arsenide device because there is no pn-junction around the drain and source terminals of a Gallium Arsenide field effect transistor.

- Another important reason for interest in Gallium Arsenide and its related compounds comes from the fact that these materials have a direct bandgap. This property is very efficient in opto-electronic applications and research has led to exciting developments in LASERS, LEDs optical detectors and integrated optical circuits. These components form the basis of modern optical-communication systems; this is a function that Silicon devices could not fulfill.

- The availability of excellent heterostructure Gallium Arsenide based systems, such as AlGaAs/GaAs, GaInAs/InP, InGaAs/AlGaAs, etc., and new technologies, such as Molecular Beam Epitaxy (MBE), open up unlimited opportunities for experimentation with new devices, such as Heterostructure Field Effect Transistors (HFETs), Heterojunction Bipolar Transistors (HBTs), Hot Electron Transistors (HETs), Vertical Ballistic Transistors (VBTs), and many novel quantum devices [4].

So the fast switching capability of Gallium Arsenide devices is primarily due to their ability to deliver high currents with small changes in the input voltage and to their low internal capacitances. All of the above characteristics contribute to the realization of high-speed low-power circuits.

1.2 Disadvantages of Gallium Arsenide

Gallium Arsenide presents some disadvantages that prevent it from replacing Silicon in the commercial market due in part to the material itself (Gallium Arsenide) and also to the technology. Here we discuss some of these major problems.

1.2.1 Yield of LSI/VLSI Circuits

The most important barrier to Gallium Arsenide technology is that the yield for complex circuits is much lower than for Silicon ICs, due in part to more defects in the basic semiconductor material, because Gallium Arsenide wafers and chips are, indeed, far more fragile compared to Silicon. Therefore, for the same functional complexity the cost of Gallium Arsenide ICs is much higher than for Silicon ICs, and the feasible chip size is much lower [5].

In addition to material defects, parametric nonuniformity causes nonuniform diode and transistor characteristics which, in turn, cause logic gate characteristic variations. These variations influence the electrical yield of VLSI ICs. Because of this parametric nonuniformity, and because of the low noise margins in Gallium Arsenide FET ICs due to low voltage swings and forward gate conduction clamping, Gallium Arsenide circuits are more sensitive to parameter variations, and, being so, usually the yield is drastically low [1], [7], [9].

1.2.2 Other Limitations of Gallium Arsenide

- Complementary circuits are not attractive because the hole mobility is about the same as in Silicon.

- Greater control of the technology, ion implantation, passivation etc., is needed in order to achieve optimal production efficiency and thus obtain competitive prices in the market area.

- Because new materials and processes are involved, the reliability of Gallium Arsenide integrated circuits is still far behind Silicon integrated circuits.
- While Silicon is blessed with excellent native oxide, Gallium Arsenide has a poor and unstable one. This makes it difficult to fabricate Gallium Arsenide MOSFETs.

The major Gallium Arsenide transistor is the Metal Semiconductor FET or MESFET. However, MESFETs have their own limitations which are:

- Backgating and sidegating between devices.
- Frequency dependent small signal conductance.
- Poor absolute accuracy and pair matching.
- Drain current transients with time constants on the order of seconds.

Gallium Arsenide is not thought of as a replacement for Silicon but more as a special material which will find a role in high-frequency active devices, for use in both analog integrated circuits, with the potential large market products such as complete front end receivers for direct home reception in satellite television, and for digital integrated circuits to operate at speeds beyond the capability of Silicon systems [4], [8].

1.3 Outline of the Thesis

In Chapter 2, a yield study is reported which was based on the BNR[1] Source Coupled FET Logic (SCFL) technology. This study investigates the influences of the internal circuit structure and the characteristics of the output cell upon the electrical yield. In Chapter 3, the double-phase and single-phase SCFL circuit design techniques are compared, then the latency problem in SCFL circuits driven at high and low frequencies is discussed in addition to possible solutions. In Chapter 4, an analysis of a Gallium Arsenide-to-Silicon ECL driver is carried out. The problem of the poor yield encountered is studied and a solution is presented. Finally we conclude in the last chapter by showing the impact of our work on the electrical yield, and suggesting some future work that could be carried out.

[1] BNR: Bell-Northern Research Ltd. P.O.Box 3511, Station C, Ontario, Canada, K1Y 4H7

Chapter 2

Analysis of the High Speed SCFL

This chapter describes the basic properties of the Source Coupled FET Logic (SCFL) in terms of the dc characteristics, output gains and other features. In Section 2, we deal with the SCFL output cell and the measurements of the diode and transistor characteristics from a typical wafer at BNR. Section 3 introduces the limitations of the work done so far to deal with this subject. Finally we conclude by stating the purpose of this thesis.

2.1 Source Coupled FET Logic

Differential amplifier circuit structures have been successfully used for logic applications for years [11]. Bipolar ECL (Emitter Coupled Logic) or CML (Current Mode Logic) circuits are the most widely recognized examples. This technique has also been employed in Gallium Arsenide MESFET logic to produce a new family of Gallium Arsenide logic. The present Gallium Arsenide CML circuit consists of MESFETs, resistors, and level shift diodes. This Gallium Arsenide MESFET CML is called a Source Coupled FET Logic (SCFL). SCFL is the fastest logic circuit among Gallium Arsenide logic circuits, such as DCFL, BFL.

2.1.1 DC Characteristics

The SCFL inverter consists of a differential amplifier and two source follower buffers

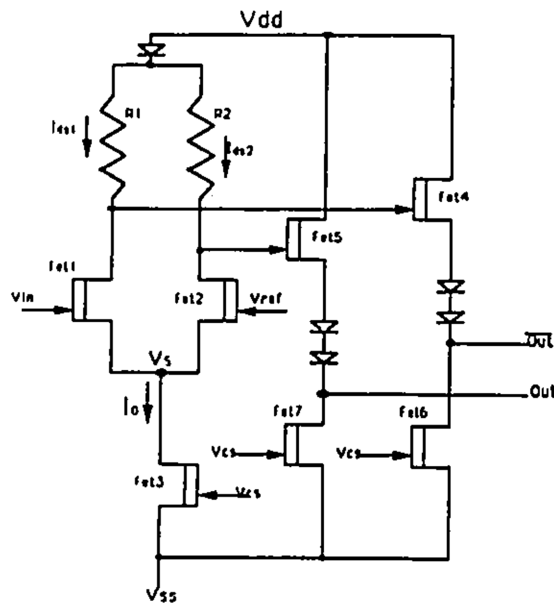


Figure 2.1: GaAs MESFET SCFL gate configuration.

with diode level shifters as shown in Fig 2.1. The input terminal is FET_1, output terminals are the drains of FET_6 and FET_7, but these are load devices, the outputs are driven by the source followers FET_4 and FET_5. When V_{in} is equal to V_{ref}, the same magnitude of the current flows through FET_1 and FET_2 to ground. At an input voltage higher than V_{ref}, the current mostly flows through FET_1. At an input voltage lower than V_{ref}, the current mostly flows through FET_2. So basically the voltage V_{in} is compared to the fixed reference voltage V_{ref} applied to FET_2 so that either FET_1 or FET_2 can turn "on" in a current mode depending on whether or not V_{in} is higher or lower than V_{ref}. Consequently at the drain of FET_1, an output that is the complement of its input is obtained. At the drain of FET_2, the same phase of the signal at the input is available [13].

Now dealing with the switching behavior of the differential amplifier which determines the dc characteristics of the SCFL [12], [13].

Assuming a basic FET equation in the saturation region as:

$$I_{DSi} = \beta_i (V_{Gi} - V_S - V_{Ti})^2, \qquad (i = 1, 2) \tag{2.1}$$

where:

i represents FET_i.

V_{Gi} is the gate voltage.

V_{Ti} is the threshold voltage.

V_S is the common source voltage.

The current I_0, which flows through the common source, is given as the sum of the currents through FET_1 and FET_2:

$$\begin{aligned} I_0 &= I_{DS1} + I_{DS2} \\ &= \beta_1 (V_{in} - V_S - V_{T1})^2 + \beta_2 (V_{ref} - V_S - V_{T2})^2 \end{aligned} \tag{2.2}$$

Elimination of V_S from equations (2.1) and (2.2) and assuming that for neighboring FETs $\beta_1 = \beta_2 = \beta$ yields:

$$I_{DS1} = \frac{I_0}{2} + \frac{\beta}{2}(V_{in} - V_{ref} + V_{T1} - V_{T2})\sqrt{\frac{2I_0}{\beta} - ((V_{in} - V_{ref}) + (V_{T1} - V_{T2}))^2} \tag{2.3}$$

and

$$I_{DS2} = \frac{I_0}{2} - \frac{\beta}{2}(V_{in} - V_{ref} + V_{T1} - V_{T2})\sqrt{\frac{2I_0}{\beta} - ((V_{in} - V_{ref}) + (V_{T1} - V_{T2}))^2} \tag{2.4}$$

From equations (2.3) and (2.4) we can deduce the following features and advantages exclusively found in SCFL [12], [14], [15]:

- Switching of the differential amplifier is influenced by the difference between the threshold voltages of the input FETs, which is negligible for adjacent FETs, and not by the absolute value of the threshold voltages. This means that unlike the DCFL gate, the SCFL gate can operate over a wide range of threshold voltages.

- Complementary outputs are obtainable from the differential amplifier as shown in Fig 2.1.

Other features of the SCFL family are:

- Output voltage swing and output voltage levels are unaffected, due to the use of a constant current source (I_0).
- Capability of driving large loads because of source-follower buffers. The source follower has high input impedance and low output impedance.
- High functionality, for example the OR/NOR gate is obtained from this configuration by just adding another FET in parallel to FET_1, and only a few gates are required to realize common logic functions such as XOR, D flip-flop. This feature yields a net savings in power and area.
- Versatility in application.

2.1.2 SCFL Differential and Common Mode Gains

There are several potential advantages of the differential circuit over the more conventional logic circuits which switch between the cutoff and ohmic regions of the FET. The major advantage is that differential circuits provide the benefit of good common mode rejection. The ideal differential amplifier should produce no output for a common mode input. This property is important for logic applications because any wafer to wafer variation in FET threshold voltage is a common mode voltage and will not strongly affect the switching of the gate [15].

Fig. 2.2 shows the basic differential circuit with differential and common mode input signals. Let V_{CM} be the common mode input signal and V_{DM} be the differential mode input signal. In this case:

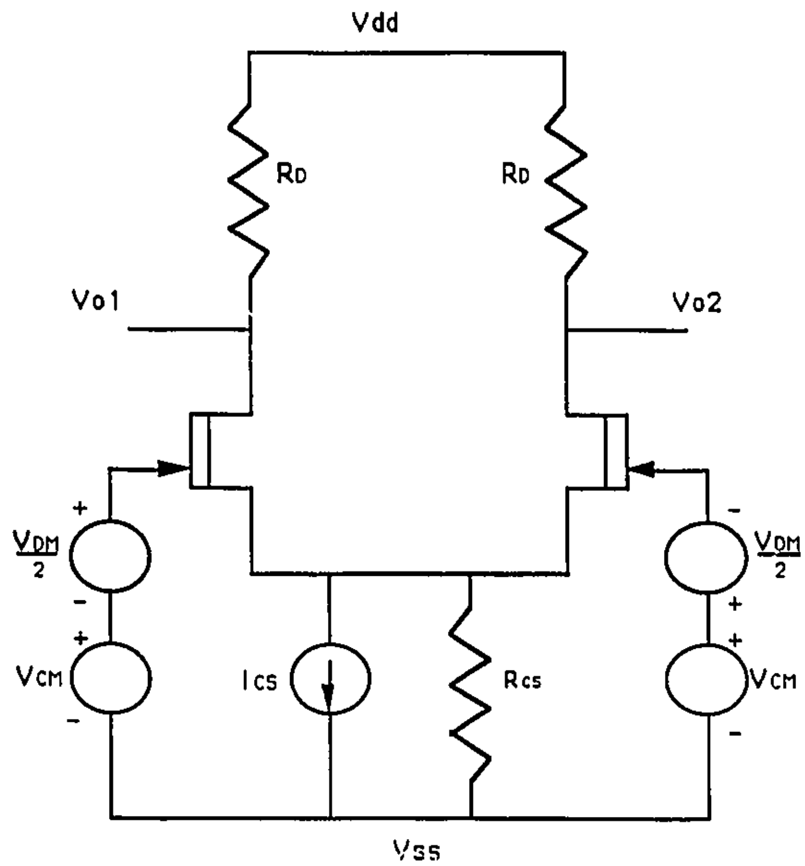


Figure 2.2: FET differential amplifier with differential and common mode input sources.

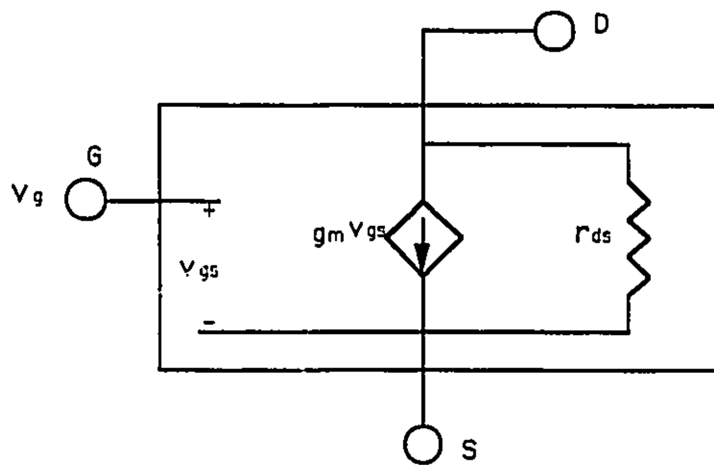


Figure 2.3: Small-signal model for MESFET

$V_1 = \frac{V_{DM}}{2} + V_{CM}$, and

$V_2 = -\frac{V_{DM}}{2} + V_{CM}$

Let A_{DM} and A_{CM} be the differential and common mode gains respectively. The FET model used to carry out this analysis is the small signal equivalent circuit model shown in Fig. 2.3.

The small signal A_{DM} and A_{CM} are given by:

$$A_{DM} = \frac{V_{o1}}{V_{DM}/2} = -g_{m1}(R_D \parallel r_{ds1}) \tag{2.5}$$

$$A_{CM} = \frac{V_{o1}}{V_{CM}} = \frac{-g_{m1}R_D}{1 + 2g_{m1}R_{cs}} \tag{2.6}$$

where g_{m1} and r_{ds1} are the transconductance and drain resistance in saturation of FET_1. From Eq. 2.6, it is seen that R_{cs}, which is the output resistance of the current source, must be made very large in order to diminish the common mode gain. The current I_{CS} is usually supplied by a current source formed by a pull-down FET, controlled at the gate by a voltage V_{CS}.

2.2 Experimental SCFL Data

The SCFL inverter gate used for our study is shown in Fig. 2.4, it is a standard SCFL gate developed at BNR and is the basis of their Gallium Arsenide ICs. Here are some of its characteristics:

- complementary inputs V_{in} and $\bar{V_{in}}$ are used because it is hard to provide a constant reference voltage V_{ref}. Another reason is that complementary outputs are already available for gates in cascade. This will insure good CMRR in all stages in a circuit.

- Only depletion mode FETs are used because it is difficult and expensive to produce both types, enhancement and depletion MESFETs, in the same wafer.

Figure 2.4: BNR SCFL inverter gate

- Many diodes are used at the output source-follower buffer. These are level shifting diodes required between stages to avoid driving the differential amplifier transistors into the ohmic region.

- Three output signals $(V_{o1}, \overline{V_{o1}})$, $(V_{o2}, \overline{V_{o2}})$, and $(V_{o3}, \overline{V_{o3}})$ are available. This level shifting is needed when the series transistor approach is used, so that inputs of the next stage can be driven from these different outputs to maintain proper biasing of their respective FETs.

- Resistors $(R_1 \& R_2)$ are used rather than FET active loads in order to simplify the biasing of the SCFL gate. When d-mode active loads are used as pull-ups, it is difficult to maintain all FETs in the saturation region, a necessary condition if the differential gain is to be adequate.

2.2.1 SCFL Output Cell

Generally a digital system is designed using only a single logic family, such as Silicon TTL, ECL, CMOS, or Gallium Arsenide logic [16]. However, sometimes this is impossible or not advantageous. Sometimes the desired components such as gates, registers, and microprocessors are not available in a single logic family. Also, and this is usually the case, it may be only the "front end" logic that requires the high speed of Gallium Arsenide SCFL; for the slower logic the less-expensive Silicon logic may be adequate. Then it becomes necessary to interconnect components from different technologies.

Another gate that has to be considered in this study is then the SCFL output cell used to solve this interconnection, or interfacing problem. This cell shown in Fig. 2.5 is basically a GaAs-to-ECL driver, specially designed to connect the Gallium Arsenide SCFL chip to a Silicon ECL chip functioning at a lower speed and different signal levels.

It is required that the output characteristics of the interface be similar to those of the receiver gate, while the input characteristics of the interface match the output

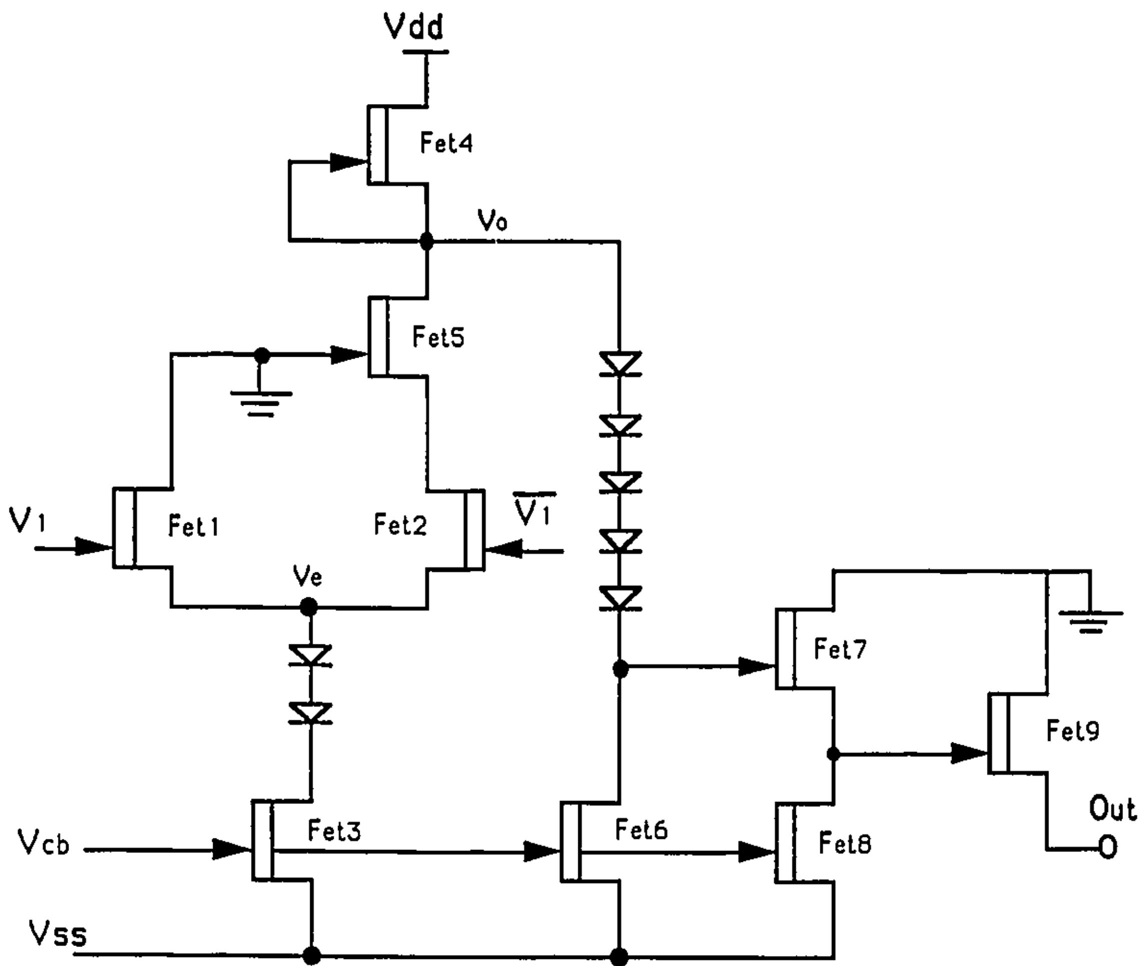


Figure 2.5: SCFL Output Cell.

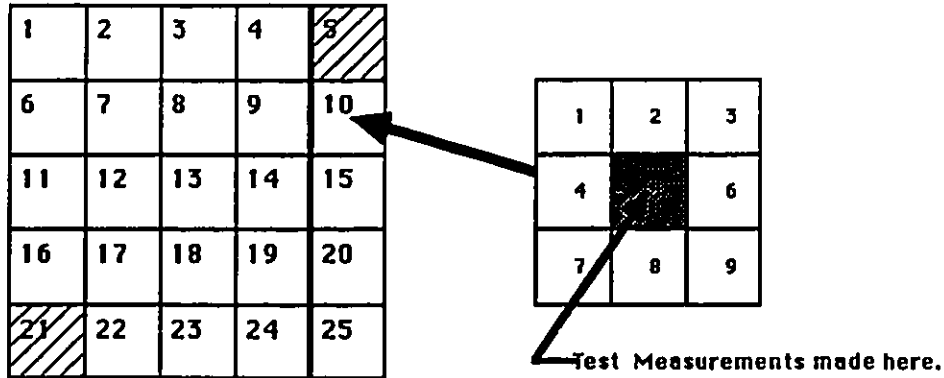


Figure 2.6: A typical GaAs wafer from BNR.

characteristics of the driving gate. The output cell will be further studied in detail in the next chapter.

2.2.2 BNR Wafer

Fig. 2.6 shows a typical wafer from BNR. The wafer is divided into 25 small squares called sites. Each site is then further divided into 9 squares and probe measurements of transistor and diode parameters are made in the middle square to characterize the given site. Sites 5 and 21 are not considered because of the difficulty in taking measurements. In all further discussions of the BNR wafer, sites 5 and 21 will not be considered. Some of the parameters obtained from test measurements are:

- V_{th}: Transistor threshold voltage.
- I_{dss}: Transistor saturated drain current.
- $R_{\square}$: Sheet resistance for implanted resistors.
- V_{to}: Diode turn-on voltage.
- R_{con}: Contact resistance for implanted resistors.

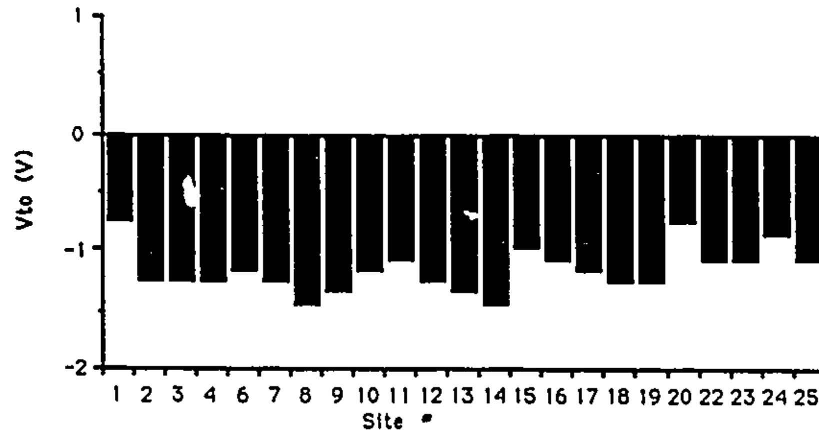


Figure 2.7: Threshold variations across the wafer.

- *Go*: Transistor output conductance.

As an example the threshold voltage V_{th} as a function of site position is drawn in Fig. 2.7. The other parameters that we extracted from this measured data using circuit model formulas are:

- β The transconductance gain parameter
- λ The channel-length modulation parameter
- α The saturation voltage parameter
- I_S The diode saturation current

2.3 Yield and Parameter Uniformity

In determining the electrical yield of LSI/VLSI circuits, Long [9] focuses on the noise margin which is the tolerance window available for the high and low logic levels. He found that unlike Silicon integrated circuits, where the noise margin is quite large because of

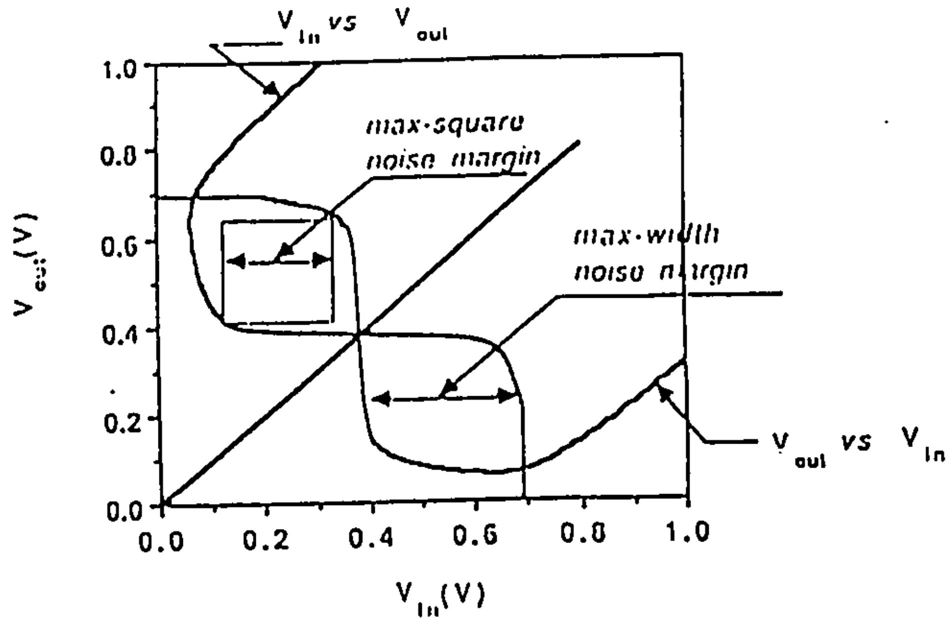


Figure 2.8: Maximum Width and Maximum Square noise margins [Long]

high power supply, Gallium Arsenide MESFET ICs have small noise margins due to small voltage swings. Therefore the electrical yield of Gallium Arsenide ICs may be constrained by parameter uniformity that determines or affects the noise margin.

The two most recognized definitions for noise margin are: The maximum width V_{MW} and the maximum square V_{MS} noise margin which represents the worst case [17], see Fig. 2.8. The method used to predict the electrical yield is as follows [9], [18]: The circuit under consideration is analyzed to determine the optimized noise margin M^*. Next, it is analyzed for the sensitivities of the noise margin to changes in device parameters which would be:

V_{to}: The FET threshold voltage.

g_{ds}: The saturation region slope parameter.

β: The transconductance parameter gain.

R_S: The ohmic source resistance.

Most circuits, however, are found to be more sensitive to the threshold parameter V_{to}. The parameters are presumed to vary independently of each other. Therefore the

standard deviation (mean square variance) of the noise margin, M_σ is given by:

$$M_\sigma^2 = \sum_{i=1}^{n} (R_i \sigma_i)^2 \tag{2.7}$$

Where R_i represents the sensitivity of the noise margin to each device parameter x_i, and σ_i is the associated variance.

Finally the available noise margin is computed as:

$$\Delta M = M^* - M_{min} \tag{2.8}$$

Where M_{min} is the minimum acceptable noise margin, arbitrarily assumed 0.1V.

The electrical yield can be related to the ratio of the available noise margin ΔM to the mean square variance M_σ by the following probability distribution function:

$$P(-X_1 < X < X_1) = \frac{1}{\sqrt{2\pi}} \int_{-X_1}^{X_1} exp(-\frac{X^2}{2}) dX \tag{2.9}$$

$$X = \frac{M}{M_\sigma} \tag{2.10}$$

$$X_1 = \frac{\Delta M}{M_\sigma} \tag{2.11}$$

The above equations give the probability of finding the noise margin of a single inverter within $\pm\Delta M$. The electrical yield of a circuit of N gates can be deduced from eq. 2.9 and is given by :

$$P(N) = P(X)^N \tag{2.12}$$

From the above expressions we see that if the value of X_1 is high, which is the case when the available noise margin is high as for Si CMOS, or when the noise margin variation is small as for Si Bipolar circuits, then the value of the integral will approach unity i.e. there will be a high yield. Fig. 2.9 describes the maximum yield that can be obtained in a circuit of N gates which have a noise margin window centered at M^* with a width of $2\Delta M$. Table 2.1 shows that the projected number of functional gates at 50 percent yield level for DCFL inverters with 0.22V noise margin at V_{TE} (enhancement threshold voltage) of 0.2V and V_{TD} (depletion threshold voltage) of -0.9V, is 10,000 gates. But

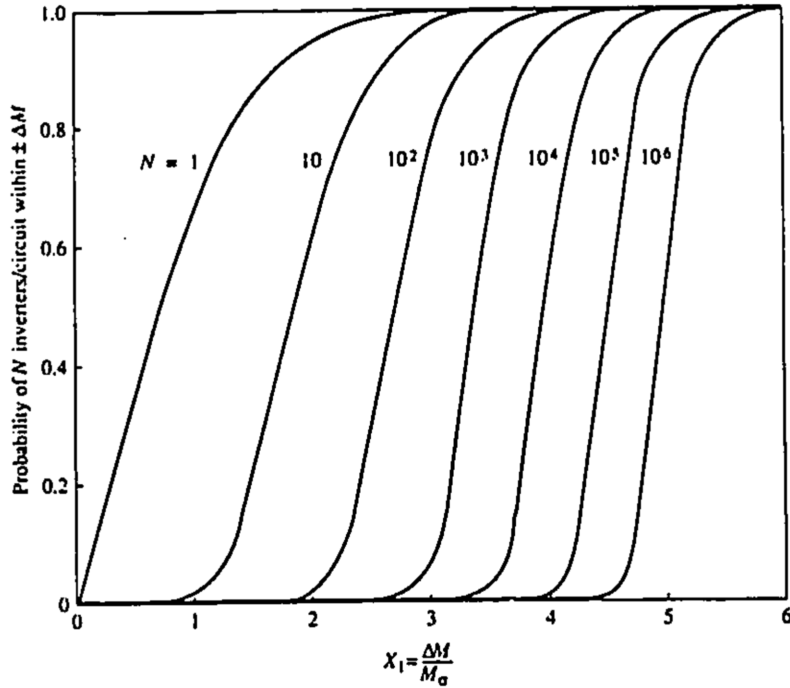


Figure 2.9: Yield of GaAs circuits with N gates [7]

$V_{TE}(V)$	$V_{TD}(V)$	NM(V)	$\sigma_{V_t}(mV)$	$\Delta M/M_\sigma$	# Gates
0.2	-0.9	0.22	53	4	10K
0.3	-0.8	0.16	53	2	10-100
0.3	-0.8	0.16	25	4	10K

Table 2.1: Projected number of functional gates at the 50 percent yield level [7]

when the mean threshold voltages are changed by only 0.1V then the projected number of functioning circuits drops to a very small value (10 to 100) in Fig. 2.9. So, in order to restore the previous yield of 50 percent, the variance on the threshold voltage must be reduced.

So in designing a circuit one should seek a topology and an architecture that maintains sufficiently large noise margins over the range of parameter variations.

2.3.1 Contributions of Other Members of the Research Group

The analysis of the SCFL data done by Djadi [19], another member of this research team, showed that the cause of the drastically low electrical yield of Gallium Arsenide ICs was the Output Cell caused by the wide spread of parameter variations over the 25 sites in a wafer. The voltage high level at the output of the cell was not within the specifications required by Silicon ECL input levels. This was observed in as many as half of the 25 sites.

Another problem revealed by this analysis was the latency problem in SCFL gates that limits the operating speed of complex circuits. This latency which is similar to the clock skew in clock buses, puts a limit to the number of gates in cascade and the complexity of the circuit, hence it affects the yield if a projected speed is set beforehand.

Both problems with Gallium Arsenide SCFL were again stated, however no solution was found to either of them.

2.4 Motivation

Gallium Arsenide SCFL circuits are so far the fastest among digital logic circuits, this high speed they offer is an important feature for telecommunications, space and military applications. Unfortunately, the yield of Gallium Arsenide SCFL circuits is found to be very low, which increases their chip cost, a fact that makes them unaffordable for many applications.

In addition to material defects, the electrical yield is found dependent on the poor parameter uniformity which affects the gate performance. This parameter uniformity affects the voltage swing, clock duty cycle and signal levels of the output SCFL cell, dropping the yield, thereafter, to less than 50% even at low speed.

A remedy to this problem could be to improve the Gallium Arsenide technology and

maintain a stringent control over all steps of Gallium Arsenide wafer processing, to insure less parameter variations. However, this solution may take time and require more research and funding, Gallium Arsenide being still a new material with some unpredictable properties and its technology is not yet brought to the level of silicon technology.

The purpose of this thesis is to find a topology or a solution for the SCFL gate and output cell that assure proper performances over the entire range of parameter variations existent in a typical wafer. As a direct consequence the yield will be raised to an adequate level. Our approach to deal with this subject and the solutions found are presented in the following chapters.

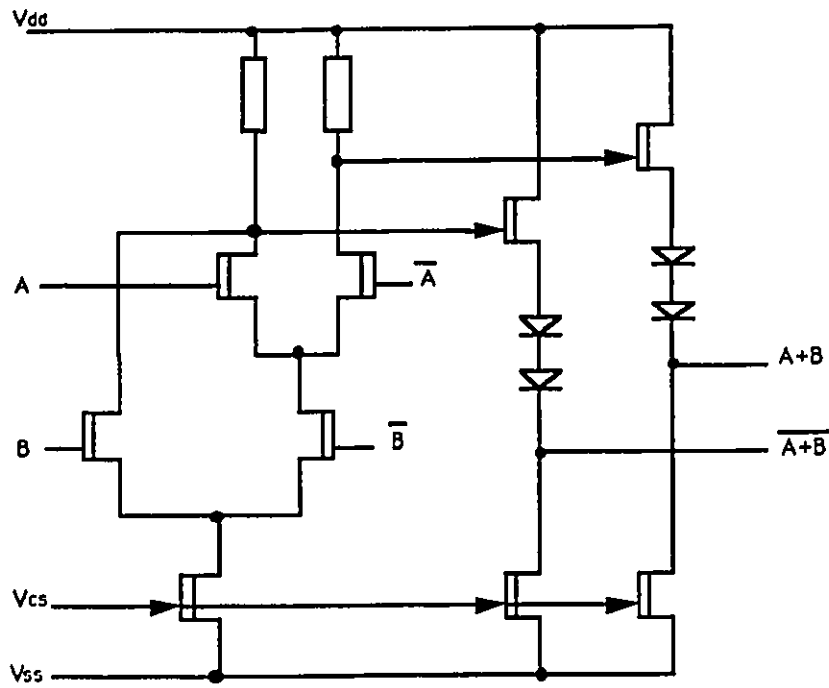
Chapter 3

SCFL Circuits at High Speed

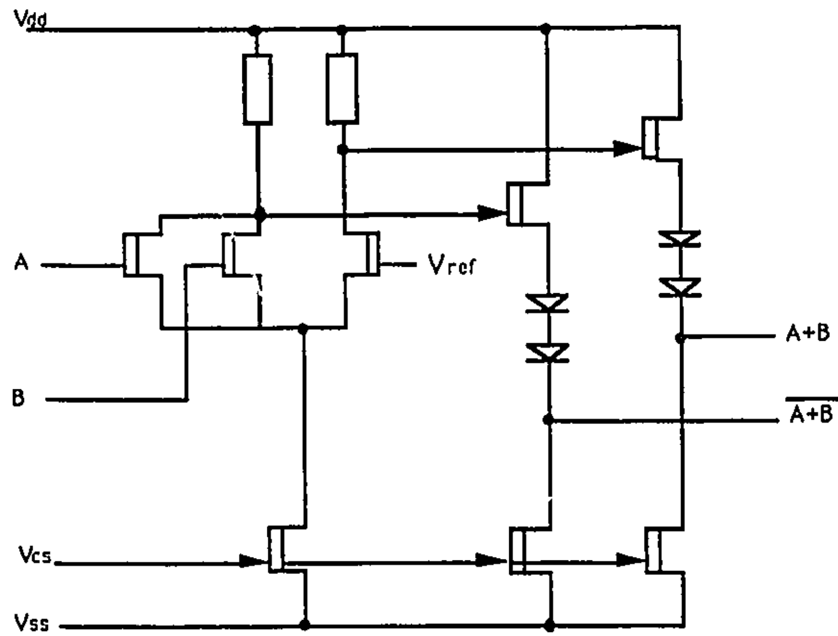
This Chapter describes complex circuits composed of Source Coupled FET Logic. First, in Section 1, we discuss the advantages of using a double-phase SCFL as a basic logic circuit, especially from the point of view of the allowance for the variation of the FET threshold voltage. A study of the electrical yield versus the threshold variations is presented. In Section 2 we deal with the problem of signal latency encountered when driving the SCFL circuits at high speeds. The problem is defined and solutions are suggested.

3.1 Double-phase and Single-phase SCFL

Among the various Gallium Arsenide logic circuits, Source Coupled FET Logic appears to be one of the most promising circuit configurations for realizing production level integrated circuits. As was previously shown is section 2.1.1, the compliance range for the FET threshold voltage of the SCFL is very large compared with other FET logic circuits because the logic switching level is not directly related to the FET threshold voltage. In particular, double-phase operation of SCFL is highly tolerant to the FET threshold voltage fluctuation within the wafer. In double-phase SCFL both the input signal V_{in} and its complement $\overline{V_{in}}$ are supplied whereas, for single-phase operation, no complement signal is supplied, but instead, a reference voltage V_{ref} is included to set up

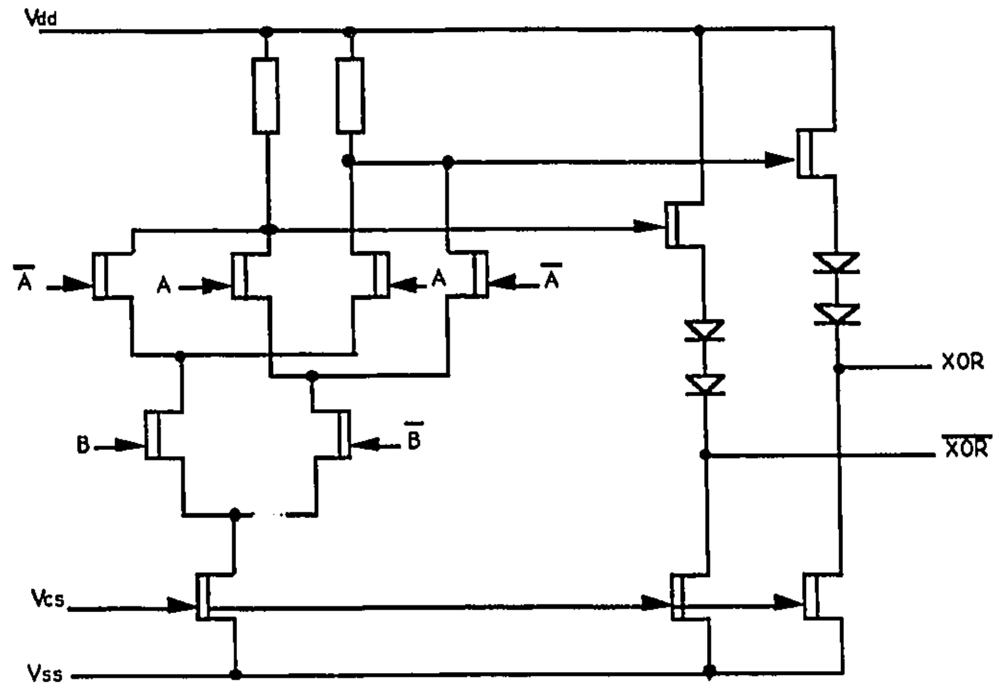


a. Series Gate



b. Parallel FET

Figure 3.1: Double/Single-phase SCFL NOR/OR gates.



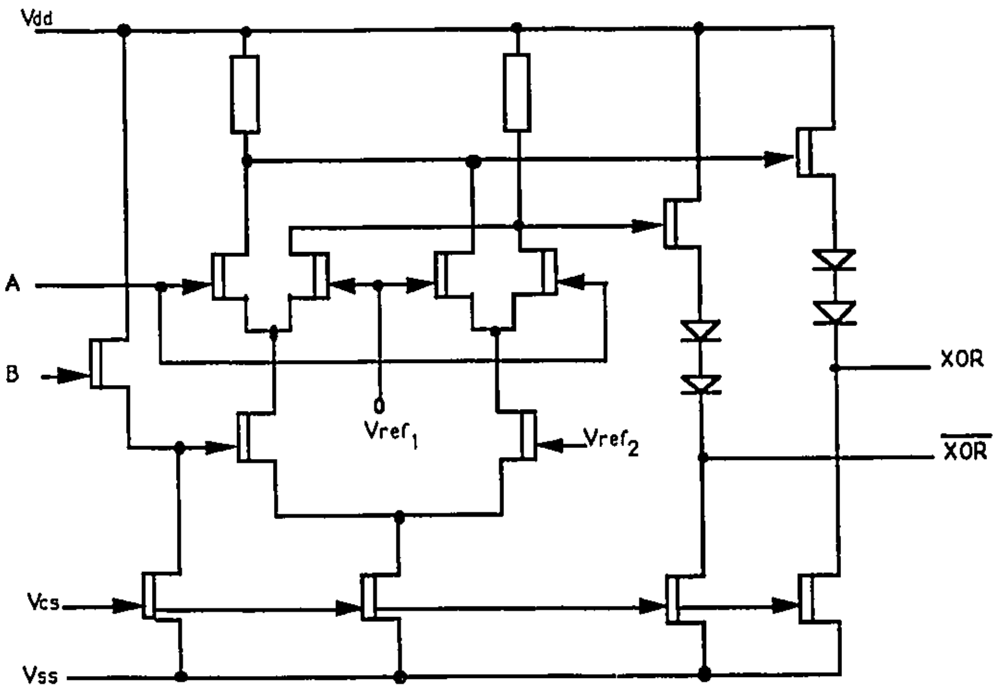


Figure 3.2: Double/Single-phase SCFL XOR/XNOR gates.

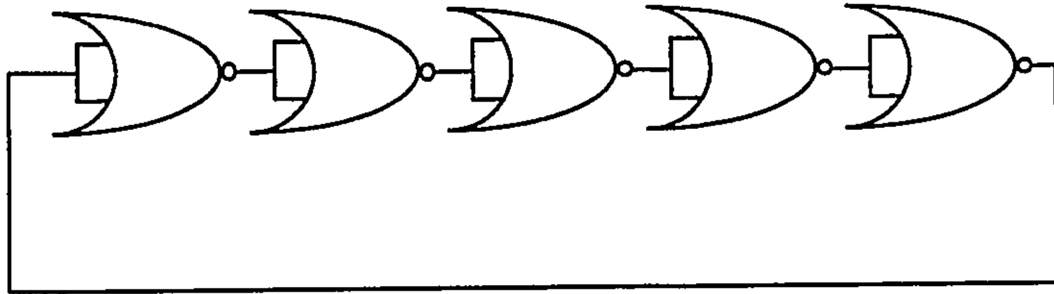


Figure 3.3: Test Circuit for Yield Calculation.

the switching level of the circuit [13]. The double-phase circuit can be easily implemented using a series gate configuration. Single-phase circuits, however, are easily realized by using parallel FETs [2]. Both types of SCFL dual input OR/NOR gates are shown in Fig. 3.1. Fig. 3.1(a) is a double-phase OR/NOR circuit using a series gating technique and Fig. 3.1(b) is a single-phase circuit with parallel FETs. Fig. 3.2 shows an XOR/XNOR circuit designed using both series gating and parallel FET techniques.

3.1.1 Yield of Double & Single-phase circuits

To compare the double-phase and single-phase techniques, a simulation was carried out to estimate the tolerance to the threshold voltage variation. The test circuit chosen was the ring oscillator shown in Fig. 3.3. A gaussian distribution is assumed to represent the scattering of the threshold voltages of each FET in the circuit. 5, 10 and 20 mV threshold voltage standard deviations are assumed respectively. As reported in [20], the results show that the propagation delay is smaller in double-phase configuration (series gate) than in single-phase configuration (parallel FETs). Furthermore, some single-phase circuits did not function at all as the standard deviation of V_T is increased, while double-phase circuits show stable operation over a wide range of V_T. In Fig. 3.4 the calculated yield of the double-phase circuits as opposed to that of single-phase circuits is drawn as

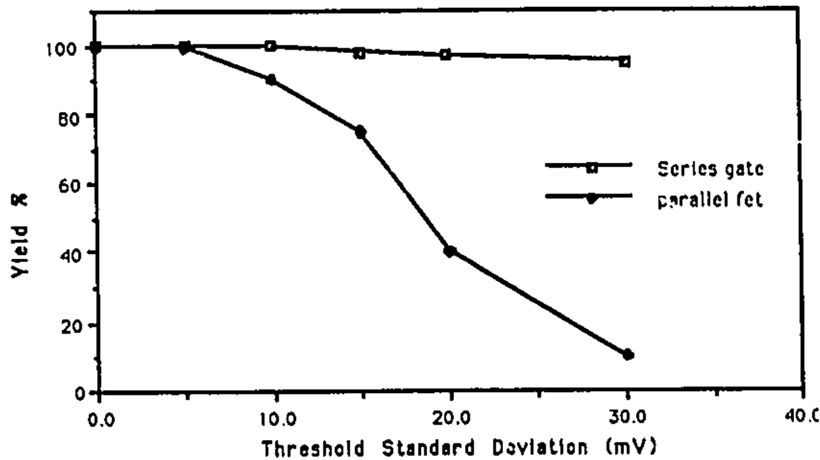


Figure 3.4: Yield of the test circuit vs. V_T standard deviation.

a function of standard deviation of V_T. We see that while even $30mV$ threshold voltage scattering is allowable in double-phase series gating circuits, the yield of single-phase parallel FET circuits reduces to 75% at $15mV$ threshold standard deviation.

3.2 SCFL at High Speed

The double-phase XOR/XNOR gate in Fig. 3.2 was simulated to determine its maximum frequency of operation. Because of parameter variations from site to site in the wafer, we expect to have a different frequency for each site. The resulting frequency plot as a function of site position within the wafer is shown in Fig. 3.5.

Now, when driving more complex circuits, this frequency is expected to drop because of the delay from gate to gate. For instance, a parity generator circuit consisting of three XOR/XNOR gates is used to test the SCFL performances.

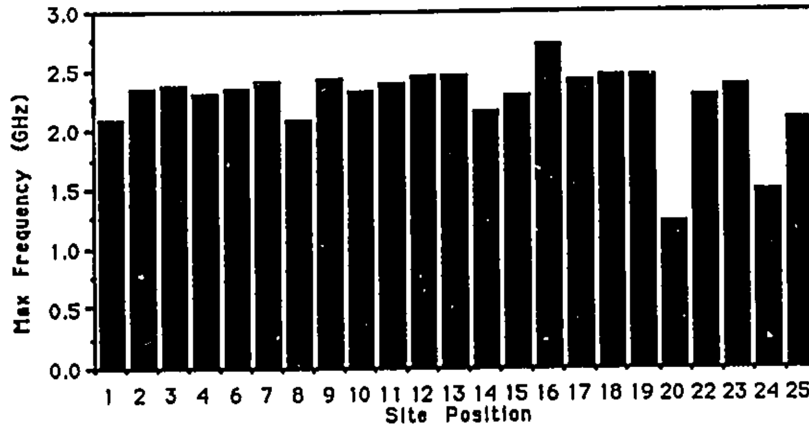


Figure 3.5: XOR/XNOR Gate Maximum Frequency of Operation.

3.2.1 Latency Problem

The parity generator circuit is shown in Fig. 3.6 along with the input frequencies at each pin. When this circuit is driven with both high and low frequency signals, we are faced with a specific problem which is the latency problem [19]. The end result is that we obtain an incorrect response at the output, in fact, for this input data a bit signal is lost because a false pulse is generated by the XOR gate.

This problem is due to the fact that the gate with low input frequency is not allowed to reach its maximum and minimum levels and the circuit changes state as soon as the high frequency signal crosses the zero axis. The circuit will toggle again when the low frequency signal crosses the zero axis later in time, as shown in Fig. 3.7. The width of this false pulse represents the latency of that gate. If the latency is greater than the delay of the gate, a false pulse is generated and, consequently, a wrong response will be obtained at the output. Fig. 3.8 shows the latency generated by an SCFL XOR/XNOR gate for all sites within the wafer.

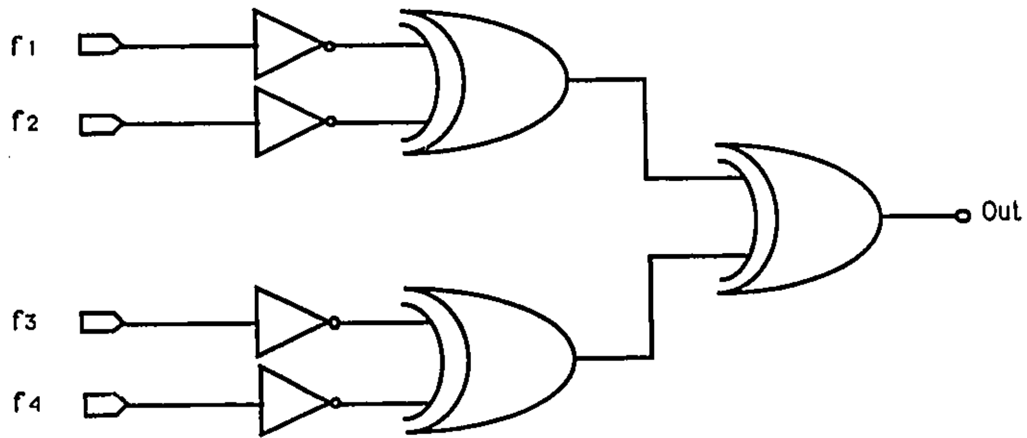


Figure 3.6: Parity Generator Circuit.

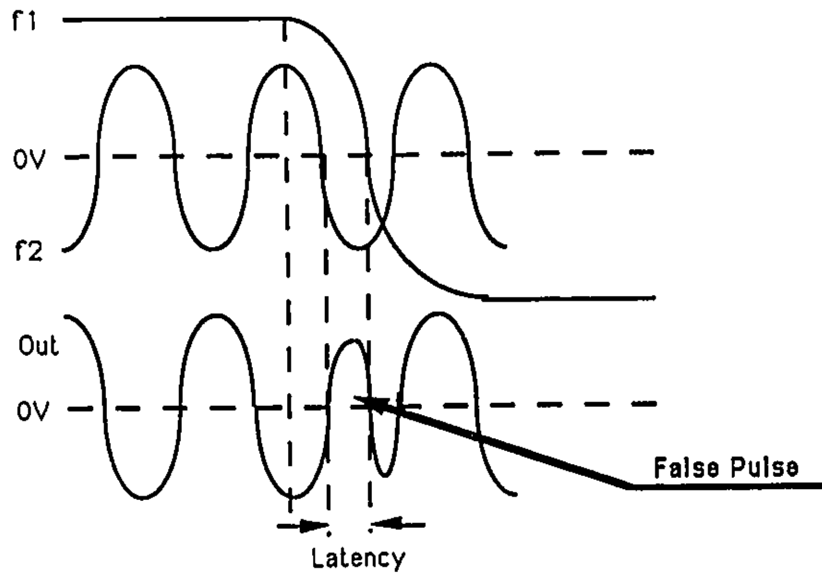


Figure 3.7: Gate Latency creation.

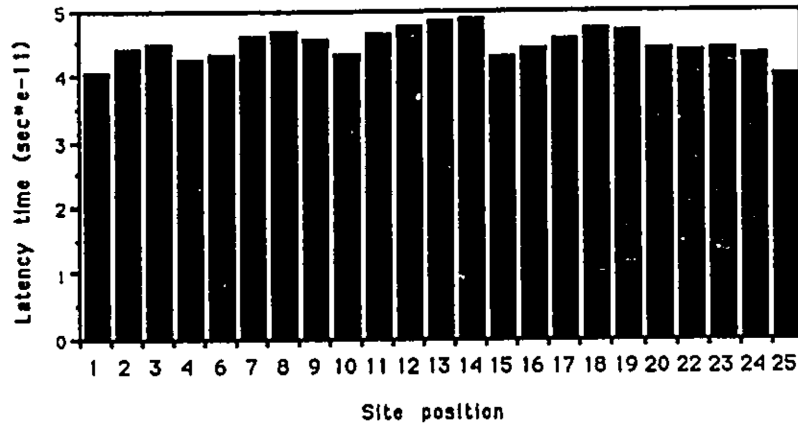


Figure 3.8: Latency of an SCFL XOR gate vs. Site position.

Effect on circuit frequency

The latency puts a limit to the maximum frequency of operation of the circuit, in that the input frequency should be reduced in order for the circuit to function properly. The new maximum frequency of the circuit is obtained from the maximum frequency of a single gate used in the construction of the circuit, according to the following formula [19] (see Appendix B):

$$f_{inMax} = \frac{f_{Max}}{1 + 2n\Delta T f_{Max}} \tag{3.1}$$

Where:

ΔT: is the latency time period

n: is the number of gates in series

f_{Max}: is the maximum frequency of a single gate

f_{inMax}: is the maximum frequency of the circuit

Fig. 3.9 gives the maximum operating frequencies of the parity generator circuit versus site position and Fig. 3.10 shows its yield versus frequency.

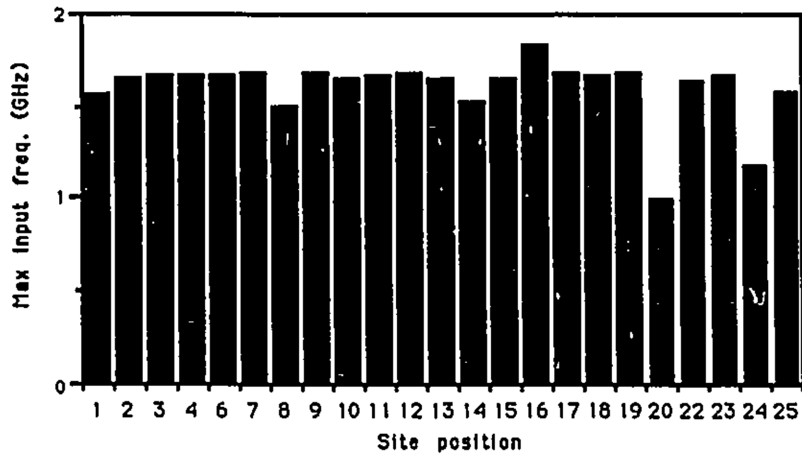


Figure 3.9: Maximum frequency of the Parity generator.

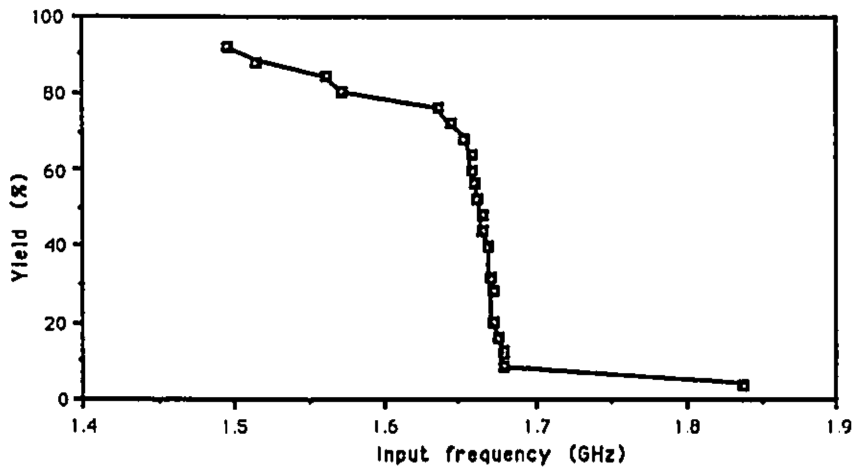
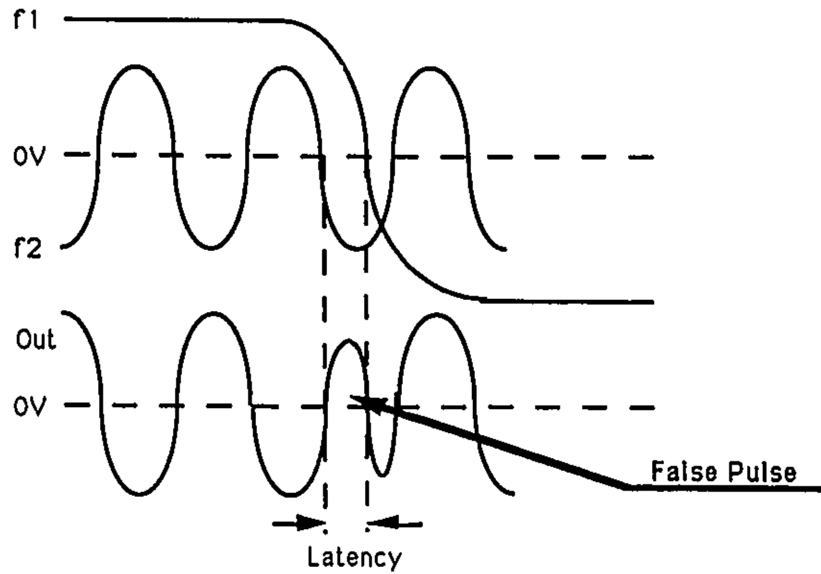


Figure 3.10: Yield of the Parity generator vs. frequency.

3.3 Solution to the Latency Problem

If we look at the series gate XOR/XNOR circuit in Fig. 3.2(a), we see that the signal A encounters three FETs in series, on its way down to the V_{ss} potential line, whereas signal B encounters only two FETs. Hence, the output signal derived from signal A will take more time to reach its minimum and maximum values than the output signal derived from signal B. It is advisable then, to forward the low frequency signal to input pin B and the high frequency signal to input pin A. By doing this we are increasing the delay of the fast signal while reducing the delay of the low frequency signal. The result is a net decrease in the delay time between the crossing points of the zero axis by both output signals, in other words, a net decrease in the latency time as shown in Fig. 3.11. Note that, even if a very short pulse is generated, it will not be, in our case, recognized by the next consecutive gate or circuit.

The signal obtained at the output of the parity generator circuit was not clean and the voltage levels were slightly low, so we increased the size of the source follower buffer FETs in Fig. 3.2(a) from $20\mu m$ to $30\mu m$ to give the circuit more driving capability. The latency is reduced to a point where it does not affect the functioning of the circuit. The new latency time period obtained in each site of the wafer is shown in Fig. 3.12 in addition to the original one. We note that a one sixth ($\frac{1}{6}$) reduction is realized, which converts to an improvement beyond 75% in latency time. This high reduction in latency induces an important improvement in frequency of operation of the circuit in all sites as shown in Fig. 3.13, where we notice up to 40% increase compared to the original case. Now the parity generator circuit frequency approaches very much that of a single XOR circuit (see Fig. 3.5). The new yield graph of the parity generator is shown in Fig. 3.14 along with the original yield curve for comparison.



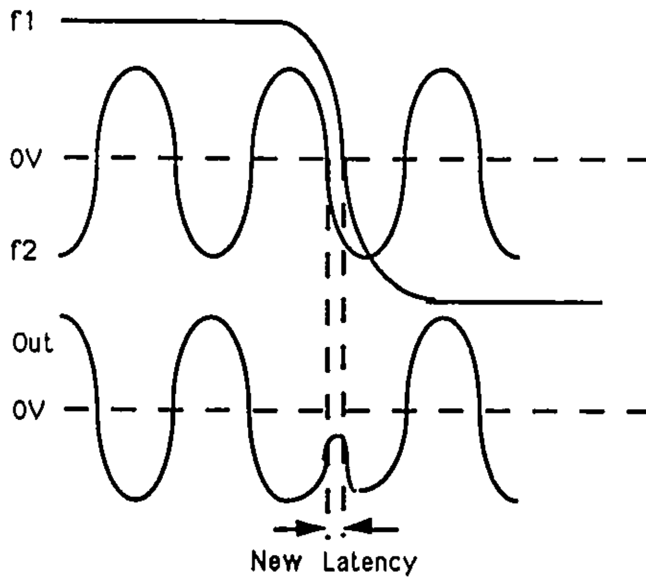


Figure 3.11: Effect of reducing Gate Latency.

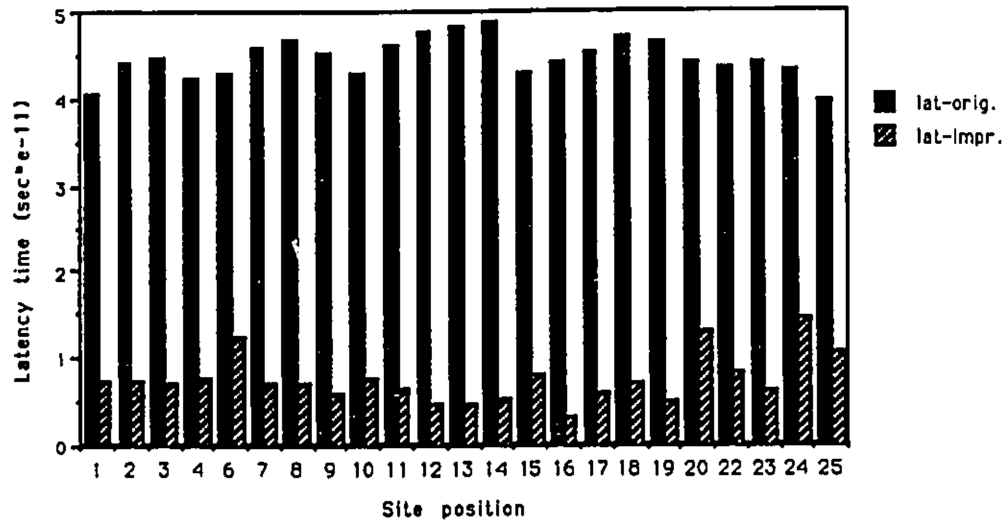


Figure 3.12: Original & Improved Latency vs. Site position.

Effect on circuit complexity

Since the latency time period is divided by six, it means that either the input frequency can be highly increased as shown above or if the frequency is kept unchanged then, according to Eq.B.6, the circuit complexity (number of gates in series) can by multiplied by up to 6 times safely, i.e. without affecting the circuit response.

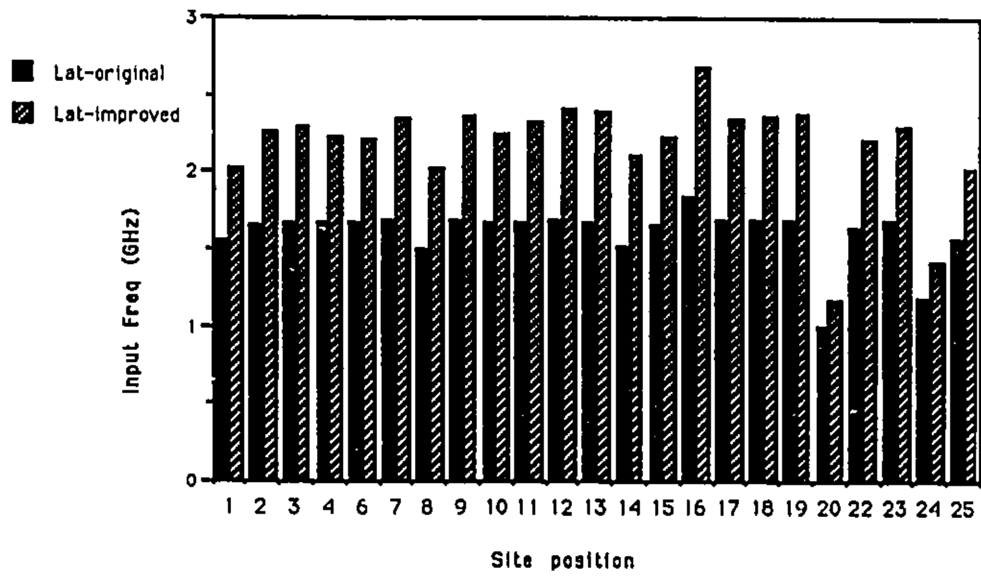


Figure 3.13: Maximum freq. of the Improved and Original Parity generator.

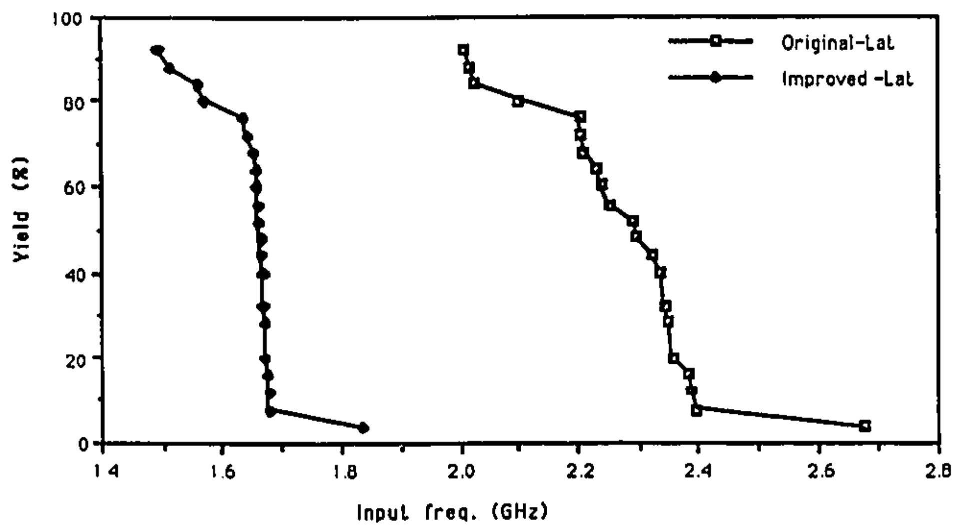


Figure 3.14: Yield of the Improved Parity generator vs. frequency.

Chapter 4

ECL-Compatible GaAs SCFL Output Cell

In this chapter an ECL-Compatible Gallium Arsenide SCFL output cell is analyzed to identify its associated problems and weakest points, and a solution is presented. In Section 1, the characteristics of the most common Silicon ECL circuits are considered. Section 2 deals with the limitations and problems encountered so far with the Gallium Arsenide output cell used at BNR. These problems that affect the electrical yield are: duty cycle below the required limit and output voltage levels out of specification. In Section 3, our approach to solving this problem is presented, a solution is offered and the results are discussed.

4.1 Silicon ECL Characteristics

Emitter Coupled Logic (ECL) using bipolar technology is a non-saturating form of Silicon digital logic permitting high speeds of operation. ECL ICs are presently the fastest among Silicon ICs and widely used in various high performance digital circuits [16]. The basis of all ECL circuits is the non-saturating current switch, also called the emitter coupled pair, shown in Fig. 4.1.

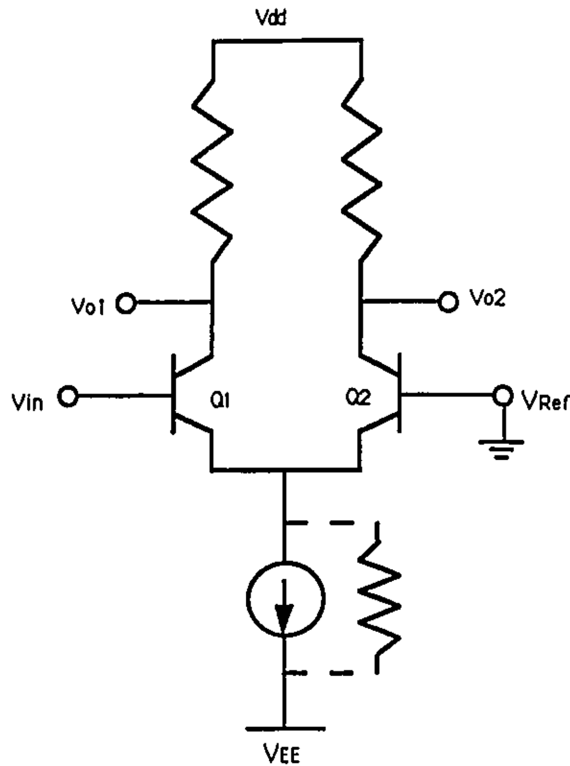


Figure 4.1: Emitter Coupled Pair Configuration.

Fig. 4.2 shows the schematic of the most popular form of ECL, produced by many manufacturers and known as the 10K Series. A listing of the typical electrical characteristics for the 10K Series 2-input OR/NOR gate is given in Table 4.1.

Another advanced and more improved form of ECL circuits is the 100K Series shown in Fig. 4.3. The circuit is similar to that of the 10K Series except that a transistor current source Q_4 is used in the emitter-coupled current switch, and back-to-back diodes D_1 and

V_{OH}/V_{OL}	-0.9 V/-1.7 V	Fan-out	10
V_{IH}/V_{IL}	-1.2 V/-1.4 V	Supply volts	-5.2
NM_H/NM_L	0.3 V/0.3 V	Power dissipation per gate	24 mW
Logic swing	0.8 V	Propagation delay time	2 ns

Table 4.1: ECL 10K Series typical electrical characteristics [14].

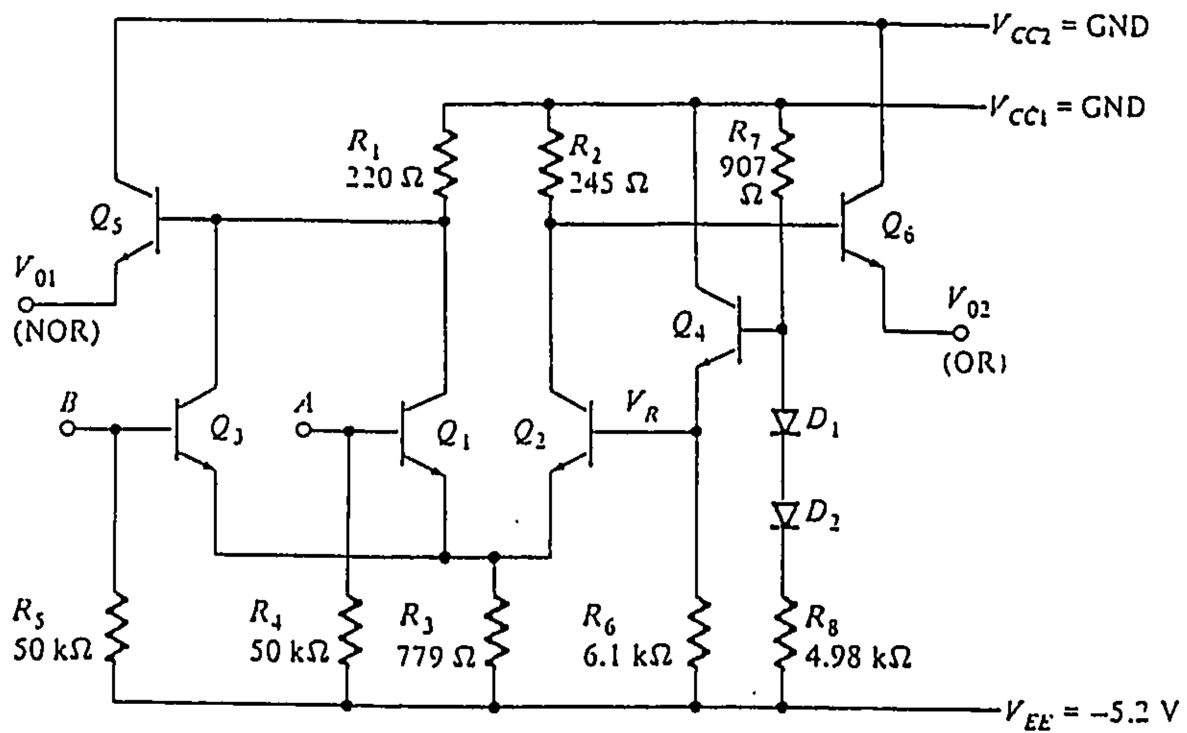


Figure 4.2: Schematic of ECL 10K 2-input OR/NOR gate [14].

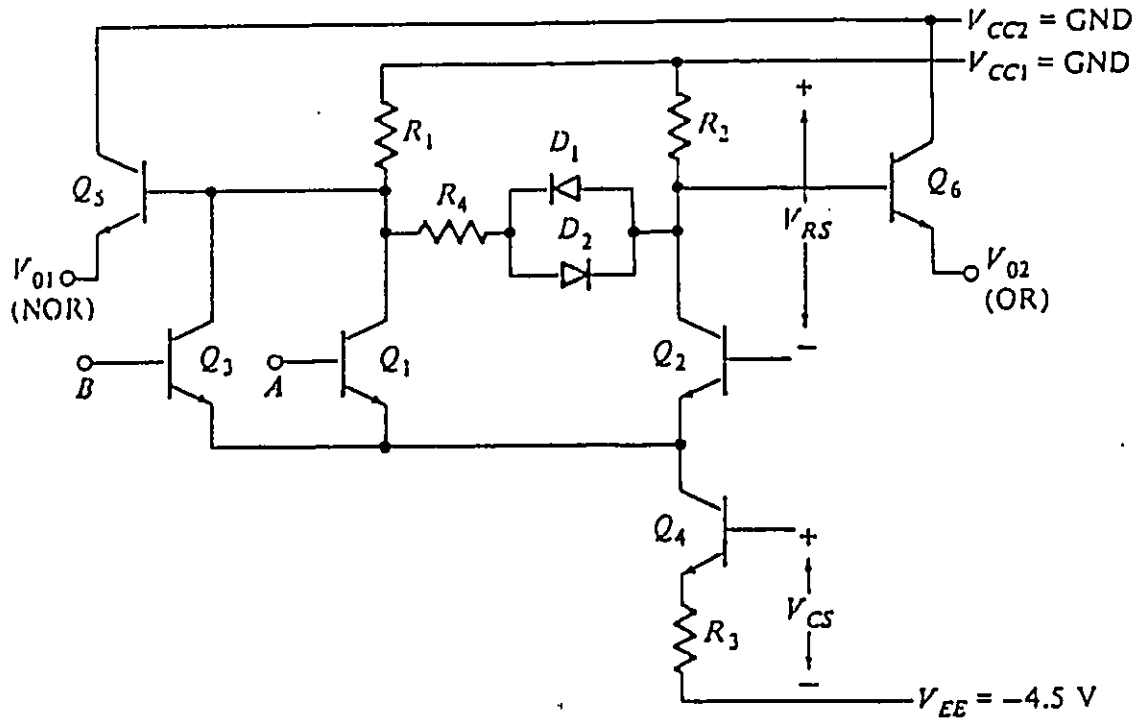


Figure 4.3: Schematic of ECL 100K 2-input OR/NOR gate [14].

D_2 with resistor R_4 are connected between the complementary outputs of the emitter pair. Another important modification added is the V_{EE} supply which has been changed to -4.5V in order to reduce the power dissipation of the circuit. The 100K Series OR/NOR gate offer a typical propagation delay time of 0.75 ns, with an increase in power dissipation to 40 mW.

4.2 Requirements and Constraints of the SCFL Output Cell

Although the high-speed capability of Gallium Arsenide enhancement/depletion (E/D)-MESFET technology is well established [20], [21], [23] most circuits reported to date have been limited by low output voltage swings when driving a 50Ω load. Because

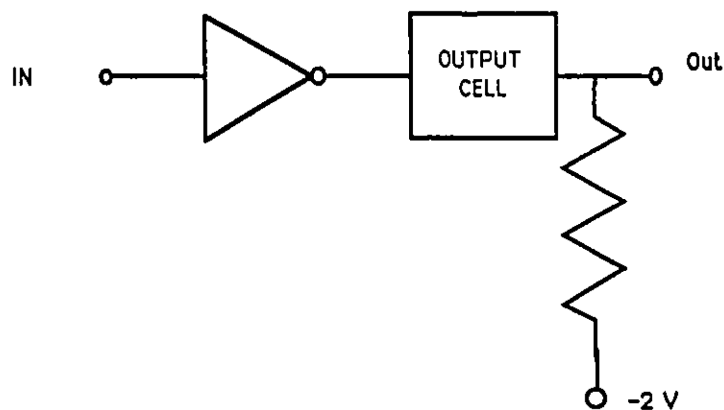


Figure 4.4: Test circuit for output voltage level measurements

most system applications of Gallium Arsenide integrated circuits will require interfacing with Silicon circuits, ECL compatibility is an extremely important feature.

Several SCFL circuit design methods have been proposed [13], [20], [23] but most of them mainly focused on how to improve the SCFL operational frequency without considering compatibility to ECL circuits. A study of compatibility with ECL in terms of power supply voltage was reported [22], [24]. In this thesis we discuss ECL compatibility in terms of output voltage levels, voltage swing, and output clock duty cycle.

4.2.1 Output voltage levels and voltage swing

In order for the SCFL output cell to be compatible with ECL circuits, it has to have output voltage levels within the range of permissible levels required to drive ECL gates. This range is known to be:

$$\begin{cases} -2 \leq V_{OL} \leq -1.62 & ; V_{OL}: \text{ Low logic voltage level.} \\ -0.98 \leq V_{OH} \leq -0.5 & ; V_{OH}: \text{ High logic voltage level.} \end{cases}$$

The actual logic voltage levels V_{OL} and V_{OH} obtained from the output cell driven by an SCFL inverter as shown in Fig. 4.4, are given in Table 4.2. Figures 4.5 and 4.6 show the spread of these two parameters as a function of site position in a wafer.

A simple way to estimate the electrical yield of the SCFL circuits with the output cell

Site Position	High Voltage VH(V)	Low Voltage VL(V)	Voltage Swing VH(V)-VL(V)	Duty Cycle %
1	-1.658	-1.937	0.279	< 10
2	-0.963	-1.922	0.959	43
3	-0.959	-1.921	0.962	43.4
4	-0.967	-1.922	0.955	42.3
6	-1.013	-1.929	0.916	39.5
7	-0.958	-1.912	0.954	43.9
8	-0.948	-1.861	0.913	45
9	-0.937	-1.893	0.956	45
10	-1.001	-1.908	0.907	38.5
11	-1.006	-1.908	0.902	42
12	-0.958	-1.905	0.947	43.6
13	-0.942	-1.891	0.949	46.3
14	-0.938	-1.858	0.92	46
15	-1.034	-1.968	0.934	41.9
16	-0.974	-1.906	0.932	40.7
17	-0.993	-1.931	0.938	41.3
18	-0.968	-1.906	0.938	44
19	-0.961	-1.906	0.945	43.2
20	-1.837	-1.887	0.05	< 10
22	-1.007	-1.896	0.889	41.3
23	-1.001	-1.914	0.913	42
24	-1.748	-1.881	0.133	< 10
25	-1.493	-1.787	0.294	< 10

Table 4.2: Measurements obtained from old Output Cell.

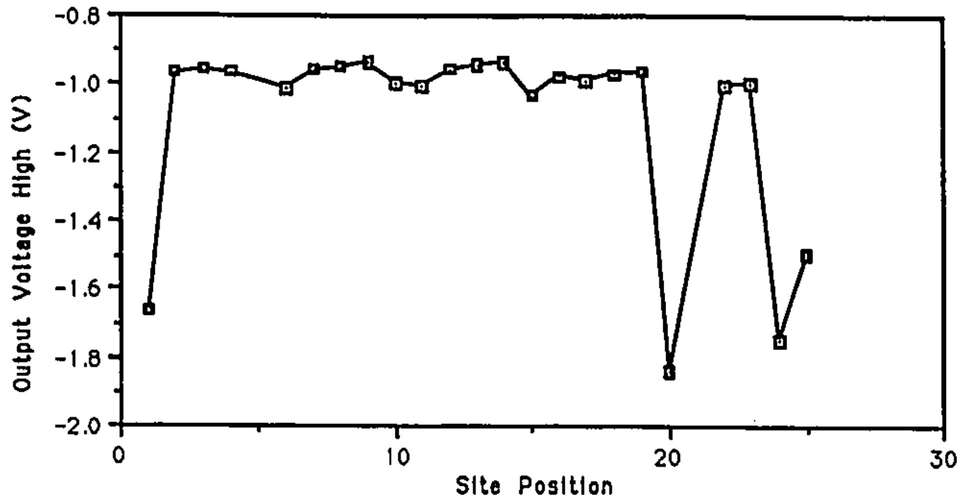


Figure 4.5: Output High logic level vs. Site position

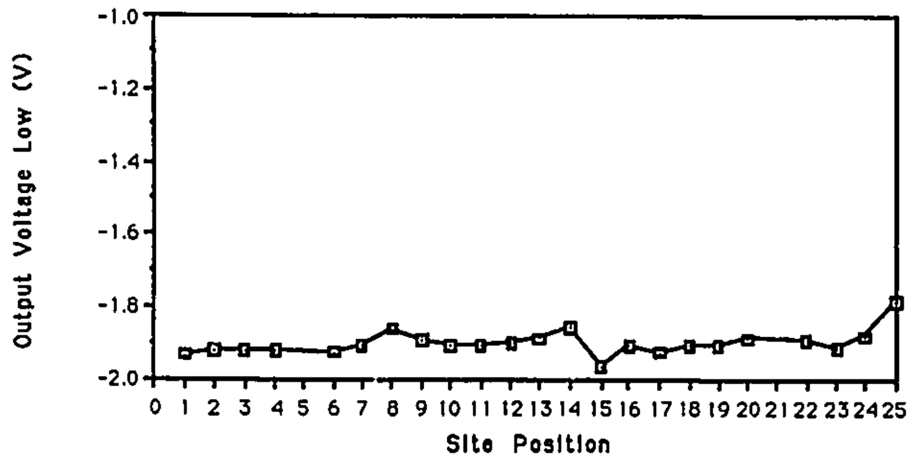


Figure 4.6: Output Low logic level vs. Site position

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25

Figure 4.7: ECL-Nonfunctional sites in the wafer

would be to consider a circuit accepted if the output voltage levels lie within the interval of ECL levels. From Table 4.2 we see that the low voltage level is ECL compatible in all sites of the wafer The high voltage level V_{OH}, however, is within the ECL interval in only 12 sites. This means that only circuits in those 12 sites will be ECL compatible in terms of output voltage levels. This problem decreases the electrical yield of Gallium Arsenide SCFL circuits to as low as 48%. Note that most of the bad sites lie in the corners of the wafer as shown in Fig. 4.7. The electrical yield of SCFL inverters versus frequency considering the ECL output cell levels can then be determined based on the site frequency histogram in Fig. 4.8, and is shown in Fig. 4.9. So the maximum yield that could be achieved with this ECL output cell is only 48% at the lowest frequency of operation.

The voltage swing is quite good, above 0.88 volts, except for sites 1, 20, 24, and 25 which are already discarded because of the high output voltage V_{OH} did not conform to specifications.

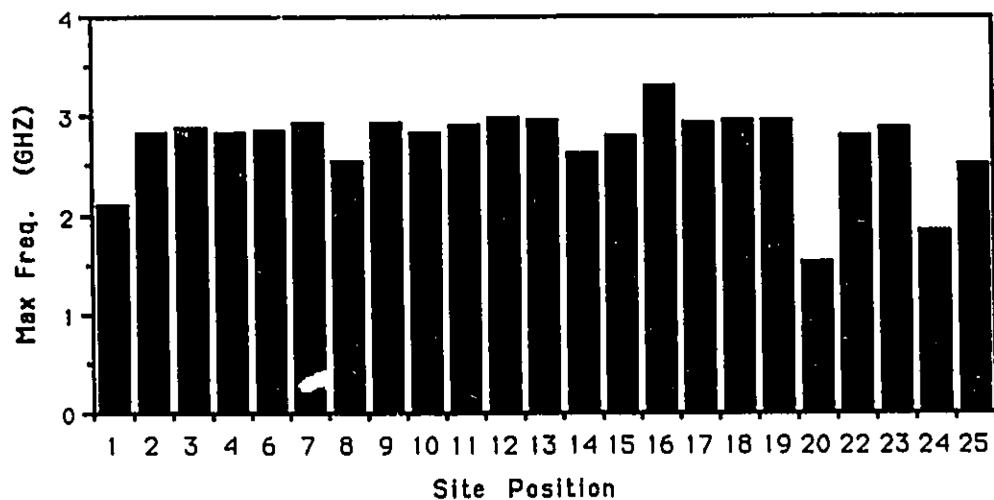


Figure 4.8: Maximum Frequency of Operation vs. Site position.

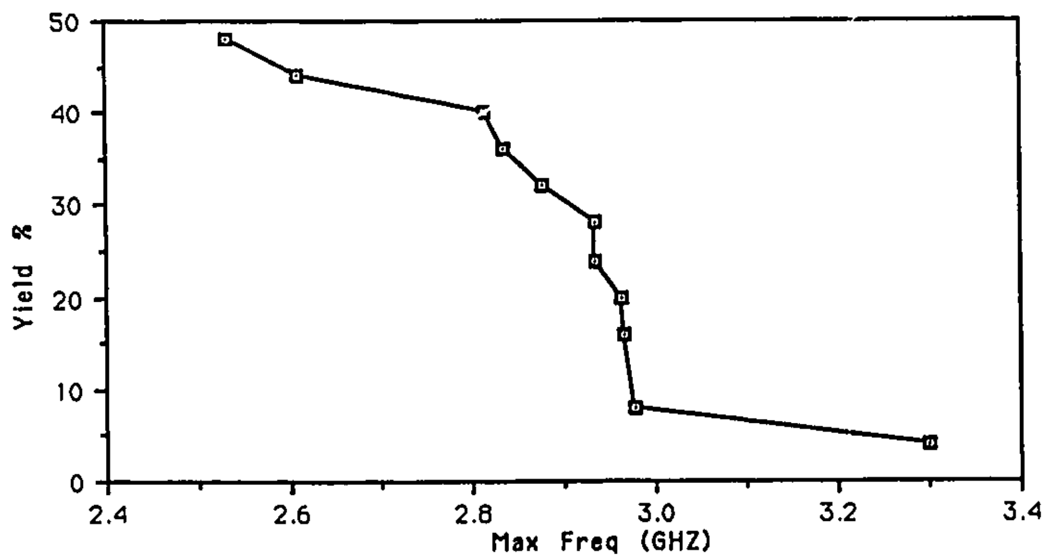


Figure 4.9: Yield of SCFL inverters vs. Frequency

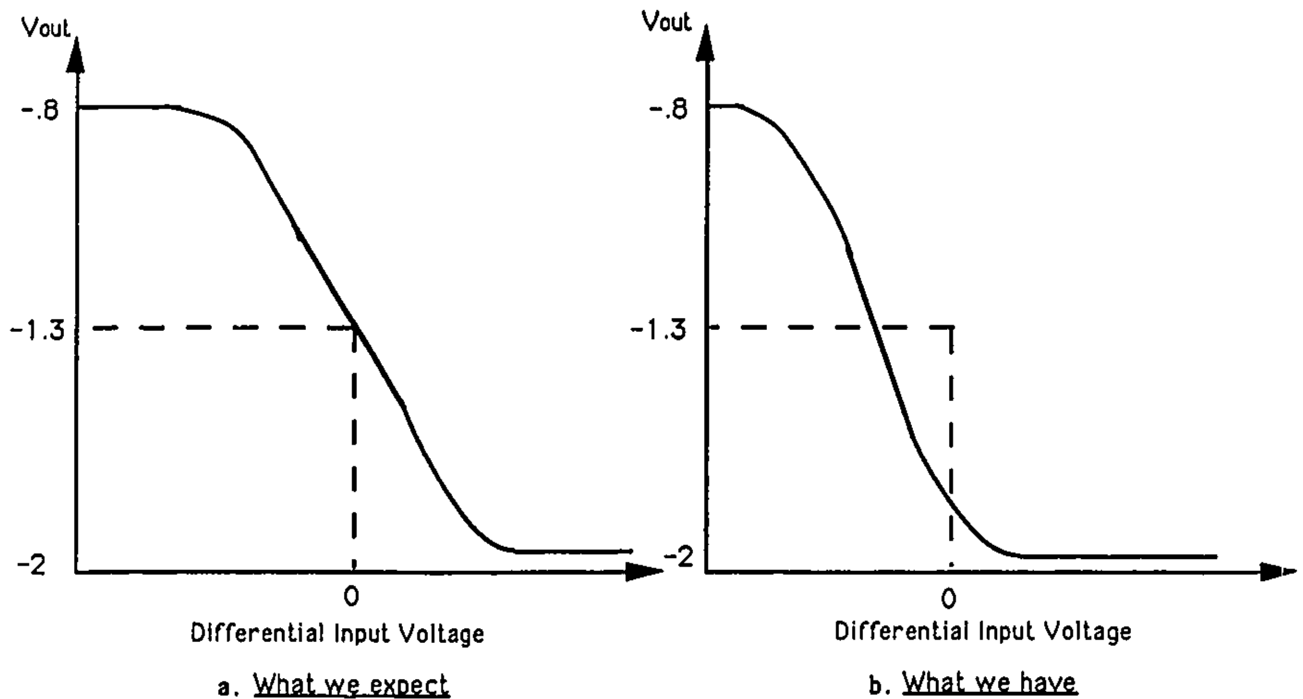


Figure 4.10: Cell Transfer Function.

4.2.2 Duty Cycle

Another problem with the Gallium Arsenide SCFL low speed output cell is that the clock output duty cycle drops below 45%, this is another reason for getting very poor yield. A suitable clock duty cycle is required for proper detection of the signal logic by the loading ECL circuit. The duty cycle specification is to get a high clock output between 45% and 55% of the total clock cycle. Measurements for calculating the duty cycle are made at the average point of the output signal. Fig. 4.10(a) shows the expected transfer function for getting a proper duty cycle. However what we have is an incorrect transfer characteristic as shown in Fig. 4.10(b). The measured duty cycle as a function of site position in the wafer is shown in Fig. 4.11. A new curve in Fig. 4.12 representing the yield of SCFL circuits can be obtained, then, considering the output clock duty cycle criteria. This figure reveals that the electrical yield further drops to 16% at lower frequency. We note again that all the good sites are grouped in the center of the wafer, which is consistent with the fabrication process being radial.

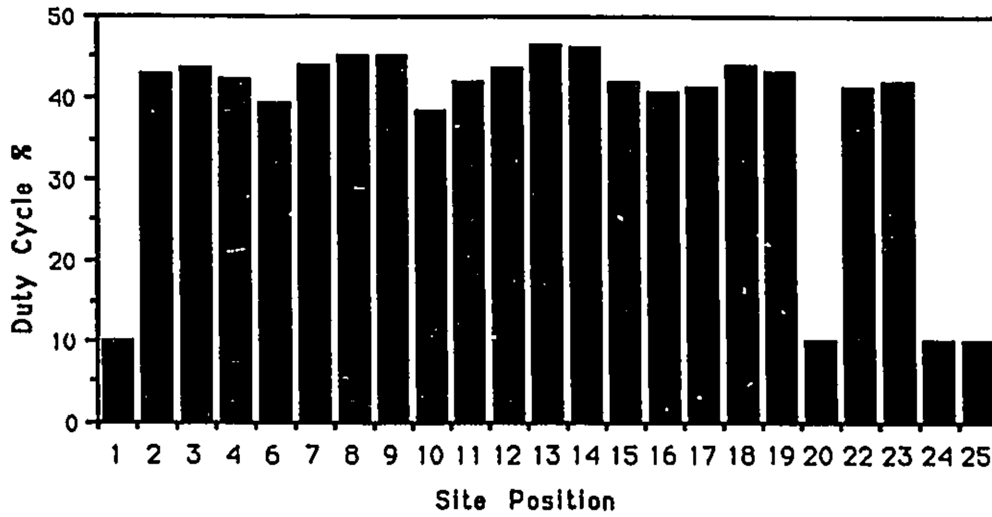


Figure 4.11: Duty cycle vs. Site position

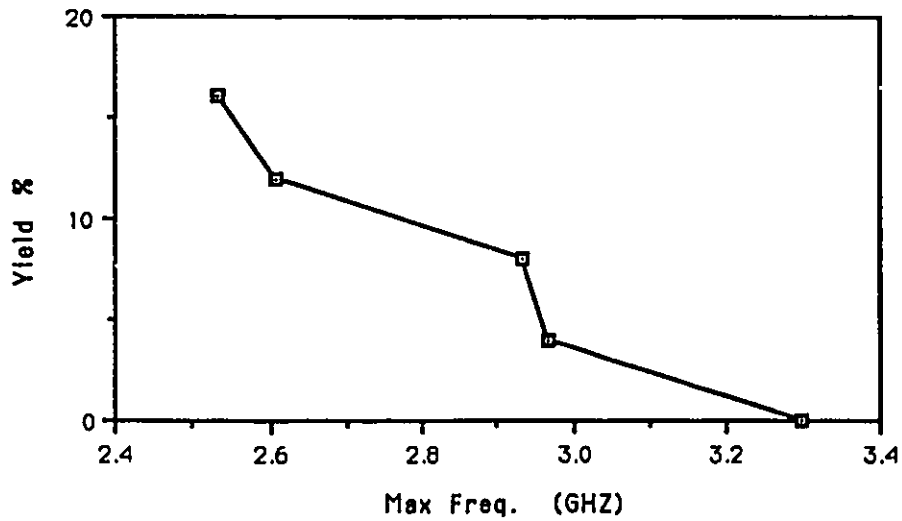


Figure 4.12: Yield of SCFL inverters vs. Frequency, considering Duty Cycle.

4.3 Solution Suggested

From the above section we conclude that the present Gallium Arsenide ECL output cell is really handicapped in terms of both duty cycle as well as output voltage levels that are out of specifications in most of the wafer sites. This causes the electrical yield of SCFL circuits to drop to 48% if one considers only output voltage levels and as low as 16% considering both output voltage levels and clock duty cycle.

The output FET_9 in Fig. 2.5, has a width size of $192\mu m$ and consists of 6 $30\mu m$ FETs in parallel. We tried first to figure out the effect of this transistor on the cell as follows:

- When we reduce the size of FET_9 to $175\mu m$, the high output voltage gets worse.
- When we increase the $192\mu m$ FET to $222\mu m$, we get a better high voltage level but the clock duty cycle falls out of specification.

So the output FET is properly set for normal operation.

We thought also about changing the $20\mu m$ drivers FET_7 and FET_8 of the output ECL cell in Fig. 2.5. The simulation results yields the following conclusions:

- With $30\mu m$ drivers, the rise time gets worse and the high output logic gets slightly worse too.
- With $10\mu m$ FETs, the output cell does not function properly in all sites.

So $20\mu m$ for the drivers looks like some sort of optimum.

4.3.1 Sensitivity to common mode signals

Let's state the input signals V_1 and $V_2 = \overline{V_1}$ in terms of the differential and common mode signals V_{DM} and V_{CM} respectively. We have:

$$\begin{cases} V_1 = & +\frac{V_{DM}}{2} + V_{CM} \\ V_2 = & -\frac{V_{DM}}{2} + V_{CM} \end{cases} \tag{4.1}$$

We have also from the circuit model configuration in Fig. 2.3:

$$\begin{cases} V_1 = & V_{gs_1} + V_e \\ V_2 = & V_{gs_2} + V_e \end{cases} \implies \qquad V_{gs_1} + V_{gs_2} = 2V_{CM} - 2V_e \tag{4.2}$$

Now, in order to determine the differential and common mode gains, we use nodal analysis to find first the current equations of the output cell circuit in Fig. 2.5, as follows:

$$\begin{cases} g_{m_5}V_{gs_5} + \frac{V_o+V_{gs_5}}{r_{ds_5}} &= g_{m_2}V_{gs_2} - \frac{V_e+V_{gs_5}}{r_{ds_2}} \\ g_{m_5}V_{gs_5} + \frac{V_o+V_{gs_5}}{r_{ds_5}} &= -\frac{V_o}{R_d} \\ -g_{m_1}V_{gs_1} + \frac{V_e}{r_{ds_1}} + \frac{V_e}{R_s} &= -\frac{V_o}{R_d} \\ -g_{m_1}V_{gs_1} + \frac{V_e}{r_{ds_1}} - g_{m_2}V_{gs_2} + \frac{V_e+V_{gs_5}}{r_{ds_2}} &= -\frac{V_e}{R_s} \end{cases} \tag{4.3}$$

Replacing V_{gs_1} by its value $\frac{V_{DM}}{2} + V_{CM} - V_e$, in Eq. 4.3 we get:

$$V_e = \frac{g_{m_1}(\frac{V_{DM}}{2} + V_{CM}) - \frac{V_o}{R_d}}{g_{m_1} + \frac{1}{R_s} + \frac{1}{r_{ds_1}}} \tag{4.4}$$

From equation 4.3 we can find V_{gs_5} in terms of V_o:

$$V_{gs_5} = -V_o\frac{\frac{1}{R_d} + \frac{1}{r_{ds_5}}}{g_{m_5} + \frac{1}{r_{ds_5}}} \tag{4.5}$$

If the differential pair formed of FET_1 and FET_2 is made of neighboring FETs, one can safely assume that $g_{m_1} \cong g_{m_2} = g_m$ and $r_{ds_1} \cong r_{ds_2} = r_{ds}$. Using this assumption and substituting Eqs. 4.4 and 4.5 in eq.. 4.3, we end up with the following equation:

$$\frac{g_m R_d}{1 + g_m R_s + \frac{R_s}{r_{ds}}} V_{CM} + g_m R_d \frac{1 + 2g_m R_s + 2\frac{R_s}{r_{ds}}}{1 + g_m R_s + \frac{R_s}{r_{ds}}} V_{DM} = -V_o\Delta \qquad \text{where,} \tag{4.6}$$

$$\Delta = \frac{2g_m + \frac{1}{R_s} + \frac{2}{r_{ds}}}{g_m + \frac{1}{R_s} + \frac{1}{r_{ds}}} + \frac{R_d}{r_{ds}} \frac{\frac{1}{R_d} + \frac{1}{r_{ds_5}}}{g_{m_5} + \frac{1}{r_{ds_5}}} \tag{4.7}$$

From the above equation, the differential and common mode gains A_{DM} and A_{CM} respectively, are deduced:

$$A_{DM} = -\frac{g_m R_d}{\Delta} \frac{1 + 2g_m R_s + 2\frac{R_s}{r_{ds}}}{1 + g_m R_s + \frac{R_s}{r_{ds}}} \tag{4.8}$$

$$A_{CM} = -\frac{g_m R_d}{\Delta(1 + g_m R_s + \frac{R_s}{r_{ds}})} \tag{4.9}$$

We note that FET_5 model characteristics v_{gs_5}, g_{m_5}, and r_{ds_5} show up only in the factor Δ whether in the differential or the common mode gain, which means that this transistor amplifies both differential and common mode signals in the same way. This, though, can be inferred directly from the circuit configuration of the output cell. R_s and R_d are the drain resistance in saturation (r_{ds}) of the pull-down FET_3 and pull-up FET_4 respectively. The common mode rejection ratio (CMRR) which is an important figure of merit parameter, can now be determined from the above results as follows:

$$CMRR = \frac{A_{DM}}{A_{CM}} = 1 + 2g_m R_s + 2\frac{R_s}{r_{ds}} \tag{4.10}$$

The parameters g_m, R_s, R_d, v_{gs}, and r_{ds} are determined from the circuit model equations used for simulating the circuit. The model used is based on the Statz model [27] which is a cubic approximation of the Curtice model. This is one of the models used in the Hspice circuit simulator [28]. The current-voltage relationship which characterizes this model is given in Appendix A.

g_m and r_{ds} are given by:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} |_{V_{DS}=\text{constant}} \tag{4.11}$$

And:

$$r_{ds} = \frac{\partial V_{ds}}{\partial I_{ds}} |_{V_{GS}=\text{constant}} \tag{4.12}$$

As an example we calculated the differential and common mode gains at the DC operating point voltages obtained when simulating the output cell using the Hspice circuit simulator. These turned out to be:

$$A_{DM} = 27dB$$
$$A_{CM} = -14.7dB$$

This gives a CMRR of 42dB which is not high compared with the CMRR of an operational amplifier [26].

4.3.2 Solution and Results

The small CMRR value found suggests that the output cell under study is sensitive to both differential as well as common mode input signals. This further suggests that the cell is dependent on the input levels which determine, to a certain extent, the amount of common mode signal. To find the right input level which drives the cell properly, we designed an input buffer inspired from the SCFL basic inverter circuit, that has lower output voltage levels found consistent with the output cell requirements.

Driving our ECL output cell with this special buffer shown in Fig. 4.13 assures proper biasing of all cell FETs and consequently proper performances of the Gallium Arsenide SCFL output cell as of ECL compatibility. This buffer which is also an SCFL inverter, has 2 more shifting diodes in the output source followers to bring the signal down to the appropriate level sought for our application. The diodes have $15\mu m$ width size each, with a channel length of $1\mu m$, which is the original size of all other diodes. More description of the diodes follows in Appendix A.

The results obtained, output voltage levels, voltage swing and clock duty cycle, using this buffer when simulating the ECL output cell are shown in Table 4.3. As indicated by these data, most of the sites now are performing properly, since the high output voltage V_{OH} is within the ECL interval. Figure 4.14 shows both the old and the new high output levels. The low output level V_{OL}, even though it is shifted up from its previous value ($\cong -1.9Volts$), it is still within the ECL interval. This slight increase in V_{OL} does not reduce the voltage swing of the output signal, in fact, the voltage swing has been further improved. Actually the slight shift in V_{OL} was accounted for by a bigger shift in V_{OH}, clearly seen in Fig. 4.14, and as a result an increase from 2% to 80% in voltage swing has been achieved over the 23 sites. As for the output voltage levels, the clock duty cycle has also improved and is within the specifications in all those sites. An improvement of about 40% is obtained.

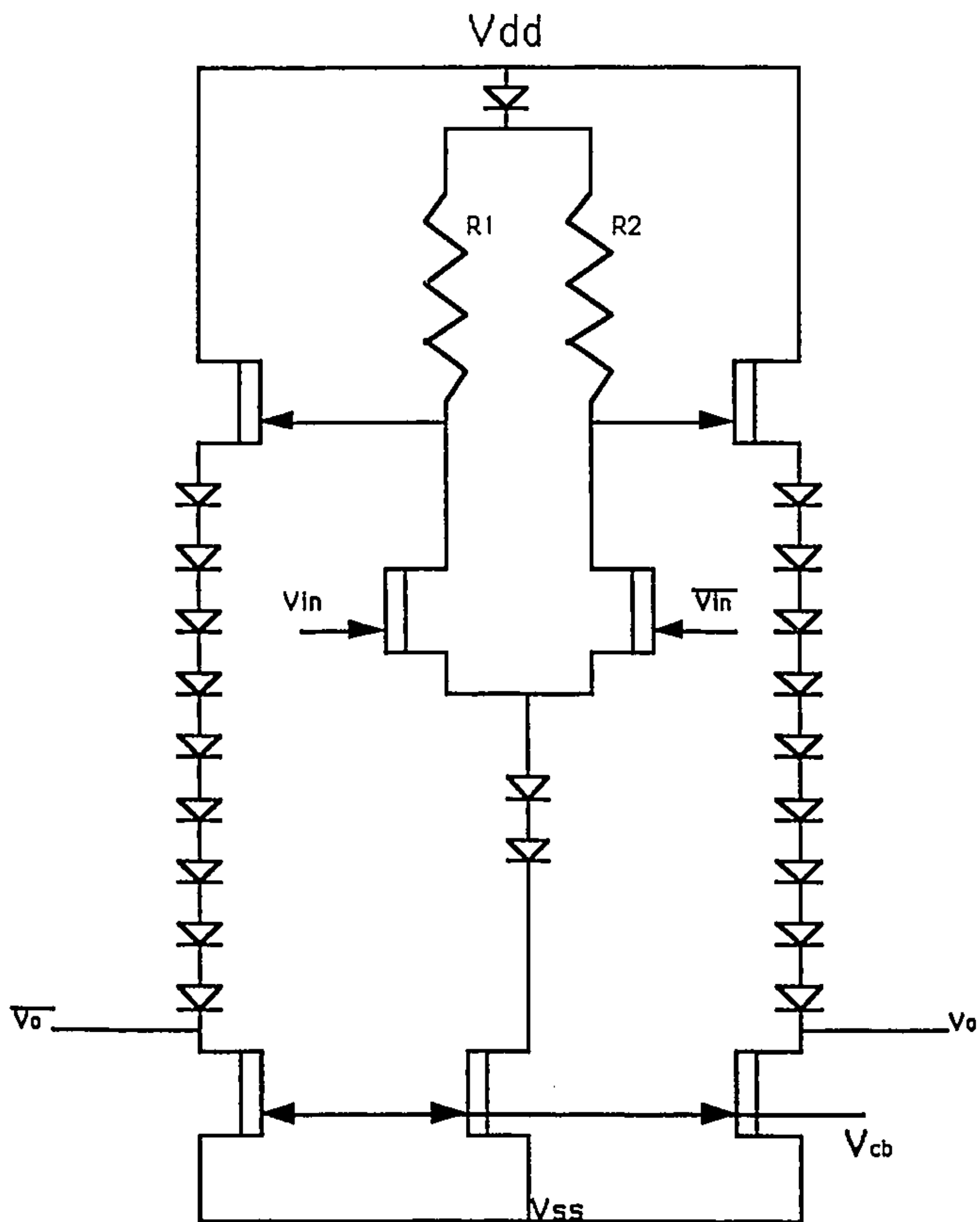


Figure 4.13: Input Buffer Designed to Drive the Output Cell.

	PREVIOUS			NEW		
Site Pos.	High Voltage VH(V)	Low Voltage VL(V)	Volt. Swing VH-VL (V)	High Voltage VH(V)	Low Voltage VL(V)	Volt. Swing VH-VL (V)
1	-1.658	-1.937	0.279	-1.048	-1.996	0.948
2	-0.963	-1.922	0.959	-0.863	-1.851	0.988
3	-0.959	-1.921	0.962	-0.862	-1.852	0.99
4	-0.967	-1.922	0.955	-0.853	-1.821	0.968
6	-1.013	-1.929	0.916	-0.899	-1.869	0.97
7	-0.958	-1.912	0.954	-0.873	-1.856	0.983
8	-0.948	-1.861	0.913	-0.886	-1.808	0.922
9	-0.937	-1.893	0.956	-0.853	-1.815	0.962
10	-1.001	-1.908	0.907	-0.882	-1.858	0.976
11	-1.006	-1.908	0.902	-0.941	-1.923	0.982
12	-0.958	-1.905	0.947	-0.872	-1.847	0.975
13	-0.942	-1.891	0.949	-0.879	-1.829	0.95
14	-0.938	-1.858	0.92	-0.885	-1.811	0.926
15	-1.034	-1.968	0.934	-0.948	-1.975	1.027
16	-0.974	-1.906	0.932	-0.881	-1.891	1.01
17	-0.993	-1.931	0.938	-0.881	-1.864	0.983
18	-0.968	-1.906	0.938	-0.888	-1.856	0.968
19	-0.961	-1.906	0.945	-0.864	-1.839	0.975
20	-1.837	-1.887	0.05	-1.232	-1.941	0.709
22	-1.007	-1.896	0.889	-0.939	-1.923	0.984
23	-1.001	-1.914	0.913	-0.922	-1.941	1.019
24	-1.748	-1.881	0.133	-1.148	-1.948	0.8
25	-1.493	-1.787	0.294	-0.975	-1.867	0.892

Table 4.3: Measurements obtained from new and old Output Cell.

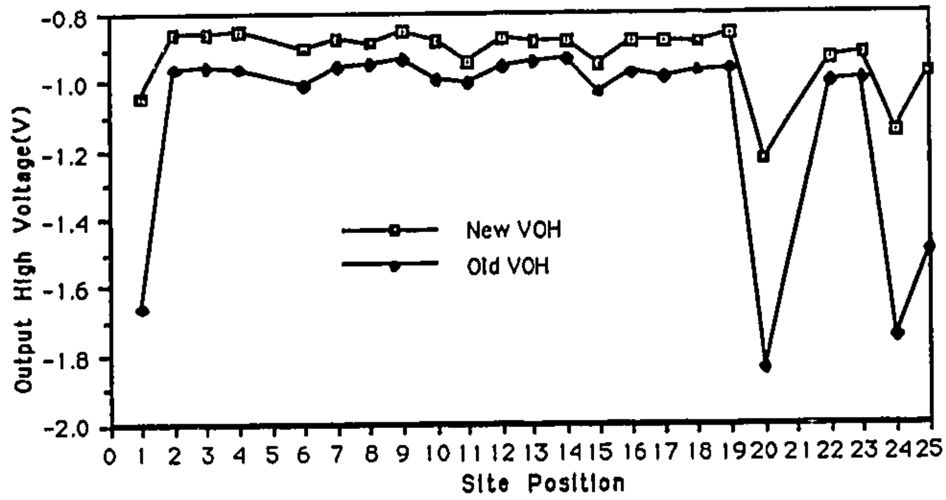


Figure 4.14: High Output Voltage before & after Cell modification

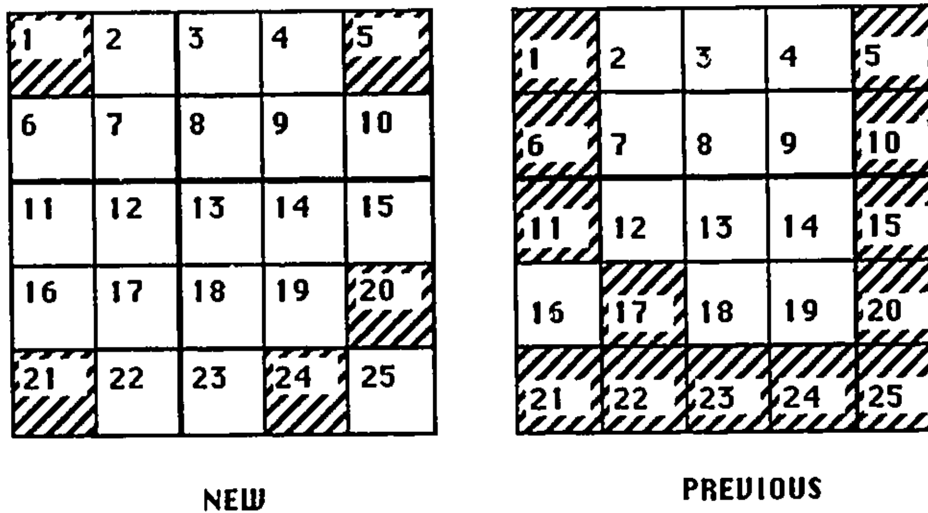


Figure 4.15: ECL-Nonfunctional sites in the wafer before & after Cell modification

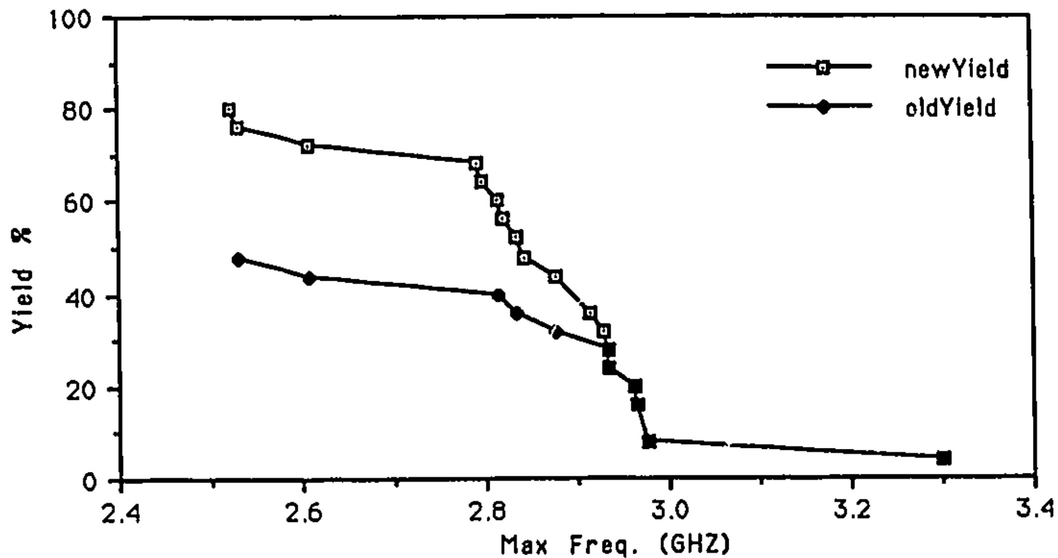


Figure 4.16: New Yield of SCFL inverters vs. Frequency

A new wafer drawing can then be made, to show functional and non-functional sites as was previously done. For the sake of comparison both wafers are drawn in Fig. 4.15. This figure clearly shows that 20 sites are now available, instead of 12, to build Gallium Arsenide SCFL ECL compatible circuits in terms of power supply, voltage levels, voltage swing, and clock duty cycle. Let the SCFL electrical yield curve shown in Fig. 4.9 be called oldYield. The new SCFL electrical yield curve labeled newYield is drawn in Fig. 4.16. This new curve shows that the electrical yield of SCFL ECL compatible circuits is now as high as 80% compared to 48% previously, at the output cell frequency of operation.

When we consider the duty cycle as a second criterion in finding the electrical yield, the number of functional sites is 19 compared to 20 sites in the initial case. The yield then is still high with a 72% value, whereas it was only 16% as stated in section 4.2.2. Both previous and new yield curves considering the duty cycle are shown in Fig.4.17 as old-Yield and new-Yield respectively.

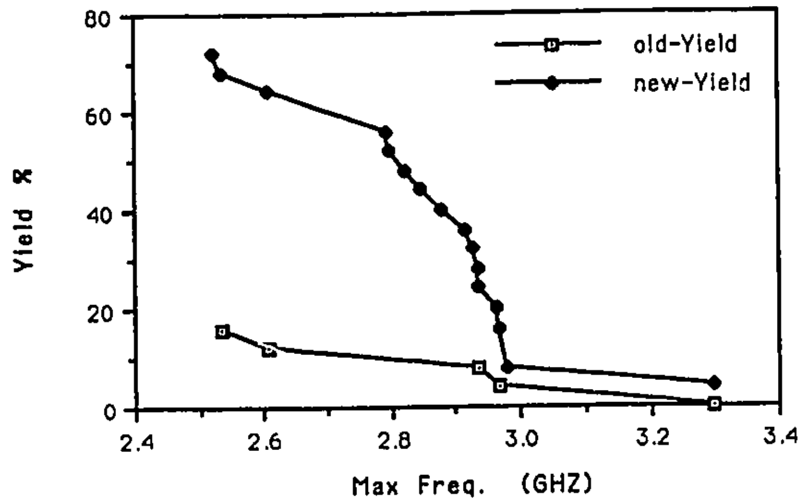


Figure 4.17: Yield of SCFL inverters considering Duty Cycle.

Two choices are possible to implement the above mentioned solution. Firstly, all SCFL inverter cells in all circuits could be modified, but this means increasing the size of all circuits by adding extra diodes which will decrease the chip integration and may affect the gate speed at high frequencies. Secondly, and most appropriately, which is suggested here, is to use this special buffer only once in the circuit to drive the low speed ECL output cell.

4.3.3 Effect on Circuit Complexity

In the yield study done so far, only one site at a time was taken into consideration, and the yield was estimated according to the number of functional sites. Each site contains about 100 SCFL cells, if we assume a functionality of 4 for SCFL cells, this will be equivalent to 400 gates.

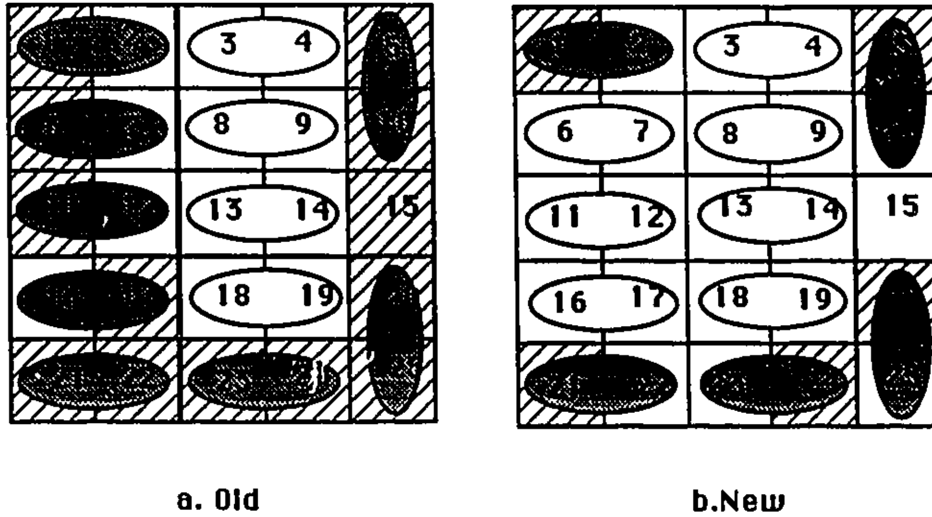


Figure 4.18: ECL-Nonfunctional sites in the wafer for 2-site complexity.

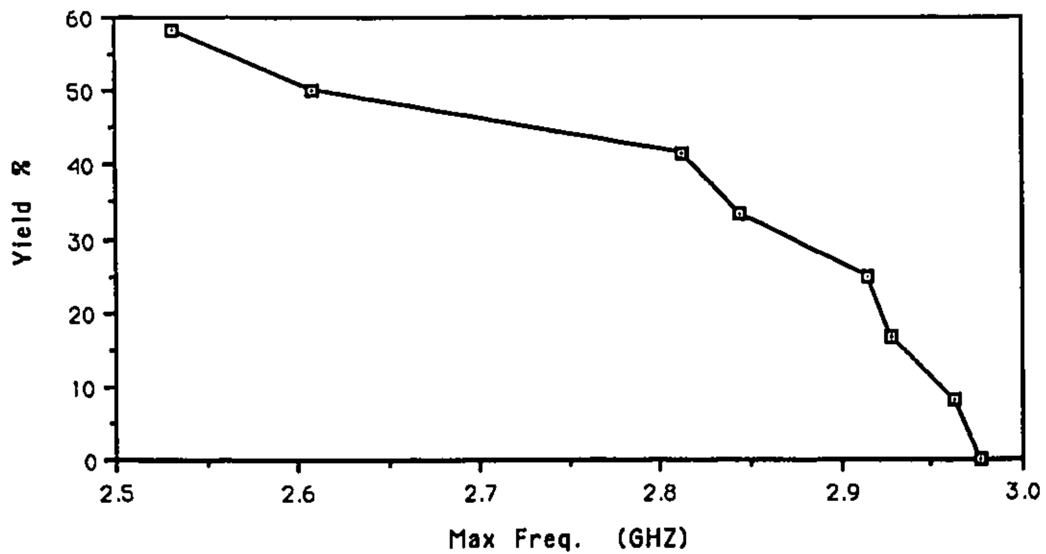


Figure 4.19: Yield of SCFL inverters vs. Frequency with 2-site complexity.

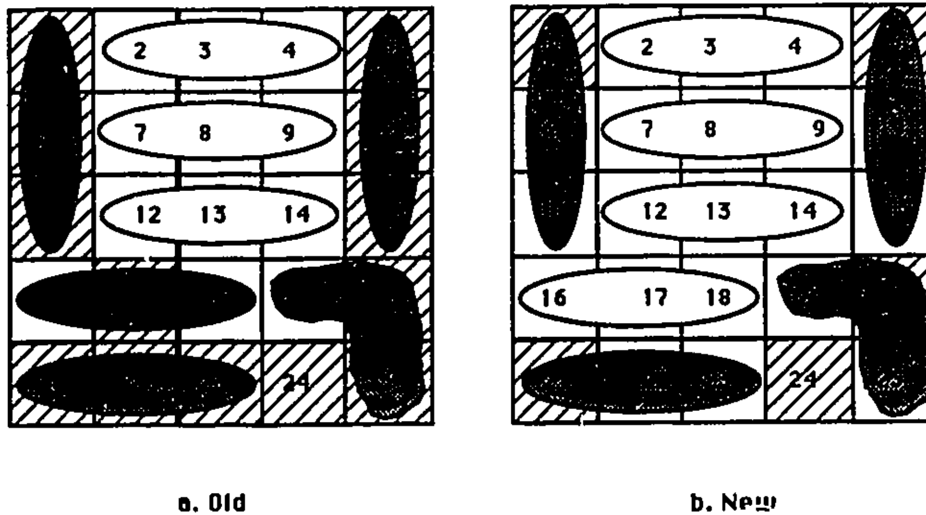


Figure 4.20: ECL-Nonfunctional sites in the wafer for 3-site complexity.

Suppose that we want to fabricate SCFL circuits of 200 cells, then we will have to use two sites at a time. In doing so, some of the individual ECL functional sites will be nonfunctional when taken with a nonfunctional site. Therefore the yield is expected to drop, as the complexity increases. From Fig 4.18 we see that the maximum number of functional circuits with an ECL interface will be 7 out of 12 that is the best yield will be 58% instead of 80% when taking one site at a time. This is a decrease in yield, however, an improvement of 66% is obtained over the previous case where the best expected yield was only 35%. The yield versus frequency characteristics for the new complexity is shown in Fig 4.19. The idea used in drawing these characteristics is that if we take two sites with different maximum operating frequencies, then the maximum operating frequency of the new higher complexity site will be equal to the minimum of the maximum frequencies of the two sites.

If we increase the complexity and take three sites at a time which will be equivalent to 600 cells per circuit, there will be 4 ECL functional sites out of 8, as shown by the non-shaded sites in Fig. 4.20. Consequently, the maximum yield that can be achieved will

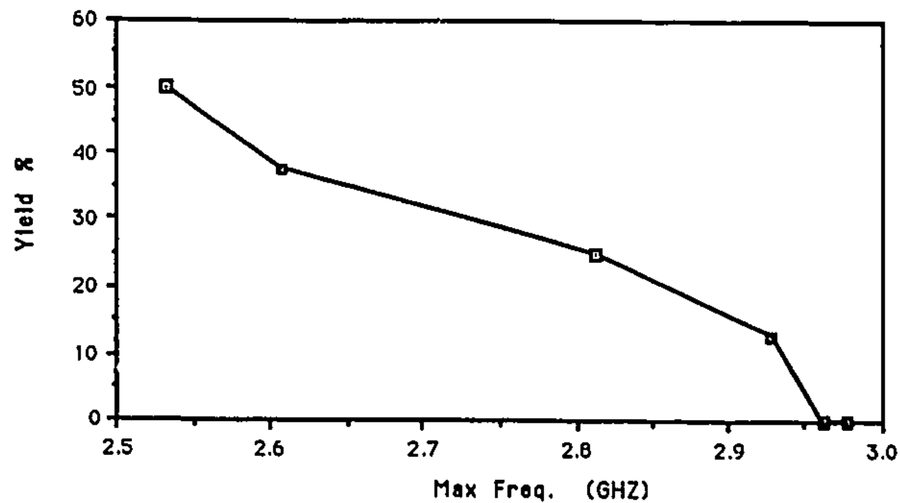


Figure 4.21: Yield of SCFL inverters vs. Frequency with 3-site complexity.

be 50%. Using the same idea as for the previous case, a new yield versus frequency characteristic is drawn in Fig. 4.21. Here again the electrical yield for three level complexity is increased from 37.5% to 50% which in a considerable improvement. Previous and new 1, 2, and 3-site complexity yield curves are superimposed in Fig. 4.22 for comparison.

A conclusion to this chapter is that the problems of the SCFL output cell as not being ECL compatible in most parts of the wafer have been solved. The cell output voltage levels and clock duty cycle are within specifications and the electrical yield has been highly improved.

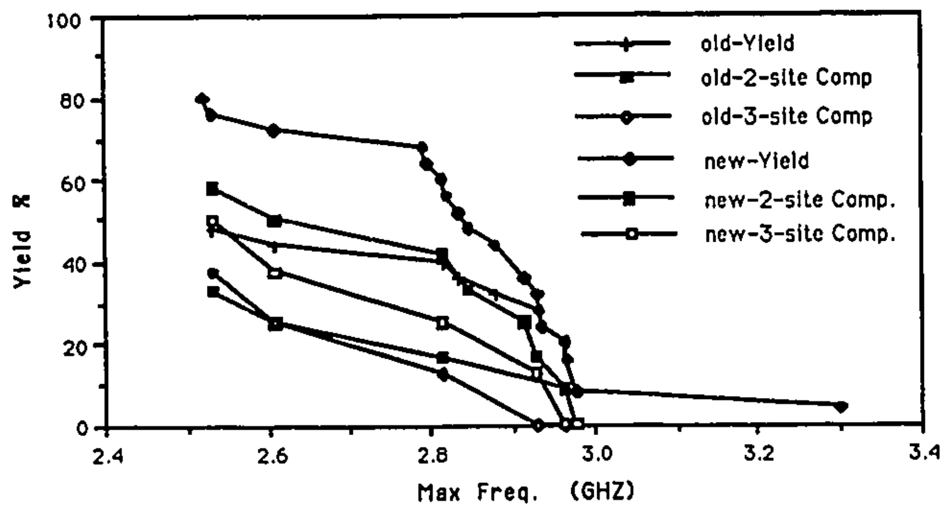


Figure 4.22: Yield of SCFL inverters vs. Frequency 1, 2, and 3-site complexities.

Chapter 5

Conclusion

In this thesis a solution to the silicon ECL compatibility of Gallium Arsenide SCFL VLSI circuits, in terms of output voltage levels, voltage swing and output clock duty cycle, was presented and the yield was highly improved. A buffer circuit was designed to drive the Gallium Arsenide ECL output cell. The simulation results proved the effectiveness of the use of the buffer circuit since the electrical yield was raised to 80% while it was only 48% previously. With this solution, the parameter non-uniformity does not affect the functioning of the SCFL circuits in most of the wafer sites. Furthermore, the duty cycle of the output ECL cell was brought within specifications in nineteen (19) sites, whereas before, only four (4) sites were accepted when considering duty cycle as a second determining factor in calculating the electrical yield. In summary we have:

- 20 sites have correct ECL voltage levels vs. 12 sites previously.
- 19 sites have acceptable clock duty cycles vs. only 4 previously.

The solution was proven effective also when considering high complexity SCFL circuits, where more than one site is needed to build the required circuit. In this case the calculated electrical yield was highly improved even for three site-complexity Gallium Arsenide SCFL circuits.

The double-phase series gating SCFL circuit design method was proven to be more resistant to the threshold voltage fluctuations than the single-phase parallel FET design method. Therefore, the double-phase series gating design method was chosen to make our circuits for this research.

The latency problem, which occurs when the SCFL circuit is driven at both high and low frequency signals, was solved. In fact, the latency time period was reduced by one sixth from its previous value and consequently the circuit maximum frequency of operation was highly improved and the circuit complexity was increased by up to six times. So we have:

- 75% improvement in latency time period ΔT
- up to 40% increase in frequency of operation

For more complex circuits, where a large number of gates are connected in series, the latency time period will accumulate from gate to gate and can affect the circuit response. In this case, it is advisable to use retiming flip-flops to synchronize all signals by a single clock signal. This way, the latency will disappear and start accumulating again from a zero value until the next retiming flip-flop, if required. Further research should consider the calculation of the exact number of gates after which synchronization of the signals is required and where, in the wafer, a flip-flop can be introduced.

Another alternative to design SCFL ECL compatible circuits is to use SCFL output levels instead of Silicon ECL levels, and design a Silicon circuit with an SCFL compatible input port and an ECL compatible output port. Other interesting topics consist of performing the same study done here, ECL compatibility of SCFL circuits, for other Gallium Arsenide logic families.

Appendix A

Transistor and Diode Models

The simulation of high speed Gallium Arsenide integrated circuits requires the use of accurate models for the active devices and for passive circuit elements. For our research we used a popular circuit simulation tool for IC design which is HSPICE[1]. At room temperature the SCFL circuits were functioning as required, so to account for temperature changes and parameter variations with temperature we ran simulations at the worst case temperature 150 degrees celsius. The models for Schottky barrier diode and Gallium Arsenide MESFET transistor are presented in the following sections.

A.1 Transistor Circuit Model

Because of the limited voltage swing and low power requirements of Gallium Arsenide logic circuits, an accurate dc model over all operating regions is especially critical. Many MESFET models were reported in the literature [10], [27], [28]. Fig. A.1 presents a schematic diagram of the equivalent circuit commonly used to model the Gallium Arsenide MESFET device. The controlled current source, $I_D(V_{GS,i}, V_{DS,i})$, at the center constitutes the key element for the dc model. It produces a drain current that is dependent on the internal gate-to-source (GS) and gate-to-drain (GD) voltages across the two

[1]HSPICE: Circuit simulation software, a product of Meta-Software, Inc. 1300 White Oaks Road, Campbell, CA 95008

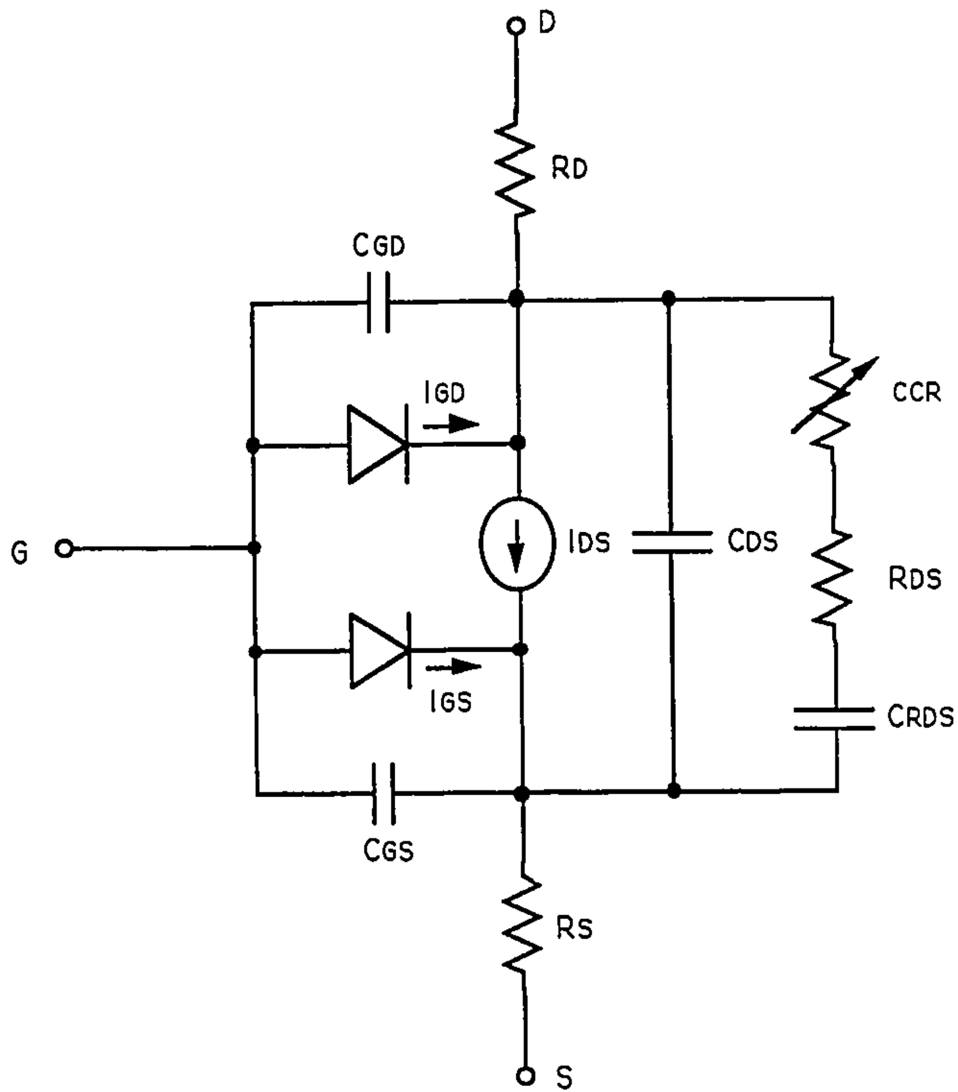


Figure A.1: MESFET equivalent circuit

junction diodes. This model in an improvement of the JFET model, modified to accommodate more accurately the Gallium Arsenide MESFET.

It is a cubic approximation of the Curtice model [27] and is represented by the following equations:

Let:

$$V_{GST} = V_{GS} - (V_{to} + \gamma_{DS} \cdot V_{DS}) \tag{A.1}$$

The drain current is given by:

For: $V_{GST} < 0$

$$I_{DS} = 0. \tag{A.2}$$

For: $V_{GST} > 0, V_{DS} < \frac{3}{\alpha}$

$$I_{DS} = \beta_{eff} V_{GST}^2 (1 + \lambda V_{DS}) \left[1 - (1 - \frac{\alpha V_{DS}}{3})^3\right] \tag{A.3}$$

For: $V_{GST} > 0, V_{DS} > \frac{3}{\alpha}$

$$I_{DS} = \beta_{eff} V_{GST}^2 (1 + \lambda V_{DS}) \tag{A.4}$$

Where:

$$\beta_{eff} = \frac{\beta \cdot W \cdot M}{L(1 + U_{crit} \cdot V_{GST})} \tag{A.5}$$

And:

V_{to}: is the threshold voltage.

γ_{DS}: is the drain voltage induced threshold voltage lowering coefficient.

β: is the transconductance parameter gain.

α: is the saturation voltage parameter.

λ: is the channel length modulation parameter.

U_{crit}: is the critical field parameter for mobility degradation.

W and L: are the MESFET width and length respectively.

M: is the number of fingers.

Table A.1 shows most MESFET model parameters used in the Hspice simulator with typical values.

Name	parameter	Units	Typ. Value
V_{to}	Threshold voltage	V	-1.128
β	Transconductance parameter	A/V^2	120.3e-6
λ	Channel length modulation parameter	1/V	-23.62e-3
α	Saturation voltage parameter	1/V	3.732
R_G	Gate ohmic resistance	Ω	8.3
R_S	Drain ohmic resistance	Ω	774
R_S	Source ohmic resistance	Ω	774
γ_{DS}	Drain voltage, induced threshold voltage lowering coefficient	-	-67.16e-3
U_{crit}	Critical field for mobility degradation	cm/V	0.288
I_S	Gate junction saturation current	A	73.0e-15
n	Gate junction ideality factor	-	1.14
C_{GS}	Zero bias GS junction capacitance	F	906e-18
C_{GD}	Zero bias GD junction capacitance	F	150e-18
C_{DS}	Drain to source parasitic capacitance	F	220e-18
V_{BI}	Gate diode built-in voltage	V	0.9

Table A.1: Hspice model parameters for GaAs MESFET

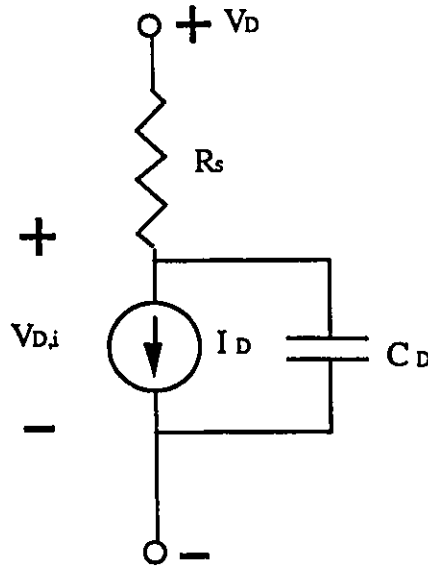


Figure A.2: Schottky Barrier Diode equivalent circuit

A.2 GaAs Diode Model

The diode we used for level shifting in SCFL circuits is one of the high performance components available in Gallium Arsenide IC technology and known as the Schottky barrier diode (SBD) [15]. Fig. A.2 shows the diode equivalent circuit used in the Hspice simulator. The characteristic equation modeling the diode is:

$$I_D = I_S \left[\exp\left(\frac{qV_{D,i}}{nkT}\right) - 1\right] \tag{A.6}$$

Where:

I_s: is the diode saturation current.

n: is the ideality factor.

k: is Boltzmann's constant.

T: junction temperature in Kelvin.

The above equation is for an ideal diode. To account for the series resistance which is due to the contacts, neutral n-GaAs, and current crowding at the edges of the contacts,

the following equation is used to incorporate this series resistance by defining $V_{D,i}$ as:

$$V_{D,i} = V_D - I_D R_S \tag{A.7}$$

Where:

I_D: is The current through the diode.

V_D: is the voltage across the actual diode.

R_S: is the total parasitic diode resistance.

Appendix B

Latency Effect on Frequency

The effect of latency on the maximum frequency of operation of the circuit can be seen through this simple mathematical formula reported in [19]. Let ΔT be the latency time period, and T_{PIN} be pulse width of the high frequency input for a XOR gate, then the output pulse width will be:

$$T_{POUT} = T_{PIN} - \Delta T \tag{B.1}$$

So, for an input signal of period T_{IN}, where:

$$T_{IN} = 2T_{PIN} \tag{B.2}$$

The output signal period will be T_{OUT}, where:

$$T_{OUT} = 2T_{POUT} = 2T_{PIN} - 2\Delta T \tag{B.3}$$

Substituting Eq. B.2 into Eq. B.3 we get:

$$T_{IN} = T_{OUT} + 2\Delta T \tag{B.4}$$

In terms of frequency, Eq. B.4 yields:

$$f_{IN} = \frac{f_{OUT}}{1 + 2\Delta T f_{OUT}} \tag{B.5}$$

Where: $f_{IN} = \frac{1}{T_{IN}}$, and $f_{OUT} = \frac{1}{T_{OUT}}$

For a gate whose maximum frequency of operation is f_{MAX}, the maximum input frequency,

taking the latency into account, can be deduced from Eq. B.5 by just replacing f_{OUT} by f_{MAX}, which gives:

$$f_{InMAX} = \frac{f_{MAX}}{(1 + 2\Delta T f_{MAX})} \tag{B.6}$$

From equation B.6, and assuming that the latency accumulates from gate to gate, we can find the maximum frequency of operation for a circuit of n-levels of XOR gates, as follows:

$$f_{InMAX} = \frac{f_{MAX}}{1 + 2n\Delta T f_{MAX}} \tag{B.7}$$

Bibliography

[1] D. A. Hodges and H. G. Jackson, *Analysis and Design of Integrated Circuits,* Chap. 11, McGraw-Hill, New York, 1988.

[2] O. Wing, *Gallium arsenide digital circuits,* Kluwer Academic Publishers, 1990.

[3] G. W. Taylor, *et al.,* "A comparison of Si MOSFET and GaAs MESFET enhancement/depletion logic performance," *IEEE Trans. Electron Devices,* vol. ED-32, no. 9, pp. 1633-1640, Sept. 1985.

[4] K. Lee, *et al., Semiconductor Device Modeling for VLSI,* Prentice-Hall, New Jersey, 1993.

[5] R. D. Skinner, "What GaAs Chips Should Cost," *IEEE GaAs IC Symp.*, pp. 273-276, 1991.

[6] D. V. Morgan, "Gallium Arsenide a New Generation of Integrated Circuits," *IEE Review,* pp. 315-319, September 1988.

[7] H. Thomas, *et al., Gallium Arsenide for Devices and Integrated Circuits,* Peter Peregrinus Ltd., London, 1986.

[8] M. J. Howes and D. V. Morgan, *Gallium Arsenide Materials, Devices, and Circuits,* Chap. 13, Wiley, New York, 1985.

[9] S. I. Long, "Noise-Margin limitations on gallium-arsenide VLSI," *IEEE J. Solid-State Circuits,* vol. 23, pp. 893-900, Aug. 1988.

[10] S. I. Long and S. E. Butner, *Gallium arsenide digital IC design*, Chap. 1, McGraw-Hill, New York, 1990.

[11] A. A. Sharratt and S. Ward, "Comparison of Current- Switched Logic Gates for High-Speed Communications Applications," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 307-309, Feb. 1990.

[12] S. Katsu, *et al.*, "A Source Coupled FET Logic-A New Current-Mode Approach to GaAs Logics," *IEEE Transactions on Electron Devices*, vol. ED-32, no. 6 pp. 1114-1118, June 1985.

[13] M. Idda, *et al.*, "Analysis of high speed GaAs source-coupled FET logic circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, no. 1, pp. 5-10, Jan. 1984.

[14] T. Vu, *et al.*, "The Performance of Source-Coupled FET Logic Circuits that use GaAs MESFET's," *IEEE J. Solid-State Circuits*, vol. 23, no. 1, pp. 267-279, Feb. 1988.

[15] S. I. Long and S. E. Butner, *Gallium arsenide digital IC design*, Chap. 4, McGraw-Hill, New York, 1990.

[16] D. A. Hodges and H. G. Jackson, *Analysis and Design of Integrated Circuits*, Chap. 7, McGraw-Hill, New York, 1988.

[17] S. I. Long and S. E. Butner, *Gallium arsenide digital IC design*, Chap. 3, McGraw-Hill, New York, 1990.

[18] M. G. Buehler and T. W. Griswold, "The Statistical Characterization of CMOS Inverters Using Noise Margins," *J. Electrochem. Soc.*, vol. 83-1, pp. 391-392, May 1983.

[19] Y. Djadi, *Yield Study of GaAs SCFL Circuits*, M.A.Sc. thesis, Dept. Electrical Engineering, University of Ottawa, 1992.

[20] K. Hasegawa, *et al.*, "High Yield and Low Power Multiplexer/Demultiplexer by SCFL," *IEEE GaAs IC Symp.*, pp. 147-150, 1986.

[21] N. Yokoyama, *et al.*, "A 3-ns GaAs 4K/ 1-bit static RAM," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1797-1801, 1985.

[22] S. Shimizu, *et al.*, "An ECL-Compatible GaAs SCFL design method," *IEEE J. Solid-State Circuits*, vol. 5, no. 2 pp. 539-545, April 1990.

[23] S. Katsu, *et al.*, "A GaAs monolithic frequency divider using source coupled FET logic," *IEEE Electron Device Lett.*, vol. EDL-3, no 8, pp. 197-199, Aug. 1982.

[24] W. V. McLevige, *et al.*, "An ECL-Compatible GaAs MESFET 1-kbit Static RAM," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 2 pp. 262-267, April 1987.

[25] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Chap. 6, Wiley, New York, 1984.

[26] N. Scheinberg, "High-Speed GaAs Operational Amplifier," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 4 pp. 522-527, Aug. 1987.

[27] W. R. Curtice, "A MESFET model for use in the design of GaAS integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, no. 5, pp. 448-455, May 1990.

[28] META-SOFTWARE, *HSPICE user's manual H9001*, 1990.