DESIGN AND EVALUATION OF A SIXTEEN STATE AMPLITUDE PHASE KEYED QUASI UNIVERSAL DATA MODEM

by

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ABSTRACT

After a brief discussion of phase shift and amplitude shift keying, the concept of sixteen-state amplitude phase shift beying (16-APK) is introduced and is shown to be the most feasible when high spectral efficiencies are desired.

We then present the design and implementation of a 16-state APK modem taking into account spectral and power efficiency and find the spectral efficiency obtained in excess of three bits per second per hertz. The detailed designs of the modulator and demodulator are presented. The design philosophy of the quasi universal modem concept is discussed, and the modem which is switchable from 16-APK to BPSK or QPSK is implemented.

Evaluations of the modem performance when the modulated signal is perturbed by Additive White Gaussian Noise (AWGN), sinusoidal interference (SI) of varying peak factor, adjacent channel interference (ACI) and Co-channel interference (CCI) are pursued. These evaluations signify a major contribution to the understanding of the 16 APK modulation technique since most published results consider only the AWGN case. Here, we suggest the use of certain theories applicable in the PSK case to explain different phenomena observed during our evaluation. The experimental results for interference in APK systems are compared with existing (limited) theoretical bounds. For the AWGN case, the agreement is within two dB.

This research is expected to accelerate the acceptance of this modulation technique in future industrial application in the light of its higher spectral efficiency and potential power efficiency in non-linear channels.

RESUME

Après une brève discussion sur les modulations d'amplitude et les modulations de phase numériques, nous introduisons la modulation d'amplitude et de phase à 16 états. Nous montrons que, tenant compte de paramètres généraux tels que, facilité de réalisation, faible coût, etc., cette modulation représente le meilleur compromis lorsque de forts rendements spectraux sont recherchés.

Nous présentons ensuite la conception et la réalisation d'un ensemble modulateur-démodulateur (modem) fonctionnant avec une telle modulation (16-APK) et prenant en compte le rendement spectral et "le rendement en puissance." Le rendement spectral obtenu est supérieur à 3 bits par seconde par hertz. Après une description détaillée du modulateur et démodulateur, nous discutons la philosophie générale de ce modem quasi universel, c'est-à-dire convertible de 16-APK en BPSK ou QPSK.

Les performances de ce modem sont évaluées quand le signal modulé est perturbé par un bruit additif blanc gaussien (AWGN), un brouilleur sinusoïdal avec différents facteurs de crête (SI), de l'interférence entre canaux (ACI-CCI). La plupart des publications prenant uniquement en compte le bruit additif (AWGN), ces résultats sont en soit une contribution importante à l'étude de ces modems. Nous suggérons alors l'utilisation de théories applicables au cas

des modulations de phase pour expliquer différents phénomènes observés lors de ces évaluations. Les résultats expérimentaux sont comparés pour ces différents cas avec les limites théoriques (peu nombreuses) existantes. En présence du seul bruit additif (AWGN), les performances obtenues indiquent une dégradation inférieure à deux decibels par rapport à la courbe théorique.

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TABLE OF CONTENTS

		Page
ABSTRACT		ii
RESUME		iv
ACKNOWLEDGEMENT		vi
TABLE OF CONTENTS		vii
LIST OF FIGURES		ix
LIST OF TABLES		xiii
LIST OF SYMBOLS		xiv
I	INTRODUCTION	1
	1.1 The Purpose of This Thesis	1
	1.2 Content of this Thesis	2
II	A REVIEW OF THE LITERATURE	5
	2.1 Introduction	5
	2.2 Possible Modulation Schemes	6
	2.3 Digital Phase Modulation	12
	2.4 Digital Amplitude Modulation	15
	2.5 Combined Digital Phase and Amplitude Modulated Systems	20
III	ON THE DESIGN OF THE MODULATOR	34
	3.1 Introduction	34
	3.2 Functional Description	38
	3.3 Serial to Parallel Converter and Mode Control Logic	41
	3.4 Predistortion Equalization	45
	3.5 Premodulation Data Conditioning and Filtering	53
	3.6 Low-Pass Filter Design	57
	3.7 Base Band Transformation to an Intermediate Frequency	65
	3.8 A Discussion of the Sixteen-State Constellation Diagram	69
IV	ON THE DESIGN OF THE DEMODULATOR	73
	4.1 Introduction	73
	4.2 A Macro View of the Demodulator	75
	4.3 Detection of the Modulated Data	78
	4.4 Harmonic Suppression Using Low-Pass Filtering	80
	4.5 Four-to-Two Level Conversion in the I and Q Channel	82
	4.6 Four-to-Two Decoder Logic for BPSK, QPSK and APK	86

		Page
V	EVALUATION OF MODEM PERFORMACE	88
	5.1 Introduction	88
	5.2 Spectral Performance	89
	5.3 Experimental Analysis of Probability of Error Performance	98
	5.4 Switching Between 16-APK and QPSK or BPSK	112
VI	CONCLUSIONS AND RECOMMENDED FUTURE RESEARCH ..	120
APPENDIX A	....	123
APPENDIX B	....	133
APPENDIX C	....	166
APPENDIX D	....	168
REFERENCES	....	169

LIST OF FIGURES

Figure		Page
2.1	(a) Ideal Nyquist Filter Transfer Function for Impulses	8
	(b) Phase Function of an Ideal Nyquist Filter	8
	(c) Impulse Response of the Nyquist Filter-Nyquist Pulse [2]	8
2.2	Practice Nyquist Filter for Pulse Transmission	10
2.3	Probability of Error Comparison of Coherent and Phase Comparison Detection for BPSK Modulation from [4]	15
2.4	P(e) as a Function of S/N from Equation 2.9	18
2.5	Increase in Signal-to-Noise Ratio to Maintain Fixed Error Rate with Coherent Phase Demodulation from [9]	23
2.6	Probability of Error vs. Signal-to-Noise Ratio from Reference [13]. For the Same Probability of Phase Error	26
2.7	(a) Eight ary Signal Set Design	28
	(b) Sixteen ary Signal Set Design	29
2.8	Probability of Symbol Error as a Function of E_S/N_0 from Reference [15]	30
3.1	16-APK Rectangular Signal State Space Diagram	35
3.2	16-APK Modulator (2-4 Level Converter Method)	36
3.3	16-APK Demodulator	37
3.4	16-APK Modulator (Miyauchi Method) [19]	39
3.5	A Typical BPSK Modulated Channel in the 16-APK Modem	41
3.6	Serial-to-Parallel Converter of Mode Control Logic Block Diagram	43
3.7	Serial to Parallel Converter and Mode control Logic Circuitry	4[illegible]
3.8	Block Diagram Predistortion Equlizer	47

Figure		Page

Figure		Page
3.9	Photograph of Measured	
	(a) Unequalized Receive Pulse Response	48
	(b) Equalized Receive Pulse Response	48
3.10	Predistortion Equalization Circuitry	51
3.11	Photograph of Measured	
	(a) Undistorted Data	52
	(b) Predistorted Data	52
	(c) Eye Diagram Before Equalization	52
	(d) Eye Diagram After Equalization	52
3.12	Data Conditioning and Low-Pass Filter	55
3.13	Bode Magnitude Phase Response (E.C.A.P. Analysis) and Group Delay Measurement	59
3.14	Second Order Low-Pass Filter	61
3.15	Modified 5th Order Low-Pass Butterworth Filter F_0=32KHz	63
3.16	(a) Measured Eye of a 64 kbaud Random NRZ Data Over 1 Symbol	64
	(b) Measured Eye of a 64 kbaud Random NRZ Displayed Over Several Symbols	64
3.17	Modulated BPSK Output Channel	66
3.18	Double-Sideband-Suppressed Carrier Balance Modulator With LO Buffer	66
3.19	Final Configuration for APK Generation	68
3.20	(a) Vector Diagram Output QPSK I	69
	(b) Vector Diagram Output QPSK II	69
	(c) 16-APK State Constellation Diagram	69
3.21	Measured Signal State Space Diagram	72
4.1	16-APK Remodulation-Subtraction Demodulator [29]	74
4.2	16-APK Signal State Space Component Vector Diagram	76
4.3	16-APK Demodulator	77
4.4	Connection of DSB-SC Modulator for Detection	79

Figure		Page

Figure	Title	Page
4.5	Tarnished Bandlimited Data at I Port	80
4.6	Eye Pattern of 16-APK Data at Slicer Input	81
4.7	Receive LPF and Slicer Circuit Diagram for I and Q Channels	82
4.8	(a) Four-Level Representation of the I and Q Channels	83
	(b) Four-to-Two Level Converter	83
4.9	16-APK Demodulator Decoding Logic Circuitry	85
5.1	(a) Spectrum of Random NRZ Data Unfiltered	91
	(b) Spectrum of Random NRZ Data Filtered	91
	(c)-(d) Spectrum of Random NRZ Data Filtered and Modulated	91
	(e) FCC Mask Applied to Translated 16-APK Transmit Spectrum	94
5.2	FCC Mask for 6-GH_2 Band with 8-PSK and 16-APK Emission =35]	97
5.3	Performance of a 16-APK Modem in the Presence of Both Sinusoidal Interference and Gaussian Noise for Various Levels of Inferference from a Single Sinusoid	100
5.4	Performance of a 16-APK Modem in the Presence of Both Sinusoidal Interference and Gaussian Noise for Various Levels of Inferference from Two Sinusoids	101
5.5	Performance of a 16-APK Modem in the Presence of Both Sinusoidal Interference and Gaussian Noise for Various Levels of Inferference from Three Sinusoids	102
5.6	Upper Bound for BPSK for CIR=10 dB, Lowermost Curve PF=0 dB, Uppermost Curve PF=7 dB Intermediate Curves in Increment of 0.5 dB PF [36]	104
5.7	Derived P(e) vs. CNR from Rosenbaum and Glave [27] Bound for a PF=3 dB as in the Case of a Single Sinusoidal Inteferer for a 16-PSK System	106
5.8	Performance of a 16-APK Modem in the Presence of a Bandlimited BPSK Adjacent Channel Interferer Centered 45 kHz above the Desired	

Figure		Page

	Signal, along with Gaussian Noise for Different Levels of Interference	108
5.9	Performance of a 16-APK Modem in the Presence of a Bandlimited BPSK Co-Channel Interferer along with Gaussian Noise for Different Levels of Interference	109
5.10	Performance of a 16-APK Modem in the Presence of a Single Sinusoid, Adjacent and Co-Channel Interference Only	113
5.11	System Configuration for Adaptable Modulation Technique	114
5.12	Performance of the Modem in the BPSK and QPSK White Perturbed by AWGN	116
5.13	16-APK Modem Hardware and Test Equipment	118
5.14	Typical Control Card Hardware	119

LIST OF TABLES

Tables		Page
2.1	P(e) Improvement with S/N Ratio 100 kb/s Data Rate	19
2.2	Optimum Number of Amplitude Levels and Phase Positions for Minimum Peak Power (Numbers Restricted to Powers of 2)	22
2.3	Optimum Number of Amplitude Levels and Phase Positions for Minimum Average Power (Number Restricted to Powers of 2)	22
3.1	Summary of ISI at Sampling Instants from Figure 3.9	49
3.2	ECAP Magnitude Response	57
3.3	ECAP Phase Response	58
3.4	Binary Representation of Constellation Diagram With I and Q Level/Bit Interpretation Shown	71
4.1	4-2 Level Converter Truth Table I and Q Channels	84
5.1	Normalize Transmit Spectrum with Translated Frequencies	93
A.1	Mode Selection Switch Operation	127
A.2	Clock Selection Table	129

LIST OF SYMBOLS AND ABBREVIATIONS

ACI	Adjacent channel interference
ASK	Amplitude shift keying
AWGN	Additive white gaussian noise
b/s	Bits per second
b/s/Hz	Bits per second per Hertz
BER	Bit error rate
BNR	Bell-Northern Research
CCI	Co-channel interference
C/N	Carrier power-to-noise power ratio
CNR	Carrier-to-noise ratio in dB
dB	decibel
dBm	decibel relative to one milliwatt
DOC	Department of Communications
E_b/N_0	Energy per bit-to-noise density ratio
erf(x)	Error function $\frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}dt \leq 1$
erfc(x)	Complementary error function $\frac{2}{\sqrt{\pi}}\int_x^\infty e^{-t^2}dt \leq 2$
FCC	Federal Communications Commission
f_s	Signalling frequency
h(t)	Impulse response
H(f)	Network transfer function
Hz	Hertz
IF	Intermediate frequency
ISI	Intersymbol interference

m	Integer
M	$=2^n$ number of phases in an M-ary PSK signal
N	$=2^n - 1$ period of an n-stage maximal length shift
N	Noise power
NRZ	Nonreturn to zero
PAM	Pulse amplitude modulation
PCM	Pulse code modulation
pdf	Probability density function
P(e)	Probability of error
PRBS	Pseudo-random binary sequence
P/S	Parallel-to-serial
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase-shift keying
RF	Radio frequency
S	Signal power
SI	Sinusoidal interference
S/I	Signal-to-interference power ratio
SIR	Signal-to-interference ratio in dB
S/N	Signal-to-noise power ratio
SNR	Signal-to-noise ratio in dB
S/P	Serial-to-parallel
t	Time variable
T	Symbol Interval
TTL	Transistor-transistor logic
TWT	Travelling wave tube
	Fractional excess Nyquist bandwidth

$\delta(t)$	Dirac delta function or unit impulse function
σ	Standard deviation
	- Rms value of noise voltage
ω	Angular frequency in radians, $= 2\pi f$
ω_c	Carrier (angular) frequency
π	Ratio of the circumference of a circle to its diameter, $\approx 22/7$
$\sum_i$	Summation over i

CHAPTER I

INTRODUCTION

1.1 The Purpose of This Thesis

This research is conducted with the objective of investigating the effect of various interference on a hybrid modulated signal originating from an Amplitude Phase Shift Keyed (APK) modulator-demodulator (modem). This modem was designed and implemented and has possible extended applications to digital microwave and satellite systems.

In the light of increased spectral congestion and more stringent specifications of the emission mask by the regulatory bodies for these systems, the stated research objective takes on greater ambience because of the high spectral efficiency of the modulation technique employed (theoretically four bits per second per hertz). Since the error rate of the modem is not a function of carrier frequency or bit rate, a frequency of 1 MHz and a bit rate of 256 kb/s, which is a multiple of the PCM voice channel bit rate has been selected. These parameters were also attractive because of the ease in obtaining hardware which saved on the implementation time.

The evaluation of the probability of error performance of this modem as a function of carrier and signal-to-noise ratio has been performed in a noise and interference environment. The measured results obtained from the evaluation will be compared with theoretical values when the modulated signal is first in the presence of Additive White Gaussian Noise (AWGN) which is, for the most part present in a typical transmission channel. Secondly, in an environment characterized by AWGN plus Sinusoidal Interference (SI) which simulate conditions where there is co-channel interference. Thirdly, in the presence of AWGN, Cochannel (CCI) and Adjacent channel (ACI) interference as derived from a band-limited Binary Phase Shift Keyed (BPSK) modulated inteferer.

1.2 Content of this Thesis

This thesis is presented in five parts as follows. In Chapter II a review of the relevant literature led from the development of multi-level Phase Shift Keying (PSK) systems, to multi-level Amplitude Shift Keying (ASK) and finally to multi-level Amplitude and Phase Shift Keying (APK) is presented. This chapter is intended to introduce APK, which is the modulation scheme studied in this work, in a chronological manner.

Details of the conception and design of the APK modulator are presented in Chapter III. The overall block diagram of how the system fits together is first presented. The circuit diagram of each block is discussed and relevant design calculations shown. A more in-depth look is taken at filtering. A computer simulation of the magnitude of phase response of the filters along with their actual response as obtained in the laboratory is presented and compared. Variation of propagation conditions in terrestial microwave and satellite systems causes fading which may degrade the error rate so much that the system performance could become unacceptable. Under such conditions the modulation technique can be switched from the APK to Quadrature Phase Shift Keying (QPSK) or BPSK mode depending on the severity of the fade. An explanation of the logic circuitry which makes it possible to switch between the different modes is presented.

Chapter IV considers the design of the demodulator with a similar analysis and presentation as is given in Chapter III. Additionally, circuitry is designed which will compensate for delays in the carrier and symbol clock. Decoding logic is included which detects which mode is being transmitted and automatically adjusts the receiver to accept that mode. These considerations are necessary because carrier and symbol timing recovery subsystems are not incorporated in this research and are assumed to be ideal. This is a realistic assumption for existing modems where the degradation contributed by these subsystems is in the order of 0.2 dB.

The evaluation of the modem in the presence of noise and interference is given in Chapter V. Here the results of laboratory measurements of the probability of error P(e) as a function of Signal to Noise Ratio (S/N) and Carrier to Noise (C/N) is given in graphic form. For each case, there is plotted, the P(e) performance as a function S/N, C/N as is derived theoretically in the references. An attempt to justify any discrepancy is also given.

In Chapter VI a summary and conclusion from the four technical chapters is given. Applications of the results are given and suggestions for improvements to the existing modem are presented. Future research topics based on this thesis are given and finally, a list of references and an appendix consisting of a computer program of the filter simulation are included to assist and further motivate any interested reader. Additional appendices giving circuit design details are also included.

CHAPTER II

A REVIEW OF THE LITERATURE

2.1 Introduction

Recent developments in digital communication systems are such that the importance of the design of highly spectral efficient (large number of b/s/Hz) modems is paramount. This ensures that spectral constraints imposed by the regulatory bodies such as the Department of Communications (DOC) in Canada and the Federal Communications Commission (FCC) in the United States are adhered to. With this view in mind, the design and evaluation of a universal data modem to investigate the performance of various modulation techniques were carried out. This modem has the capability of switching from the APK mode, which gives a spectral efficiency in excess of 3.2 b/s/Hz, when propagations conditions are good to the QPSK or BPSK modes as propagations conditions deteriorate. Automatic switching of operating mode could be obtained by using a pseudo error monitor at the receiver which would command the transmitter to modify its mode in accordance with the severity of the channel degradation. This enables an improved probability of error performance as propagations conditions deteriorate. Of course this is made at the expense of reduced transmission rate. Before embarking on the details of this research in general, or the evaluation of the modem performance in particular, a brief literature review is introduced here. This review forms the basis for the logical choice of 16-state APK as the modulation technique most suited for the generation of spectral efficiencies in excess of 3 b/s/Hz.

2.2 Possible Modulation Schemes

Of the many factors governing the choice of modulation schemes in digital communications, the following are among the most important:

a) Spectral efficiency

b) Performance in noise and interference environment

c) Ability to perform well in a multipath frequency selective fading environment

d) Performance degradation in a nonlinear channel.

The first three can be improved by shaping the overall spectrum in a way that is optimally consistent with the modulation scheme employed. This suggests that filter design should be kept as close to the Nyquist criteria as is practically tolerable, taking into account intersymbol interference (ISI) degradation. Since filtering is of major importance in the consideration of both spectral and probability of error performance, a few basic concepts are worth noting.

Lucky, Saltz and Weldon [1] showed that band pass filters (BPF) and low-pass filters (LPF) are interchangeable using a band-pass low-pass transformation. This transformation essentially states that a LPF is equivalent to a BPF centered at $\omega = 0$ Hz. Thus LPF's are used for bandlimiting the signal spectrum in the modulator. An ideal minimum-bandwidth Nyquist filter has a magnitude of unity up to the cut-off frequency f_1 and zero elsewhere. Its phase response is a linear function of f. The transfer function of this filter is given by

$$H(f) = \begin{cases} 1, & 0 \leq |f| \leq f_1 \\ 0, & \text{elsewhere} \end{cases} \tag{2.1}$$

The impulse response of this filter is

$$h(t) = \int_{-\infty}^{\infty} H(f)e^{j2\pi ft}df = \int_{-f_1}^{f_1} e^{j2\pi ft}df = 2f_1 \frac{\sin 2\pi f_1 t}{2\pi f_1 t} \tag{2.2}$$

The corresponding amplitude, phase and impulse responses are shown in Figure 2.1 [2]. For a train of impulses, the condition of flat amplitude and linear phase vs. frequency filter response results in distortionless transmission thus the signal shape is preserved.

Using an ideal Nyquist filter, Nyquist, in his theorem on minimum bandwidth transmission essentially states that it is possible using an ideal Nyquist filter to transmit symbols at a rate of $2f_s$ symbols per second without intersymbol interference, if the cut off frequency of this filter is f_s

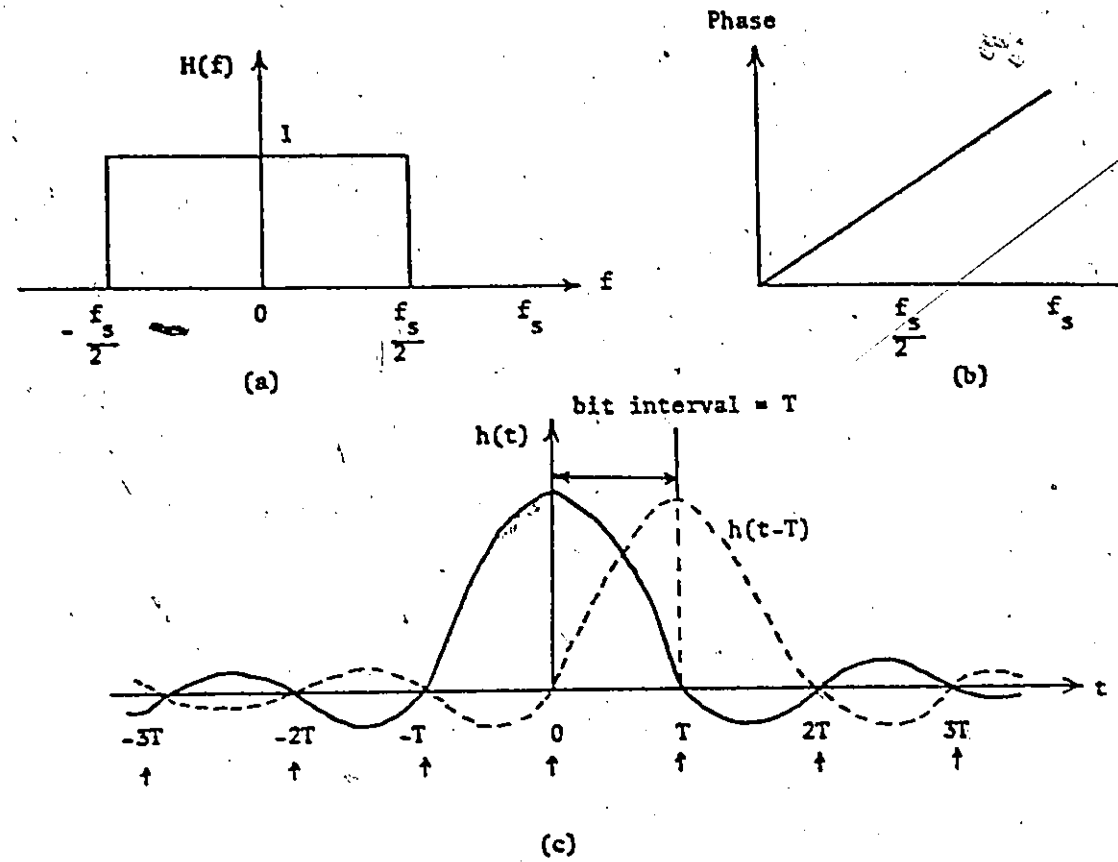


Figure 2.1 - (a) Ideal Nyquist Filter Transfer Function for Impulses.
(b) Phase Function of an Ideal Nyquist Filter.
(c) Impulse response of the Nyquist Filter - Nyquist Pulse [2]

Hz. Thus impulses can be transmitted at intervals of 1/2 fs seconds without interference between the peaks of the received pulses as shown in Figure 2.1c. It is seen that a signal transmitted through an ideal Nyquist filter experiences an amplitude multiplication by a constant and an overall delay due to the phase of the filter. In practice, a filter with a transmission function given in (2.1) is not attainable since it would require infinite roll off and zero phase non linearity. Also, practically, impulse transmission is of no interest, but one rather transmits pulses through the system. Hence, modifications to the above argument is necessary if meaningful band-limited transmission is to be obtained. A very useful solution to the former problem was proposed by Nyquist where he states that if a real-valued transmittance function having a skew symmetry about the cut-off frequency is added to the transmittance of an ideal LPF, the same zero crossings exist as in the case of impulse transmission hence there will be no intersymbol interference [3]. Filters which approximate a sinusoidal roll off are used in practice to solve these problems. The latter problem can be solved by modifying the transmission characteristics of the ideal LPF by the factor whose shape is that of x/sinx. Figure 2.2 shows the shape of a practical Nyquist filter through which pulses are transmitted. This filter has a transmittance

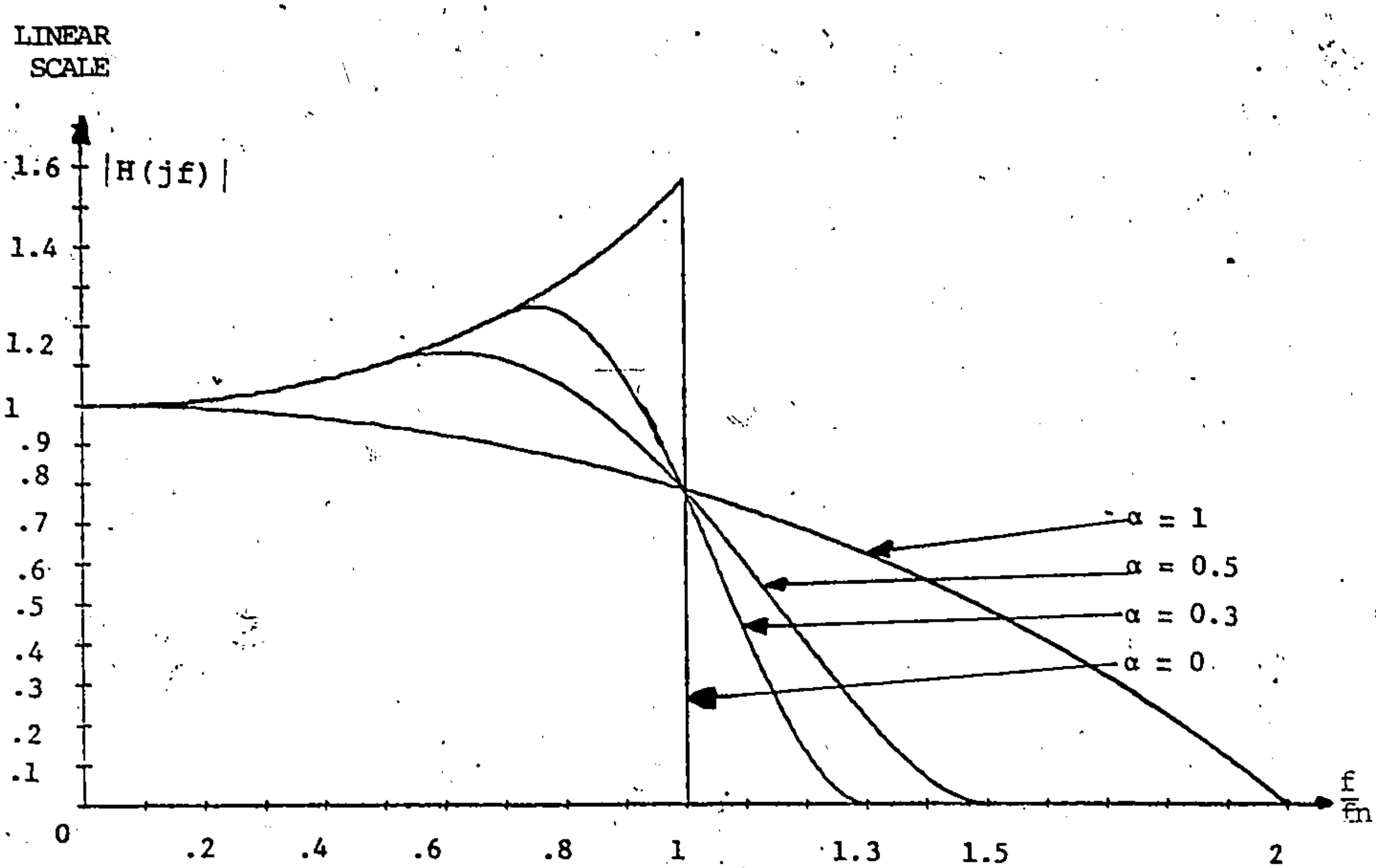


Figure 2.2 - Practical Nyquist Filter for Pulse Transmission

characteristic of the x/sinx shape up to the point where the skew-symmetric roll off begins. The skew-symmetric function (i.e., the raised-cosine function) whose point of skew-symmetry is centered at the Nyquist frequency has zero transmittance outside the region of skew-symmetry. Mathematically, this transmittance function is given by

$$H(f) = \begin{cases} \dfrac{\omega T_s/2}{\sin(\omega T_s/2)} & 0 \le \omega \le \dfrac{\pi}{T_s}(1-\alpha) \\[2ex] \dfrac{\omega T_s/2}{\sin(\omega T_s/2)} \cdot \cos^2\left(\dfrac{T_s}{4\alpha}\left[\omega - \dfrac{\pi(1-\alpha)}{T_s}\right]\right) & \dfrac{\pi}{T_s}(1-\alpha) \le \omega \le \dfrac{\pi}{T_s}(1+\alpha) \\[2ex] 0 & \omega > \dfrac{\pi}{T_s}(1+\alpha) \end{cases} \quad (2.3)$$

where

α - percentage of excess bandwidth over the theoretical Nyquist bandwidth.

T_s - symbol[1] duration.

ω - angular frequency in radians.

Thus a filter with characteristics given by (2.3) will exhibit no intersymbol interference with pulse transmission at the Nyquist rate. Use of the above concepts will be employed in the design of filters used in this work.

Of the set of possible digital modulation techniques the three most popular choices for the type of modulation schemes are,

a) digital phase modulation

b) digital amplitude modulation

1. A "symbol" is a composition of bits assigned to a waveform by the transmittor.

c) combined digital amplitude and phase modulation.

In the following paragraphs, each of these shall be discussed briefly.

2.3 Digital Phase Modulation

In the case of digital phase modulation systems where the information is encoded into the phase of the transmitted carrier, two detection schemes are frequently used, namely coherent and phase comparison detection. In both cases the signal at the receiver is of the form

$$s(t) = \sqrt{2S} \cos (\omega_0 t + \emptyset) \tag{2.4}$$

where S is the signal power, ω_0 is the unmodulated carrier frequency, $\emptyset$ is the phase which takes on values $2\pi k/m$; $0 \leq k \leq m-1$, and m is the number of phase states. In digital phase modulation, the basic problem is to determine $\emptyset$ given that s(t) is received in the presence of AWGN and interference. The noise is of the form

$$n(t) = x(t) \cos \omega_0 t + y(t) \sin\omega_0 t \tag{2.5}$$

where n(t) is a random process, x(t) and y(t) are random variables with zero mean and the average power of n(t) is $\overline{n2} = N$. If coherent detection is used in the receiver, a decision is made as to what was transmitted by comparing the phase of the received signal with a phase reference in the receiver which is idential to the phase reference in the transmitter. Now, the probability of error resulting from noise in the transmission medium when an M-ary signal set is used is equal to the probability that the phase of the signal plus noise does not lie in the region $-\pi/m < \emptyset < \pi/m$ if zero degree is the transmitted undistorted phase. It has been shown by Cahn [4] that for the case of the AWGN channel, the probability density of $\emptyset$ is given by

$$p(\emptyset) = \frac{1}{2\pi} e^{-S/N}[1+ \sqrt{4\pi S/N} \cos \emptyset \; e^{(S/N)\cos^2 \emptyset} . \Phi(\sqrt{2S/N} \cos\emptyset)] \quad (2.6)$$

where

$$\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-x^2/2} dx$$

By integrating (2.6) the probability of error P(e) as a function of signal to noise ratio can be found as follows

$$P(e) = 1 - \int_{-\pi/m}^{\pi/m} p(\emptyset) \, d\emptyset \qquad (2.7)$$

Also integration of (2.6) yields the probability distribution of phase as a function of S/N, and this has been derived by

Norton, Shultz and Yarbrough [5]. Using this result, Cahn [4] showed that as the number of phase states of the modulation scheme is increased, a greater S/N ratio is required to maintain the same probability of error performance. This implies that a shift to the right of the P(e) curves as a function of S/N should be expected if a modulation method with a higher spectral efficiency is used.

For the case of phase comparison detection, a decision is made as to what was transmitted by looking at the phase transition between the pulses. This is achieved by comparing the relative phase of successive signal samples. For multiphase modulation the degradation caused by this detection method is approximately 3db over that of coherent detection. In the binary case, the degradation is somewhat less [6].

Figure 2.3 shows a comparison of the probability of error for binary transmission using coherent and phase comparison detection schemes. Clearly, this shows that coherent phase detection is superior to phase comparison detection.

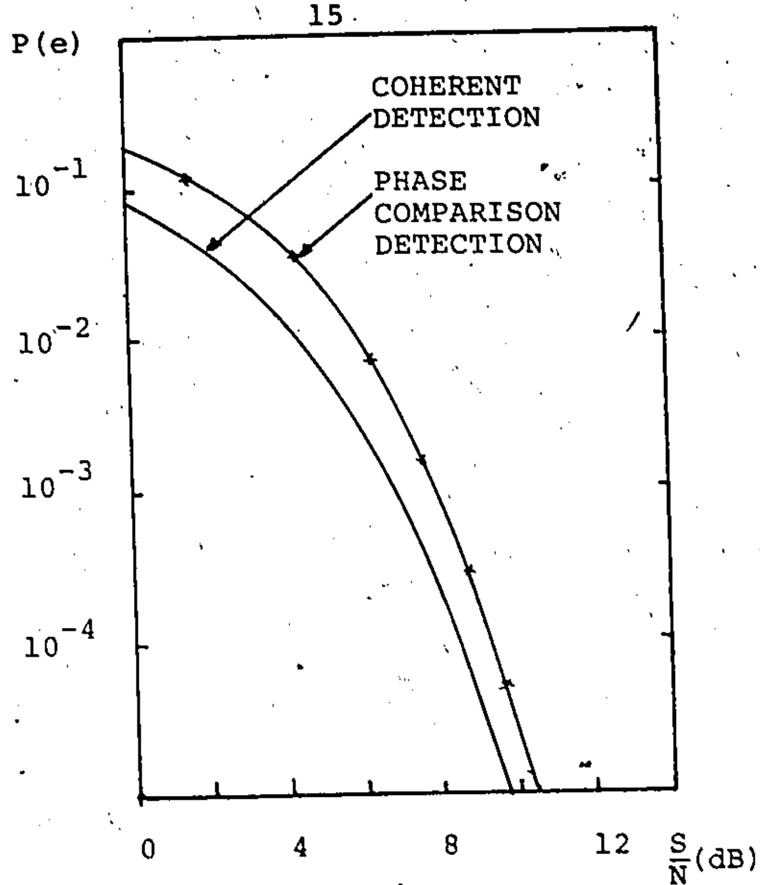


Figure 2.3 - Probability of Error Comparison of Coherent and Phase Comparison Detection for BPSK Modulation from [4].

In summary, one may conclude that M-ary PSK can be used to increase spectral efficiency by increasing the number of phase states. However, this is at the expense of a higher required carrier-to-noise ratio since the number of decision thresholds are increased. For certain M-ary PSK schemes, coherent phase detection is preferred to phase comparison detection as it results in improved probability of error performance for a given signal-to-noise ratio.

2.4 Digital Amplitude Modulation

In digital amplitude modulation, the information is contained in the signal amplitude level. Each amplitude or quantized level is transformed into a code with alphabet size b such that if n is the number of bits per code word, the number of possible quantization levels (M) can be expressed as $M=b^n$.

In considering the bandwidth required to transmit such a signal, it is theoretically possible to transmit 2ω independent pulses over a channel of bandwidth ωHz [7]. Thus, after coding a signal, $2\omega_0$ bauds[2] are being sent where each baud represents n bits. The desired bit rate is therefore $2n\omega_0$ bits per second requiring a bandwidth of $\omega = n\omega_0$. For double sideband transmission the required bandwidth is $2n\omega_0$.

The signal after being received must be of suffcient power such that an error is not made in determining if a "1" or "0" were sent. This is ensured by keeping the signal-to-noise (S/N) ratio at or above some threshold level. With this, the signal power will be great enough to ensure that the probability of error is relatively small for a given transmission rate. For binary transmission, the decision threshold is set to $V_0/2$ where Vo is the amplitude of the bit. If the signal after sampling exceeds $V_0/2$, a "1" is perceived as being sent, conversely, if the sampled signal is less that Vo/2 a "0" is the most reasonable guess as to what was transmitted. In order for the guess to be in error, the noise magnitude at the sampling instant must exceed the

2. A "baud" is a unit of signally speed expressed in symbols per second.

level Vo/2 and must be in the opposite direction to the signal present at that instant. If the noise is white gaussian noise with uniform power spectral density, the probability of error is proportional to the complementory error function of

$$\frac{Vo}{2\sigma} = \sqrt{\frac{S}{4N}} \tag{2.8}$$

where

N = noise power in the bandwidth $\omega = \sigma^2$

σ = rms noise amplitude

S = normalized signal power = $V_0{}^2$

Thus the probability of error P(e) is given by [8].

$$P(e) = \tfrac{1}{2}\left(1 - \text{erf}\,\frac{Vo}{2\sigma\sqrt{2}}\right) = \frac{1}{2}\,\text{erfc}\left(\frac{Vo}{2\sigma\sqrt{2}}\right) \tag{2.9}$$

where $\text{erf}(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2/2}dt$

A plot of this function is shown in Figure 2.4 where it is seen that as the signal power increases the function decreases very rapidly, thus at a large enough values of S/N ratio, the signal received can be interpreted correctly. However, with a slight increase over this threshold S/N value, transmission can be said to be almost perfect.

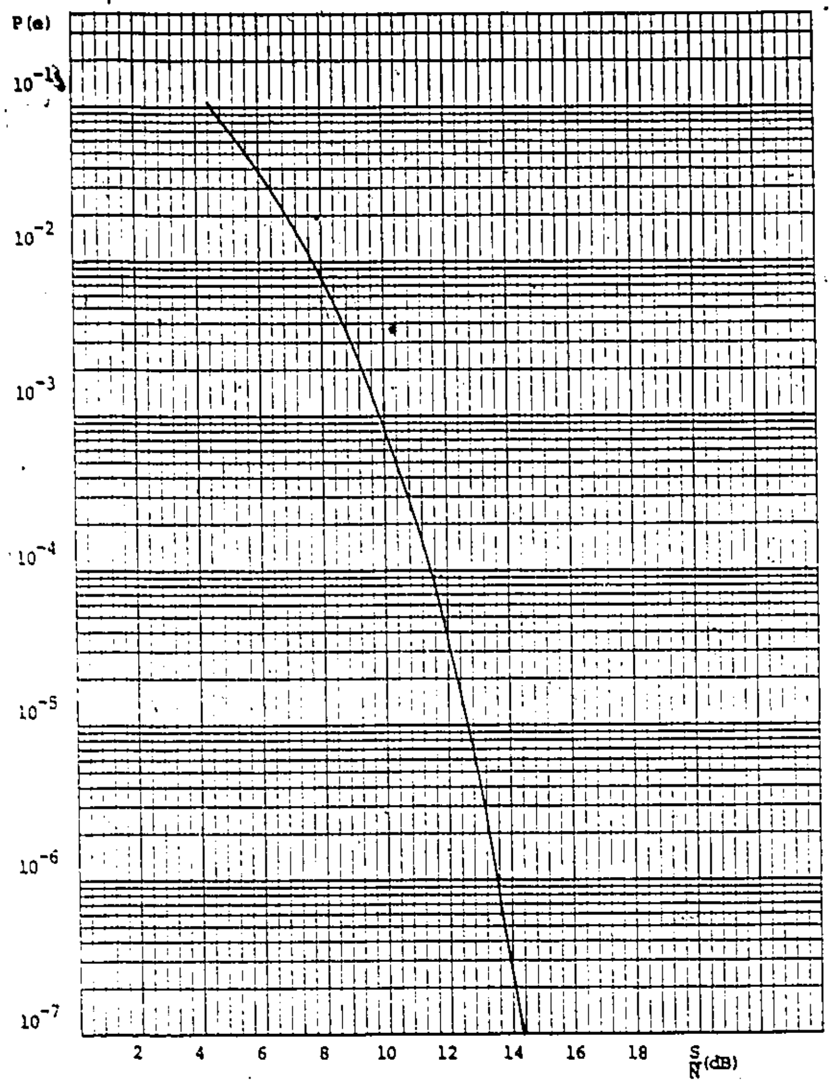


Figure 2.4 - P(e) as a Function of S/N from Equation 2.9

Table 2.1 shows how rapidly the P(e) performance improves with an increase in S/N for a data rate of 100 kb/s.

Table 2.1

P(e) IMPROVEMENT WITH S/N RATIO
100 kb/s data rate in the Nyquist channel

Signal to Noise	Probability of Error	Approximately One Error Every
13.3	10^{-2}	1 msec.
17.4	10^{-4}	100 msec.
19.6	10^{-6}	10 sec.
21.0	10^{-8}	20 min.
22.0	10^{-10}	1 day
23.0	10^{-12}	3 months

From this it is observed that a good threshold is approximately 21 db. Thus, for S/N below this value the error rates may be said to be unacceptable, and a S/N of at least that value would have to be maintained for the system to operate adequately.

For multilevel amplitude modulation, it has also been shown by B.M. Oliver et al. [7] that for a system operating with b different amplitude levels with a constant separation, K, between levels, the average signal powers required is given by

$$S = K^2\sigma^2 \frac{b^2-1}{12} \tag{2.10}$$

From this, we may conclude that the signal power requirements for a PAM system varies as the square of the number of amplitude levels. Cahn [9] showed that the signal power requirements vary linearly with the number of phase positions. Thus less power is required as the number of phase position increase vis-à-vis an increase in the number of amplitude levels. Arthur and Dyn [10] showed that the P(e) for an L-level coherent ASK system is given by

$$P(e) = \left(\frac{1}{\mathrm{Log}_2 L}\right)\left(\frac{L-1}{L}\right) \mathrm{erfc} \left[3/2(\log_2 L) \frac{E_b}{N_0} \frac{1}{(L-1)(2L-1)}\right]^{\frac{1}{2}} \quad (2.11)$$

where

L - number of levels

Eb - energy per bit = ST_b

N_0 - noise power in 1 Hz of bandwidth

T_b - bit duration

2.5 Combined Digital Phase and Amplitude Modulated Systems

It is known that digital phase modulation requires lower signal power to maintain a given signal to noise ratio than does digital amplitude modulation [11]. However, since the amplitude of the modulated signal of a M-ary phase modulation scheme is essentially constant, it is not the optimal scheme if channel capacity is to be maximized. This is a result of Shannon's postulate that a Gaussian amplitude distribution provides maximum transmission capacity when the signal is average power limited [7]. This is one of the main reasons for considering a combination of digital amplitude and phase modulated schemes for transmission of digital data. Thus, there is a significant power saving by the use of combined amplitude and phase modulation schemes for the same number of signal levels as in PSK and PAM systems. Elaborating, it is known that if we wish to increase the number of bits per symbol, it can be done by one of two ways: firstly, the number of phase positions may be doubled while keeping the amplitude level constant. The same can be accomplished by keeping the number of phase positions constant and increasing the number of amplitude levels from one to two with the amplitude levels equally spaced such that uniform probabilities of amplitude and phase are obtained. Thus, the amplitude decision thresholds should be symetrically spaced between adjacent amplitude levels. To simplify coding complexity, it is necessary to limit the number of amplitude levels to some power of two. Therefore if M = n x m is required, where M is the number of states, n is the number of phase positions and m is the number of amplitude positions, then Tables 2.2 and 2.3 give the optimum numbers for m and n when the peak and average power are minimized respectively [9]. The latter two-dimensional modulation scheme results in a significant power saving over pure phase shift keying (PSK) or amplitude shift keying (ASK).

Table 2.2

OPTIMUM NUMBER OF AMPLITUDE LEVELS AND PHASE POSITIONS FOR MINIMUM PEAK POWER (Numbers Restricted to Powers of 2)

Bits per symbol	Total number of states	Number of amplitude levels (m)	Number of phase positions (n)
1	2	1	2
2	4	1	4
3	8	1	8
4	16	2	8
5	32	2	16
6	64	4	16
7	128	4	32
8	256	8	32

Table 2.3

OPTIMUM NUMBER OF AMPLITUDE LEVELS AND PHASE POSITIONS FOR MINIMUM AVERAGE POWER (Number Restricted to Powers of 2)

Bits per symbol	Total number of states	Number of amplitude levels (m)	Number of phase positions (n)
1	2	1	2
2	4	1	4
3	8	2	4
4	16	2	8
5	32	4	8
6	64	4	16
7	128	8	16
8	256	8	32

Figure 2.5 shows the increase in signal to noise ratio (SNR) required to maintain a probability of error of 10^{-4} as the total number of states is increased for the case of coherent phase demodulation. It is seen that the

signal-to-noise ratio requirement decreases from the case of phase modulation (i.e., single amplitude level) to combined amplitude and phase modulation for a fixed number of signal states M. For the case where M=16, it is observed that 16-APK shows approximately a 5dB improvement in SNR requirement over its 16-PSK counterpart.

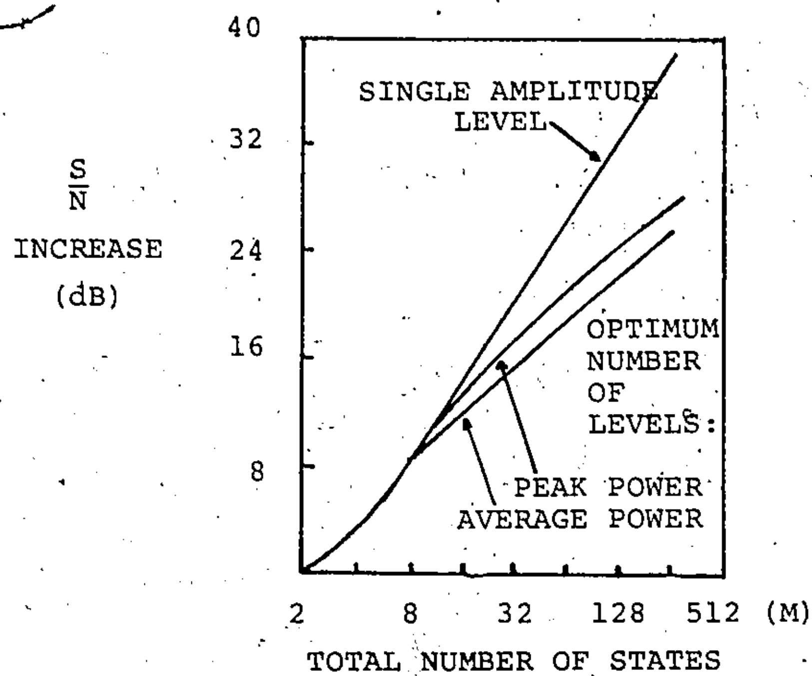


Figure 2.5 - Increase in Signal-to-Noise Ratio to Maintain Fixed Error Rate with Coherent Phase Demodulation from [9].

In a type 1 amplitude phase shift keyed system (APK) [12] that is, a system where the same number of phase positions are available no matter how many amplitude levels are used, Cahn [9] showed that the probability of phase error $P(e\ \emptyset)$ for the k^{th} amplitude is a function both of the normalized amplitude A_k at the k^{th} level and the number of phase positions n_k at the k^{th} level. That is,

$$P(e_\phi) = f(\frac{A_k}{\sqrt{2}} \sin \frac{\pi}{n_k}) \tag{2.12}$$

or more specifically

$$P(e_\phi) = \frac{e^{-(A_k{}^2/2)\sin^2\pi/n_k}}{\frac{A_k}{2} \sin \pi/n_k} \tag{2.13}$$

based on a power spectral density of one watt per hertz in the channel.

Hancock and Lucky [13] have shown that the probability of error for a received symbol is the sum of the probability of phase error and the probability of amplitude error minus the probability of both the amplitude and phase error because the phase and amplitude of the received signals are independent. Since the probability of both errors occurring is small, it can be neglected, Hence, the probability of both amplitude and phase error is twice the $P(e_\phi)$ given in (2.13). In a phase shift keyed system, the $P(e_\phi)$ decreases as the amplitude levels increase. To keep the Pe_ϕ constant on each amplitude level, the number of phase positions on each successive level is increased. Thus

$$P(e) = \frac{2e^{-(A_1^2/2)\sin^2 \pi/n_1}}{\sqrt{\pi}\,\frac{A_1}{2}\sin \pi/n_1} \tag{2.14}$$

This equation assumes all amplitude and phase levels equally probable. The object now is to minimize (2.14) subject to the constraints of average power and variable alphabet size. Hancock and Lucky have derived the required expression as

$$P(e_{min}) = \frac{2e^{-P(8/9M-4/3)}}{\sqrt{\pi}\,\frac{P}{8/9M - 4/3}} \tag{2.15}$$

where P is the average signal to noise ratio remembering that the noise power spectral density is unity and M is the alphabet size. A plot of equation (2.15) gives the minimum probability of error for an APK system as a function of signal to noise ratio and is shown in Figure 2.6. However, systems exibiting characteristics as shown above are very difficult to implement and are not as yet practical. With this type of system, Figure 2.6 shows that there is a 3 dB improvement every time the alphabet size is doubled.

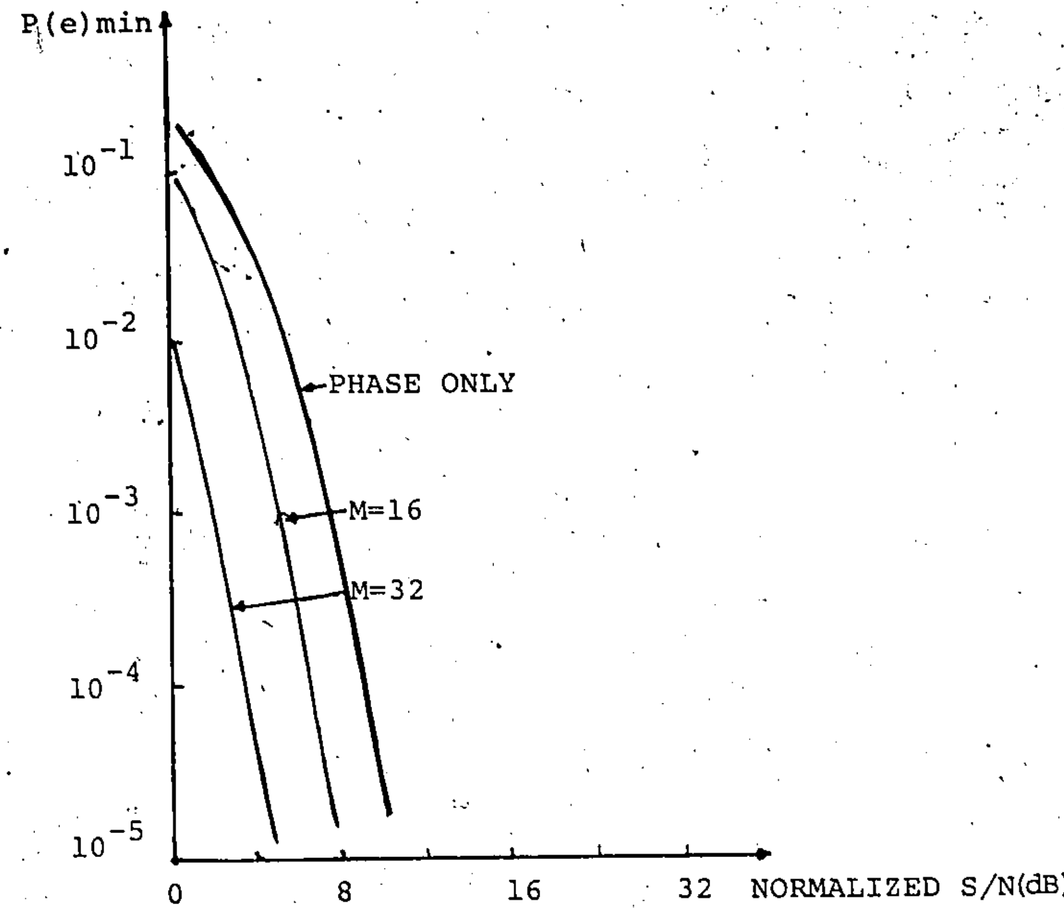


Figure 2.6 - Probability of Error vs. Signal-to-Noise Ratio from Reference [13]. For the Same Probability of Phase Error on each level

It also shows that an improvement in signal-to-noise ratio for a system combining amplitude and phase modulation schemes is a function of alphabet size. Thus, it is obvious that there are advantages in considering digital amplitude phase keying (APK) with M-ary alphabets as a possible highly spectral efficient modulation technique for the future.

Twenty-nine empirically generated signal sets with M-ary alphabets from 4-128 have been investigated to determine the optimal design [14]. With a larger alphabet size, bandwidth conservation is realized and the S/N requirement is not as high as that necessary for M-ary PSK with the same spectral efficiency. It is also true that APK has superior P(e) performance for the same E_s/N_0 ($E_b/N_0=E_s/N_0-6$dB for 16-APK, E_s is the energy in one symbol) to its PSK counterpart [15] although its performance is inferior to PSK in a nonlinear channel due to inherent envelope fluctuation.

Thomas et al. [14] studied M-ary alphabets for M (4, 8, 16, 32, 128). Here we look at two subjects of the set specifically M(8, 16). These configurations give a theoretical bandwidth efficiency of 3 b/s/Hz and 4 b/s/Hz respectively.

For M=8, four configurations were studied, (the notation used for configurations with circular symmetry is [a, b, c] meaning a display consisting of three concentric circles with a signals on the inner circle, b signals on the next circle and so on), they are: (1, 7), (4, 4), 3x3 grid minus the signal at the centre, and a triangular design. Figure 2.7 shows the design of these and also the 16-ary configurations. From Figure 2.8 which shows the P(e) as a function of Es/No for 8- and 16-ary alphabets, it is seen that in the case of 8-ary alphabets, at a probability of symbol error of 10^{-6} the best performance is obtained from (1, 7) signal

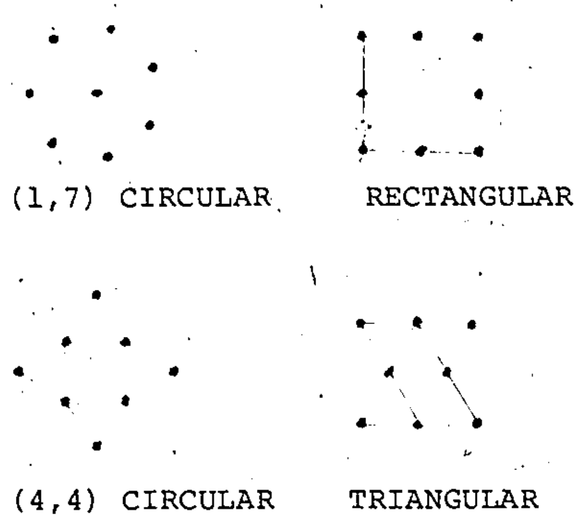


Figure 2.7(a) - Eight ary Signal Set Design

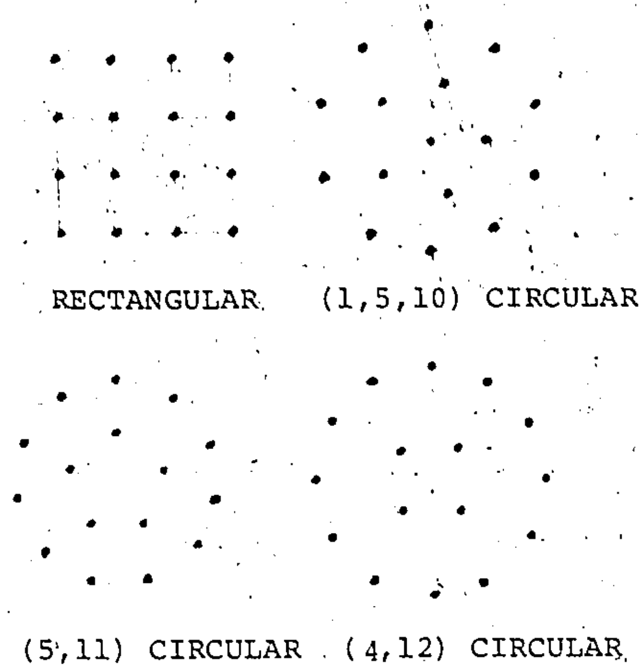


Figure 2.7(b) - Sixteen ary Signal Set Design.

set with an Es/No of 17.5 dB, followed by triangular (4, 4) and rectangular with Es/No of 17.6, 17.75, and 18.9 dB respectively. All 8-APK set configuration outperformed 8-PSK which has an Es/No of 19.5 dB.

In the case of 16-APK there are four design categories. These are rectangular, triangular, circular and hexagonal. The best P(e) performance was obtained for (1, 5, 10) signal set followed by rectangular (5, 11), triangular, (4, 12), (8, 8) and hexagonal with Es/No of 20.8, 20.9, 21, 21.5, 21.7, and 21.9 dB respectively. Again all 16-APK configurations outperformed their 16-PSK counterparts which gives a P(e) of 10^{-6} at an Es/No of approximately 26 dB.

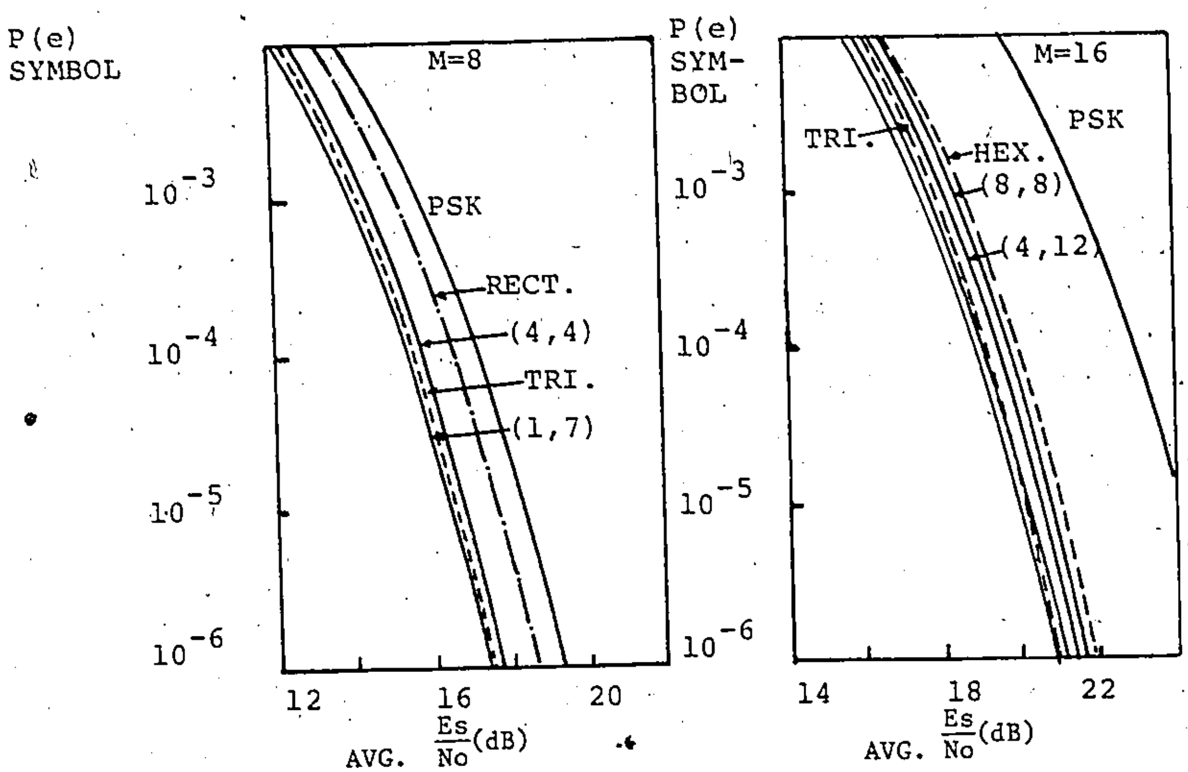


Figure 2.8 - Probability of Symbol Error as a Function of E_S/N_0 from Reference [15].

Fielding [16] has shown that the probability of error in the detection of APK for large S/N's is given by

$$P(e) = \frac{1}{M}\sqrt{\frac{1}{2\pi}}\sum_{i=1}^{M}\sum_{\substack{j=1\\j\neq i}}^{M}\frac{\exp(-|S_i - S_j|^2/4\sigma^2)}{|S_i - S_j|\sqrt{2\sigma}} \qquad (2.16)$$

where M - number of signal states

S_i - is the complex envelope of the i^{th} signal state

S_j - is the complex envelope of the j^{th} signal state

σ^2 - r.m.s. noise power.

Here the P(e) considers M(M-1) binary sets made up of all possible distinct signal pairs (S_i, S_j).

One of the major problems in APK is the distortion caused by AM-AM and AM-PM nonlinearities in a device like a TWT. This problem can be reduced by back-off from the saturation drive level of the tube resulting in a loss of transmitter power. This implies that there exist a trade-off between signal quality, hence P(e) performance, and output power.

Another method by which this nonlinearity problem may be reduced is by predistorting the transmitted signal set so that when it passes through the TWT it will become linear. However, if the distortion resulting from a high-power amplifier or a TWT nonlinearity is not corrected, it becomes responsible for additional P(e) degradation on detection in the receiver.

With 16-APK, the TWT nonlinearities are intolerable at 0 dB back-off. This is where the advantage of 16-PSK is made clear. Thomas et al. [14] have shown that the approximate 2.7 dB advantage of APK over PSK in a linear channel becomes a 3.7 dB disadvantage in a nonlinear channel. This is true for a single channel per carrier operation. In the case of multichannel operation, the performance of APK relative to PSK improves. This improvement is realized because the 16-phase PSK system requires a 4-6 dB back-off in order that intermodulation distortion be acceptable.

The transmitted signal of an APK modulator can be described as

$$S_{i_j}(t) = \begin{cases} \sqrt{\frac{2Ei}{T}}\cos\left(\omega_0 t + \frac{2\pi(j-1)}{n}\right) & 0 < t < T \\ 0 \text{ elsewhere} & \begin{matrix} i = 1, 2, \ldots, m \\ j = 1, 2, \ldots, n \end{matrix} \end{cases} \tag{2.11}$$

where $S_{i_j}(t)$ - Power in the i^{th} amplitude level and j^{th} phase position

E_i - Energy level of the (i, j) signal vector

ω_0 - angular velocity of the carrier

i, j - integers

Because of the two-dimensional nature of APK, its hardware implementation is significantly more complex than that of a comparable PSK system [17]; thus APK systems are more expensive. Additionally the hardware complexity may also affect the reliability and ease of system maintenance.

However, as spectral congestion and transmission rate requirements increase, APK becomes more attractive as the modulation scheme to alleviate these problems. This is because of the reduced SNR requirement and its improved performance over PSK in a multichannel environment.

16-ary APK has been used throughout this research with virtually no mention of sixteen-ary quadrature amplitude modulation (16-ary QAM). However, where such mention is made, particularly in the references, these terms, viz 16-APK and 16-QAM can be used interchangeably as applied to rectangular signal constellations. This is because 16-QAM is a special case of the class of APK modulation techniques where the signal set is generated using amplitude modulated signals in quadrature. Thus, the information is also contained in both the amplitude and phase of the signal. It is therefore also correct to refer to this same 16-ary signal set as 16-APK. We shall now continue our investigation on 16-ary APK.

CHAPTER III

ON THE DESIGN OF THE MODULATOR

3.1 Introduction

The objective of this chapter is to investigate two approaches to the implementation of a 16-APK modulator with one of these methods being chosen for this research. An original approach to system circuit design is applied to several circuits which are used to realize the control of the operating mode of the modulator. Implementation of these and other modem subsystems are expected to lead to the development of a quasi universal modulator switchable from BPSK to 16-APK. The usefulness of this feature will become apparent in Chapter 5 when the control by pseudo error monitor is presented.

The system designed in this research is a type one 16-ary APK system with the following parameters:

$$M = 16$$

$$m = 4$$

$$n = 4$$

Bit rate = 256 kb/s

Carrier freq. = 1 MHz

Symbol rate = 64 kbaud

A rectangular signal state space representation is used for this system as shown in Figure 3.1 [18]. The use of this

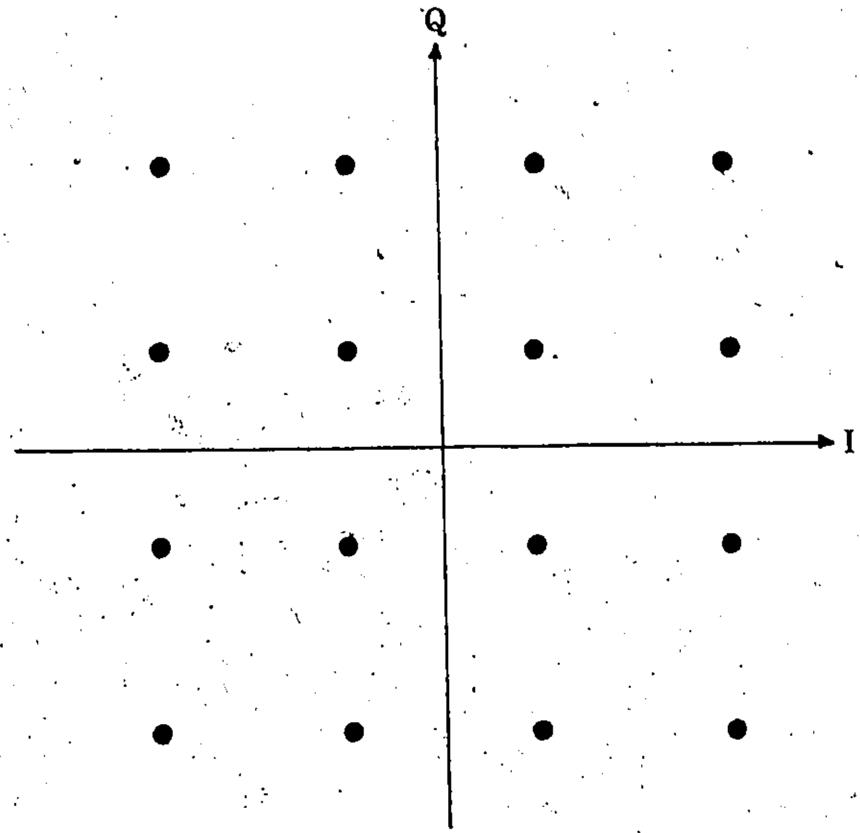


Figure 3.1 - 16-APK Rectangular Signal State Space Diagram

representation was selected because of its rectangular symmetry with respect to the I and Q axes. This choice greatly reduces the problem of hardware implementation. There are two frequently employed ways of generating a 16-state space rectangular array. The first is by splitting serial data into two parallel streams as in Figure 3.2, each of the two data streams are two-to-four-level converted and used to modulate two carriers in quadrature.

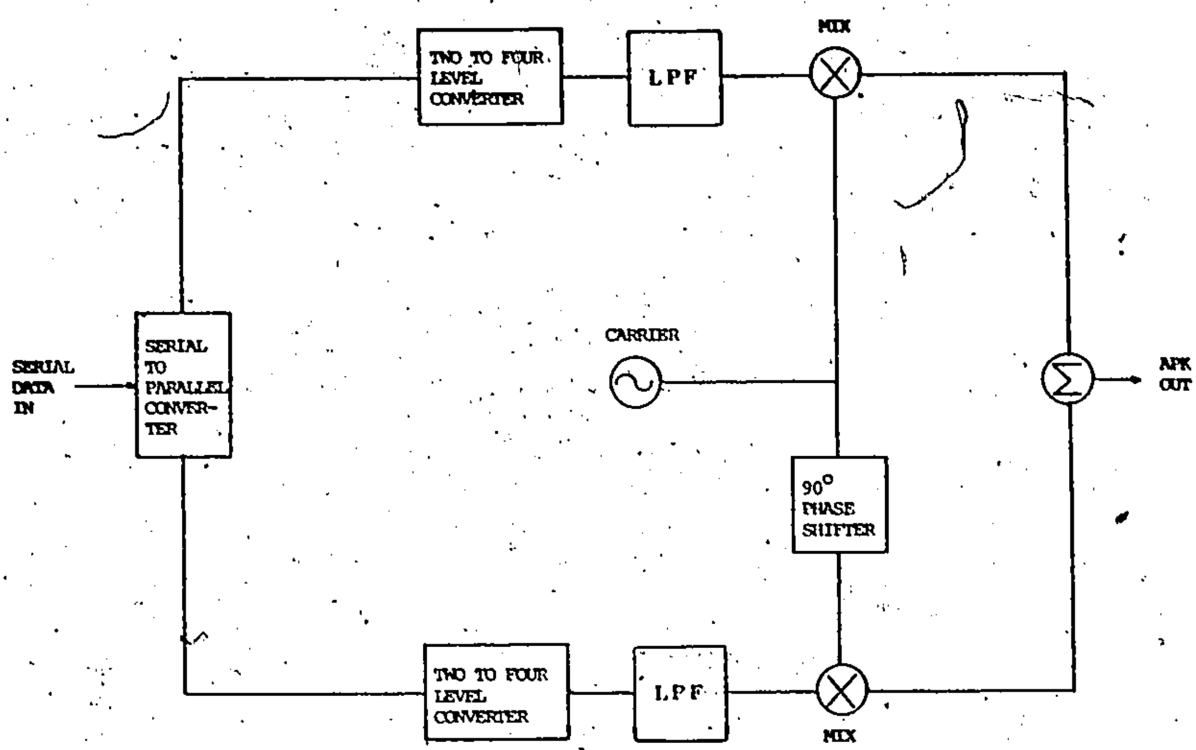


Figure 3.2 - 16-APK Modulator (2-4 Level Converter Method)

The two modulated carriers are added vectorially, band limited using a band-pass filter (BPF) or premodulation LPF, and transmitted through the channel. Figure 3.3 shows the demodulator. Here, the modulated signal is split into two parallel paths and detected using balanced modulators which are also fed with coherent carriers in quadrature. The detected data is passed through low pass filters (LPF) to remove noise and interference plus second-order and higher spectral products, four to two level converted, and parallel to serial converted to give the original data.

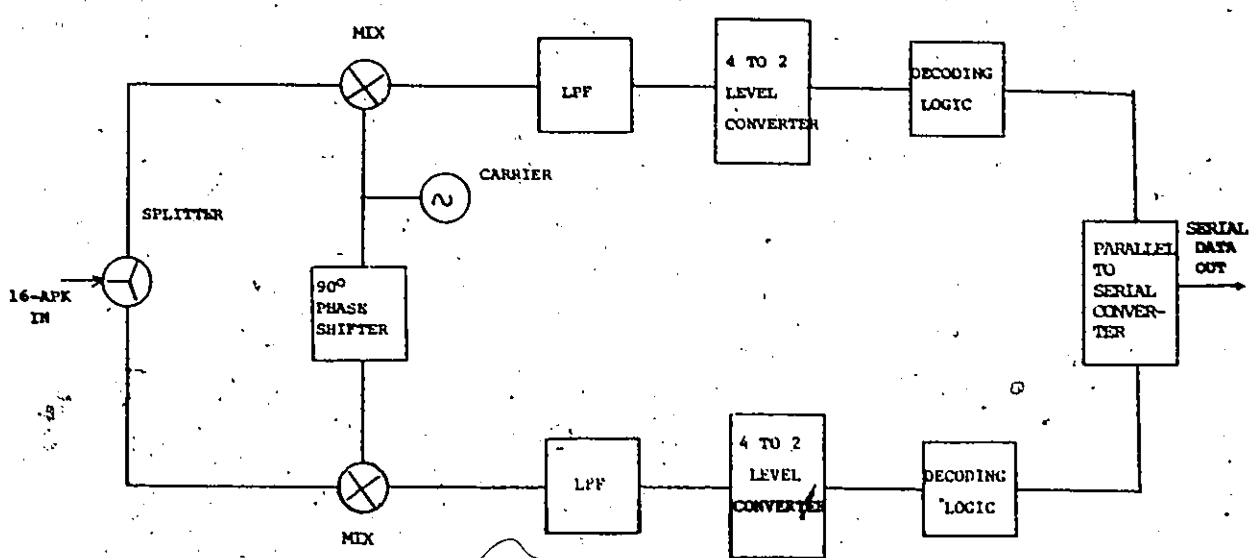


Fig. 3.3 - 16-APK Demodulator

The second method, and the one used in this research employs the technique suggested by Miyauchi et al. [19] with the addition of a carrier phase trim circuitry to improve the performance of the modulator vis-à-vis crosstalk. The main advantage in the selection of this method is that it allows for easy implementation of the switching functions which selects the operating mode (BPSK, QPSK or APK) for the modem. Additionally, this method gives the required versatility needed to study the performance of APK in a nonlinear channel (in a future research) where AM/AM and AM/PM distortions are prevalent. This method may well provide an advantage in P(e) degradation over the previously mentioned method when used over a nonlinear channel.

3.2 Functional Description

The essential parts of the 16-state APK modulator are shown in Figure 3.4. Here, QPSK modulators I and II operate in parallel with their outputs attenuated with respect to each other and then added vectorially at the secondary combiner to form the modulated signal. To simulate random NonReturn-to-Zero (NRZ) data at the modulator input, a Pseudo-Random Binary Sequence (PRBS) generator is used as the data source. This PRBS generates a repetitive 2^n-1 bit maximal length sequence where n may vary from 3 to 15 as desired [20]. Thus the sequence length can be varied in order to ensure sufficient randomness in the input data such that the transmitted spectrum is rendered continuous.

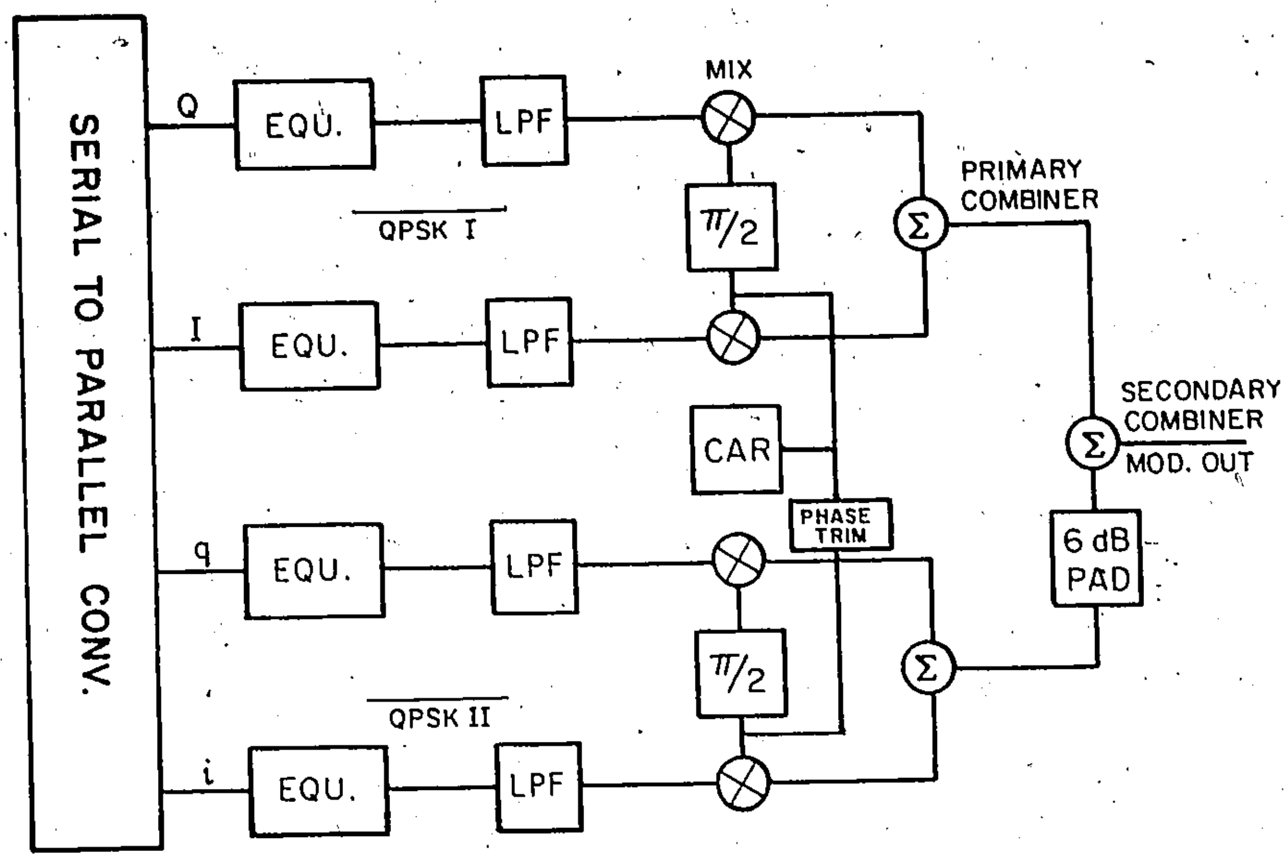


Fig. 3.4 - 16-APK Modulator (Miyauchi Method) [19]

Data from the PRBS is passed through a four bit serial to parallel converter to the mode control logic. Before this converted data is used to phase modulate the carrier, it is passed through an equalizer and low pass filter (LPF). The equalizer predistorts the data in order that phase and amplitude nonlinearities in the transmit and receive LPF's are to some extent compensated for. The LPF at the transmitter limits the bandwidth of the baseband signal thus restricting the power of the side lobes produced by the linear modulation process. Hence the 256 kb/s data is clocked in synchromism to the four channels Q, I, q, i, at a rate of 64 kbaud. Q, I, and q, i constitute the inphase and quadrature channels of two quadrature phase shift keyed (QPSK) modulators. These "I" and "Q" channels each double-sideband- suppressed-carrier (DSB-SC) modulate a carrier and its quadrature component. These modulated signals are combined to form two QPSK modulated signals. Furthermore, QPSK signal two is attenuated by 6 db with respect to QPSK signal one and combined with it to form a 16-APK signal. This 16-APK signal is then transmitted through the channel. As can be seen from Figure 3.4, the 16-APK modulator is essentially four BPSK modulators in parallel, with appropriate phase shift and attenuation between them. A detailed description of one BPSK channel will be given next. This description holds for all four BPSK channels which are combined to form the 16-APK signal. Figure 3.5 shows a block diagram of one of the four BPSK modulator channels. A description of each block is given in the following paragraphs.

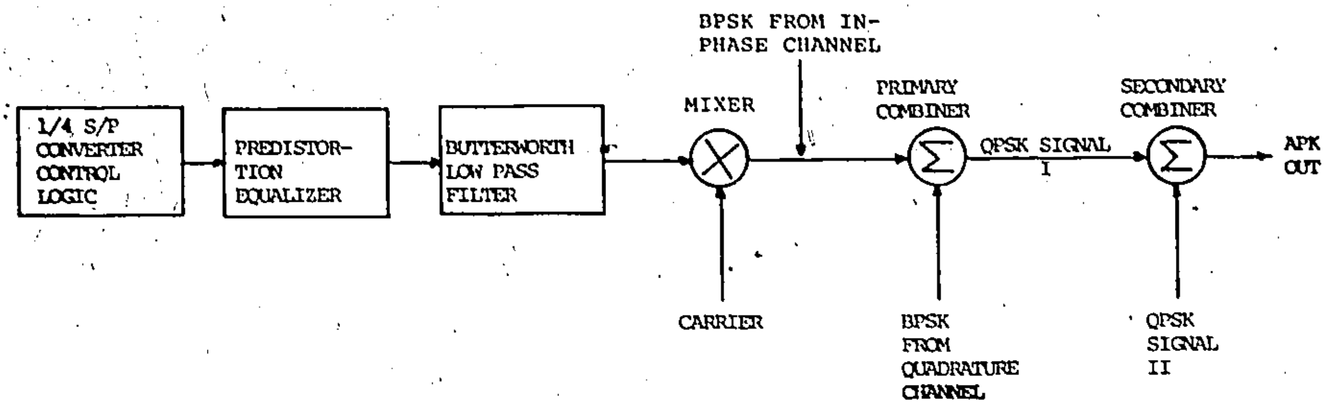


Fig. 3.5 - A Typical BPSK Modulated Channel in the 16-APK Modem

3.3 Serial to Parallel Converter and Mode Control Logic

This subsystem consists of many circuits as shown in Figures 3.6 and 3.7 of which only the serial-to-parallel converter and latch are an integral part of the modem. The remaining circuitry provides controlling functions necessary since this modem is operating in the laboratory where symbol timing and carrier recovery sub-systems are not included. However, this makes it essential to provide internally, timing and clocking pulses for both the transmitter and receiver.

Source data arrives to the modem at a bit rate of 256 kb/s when the modem is operated in the 16-APK mode. To make the modem quasi-universal (capable of performing in the BPSK and QPSK as well as APK modes), control logic is incorporated in the logic circuit design. The basic philosophy behind the functioning of the control logic circuitry is that the data source or PRBS is made a slave to the mode control logic (MCL). This ensures that the bit rate changes automatically in accordance with the modulation scheme selected thereby simplifying LPF design. Hence, for operation in the BPSK mode, the MCL forces the PRBS to operate at a bit rate of 64 kb/s and at 128 kb/s when operating in the QPSK mode.

Figure 3.6 shows a block diagram of the serial-to-parallel converter and mode control logic. This diagram shows that in addition to carrying out master control functions, this circuitry also provides the symbol rate and predistortion equalizer clocks. The symbol rate clock is used to syncronize the measuring instruments and regenerate the received data. The predistortion equalizer clock controls the predistortion filters incorporated in each channel.

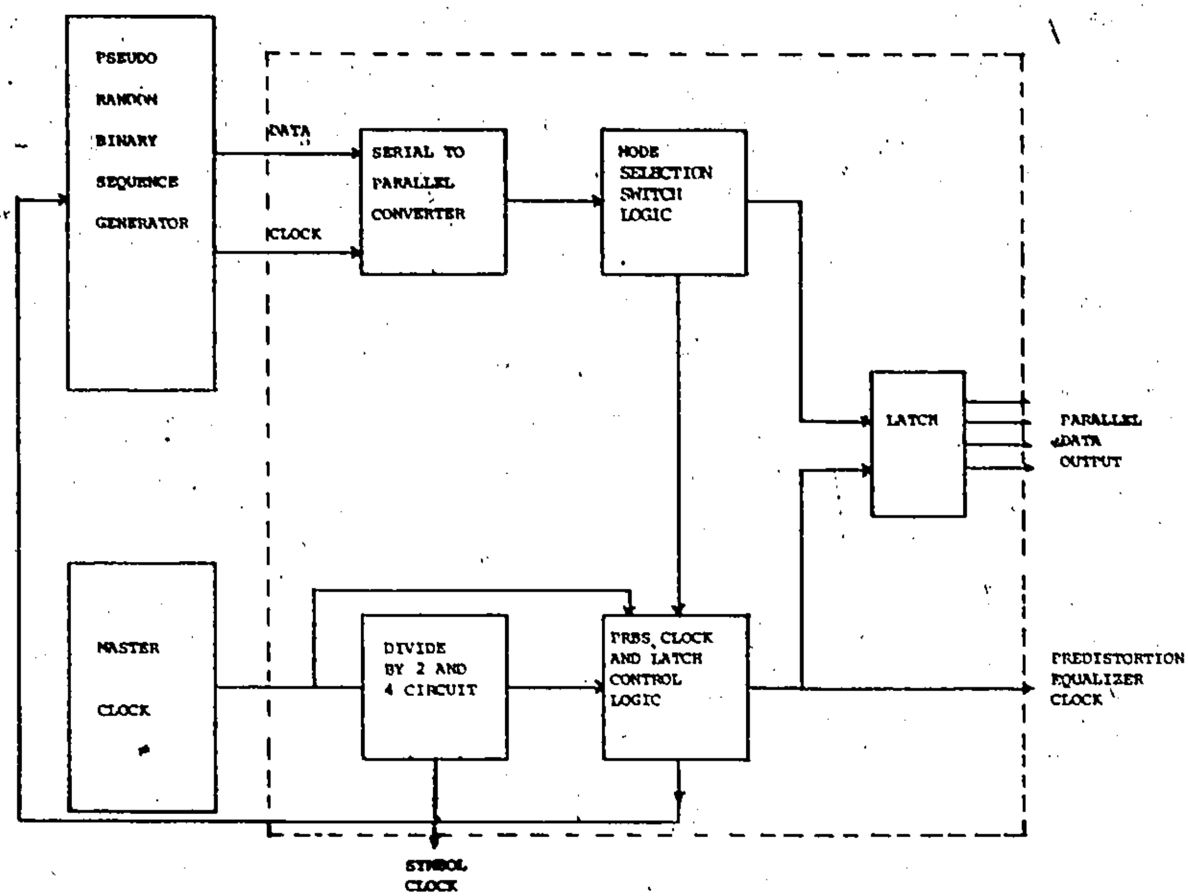


Fig. 3.6 - Serial-to-Parallel Converter of Mode Control Logic Block Diagram

Figure 3.7 shows the physical realization of the block diagram shown in Figure 3.6. The intricate details of its operation are presented in Appendix 1. In addition to this circuitry, delay controls are incorporated to compensate for

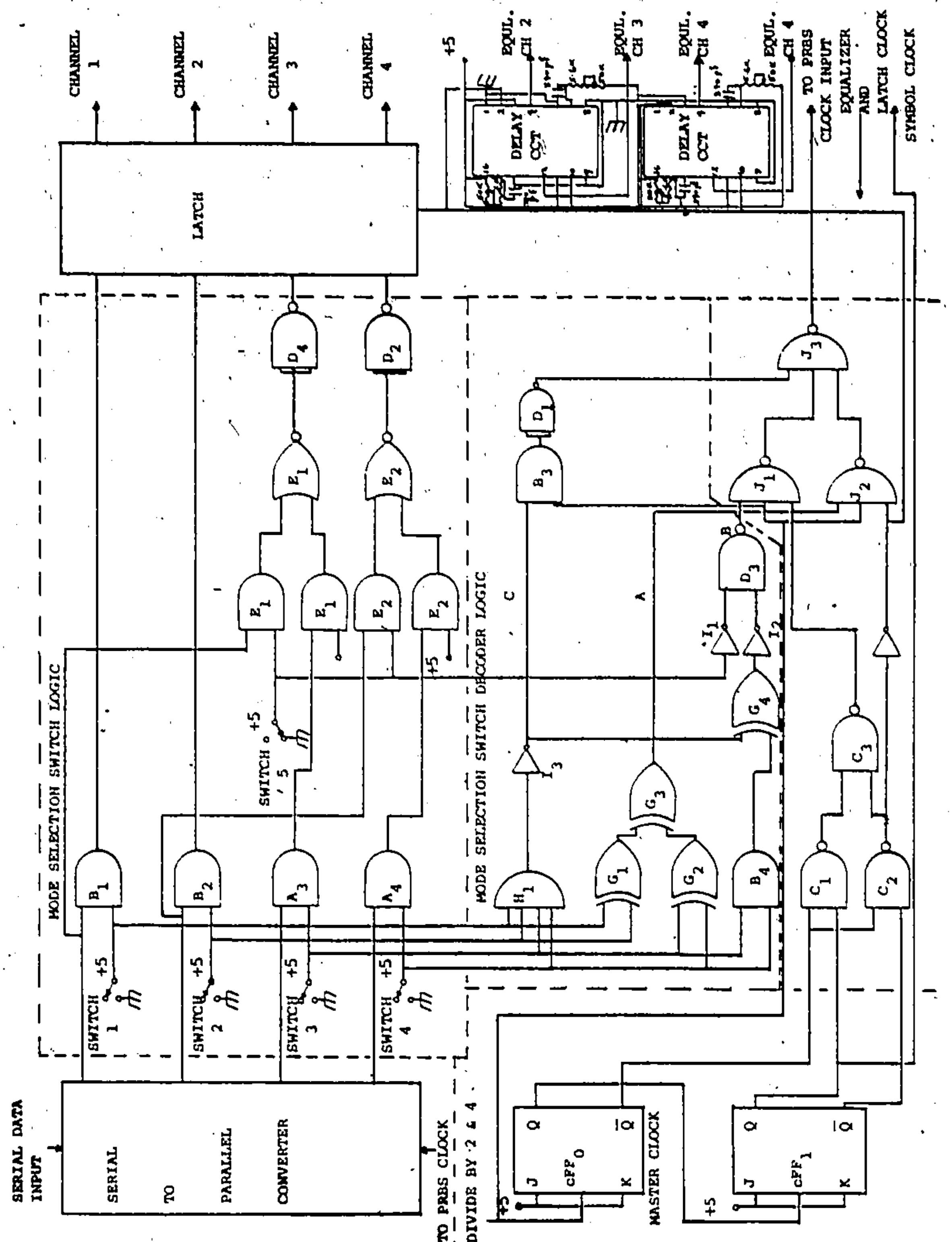


Fig. 3.7 - Serial to Parallel Converter and Mode Control Logic Circuitry

the difference in propagation delay of the signals as they pass through each of the four channels. This delay results mostly from filtering and is severe enough to cause noticeable misalignment of the separate channel signals with respect to each other at the modulator output. If unattended, this would create problems in synchronization of the transmitted and received signal making it virtually impossible to interpret correctly what data was transmitted. Thus, four delay circuits, one for each channel as shown in Figure 3.7, were necessary to alleviate this problem.

3.4 Predistortion Equalization

When data is transmitted through a channel, (here channel includes the pre-modulation and post detection LPF's) it is highly desirable that the received data be free from distortion at the sampling instant. A necessary condition for distortion free transmission is that the channel have a flat amplitude and linear phase vs. frequency response for impulse transmission and x/sinx equalization for pulse transmission as discussed in Chapter II. It is indeed unfortunate that infinite bandwidth is not available; if this were the case, rectangular pulses could be transmitted and channel equalization problems would not exist. However, in a practical system bandwidth is conserved by bandlimiting the data, that is curtailing the signal spectrum. The result of this bandlimiting is a nonlinear amplitude and/or phase response. The net effect of the transmit and receive filters nonlinearities is to generate intersymbol interference (ISI) in the received data which ultimately results in serious probability of error degradation if steps are not taken to minimize it. To keep this ISI within reasonable limits it is necessary to equalize the data channel. R.E. Kalman [21] has shown that, using tapped delay lines, it is possible to design filters that have no phase distortion at all, and have very slowly varying phase response regardless of their amplitude response. This method effectively distorts the channel thereby providing equal delay to all frequencies passed. An alternative method suggested in Bennett and Davey [3] is to predistort the data to compensate for amplitude distortion and group delay in the channel. Since the data being transmitted is in binary form, the simplest method of equalization is by predistortion using a shift register. The ease of implementation vis-à-vis analog methods also makes predistortion equalization most attractive as a means of amplitude and group delay equalization. This equalizer is used to condition the data at the transmitter in order that the data at the output of the post detection LPF is optimized with respect to ISI and noise bandwidth. In this case optimization means minimum vertical eye closure at the sampling instant which, in our case, is at the centre of the eye. Figure 3.8 shows the block diagram of the predistortion

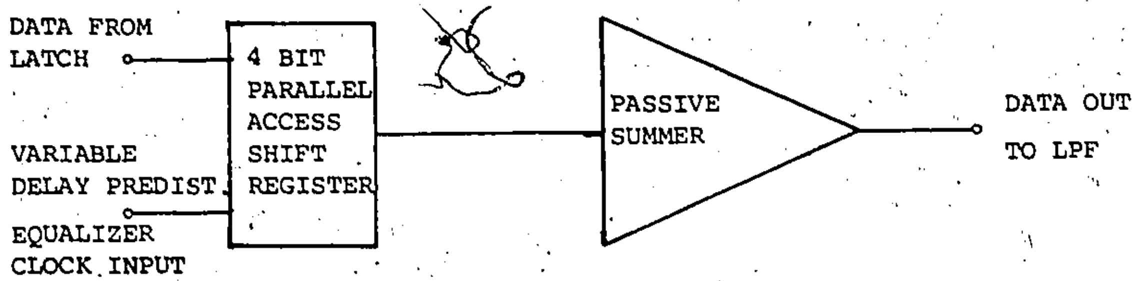


Fig. 3.8 - Block Diagram Predistortion Equalizer

equalizer. Data is fed into and clocked through the shift register in serial form. At the output of each flip-flop in the shift register, data is available at the Q and $\overline{Q}$ outputs. The complementary outputs of each flip-flop are added linearly and the weighted sum of each of the four flip-flops is taken by the summer. The bias is removed from this signal by a capacitor since the average voltage value of the data is 2.5 volts dc and should be 0 volts dc. The signal which has been conditioned for filtering is then available at the output.

The theory and operation of predistortion equalizers has been well explained in reference [22]. However, we know that if a single pulse is passed through a LPF, a sin x/x response should be obtained under ideal conditions. Since the filters used here are neither ideal nor equalized, the response shown in Figure 3.9a, which is not truly sinx/x in shape, resulted.

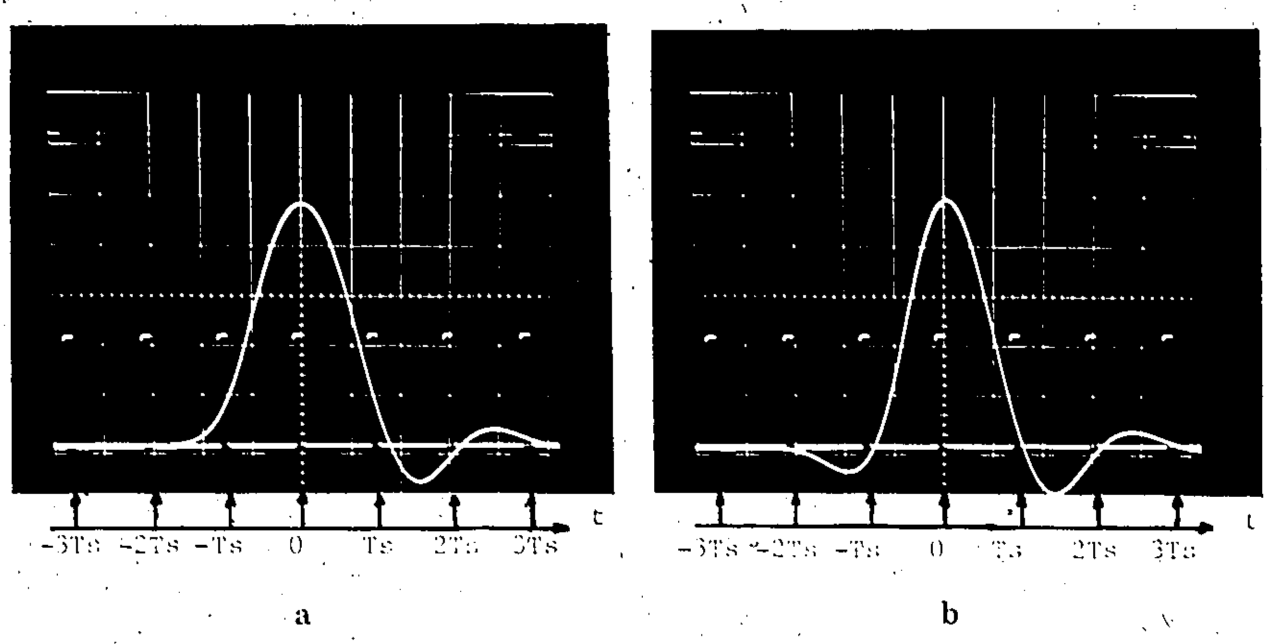


Figure 3.9 - Photograph of Measured
(a) Unequalized Receive Pulse Response
(b) Equalized Receive Pulse Response

This problem, which arises when filtering is executed without equalization is clearly seen by observing these responses at intervals $T_s = 1/f_s = 15.6\ \mu s$ where T_s is the symbol duration and f_s is the symbol rate. The duration between symbol clock pulses is equal to T_s in the figure. Table 3.1 gives a summary of the intersymbol interference at integer multiples of the sampling instant before and after equalization. These observations indicate

Table 3.1

SUMMARY OF ISI AT SAMPLING INSTANTS FROM FIGURE 3.9

Sampling instant Ts	% peak value of pulse at sampling instant nTs	
n	before equalization	after equalization
-3	-	-
-2	-	0
-1	+ 25	0
0	peak	peak
1	+ 15	0
2	-.15	0
3	-.1	0

virtually no zero crossing at the sampling instants $\pm nT_s$ where n is an interger before equalization. This represents significant ISI when the next pulse comes along since it peaks at $-T_s$. The predistortion equalization removes this ISI when the tap gain coefficients are set such that the pulse response is zero at $\pm nT_s$ as summarized in Table 3.1. This result is shown in Figure 3.9(b) where it is seen that the pulse response is zero at each sampling instant. Thus, when remnants of the previous pulse and the next pulse arrive, there will be no interference with the present pulse, that is to say, there will be virtually no ISI. This behaviour is in good agreement with theory as explained by Lucky [23]. Figure 3.10 shows the actual design of the equalizer used in this modulator. Random data from the serial-to-parallel converter and mode control logic card are fed into each of four predistortion equalized channels. This data is clocked through the shift registers at a clock rate of 64 kHz. The aggregate of the weighted sum of the output of each flip-flop is passed through a decoupling and level shifting capacitor to the channel premodulation LPF. The actual design of the predistorter simply involves cascading a number (in this case 4) D type flip flops. A weighted summing network is introduced at the output of each flip flop between the Q and $\overline{Q}$ as shown in Figure 3.10. The aggregate sum is taken by adding the output of all flip flops together through the summing network. Given the input data shown in Figure 3.11(a) to a predistorter, the output data shown in Figure 3.11(b) results when the taps (i.e., the 1 K pots) in the summing network are adjusted, as outlined in Appendix D.

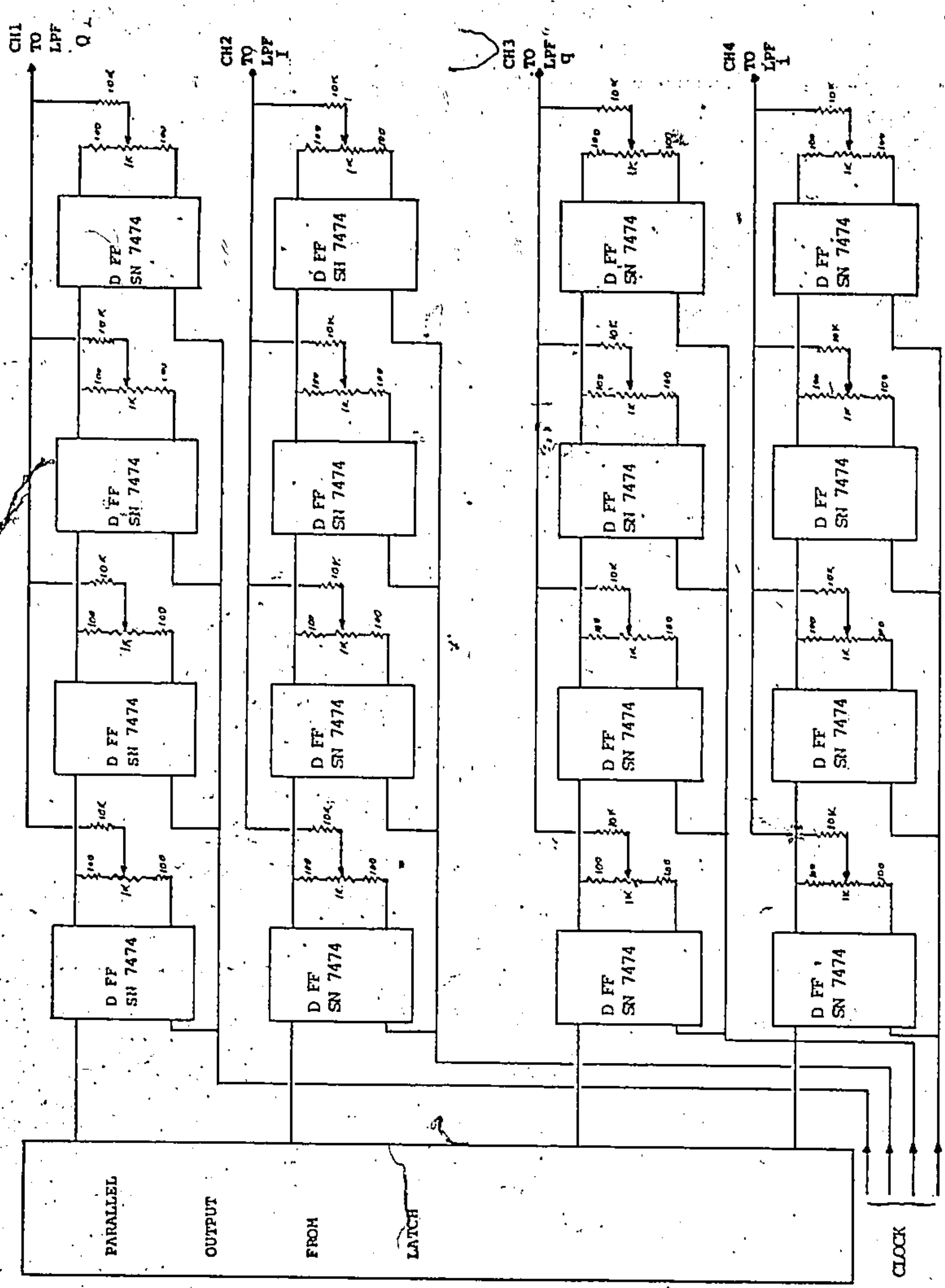
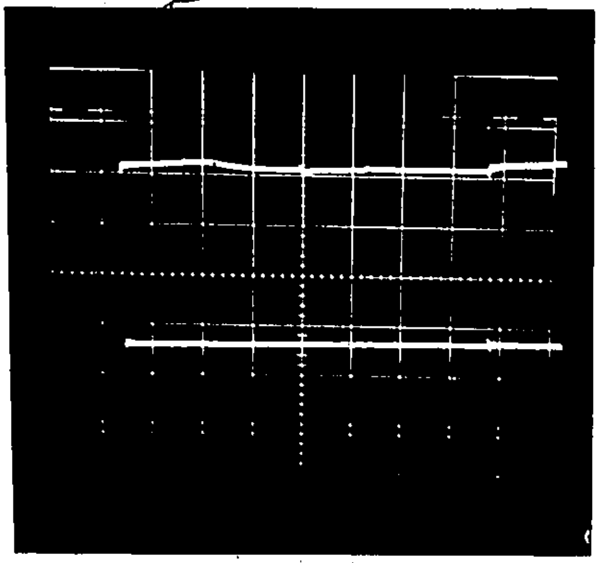
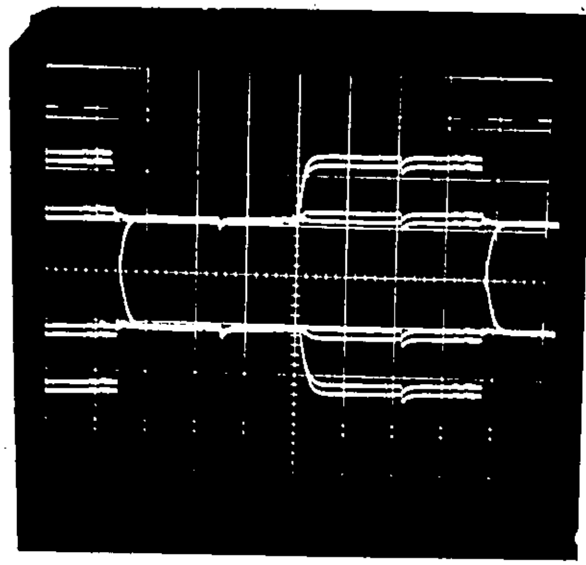


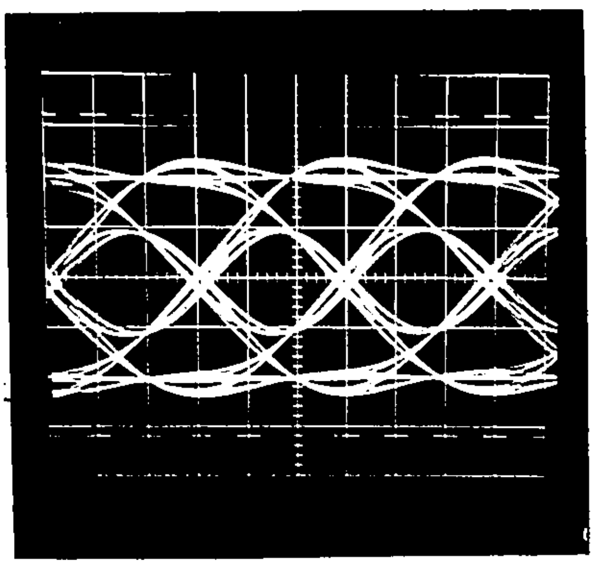
Figure 3.10 - Predistortion Equalization Circuitry



(a) VERTICAL: 1V/div
HORIZONTAL: 2μs/div

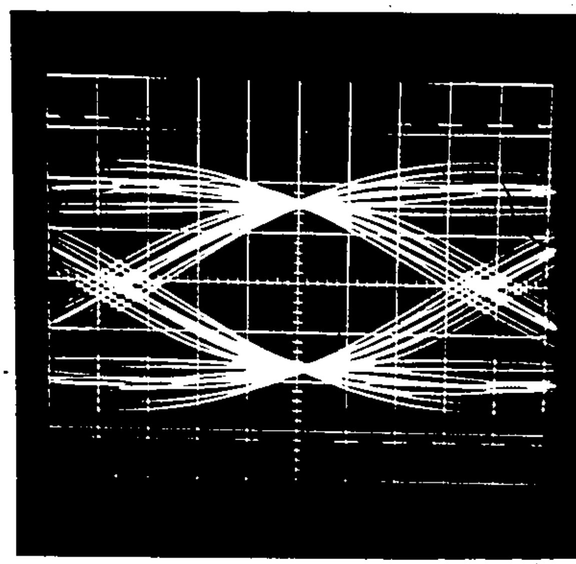


(b) VERTICAL: 1V/div
HORIZONTAL: 2μs/div



(c) VERTICAL: 20mV/div
HORIZONTAL: 5μs/div

Transmit & Receive LPF cascaded



(d) VERTICAL: 20mV/div
HORIZONTAL: 2μs/div

Tx and Rx LPF cascaded

Figure 3.11 - Photograph of Measured
(a) Undistorted Data
(b) Predistorted Data
(c) Eye Diagram Before Equalization
(d) Eye Diagram After Equalization

The photographs in Figure 3.11(a) show the undistorted infinite-bandwidth data which is fed into channel 1 of the equalizer, Figure 3.11(b) shows the predistorted data at the input to the BPSK1 channel filter, Figure 3.11(c) and 3.11(d) show the eye diagrams before and after equalization. Comparing the latter two pictures, it is seen that the vertical eye opening improves from 50% to 100%. This increase in the vertical eye opening will account for a significant improvement in the probability of error performance of the modem.

It is clear, that predistortion equalization improves the performance of the modem as seen from the eye diagrams. The amount of improvement in the $P_{(e)}$ performance will be shown in Chapter 5. Further discussion of the equalizer tap setting is presented in Appendix D.

3.5 Premodulation Data Conditioning and Filtering

The operation of this modem in either of the BPSK, QPSK or APK modes renders premodulation low-pass filtering (LPF) more suitable since only one set of filters and equalizers need to be designed to handle data at a rate of 64 kbaud. If post modulation band-pass filtering (BPF) were used, additional problems would arise from the difficulty of meeting the requirements for BPF symmetry. This problem would contribute a further degradation in the overall system P(e) performance. Since premodulation and post-detection

LPF's are equivalent to post-modulation and pre-detection BPF's [1] as explained in Chapter II, the former set of filters have been employed.

In this work, the filters have not been designed with x/sinx amplitude shaping and raised-cosine roll-off since predistortion equalization has been employed. Thus, the problems which result from not adhering to these two requirements have been compensated for with predistortion equalization as discussed in Section 3.4. The filters used here are modified Butterworth filters of fifth order. For transmission of 256 kb/s of information in the APK mode, a theoretical spectral efficiency of 4 b/s/Hz is expected since this is a 16-state system. Thus for APK, QPSK and BPSK which are 16, 4, and 2 state systems a theoretical spectral efficiency of 4, 2, 1 b/s/Hz is realized respectively. There are, therefore, 4, 2, and 1 bits in symbol transmitted at baseband. This means that 256, 128 and 64 kb/s of information can be transmitted at a rate of 64 kSymbols/s for the APK, QPSK and BPSK modes respectively. Nyquist's minimum bandwidth filtering allows for a transmission of 64 kSymbols of information in 32 kHz of baseband bandwidth. The transmit modified Butterworth LPF's are designed to be 6 dB down at 32 kHz. The objective here is to design the Butterworth LPF in conjunction with premodulation equalization such that the x/sinx and raised-cosine channel is approached at the

Nyquist's cut-off frequency. Before explaining the actual filter design, we shall trace the signal to the input of the LPF.

Figure 3.12 shows the data conditioner and LPF. The predistorted data is conditioned for filtering and mixing by the conditioning circuit which consists of a capacitive buffer attenuator at the input along with a buffer driver at

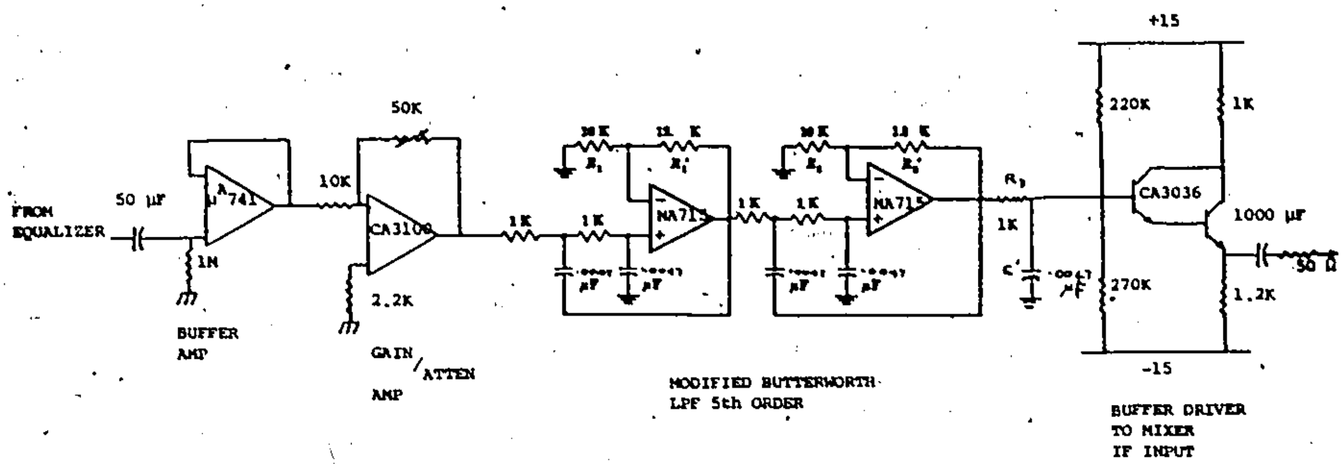


Figure 3.12 - Data Conditioning and Low-Pass Filter

the output of the LPF. The capacitor level shifts the signal so that its average value at the input of the buffer attenuator is zero. It also provides D.C. isolation. The buffer isolates the capacitor from the attenuator amplifies which controls the gain of the filter, thus controling the level of the band limited data at the signal input of the mixers. The buffer driver provides the necessary isolation of the filter from the mixer and also the required signal power to drive the mixers. One of its most important functions is to provide an impedance matching of 50 Ω to the mixer intermediate frequency (IF) ports. A note of worth is that the D.C. blocking capacitor at the buffer output [24] must be large enough for a maximal length sequence to pass through it with little low frequency distortion. That is to say, the frequency f' of a $2^{15}-1$ maximal length sequence at 64 kbaud is

$$f' = \frac{1}{(2^n-1).\text{symbol duration}} = \frac{1}{(2^{15}-1)64\text{X}10^3} = 2\text{Hz} \qquad (3.1)$$

Thus the capacitor must pass a 2Hz signal free from distortion when terminated in a 50 Ω impedance. The required value of capacitance c is given by

$$c = \frac{1}{2\pi Rf} = \frac{1}{2\pi \text{X}50\text{X}2} = 1500\,\mu\text{F} \qquad (3.2)$$

Using a capacitor of value 1000 μF yields a 3dB attenuation at 3Hz. This means that there is virtually no low frequency distortion to the signal given the above sequence length and symbol rate. If this rule is not adhered to, degradation of the eye diagram results which contributes to a reduced P(e) performance [2]. We have traced the signal to the input of the LPF and discussed the interface to the mixer and LPF i.e. the buffer drive. We now discuss in detail the design of the LPF.

3.6 Low-Pass Filter Design

The computer was used to analyze the amplitude and phase response of the filter before it was implemented [25]. The application of this program, Electronic Circuit Analysis Program (ECAP) is outlined in Appendix II. The magnitude and phase responses obtained from the analysis are tabulated in Tables 3.2 and 3.3 respectively.

Table 3.2

ECAP MAGNITUDE RESPONSE

Frequency (Hz)	Gain (db)
10	7.9
31.6	7.9
100	7.9
316	7.9
1K	7.9
3.16K	7.9
10K	7.7
17.7K	6.75
31.6K	3.1
32K	2.9
56K	-15.9
100K	-40

Table 3.3

ECAP PHASE RESPONSE

Frequency Hz	Phase (degrees)
10	- .06
31.6	- .19
100	- .62
316	- 1.9
1K	- 6.2
3.16K	-19.4
10K	-61.7
17.7K	- 111
31.6K	- 213
32K	- 315
56K	- 324
100K	- 340

The Bode magnitude and phase responses of the final filter are plotted in Figure 3.13. This figure shows that the filters have significant group delay at the band edge as

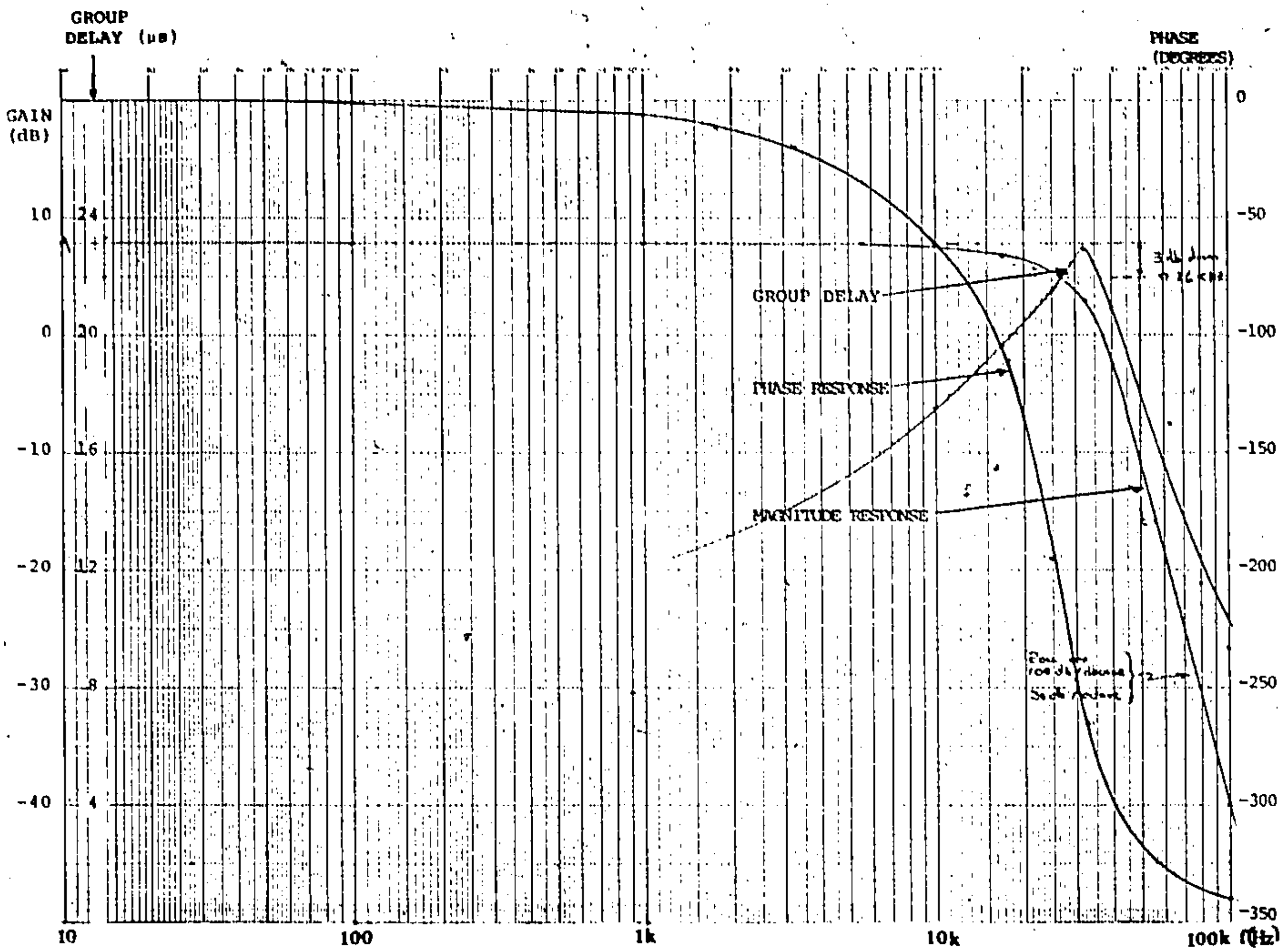


Fig. 3.13 - Bode Magnitude Phase Response (E.C.A.P. Analysis) and Group Delay Measurement

can be seen from the figure (remembering that group delay is given by do/df). The amplitude response is flat, 6 dB down at 32 kHz and rolls off at 30 dB per octave. The attenuation for 30% excess Nyquist ($\alpha = 0.3$), which is at 41.7 kHz, is approximately 18 dB. The problems with amplitude and phase response have been adequately compensated for with predistortion as discussed earlier. The above computer evaluation shows that this filter will perform adequately as a first approximation. The final realization of this filter is shown in Figure 3.15. The following outlines the filter design procedure.

The generalized response of a Butterworth LPS is given by [26].

$$A_v(s) = \frac{Av_0}{B_n(s)} \tag{3.3}$$

where

$Av(s)$ is the magnitude response of the circuit.

Av_0 is the response gain at DC.

$B_n(s)$ is the Butterworth polynomial.

By modifying the response of an operational amplifier in accordance with equation (3.3), it is possible to obtain a low pass-filter of order n. For the second-order case where n=2, (3.3) takes the form given in equation (3.4) below.

$$Av(s) = \frac{Av_0}{(RC)^2 s^2 + 2k(RC)s + 1} \tag{3.4}$$

where

$RC = 1/\omega_0$.

k - damping factor.

ω_0 - angular break velocity.

The denominator of (3.4) is the polynomial of the generalized second order system with ω_0 replaced by 1/RC.

Considering the first stage of the circuit Figure 3.14, and applying ideal op-amp theory, it is known that the gain Av_0 is given by

$$Av_0 = 1 + R'/R_1$$

If the values $Z_1=Z_2=R$ and $Z_3=Z_4=C$ in Fig. 3.14 then it can be shown after some manipulation that

$$A_v(s) = Av_0 \frac{1}{(RC)^2s^2 + (3-Av_0)RCs + 1} \tag{3.5}$$

Comparing (3.4) and (3.5) we see that

$$2k = 3 - Av_0 \quad \text{i.e. } Av_0 = 3 - 2k \tag{3.6}$$

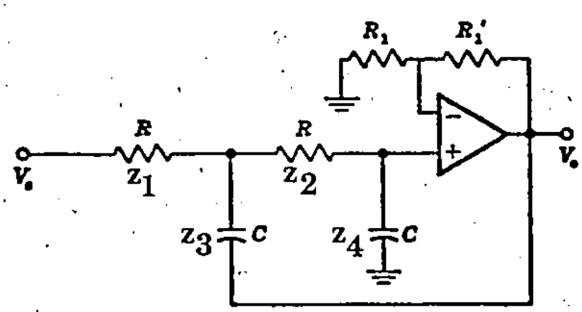


Fig. 3.14 - Second Order Low-Pass Filter.

By cascading two second order low-pass filters using identical R's and C's and adjusting the gain Av_0 such that the coefficients of the Butterworth polynomial are satisfied, we can obtain a 4th-order Butterworth filter. For a 4th-order filter, the Butterworth polynomial [26] is

$$B_4(s) = \underbrace{(s^2 + 0.765s + 1)}_{\text{first stage polynomial}}\underbrace{(s^2 + 1.8488 + 1)}_{\text{second stage polynomial}} \tag{3.7}$$

thus it follows that we need two stages of gain. Comparing (3.7) with (3.4) we see that 2k=0.765 and 1.8488 for the first and second stage polynominals. Using equation (3.6), the gain of the first stage is $Av_{01} = 3 - 0.765 = 2.235$ and the stage $Av_{02} = 3 - 1.848 = 1.152$. Also, since $Av_{01} = 1 + R'/R1$, we have for the first stage $R_1' = 12k$ and $R_1 = 10k\Omega$ for the second stage $R_2 = 1.5k\,\Omega$ and $R_2 = 10k\,\Omega$.

For the required filter, $f_0 = 32kHz$.

$$RC = \frac{1}{2\ x32x10^3} \qquad \text{let } R = 1k\Omega\text{, then} \tag{3.8}$$

$C = 4.7nF$

An additional pole was inserted at 32kHz to convert this 4th-order Butterworth filter into a modified 5th-order filter and so improve its attenuation properties. R_3 and C' modify the Butterworth filter such that a roll at 30 dB per octave and an attenuation 6 dB at the Nyquist frequency is obtained. This implies improved spectral efficiency. The final circuit is shown in Figure 3.15. The magnitude and phase response as obtained from laboratory measurements for this filter conforms with the results of ECAP Analysis which is shown in Appendix II. Bandlimiting the data by passing it through

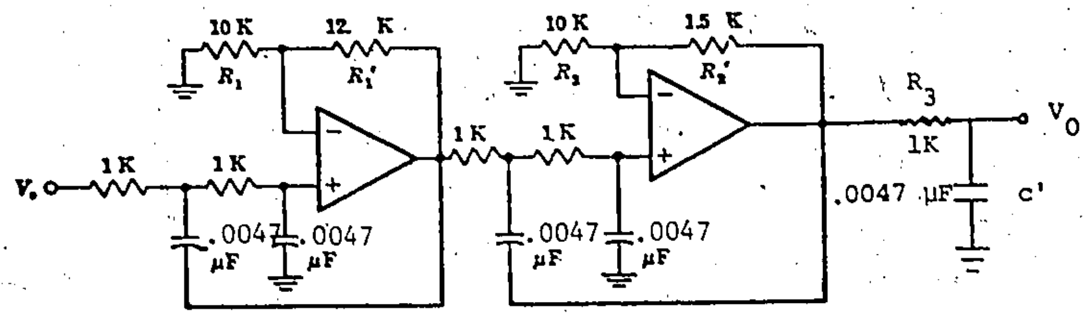
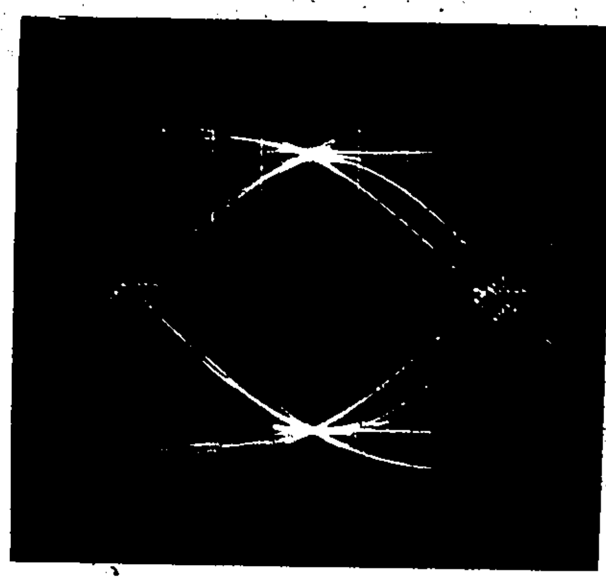


Fig. 3.15 - Modified 5th Order Low Pass Butterworth Filter f_0=32KHz.

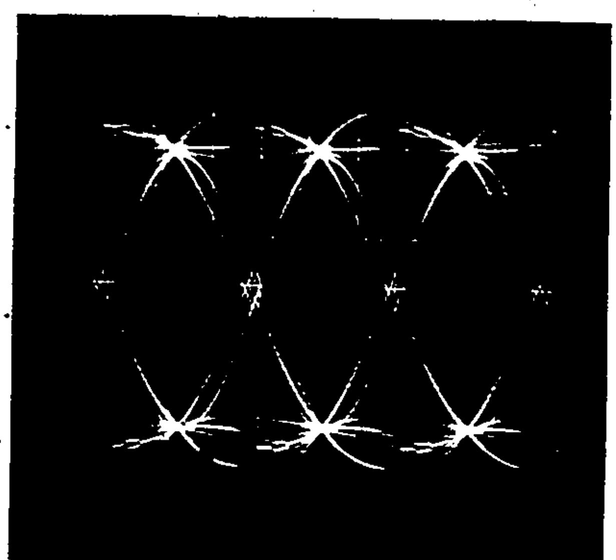
this modified Butterworth LPF resulted in the eye diagrams shown. These eye diagrams were taken just before the mixer at the IF port.



Vertical: 200mV/div

Horizontal: 2 µs/div

Fig. 3.16a Measured Eye of the filtered 64 kbaud random NRZ Data Over 1 Symbol.



Vertical: 200mV/div

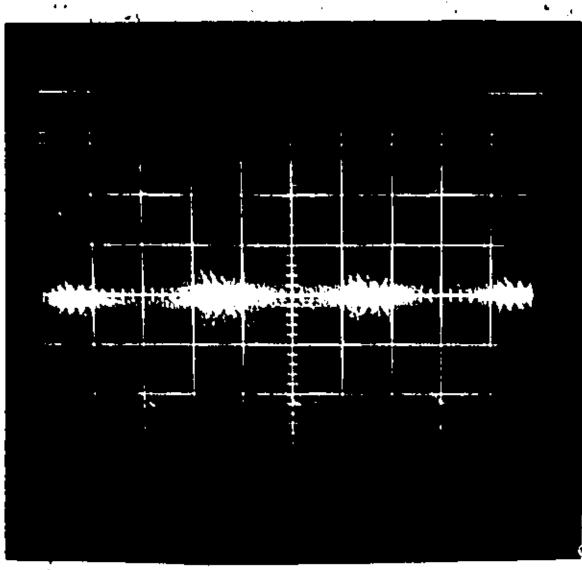
Horizontal: 5 µs/div

Fig. 3.16b Measured Eye of the filtered 64 kbaud random NRZ Displayed Over Several Symbols.

From Figure 3.16a and 3.16b, it is seen that the eye is approximately 100% open. However, after demodulation, it may be necessary to adjust this transmit eye such that the received eye diagram as measured just before the threshold comparators is maximally open. This may be necessary because of additional group delay introduced by the receive filters. The adjustments are accomplished by changing the tap position on the predistortion equalizer. These bandlimiting filters are responsible for spectral shaping and their attenuation responses are directly responsible for the spectral efficiency of the modem.

3.7 Base Band Transformation to an Intermediate Frequency

The band limited 64 kbaud data is now passed on to the intermediate frequency (IF) port of a double sideband-suppressed-carrier (DSB-SC) balanced modulator. The carrier at a frequency of 1 MHz is fed into the local oscillator port and is modulated in accordance with the data at the IF port. The modulated BPSK output is obtained at the Radio Frequency (RF) port of the balanced modulator. This is shown in Figure 3.17 and the associated circuitry in Figure 3.18.



Vertical: 200mV/div

Horizontal: 5 µs/div

Figure 3.17 - Modulated BPSK Output Channel

Figure 3.17 is obtained on the oscilloscope by feeding the modulated signal to scope input while triggering the scope from the symbol clock available at a demodulator output

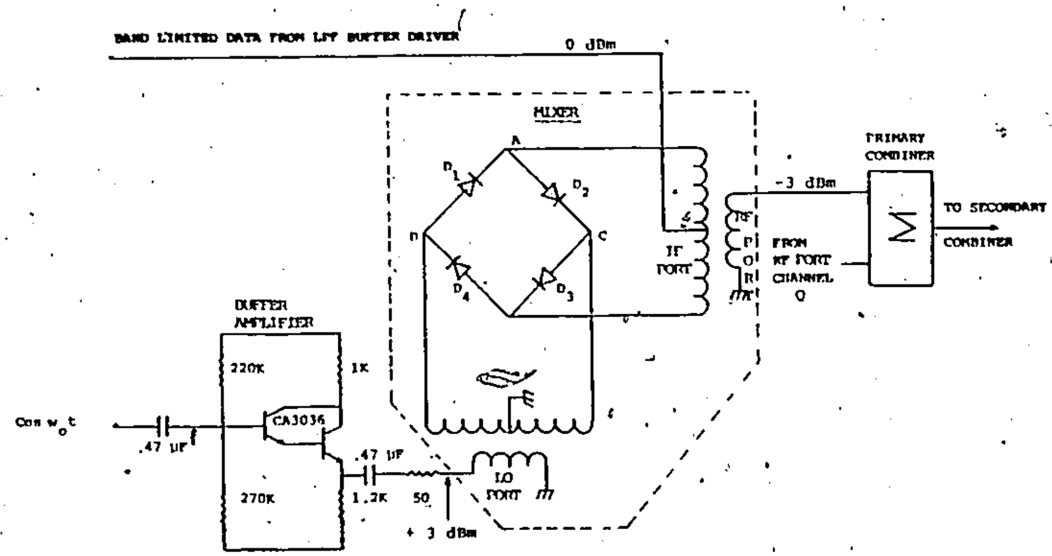


Fig. 3.18 - Double-Sideband-Suppressed Carrier Balance Modulator with LO Buffer.

port. The modulator used here was chosen to give the best performance with respect to isolation between Local Oscillator (LO), Intermediate Frequency (IF) and Radio Frequency (RF), linearity, conversion loss, and conversion compression at a LO drive frequency of 1 MHz. Elaborating, isolation is a measure of the circuit balance within the mixers, i.e. how well the diodes and transformers are matched. The higher the isolation, the smaller the amount of "leakage" or feedthrough between mixer ports. Maximizing the isolation enables less distortion in the RF output. The isolation of the mixers selected is in excess of 55 dB between ports. High isolation between mixer ports is also important because it improves the performance of the modulator by reducing the I channel-to-Q channel crosstalk. By the process of modulation, the signal on the IF port is translated to a higher center frequency. This process inherently introduces distortion because of the nonlinearity of the diodes. One measure of the degree of nonlinearity is the two tone third order intermodulation distortion [27]. For further details on mixing refer to Appendix C.

We have completed the description of the design and implementation of one BPSK channel. The remaining three parallel BPSK channels are designed in the same manner. Figure 3.19 shows the configuration used in combining the four BPSK channels to form two QPSK and one APK channel. As can be observed from this figure, data from the I channel

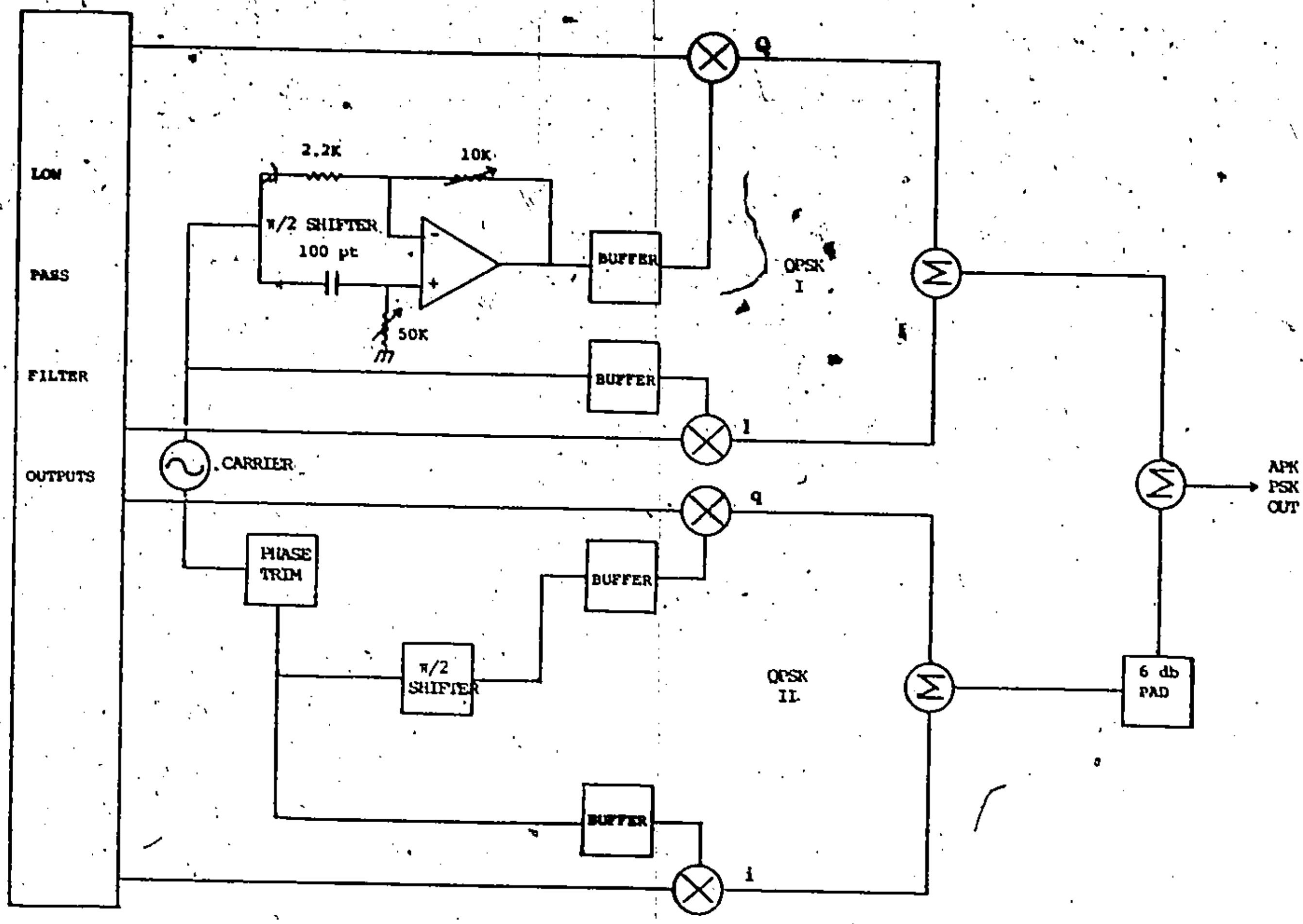


Fig. 3.19 - Final Configuration for APK Generation

enters the IF port of the mixer, the carrier after passing though a buffer amplifier which provides the necessary current drive and impedance matching enters the LO port. The modulated RF output is sent to the primary combiner where it is passed directly to the secondary combiner if BPSK 1 is selected. If QPSK I or APK was selected, the I channel output is combined with data from the Q channel which modulates a carrier phase shifted by ninety degrees with respect to the I channel. This carrier is also passed through a buffer amplifier for the same reasons as stated above. Similar circuitry exist in the QPSK II modulator. The modulated signal from QPSK 1 is sent to the secondary combiner where it is vectorially added to the output of QPSK II which has been attenuated by 6 dB. This results in a modem 16-state signal state space diagram shown in Figure 3.20.

The resulting spectrum of this bandlimited modulation process is presented in Chapter 5 where the evaluation of the modem performance is introduced.

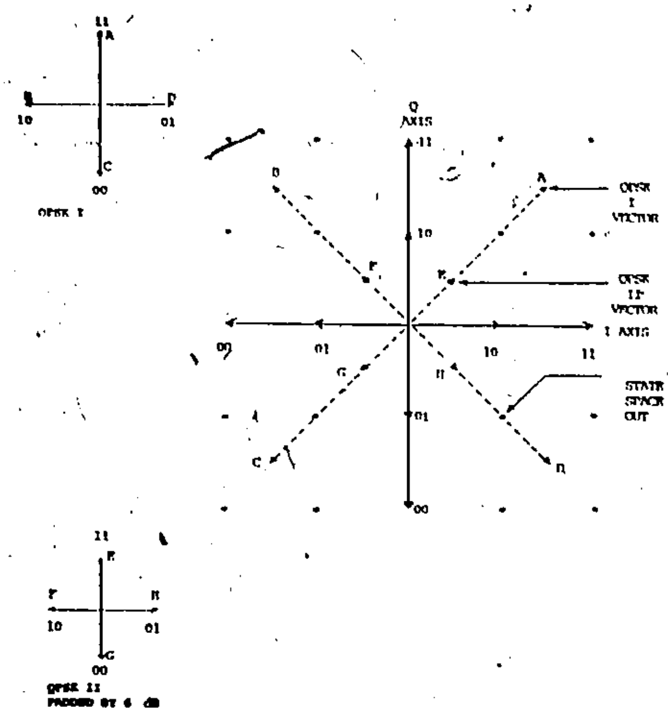


Figure 3.20 - (a) Vector Diagram Output QPSK I
(b) Vector Diagram Output QPSK II
(c) 16-APK State Constellation Diagram

3.8 A Discussion of the Sixteen-State Constellation Diagram

The above figure shows the 16-state signal constellation diagram for the modem. This is generated by vectorially adding the four resulting vectors E, F, G, H, of a QPSK modulator output to each of four resultant vectors A, B, C, D, (whose amplitude are 6 dB greater than EFGH) of a second modulator. By adding any two vectors, one from each modulator output, a resultant point signified by a dot in the state space results. Each dot represents four binary digits (bits of information) obtained from the two QPSK modulators in the order Q , I, q, i, where Q, I, represents bits from the quadratur and inphase channels of the high level modulator, similarly q, i represents bits from the QPSK modulator which is 6 dB lower in level. The binary representation of each dot is shown at their respective positions in Table 3.4. When all combinations of mutually exclusive QPSK modulator vectors from the two modulators have been taken, the signal state space diagram in Figure 3.20 results. It should be now apparent that the function of the modulator is to produce a signal which has a state constellation as shown above. From this figure, projections are made onto the quadrature axis for the bits Q, q and four levels each of which represent two bits results. The corresponding levels and bits for each of these projections are also given in Table 3.4 under the column Q axis (level, bit). Doing a similar projection of onto the I axis of bits I, i results in four similar levels with similar binary representations. This is shown in the row designated I axis (level, bits) in Table 3.4.

Table 3.4

BINARY REPRESENTATION OF CONSTELLATION DIAGRAM WITH I AND Q LEVEL/BIT INTERPRETATION SHOWN

Q Axis Level	Q Axis Bits	Q I	q i	Q I	q i	Q I	q i	Q I	q i
4	11	1 0	1 0	1 0	1 1	1 1	1 0	1 1	1 1
3	10	1 0	0 0	1 0	0 1	1 1	0 0	1 1	0 1
2	01	0 0	1 0	0 0	1 1	0 1	1 0	0 1	1 1
1	00	0 0	0 0	0 0	0 1	0 1	0 0	0 1	0 1
I	Bits	0	0	0	1	1	0	1	1
Axis	Level	1		2		3		4	

The demodulator demodulates the incoming signal along the I and Q axis, thus generating a four level baseband signal which signifies the binary representation given in the table above at each level. This is true for both the I and Q channels of the demodulator. Further processing yields the transmitted data. A signal state space diagram as measured at the input to the threshold detectors is shown in Figure 3.21.

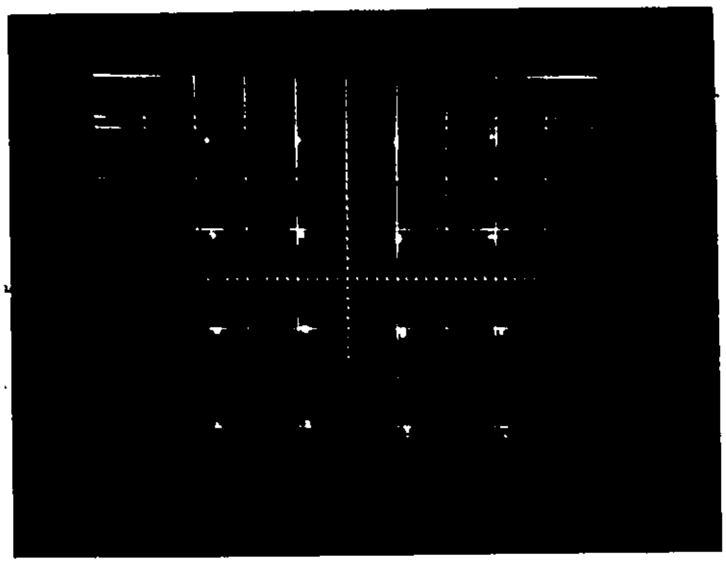


Figure 3.21 - Measured Signal State Space Diagram

This signal state space diagram is obtained by taking the signal from the I and Q channels of the demodulator after filtering, using the I signal to diflect the x plates and the Q signal to deflect the y plates. The amount of dispersion of the dots in the state space is an indication of the amount of ISI present [28].

CHAPTER IV

ON THE DESIGN OF THE DEMODULATOR

4.1 Introduction

The signal originating from the data source is modulated and transmitted through the channel where it is exposed to the AWGN, adjacent and cochannel interference. These corruptions to the transmitted signal are a major contribution to the degradation of system performance. This impure signal arrives at the demodulator input in a form which is conducive to demodulation by one of two methods namely, the remodulation-substraction or the four-to-two level slicing method. In the following, we first compare the two methods in order to enable us to make a decision as to which approach to follow. Figure 4.1 show the block diagram of the remodulation-subtraction demodulator [29].

The incoming 16-state APK signal from the channel passes through a QPSK demodulator and the digital baseband signals corresponding to the I, Q channels of the modulator are generated at ports 11 and 12. These baseband signals are used to remodulate a QPSK modulator whose output passes through a subtraction circuit where it is subtracted from the original incoming signal. The resultant signal is passed through another QPSK demodulator which extracts the baseband data corresponding to the i, q channels of the modulator. These appear at ports 13 and 14. The data at ports 11, 12,

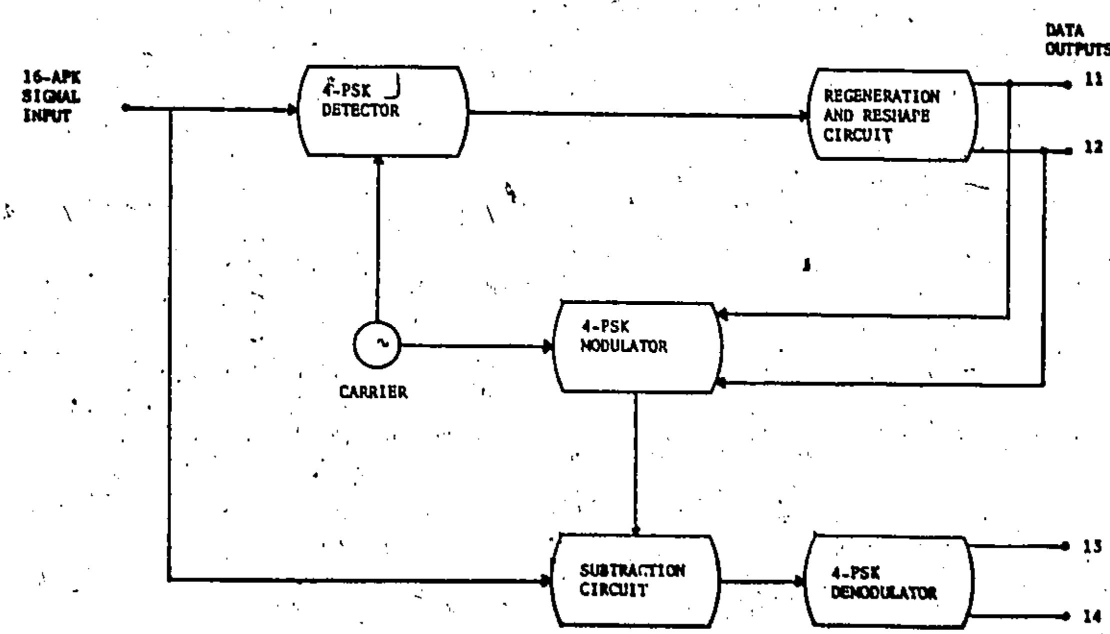


Figure 4.1 - 16-APK Remodulation-subtraction Demodulator [29]

13 and 14 are passed through a parallel-to-serial converter in order to obtain the original data. In theory this method works well, but there are some severe practical problems with it at the frequency of operation used in this work. Firstly there is a significant delay between the incoming signal and the remodulated signal at the input to this subtraction circuit. Exact compensation for this analog delay is difficult. Secondly, the error performance of this method would appear to be suboptimal because any errors at ports 11 and 12 would be transferred to ports 13 and 14 through the subtraction circuit resulting in overall system degradation. Thirdly, it would be difficult to adjust the amplitude and

phase characteristics of the two signals being subtracted such that a high fidelity signal results. Finally, because of the circuit complexity, and the required timing precision, implementation would be rather difficult. For these reasons, this method of demodulation was disqualified. The four level-to-two level slicing method to be described next was adopted.

4.2 A Macro View of the Demodulator

The component vectors comprising the signal state space diagram of Figure 3.21 are shown in Figure 4.2.

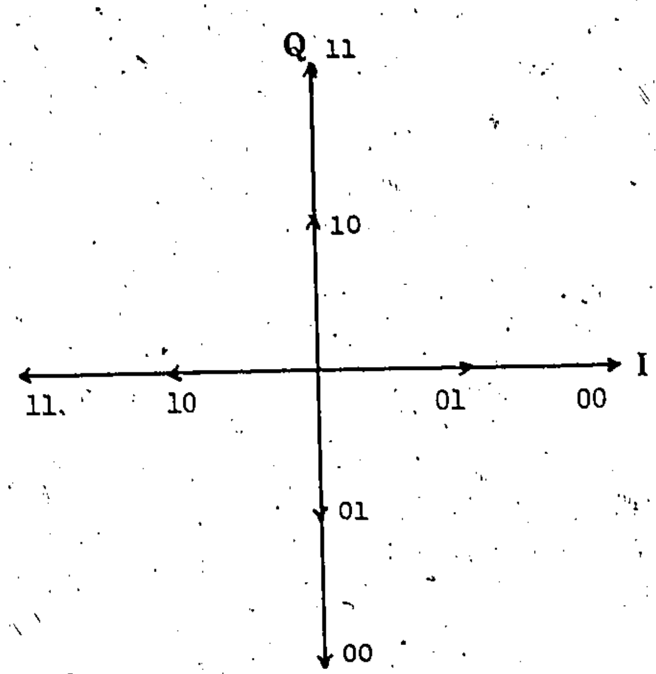


Figure 4.2 - 16-APK Signal State Space Component Vector Diagram.

The horizontal and vertical axes represent the I and Q channels respectively in the demodulator. As can be seen from the figure there are four levels on each axis, thus after detection a four-level eye diagram will exist. Decoding of the information in the eye diagram will yield the transmitted information. This is the basic philosophy.

A block diagram of the demodulator is shown in Figure 4.3.

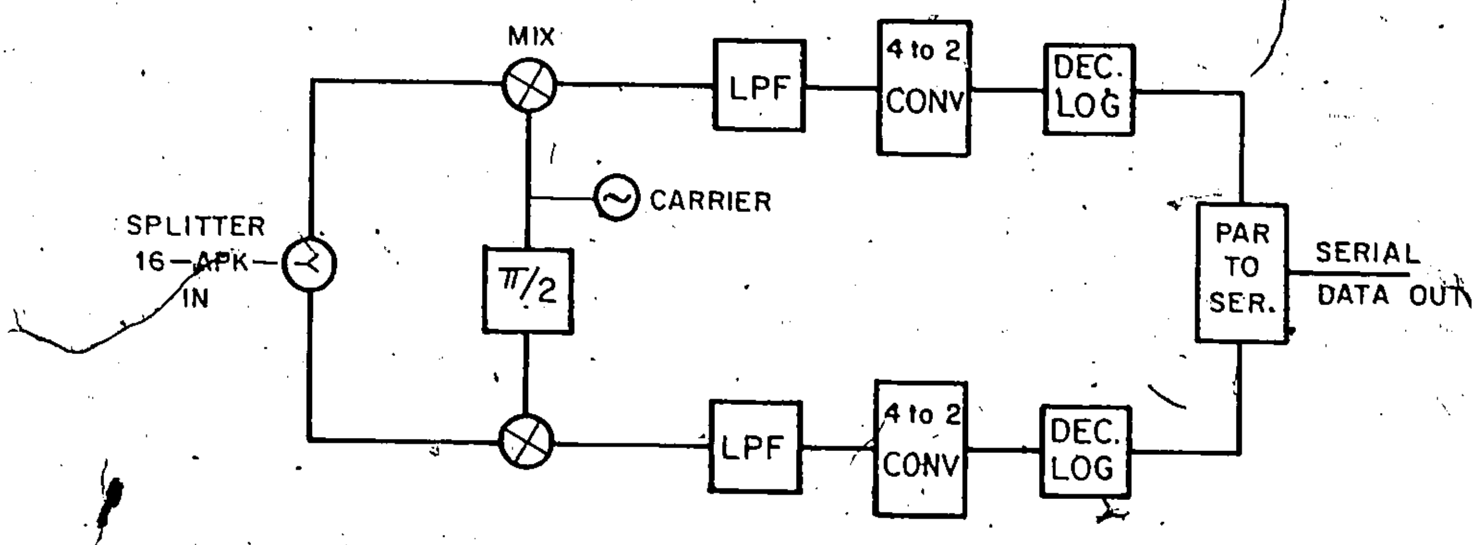


Figure 4.3 - 16-APK Demodulator

The modulated signal arriving from the channel is split and demodulated in the I and Q channels by two DSB-SC balanced modulators whose LO ports are driven by a coherent carrier and its quadrature component respectively. The excess carrier and any harmonics resulting from multiplication (demodulation) are removed by the LPF to which the demodulated signal is fed. At the output of the LPF there is a four level eye diagram. By using a three bit slicer, the four levels are used to obtain a data pattern which is rich in data transition jitter [30]. This jitter is removed by a flip-flop at the output of each slicer since the flip-flop changes state only when the symbol clock leading edge transition is present. The regenerated data is fed into a decoding logic network where the data is placed in the proper channel sequence as was transmitted. The decoding logic also determines and routes data to the correct channel when any of the four BPSK, two QPSK and APK modes are selected at the transmitter. Finally, the data is parallel-to-serial converted and clocked out of the demodulator in serial form. A more detailed study of the demodulator follows.

4.3 Detection of the Modulated Data

The detectors used are the same type of double balanced modulators as was used for modulation. However, the connections for detections are as shown in Figure 4.4.

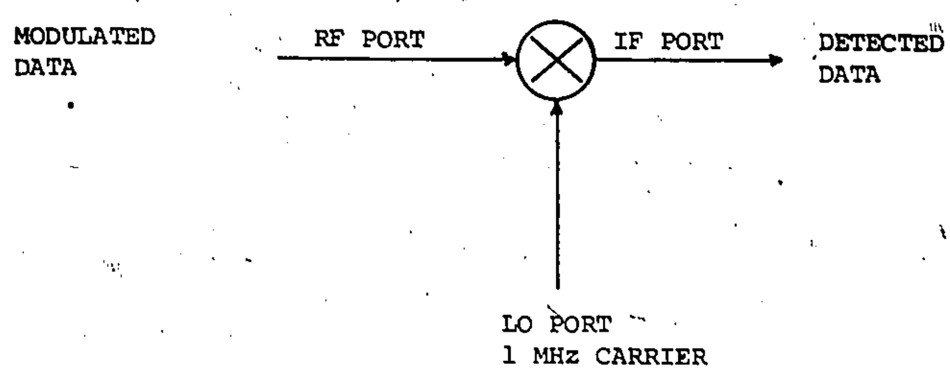
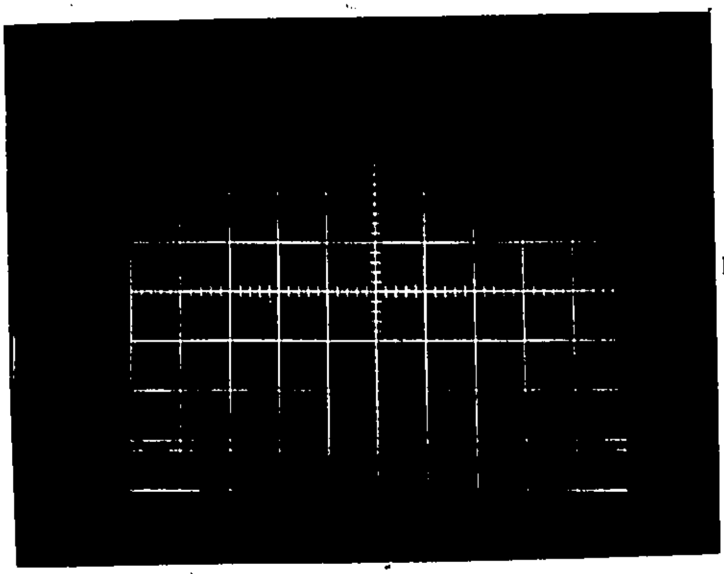


Figure 4.4 - Connection of DSB-SC Modulator for Detection

The mathematics of detection is explained in Appendix C. Here the suppressed carrier is reinserted and beats with the modulated signal to give a tarnished replica of the bandlimited data. This replica is shown in Figure 4.5 and is passed through a LPF to remove unwanted signal components. The circuit design for driving the mixer is the same as discussed for the modulator in Chapter III.

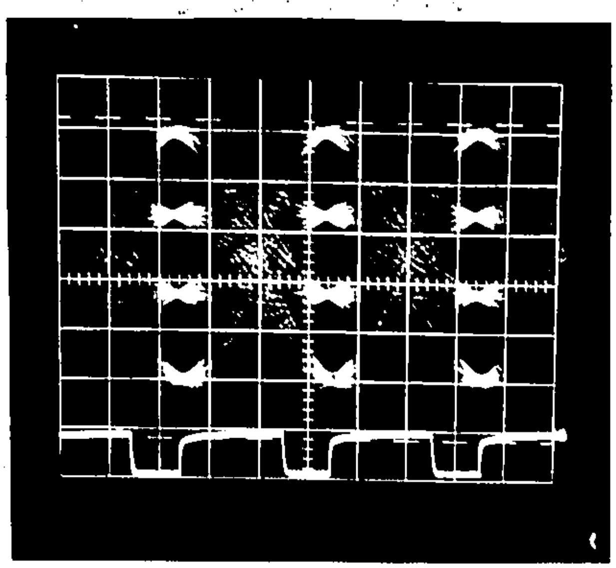


Vertical: 200mV/div
Horizontal: 5 μs/div

Figure 4.5 - Tarnished Bandlimited Data at I Port

4.4 Harmonic Suppression Using Low-Pass Filtering

The design of the LPF is done keeping in mind the trade-off between noise bandwidth, intersymbol and adjacent channel interference. The filters used are modified Butterworth's of fifth order. The design is the same as discussed in Chapter III except that the 3 dB point is at 37 kHz instead of 32 kHZ. This relaxation of the filter poles yield a 3 dB improvement in ISI and a 1 dB reduction in SNR for a net gain of 2 dB improvement in P(e) performance. Passing the detected data (Figure 4.5) through it yields a clean bandlimited data eye pattern as shown in Figure 4.6.



Vertical: 200mV/div

Horizontal: 5 µs/div

Figure 4.6 - Eye Pattern of 16-APK Data at Slicer Input

The data are passed to the slicer input where the bandlimited baseband data is reshaped. The circuit diagram is shown in Figure 4.7.

Here again, the circuit design of the LPF's and the circuit diagram of this filter shown in Figure 4.7 are the same as in Chapter III with the exception of the value of the capacitors that control the break point. Thus relaxation of the filter poles is achieved by using 0.0043 µF rather than 0.0047 µF capacitors, resulting in a shift in the 3 dB cut-off frequency of these filters to 37 kHz.

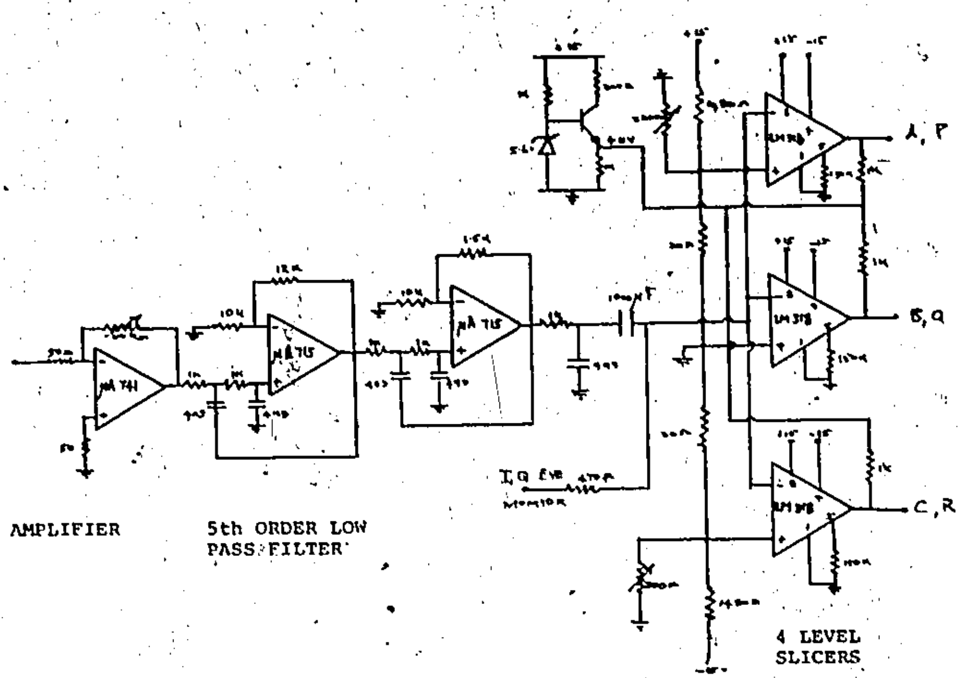


Figure 4.7 - Receive LPF and Slicer Circuit Diagram for I and Q Channels

4.5 Four-to-Two Level Conversion in the I and Q Channel

Data from the slicer outputs in the I and Q channels passes to the decoding circuitry which reshapes and converts it from four levels to two levels. Figure 4.8a shows the four levels on the I and Q channels along with their binary representation, voltage values, and three threshold levels ABC above and below which the respective comparators change states. Since each level in the eye pattern represents two bits, a three bit slicer is used to decode these levels. The associated circuitry and level diagram is shown in Figures

4.7 and 4.8a respectively. Additional logic circuitry as shown in Figure 4.9 is required in order to obtain the original two bits fed in, from the three bits obtained, as a result of four-to-two level conversion.

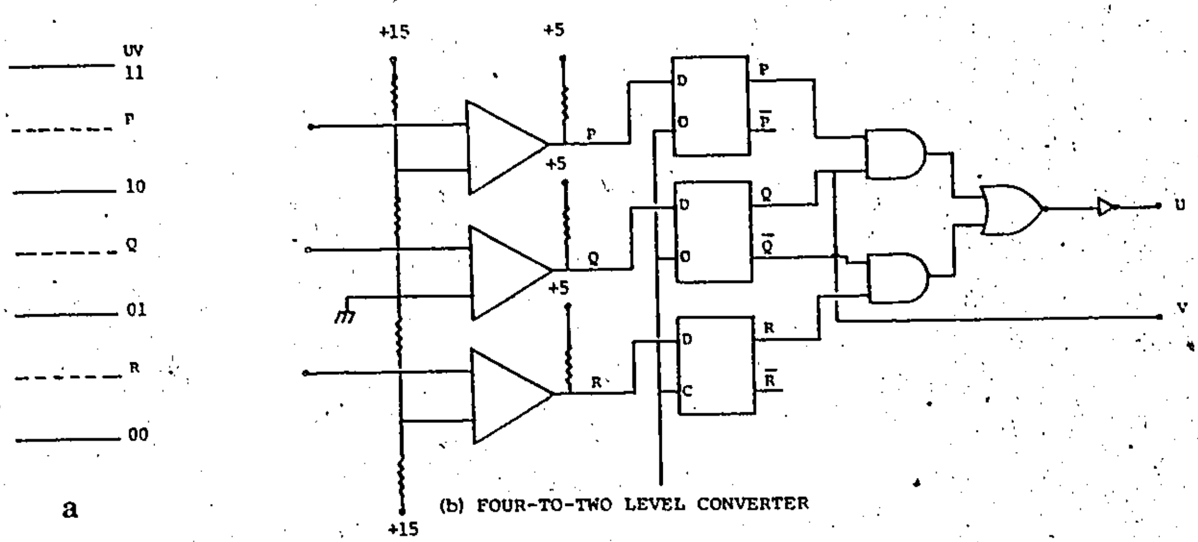


Figure 4.8 (a) Four-Level Representation of the I and Q Channels
(b) Four-to-Two Level Converter

Table 4.1 shows the truth table for a 4-to-2 level converter. Here, ABC, PQR and XY, UV represent the thresholds of the four-level eye diagram and the two-level outputs of the four-to-two level converters in the Q and I channels respectively.

Table 4.1

4-2 LEVEL CONVERTER TRUTH TABLE I AND Q CHANNELS

inputs at slicer			Outputs at 4-2 level converter	binary representation	
A,P	B,Q	C,R	level	X,U	Y,V
0	0	0	1	0	0
0	0	1	2	0	1
0	1	1	3	1	0
1	1	1	4	1	1

From the slicer outputs it is seen by comparing with the slicer inputs that

$$X,U = B = Q,\ I,$$
$$Y,V = A\bar{B} + BC = q,\ i$$

Figure 4.8b and 4.9 show the implementation of these functions at the output of the regenerator. The outputs X,U and Y,V must be processed further as shown in Figure 4.9 in order to realize the proper order and identity of the transmitted data. The outputs X,Y and U,V represent those of the 4-2 level converter found in the Q and I channels respectively. Elaborating, X or Y represents a transmission from channel Q or q respectively, likewise U or V is equivalent to transmission received from I or i respectively.

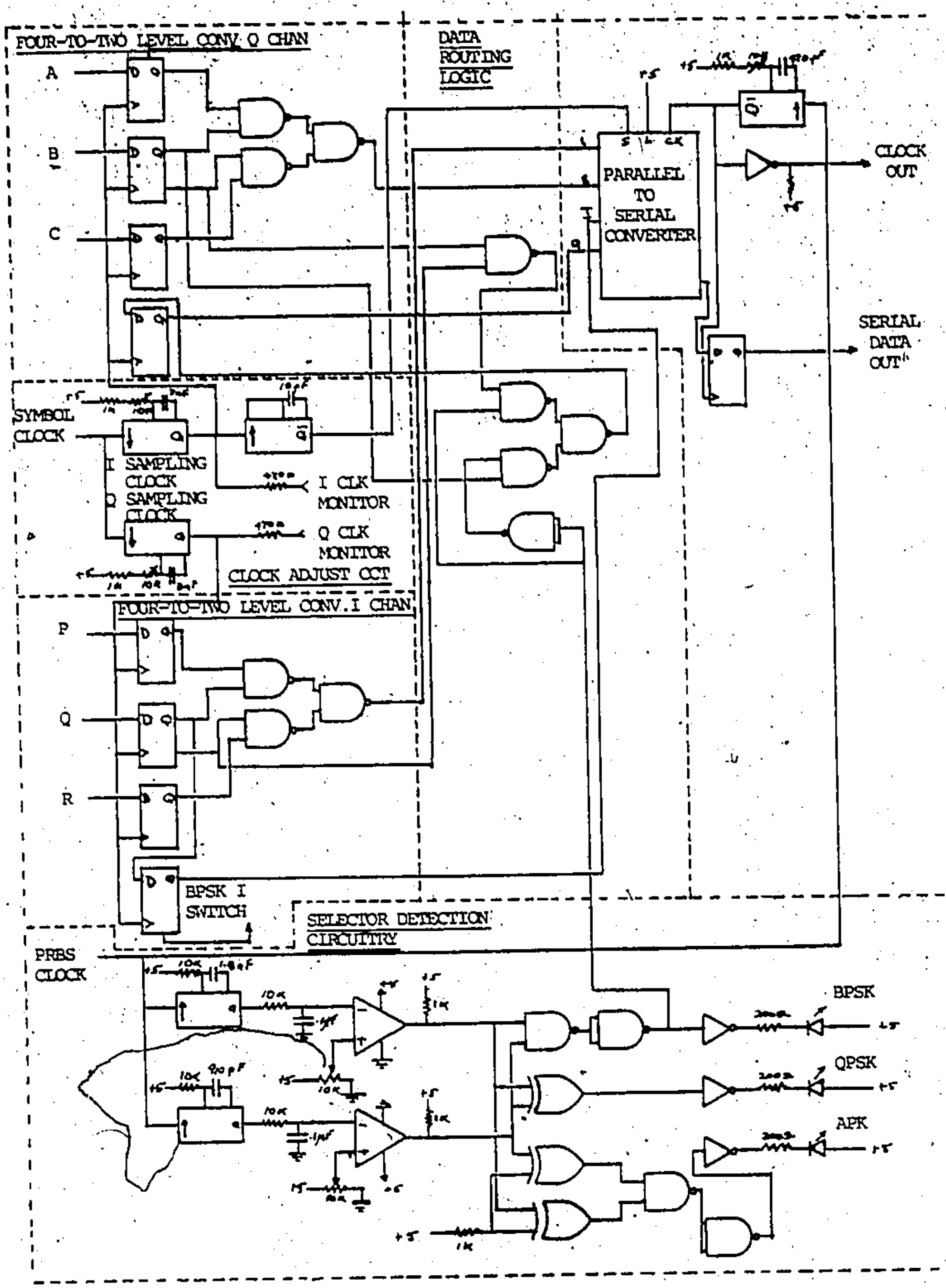


Figure 4.9 - 16-APK Demodulator Decoding Logic Circuitry

4.6 I and Q Channel Decoder Logic for BPSK, QPSK and APK

The outputs X,Y and U,V of the four-to-two level converters in the Q and I channels contain information which must be selected and routed to the parallel-to-serial converter in accordance with the mode (BPSK, QPSK, APK) and channel selected at the modulator. Referring to Figure 4.9 the mode Selector Detection circuitry determines in which mode the modulator is transmitting and sends the appropriate signal to the Data Routing Logic. This logic is necessary because under BPSK and QPSK operation, the data entering the parallel-to-serial converter must enter at the most significant bit (MSB), and two MSB positions respectively if the data transmitter and that received are to be compatible. The operation of the Q and I channel 4-2 level converters have been explained above. The remaining circuitry adjusts the rising edge of the sampling clock so that the position of the sampling instant can be adjusted manually to the point of maximum eye opening. Delay trim circuitry is also included to compensate for propagation delays in the transmission of the data.

The channel decoder logic circuitry collectively clocks the four channels Q, I, q and i through the parallel-to-serial converter in synchronism in order to generate a serial data stream. The bit rate of this data stream varies from 64, 128 and 256 kb/s when the BPSK, QPSK and APK modes respectively are being transmitted.

We have discussed the design of the modem and are now in a position to evaluate its performance in the presence of AWGN and interference.

CHAPTER V

EVALUATION OF MODEM PERFORMANCE

5.1 Introduction

At the present time, there is only one commercially 16-APK system reported by Farinon Canada. Although experimentation and studies are being carried out by companies such as Farinon, Bell Northern Research, Bell Laboratories and the Centre Nationale d'Etudes Télécommunications Laboratory in France, the measured performance of 16-APK modems as reported in the literature has considered only the AWGN environment. Of importance, is the case where spurious signals or interference fall in the band of the desired signal. Such cases can be well simulated with inband SI of various peak factors, bandlimited Co-Channel Interference (CCI) and ACI. These cases should be of special interest because of the presently congested frequency plans where adjacent channels are closely spaced.

The spectral performance of the model will be evaluated with the aim of obtaining its spectral efficiency, that is to say, the number of bits per second that can be transmitted in one hertz of radio frequency bandwidth.

The performance of this modem in an additive white gaussian noise and interference environment will be evaluated with it operating in the 16-APK mode only. This evaluation will compare its probability of error performance as a function of carrier to noise ratio (CNR) and signal to noise ratio with theoretical curves. These comparisons are for the case where the modulated 16-state signal is perturbed by Additive White Gaussian Noise (AWGN), Sinusoidal Interference (SI), Co-channel (CCI) and Adjacent Channel (ACI) interference as derived from a bandlimited BPSK modulated interferer. Although a limited amount of theory on interference for 16-APK exists [31, 32], there has been very little attention paid to relating these theories to practical results in a complex noise and interference environment. This problem has been successfully tackled here and hypothesis have been suggested to explain certain observations. Explanations have been given as to why some theoretical upper bounds have been violated with respect to probability of error performance under certain conditions.

An in-depth study of BPSK or QPSK is not given here as these have been well documented in the literature. However, the P(e) performance is given for these systems only in the case where the pertubation to the modulated signal is AWGN.

5.2 Spectral Performance

Tight specification on spectral out-of-band emission and constraints on spectral efficiency have been set by the Federal Communication Commission (FCC) in the United States and the Department of Communicatins (DOC) in Canada. These apply to common carrier radio systems in the respective country. This has forced the transmission engineer to consider, sometimes at great expense, the problem of spectral shaping.

In this research we chose to employ premodulation low pass filtering to ensure spectral shaping which would yield a spectral efficiency in excess of 3 b/s/Hz.

The power spectrum of a 16-APK signal is given by

$$S(f) = 5T_s|H(f)|^2 \cdot \left| \frac{A \sin \pi T_s(f-f_c)}{\pi T_s(f-f_c)} \right|^2 \quad (5.1)$$

where H(f) is the transfer function of the premodulation low-pass filter,

A amplitude of the modulated 16-APK signal,

T_s symbol duration,

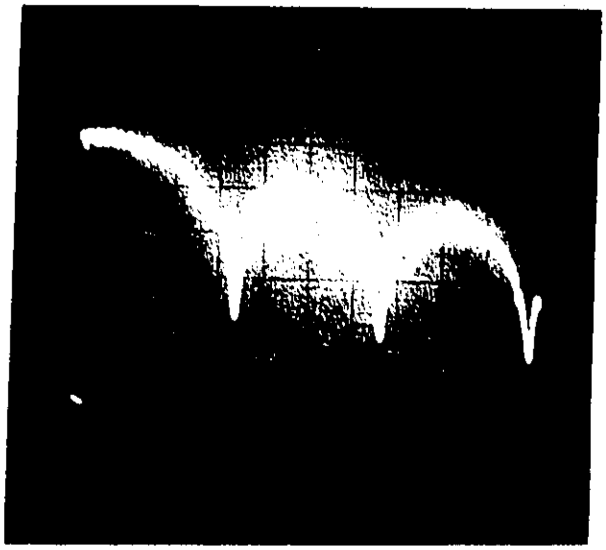
f frequency of interest,

f_c unmodulated carrier frequency.

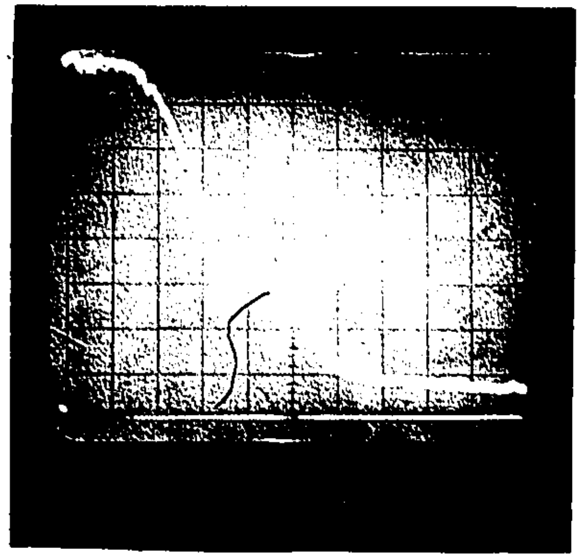
In Figure 5.1a, the measured spectrum of the premodulated pre filtered NRZ signal is shown. This is the case when $|H(f)| = 1$ and $f_c = 0$ in equation 5.1 above. When the random NRZ data is filtered but not modulated (i.e., $|H(f)| \neq 1$ and $f_c = 0$ in equation 5.1), the spectrum shown in Figure 5.1b results. Finally, 5.1c shows the modulated 16-APK signal spectrum which is represented by equation (5.1).

Comparing Figures 5.1a and 5.1b, it is seen that the first spectral null occurs at 64 kHz and that the first side lobe is attenuated by 13 dB and 32 dB respectively with

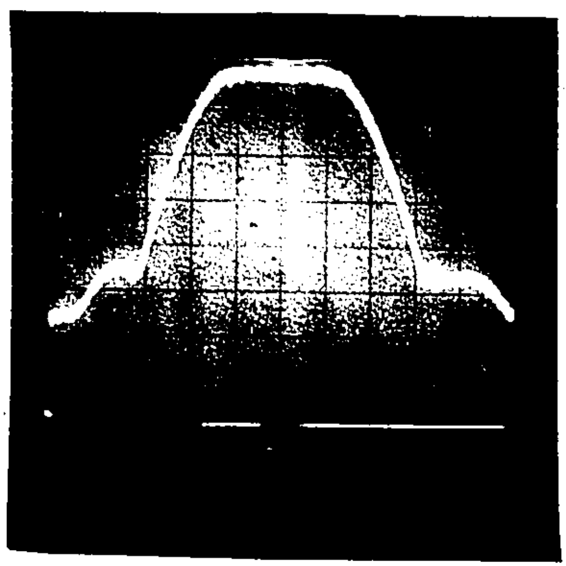
Symbol rate:64 Kbaud, video bandwidth:10 Hz, Bandwidth:1 kHz



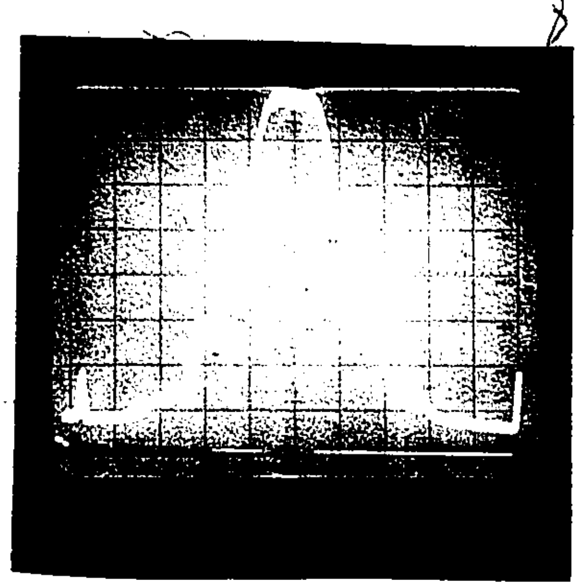
(a) Vertical : 10 dB/div.
Horizontal: 20 kHz/div.



(b) Vertical : 10 dB/div.
Horizontal: 20 kHz/div.



(c) Vertical : 10 dB/div.
Horizontal: 20 kHz/div.



(d) Vertical : 10 dB/div.
Horizontal: 50 kHz/div.

Figure 5.1a - Spectrum of Random NRZ Data Unfiltered
b - Spectrum of Random NRZ Data Filtered
c, d - Spectrum of Random NRZ Data Filtered and Modulated.

respect to the main lobe. The 13 dB attenuation of the first lobe in Figure 5.1a results from the $(\sin x/x)^2$ characteristic of the signal. For the case of Figure 5.1b, in addition to the $(\sin x/x)^2$ attenuation characteristic of the signal, the spectrum is further curtailed by the filter response attenuation. This resultant spectrum is translated to an intermediate frequency by the modulation process as in Figure 5.1c. Figure 5.1d also shows the spectrum at IF to give a clearer picture of the side lobe attenuation. In order to measure the spectral efficiency of the modem, it is first necessary to define the bandwidth. To do this, two bandlimited adjacent channels of 16-APK modulation should be placed one on either side of the desired channel. The separation between the adjacent channels should be adjusted such that they are as close as possible without causing errors in the desired channel. The bandwidth needed to calculate the spectral efficiency could then be calculated. However, this method is not possible since the necessary modulators are not available. As an alternate method, which also gives spectral efficiency of the modem, the spectrum shown in Figures 5.1c and 5.1d was translated up to 6 GHz. The bit rate was translated and adjusted to fit within the Federal Communications Commission (FCC) mask for an authorized bandwidth of 30 MHz. This is a valid approach because the FCC mask was designed such that any spectrum fitting within it, automatically satisfy adjacent channel emission requirements.

The transmit spectrum (Figure 5.1c) is normalized with respect to the bit rate as follows

$$f_n = f/f_b$$

where f_n - normalized frequency

f - a frequency component from Figure 5.1c

f_b - bit rate (256 Kb/s)

The attenuation of the spectrum is unchanged. Table 5.1 gives the relevant values for the normalized spectrum and the

Table 5.1

NORMALIZED TRANSMIT SPECTRUM WITH TRANSLATED FREQUENCIES

Normalized Frequency (f_n)	Attenuation dB	Translated Frequency (f_f) MHz
0	0	0
.0781	1	7.9
.0976	3	9.9
.1172	7	12.0
.1562	15	15.9
.1953	27	19.9
.2188	35	22
.2344	43	24
.2734	46	27.9
.3125	45	32
.3906	51	39.9

translated f_f such that

$$f_f = f_n \times f_s$$

where f_s is the bit rate transmitted in the authorized bandwidth. This rate is $f_s = 400 \times f_b = 102.4$ Mb/s and was obtained using equation 5.2 below. This bit rate is equivalent to 16-APK modulation using four parallel bit streams each of 25.6 Mb/s. These bit streams would be used to modulate a 70 MHz carrier which would be converted to the 6 GHz band. This process would yield the spectrum in Figure 5.1e. It is clear then, that using this scheme, there would be no problem in fitting two scrambled DS-3 signals in 30 MHz

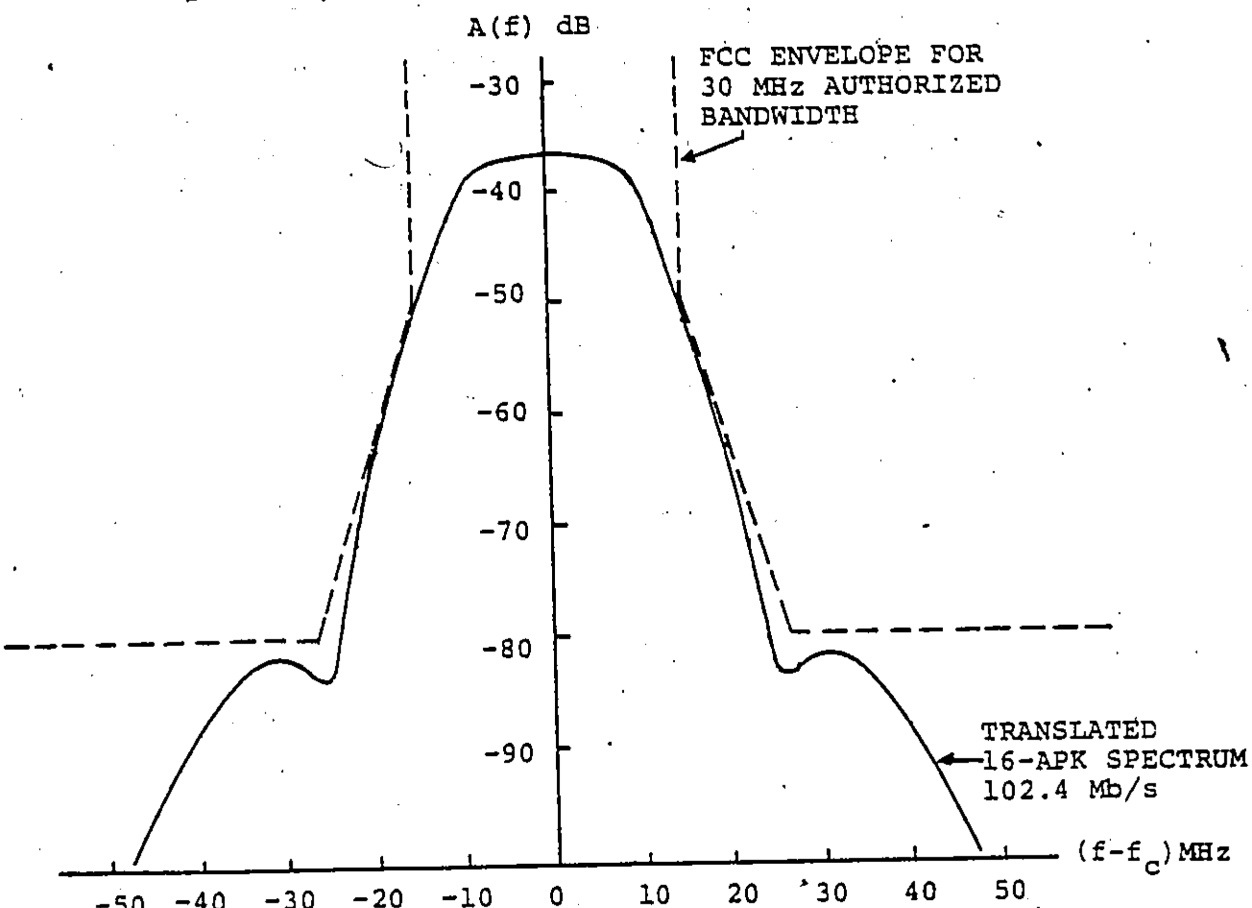


Figure 5.1e - FCC Mask Applied to Translated 16-APK Transmit Spectrum

of bandwidth where each bit stream need only be at a rate of 22.5 Mb/s.

To fit the spectrum within the FCC mask, it was necessary to determine the maximum possible data rate R. This was determined to be 102.4 Mb/s using the following equation [43].

$$A(f) = 10 \log_{10} 4000 + 10 \log_{10} S_n(f) - 10 \log_{10} B_N R \quad (5.2)$$

where $A(f)$ - power in a 4 kHz band per total power

$S_n(f)$ - normalized power spectral density of the transmit spectrum

B_N - normalized noise bandwidth of the transmit spectrum

R - transmission bit rate

The normalized values of $S_n(f)$ are given in Table 5.1, thus, only the normalized noise bandwidth of the transmit spectrum is needed. This was found by integrating the normalized bandlimited BPSK signal spectrum over ten symbol intervals and dividing by four since 16-APK is four times as spectrally efficient as BPSK. Thus

$$B_N = \frac{1}{4} \int_{-5/T}^{5/T} \underbrace{\left(\frac{\sin \pi x}{\pi x}\right)^2}_{\text{normalized NRZ spectrum}} \cdot \underbrace{\frac{1}{[1 + x/.468]^{10}}}_{\text{5th order Butterworth filter response}} dx \quad (5.3)$$

where T - symbol duration

x - frequency

The constant 0.468 in equation 5.3 represents the normalized 3 dB attenuation frequency for the bandlimited BPSK signal spectrum. Equation 5.3 was solved using the computer and the value of B_N was found to be

$$B_N = 0.185$$

Substituting for B_N in equation 5.2 and taking the required logarithms yielded

$$A(f) = 43.3 - 80.1 + 10 \log S_n(f)$$

$$= 36.8 + 10 \log S_n(f) \tag{5.4}$$

From equation 5.4 it is clear that the spectrum, the translated power spectrum from Table 5.1, should be placed in the FCC mask with the power of the center frequency positioned at the -36.8 dB mask attenuation point as shown in Figure 5.1e. From this figure it is seen that the 16-APK modem has an equivalent transmission rate of 102.4 Mb/s in 30 MHz of RF bandwidth. Thus

$$\text{Spectral Efficiency} = \frac{\text{Transmit bit rate}}{\text{RF bandwidth}}$$

$$= \frac{102.4 \times 10^6}{30 \times 10^6} = 3.41 \text{ b/s/Hz}$$

This is the same as transmitting 256 Kb/s in 75 KHz of RF bandwidth as was accomplished in this research. With regards to the spectral performance of 16-APK as compared with advanced modulation systems such as 8-PSK and 16-PSK, 16-APK has superior spectral performance [34] as compared with 8-PSK. Elaborating, in order to obtain the spectral efficiency required by the regulatory bodies for certain digital microwave systems, the filtering required for 8-PSK is severe. This filtering has been achieved to meet the 2.6 b/s/Hz required in the 6-GHz carrier band [35]. For this efficiency, the spectrum of the 8-PSK radio system fits tightly in the FCC mask as shown in Figure 5.2.

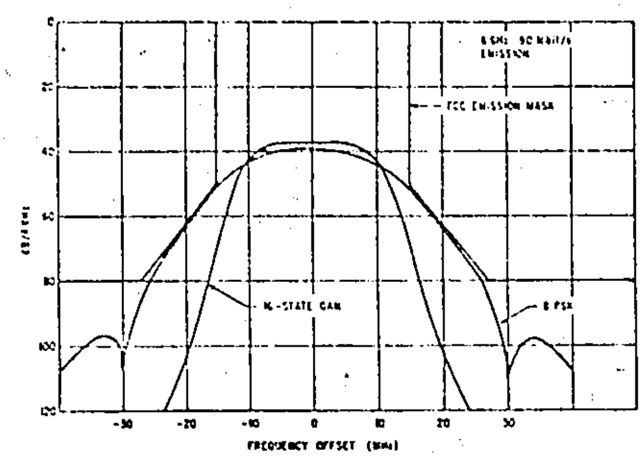


Figure 5.2 - FCC Mask for 6-GHz Band with 8-PSK and 16-APK Emission [35]

However, this mask does not provide sufficient out-of-band attenuation to permit satisfactory adjacent channel application particularly under conditions of adverse propagation condition [35]. The superior spectral performance of 16-APK is apparent since for the same spectral efficiency as 8-PSK, tighter filters can be used yielding superior adjacent channel attenuation properties as shown in Figure 5.2 Experimental work on 16-PSK has not been persued with much enthusiasm because of the superior performance of 16-APK.

5.3 Experimental Analysis of Probability of Error Performance

An evaluation of the probability of error (P(e)) performance of the modem as a function of carrier-to-noise ratio (C/N) has resulted in P(e) curves which compare well with those theoretically derived. The theoretical P(e) curves shown in this section are as would be obtained from a theoretically optimum receiver when the received signal is perturbed by Additive White Gaussian Noise (AWGN) in the Double-Sided Nyquist Bandwidth (DSNB) [6]. The P(e) curves plotted for infinite carrier-to-interference ratio (CIR) as well as those obtained for various levels of sinusoidal, adjacent and co-channel interference were measured in a noise bandwidth of 74 kHz corresponding to the cut-off frequency of filters used for a symbol rate of 64 kbaud. Premodulation fifth-order Butterworth filters are used to curtail the signal spectrum thus resulting in a loss of approximately 0.6

dB in spectral power. To compensate for this, all measured P(e) curves have been shifted to the right by that amount.

The P(e) performance of the modem in the presence of AWGN and a single inband sinusoidal interferer is shown in Figure 5.3.

For this (and all other) interferers, the peak factor is measured at the input to the threshold detectors (four-to-two level converters) since this is where the decisions are being made. The measured value of peak factor for a single sinusoid is 3 dB as calculated by the following formula where peak and rms interference are measured.

$$\text{peak factor} = 20 \log_{10} \left[\frac{\text{peak interference}}{\text{rms interference}}\right] \qquad (5.5)$$

Figures 5.4 and 5.5 show the modem performance when two and three inband sinusoids interfere with the wanted signal respectively. For the case of two sinusoids (Figure 5.4) the peak factor was measured to be 6 dB, similarly, it was measured to be 8 dB for the case of three interfering sinusoids. Common to the above three cases is a rightward shift in the P(e) curves as the interference level increases (ie. CIR decreases). This is expected given the decrease in eye aperture for increased interference level. Comparing these cases, it is observed that there is a shift for any given CIR < ∞ as the number of interfering sinusoids increase. Rosenbaum and Glave [36] showed that an upper bound in error probability exist for M-ary coherent phase shift keyed systems which depends solely on the relative rms

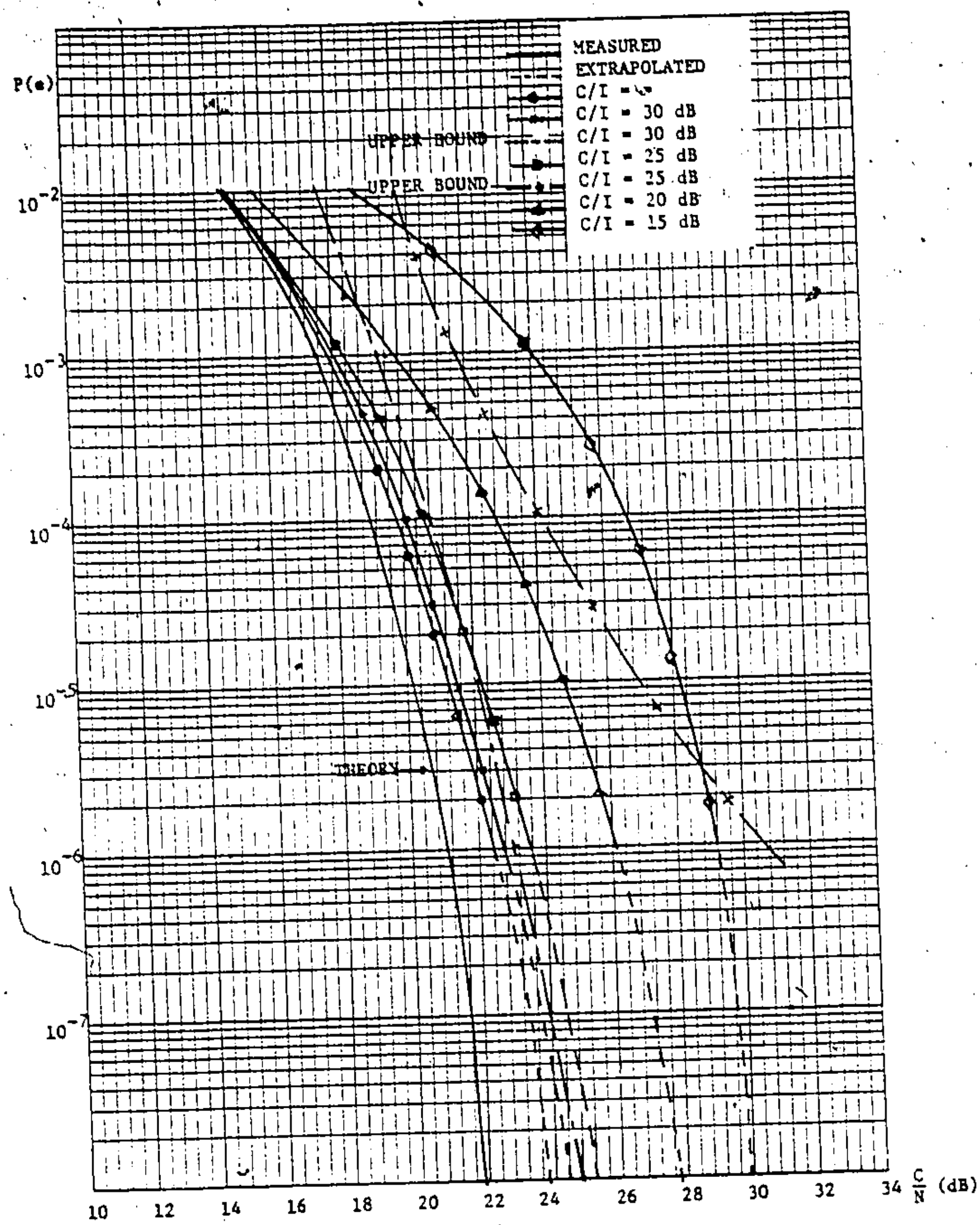


Figure 5.3 - Performance of a 16-APK Modem in the Presence of Both Sinusoidal Interference and Gaussian Noise for Various Levels of Interference from a Single Sinusoid

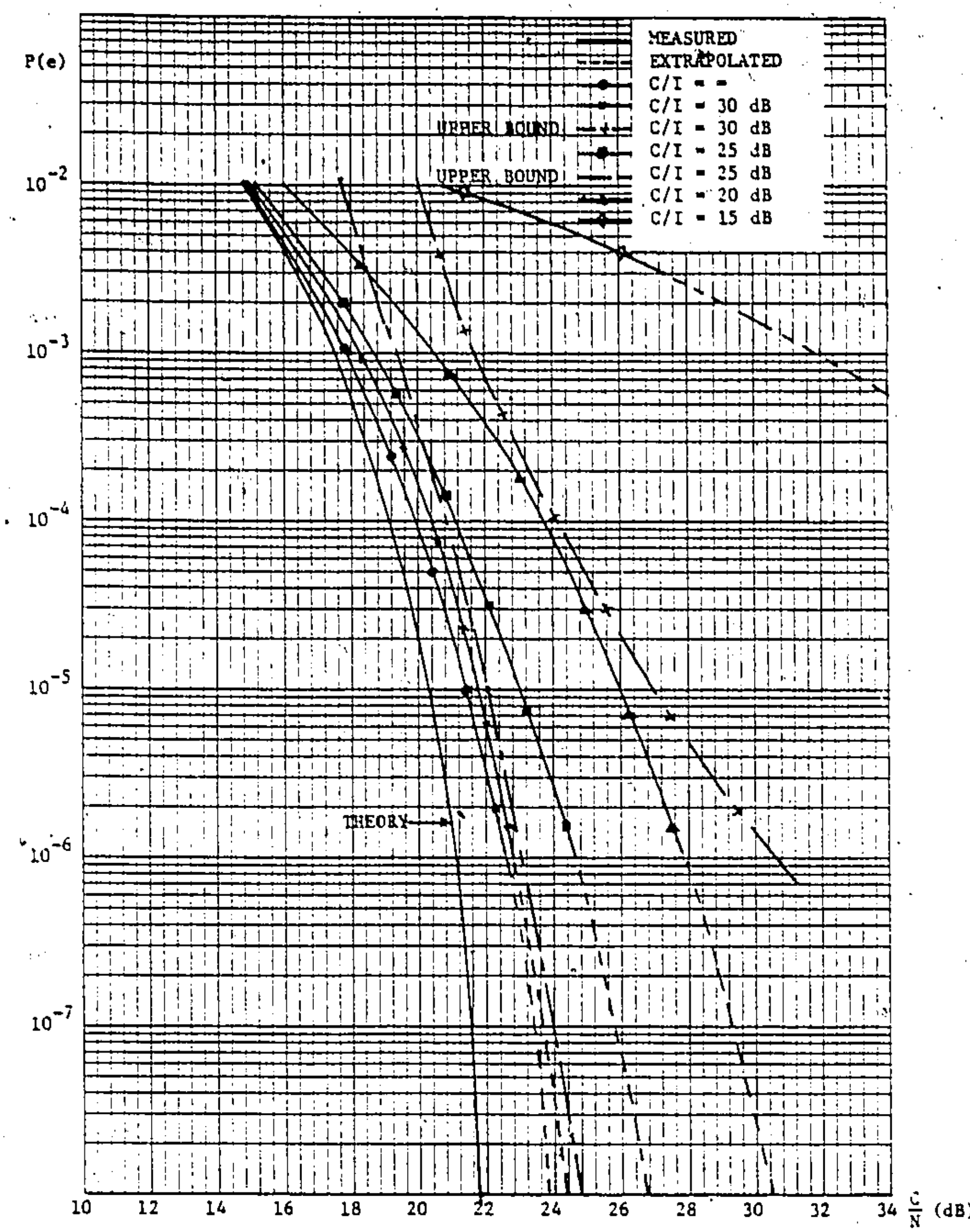


Figure 5.4 - Performance of a 16-APK Modem in the Presence of Both Sinusoidal Interference and Gaussian Noise for Various Levels of Interference from Two Sinusoids

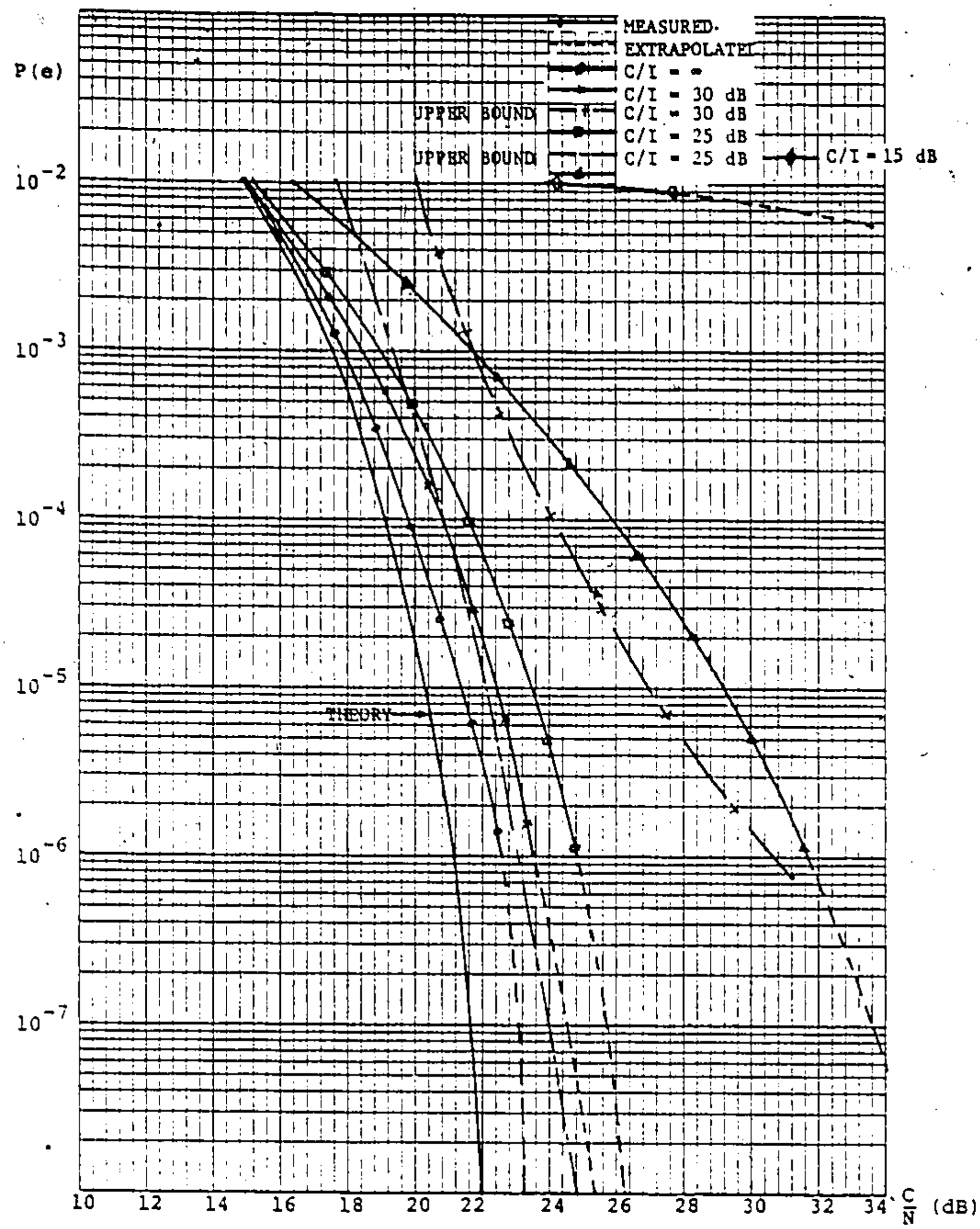


Figure 5.5 - Performance of a 16-APK Modem in the Presence of Both Sinusoidal Interference and Gaussian Noise for Various Levels of Interference from three Sinusoids

and peak value of the interfering envelope (ie, the peak factor). They showed that

$$P(e) \le \underbrace{\frac{1}{2}\,\mathrm{erfc}(\sqrt{Y})}_{①} + \rho\frac{e^{-Y}}{\sqrt{\pi}} \sum_{\ell=1}^{\infty} \underbrace{\frac{H_{2\ell-1}(\sqrt{Y})}{2^{2\ell}\,\ell!\,\ell!}\left[\sqrt{Y}\,\frac{R}{p(0)}\right]^{2\ell}}_{②} \qquad (5.6)$$

where $\mathrm{erfc}(x) = \frac{2}{\pi}\int_x^{\infty} e^{-t^2}\,dt$

Y	= carrier to noise ratio
ρ	= r^2/R^2_{xy} = antilog (-0.1 peak factor)
ℓ	= a positive integer which determines the number of terms in the series
H	= Hermite polynominal
R	= peak value of the interference envelope
r^2	= variance of the interference
$p(0)$	= modulated carrier wave

Equation (5.6) shows that the upper bound on the P(e) of a binary coherent phase-shift keyed system is a function of the CNR, represented by ① in equation (5.6), the reciprocal peak factor is proportional to ρ and the reciprocal CIR = R/p(0). Thus, if the CIR=∞ , ② in equation (5.6) is zero for all and P(e)= 1 as is expected in the binary case. As the CIR approaches 0 dB the term ② adds to term ① shifting the P(e) curve to the right by an amount dependent on | CIR| and the peak factor which is proportional to $1/\rho$. Although ① is easily evaluated, the series has to be evaluated by computer and is not a simple task. This evaluation was executed by Rosenbaum and Glave and documented on P(e) versus CNR curves for fixed values of CIR and various values of peak factor for the BPSK case. A typical set of curves for CIR=10 dB is shown in Figure 5.6

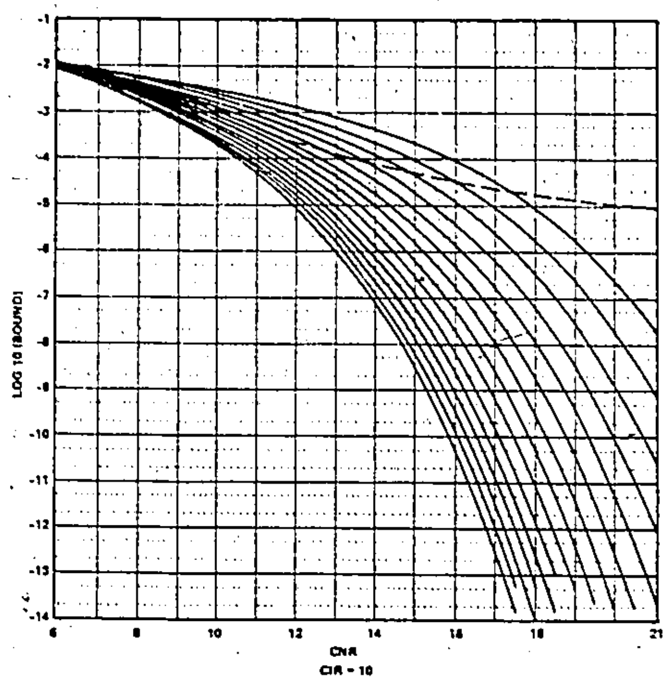


Figure 5.6 - Upper Bound for BPSK for CIR=10 dB, Lowermost Curve PF=0 dB, Uppermost Curve PF=7 dB Intermediate Curves in Increment of 0.5 dB PF [36]

They extended these bounds to the M-ary PSK case by modifying the relationship for the binary case as follows.

P(e)(M-ary) at [CNR=XdB]=2P(e)(BPSK) at [CNR=(X+CF)dB) (5.7)

for a given C/R(M-ary) = C/R(BPSK) + CF

where

$$CF = -20 \log_{10} \sin \frac{\pi}{M} \tag{5.8}$$

is the correction factor.

For comparison with 16-APK (i.e., M=16), the curves for 16-PSK using the above relationships will be derived for a peak factor of 3 dB.

From equation (5.8) $CF = -20 \log_{10} \sin \frac{\pi}{16}$

$= 14$ dB

Thus 14 dB must be added to CNR abscissa, and to each value of CIR in the BPSK case while the ordinate is multiplied by 2 with respect to the binary case to obtain 16-PSK. This is shown in Figure 5.7. Comparing these results with those in Figure 5.3 it is observed that the 3 dB peak factor has a more degrading effect on the overall performance of a 16-PSK than it does on a 16-APK system.

Extending this concept to the 16-APK case, we note that although the theory has not yet been established, there is positive correlation between the peak factor of the interfering sinusoids and the amount of degradation of C/N ratio and hence P(e) performance of the modem as shown in Figures 5.3 to 5.5.

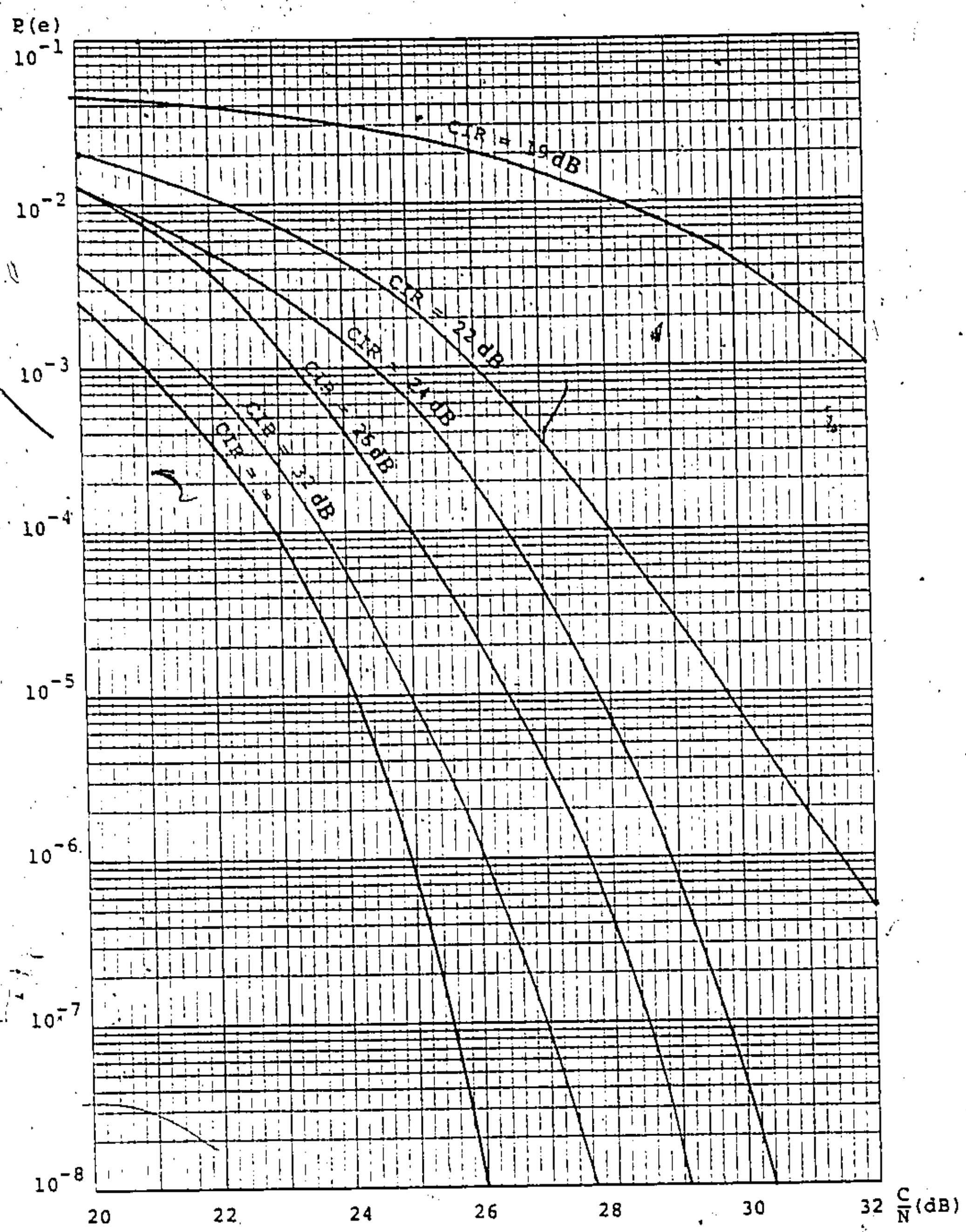


Figure 5.7 - Derived P(e) vs CNR from Rosenbaum and Glave [27] Bound for a PF=3 dB as in the Case of a Single Sinusoidal Interferer for a 16-PSK System

This hypothesis is further substantiated by a study of modem performance, as shown in Figure 5.8, when a bandlimited BPSK modulated signal centered 45 kHz above the wanted carrier as in single channel per carrier (SCPC), perturbs the 16-APK modulated signal. The BPSK signal constitutes adjacent channel interference, i.e., interference where the undesired signal is primarily outside the passband of the wanted signal. For this case the peak factor was measured to be 6.4 dB and yielded a P(e) performance which is better than that obtained with three interfering sinusoids where the peak factor is 8 dB, but worse performance than obtained with two sinusoids where the peak factor is 6 dB.

More evidence for the acceptance of this hypothesis is obtained by the results obtained from co-channel interference shown in Figure 5.9. The interferer is a bandlimited BPSK modulated signal centered on the same nominal carrier frequency as the desired signal. In this case the peak factor was measured to be 7.4 dB (here the effect of the band edge on CCI is not as severe as with ACI) and the P(e) performance of the modem under these conditions was better than in the case of three sinusoid where the peak factor is greater, and worse than that of adjacent channel interference where the peak factor is less than 7.4 dB.

On all figures showing the P(e) performance of the modem, two additional curves have been drawn. These curves indicate an upper bound to the probability of error for the 16-APK system with AWGN and interference as derived by Javed

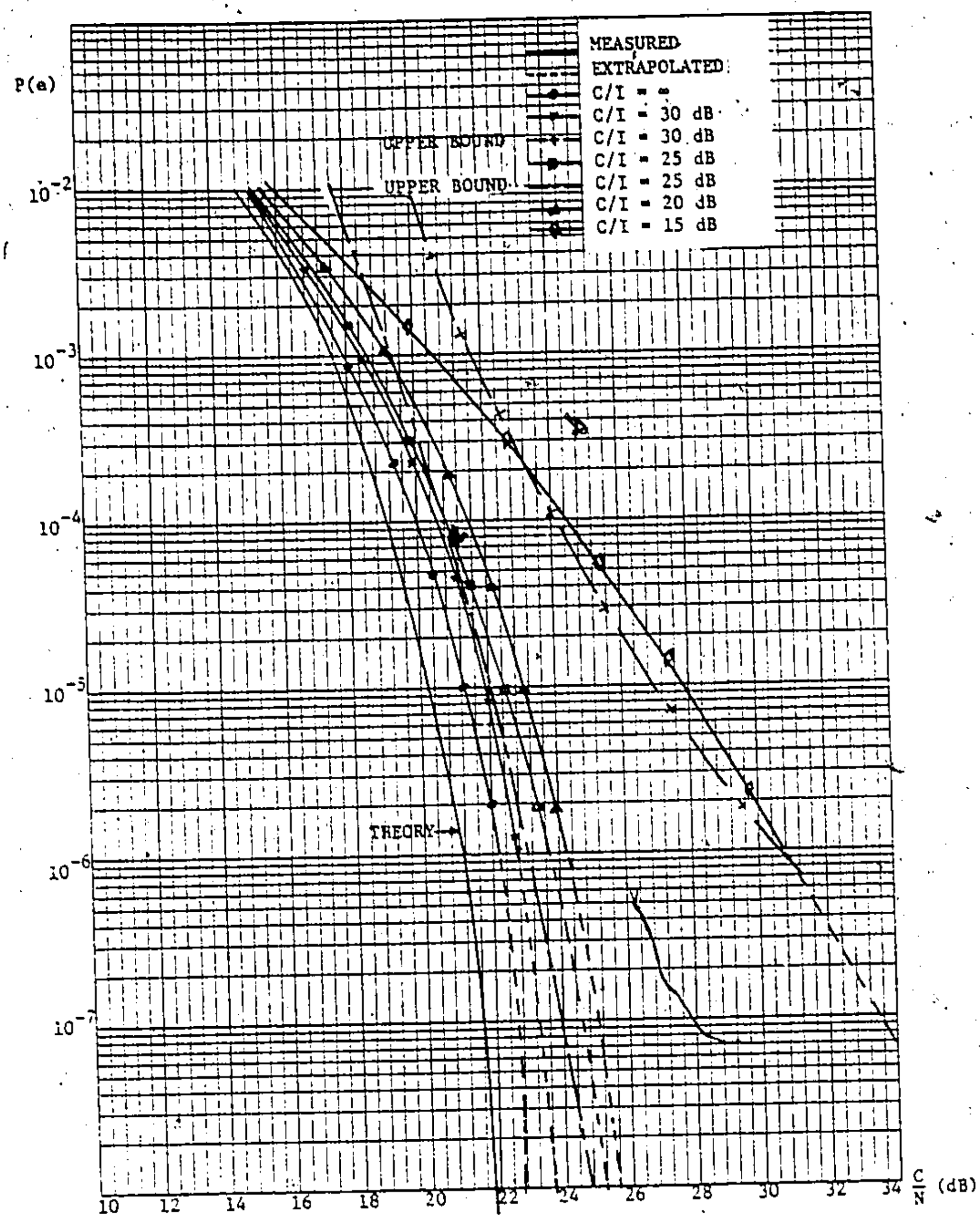


Figure 5.8 - Performance of a 16-APK Modem in the Presence of a Bandlimited BPSK Adjacent Channel Interferer[1] Centered 45 kHz above the Desired Signal, along with Gaussian Noise for Different Levels of Interference

1. The interference power in the adjacent channel is proportional to the spill over energy as a 66 kHz BPF was used in the wanted channel.

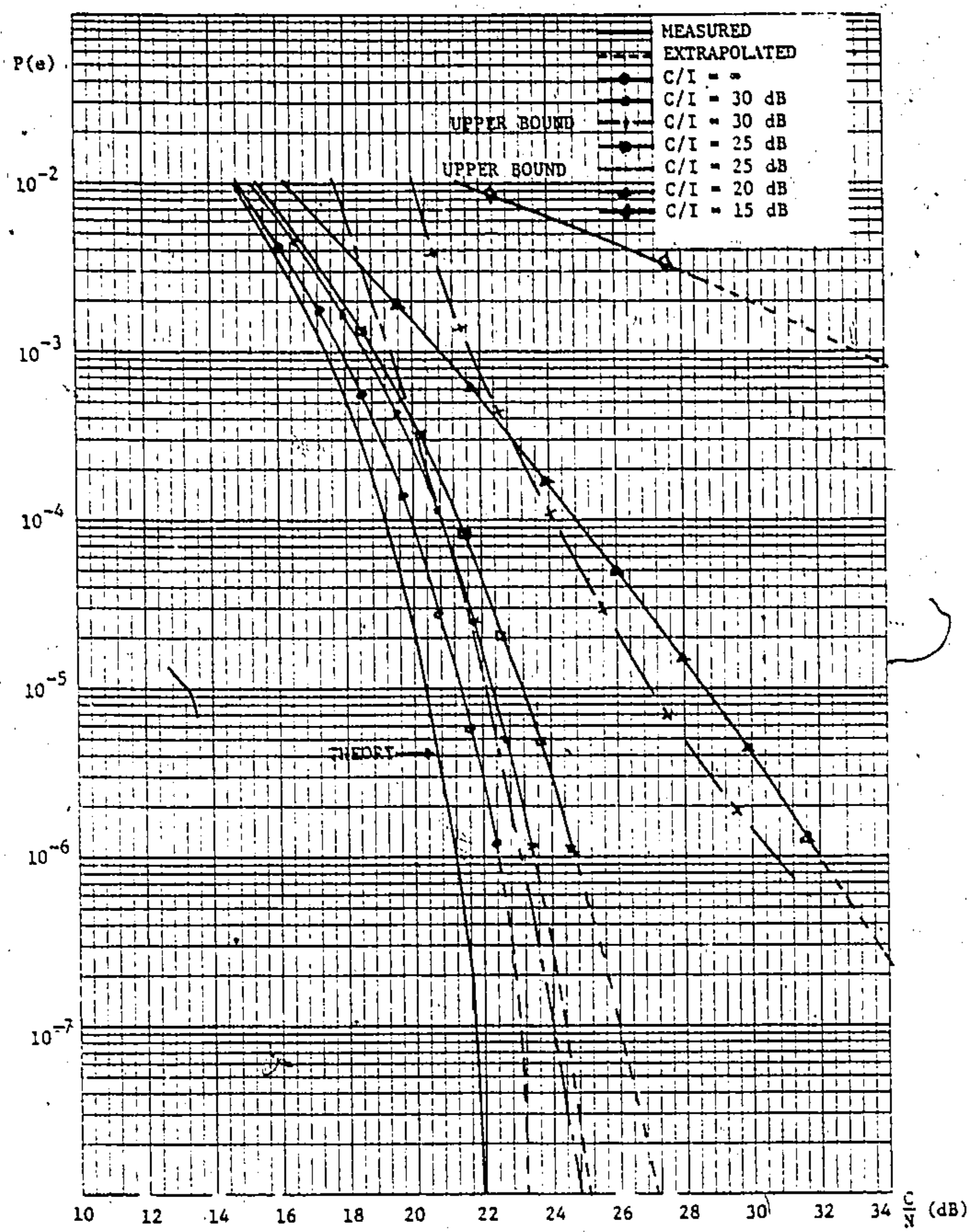


Figure 5.9 - Performance of a 16-APK Modem in the Presence of a Bandlimited BPSK Co-Channel Interferer along with Gaussian Noise for Different Levels of Interference

and Tetarenko [37]. They showed that the upper bound for the average probability of error in a coherent M-ary QASK i.e., M-ary APK system is given by

$$P(e) \le \frac{(2N-1)}{2N}\exp[-\frac{1}{2}(\frac{3}{4N^2-1})\frac{S}{1+\sum_{k=1}^{P}2S\alpha_k^2}] \tag{5.9}$$

where S - average signal-to-noise ratio given by

$$S = (\frac{4N^2-1}{3})d^2/\sigma_n{}^2 \tag{5.10}$$

N - an integer such that $M=(2N)^2$,

M - number of states in the signal space,

k - number of interferers,

α_k^2 - power in the k^{th} interferer,

σ^2 - variance of the noise,

d - minimum half distance between any two signal states.

Substituting (5.10) in (5.9)

$$P(e) \le \frac{(2N-1)}{2N}\exp[\frac{1}{2}(\frac{3}{4N^2-1})\frac{\frac{(4N^2-1)}{3}\frac{d^2}{\sigma_n^2}}{1+\sum_{k=1}^{P}2\,\alpha_k^2\,\frac{(4N^2-1)}{3}\,\frac{d^2}{\sigma_n^2}}] \tag{5.11}$$

but N = M/2 = 2 for the case of 16-QASK.

Substituting for N in equation (5.11) and simplifying

$$P(e) \le \frac{3}{4} \exp \frac{1}{2} \frac{d^2}{\sigma_n^2} \left(\frac{1}{1 + \sum_{k=1}^{P} 10\alpha_k^2 d^2/\sigma_n^2} \right) \tag{5.12}$$

This bound is plotted on Figures 5.3, 5.4, 5.5, 5.8 and 5.9 for CIR of 25 and 30 dB.

From our results, the tightness of the bound with respect to any interferer is a function of its peak factor. thus, for example, the CIR=30 dB bound becomes pessimistic if the peak factor of the interferer is greater than approximately 7 dB for that level of CIR. This is verified by the fact that for interference with one and two sinusoids as well as adjacent channel, which all have peak factors less than 7 dB, the P(e) performance of the modem as a function of CNR all lie within the bound for CIR=30 dB. However, for three interfering sinusoids and co-channel interference each of which have peak factor greater than 7 dB, the bound proves pessimistic beyond the threshold P(e) of 10^{-4}. The theoretical upper bound for CIR=25 dB is loose enough such that all interferers considered here have P(e) performance for CIR=25 dB which lie within this bound. This can be observed on all figures.

Figure 5.10 shows the P(e) performance when the 16-APK signal is perturbed by sinusoidal adjacent and co-channel interference. This figure shows that a greater degradation in performance should be expected with co-channel than with adjacent channel interference or a single sinusoid, similarly greater degradation results when the interference is adjacent channel rather than a single sinusoid. This is clear from the above discussion on peak factor.

5.4 Switching Between 16-APK and QPSK or BPSK

The quasi-universal property of the modem is demonstrated by switching modulation techniques from 16-APK to QPSK or BPSK [38]. This property may be useful because digital radio microwave systems are expected to maintain a high Probability of Error P(e) performance under varying propagation conditions. However, there are occasions when changing channel characteristics such as fading forces these systems to fall below the operating threshold. It is with such conditions in mind that we included the switchable feature in our modem. Figure 5.11 shows a conceptual diagram of the system configuration.

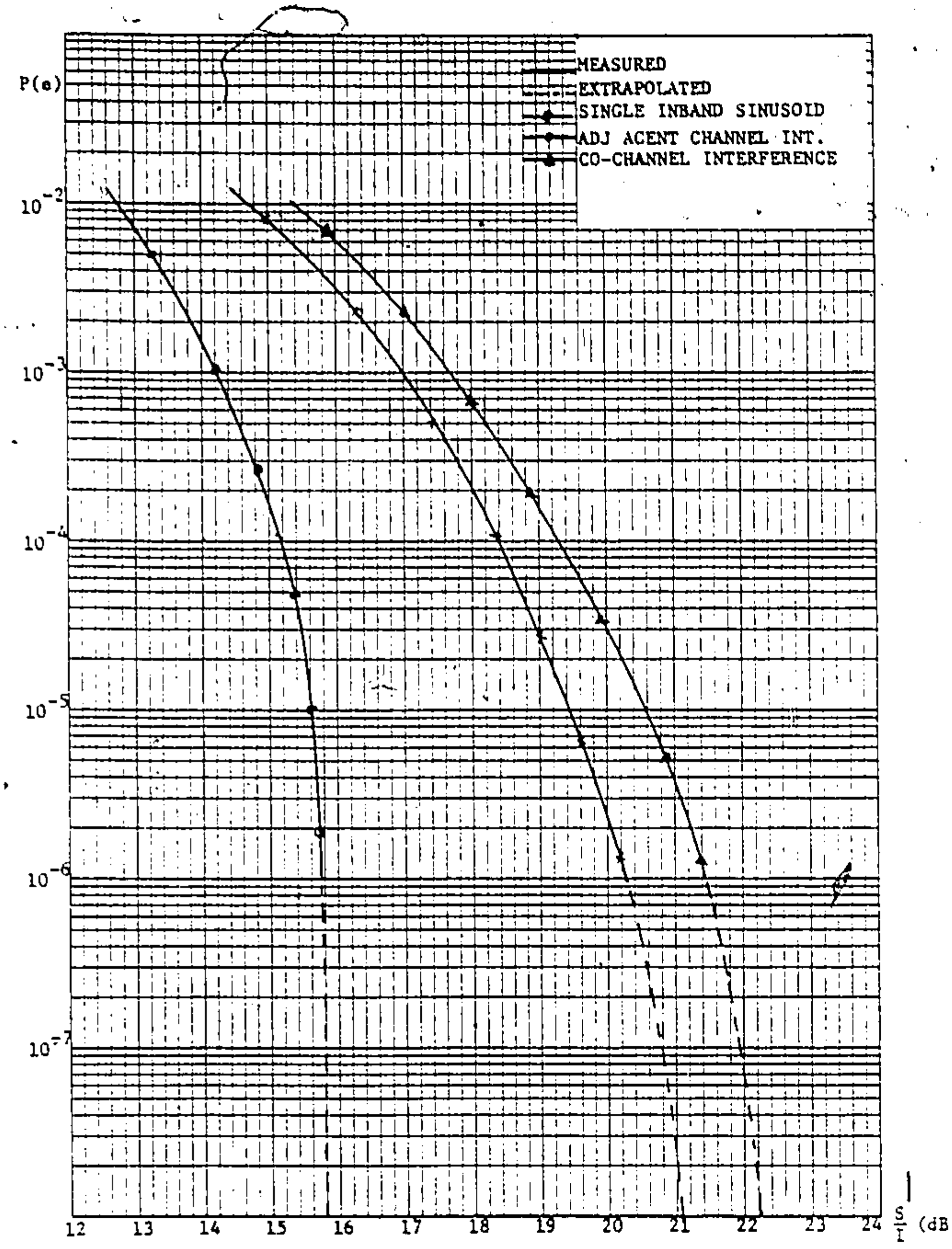


Figure 5.10 - Performance of a 16-APK Modem in the Presence of a Single Sinusoid, Adjacent and Co-Channel Interference Only with S/I measured at base band at the slicer input.

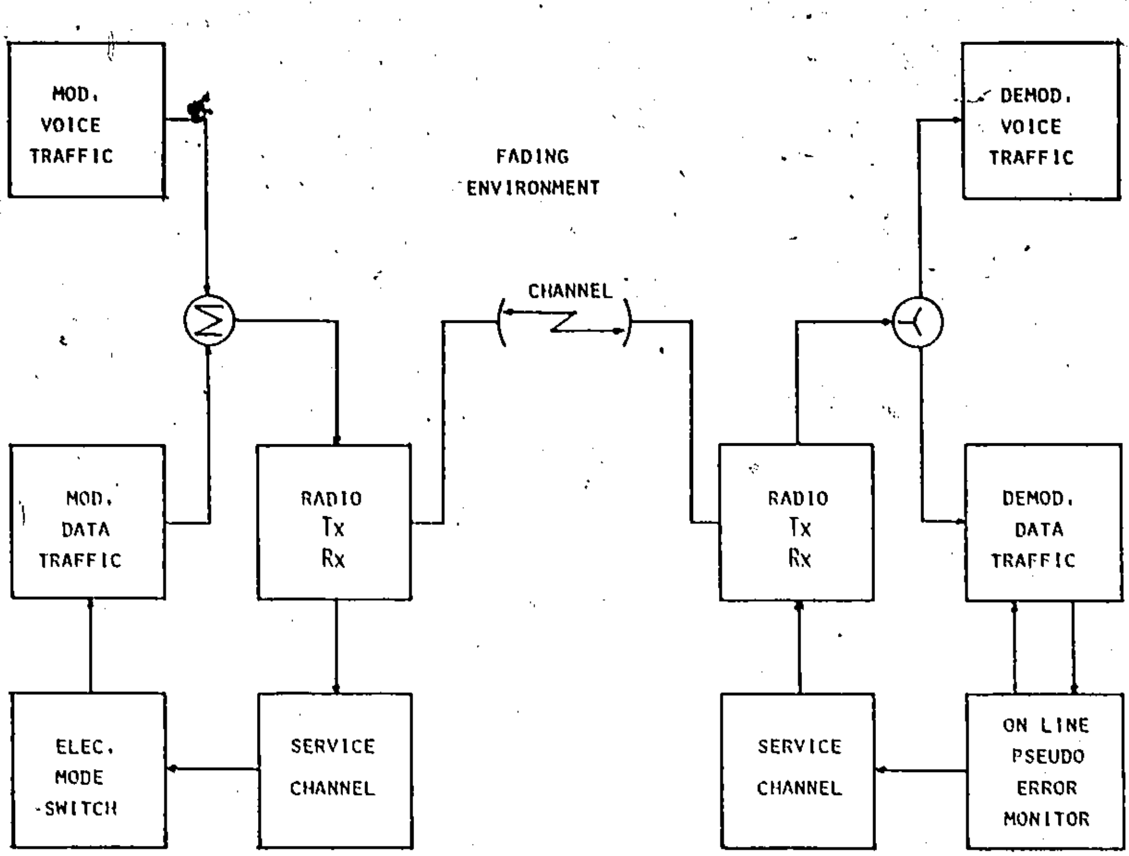


Figure 5.11 - System Configuration for Adaptable Modulation Technique

First we must point out that our system employs manual selection of the operating mode (APK, QPSK, BPSK) at the modulator and that the demodulator adjusts automatically to the mode selected. Automatic selection of the mode is a topic that will be studied as an extention to this research.

Referring to Figure 5.11, the modulated say 16-APK data and voice traffic is transmitted through a channel and is received at some destination where it is demodulated. An on-line Pseudo-Error Monitor (PEM) [39] is used to monitor the performance of the system constantly. When propagation conditions worsen such that the system falls below the threshold P(e) the PEM commands the demodulator directly and the modulator via the service channel to change to QPSK. (QPSK requires less signal-to-noise (S/N) ratio than 16-APK to operate.) The system bit rate is now halved so only the most important digital and voice traffic is carried. If conditions worsen still further, or if initially the condition for propagation was very bad, the PEM can order a further change to BPSK again with adjustment in data and voice traffic load. When things get back to normal, the most efficient modulation technique is maintained enabling normal voice and traffic loading.

In our system, the symbol rate remains the same and the bit rate changes as the modulation technique changes. This simplifies the problem of filter design enabling the use of one set of filters for all three modulation techniques. Three sets of filters would be needed, one for each modulation technique if the bit rate were to remain constant regardless of the modulation technique selected. This adaptive modulation technique may also have application in UHF mobile and satellite communication systems.

Figure 5.12 shows the P(e) performance of BPSK and QPSK as a function of energy per symbol-to-noise density (E_S/N_0) ratio. Since the performance of BPSK and QPSK in an AWGN and interference environment is well established [40,

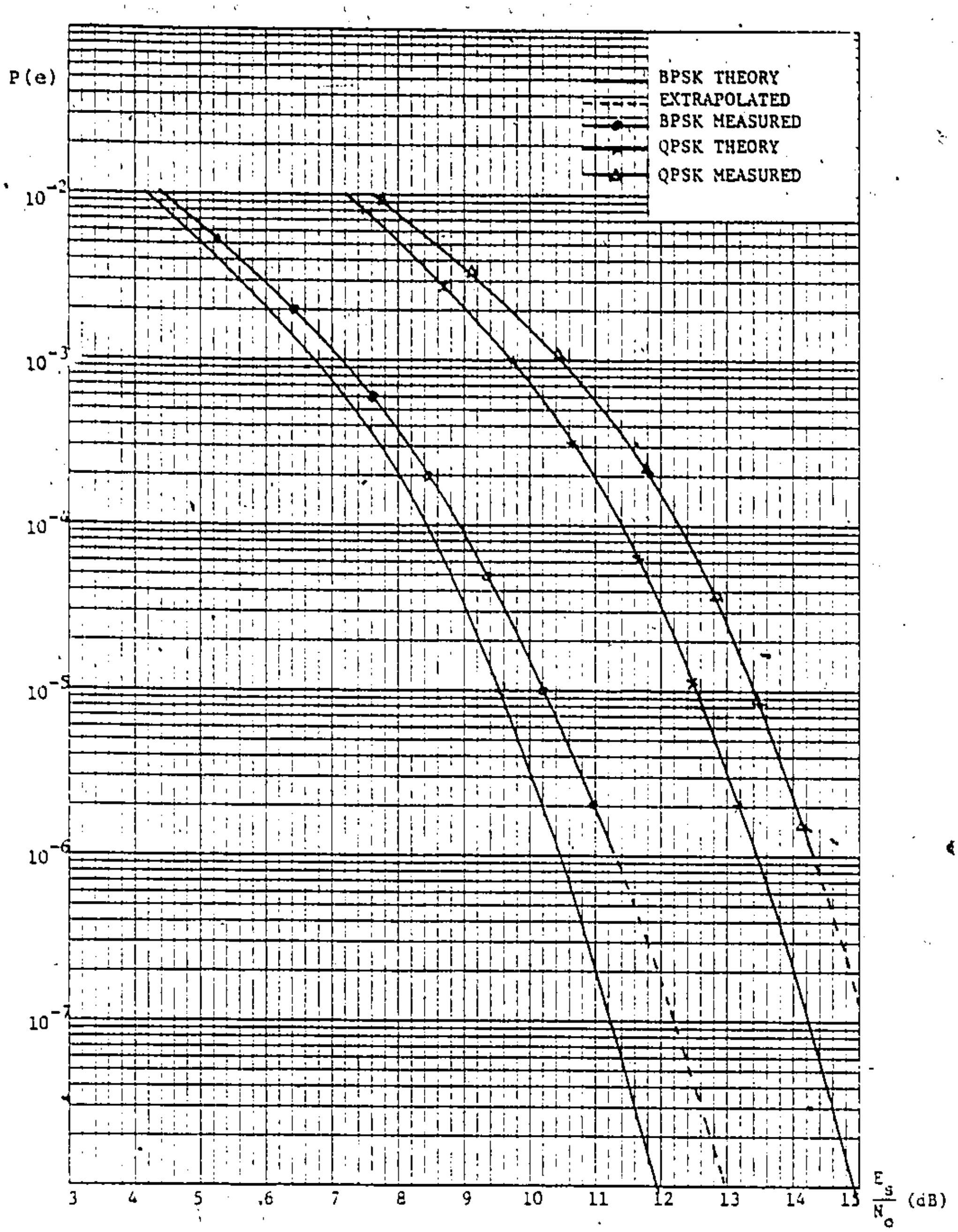


Figure 5.12 - Performance of the Modem in the BPSK and QPSK Mode while Perturbed by AWGN

41], there will be no further elaboration on these here. However, Figure 5.12 indicates that the performance of the modem in both these modes is less than 1 dB away from theory. Figure 5.13 shows the 16-APK modem with associated measurement equipment. Figure 5.14 shows a typical control card hardware found in the modulator.

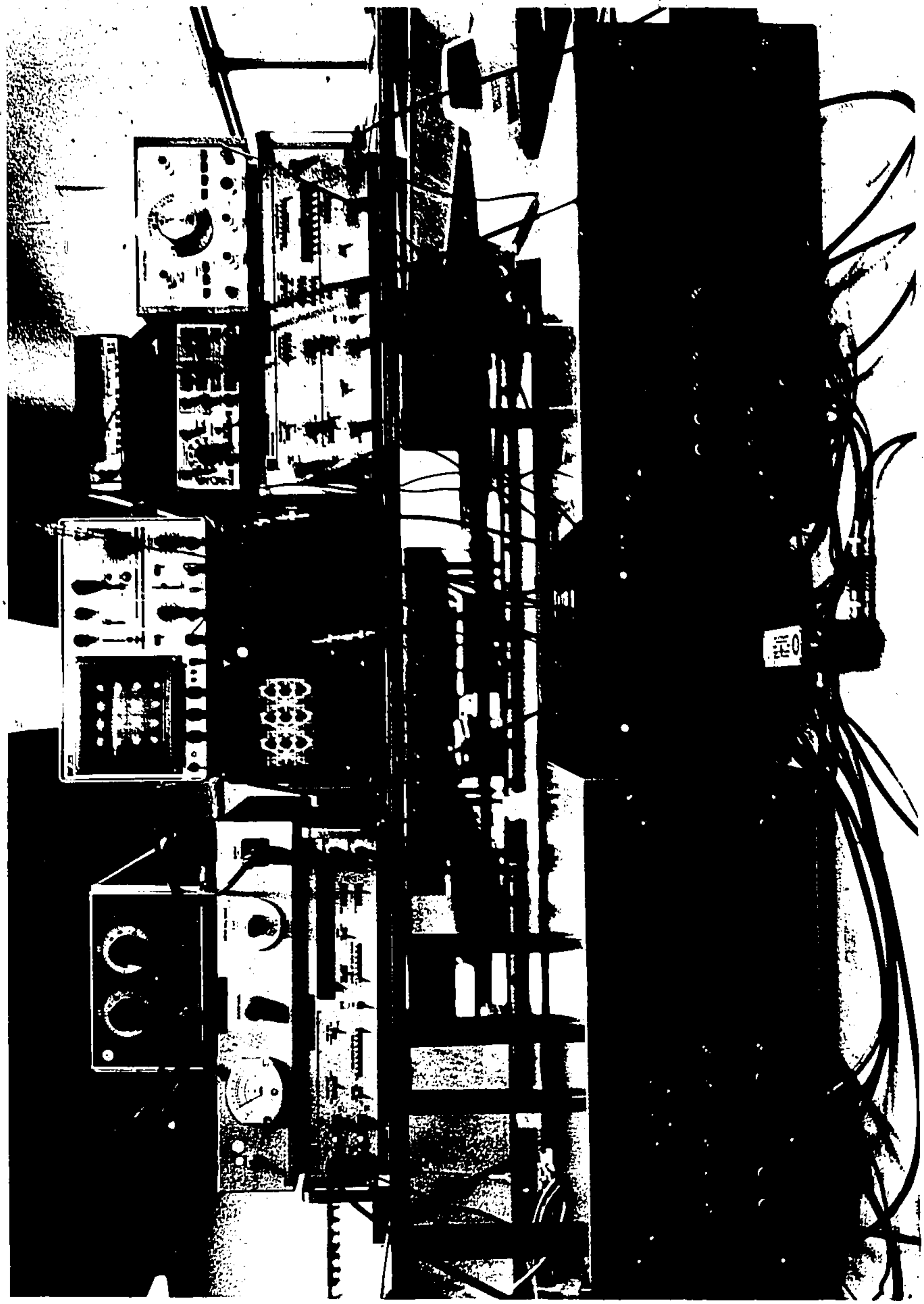


Figure 5.13 - 16-APK Modem Hardware and Test Equipment

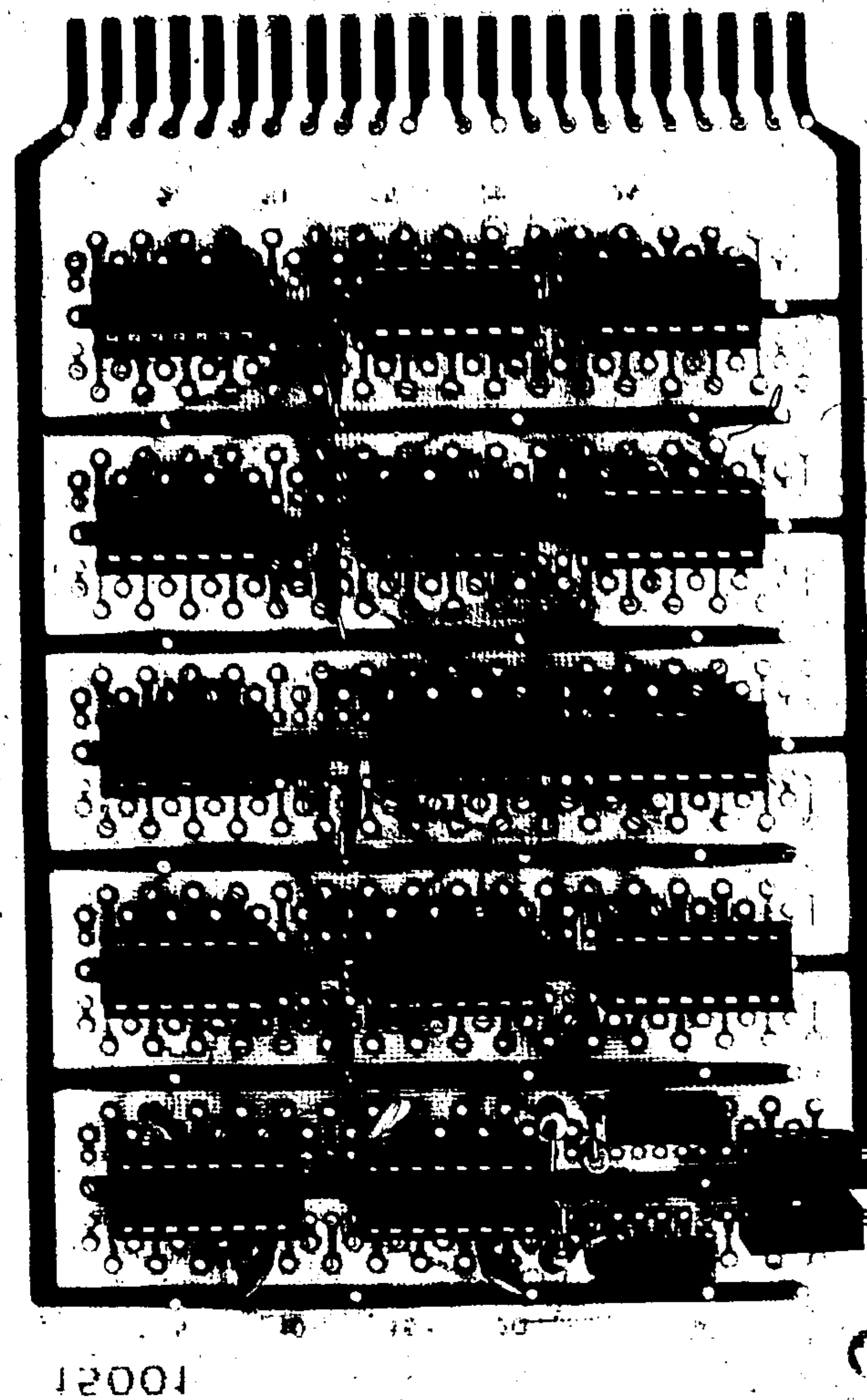


Figure 5.14 - Typical Control Card Hardware

CHAPTER VI

CONCLUSIONS AND RECOMMENDED FUTURE RESEARCH

Hybrid modulation schemes are beginning to gain wide acceptance as the modulation scheme of the future. This is because of the increased demand for communication facilities which invariably must operate at higher speed in order to meet customer traffic requirement. These demands, whether met by transmission over cable, satellite, or microwave transmission facilities result in the reduction of available bandwidth and increase the possibility of adjacent channel interference. Under adverse propagation conditions, the system performance may degrade below the threshold probability of error causing system failure. With these points in mind an experimental research program including the design and implementation of a modem employing a hybrid 16-APK modulation scheme was carried out. This scheme was chosen over similar modulation schemes such as 16-PSK which yield a theoretical 4 b/s/Hz because of the superior probability of error performance with respect to signal to noise ratio requirements, coupled with its relative ease of implementation. The implementation of this scheme employed premodulation filtering to shape the signal spectrum and post detection filtering to limit the noise bandwidth. The spectral efficiency obtained with this filtering was 3.28 b/s/Hz at the 25 dB attenuation point.

To make the system remain functional under poor propagation conditions the modem was made quasi universal by including in addition to the 16-APK mode of operation, modes such as BPSK and QPSK. The technological advantage of this feature which enables a change in modulation technique from APK to QPSK or BPSK becomes apparent when propagation condition become too poor to maintain the threshold P(e) in the APK mode.

The evaluation of its P(e) performance in the presence of AWGN, sinusoidal, adjacent and co-channel interference was carried out while the system was operating in the 16-APK mode. The results of the evaluation indicate that the C/N ratio degradation (hence P(e)) is strongly dependent on the peak factor of the interferer. Severe degradation in performance which exceeded the Javed et al. upper bound for CIR=30 dB below the threshold P(e) of 10^{-4} was experienced for the cases of three sinusoidals and co-channel interference where the peak factor exceeds 7 dB. For the other interferers studied where the peak factor was less than 3 dB this bound was found to be loose enough. For the theoretical upper bound corresponding to CIR=25 dB all experimental results were within that limit. Thus it is apparent that these bounds can be violated if the intefering peak factor is high enough.

The performance in the presence of interference validates the point that better performance is realized by a single sinusoid than with adjacent and co-channel interference assuming the same power and that the adjacent channel interferer falls within the receiver bandwidth.

At the present time, efforts are being directed towards making digital systems more spectrally efficient and to some extent more power efficient. On the former, further research can be carried out by modifying the premodulation filter to fifth order Chebyschev with say half of a dB ripple. These filters have better amplitude attenuation characteristics but worse group delay which could be compensated for by increasing the number of taps in the equalizer. The problem of power efficiency can be studied by investigating the possibility of amplifying the signal at the output of each QPSK modulator and combining after HPA thus creating an RF signal not susceptable to AM/AM and AM/PM conversion effects of the HPA amplifier. This will be useful for terrestial microwave systems.

Further experimentation is possible by changing the relative phase of the carrier between QPSK I and QPSK II in the modulator thus generating a circular symetric two level signal state rather than rectangular signal state space as is presently used. This may result in a signal which is more robust with respect to nonlinear amplification. Additionally, studies can be carried out on the effects of offset-keyed 16-APK which may also result in improved spectral performance under conditions of nonlinear amplification. Another topic for additional research could be to investigate the use of some predistortion network which would transform the signals such that when transmitted through cascaded nonlinearities, the received signal is rendered undistorted. This would make 16-APK a more attractive modulation technique for satellite systems.

The results obtained in this study have been encouraging and indicate that 16-APK is a viable modulation technique to help in the alleviation of problems associated with spectral congestion and adjacent channel interference. It is hoped that these results will motivate industry to more readily accept this modulation method and to investigate some of the topics suggested as an extension to this work.

APPENDIX A

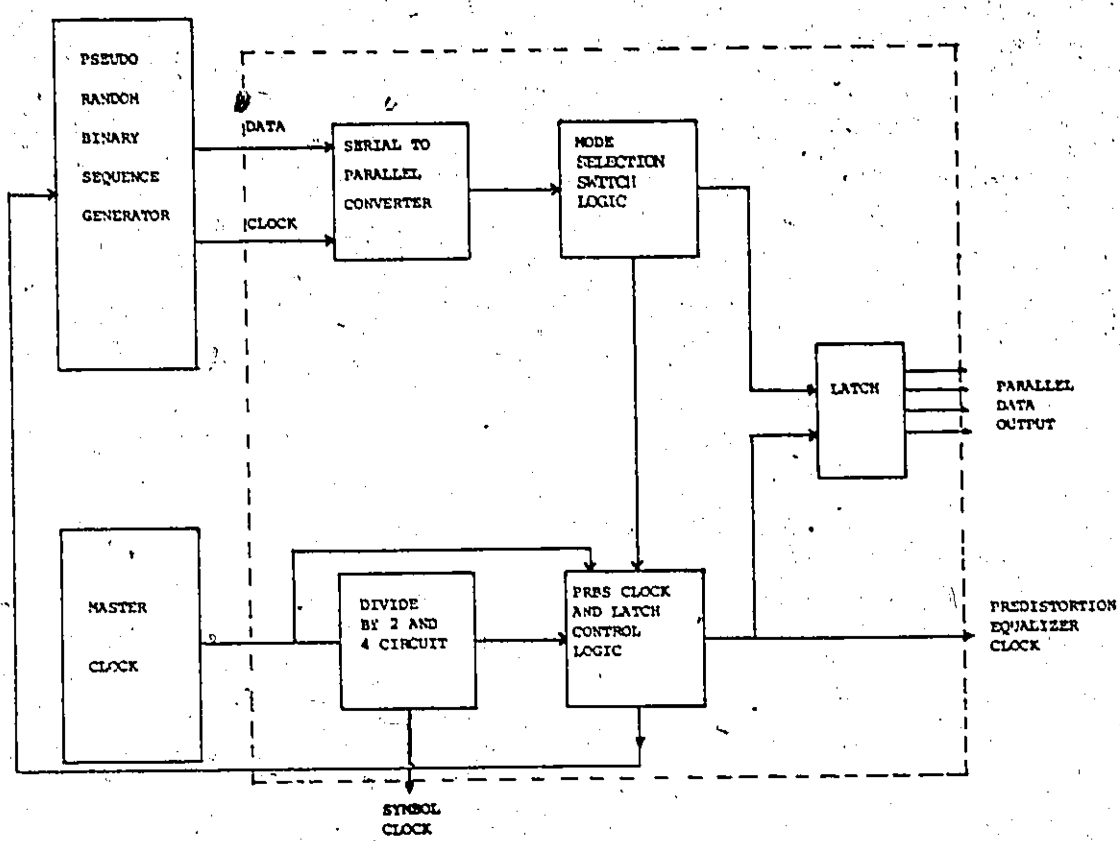


Fig. A.1 - Serial to Parallel Converter & Mode Control Logic - Block Diagram

To describe the operation of this circuit, let's assume for a moment that the modem is required to operate at a bit rate at 256 kb/s in the APK mode. The only initial conditions is that the master clock is set at a rate of 256 kHz which remains fixed regardless of the mode of operation selected and that the PRBS are properly connected as shown in

Figure A.1. By setting the appropriate mode control switches on the front pannel of the modem, the mode control switch logic is activated. This changes two conditions in the circuit (refer to Figure A.3). First it switches the four

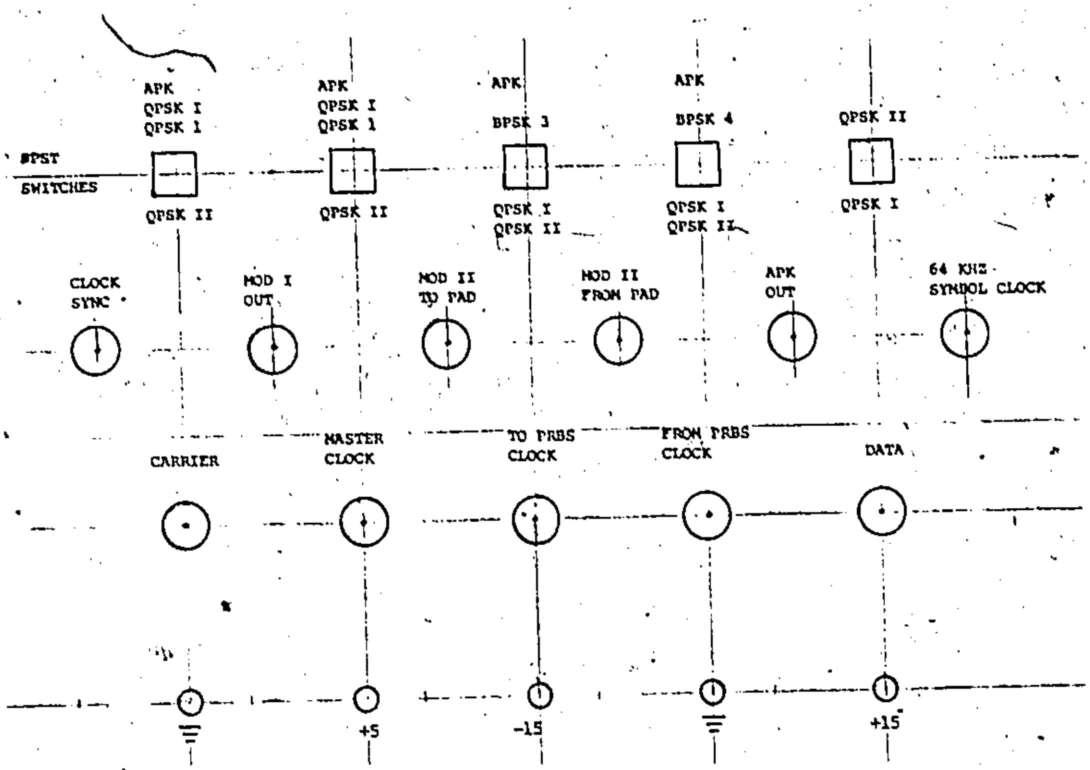


Fig. A.2 - Front Pannel of Modulator

outputs of the serial to parallel converter to the input of the latch. Secondly, it causes the PRBS clock and latch control logic to send a clocking signal to the PRBS clock input at a rate of 256 kHz. This causes the PRBS to send data to the serial to parallel converter at a rate of 256 kb/s and also a 256 kb/s clock is sent from its clock output to clock the incoming data into the serial to parallel converter. In addition to the 256 kb/s clock sent from the PRBS clock and latch control logic a fixed latch clock of 64 kb/s is sent continuously to the latch. This clock is narrower than the baud rate clock to allow time for all four parallel data sterams to arrive at the latch. (This will be shown in the timing diagram). When all four bits of data have arrived at the latch, the latch clock enables the latch thus passing the parallel data through to the predistortion equalizers in synchronism (Figure 3.1). Now, these four parallel bit streams used in APK are used to produce two QPSK or four BPSK modulators. In the case of QPSK operation, the desired channel is selected by the mode control switch logic which also cause the PRBS clock and logic to clock the PRBS at a rate of 128 KHz. This corresponds to two parallel data streams from the PRBS at a baud rate of 64 kbaud. Similarly, any one of four BPSK channels can be selected by appropriate switching. The PRBS clock and latch control logic sends a 64 kHz clock to the PRBS and 64 kbaud BPSK data results.

The details of the serial to parallel converter and mode control logic are shown in Figure A.3. From this figure, it is seen that the circuit is divided into three parts namely:

mode selection switch logic

mode select switch decoder logic

PRBS latch baud rate and equalizer clock logic

The mode selection switch logic enables data transfer from the serial to parallel converter through any one of four paths, path one and two or three and four, or all four data paths when BPSK, QPSK or APK modes are selected respectively. To realize this operation five switches are used and mode selection is made according to the boolean expressions.

$$BPSK = A + B + C + D$$

$$QPSK = (A.B) + E$$

$$APK = A.B.C.D.$$

These operations are shown in Table A.1.

Table A.1

MODE SELECTION SWITCH OPERATION

Switch					Mode
A	B	C	D	E	Selected
1	0	0	0	0	BPSK 1
0	1	0	0	0	BPSK 2
0	0	1	0	0	BPSK 3
0	0	0	1	0	BPSK 4
1	1	0	0	0	QPSK I
0	0	0	0	1	QPSK II
1	1	1	1	1	APK

As explained above, the PRBS receives a 64, 128 and 256 KHz clock when the modem is operating in the BPSK, QPSK and APK modes respectively. The purpose of the mode selection switch decoder logic is to detect which mode has been selected and to enable the appropriate bit rate clock. As shown in Figure A.3 the expressions given above are detected by gate G_1, G_2 and G_3 for BPSK, B_4, G_0 and D_3 for QPSK and H_1 for the APK mode, let A, B, C be the outputs of the BPSK, QPSK and APK decoder respectively. The outputs A, B and C of the three decoders are used to control the PRBS, latch, baud rate and equalizer (PLBE) clock generator.

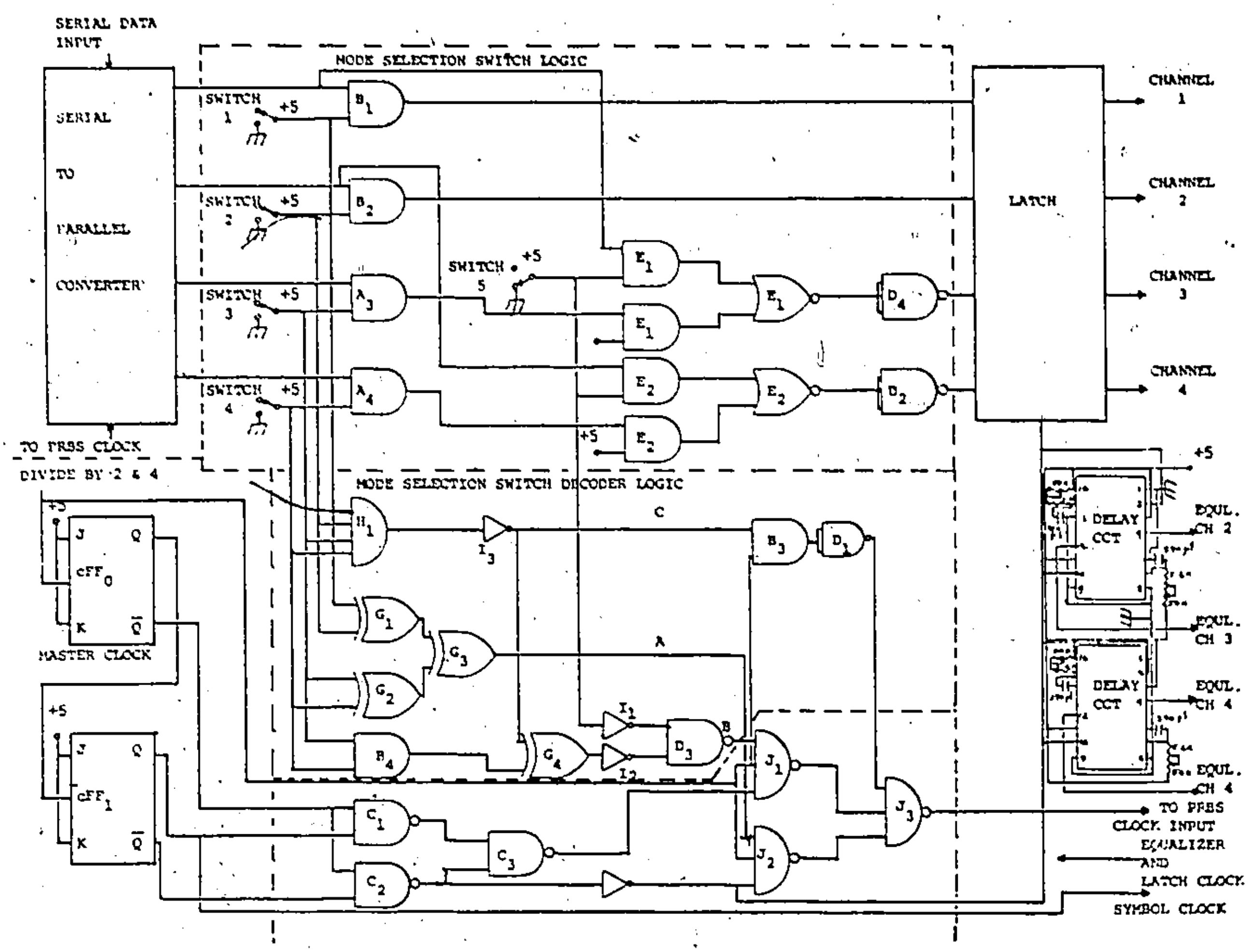


Figure A.3 - Serial to Parallel Converter and Mode Control Logic

The PLBE clock generator uses the master clock of rate 256 kHz and two flip flops to generate the timing and clocking required for the modem. The flip flops (FF) are operated as toggle FF and as shown, Q_0 of FF_0 clocks FF_1, thus, by the appropriate combination of the master clock (MC), Q_0, Q_0, Q_1, and Q_1, clock and timing generation for the PLBE is possible. The proper combinations of flip flop outputs are determined according to the number of MC pulses clocked into the FF as shown in Table A.2.

Table A.2

CLOCK SELECTION TABLE

FF_0 Q_0	FF_1 Q_1	# master clock pulses in FF_0 and FF_1
1	0	1
0	1	2
1	1	3
0	0	4

To enhance the validity of the data, the clocking and timing circuits should be independent of propagation delay. The use of the MC and flip flops in accordance with Table A.2 ensures this. The timing diagrams in Figure A.4 make this clear.

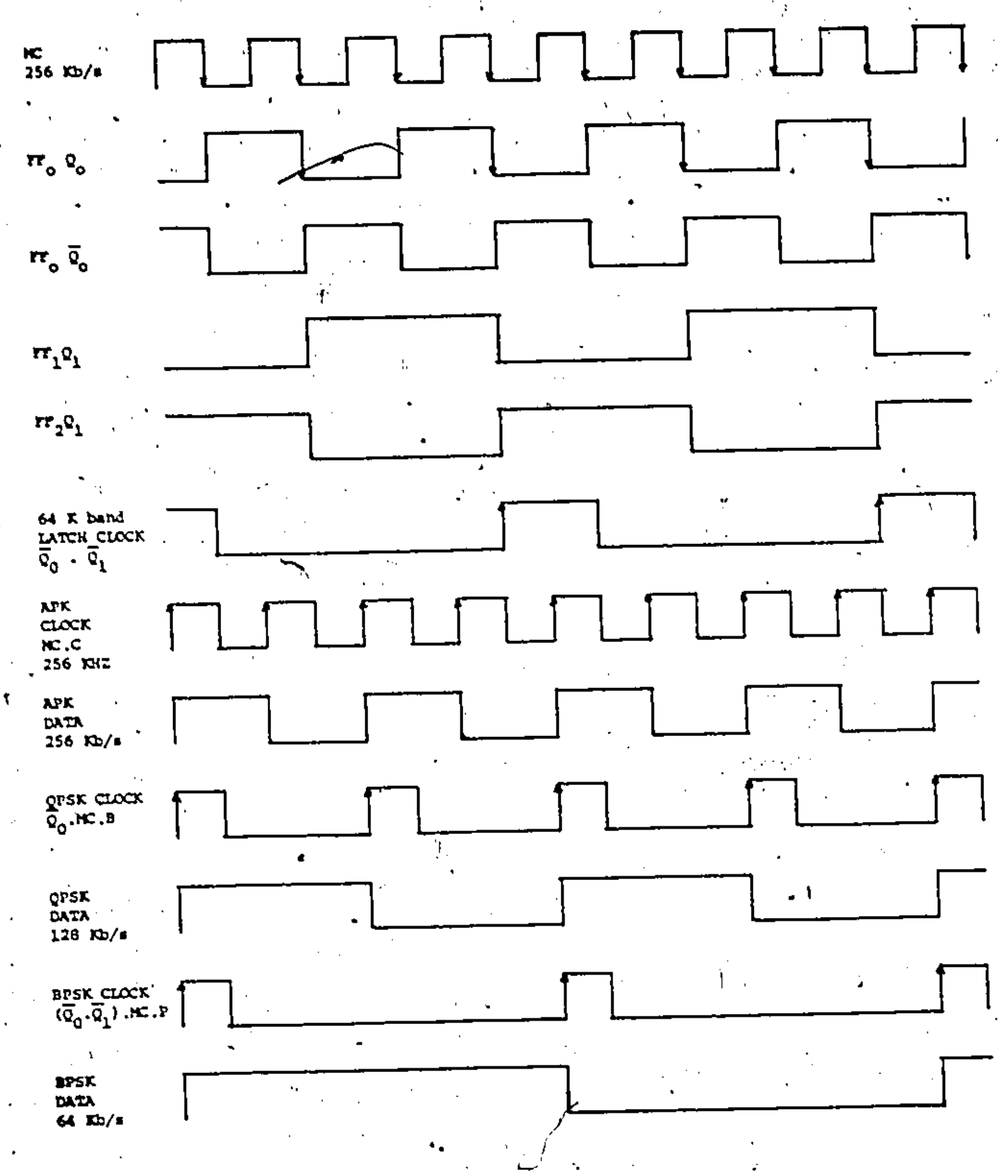


Figure A.4 - Timing Diagram for S/P Converter and Mode Control Logic

In this figure, the top six timing pulse trains are generated continuously. The bottom six pulse trains are generated in accordance with the mode in which the modem is operating. Of these bottom six trains, only two are generated in any particular mode. In the APK mode, gate B_2 (Figure A.3) provides the APK clock when MC.C (Figure A.4) are present at its input. This APK clock produces APK data (Figure A.4) at a rate of 256 Kb/s. When four serial bits are converted to parallel and have all arrived at the input to the latch, the latch pulse LC_1 clocks the data in parallel to its output on the rising edge of the LC_1 pulse. For QPSK, gate J_2 (Figure A.3) provide the QPSK clock by carrying out the operation Q.MC.B. This generates QPSK data at a rate of 128 Kb/s as shown in Figure A.4. This data is serial to parallel converted and after two clock pulses, is available at the input of the latch. LC_1 then clocks the parallel data to its output. Similarly, for the case of PBSK, gate J_2 provides the BPSK clock by performing the logical operation as follows.

$$\text{BPSK clock} = (Q_0.Q_1).MC.A$$

BPSK data at 64 Kb/s is made available at the latch input and is clocked out by the latch pulses at the same rate. For all of the above case the data available at the output of the latch is at a rate of 64 K band.

Figure A.5 shows the bread board layout, corresponding to the diagram Figure A.3.

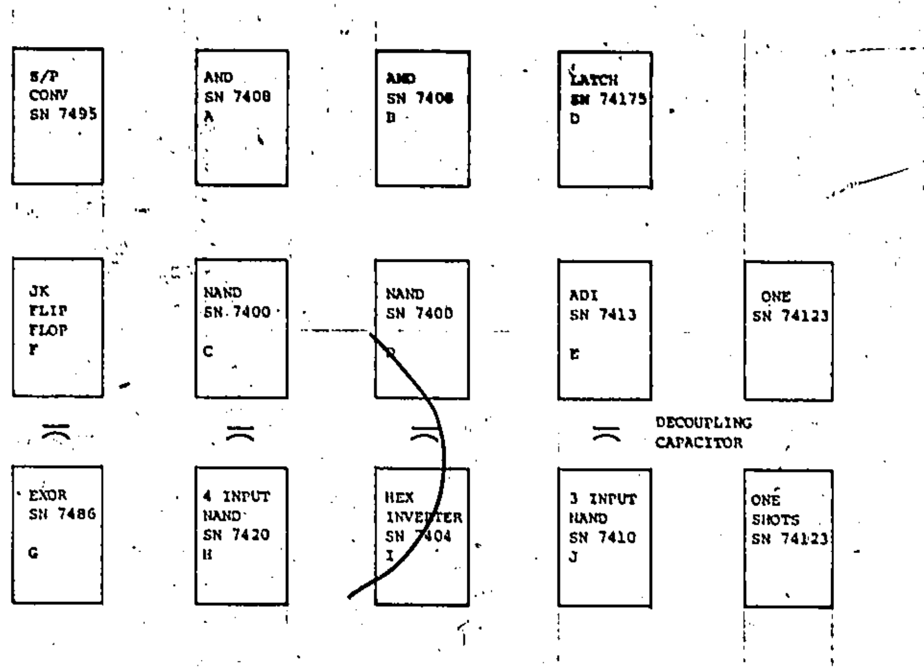


Fig. A.5 - Bread Board Layout of Serial to Parallel Converter and Mode Control Logic

In summary, the serial data stream is converted to a parallel data stream and switched selectively to the latch. PRBS clock rate of 256, 128, and 64 KHz are generated according to the mode of operation selected, thus serial data is generated at these rates. Additionally, a predistortion equalization clock, and baud rate clock rate of 256 and 128 Kb/s are generated respectively. These are the necessary pulse trains for the timing and control of the modem.

APPENDIX B

APPLICATION OF E.C.A.P. TO THE ANALYSIS OF AN ACTIVE FILTER

TABLE OF CONTENTS

Title	Page
TABLE OF FIGURES	135
LIST OF TABLES	136
ABSTRACT	137
INTRODUCTION	138
THE STANDARD-BRANCH CONCEPT	140
MODEL BUILDING	141
THE INPUT LANGUAGE	146
CONCLUSION	165
REFERENCES	169

TABLE OF FIGURES

Figure	Description	Page
1	The Standard Branch	141
2	Collector characteristics of an NPN transistor in the common emitter configuration	143
3	Base characteristics of an NPN transistor	143
4	Cutoff, active, and saturation equivalent circuit for an NPN transistor	145
5	Sample E.C.A.P. input data	147
6	Second order low pass filter	152
7	Fourth order low pass Butterworth Filter f_0=32KHz	153
8	Bode magnitude response (measured)	154
9	Bode phase response (measured)	155
10	Fairchild A715 op. amp. equivalent circuit	155
11	A715 compensated open loop response	156
12	A715 open loop response	156
13	Three stage model of A715 op. amp.	157
14	Final circuit - three stage model of A715 op. amp.	159
15	E.C.A.P. model of a 4th order Butterworth filter	160
16	Coded statements for E.C.A.P. analysis of filter	161
17	Computer generated input statements and a typical output table	162
18	Bode magnitude response (E.C.A.P. analysis)	164
19	Bode phase response (E.C.A.P. analysis)	164

LIST OF TABLES

Table	Description	Page
I	Output block indicators	150
II	Magnitude and phase data obtained from E.C.A.P. and measurement	163

ELECTRONIC CIRCUIT ANALYSIS PROGRAM (E.C.A.P.)

ABSTRACT

Fundamental principles of electronic circuit analysis program are introduced. Its requirement with respect to the modelling of the transistor and diode are discussed and its application of the analysis of a fourth order Butterworth Filter is presented. Finally, a brief comparison of laboratory and analytical results is done.

ELECTRONIC CIRCUIT ANALYSIS PROGRAM (E.C.A.P.)

INTRODUCTION

Electronic circuit analysis program is designed to assist engineers in the design and analysis of electronic circuits. The program provides the engineer with three analytical options as follows:

D.C. Analysis

A.C. Analysis

Transient Analysis

E.C.A.P. recognizes all standard electrical circuit elements, however, electronic components such as transistors and diodes have to be modelled using standard elements.

The way E.C.A.P. carries out electronic analysis on a circuit is by interpreting the input statements fed into the computer, it then determines the network topology, and generates the network equations. Following this, the computer performs the desired analysis and produces the specified output in tabular form.

E.C.A.P. allows the circuit designer to economically and efficiently examine the performance of a circuit during the different stages of design by using the computer rather than the breadboard. This is an advantage in that it eliminates the need for having costly components which may be difficult to obtain in hand during the design stages. Destructive excitation can be applied without destruction of the circuit. Difficult and time consuming measurements can be examined. Circuit connections can be changed rapidly also much better insight is gained through E.C.A.P. analysis than with a breadboard study, and finally reliability along with the effects of component tolerance on the operation circuit can be examined.

The structure of E.C.A.P. is such that it consists of four programs which are, the input language plus one program for each of the three analytical options stated above. A brief description of each of these programs follows.

The input language program provides the interface between the user and the three types of analysis. There are only six types of input statements used to completely define the circuit. These inputs specify the following:

Network topology

Circuit element values

Type of analysis desired

Type of circuit excitation

Desired output

The input statements will be discussed in greater detail later.

D.C. Analysis provides a steady state solution and gives voltages, currents, power losses, and sensitivity analysis of elements of a linear circuit.

A.C. Analysis provides a time independent solution of voltage, current, and power losses in circuit elements of a linear circuit subject to sinewave excitation at a fixed frequency. Frequency response measurements can be obtained by using a modification statement of the form $p_1\ (p_2)\ p_3$ where p_1 represents the starting frequency, p_3 the ending frequency and $p_2 = (p_3/p_1)^{\frac{1}{K-1}}$ where K is the number of steps desired over the frequency range. The steps are incremented in a logarithmic manner.

Transient analysis provides a time response of an electrical network subject to the user specified driving function. This analysis handles problems characterized by the presence of nonlinearities in the circuit configuration.

The remainder of this paper is devoted to explaining the essentials of E.C.A.P. such that the engineer will have sufficient knowledge to enable him to use E.C.A.P. An example of the application of E.C.A.P. to the analysis of a fourth order Butterworth active filter is also presented.

THE STANDARD BRANCH CONCEPT

E.C.A.P. recognizes a circuit configuration called the standard branch. This branch must contain at least one passive element and may contain a voltage source (V), an independent current source (I), and one or more dependent current sources ($\hat{I}$). The layout of a standard branch is shown in Figure 1.

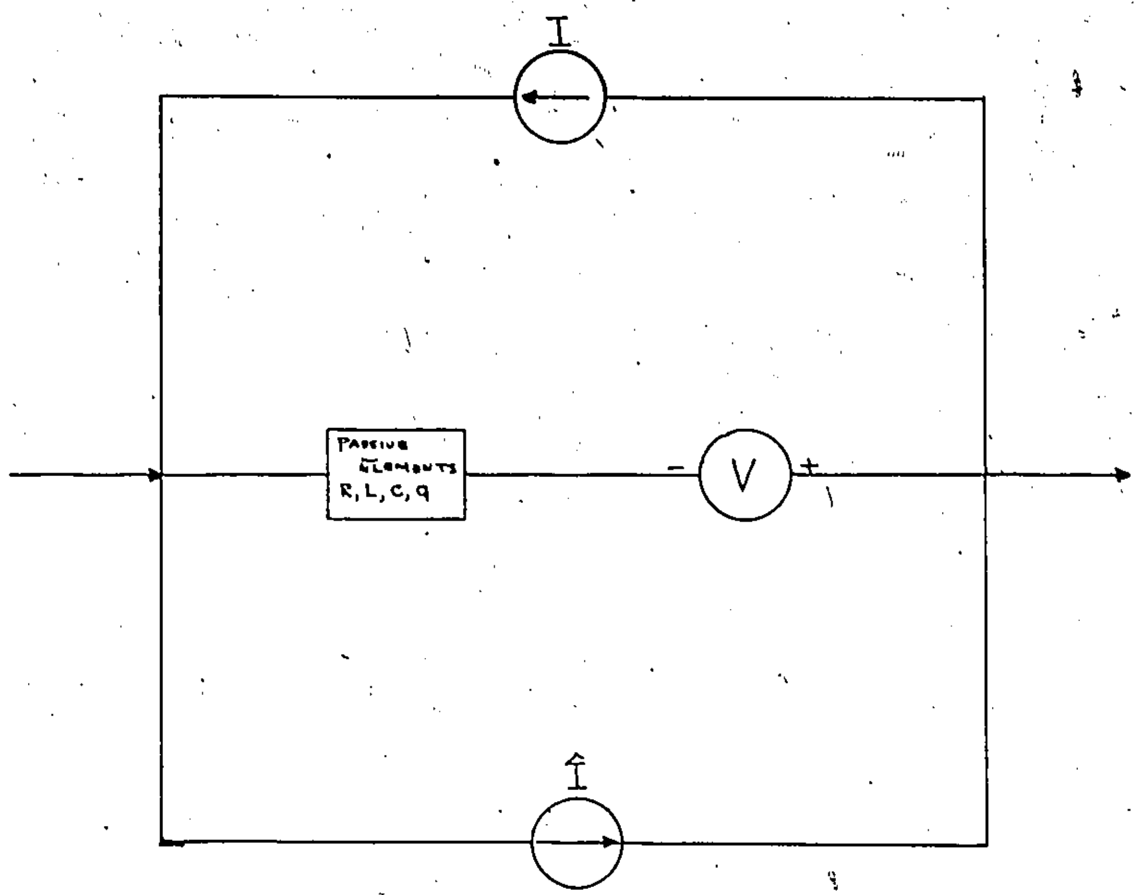


Figure 1. The Standard Branch

The program will assume that only the passive element exists in the branch if values for V, I, or Î are not specified. In D.C. Analysis, the only valid passive element is the resistor. For A.C. and transient analysis any combination of resistors, inductors, and capacitors can be used as passive elements.

MODEL BUILDING

As stated above, all electronic components must be modelled using a combination of standard elements before E.C.A.P. will recognize those devices. By looking at the voltage and current characteristics of the device, the proper combination of standard elements can be obtained to represent device.

Elementary electronic theory tells us that the transistor has three distinct modes of operation namely cut off, active and saturation. In D.C. and A.C. analysis the transistor operates in only one of these modes but in transient analysis the transistor may switch from one mode to the other as the solution progresses. The transistor model consists of 3 submodels, one for each mode of operation. E.C.A.P. uses switches to alter the circuit parameters such that the circuit is transformed from the cutoff model, to the active model, to the saturation model and vice versa in transient analysis.

Figure 2 and 3 show the collector and base characteristics of the transistor. From these it is seen that in the cutoff region the base

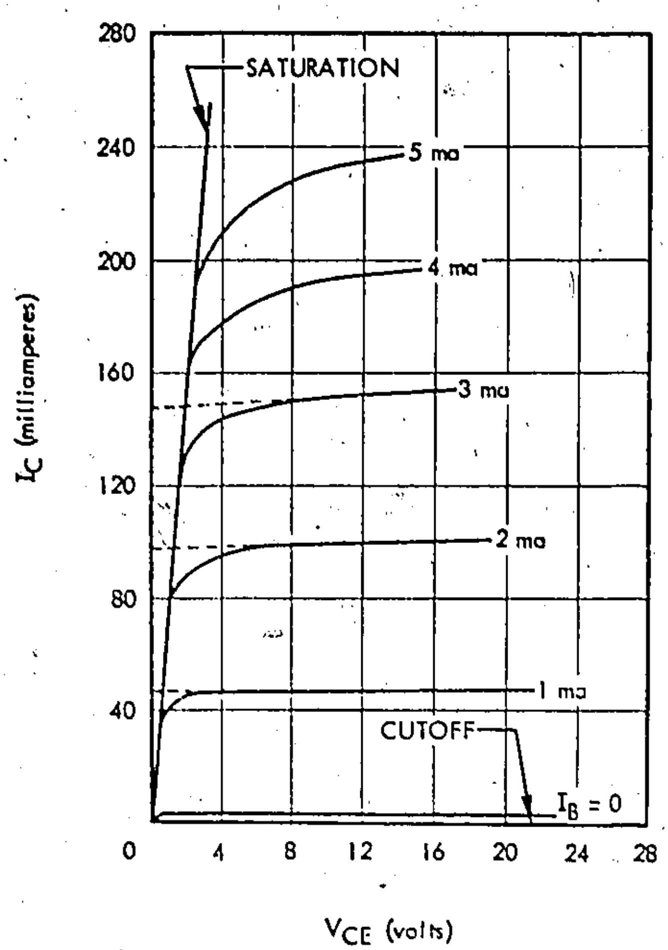


Figure 2. Collector characteristics of an NPN transistor in the common emitter configuration.

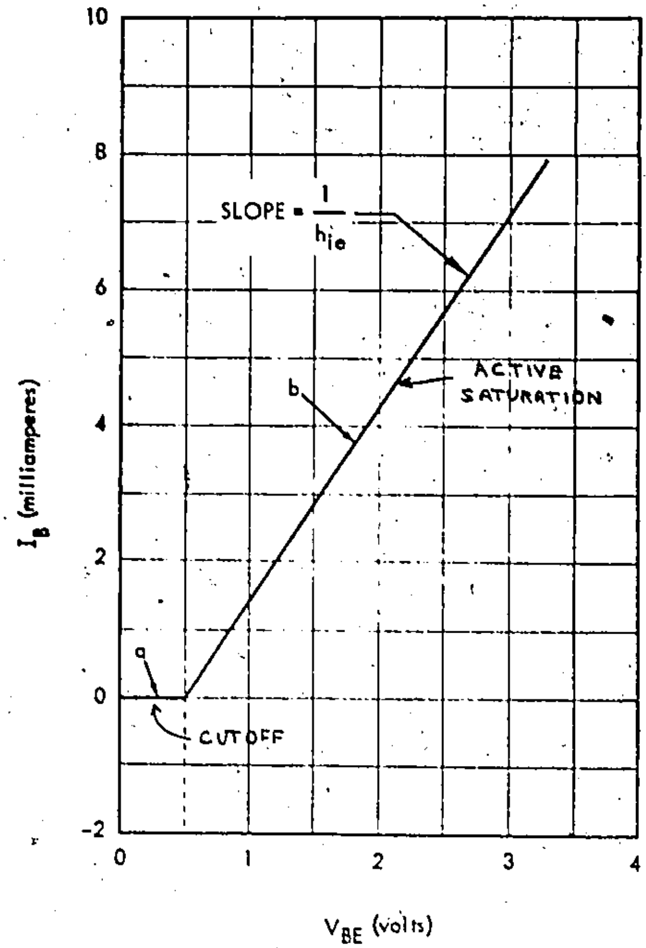


Figure 3. Base characteristics of an NPN transsistor.

current $I_B \leq 0$ so that the base emitter junction is reverse biased. As a result, there is virtually no collector or emitter current thus the desired model (as shown in Figure 4) has a very large resistor between collector and base emitter junctions.

In the active region, it is observed from Figures 2 and 3 that there is some base and collector current also there is some amplification since the base current is multiplied by the amplification factor (β) in the collector and ($1+\beta$) in the emitter. This is explicit on the collector characteristics (Figure 2) where it is observed that, for example, a 1mA base current gives 50 mA collector current and so on. By taking the collector characteristics and the positive slope of the base emitter characteristics we obtain the equivalent circuit current for the active region. The collector current in this region is given by

$$I_C = h_{FE} I_B + \frac{1}{h_{0E}} V_{CE}$$

where

$$h_{FE} = \frac{I_C}{I_B}$$

h_{0E} - slope of the collector characteristics curve.

The model for the active region is therefore represented as shown in Figure 4.

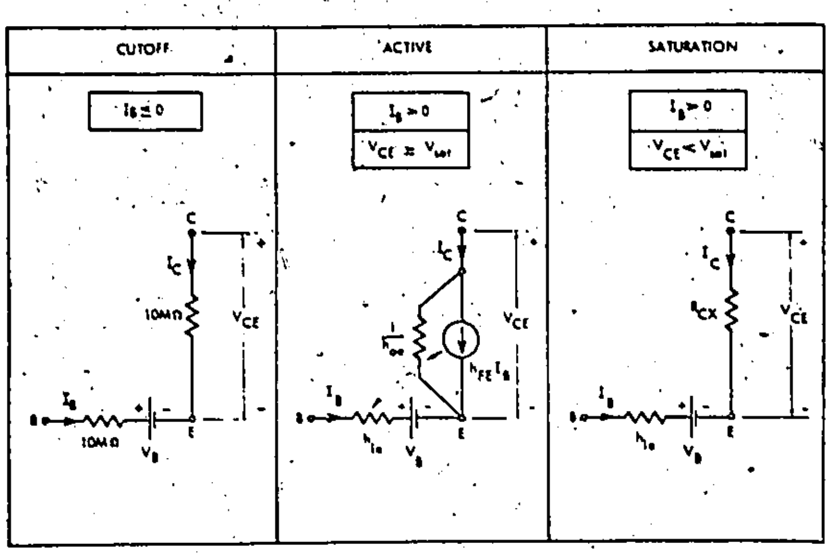


Figure 4. Cutoff, active, and saturation equivalent circuit for an NPN transistor.

To model the saturation region we remember that the base characteristics is essentially the same as it was in the active state with $V_{BE} \cong 0.6$ in series with some resistance h_{ie} which is determined from the slope of the base characteristic curve in the active region. The difference is that now the collector current is no longer a function of the base current and is given by

$$I_C = \frac{V_{CE}}{R_{CX}}$$

where $1/R_{CX}$ is the slope of the collector characteristics at saturation. The saturation model is also shown in Figure 4.

In A.C. and D.C. analyses one of the three circuits in Figure 4 are used dependent on which is appropriate. Superposition of the results from A.C. and D.C. analysis on a circuit give both A.C. and D.C. values at a particular node of the circuit.

Being aware of these models gives us the power to carry out E.C.A.P. analysis on any combination of circuits consisting of standard elements, standard branches, diodes and transistors.[1]

We are now in a position to take a look at how to make the computer do some analysis for us. To this end we study the E.C.A.P. input language.

THE INPUT LANGUAGE

For the most part the input to E.C.A.P. are punched on cards. There are as many as six different types of input statements as follows:

System Control

Comment

Command

Data

1. For modelling of additional elements see reference [1].

Solution Control

Output Specification

The general format as would be used in the analysis of a circuit is shown in Figure 5. Specification of the above six statements is all that is required to analyze a circuit. The following is a brief description of each statement.

The system control card commands the system to type out the input cards on the console typewriter if entered as in row 1, Figure 5. If

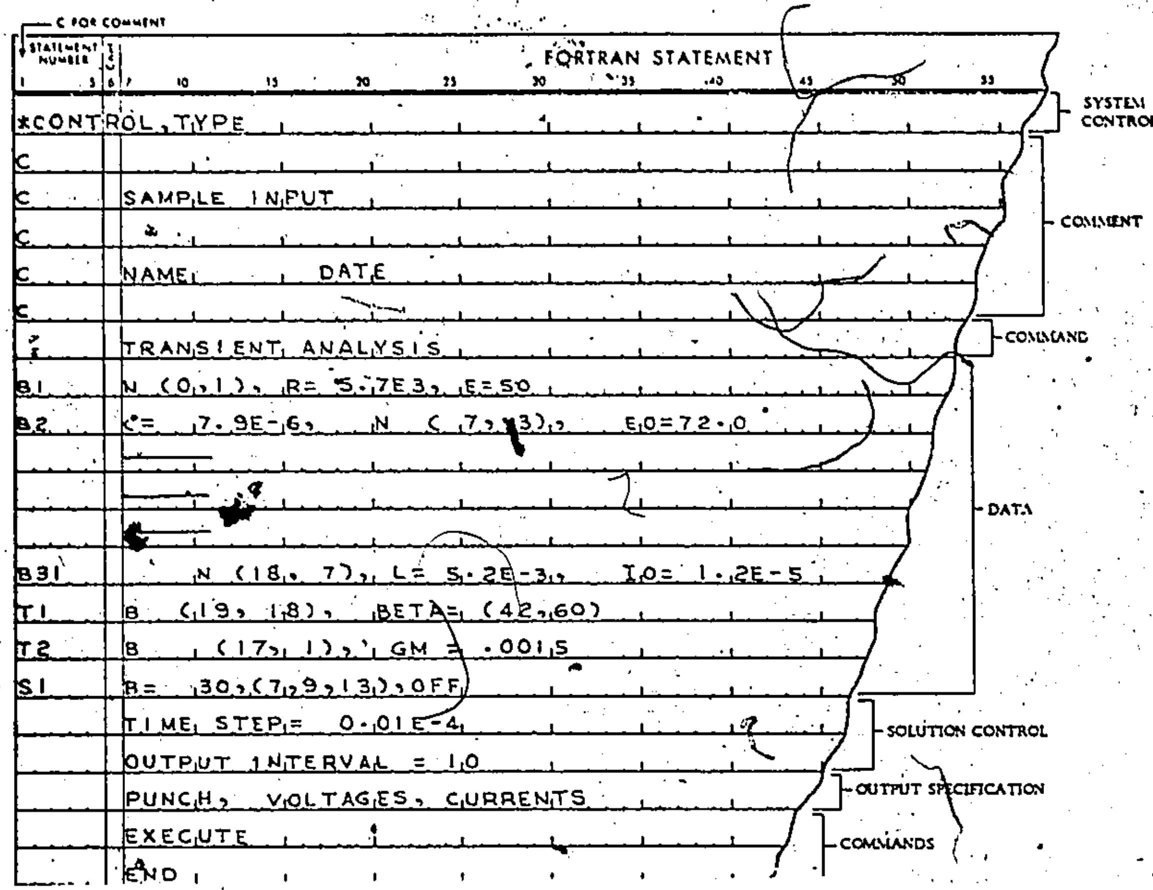


Figure 5. Sample E.C.A.P. input data.

the word TYPE is replaced or followed by a comma and the word PUNCH, the input deck will be reproduced. The word CONTROL and the asterisk must appear in columns 1 through 8.

The comment card is used to give useful information about the analysis. This is made possible by typing a C in column 1 followed by the comment in columns 2 to 72.

Command cards are used to specify the desired type of analysis (DC, AC, or transient), to request modification of a parameter, to specify the end of the job input or to establish that all E.C.A.P. jobs are finished. Command statements start in column 7 through 72 if necessary.

Data cards are the most commonly used input statement and serve to give the computer all the relevant information about the circuit. The four classifications of data cards with their references are as follows:

Data Card	References
Branch	B-card
Dependent Current Source	T-card
Mutual Inductances	M-card
Switches	S-card

Here we will only study the first two, information on the others is available in reference [25]. Each data card has two fields (a) column 1 through 5 and (b) column 7 through 72. In columns 1 through 5, the type of data card is specified such as Bxx and Txx where the xx is a serial number. Each data card of a given type must be consecutively numbered. The maximum number of B and T cards are 60 and 10 respectively. The information punched in column 7 through 72 defines the element contained in the branch in the case of the B-card and the transconductance or beta in the case of the T-cards as shown in Figure 5.

B-cards must always contain nodal information starting in column 7, being of the form $N(n_1, n_2)$, $P_1 = \ldots$, $P_2 \ldots$, where n_1 is the initial node and n_2 is the final node. The order is determined by the conversion used in the standard branch. The P_i represent the passive element or elements found between nodes n_1 and n_2. A B-card must contain at least one passive element. Branch cards may also consist of fixed voltages and/or current sources plus information about the initial voltages and current in the branches.

Each T-card must have branch data starting in column 7 of the form $B(b_1, b_2)$, $Q = \ldots$ where b_1 is the branch number of the controling branch and b_2 is the controled branch. Q is replaced by the word BETA or the letters GM representing the transconductance. These values are calculated from the circuit parameters.

Solution control cards provide data pertaining to the analysis such as FREQUENCY = 10E+06, or calculations to be made such as standard deviations. This data must be punched starting in column 1.

Output specifications command E.C.A.P. to print or type the parameter specified in the column called "output block indicator" found in Table 1. The desired output specification are punched starting in

Output Block Indicators	Description of Output	Analysis DC	AC	TR
NV or VOLTAGES	Node voltages	x	x	x
CA or CURRENTS	Element currents	x	x	x
CV	Element voltages	x	x	
BA	Branch currents	x	x	
BV	Branch voltages	x	x	
BP	Element power loss	x	x	
SE or SENSITIVITIES	Sensitivities and partial derivatives	x		
WO or WORST CASE	Worst case	x		
ST or STANDARD DEVIATION	Standard deviations	x		
MI or MISCELLANEOUS	Miscellaneous output: nodal admittance matrix, equivalent current vector, and (for DC analyses only) nodal impedance matrix	x	x	

Table I. Output block indicators.

column 7.

The above brief introduction to the input language of E.C.A.P. enables the engineer to communicate to the computer relevant information about the circuit to be analyzed. With this information, the engineer can expect to obtain some useful results.

The remainder of this paper will be devoted to an example of E.C.A.P.

analysis.

The analyses will be on a fourth order Butterworth filter designed built and tested for a 256 Kbit/sec 16-level amplitude phase shift keyed (APK) modem.

By modifying the response of an operational amplifier such that

$$A_v(s) = \frac{Av_0}{B_n(s)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

where

$Av(s)$ is the response of the circuit

Av_0 is the response gain

$B_n(s)$ is the Butterworth polynomial

it is possible to obtain a low pass filter of order n. Equation (1) can be generalized for a second order system normalyzed to

$$Av(s) = \frac{Av_0}{(RC)^2S^2 + 2k(RC)S + 1} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

where

$RC = 1/w_0$

k - dampening factor

w_0 - angular break velocity.

Considering the circuit Figure 6, with gain $Av_0 = 1 + \frac{R'}{R_1}$, it can be shown after some manipulation of arithmetic that

$$Av_0(s) = Av_0 \frac{(1/RC)}{(RC)^2S^2 + (3-Av_0)RCS + 1} \quad \ldots\ldots\ldots\ldots\ldots \quad (3)$$

comparing (2) and (3) we see that

$$RC = \frac{1}{w_0} = \frac{1}{2\pi f_0} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

$$2k = 3 - Av_0 \text{ or } Av_0 = 3 - 2k \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

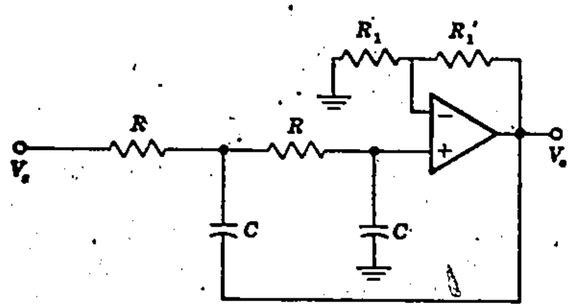


Figure 6. Second order low pass filter.

By cascading two lowpass filters using identical R's and C's and adjusting the gain Av_0 such that the coefficients of the Butterworth polynomial is satisfied, we can obtain a 4th order Butterworth filter. For a 4th order filter, the Butterworth polynomial [26] is

$$B_4(s) = (S^2 + 0.765S + 1)(S^2 + 1.8488S + 1)$$

thus it follows that we need two stages of gain. Using equation (5), the gain of the first stage is $Av_{01} = 3 - 0.765 = 2.235$ and the stage is $Av0_2 = 3 - 1.848 = 1.152$. Since $Av_0 = 1 + R'/R_1$, for the first stage $R_1' = 12k$ and $R_1 = 10k$ for the second stage $R_2' = 1.5k$ and $R_2 = 10k$.

For the required filter, $f_0 = 32KHz$.

$$RC = \frac{1}{2\pi x 32x10^3} \qquad \text{let } R = 1k\text{, then}$$

$$C = 0.0047\mu F$$

The final circuit is shown in figure 7. Also the magnitude and phase response as obtained from lab measurements for this filter are shown in Figures 8 and 9 which were plotted from the measured results in Table II.

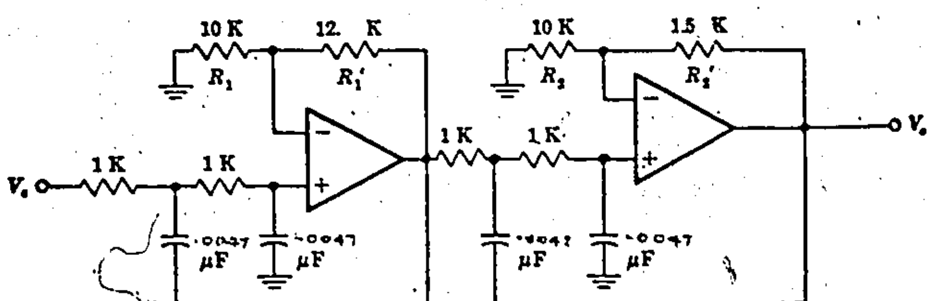


Figure 7. Fourth order low pass Butterworth Filter f_0=32KHz.

In order to carry out an E.C.A.P. analysis on this filter, it is first necessary to model the operational amplifiers. The amplifier

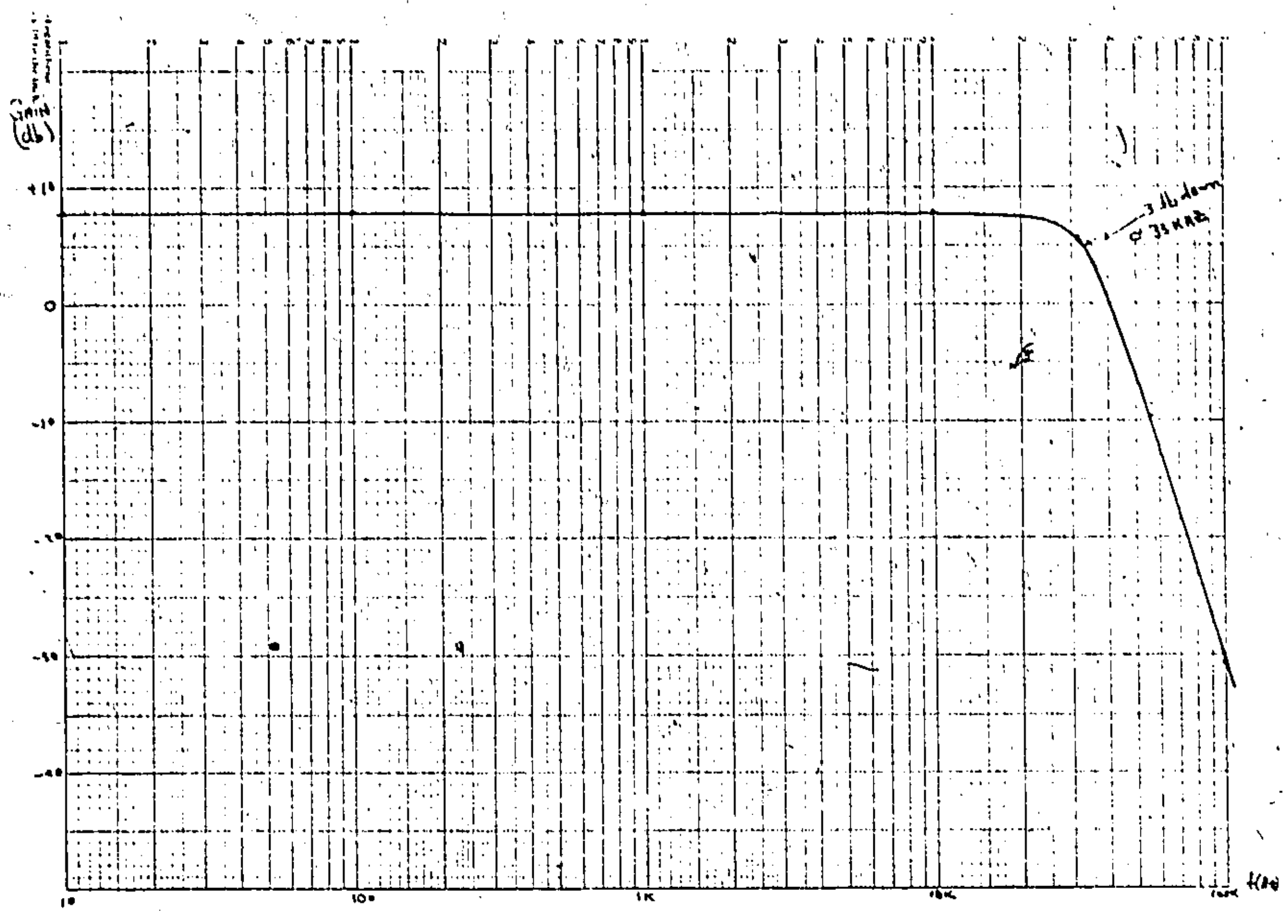


Figure 8. Bode magnitude response (measured).

under consideration here is the Fairchild µA715 whose circuit and magnitude responses are shown in Figures 10, 11, and 12 respectively. Looking at the circuit Figure 10, it becomes obvious that the modelling

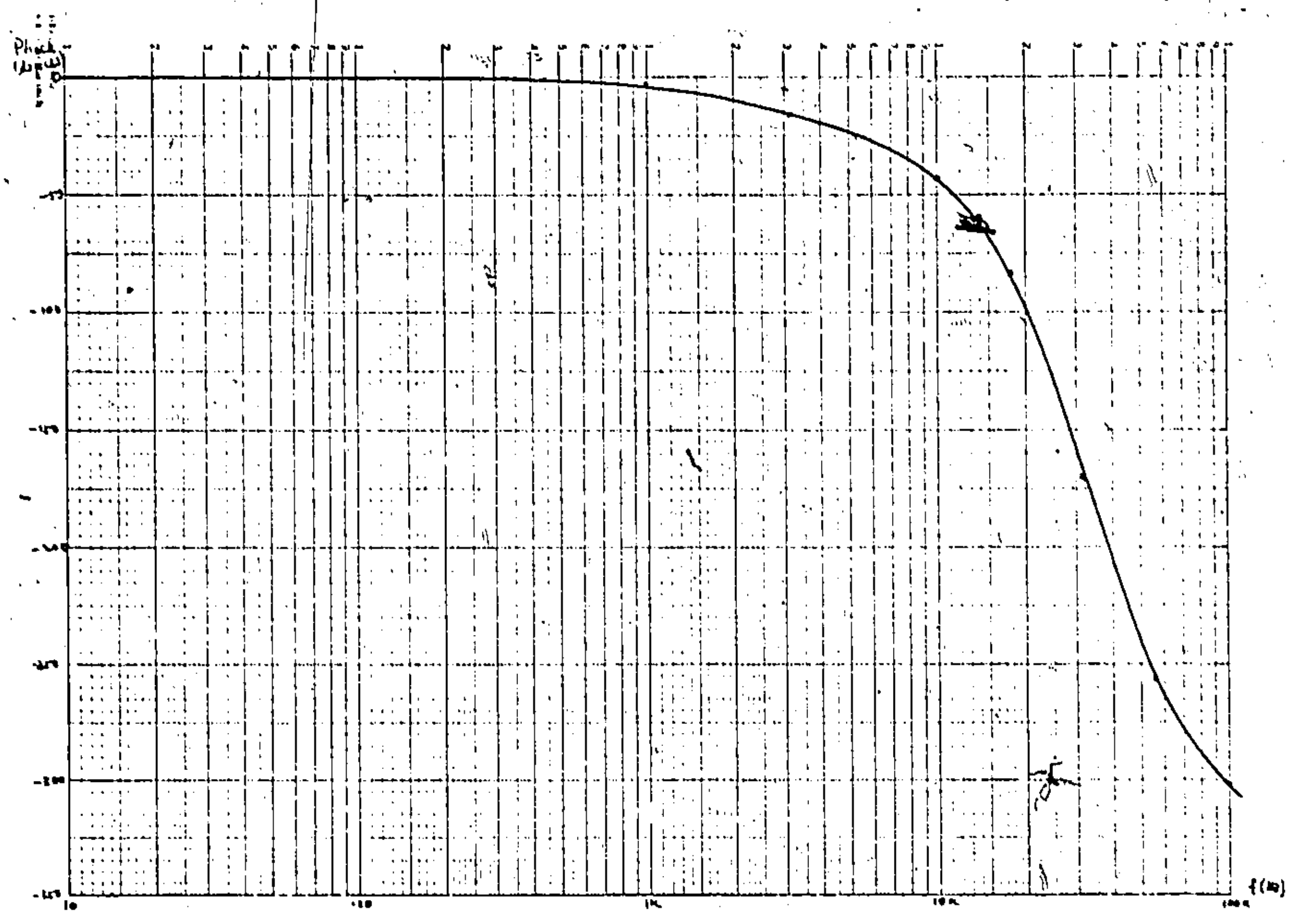


Figure 9. Bode phase response (measured).

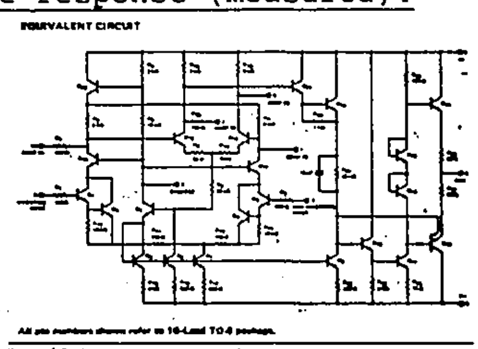


Figure 10. Fairchild μA715 Op. Amp. equivalent circuit.

of this circuit which would give us the open loop frequency response is not an easy task. A viable alternative is to observe that the filter is operating such that the amplifier is close to unity gain. With this hint we can go to the closed loop frequency response for unity gain compensation and model the amplifier from it.

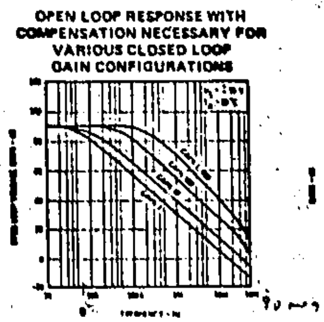


Figure 11. A715 compensated open loop response.

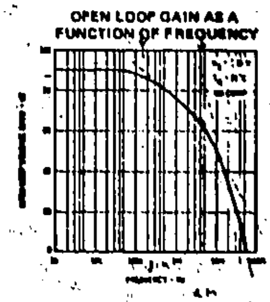


Figure 12. A715 open loop response.

Observing Figure 11, we see that the 3db point occurs at approximately 9KHz for unity gain compensation. The roll off from this point on is approximately 20db/decade and it is estimated to continue at this rate of closure until approximately 90 MHz. It is further observed that the open loop gain at low frequency is approximately 90db, also from the electrical characteristics that the input resistance is 1 MΩ and output resistance is 75Ω. Using this information we can proceed to model the operational amplifier under the conditions of unity gain compensation.

From the above, the amplifier can be represented by the transfer function

$$G(f) = \frac{Av_0}{(1+f/f_{01})(1+f/f_{02})}$$

where

Av_0 - 90db

f_{01} - 9 KHz

f_{02} - 90 MHz

Consider Figure 10 where we see that it consists of a couple of high gain stages followed by a level shifter which essentially has unity gain. This level shifter feeds into an output stage which is a buffer amplifier. This information tells us that we can use a three stage model for the amplifier as shown in Figure 13. The combination

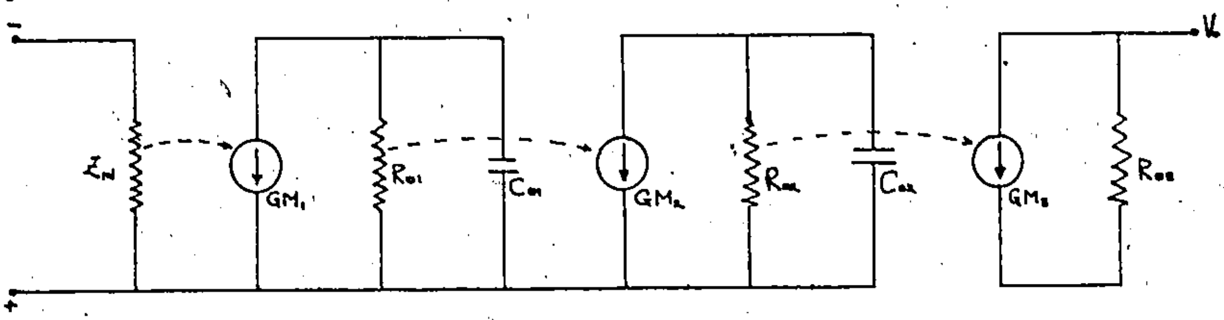


Figure 13. Three stage model of μA715 OP. Amp.

of $R_{01}C_1$ determines the first break point f_{01} = 9KHz and $R_{02}C_2$ determines the second break point at f_{02} = 90MHz. GM_1, GM_2, and GM_3 represent the transconductance of the respective stages. The following are the design calculations for the first break point:

$$\text{let } C_{01} = 1\text{nf then } R_{01} = \frac{1}{\omega_{01}C_{01}}$$

$$= \frac{1}{2\pi \times 9\times 10^{3}\times 10^{-9}}$$

for the second break point,

let $R_{02} = 17.68\text{k}\Omega$ then $C_{02} = \frac{1}{\omega_{02}R_{02}}$

$$= \frac{1}{2\pi x 90x10^{6}x17.68x10^{3}}$$

Taking a look at the transconductance we know that

$$GM = \frac{I_0}{e_{in}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

also that

$$Av = \frac{e_0}{e_{in}} = \frac{I_0R_0}{e_{in}} \text{ or } e_{in} = \frac{I_0R_0}{Av} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (7)$$

substituting (7) in (6) we get

$$GM = \frac{Av}{R_0}$$

from this we see that

$$GM_1 = \frac{Av_1}{R_{01}} = \frac{90db}{R_{01}} = \frac{31622.8}{17.68x10^3} = 1.79$$

$$GM_2 = \frac{Av_2}{R_{02}} = \frac{1}{17.68k} = 5.66x10^{-5}$$

$$GM_3 = \frac{Av_3}{R_{03}} = \frac{1}{75\Omega} = 1.33x10^{-2}$$

The final circuit for the model for the op. amp. is shown in Figure 14.

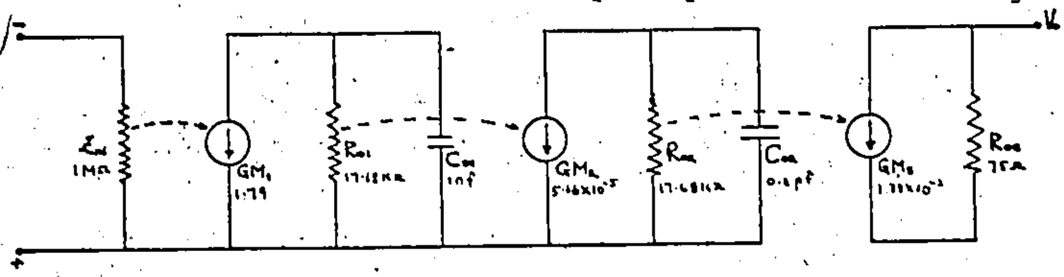


Figure 14. Final circuit - three stage model of μ A715 op. amp.

The next step is simply to replace the operational amplifiers in Figure 7 by the model in Figure 14. Doing this results in the complete model of the fourth order lowpass butterworth filter shown in Figure

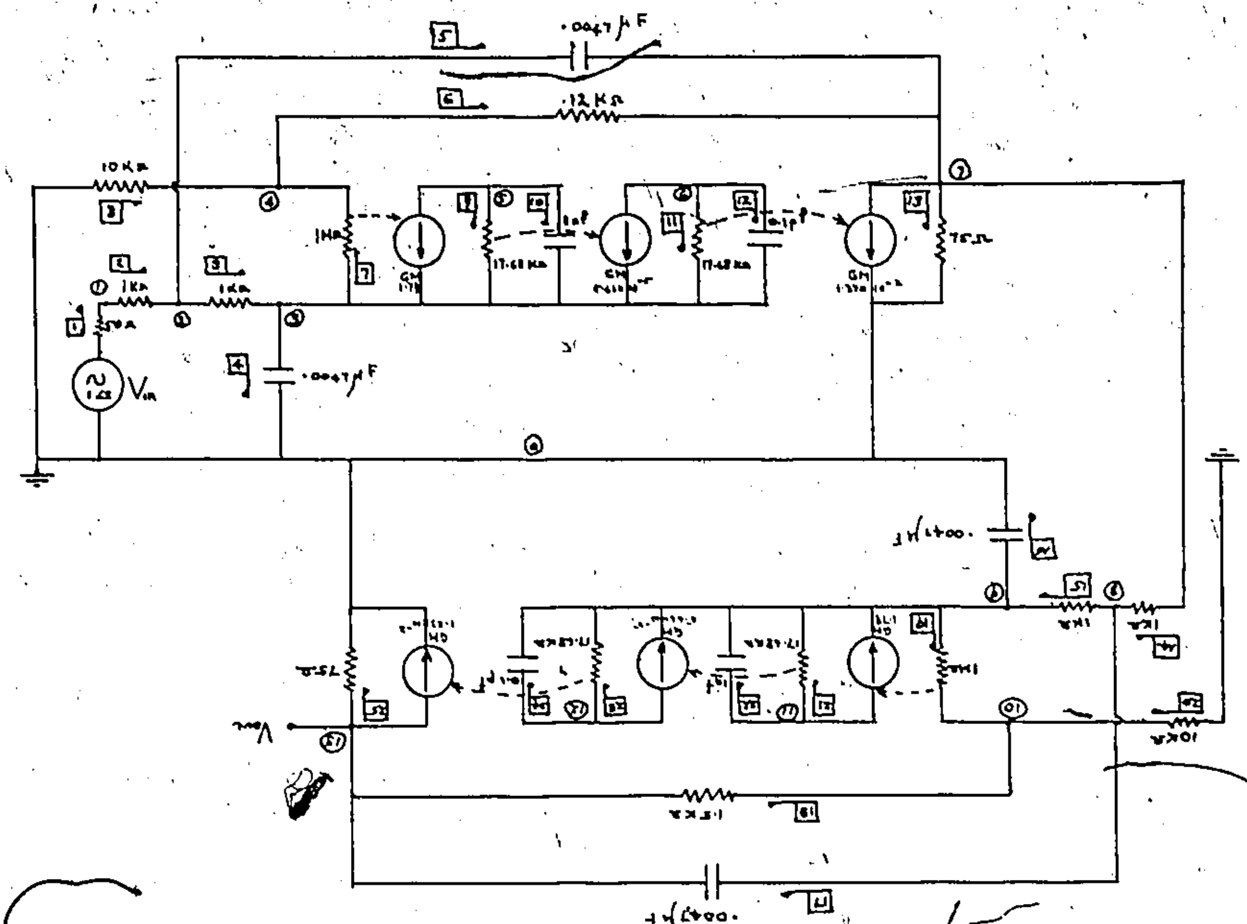


Figure 15. E.C.A.P. model of a 4th order Butterworth filter.

15. On this figure it is seen tht each node is numbered and the current direction of each branch is indicated. The arrows indicate the dependence of ~~the~~ particular current source on the branch linked by the arrow. Finally, we are now in a position to code the circuit into the language understood by E.C.A.P. as presented in the first part of this paper.

The coded statements for the model are shown in Figure 16. A typical output table is shown in Figure 17 and a table of results of the frequency response analysis as obtained from the output tables is shown in Table II.

```
//WAT01234 JOB SD06221,21,'D.PRENDERGAST',CLASS=K,
//  EXEC ECAP
//ECAP.INPUT DD *
*CONTROL PRINT
      AC ANALYSIS

   B2 N(1,2),R=1.0E+03
   B3 N(2,3),R=1.0E+03
   B4 N(3,0),C=0.047E-06
   B5 N(2,7),C=0.047E-06
   B6 N(4,7),R=12.0E+03
   B7 N(3,4),R=1.0E+06
   B8 N(0,4),R=10.0E+03
   B9 N(5,3),R=17.68E+03
  B10 N(5,3),C=1.0E-09
  B11 N(6,3),R=17.68E+03
  B12 N(6,3),C=0.1E-12
  B13 N(7,0),R=75.0
  B14 N(7,8),R=1.0E+03
  B15 N(8,9),R=1.0E+03
  B16 N(9,0),C=0.047E-06
  B17 N(8,13),C=0.047E-06
  B18 N(10,13),R=1.5E+03
  B19 N(9,10),R=1.0E+06
  B20 N(0,10),R=10.0E+03
  B21 N(11,9),R=17.68E+03
  B22 N(11,9),C=1.0E-09
  B23 N(12,9),R=17.68E+03
  B24 N(12,9),C=0.1E-12
  B25 N(13,0),R=75.0
   T1 B(7,9),GM=1.79
   T2 B(9,11),GM=[illegible]6E-05
   T3 B(11,13),GM=1.33E-02
   T4 B(19,21),GM=1.79
   T5 B(21,23),GM=5.66E-05
   T6 B(21,25),GM=[illegible]E-02
      [illegible]=20000
      PRINT,NV,
      MODIFY
      FREQUENCY=10(1.77827)1.E+06
      EXECUTE
      END
/*
```

Figure 16. Coded statements for E.C.A.P. analysis of filter.

```
 @CONTROL,PRINT

ERROR NO.  5
CARD NO.=  1   APPROXIMATE COLUMN NO. IS  2
 @CONTROL,PRINT

        AC ANALYSIS
    B1  N(0,1),R=50.0,E=1/0
    B2  N(1,2),R=1.0E+03
    B3  N(2,3),R=1.0E+03
    B4  N(3,9),C=0.0047E-06
    B5  N(3,7),C=0.0047E-06
    B6  N(4,7),R=12.0E+03
    B7  N(3,4),R=1.0E+06
    B8  N(0,4),R=10.0E+03
    B9  N(5,3),R=17.68E+03
   B10  N(5,3),C=1.0E-09
   B11  N(6,3),R=17.68E+03
   B12  N(6,3),C=0.1E-12
   B13  N(7,0),R=75.0
   B14  N(7,8),R=1.0E+03
   B15  N(8,9),R=1.0E+03
   B16  N(9,0),C=0.0047E-06
   B17  N(8,13),C=0.0047E-06
   B18  N(10,13),R=1.5E+03
   B19  N(9,10),R=1.0E+06
   B20  N(0,10),R=10.0E+03
   B21  N(11,9),R=17.68E+03
   B22  N(11,9),C=1.0E-09
   B23  N(12,9),R=17.68E+03
   B24  N(12,9),C=0.1E-12
   B25  N(13,0),R=75.0
    T1  B(7,9),GM=1.79
    T2  B(9,11),GM==5.66E-05
    T3  B(11,13),GM=1.33E-02
    T4  B(19,21),GM=1.79
    T5  B(21,23),GM=5.66E-05
    T6  B(23,25),GM=1.33E-02
        FREQUENCY=32000
        PRINT,NV
        EXECUTE

FREQ =  0.31999996E 05

        NODES            NODE VOLTAGES

MAG     1-  4   0.10192518E 01  0.18367624E 01  0.13349867E 01  0.13350601E 01
PHA            -0.32789764E 01 -0.41800583E 02 -0.85180481E 02 -0.85165070E 02

MAG     5-  8   0.44771519E 01  0.18183079E 01  0.29371328E 01  0.23072605E 01
PHA            -0.82182297E 02  0.10218869E 03 -0.85164983E 02 -0.12827788E 03

MAG     9- 12   0.16769514E 01  0.16770144E 01  0.37341652E 01  0.38206691E 00
PHA            -0.17165784E 03 -0.17164992E 03 -0.17136835E 03  0.11064524E 02

MAG    13- 13   0.19285669E 01
PHA            -0.17164992E 03
```

Figure 17. Computer generated input statements and a typical output table.

Frequency (Hz)	Gain (db) E.C.A.P. Results	Gain (db) Measured Results	Phase (degrees) E.C.A.P. Results	Phase (degrees) Measured Results
10	7.9	7.9	-0.04	-
31.6	7.9	7.9	-0.14	-
100	7.9	7.9	-0.44	-
31.6	7.9	7.9	-1.4	-
1K	7.9	7.9	-4.5	-3
3.16K	7.9	7.9	-14.5	-16
10K	7.9	7.9	-45	-43.2
17.8K	7.9	7.9	-83	-83.5
31.6K	5.9	5.8	-169	-170
32K	5.7	5.3	-171	-177
56K	-10.1	- 9.8	-264	-256
100K	-30.0	-30.6	-309	-302

Table II. Magnitude and phase data obtained from E.C.A.P. and measurement

Bode plot of magnitude and plase of the filter resulting from the E.C.A.P. analysis are shown in Figure 18 and 19.

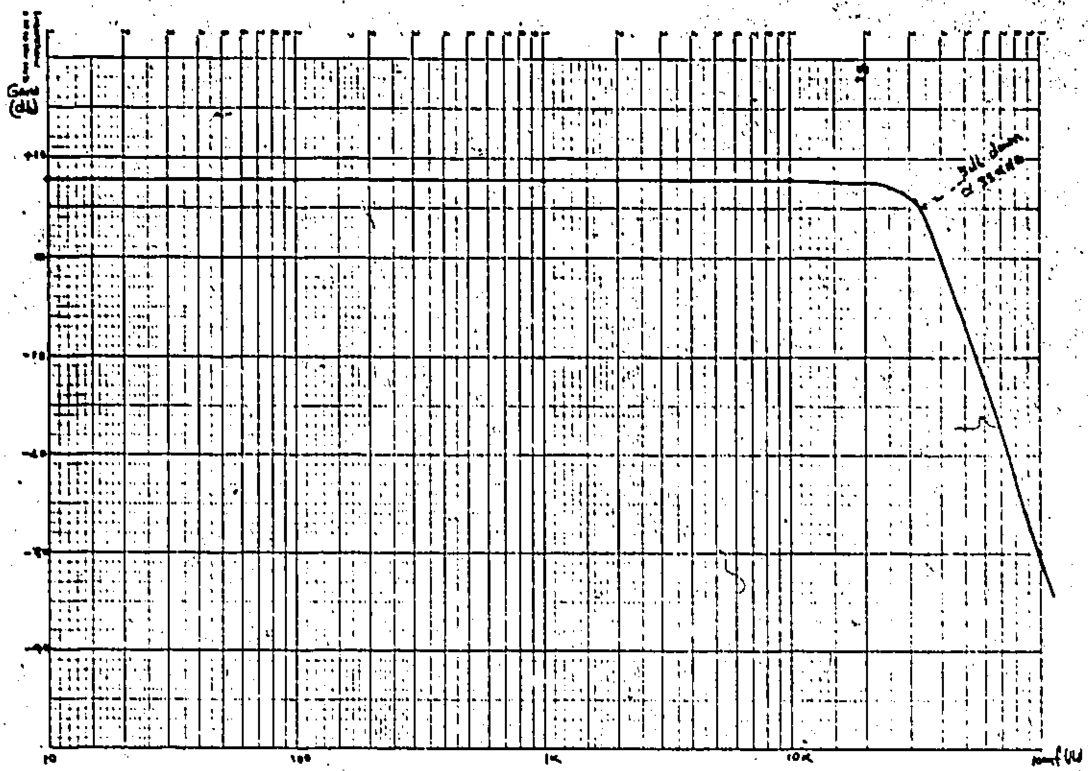


Figure 18. Bode magnitude response (E.C.A.P. analysis)

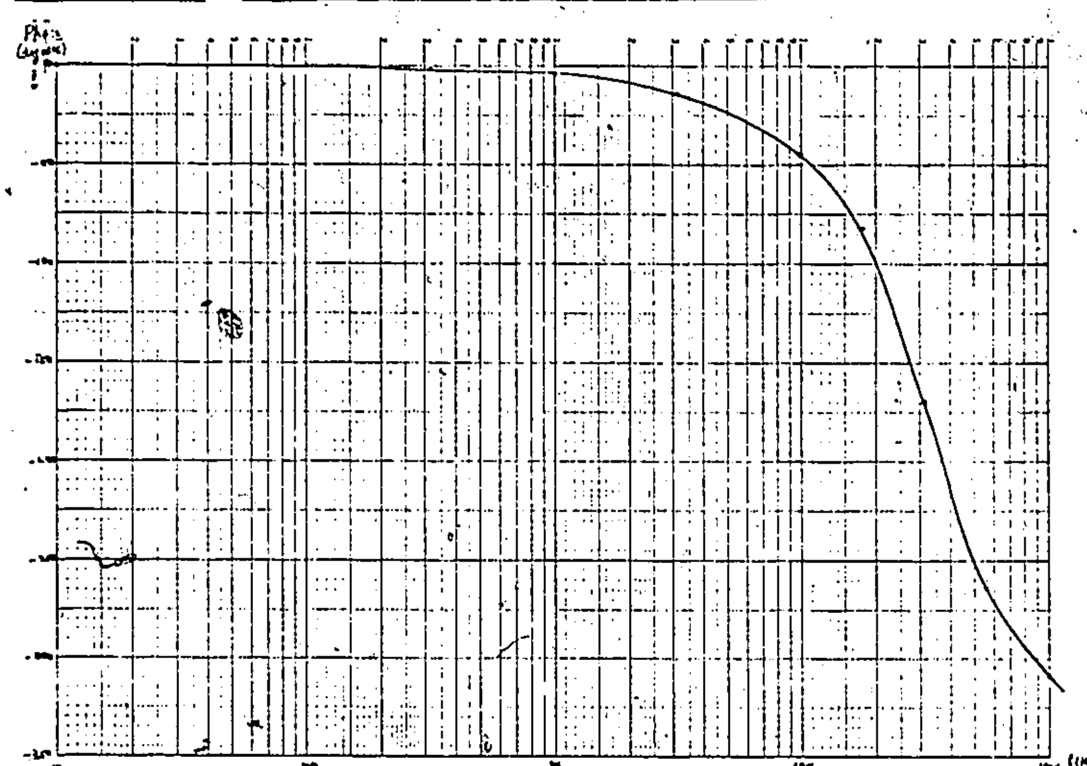


Figure 19. Bode phase response (E.C.A.P. analysis)

CONCLUSION

Comparing the results of the E.C.A.P. analysis Figures 18 and 19 with the actual laboratory analysis Figure 8 and 9 it is seen that for all practical purposes they are the same. This is indeed a clear indication of the power and versatility of E.C.A.P. analysis. Caution must be exercised in the interpretation of phase information if the results are to be meaningful. It is hoped that this paper will be of some assistance to the design engineer in the analysis of his work.

APPENDIX C

Two tone third order intermodulation distortion is measured by applying two closely spaced tones of frequency f_1 and f_2 and measuring the level of the harmonics and intermodulation products. These products will be of the form $f_c + (nf_1 + mf_2)$ and will be even when (n+m) is even, and odd when (n+m) is odd. n, m are positive intergers and f_c is the carrier frequency. The third order product pairs are most important since these are the most likely to disturb the wanted signal. This pair is of the form $f_c + (2f_2 - f_1)$ and $f_c + (2f_1 - f_2)$. The smaller the two tone third order intermod distortion, the better the mixer. As an example a mixer may be specified to be down 50 dB for two 15 dB input tones. This means that the two tone intermodulation products will be suppressed by 50 dB when two 15 dBm signals appear at the input. Conversion loss is a measure of the efficiency of the mixer in providing frequency translation between the input RF and output IF signals. The lower the conversion loss the better the mixer. Conversion compression is a measure of the maximum RF drive for which the mixer will provide linear operation. Thus for a constant LO drive, changing the RF produce a directly proportional change in RF until the RF level get to within 10 db of the LO. From then on, further increase in the RF level produces a less than direct proportional increase in IF. Mixer RF drives are specified at 1 db compression when the LO is at the manufacturers recommended drive level. The higher the conversion compression the better the mixer. Considering these factors along with the frequency of operator, the Mini Circuit MCL-SRA-3H mixer was selected for use in this modem. Now, the generation of the modulated signal can be conceptualized by studying the nonlinearity of the diodes. The equation for the modulated output signal of a conventional balanced modulator consisting of two diodes is given by [42].

$$e_0 = \underbrace{P_{\sin}\omega_m t}_{\text{Modulating Signal}} + \underbrace{Q_{\cos}(\omega_c - \omega_m)}_{\text{Lower Sideband}} - \underbrace{Q_{\cos}(\omega_c + \omega_m)t}_{\text{Upper Sideband}} \tag{3.13}$$

From (3.13) it is seen that the modelling signal is present in the output. The justification for using ring type balanced modulators as shown in Figure 3.20 is that by the addition of two extra diodes, the modulating signal as well as the other unwanted signals as shown above is also suppressed. This eliminates the need for additional filtering to remove this unwanted component. As shown in Figure 3.21 the modulated output of the mixer is passed onto the primary combiner where it is added to modulation from the Q_1 channel.

APPENDIX D

Although theoretically, the tap gains of the predistortion equilizer can be calculated and set to the required values by measurement of the tap resistances, this is by far the most cumbersome and time consuming way of tap adjustments. A more accurate (since practical components have some tolerance) is by passing a single pulse through the system, observing its points of zero crossing in the time domain and make the necessary adjustments. These adjustments ensure that the pulse response passes through zero at the sampling instant.

The first step in setting the taps is to pass the pulse from the serial to parallel converter through the predistortion equalizer. The input and output pulses are compared to ensure that they are the same sense (i.e., positive logic representation is used). If there is an inversion, the taps are adjusted until both input and output pulses are comparable.

Secondly, the pulse is allowed to go through the system (i.e. Transmitter/Receiver). The taps are then adjusted until the zero crossing as observed on the oscilloscope pass through zero at the sampling instant. This is possible since both the pulse response and the sampling clock are displayed simultaneously.

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