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A High Efficiency Power Amplifier Integrated with a Planar Transmitting Antenna

by

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ABSTRACT

In this thesis, the coplanar-waveguide-fed aperture-coupled patch antenna is studied for the purpose of integration with a high efficiency power amplifier.

A high efficiency power amplifier is designed via experimental determination of the loads required at the output of a transistor in order to maximise its efficiency. For this purpose, an active multi-harmonic load-pull system capable of independently varying the fundamental-frequency, second-harmonic-frequency and third-harmonic-frequency reflection coefficients seen at the output of a transistor is constructed. Six-port reflectometers are designed and validated for use in this application. The load-pull system's performance is also verified prior to designing the amplifier.

A power amplifier is then designed to operate at 3.5 Ghz with an input power of 4 mW. Using the load-pull system, it is found that the transistor output loads $\Gamma_{L Fo} = 0.55 \angle 39.5^{o}$, $\Gamma_{L 2Fo} = 1.0 \angle -38.8^{o}$, and $\Gamma_{L 3Fo} = 1.0 \angle 142.4^{o}$ produce a power amplifier with a gain of 7.1 dB and a PAE of 58.6%. This performance is obtained with a class B bias point. A circuit producing these optimal efficiency-enhancing loads is numerically designed. The fabricated circuit's performance is not identical to the simulated result. However, it is clear that the performance of the circuit can be tuned.

Having determined the optimal efficiency-enhancing terminations required at the output of a transistor, the design of an antenna producing these optimal efficiency-enhancing terminations is then presented. The aperture-coupled patch antenna is chosen for this purpose as it possesses many physical characteristics useful for tuning its input impedance. One active antenna is proposed where the CPW-fed slot-coupled patch is only used as a radiative element. Here, a circuit comprising of series stubs patterned inside the centre conductor of the coplanar waveguide produces the transistor's efficiency-enhancing loads A second active antenna makes use of the CPW-fed slot-coupled patch antenna not only as a radiating element, but also as an impedance element for producing the transistor's optimum efficiency-enhancing fundamental-frequency load. Here, a circuit comprising of internally patterned series stubs produces the transistor's second-harmonic and third-harmonic-frequency efficiency-enhancing loads. Numerical simulation indicates that both proposed efficiency-enhancing antenna circuits are physically realisable. Fabricated device performance differs from the numerically predicted performance. Nonetheless, the differences are not excessively significant, suggesting that these circuits can also be tuned.

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CHAPTER 1

Introduction

1.1 Research Context

Throughout the 1990's, the world has witnessed an explosion in personal telecommunication services. Wireless communication systems have been deployed throughout the globe, fuelled by the population's hunger for mobile voice and internet connectivity. In order to maximise their share of this highly competitive, multi-billion dollar market, wireless communication service providers must cater to a consumer that is demanding more compact and discreet portable communication terminals.

Two of the key components of any such portable communication terminal are the transmitter power amplifier and the antenna. The former device is critical to the communication system, as it determines the distance that a service subscriber may stray from the base station without compromising the quality of the connection. Current power amplifiers are designed to maximise the transmitted signal's power by fully exploiting available semiconductor transistor capabilities. These amplifiers are designed to operate in a non-linear regime and always constitute a major portion of the power requirement of the mobile terminal. Thus, mobile terminal producers have a vested interest in optimising the efficiency of these amplifiers. More efficient amplifiers equate to lower system power consumption. This translates directly to increased battery life and / or to a decrease in the size of the battery required to power the system. As a smaller communication handset is more attractive to the consumer, efficient amplifiers may

allow a service provider to gain a larger market share.

The antenna also impacts the roaming range of the mobile terminal. High-gain, omni-directionally radiating devices are highly sought-after, as such antennas allow for roaming in all directions around the base station. Unfortunately, antennas can often become cumbersome and aesthetically unattractive structures. Once again, the competitor offering the most attractive antenna design should realise the greatest market share.

This phenomenal market thirst for efficient amplifiers and discreet antennas has fuelled a tremendous academic research effort. In a quest to generate the most output power from an amplifier, researchers have learned to push the technological envelope of electronics to the limit. As early as the days of vacuum tube technology, it was realised that an amplifier operating in a non-linear regime produces greater output power. Theoretical investigation indicated that careful termination of harmonics generated by the non-linear amplifier produces an improvement in the device's output power and efficiency. A simple mathematical treatment showed that open-circuiting the odd-numbered harmonic signal components generated by a non-linear amplifier and short-circuiting the even-numbered harmonics optimises the amplifier's efficiency [1].

With the advent of the transistor, and as communication frequencies increased steadily, power amplifier design no longer obeyed such a simplistic formula. Complications introduced by the transformation from vacuum tube technologies to semiconductor technologies changed the rules of power amplifier design. Further problems developed due to the parasitic effects of

transistor packaging at microwave frequencies. Nonetheless, efforts continued to focus on non-linear device operation in maximising amplifier gain and efficiency. The result was the conception of new amplifier operating regimes no longer simply defined by the device's DC bias point [2, 3].

Today, a tremendous effort is deployed in an attempt to fully comprehend and optimise the operation of semiconductor amplifiers. Two main techniques are employed in doing so; computer simulation, and experimental measurement.

The speediest and commercially most attractive method is numerical simulation. This involves the generation of a model of the transistor used in the amplifier. Then, a computer simulation tool is used to design the amplifier [4 - 7]. Various device models have been developed [8 - 14], and a number of simulation methods have been devised [14 - 16]. Unfortunately, these techniques are often application-specific. For instance, one software tool combined with one specific device model may accurately predict the effect of the device's output load on the amplifier's gain. However, this same model may be incapable of predicting the efficiency of this amplifier. In addition, it is clear that the generation of a transistor model cannot be undertaken without first taking some measurements of the device. For these reasons, many engineers prefer the experimental method of amplifier optimisation.

Perhaps the most fundamental parameter affecting the gain and efficiency of a transistor amplifier is its output load. A technique known as load-pulling allows for the measurement of

amplifier gain and efficiency as a function of the device's output load. Initially, these measurements were performed entirely passively, using dielectric slugs and phase shifters to produce different reflection coefficients at the output terminal of the device-under-test [17]. As time progressed, an active load-pull system was suggested, and successfully implemented [18, 19]. Here, a phase shifter and an attenuator are used to vary the phase and the amplitude of a signal fed backward towards the output of the device-under-test, thus changing the impedance effectively observed at the terminal of the device.

In order to properly implement such an active load-pull system, an accurate means of measuring a microwave reflection coefficient is required. Traditional heterodyning network analysers are capable of performing this task [18], but they are often not suited to load-pulling applications. High-speed digital sampling oscilloscopes have been extensively analysed for the purposes of implementing reflectometers and load-pull systems [20]. Nonetheless, the most accurate, and consequently, the most academically interesting microwave reflectometer implementation remains the six-port circuit [21]. Numerous load-pull systems have been successfully implemented using six-ports [22 - 24].

As high power amplifier performance is often dependant on harmonic loading as well, multi-harmonic load-pull systems were designed [25 - 31]. These systems allow for the optimisation of the gain and efficiency of amplifiers through multi-harmonic loading [28 - 31]. Later, systems capable of measuring high frequency waveforms in the time domain established the link between the multi-harmonic loading of amplifiers and their operating efficiency [32 -

34].

These technological advances in microwave metrology and active device characterisation are also fuelling research in the area of passive microwave circuit design. Having determined the efficiency-optimising or gain-optimising reflection coefficients to be presented at the output of a transistor, a circuit must then be implemented to finalise the amplifier design. Filter design methodologies and standard impedance transformation techniques can be applied to implement such circuits. Nonetheless, some researchers are striving to develop new passive circuit design methodologies, such as photonic band-gap structures, that can be applied to the design of power amplifier loading networks [35 - 39].

Furthermore, other researchers have produced antennas to realise the efficiency-optimising reflection coefficients at the fundamental frequency of operation and at the harmonic frequencies [38 - 47]. This idea is of tremendous commercial interest, as the resulting circuits are more compact than the traditional amplifier / antenna cascade. Thus, the use of active antennas in wireless handsets can result in a more aesthetically pleasing product, providing the manufacturer with a marketing advantage.

A wide variety of novel antennas have already been used in active antenna implementations. Nonetheless, an even larger number of antennas have characteristics rendering them suitable for integration in an active antenna, and relatively few of them have been adequately studied. One such antenna is the aperture-coupled patch antenna. This specific

device is commercially attractive, as it is a discreet planar radiating structure. Furthermore, if coplanar waveguide is used for implementation of the antenna's feed circuit, an active antenna can be constructed on a single substrate. Finally, the aperture-coupled patch antenna is suitable for multi-harmonic power amplifier loading, as a significant number of its physical features can be altered in order to tune its input impedance while only slightly compromising its radiation characteristics [48 - 50].

1.2 Research Objectives

The purpose of this thesis is to produce a highly efficient power amplifier integrated with a compact, planar antenna.

First, a load-pull system is implemented using six-port reflectometers. This system is capable of measuring the power-added-efficiency and the gain of a transistor as a function of the load seen at its output at the fundamental, second-harmonic and third-harmonic frequency of operation. An Agilent ATF-26836 FET is characterised at 3.5 GHz using this tool.

Then, an antenna is designed for producing the optimal efficiency-enhancing terminations at the transistor's output. The coplanar-waveguide-fed aperture-coupled patch antenna is studied for this purpose. This specific antenna is chosen because it is compact and easily fabricated. In addition, the physical features of the aperture-coupled patch antenna can be tuned to change its input impedance while only slightly compromising its radiation characteristics.

Finally, an active antenna is constructed and its performance is studied.

1.3 Expected Research Contributions

Despite the already significant body of literature available on the integration of power amplifiers with antennas, most of the work to date presents a power amplifier designed using simulation software and a model of the device. This is the first work that is focussed on an active antenna designed using a multi-harmonic load-pull system that is capable of independently varying the load at the fundamental, second, and third harmonic frequency of operation.

Furthermore, many antennas have been studied in order to produce active integrated antennas. However, aperture-coupled patch antennas have not been very carefully studied. In addition, previous active antennas have mostly been constructed using the microstrip waveguide technology. For the first time, a coplanar-waveguide-fed aperture-coupled patch antenna is studied for the purpose of producing an active integrated antenna.

Finally, it is illustrated that the optimum efficiency-enhancing loads of a transistor can be produced using a series of coplanar waveguide stubs and the slot-coupled patch antenna. It is shown that the addition of internally-patterned stubs between the FET and the antenna can produce the optimum efficiency-enhancing loads of the transistor at the harmonic frequencies while the antenna itself produces the optimum efficiency-enhancing load at the fundamental frequency of operation.

1.4 Thesis Organisation

This thesis is subdivided into three major sections.

The first section highlights the design of a multi-harmonic load-pull system using six-ports. Chapter 2 discusses six-port reflectometer design, calibration and operation. The accuracy and the repeatability of the measurements taken with the reflectometers are compared with published data and measurements obtained with an HP-8510 network analyser. Chapter 3 presents the multi-harmonic load-pull system. Reflection coefficients measured with this device are compared with measurements obtained with an HP-8510 network analyser. Small-signal amplifier gain circles measured with this system are compared to theoretical gain circles computed using s-parameter data. The system's suitability to large-signal FET characterisation is discussed.

The second part of this thesis highlights the design of the optimally efficient amplifier. Chapter 4 highlights the design of the coplanar waveguide used in the design of the amplifier / antenna circuit. The suitability of the chosen substrate and the immunity of the waveguide to parasitic modes is discussed. The issue of coupled slot-line mode excitation in the coplanar waveguide is carefully examined. The amplifier design is also highlighted. The experimentally determined characteristics of the transistor are presented. Amplifier gain and efficiency are shown, in addition to the FET's input impedance, its input power, its output reflection coefficient at the fundamental, its fundamental output power, its output reflection coefficient at the second harmonic, and its output reflection coefficient at the third harmonic. The design of a circuit

producing the FET's efficiency-enhancing loads is presented and measured. A power amplifier is constructed and its performance is evaluated.

The third part of this document deals specifically with the antenna design. In chapter 5, an optimal coplanar-waveguide-fed aperture-coupled patch antenna radiating at 3.5 GHz is designed. Two antenna circuits producing the FET's optimal-efficiency output loads are also produced. Both circuits produce the transistor's efficiency-enhancing harmonic loads using internally patterned coplanar waveguide stubs. The first circuit uses an additional coplanar waveguide stub to produce the efficiency-enhancing load at the fundamental frequency. In the second circuit, the aperture-coupled patch antenna produces the transistor's efficiency-enhancing fundamental load directly.

Finally, chapter 6 presents the major conclusions of the study. Recommendations for future design iterations are also presented in addition to suggestions for further study.

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CHAPTER 2

Six-Port Reflectometry

2.1 Technological Background

The use of six-port circuits in the measurement of complex microwave reflection coefficients was introduced in the late 1970's [1 - 3]. The novelty of reflection coefficient measurement using six-ports lies in the fact that the complex measurement is obtained via four scalar power measurements. This feature allows for extremely accurate reflection coefficient measurements.

2.1.1. Six-Port Design

A six-port reflectometer must be properly designed to accurately measure complex reflection coefficients [4]. The device is designed such that its S-parameters define three "Q-points" in the complex Γ plane.

The specific location of these Q-points must be carefully chosen, as the accuracy of the measured reflection coefficient decreases as the unknown load approaches any of the Q-points. For this reason, the Q-points of a quality six-port are located outside the $|\Gamma| = 1$ circle. In addition, the Q-points of the six-port must not be co-linear. If this occurs, the equations relating the measured power values to the unknown reflection coefficient will be under-determined, making it impossible to solve for the measurement unknown. Ideally, the Q-points of the six-port should be located near the $|\Gamma| = 1.5$ circle and be separated by 120^{o} [1, 5].

A typical 6-port circuit designed using commercially available components is illustrated in figure 2.1. The circuit is comprised of one 6dB directional coupler (6dB), three 90^{o} hybrid couplers (Q) and one 0^{o} power divider (H).

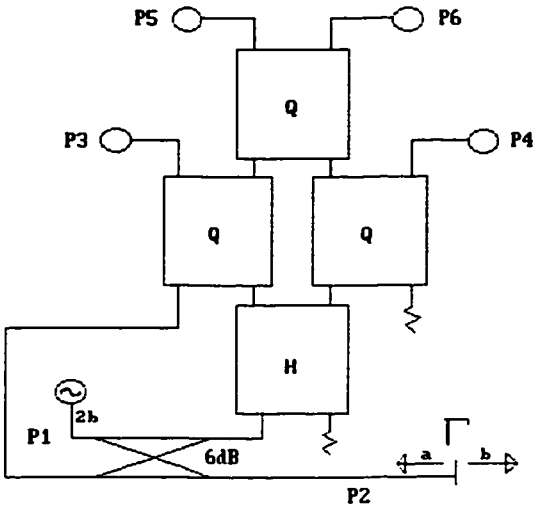

Figure 2.1 Proposed 6-port circuit

In the circuit of figure 2.1, P1 is the input of the 6-port, and P2 is the measurement port. P3, P4, P5 and P6 are connected to matched power meters. The power measured by the four matched power meters are related to the incident and reflected waves (b and a) of the load Γ as follows [1]:

$$P3 = |b_3|^2 = |S_{32} * a + S_{31} / S_{21} * b|^2 \quad (2.1a)$$

$$P4 = |b_4|^2 = |S_{42} * a + S_{41} / S_{21} * b|^2 \quad (2.1b)$$

$$P5 = |b_5|^2 = |S_{52} * a + S_{51} / S_{21} * b|^2 \quad (2.1c)$$

$$P6 = |b_6|^2 = |S_{62} * b + S_{61} / S_{21} * a|^2 \quad (2.1d)$$

Port 4 is chosen as the reference power measurement. This is accomplished by designing the six-port such that $S_{42} = 0$. The load reflection coefficient is also defined as $\Gamma = a/b$. Substitution of this expression into equation 2.1 and factoring, yields:

$$P3 = |S_{32} * b|^2 * |\Gamma + S_{31} / S_{32} / S_{21}|^2 \quad (2.2a)$$

$$P4 = |S_{41} / S_{21} * b|^2 \quad (2.2b)$$

$$P5 = |S_{52} * b|^2 * |\Gamma + S_{51} / S_{52} / S_{21}|^2 \quad (2.2c)$$

$$P6 = |S_{62} * b|^2 * |\Gamma + S_{61} / S_{62} / S_{21}|^2 \quad (2.2d)$$

From 2.2, the Q-points of the six-port are defined as:

$$Q_3 = -S_{31} / S_{32} / S_{21} \quad (2.3a)$$

$$Q_5 = -S_{51} / S_{52} / S_{21} \quad (2.3b)$$

$$Q_6 = -S_{61} / S_{62} / S_{21} \quad (2.3c)$$

Taking the ratios of P3 / P4, P5 / P4, and P6 / P4:

$$P3 / P4 = K_3 * |\Gamma - Q_3|^2 \quad (2.4a)$$

$$P5 / P4 = K_5 * |\Gamma - Q_5|^2 \quad (2.4b)$$

$$P6 / P4 = K_6 * |\Gamma - Q_6|^2 \quad (2.4c)$$

Equation 2.4 indicates that, from the four power measurements P3, P4, P5, and P6, three circles are traced in the Γ-plane. These circles are centred at the Q-points (Q_3, Q_5, and Q_6). In

addition, constants K_3, K_5 and K_6 are functions of the six-port's s-parameters only. These six unknown constants can thus be determined through an appropriate calibration routine.

Assuming that the circuit of figure 2.1 is composed of lossless components and delay-less transmission lines, the b-waves exiting the six-port towards the power meter are as follows [4]:

$$b_3 = \sqrt{6} / 4 * b * (\Gamma - j * \sqrt{2}) \quad (2.5a)$$

$$b_4 = -j * \sqrt{3} / 2 * b \quad (2.5b)$$

$$b_5 = -j * \sqrt{3} / 4 * b * \left[\Gamma + (1 + j) * \sqrt{2}\right] \quad (2.5c)$$

$$b_6 = -\sqrt{3} / 4 * b * \left[\Gamma - (1 - j) * \sqrt{2}\right] \quad (2.5d)$$

The Q-points of the six-port are as follows:

$$Q_3 = j * \sqrt{2} = 1.414 \angle 90^o \quad (2.6a)$$

$$Q_5 = -(1 + j) * \sqrt{2} = 2 \angle -135^o \quad (2.6b)$$

$$Q_6 = (1 - j) * \sqrt{2} = 2 \angle -45^o \quad (2.6c)$$

Clearly, the Q-points of this six-port are all located outside the $|\Gamma| = 1$ circle. In addition, they are separated by 90^o or 135^o. This six-port is therefore suited to the accurate measurement of complex reflection coefficients.

To this very day, six-ports continue to warrant the attention of the research community. This attention has produced a maturation of the technology [6]. Researchers have strived to produce devices covering larger bandwidths and operating higher and higher in frequency [7 - 10].

Further research has focussed on the realisation of six-ports with ideal Q-points [11, 12]. Others have studied six-port hardware and power sensors in an attempt to minimise six-port measurement error [13, 14]. Still others have focussed their efforts on the conception of novel six-port circuit architectures and on the MMIC integration of six-ports [15 - 19]. Finally, as each reflection coefficient measurement requires the reading of four power values, six-port reflectometry can be a time-consuming process. To minimise this problem, some high-speed reflectometers have been constructed and evaluated [20].

2.1.2 Six-Port Calibration

Prior to the measurement of any unknown reflection coefficient, the six-port circuit must be calibrated. This procedure consists of two major steps: the reduction of the scalar six-port to an equivalent vector four-port, and the calculation of an "error box" mapping the measured vector to the actual unknown load reflection coefficient. The calibration procedure has been carefully examined by a number of researchers [21-23]. The complete six-port calibration procedure is presented in [21] and is highlighted below.

Equation 2.2 indicates that, in general, the power measurements are

$$P_i = |\alpha_i * \Gamma + \beta_i|^2 |b_2|^2 \qquad (2.7)$$

Taking the ratios of P_3 / P_4, P_5 / P_4, and P_6 / P_4 yields:

$$q_k = |w_k|^2 = P_i / P_4 = \left| \frac{\alpha_i * \Gamma + \beta_i}{\alpha_4 * \Gamma + \beta_4} \right|^2 \qquad (2.8)$$

where for k = 1, i =3, for k = 2, i = 5, and for k = 3, i = 6.

Factoring and re-organising, the three power ratios relate to three complex w indicators such that:

$$|w_k|^2 = \left| \frac{d_k * \Gamma + e_k}{c * \Gamma + 1} \right|^2 \qquad (2.9)$$

From equation 2.8, it is concluded that the unknown reflection coefficient Γ is related to three vectorial indicators w_1, w_2, and w_3, by the following bilinear transformation:

$$\Gamma = \frac{e_1 - w_1}{c * w_1 - d_1} = \frac{e_2 - w_2}{c * w_2 - d_2} = \frac{e_3 - w_3}{c * w_3 - d_3} \qquad (2.10)$$

From 2.10, w_1 can be isolated in terms of w_2 and in terms of w_3. Substitution of these expressions in 2.8 yields (after some algebra and redefinition of terms):

$$q_1 = |w_1|^2 \qquad (2.11a)$$

$$A^2 * q_2 = |w_1 - m|^2 \quad (2.11b)$$

$$B^2 * q_3 = |w_1 - n|^2 \quad (2.11c)$$

Equation 2.11 is a dual of equation 2.4. In the latter equation, three scalar unknowns (K_3, K_5, and K_6) and three complex unknowns (Q_3, Q_5, and Q_6) must be solved in the Γ plane. However, equation 2.11 shows only two scalar unknowns (A^2, and B^2) and two complex unknowns (m. and n) that must be solved in the w_1 plane.

The six-port to four-port reduction routine essentially computes the four unknown constants of equation 2.11. Once these constants are known, equation 2.11 is used to generate a vectorial indicator w in the w_1 plane from the three power ratios q_i. Then, the error box generation algorithm simply finds the mapping from the w_1 indicator plane to the Γ reflection coefficient plane. This mapping is the bilinear transformation of equation 2.10.

2.1.2.1 Six-Port to Four-Port Reduction

As previously explained, the six-port to four-port reduction algorithm determines the two scalar constants (A^2, and B^2) and the two complex constants (m. and n) of equation 2.11 [21].

Defining $w_1 = u_1 + j * v_1$, $m = M * e^{j*\mu}$ and $n = N * e^{j*\nu}$, equation 2.11 becomes:

$$q_1 = u_1^2 + v_1^2 \quad (2.12a)$$

$$A^2 * q_2 = (u_1 - M * \cos\mu)^2 + (v_1 - M * \sin\mu)^2 \quad (2.12b)$$

$$B^2 * q_3 = (u_1 - N * \cos\upsilon)^2 + (v_1 - N * \sin\upsilon)^2 \quad (2.12c)$$

Three constants, p, q, and r, are now defined:

$$p = |m - n|^2 = M^2 + N^2 - 2MN\cos(\upsilon - \mu) \quad (2.13a)$$

$$q = |n|^2 = N^2 \quad (2.13b)$$

$$r = |m|^2 = M^2 \quad (2.13c)$$

The constants q and r are the square of the distance between the origin of the w_1 plane and the points n and m. The constant p is the square of the distance between the points m and n.

Using equation 2.12 to determine expressions for $A^2 Q_2 - Q_1$ and $B^2 Q_3 - Q_1$, the following matrix relationship is obtained:

$$\begin{bmatrix} u_1 \\ v_1 \end{bmatrix} = (\sin(\upsilon - \mu))^{-1} \begin{bmatrix} \sin\upsilon & -\sin\mu \\ -\cos\upsilon & \cos\mu \end{bmatrix} \begin{bmatrix} \beta \\ \gamma \end{bmatrix} \quad (2.14)$$

Finally, remembering that equation 2.12a states that $q_1 = u_1^2 + v_1^2$, it is observed that:

$$q_1 = \begin{bmatrix} u_1 \\ v_1 \end{bmatrix}^T \begin{bmatrix} u_1 \\ v_1 \end{bmatrix} = (\beta^2 + \gamma^2 + 2\alpha\beta\gamma) / (1 - \alpha^2) \quad (2.15)$$

where the constants α, β, and γ are defined as:

$$\alpha = -\cos(\upsilon - \mu) \quad (2.16a)$$

$$\beta = (M^2 + q_1 - A^2 * q_2) / 2M \quad (2.16b)$$

$$\gamma = (N^2 + q_1 - B^2 * q_3) / 2N \quad (2.16c)$$

However, closer examination of equation 2.13 reveals that:

$$\alpha = (p - q - r) / (2\sqrt{qr}) \quad (2.17a)$$

$$\beta = (r + q_1 - A^2 * q_2) / (2\sqrt{r}) \quad (2.17b)$$

$$\gamma = (q + q_1 - A^2 * q_3) / (2\sqrt{q}) \quad (2.17c)$$

Note that in 2.17, the constant q is not to be confused with the power ratios q_i.

Substitution of α, β, and γ as defined in 2.17 into equation 2.15 yields:

$$X_1 q_1^2 + X_2 q_2^2 + X_3 q_3^2 + X_4 q_1 q_2 + X_5 q_1 q_3 + X_6 q_2 q_3 + X_7 q_1 + X_8 q_2 + X_9 q_3 = -1 \quad (2.18)$$

Substitution of the measured power ratios q_i produced by nine different loads into equation 2.18 generates a determinate set of nine equations in the variables X_1, X_2, X_3, ... ,X_9. Solving for these unknown variables allows for the computation of the constants p, q, r, A^2, and B^2 as follows:

$$p = r + q + (X_7 / X_1) \quad (2.19a)$$

$$q = \frac{2X_4 - X_7 X_8}{2X_1 X_8 - X_4 X_7} \quad (2.19b)$$

$$r = \frac{2X_5 - X_7 X_9}{2X_1 X_9 - X_5 X_7} \quad (2.19c)$$

$$A^2 = +\sqrt{prX_2} \quad (2.19d)$$

$$B^2 = +\sqrt{pqX_3} \quad (2.19e)$$

The six-port to four-port reduction routine is now complete. As specified, the goal of this routine is to determine the constants A^2, B^2, m, and n as illustrated in equation 2.11. In equation 2.19, the constants A^2, and B^2 are clearly specified. The constants m and n, however, are not known exactly. Nonetheless, for any arbitrary unknown reflection coefficient Γ, the constants p, q, and r allow for the specification of a unique indicator w and its complex conjugate w'. Identifying w simply entails the resolution of a sign ambiguity.

2.1.2.2 Specification of a Unique "w" Indicator

Having determined the constants A^2, B^2, p, q, and r, the unique w indicator of an unknown reflection coefficient Γ can be computed.

Equation 2.11 indicates that the w indicator of this unknown reflection coefficient must lie at the intersection of three circles. More specifically, equation 2.11a indicates that one of these circles is centred at the origin of the w_1 plane. This implies that the unknown w indicator is simply a phase-shifted version of the variable w_1. Without loss of generality, it can also be specified that the w indicator lies on the line defined by the vector n of equation 2.11. Thus, w is

specified mathematically as [21]:

$$w = u + j * v = w_1 * e^{-j*\mu} = (u_1 + j * v_1) * (\cos\mu - j * \sin\mu) \quad (2.20)$$

Separating the real and imaginary part of 2.20 yields two equations as follows:

$$\begin{bmatrix} u \\ v \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\cot(\upsilon - \mu) & \csc(\upsilon - \mu) \end{bmatrix} \begin{bmatrix} \beta \\ \gamma \end{bmatrix} \quad (2.21)$$

After some algebraic manipulation, it is clear that the w = u + j * v indicator is specified as follows:

$$u = \beta \quad (2.22a)$$

$$v = (\alpha\beta + \gamma)/\pm\sqrt{1 - \alpha^2} \quad (2.22b)$$

As previously discussed, the w indicator is known within a sign ambiguity. The resolution of this ambiguity is discussed in the following section.

2.1.2.3 Error Box Computation

As previously mentioned, the second stage of the calibration procedure determines the mapping between the complex indicator w and the actual reflection coefficient Γ. This mapping is the bilinear transformation highlighted in equation 2.10. For clarity, this relationship is repeated here:

$$\Gamma = \frac{e - w}{c * w - d} \quad (2.23)$$

In 2.23, the constants c, d and e are complex quantities.

Expansion of the previous relation and separation of the real and imaginary components yields [21]:

$$u = d_R x - d_I y + e_R - (xu - yv)c_R + (xv + yu)c_I \quad (2.24a)$$

$$v = d_R y + d_I x + e_I - (xv + yu)c_R - (xu - yv)c_I \quad (2.24b)$$

In 2.24, the complex constants are expanded as follows: $\Gamma = x + j\,y$, $w = u + j\,v$, $c = c_R + j\,c_I$, $d = d_R + j\,d_I$, and $e = e_R + j\,e_I$.

Given three accurately known loads Γ, the corresponding w indicators for these three loads can be obtained. Substitution of these values in equation 2.24 produces six simultaneous equations in the six variables c_R, c_I, d_R, d_I, e_R, and e_I. Once these six values are known. the bilinear transformation of equation 2.23 is known.

Only the sign ambiguity of equation 2.22b remains. In order to resolve this unknown, it is noted that given four known reflection coefficients Γ^a, Γ^b, Γ^c, and Γ^d, their corresponding indicators w^a, w^b, w^c, and w^d must satisfy the following relation [21]:

$$\frac{(w^a - w^d)(w^b - w^c)}{(w^a - w^b)(w^c - w^d)} = \frac{(\Gamma^a - \Gamma^d)(\Gamma^b - \Gamma^c)}{(\Gamma^a - \Gamma^b)(\Gamma^c - \Gamma^d)} \quad (2.25)$$

Thus, given three very accurately known loads, the mapping from the w_I indicator plane

to the complex Γ plane is found. Additionally, a fourth fairly accurately known load allows for the resolution of the residual sign ambiguity of the six-port to four-port reduction.

2.1.2.4 Power Flow Measurement Using Six-Ports

It is also possible to use the six-port for measuring the power absorbed by the measured load Γ. The power measured at port 4 is given by equation 2.7 as follows [21]:

$$P_4 = |\alpha_4 * \Gamma + \beta_4|^2 |b_2|^2 \quad (2.26)$$

If a power meter is connected to the six-port's measurement terminal, the power that it reads is:

$$P_L = G_0 (|b_2|^2 - |a_2|^2) = G_0 (1 - |\Gamma_L|^2) |b_2|^2 \quad (2.27)$$

where Γ_L is the load presented to the six-port by the power meter.

From 2.26, an expression for $|b_2|^2$ can be derived. Furthermore, the load Γ_L can be transformed to its equivalent w indicator via the bilinear transformation of equation 2.23. Substitution of these expressions into 2.27 yields:

$$P_L = K (|d - wc|^2 - |w - e|^2) P_4 \quad (2.28)$$

Thus, once calibrated for the measurement of reflection coefficients, the six-port can also be calibrated to measure the power flow through its measurement port. Connecting a power meter to the load port, the w-indicator of this "load" is easily determined. In addition, the measure of power absorbed by this meter (P_L) is noted. As P_4 is also known, the constant K of equation 2.28 is easily determined. Thus, for any subsequent unknown load, knowledge of the corresponding w

indicator in addition to power reading P_4 allows for the computation of the power absorbed by this load.

Six-port calibration has been the object of academic interest for a number of years. Nevertheless, a number of alternative calibration schemes have appeared in the literature in recent years [24, 25]. Furthermore, some researchers have developed calibration routines that improve performance in highly noisy environments [26]. Finally, the effect of power meter error on the performance of the six-port has been analysed. Techniques for reducing these negative effects have been devised [27, 28].

2.2 Six-Port Reflectometer Conception and Realisation

2.2.1 Hardware Implementation

The implementation of a load-pull system requires two six-port reflectometers, one for measuring the input reflection coefficient, and one for measuring the output reflection coefficient. Two six-ports are constructed using commercially available components as illustrated in figure 2.2a and 2.2b. The ports of the reflectometers are labelled. Port 1 is the excitation port, and port 2 is the measurement port. It is also clear from the schematics below that port 4 is isolated from port 2. The circuits below are almost identical to the six-port illustrated in figure 2.1

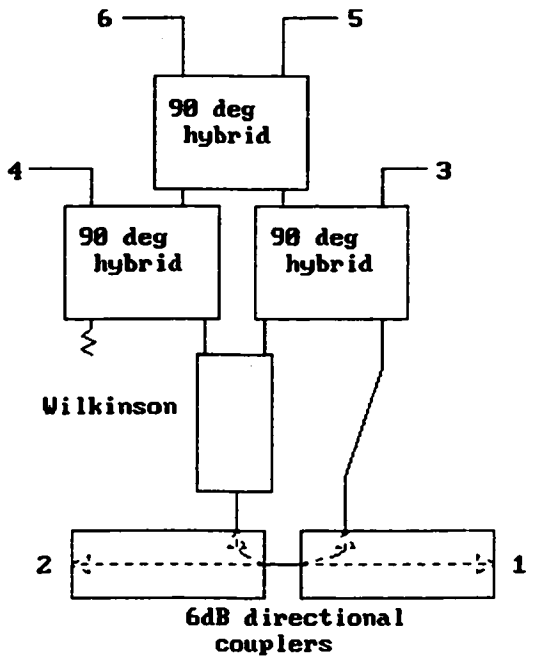

Figure 2.2a Six-Port SP1

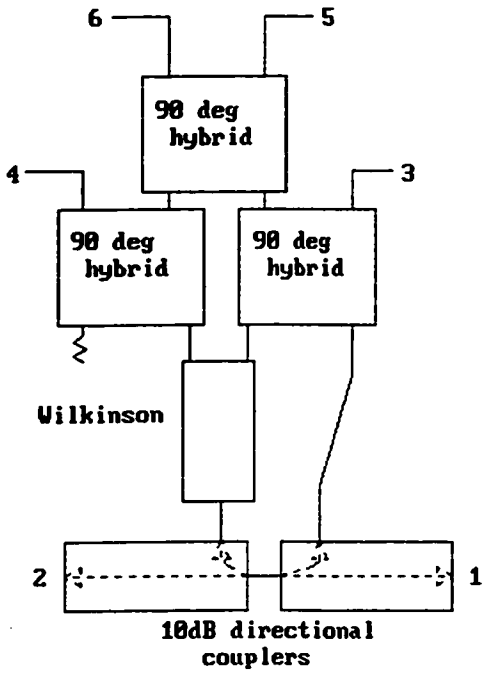

Figure 2.2b Six-Port SP2

Reflection coefficient measurement using these six-ports entails the measurement of the power flowing through ports 3 to 6. These ports are consequently connected to a single-pole four-throw microwave switch, whose output port is connected to a power meter. In order to automate the measurement procedure, the switches are actuated via a GPIB interface. The power meter is also compatible with the GPIB standard, allowing for the computer automation of the reflectometry process.

In order to validate the six-ports' applicability to microwave reflectometry, the S-parameters of the devices are measured. The Q-points of the six-ports are then computed at 3.5 GHz, 7.0 GHz, and 10.5 GHz using equation 2.3. The Q-points are given in table 2.1.

Table 2.1			
Six-Port SP1 Q-Points			
Frequency	Q3	Q5	Q6
3.5 GHz	1.1099 $\angle$86.20^o	1.3232 $\angle$-64.16^o	1.0278 $\angle$-148.83^o
7.0 GHz	1.0294 $\angle$-96.24^o	1.6911 $\angle$92.26^o	1.0208 $\angle$9.69^o
10.5 GHz	0.9770 $\angle$54.10^o	2.0318 $\angle$-94.23^o	1.0575 $\angle$159.07^o
Six-Port SP2 Q-Points			
Frequency	Q3	Q5	Q6
3.5 GHz	0.9095 $\angle$50.86^o	0.9150 $\angle$-97.76^o	1.0319 $\angle$172.47^o
7.0 GHz	0.7382 $\angle$161.24^o	1.2037 $\angle$33.60^o	1.1306 $\angle$-55.01^o
10.5 GHz	0.7301 $\angle$-64.69^o	1.0652 $\angle$159.39^o	1.6402 $\angle$59.49^o

Examination of the Q-points of six-port SP1 shows clearly that this circuit is suitable for reflectometry. Almost all Q-points are outside the $|\Gamma| = 1$ circle. They are also adequately separated and are clearly not co-linear. Unfortunately, six-port SP2 has more Q-points within the $|\Gamma| = 1$ circle. This is a consequence of the use of 10dB directional couplers rather than the 6dB couplers used in the six-port of figure 2.1. Nonetheless, the Q-points are not too close to the $|\Gamma| = 1$ circle, and their angular separation is adequate. This six-port is also suited to reflectometry applications.

2.2.2 Reflectometer Software

Software routines are designed to automate the six-ports' calibration procedure. The measurement procedure of the reflectometers is also automated.

2.2.2.1 Calibration Software

Automation of the reflectometers is accomplished via GPIB communication with a personal computer. Calibration routines are implemented using the Labview commercial software suite.

Two automatic calibration routines are implemented. The first takes the necessary power measurements for calibrating the six-port's power measurement feature. The program prompts the user to connect a power sensor to the reflectometer's measurement port. A file is then created containing five power measurements; four power measurements used for determining the w indicator of the load presented by the power sensor, and a fifth measurement indicating the power absorbed by the sensor.

The second calibration routine prompts the user to successively connect thirteen loads to the measurement port. The first load is an accurately known offset short. The second is an accurately known offset open. The third is a matched load. The fourth is a fairly accurately measured open circuit. Finally, a sequence of nine different (but not precisely known) loads are connected to the measurement port. These loads are generated with a phase shifter, some attenuators and an open circuit. The automation creates a file containing the four power measurements needed to generate the w indicator of all thirteen loads.

A Matlab routine is then executed to complete the calibration routine. All thirteen loads are used to generate thirteen simultaneous equations using 2.18. Only nine loads are needed to

solve for the constants X_1, X_2, X_3, ... , and X_9. Nonetheless, thirteen loads produce an over-determined set of equations that can be solved using a least-squares error function. This results in greater solution accuracy [21]. The values for p, q, r, A^2, and B^2 are then found using 2.19. This completes the six-port to four-port reduction.

The same Matlab routine then computes the error boxes of the six-port. Using 2.17, 2.22 and the appropriate power measurements, the w indicators of the first four loads are computed. The sign ambiguity of equation 2.17 is then resolved using 2.25. The program then generates a constant indicating whether the square root in equation 2.22 is positive or negative.

The w indicators of the first three loads are then substituted in 2.24. Since these three loads are accurately known, the values of Γ are also entered in this equation. The values of c_R, c_I, d_R, d_I, e_R, and e_I are computed.

The program continues to calibrate the six-port for power measurements. First, the w indicator of the power sensor is computed. This w indicator in addition to the measured power flow and all known constants are substituted in equation 2.28. The constant K is finally found.

The result of all this mathematical manipulation is the creation of a file containing thirteen calibration constants. It includes: the constants p, q, r, A^2, and B^2 as computed in 2.19; the sign constant resolving the ambiguity of 2.22; the constants c_R, c_I, d_R, d_I, e_R, and e_I specifying the bilinear transformation of 2.23; and the constant K of equation 2.28.

2.2.2.2 Measurement Software

The measurement mathematics of the reflectometer are also automated using Labview.

This software routine begins by reading the previously generated calibration constants. Then, the four powers needed to compute the unknown load's w indicator are measured, and the corresponding q-ratios are computed. Substitution of these q-ratios and the appropriate calibration constants in 2.17 produces the corresponding α, β, and γ constants. These are then substituted in 2.22. The sixth calibration constant resolves the sign ambiguity of 2.22b and the unknown load's w indicator is thus obtained. Finally, the bilinear transformation of 2.23 is computed and the unknown Γ is thus measured. The power absorbed by the load is also computed using 2.28.

2.2.3 Specification of Accurately Known Calibration Standards

In order to accurately determine the bilinear transformation from the w plane to the Γ plane in the error box computation algorithm, a set of three accurately known calibration standards is required. For this purpose, the standards of an HP-85052D calibration kit are used. This kit is produced by Hewlett-Packard as a calibration tool for network analysers.

The kit contains a very accurate matched load, an offset short circuit and an offset open circuit. These standards are accurately characterised by Hewlett-Packard, and their specifications are provided with the HP-85052D kit. Equations are provided relating these specifications to the actual reflection coefficients of the standards [29]. These standard reflection coefficients are

listed in table 2.2.

Table 2.2						
Accurately Known Calibration Standards						
Frequency	|short|	∠short	|open|	∠open	|50 Ω|	∠50 Ω
3.5 GHz	0.9972	99.82°	0.9976	-79.81°	0.0000	0.00°
7.0 GHz	0.9960	19.66°	0.9966	-159.52°	0.0000	0.00°
10.5 GHz	0.9952	-60.47°	0.9958	120.73°	0.0000	0.00°

These are the standards used for computing the error box constants c_R, c_I, d_R, d_I, e_R, and e_I using equation 2.24.

2.3 Reflectometer Validation

The repeatability, stability, and accuracy of the six-ports are examined.

2.3.1 Repeatability of Six-Port Measurements

The repeatability of the measurements taken with the reflectometer is a function of two entities. First, the six-port's hardware, including the microwave switch, must be capable of producing repeatable measurements. Secondly, the power meter must also measure power consistently.

In order to ensure that accurate Γ measurements are possible over a broad range of powers, the reflectometer is implemented with a power meter possessing a very large dynamic range. It is interesting to consider the accuracy and repeatability of the reflectometer when the

power meter operates near the top and near the bottom of this dynamic range. In addition, the power meter is capable of averaging a number of power samples in an attempt to improve the accuracy of its measurement. It is also interesting to study the repeatability of measurements taken with a varying number of samples.

In order to examine the repeatability of the six-ports' measurements, the reflection coefficient produced by a short-circuited 3dB attenuator is studied. Twenty sample measurements of this load are taken at 3.5GHz, 7.0 GHz, and 10.5 GHz. The average and the standard deviation of these twenty samples are then computed. The experiment is repeated with the power meter averaging 32 power readings, 128 power readings, and 512 power readings. Measurements are also repeated with the power meter operating in the high-power end of its dynamic range and with the power meter operating at the low-power end of its dynamic range. Results are highlighted in table 2.3a for six-port SP1 and in table 2.3b for six-port SP2.

Table 2.3a			
Repeatability of Six-Port Measurements (Six-Port SP1)			
High-Power Operation of Power Meter			
	32 sample averaging	128 sample averaging	512 sample averaging
$\|\Gamma\|$ @ f_o	standard dev = 0.000339	standard dev = 0.000281	standard dev = 0.000383
$\angle\Gamma$ @ f_o	standard dev = 0.024°	standard dev = 0.022°	standard dev = 0.026°
$\|\Gamma\|$ @ $2f_o$	standard dev = 0.000591	standard dev = 0.00746	standard dev = 0.000611
$\angle\Gamma$ @ $2f_o$	standard dev = 0.043°	standard dev = 0.054°	standard dev = 0.045°
$\|\Gamma\|$ @ $3f_o$	standard dev = 0.000733	standard dev = 0.000633	standard dev = 0.000766
$\angle\Gamma$ @ $3f_o$	standard dev = 0.057°	standard dev = 0.10°	standard dev = 1.40°
Low-Power Operation of Power Meter			
	32 sample averaging	128 sample averaging	512 sample averaging
$\|\Gamma\|$ @ f_o	standard dev = 0.0145	standard dev = 0.00361	standard dev = 0.00782
$\angle\Gamma$ @ f_o	standard dev = 0.605°	standard dev = 0.296°	standard dev = 0.442°
$\|\Gamma\|$ @ $2f_o$	standard dev = 0.0143	standard dev = 0.00904	standard dev = 0.00570
$\angle\Gamma$ @ $2f_o$	standard dev = 1.129°	standard dev = 0.638°	standard dev = 0.332°
$\|\Gamma\|$ @ $3f_o$	standard dev = 0.0136	standard dev = 0.0140	standard dev = 0.0052
$\angle\Gamma$ @ $3f_o$	standard dev = 2.22°	standard dev = 1.21°	standard dev = 0.731°

Table 2.3b			
Repeatability of Six-Port Measurements (Six-Port SP2)			
High-Power Operation of Power Meter			
	32 sample averaging	128 sample averaging	512 sample averaging
$\|\Gamma\|$ @ f_o	standard dev = 0.000152	standard dev = 0.000168	standard dev = 0.000228
$\angle\Gamma$ @ f_o	standard dev = 0.013°	standard dev = 0.016°	standard dev = 0.013°
$\|\Gamma\|$ @ $2f_o$	standard dev = 0.000501	standard dev = 0.00111	standard dev = 0.000543
$\angle\Gamma$ @ $2f_o$	standard dev = 0.051°	standard dev = 0.280°	standard dev = 0.041°
$\|\Gamma\|$ @ $3f_o$	standard dev = 0.000465	standard dev = 0.000506	standard dev = 0.000633
$\angle\Gamma$ @ $3f_o$	standard dev = 0.044°	standard dev = 0.044°	standard dev = 0.048°
Low-Power Operation of Power Meter			
	32 sample averaging	128 sample averaging	512 sample averaging
$\|\Gamma\|$ @ f_o	standard dev = 0.0155	standard dev = 0.00568	standard dev = 0.00558
$\angle\Gamma$ @ f_o	standard dev = 0.569°	standard dev = 0.400°	standard dev = 0.424°
$\|\Gamma\|$ @ $2f_o$	standard dev = 0.00964	standard dev = 0.00874	standard dev = 0.00345
$\angle\Gamma$ @ $2f_o$	standard dev = 1.296°	standard dev = 0.698°	standard dev = 0.524°
$\|\Gamma\|$ @ $3f_o$	standard dev = 0.0308	standard dev = 0.0140	standard dev = 0.0127
$\angle\Gamma$ @ $3f_o$	standard dev = 2.77°	standard dev = 1.21°	standard dev = 0.890°

An examination of tables 2.3a and 2.3b reveals that the effect of power measurement averaging is negligible when the power meter operates at the high-power end of its dynamic range. However, power measurement averaging has a significant effect when the power meter operates at the low-power end of its dynamic range. Since the six-ports are designed specifically for the implementation of a multi-harmonic load-pull system, it is expected that they will deal with fairly low powers, especially when measuring a FET's harmonic terminations. Thus, it is

concluded that every power measurement should be the average of 512 samples.

Comparison of the six-ports' performance with published data reveals that the six-ports are indeed very good. Using standard deviation as an indicator of six-port repeatability, one study has shown that the standard deviation of five $|\Gamma|$ measurements can be as low as 0.0001. This same reflectometer measured the phase of Γ with a standard deviation of 0.01^{o} [17]. The results presented in tables 2.3a and 2.3b indicate that the six-ports can measure twenty values of a given Γ with comparable standard deviations if the power meter is operated at the high-power end of its dynamic range. Furthermore, a standard deviation of 0.01 on the measurement of $|\Gamma|$ and a standard deviation of a few degrees on the measurement of $\angle\Gamma$ is obtained at the low-power end of the power meter's dynamic range. This measurement repeatability is sufficient for the load-pulling application that is envisioned for the six-ports.

2.3.2 Six-Port Calibration Stability

If the reflectometers are to be used in a load-pull system, they must be capable of retaining their measurement accuracy long after the point of calibration. A verification of the six-ports' calibration stability over the course of one hour is undertaken here.

The variation in the measurements of the six-ports over a one hour period is highlighted in table 2.4. During this period, six hundred reflection coefficient measurements are collected. The average of the first one hundred measurements is computed. This is compared to the average of the first two hundred measurements, and so forth.

Table 2.4						
Six-Port SP2 Calibration Stability						
	$\lvert\Gamma\rvert$ f_o	$\angle\Gamma$ f_o	$\lvert\Gamma\rvert$ $2f_o$	$\angle\Gamma$ f_o	$\lvert\Gamma\rvert$ $3f_o$	$\angle\Gamma$ f_o
avg of 100 samples	0.5416	-120.31°	0.4329	-63.07°	0.4876	11.65°
avg of 200 samples	0.5453	-120.12°	0.4341	-63.11°	0.4877	11.63°
avg of 300 samples	0.5519	-115.56°	0.4340	-63.13°	0.4844	11.78°
avg of 400 samples	0.5414	-116.99°	0.4340	-63.14°	0.4828	12.12°
avg of 500 samples	0.5439	-117.52°	0.4342	-63.17°	0.4827	12.14°
avg of 600 samples	0.5433	-120.77°	0.4342	-63.17°	0.4804	11.97°
Six-Port SP1 Calibration Stability						
	$\lvert\Gamma\rvert$ f_o	$\angle\Gamma$ f_o	$\lvert\Gamma\rvert$ $2f_o$	$\angle\Gamma$ f_o	$\lvert\Gamma\rvert$ $3f_o$	$\angle\Gamma$ f_o
avg of 100 samples	0.5498	-119.95°	0.4288	-62.96°	0.4843	12.85°
avg of 200 samples	0.5498	-119.99°	0.4289	-62.98°	0.4843	12.82°
avg of 300 samples	0.5496	-120.34°	0.4290	-63.00°	0.4847	12.78°
avg of 400 samples	0.5495	-120.09°	0.4287	-63.00°	0.4843	12.72°
avg of 500 samples	0.5494	-120.12°	0.4285	-62.99°	0.4842	12.61°
avg of 600 samples	0.5494	-120.16°	0.4284	-63.01°	0.4844	12.56°

Examination of table 2.4 shows that the measurements vary within ±0.01 for $\lvert\Gamma\rvert$ and withing ±3° for $\angle\Gamma$. This indicates that, over the course of one hour, the calibration of the six-ports is very stable. Further experimentation has shown that, over the course of twenty-four hours, the calibration remains relatively constant. The six-ports are thus suitable for prolonged, continuous operation in a load-pull system.

2.3.3 Six-Port Γ-Measurement Accuracy

Having determined that the six-ports are stable over time and produce repeatable measurements, the accuracy of these measurements is scrutinised. For this purpose, a number of loads are measured with an HP-8510 network analyser. These same loads are then measured with the six-ports and the results are compared.

Table 2.5a, 2.5b and 2.5c show this comparison for seven different loads. These loads are: a matched load, an offset short circuit, an offset open circuit, a short-circuited 3dB pad, an open-circuited 3dB pad, a short-circuited 6dB pad, and an open-circuited 6dB pad. During the experiment, the latter four loads are created by making use of a high-quality attenuator and the appropriate offset open circuit or offset short circuit termination.

Table 2.5a				
Comparison of Six-Port Measurements with HP-8510 Network Analyser at 3.5 GHz				
	Six-Port SP1		Six-Port SP2	
High Power	$\|\Gamma\|$ difference	$\angle\Gamma$ difference	$\|\Gamma\|$ difference	$\angle\Gamma$ difference
Matched load	0.0006	14.65^{o}	0.0024	48.91^{o}
Short circuit	0.0080	0.32^{o}	0.0130	0.31^{o}
Open Circuit	0.0176	0.00^{o}	0.0062	0.40^{o}
Short + 3dB	0.0078	0.62^{o}	0.0081	0.39^{o}
Open + 3dB	0.0111	1.43^{o}	0.0102	0.07^{o}
Short + 6dB	0.0031	0.08^{o}	0.0028	0.17^{o}
Open + 6dB	0.0030	1.45^{o}	0.0014	0.50^{o}
	Six-Port SP1		Six-Port SP2	
Low Power	$\|\Gamma\|$ difference	$\angle\Gamma$ difference	$\|\Gamma\|$ difference	$\angle\Gamma$ difference
Matched load	0.0000	55.58^{o}	0.0011	52.67^{o}
Short circuit	0.0046	0.05^{o}	0.0011	0.21^{o}
Open Circuit	0.0176	0.06^{o}	0.0151	0.26^{o}
Short + 3dB	0.0058	0.43^{o}	0.0044	0.50^{o}
Open + 3dB	0.0092	1.35^{o}	0.0110	0.18^{o}
Short + 6dB	0.0030	0.30^{o}	0.0004	0.43^{o}
Open + 6dB	0.0020	1.41^{o}	0.0013	0.43^{o}

Table 2.5b				
Comparison of Six-Port Measurements with HP-8510 Network Analyser at 7.0 GHz				
	Six-Port SP1		Six-Port SP2	
High Power	$\lvert\Gamma\rvert$ difference	$\angle\Gamma$ difference	$\lvert\Gamma\rvert$ difference	$\angle\Gamma$ difference
Matched load	0.0018	83.57^{o}	0.0013	34.46^{o}
Short circuit	0.0112	0.19^{o}	0.0044	0.26^{o}
Open Circuit	0.0182	0.10^{o}	0.0130	0.28^{o}
Short + 3dB	0.0175	2.16^{o}	0.0073	1.68^{o}
Open + 3dB	0.0012	2.34^{o}	0.0000	1.05^{o}
Short + 6dB	0.0026	0.10^{o}	0.0034	0.00^{o}
Open + 6dB	0.0026	0.77^{o}	0.0043	0.34^{o}
	Six-Port SP1		Six-Port SP2	
Low Power	$\lvert\Gamma\rvert$ difference	$\angle\Gamma$ difference	$\lvert\Gamma\rvert$ difference	$\angle\Gamma$ difference
Matched load	0.0005	44.73^{o}	0.0003	73.2^{o}
Short circuit	0.0017	0.48^{o}	0.035	0.01^{o}
Open Circuit	0.0004	0.04^{o}	0.0101	0.43^{o}
Short + 3dB	0.0147	2.05^{o}	0.0077	1.76^{o}
Open + 3dB	0.0003	0.90^{o}	0.0022	1.03^{o}
Short + 6dB	0.0034	0.24^{o}	0.0014	0.10^{o}
Open + 6dB	0.0002	0.07^{o}	0.0031	0.03^{o}

Table 2.5c				
Comparison of Six-Port Measurements with HP-8510 Network Analyser at 10.5 GHz				
	Six-Port SP1		Six-Port SP2	
High Power	$\|\Gamma\|$ difference	$\angle\Gamma$ difference	$\|\Gamma\|$ difference	$\angle\Gamma$ difference
Matched load	0.0004	38.11^{o}	0.0013	71.79^{o}
Short circuit	0.0151	0.54^{o}	0.0148	0.55^{o}
Open Circuit	0.0107	0.64^{o}	0.0103	0.69^{o}
Short + 3dB	0.0330	2.61^{o}	0.0120	4.14^{o}
Open + 3dB	0.0012	0.72^{o}	0.0065	1.72^{o}
Short + 6dB	0.0080	2.59^{o}	0.0063	3.20^{o}
Open + 6dB	0.0003	0.25^{o}	0.0072	0.48^{o}
	Six-Port SP1		Six-Port SP2	
Low Power	$\|\Gamma\|$ difference	$\angle\Gamma$ difference	$\|\Gamma\|$ difference	$\angle\Gamma$ difference
Matched load	0.0004	36.14^{o}	0.0005	70.92^{o}
Short circuit	0.0173	0.93^{o}	0.0169	0.60^{o}
Open Circuit	0.0187	0.67^{o}	0.0139	0.60^{o}
Short + 3dB	0.0330	1.77^{o}	0.0123	4.34^{o}
Open + 3dB	0.0040	1.15^{o}	0.0028	2.00^{o}
Short + 6dB	0.0077	2.41^{o}	0.0050	1.97^{o}
Open + 6dB	0.0049	0.33^{o}	0.0032	0.78^{o}

Published results comparing six-port measurements to those obtained with an HP-8410B network analyser are available [16]. The comparison is performed for a short circuit and a short-circuited 3dB attenuator. A difference of 0.02 is noted in the measurement of $|\Gamma|$ taken with the six-port and that taken with the HP-8410B analyser. The measurements of $\angle\Gamma$ taken with the two

instruments differ by approximately 2^{o} for the short and by as much as 8^{o} for the short-circuited 3dB pad. The table above shows a maximum difference of 0.035 in the measurements of $|\Gamma|$ and a maximum difference of 4.5^{o} in the measurements of $\angle\Gamma$. The constructed six-ports are thus as accurate as previously published designs.

As a further gauge of the accuracy of the six-ports, the precisely-known standards used in the calibration routine are measured. Comparison of the measurement to the accurately known standard value constitutes the most accurate means of estimating the precision of the reflectometers. The same comparison is performed with the HP-8510. Table 2.6 shows the difference between reflection coefficients measured by individual reflectometers and the accurately known value of these reflection coefficients. Interestingly, both six-ports are more accurate than the HP-8510 in measuring the calibration standards. This suggests that the reflectometers may be even more accurate than indicated in tables 2.5a, 2.5b, and 2.5c.

Table 2.6				
Comparison of Measurement Standards				
3.5 GHz				
	|offset short|	∠offset short	|offset open|	∠offset open
Six-Port SP1	0.0069	0.54^{o}	0.0053	0.21^{o}
Six-Port SP2	0.0011	0.01^{o}	0.0027	0.05^{o}
HP-5810	0.0022	0.22^{o}	0.0124	0.21^{o}
7.0GHz				
	|offset short|	∠offset short	|offset open|	∠offset open
Six-Port SP1	0.0072	0.07^{o}	0.0048	0.18^{o}
Six-Port SP2	0.0004	0.00^{o}	0.0004	0.00^{o}
HP-5810	0.0040	0.26^{o}	0.0134	0.28^{o}
10.5 GHz				
	|offset short|	∠offset short	|offset open|	∠offset open
Six-Port SP1	0.0020	0.07^{o}	0.0002	0.16^{o}
Six-Port SP2	0.0009	0.01^{o}	0.0010	0.01^{o}
HP-5810	0.0148	0.53^{o}	0.0142	0.73^{o}

2.3.4 Six-Port Power Measurement Accuracy

Finally, the load-pull system's reflectometers must accurately measure power flow in order to produce accurate amplifier gain measurements. The accuracy of the power flow measurements taken by the six-ports is investigated here.

A power sensor is connected to the measurement port of the six-port circuit and the power absorbed by this sensor is measured using both the six-port and the power meter itself.

Table 2.7 highlights the results.

Table 2.7		
Six-Port SP1 Power Flow Measurement Verification		
	Six-Port Measurement	Power Meter Measurement
3.5 GHz		
High Power	466.064 μW = -3.316 dBm	466.508 μW = -3.311 dBm
Low Power	453.6 nW = -33.433 dBm	455.7 nW = -33.413 dBm
7.0 GHz		
High Power	339.740 μW = -4.689 dBm	340.139 μW = -4.683 dBm
Low Power	348.3 nW = -34.580 dBm	343.1 nW = -34.646 dBm
10.5 GHz		
High Power	287.586 μW = -5.412 dBm	287.736 μW = -5.410 dBm
Low Power	290.6 nW = -35.367 dBm	282.031 nW = -35.497 dBm
Six-Port SP2 Power Flow Measurement Verification		
	Six-Port Measurement	Power Meter Measurement
3.5 GHz		
High Power	497.164 μW = -3.035 dBm	491.383 μW = -3.086 dBm
Low Power	489.5 nW = -33.102 dBm	485.4 nW = -33.139 dBm
7.0 GHz		
High Power	365.628 μW = -4.370 dBm	364.862 μW = -4.379 dBm
Low Power	361.6 nW = -34.418 dBm	362.1 nW = -34.412 dBm
10.5 GHz		
High Power	324.793 μW = -4.884 dBm	325.920 μW = -4.869 dBm
Low Power	321.5 nW = -34.928 dBm	328.9 nW = -34.829 dBm

The measurements highlighted in table 2.7 indicate that the measurements obtained with a six-port agree to those taken with a power meter within 0.1 dB. When these measurements are

used to calculate the amplifier's gain, the combined errors of the input power and the output power will produce an error of approximately 0.2 dB. Published results indicate that it is possible to calibrate six-ports to measure power with an accuracy of 0.03 dB [30]. Nonetheless, the accuracy of both six-ports shown here is suitable for the application at hand.

Clearly, two six-port reflectometers suitable for accurate Γ measurement are constructed and automated. The reflectometers are suitable for use in a multi-harmonic load-pull system.

2.4 Chapter 2 References

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CHAPTER 3

Load-Pull System Design

3.1 Load-Pull System Technologies

The technique known as load-pulling allows for the experimental study of the effect of a transistor's output load on its performance. In order to carry out these measurements, specialised hardware and software are needed.

3.1.1 Load-Pulling Hardware

A load-pull system essentially consists of hardware allowing for the variation of a transistor's output load. The system will typically contain two reflectometers, capable of measuring the transistor's input reflection coefficient, and the transistor's output load. A method for measuring the transistor's gain and efficiency is also incorporated.

Early load-pull systems varied the output load of a transistor by means of moveable dielectric slugs [1]. Then, active load-pulling systems were constructed [2, 3]. In these systems, a signal is fed backward toward the device of interest. Attenuators and phase shifters are used to vary the amplitude and phase of this feedback signal. In this manner, the effective load presented to the transistor can be varied.

Figure 3.1 illustrates a typical load-pull system. The input branch and the output branch

of the system are clearly visible in the diagram. The purpose of the former branch is to feed microwave power to the device-under-test. Attenuator VA-I is used to control the power reaching the device-under-test. The purpose of the latter branch is to feed power back into the output port of the device-under-test, thus changing the effective load seen by the device. Attenuator VA-O and phase shifter VP-O respectively vary the amplitude and phase of this feedback signal. Finally, reflectometers RM-I and RM-O measure the DUT's input reflection coefficient and output load respectively.

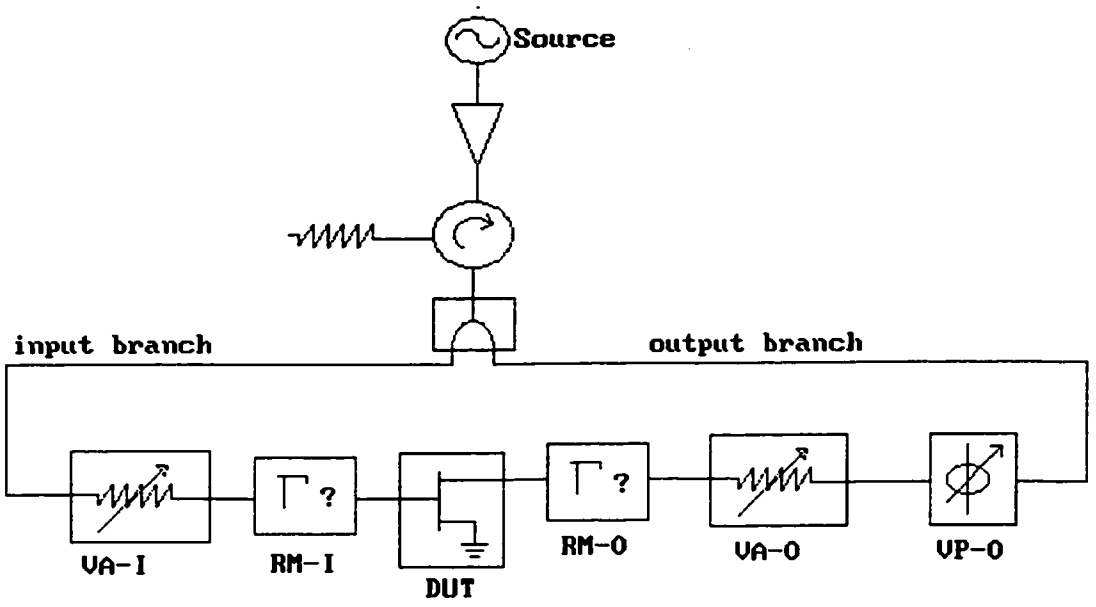

Figure 3.1 A Simple Load-Pull System

In order to study a non-linear device, such as a transistor power amplifier operating in a non-linear regime, the load-pull system must be extended to make it capable of measuring loads at harmonic frequencies in addition to the fundamental frequency [4]. This simply requires the addition of a further number of branches on the output side of the system. A number of load-pull

systems have been implemented for this purpose [5 - 9]. A typical system is illustrated in figure 3.2.

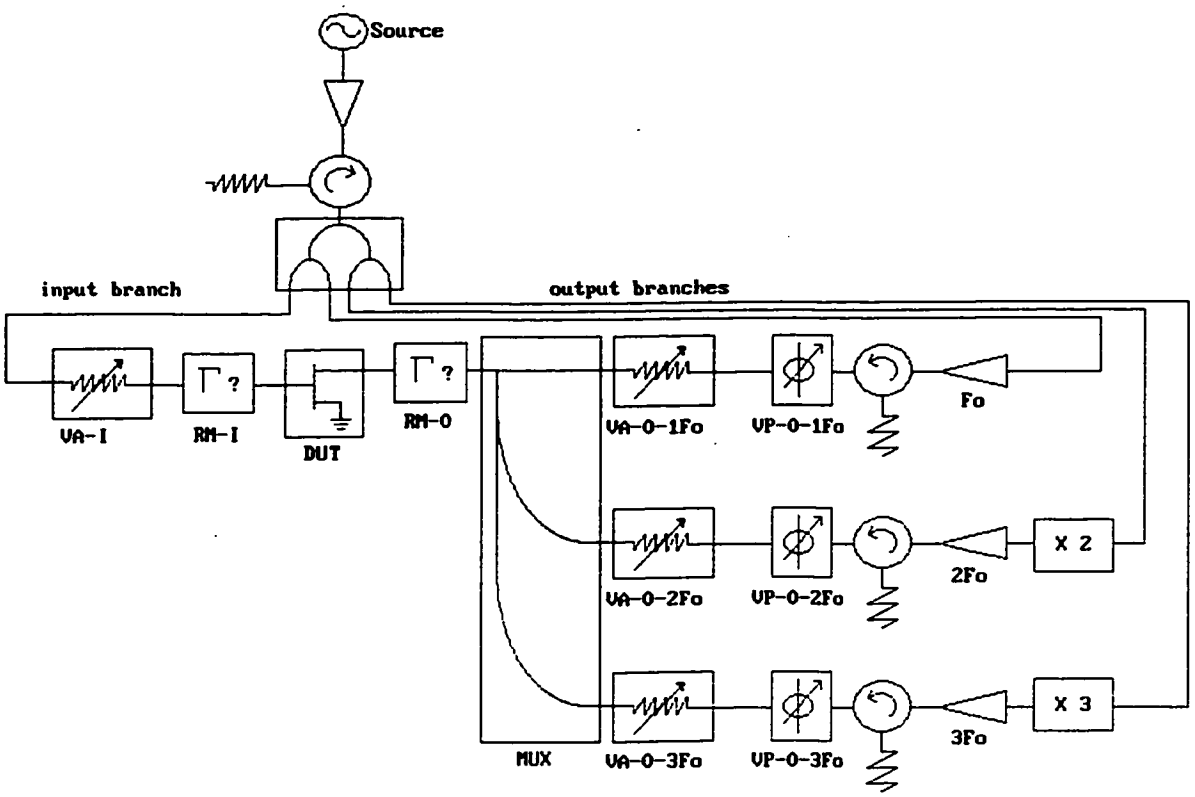

Figure 3.2 A Three-Harmonic Load-Pull System

The components of the system of figure 3.2 function exactly as those of the system of figure 3.1. However, a frequency multiplexer (MUX) is added to combine the feedback signals at the fundamental, at the second-harmonic, and at the third-harmonic frequency of operation of the DUT. A simple, broadband power combiner can be used to perform the same task. However, a multiplexer ensures that signals of only one frequency propagate in each branch of the load-pull system. This simplifies the design of the branches.

3.1.2 Load-Pulling Software

Automation of the load-pull system using appropriately designed software is also possible.

The automation of the reflectometers is the most obvious function suitable for software implementation. Depending on the reflectometer in question, an appropriate software routine is written to obtain the raw data from the device. As indicated previously, this data consists of four scalar power measurements if six-port circuits are used in this application. The reflection coefficient is then computed.

It is also possible to fully automate the operation of the load-pull bench. Traditionally, the variable attenuators and phase shifters used in the system are simple. manually tuned devices. However, some microwave component suppliers offer variable attenuators and phase shifters that can communicate via GPIB or some other communication scheme. Using these devices in conjunction with an appropriate software algorithm, load-pull systems capable of finding the optimal efficiency-enhancing or gain-enhancing loads of a transistor automatically can be implemented [8 - 10].

3.1.3 Other Load-Pull System Applications

Load-pull systems are not limited to the experimental determination of a transistor's gain-enhancing or efficiency-enhancing loads [5 - 9].

It is also possible to make use of these systems to measure the time-domain waveforms at the output of an amplifier [10 - 12]. Linearity is yet another amplifier parameter that can seriously affect the operation of a system. Some researchers have used load-pull techniques to examine the effect of a transistor's output load on the signal distortion introduced by the amplifier [13 - 17].

3.2 Load-Pull System Design and Construction

In the context of this work, a load-pull system allowing for the measurement of a transistor's efficiency-enhancing terminations is implemented. The system operates at a fundamental frequency of 3.5 GHz and is capable of measuring the transistor's output load at 3.5 GHz, 7.0 GHz, and 10.5 GHz.

3.2.1 Load-Pull System Construction

A load-pull system similar to that illustrated in figure 3.2 is constructed. The specific functional blocks of the system are discussed below.

3.2.1.1 Input Feed Branch

The branch of the system that feeds the DUT is identical to that of figure 3.2 with the addition of a filter. This filter is added in front of the attenuator. It ensures that the signal feeding the DUT is spectrally pure.

3.2.1.2 Loading Branches

The loading branches of the system are exactly as indicated in figure 3.2. An amplifier, a circulator, a variable attenuator, and a phase shifter designed to operate at the correct frequency are cascaded.

The variable attenuators and phase shifters are manually tunable devices. Unfortunately, this means that the task of load-pulling requires the attention of a system operator. However, those devices that are automated via computer control are usually electronic in nature. Such electronic attenuators and phase shifters are often slightly non-linear, generating harmonic content when a signal passes through them. These harmonics would compromise the accuracy of the load-pull system and thus, manually tunable, passive devices are better suited to this high-accuracy load-pulling application.

3.2.1.3 Combiner for Output Feedback Signal

In figure 3.2, a frequency multiplexer is shown to be the ideal device for combining the signal from the three output loading branches of the system. Unfortunately, the design of such a frequency multiplexer is a fairly significant task. It is thus replaced by a power combiner in this implementation of the load-pull system.

The replacement of the frequency multiplexer by a simple power combiner implies that signals at all three operating frequencies are present in all three branches of the system. Care must thus be taken to ensure that none of these signals have an adverse effect on the operation of

the individual branches. Most importantly, these out-of-band signals must not be allowed to perturb the amplifiers found in each of the branches. Unfortunately, broad-band circulators are not commercially available. Nonetheless, the devices used to protect the amplifiers are measured to confirm their suitability for this application.

3.2.1.4 System Reflectometers

Of course, six-ports are used to measure the input reflection coefficient and the output load of the device-under-test.

The input six-port must measure the input reflection coefficient of the transistor. This is needed only at 3.5 GHz. Thus, this six-port needs no additional hardware. Six-port SP2 (as described in chapter 2 of this work) is utilised here.

The output six-port must measure the output load of the transistor. This measurement is needed at 3.5 GHz, 7.0 GHz, and 10.5 GHz. A tunable YIG filter is added between the six-port's switch and the power meter in order to facilitate this multi-frequency load measurement. When the measurement is taken at 3.5 GHz, the YIG filter is tuned to the appropriate band, thus rejecting the other signals. The YIG filter is then moved to 7.0 GHz when the measurement is taken at this frequency. Then, the YIG filter is tuned to 10.5 GHz and the measurement is taken at the third harmonic. One by one, an accurate measurement of the transistor's load at all three frequencies of interest is obtained in this manner.

Six port SP1 (as described in chapter 2 of this work) is utilised to measure the efficiency-optimising loads of the transistor. Six-port SP1 is constructed with 10dB couplers (rather than 6dB couplers for SP2). This implies that, in general, the power levels measured at the four reflectometer data ports will be smaller for SP1 than for SP2 for a given load. However, the power levels at the output of the amplifier are certainly larger than the power levels at the input of the amplifier. Larger signal attenuation in the reflectometer connection between the DUT and the power meter is thus less significant on the output side of the DUT than on the input side. In addition, the YIG filter used to measure the multi-harmonic terminations of the DUT becomes non-linear at high signal powers, thus affecting measurement accuracy. For these reasons, it is desirable to place SP1 on the output side of the DUT and SP2 on the input side.

3.2.1.5 Frequency Multipliers

As indicated in figure 3.2, a frequency doubler and a frequency tripler are needed to construct the three-harmonic load-pull system. A number of tools can be employed in the generation of the second-harmonic and third-harmonic signals needed to study the DUT.

A highly over-driven transistor biased in cutoff is used to generate the required signals. Resonant stubs are implemented in microstrip technology in order to select the appropriate harmonic at the output of the transistors. The frequency doubler produces approximately 6 dBm at 7.0 GHz given an input signal of 9 dBm at 3.5 GHz. The frequency tripler produces approximately -6 dBm at 10.5 GHz given an input signal of 18.6 dBm at 3.5 Ghz.

Naturally, the resonant stub filters do not completely eliminate the unwanted signal components at the output of each transistor. Nonetheless, the amplifiers used in the system's output branches eliminate some of the unwanted components. In addition, appropriately designed band-pass filters are placed at the output of these amplifiers, thus ensuring that only the signal of interest is allowed to reach the DUT.

3.2.1.6 System Automation Hardware

In order to automate the system, a computer capable of communicating via GPIB is installed near the measurement hardware. This equipment is used to automate the process of calibrating the system and the process of transistor characterisation.

Software routines are used to control, via GPIB, the relay actuators that automate the six-ports. The GPIB bus is also used to transfer the power meter data to the computer. A GPIB compatible ammeter is also added to the system in order to automate the measurement of the DC current flowing in the transistor. The computer is also fitted with an addressable analog output card capable of producing any voltage between 0 and 15 volts. This control signal is used to tune the YIG filter, thus automating the measurement of the transistor's output load.

3.2.2 Load-Pull System Software

The operation of the load-pull system is governed by two programs. The first allows for the calibration of the six-ports. The second automates the characterisation of the DUT.

3.2.2.1 Calibration Software

The calibration of the load-pull system consists of four six-port calibration routines.

First, the input six-port is calibrated at 3.5 GHz. Then, the output six-port is calibrated, first at 3.5 GHz, then at 7.0 GHz ,and finally at 10.5 GHz. Each of these routines involves the connection of thirteen calibration standards to the measurement port of the appropriate reflectometer, as highlighted in chapter 2 of this work. A routine prompting the user to connect the calibration standards at the appropriate time is written in Labview. This same routine transfers the measurement data of the standards to the computer.

However, the calibration of the system for power measurements is slightly more complicated. For the input six-port, this calibration is only required at 3.5 GHz, and is thus no more complicated than for a six-port reflectometer in any other application.

For the output six-port, the calibration must be conducted for three frequencies. No problems are encountered at the power meter ports, as the YIG filter ensures that only one signal frequency reaches the power meter at one time. Unfortunately, this is not the case at the six-port's measurement port. When a power meter probe is connected to this port, it measures the power of all three frequency components. Experiment has shown that, in order to accurately calibrate the output six-port for power measurements at 3.5 GHz, the 7.0 GHz and 10.5 GHz, the unnecessary output loading branches of the system must be disconnected. Care must be taken in disconnecting these output branches. One must ensure that the signal at 3.5 GHz sees the same

impedance looking into the disconnected output branches as it would looking into the connected output branches. Otherwise, it will be impossible to obtain accurate power flow measurements.

A routine prompting the user to connect a power sensor to the appropriate six-port is written in Labview. The same routine transmits the reflectometer's measurement data to the computer. The power absorbed by the power sensor "load" is also transmitted to the computer and saved.

A Matlab routine completes the system's calibration. The files generated by Labview are used to supply the raw data to the Matlab routine. The six-port to four-port reduction and the error box computation is performed for the input six-port at 3.5 GHz, the output six-port at 3.5 GHz, the output six-port at 7.0 GHz, and the output six-port at 10.5 GHz. The resulting constants are saved in a file. The input six-port and the output six-port are also calibrated to measure power flow at 3.5 GHz.

3.2.2.2 Transistor Characterisation Software

A software tool is created to automate the characterisation of a transistor as well. This routine, written in Labview, automates the measurement of the input reflection coefficient, output load, gain, and efficiency of the device under test.

First, the input reflection coefficient of the transistor is computed. In addition, the input power of the device is measured. Then, the output load of the transistor at 3.5 GHz is measured

along with the output power of the device. Finally, the output load of the transistor at 7.0 GHz, and then at 10.5 GHz is measured. The DC current flowing through the transistor is also measured.

The software routine controls the operation of the reflectometers. The measurement data of the six-ports is transferred to the computer and the appropriate calibration constants are used to calculate the required reflection coefficients in addition to the input and output power of the device at 3.5 GHz. The program also controls the YIG filter. The power measurements are also used to calculate the amplifier's gain. This gain, along with the DC current measurement, can be used to calculate the transistor's power-added-efficiency. The program contains a graphical user interface capable of displaying all this information on the computer's monitor and the user can also choose to save the information in a file.

3.3 Load-Pull System Validation

In order to verify the accuracy of the load-pull system, a number of experiments are performed. A satisfactory load-pull system will provide accurate reflection coefficient measurements in addition to accurate power flow measurements. For accurate power-added-efficiency computations, the system must also accurately measure the DC current flowing through the transistor.

3.3.1 Verification of DC Current Measurement

The accuracy of the system's DC current measurement is verified in a very simple experiment. An electrical potential is applied across a resistor and, by Ohm's law, the current flowing through it is calculated. This current is measured using a standard hand-held ammeter and using the GPIB compatible ammeter used in the system. The measurements taken with the latter device agreed within one-hundredth of a milliampere with the hand-held device and the calculated values.

3.3.2 Verification of Reflection Coefficient and Power Flow Measurements

Because the six-ports can measure a reflection coefficient and a power flow simultaneously, the accuracy of the load-pull system's reflection coefficient measurements and the accuracy of the system's power flow measurements are verified in a single experiment.

The system is used to measure a number of different loads and the results are compared to measurements taken with an HP-8510 network analyser. Although the individual six-ports are validated in chapter 2 of this work, a further evaluation of their performance as entities within the load-pull system is performed here. This experiment illustrates the effect of the signal feeding branches on six-port operation. The experiment also highlights the effect of the YIG filter on the performance of the six-port used to measure the DUT's output load. The results of the experiment are shown in Table 3.1.

Table 3.1				
Load-Pull System Accuracy Verification: Γ - Measurement Error				
	High Power		Low Power	
Input	$\lvert\Gamma\rvert$ Error	$\angle\Gamma$ Error	$\lvert\Gamma\rvert$ Error	$\angle\Gamma$ Error
Matched load	0.0088	-	0.0329	-
Short circuit	0.0025	0.16^{o}	0.0065	0.12^{o}
Open Circuit	0.0125	0.17^{o}	0.0074	0.23^{o}
Short + 3dB	0.0008	0.05^{o}	0.0033	0.23^{o}
Open + 3dB	0.0052	0.29^{o}	0.0011	0.10^{o}
Short + 6dB	0.0017	0.05^{o}	0.0005	0.10^{o}
Open + 6dB	0.0007	0.95^{o}	0.0030	0.34^{o}
	High Power		Low Power	
Output Fo	$\lvert\Gamma\rvert$ Error	$\angle\Gamma$ Error	$\lvert\Gamma\rvert$ Error	$\angle\Gamma$ Error
Matched load	0.0042	-	0.0176	-
Short circuit	0.0204	0.68^{o}	0.0002	0.32^{o}
Open Circuit	0.0034	0.69^{o}	0.0191	0.66^{o}
Short + 3dB	0.0039	0.15^{o}	0.0022	1.39^{o}
Open + 3dB	0.0013	0.67^{o}	0.0063	1.62^{o}
Short + 6dB	0.0005	0.24^{o}	0.0036	2.66^{o}
Open + 6dB	0.0045	1.13^{o}	0.0001	4.09^{o}

	High Power		Low Power	
Output 2Fo	$\|\Gamma\|$ Error	$\angle\Gamma$ Error	$\|\Gamma\|$ Error	$\angle\Gamma$ Error
Matched load	0.0281	-	0.0289	-
Short circuit	0.0033	0.91^{o}	0.0080	1.00^{o}
Open Circuit	0.0103	0.20^{o}	0.0222	0.12^{o}
Short + 3dB	0.0146	1.13^{o}	0.0166	1.08^{o}
Open + 3dB	0.0037	2.71^{o}	0.0020	2.81^{o}
Short + 6dB	0.0006	1.89^{o}	0.0019	1.77^{o}
Open + 6dB	0.0023	0.27^{o}	0.0033	0.48^{o}
	High Power		Low Power	
Output 3Fo	$\|\Gamma\|$ Error	$\angle\Gamma$ Error	$\|\Gamma\|$ Error	$\angle\Gamma$ Error
Matched load	0.0660	-	0.0434	-
Short circuit	0.0046	0.14^{o}	0.0104	0.25^{o}
Open Circuit	0.0139	0.36^{o}	0.0134	1.26^{o}
Short + 3dB	0.0003	3.71^{o}	0.0070	2.40^{o}
Open + 3dB	0.0100	3.07^{o}	0.0004	0.57^{o}
Short + 6dB	0.0023	0.84^{o}	0.0109	3.31^{o}
Open + 6dB	0.0094	0.31^{o}	0.0056	4.74^{o}

It is clear from table 3.1 that at 3.5 GHz, both the input and the output reflectometers measure reflection coefficients with a magnitude error of $\pm$ 0.02 and a phase error of approximately 4^{o}. The maximum measurement error of the output six-port at 7.0 GHz and 10.5 GHz is also $\pm$ 0.02 in magnitude. However, as the frequency increases a slightly larger phase error of 6^{o} is noticed. Despite the presence of these measurement errors, the system is sufficiently accurate to produce reliable load-pull measurements.

The accuracy of the system's power measurements is also verified. Power flow measurements obtained with the load-pull system are compared to a calculated power flow. This calculation is performed using the measured $|\Gamma|$ of the load-under-test, the measured $|\Gamma|$ of a matched load, and the power flow measurement of the matched load as follows:

$$P_{LOAD} = \frac{(1 - |\Gamma_{LOAD}|^2) * P_{MATCHED}}{(1 - |\Gamma_{MATCHED}|^2)} \quad (3.1)$$

Table 3.2 highlights the results of this comparison.

Table 3.2

Load-Pull System Accuracy Verification: Power Measurement Verification

	High Power		Low Power	
Input	Six-Port Meas.	Calculated	Six-Port Meas.	Calculated
Matched load	9.80 μW	-	0.88 μW	-
Short circuit	46.96 nW	48.54 nW	-2.46 nW	-2.62 nW
Open Circuit	51.23 nW	49.41 nW	-4.74 nW	-4.49 nW
Short + 3dB	7.04 μW	6.94 μW	636.98 nW	618.24 nW
Open + 3dB	7.82 μW	7.91 μW	684.72 nW	706.16 nW
Short + 6dB	9.09 μW	9.02 μW	817.08 nW	806.88 nW
Open + 6dB	9.37 μW	9.41 μW	829.18 nW	842.31 nW

	High Power		Low Power	
Output Fo	Six-Port Meas.	Calculated	Six-Port Meas.	Calculated
Matched load	3.38 mW	-	2.26 μW	-
Short circuit	-99.26 μW	-104.85 μW	22.70 nW	23.46 nW
Open Circuit	-48.29 μW	-44.96 μW	42.22 nW	41.11 nW
Short + 3dB	2.18 mW	2.38 mW	1.51 μW	1.60 μW
Open + 3dB	2.65 mW	2.71 mW	1.88 μW	1.83 μW
Short + 6dB	2.99 mW	3.11 mW	2.02 μW	2.08 μW
Open + 6dB	3.34 mW	3.24 mW	2.20 μW	2.17 μW
Output 2Fo	Six-Port Meas.	Calculated	Six-Port Meas.	Calculated
Matched load	1.51 mW	-	62.02 μW	-
Short circuit	10.68 μW	9.84 μW	1.07 μW	0.98 μW
Open Circuit	0.76 μW	0.83 μW	1.41 μW	1.50 μW
Short + 3dB	1.26 mW	1.23 mW	51.58 μW	50.64 μW
Open + 3dB	1.04 mW	1.07 mW	42.59 μW	44.53 μW
Short + 6dB	1.44 mW	1.44 mW	55.76 μW	59.10 μW
Open + 6dB	1.38 mW	1.41 mW	54.10 μW	58.03 μW
Output 3Fo	Six-Port Meas.	Calculated	Six-Port Meas.	Calculated
Matched load	0.40 mW	-	26.01 μW	-
Short circuit	-4.44 μW	-4.33 μW	-1.07 μW	-1.07 μW
Open Circuit	2.85 μW	3.07 μW	0.17 μW	0.18 μW
Short + 3dB	0.37 mW	0.30 mW	24.17 μW	19.51 μW
Open + 3dB	0.27 mW	0.31 mW	16.91 μW	20.00 μW
Short + 6dB	0.42 mW	0.38 mW	26.52 μW	24.63 μW
Open + 6dB	0.35 mW	0.38 mW	22.47 μW	24.48 μW

From table 3.2, it is clear that the accuracy of the power measurement is somewhat compromised as the frequency of the measurement increases. The measurements at 10.5 GHz are more significantly different from the calculated value. This is not problematic as only the power at 3.5 GHz must be measured to accurately measure the gain of the amplifier. Power measurements for loads having $|\Gamma| = 1$ are also not very accurate. As the optimal output load of the amplifier at 3.5 GHz will certainly not lie on the $|\Gamma| = 1$ circle, this problem will not affect the reliability of the load-pull measurements.

3.3.3 Small-Signal Load-Pull Measurements

As an additional test of measurement reliability, the load-pull system is used to design a small-signal amplifier. Using a vector network analyser to measure the s-parameters of the device-under-test, it is possible to compare the load-pull data to a theoretical prediction based on these s-parameters.

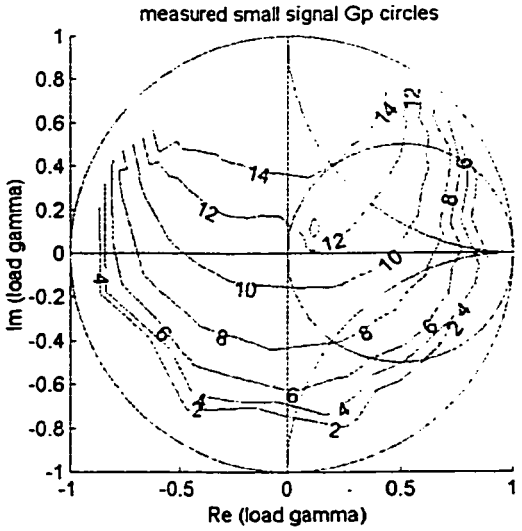

Figure 3.3 Measured FET Gp Circles (Gain labelled in dB)

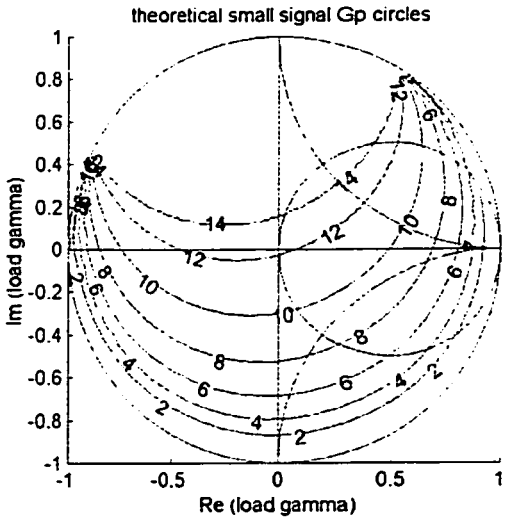

Figure 3.4 Theoretical FET Gp Circles (Gain labelled in dB)

Figures 3.3 and 3.4 show respectively the measured small-signal gain circles and the theoretically computed small-signal gain circles of an ATF-26836 transistor. Clearly, the circles are in good agreement. However, the measured circles near the transistor's maximum gain differ more significantly from the theoretical results than the smaller gain circles. Using a spectrum analyser to examine the signal at the output of the transistor, it was found that the device-under-test was slightly over-driven when the measurements were taken. This may explain the difference between the measured and the theoretical gain circles.

Thorough examination of these small-signal gain circles highlights one of the fundamental limitations of load-pulling using six-ports. In the load-pull system, the six-port is positioned not to measure the transistor's output load, but to measure the transistor's output reflection coefficient, as illustrated in figure 3.5. As the device's output load Γ_L is simply the reciprocal of this output reflection coefficient Γ_{OUT}, the computation of the output load is mathematically trivial.

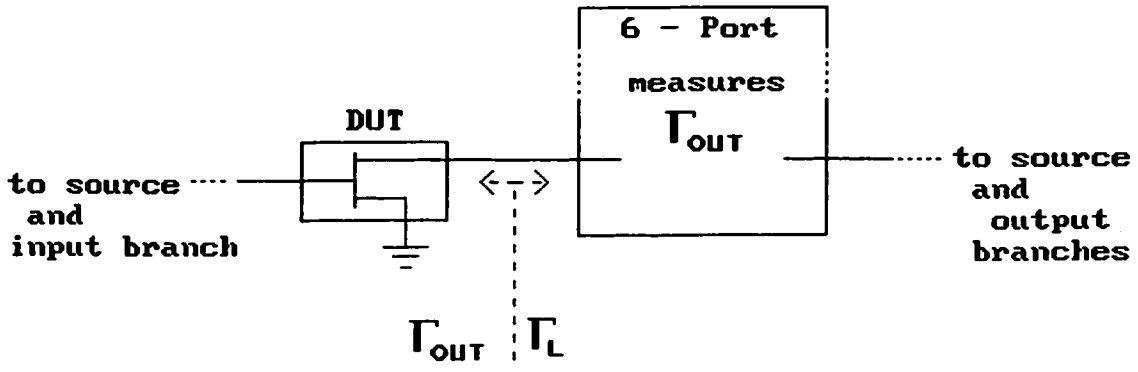

Figure 3.5 DUT Output Load Measurement

This reciprocation of the six-port's measurement introduces a fundamental problem. Consider for instance that the output of the transistor is matched. This implies that the output load of the transistor is $|\Gamma_L| = 0$. Unfortunately, the six-port measures $1 / |\Gamma_L|$ and not $|\Gamma_L|$. Thus, the six-port must measure an infinite value.

In order for a six-port to measure an infinite load, the $|\Gamma|$ circles that intersect on the load in the Γ-plane must have an infinite radius. This implies that the power ratios, Q_1, Q_2, and Q_3 must be infinite. If this is the case, then the reference power measurement P_4 must be zero. This is impossible, as the power meter is limited by a noise floor that is non-zero. This is a physical reality of any measurement instrument and thus cannot be avoided. In a load-pull system such as the one described here, this problem renders inaccurate all load measurements near $|\Gamma_L| = 0$.

This problem is worsened as the output power of the transistor becomes smaller. Consider a load reflection coefficient with $|\Gamma_L|$ = -30dB. To actively synthesise this load using the load-pull system, the power flowing back towards the transistor must be -30 dBm if the power flowing out of the transistor is 0 dBm, For the same load, the power flowing back to the transistor must be -90 dBm if the power flowing out of the transistor is -60 dBm. If the power meter's noise floor is at -80 dBm, it is clear that the load can be accurately measured in the first scenario, but cannot be accurately measured in the second scenario. Thus, the power meter's noise floor introduces more significant measurement inaccuracies when the output power of the device-under-test is lower.

Another problem arises when couplers with imperfect isolation are used in the construction of the six-ports. Again, this problem mostly affects the accuracy of the load-pull measurements near $|\Gamma_L| = 0$.

When the transistor is mounted as illustrated in figure 3.5, the reference power measurement P_4 should be proportional only to the power fed back to the transistor. However, if the fourth port of the reflectometer is not perfectly isolated from port two (the measurement port), the reference power measurement P_4 contains a component that is related to the output power of the transistor. As this output power increases, the fraction of P_4 that relates to it also increases.

If a matched load is synthesised at the output of the transistor, it is shown above that P_4 must be zero. Unfortunately, the minimum value of P_4 is now limited not only by the noise floor of the power meter, but also by power arriving at the reflectometer's fourth port due to this imperfect isolation. This results once again in inaccurate measurements near the centre of the Γ-plane.

3.4 TRL De-Embedding of Measurements

Having calibrated and verified the operation of the load-pull system, one final detail must be addressed prior to proceeding to the characterisation of a transistor. The load-pull system is completely fabricated using coaxial cable and coaxially connectorised components. However,

the amplifier will be constructed on another more suitable waveguide (coplanar waveguide, as explained in the next chapter). It is thus necessary to transform the load-pull measurements obtained in the coaxial system to reflect the loads seen by the transistor embedded in coplanar waveguide. The TRL calibration method is ideally suited to such measurement de-embedding [18, 19].

3.4.1 TRL Calibration Standards

The TRL calibration routine requires three standards, a THRU, a LINE, and a REFLECT.

The THRU standard is simply a length of the waveguide into which it is desired to de-embed a measurement. The LINE standard is simply a segment of waveguide that has an electrical length that is different to that of the THRU standard by 45^{o} to 135^{o}. The REFLECT standard is simply an open-circuited or short-circuited segment of waveguide [19].

For this purpose, a 30 mm long length of 50 Ω coplanar waveguide serves as a THRU standard. A 39 mm length of 50 Ω coplanar waveguide serves as a LINE standard. Finally, two 15 mm long segments of short-circuited coplanar waveguide serve as an appropriate REFLECT standard.

3.4.2 TRL Calibration Mathematics

Interestingly, the arithmetic of the TRL de-embedding routine reduces exactly to the arithmetic of the error-box routine used to measure reflection coefficients with six-ports. In the

latter case, the w-indicator obtained through a six-to-four port reduction algorithm is mapped to an unknown reflection coefficient through a bilinear transform as shown in equation 3.2.

$$w = \frac{a\Gamma_L + b}{c\Gamma_L + 1} \quad (3.2)$$

In the case of a TRL de-embedding, a previously measured reflection coefficient serves as the "w-indicator" in an identical bilinear transformation. The mapping is from a Γ in the coaxial system to a Γ in the coplanar waveguide system. It is thus clear that the TRL calibration routine simply involves the computation of the complex constants a, b and c in the bilinear transformation of equation 3.2.

Despite this striking similarity, the two calibration routines do differ quite significantly. The error box computation used to calibrate the six-port relies on three accurately known loads to compute the constants required in the bilinear transformation. The TRL routine, on the other hand, uses the s-parameters of the TRL calibration standards in determining these constants. Figure 3.6 illustrates the operation of the TRL de-embedding scheme.

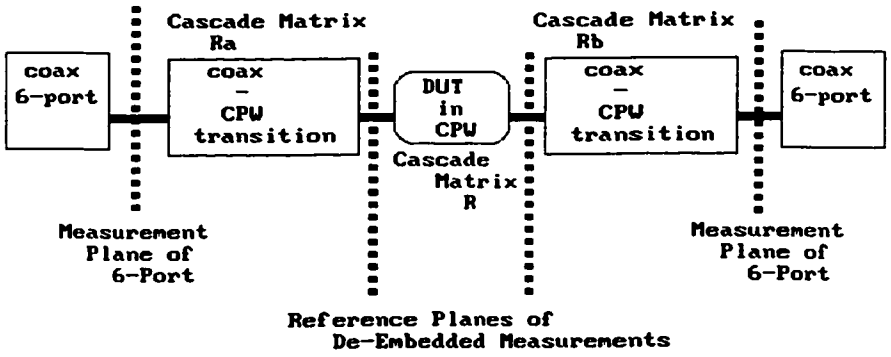

Figure 3.6 TRL De-Embedding Block Diagram

Figure 3.6, highlights one of the key features of the de-embedding algorithm. Namely, it is a two-port calibration scheme. In fact, the scheme was initially devised to calibrate a network analyser consisting of two six-ports. Thus, one single TRL de-embedding calibration routine provides the necessary constants for de-embedding a set of two reflection coefficients, each measured via a different six-port. Secondly, Figure 3.6 illustrates that the TRL de-embedding completely removes the effect of the waveguide transitions in the measurement of the DUT's characteristics. This is another convenient feature of this powerful metrology tool.

As indicated earlier, the six-port routine consists of finding the constants relating a measured w-indicator to a reflection coefficient of interest. This is accomplished by solving for the elements of the two wave cascading matrices R_A and R_B. These matrices are as follows [18]:

$$R_A = r_{22}\begin{pmatrix} a & b \\ c & 1 \end{pmatrix} \quad (3.3)$$

$$R_B = \rho_{22}\begin{pmatrix} \alpha & \beta \\ \gamma & 1 \end{pmatrix} \quad (3.4)$$

Using the measured S-parameters of the THRU and LINE standards, wave cascading matrices R_{THRU} and R_{LINE} are defined for these standards as follows:

$$R = \frac{1}{S_{21}}\begin{pmatrix} -(S_{11}S_{22} - S_{12}S_{21}) & S_{11} \\ -S_{22} & 1 \end{pmatrix} \quad (3.5)$$

In order to avoid leading the reader onto a rather significant mathematical tangent, the algebraic details of the TRL calibration routine are omitted. The interested reader is nonetheless referred to the original work by G. Engen [18]. For the purpose of this work, it suffices to say that after some algebraic manipulation, expressions for the constants a, b, c, α, β, and γ are obtained. In the algorithm, the s-parameters of the REFLECT standard are used to resolve a sign ambiguity. This standard also determines the location of the reference plane of the de-embedded measurements.

Given constants a, b, and c, a measurement w taken at port 1 can be de-embedded as illustrated in equation 3.2. A measurement taken at port 2 can be de-embedded using constants α, β, and γ as follows [18]:

$$w = \frac{\alpha\Gamma_L - \gamma}{-\beta\Gamma_L + 1} \quad (3.6)$$

3.4.3 Verification of the TRL Calibration

One useful feature of the TRL calibration routine lies in the fact that the calibration standards must not be accurately known. It is thus possible to verify the computed calibration constants with the measured s-parameters of the calibration standards. The de-embedded s-parameters of the calibration standards are as follows:

Table 3.3					
De-Embedded S-Parameters of TRL Calibration Standards					
Standard		S11	S21	S12	S22
THRU	F_o	6.058×10^{-10} $\angle -58.01^o$	1.000 $\angle 3.146\times10^{-11\,o}$	0.9999 $\angle 1.521\times10^{-7\,o}$	6.177×10^{-10} $\angle 175.29^o$
	$2F_o$	7.709×10^{-10} $\angle -146.97^o$	1.000 $\angle -1.057\times10^{-9\,o}$	1.000 $\angle -2.994\times10^{-9\,o}$	4.641×10^{-10} $\angle -53.51^o$
	$3F_o$	4.958×10^{-9} $\angle 124.27^o$	1.000 $\angle 2.905\times10^{-8\,o}$	1.000 $\angle -5.517\times10^{-7\,o}$	4.668×10^{-9} $\angle -99.07^o$
LINE	F_o	5.333×10^{-10} $\angle -100.00^o$	0.9994 $\angle -46.41^o$	0.9987 $\angle -46.38^o$	8.653×10^{-10} $\angle 126.21^o$
	$2F_o$	1.930×10^{-10} $\angle 29.51^o$	0.9953 $\angle -90.54^o$	0.9965 $\angle -90.52^o$	3.943×10^{-10} $\angle -108.87^o$
	$3F_o$	5.279×10^{-9} $\angle -150.69^o$	1.005 $\angle -139.13^o$	1.004 $\angle -130.10^o$	4.365×10^{-9} $\angle -10.18^o$
REFLECT	F_o	1.009 $\angle 176.27^o$	1.962×10^{-2} $\angle 90.56^o$	1.967×10^{-2} $\angle 90.72^o$	1.009 $\angle 176.27^o$
	$3F_o$	0.9932 $\angle 174.77^o$	2.613×10^{-2} $\angle 81.33^o$	2.622×10^{-2} $\angle 81.57^o$	0.9932 $\angle 174.77^o$
	$3F_o$	1.039 $\angle 171.95^o$	3.458×10^{-2} $\angle 82.04^o$	3.445×10^{-2} $\angle 81.86^o$	1.039 $\angle 171.95^o$

The table above clearly illustrates that the THRU standard is being de-embedded properly. This standard's de-embedded s-parameters clearly correspond to a zero-length matched

transmission line. The LINE standard is also properly de-embedded. It's de-embedded s-parameters correspond to those of a matched transmission line that is approximately 45^{o} in length at 3.5 GHz, 90^{o} in length at 7.0 GHz, and 135^{o} in length at 10.5 GHz.

The most significant test of the TRL calibration's accuracy lies in its treatment of the REFLECT standard. Observing the de-embedded s-parameters of this final standard, one notices immediately that the TRL routine gives $|S11| = |S22| = 1.0$ for all standards. Unfortunately, one also notices that the de-embedded s-parameters at 10.5 GHz show $|S11| = |S22| = 1.04$. This is a fairly significant over-estimation of the true reflection coefficient. Unfortunately, attempts to improve this calibration routine did not affect this result. The load-pull system's user must thus remember that reflection coefficients measured at 10.5 GHz are slightly over estimated.

Despite this error in de-embedding the magnitude of the REFLECT standard's reflection coefficients, the TRL routine performs very well in de-embedding this standard's phase. Using Agilent Technologies' Momentum software package, the de-embedded reflection coefficient of the REFLECT standard were numerically simulated. A comparison of this result with the above measurement is shown here:

Table 3.4			
Comparison of Simulated and Measured REFLECT Standard S-Parameters			
Frequency	de-embedded ∠S11	de-embedded ∠S22	simulated phase
3.5 GHz	176.27°	176.27°	177.271°
7.0 GHz	174.77°	174.77°	174.280°
10.5 GHz	171.95°	171.95°	171.756°

Clearly, the de-embedded measurements are in good agreement with the numerically simulated values.

It is now evident that a multi-harmonic load-pull system capable of characterising an active device operating in a non-linear regime at 3.5 GHz has been constructed.

3.5 Chapter 3 References

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CHAPTER 4

Power Amplifier Design

4.1 Power Amplifier Architecture

In order to implement a power amplifier, a number of architectural options are available. Most amplifier designs reported in the literature are constructed using the microstrip planar waveguide technology, as this technology offers a very convenient means of creating compact planar circuits. However, the coplanar waveguide technology is also useful in the design of such circuitry.

4.1.1 Coplanar Waveguide

The coplanar waveguide first appeared in the public literature in 1969 [1]. A significant theoretical framework has been published in regards to this waveguide [2 - 7].

The waveguide consists of two parallel slots etched in a ground plane, as illustrated in figure 4.1.

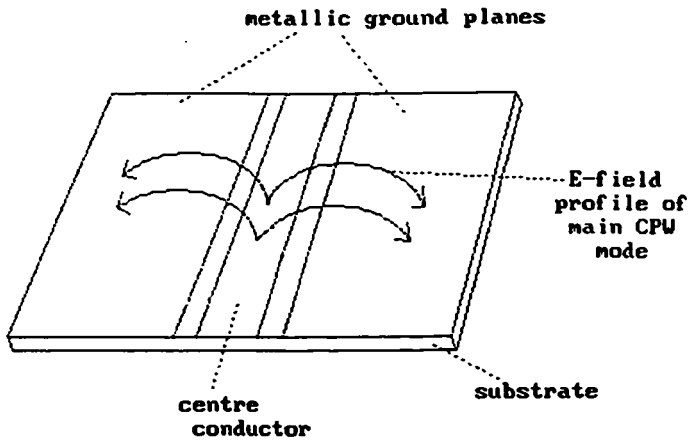

Figure 4.1 Coplanar Waveguide

Like the microstrip technology, the coplanar waveguide is planar, and easily constructed using convenient metal etching technologies.

The coplanar waveguide does have a number of other useful characteristics. First of all, if a connection must be made between the centre conductor and the ground plane, it can be made directly. Such a connection would require the construction of a via hole in microstrip technology. Furthermore, numerical analysis has shown that coplanar waveguide can be less lossy and less dispersive than microstrip [8]. Finally, the coplanar waveguide offers the designer many options in the creation of stubs. As in the microstrip technology, stubs can be etched in parallel to the centre conductor [9]. However, shunt stubs and series stubs can be patterned inside the centre conductor as well [10]. This allows for many interesting design solutions.

For these reasons, the coplanar waveguide is chosen for implementing the power amplifier.

4.1.2 Amplifier Substrate

In order to construct the amplifier, an appropriate substrate material must be chosen.

The substrate chosen for this application is Rogers' RT Duroid 5880. This material has a relative dielectric constant $\epsilon_r = 2.2$ and dielectric losses given by loss tangent $\tan \delta = 0.0015$ at 10.0 GHz. The dielectric is 61 mil in thickness and the metal is 34 μm thick.

In addition to the well-known dielectric loss mechanisms and the resistive ohmic losses in the conductors, additional losses will occur if parasitic surface waves are excited in the substrate [11]. The losses associated with these parasitic surface waves will be minimised if

$$h\sqrt{\varepsilon_r} \leq 0.12\lambda_o \quad (4.1)$$

where h is the substrate height and λ_o is the shortest wavelength travelling along the waveguide.

For the Rogers' 5880 Duroid, equation 4.1 indicates that no parasitic surface waves will be excited as long as the signal frequency remains below 30.8 GHz. If a conductor-backed coplanar waveguide is constructed using this substrate, parasitic surface waves can be excited at even lower frequencies. For some surface modes, a conductor-backed substrate effectively behaves like an identical substrate that is twice as thick. Thus, no signal of frequency above 15.4 GHz must be excited on such a conductor-backed coplanar waveguide in order to avoid excitation of the parasitic surface waves.

In addition, the conductor-backed coplanar waveguide can also support the same propagating modes that are supported in a simple parallel-plate waveguide [12]. The cutoff frequency of the first parallel-plate mode is:

$$f_c = \frac{c}{2d\sqrt{\varepsilon_r}} \quad (4.2)$$

where c is the speed of light, d is the dielectric thickness, and ϵ_r is the relative permittivity of the

dielectric. The characteristics of the Rogers' Duroid 5880 substrate are such that the cutoff frequency of this parallel-plate mode is 128.4 Ghz.

The amplifier is to be designed to operate at 3.5 GHz. As the operating mode of the amplifier is non-linear in nature, harmonics are generated as the signal is amplified. Harmonic tuning will be performed at the second and third harmonic in order to design a high efficiency amplifier. This third-harmonic component is at a frequency of 10.5 GHz. The analysis above shows that all problems of parasitic parallel-plate mode and parasitic surface wave mode excitations will be avoided provided that no signal of frequency greater than 15.4 GHz is transmitted through the coplanar waveguide. The substrate is thus suitable for the design of such a power amplifier.

4.1.3 50 Ω Coplanar Line

The coplanar waveguide used to construct the amplifier should have a characteristic impedance of 50 Ω. This will simplify the integration of the amplifier with existing microwave systems, as these systems are most often constructed using 50 Ω transmission lines. In addition, the load-pull system devised specifically for designing this amplifier is constructed with 50 Ω components. Using a 50 Ω transmission line to construct the amplifier simplifies the design process as well.

The characteristic impedance of a coplanar waveguide (not conductor-backed) can be computed using well-known relations derived using conformal mapping [1, 6, 7]. The

characteristic impedance of a coplanar waveguide having centre conductor width s and slot width w is [1]:

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K'(k)}{K(k)} \quad (4.3)$$

where ϵ_{eff} is the effective dielectric constant of the substrate and K(k) is the complete elliptical integral of the first kind with argument k. For a finite substrate of thickness h, the material's relative dielectric constant can be computed as [7]:

$$\varepsilon_{eff} = 1 + \left(\frac{\varepsilon_r - 1}{2}\right) \frac{K'(k)}{K(k)} \frac{K(k_1)}{K'(k_1)} \quad (4.4)$$

where $k = s / (s + 2w)$ and $k_1 = (\sinh(\pi s / 8h)) / (\sinh(\pi (s + 2w) / 8h))$.

Using these relations, a 50 Ω coplanar transmission line is designed as illustrated in figure 4.2.

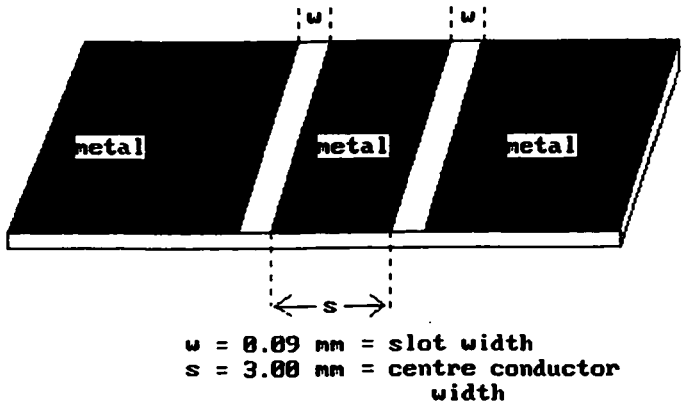

Figure 4.2 50 Ohm Coplanar Waveguide

The characteristic impedance of this waveguide is confirmed to be 50 Ω using the Momentum simulator produced by Agilent Technologies.

4.1.4 The Coupled Slot-Line Mode

The coplanar waveguide does suffer from one significant disadvantage in comparison to the microstrip technology. At any signal frequency, the coplanar waveguide can support two propagating modes.

The main mode of propagation (termed the CPW mode) is a quasi-TEM mode that has E-field pattern as illustrated in figure 4.1. Here, the two metal planes located on either side of the centre conductor are maintained at an equal potential to serve as a ground plane. This is the most interesting mode of propagation on coplanar waveguide as it exhibits low loss and is well confined to the waveguide.

A second mode (termed the coupled slot-line mode) can also propagate along a coplanar waveguide. The E-field pattern of this mode is illustrated in figure 4.3.

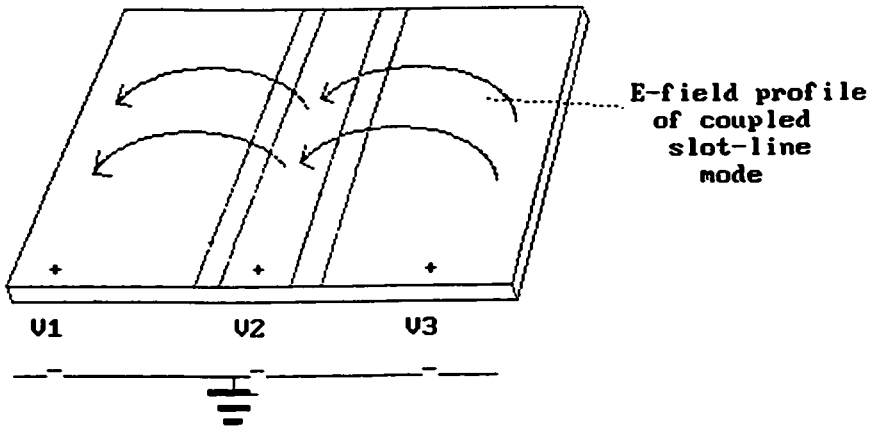

Figure 4.3 Coupled Slot-Line Mode Field Profile

Here, the two large metal planes are not maintained at the same potential. Specifically, the planes are held at voltages $V1 \leq V2 \leq V3$. The mode is highly radiative and thus, highly lossy.

It is clear that the coplanar waveguide must be properly excited if a signal is to propagate along it with low loss. Unfortunately, any discontinuities (like tees, stubs, etc.) along the waveguide will excite to some degree the coupled slot-line mode. This problem virtually renders the waveguide impractical in any real world circuit application. However, it is possible to control the losses induced by the excitation of the coupled slot-line mode by constructing air-bridges to connect the two metallic ground planes of the waveguide in the vicinity of circuit discontinuities [13 - 16]. The air-bridges used in this application must be properly designed. They must provide adequate suppression of the coupled slot-line mode while minimising their perturbation of the signal propagating along the waveguide in the main coplanar mode.

Using Agilent Technologies' Momentum simulator, a bridge providing adequate coupled slot-line mode suppression at 3.5 GHz is conceived. The bridge is etched on the reverse side of the substrate and is connected to the coplanar waveguide ground plane using a fine wire via hole connection. Figure 4.4 illustrates the bridge.

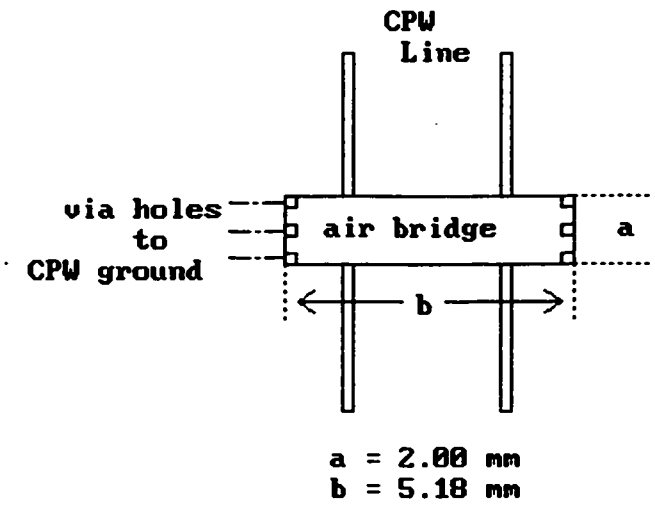

Figure 4.4 Bridge Providing Adequate Coupled Slot-Line Mode Suppression

A simple experiment can be conducted in order to ensure that the bridge does indeed suppress the radiative coupled slot-line mode. It is well known that a lossless two-port circuit has s-parameters that obey the following relation:

$$|S_{21}|^2 = 1 - |S_{11}|^2 \qquad (4.5)$$

A coplanar waveguide is unfortunately not lossless. However, the losses are small enough that equation 4.5 is obeyed very closely. In order to verify the performance of the bridge, a coplanar circuit containing a pair of balanced shunt stubs is numerically simulated. The result of this simple experiment is illustrated in table 4.1.

Table 4.1			
Evaluation of Bridge Performance			
Frequency	$S_{11} = S_{22}$	$S_{12} = S_{21}$	$(1 - \|S_{11}\|^2)^{1/2}$
3.5 GHz	$0.693 \angle 15.813^{o}$	$0.717 \angle -74.317^{o}$	0.721
7.0 GHz	$0.083 \angle -175.401^{o}$	$0.973 \angle 101.025^{o}$	0.997
10.5 GHz	$0.096 \angle -11.777^{o}$	$0.895 \angle -73.484^{o}$	0.995

The results highlighted in table 4.1 indicate that there is very little loss in the circuit at 3.5 GHz. However, the loss is more significant at 7.0 GHz and even more so at 10.5 GHz. This implies that, given the chosen circuit fabrication technology, shunt stubs patterned outside the coplanar waveguide's centre conductor can be exploited beneficially at 3.5 GHz only. This is a severe technological limitation, as the amplifier design must consist of an appropriately loaded active device at 3.5 GHz, 7.0 GHz, and 10.5 GHz.

4.1.5 Internally Patterned Series Stubs

Fortunately, the coplanar waveguide allows for the design of series stubs patterned inside its centre conductor. Such an internally patterned stub, if properly constructed, will not excite the unwanted coupled slot-line mode as much as externally patterned stubs.

Figure 4.5 illustrates a typical internally patterned series stub.

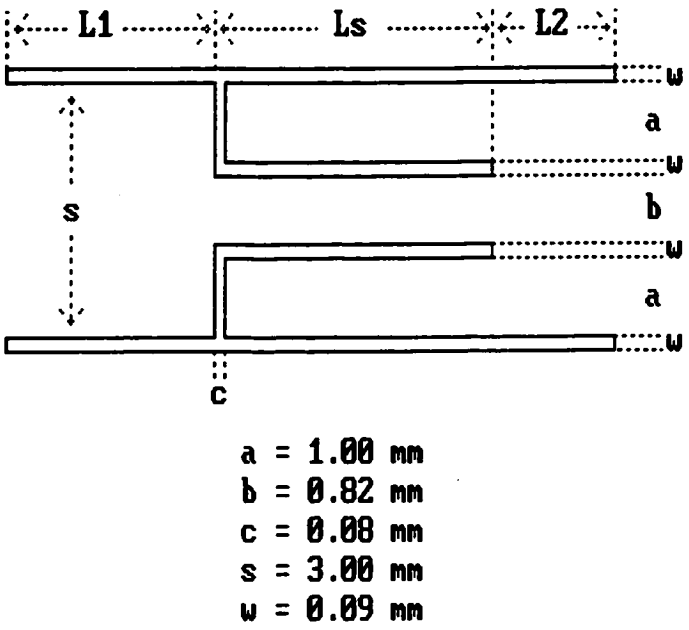

Figure 4.5 Internally Patterned Series Stub

In contrast to the externally patterned stubs. these stubs do not excite significantly the coupled slot-line mode. Table 4.2 illustrates the performance of a typical internally patterned stub as simulated using HP's Momentum simulator. The simulated stub has L_1 = 7.905 mm, L_S = 5.985 mm, and L_2 = 2.000 mm.

Table 4.2

Evaluation of Symmetric Internally Patterned Series Stub Performance

Frequency	S_{11}	$S_{12} = S_{21}$	$(1 - \|S_{11}\|^2)^{1/2}$
3.5 GHz	0.334 ∠-12.031°	0.941 ∠-101.553°	0.942
7.0 GHz	0.863 ∠-134.861°	0.489 ∠137.214°	0.505
10.5 GHz	0.808 ∠77.800°	0.579 ∠169.293°	0.589

Table 4.2 illustrates that a symmetric internally patterned stub does not excite the coupled slot-

line mode at all at 3.5 GHz. It is also clear that the coupled slot-line mode is excited minutely at 7.0 GHz and 10.5 GHz. However, the performance of the internally patterned stub is much better than that of an externally patterned stub. Table 4.2 thus shows that it is possible to design a circuit that performs well at all frequencies of interest using these internally patterned stubs.

Later in this work, a number of circuits containing such internally patterned stubs are presented. All stubs shall be constructed as specified in figure 4.5. Specifically, the dimensions a, b, c, s, and w will be exactly as shown. Circuit schematics will specify the length L_S of the stub, as well as the dimensions L_1 and L_2. The stub length L_S shall include the width c of the slots connecting the internally patterned stub to the main CPW line. The distance separating the internally patterned stubs from the circuit's extremities and / or adjacent circuit elements shall be specified by lengths similar to L_1 and L_2 as highlighted in figure 4.5.

It is clear at this point that reliable passive components can be designed and implemented using the Rogers' Duroid substrate and the coplanar waveguide.

4.2 Active Device

A suitable transistor must be selected in order to design and construct a high-efficiency power amplifier. An ATF-26836 GaAs FET manufactured by Agilent Technologies is selected for this application.

4.2.1 Transistor Specifications

The ATF-26836 is a GaAs FET. A typical transistor will produce an output power of 18 dBm at its 1 dB gain compression point. The transistor has a pinch off voltage V_p = -1.5 V and a saturated drain current I_{DSS} = 50 mA.

The ATF-26836 is clearly not a power transistor. Unfortunately, the equipment available for this work is not capable of handling power levels that are significantly higher than 18 dBm. Nonetheless, the theoretical concepts that are demonstrated using this transistor can be easily ported to a higher power device.

4.2.2 Transistor DC Characteristics

In order to gain a more thorough understanding of the transistor's characteristics, the DC current-voltage curves of the device are measured. These characteristics are illustrated in figures 4.6 and 4.7. The figures also illustrate typical bias points for a class A, class AB and a class B amplifier constructed with the ATF-26836 transistor.

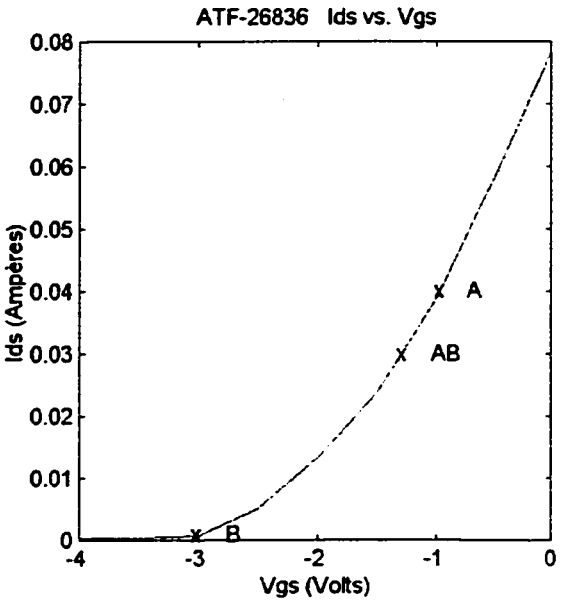

Figure 4.6 ATF-26836 Ids vs Vgs Curve with class A, AB, and B bias points

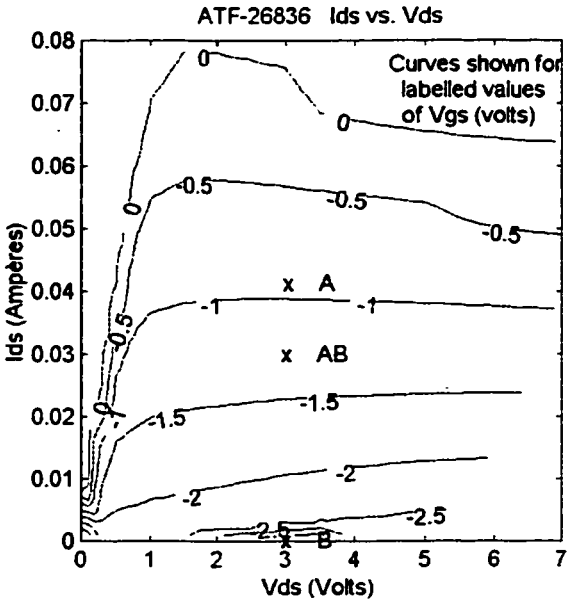

Figure 4.7 ATF-26836 Ids vs Vds Curve with class A, AB, and B bias points

Figure 4.7 clearly indicates that V_{DS} can swing between 0 V and approximately 6 V. To maximise the output power of the device, it is clear that the transistor should be biased at V_{DS} = 3 volts. In order to maximise the power amplifier's efficiency, the device should be operated in a class B or class AB mode. Experimentation has shown that the signal at the output of the device is richer in harmonic content if a class B mode is chosen. Since this project is concerned with the study of the effect of harmonic loading on the performance of the amplifier, a class B mode of operation is chosen. The bias point of the transistor is thus fixed at V_{DS} = 3.0 V, and I_{DS} = 0.5 mA.

4.3 Transistor Efficiency Optimisation

Having chosen an appropriate DC bias point for the transistor, the design of the high-efficiency power amplifier now reduces to a two-stage process. First, the input power of the transistor must be selected in order to operate the device in an appropriately non-linear regime. Secondly, the efficiency-optimising output loads of the transistor must be determined at 3.5 GHz, 7.0 GHz, and 10.5 GHz.

4.3.1 Input Power

The input power of the transistor must be selected in accordance with a number of criteria. First of all, it is clear that over-driving the device may either destroy it or shorten its useful life. However, if the device is not operated in an adequately non-linear regime, the signal at its output will not be very rich in harmonic content. In addition, an appropriate drive power level will result in good amplifier efficiency.

Experimentation with the ATF-26836 transistor has revealed that when the input power is approximately 4 mW (or 6 dBm), sufficient harmonic content is present at the output of the device. In addition, this level of power is not significant enough to compromise the device's reliability.

4.3.2 Determination of Efficiency-Optimising Output Loads

Chapter 3 of this work highlights the design and validation of a load-pull system capable of determining the output loads that must be presented to a transistor in order to optimise its amplifying efficiency. This system is used to design a high-efficiency power amplifier using the ATF-26836 transistor biased in class B as specified in section 4.2.2. The amplifier's input power is furthermore maintained at 4 mW as specified in section 4.3.1 of this work.

Figure 4.8 plots the power added efficiency (PAE) curves of the transistor on a Smith chart. The Smith chart represents the reflection coefficient presented to the transistor at 3.5 GHz. During this measurement, the reflection coefficients at 7.0 GHz and 10.5 GHz are held constant. The exact value of these reflections coefficients is unknown. However, it is known that their magnitudes are in the area of $|\Gamma| = 0.2$.

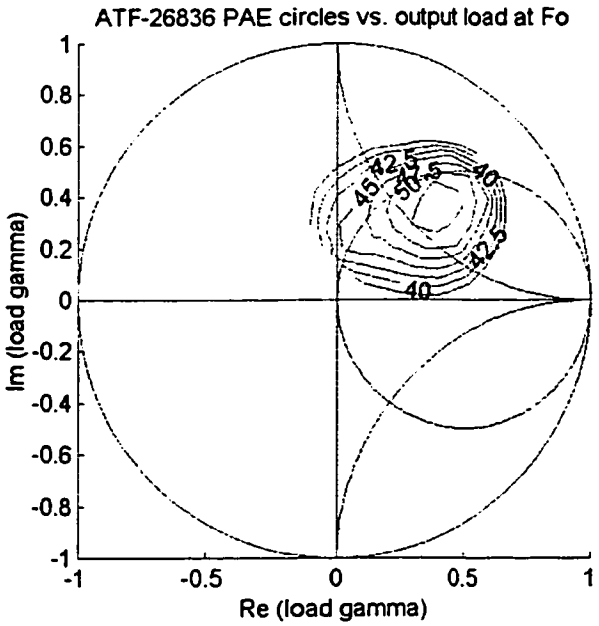

Figure 4.8 PAE Circles as a Function of Fundamental Output Load (PAE circles labelled in %)

Figure 4.8 clearly illustrates that an optimum PAE of 53.8% is achieved when $\Gamma_{L\,Fo} = 0.55\ \angle 39.4^{o}$.

A further increase in PAE can be obtained by choosing an appropriate transistor output load at the second harmonic frequency in addition to the output load at the fundamental frequency of the output signal. Since the goal of the amplifier design is to amplify the signal at 3.5 GHz, any signal power appearing at the harmonics is viewed as power "stolen" from the signal at the fundamental frequency. Experiment confirms this intuitive statement, indicating that the magnitude of the efficiency-enhancing reflection coefficients at the harmonics should be $|\Gamma_{HARMONICS}| = 1.0$.

Figure 4.9 shows the amplifier's PAE as a function of the phase of the reflection coefficient presented to the second harmonic component of the signal at the output of the amplifier. During this measurement, the reflection coefficient presented to the fundamental component of the signal at the output of the transistor is held constant at $\Gamma_{L\,Fo} = 0.55\ \angle 39.4^{o}$. In addition, $\Gamma_{L\,3Fo}$ is maintained constant at an unknown but small value ($|\Gamma| \approx 0.2$).

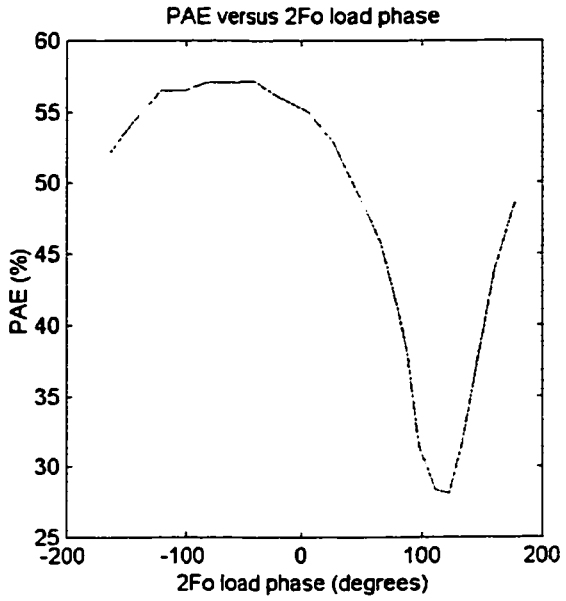

Figure 4.9 PAE as a Function of Second-Harmonic Load Phase

It is clear from figure 4.9 that a proper choice of $\angle\Gamma_{L\,2Fo}$ can increase the PAE of the amplifier from 53.8% to 57.1%. However, a poor choice of $\angle\Gamma_{L\,2Fo}$ will cause the amplifier's PAE to fall to less than 30%. This clearly illustrates the need to control the transistor's output load at the second harmonic when designing high-efficiency amplifiers.

Optimising only $\Gamma_{L\,Fo}$ and $\Gamma_{L\,2Fo}$, a PAE of 57.1% is obtained when $\Gamma_{L\,Fo} = 0.55\ \angle 39.3^{o}$ and $\Gamma_{L\,2Fo} = 0.99\ \angle -39.4^{o}$. However, it is clear in figure 4.9 that the amplifier's PAE remains fairly constant over the entire range of $-100^{o} \leq \angle\Gamma_{L\,2Fo} \leq -20^{o}$.

Finally, the reflection coefficient presented to the output of the transistor at the third harmonic is optimised. Again, the magnitude of this reflection coefficient is held constant at $|\Gamma_{L\,3Fo}| = 1.0$. During this measurement, the $\Gamma_{L\,Fo}$ is held constant at $\Gamma_{L\,Fo} = 0.55\ \angle 39.3^{o}$ and

$\Gamma_{L\,2Fo}$ is held constant at $\Gamma_{L\,2Fo} = 1.0\ \angle -39.4^{o}$. Figure 4.10 highlights the amplifier's PAE as a function $\angle\Gamma_{L\,3Fo}$.

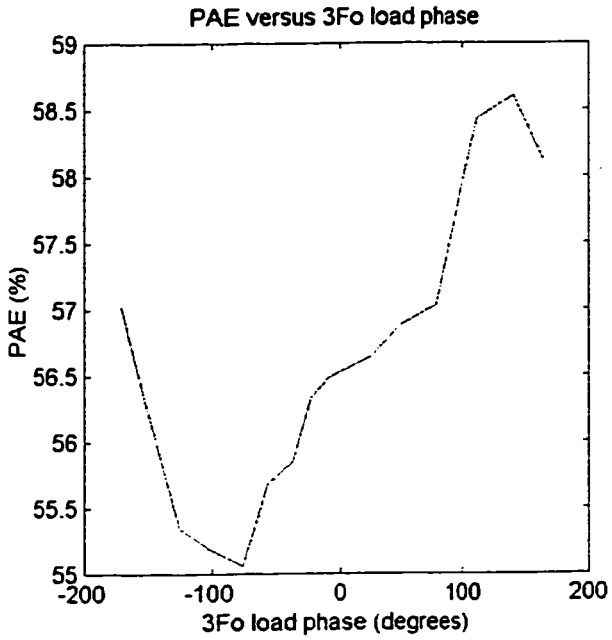

Figure 4.10 PAE as a Function of Third-Harmonic Load Phase

Examination of figure 4.10 reveals that optimisation of the reflection coefficient at the third harmonic does not provide such a significant improvement of the amplifier's PAE. Nonetheless, the PAE is increased from a value of 57.1% to a value of 58.6% when $\angle\Gamma_{L\,3Fo}$ is properly chosen. In addition, it is shown that an inadequate choice of $\angle\Gamma_{L\,3Fo}$ can decrease the amplifier's PAE to approximately 55%, effectively cancelling any improvement provided by optimising $\angle\Gamma_{L\,2Fo}$.

Clearly, the plot of figure 4.10 is not as smooth as that of figure 4.9. Unfortunately, it is shown in chapter 3 of this work that the load-pull system measures less accurately at

10.5 GHz than at 3.5 GHz and 7.0 GHz. Despite the presence of these measurement inaccuracies, the experimental result clearly indicates the benefit of choosing $\angle\Gamma_{L3Fo}$ intelligently.

The experimental characterisation of the transistor reveals that a power amplifier having PAE of 58.6% can be produced by appropriately choosing the output load of an ATF-26836 transistor. The final amplifier operates as illustrated in table 4.3.

Table 4.3	
Power Amplifier Operating Characteristics	
Drain-Source Bias Voltage (V_{DS})	3.0 V
Drain-Source Bias Current (I_{DS})	0.5 mA
Input Signal Power	4 mW = 6 dBm
Fundamental Signal Output Power	20.5 mW = 13.1 dBm
Amplifier Gain	7.1 dB
Power-Added-Efficiency	58.6%
Collector Efficiency	72.8%
Input Reflection Coefficient Γ_{IN}	$0.85\ \angle -60.3^{o}$
Fundamental Output Load Γ_{LFo}	$0.55\ \angle 39.5^{o}$
Second Harmonic Output Load Γ_{L2Fo}	$1.0\ \angle -38.8^{o}$
Third Harmonic Output Load Γ_{L3Fo}	$1.0\ \angle 142.4^{o}$

It is known that the theoretical maximum collector efficiency of a class B amplifier is 78.5% [17]. The value of 72.8%, though not in direct agreement with the theoretical maximum, is certainly respectable in its own right. In addition, published results indicate that power

amplifiers operated in a class B or class AB regime can achieve power-added efficiencies in the order of 50 to 70% [18, 19]. It is thus concluded that the performance of the power amplifier is consistent with previously published results.

Finally, the efficiency optimising values of $\angle\Gamma_{L\,2Fo}$ and $\angle\Gamma_{L\,3Fo}$ are consistent with an older theoretical analysis [20]. It is shown that at low frequencies, the efficiency of an amplifier operating in a class B mode is optimised when $\Gamma_{L\,2Fo} = 1.0\ \angle 180^{o}$ and $\Gamma_{L\,3Fo} = 1.0\ \angle 0^{o}$. The experiment above shows that the optimum $\angle\Gamma_{L\,2Fo}$ is -38.8^{o} and the optimum $\angle\Gamma_{L\,3Fo}$ is 142.4^{o}. At higher frequencies, the optimum loads are not so simply determined due to parasitic effects introduced by the active device and its packaging. However, it is interesting that both the theoretical analysis and the experimental measurement indicate that the optimum $\angle\Gamma_{L\,2Fo}$ and $\angle\Gamma_{L\,3Fo}$ must differ by approximately 180^{o}. This consistency of the experimental result with a theoretical analysis provides a certain degree of confidence in the accuracy of the load-pull measurements.

4.4 Power Amplifier Loading Circuit

Having experimentally determined the loads that must be presented to the transistor in order to maximise its power-added-efficiency, a circuit that produces these loads must be designed.

4.4.1 Numerical Design of Loading Circuit

The amplifier's loading circuit is designed using the Momentum numerical simulation

tool. Three internally-patterned series stubs are used to produce the optimum loads at the output of the transistor. Figure 4.11 illustrates the output loading network of the power amplifier.

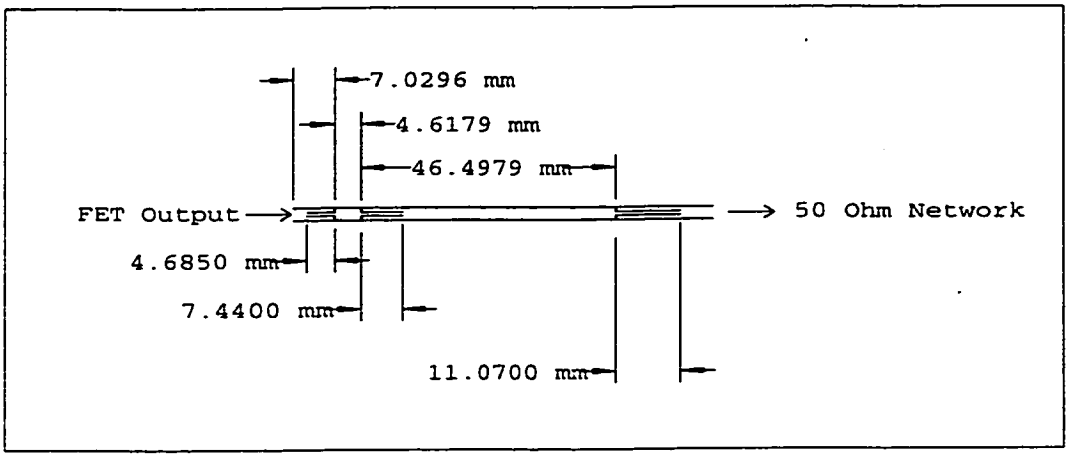

Figure 4.11 Power Amplifier Output Loading Network

As illustrated above, the network is comprised of a sequence of series coplanar stubs patterned inside the main coplanar waveguide's centre conductor. The 4.6850 mm long stub has an electrical length of $\lambda/4$ at 10.5 GHz. It produces the transistor's optimum efficiency-enhancing load at this frequency. The 7.4400 mm long stub has an electrical length of $\lambda/4$ at 7.0 GHz. It, in conjunction with the first stub, produces the transistor's optimum efficiency-enhancing load at 7.0 GHz. Finally, the output load at 3.5 GHz is provided by the 11.0700 mm stub in conjunction with the two first stubs. All three stubs are positioned along the main coplanar waveguide in order to optimise the phase of the loads presented to the transistor. Table 4.4 compares the simulated input reflection coefficient of the loading network to the optimum efficiency-enhancing reflection coefficients determined using the load-pull system.

Table 4.4		
Comparison of Simulated Loading Network Input Γ with Optimum Efficiency-Enhancing Γ		
Frequency	Simulated Network Γ	Optimum Γ
3.5 GHz	$0.547\angle 39.431^{o}$	$0.55\ \angle 39.5^{o}$
7.0 GHz	$0.990\ \angle -38.518^{o}$	$1.0\ \angle -38.8^{o}$
10.5 GHz	$0.988\ \angle 142.326^{o}$	$1.0\ \angle 142.4^{o}$

It is clear that the simulated coplanar waveguide loading circuit does indeed produce the optimum efficiency enhancing reflection coefficients at the output of the transistor.

4.4.2 Experimental Validation of the Output Loading Network

Experimental validation of the output loading network is performed using an HP-8510 network analyser manufactured by Hewlett-Packard.

Measurements taken with this device are obtained in a coaxial waveguide system. As in the load-pull system, these measurements are de-embedded to a reference plane in coplanar waveguide using the TRL de-embedding method. Table 4.5 compares the measured reflection coefficient of the loading network with the numerically simulated data.

Table 4.5		
Comparison of Measured Loading Network Input Γ with Simulated Loading Network Input Γ		
Frequency	Measured Γ	Simulated Γ
3.5 GHz	$0.626\ \angle\ 21.398^{o}$	$0.547\angle 39.431^{o}$
7.0 GHz	$0.938\ \angle -51.762^{o}$	$0.990\ \angle -38.518^{o}$
10.5 GHz	$1.004\ \angle 127.153^{o}$	$0.988\ \angle 142.326^{o}$

Table 4.5 unfortunately illustrates that the constructed power amplifier loading circuit does not properly produce the transistor's efficiency-enhancing loads. This is not completely surprising, as microwave circuit construction often requires more than one design iteration. The results above indicate that the circuit's performance differs most significantly from the simulated value at 3.5 GHz. Here, both the magnitude and the phase of the circuit's input reflection coefficient differ from the simulated value. At 7.0 GHz and 10.5 GHz, it is mostly the phase of the circuit's input reflection coefficient that is not consistent with the simulated values.

The behaviour of this circuit can be explained by referring to figure 4.11. As indicated earlier, the optimum fundamental-frequency efficiency-enhancing reflection coefficient of the transistor is produced by the stub that is located the farthest away from the device. This implies that this reflection coefficient depends on the performance of the first two stubs in addition to the accurate positioning and patterning of the third one. The reflection coefficient at 10.5 GHz, on the other hand, depends only on the first stub. In addition, the reflection coefficient at 7.0 GHz depends only on the first and second stub. It is thus clear that the reflection coefficient at 3.5 GHz is sensitive to a larger number of circuit parameters and thus, more subject to error.

The circuit, though its performance is not in complete agreement with the simulated result, may be salvaged. A minor tuning effort may result in a circuit that more accurately produces the transistor's efficiency-enhancing loads. Such a tuning effort will nonetheless be challenging, as coplanar waveguide is not easy to tune.

4.4.3 Power Amplifier Validation

Having examined the performance of the power amplifier's loading network, the power amplifier is now constructed and tested.

In order to validate the power amplifier design, the performance characteristics of the amplifier are measured. The input reflection coefficient and input power of the device are measured using a properly calibrated six-port circuit. The output power is simply measured using a power meter. Efficiency values are calculated using the measured current flowing through the device during operation. Table 4.6 compares the constructed power amplifier with the operating characteristics of the device-under-test in the load-pull system.

Table 4.6

Comparison of Constructed PA With Optimum Operating Characteristics of ATF-26836 FET

	Realised PA	Load-Pull PA Design
Drain-Source Bias Voltage (V_{DS})	3.0 V	3.0 V
Drain-Source Bias Current (I_{DS})	0.5 mA	0.5 mA
Input Signal Power	3.95 mW = 5.97 dBm	4 mW = 6 dBm
Fundamental Signal Output Power	9.08 mW = 9.58 dBm	20.5 mW = 13.1 dBm
Amplifier Gain	3.6 dB	7.1 dB
Power-Added-Efficiency	22.1%	58.6%
Collector Efficiency	39.1%	72.8%
Input Reflection Coefficient Γ_{IN}	$0.74 \angle -49.0^{o}$	$0.85 \angle -60.3^{o}$

As the power amplifier's loading circuit does not produce the transistor optimum efficiency-enhancing loads, it is not surprising that the amplifier itself does not function

optimally. However, it is clear that the improper loading of the active device produces a significant degradation in the ampifier's performance. Table 4.6 indicates that the realised amplifier's power-added-efficiency is only 22.1%, a value that is much smaller than the optimum 58.6%. The results shown in figure 4.8 indicate that, if the transistor's fundamental-frequency output load is moved from $\Gamma_L = 0.547\angle 39.431^o$ to $\Gamma_L = 0.626 \angle 21.398^o$, a decrease in PAE of approximately 8% can be expected. The 37% loss of efficiency observed in table 4.6 must thus be the result of the combined effect of the inappropriate transistor loads at all three frequencies of interest. This is a dramatic illustration of the importance of adequate harmonic control at the output of high efficiency power amplifiers.

At this point, the optimum efficiency-enhancing terminations of the Agilent ATF-26836 transistor have been determined. Numerical simulation indicates that these loads can be physically realised with an appropriate circuit constructed in coplanar waveguide. Unfortunately, the constructed circuit's performance does not correspond exactly to numerically predicted performance. Nonetheless, the feasibility of the amplifier's realisation is demonstrated. An in-depth study of the constructed amplifier will likely reveal the source of its performance degradation and a second design iteration will produce a much better circuit.

4.5 Chapter 4 References

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CHAPTER 5

Active Antenna Construction

5.1 Active Antenna Structures

Having evaluated the performance of a high-efficiency power amplifier, an active antenna is now studied.

Not all antenna structures are suitable for the construction of active antennas. An appropriate antenna must have physical characteristics that can allow for impedance tuning while not significantly compromising the device's radiation characteristics.

5.1.1 Previously Published Active Antennas

The study of active antennas has already attracted significant attention in the research community [1, 2]. However, most published antennas are constructed using the microstrip waveguide technology [3 - 6]. In addition, many publications illustrate designs that make use of photonic band gap structures and other methods for producing the optimum load terminations at the harmonic frequencies [7 - 9].

A few papers do highlight active antennas designed using the coplanar waveguide. However, most of these make use of coplanar-fed slot antennas [10, 11]. In addition, most of these antenna-amplifiers are designed using simulation techniques, not experimental device characterisation techniques such as load-pulling.

5.1.2 Radiators Suitable for Active Antenna Design

As indicated earlier, an antenna that is useful for the implementation of an active antenna must allow for input impedance tuning without excessively compromising the radiation pattern. It is clear nonetheless that any impedance tuning will involve a compromise with some other antenna performance parameter.

A significant body of existing work analyses the impedance characteristics of microstrip-fed or aperture-coupled microstrip-fed patch antennas [12 - 14]. Stacked antennas are also analysed extensively in the literature [15 - 17]. These latter antennas are interesting since they are most often composed of arrayed antenna stacks. The presence of many radiating elements is quite useful, as it provides for impedance tuning capabilities. Unfortunately, such stacked antennas are difficult to fabricate.

Coplanar-waveguide-fed slot antennas are also analysed in detail in published literature [18 - 23]. Unfortunately, these antennas are not very useful in impedance tuning applications, as only the length and width of the slot can be used to vary its impedance.

One of the most useful structures for active antenna implementation is the coplanar-waveguide-fed slot-coupled patch antenna [24 - 26]. This antenna is very simple to construct, as its fabrication requires only the patterning of metal on both sides of commercially-available microwave substrate. In addition, its input impedance can be tuned by varying a surprisingly large number of the antenna's physical parameters [27, 28]. Figure 5.1 illustrates the many

antenna parameters that are useful in tuning its impedance. Additional publications also highlight creative slot designs that also provide input impedance tuning capability [29, 30].

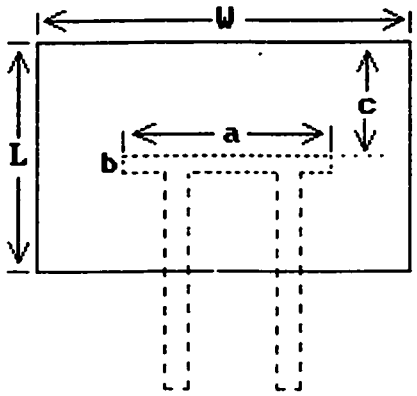

Figure 5.1 CPW-Fed Slot-Coupled Patch and Its Impedance Tuning Parameters

As mentioned earlier, the CPW-fed slot-coupled patch antenna has many physical parameters that can be used to tune its input impedance. Figure 5.1 highlights them. Here, W is the patch antenna's width and L is the patch antenna's length. The length L determines the frequency f_r at which the patch radiates. It is clear that the input impedance of the patch is affected at a given frequency when L is changed. It is known that the value of W must be adequately chosen to obtain a patch antenna with good radiation characteristics [31]. Changing this value of W does change the antenna's input impedance. However, too large a change in W will compromise the antenna's radiation efficiency.

The physical parameters of the coupling slot will also affect the antenna's input impedance. Here, the parameter a is the coupling slot length, b is the coupling slot width and c is the distance between the top of the patch and the coupling slot. Interestingly, the magnitude of the antenna's input reflection coefficient is decreased by an increase in a or b. Again here, too large a value for parameter a or parameter b compromises the antenna's radiation efficiency. In this case, it is the antenna's front-back radiation ratio that suffers [27, 28]. Optimally, the slot length a should be as wide as the signal feeding waveguide (3.18 mm in this case) and the slot width b should be similar to the coplanar waveguide's slot width (0.09 mm in this case).

Interestingly, the position of the slot under the patch affects mostly the phase of the antenna's input reflection coefficient. However, this parameter also allows for impedance tuning at twice the resonant frequency of the antenna ($2f_r$). Specifically, if the parameter c is chosen such that the coupling slot is directly centred under the patch, the magnitude of the input reflection coefficient at $2f_r$ will be 1. This may be useful for producing a power amplifier's efficiency-enhancing load at the second harmonic.

For these reasons, the CPW-fed slot-coupled patch antenna is chosen for the implementation of the active antenna. Using this antenna structure, a compact, easily fabricated, active antenna can be realised on a single substrate.

5.2 Coplanar-Waveguide-Fed Slot-Coupled Patch Antenna Design

5.2.1 Design of the CPW-Fed Slot-Coupled Patch Antenna Using Empirical Formulas

The patch antenna is one of the most extensively studied antenna structures. Well-known mathematical formulas allow for the design of such an antenna [31].

The width of a patch antenna can be calculated given its radiant frequency (f_r), the velocity of radiation in the medium surrounding the patch (c), and the substrate dielectric constant (ϵ_r).

$$W = \frac{c}{2 f_r \sqrt{\frac{2}{\varepsilon_r + 1}}} \quad (5.1)$$

The length of the patch is given as follows:

$$L = \frac{c}{2 f_r \sqrt{\varepsilon_{reff}}} - 2\Delta L \quad (5.2)$$

where ϵ_{reff} is given in terms of the ϵ_r and the ratio of patch width W to substrate height h as follows:

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + 12\frac{h}{W}\right]^{-\frac{1}{2}} \quad (5.3)$$

The length correction ΔL is also calculated in terms of ϵ_{reff} and the ratio of patch width W to substrate height h.

$$\frac{\Delta L}{h} = 0.412\left\{\frac{\left(\varepsilon_{reff} + 0.3\right)\left(\frac{W}{h} + 0.264\right)}{\left(\varepsilon_{reff} - 0.258\right)\left(\frac{W}{h} + 0.8\right)}\right\} \quad (5.4)$$

The above relations indicate that a patch antenna constructed on Rogers' RT Duroid 5880 and designed to radiate at 3.5 GHz must have length L = 28.5 mm and width W = 33.9 mm.

5.2.2 CPW-Fed Slot-Coupled Patch Antenna Design Using Numerical Simulator

In order to verify the above antenna design, a numerical simulation of the antenna's characteristics is performed using Agilent Technologies' Momentum simulation tool.

A slight modification of the original antenna produces an optimally resonant radiator at 3.5 GHz. The dimensions of the optimised antenna are illustrated in figure 5.2. Here, L = 28.00 mm, W = 33.90 mm, a = 3.18 mm, b = 0.09 mm, and c = 13.955 mm.

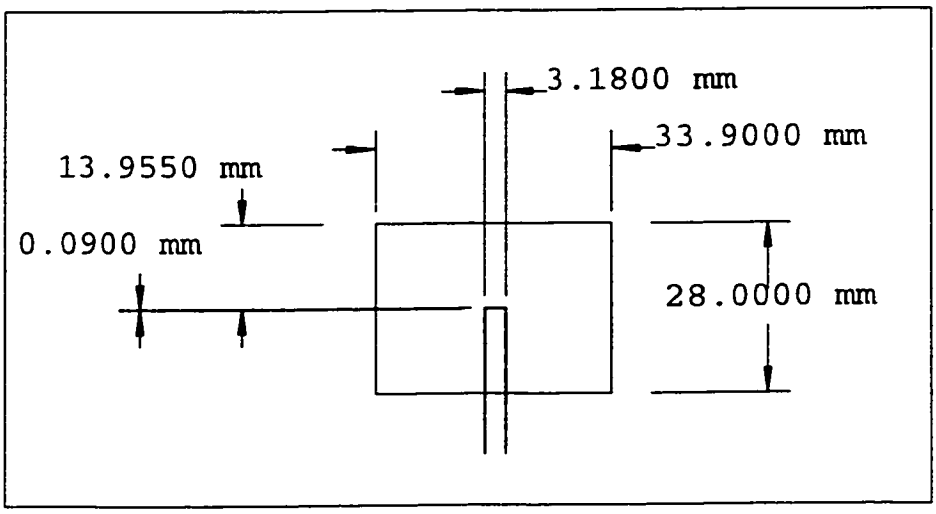

Figure 5.2 Dimensions of 3.5GHz CPW-Fed Slot-Coupled Patch

Figure 5.3 illustrates the antenna's input reflection coefficient as a function of frequency. Though not a rigorous confirmation of the antenna's exact resonant frequency, the figure does nonetheless show that the antenna does radiate at 3.5 GHz.

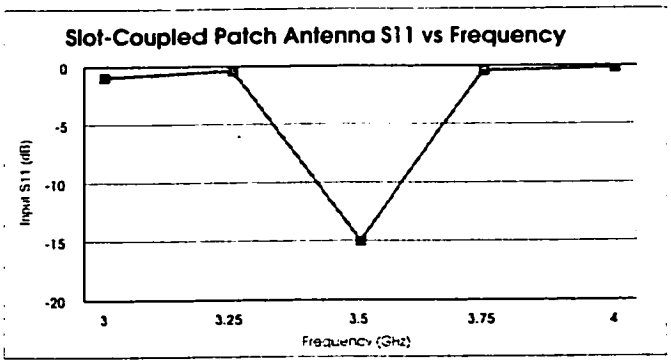

Figure 5.3 CPW-Fed Slot-Coupled Patch Antenna Input Impedance

In addition, the antenna's input reflection coefficient at $2f_r$ is $\Gamma_{7GHz} = 0.971 \angle -160.40^{\circ}$. It is clear that the magnitude of this reflection coefficient is very nearly equal to 1.0 and thus, the antenna may be used for providing the second harmonic termination of the transistor.

5.3 Active Antenna Design

Having chosen an appropriate antenna structure, the active antenna is now conceived and constructed.

5.3.1 Active Antenna Architectures

The goal of this exercise is to create a radiating structure that produces the optimal efficiency-enhancing terminations at the output of the transistor, thus operating as a high-efficiency power amplifier. As the active device is embedded inside this structure, a means of applying a DC bias signal to this device without perturbing the high frequency signals must be devised. Figure 5.4 illustrates an interesting and effective active antenna architecture.

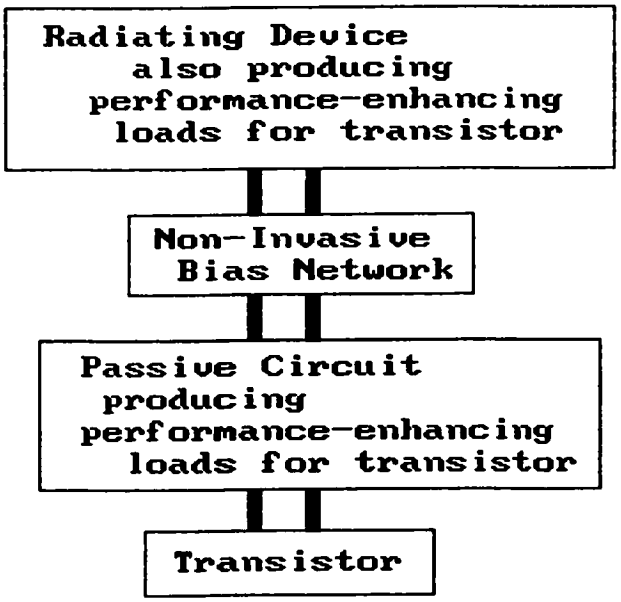

Figure 5.4 Conceptual Diagram of Transmitting Active Antenna

5.3.2 Design and Experimental Validation of Bias Network

A number of methods allow for the delivery of the drain bias signal to the transistor.

One method consists of connecting a very fine, high impedance wire directly to the transistor's drain pad. Unfortunately, experiment has shown that this bias application system significantly perturbs the microwave signal travelling along the coplanar waveguide.

Another method consists of the design and construction of a more traditional bias tee. Figure 5.5 illustrates an adequate bias tee constructed using the coplanar waveguide technology highlighted in chapter 4.

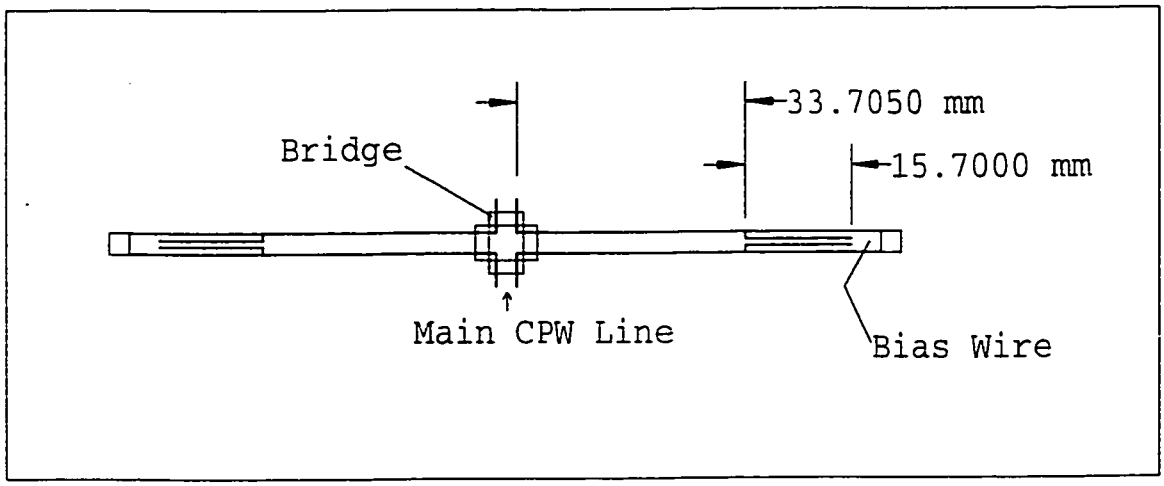

Figure 5.5 Bias Tee

In the circuit of figure 5.5, the 15.70 mm stub fully reflects any 3.5 GHz signal component travelling along the arms of the bias tee. This produces a section of waveguide that is isolated from the main coplanar line at 3.5 GHz, thus producing a convenient location for attaching a wire for the purpose of delivering the transistor's bias signal. The stub's location away from the main

coplanar line is chosen in order to produce an open circuit in parallel with this main line. This produces a bias tee that does not perturb the signal travelling along this main coplanar waveguide.

The bias tee is designed as a symmetric circuit as this architecture does not excite the coupled slot-line mode as significantly as an asymmetric design. To suppress any excitation of the coupled slot-line mode, bridges are constructed to connect the waveguide ground planes as recommended in chapter 4 of this work. Unfortunately, the coupled slot-line mode is not adequately suppressed by these bridges at 7.0 GHz and 10.5 GHz. This implies that the bias tee only functions correctly at 3.5 GHz. Consequently, all circuitry used to produce the transistor's efficiency-optimising loads at 7.0 GHz and 10.5 GHz must be located between the device's output port and the bias tee. Otherwise, the signal components at these frequencies will excite the coupled slot-line mode and radiate away unpredictably.

In order to verify the operation of the bias tee, the circuit's measured s-parameters are compared to numerically simulated values. Table 5.1 illustrates this comparison.

Table 5.1

Comparison of Measured and Numerically Simulated Bias Tee S-Parameters at 3.5 GHz

Parameter	Simulated Value	Measured Value
S_{11}	$0.052 \angle 14.508^{o}$	$0.030 \angle -77.4^{o}$
S_{21}	$0.987 \angle -73.876^{o}$	$0.944 \angle -86.5^{o}$
S_{12}	$0.987 \angle -73.876^{o}$	$0.944 \angle -86.3^{o}$
S_{22}	$0.052 \angle 14.508^{o}$	$0.069 \angle 78.0^{o}$

The results illustrated in table 5.1 indicate that the bias tee does indeed function properly. The parameters S_{21} and S_{12} indicate that the signal at 3.5 GHz travelling along the main coplanar waveguide is unperturbed by the bias tee. However, the measured circuit's s-parameters do not coincide exactly with the simulated values.

The most problematic elements of the bias tee circuit are certainly the coupled slot-line mode suppressing bridges. Such structures are indeed difficult to model accurately. In addition, the bridges of the bias circuit are constructed by soldering thin wires between bridge planes patterned on the back of the circuit's substrate and the ground plane patterned on the front of the substrate. This fabrication task is performed manually. and is thus not very repeatable. This problem can be eliminated by making use of a more repeatable bridge fabrication technique (like a via hole construction process provided by a professional MMIC fabricator). Having established a repeatable bridge fabrication process, a more rigorous numerical model of the bridge can be developed.

5.3.3 Revised Active Antenna Architecture

As indicated earlier, the fact that the circuit available for applying the transistor's bias signal is not functional at 7.0 GHz and 10.5 GHz imposes a major design constraint on the active antenna. Specifically, all circuitry needed to provide the transistor's efficiency-enhancing loads at these frequencies must be placed between the transistor's output port and the bias tee. Figure 5.6 illustrates a feasible architecture for an active antenna constructed using the available bias tee and the CPW-fed slot-coupled patch antenna.

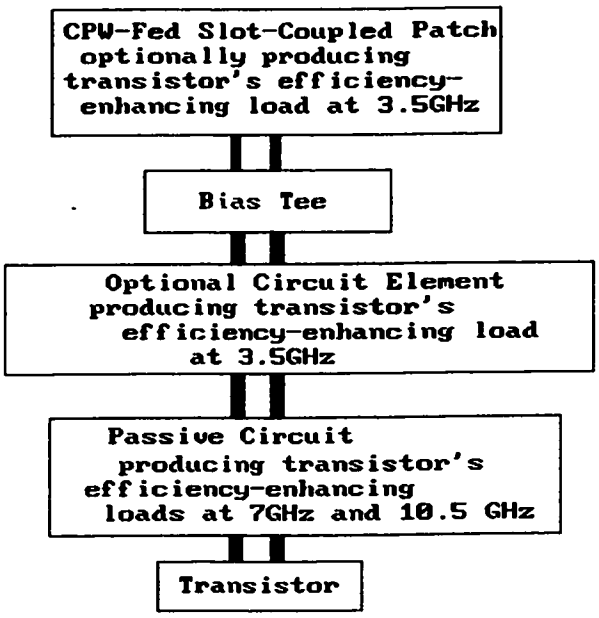

Figure 5.6 Active Antenna Architecture Making Use of CPW-Fed Slot-Coupled Patch and Available Bias Network

5.3.4 Design and Experimental Validation of Harmonic Loading Circuit

In order to produce the transistor's optimum efficiency-enhancing loads at the harmonic frequencies, a circuit comprised of two internally patterned series resonant stubs is placed immediately at the output of the transistor. The circuit is illustrated in figure 5.7.

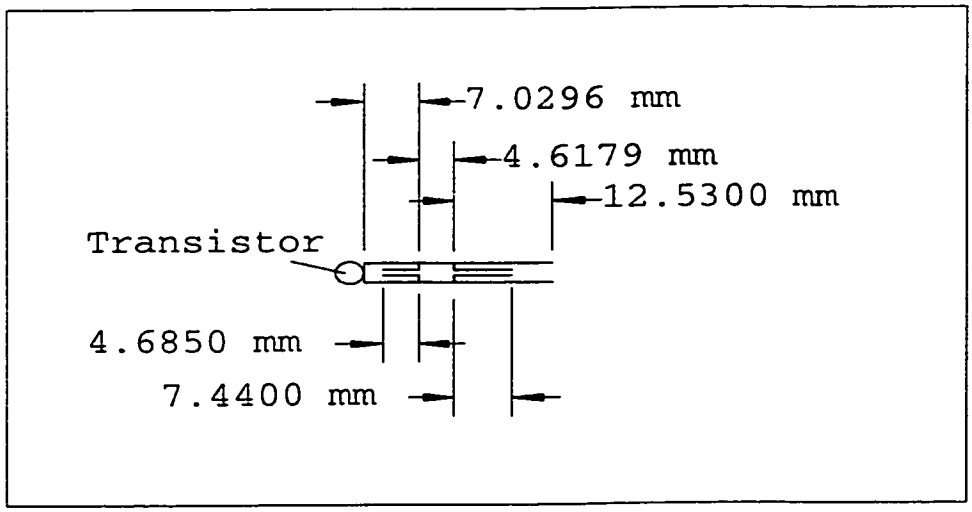

Figure 5.7 Harmonic Frequency Loading Circuit

In figure 5.7, the 4.685 mm stub produces $|\Gamma| = 1.0$ at 10.5 GHz. The distance between this stub and the transistor drain is chosen to produce the optimum efficiency-enhancing load at 10.5 GHz. The 7.440 mm stub produces $|\Gamma| = 1.0$ at 7.0 GHz. The distance between this stub and the previous stub is chosen to optimally load the transistor at 7.0 GHz.

In order to validate the harmonic loading circuit, the numerically simulated s-parameters are compared with measured values. Table 5.2 illustrates this comparison.

Table 5.2

Comparison of Measured and Simulated Harmonic Loading Circuit S-Parameters

3.5 GHz	Simulated Value	Measured Value
S_{11}	0.511 ∠ -48.524°	0.553 ∠ -58.24°
S_{21}	0.857 ∠ -158.939°	0.805 ∠ -164.75°
S_{12}	0.857 ∠ -158.939°	0.807 ∠ -164.67°
S_{22}	0.510 ∠ -89.456°	0.537 ∠ -92.86°
7.0 GHz		
S_{11}	0.990 ∠ -38.507°	0.941 ∠ -40.65°
S_{21}	0.020 ∠ -54.768°	0.023 ∠ 73.20°
S_{12}	0.020 ∠ -54.768°	0.023 ∠ 73.58°
S_{22}	0.993 ∠ 102.921°	0.928 ∠ 93.96°
10.5 GHz		
S_{11}	0.988 ∠ 142.326°	1.02 ∠ 148.81°
S_{21}	0.019 ∠ 57.961°	0.028 ∠ 35.05°
S_{12}	0.019 ∠ 57.961°	0.028 ∠ 34.91°
S_{22}	0.972 ∠ -92.709°	0.903 ∠ -111.48°

Examination of the information presented in table 5.2 indicates that the measured values of S_{11} and S_{22} correspond fairly well with the numerically simulated values. Specifically, the measured values of S_{11} at 7.0 GHz and 10.5 GHz do correspond to the simulated values. A maximum phase difference of only 6^{O} is observed between the measured values of S_{11} and the simulated values of S_{11}. As the transistor's drain pad is connected to port 1 of the harmonic loading circuit, it is clear that the circuit does indeed produce the efficiency-enhancing loads at the output of the device. An examination of figures 4.9 and 4.10 indicates that the measured phase values of the circuit remain well within the transistor's maximum efficiency operation zone.

Interestingly, there is a more significant difference between the measured values and the simulated values of the phase of S_{21} and S_{12} at all frequencies. This difference is most significant at 7.0 GHz, but even at 3.5 GHz a phase difference as high as 6^{O} is observed. At 10.5 GHz, the difference between the measured and simulated value is in the area of 20^{O}.

At 3.5 GHz, the measured values of S_{11} and S_{22} also differ from the simulated values. The measured magnitude of these parameters is slightly larger than the simulated values. As the transistor's efficiency-enhancing load at 3.5 GHz is created with an additional circuit element located beyond the harmonic loading circuit, accurate values of the harmonic loading circuit's s-parameters are required if the antenna is to be accurately designed. A numerical simulation tool that more accurately predicts the circuit's performance is also desirable.

5.4 Active Antenna Using Slot-Coupled Patch as Radiating Element Only

One active antenna architecture consists of making use of the slot-coupled patch antenna as a radiating element only. An additional internally-patterned series stub is added to optimally load the transistor at the fundamental frequency.

5.4.1 Numerical Design of Active Antenna Using Slot-Coupled Patch as Radiator Only

The antenna is designed using the Momentum simulation tool. However, as the complete active antenna circuit is too large to be practically simulated, its design is broken down into more manageable blocks.

First, the s-parameters of the slot-coupled patch (presented in section 5.2.2), the bias network (presented in section 5.3.2), and the harmonic loading circuit (presented in section 5.3.4) are simulated using Momentum. Then, the input reflection coefficient of the cascaded bias tee and patch antenna is computed using well-known relations describing the combined effect of cascaded s-parameter blocks [32]. Using the same equations, it is possible to compute the reflection coefficient required at the output of the harmonic loading circuit in order to produce the transistor's fundamental-frequency efficiency-enhancing load at the input of this circuit. The design of the active antenna now reduces to the computation of a two-port s-parameter block that takes the input reflection coefficient of the combined bias tee / patch antenna, and produces the required reflection coefficient at the output of the harmonic loading circuit.

The s-parameters of such a circuit can be computed if a few simplifying assumptions are

made. First, it is clear that, in this application, the s-parameter block must be entirely passive. In an ideal circuit, this implies that S_{21} and S_{12} must be equal. Secondly, it is assumed that the s-parameter block has $S_{11} = S_{22}$. Utilising a search routine programmed in Matlab, it is found that the required circuit must have s-parameters approximately as follows:

$S_{11} = S_{22} = 0.590 \angle 61.00^{o}$ and $S_{21} = S_{12} = 0.807 \angle 171.00^{o}$. Using Momentum, it is found that a single internally-patterned series stub embedded appropriately inside a segment of coplanar waveguide has s-parameters $S_{11} = 0.674 \angle 65.80^{o}$, $S_{22} = 0.676 \angle 66.05^{o}$, and $S_{12} = S_{21} = 0.732 \angle 156.04^{o}$. This circuit transforms the reflection coefficient of the bias tee / patch cascade to the appropriate reflection coefficient at the output of the harmonic loading circuit.

The active antenna designed using this stub is illustrated in figure 5.8.

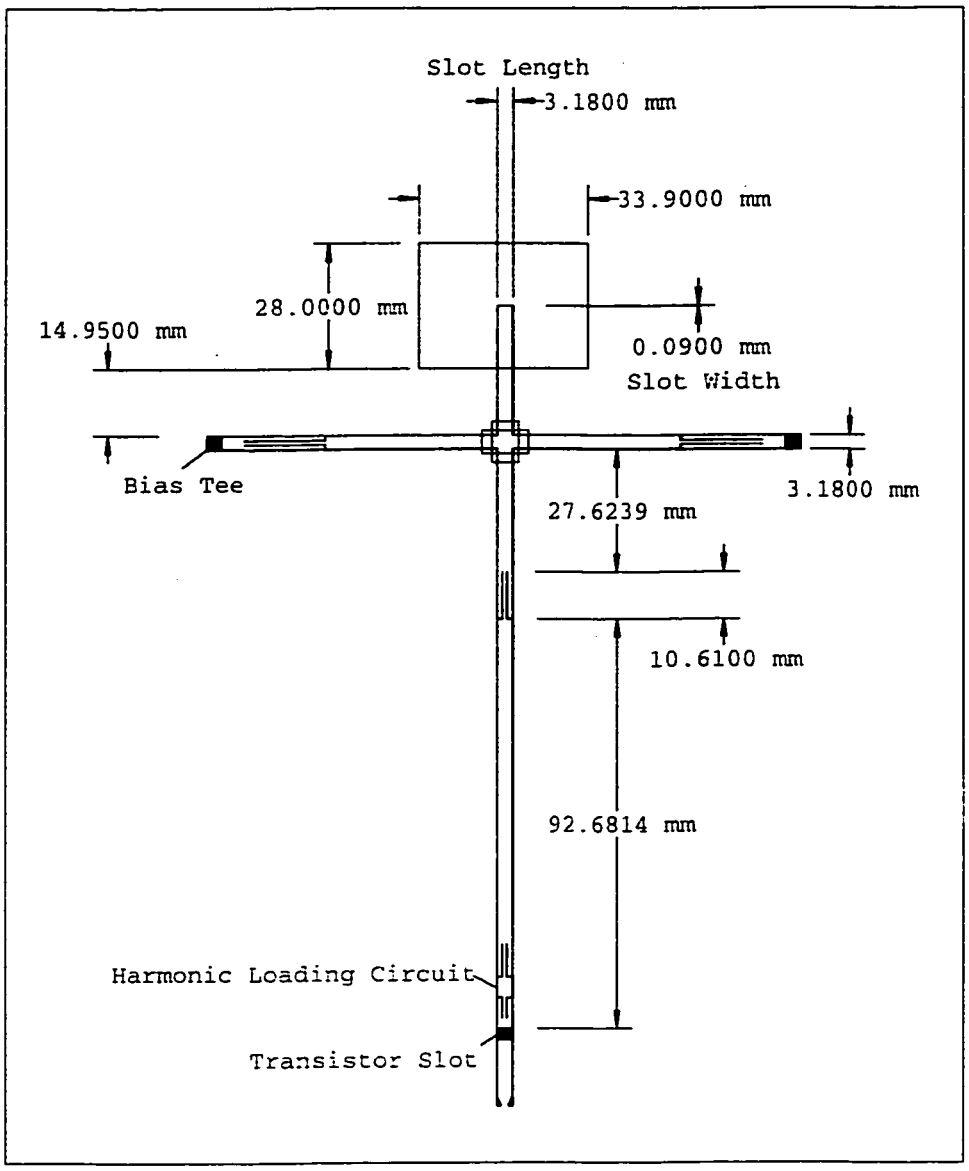

Figure 5.8 Active Antenna Using Slot-Coupled Patch as Radiation Element Only

In figure 5.8, the CPW-fed slot-coupled patch antenna is exactly as highlighted in section 5.2.2, the bias tee is as shown in section 5.3.2, and the harmonic loading circuit is as illustrated in section 5.3.4.

As indicated earlier, the Momentum simulation tool permits the numerical evaluation of the s-parameters of the individual constitutive components of the active antenna. The reflection coefficient presented to the transistor by the cascade of these individual components is computed using Matlab. Table 5.3 compares the computed input reflection coefficients of the antenna with the optimum efficiency-enhancing loads of the transistor.

Table 5.3

Comparison of Calculated Antenna Input Impedance with Optimum Transistor Loads

Frequency	Calculated Antenna Input Γ	Efficiency-Enhancing Load
3.5 GHz	$0.55 \angle 39.5^{o}$	$0.55 \angle 39.5^{o}$
7.0 GHz	$0.990 \angle -38.507^{o}$	$1.0 \angle -38.8^{o}$
10.5 GHz	$0.988 \angle 142.326^{o}$	$1.0 \angle 142.4^{o}$

In table 5.3. only the antenna's input reflection coefficient at 3.5 GHz is computed via the cascade of its constitutive elements. At the two other frequencies. the antenna's input reflection coefficients are taken to be identical to those of the harmonic loading circuit. This is a valid assumption, since the magnitude of the harmonic loading circuit's reflection coefficients is very near unity at these frequencies. This implies that the circuitry located beyond the harmonic loading circuit has a minimal impact on the reflection coefficient seen at the input of this circuit. It is clear that the calculated antenna's input reflection coefficients are in good agreement with the transistor's efficiency-enhancing loads.

5.4.2 Experimental Verification of the Antenna's Input Impedance

The antenna's input impedance is verified using an automatic network analyser and a TRL de-embedding routine. Table 5.4 compares the antenna's measured input impedance with the transistor's optimum efficiency-enhancing loads.

Table 5.4

Comparison of Measured Antenna Reflection Coefficients with Transistor's Optimum Loads

Frequency	Measured Input Γ	Efficiency-Enhancing Load
3.5 GHz	$0.39 \angle 34.6^{o}$	$0.55 \angle 39.5^{o}$
7.0 GHz	$0.95 \angle -22.0^{o}$	$1.0 \angle -38.8^{o}$
10.5 GHz	$1.01 \angle 158.9^{o}$	$1.0 \angle 142.4^{o}$

Interestingly, the input reflection coefficient of the circuit at 3.5 GHz has a magnitude that is smaller than that of the transistor's efficiency-enhancing load. It is possible that the stub added for the purpose of producing this efficiency-enhancing load is not correctly implemented. Earlier experimentation has illustrated that both the physically realised bias tee and the harmonic loading circuit do not perform exactly as simulated, and the active antenna circuit is designed using a numerical evaluation of the performance of these circuits. Fortunately, the fundamental-frequency loading stub can be tuned. Thus, its contribution to the input reflection coefficient of the antenna can be evaluated.

Secondly, the measured phase of both harmonic terminations differs from the optimum phase by approximately 17^{o}. In addition, the measured phase of the input reflection coefficient at 10.5 GHz is only 10^{o} larger than the measured phase of the harmonic loading circuit while the phase of the input reflection coefficient at 7.0 GHz is approximately 18^{o} larger than the measured

phase of the harmonic loading circuit. Interestingly, the magnitude of the active antenna's input reflection coefficient at both 7.0 GHz and 10.5 GHz corresponds nearly exactly to the magnitude of the input reflection coefficient of the harmonic loading circuit. In addition, the magnitude of the harmonic loading circuit's input reflection coefficient is approximately 0.95 at 7.0 GHz and approximately 1.0 at 10.5 GHz. It is thus plausible that the more significant phase error observed at 7.0 GHz is the result of a signal perturbation caused by the circuitry that is located beyond the harmonic loading circuit. The presence of a phase error at 10.5 GHz despite the unity magnitude of the input reflection coefficient at this frequency may be the result of fabrication process variations or of a minute excitation of the coupled slot-line mode.

It is clear at this point that the implementation of the suggested active antenna is physically feasible. Unfortunately, the input reflection coefficient of the fabricated device does not correspond exactly to that predicted using the Momentum simulator. However, it is possible that a minor tuning effort will resolve the problem. At the very least, the impact of the stub producing the fundamental-frequency efficiency-enhancing load on the performance of the circuit will be understood. Further experimentation is likely to establish the relationship between the physical device's performance and the numerically simulated result. Thus, a second design iteration will certainly improve the active antenna's performance.

5.5 Active Antenna Using CPW-Fed Slot-Coupled Patch as Radiating Element and Impedance Tuning Element

It is also possible to construct an active antenna where the slot-coupled patch serves to optimally load the transistor in addition to its function as a radiating element.

5.5.1 Numerical Design of Active Antenna

This antenna is designed using the Momentum simulation tool. Once again, the complete active antenna circuit is too large to be practically simulated, and thus, its design is broken down into more manageable blocks.

Here, the s-parameters of the bias tee (as presented in section 5.3.2) and those of the harmonic loading circuit (as presented in section 5.3.4) are simulated using the Momentum simulation tool. These s-parameters are then used to calculate the combined effect of the harmonic loading circuit cascaded with the bias tee using well-known relations [32]. Having computed the s-parameters of the bias-tee / harmonic loading circuit cascade, these new s-parameters are used to find the reflection coefficient that must be seen at the output of the bias tee in order to obtain the transistor's fundamental-frequency efficiency-enhancing load at the input of the harmonic loading circuit. The active antenna design then reduces to the problem of designing a CPW-fed slot-coupled patch that produces the correct reflection coefficient at the output of the bias tee.

The design of such a CPW-fed slot-coupled patch antenna is tackled using the Momentum simulation tool. Numerical experimentation has revealed that augmenting the coupling slot's length and the coupling slot's width only further decreases the input reflection coefficient of the antenna presented in section 5.2.2. Thus, the magnitude of the antenna's input reflection coefficient is augmented by altering the patch's length L. This unfortunately means that the patch antenna is not operated at its optimal radiant frequency.

The final design is illustrated in figure 5.9.

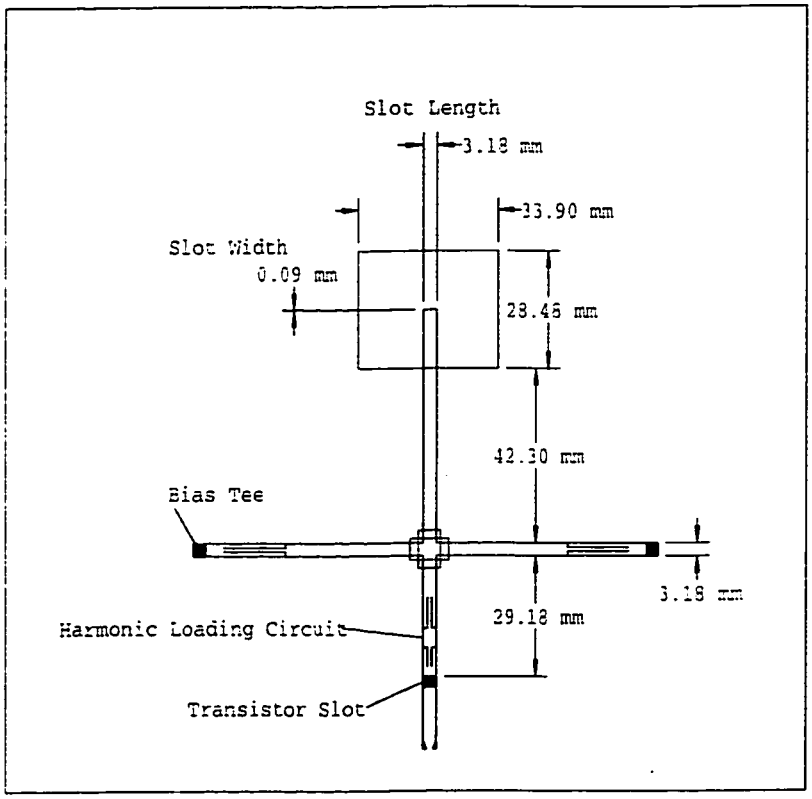

Figure 5.9 Active Antenna Using Slot-Coupled Patch as Radiation Element and Transistor Loading Element

In figure 5.9, it is clear that the dimensions of the coupling slot are identical to those presented in section 5.2.2 of this work. More specifically, the slot length is a = 3.18 mm, the slot width is b = 0.09 mm. In addition, the position of the slot under the patch is maintained at c = 13.955 mm and the width of the patch is maintained at W = 33.9 mm. However, the patch length is changed to a value of L = 28.48 mm from a value of L = 28.00 mm.

The simulation tool permits the numerical evaluation of the s-parameters of the active antenna. Table 5.5 compares the numerically computed input reflection coefficients of the antenna with the optimum efficiency-enhancing loads of the transistor.

Table 5.5

Comparison of Simulated Antenna Input Impedance with Optimum Transistor Loads

Frequency	Simulated Antenna Input Γ	Efficiency-Enhancing Load
3.5 GHz	$0.539 \angle 40.388^{o}$	$0.55 \angle 39.5^{o}$
7.0 GHz	$0.990 \angle -38.507^{o}$	$1.0 \angle -38.8^{o}$
10.5 GHz	$0.988 \angle 142.326^{o}$	$1.0 \angle 142.4^{o}$

In table 5.5, only the antenna's input reflection coefficient at 3.5 GHz is computed via the cascade of its constitutive elements. At the two other frequencies, the antenna's input reflection coefficients are taken to be identical to those of the harmonic loading circuit. As highlighted earlier, this assumption is valid since the magnitude of the harmonic loading circuit's reflection coefficients is very near unity at these frequencies. This implies that the circuitry located beyond the harmonic loading circuit has a minimal impact on the reflection coefficient seen at the input of this circuit. Clearly, the simulated antenna's input reflection coefficients are in good agreement with the transistor's efficiency-enhancing loads.

5.5.2 Experimental Verification of the Antenna's Input Impedance

Again, the antenna's input impedance is verified using an automatic network analyser and a TRL de-embedding routine. Table 5.6 compares the antenna's measured input impedance with the transistor's optimum efficiency-enhancing loads.

Table 5.6

Comparison of Measured Antenna Reflection Coefficients with Transistor's Optimum Loads

Frequency	Measured Input Impedance	Efficiency-Enhancing Load
3.5 GHz	$0.68 \angle 2.2^{o}$	$0.55 \angle 39.5^{o}$
7.0 GHz	$0.95 \angle -35.9^{o}$	$1.0 \angle -38.8^{o}$
10.5 GHz	$1.01 \angle 150.9^{o}$	$1.0 \angle 142.4^{o}$

Table 5.6 clearly illustrates the input reflection coefficient of the circuit at 3.5 GHz has a magnitude that is larger than that of the transistor's efficiency-enhancing load. It is also evident that the phase of the antenna's input reflection coefficient at 3.5 GHz is not coincident with the transistor's fundamental-frequency efficiency-enhancing load. This is likely to be the result of poor concordance between the simulation tool's treatment of the CPW-fed slot-coupled patch antenna and the physical device's characteristics. Accurate numerical modelling of antenna performance is often more difficult than accurate numerical treatment of non-radiative structures. In addition. earlier experimentation has illustrated that both the physically realised bias tee and the harmonic loading circuit do not perform exactly as simulated. As the active antenna circuit is designed using a numerical evaluation of the performance of these circuits, it is clear that an error is introduced in the simulation result. A careful study of the relationship between circuit performance as simulated by Momentum and actual device operation will lead to a better understanding of the antenna.

Secondly, this active antenna performs much better at the harmonic frequencies than the antenna presented in section 5.4 of this work. Here, the difference between the phase of the harmonic loads of the realised antenna and the phase of the transistor's efficiency-enhancing loads is only 3^{o} to 9^{o}. Furthermore, the measured phase of the input reflection coefficient at 10.5 GHz is only 2^{o} larger than the measured phase of the harmonic loading circuit while the phase of the input reflection coefficient at 7.0 GHz is approximately 5^{o} larger than the measured phase of the harmonic loading circuit. Interestingly, the magnitude of the active antenna's input reflection coefficient at both 7.0 GHz and 10.5 GHz corresponds nearly exactly to the magnitude of the input reflection coefficient of the harmonic loading circuit. In addition, the magnitude of the harmonic loading circuit's input reflection coefficient is approximately 0.95 at 7.0 GHz and approximately 1.0 at 10.5 GHz. It is thus plausible that the more significant phase error observed at 7.0 GHz is the result of a signal perturbation caused by the circuitry that is located beyond the harmonic loading circuit. The presence of a phase error at 10.5 GHz despite the unity magnitude of the input reflection coefficient at this frequency may once again be the result of fabrication process variations or of a minute excitation of the coupled slot-line mode.

It is clear at this point that the implementation of this second active antenna is also physically feasible. The study of this antenna in conjunction with that presented in section 5.4 will result in a more thorough understanding of the limitations of the numerical simulator and the operating characteristics of the antenna's constitutive components. It is likely that a second design iteration will produce an antenna that does indeed produce the transistor's efficiency-enhancing terminations.

At this point, it is clear that two proposed active antenna architectures making use of a CPW-fed slot-coupled patch antenna are physically realisable. Despite the fact that currently realised antennas do not optimally load the transistor, further study is highly likely to result in the realisation of antennas that do so.

5.6 Chapter 5 References

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CHAPTER 6

Conclusion

6.1 Research Summary

This thesis presents the design of active transmitting antenna's integrated with a high efficiency power amplifier.

A high efficiency power amplifier was designed experimentally via the load-pulling technique. For this purpose, a multi-harmonic active load-pull system was conceived and validated. Two six-port reflectometers were constructed and characterised for use in this load-pull system.

A high efficiency power amplifier implemented in coplanar waveguide and operating in class B at 3.5 GHz was designed. The load-pull system was used to determine the optimum efficiency-enhancing terminations required by the active device at 3.5 GHz, 7.0 GHz, and 10.5 GHz. A numerical simulator was then used to design a circuit whose input impedance corresponds to these optimum efficiency-enhancing loads. The circuit was fabricated and its performance was evaluated.

Finally, two antennas were designed to produce the transistor's efficiency-enhancing loads. The coplanar-waveguide-fed slot-coupled patch antenna was the radiating element of choice for implementing these circuits. One active antenna was conceived where the CPW-fed

slot-coupled patch served as a radiating element only. The transistor's efficiency-enhancing loads were produced by appropriately patterned stubs in the coplanar waveguide platform. The second active antenna made use of the CPW-fed slot-coupled patch as a radiating element and as an impedance tuning element to optimally load the transistor. Both antennas were designed numerically. The circuits were then constructed and tested.

6.2 Thesis Contributions

The specific contributions of this work include:

(i) Proposed architectures for two novel active antennas comprised of a high-efficiency power amplifier integrated with a coplanar-waveguide-fed slot-coupled patch antenna.

(ii) An evaluation of the performance of Agilent Technologies' Momentum electromagnetic simulator in predicting the performance of coplanar waveguide circuits.

(iii) An evaluation of the performance of the Momentum simulator in predicting the operation of coupled-slot-line-mode-suppressing air bridges.

(iv) The design of a narrow-band bias tee implemented in coplanar waveguide on Rogers' RT Duroid 5880 microwave substrate.

(v) The experimental determination of the optimum efficiency-enhancing loads of Agilent Technologies' ATF-26836 FET when operated as a class B power amplifier constructed in coplanar waveguide on Rogers' RT Duroid 5880 substrate. This data is obtained for amplifier operation at 3.5 GHz and includes the FET's optimum termination at 3.5 GHz, 7.0 GHz and 10.5 Ghz.

(vi) The construction and evaluation of a multi-harmonic load-pull system operating at 3.5 Ghz.

(vii) The conception and evaluation of two six-port reflectometers.

Unfortunately, the physical implementation of the active antennas proposed in this work did not function as predicted by the numerical simulator that was used to design them. However, it is clear that further study of these circuits will certainly lead to the conception of a working active antenna.

6.3 Future Work

It is immediately evident that further study of the proposed active antennas is required. Despite the disappointing performance of the constructed circuits, the physical realisation of these active antennas remains feasible.

In order to realise the proposed active antennas, a thorough study of the simple power amplifier designed in chapter 4 is required. A comparison of the performance of the transistor's loading circuit and the results obtained with Momentum will lead to a more thorough understanding of the relationship between the simulated circuit parameters and the measured circuit parameters. This information can be used to design a better performing circuit later.

An effort should also be deployed in an attempt to tune this power amplifier using dielectric and / or metallic slugs. Any information obtained in regards to the specific contribution of the circuit's constitutive elements (stubs and line lengths) to the overall input impedance of the circuit can also be used to fine-tune the amplifier's design process.

Of course, the performance of the two active antennas also requires further study. In regards to the antenna architecture where the radiating element is not used as an impedance tuning device, the effect of the fundamental-frequency loading stub on the antenna's input reflection coefficient must be more adequately understood. An in-depth comparison of the input impedance of physically realised CPW-fed slot-coupled patch antennas with that predicted by the Momentum simulator is also recommended. Understanding the relationship between these parameters will lead to the physical realisation of an active antenna that uses such a patch to produce the transistor's efficiency-enhancing load at the fundamental frequency.

Other integrated antenna architectures should also be envisioned. One interesting possibility is the construction of a bias tee that not only provides a non-invasive means of applying the bias signal to the active device, but also produces one of the device's efficiency-enhancing loads. Any creative, dual-purpose implementation of traditionally single-purpose amplifier circuitry is academically and commercially interesting.

Low-temperature co-fired ceramic (LTCC) technologies also make possible a large number of novel amplifier configurations. This technology allows for the design of compact, three-dimensional microwave circuits. Almost any integrated amplifier / antenna configuration that is constructed on an LTCC platform will be academically interesting as this technology is not very mature.