Efficiency Enhancement of Pico-cell Base Station Power Amplifier MMIC in GaN HFET Technology Using the Doherty technique

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Abstract

With the growth of smart-phones, the demand for more broadband, data-centric technologies are being driven higher. As mobile operators worldwide plan and deploy 4th generation (4G) networks such as LTE to support the relentless growth in mobile data demand, the need for strategically positioned pico-sized cellular base stations known as 'pico-cells' are gaining traction. In addition to having to design a transceiver in a much compact footprint, pico-cells must still face the technical challenges presented by the new 4G systems, such as reduced power consumptions and linear amplification of the signals.

The RF power amplifier (PA) that amplifies the output signals of 4G pico-cell systems face challenges to minimize size, achieve high average efficiencies and broader bandwidths while maintaining linearity and operating at higher frequencies. 4G standards as LTE use non-constant envelope modulation techniques with high peak to average ratios. Power amplifiers implemented in such applications are forced to operate at a backed off region from saturation. Therefore, in order to reduce power consumption, a design of a high efficiency PA that can maintain the efficiency for a wider range of radio frequency signals is required.

The primary focus of this thesis is to enhance the efficiency of a compact RF amplifier suitable for a 4G pico-cell base station. For this aim, an integrated two way Doherty amplifier design in a compact 10x11.5mm^2 monolithic microwave integrated circuit using GaN device technology is presented. Using non-linear GaN HFETs models, the design achieves high efficiencies of over 50% at both back-off and peak power regions without compromising on the stringent linearity requirements of 4G LTE standards. This demonstrates a 17% increase in power added efficiency at 6 dB back off from peak power compared to conventional Class AB amplifier performance. Performance optimization techniques to select between high efficiency and high linearity operation are also presented.

Overall, this thesis demonstrates the feasibility of an integrated HFET Doherty amplifier for LTE band 7 which entails the frequencies from 2.62-2.69GHz. The realization of the layout and various issues related to the PA design is discussed and attempted to be solved.

Acknowledgment

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List of Acronyms and Abbreviations

Acronym	Meaning
3GPP	Third generation partnership project
4G	Fourth Generation
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
CAD	Computer aided design
CCDF	Complementary Cumulative Distribution Function
DC	Direct current
DPD	Digital pre-distortion
EER	Envelope elimination and restoration
ET	Envelope tracking
FET	Field effect transistor
GaN	Gallium Nitride
HEMT	High electron Mobility transistor
HFET	Heterostructure field-effect transistor
IC	Integrated circuit
IIP3	Third order input intercept point
IMD	Intermodulation distortion
IMD3	Third order intermodulation distortion
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LINC	Linear Amplification Using Non-linear Components
LTE	Long term evolution
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise figure
OFDMA	Orthogonal frequency division multiple access
OIP3	Third order output intercept point
P1dB	Output Power at 1 dB compression
P3dB	Output Power at 3 dB compression
PA	Power amplifier
PAE	Power added efficiency
PAPR	Peak-to-average power ratio
Psat	Saturated output power
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency

Chapter 1 Introduction

1.1 Motivations

With the growth of smart-phones, the demand for more broadband, data-centric technologies are being driven higher. As mobile operators worldwide plan and deploy 4th generation (4G) networks such as LTE to support the relentless growth in mobile data demand, the need for strategically positioned pico-sized cellular base stations known as 'pico-cells' are gaining traction. Making capacity available to customers in densely populated areas during peak hours with limited spectrum is one of the biggest challenges that all operators across the world are faced with. Adding another macro-cell could be costly. In such cases, pico-cells help maximize spectrum re-use, providing sufficient capacity for more bandwidth-intensive activities.

In cellular wireless networks, the pico-cell base station is typically a low power, small unit (i.e. the size of a ream A4 paper), that connects to a Base Station Controller [1]. Pico-cells are typically used to extend coverage to indoor areas where outdoor signals do not reach well or to add network capacity in areas with very dense phone usage such as shopping malls and train stations. According to industry research firm In-Stat, the outdoor metropolitan pico-cell market is forecast to top $5 Billion in 2014 [2].

In addition to having to design a transceiver in a much compact footprint, pico-cells must still face the technical challenges presented by the new 4G systems, such as reduced power consumptions and linear amplification of the signals.

Fourth generation (4G) wireless communication standards employ spectrum efficient modulation techniques like phase shift keying (PSK) and quadrature amplitude modulations (QAM) that result in signals with non-constant envelopes with high peak to average power ratios (PAPR) and broad modulation bandwidths [3]. In order to avoid spectral spreading and signal clipping, these signals are required to be amplified linearly [4, 5]. These techniques that produce non-constant envelope signals with high PAPR, require the RF power amplifier

to also function at a backed off power level to operate over the full dynamic range of the signal. However, this drastically reduces the efficiency of the power amplifier since the most efficient operation of a power amplifier is near compression. Thus, higher spectral efficiency is achieved at the cost of power efficiency. This scenario requires strategic trade-offs between linearity and efficiency for RF power amplifier design. Consequently, analysis and design of highly linear power amplifiers with high efficiency at large power back off levels becomes more critical.

A summary of challenges faced in RF power amplifier design to meet these requirements will be discussed in the following section 1.2.

1.2 Background: Power Amplifier Design Challenges for pico-cells

The RF power amplifier (PA) that amplify the output signals of 4G pico-cell systems face challenges to minimize the size, to achieve high average efficiency and broad bandwidths while maintaining linearity and operating at higher frequencies. For instance 4G standards as LTE has to support channel bandwidths up to 20MHz [6] and PAPRs of 6 to 10dB [4] for frequencies up to 2.6GHz [7]. Hence, the RF power amplifiers need to be able to handle these stringent requirements.

Amongst these many requirements of a base station amplifier, linearity and efficiency are the most crucial. To meet the linearity requirements, power amplifiers can be operated at a back-off power level from the peak output power in a linear and efficient class of operation, such as class AB. But due to the high PAPR of the signal, this will lead to very low efficiency at the signals average output power. On the other hand more efficient classes of operation such as class B are extremely non-linear, even with linearization techniques such as digital pre-distortion this would not be a suitable solution. Therefore, the design of power amplifiers generally forces trade-offs between linearity and efficiency.

Thus, a 4G pico-cell base station power amplifier needs to be designed in a small real estate area, also referred to as form factor, to operate at high frequencies while maintaining high average efficiency, linearity and broad envelope and RF bandwidths. Following are a few options that could be proposed to address these multiple challenges.

1.2.1 Addressing Linearity challenges

Several linearization techniques have been developed which facilitates the PA design to focus more on the efficiency aspect of the design by essentially minimizing linearity requirements from the design goals. Power amplifiers linearity can be improved by both system level and circuit level optimizations. Several system level linearization techniques such as Feed Forward Linearization [8] [9], Cartesian Feedback [10, 11], LINC (Linear amplification using Nonlinear components) [12] and Digital pre distortion (DPD) [13 - 15] have been developed and implemented. Note that power amplifiers also possess memory effects that contribute to the distortion of the input signal when the signal has a broad envelope bandwidth. The main outcome of memory effect is that it makes most standard linearization inefficient [16]. Although some Digital pre distortion (DPD) algorithms do correct for some memory effects [13], it is fundamentally important to minimize the memory effects at the amplifier circuit design level. One method is to increase the video bandwidth of the amplifier through improved bias and matching circuit design methods [17] [18]. Linearity can also be optimized at the device level through the use of improved device processes, such as the use of field plated HEMT structures in GaN devices [19].

1.2.2 Addressing average efficiency challenges

Achieving high efficiency for a single power level can be attained through harmonic tuning [20], switch mode amplifier designs [21] and single stage class B or class AB designs. The problems with such techniques are that either they are extremely non-linear or they have poor average efficiency when a non-constant envelope signal is being amplified. To address these issues, several efficiency enhancement techniques such as Chireix Outphasing [22 - 24], Envelope elimination and restoration (EER) [25-27], Doherty [28] and Envelope tracking (ET) [29] have been suggested and studied to date. The strengths and limitations of each of these efficiency enhancements techniques are discussed in Chapter 2. When such an efficiency enhancement technique is combined with a linearization method, a RF amplifier would be able to handle some of its most stringent design requirements.

1.2.3 Addressing design space challenges

Since a pico-cell base station is a much smaller unit compared to a macro-cell, an additional challenge is presented in implementing a highly efficient, highly linear power amplifier in a compact design area. This is where new wide bandgap device technologies as GaN HFETs present architectural benefits. Recent developments have shown that GaN fabrication has made it possible to reach power densities up to 30W/mm [19]. This allows transistor sizes to be much smaller and be able to achieve high power levels. GaN device technology shows superior advantages beyond other materials such as GaAs, SiC and Si in terms of high power and frequency operation range [21]. They also offer slightly higher efficiency and a much wider bandwidth due to their lower parasitics [30]. The lower parasitics also allow the output impedances to be much larger compared to technologies as Si-LDMOS, which makes matching structures less complex to implement. This makes it possible to realize small-sized circuit structures for the full power amplifier design. Therefore a power amplifier design for a 4G network needs to consider all these aspects in order to satisfy requirements.

1.3 Research Goals

Among all the challenges discussed in section 1.2, that of efficiency and real-state will be addressed in this thesis through a compact design achieving high efficiency at 6dB back-off and peak power levels.

Therefore the primary focus of this thesis is to enhance the efficiency of a compact RF amplifier that is suitable for a 4G pico-cell base station. For this objective, an integrated two way Doherty amplifier design in a monolithic microwave integrated circuit (MMIC) using GaN device technology will be designed. Implementation of the design will be done using non-linear models of GaN HFETs. The design intends to achieve high efficiencies above 50% at both back off and peak power without compromising on the stringent linearity requirements of 4G LTE standards .The thesis will demonstrate the feasibility of an integrated HFET Doherty amplifier in a MMIC for LTE band 7. A complete realization of the layout and various issues related to the RF power amplifier design will be discussed and attempted to be solved.

1.4 Thesis Organization

The content of this thesis is divided into five chapters as follows:

Chapter 1 presents the motivation for this research and the objective of this thesis.

Chapter 2 presents a quick review of PA classes and the most common metrics used to assess PA performance. Furthermore, efficiency enhancement techniques is discussed and compared to show the advantages and limitations of each approach. Main techniques that are discussed are Envelope elimination and restoration, Envelope tracking, Chireix outphasing technique and Doherty amplifier technique. Different state of the art variations of the Doherty architecture is also reviewed and compared. A detailed explanation of the principle of operation of Doherty architecture is presented. The chapter concludes with a detailed discussion on the selection of the most appropriate power amplifier architecture for this thesis.

Chapter 3 presents a brief outline of material properties of GaN highlighting the advantages of GaN for efficient and linear power amplifier design at high frequencies. An analysis of the use GaN compared to GaAs, SiC MESFT and LDMOS is also presented. A brief overview of the GaN MMIC process is discussed. A design and implementation of a classical printed circuit board (PCB) design of a single stage class AB amplifier using Cree's CGH25120F GaN HEMT transistor is also presented in this chapter. A comparative analysis of the performance between a simulated design using a non-linear model of CGH25120F and measured data of CGH25120F is provided. This experiment is performed to validate the GaN non-linear model by comparing the measured and simulated behaviour of the transistor.

Chapter 4 provides the design and implementation of the integrated two way MMIC Doherty amplifier using GaN HFETs. The full layout of the design is presented. Simulated results of the implementation are provided to ensure the performance of the design in overcoming the low-efficiency problems at average power of the non-constant envelope signal. Performance optimization techniques to select between high efficiency and high linearity operation are also described in this chapter.

Chapter 5 summarizes the contributions of this thesis and provides ideas for future research in this area.

Chapter 2 Basics of RF Power Amplifier Design

2.1 Classes of Operation in RF Power Amplifiers

Amplifiers are classified according to their circuit configurations and methods of operation into different classes such as A, B, AB, C, D, E and F. The DC bias applied to the transistor determines the Class of operation. The Class of operation determines the portion of the input RF signal for which there is an output current in the transistor. Depending on the application, it may be desirable to have the transistor conducting for only a certain portion of the input signal. These classes range from entirely linear with low efficiency to entirely non-linear with high efficiency.

Figure 1 depicts the load lines for each of the classes on a DC –IV plot. Note that as the class of operation moves through class A to class C, the load line moves out of the saturation region. Class F, D and E load lines are mainly on the ohmic and pinch-off regions. This makes the devices biased under these classes to operate in two discrete states of On and Off, which is also commonly known as switch mode operation.

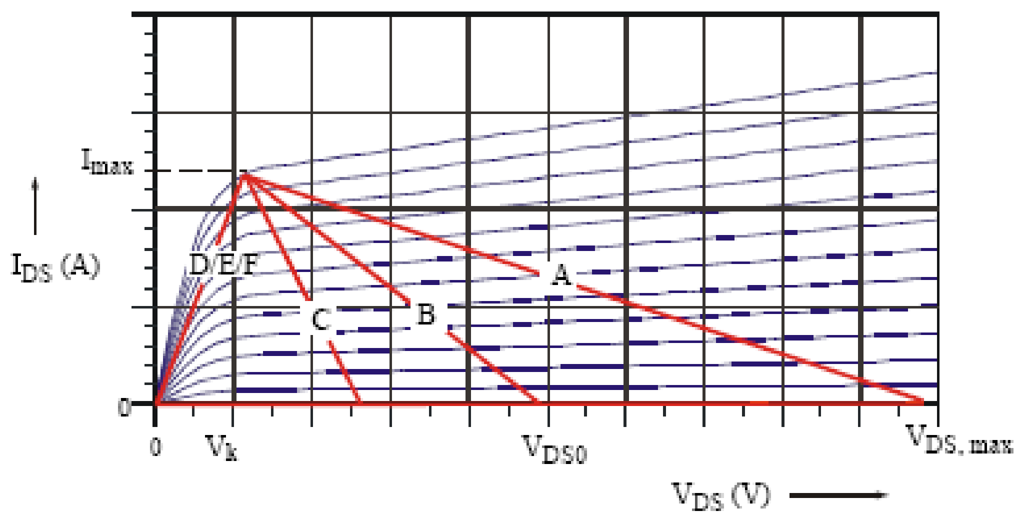
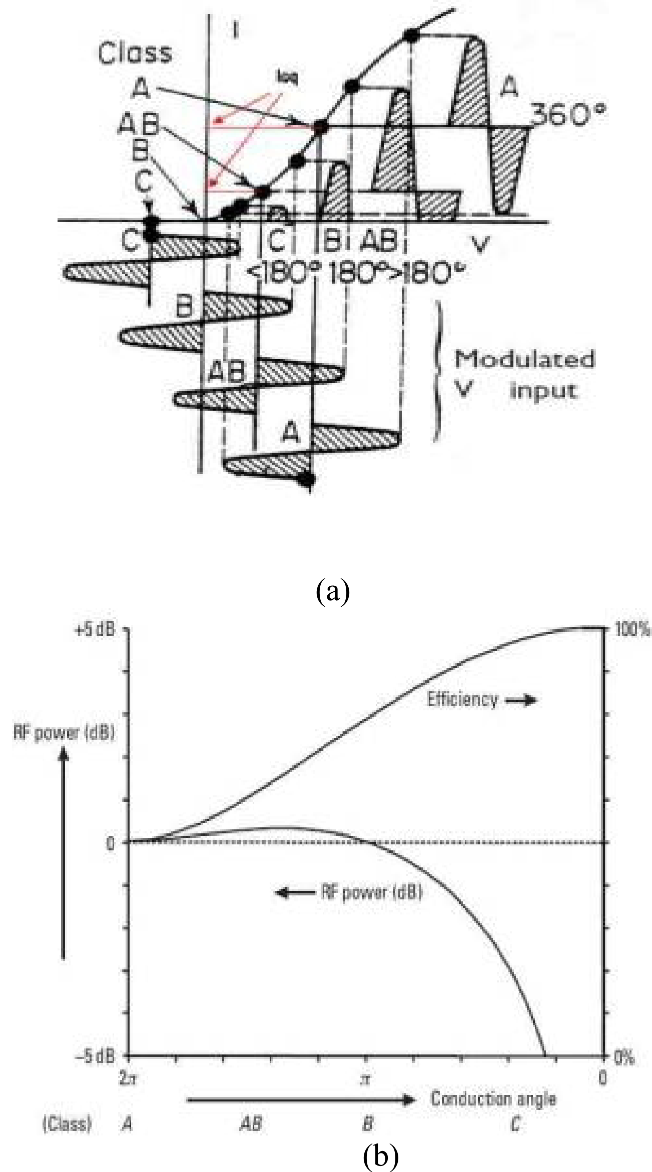


Figure 1: Load lines of various power amplifier classes of operation

This chapter analyzes four classes (A, B, AB, and C) of power amplifier operation, which are mainly associated with Doherty power amplifier operation. Figure 2 shows a summary of these four power classes based on their transistor transfer characteristics and their classical definitions.



(a)

(b)

Figure 2: (a), (b) Classes of operation of Power amplifiers and their standard definition [31]

2.1.1 Class A

Class-A is the most linear of all amplifier class types. It can be defined, as an amplifier that is biased such that the output current flows at all times and the input signal drive level is kept small enough to avoid driving the transistor in to cut-off. In a Class A operation, the transistor conducts for the full cycle of the input signal, meaning that the conduction angle of the transistor is 360°. As seen in Figure 3, the bias point is set in the active region which is closer to the center of the transistor's range of operation.

Although class A amplifiers are highly linear, since the device is conducting at all times and is constantly carrying current, consequently there is a continuous loss of power in the device, which results in poor efficiency. The maximum efficiency of an ideal Class-A PA is 50 % at peak envelope power. Due its linear nature, IMD and harmonic levels of a class A amplifier decreases or increases monotonically with the input signal level. The low levels of harmonics in the amplification process allows Class-A to be used at frequencies close to the maximum capability (fmax) of the transistor. With good linearity but low efficiency, Class-A PAs are suitable for applications requiring low power, high linearity, high gain and broadband operation.

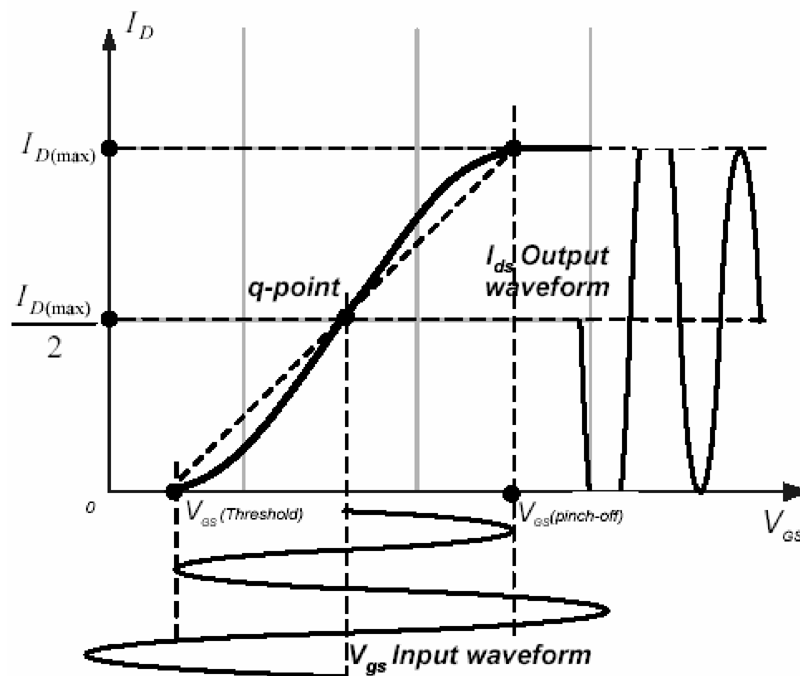


Figure 3: Class A transfer characteristic [32]

The DC power consumption of a class A amplifier can be calculated as:

$$P_{dc} = V_{dd} \times I_{dq} \qquad (2.1)$$

The maximum output power is:

$$P_{out_max} = \frac{1}{2} \times V_{dd} \times I_{dq} \qquad (2.2)$$

where Vdd= drain voltage and Idq= Quiescent current. Note that maximum ac output current is equal to Idq.

2.1.2 Class B

This is an amplifier where the transistor conducts only half of the time either on positive or negative half cycle of the input signal. The conduction angle for the transistor is approximately 180°. The class-B amplifier operates ideally at zero quiescent current. This is achieved by biasing the transistor at its cut off voltage and any current through the device goes directly to the load.

Compared to a class A amplifier the efficiency of a class B amplifier is higher. For an ideal class B PA the maximum efficiency can reach up to 78.5 % at peak envelope power. However, the trade-off is linearity. A typical Class-B amplifier will produce considerable amounts of harmonic distortion that must be filtered from the amplified signal.

Class B power amplifiers are often implemented using push-pull configuration, which uses two transistors in parallel [32]. In this configuration one transistor conducts during positive half cycles of the input signal and the second transistor conducts during the negative half cycle. This method ensures that the entire input signal is reproduced at the output. The DC power consumption of a class B amplifier can be calculated as:

$$P_{dc} = \frac{2}{\pi} \times V_{dd} \times I_{ac_max} \qquad (2.3)$$

where Vdd = drain voltage, Iac_max = maximum ac output current. Figure 4 shows how the class-B amplifier operates.

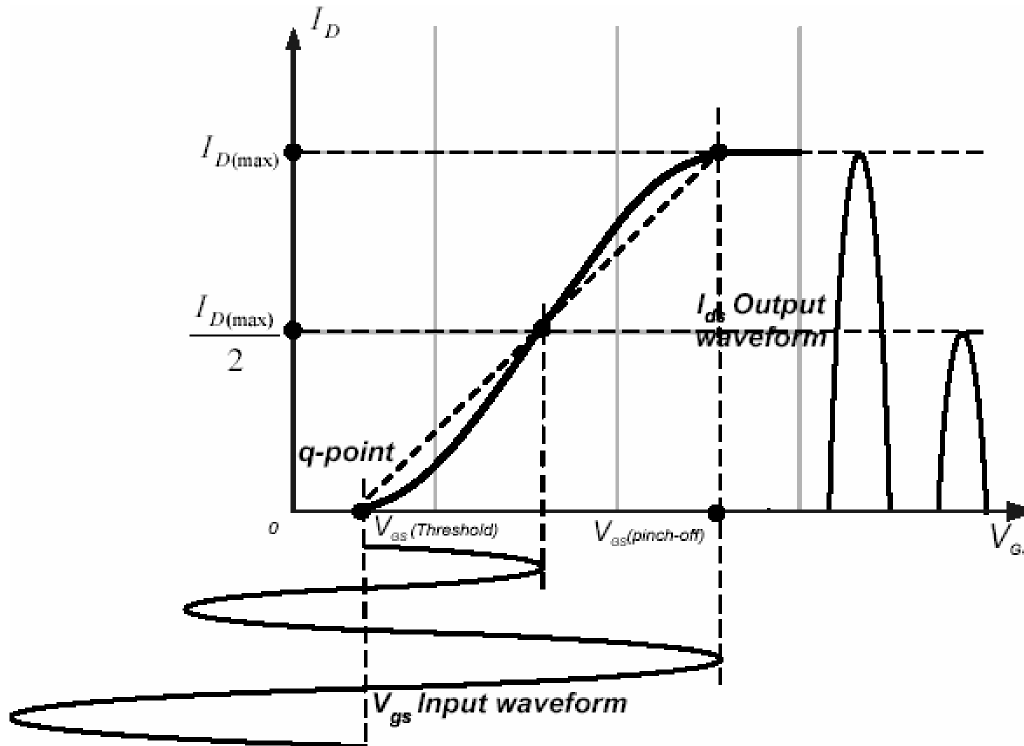


Figure 4: Class B transfer characteristic [32]

2.1.3 Class AB

In terms of linearity and efficiency, Class AB amplifiers are a balance between Class A and Class B amplifiers. The dc operating point of the class AB operation is in the region between the cut-off point and the Class A bias point. This would lead to a quiescent current of 10% - 15% percent of Idss. The conduction angle in Class-AB is between 180° and 360 ° which would have the transistor on for more than half a cycle, but less than a full cycle of the input signal. The linearity of a class AB power amplifier is closer to Class A operation and its maximum efficiency is between 50% -78.5%.

2.1.4 Class C

In class C operation the conduction angle for the transistor is significantly less than 180°. It is biased so that the output current is zero for more than one half cycle of the input signal. Linearity of the Class-C amplifier is the poorest of the four classes of amplifiers discussed in this chapter. The maximum Efficiency of Class-C can approach as high as 85 %.

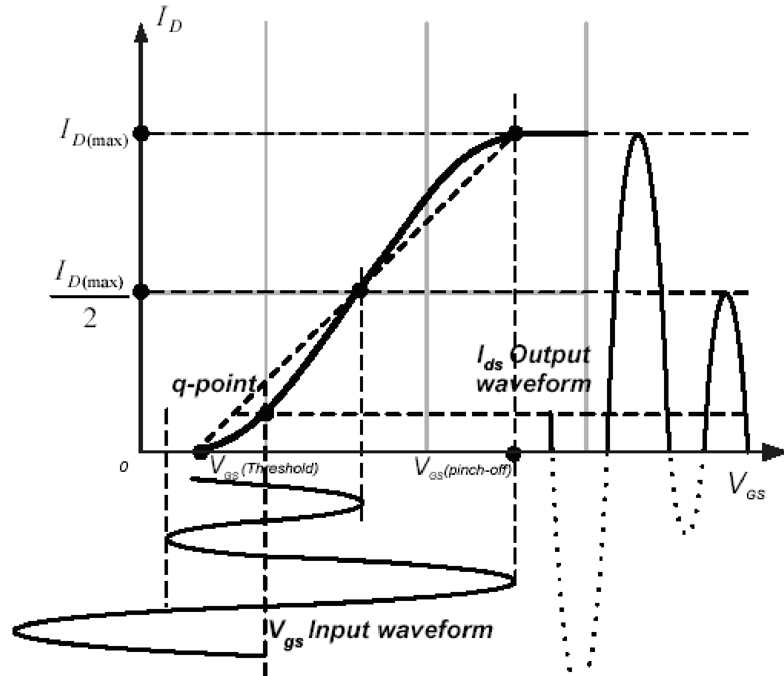


Figure 5: Class AB transfer characteristic [32]

2.1.5 Additional power Classes

There are additional power classes such as F, D, E, G, H, and S. All these classes are catered for power amplifiers that target high-efficiency performance. Each of these classes uses a variety of techniques to reduce the average drain power to achieve high efficiency. For instance, Class F uses harmonic resonators in the output network to shape the drain waveforms to achieve high efficiency. Classes D, E, and S use switching techniques. Classes G and H use resonators and multiple power-supply voltages to reduce the drain current-voltage product.

Classes S, D, E, F, G, and H are widely used for narrowband tuned amplifiers that require higher efficiency but do not require linear amplification, such as amplification of CW, FM or PM that have constant envelopes.

2.2 Power Amplifier Performance Metrics

Power amplifiers are available in various form factors ranging from miniature ICs to high power transistors on printed circuit boards. Depending on the various system requirements,

the specific requirements of a given power amplifier will also vary considerably. However, there are common metrics, such as linearity, efficiency, gain flatness, noise figure and stability that are used to assess the performance of any type of PA. Often design trade-offs are required to optimize one parameter over another and necessitates performance compromises. In this section, a few common amplifier performance metrics are discussed.

2.2.1 Stability

Stability refers to an amplifier's resistance to causing spurious oscillations. Means of feedback and gain are the fundamental conditions for oscillation. Ensuring stability of an amplifier with considerable gain over a large bandwidth would require that all conducted and radiated feedback paths are sufficiently attenuated. A conducted feedback path could be through a bias feedback and a radiated feedback path could be in the form of a waveguide cavity in which active elements are shielded with.

Although it is expected for an amplifier to be stable, often it is difficult to determine if this is the case in RF power amplifier applications. For instance, while it may appear that there are no obvious oscillations generated from the amplifier, it can be such that the oscillation frequency is low enough that the DC blocking capacitors attenuate the signal sufficiently to make it very difficult to measure. Or there may appear an unexplained spurious signal at high frequencies in the output spectrum that is the mixing product of the desired signal and an oscillation tone that is out of band of the measuring receiver.

A formal set of conditions for unconditional stability can be expressed in a set of formulas by the Rollett's stability factor (K factor):

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12} \cdot S_{21}|} > 1$$

$$|\Delta| = |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}| < 1 \qquad (2.4)$$

along with one of the following auxiliary conditions:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0$$
$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 > 0$$
$$\beta_1 = 1 - |S_{22}|^2 - |S_{12}S_{21}| > 0$$

$\beta_2 = 1 - |S_{11}|^2 - |S_{12}S_{21}| > 0$

The above conditions only apply when source and load reflection coefficients have a magnitude of less than one ($\Gamma_{in} < 1$ and $\Gamma_{out} < 1$).

2.2.2 1 dB Compression point (P_{1dB}) and Psat

One of the primary figures of estimating the linearity of an amplifier is its 1dB compression point. The output power specifications for RF amplifiers are typically specified at one dB of compression (P_{1dB}) or at saturation (Psat).

At small-signal levels, the transfer characteristic is constant with input drive level, and is equal to the linear small-signal gain of the device. At higher power levels, the amplifier's power gain is reduced, and enters into gain compression. The output 1 dB compression (OP1dB) point can be expressed as the output level at which the gain is compressed by 1 dB from its linear value. At a certain power level the output power saturates, and no additional power results at the output as the input is driven harder. This output power level where the amplifier is saturated is referred to as the P_{sat} level of the amplifier. Implicitly it is assumed that these are operating points where the amplifier will be exhibiting some degree of non-linearity. Figure 6 shows the relationship between the input and output power of a typical power amplifier. At low level of input signal the graph coincides with the straight line with slope angle tangency of one.

This segment of the graph corresponds to the linear region of the amplifier. Further as the input power increases, the graph changes its slope and becomes almost flat as the point where the stage enters saturation mode. Essentially, this segment of the graph corresponds to non-linearity. The input P1dB point (IP_{1dB}) can be derived from the OP_{1dB} with the following relationship:

$$OP_{1dB} = IP_{1dB} + (G\text{-}1) \quad [dB] \qquad (2.5)$$

where G= Linear gain of the amplifier (dB).

Although P1dB has been a fundamental metric of estimating linearity of an amplifier, for some devices types with certain characteristics, assessing the P1dB point may not be as apparent.

For instance, due to the smooth transition from the linear to the saturation region, GaN amplifiers typically define their output power at the 3dB compression point.

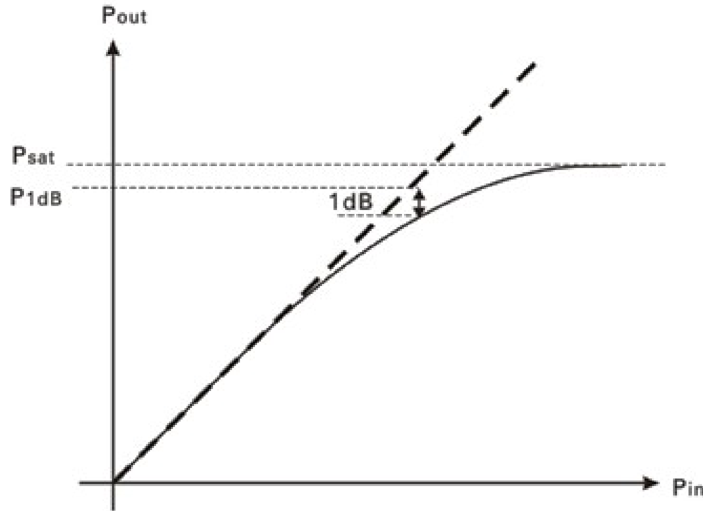


Figure 6: 1 dB Compression point (P1dB) and Psat

2.2.3 Efficiency

Efficiency is a measure of a device's ability to convert one energy source to another. In power amplifier design, efficiency indicates the Power Amplifier's ability to convert the DC power of the supply into the signal power delivered to the load. Power that is not converted to useful signal is dissipated as heat. Therefore Power Amplifiers that has low efficiency have high levels of heat dissipation. To obtain the maximum efficiency of a RF power amplifier, one has to consider multiple aspects of the design as frequency, temperature, input drive level, load impedance, bias point, device geometry, and intrinsic device characteristics. In typical microwave designs, efficiency is presented in three forms:

- *Drain efficiency:* Drain efficiency is the ratio of output RF power to input DC power.

$$\eta = \frac{P_{RFout}}{P_{DC}} = \frac{P_{RFout}}{V_{DC} \times I_{DC}} \qquad (2.9)$$

In this unit of measure the incident input RF power that goes into the device is disregarded.

- *Power added efficiency (PAE):* Power added efficiency takes into account the input RF power to the device in its calculation of efficiency.

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} = \frac{P_{RFout} - P_{RFin}}{V_{DC} \times I_{DC}} \quad (2.10)$$

A theoretical amplifier with infinite linear gain will have the same efficiency value with the drain efficiency and PAE calculations. In practical amplifiers PAE will always be less than drain efficiency. Although for amplifiers with high gain the two calculations would yield very close results, since the input power levels are only a fraction of the output power.

- *Total efficiency*: Total efficiency gives a complete sense of the ratio of output power to both types of DC and RF input power.

$$P_{total} = \frac{P_{RFout}}{P_{DC} + P_{RFin}} = \frac{P_{RFout}}{(V_{DC} \times I_{DC}) + P_{RFin}} \quad (2.11)$$

2.2.4 Linearity

All RF microwave circuits generate signal distortion as a result of non-linear behavior .In a RF power amplifier, it is inevitable that non-linear behavior exists which is attributed mainly to gain compression. It is characterized by various techniques depending upon s pecific modulation and application. Harmonics, Inter-modulation distortion and intercept points are few of the most commonly used figures for quantifying linearity.

- *Intermodulation distortion (IMD):* When multiple signals are injected to an amplifier simultaneously, the sum and difference products of each of the fundamental input signals and their associated harmonics create distortion products, which are referred to as inter-modulation distortion (IMD). IMD products are more difficult to deal with compared to harmonic distortion. Harmonics can be filtered from the output spectrum but IMD products, especially third order IMD products occur close to the desired signal.

Also lower frequency second-order IMD products can interfere with the DC bias of the transistor, increasing the non-linearity and decreasing efficiency. When two signals at frequencies f1 and f2 are input to any nonlinear amplifier, the following output components will result as in Figure 7.

Note that odd order intermodulation products (2f1-f2, 2f2-f1, 3f1-2f2, 3f2-2f1) are close to the two fundamental tone frequencies f1 and f2.

The magnitude of Intermodulation distortion can be given by:

$$\text{IMD (dBc)} = \text{Pout}_{1dB} - \text{Pout}_{IMD} \quad (2.12)$$

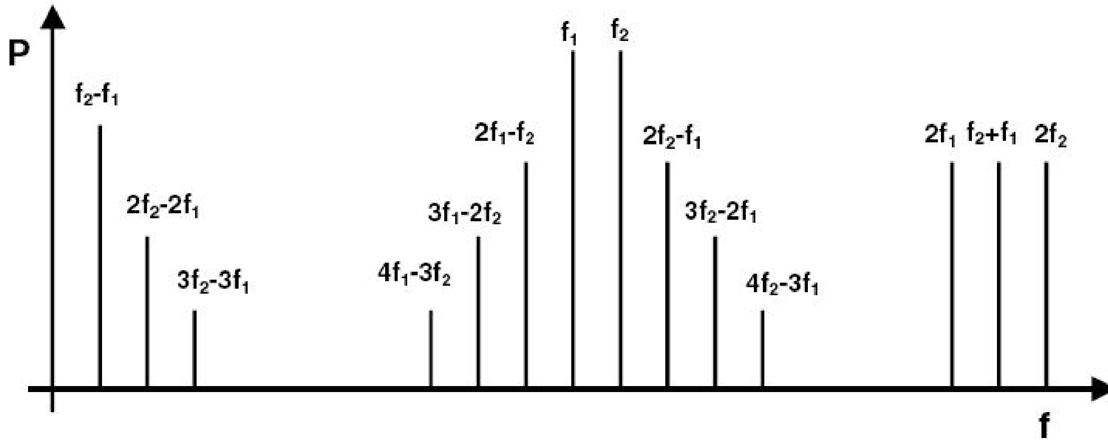


Figure 7: Frequency spectrum of a two-tone signal

where Pout_{IMD} represents the output power of the third order intermodulation product. IMD magnitudes can increase with carrier spacing and can distort the output signal significantly as wider bandwidths are explored. Therefore, it is important to minimize IMD products as much as possible when designing RF amplifiers for wide bandwidths.

- *Intercept point*: As the input power to a power amplifier is increased, the slope of the amplitude of the harmonics at the output increases more swiftly with respect to the fundamental tone. If the amplitude of the fundamental and higher order products are plotted on a log scale with their respective slopes, the intercept point is where their linear extension intersects with the linear extension of the 1:1 slope of the fundamental slope. Figure 8 represents the second and third order intercept points (IP2 and IP3) in a plot of input power versus the output power. Third order intercept point (IP3) in particular plays a significant role in assessing a power amplifiers performance. Higher the IP3, lower is the distortion at higher power levels. The magnitude of the third order output intercept (OIP3) point and the third order input intercept point (IIP3) can be calculated as follows:

$$OIP3 = P_{out} + \frac{P_{out,\,IMD}}{2} \quad (2.13)$$

$$IIP3 = OIP3 - Gain \quad (2.14)$$

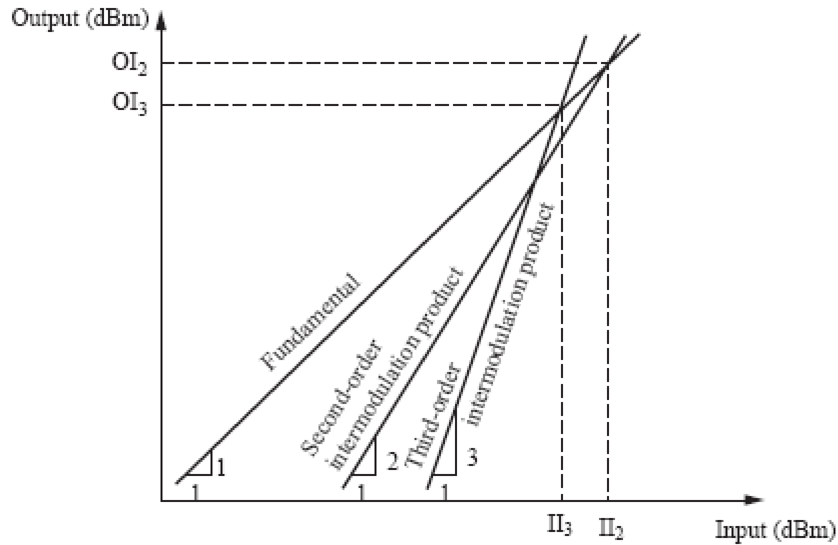


Figure 8: Second and third-order intercept points

2.3 Efficiency Enhancement Techniques

With wireless communication systems evolving, standards such as LTE use more efficient modulation schemes as orthogonal frequency division multiple access (OFDMA) to achieve higher data rates and better spectral efficiency. The non-constant envelope signals of these systems have large peak-to-average power ratios (PAPRs) of around 6-10dB [33]. The RF power amplifier (PA) that amplifies the output signals of these systems faces challenges to achieve increased bandwidth, to minimize the size, to achieve high efficiency while maintaining linearity.

Power amplification of amplitude-modulated signals with fluctuating envelopes used in these systems face challenges where the modulated signal gets distorted when the power amplifier is used at its full rated RF power level. An apparent solution is to operate the power amplifier in the linear region where the average output power is much smaller than the amplifier's saturation power. But this increases cost and reduces efficiency, since the most efficient operation of a power amplifier is near compression. In addition to non-linearity, power amplifiers also possess memory effects that contribute to the distortion of the input signal when the signal has a broad envelope or video bandwidth. Memory effect could be explained as a time lag between AM-AM (amplitude dependent gain) and AM-PM (amplitude dependent phase shift) response of the amplifier by changes in the modulation frequency [16]. The most

common outcome of memory effects in an amplifier is the variation of IMD3 sidebands with tone spacing and asymmetry between the lower and upper band IMD3 [16, 34].One approach to reduce nonlinear distortion is the linearization of the power amplifier. Several linearization techniques such as Feed Forward Linearization [8-9], Cartesian Feedback [10-11], LINC (Linear amplification using Nonlinear components) [12] and Digital pre distortion (DPD) [13-15] have been developed. Note that one of the main consequences of memory effect is that it makes most standard linearization in efficient [16]. Even though there are a number of Digital pre distortion (DPD) algorithms that do correct for some memory effects [13], it is fundamentally important to minimize the memory effects at the amplifier design level. Although these linearization techniques fulfill the linearity requirements, it may contribute to overall efficiency degradation due to additional circuitry involved in the linearization process.

Another challenge is to achieve high efficiency at two power levels for non-constant envelope signal amplification. Maximum efficiency is attained only at one single power level, usually closer to the maximum rated power of the device. For a signal with a 6-10dB PAPR, efficiency would be degraded in the back-off power level. An implementation of efficiency enhancement technique that results in high efficiency in the back-off power level of operation of the power amplifier would be the solution for this issue. Several efficiency enhancement techniques have such as Chireix Outphasing [22 - 24], Envelope elimination and restoration (EER) [25-27], Doherty [28] and Envelope tracking (ET) [29] have been suggested and studied to date.

2.3.1 Envelope elimination and restoration (EER)

The envelope elimination and restoration (EER) also referred to as the Kahn method was proposed by L. R. Kahn in 1952 as a method for implementing efficient, high power single-side-band (SSB) transmitters [26]. As seen in Figure 9 below, a typical amplifier that uses Envelope elimination and restoration (EER) consists of a highly efficient non-linear amplifier and a limiter that eliminates the envelope. An envelope detector and a limiter configuration split a modulated RF input to its polar form in to amplitude and phase components. The phase component of the signal has constant amplitude but modulated phase. The limiter output is a constant envelope signal that is amplified by an efficient but very non-linear amplifi-

er. A constant envelope enables the non-linear amplifier to operate near compression without any distortion, enhancing its efficiency. The envelope information is restored at the output by modulating the supply voltage (Vdd) of the amplifier, where the modulating signal is derived from the envelope detector.

There are various issues that need to be resolved when implementing this method. There could be phase and gain mismatch between the RF and envelope paths due to different circuits that are operated at different frequencies. Correcting for this type of mismatch could be complex. The dc controller's efficiency and bandwidth would add further limitations as well. The association between the PA and drain modulator is a complex and costly implementation as well.

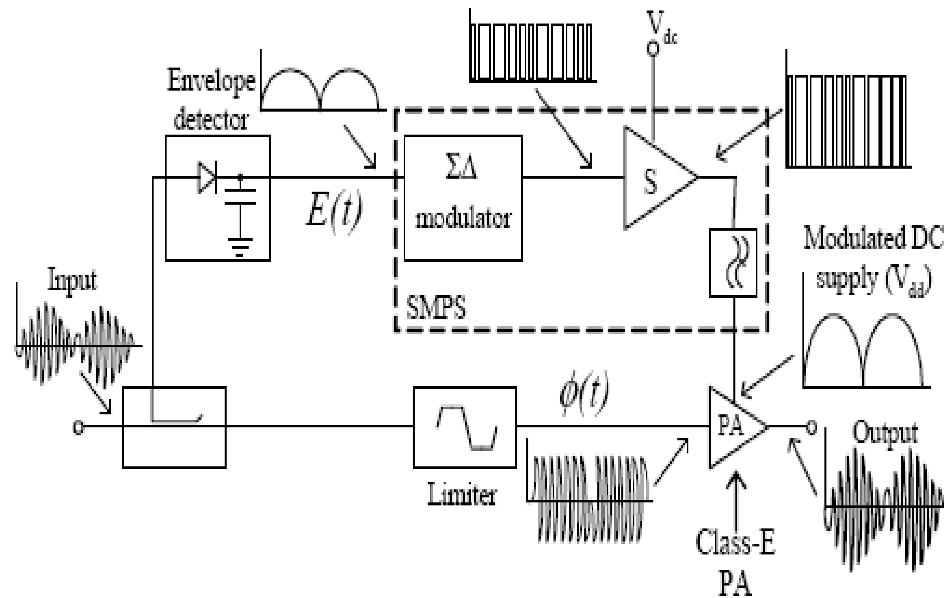


Figure 9: Envelope elimination and restoration (EER) system block diagram [35]

2.3.2 Envelope tracking (ET)

Envelope tracking is a method similar to the EER technique; however the limiter circuit is not required as shown in Figure 10. It superimposes the envelope signal at the drain by dynamically varying supply voltage that conserves power while allowing the PA to operate in linear mode. The difference between this technique and EER is the input signal that contains both amplitude and phase information. It maximizes PA efficiency by keeping RF transistor closer to saturation for all envelope amplitudes. Though the performance of envelope track-

ing is better than a linear amplifier, it is not as good as the EER technique. This is due to the increased flexibility of the supply voltage control, compared to the EER technique. On an ET system the drain modulator does not have to perfectly match with the input envelope which allows more errors and design relaxation, compared to EER.

The design of a highly efficient dc modulator with high output voltage and current is the biggest challenge of implementing this technique. Although ET yields lower efficiency compared to EER, it is more attractive and has already been implemented in several RF applications today [29, 36] because of its simplicity and practicality compared to EER.

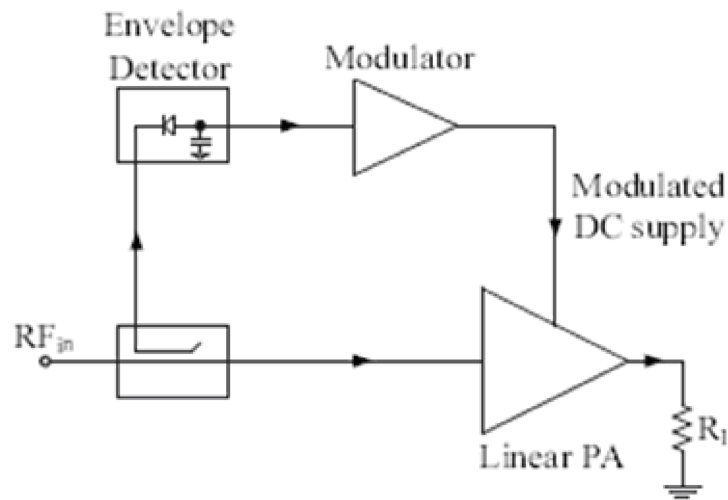


Figure 10: Envelope Tracking (ET) system block diagram

2.3.3 Chireix Outphasing

Chireix outphasing power amplifier system was first introduced by Henri Chireix in 1930s [22]. Chireix Power combining system uses two nonlinear amplifiers to amplify two input signals with different phases, which are finally combined at the output to regain amplitude and phase modulated signal. Firstly, a single input signal containing both amplitude and phase modulation is divided into two constant envelope input signals by an AM-PM modulator where the input signal amplitude is transformed into phase deviation [17]. Conventional power combining at the output could result in severe losses when the phases of the two signal paths vary. A Chireix combiner has resolved this issue by a reactance compensation load design technique that further results in improved efficiency in the back-off region. At two pre-

defined phase offset values, the generator sees a purely resistive load impedance resulting in maximum power combining efficiency. Thorough explanation of the principle and in depth details of the load design and other practical issues are available in [17, 37, 38].

2.3.4 Doherty Amplification Technique

William H. Doherty first introduced the Doherty technique in 1936 [28] which was originally designed using vacuum tubes. This is one of the most implemented techniques today for improving efficiency at back-off output power levels. Doherty technique involves the implementation of efficiency enhancement on a power amplifier circuit that requires linear amplification. Linear amplification is required when the signal contains AM (Amplitude Modulation) or a combination of both, Amplitude and Phase Modulation (SSB, QPSK, QAM, OFDM).

The most conventional configuration of a Doherty circuit is shown in Figure 11. It consists of two amplifiers, namely the main and the peaking. The peaking amplifier is also known as the "auxiliary" amplifier. The amplifiers are connected in parallel with their outputs joined by a quarter-wave transmission line, which performs impedance transformation.

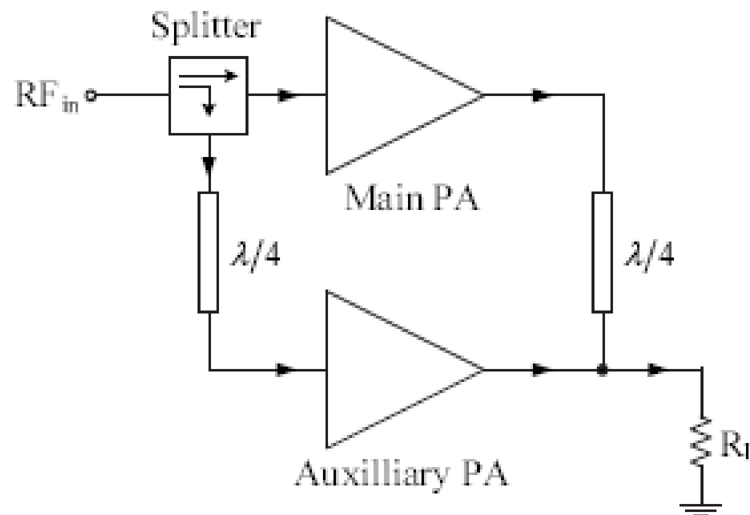


Figure 11: Doherty amplifier block diagram

Each amplifier is biased into different bias conditions. The main amplifier is typically biased in Class AB and the peaking amplifier in class C. It is designed to have different load terminations at multiple power levels, so it has the optimized performed for each power level. The conventional Doherty amplifier design uses two amplifiers to compromise between efficiency and linearity in low power and high power regions.

The peaking amplifier is used to control the load of the main amplifier for a particular range of input power level. The main amplifier is designed such that it will saturate at a certain backed off power level from the power amplifiers nominal output power level. This is performed by presenting a higher impedance at that particular backed off power level. Note that only the main amplifier operates at this backed off power level. As the main amplifier saturates, the peaking amplifier starts to deliver current, reducing the impedance seen at the output of the main amplifier. For instance, for a conventional symmetrical Doherty operation where the main and peaking amplifiers have the same device sizing, at a 6dB backed off power level the main amplifier would be presented with two times its optimum impedance. When the main amplifier saturates, the peaking amplifier will start to operate and modulate the main amplifier load from twice the optimum impedance to its optimum impedance. The peaking amplifier is turned on only during the peaks of the input signal. This is achieved by biasing the device in class C where the bias point is below its pinch-off voltage. Consequently, the peaking amplifier gets turned on when the main amplifier reaches a level closer to saturation. Since the main amplifier remains closer to saturation for a range of 6 dB backed off from the maximum input power, the total efficiency of the system remains high over the full dynamic range.

The Design principles of the conventional Doherty amplifier will be further discussed in detail in section 2.5. In order to optimize the Doherty PA architecture for various signal conditions, the standard Doherty Architecture can be further branched out to various sub categories. There can be several variations of the standard Doherty amplifier architecture. The majority of these variations can be subdivided into three basic categories: symmetrical, asymmetrical, and N-stage Doherty.

- *Symmetrical Doherty architecture:* This is the most conventional and commonly used Doherty amplifier architecture, which was discussed in section 2.3.4. The main benefit of using this architecture is its simplicity. Since the main and peaking amplifiers use the

same device sizing (same peak power capability), the same matching networks can be utilized with a relatively simple 3 dB power splitting at the input, usually implemented with a 90 degree hybrid. The downside of this architecture is that its only optimum for signals with a 6dB peak to average ratio (PAR). This is due to the fact that the second efficiency peak of a symmetrical Doherty design falls at an output power range that is 6dB backed off from its peak power. Therefore for a signal with a higher than 6dB peak to average ratio (PAR), the full efficiency benefit introduced by a symmetrical Doherty would not be properly utilized. Figure 12 shows an efficiency plot of a symmetrical Doherty PA compared to a class B PA.

- *Asymmetrical Doherty Architecture:* The main difference of an asymmetrical Doherty in comparison with a symmetrical Doherty is the use of devices with different peak power capabilities for main and peaking amplifiers. The power ratio between the peak and main amplifier is dependent on the design requirement of where the second efficiency peak needs to be at.

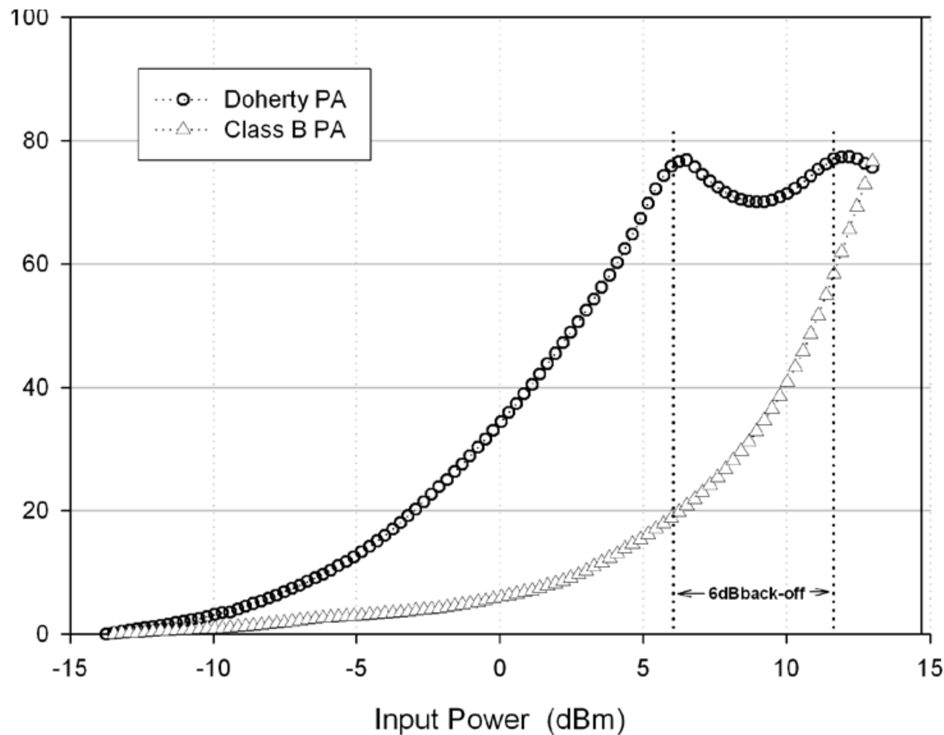


Figure 12: Efficiency of a conventional symmetrical Doherty PA compared to a class B PA [82].

The advantage of the asymmetric Doherty architecture is that the main-peak power ratio can be selected such that the optimum back off efficiency point can be achieved for signals with PARs in the range of 6-10dB, whereas with a symmetrical Doherty architecture the optimum back off efficiency is limited to only 6dB. The theory and implementation of asymmetric Doherty architecture is well described in [39].

- *N-stage Doherty Architecture:* The N-stage Doherty implies the use of "N" number of peaking amplifiers (biased in class C or B) rather than a single peaking amplifier as in the asymmetrical/symmetrical amplifier architecture. At higher drive levels, all of the peaking amplifiers will be engaged and will be contributing to the overall output-combined signal level. At low drive levels only the main amplifier would be turned on. The output power versus efficiency curve of a N-stage Doherty design would consist of N number of efficiency peaks, offering the capability of presenting a high efficiency response at multiple back off power levels. Theory and implementation of N Doherty architecture is well described in [40, 41]. Figure 13 summarizes the efficiency behaviour of the above described Doherty architectures.

- *Digital Doherty:* Although the concept of Doherty architecture has been around for several years, the various enhancements and extensions of this architecture have mostly been based on the standard analog Doherty. The concept of digital Doherty was introduced and explored more in recent years. The basic architecture of a digital Doherty consists of separate dual-inputs for the main and peaking amplifiers that is digitally driven. By using digital adaptive phase alignment techniques the performance degradation that is caused by the bias and power dependent phase misalignment between the main and peaking branches is compensated.

Although research has demonstrated, that in comparison with the conventional analog Doherty PA, a digital Doherty PA can achieve a 10% improvement in PAE over the same back off output power range [42], there are some drawbacks of implementing digital Doherty. For an analog Doherty design, a single input signal is split to drive the main and peaking amplifiers. Therefore, only a single line-up of driver amplifiers is required. Since a

Digital Doherty design has separate inputs for the main and peaking amplifiers, two separate driver line-ups would be required to drive each of the main and peaking paths.

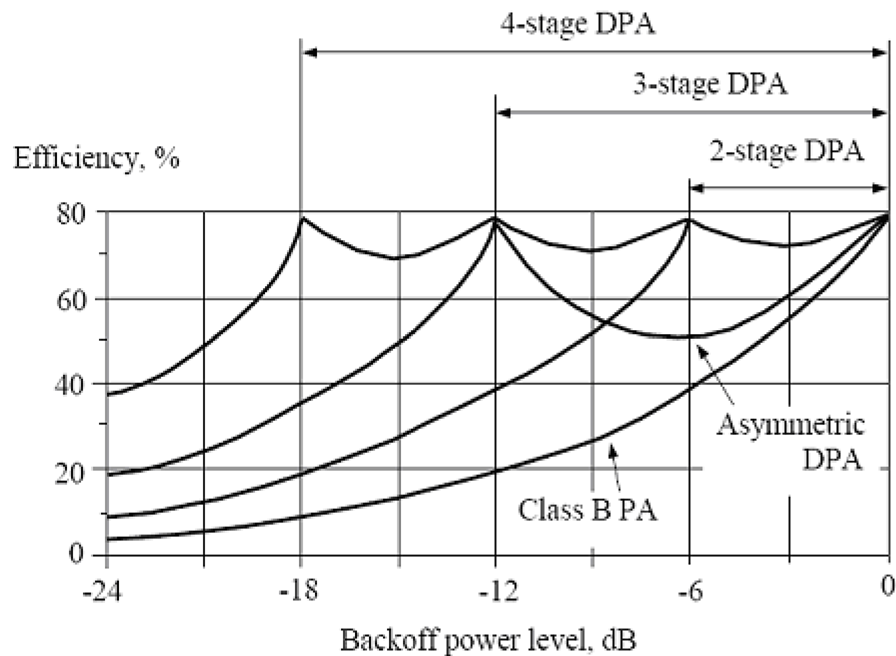


Figure 13: Efficiency behavior of N-stage and asymmetric Doherty PA architectures compared to Class B PA [39]

This increases the number of devices used in the full power amplifier design, driving the overall cost of the design higher. Also with demanding real estate requirements on base station power amplifier PCB boards, accommodating additional driver lineups adds another challenge to the overall design. The implementation of a digital Doherty design becomes far more complex and costly compared to an analog Doherty design due to the digital adaptive phase alignment system that is required.

2.4 Power Amplifier Topology Selection

When deciding the type of amplifier architecture that is best suited for a particular application other parameters of the design requirements such as the RF bandwidth, linearity, linearization technique and RF gain need to be considered. Understanding not only the strengths but also the limitations of a particular architecture is also important to assess the feasibility of implementing that architecture for an application.

Figure 14 represents the theoretical efficiency plots of some of the efficiency enhancement techniques discussed above. Doherty being a well understood and mature technique has many advantages over other efficiency enhancement techniques. Although efficiency enhancing techniques like Envelope Elimination and Restoration and Envelope tracking may provide greater performance than Doherty, their corresponding architectures are far more complex, costly to implement and as discussed previously, have various issues involved in implementation. The Doherty PA can accomplish high efficiency without adding any extra circuitry such as complex envelope control circuits used in Envelope elimination and restoration and Envelope tracking .Due to the simplicity of the Doherty configuration, conventional linearization methods like feed-forward and digital pre-distortion can be easily implemented with the Doherty amplifier. Compared to EER, ET and Chierex out phasing, Doherty technique also has much larger video bandwidth [41] which also helps to minimize memory effects. The main limiting factor of the Doherty technique is the quarter wave transformer. This makes this method limited to only narrow band designs. Since modern wireless communication spectrums utilize narrow bandwidths, this is not a severe drawback.

Another shortcoming is the gain degradation caused due to the peaking amplifier. The typical degradation for a symmetric Doherty design is around 2dB. As long as this degradation is considered at an early design stage in the link budget, appropriate driver amplifiers can be selected to compensate for this. This degradation can be also kept low with a higher gain main amplifier at low power levels. Another familiar issue that can be seen from the configuration of a Doherty system is resistive load matching. Techniques such as using offset lines to load modulate reactive termination have been studied [41] and been implemented in designs.

Achieving high efficiency for a pico-cell base station power amplifier would be tackled in this thesis. One of the main challenges of a pico-cell base station is the limited real estate. Since a Doherty PA can accomplish high efficiency at back- off power levels without adding any extra circuitry, this technique can be implemented on an integrated circuit (IC).Which makes this technique an ideal candidate for a pico cell application. Since the peak to average ratio of the signal of the targeted 4G standard would be around 6dB, a symmetrical Doherty design was selected for this design.

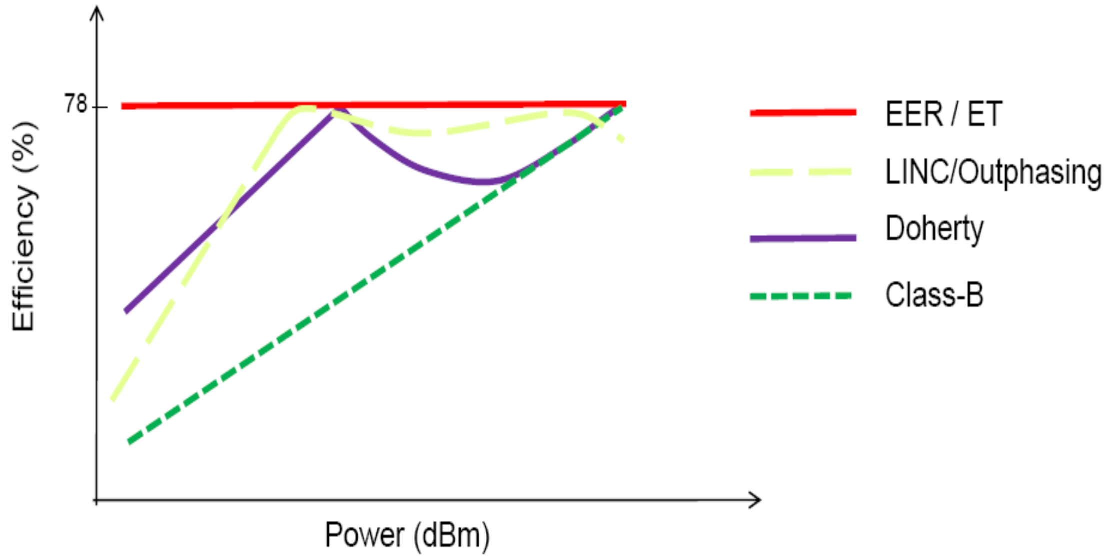


Figure 14: Theoretical efficiency behavior of various efficiency enhancement techniques [83].

2.5 Doherty Operation

The fundamental principle of operation of the Doherty architecture was briefly discussed in section 2.3.4. In this section an in-depth analysis of its operating principle is presented.

2.5.1 Doherty load modulation technique

As discussed in section 2.3, the most conventional configuration of a Doherty circuit consists of two amplifiers, namely the main and the peaking amplifiers. The peaking amplifier is also known as the “auxiliary” amplifier. The amplifiers are connected in parallel with their outputs joined by an impedance inverting quarter-wave transmission line. Each amplifier is biased into different bias conditions. The main amplifier is typically biased in Class AB and the peaking amplifier in class C. It is designed to have different load terminations at multiple power levels, so it has the optimized performed for each power level. Although the final output power is the combined output power of both main and peaking amplifiers, as the input drive level is reduced to a level typically 6dB below the maximum output power, the peaking amplifier is turned off. Therefore below the 6dB back off position, the number of active devices has been reduced by half, improving the efficiency at lower power levels significantly.

One of the key elements of the Doherty architecture is the active pulling or modulation of the main amplifier load impedance by the activity of the peaking amplifier. The active load pull technique is based on the principle that applying current from a second source can vary the resistance or reactance of a RF load. This concept is presented by Cripps in [17] as follows:

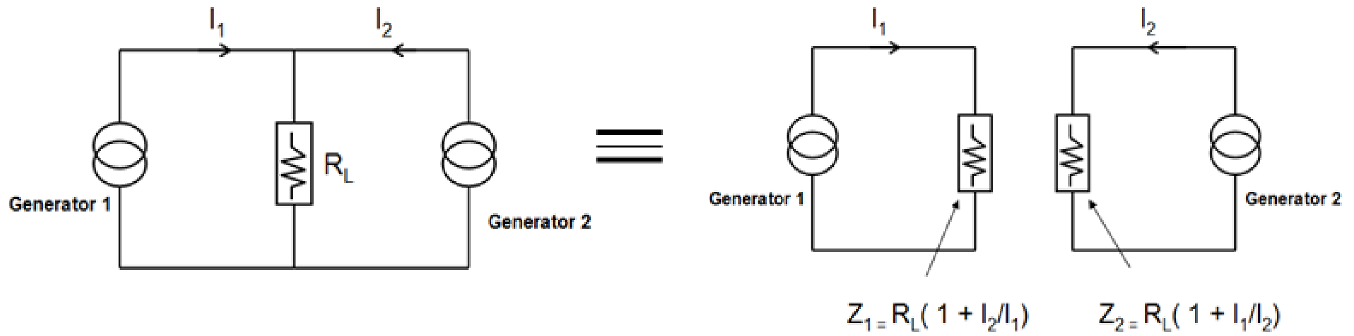


Figure 15: Active load modulation technique

Basic circuit theory suggests that when the supply current I_2 of generator 2 is set to zero, generator 1 would see a load resistance of R_L. If generator 2 starts to supply current along with generator 1 (I_1 and $I_2 > 0$), the voltage appearing across the load resistor R_L would change along with the resistance seen by generator 1 and generator 2.This concept can be extended to ac circuits by using complex notation for representing the magnitude and the phase of the currents and voltages and the resistive and reactive components.

Therefore the impedance seen by generator 1 and generator 2 when both generators are supplying current can be represented as:

$$Z_1 = R_L\left(1 + \frac{I_2}{I_1}\right) \tag{4.1}$$

$$Z_2 = R_L\left(1 + \frac{I_1}{I_2}\right) \tag{4.2}$$

If I_2 is in phase with I_1, the impedance Z_1 seen by generator 1 can be transformed to higher value. If I_2 is out of phase with I_1, Z_1 can be transformed to a smaller value. A key point to illustrate in the Doherty operation is the impedance inversion performed by the λ/4 wave transformer. A few derivations according to [17] are presented in order to illustrate the relationship between the voltages, currents and the impedances of the main and peaking amplifiers. Figure 16 shows an operational diagram to analyze the Doherty amplifier circuit.

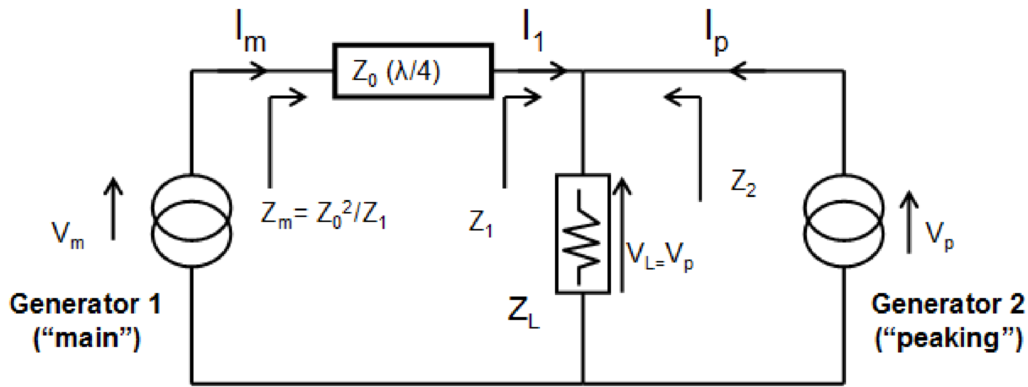


Figure 16: Operational diagram of the Doherty amplifier

Doherty amplifier configuration needs an impedance inverter between the main amplifier and the load Z_L, for the proper implementation of the load modulation. Note that although the quarter wave transformer is the most commonly used impedance inverter in a Doherty amplifier, other alternatives such an L or T networks can be used to achieve the same function [56].

An ideal impedance inverter transforms a current source into a voltage source. This relationship for figure 16 can be derived by looking at the impedance matrix of a lossless λ/4 wave transformer as follows [17]:

$$\begin{bmatrix} V_p \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ 1/jZ_0 & 0 \end{bmatrix} \begin{bmatrix} V_m \\ I_m \end{bmatrix} \tag{4.3}$$

The voltage of the peaking amplifier when it is operating at high power level can be deduced from (4.3) as:

$$V_p = jZ_0 I_m \tag{4.4}$$

From (4.4) it can be seen that the peaking amplifier output voltage, which is also equal to the load voltage, is dependant only on the main amplifier current. Expression for V_p shows that the output voltage is a simple linear function of I_m. At lower power levels only the main amplifier is active and delivers current. The peaking amplifier simply maintains the level of the main amplifier voltage Vm below the clipping level.

This relationship can be given by equation (4.5) below:

$$I_1 = \left(\frac{1}{jZ_0}\right)V_m \qquad (4.5)$$

Considering the 90^0 phase shift introduced by the λ/4 wave line, the peaking amplifier current can be expressed as jI_p . In reference to figure 16, the relationship between I_1 and jI_p can be expressed as in equation (4.6). This defines the current delivered by the peaking amplifier, at higher power when the peaking amplifier is active.

$$jI_p = \left(\frac{V_p}{Z_L}\right) + I_1 \qquad (4.6)$$

Therefore the impact of the peaking amplifier on the main amplifier voltage can be consolidated to the following:

$$V_m = Z_0\left[\left(\frac{Z_0}{Z_L}\right)I_m - I_p\right] \qquad (4.7)$$

The main point that can be understood from equation (4.7) is that the λ/4 wave line creates a relationship between the main amplifier and the peaking amplifier such that it prevents the main amplifier from exceeding its maximum voltage swing, keeping it constant until the peaking amplifier itself saturates [19]. Hence efficiency enhancement is attained in the 6dB backed off range by keeping Vm constant.

In order to characterize the impedances seen by the main and peaking devices during Doherty operation, the ideal characteristics of current and voltage of the main and peaking amplifier needs to be understood. Figure 17 shows the two device current amplitudes plotted as a function of voltage input drives [17]. Note that in this graph it is assumed that both main and the peaking amplifier have the same maximum linear current swing of Imax. Therefore the maximum linear value for each device will be Imax /2. The most important activity of the Doherty amplifier occurs during the upper 6dB region where both main and peaking amplifiers are active. In reference to figure 16 and figure 17, the currents of the main and peaking amplifiers can be expressed as follows:

$$\left.\begin{aligned} I_m &= \frac{I_{\max}}{4}(1+\gamma) \\ I_p &= \frac{I_{\max}}{2}(\gamma) \end{aligned}\right\}\gamma = 0 \text{ and } 1 \qquad (4.8)$$

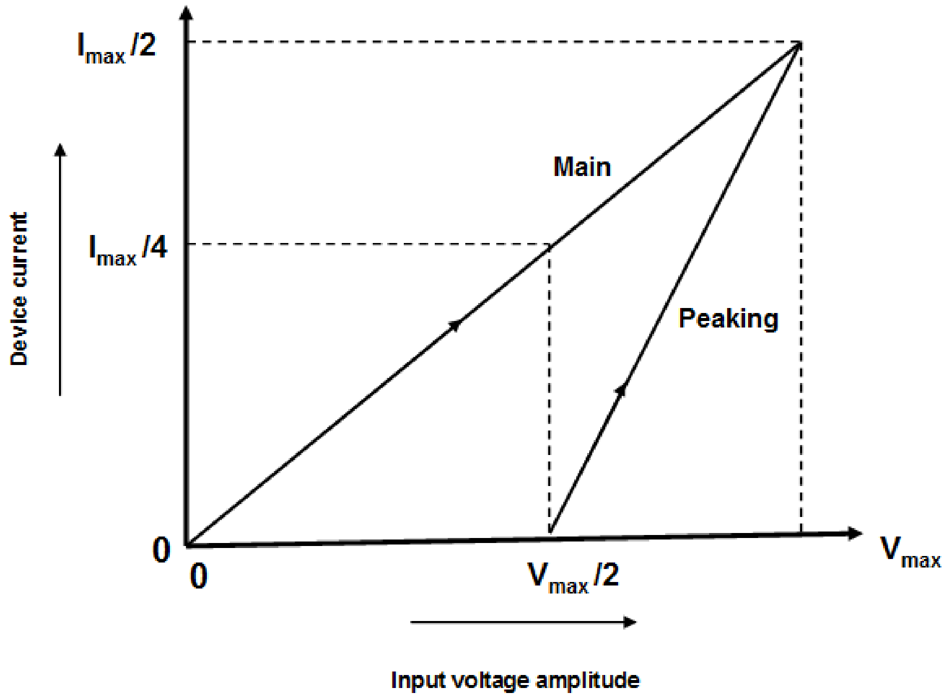


Figure 17: Main and peaking device currents Vs input voltage amplitude

where γ = 0 corresponds to the 6dB back off point and γ = 1 to the maximum power point. Now we can proceed to derive how the λ/4 wave transformer, causes the impedance seen by the main amplifier to reduce as the peaking amplifier current I_p increases. If the load modulation equation (4.1) and (4.2) is applied to Figure 16, the impedances on each side of the load impedance Z_L can be gives as:

$$Z_1 = Z_L\left(1 + \frac{I_p}{I_1}\right) \quad (4.9)$$

$$Z_2 = Z_L\left(1 + \frac{I_1}{I_p}\right) \quad (4.10)$$

The relationships between the input and output voltages and currents of the λ/4 wave transformer can be defined as follows:

$$I_l V_p = I_m V_m \quad (4.11)$$

since

$$Z_0^{\ 2} = Z_m Z_1 \quad (4.12)$$

and

$$Z_0^{\,2} = \left(\frac{V_m}{I_m}\right)\left(\frac{V_p}{I_1}\right) \tag{4.13}$$

From (4.13) and (4.11):

$$I_1 = \frac{V_m}{Z_0} \tag{4.14}$$

Substituting I_1 in the expression for Z_1 in (4.9) would give:

$$Z_1 = Z_L\left(1 + \frac{I_p Z_0}{V_m}\right) \tag{4.15}$$

Substituting (4.15) in (4.12) gives the output impedance seen by the main device:

$$Z_m = \frac{Z_0^{\,2}}{Z_L\left(1 + \frac{I_p Z_0}{V_m}\right)} \tag{4.16}$$

where $V_m = I_m Z_m$. By using the relationship defined in (4.8) and (4.16), V_m (which is the amplitude of the RF voltage swing at the output of the main device) can be re-written as the following:

$$V_m = \frac{Z_0^{\,2}\left(\frac{I_{max}}{4}\right)(1+\gamma)}{Z_L\left(1 + \frac{\left(\frac{I_{max}}{2}\right)(\gamma)Z_0}{V_m}\right)} \tag{4.17}$$

(4.17) can be re-written as:

$$V_m = \left(\frac{Z_0}{2Z_L}\right)\left(\frac{I_{max}}{2}\right)\left(Z_0 + \gamma(Z_0 - 2Z_L)\right) \tag{4.18}$$

Earlier it was stated that the λ/4 wave line creates a relationship between the main amplifier and the peaking amplifier such that it prevents the main amplifier from exceeding its maximum voltage swing, keeping it constant until the peaking amplifier itself saturates. Therefore efficiency enhancement in the 6dB backed off range is attained when V_m remained constant.

By examining equation (4.18) it can be seen that the main device voltage becomes independent of γ and V_m remains constant only if $Z_0 = 2Z_L$. Therefore, by having the characteristic impedance of the $\lambda/4$ wave line twice the resistive load, the main amplifier sees twice the output impedance and reaches the maximum voltage when the current is only half the maximum value at back off power levels.

2.5.2 Doherty Amplifier Operation

The Doherty amplifier operation can be described based on three operating regions related to the input power levels, namely low, medium and high power regions. Depending on the input drive level, the load impedances seen by the main and peaking amplifier will change based on the technique described in section 2.5.1.

Based on figure 16, the load impedances of main and peaking amplifiers for the operating regions can be summarized as follows by equation (4.19) and (4.20) [17]:

$$Z_m = \begin{cases} \dfrac{Z_0^{\ 2}}{Z_L} & 0 < V_{in} < \dfrac{V_{in\max}}{2} \\[2ex] \dfrac{Z_0^{\ 2}}{Z_L\left(\dfrac{I_m + I_p}{I_m}\right)} & \dfrac{V_{in\max}}{2} < V_{in} < V_{in\max} \end{cases} \tag{4.19}$$

$$Z_2 = \begin{cases} \infty & 0 < V_{in} < \dfrac{V_{in\max}}{2} \\[2ex] Z_L\left(\dfrac{I_m + I_p}{I_p}\right) & \dfrac{V_{in\max}}{2} < V_{in} < V_{in\max} \end{cases} \tag{4.20}$$

- *Low power region of operation:*

In the low-power region ($0 < V_{in} < \frac{V_{in\max}}{2}$), the peaking amplifier is turned off and in reference to figure 18, the main amplifier sees the load Z_1 inverted to Z_m by the λ/4 line. The peaking amplifier sees very large impedance (theoretically an open circuit) and facilitates the load impedance of the main amplifier to be two times larger than that of the optimum resistance required to deliver maximum power. Therefore, the high output impedance seen by the main amplifier forces it to saturate prematurely. At this point, at an input voltage of $\frac{V_{in\max}}{2}$, the maximum fundamental current swing is half and the voltage swing reaches V_{dc} which is the ideal maximum voltage swing [17]. As a consequence of this, half of the main amplifier's allowable power level (a quarter of the total maximum power or 6 dB down from the total maximum power) is presented, while the efficiency is equal to the maximum efficiency of the main amplifier. This is shown in figure 19 below. Note that, 78.5% theoretical maximum efficiency illustrated in figure 19 is based on a class B operation of the main amplifier. In conclusion, at low input drive levels the main amplifier is presented with a high efficiency load and the since peaking amplifier is off the efficiency is maximized.

- *Medium power region of operation:*

In the medium power range ($\frac{V_{in\max}}{2} < V_{in} < V_{in\max}$), the peaking amplifier is turned on and starts to generate current while the main amplifier is saturated. By inspecting the equation (4.19), it is evident that the peaking amplifier current contributes in modulating the load impedance seen by the main amplifier.

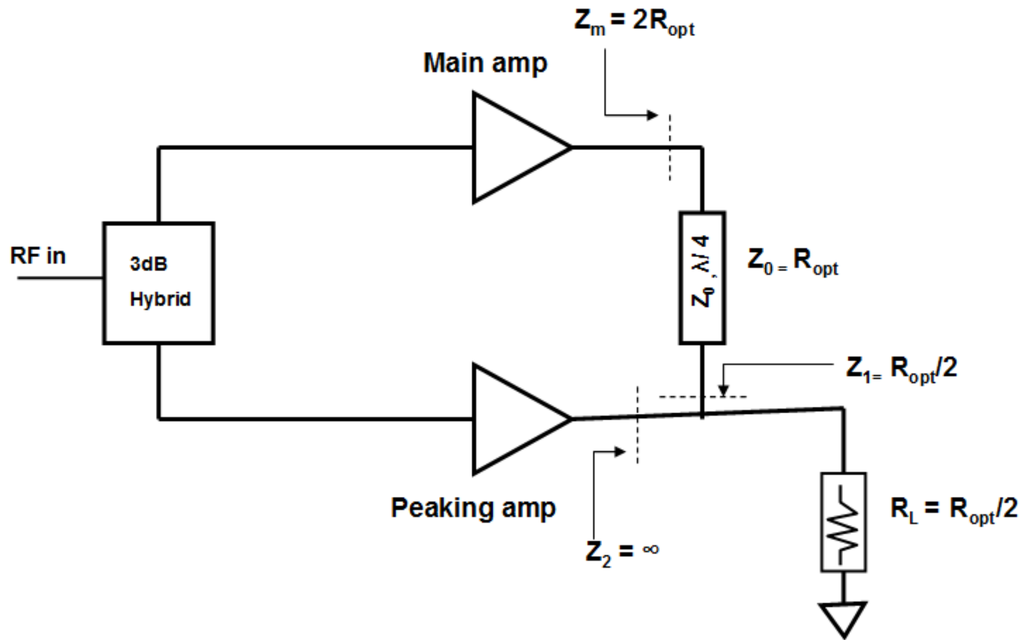


Figure 18: Doherty low power operation diagram

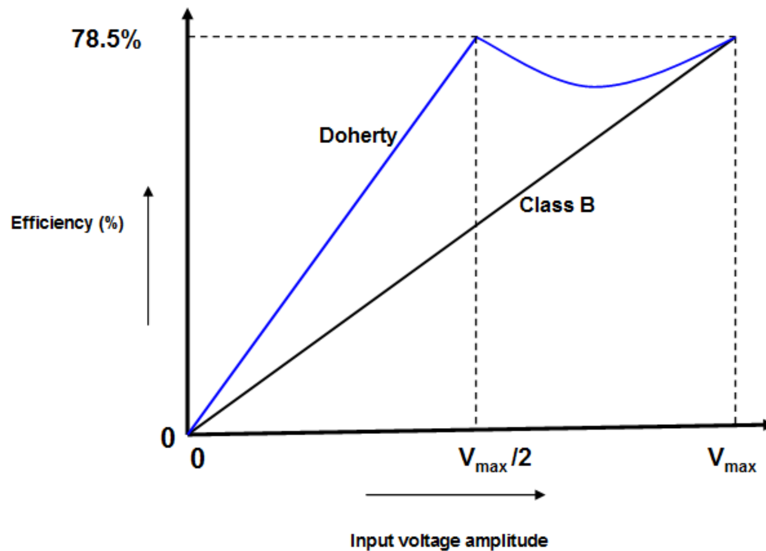


Figure 19: Doherty amplifier efficiency Vs input drive level

Implementing the load modulation technique described in section 2.5.1, it can be seen that the as the peaking amplifier current increases, the impedance Z_1 shown in figure 20 would be increased.

With the λ/4 line, this would be transformed to a reduced Z_m seen by the main amplifier. This will prevent the main amplifier from exceeding its maximum voltage swing, keeping the out-

put voltage constant while still generating output current. The output power of the Doherty system increases since the peaking amplifier is starting to deliver power to the load and the main amplifier is able to contribute more power due to the increased output current. As the input level increases, the output impedance of the peaking amplifier keeps decreasing and that of the main amplifier with the quarter wave transmission line keeps increasing. Figure 21 summarizes the behavior of voltage amplitudes of the main and peaking amplifiers over the full power range [17]. The output voltage of the main amplifier increases linearly with the input voltage, with a forced saturation up to the maximum voltage point. Once it reaches saturation, it remains constant for the upper 6dB range of operation. Since the voltage amplitude is remained constant closer to saturation at an ideal maximum level, the efficiency stays close to the maximum.

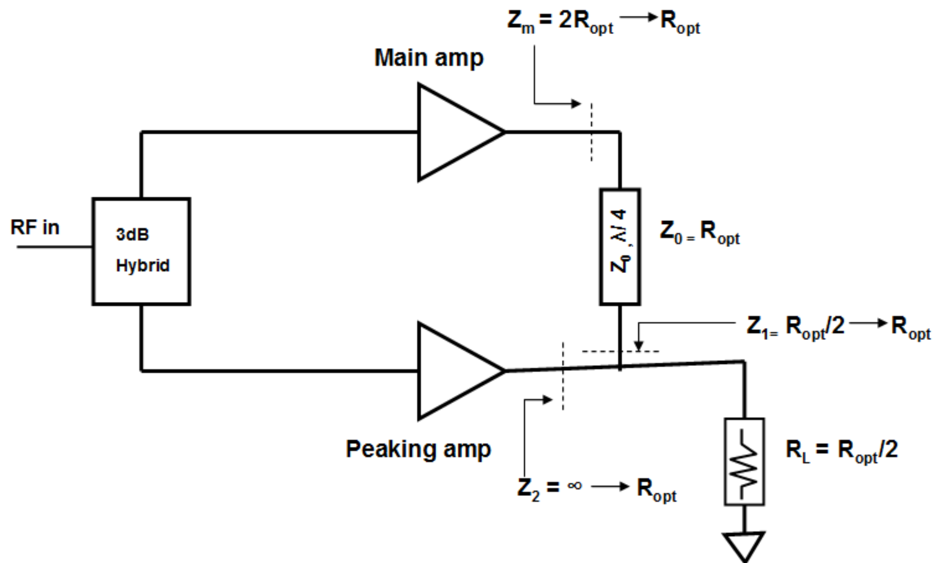


Figure 20: Doherty medium power operation diagram

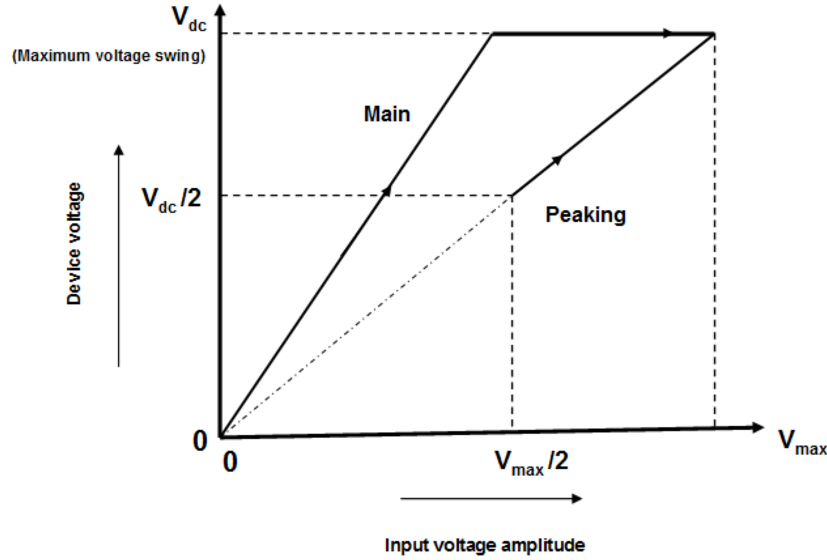


Figure 21: Main and peaking device voltages Vs input voltage amplitude

- *High power region of operation:*

With the increased input level, the load impedance Z_2 seen by the peaking amplifier in figure 22 is altered until the peaking amplifier is saturated. At this point both main and peaking amplifiers are both presented with the maximum power load R_{opt}. Therefore in this power region, with high input drive levels both amplifiers are saturated and deliver equal power to the load.

The maximum output power of the Doherty amplifier is achieved at this point. Overall drain efficiency of the full Doherty system is derived by Cripps in [17] as:

$$\eta = \frac{\pi}{2} \frac{\left(\frac{V_{in}}{V_{\max}}\right)^2}{3\left(\frac{V_{in}}{V_{\max}}\right) - 1} \tag{4.21}$$

where $V_{in}=V_{max}$ would be the maximum power condition and $V_{in}=V_{max}/2$ would be the 6dB back off condition. This theoretical overall efficiency for a symmetrical two way Doherty system has been plotted as a function of power back off in figure 23. Note that, 78.5% theoretical maximum efficiency illustrated in figure 23 is based on a class B operation of the main amplifier.

The slight dip in efficiency in the middle is caused by the DC consumption of the peaking amplifier.

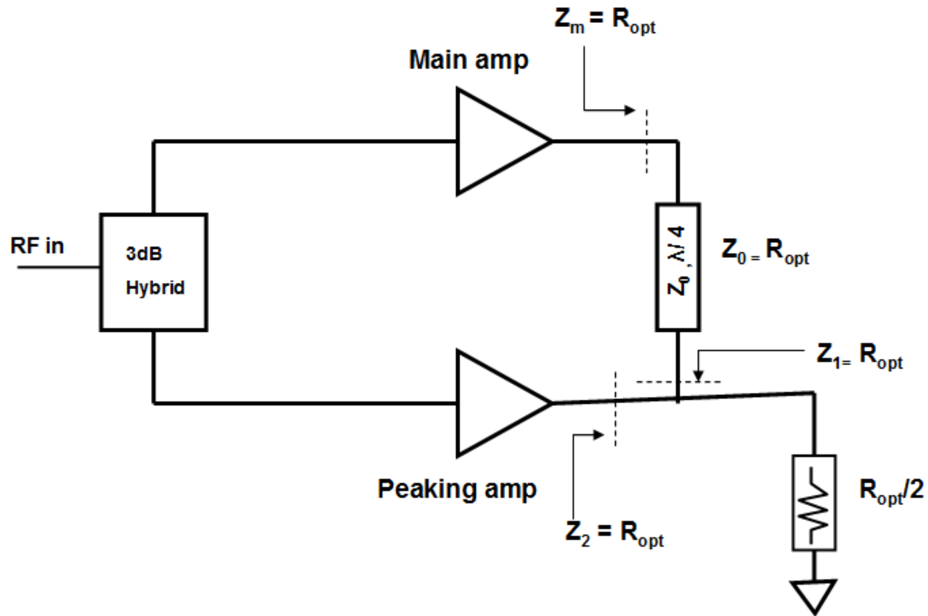


Figure 22: Doherty high power operation diagram

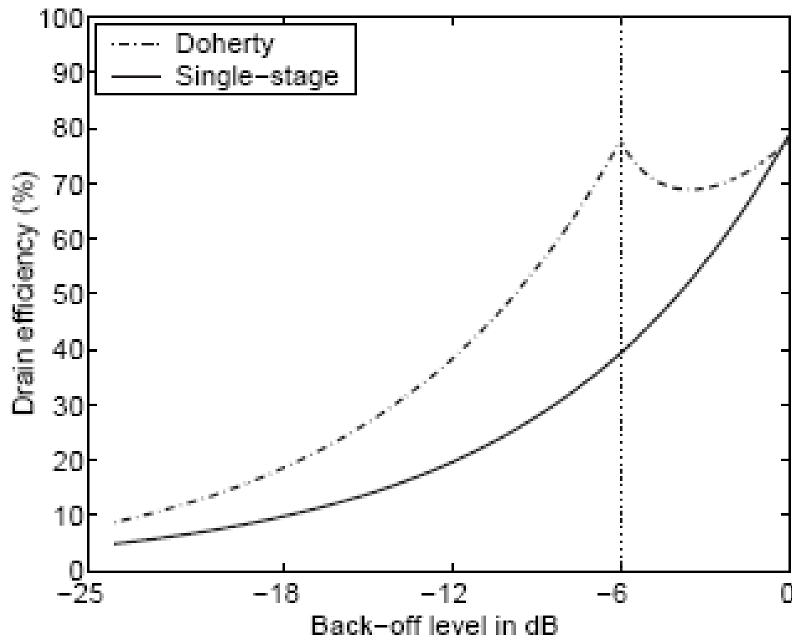


Figure 23: Doherty amplifier efficiency Vs power back off

2.6 Conclusion

The Doherty technique has already been implemented using a variety of device technologies, predominantly using LDMOS and GaAs. With these technologies, the reported efficiency numbers have been lower than the theoretical efficiencies, especially at frequencies higher than 2.5GHz.Emerging device technologies such as the GaN technology presents an attractive option for Doherty design due its low output capacitance and high output impedance. This aspect of GaN devices simplify the matching networks significantly, which makes it a more favorable option when implementing a PA design on a very small design real estate of an IC. Therefore, in this thesis GaN power cells are used to implement the Doherty design. Detailed discussion on the GaN HFET technology would be discussed in Chapter 3.

Chapter 3 Semiconductor Technology Selection and GaN Large-Signal Model Evaluation

3.1 Semiconductor Technology selection

The RF power amplifier, a key module of a base station, can be designed using transistors from a wide variety of semiconductor technologies. Apart from the performance specifications as output power, efficiency, and linearity, there are additional requirements that a power amplifier transistor needs to consider, such as supply voltage, ruggedness, physical size, reliability, and cost. Depending on the modulation format of the wireless system, the transistors for the power amplifier may have different specifications. An excellent study comparing the performance of RF output devices from various device technologies such as InGaP HBT, EpHEMT, Si BJT, SiGe HBT, and Si LDMOS technologies for GSM, CDMA, and WCDMA applications is presented in [43, 44].

A broad range of semiconductor technologies, such as Si LDMOS FET, Si BJT, GaN HFET, GaAs MESFET, GaAs HEMT, and GaAs HBT have been used to design RF power amplifiers. The type of semiconductor technology plays a critical role in the RF power amplifier performance. Each of the technologies has its strengths and limitations. For instance, if GaAs HBT, GaAs FET and LDMOS FET are compared, following can be observed; GaAs HBT's have the highest power density which leads to the smallest amplifier die size, GaAs FET's have lower RF power density but has higher power gain and PAE. Even though Si LDMOS FETs have the lowest power densities leading to the largest die sizes they are the lowest in cost [45]. In general, Si LDMOS FET’s are much more rugged as well [45]. Ruggedness of an amplifier is its ability to survive large load mismatches, while delivering the rated output power.

Another requirement that has been growing in demand is the thermal stability of high power RF devices. Most common power devices that are currently used are Si LDMOS FETs and

GaAS MESFETs. These device technologies are reaching their maximum capabilities. Hence more emphasis has been placed on research and material processing technologies for device technologies like SiC MESFET and GaN HEMT [46] [47]. Among these, GaN devices produce higher output power and power efficiency [47]. GaN device technology has greater advantages beyond other materials such as GaAs, SiC and Si, not only in terms of high power but also the range of frequency operation [30]. The wide bandwidth is achieved in GaN due to higher input and output impedances. Higher power is achieved due to the high charge density of the material.

The Doherty power amplifier architecture on MMICs has been implemented using various device technologies, predominantly using Si-LDMOS [48] and GaAs [49] devices. But the efficiencies achieved at frequencies, especially higher than 2.1GHz has been lower than theoretical efficiencies. Hence, newer device technologies like GaN should be further analyzed to achieve maximum possible efficiency. The GaN technology presents an attractive option for MMIC Doherty design, due to its high power density, higher efficiencies at high frequencies, and high output impedance which can simplify the matching network significantly.

The next section of this chapter will present an overview of GaN material properties. A comparison of GaN properties to some other semiconductors as Si and GaAs will also be discussed. Some commonly known limitations and issues with the GaN technology will be provided in section 3.1.2

3.1.1 GaN properties

The most important properties of a semiconductor material that influences the power amplifier performance are the breakdown field, thermal conductivity, energy band-gap, and electron velocity [50]. Table 1 is a quick summary of how each of these material properties can influence the power amplifier system performance. As seen in that table, there is a direct relationship between the material properties, device characteristics and power amplifier system performance. Therefore, it is critical to select the appropriate device technology to meet the power amplifier design requirements. Several of these material properties of common semiconductor materials as Si, GaAs, and GaN are summarized in table 2.

Table 1: Semiconductor material properties and their relationship with power amplifier system performance [50].

Material property	Device characteristics	Improved device metrics	System Advantages
High breakdown field	High voltage High doping	Power density Gain Efficiency Larger output impedance levels	The higher power density will reduce the number of die used Improved output impedance characteristics with lead to increased bandwidth Higher efficiency will lead to lower total energy usage
Wide Band-gap High Thermal Conductivity	High temperature	Smaller die size More power per die	High Thermal conductivity will allow the possibility of smaller packages and will reduce the system cooling requirements. The band-gap determines the upper temperature limit of device operation. Hence, wider band gap devices are able to withstand higher channel and ambient temperatures, which will also reduce the system cooling requirements
High Electron Velocity	High Frequency	High ft High fmax	High electron velocities will contribute to a very high speed device which results in high system frequencies

Table 2: Material Properties of GaN, Si and GaAs [50]

Property	GaN	Si	GaAs
Band-gap (eV)	3.4	1.11	1.43
Breakdown field (V/cm)	35×10^5	7×10^5	7×10^5
Saturation velocity (cm/sec)	1.5×10^7	1×10^7	1×10^7
Saturation field (V/cm)	15×10^3	8×10^3	3×10^3
Thermal conductivity (W/cm-K)	1.7/substrate*	1.5	0.46
Electron mobility (Cm^2/V-sec)	1000	1350	6000
Hole mobility (Cm^2/V-sec)	300	450	330

*Refer to section 3.1.1 for details on GaN substrate materials

From the table above, it can be seen that GaN has material properties that would be suitable for high power implementations. For instance GaN has breakdown fields five times that of Si or GaAs. Breakdown field determines the highest operating voltage of a transistor for a given device design and channel doping [50]. Higher operating voltage results in higher power handling capabilities and higher power density in the device. Due to this GaN devices can be operated with high drain voltages since its break down voltages are greater than 70V [19].

GaN also has a large band-gap of 3.4 eV compared to Si, GaAs .This gives GaN an advantage in high temperature performance over Si and GaAs, since the band-gap determines the upper temperature limit of device operation. For this reason, GaN devices would be able to withstand higher ambient and channel temperatures. GaN can operate at higher channel temperatures up to 300 ^{0}C [19].

GaN has a saturated electron velocity of 1.5 x 10^{7}cm/second, which is still higher than that of Si or GaAs. The saturated electron velocity of device determines the frequency performance, in particular, f_t of a device [50]. Due to this high cut off frequency, GaN is able to operate at frequencies much higher than Si and GaAs.

Note that GaN have electron and hole mobilities much less than Si and GaAs. Low mobility results in increased parasitic resistance, increased losses, and reduced gain [50]. These problems are worsened as operating frequency is increased. Therefore when using a GaN device for a power amplifier design, it is important to keep in mind the lower gain of the amplifier path, so driver amplifiers may be included in the link budget to compensate for the low gain.

GaN devices have been grown on a number of different substrates such as Silicon (Si), Silicon carbide (SiC) and Sapphire. Compared to other available substrate choices, Sapphire is relatively cheap and is offered in large diameter (4″ to 6″) wafers [50]. At microwave frequencies it works great as a low-loss substrate. However due its low thermal conductivity of 0.46 W/cmK Sapphire will severely limit the power density and total power performance of devices fabricated on it [50].SiC on the other hand has a thermal conductivity of 4.9 W/cm-K that is three times that of Si and ten times that of Sapphire. This gives a tremendous advantage for SiC-based devices. SiC also have much better microwave performance than devices fabricated on highly doped silicon substrates [50].The best GaN performance has been from devices utilizing semi-insulating SiC substrates [50]. Although GaN-on-Si platform

technology is not as mature, efforts are now focused on continual evolution of this technology.

The resulting GaN-on-Si device technology offers high power performance at high levels of reliability and is ideally suited for large area RF circuits. Compared to SiC, it is also less costly and is in high volume production today and readily available [30].The cost of a high resistivity silicon substrates is a fraction of the cost of 2" high resistivity SiC substrates which are limited in quality, volume and availability [30].Based on the reliability results of GaN-on-Si, it has been shown that that GaN-on-Si offers superior reliability to other substrates [30].

3.1.2 GaN issues and limitations

Despite all the great characteristics of GaN devices, this device technology is still not mature and has various issues that are still being addressed. The main reported problems of GaN devices are current collapse, drain current compression and frequency dispersion of transconductance and capacitances [50 - 53]. These issues of GaN devices have been attributed primarily due to the trapping effects. Trapping effects can be described as the surface trapping-detrapping of electrons at the various surface states or trap states in the GaN structure [50, 53]. Trap states refer to the deep level states in the band-gap [19]. Detailed discussion of the GaN device trapping and de-trapping process is presented in [51].These trap states induce power loss, degrade power handling capability and causes voltage delays in device operation [51]. Current collapse or current dispersion can be described as discrepancy between the DC predicted and RF measured performance [53]. This phenomena leads to changes in the maximum drain current and knee voltage. These result in a change of load line and reduced power and gain. Any type of DC-to-RF dispersion causes device degradation and makes circuit design very difficult. Various solutions to minimize some these problems have been proposed. An overview of these proposals can be found in [53].

Despite these limitations of GaN, outstanding device performance (i.e reported fmax = 139 GHz and power densities of 30 W/mm [50]), can be seen from this relatively immature technology. Any performance limiting effects will have to be eliminated for these devices to move from research to mass production.

3.1.3 GaN MMIC process

The technology being explored in this project is Gallium Nitride (GaN)-based Heterostructure field-effect transistor (HFET) technology offered by the Canadian Photonics Fabrication Centre (CPFC) of National Research Council (NRC). It is fabricated on 3-inch diameter Silicon Carbide (SiC) wafer. This MMIC circuit process of the HFET involves a total of nine mask steps. The overall process includes a standard GaN device process. Thorough explanation of process details can be found in [78]. The layer numbers in the foundry is used to define the mask levels used at the various steps of the process. In total there are 9 layers [78]:

- Layer 1-Mesa
- Layer 2-Ohmic
- Layer 3-Gate
- Layer 4-Via1
- Layer 5-Nichrome
- Layer 6-1Me
- Layer 7-Via2
- Layer 8-Bridge
- Layer 9-2Me

The process sequence steps applied to the HFET is described in the GaN foundry user manual as follows [78]:

1. In the fundamental stage in the processing of the device, the Ohmic contact is defined using the Ohmic mask and the contacts are deposited.
2. The second step in the process is the definition of the active area of the devices using the Mesa mask, and etching the area outside it down to the buffer layer.
3. In the third step the gate metal in the channel area is deposited using the Gate mask.
4. The wafers are then passivated using a thin layer of dielectric. This is a critical layer since it modifies the electrical properties of the surface of the AlGaN layer and provides added isolation between the substrate and metal layers after. Via1 mask is used to define openings in a resist layer to etch the needed openings into the dielectric.
5. Next a thin layer of Nichrome is deposited where resistors are required.

6. 1μm of gold is used as the first level on interconnect metal. It is deposited using the 1Me mask. The 1Me has contacts to the gate pads, the nichrome layer and the ohmic metal.
7. Then a thin layer of dielectric is deposited to be used as the insulator in the MIM capacitors. The Via2 mask is used to define the vias for the openings in this layer.
8. In the next step, a second level of interconnect is introduced to bridge over other layers. It is defined in a temporary layer of a special resist using the Bridge mask.
9. In this step, another layer of interconnect is defined using the 2Me mask. This layer is usually 1 μm of gold. 2Me is used to make the top layer of the MIM capacitors.

3.2 Conclusion

In conclusion, Gallium Nitride (GaN) is a new device technology that shows greater advantages beyond other materials such as GaAs and Si LDMOS for RF power amplifier design. Silicon LDMOS performance drops off as the frequency of operation increases to >2.5GHz while GaAs suffers from low power even though it has potential to operate at high frequency. This can be seen by the comparisons shown in figure 24 and figure 25. The material properties of GaN produce devices that have high breakdown voltages and high power densities that can operate at higher frequencies. This results in low parasitic capacitance and high input and output impedances. High impedance levels and low output capacitance plays an essential role in designing broadband amplifiers that are highly linear and efficient.

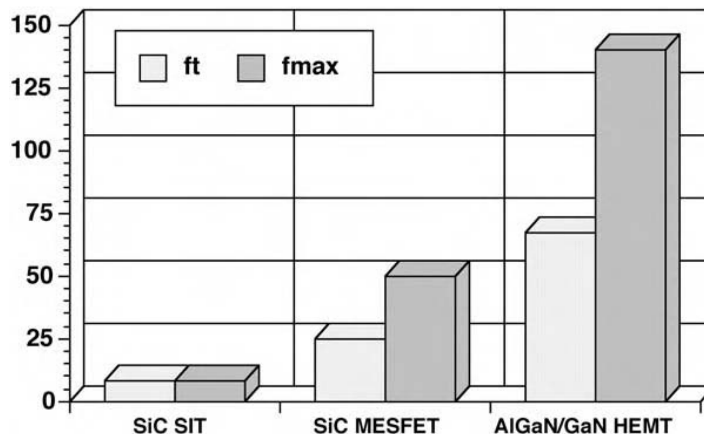


Figure 24: Comparison of highest reported ft and fmax for different RF device technologies [50]

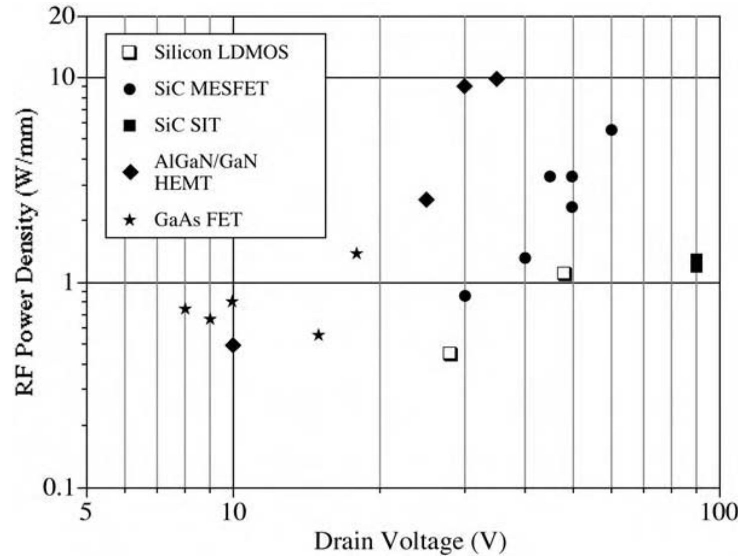


Figure 25: Comparison of RF power density for different RF device technologies [50]

3.3 Transistor model evaluation with a Single stage GaN PA design using CGH25120F

Power amplifier design is a multi-step design procedure that is complex. Through the use of accurate and reliable large-signal device models, the design process can be carried out from start to end and the designer can have a reasonable idea of what to expect when the design is fabricated.

The performance of the GaN MMIC Doherty amplifier designed in this thesis is assessed based on the simulated performance using large-signal models. Hence, it was essential to assess the accuracy and reliability of large-signal models for a new device technology as GaN .It was crucial to perform an experiment to validate the large-signal models for GaN devices by comparing the measured and simulated behavior of a GaN power amplifier design. Therefore, in this section an analysis of a classical printed circuit board (PCB) design of a single stage class AB amplifier using Cree’s CGH25120F GaN HEMT transistor will be presented. A comparative analysis of the performance between the simulated data using the large signal model of CGH25120F and measured data of the CGH25120F will be discussed.

The content of this section can be split into two distinct categories; theoretical simulations using a large-signal model and practical performance testing. For the practical performance testing, Cree's Class AB evaluation board design for CGH25120F was utilized. Cree's large-signal model for CGH25120F was used to simulate the evaluation board design in Agilent's Advanced Design System (ADS) and Agilent's Momentum. The performance of the simulated and measured data will be analyzed to assess the large-signal model of the GaN HEMT. The frequency range of operation for this analysis would be the same range of operation as the MMIC design presented in this thesis, which is 2.62-2.69GHz, which covers the range for down link operation of LTE band 7.

3.3.1 DC analysis

As the first step in characterizing the GaN HEMT device, an analysis of the DC output and transfer characteristics of CGH25120F will be discussed in this section. The operating points of the HEMT corresponding to the different classes of operation can be easily assessed from the transfer characteristics as shown in Figure 26. The plot represents the range of gate voltages and the corresponding mode of operation with a drain voltage of 28V. The specified quiescent drain current (Idq) for the CGH25120F evaluation board is 500mA [54]. The results of this analysis provide a better understanding of the bias voltage requirements and how it is operated at an Idq of 500mA.

It can be seen from figure 26 above that the HEMT model predicts a rapidly increasing drain current as the gate to source voltage (Vgs) exceeds around -3.4V with saturation occurring around 0.8V.For class AB operation this transistor would need to be biased between the class B operation and class A operation point. Since the datasheet recommends an Idq of 500mA, a closer look at the class AB bias region is shown in figure 27. Figure 28 shows the DC output characteristics of the GaN HEMT. The output characteristics provide a method to identify the device's linear and saturation regions.

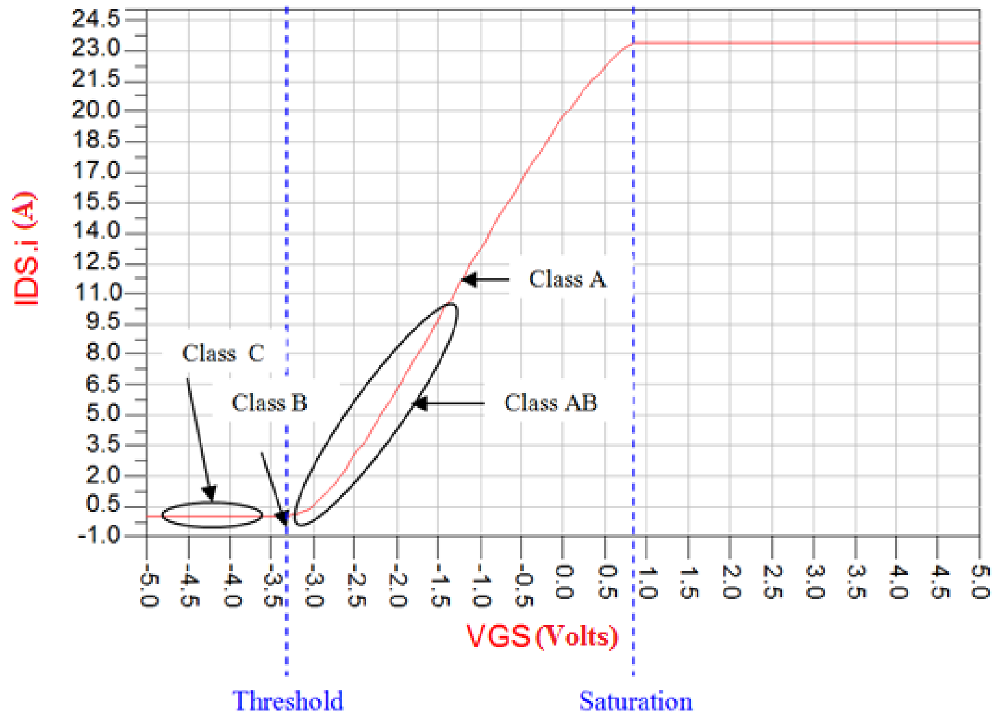


Figure 26: CGH25120F large signal transistor model's transfer characteristic

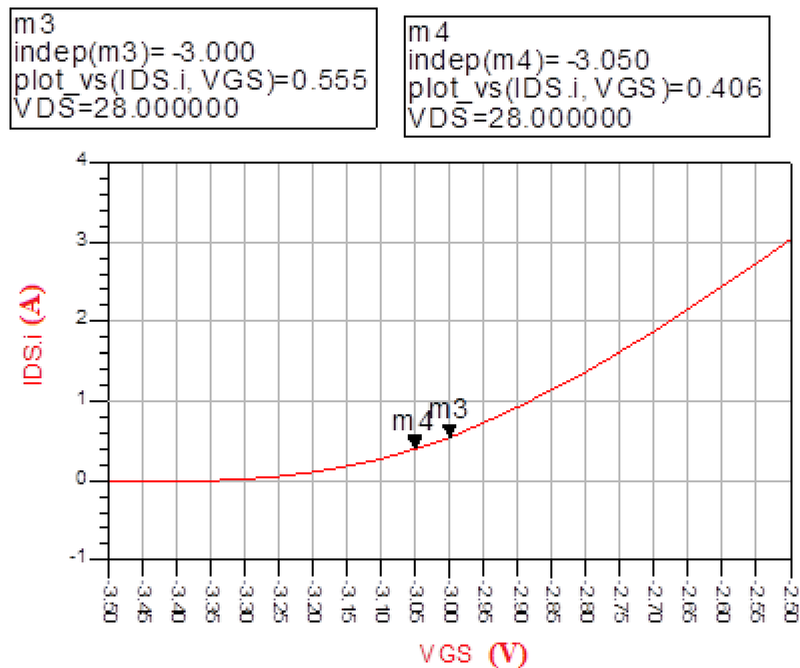


Figure 27: A closer look at the quiescent current (Idq) Vs gate to source voltage (Vgs) for class AB operation of CGH25120F

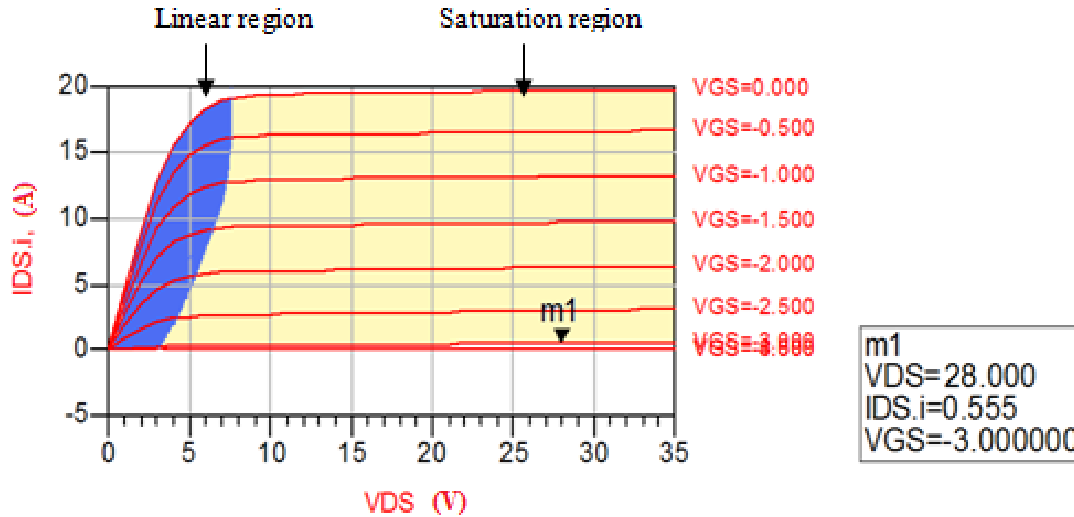


Figure 28: DC output characteristics of CGH25120F

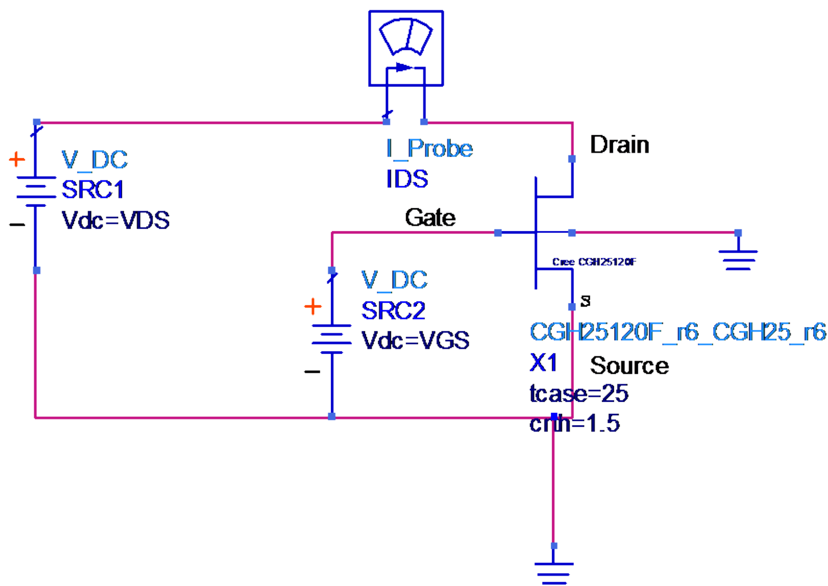


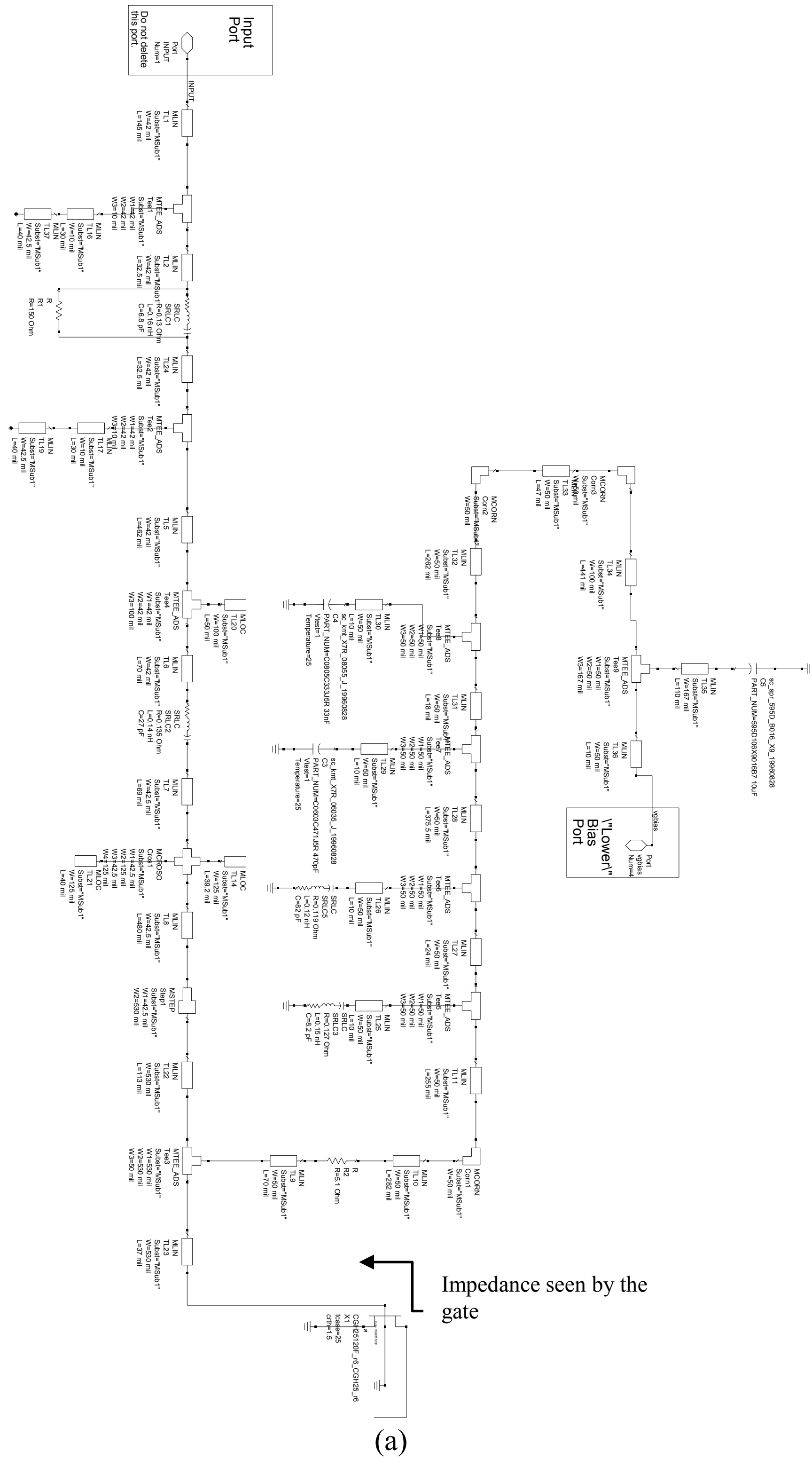
Figure 29: Test bench for DC analysis of Cree's CGH25120F large signal transistor model

The above graphs clearly indicate that the required Vgs to achieve an Idq of 500mA is around -3.02V.Such an operating point will allow for class AB operation of the CGH25120F GaN transistor. Note that during the practical measurements in the lab, a Vgs of -3.26V needed be applied to achieve 500mA for a 28V supply voltage.

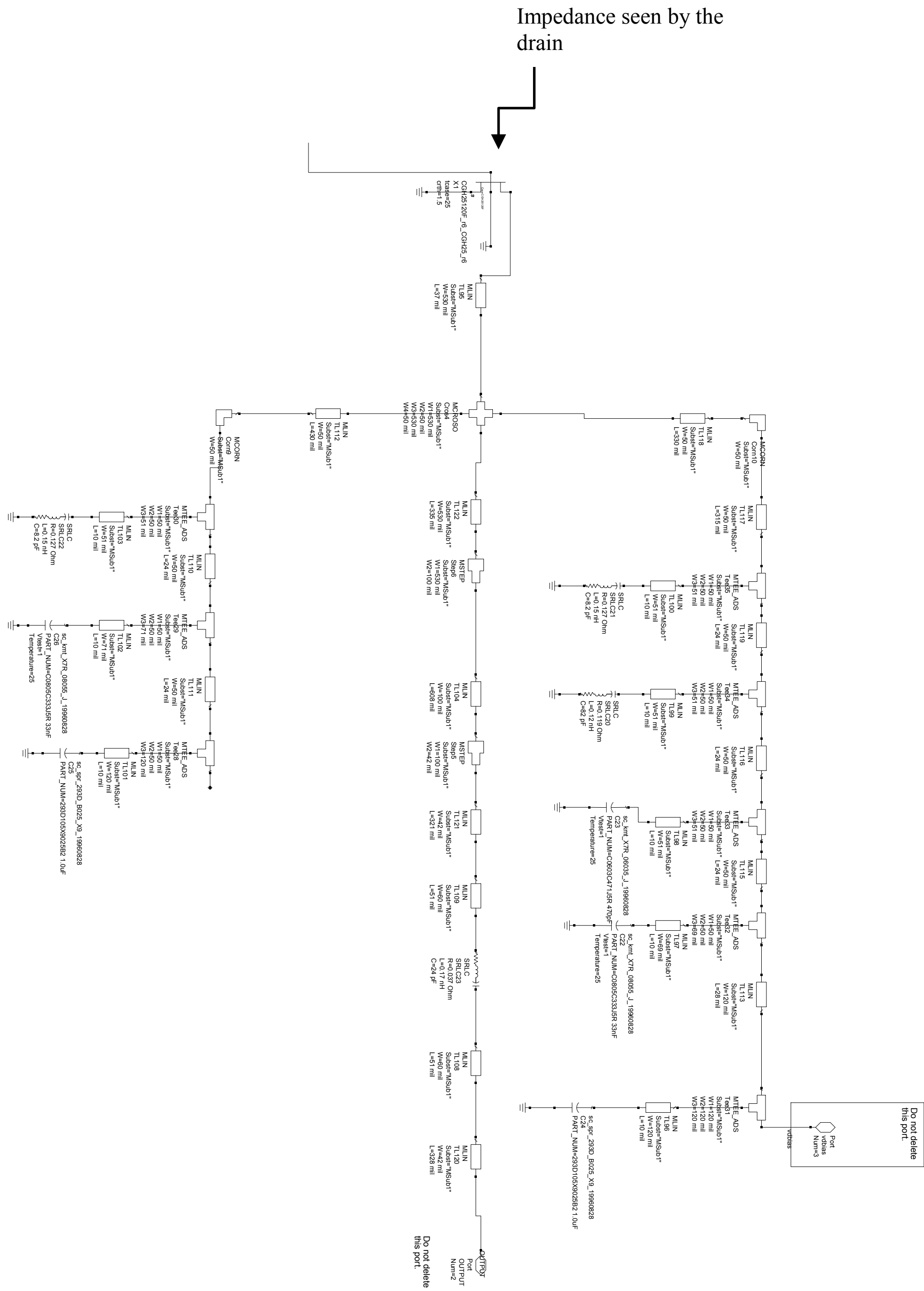
3.3.2 CGH25120F evaluation board matching network analysis

In order to evaluate the CGH25120F large signal model, first, the matching networks implemented on Cree's CGH25120F evaluation board was simulated in ADS and Momentum to work out the impedances the evaluation board was designed to.

Load-pull simulations were further performed on the GaN HEMT to assess the contour results at the impedances of the matching networks extracted from the previous step. Since Cree designs their evaluation boards based fully on Load-pull data extracted from the large signal models, the simulated results and measured results are expected to yield results without much deviation. The dimensions of the distributed elements in the matching networks and the bill of material of the CGH25120F printed circuit board was extracted from the CAD files received from Cree in .dxf format. Substrate properties such as height (20 mil), loss tangent (0.004) and relative dielectric constant (3.66) used in the simulations resemble the properties of Rogers 4350B material used by Cree. The ADS schematic for the input and output matching networks of CGH25120F, including their gate and drain bias networks are presented in figure 30 below. The Momentum layout of the input and output matching networks with bias feeds are presented in figure 31 and figure 32 below.



(a)



(b)

Figure 30: ADS schematic of CGH25120F evaluation board matching networks ; (a) input matching (b) output matching

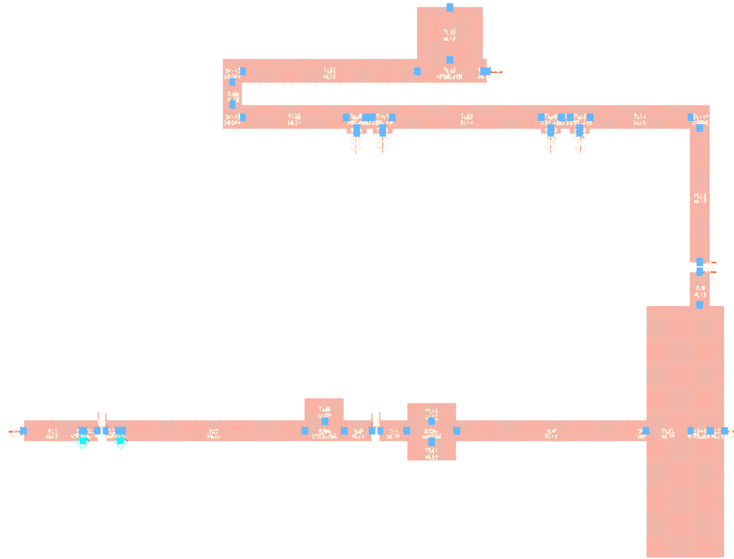


Figure 31: Layout of CGH25120F evaluation board input matching network with bias feeds

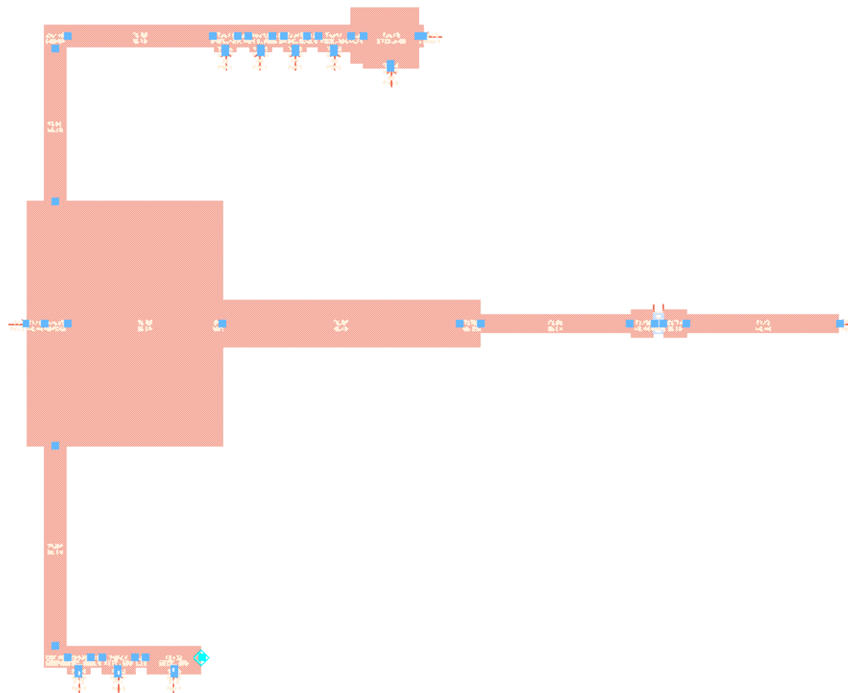


Figure 32: Layout of CGH25120F evaluation board output matching network with bias feeds

Table 3 summarizes the measured and simulated gate and drain impedances achieved at 2.650GHz.

Table 3: Comparison of measured and simulated impedances of CGH25120F

	Datasheet measured impedance of the evaluation board at 2.650GHz	Impedance of the simulated structure with Momentum at 2.650GHz	Impedance of the simulated structure with ADS at 2.650GHz
Impedance seen by the device gate	4.39-10.3j	4.32-10.9j	4.04-12.8j
Impedance seen by the device drain	3.98-1.37j	3.35-2.87j	4.22-2.53j

From this table, it can be been that both momentum and ADS simulations provide close impedances to the measured impedances stated on the datasheet [54] for the CGH25120F evaluation board. Since momentum simulations would provide the closest estimation of the actual effects of the copper structures, for further assessment of the CGH25120F large signal model, the evaluation was carried out in co-simulation using momentum structures. The differences in the datasheet stated impedances versus the simulated impedances could be due to several reasons. If the output matching structure of the datasheet is compared to the output structure of the evaluation board , it can be seen that the datasheet output structure is slightly different; it has an additional open stub in the matching network (refer to figure 73 and figure 73 in Appendix A) which would change the impedance seen by the device. The lumped component models may not model all parasitic effects which would also alter the impedances.

Load-pull simulations are an important step to understand the behavior of a large signal model. The optimum impedance of a device can be extracted through non-linear simulations if accurate large signal models are available. Agilent's ADS Load-pull simulations show the performance of the large signal model under different load conditions using harmonic balance (HB) analysis.

Load-pull simulations performed on C ree's CGH25120F large signal model are shown in figure 33 and figure 34. Single tone simulations were performed with fundamental source (Zs) impedance of 4.32-10.9j, drain voltage of 28V and gate voltage of -3.02V to achieve an Idq of 500mA at 2.650GHz. At the given bias point, input power and frequency, output power contours elliptically in a 0.6dB step and power added efficiency in a 5% step.

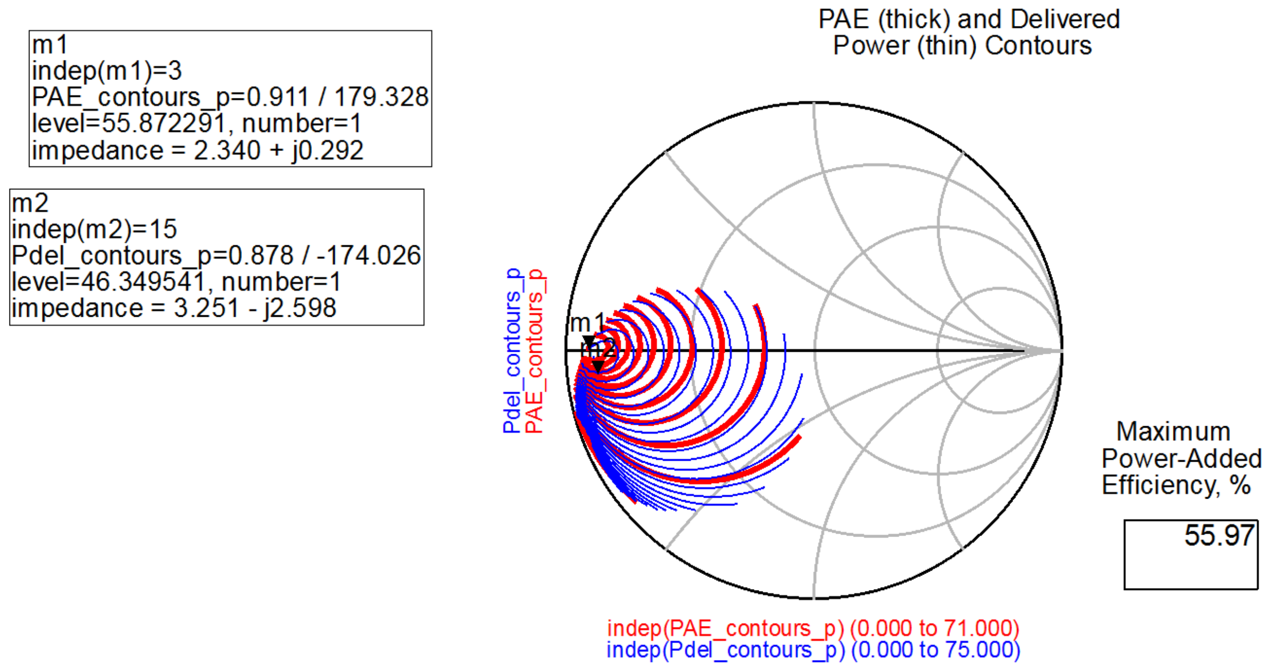


Figure 33: Simulated efficiency and power delivered Load-pull contours at the load impedance from the simulated momentum structures for CGH25120F evaluation board

Figure 33 shows the simulated contour lines for Power added efficiency (PAE) and power delivered to the load (Pdel).Although the highest achievable efficiency for this device is 55.97%, the evaluation board has been designed at an impedance of 3.35-2.87j where the efficiency is around 40% at an output power of 46dBm. This indicates that the impedance has been selected to have a good compromise between linearity and efficiency. This assumption can be further established by observing the IMD3 contours extracted from the two-tone Load-pull simulations. From figure 34 it can be seen that, although the PAE and Pdel contours rotate in the same direction, the IMD3 contours rotate differently. This indicates that a higher efficiency impedance point could yield lower linearity.

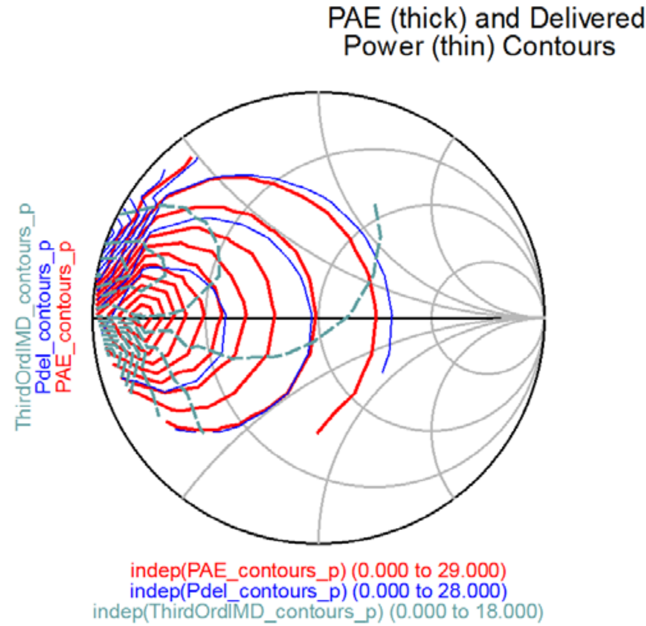


Figure 34: Simulated IMD3, efficiency and power delivered Load-pull contours from the simulated momentum structures for CGH25120F evaluation board

3.3.3 Comparison of Measured and Simulated Performance of CGH25120F

In order to determine the performance of the CGH25120F large signal model, gain, drain efficiency and compression points have been characterized with the measured and simulated test setups. The simple measurement setup for such characterization includes a power meter, signal generator and power supplies as shown in figure 35. The measurement setup has been fully calibrated to accurately determine the large signal performance. An image of the actual setup can be found in appendix C. Table 4 summarizes the simulated and measured data collected at the centre band of 2.65GHz.

Table 4: Measured and simulated performance data of the CGH25120F evaluation board

	P3 dB (dBm)	Gain(dB) at 2.65GHz for Pout of 46dBm	Drain efficiency at 2.65GHz for Pout of 46dBm
Simulated	50.4	14.03	39.9 %
Measured	51.2	13.68	45.03 %

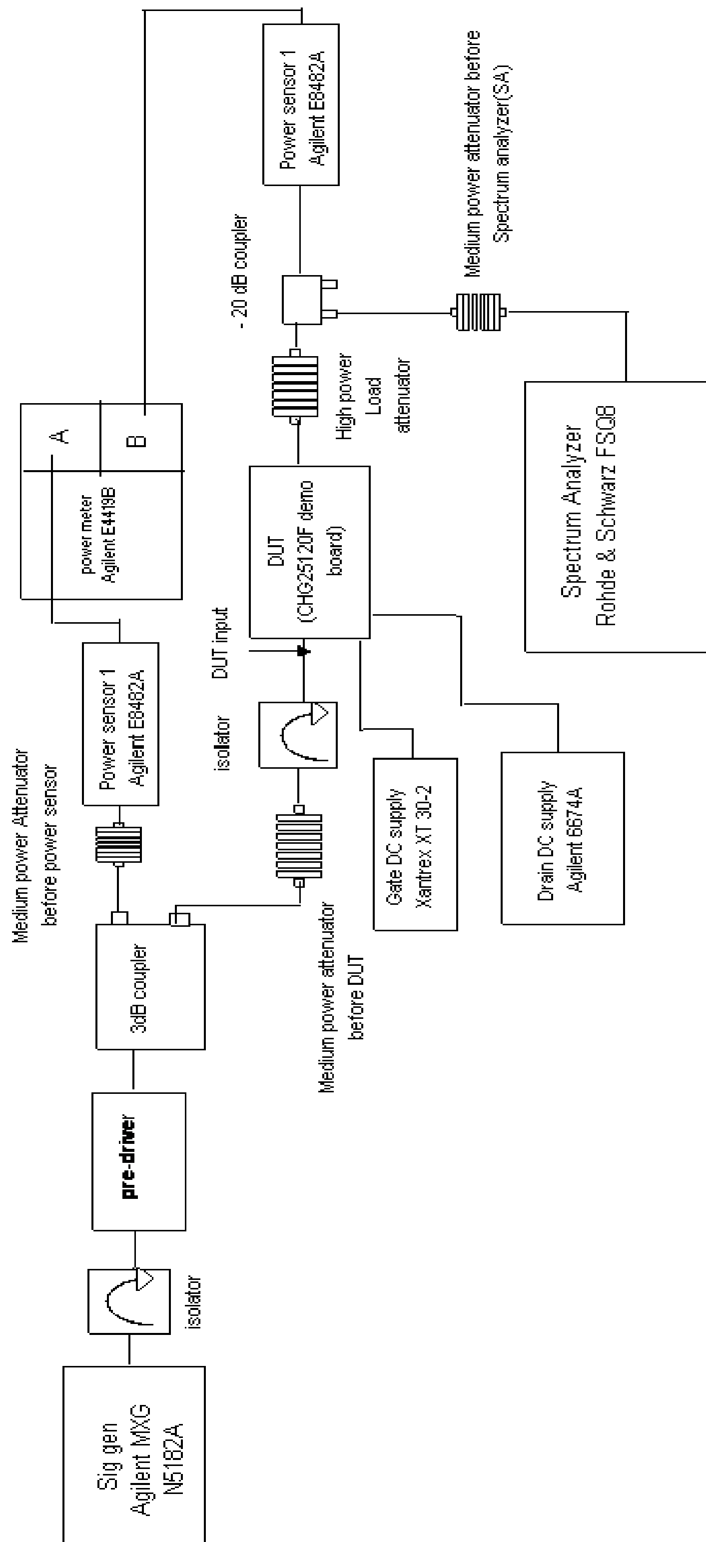


Figure 35: Measurement setup of CGH25120F evaluation board

Analysis of the 3dB compression points and gain suggests that the simulated design provides very close results to the measured results. Figure 36 depicts the compressions points of the simulated and measured CGH25120F design. Measurements were performed with a pulsed CW signal with a 12% duty cycle from the signal generator. Simulated performance has been done using a single tone source. Note that although P1dB is the fundamental metric of estimating linearity of an amplifier, for some devices types with certain characteristics, assessing the P1dB point may not be as apparent. For instance, due to the smooth transition from the linear to the saturation region, GaN amplifiers typically define their output power at the 3dB compression point. This can be clearly seen by the measured data in figure 36. The measured and simulated 3dB compression points for the CGH25120F design only deviate by 0.8 dB. Even though the simulated P3dB point is very close to the measured data, the large signal model does not seem to model the true transition characteristics from the linear to the saturation region of the device. The measured gain data depicted in figure 37 has been done using a 10MHz LTE signal with a 7dB PAR at 0.01% probability on CCDF. As revealed in figure 37, measured and simulated gain differs only by 0.4dB at the band centre (2.65GHz). Although, the simulated gain predicts a flat response for the full band of 2.62-2.69GHz, the measured gain shows a roll off around 0.5dB at the band edges.

Again, the large signal model fails to fully predict the over frequency response of the CGH25120F design. In figure 38, the measured and simulated drain efficiency is shown to be different by approximately 5%, where the measured data shows the higher efficiency of 45%. Overall, the large signal simulations predicted the gain and P3dB performance quite well. Although the simulated efficiency results were 5% less than the actual measurements, the large signal model does give a good indication of the expected measured performance. What the large signal model seem to lack is to accurately predict the over frequency and over power performance of the device. Other factors can also contribute to the difference in the measured over frequency response, that may not be captured in the simulated environment accurately, such as coupling effects, parasitic effects of the lumped elements, SMA connector impacts and so on.

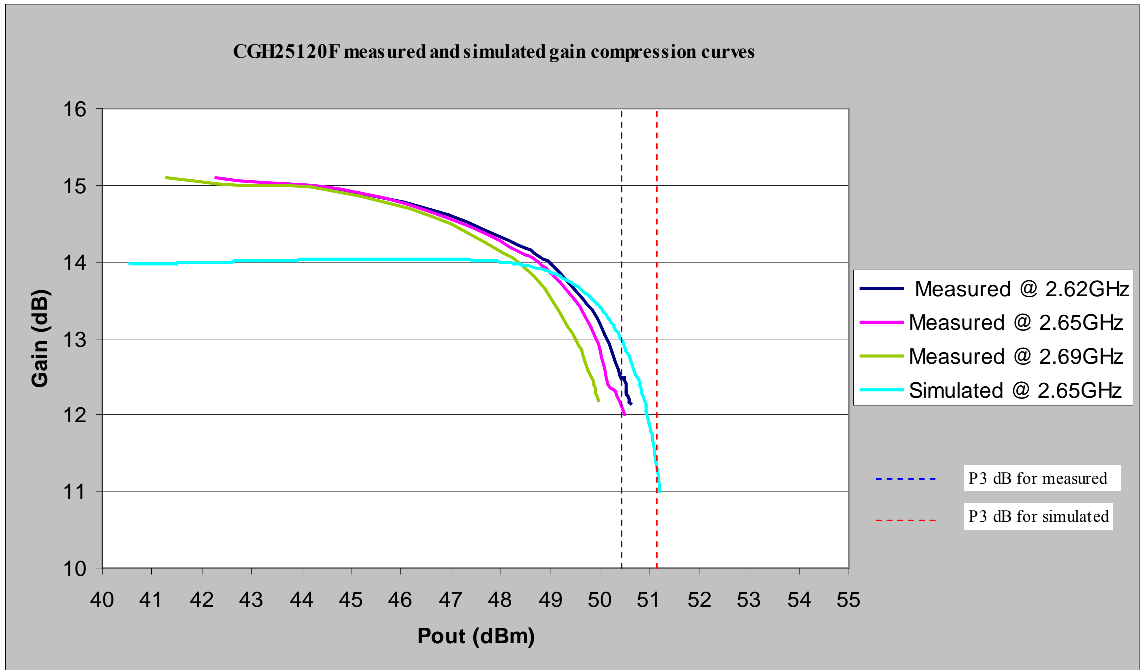


Figure 36: Measured and simulated compression curves for CGH25120F

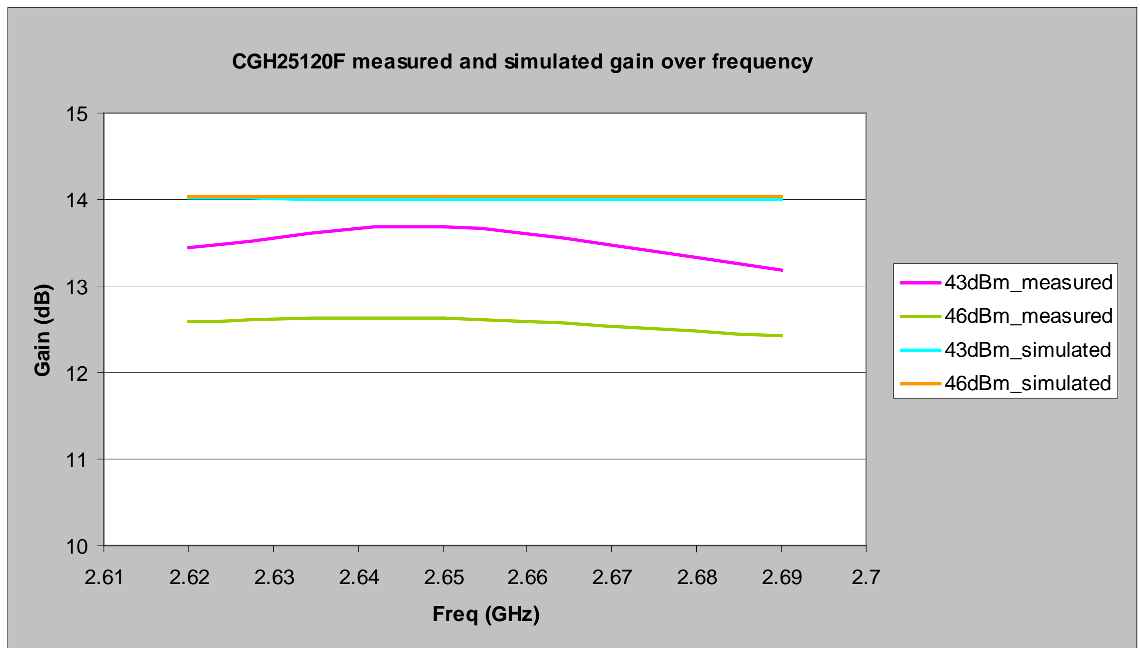


Figure 37: Measured and simulated gain over frequency for CGH25120F

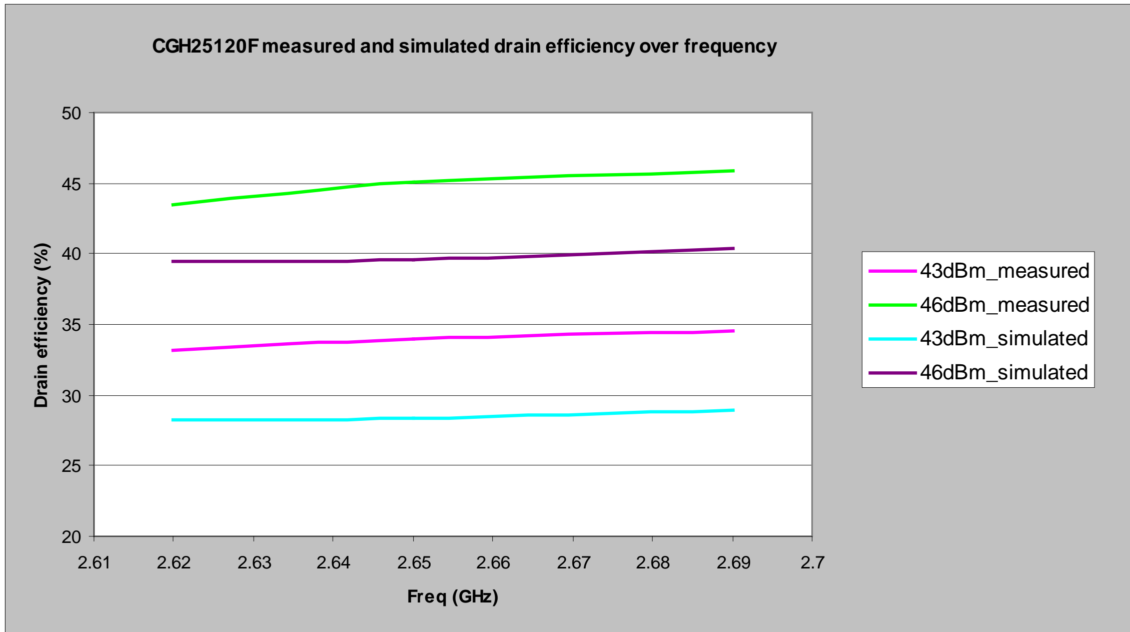


Figure 38: Measured and simulated drain efficiency over frequency for CGH25120F

Chapter 4 Doherty Power Amplifier Design Implementation & Results

4.1 Doherty Amplifier Design for a 5W pico-cell base station

In this section a MMIC design of a Doherty power amplifier in Gallium Nitride (GaN) transistor technology will be provided. This entails a detailed design procedure of a two way symmetrical Doherty amplifier for a 5W base station and its performance evaluation in LTE band 7. A concise summary of the design procedure will be followed by the design, simulation and characterization of the amplifier. It features a link budget analysis along with device characterization, DC simulation, load pull characterization, design and optimization of bias networks and matching circuits. Two 8 x 200µm GaN HFETs will be utilized for each main and peaking amplifiers in Doherty configuration on a 10mm x 11.5mm chip. The design of a Doherty amplifier is an intricate procedure that involves the design of several sub circuits such as the main and peaking amplifiers, power combiner and divider networks. This section will present the design of each sub circuit in detail and finally an analysis of the final Doherty amplifier performance. Section 4.1.9 will present a discussion on the layout design of the two-way Doherty amplifier. Results of the designed PA will be provided in section 4.2.

4.1.1 Design Specifications for LTE

The foremost step in designing a power amplifier is to specify the system requirements. Since the goal of this thesis is to realize a Doherty power amplifier for LTE applications, the specifications would be based on s tandards developed by the third generation partnership project (3GPP).

LTE was introduced in 3GPP Rel8. Its radio access is referred to as Evolved UMTS terrestrial radio access network (E-UTRAN). LTE can use QPSK, 16QAM or 64QAM modulation schemes, and can be either frequency division duplex (FDD) or time division duplex (TDD).

It can support up-to six different channel bandwidths of 1.4MHz, 3MHz, 5MHz, 10MHz, 15MHz, and 20MHz, which provides more deployment flexibility than previous systems. According to 3GPP specifications, LTE can provide more than 100Mbps of maximum down-link speed [6]. Although the traditional pico-cell base station output powers typically range from around 200mW-1W [79], recently developed pico-cell base stations announced by vendors such as Nokia Siemens Networks and Huawei are fairly large devices, with transmit powers of 2 X 5W (2 X 37dBm)[84]. Hence, this project will focus on a power amplifier design that is suitable for a pico-cell base station with an output power of 5W.

Another important design parameter is the crest factor or the peak to average power ratio of the signal (PAPR). The PAPR depends on the number of data channels being used. Therefore higher data rates results in very high peak to average ratios. LTE offers variable data rates of more than 100Mbps which result in large peak to average ratios of 6dB and higher at 0.01 clipping probability [80].

ACLR is another important design specification. There are two ACLR measurements in LTE, E-UTRA ACLR and UTRA ACLR. E-UTRA uses LTE to LTE adjacent signal, and UTRA ACLR uses LTE to WCDMA adjacent signal. The frequently used the limit for UTRA ACLR is -36dBc and -33dBc for E-UTRA ACLR [81]. Often base station power amplifier ACLR is measured on a system with a linearization technique such as digital pre-distortion, where typical minimum correction is around 25dB. Hence, if the intent is to use the PA design with a linearization technique such as digital pre-distortion, less emphasis can be placed on linearity during the design of the PA and trade-offs can be made to place more emphasis on efficiency or gain. Design requirements for the pico-cell baste station power amplifier designed in this project can be summarized in Table 5.

Table 5: Design requirements

Parameter	Design specifications
Operating Frequency (LTE Downlink operating band 7) [6]	2.62-2.69GHz
Base station average output power (Pout)	5W
Power Amplifier average output power (PA Pout)*	40dBm
Gain at PA output	>10dB
Average power added efficiency (PAE)	>35%

* Refer to section 4.1.3 for detailed calculations

4.1.2 Design procedure

Following design procedure was followed to realize the Doherty amplifier:

1. Determine the GaN HFET sizing (number of FETs, number of fingers, unity gate width) to achieve the power required
2. Determine the bias point for the main and peaking amplifier to achieve the desired operation in Doherty topology.
3. Design DC bias circuit.
4. Set the selected input impedance as the source impedance and load pull the device. From the contours, determine output impedances required for low and high power regions of operation. The load seen from the main amplifier at the low power region when the peaking amplifier is still off should ensure maximum efficiency at a saturated output power 3dB less than the maximum PA output power as per Doherty operation discussed in chapter 2. The second main amplifier load for the high power region should ideally assure maximum output power with roughly the same efficiency.
5. Once the desired loads have been found, design the output matching networks
6. Design input matching networks.
7. Design the Doherty combiner. Doherty output combiner consists of a quarter- wave transmission line with the characteristic impedance of R_{opt} and a quarter-wave transmission line that transforms from $R_{opt}/2$ to 50 Ohm, which is the required system output impedance.
8. Complete Doherty PA design
    a. Utilizing the designed input/output matching structures, combine the Class AB and Class C biased amps with the Doherty combiner.
    b. Adjust the main and peaking amplifier offset lines to optimize the performance. Due to die and package parasitics and external matching circuits, the required 2 R_{opt} interface at the main amplifier device plain in the low power regime may not necessarily result in a purely resistive translation at the load line, therefore phase compensation will typically be required to rotate the load line impedance back to the real axis for the desired resistive load. Same applies for the peaking amplifier, which would also require an offset line. Note

that the offset lines will not affect the overall matching condition and load modulation because they are matched to the characteristic impedance of 50 Ohm.

9. Verify out power, efficiency gain and other requirements of complete power amplifier over frequency once layout components are realized in the design. Figure 39 below summarizes the sub blocks required for the Doherty design procedure discussed above.

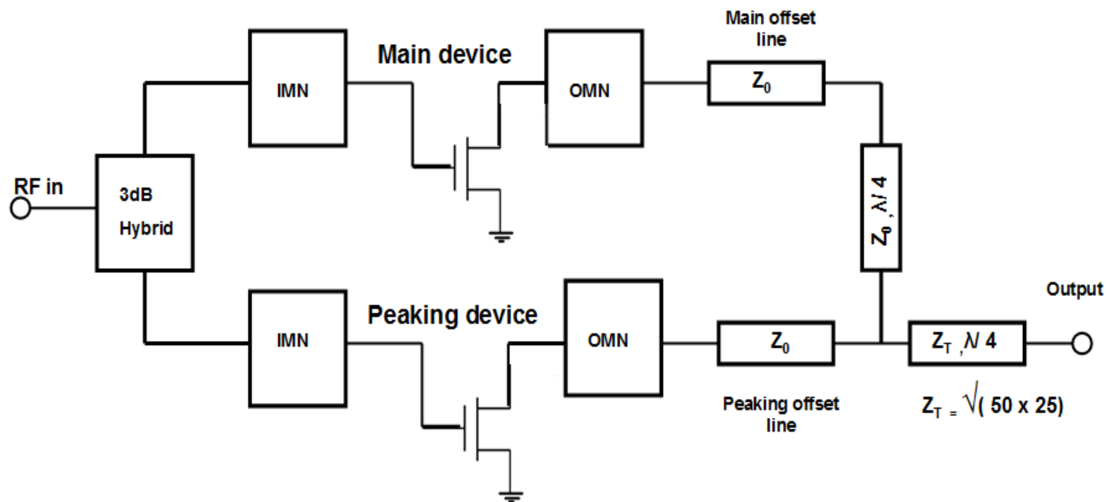


Figure 39: Doherty Amplifier design blocks

4.1.3 Device Sizing

The required FET size (number of fingers x gate width) is dependent on the required power amplifier output power, peak-to-average power ratio (PAPR) of the signal and the power density of the device. The peak to average ratio depends on the number of data channels being used in a specific standard. LTE offers variable data rates which would result in peak to average ratios of 6dB and higher .Therefore 6dB PAPR was selected to the estimate the requirements for this project. Following calculations were performed to assess the device size. Primary step is to assess the losses between the power amplifier and the base station antenna to calculate the required output power from the Doherty amplifier. Typical worst case back end losses at 2.6GHz would include microstrip losses (0.1dB) + directional coupler (used to couple the output signal for linearization) insertion loss (0.3dB) + output circulator insertion

loss (0.3dB) + output connector loss (0.2dB) + duplexor filter insertion loss (2.1dB), which would total to around 3.0 dB of losses. Hence to have an output power of 5W (37dBm) at the pico-cell base station, the power amplifier average output power needs to be 37dBm + 3.0dB = 40 dBm. Therefore the assumed average PA output power (Pavg) = 40 dBm and PAPR = 6dB. Typically amplifier devices are sized such that P1dB (dB) = Pavg + PAR = 40 + 6dBm = 46dBm (40W). Therefore the total required device size would be 40W.

In a two way Doherty configuration each device size would be 40W /2 = 20W per main/peaking amplifier. The Device power density can be calculated using the following:

$$\text{Device power density} = \frac{V_{breakdown}}{2\sqrt{2}} \times \frac{I_{dss}}{2\sqrt{2}} \qquad (4.22)$$

From the I-V curves of the GaN MMIC design foundry manual [78]: $V_{breakdown}$ = 100 V, I_{dss} = 0.55A. Applying this to equation (4.22), would give a device power density of 6.875 W/mm. Since the devices would be operating at a lower current than Idss, 6.5W/mm was used for the estimation.

The required gate width would be = 20W / 6.5W = 3.08 mm

The largest gate fingers available in foundry = 8 x 200µm = 1.6 mm

Therefore the minimum number of 8 x 200µm cells required = 3.08 mm / 1.6mm = 1.92. Thus, two 8 x 200µm cells per main and peaking amplifier were used. All simulations will be performed using the ADS GaN MMIC design foundry provided by NRC.

4.1.4 DC analysis

The Doherty configuration requires two different biasing for the main and peaking stages .Both main and peaking amplifiers are designed to deliver maximum power with optimum efficiency at a specified load. Analysis of different classes of power amplifier shows that the required performance of the main amplifier can be very closely achieved by biasing the transistor in Class AB or B mode of operation. The peak amplifier is made active only during the peaks of the input signal and hence is designed to only amplify signals that cross a minimum threshold. This is achieved by biasing the device below its pinch-off voltage for operation similar to class C. For this project, the main amplifier was chosen to be biased in class AB and the peaking in class C. The transfer characteristics and IV curves of the GaN HFET under consideration is shown in figure 40 and figure 41 below.

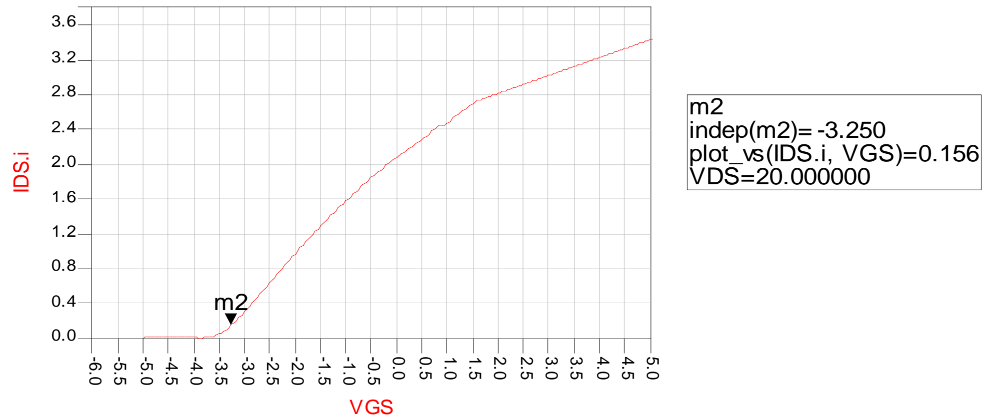


Figure 40: Transfer characteristic for two 8 x 200µm HFETs at 20V drain voltage

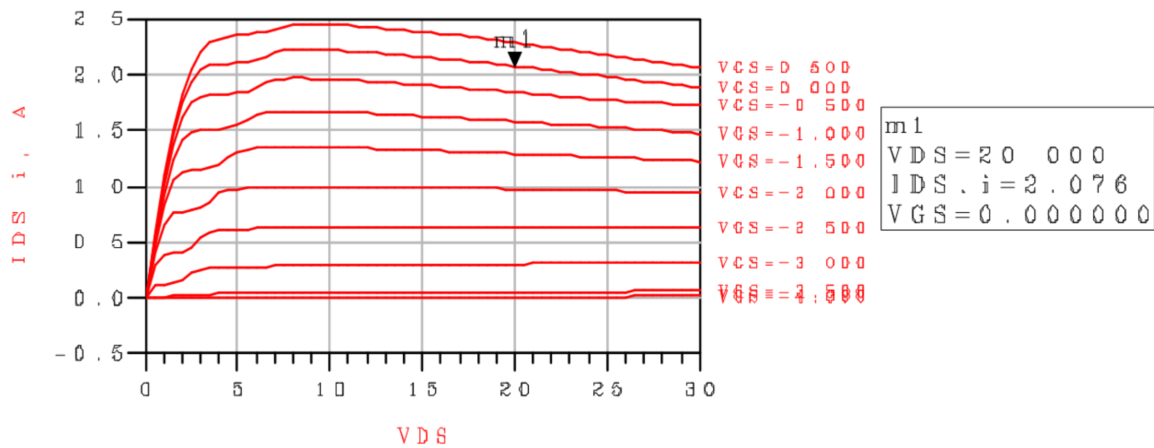


Figure 41: I-V curves for two 8 x 200µm HFETs

The operating points of the device corresponding to the different classes of operation can be easily judged from the transfer characteristics .The IV curves and the transfer characteristics of the two 8 x 200µm GaN HFETs show that Vgs = -3.0V achieves Ids of approximately 0.303mA (~15% Idss) at Vds =20V for class AB operation of the main amp. Pinch-off voltage seems to occur around Vgs = -3.8V. Therefore for class C operation, the peaking amp would need to be biased below Vgs = -3.8 V at Vds =20V. The plot represents the range of gate voltages and the corresponding mode of operation. Table 6 summarizes the biasing for the main and peaking stages.

Table 6: Main and peaking amplifier gate bias voltages for class AB and class C operation

Class of operation	**Drain Voltage**	**Gate Voltage**
AB (main amp)	20V	-3.0V
C (peaking amp)	20V	Less than -3.8V

4.1.5 Main and peaking amplifier design

As any standard power amplifier design, matching networks at the input and the output are required to transform the input and output impedances of the device to a desired standard real load impedance .Therefore, to start with, the optimum input and output impedance of the device needs to be determined. For a standard symmetrical two-way Doherty design, the main and peaking amplifiers would have the same matching network designs.

4.1.5.1 Optimum load selection

Load pull simulations provide a means to determine the optimum complex impedance that needs to be seen by a device to achieve a certain performance. Impedances acquired from load pull will assure the compensation of the device output reactance, since other calculated estimations of optimum impedances would not account for the parasitics of the device.
Note that the source impedance was set to the conjugate of the impedance looking into the device input. According to simulation results of the load pull analysis presented in Figure 42 and 43, the load impedance that would enable the transistor to operate at maximum output power and efficiency is 21.6+3.7j. This selected impedance would be the impedance seen by the main amplifier at the high power region of operation.

4.1.5.2 Main and Peak amplifier matching network design and verification

The input matching network of the main amplifier has been designed to fulfill the complex conjugate matching conditions. The simulated input impedance was 1.36 - 4.0j. The imaginary part of this input impedance at the desired frequency needs to be cancelled. This ensures that the source is resistive and the entire input signal at the fundamental frequency is converted into real power.

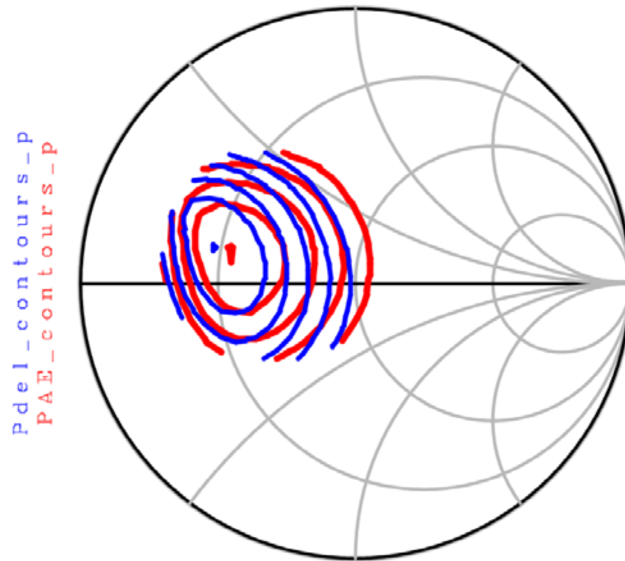


Figure 42: Power added efficiency and power delivered contours with Vds=20V and Vgs=-3.0V

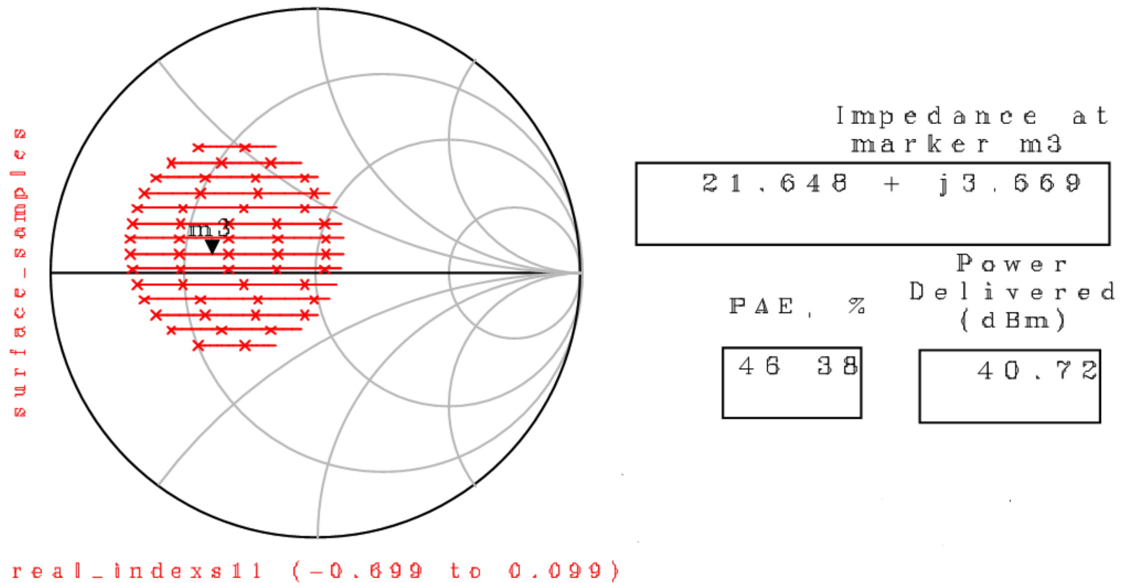


Figure 43: Simulated load impedances with Vds=20V and Vgs=-3.0V

The simplest way to cancel the imaginary part is to create a series inductor to negate the reactance of the series capacitance. Hence, the input was matched with a series inductor of 0.243nH in order to make the output impedance real. This will also facilitate the impedance

transformation with the quarter wave line. The characteristic impedance of the input quarter wave line was calculated to be 8.3Ω. With the substrate parameters defined in the Gallium Nitride MMIC Foundry Design Manual used in this project [78], the required width and length of the quaterwave transformer would be W = 5079.6 µm, L = 9730.9 µm.

Since this large W and L would take up too much layout area, the equivalent circuit of the quarter wavelength line was calculated using basic microwave theory as follows:

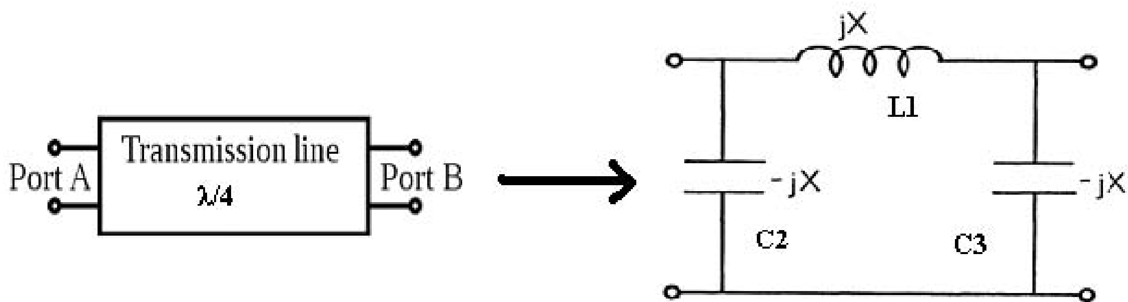


Figure 44: Quarter wave transmission line equivalent model

where $L = Z_0 / (2\Pi f)$ and $C = 1/ Z_0 (2\Pi f)$ .By using Z_0= 8.3 Ω and f= 2.655GHz we obtain: L1 = 0.496nH and C2 and C3 = 7.23pF. The complete input matching network with ideal components is presented in figure 45 below:

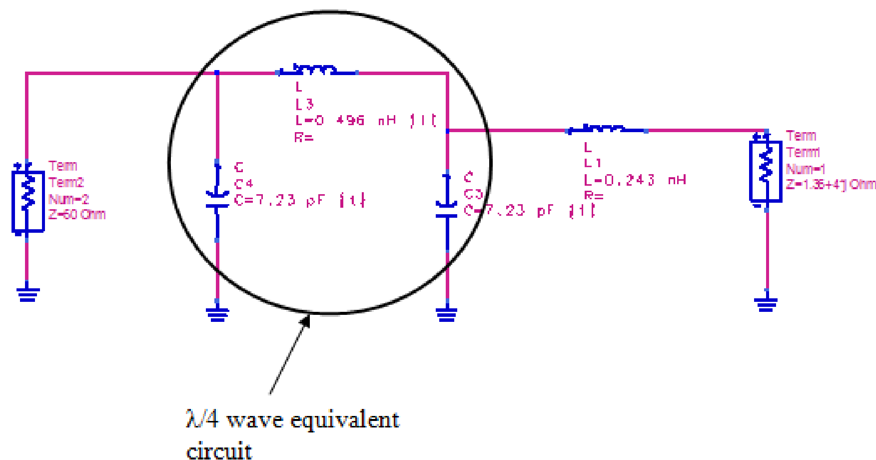


Figure 45: Input matching network with ideal components

The results of the load pull analysis from section 4.1.5.1 show that the device needs to see an output impedance of 21.6+3.7j for its optimum high power performance. Several options were available to achieve this match from the output load impedance of Z_{out} to 50Ω, but taking layout area constraints in to consideration, a lumped element match was the selected as the optimum match. ADS's Smith tool was used to calculate the required shunt inductance and series capacitance. The match presented in figure 46 below, sits well within a Q=1 circle to ensure a low Q match to maximize the bandwidth.

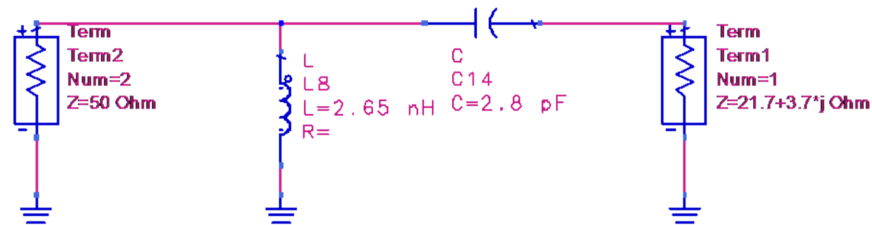


Figure 46: Output matching network with ideal components

In order to verify the selected impedance points for the main peaking amplifiers, the HFET was operated in class AB mode and class C mode with GaN foundry elements in ADS. Initially ideal components were used to realize the matching .Secondly the components were replaced by foundry elements and tuned to achieve the optimum performance. Figure 47 shows the input and output matching networks with GaN foundry schematic elements.

The simulated main amplifier performance characterization with foundry schematic elements is shown in figure 48 below. The main amplifier has a saturated output power approximately 6dB below the estimated peak power as required in a Doherty operation.

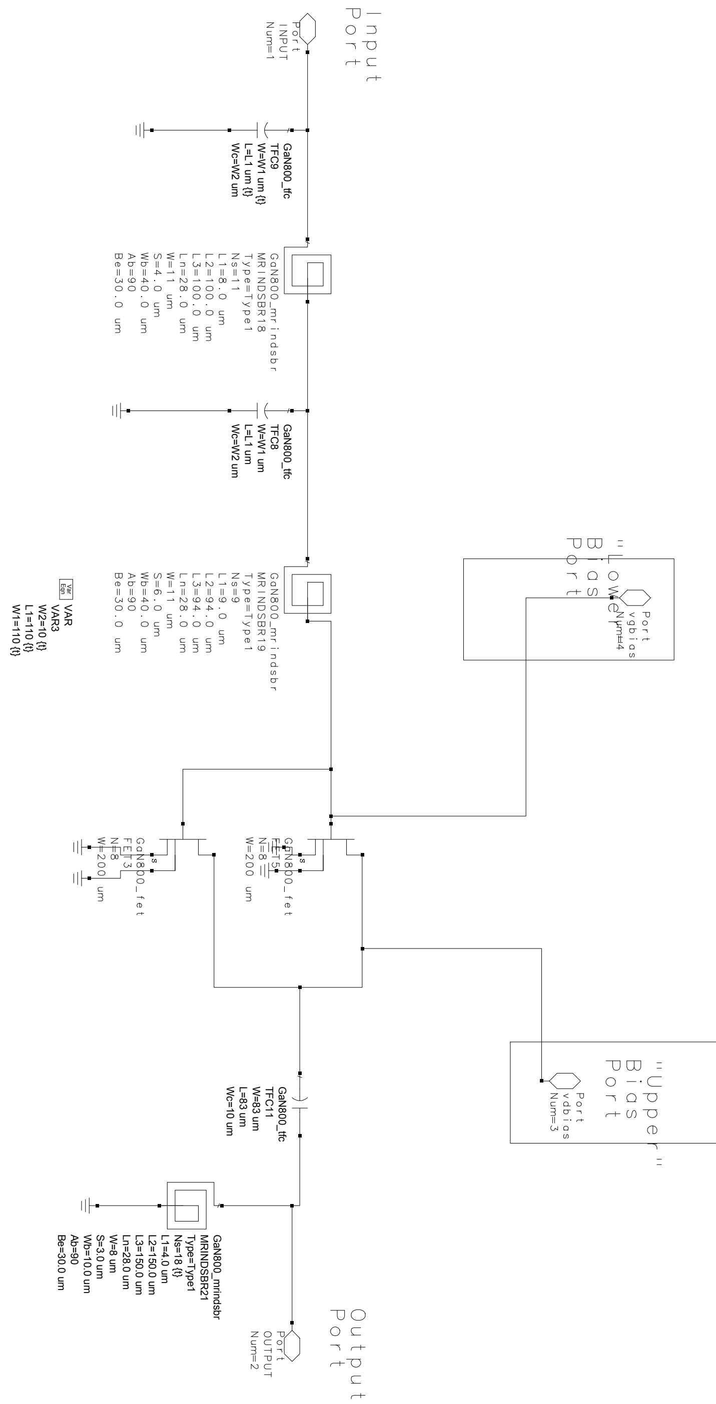
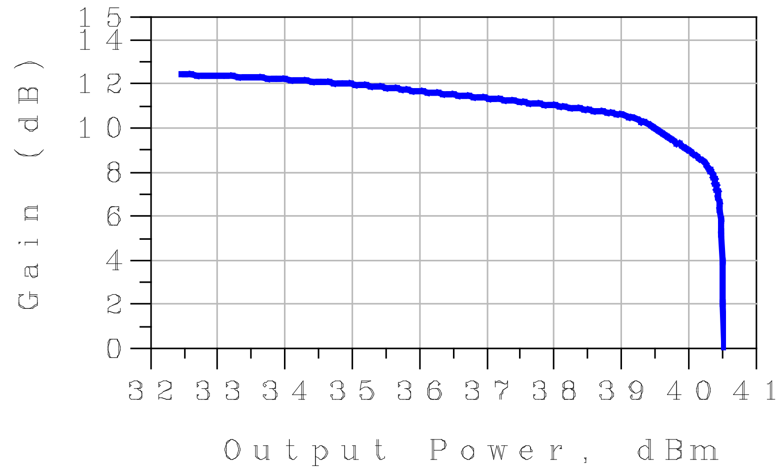
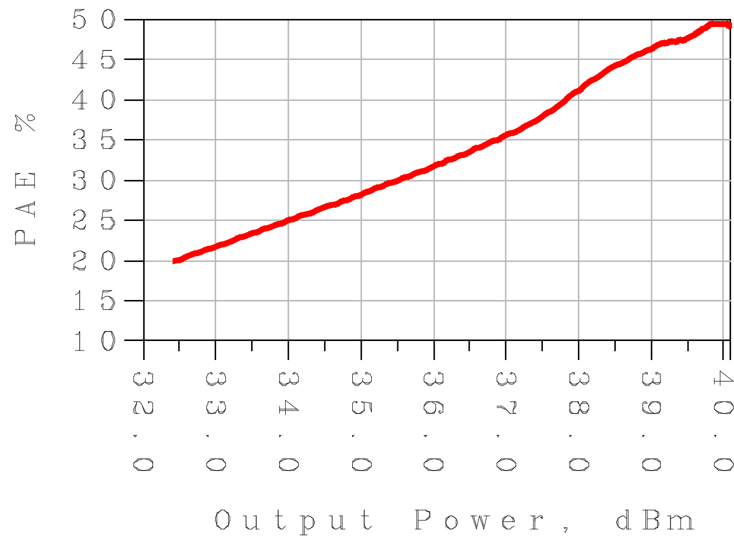


Figure 47: Input and output matching networks with foundry schematic elements



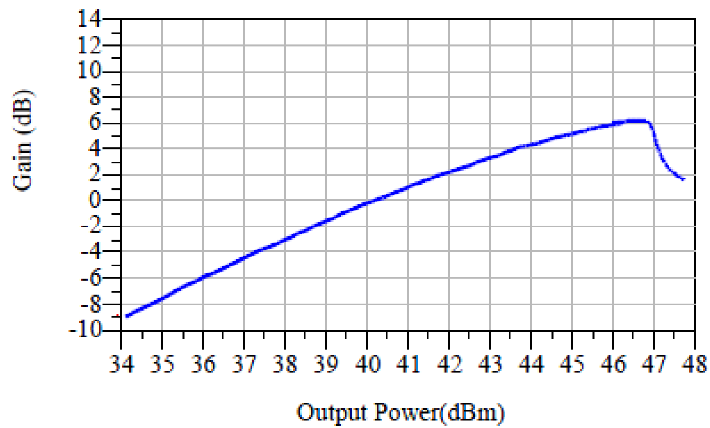
(a)



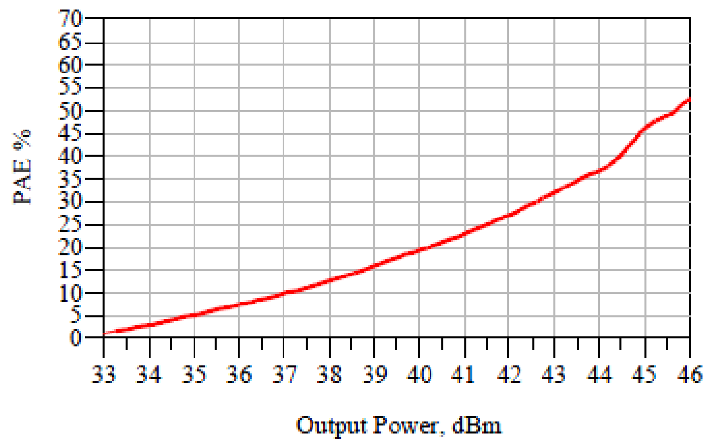
(b)

Figure 48: Main amplifier single-tone simulations at Vdd =20V, Vgs= -3.0V, (a) Output power Vs gain, (b) Output power Vs Power added efficiency

The peaking amplifier is designed to operate to reach the device maximum output current for a class C operation. For a symmetrical 2-way Doherty design, the peaking amplifier would utilize the same output and input matching networks. The key point is to select the suitable bias point to ensure proper turn on conditions. Hence the peaking amplifier bias is set so that it enters its active region at the 6dB back-off with respect to the total Doherty maximum output power. The peaking amplifier simulated performance is shown in figure 49.



(a)



(b)

Figure 49: Peak amplifier single-tone simulations at Vdd =20V, Vgs= -4.9V, (a) Output power Vs gain, (b) Output power Vs Power added efficiency

Looking at the gain and efficiency of the amplifier under class C bias conditions, it can be seen that the peaking amplifier has around 51% power added efficiency (PAE) at 46 dBm output power. It is interesting to note the expected non-linear gain of class C operation properly being predicted by the GaN model. It is also important to note from the gain plot, that the peaking amplifier turns on (non-zero gain) around 6dB backed off from the peak output power .This ensures that the peaking amplifier will turn on at the expected level when working with the main amplifier.

4.1.6 Bias network design

Like in any PA design, the DC biasing circuitry had to be properly designed to isolate the DC signal from the RF signal through the use of RF chokes and blocking capacitors. The RF chokes are designed to have high impedance only over the vicinity of the design frequency. Several options were considered for the bias networks for this project:

4.1.6.1 Quarter wave feed with a shunt RF resonant capacitor

The goal of this circuitry is to isolate RF signals from DC that is sent to the transistor from a power supply for biasing. In any RF design, capacitors act as RF bypass or DC block filters. A DC block is a series capacitor that has low reactance for the RF frequency of interest (an RF short), but blocks DC because it is an open circuit at zero hertz. A RF bypass is a shunt element that acts like a short circuit to microwave signals .Therefore, in a gate/drain biasing network ,there could be a configuration of a quarter wave transmission line and a shunt RF resonant (at the fundamental operating frequency) capacitor at the end of it. This RF cap would present an open circuit at RF frequency to isolate RF from DC. With a quarter wave length transmission line, if started with an open circuit, one quarter wavelength away it will see a short circuit. If it started from a short circuit, one quarter wave away it will have an open circuit. The quarter wave length concept can also be implemented such that dual bias feeds of half of quarter wave lengths ($\lambda/8$) are used on either side of the drain or the gate. For this project this type of bias network was selected for the device drain side. The characteristic impedance of the bias feed for this project was selected to be 100Ω, which would result in a line length of 5825um for $\lambda/8$. A 27pF was be utilized as a resonant capacitor. Additional de-coupling capacitors could also be added to the bias network to present low impedance at baseband frequencies to minimize memory effects of the amplifier. The baseband capacitors tend to be in the order of 10uF, 100nF, 10nF. These should not have an impact on the match-ing structures in RF frequencies.

4.1.6.2 Quarter wave feed with a radial stub

One of the limitations of the bias network described in 4.1.6.1 is the RF bandwidth limitation due to the parasitic effects of the shunt resonant capacitor. To resolve this problem a radial stub can be used to provide the RF short instead of the resonant capacitor. Radial stubs would serve the same purpose as the previous option but with an added advantage: they provide better bandwidth. The length and angle of the radial stub can be calculated as follows:

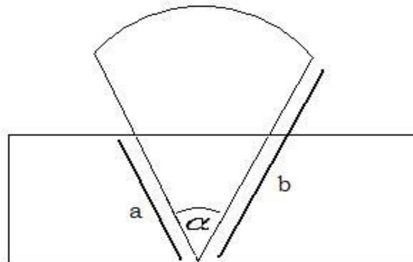


Figure 50: Radian stub

In order for a radial stub to work well, α needs to be $90 < \alpha < 120$ and the radius b-a = λ/6. If α = 90, using the Pythagoras theorem the length "a" can be calculated as follows:

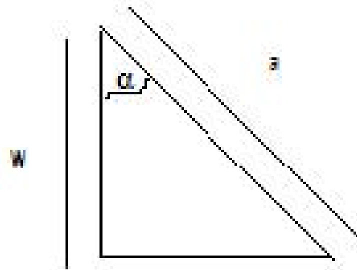


Figure 51: Radial stub section

The height W is the width of the microstrip which is calculated to be 390 um for a 50 Ω line with the substrate definitions in [78].

$$\therefore a = \frac{W}{\cos\alpha} = \frac{390\mu m}{\cos 45} = 685.3\mu m$$

With the following:

$$b-a=\frac{\lambda}{6}\ , \qquad \lambda=\frac{c}{f}=\frac{3\times10^{8}}{2.655GHz}$$

The calculated radius “b” would need to be around 19.7mm. The main disadvantage of the radial stubs is the circuit size. For this project as seen above, at the fundamental operating frequency the radial stubs proved to be too large to be implemented.

4.1.6.3 Lumped element bias network

The drain and gate bias networks could also be replaced by a lumped element network. Typically an inductor, with high impedance at the fundamental frequency would be used in series with a resistor that would be used to ensure stability on the gate side of the device. The series resistor would be placed as close as possible to the date to ensure stability of the device. An approximate value of resistance can be estimated by 400/Psat [19], where Psat is the saturated power of the device. With the requirements of this project, the resistance would be 32Ω and inductance would be 33nH.
The intent was to use lumped circuits for the gate bias network, employing large inductors and resistors, while a semi-lumped structure with a λ/8 line and a resonant capacitor was intended for the drain bias networks. Yet, the final implementation was done using the semi-lumped structure with a λ/8 line and a resonant capacitor for both drain and gate bias networks.

4.1.7 Doherty Combiner design

As shown in figure 52 below, the Doherty combiner consists of two quarter wave lines. The first λ/4 wave line with $Z_0 = 50Ω$ is required for load modulation. The second λ/4 wave is required to combine the main and peaking amplifier and to transform $Z_0/2$ to the desired system impedance of 50Ω.

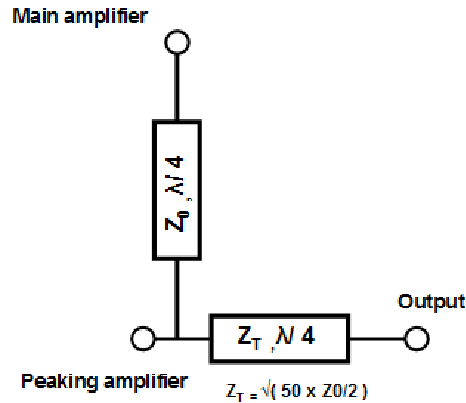


Figure 52: Doherty Output combiner

The characteristic impedance of the transformer Z_T has been calculated as $Z_T = \sqrt{(Z_{load} \times Z_0/2)} = \sqrt{(50 \times 25)} = 35.35\ \Omega$. The initial design has been implemented using ideal transmission lines, which was later replaced with meandered transmission lines, which will be discussed in section 4.1.9.

4.1.8 Implementation

With all sub circuits in place, the complete Doherty design can now be assembled as parallel blocks. Identical GaN HFETs are used as main and peaking amplifiers with both output matched to 50 Ω to have a load impedance of 21.6+3.7j. A 50 Ω quarter wave line is utilized for load modulation and a 35.35 Ω quarter wave line is used to transform the impedance at the combiner node to the required system impedance of 50 Ω. The input signal is split into two quadrature components having a 90 degrees phase difference by the hybrid divider. The split input signals are applied to two stages, the main and peaking, which are identical except for their gate bias levels. The main is connected to the in-phase port of the hybrid with 0 degrees output and the peaking is connected to the quadrature port of the hybrid with 90 degrees output. This compensates for the phase mismatch caused by the quarter-wave line at the output of the main stage used for load modulation.

Additional offset lines were added at the output of both the main and peaking amplifier after the output matching networks to optimize Doherty performance. The reason for this is, due to die and package parasitics and external matching circuits; the required $2R_{opt}$ interface at the

main amplifier device plain in the low power regime may not necessarily result in a purely resistive translation at the load line. Therefore phase compensation will typically be required to rotate the load line impedance back to the real axis for the desired resistive load. The peaking amplifier would also require an offset line. Typically the transistors suited for the peaking stage of the Doherty power amplifiers have large shunt and feedback capacitances, which render strongly to reactive output impedances with low resistance. Therefore at the low power regime the peaking amplifier would not be a perfect open at the transition point which will cause improper load modulation. This causes power leakage from the main amplifier to the peaking amplifier which degrades the efficiency performance. The complex output impedance of the peaking stage due to the parasitic feedback and shunt capacitance makes pure resistive load modulation harder to achieve. Therefore offset lines for the peaking amplifiers are required in order to transform its output impedance closer to an open circuit. Note that the offset lines will not affect the overall matching condition and load modulation because they are matched to the characteristic impedance of 50 Ohm.

The following procedure was used to tune the offset lines for the main and peaking amplifiers:

1. Disable the peaking amp and adjust the length of the delay transmission line at the output until 2xRopt impedance is purely real as seen by the main amp at the input of the quarter wave transformer.
2. Disable the peaking amp and tune the delay at the input to maximize the efficiency of the main amp. This effectively removes the imaginary component of the load line at the die reference plane and establishes the correct slope.
3. Bias the peaking amp in class AB and adjust the output delay line so the main amp and the peaking amp load impedances are purely real.
4. Decrease the peaking amp gate bias until the Doherty amp performs as desired.
5. Figure 53 shows the schematic diagram of the complete Doherty amplifier with the parallel combination of main and peaking amplifier blocks with all sub circuits.

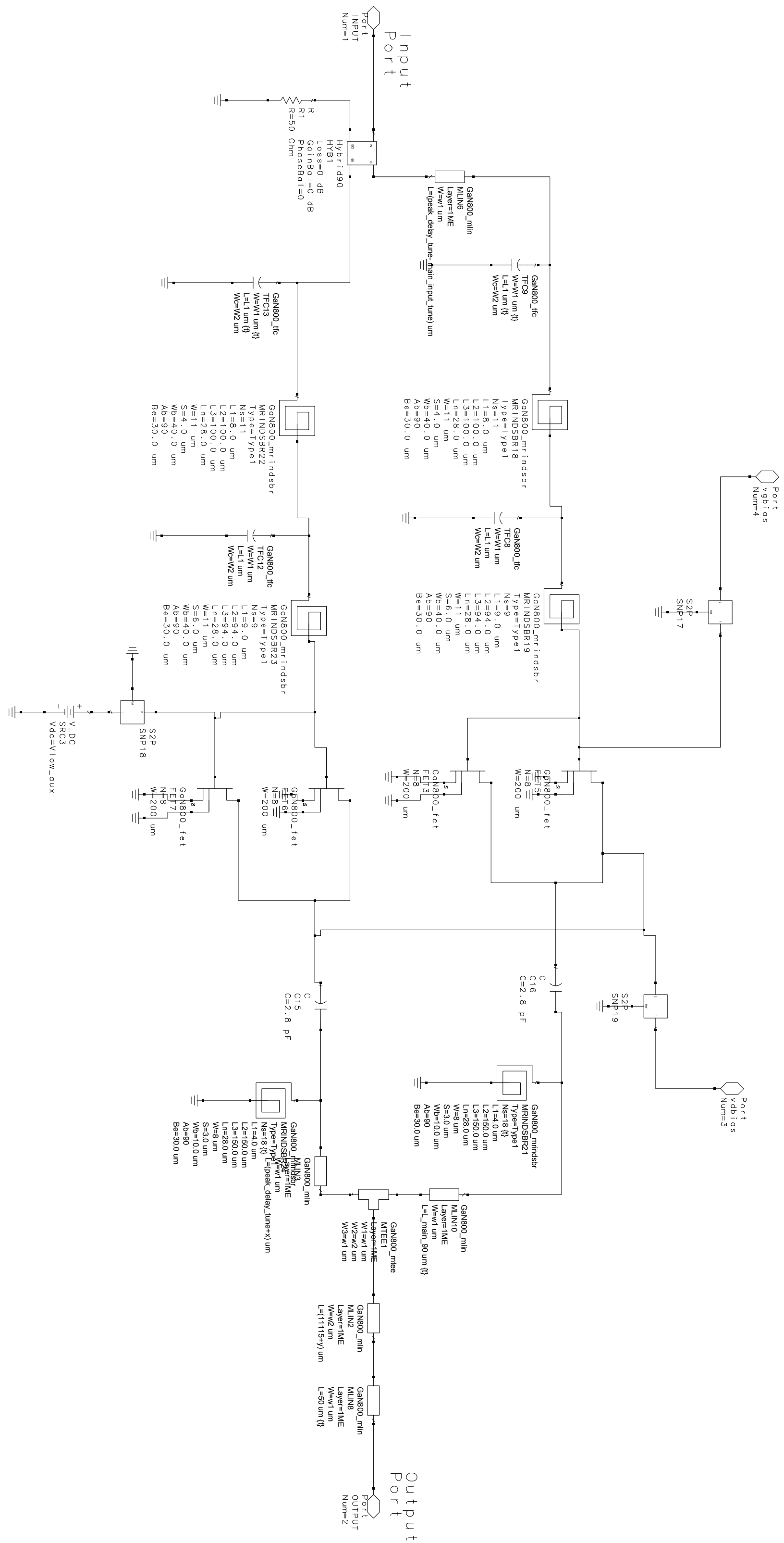


Figure 53: Schematic of the Doherty power amplifier

4.1.9 Layout design

The layout aspect of the design comprises the conversion of the schematic design into something that is able to be fabricated by the foundry. Due to coupling and parasitic effects that is not accurately modeled in the schematic, the both lumped and distributed elements had to be tuned in the layout design. The approach for the layout is to perform EM simulations and adjustments after each individual addition to the layout. This will allow more control over the coupling effects and will increase the likelihood of the layout yielding results close to the fabricated design.

4.1.9.1 Passive Components

This section would discuss the passive components implemented in the layout design of the Doherty PA. At LTE band 7 frequencies, the design kit passives are all within their self-resonance frequency. Therefore MIM capacitors and spiral inductors provided in the design kit were used.

Capacitors

The capacitors required for this project are implemented using Metal-insulator-metal (MIM) capacitors. A MIM structure is used to fabricate capacitors in a two-metal-layer process. The MIM capacitors used in this project are formed by layer 2Me on top of layer1Me. A thin layer of silicon nitride is used as the dielectric layer. The capacitance of the MIM structure is 0.58 fF/sq.µm. The connection to the top plate is by Air Bridge. The top plate of the capacitors in the design kit is limited to 150µm x 150µm. This limits the maximum capacitance to 13.5pF. The figure 54 below shows the layout of the input matching capacitor.

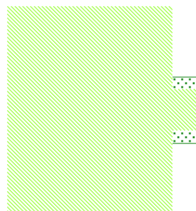


Figure 54: MIM capacitor layout

Inductors

The inductors required for this project are implemented using Spiral inductors provided in the GaN design kit. Inductors are wound round a central empty area, with a recommended minimum size of 50x50µm. Various inductor parameters such as the line width, line spacing, inner dimension and number of turns for each were altered to achieve the required inductance. Note that a smaller inner dimension resulted in a higher self-resonance, larger line width and line spacing resulted in a higher Q and increased number of turns decreased the maximum useful operating frequency of the inductor. The figure 55 below shows the layout of an inductor from the output matching network.

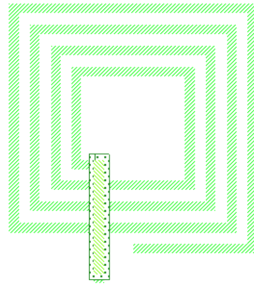


Figure 55: Spiral inductor layout

4.1.9.2 Bonding Pads

The bonding pads provide an interface between the IC and the external circuit. Two types of bond pads were used in this project. One type is for RF connections and the other is for DC connections. For the first type of bond pad, the characteristic impedance plays an important role. They are designed to be 50 Ω from the probing location all the way to the transmission line. The pitch between the pads is 250 µm to ensure proper probing. The bond pads used for DC interconnections are much simpler since the characteristic impedance would not be of relevance. The only design criteria would be to make them dense to conserve layout form factor. Figure 57 below shows the DC supply bond pads used in the design. The pitch between the pads is 150 µm to ensure proper probing.

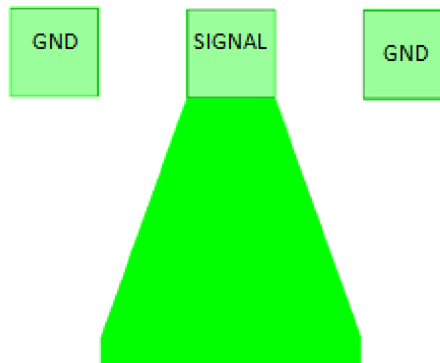


Figure 56: RF bond pads

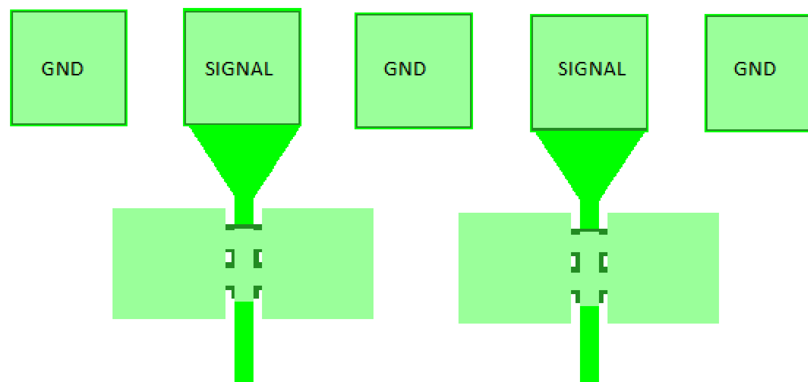


Figure 57: DC bond pads

4.1.9.3 Bias circuit

In section 4.1.6 the type of bias circuits considered and the selected bias circuit design was discussed. The selected gate and drain bias circuit design was a quarter wave transmission line with a capacitor that is self-resonant at the band center frequency. The figure 58 below shows the biasing circuit employed in the layout .Although the initial plan was to employ a different bias circuit for the gate side with a resistor to enhance stability to minimize the possibility of oscillations, due to time limitations, the same bias circuit design was employed at the gate and drain for both main and peak amplifiers.

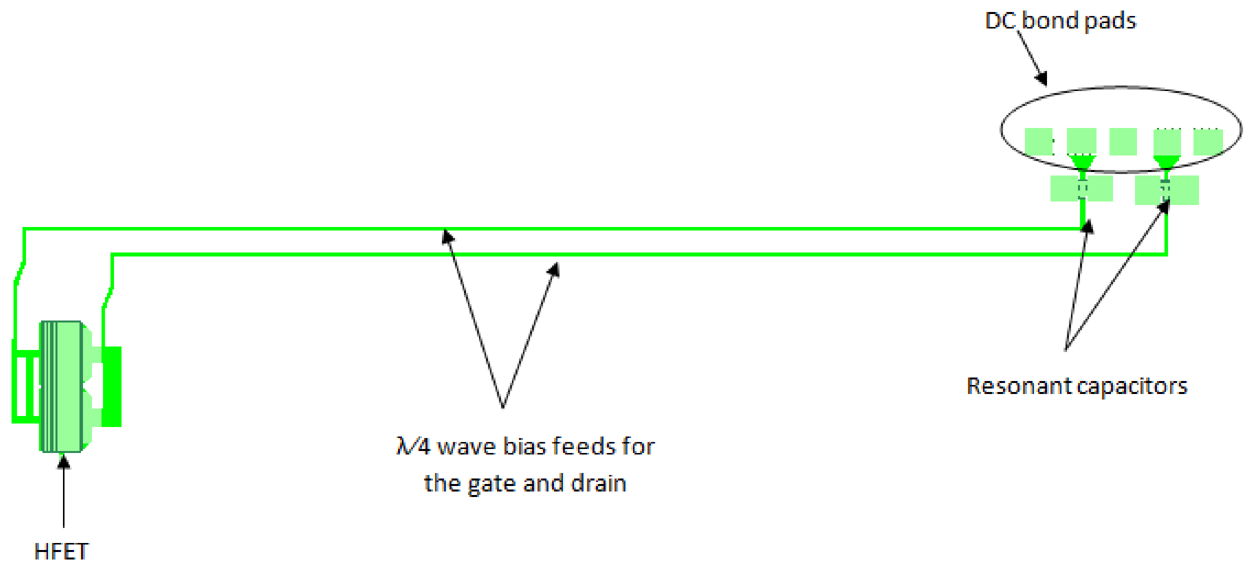


Figure 58: Layout design of bias circuit

4.1.9.4 Layout input and output matching networks

In section 4.1.5.2 schematic components were used to realize the matching. Then the components were replaced by layout foundry elements and additional transmission lines were included to realize the layout. In order to null the ESR and ESL effects of the lumped elements of the foundry and to take into account capacitances and inductances of the added distributed elements, matching component values needed to be tuned to achieve the optimum impedances. Figure 60 and figure 61 depicts the schematic and layout designs of the matching networks. In reference to the following elements in figure 59, input matching components were tuned as follows:

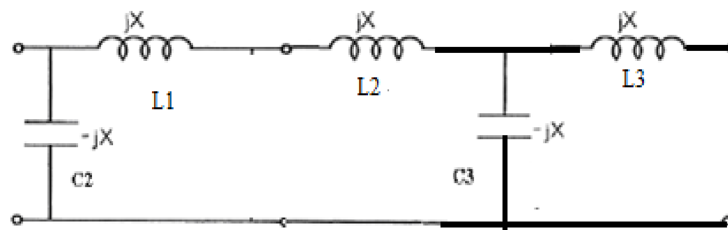


Figure 59: Tuned input matching equivalent circuit

Table 7: Input matching components before and after tuning

Component	Original match	Tuned match
L1	0.4nH	0.8nH
L2	n/a	0.3nH
L3	0.24nH	0.24nH
C2	7.2pF	0.9pF
C3	7.2pF	3.8pF

Output matching L and C values were changed as follows after tuning:

Table 8: Output matching components after and before tuning

Component	Original match	Tuned match
L	2.6nH	3.6nH
C	2.8pF	3.8pF

Following table summarizes the simulated verification results of the tuned layout match:

Table 9: Layout and schematic class AB performance summary

Parameter	Class AB performance @ 2.655GHz in schematic design	Class AB performance @ 2.655GHz in layout design
Compressed Pout	39.7 dBm	40.23dBm
Efficiency at compressed Pout	52.6%	49.98%
Gain at compressed Pout	9dB	10dB

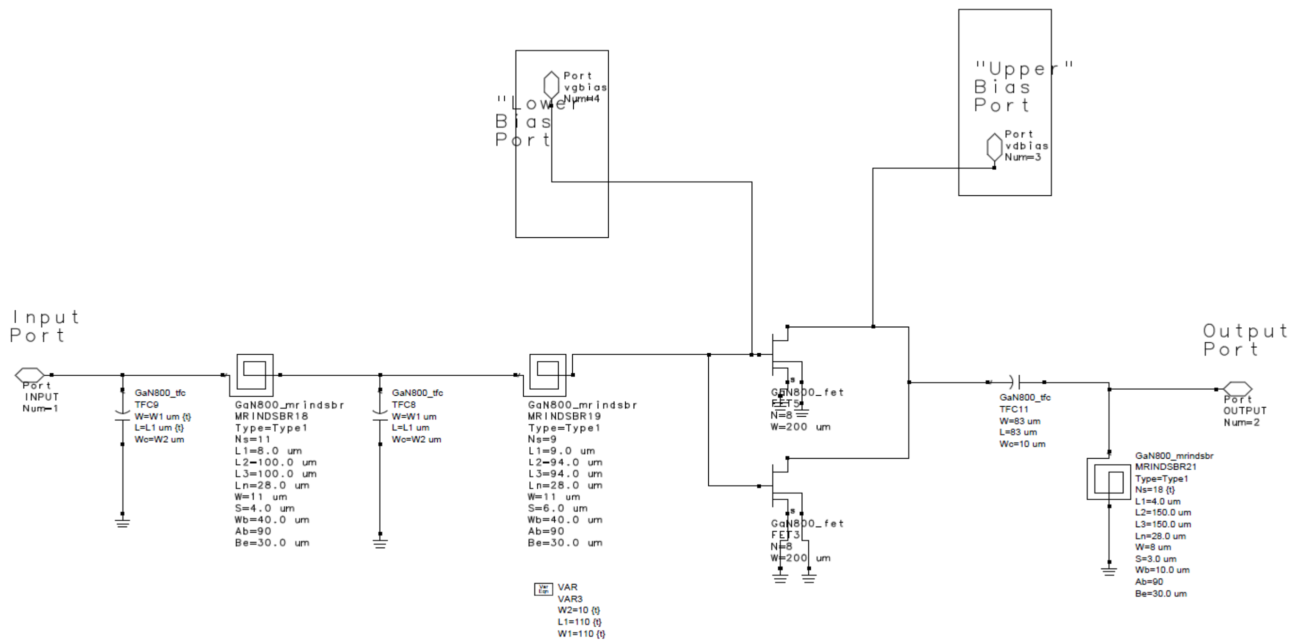


Figure 60: Schematic input and output matching networks

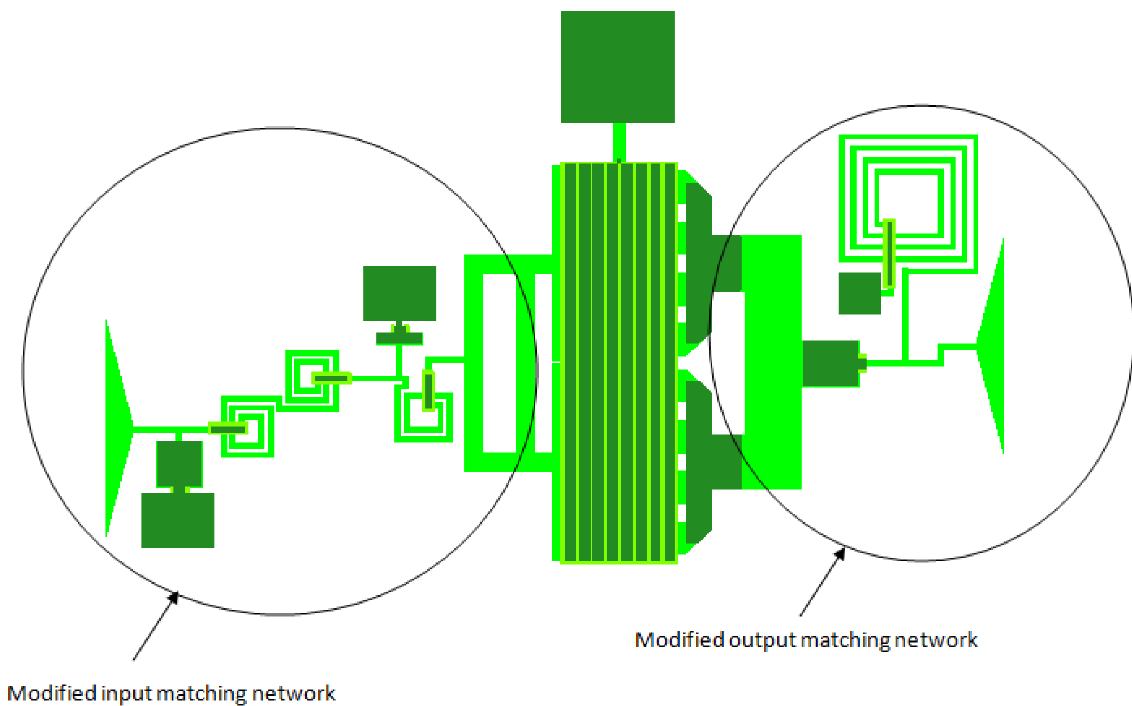


Figure 61: Layout input and output matching networks.

4.1.9.5 Doherty combiner layout

In order to fit the full design in a 10mm x 11.5mm layout area, the Doherty combiner had to be meandered as shown in figure 62 below:

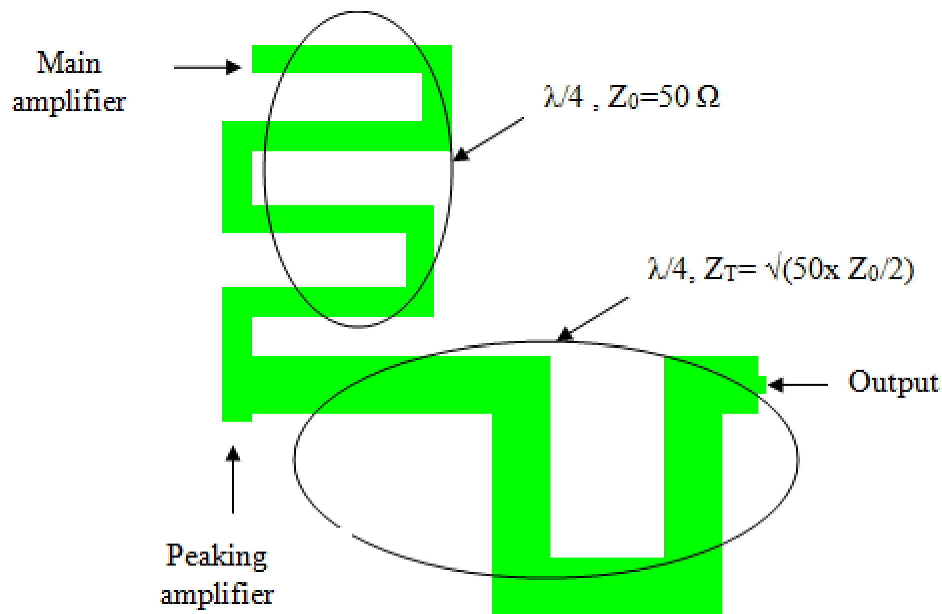


Figure 62: Doherty combiner layout

To verify the Doherty combiner design structure, a secondary set of impedances can be defined as per figure 63 at nodes A, B and C with 50Ω load terminations.

If all three nodes (A, B and C) in figure 63 were terminated with 50Ohm, the impedances looking into each node of the combiner would be:

A= 150Ω= (Zo^2 / impedance 17 Ω at node B)

B = 17 Ω = (50 Ω parallel with 25 Ω)

C= 50 Ω

The simulated designed combiner impedances are reported in Figure 64.

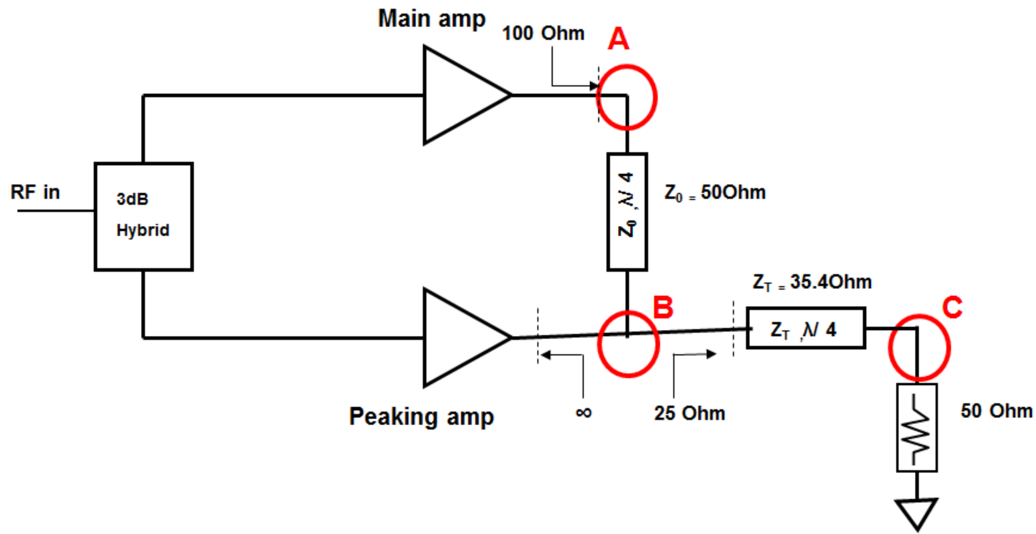


Figure 63: Doherty combiner verification

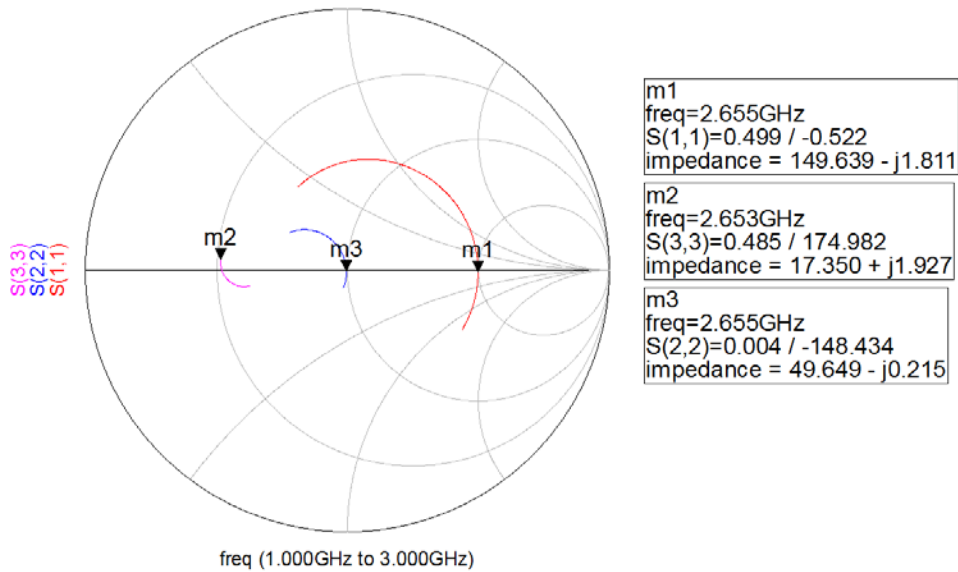


Figure 64: Verification of layout design of the Doherty combiner

As seen in figure 64, the designed combiner provides impedances close to the targeted impedances at each node.

4.1.9.6 Complete Doherty amplifier layout

Figure 65 below depicts the complete layout of the designed MMIC Doherty amplifier.

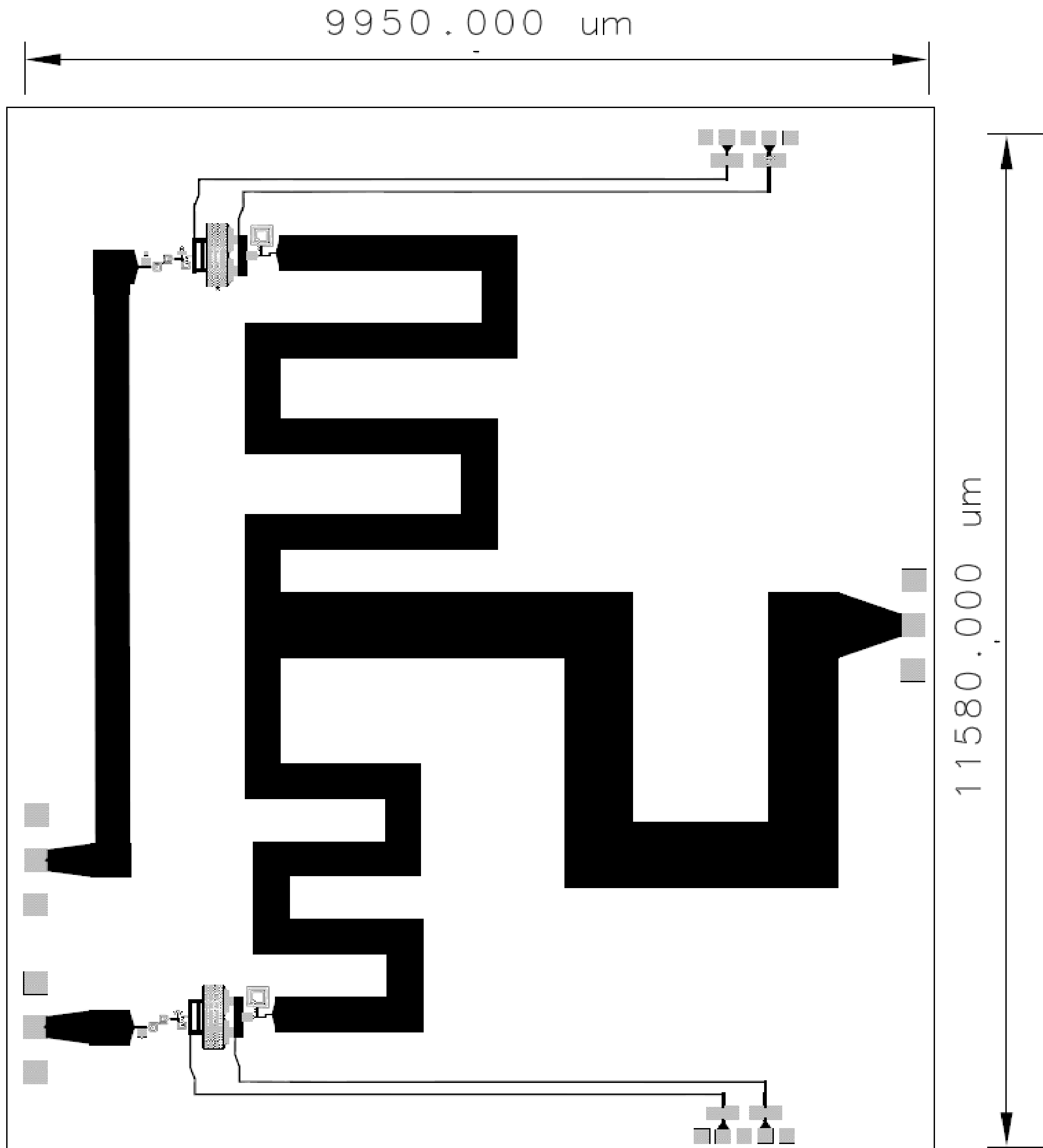


Figure 65: Layout of the designed MMIC Doherty amplifier

4.2 Doherty amplifier Performance Evaluation

This section of the report provides the single and dual tone simulation results of the designed Doherty Power Amplifier. This segment also discusses various optimization methods to tune the design for either optimum efficiency or linearity. Finally a literature study is presented to compare the designed MMIC Doherty amplifier performance to previously published MMIC amplifiers. The performance analysis of the designed Doherty topology was executed in co-simulation of Agilent's Advanced Design System 2009. Before proceeding with the large signal performance evaluation, a small-signal S-parameter characterization was performed on the Doherty amplifier under a fixed drain bias of 20V and gate bias voltages of -3.0V and -4.9V for the main and peaking amplifiers respectively.

The simulated small signal parameters S11 and S21 are shown in figure 66 below. It can be observed that the Doherty amplifier provides a return loss of -14dB over the bandwidth of 2.62 to 2.69GHz.However, a frequency shift in the return loss can be observed. A flat small signal gain of approximately 11.0dB has been measured over the frequency range of 2.62 to 2.69GHz.This accounts for the required bandwidth of the LTE band 7 base station applications.

4.2.1 Large signal single tone simulations

In order to assess the large-signal performance of the Doherty amplifier single-tone and two-tone large signal simulations have been performed with a fixed drain bias of 20V. Figure 67 (a) and (c) show the single-tone power added efficiency response of the Doherty amplifier along with that of a conventional class AB power amplifier. The figure clearly depicts that the Doherty power amplifier has higher efficiency over a wider range of output power compared to a Class AB power amplifier of the same power sizing. The key point to note is the 17% increase in efficiency at the back off power level of the Doherty power amplifier. Although a relatively constant efficiency is expected in the full 6dB back off range, a slight dip in the PAE between the two peak points can be noticed. This is due to the lower gain of the peaking amplifier from Class C operation. This situation could be overcome by having an unequal power division at the input, delivering higher power to the peaking amplifier than the main amplifier [49].

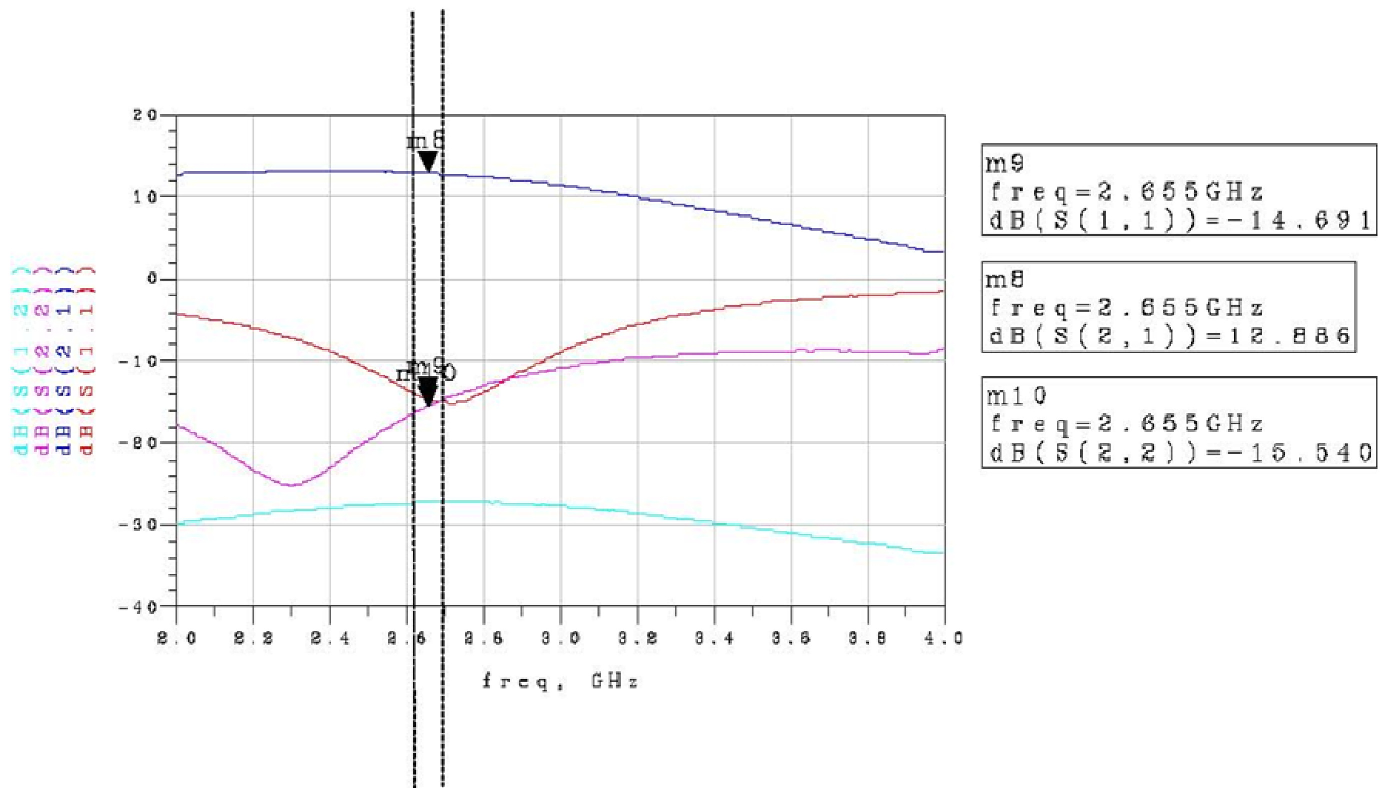
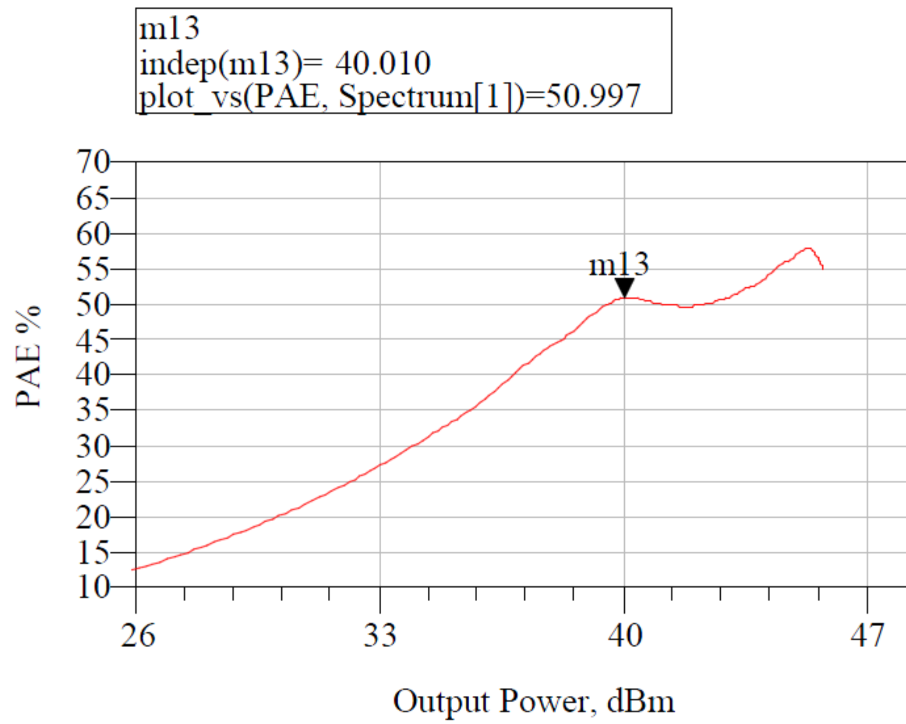
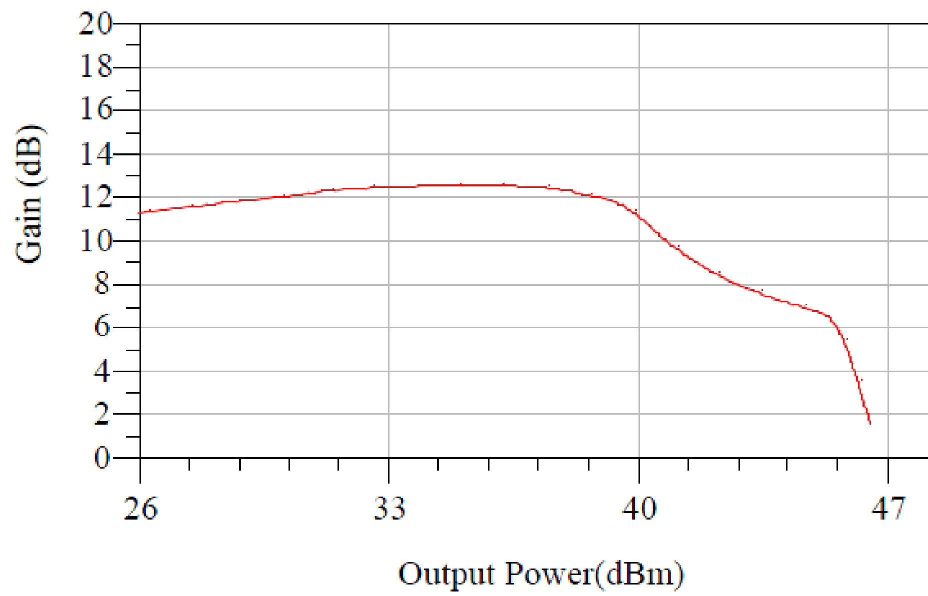


Figure 66: Simulated small signal S-parameters of the Doherty Amplifier

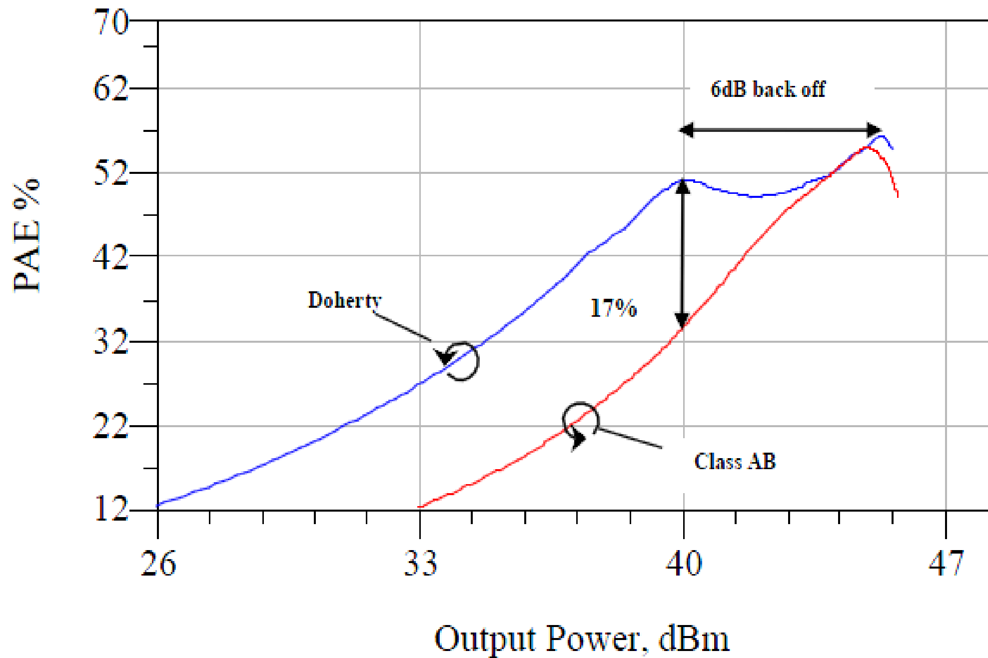
Figure 67 (b) shows the gain vs output power of the Doherty amplifier. Note the reduced gain in Doherty mode in the upper 6dB range. This caused by the class C bias of the peaking amplifier. With this class C bias, it is typically difficult to match the gain of the full Doherty amplifier to be greater than the main amplifier. Also note that, as per theory, the saturated output power of the Doherty topology is approximately 6dB higher than the main amplifier saturated output power which was shown in figure 48.



(a)



(b)

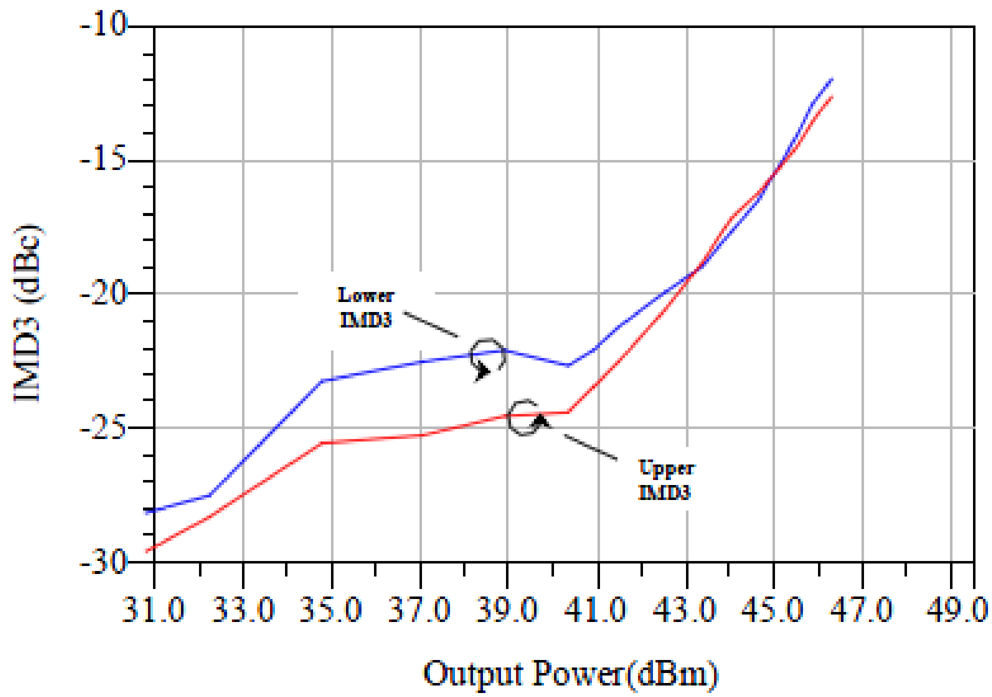


(c)

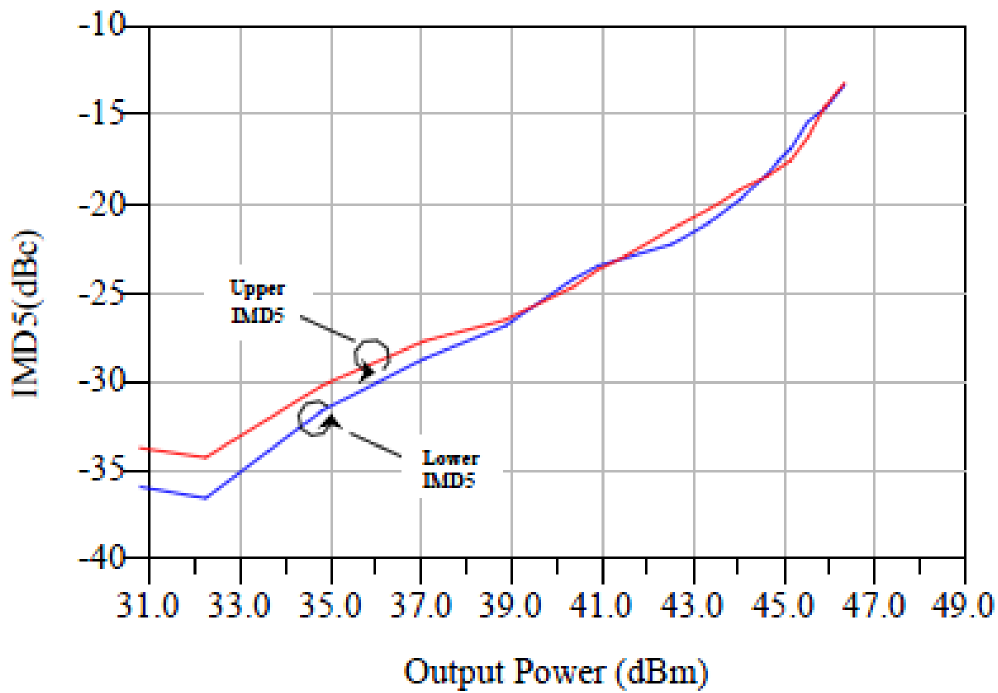
Figure 67: Single tone simulations with Vdrain=20V, Vgs_main=-3.0V,Vgs_peak=-4.9V (a) Power added efficiency of the Doherty amplifier (b) Gain of the Doherty amplifier (c) Comparison of Power added efficiencies of Class AB and Doherty amplifiers

4.2.2 Large signal two tone simulations

Two tone simulations were performed to qualitatively analyze the linearity of the Doherty amplifier. Figure 68 shows the simulated third and fifth order intermodulation products (IMD3 and IMD5) of the Doherty amplifier at its nominal bias points for main and peaking amplifiers (Vdrain=20V, Vgs_main=-3.0V, Vgs_peak=-4.9V) at 2.655GHz with tone spacing of 1MHz. Due to the distortion caused by the low biasing of the peaking amplifier the intermodulation distortion of the Doherty amplifier looks to be poor. By altering the bias conditions of the peaking amplifier, proper turn on characteristics can be achieved to suppress these distortion levels. This would be further discussed during Doherty topology optimization in section 4.2.4. Also, since the base station power amplifiers are typically operated with a linearization system, the observed IMD levels should be sufficient for a base station application.



(a)



(b)

Figure 68: Two tone simulations with Vdrain=20V, Vgs_main=-3.0V,Vgs_peak=-4.9V (a) IMD3 Vs output power of the Doherty amplifier (b) IMD5 Vs output power of the Doherty amplifier

4.2.3 Thermal dissipation

Following Table 10 shows the current draw and the thermal dissipation of the designed Doherty MMIC.

Table 10: Thermal dissipation and total current draw of the Doherty PA

Available Source Power dBm	OutputPower dBm	DC Power Consumpt. Watts	High Supply Current	Thermal Dissipation Watts
26.500	39.043	21.190	1.058	3.682
26.600	39.142	21.377	1.068	3.450
26.700	39.239	21.558	1.077	3.215
26.800	39.334	21.730	1.085	2.971
26.900	39.425	21.880	1.093	2.707
27.000	39.515	22.013	1.099	2.423
27.100	39.604	22.154	1.106	2.138
27.200	39.693	22.315	1.115	1.860
27.300	39.782	22.486	1.123	1.575
27.400	39.871	22.646	1.131	1.263
27.500	39.960	22.798	1.139	0.932
27.600	40.047	22.958	1.147	0.600
27.700	40.132	23.130	1.155	0.277

As seen by the data in the table, the thermal dissipation for this design is quite low. When working with GaN it is critical to pay attention to thermal dissipation. While the RF power densities of GaN scale up to values of 30 w/mm unit-gate width but quantities such as thermal conductivities of the substrate and packaging materials, maximum system temperatures, and allowable dissipated power per area do not scale accordingly. Therefore, thermal management is crucial in order to utilize at least a fraction of the maximum potential of GaN in packaged devices and mounted MMICs . A commercial GaN vendor Cree states the following "Reports of high total RF power from both SiC and GaN over a wide frequency range are beginning to validate the very high power densities that have been demonstrated on small periphery devices for several years. These high power densities in terms of W/mm also present an extreme power dissipation demand on the substrate. Fortunately, the high thermal conductivity of the SiC substrates, >3.3 W/cm-K, allows these higher power densities to be efficiently dissipated, preventing the extreme channel temperatures due to self-heating that are likely with low thermal conductivity substrates such as sapphire and silicon." [54].

There are number of methods that can be implemented to ease this high thermal dissipation such as flip-chip mounting, cluster matching (a way of distributing the signal among a number of smaller devices in order to spread the head over a wider area) and bath-tub via processing (substrate is thinned only under the power devices since a thinner substrate would provide good heat dissipation).

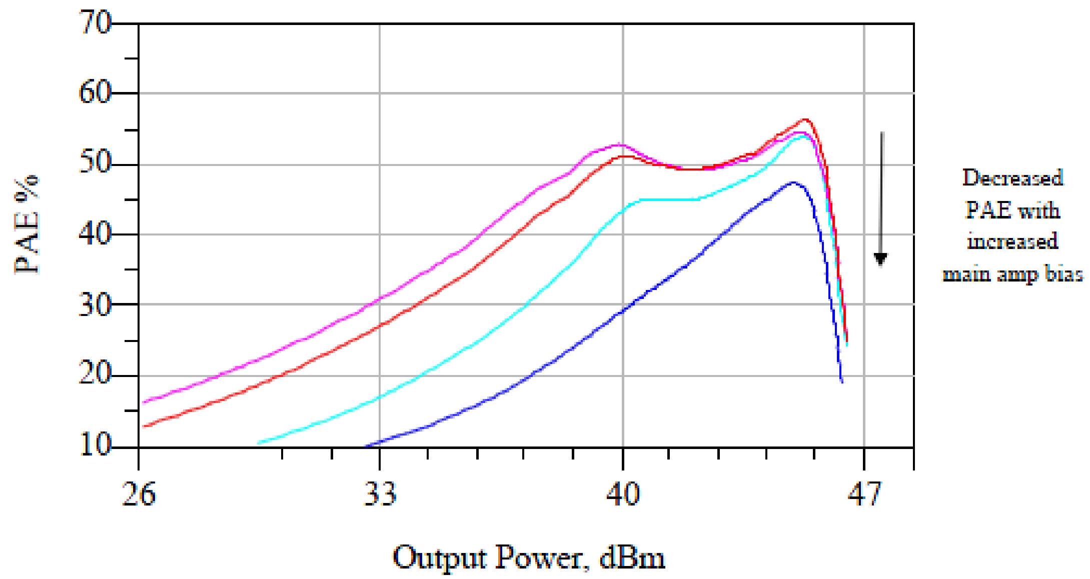
4.2.4 Performance Optimization

In this section of the report, performance optimization of the Doherty amplifier is executed by altering the biasing of the main and peaking amplifier. An analysis of the impact of various biasing on the main and peaking amplifier of the Doherty amplifier is discussed showing the trade-offs between gain and efficiency of the full Doherty amplifier. The choice of operation of the amplifier depends mainly on the requirement of the application; therefore a suitable biasing scheme needs to be selected depending on the application.

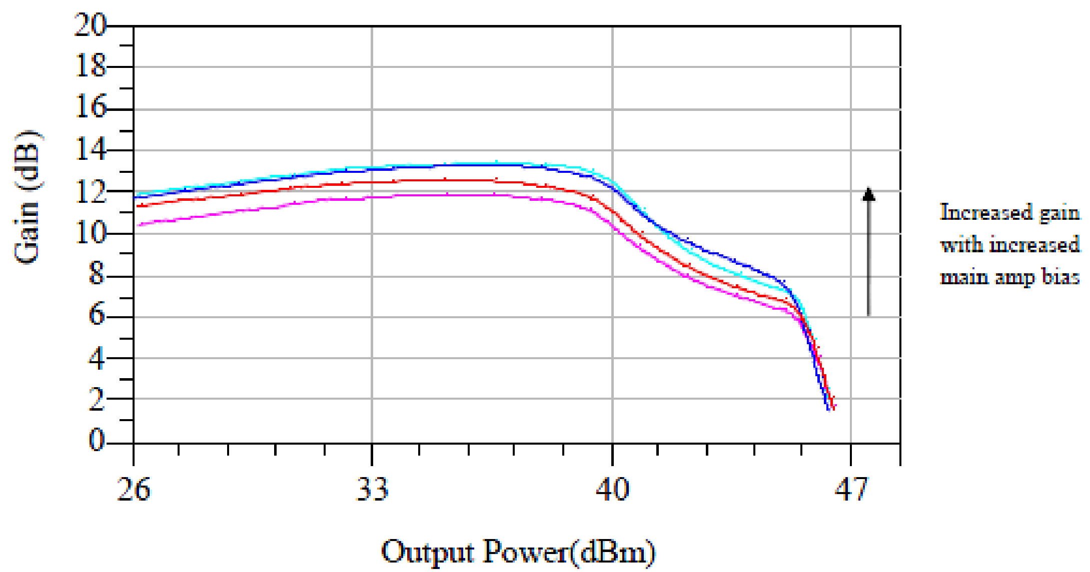
4.2.4.1 Main and peaking amplifier bias optimization

This section discusses the impact on the full Doherty amplifier with various biasing of the main and peaking stages of the amplifier. As the primary intent of the Doherty technique is to provide high efficiency, the common approach is to bias the main amplifier for class AB or B operation .In this optimization step, the peaking amplifier was biased at a constant class C (Vgs= -4.9V) and the main amplifier gate voltage was adjusted from -0.5V to -3.5V to vary the class of operation from class A to deep class AB to class AB. Figure 69 summarizes the outcome of this experiment.

By observing Figure 69 (a), it can be seen that there is a drop in efficiency, as the gate voltage is increased closer to class A operation of the main amplifier. The effect of the increased gate voltage can be seen especially at the back off power level. The gain response of the amplifier in Figure 69 (b) indicates a reduction in gain with reduced bias of the main amplifier.



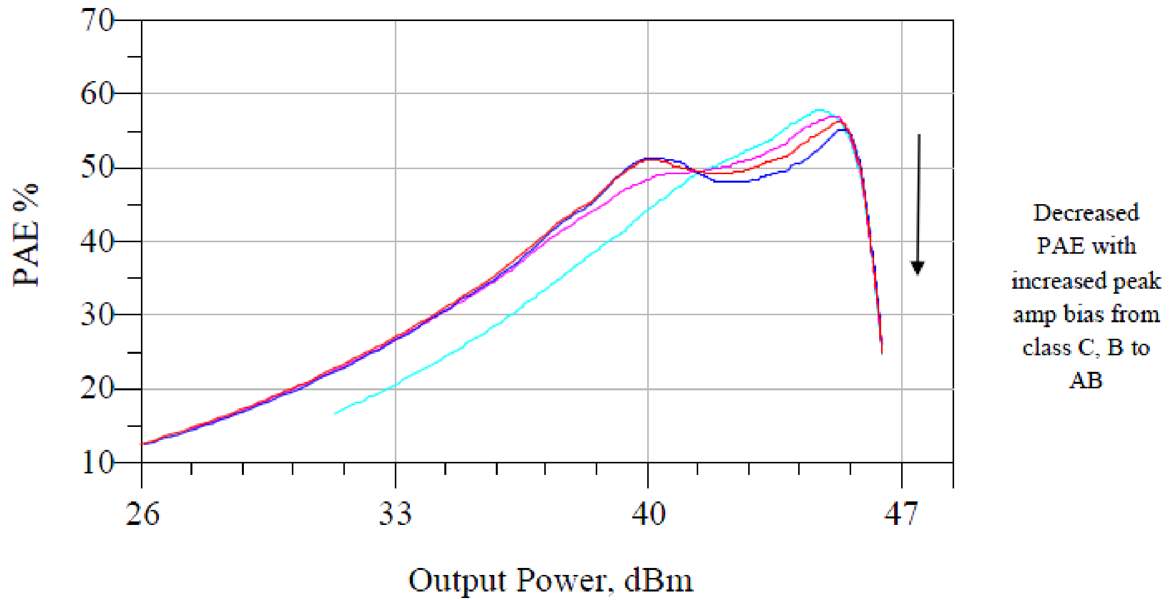
(a)



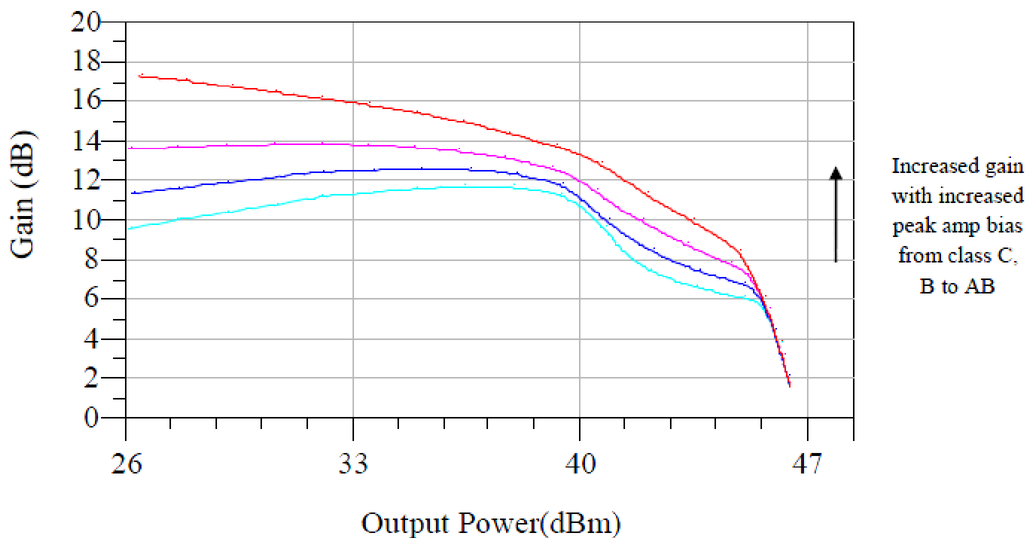
(b)

Figure 69: Doherty amplifier optimization with main amplifier bias variation (a) PAE response of Doherty amplifier with variation in main amplifier bias (b) Gain response of Doherty amplifier with variation in main amplifier bias

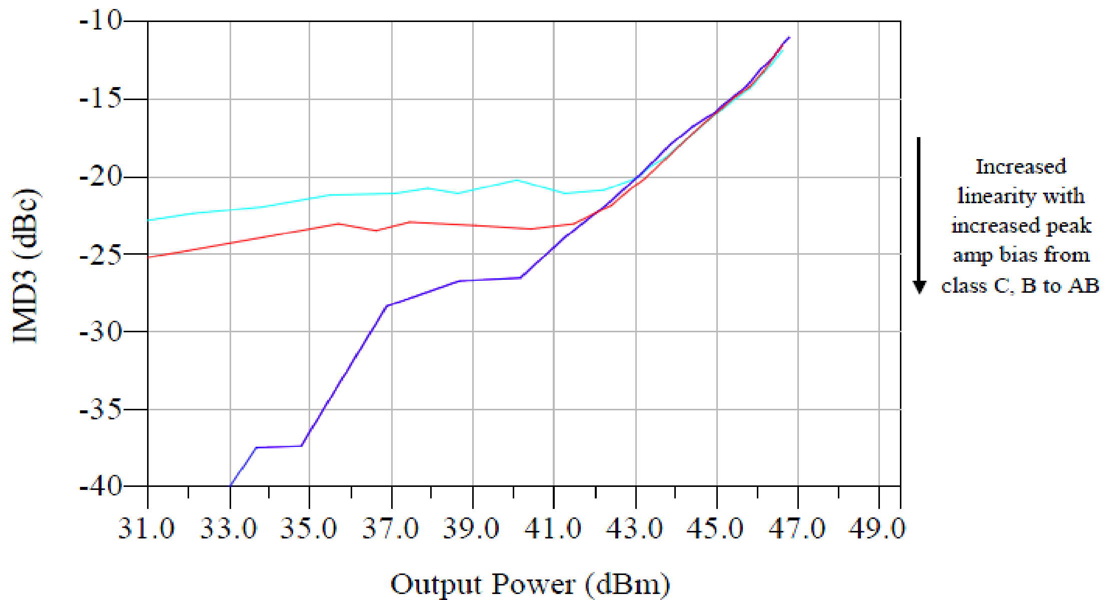
The second approach for optimization was done by varying the peak amplifier gate bias voltage from class C, class B and class AB with constant main amplifier class AB bias of -3.0V. As described previously, the role of the peaking amplifier to act as an active load to the main amplifier. As the peaking amplifier begins to conduct, the load presented to the main amplifier gets altered. Figure 70 below summarizes the analysis of the Doherty amplifier with varying gate bias of the peaking amplifier.



(a)



(b)



(c)

Figure 70: Doherty amplifier optimization with peaking stage bias variation (a) PAE response of Doherty amplifier with variation in peaking amplifier bias (b) Gain of the Doherty amplifier with variation in peaking amplifier bias (c) IMD3 response of Doherty amplifier

By observing the PAE response in figure 70 (a), the corresponding reduction in the back off efficiency can be observed with Class B and AB bias of the peaking amplifier. The maximum efficiency at back off reached when the peaking amplifier is biased in class C. Figure 70 (b),exhibits that maximum output power can be varied with variation in gain by adjusting the class of peaking amplifier bias. There is also degradation in linearity with peaking amplifier bias closer to class C mode which is indicated by the IMD3 plots in figure 70(c). With the above results, the following can be concluded:

- When main amplifier is biased higher, the overall gain of the Doherty amplifier reduced.
- When peaking amplifier is operated at higher bias levels, the overall Doherty amplifier exhibits better linearity with higher gain but reduces the back off efficiency of the Doherty amplifier as a result of reduced load modulation range.
- When peaking amplifier is operated at lower bias levels as class C, efficiency at back off is increased but with reduced linearity.

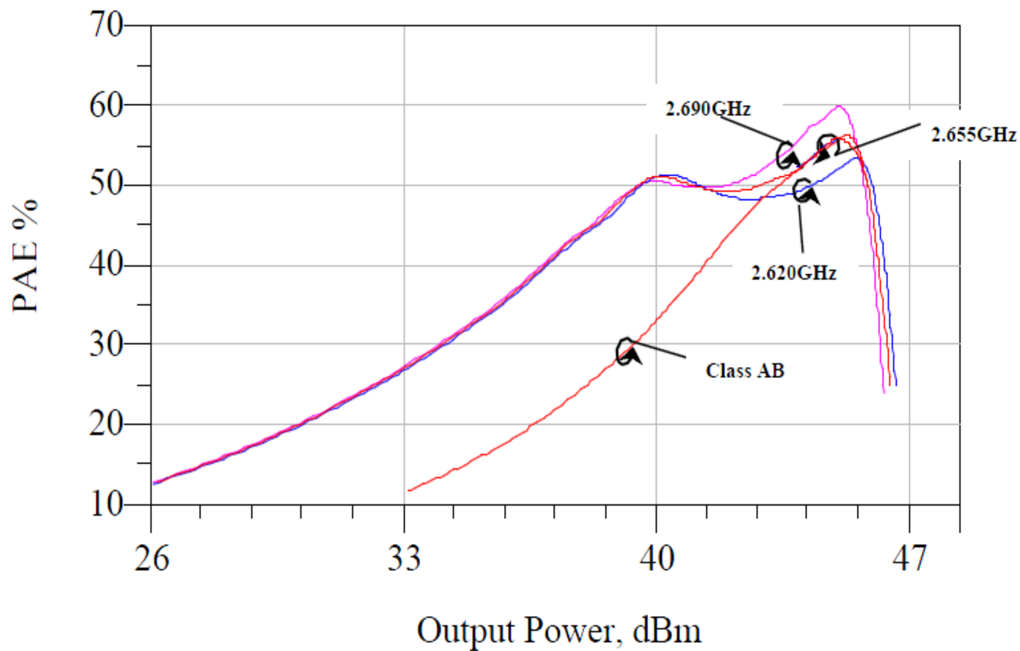
Thus, the operating point of the Doherty amplifier has to be decided based on the system considerations of the full base station to decide the proper trade-offs between efficiency and linearity. For instance if the power amplifier is intended to be implemented with a linearization technique as digital pre distortion, more emphasis can be placed on the efficiency aspect of linearization.

4.2.5 Full LTE band-7 over frequency performance summary

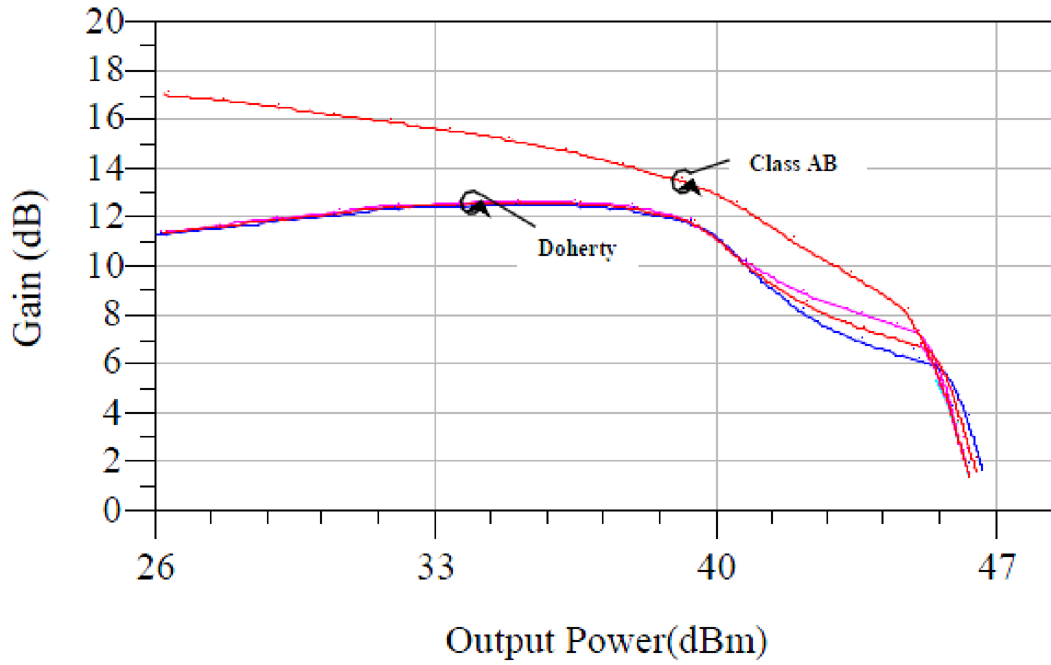
A summary of full LTE band-7 over frequency performance of the designed MMIC Doherty Amplifier is given in Table 11.

Table 11: Full LTE band-7 performance summary of the MMIC Doherty Amplifier

Parameter	2.62 GHz	2.655GHz	2.69GHz
Gain (dB)	11.19	11.10	11.09
PAE at back off power (%)	51.29%	51.09%	50.52%
PAE at peak power (%)	53.31%	56.27%	59.89%
IMD3 (dBc)	-19.95	-20.2	-21.45



(a)



(b)

Figure 71: Simulated over Frequency performance of the Doherty Amplifier with Vdrain=20V, Vgs_main=-3.0V,Vgs_peak=-4.9V (a) Over frequency PAE % of the designed MMIC Doherty Amplifier

The designed MMIC Doherty amplifier performance can be compared to published MMIC amplifier performances as follows:

Table 12: Performance comparison of the designed Doherty PA to published MMIC PAs.

Ref	Year published	Frequency (GHz)	Device Technology	Peak power (W)	PAE at peak power (%)	PAE at back off power (%)
	This thesis	2.65	GaN	40	56.3% [3]	51.1% [3]
[69]	2011	3.5	GaN	31	45% [2]	15% [2]
[70]	2010	7.0	GaN	2.5	51% [3]	31% [3]
[71]	2010	2.6	GaAs	0.5	34% [1]	23% [1]
[72]	2009	2.0	GaN	2	35%	18%
[73]	2009	2.0	GaN	10	42.2 %	33%
[74]	2008	3.1	GaN	38	37% [2]	18% [2]
[75]	2008	3.0	GaN	5	32.5 %	18 %
[76]	2008	4.0	GaN	10	45 %	35%
[77]	2006	1.9GHz	GaAs	1	38% [1]	35% [1]

[1] Measured Doherty results
[2] Simulated results with other architectures
[3] Simulated Doherty results

Chapter 5 Conclusion and Future Work

5.1 Summary

In this research efficiency enhancement of a GaN based power amplifier is explored. This is implemented through the design of a MMIC two-way Doherty power amplifier for a pico-cell base station that would meet requirements of LTE standards. The intent was to realize a Doherty topology suitable for a base station by improving its characteristics compared to existing conventional power amplifiers and other efficiency enhancement techniques while meeting the stringent form factor requirements of a pico-cell. Demonstrative design and implementation have been provided based on the emerging GaN device technology. Specific advantages of GaN such as low output capacitance, high output impedance and higher power density have been utilized at various stages of the thesis.

During this research, the most common conventional PAs such as class A, B, AB and C were reviewed. An overview of currently available power amplifier efficiency enhancing methods such as Envelope Elimination and restoration, Envelope tracking and Chireix Outphasing is also presented. A detailed discussion on the theory of the Doherty topology was provided along with an overview of GaN semiconductor technology. It is illustrated how a GaN based Doherty architecture is the optimum selection for the application considered.

The Doherty amplifier design approach presented in this dissertation relies on reliable accurate CAD tools for analysis and optimization. Therefore in order to assess the accuracy and reliability of large-signal models for a new device technology as GaN, experiments were performed on a commercial GaN design to validate the large-signal models by comparing the measured and simulated behavior of a printed circuit board (PCB) based class AB GaN power amplifier design.

Based on the Doherty concept, a design of a MMIC power amplifier was implemented for LTE band 7 which entails the frequency band from 2.62-2.69GHz. . The design was simulated and the results were compared with that of the theoretical Doherty amplifier as well as a

corresponding conventional class AB power amplifier. The full layout of the design is presented comprising the conversion of the schematic design into something that is able to be fabricated by the foundry. The impact of the main and peaking stage biasing on the overall performance was also analyzed and options to optimize linearity with the least amount of reduction in the improved efficiency is presented to cater various system requirements.

5.2 Conclusion

The MMIC Doherty amplifier design, reported in this thesis has demonstrated the feasibility of achieving high efficiency at the back off power levels while maintaining reasonable linearity compared to conventional PA designs. Although the linearity reported in this design does not directly satisfy LTE requirements, additional linearization can be applied to achieve the required correction. It is essential to note the efficiency achieved in this thesis is the highest at back off power levels compared to published MMIC PA designs. The most significant contribution of this thesis is the detailed design and implementation of a two way MMIC Doherty amplifier for LTE standards that is applicable for a pico-cell base station. It demonstrates a PAE of 50.5% in the 6dB back off power from a peak power of 46dBm, for the full LTE band 7 which entails the frequency band from 2.62-2.69GHz.Additional contribution is offered through the bias optimization technique presented for the main and peaking amplifiers to shift between a highly linear or highly efficient performance of the same design.

5.3 Future Work

Improving efficiency of power amplifiers at high back off levels while sustaining linearity will remain an essential aspect of future work. With the growing trend towards the usage of pico-cell base stations, fully integrated MMIC designs of power amplifiers will also gain more traction. 4G standards as LTE could utilize signals with PAPRs up to 10dB with broad instantaneous bandwidths (IBWs) of up to 60MHz.The following recommendations can be considered to further expand the direction of research:

- MMIC Doherty amplifier presented in this thesis can be further analyzed by implementing a linearization technique such as digital pre-distortion. This would add fur-

ther value to the design by retrieving the degraded linearity that was compromised for higher efficiency.

- In order to support PAPRs of higher than 6dB, the back-off region can be extended by implementing the MMIC design in an asymmetrical or a multi-stage Doherty architecture. An asymmetric topology would consist of main and peaking amplifiers of different sizing and N-stage design would consist of multiple peaking amplifiers.
- In order to support higher IBWs, the MMIC Doherty amplifier design can be further optimized to have broad video bandwidths. Implementation of multi section $\lambda/4$ bias feeds, multiple radial stubs and addition of selected decoupling capacitors with resonance frequencies distributed over the entire video bandwidth are a few methods that can be implemented.

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Appendix A: CGH25120F evaluation board

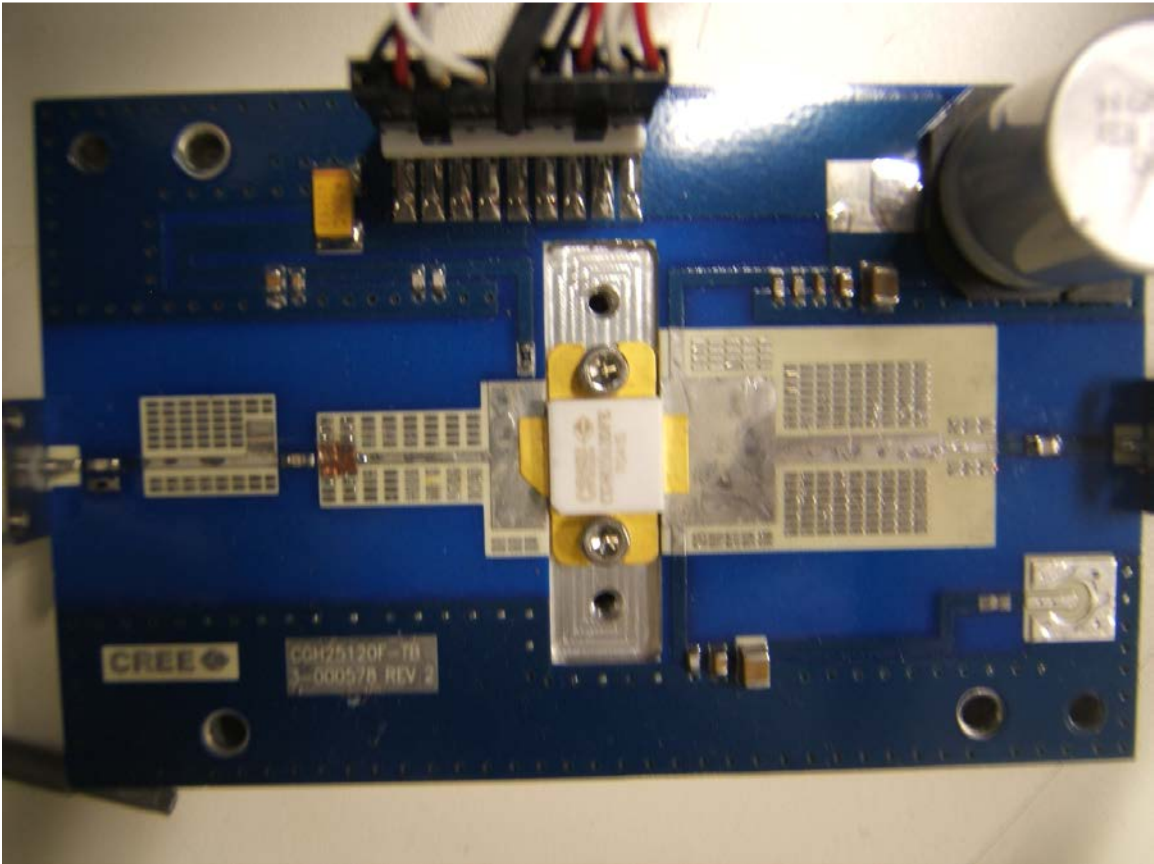

Figure 72: Tested CGH25120F evaluation board

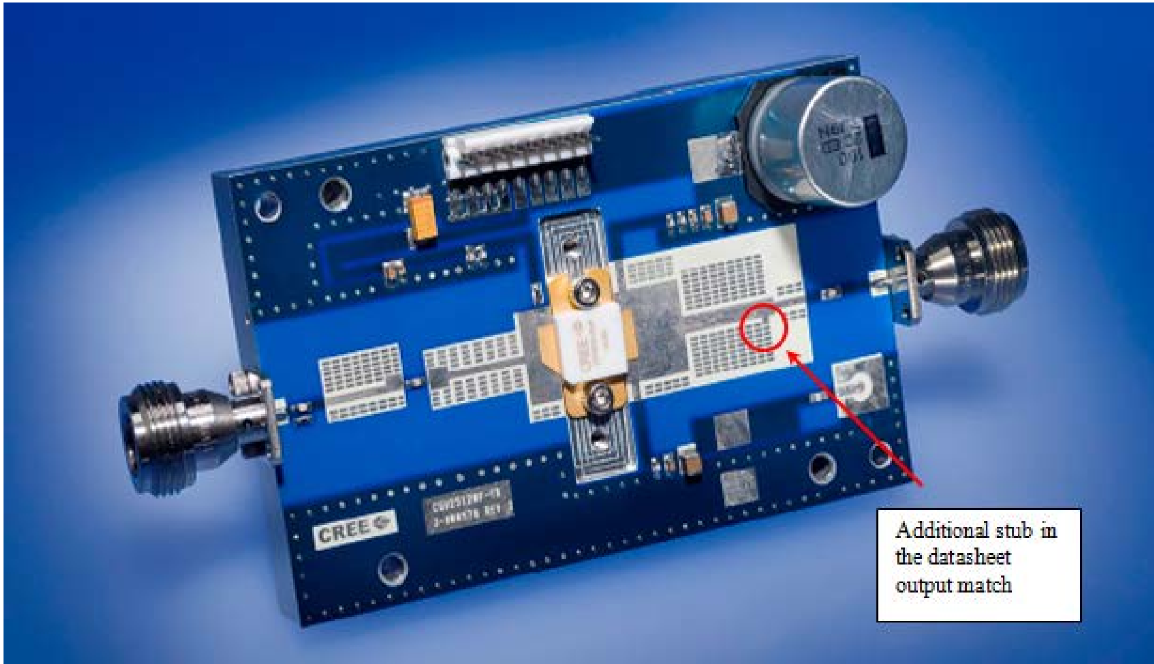

Figure 73: Datasheet image of CGH25120F evaluation board [54]

Appendix B: Simulation test bench and results of CGH25120F

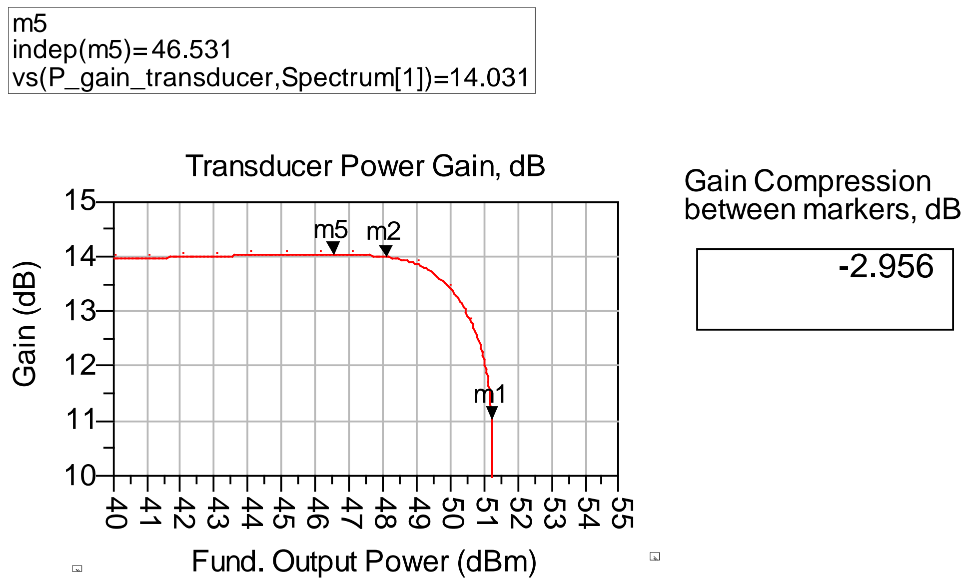

Figure 74: CGH25120F evaluation board simulated gain compression curve at 2.650GHz

m7
indep(m7)= 46.032
vs(real(Is_high.i[0]),Spectrum[1])=3.594

m6
indep(m6)= 43.003
vs(real(Is_high.i[0]),Spectrum[1])=2.512

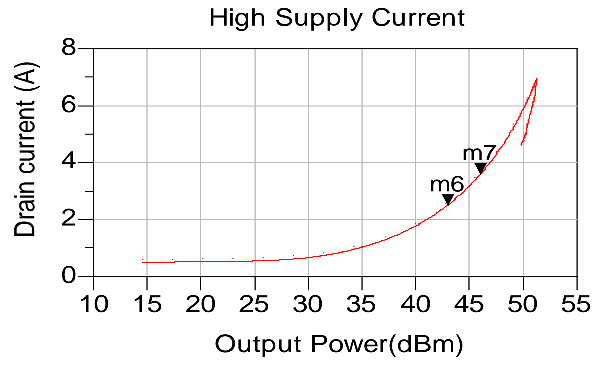

Figure 75: CGH25120F evaluation board simulated current consumption Vs output power at 2.650GHz

Momentum input matching block

Momentum output matching block

Figure 76: CGH25120F evaluation board co- simulation test bench

Appendix C: Measurement setup for CGH25120F

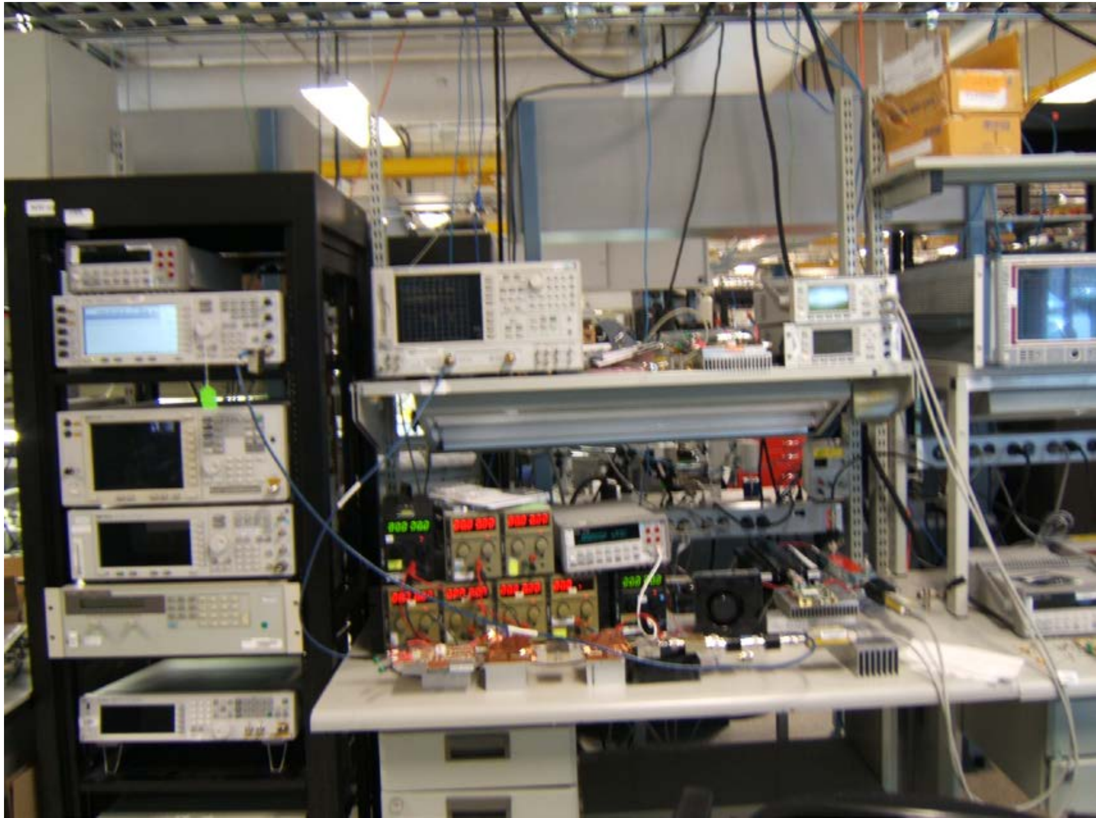

Figure 77: Measurement setup for CGH25120F