Gated Quantum Structures in Two-Dimensional Semiconductors

by

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Declaration of Authorship

I hereby certify that this thesis is entirely my own original work except where otherwise indicated. I am aware of the University of Ottawa regulations concerning plagiarism, including those regarding consequent disciplinary actions. Any use of the works of any other author, in any form, is properly acknowledged at their point of use.

Summary

The family of semiconducting 2H-phase group-VI transition metal dichalcogenides (TMDs) have been suggested to be promising candidates for hosting optically accessible spin qubits due to their desirable optical and electrical properties, however, experimental progress towards this goal has been impeded by the difficulties associated with the fabrication of clean structures with quality contacts. In this thesis, we present the complex process for obtaining functional contacts to two particular TMDs, molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2), from which we use as the foundation for the fabrication of three important gate defined quantum structures: quantum dots, a charge detector, and a long 1D channel. These structures all play an important role in furthering the understanding of these materials and are the building blocks for achieving functional spin qubits.

More precisely, we investigate the contact resistances associated with various cleaning procedures and contact architectures and report a recipe that results in an ultra-low contact resistance even at cryogenic temperatures. We then demonstrate electrical control of hole quantum dots, the host of the spin qubit, in gated heterostructure devices based on monolayer WSe_2 and study its properties. With a similar structure, we demonstrate that a gate-defined nano-constriction is sensitive to the charge occupation of a nearby quantum dot and is therefore suitable to be used as a charge sensor, a valuable component of elaborate quantum circuits. Finally, we demonstrate the realization of a gate-defined quantum confined 1D channel in a high mobility monolayer WSe_2 sample and observe an anomalous conductance quantization in units of e^2/h.

These results pave the way for the development of quantum devices based on electrostatically confined quantum dots defined in semiconducting TMDs and push forward our understanding of their electronic properties.

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À ma belle Mimi et Jude

List of Publications

1. **J. Boddison-Chouinard**, A. Bogan, P. Barrios, J. Lapointe, K. Watanabe, T. Taniguchi, J. Pawlowski, D. Miravet, M. Bieniek, P. Hawrylak, A. Luican-Mayer, and L. Gaudreau. Anomalous conductance quantization of a one-dimensional channel in monolayer WSe_2. *Manuscript submitted for publication*, 2022.

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3. **J. Boddison-Chouinard**, A. Bogan, N. Fong, K. Watanabe, T. Taniguchi, S. Studenikin, A. Sachrajda, M. Korkusinski, A. Altintas, M. Bieniek, P. Hawrylak, A. Luican-Mayer, and L. Gaudreau. Gate-controlled quantum dots in monolayer WSe_2. *Applied Physics Letters*, 119, 133104, 2021.

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Chapter 1

Introduction

In recent years, quantum information processing has received an enormous amount of attention and has developed dramatically. As classical computation has begun to reach its physical limits, the desire to investigate quantum technologies has grown. Potential applications of quantum computing have emerged, including understanding the dynamics of quantum systems with many degrees of freedom through quantum simulations [1], assisting in the exchange of private communications through quantum cryptography [2], and providing new quantum algorithms such as the factoring [3] and searching [4] algorithm.

Many implementations of quantum information have been developed or envisioned, including superconducting qubits [5–11], spin defects in wide-bandgap materials [12–15], photonic qubits [16, 17], ion trap systems [18, 19], topological protected qubits [20, 21], and semiconductor quantum dots [22, 23].

Semiconductor quantum dots realized by patterned electrostatic gates are particularly attractive due the large degree of electrical tunability of the quantum dot properties. Furthermore, by their nature of fabrication, nanolithography, the precise placement of quantum

dots to create large arrays is achieved relatively easily.

Early implementation of qubits based on the electron spin confined to a quantum dot were demonstrated in gate-defined quantum dots in the two-dimensional electron gas (2DEG) in a III-V semiconducting heterostructure [24–27]. Although 2DEGs created in these materials have demonstrated high mobilities and possess a standard fabrication process, the qubit coherence time is limited by the hyperfine interactions between the spin qubit and the non-zero nuclear spins of the host material [28]. Due to the low abundance of spin-1/2 ^{29}Si isotopes in natural silicon (Si) [29], interest in Si/SiGe quantum dot devices has grown over the past years. The ability to synthesize isotopically purified silicon has led to the reduction of the hyperfine interaction between the spin qubit and the nuclear bath, resulting in longer coherence times [30]. However, these materials do not possess a direct-band gap, therefore the development of optical photon-to-spin hybrid systems and long-distance quantum network communication remains a challenging feat [31].

Transition metal dichalcogenides (TMDs) are a class of materials that belong to the family of two-dimensional (2D) materials which can be mechanically exfoliated to isolate truly 2D atomic layers. The electronic properties of TMDs cover a broad spectrum ranging from semiconductors [32, 33], to superconductors [34], and more [35–37]. From this extensive family, the 2H-phase group-VI TMDs are the most studied. These materials follow the chemical formula MX_2 where M is either molybdenum (Mo) or tungsten (W), and X is a chalcogen such as sulfur (S), selenium (Se), or tellurium (Te). Structurally, within each layer, the atoms sit in a honeycomb lattice where neighboring lattice sites alternate between a transition metal and a chalcogen dimer (Figure 1.1a). Out-of-plane, separate layers are bonded via weak van der Waals interactions. Bulk TMDs that follow this recipe are semiconductors with an indirect bandgap. The valence band maxima are located at the Γ-point while the conduction band minima are located at the Q-points. As the thickness

of the material is reduced to a monolayer, the TMD crystal becomes a direct bandgap semiconductor with the bandgap located at $\pm K$ [32, 33, 38].

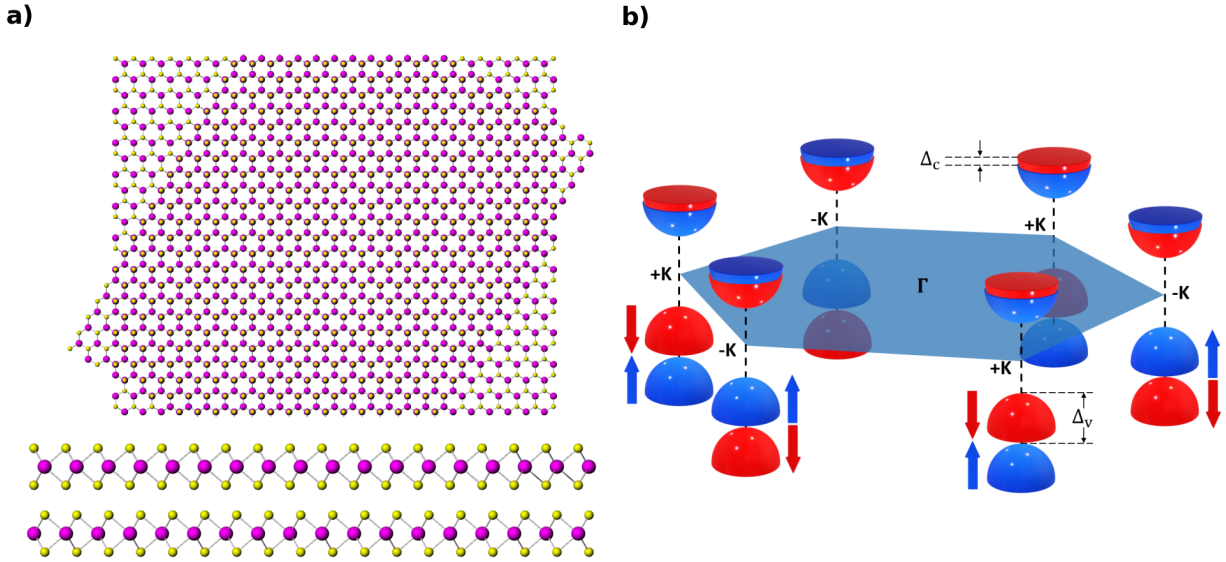

Figure 1.1: (a) Schematic representation of a top view and side view of a bilayer group-VI 2H-TMD. Purple spheres represent the transition metal while yellow spheres represent the chalcogen atoms. (b) Schematic of the direct band gap at the $\pm K$ points representative of a monolayer TMD. Conduction and valence band spin-splitting can be seen where blue (red) bands label spin up $s = 1, \uparrow$ (spin down $s = -1, \downarrow$). Values for spin splitting of MoS_2 are $\Delta_v = 148$ meV, $\Delta_c = 3$ meV, and for WSe_2 are $\Delta_v = 466$ meV, $\Delta_c = 37$ meV [39].

When group-VI TMDs are reduced to the monolayer limit, the crystal symmetry is reduced (2H to 1H), and the inversion symmetry is broken. In addition to the reduced crystal symmetry, the presence of strong spin-orbit interactions, stemming from the d orbitals in the transition metal atom, causes large spin-orbit splitting of the bands at $\pm K$ [40, 41]. A consequence of the lack of inversion symmetry in the monolayer limit and the strong spin-orbit interaction is a breaking of the spin-degeneracy of the valence and conduction bands, resulting in coupled spin and valley degrees of freedom at the $\pm K$ points (spin-

valley locking) [40, 41] (Figure 1.1b). In other words, the spin associated with the upper (lower) band of the valence (conduction) band at the $+K$ point will be opposite of the spin associated with the upper (lower) band of the valence (conduction) band at the $-K$ point. These properties can be summarized by considering the two-band $k \cdot p$ Hamiltonian expanded around the $\pm K$-points [40] which is given as:

$$\hat{H} = at(\tau k_x \hat{\sigma}_x + k_y \hat{\sigma}_y) + \frac{\Delta}{2}\hat{\sigma}_z - \lambda\tau\frac{\hat{\sigma}_z - 1}{2}\hat{s}_z$$

where a is the lattice constant, t is the hopping integral, $\tau = \pm 1$ is the valley index, $\hat{\sigma}$ are the Pauli matrices for the two basis functions, Δ is the size of the band gap, 2λ is the size of the spin splitting at the valence band, and $\hat{s}_z$ is the spin Pauli matrix.

These optical, electrical, and structural properties make monolayer group-VI TMDs an appealing material for hosting qubits. Coherence times are expected to be improved simply by the fact that the carriers are confined to a single atomic layer, hence the bulk nuclear interaction that plagues GaAs based devices is reduced in these materials. Long coherence times are further predicted in spin-valley qubits made from quantum dots in monolayer TMDs due to the spin robustness associated to the spin-valley locking; a significant amount of momentum transfer is needed to send the charge carrier from one valley to another and hence change the charge carrier spin. Furthermore, due to the spin-valley locking and the direct band gap found at the monolayer limit, opposite circularly polarized light can be used to excite carriers in each valley [41, 42]. This valley addressability through polarized light creates a possibility of designing devices operating on the valley degree of freedom instead of the charge and spin degrees of freedom [43].

The promise of TMDs as a favorable material for hosting optically accessible spin-valley qubits with long coherence times piqued the interest of many research groups who have

since demonstrated the controlled confinement of charge carriers in single and double quantum dots in multilayered MoS_2 [44, 45], monolayer MoS_2 [46], and monolayer and bilayer WSe_2 [47]. However, in all the systems, as a result from the high contact resistances, the few-carrier regime needed for quantum information applications was never achieved. Furthermore, adequate charge detection techniques are yet to be studied in TMD quantum dot devices, a key component for multi-dot systems. Additionally, the effects of quantum confinement in these materials are still misunderstood, where unexplained phenomena have been observed [48, 49]. In this thesis, these are the main subjects we investigated.

In chapter 2, we discuss various techniques for fabricating van der Waals heterostructures and introduce different recipes for cleaning the structures. The effectiveness and necessity of the many sample cleaning techniques are then demonstrated by presenting resistance measurements associated to the contacts of devices fabricated using these cleaning techniques. We demonstrate that we can achieve ohmic contacts to monolayer TMDs with low contact resistances at temperatures ranging from 300 K to 4 K using these fabrication techniques.

We then present our results on gate-controlled quantum dots formed in monolayer MoS_2 and monolayer WSe_2 in chapter 3. In both systems, we observe Coulomb blockaded transport through the quantum dots. We are able to locate the quantum dots by measuring the current's dependence on individual gates. From bias spectroscopy measurements performed on a quantum in the monolayer WSe_2 device, an addition energy of 3.4 meV is extracted resulting in the estimation of the quantum dot diameter to be ≈ 58 nm.

In systems with multiple gate-defined quantum dots, it is advantageous to use non-invasive charge detection techniques to monitor the charge occupation of each quantum dot. In chapter 4, we demonstrate that the device architecture presented in chapter 3 can be used to define a nano-constriction employable as a charge sensor for nearby quantum dots.

In chapter 5, a new device architecture is introduced with the advantage that gates can control the carrier density of the TMD sheet and the contact resistance of the leads independently. This is believed to be a key component when attempting to reach the few-charge regime in gated quantum dots. The gates in this architecture are also used to create a long gate-defined one-dimensional channel where we study the hole transport across this channel in monolayer tungsten diselenide (WSe_2). Testifying to the high quality of our device, the quasi-ballistic regime is achieved, and conductance quantization steps are measured in units of e^2/h with an additional robust plateau observed at 0.5 e^2/h in the low carrier density regime. Furthermore, the field effect mobility is acquired resulting in a high value of $\mu_{FE} = 7\ 900\ cm^2/Vs$, again demonstrating the high quality of the monolayer WSe_2 device.

We then conclude the dissertation by summarizing the main finding of the experiments presented in this thesis along with future considerations for device architectures.

Chapter 2

Device fabrication

Due to the known challenges in fabricating TMD devices for quantum transport experiments, a significant portion of the hours spent in the lab were devoted to the critical step of *device fabrication*. TMDs are notoriously difficult to electrically contact with low resistance ohmic contacts [50, 51], and they also host many defects which can greatly limit the carrier mobility of the device [52]. In this chapter, we present the various fabrication techniques and the different contact architectures we investigated, which led to the high-quality contacts and good device performance that we discuss in future chapters.

In section 2.1, we present the three main polymer based transfer techniques used throughout this thesis: the PMMA-PVA method [53, 54], the PDMS stamping method [54, 55], and the pick-up technique [56]. The instrumentation employed for conducting the transfers is also discussed in detail. In section 2.2, we discuss the various cleaning protocols used to improve the surfaces and the interfaces of the fabricated heterostructures. Finally, in section 2.3 we introduce the different contact geometries that were studied and compare their effectiveness. The effect of the discussed cleaning techniques with regard to the contact

performance is also carefully studied.

2.1 Techniques for stacking 2D materials

The backbone of the device architecture used in this thesis is a 2D material belonging to the semiconducting TMD family encapsulated between two flakes of hexagonal boron nitride (hBN), an insulating 2D material. To obtain such a heterostructure, creative fabrication techniques need to be used to precisely stack these atomically thin materials on top of each other. Luckily, not long after the first isolation of monolayer 2D materials [57, 58], research groups around the world have developed techniques [53–56, 59, 60] which continue to be used and improved to this day. The following article[1] discusses two such techniques in detail including the instrumentation necessary for implementing them.

2.1.1 Fabricating van der Waals Heterostructures with Precise Rotational Alignment

Statement of contributions

Justin Boddison-Chouinard (JBC) designed and fabricated the instrumentation used for the experiments. Ryan Plumadore (RP) aided with the design of the program user interface. JBC conducted the experiments and wrote the first draft of the manuscript. JBC and Adina Luican-Mayer (ALM) completed the manuscript.

[1] **J. Boddison-Chouinard**, R. Plumadore, and A. Luican-Mayer. Fabricating van der Waals heterostructures with precise rotational alignment. *Journal of Visualized Experiments*, 149, 2019.

Fabricating van der Waals Heterostructures with Precise Rotational Alignment

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In this work we describe a technique for creating new crystals (van der Waals heterostructures) by stacking distinct ultrathin layered 2D materials. We demonstrate not only lateral control but, importantly, also control over the angular alignment of adjacent layers. The core of the technique is represented by a home-built transfer setup which allows the user to control the position of the individual crystals involved in the transfer. This is achieved with sub-micrometer (translational) and sub-degree (angular) precision. Prior to stacking them together, the isolated crystals are individually manipulated by custom-designed moving stages that are controlled by a programmed software interface. Moreover, since the entire transfer setup is computer controlled, the user can remotely create precise heterostructures without coming into direct contact with the transfer setup, labeling this technique as "hands-free". In addition to presenting the transfer set-up, we also describe two techniques for preparing the crystals that are subsequently stacked.

I. VIDEO LINK

The video component of this article can be found at https://www.jove.com/video/59727/

II. INTRODUCTION

Research in the burgeoning field of two-dimensional (2D) materials began after researchers developed a technique which enabled the isolation of graphene[1–3] (an atomically flat sheet of carbon atoms) from graphite. Graphene is a member of a larger class of layered 2D

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materials, also referred to as van der Waals materials or crystals. They have strong covalent intralayer bonding and weak van der Waals interlayer coupling. Therefore, the technique for isolating graphene from graphite can also be applied to other 2D materials where one can break the weak interlayer bonds and isolate single layers. One key development in the field was the demonstration that just as the van der Waals bonds holding adjacent layers of two-dimensional materials together can be broken, they can also be put back together[2, 4]. Therefore, crystals of 2D materials can be created by controllably stacking together layers of 2D materials with distinct properties. This spurred a great deal of interest, as materials previously inexistent in nature can be created with the goal of either uncovering formerly inaccessible physical phenomena[4–9] or developing superior devices for technology applications. Therefore, having precise control over stacking 2D materials has become one of the main goals in the research field[10–12].

In particular, the twist angle between adjacent layers in van der Waals heterostructures was shown to be an important parameter for controlling material properties[13]. For example, at some angles, the introduction of a relative twist between adjacent layers can effectively electronically decouple the two layers. This was studied both in graphene[14, 15] as well as in transition metal dichalcogenides[16–19]. More recently, it was surprisingly found that it can also alter the state of matter of these materials. The discovery that bilayer graphene oriented at a "magic angle" behaves as a Mott insulator at low temperatures and even a superconductor when the electron density is properly tuned has sparked great interest and a realization of the importance of the angular control when fabricating layered van der Waals heterostructures[13, 20, 21].

Motivated by the scientific opportunities opened up by the idea of tuning the properties of novel van der Waals materials by adjusting the relative orientation between the layers, we present a home-built instrument along with the procedure to create such structures with angular control.

III. PROTOCOL

1) Instrumentation for the transfer procedure

1) In order to visualize the transfer process, utilize an optical microscope that can

operate under bright-field illumination. Since the typical sizes of the 2D crystals are 1–500 μm^2, equip the microscope with 5x, 50x, and 100x long working distance objectives. The microscope must also be equipped with a camera that connects to a computer (Figure 1a).

2) Use separate manipulators to individually control the position of the two crystals that are about to be stacked. Employ manipulators that are programmable and controllable by a computer to minimize vibrations during the transfer procedure.

   NOTE: The manipulators responsible for the movement of the top substrate holder (Figure 1b-c) need only move in the X, Y, and Z direction. Importantly, the manipulators responsible for controlling the bottom substrate holder (Figure 1e-f) are also able to rotate by any angle θ (translational and rotational motion).

3) In order to attach the samples onto the top stage manipulators, fabricate custom sample holders that can support a glass slide; the top crystal will be placed on the glass slide (Figure 1d).

4) For the bottom manipulators, place a flat heating element in a machined glass-ceramic holder (Figure 1g) and affix it to the rotating stage. Connect the heating element to a power supply and a temperature controller.

5) Program the controllers with an instrumentation software (e.g., LabVIEW) to control the relative position of the manipulators (Figure 2).

   1) To perform the necessary motions, program the software with the following capabilities: individually or simultaneously move the manipulators; read, save and retrieve the position of each manipulator; easily adjust the speed of the manipulators, and autofocus the bottom stage. Build-in safety features to prevent any possible collisions between the sample and the lens.

2) Mechanical exfoliation of a 2D crystal

1) Prepare a substrate for the mechanical exfoliation procedure.

   1) Submerge 1 cm x 1 cm squares of silicon/silicon oxide (Si/SiO_2) wafers into a beaker filled with acetone and place the beaker into an ultrasonic cleaner for 10 min.

2) Individually remove the wafers from the beaker with tweezers and rinse them with isopropanol (IPA) then dry them with a nitrogen (N2) gun.
NOTE: When working with acetone and IPA, it is suggested to do so under a fume hood while wearing the proper PPE.

2) Mechanically exfoliate the crystal onto the substrate.

1) Using tweezers, carefully remove a portion of the crystal and place it on a piece of semiconductor-grade adhesive tape.

2) Take a second piece of adhesive tape and firmly press it against the initial tape with crystal then peel away the two pieces of tape. After repeating several times, many thinner pieces of crystal will be found on the tape.

3) Press the adhesive tape with the thin 2D crystals onto a freshly cleaned substrate such that the crystal is in direct contact with the substrate and peel away the tape to leave exfoliated flakes on the substrate.

3) To remove any residual adhesive, place the resulting samples (substrates with 2D crystals exfoliated onto their surface) in a beaker filled with acetone for 10 min. Remove the samples using tweezers, rinse them with IPA, and dry with a N_2 gun.

4) Use an optical microscope to examine the exfoliated flakes. Estimate their thickness by assessing the flake's optical contrast with the substrate[22]. Image the flakes using atomic force microscopy (AFM) in tapping mode (see the Table of Materials) to better quantify the surface morphology and to measure the flake thickness.

3) PMMA-PVA method for fabricating van der Waals heterostructures (top substrate preparation).

1) Prepare the top substrate for the transfer procedure by exfoliating the crystal on a poly(methyl methacrylate) (PMMA) film attached to a glass slide (Figure 3a-d).

1) Follow the procedure described in step 2.1. to obtain a clean substrate. Spin coat a layer of polyvinyl alcohol (PVA) on the substrate at 3,000 rpm for 1 minute by following the protocol described in the instrument's user manual.

NOTE: When using the spin coater, it is suggested to do so under a fume hood while wearing the proper PPE.

2) Directly place the substrate on a hot plate and bake it uncovered in air at 75°C for 5 minutes.

3) Spin coat a layer of PMMA on the substrate from step 3.1.2 by following a procedure similar to the one in step 3.1.1, but this time set the spinning parameters to an angular velocity of 1,500 rpm for 1 min (Figure 3a).

4) Directly place the substrate on a hot plate and bake it uncovered in air at 75°C for 5 minutes.

5) Remove the substrate from the hot plate and place pieces of adhesive tape along its edges to create a tape frame. Then, mechanically exfoliate a 2D crystal on the PMMA surface by following step 2.2 (Figure 3b).

6) Use sharp tweezers to separate the PMMA from the PVA by slowly peeling back the tape frame. The PMMA layer and exfoliated crystal along with the tape frame will detach from the PVA and Si/SiO_2 substrate (Figure 3c).

7) Invert the tape frame and place it on a machined support such that the crystal is facing downwards (Figure 3d).
NOTE: This support enables the user to place the tape frame under an optical microscope to inspect the exfoliation onto PMMA and identify a flake with the desired thickness and geometry.

8) Use sharp tweezers and the optical microscope to place a small washer (0.5 mm inner radius) precisely on the PMMA film such that it surrounds the desired flake (Figure 3d).

9) Lower a glass slide and adhere it to the polymer by pressing it against the exposed tape.

4) Polydimethylsiloxane (PDMS) stamping method for fabricating van der Waals heterostructures (top substrate preparation).

1) Prepare a polypropylene carbonate (PPC) solution for spin coating by mixing three parts PPC crystal with seventeen parts anisole. This is done by letting the solution mix in a stirrer for approximately 8 h or until the solution is homoge-

neous.

2) Prepare the top substrate for the transfer procedure by exfoliating crystal on a PPC film and by then placing it on a PDMS stamp attached to a glass slide (Figure 4a-d).

3) Follow the procedure in step 2.1. to obtain a clean substrate. Spin coat a layer of PPC on the substrate at 3,000 rpm for 1 min (Figure 4a).

4) Directly place the substrate on a hot plate and bake it uncovered in air at 75°C for 5 minutes.

5) Remove the substrate from the hot plate and place pieces of adhesive tape along its edges to create a tape frame.

6) Mechanically exfoliate the 2D layered crystal on the PPC coated substrate by following step 2.2 and use the optical microscope to identify a flake with the desired thickness and geometry. (Figure 4b).

7) Use scissors or a surgical blade to cut a piece of PDMS into a 2 mm x 2 mm square and place it in an oxygen plasma etcher for 2 min at 50 W and 53.3 Pa.

8) At the end of the cycle, press a glass slide on the PDMS stamp to bond the two together. Place the glass slide and PDMS stamp back into the oxygen plasma etcher to undergo the same cycle. Remove the glass slide when the cycle has ended.

9) Using tweezers, carefully peel back the tape frame and pick-up the PPC film with the exfoliated crystal (Figure 4c) and place it on the PDMS stamp such that the desired flake is located on the stamp.

5) Transferring flakes from the top substrate to the bottom substrate using the PMMA-PVA method (Figure 3e-h).

1) Place a substrate on the bottom stage of the transfer setup. On this substrate, identify the position of the desired flake. This flake will be the "bottom" crystal. Also, place the top substrate (the glass slide from step 3.1.9) into the top substrate holder of the transfer setup (Figure 3e).

2) Using a low-magnification objective (5x), bring the bottom substrate into focus and center the desired flake. Slowly lower the top substrate until it enters the

depth of field of the objective. Adjust the lateral position and the rotational alignment of the two flakes.

3) Employ a higher-magnification objective (50x) and continue to lower the top substrate while adjusting the flake alignment. Lower the top substrate until the top flake entirely contacts the bottom flake. Contact is noticeable by a sudden change of color.

4) Heat the bottom substrate to 75°C for better adhesion of PMMA to the bottom substrate. The PMMA will detach from the glass slide (Figure 3f).

5) Clean the bottom substrate following step 2.3 to remove the PMMA film (Figure 3g-h).

6) Transferring flakes from the top substrate to the bottom substrate using the stamping method (Figure 4d-f).

1) Place a substrate on the bottom stage of the transfer setup. On this substrate, identify the position of the desired flake. This flake will be the "bottom" crystal. Also, place the top substrate (the glass slide with PDMS from step 4.2.5–4.2.6) into the top substrate holder of the transfer setup (Figure 4d).

2) Heat the bottom substrate to 100°C then follow steps 5.2–5.4 to align and bring into contact the top crystal with the bottom flake (Figure 4e).

3) Once complete contact is made between the two flakes (Figure 4e), slowly raise the top substrate. This results in the drop-off of the top flake from the stamp to the bottom substrate (Figure 4f).

IV. REPRESENTATIVE RESULTS

To illustrate the outcomes and effectiveness of our procedure we present a sequence of angle-controlled stacks of rhenium disulfide (ReS_2) thin crystals. To emphasize that the described method can also be applied to atomically thin layers, we also exemplify the construction of two relatively twisted monolayers of molybdenum disulfide (MoS_2).

To demonstrate the angular alignment capabilities of the transfer setup we use rhenium disulfide (ReS_2). Because of its in-plane anisotropic lattice structure, this crystal mechan-

ically exfoliates as elongated bars with well-defined edges[23, 24]. This makes it a perfect candidate for the demonstration of angular alignment. Using the PDMS stamping method described in the protocol, we transferred a "top" ReS_2 crystal from the stamp onto a silicon substrate with previously exfoliated "bottom" ReS_2. Each time we aimed to align the edges at a specific angle. Employing the angular component of the transfer setup, the "top" ReS_2 flake was placed such that it would be twisted by the specific desired angle with respect to the already present "bottom" ReS_2.

Figure 5 shows an example of a transfer where a top flake of ReS_2 was placed on a bottom ReS_2 flake with an intended relative angle of 75°. The optical micrographs of the bottom and top crystals are shown in Figure 5a and Figure 5b respectively. Using the PDMS stamping method described in the protocol, a stack was fabricated and the resulting new crystal is shown in Figure 5c. Atomic force microscopy (AFM) was used to image the stack in Figure 5d; this demonstrates that the twist angle between the top and bottom flakes measured 74.6° ± 0.1° (mean ± SD). The error bar was calculated from the uncertainty in precisely defining the edges of the ReS_2 in the micrographs. To further display the angular precision of the transfer setup we repeated this process for several other samples with intended relative angles ranging from 15° to 90° in increments of 15° (Figure 6).

Using the PMMA-PVA procedure as described in the protocol, the transfer setup is successfully used to create a structure consisting of two monolayer flakes of molybdenum disulfide (MoS_2). The individual monolayers are exfoliated onto PMMA (Figure 7a) and Si/SiO_2 respectively (Figure 7b). Our transfer procedure results in the structure presented in the optical micrograph in Figure 7c. Its morphology is further characterized by atomic force microscopy, confirming the thickness and relative position of the stacked MoS_2 monolayer (Figure 7d).

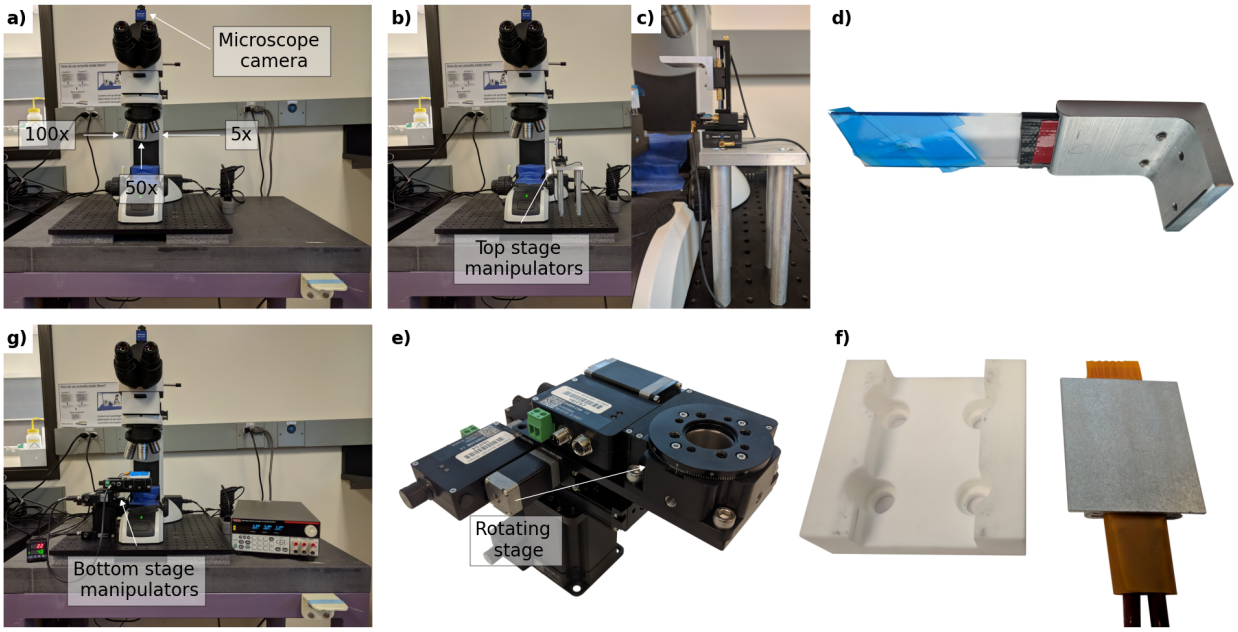

FIG. 1. **Components of the transfer setup.** (a) The optical microscope equipped with the camera and three long working distance objectives. (b) The microscope with the top manipulators which are capable of moving in the XYZ (translational) directions. (c) The top manipulators. (d) A custom machined arm which fastens to the top manipulators and is used to hold a glass slide (top sample). (e) The microscope with the bottom manipulators which can move in XYZ (translational) and θ (rotational). (f) The bottom manipulators. (g) A custom thermal insulating bottom stage holder (left) which is directly attached to the rotating stage. The temperature controlled flat heating element is shown on the right.

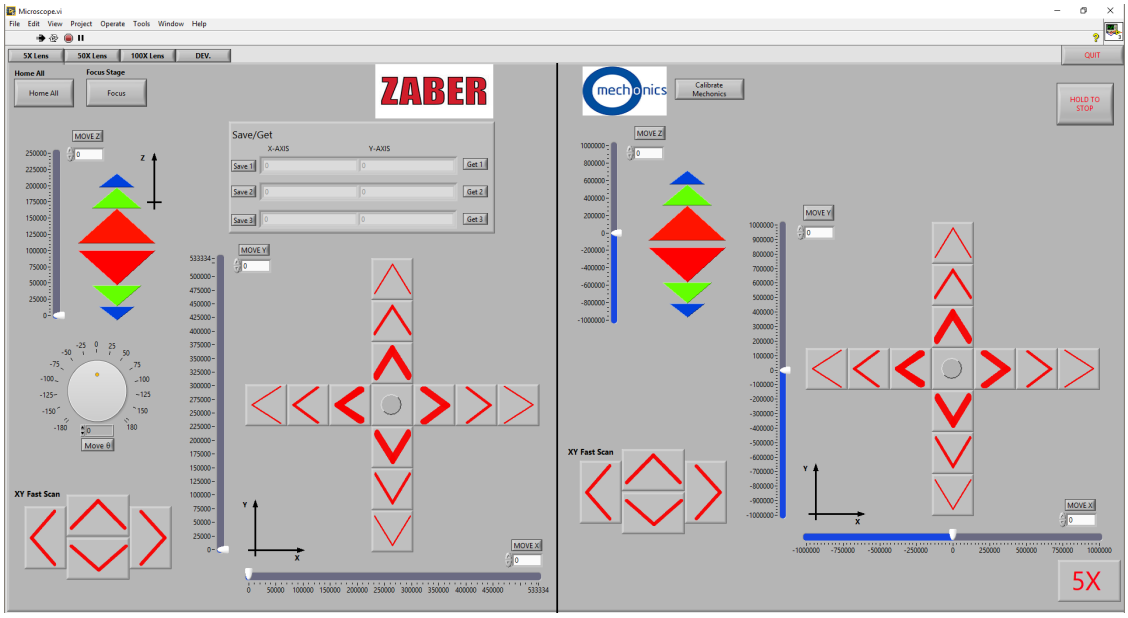

FIG. 2. **Instrumentation software front panel responsible for controlling the manipulators.** The front panel is divided into two sections; the left section controls the bottom stage whereas the right section controls the top manipulators. The user can move the manipulators individually or simultaneously, read out the position of each manipulator, save positions, adjust the speed of the manipulators, and automatically focus.

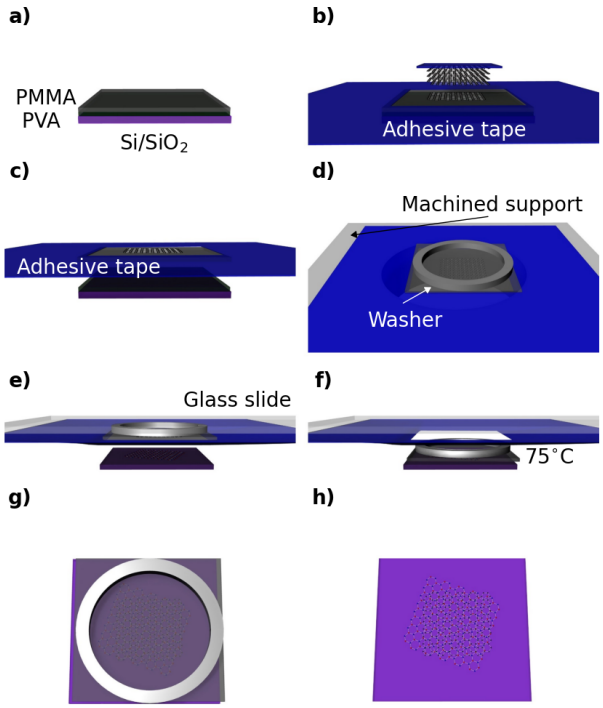

FIG. 3. **PMMA-PVA substrate preparation and transfer procedure.** (a) A bare Si/SiO2 substrate is first spin coated with PVA followed by PMMA. (b) A tape frame is placed on the substrate to hold down the polymer during mechanical exfoliation. (c) The tape frame is peeled back to pick-up the PMMA layer with the exfoliated crystal. (d) The tape frame is inverted and placed on a machined support followed by an inspection under an optical microscope. A washer is placed on the polymer film such that it surrounds the desired flake. (e) A glass slide is adhered to the tape frame and is placed into the top manipulator of the transfer setup. A previously prepared substrate with exfoliated crystal is placed on the bottom stage. (f) The top and bottom flakes are aligned and brought into contact. By heating the bottom stage to 75 °C, the PMMA detaches from the glass slide leaving (g) the top flake, the PMMA film and the washer on the bottom substrate. (h) The washer is removed and the PMMA is washed away resulting in a heterostructure.

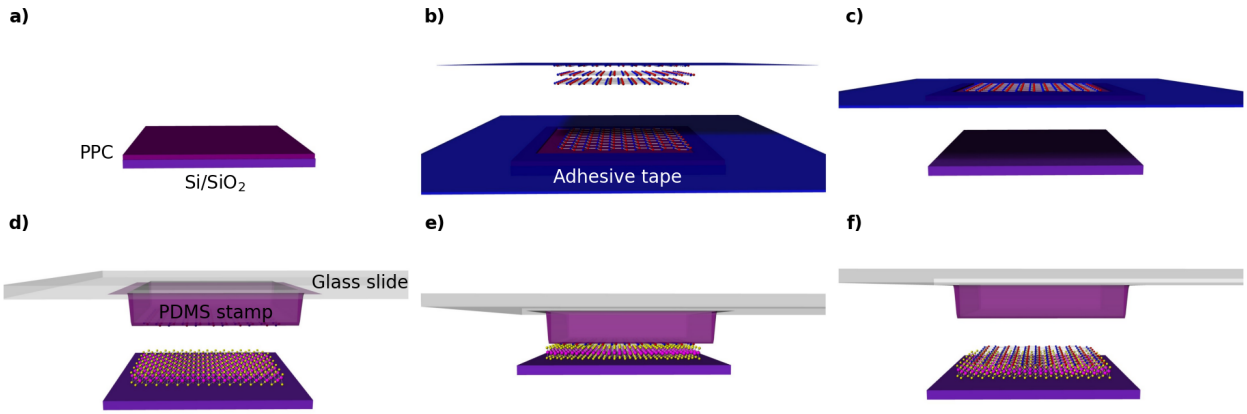

FIG. 4. **PDMS stamping preparation and transfer procedure.** (a) A bare Si/SiO2 substrate is spin coated with PPC. (b) A tape frame is placed on the substrate to hold down the polymer during mechanical exfoliation. (c) The tape frame is peeled back to pick-up the PPC layer with the exfoliated crystal. (d) The glass slide is placed into the top manipulator of the transfer setup. A previously prepared substrate with exfoliated crystal is placed on the bottom stage and heated to 100 °C. (e) The top and bottom flakes are aligned and brought into contact. (f) At 100 °C, we can slowly raise the top stage which results in the drop-off of the flake from the stamp to the bottom substrate.

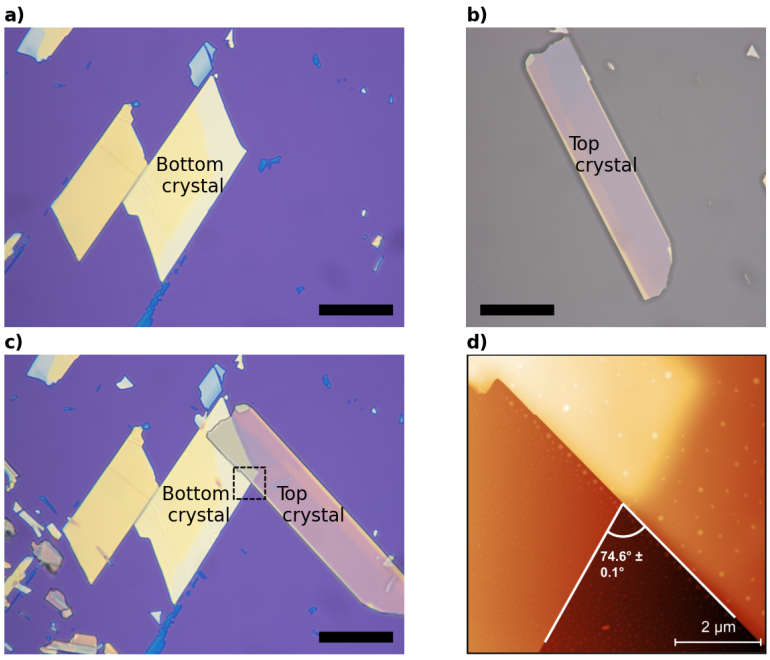

FIG. 5. **ReS_2 flakes transferred with a relative angle of 75°.** Optical micrographs of (a) a ReS_2 crystal mechanically exfoliated on a Si/SiO_2 substrate, (b) a ReS_2 crystal mechanically exfoliated on a Si/SiO_2/PPC substrate, (c) the resulting structure after transfer. (d) An AFM topographic map of the final structure corresponding to the boxed area in (c). The measured angle between the ReS_2 flakes is $74.6° \pm 0.1°$.

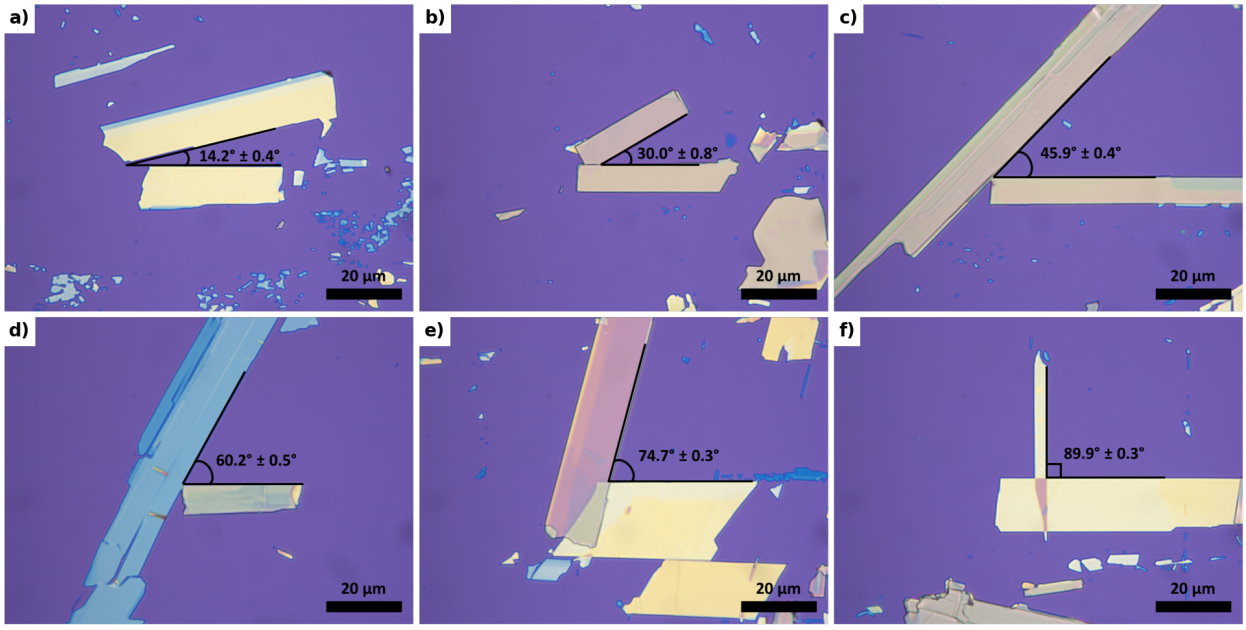

FIG. 6. **ReS_2 flakes transferred at specific relative angles.** ReS_2 flakes transferred at specific relative angles. (a-f) Optical micrographs of ReS_2 flakes transferred with the intention of forming angles ranging from 15° to 90° in increments of 15°.

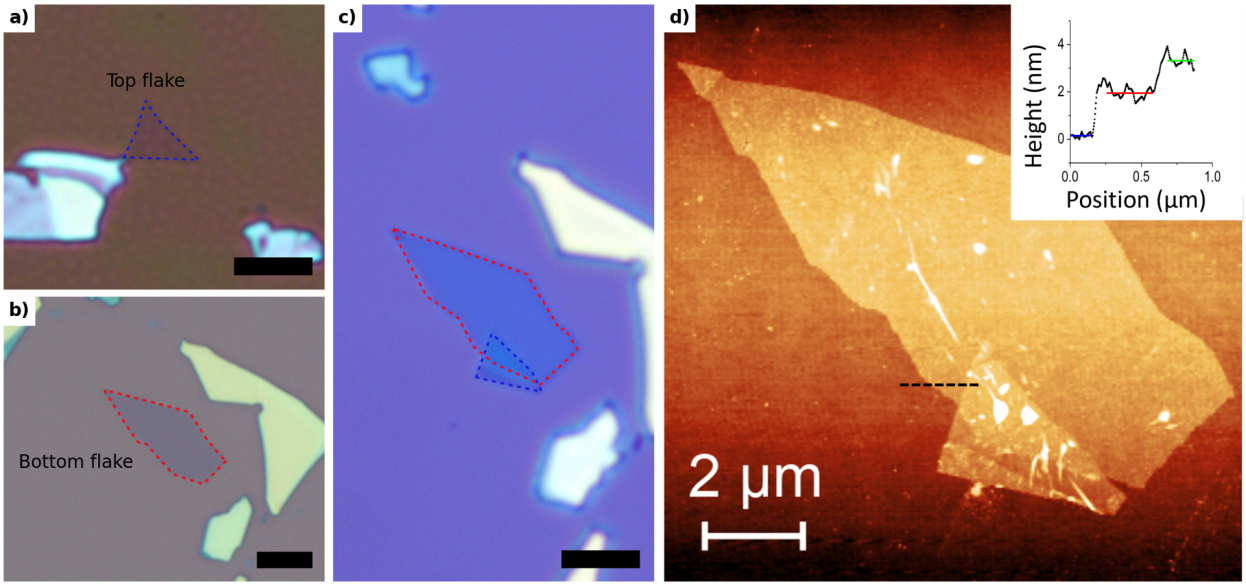

FIG. 7. **Twisted MoS_2 bilayer.** Optical micrographs of (a) the top MoS_2 flake on a PMMA film, (b) the bottom MoS_2 flake on a Si/SiO_2 substrate, (c) and the twisted MoS_2 structure. All scale bars in the optical images measure 5 μm. (d) AFM image of the twisted MoS_2 structure with a line profile (inset) along the direction indicated by the black dashed line.

V. DISCUSSION

The home-built transfer setup presented here offers a method for building novel layered materials with both lateral and rotational control. Compared to other solutions described in the literature[10, 25], our system does not require complex infrastructure, yet it achieves the goal of controlled alignment of 2D crystals.

The most critical step in the procedure is that of aligning and placing the top crystal in contact with the bottom one. Vibrations could be a cause for a failed alignment, therefore, one must minimize their effect. In this regard, the advantage of the "hands-free" set-up presented here is that the user does not risk introducing vibrations caused by the manual handling of the manipulators. Further improvements can be achieved by placing the set-up in an environment with lower vibrations or on a table equipped with vibration damping mechanisms.

As rotational alignment is becoming a more and more important parameter to consider

when creating van der Waals heterostructures, the rotational capability of this transfer setup is one of its strengths. The fact that the optical microscope is limited in resolving the edges of both crystals represents main the limitation in the alignment precision.

Not all 2D materials are inert in air. Crystals such as black phosphorus (BP)[26] or chromium triiodide (CrI_3)[27, 28] are known to degrade upon exposure to air. Therefore, to create heterostructures using these materials, and preserve the pristine interface, the transfer procedure would have to take place in an inert environment such as inside a glovebox. Because the transfer instrumentation presented here is "hands-free", it can be operated in a glovebox where these inert materials could be used.

Lastly, the stacking method presented here can have broader applicability and can be extended to situations when two crystals or a crystal and a substrate need to be precisely aligned laterally and rotationally.

VI. DISCLOSURES

The authors have nothing to disclose. The authors have no competing financial interests.

VII. ACKNOWLEDGMENTS

The authors acknowledge funding from University of Ottawa and NSERC Discovery grant RGPIN-2016-06717 and NSERC SPG QC2DM.

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2.1.2 Pick-up technique

In addition to the two fabrication techniques discussed in the above article, a third important technique should be highlighted, as it is the most often used to fabricate the devices presented in this thesis. This technique uses the same polymer stack as in the stamping method (PDMS/PPC) fixed to a glass slide but takes advantage of the temperature dependence of the adhesive properties of the PPC film to perform multiple sequential pick-up steps and a single drop-off. In more details (Figure 2.1), the glass slide with the polymer stamp is aligned with the desired exfoliated flake and slowly lowered until contact between the two is made (Figure 2.1a). The target substrate is kept at a temperature of 40°C, where the polymer is the most adhesive. The glass slide is then raised which results in the pick-up of the targeted flake (Figure 2.1c). This process can be repeated multiple times to sequentially pick-up additional flakes (Figure 2.1e-g). To perform the drop-off of the heterostructure, the substrate is heated to 80°C and the heterostructure is lowered until it contacts the target substrate (Figure 2.1i). At this point and temperature, the adhesion between the heterostructure and substrate is stronger than that of the heterostructure and polymer, therefore, the glass slide can be raised and the heterostructure will be dropped-off (Figure 2.1k).

2.2 Sample cleaning

All the transfer techniques discussed above have one similarity: they all use polymers to support the flakes to be transferred. Although the polymer is a necessity, it also leaves residues behind on the flakes which can limit the device performance and lead to high contact resistances. Furthermore, during the process of stacking two flakes together, it

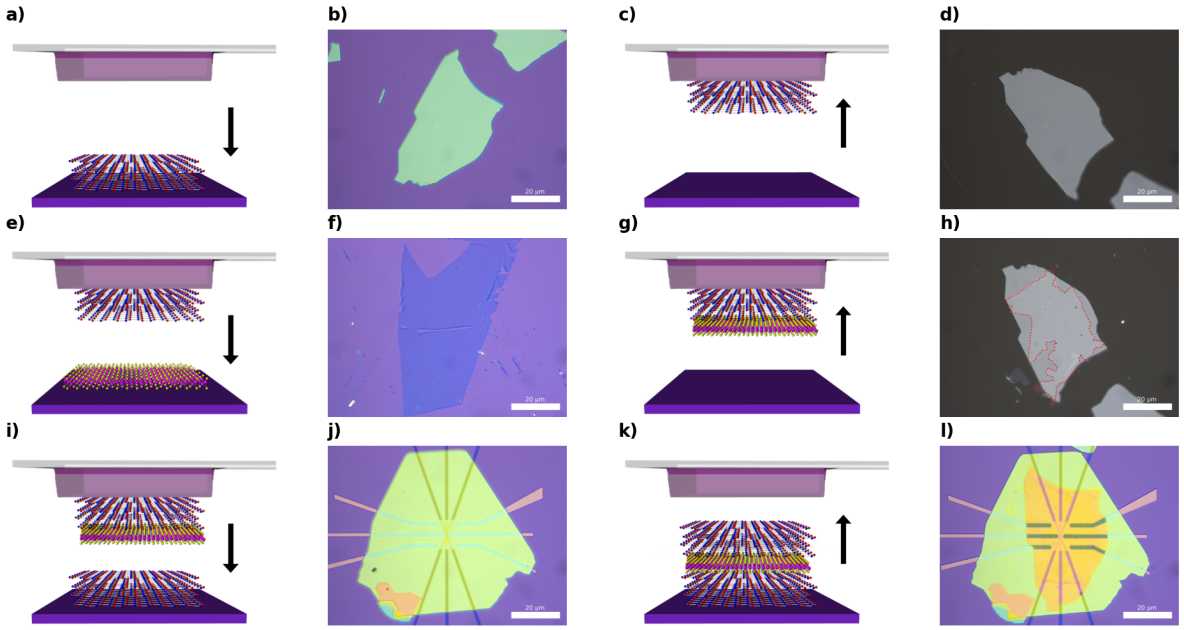

Figure 2.1: Illustrations and optical micrographs of the pick-up stacking technique. (a) The polymer stack is brought into contact with the targeted flake (b) at a temperature of 40°C. (c) The glass slide is raised and the flake is picked-up by the polymer (d). (e-f) The process can be repeated to pick-up an additional flake. The picked-up flake from (f) is outlined by a red dotted line in (h). (i-l) By maintaining the final substrate at a temperature of 80°C, the heterostructure can be dropped off from the polymer and onto the targeted structure.

is common to trap environmental contaminants at the interface of the two flakes. These contaminants form bubbles at the interface (Figure 2.2a) which can alter the electrical and optical properties of the 2D materials through strain [61–63], and can also create a non-uniform electrical environment to which the charge carriers are sensitive. Uniformity and cleanliness are key to obtaining high performance devices, therefore it is ideal to eliminate any formed interfacial bubbles and to completely remove any contaminants that may have accumulated on the surface of our flakes.

Solvents such as acetone and chloroform can be used to remove most of the polymer

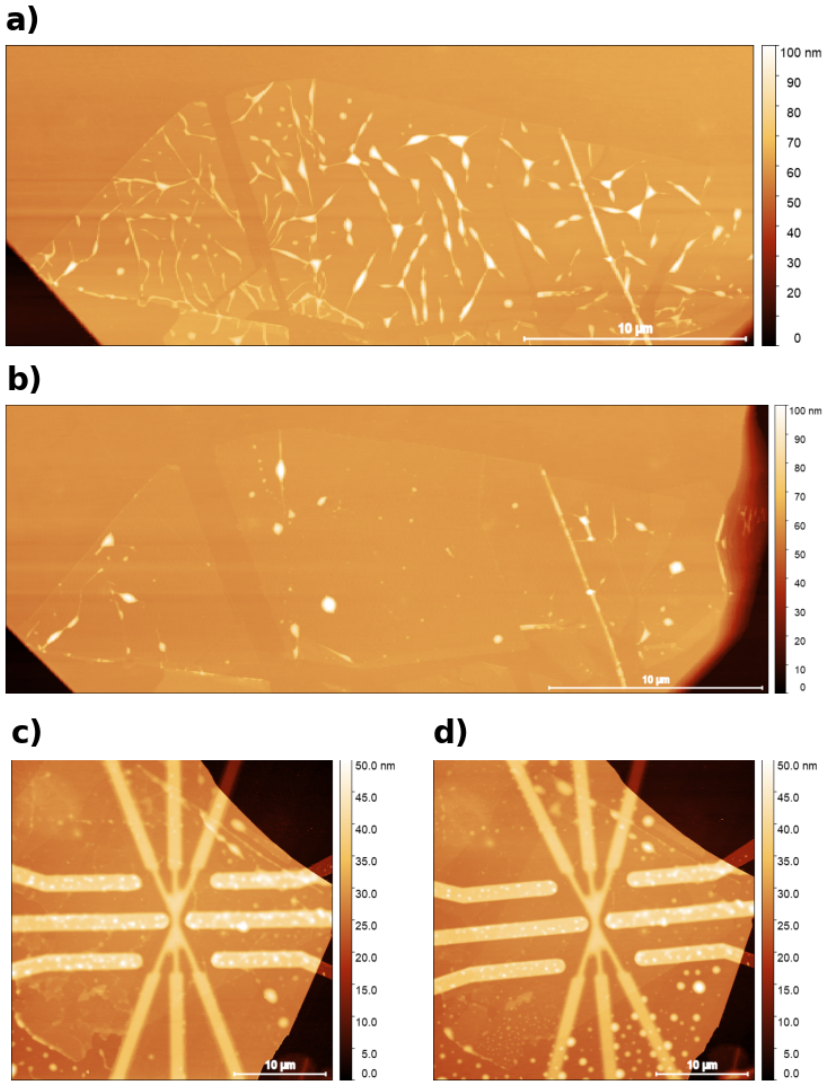

Figure 2.2: (a) AFM topography image of monolayer MoS_2 transferred onto bulk hBN showing the multiple bubbles formed at the interface of the two materials. (b) AFM topography image of the same sample as in (a) after having gone through a furnace cleaning using the tube furnace. More specifically, the sample was cleaned using a standard recipe of 8 hours at 250°C with a Ar/H_2 flow of 60 ccm. The number of bubbles is visibly reduced. (c) AFM topography image of a multilayered heterostructure with bubbles at the various interfaces and polymer at the surface. (d) AFM topography image of the same sample as in (c) after having gone through a furnace cleaning using the vacuum furnace (300°C for 30 minutes). The surface polymer and interfacial bubbles are noticeably reduced.

contamination from the surface of the flakes however, small but non-negligible quantities often remain. Throughout this thesis, we have studied the effect of additional cleaning methods for removing both polymers and interfacial bubbles. A first technique involves heating the sample in a controlled environment, either under vacuum or in a quartz tube furnace while flowing forming gas (argon-hydrogen mixture [5% H_2, 95% Ar]). By heating the sample in the range of 300°C, residual polymer is boiled off the surface of the sample, and large areas free of bubbles are formed due to the grouping effect (Figure 2.2). A second technique uses an atomic force microscope (AFM) tip to mechanically sweep any polymer gathered on the surface of the sample and to push away the interfacial bubbles leading to a flattened and cleaned area [64, 65]. The effectiveness of this technique can be seen in Figure 2.3 where it was used to clean monolayer MoS_2 that has been transferred on top of hBN. As a result of the transfer, there are multiple bubbles at the interface of the two-dimensional materials and polymer on the surface (Figure 2.3a). The AFM tip was brought into contact with the surface and multiple 2 μm X 2 μm squares were scanned at various forces to demonstrate this cleaning technique (Figure 2.3b-c). At low forces (49 – 88.2 nN), the polymer is successfully "broomed" to the perimeter of the scan area. At higher forces ($\leq$ 88.2 nN), both the polymer and the bubbles are cleaned away. Appendix B.3 presents a complete AFM brooming protocol.

A final technique uses a focused laser to locally heat and clean samples. This is the subject of the following letter.[2]

[2] **J. Boddison-Chouinard**, S. Scarfe, K. Watanabe, T. Taniguchi, and A. Luican-Mayer. Flattening van der Waals heterostructures interfaces by local thermal treatment. *Applied Physics Letters*, 115, 2019

2.2.1 Flattening van der Waals heterostructure interfaces by local thermal treatment

Statement of contributions

JBC and ALM developed the idea for the work presented in this letter. JBC and Samantha Scarfe (SS) conducted the experiments, analyzed the data, and wrote the first draft of the manuscript which was then completed with ALM. Kenji Watanabe (KW) and Takashi Taniguchi (TT) grew and provided the hexagonal boron nitride.

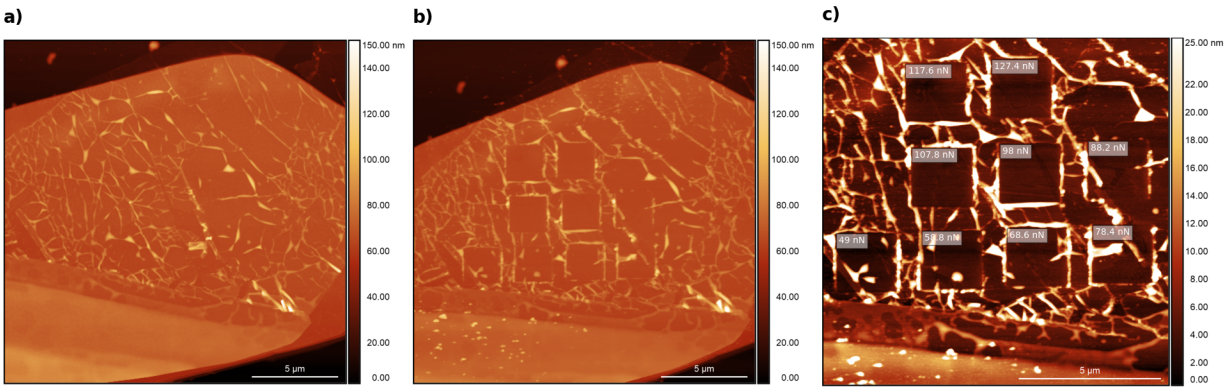

Figure 2.3: (a) AFM topography image of monolayer MoS_2 transferred onto bulk hBN showing the multiple bubbles formed at the interface of the two materials. (b) AFM topography image of the same sample as in (a) after having been cleaned using a separate AFM tip in contact mode. Individual square areas were cleaned using different contact forces as specified in the high-resolution AFM image (c).

Flattening van der Waals heterostructure interfaces by local thermal treatment

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Fabrication of custom-built heterostructures based on stacked 2D materials provides an effective method to controllably tune electronic and optical properties. To that end, optimizing fabrication techniques for building these heterostructures is imperative. A common challenge in layer-by-layer assembly of 2D materials is the formation of bubbles at atomically thin interfaces. We propose a technique for addressing this issue by removing the bubbles formed at the heterostructure interface in a custom-defined area using the heat generated by a laser equipped with raster scanning capabilities. We demonstrate that the density of bubbles formed at graphene-ReS2 interfaces can be controllably reduced using this method. We discuss an understanding of the flattening mechanism by considering the interplay of interface thermal conductivities and adhesion energies between two atomically thin 2D materials.

The ability to design and synthesize high-quality materials with minimal contamination and low defect density has historically resulted in scientific and technological breakthroughs. The family of layered van der Waals 2D crystals represents a promising platform for developing new classes of custom-tailored materials[1]. It comprises a wide range of electronic

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properties such as insulating (hBN), semiconducting (MoS_2 and WS_2), and metallic transitioning into correlated states of matter when cooled down: charge density order (1T-TaS_2 and $TiSe_2$) or superconductivity ($NbSe_2$ and 1H-TaS_2)[2]. The ability to controllably stack their atomically thin layers can lead to the realization of original materials with properties previously inaccessible[3]. Experimentally, a key step in achieving this goal is to ensure pristine interfaces between layers. One of the typical difficulties in layer-by-layer assembly of 2D materials is the formation of bubbles at the atomically thin interfaces, which introduce inhomogeneities in the device's electronic properties[4–8].

van der Waals heterostructures are commonly assembled by a variety of dry mechanical stacking techniques[9, 10]. Such methods generally involve bringing a bottom-2D material into contact with a stamp supporting a top-2D material, and frequently, environmental contaminants are trapped at the interface during this process. These environmental contaminants aggregate into inhomogeneously distributed blisters (or "bubbles") which are hundreds of nanometers wide and tens of nanometers tall, as schematically shown in Fig. 1(a).

Bubbles have been observed to be not only a result of the dry stamping method but also after irradiation with proton beams or chemical etching processes[11]. These bubbles have been extensively studied ranging from proposals on how to minimize their formation[4, 9, 12–15] to addressing their content and shape/size distribution[16–21]. The atomic force microscopy (AFM) topograph in Fig. 1(b) shows the surface morphology of a MoS_2/BN heterostructure[10] with bubbles formed at the interface as indicated. These types of nanoblister shapes are similar to those commonly reported in the literature[17, 22]. We observe that these blisters are interconnected by narrow channels, suggesting that the trapped contaminants might be able to traverse the sample through pressure or heat gradients[11]. While there is no firm consensus on the contents of these bubbles, they are widely believed to be trapped hydrocarbons from air contaminants present in ambient lab conditions[5] or water[4, 5, 17, 18, 21]. It was found that from the aspect ratio of the bubbles, one can infer the adhesion energy of a specific interface[17, 18, 20, 21]. In Fig. 1(c), we plot the variation in aspect ratios for different heterostructures that we measured, in good agreement with those measured across the literature[5, 18, 23–25].

Although an interesting playground for studying the elastic properties of atomically thin

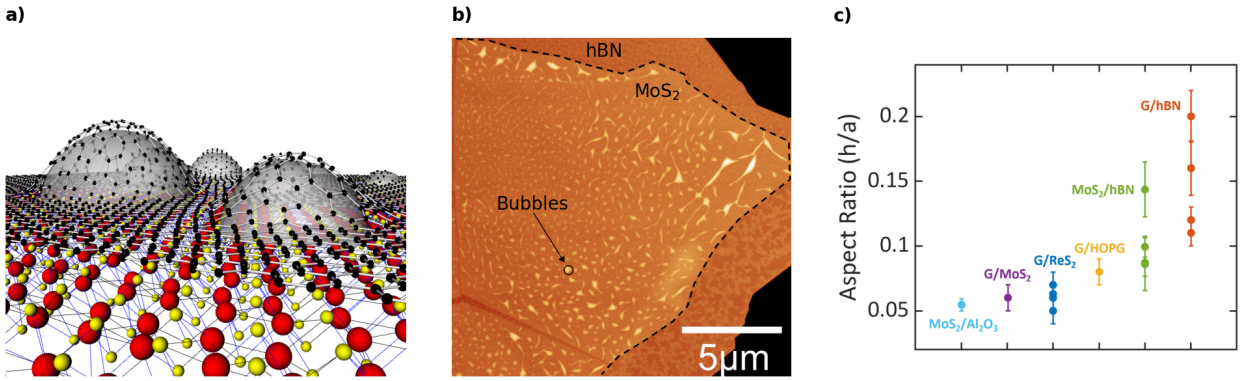

FIG. 1. (a) Visual representation of interface contaminants trapped between a graphene film and a transition metal dichalcogenide substrate. (b) Atomic force microscope image of MoS_2 supported by an hBN substrate. Bubbles are indicated by the arrow. (c) Aspect ratio of the measured bubbles formed at the interface of different 2D material stacks.

membranes[17], from a practical perspective, the blisters represent an issue for the device community as they introduce charge inhomogeneities[6] that significantly degrade device performance. Currently, techniques used to eliminate bubbles from heterostructures are preventive (careful transfer), nontargeted (thermal treatments), or invasive (pushing the bubbles with an AFM tip in contact mode). Preventive techniques involve slowly laminating the heterostructure at a raised temperature[9]. A common non-targeted technique involves heating the entire sample in a controlled environment at 200°C−300°C[7, 12];

this leads to an increased amount of flattened regions as bubbles diffuse under temperature gradients. The drawback of this approach is that it cannot be used when parts of a device might contain crystals that change their structure or are unstable upon heating. Another method relies on the force of an AFM tip to mechanically push bubbles and ultimately flatten the film[15]. Therefore, a targeted and noninvasive technique that addresses the presence of bubbles at the interface of 2D materials is still missing.

Here, we present a method that achieves targeted and noninvasive manipulation of bubbles at 2D heterostructure interfaces. By using a localized heat treatment through laser exposure, we combine the diffusive, non-contact nature of a thermal treatment with the targeted and spatially resolved capabilities of a local probe.

Our method makes use of a 532 nm CW laser with raster scanning capabilities to systematically flatten out 2D heterostructures. Using a Horiba XPlora Plus Raman microscope

setup, we use a 100X objective to focus the laser spot to 0.5 μm and define a path for the laser to collect Raman spectra, collecting a Raman map of a desired heterostructure. We illustrate the use of this method for a heterostructure having a graphene film supported by a thick (30–100 nm) ReS_2 substrate. Figures 2(a) and 2(b) show the AFM topographic images of a graphene/ReS_2 stack before and after laser exposure, respectively. While initially we obtained a dense amount of small bubbles (average height of 15 nm), after laser exposure the bubbles are more sparsely distributed and taller (average height of 80 nm). This is demonstrated by the height histogram of the graphene flake before and after exposure presented in Fig. 2(c).We notice that after laser exposure, the distribution of heights shifts toward 0 nm, indicating an increase in flattened regions. At the opposite end, the presence of few tall bubbles is only seen in the flake after exposure. The similarities with thermal treatments indicate that the most probable driving mechanism is the diffusivity of the bubble contents through heat[11].

We propose the following process: the laser power provides kinetic energy to the bubble content, partly dissipated through the substrate and partly dissipated laterally; the remainder will work against the film-substrate adhesion energy as illustrated in Fig. 2(d). Importantly, when the adhesion energy is overcome, the bubble content will be allowed to migrate, leaving behind areas of flat graphene.

By estimating how much energy is needed for the bubble contents to overcome the adhesion energy of a particular heterostructure, we can obtain a minimum temperature for bubble migration as described below.

The adhesion energy per unit area is given by[18] $\frac{6E_{2D}h^4}{5a^4} + \gamma_w(\cos\theta_t + \cos\theta_b)$, where E_{2D} is the in-plane elastic stiffness of the top film ($E_{2D}^{graphene} = 340$ Nm^{-1})[18], h is the height of the bubble, a is the bubble radius, γ_w is the surface tension of water (≈ 0.072 J/m^2), θ_t and θ_b are the water contact angles of the top crystal and bottom crystal, respectively.

We consider the kinetic energy delivered to bubble contents $K_{bubble} = \frac{3}{2}k_BTN$, where k_B is the Boltzmann constant, T is the temperature in the bubble, and N is the number of molecules. We assume the contents to be water molecules[18], and we approximate the bubble shape as a spherical cap.

Now, we equate $E_{adhesion}$ to K_{bubble} to calculate the minimum bubble migration temperature,

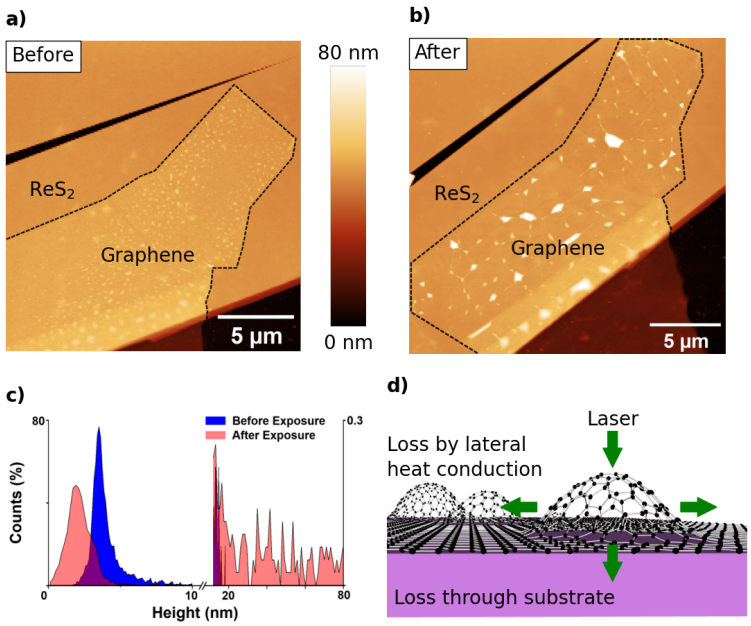

FIG. 2. (a) AFM topograph of a graphene flake transferred on a ReS_2 substrate. (b) AFM of the same graphene flake in (a) after exposure to a rastering laser at 8.7 mW. (c) Histogram of AFM pixel heights before and after laser exposure. (d) Schematic of the flattening mechanism—interplay of heat loss and surface adhesion.

$$T = \frac{4(d^2 - \pi a^2)}{k_B \rho \pi h (3a^2 + h^2)} \left(\frac{6 E_{2D} h^4}{5a^4} + \gamma_w (\cos\theta_{graphene} + \cos\theta_{ReS_2}) \right)$$

Using AFM scans of graphene on ReS_2, we extract an average value for the bubble geometric parameters: $a = 74 \pm 2$ nm, $h = 6 \pm 1$ nm, and $d = 500 \pm 100$ nm. For the water contact angles, we use $\theta_{graphene} = 64°$[18] and $\theta_{ReS_2} = 60°$. We consider the water contact angle for ReS_2 similar to that for other 2D materials[26, 27]. Finally, we obtain the minimum migration temperature $T = 157°$C. This is consistent with measurements we performed by thermally annealing graphene/ReS_2 in a furnace.

To relate the laser power, the temperature in the bubble, and the interface thermal conductance, we solved the steady state heat equation, following the procedures used in Refs[28–32]. By equating this value with the minimum migration temperature obtained above, we extract the interface thermal conductance for graphene on ReS_2 to be $g = 0.725$ MW/(m^{2}K), a parameter that has not been reported thus far. We note that the value of

interface thermal conductance varies depending on the 2D layers forming the interface.While the literature has still large variations for this parameter in 2D heterostructures, the value we found is close to the reported experimental values for interfaces of MoS_2 with Au[33] and smaller than those calculated for MoS_2 and SiO_2[34, 35] or graphene/BN[36]. This suggests that stronger adhesion leads to better heat conduction at interfaces.

The importance of reaching the minimum migration temperature is experimentally demonstrated in Fig. 3, where it is apparent that a minimum laser power is required for flattening the graphene flake. A graphene/ReS_2 heterostructure [Fig. 3(a)] is exposed to the laser at a power of 4.35 mW. According to our model, this corresponds to a bubble content temperature of 120°C, below the minimum migration temperature for this heterostructure. The result is presented in the AFM image of Fig. 3(b), showing no change in the bubble distribution. We then increase the power to 8.7 mW(corresponding to 215°C), and as seen in Fig. 3(c), we obtain larger regions of flat graphene. We note that we do not find the graphene to be damaged by this process, as verified by Raman spectroscopy [Fig. 3(d)], which does not indicate the presence of a defect feature or changes in the typical graphene peaks.

While for a given adhesion energy, one needs an adequately high laser power to overcome it, the same laser power might not be sufficient for an interface with a higher adhesion energy. To demonstrate that, we consider a graphene/BN

interface. As inferred from the aspect ratio of bubbles created at this interface [Ref.[18] and Fig. 1(c)], the adhesion energy is larger and thus corresponds to a larger minimum migration temperature. In Figs. 4(a) and 4(b), we show the results obtained when we applied our method to a heterostructure having graphene supported by a thick (30–100 nm) BN substrate. We expose these structures to identical laser rastering paths as the graphene on ReS_2 samples and observe that for the same laser power, there is no bubble migration or coalescence. This finding is consistent with our model, as the adhesion energy at the graphene/hBN interface is larger than that at the graphene/ ReS_2 interface ($E_{adhesion\ G/hBN} = 126$ mJ/m^2); at the same time, the losses to the substrate are larger, as the thermal conductance of graphene on hBN[36] ($g = 52.2$ MW/m^{2}K) is greater than that in the ReS_2 case. Using the model described above and the typical geometric parameters we obtained for bubbles at the graphene/hBN interface, we estimate that flattening graphene

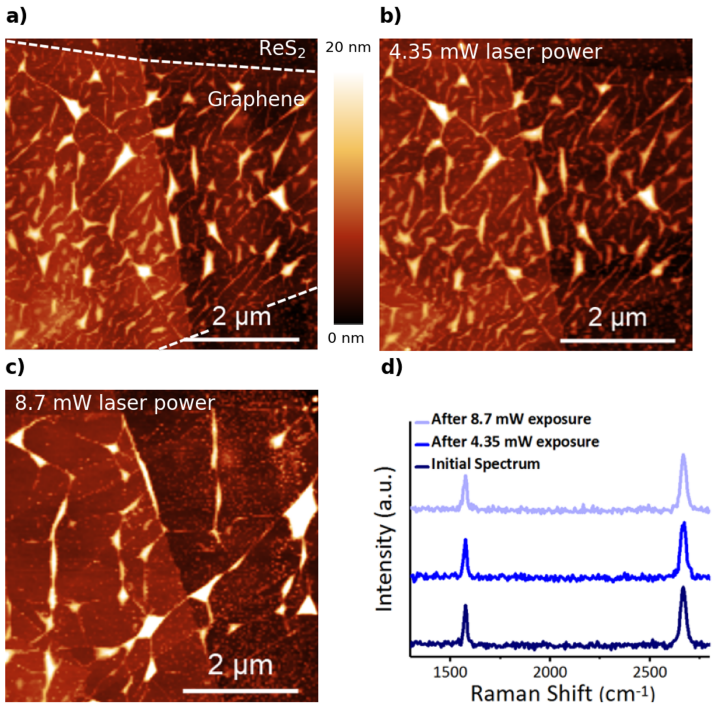

FIG. 3. Flattening requires sufficient laser power heating. (a) AFM of a graphene flake supported by a ReS_2 substrate. (b) AFM of the same graphene flake after laser exposure at 4.35 mW, indicating no bubble diffusion or morphological change. (c) AFM of the same graphene flake after laser exposure at 8.7 mW, demonstrating that ≈8 mW is required to diffuse the transfer bubbles. (d) Post-exposure spectra showing no defect activated Raman peak.

on hBN requires temperatures of $T \approx 324^\circ$ C, consistent with the values used for thermal annealing.

A great strength of the method we propose here is offering an alternative for a situation when the entire sample cannot be exposed to heat. Using the technique of localized thermal laser treatment, it is possible to flatten out specific and targeted sections of graphene supported by ReS_2 substrates by programming the laser path to only cover the desired spots. This feature is demonstrated in Fig. 4(b) where two graphene flakes are placed on a ReS_2 substrate. We indicate the target area, and as shown by the zoom-in topographs on the right side of Fig. 4(b), we will only flatten the graphene flake in the desired region (black box) and not on the different flake (blue box).

In conclusion, we present a method for eliminating bubbles at 2D material interfaces based on localized thermal laser treatment. We discuss its range of applicability based

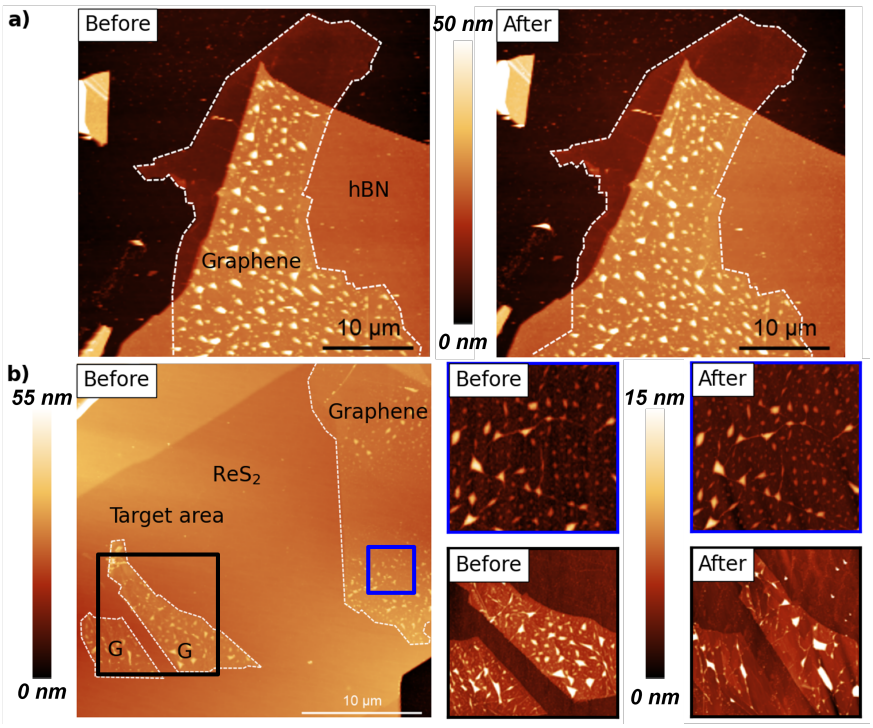

FIG. 4. (a) AFM of a graphene flake supported by hBN before and after an 8.7 mW laser exposure. (b) AFM of separated graphene flakes supported by the same ReS_2 substrate before and after exposure to the target area at 6 mW. A high resolution AFM topograph of the targeted flake (black box) shows substantial flattening, whereas the unexposed flake (blue box) demonstrates no bubble changes.

on a model that considers the balance of heat loss at the interface and adhesion energy. By exemplifying its application to a graphene/ReS_2 interface, we were also able to extract the interface thermal conductance for this system $g = 0.725$ MW/(m^{2}K). The demonstrated control over the section to be flattened offers a great advantage for optimizing custom device fabrication.

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2.3 Electrical contacts to 2D materials

The bulk of this thesis discusses various transport experiments performed on semiconducting transition metal dichalcogenides, and in order to conduct these experiments, electrical contacts must be made to the TMD. Properly contacting semiconducting TMDs is particularly difficult to accomplish due to the surface of the material lacking the ability to form covalent bonds with the contacting 3D metal [50]. The contacting mechanism between the TMD and the metal is therefore formed by a weak van der Waals bond which results in a tunneling barrier for carriers, in addition to the Schottky barrier [50, 66, 67].

In order to minimize any additional tunneling barrier between the metal and the TMD caused by interfacial impurities, various cleaning techniques and contact architectures were studied. To evaluate the effectiveness of these cleaning techniques and contact architectures, two-point electrical measurements were performed on the completed devices and the total electrical resistance was measured for various charge carrier densities. These resistances are plotted in Figure 2.4. Although the two-point resistance includes both the contact resistance (R_C) and the channel resistance (R_{ch}), the channel remained fairly constant throughout the device iterations. This means that for a particular carrier density, the channel resistance for each device should be comparable and the differences noted in Figure 2.4 are mostly attributable to the contact resistance. We now discuss the fabrication processes that were studied and are presented in Figure 2.4.

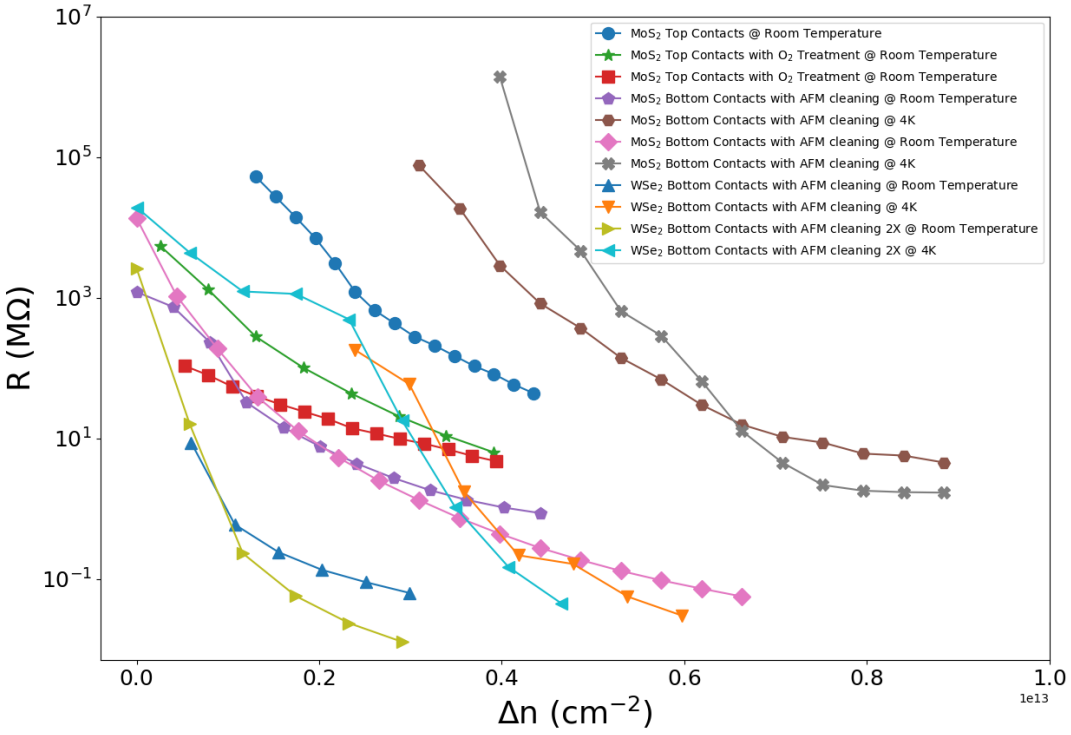

Figure 2.4: Total 2-point resistance as a function of the change of carrier density (accumulation gate voltage) for various cleaning recipes and contact architectures. Blue circles are measurements taken at room temperature of a monolayer MoS_2 flake contacted using the top contact architecture. Green stars and red squares are measurements taken at room temperature of MoS_2 flakes contacted using the top contact architecture with an additional oxygen plasma cleaning prior to the deposition of the metallic contacts. Purple pentagons and pink diamonds represent the measurements taken on MoS_2 flakes contacted from the bottom at room temperature. Prior to the placement of the MoS_2 flakes onto the contacts, the contacts were cleaned using the AFM brooming technique. Grey 'X's and brown hexagons are electrical measurements taken at 4 K of the same two devices represented by the purple pentagons and pink diamonds. Blue (orange) triangles are measurements taken at room temperature (4 K) of monolayer WSe_2 devices prepared in the same way as the previous two MoS_2 devices. Yellow (cyan) triangles represent the electrical measurements taken at room temperature (4 K) of monolayer WSe_2 where the contacts and the WSe_2 flake were cleaned following the AFM brooming technique directly before assembly.

2.3.1 Top contacts

The most straight forward method for contacting the 2D material is by defining the contact pattern directly on top of the TMD using standard electron beam lithography procedures and by filling the pattern with the contacting metal resulting in "top contacts" (2.5a). In this approach, a selective solvent is used to reveal the defined pattern in the electron beam resist mask, however, it is common that some residual resist remains on the surface which leads to an increased contact resistance. In the attempt to remove this residual polymer, we followed a standard approach known as "descumming" where we introduce the sample to a light oxygen plasma (30 seconds at 50 W). Samples that were cleaned using this treatment showed a total resistance that was a full order of magnitude less than samples that were not introduced to an oxygen plasma as indicated by the green stars and red squares in Figure 2.4. Although the use of an oxygen plasma to remove residual polymer has proven to decrease the total resistance of the device, the quality of the TMD layer under the contacts may have been compromised which can be the cause of the slightly lower yet relatively large contact resistance.

2.3.2 Bottom contacts

An alternative method for contacting the TMD flake is from the bottom, where the TMD flake is placed on pre-deposited metallic contacts (Figure 2.5b). Using this contact architecture, we can ensure that the contacts are absolutely clean before depositing the TMD flake. With a focus on clean contacts, an AFM tip in contact mode was scanned directly on the contacts, resulting in the "brooming" of any impurity that may have gathered on their surfaces (Figure 2.5 c-d). The resulting resistances for three different devices that were fabricated using this contact architecture and cleaning technique are

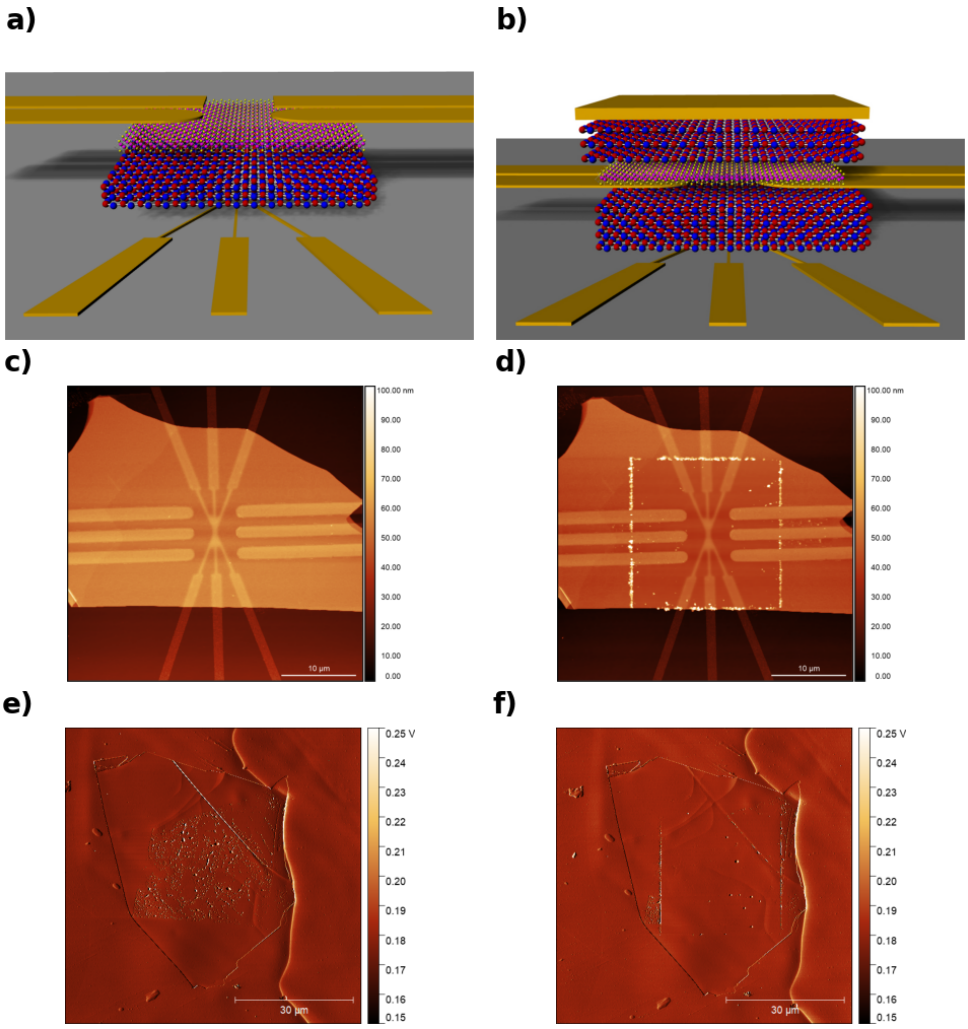

Figure 2.5: (a) Schematic of the top contact architecture where the metallic electrical contacts touch the top surface of the TMD flake. (b) Schematic of the bottom contact architecture where the metallic electrical contacts touch the bottom surface of the TMD flake. (c) AFM topography image of the electrical contacts on a flake of hBN. (d) AFM topography image of the same electrical contacts as in (c) on a flake of hBN after AFM brooming where surface residues have visibly gathered to the perimeter of the scan area. (e) AFM peak force signal of WSe_2 on a flake of hBN supported by a PDMS stamp. (f) AFM peak force signal of the same WSe_2/hBN heterostructure as in (e) after AFM brooming where surface residues and interfacial bubbles have visibly gathered to the perimeter of the scan area.

presented in Figure 2.4. Comparing MoS_2 based devices fabricated following this architecture (purple pentagons and pink diamonds) to the best top contacted MoS_2 based device (red square), we see the resistance decrease by a factor of 5-10. Furthermore, this technique has led to contact resistances that remain low enough such that we can measure these devices at low temperatures (see the brown hexagons, grey crosses, and the orange triangles in Figure 2.4), a task that was unachievable using the top contact method.

The interface cleanliness between the contacting metal and the semiconducting TMD can be further optimized by cleaning the surface of the TMD flake prior to its transfer onto the contacts. This is once again achieved using the AFM "brooming" technique as demonstrated in Figure 2.5 e-f. In Figure 2.4, we compare this technique (yellow and cyan triangles) to the case where the TMD flake is not pre-cleaned (blue and orange triangles) and we once again observe an improvement in contact resistance at room temperature and at 4 K.

2.4 Conclusion

Careful attention to sample fabrication and cleanliness must be taken in order to properly contact TMD monolayers. In this chapter, we presented a fabrication procedure which leads to ohmic contacts with ultra low contact resistances even at low temperatures, a necessity for observing quantum transport phenomena. In the following chapters, we present the observed quantum phenomena resulting from the electrical transport measurements performed on monolayer TMD samples fabricated using this procedure.

Chapter 3

Gate-controlled quantum dots in monolayer transition metal dichalcogenides

Monolayer semiconducting transition metal dichalcogenides like MoS_2 and WSe_2 are promising candidates for hosting spin qubits due to their expected long coherence times [68], and the prospect of addressing the spin qubits optically [32]. The first step towards achieving a spin qubit in these materials is to create quantum dots that are fully controllable.

The basic principle for creating nanostructures such as quantum dots in TMD materials relies on electrostatic gating. Just like opposite charges can accumulate on the two faces of a parallel plate capacitor by applying a potential difference between the two plates, metallic structures (called gates) can be used to control the charge carrier density in the TMD sheet. These gates are placed in a plane parallel to the TMD sheet and separated by a dielectric. One can imagine that these gates cast a shadow on the TMD flake where that

shadow's carrier concentration can be tuned by applying a potential difference between the gate and the TMD. Therefore, small electrostatic gates can be used to selectively deplete regions of the TMD sheet and define nanostructures where the transport is now affected by quantum effects. The geometry of these gates can be designed such that the carriers can be confined to a 0-dimensional (0D) region, known as a quantum dot.

3.1 Transport through a quantum dot

To understand the phenomena associated with transport through a quantum dot, we can consider the circuit where the quantum dot contains a charge Q at a voltage V and is tunnel coupled to two charge carrier reservoirs called source (V_S) and drain (V_D). Furthermore, the quantum dot is capacitively coupled to a gate with an applied potential V_G. The value of capacitance between the charge reservoirs and the quantum dot are labelled C_S for the source and C_D for the drain. Similarly, the capacitance between the gate electrode and the quantum dot is labelled as C_G. The charge of the quantum dot can be calculated by considering the charge contributions from each element:

$$Q_{QD} = qN = \sum_{i=1} C_i \Delta V_i = \sum_{i=1} C_i (V - V_i)$$

where N is the number of charges q (holes or electrons) that occupy the quantum dot. This expression can be evaluated for the three electrical elements in the circuit where we obtain:

$$Q_{QD} = qN = C_G(V - V_G) + C_S(V - V_S) + C_D(V - V_D)$$

From this expression, we can solve for CV, with $C = C_G + C_S + C_D$ being the capacitance of the dot, and calculate the electrostatic energy of the quantum dot [69].

$$E_{QD} = \frac{1}{2}CV^2 = \frac{(CV)^2}{2C} = \frac{(C_G V_G + C_S V_S + C_D V_D - qN)^2}{2C}$$

When transport measurements are operated in the low source-drain bias regime, we can ignore the terms containing V_S and V_D which leads to:

$$E_{QD} = \frac{(C_G V_G - qN)^2}{2C} \tag{3.1}$$

From this equation, we directly see that the energy is quadratic in gate voltage V_G. The energy is plotted in Figure 3.1a as a function of V_G and for various values of N, where we see that adjacent parabolas intersect at $E(N) = E(N \pm 1)$. Therefore, as the gate voltage is changed, the quantum dot will either lower or increase its occupancy to minimize its total energy. These intersections are in fact at the heart of the phenomenon known as Coulomb Blockade (Figure 3.1b) where current can flow between the two reservoirs strictly under specific conditions.

It is important to note that the confinement potential that leads to the quantization of the number of charges also produces a discrete energy spectrum, similar to an atom, which needs to be considered in the expression for the total energy. Taking these energy levels (E_i) into account, the total energy of the quantum dot is given by [28, 70]

$$E_{QD} = \frac{(C_G V_G + C_S V_S + C_D V_D - qN)^2}{2C} + \sum_{i=1}^{N} E_i$$

To discuss the transport conditions related to the Coulomb Blockade phenomenon, let's first introduce the electrochemical potential of the quantum dot which is the energy associated

with the addition of the N^{th} charge to the quantum dot and is given by $E_{QD}(N) - E_{QD}(N-1)$:

$$\begin{aligned}\mu_{QD}(N) &= E_{QD}(N) - E_{QD}(N-1) \\ &= \frac{(C_G V_G + C_S V_S + C_D V_D - qN)^2 - (C_G V_G + C_S V_S + C_D V_D - q(N-1))^2}{2C} + E_N \\ &= \frac{q^2}{C}\left(N - \frac{1}{2}\right) + q\frac{C_G V_G + C_S V_S + C_D V_D}{C} + E_N\end{aligned}$$

From this equation, we can calculate the difference between two consecutive electrochemical potentials which leads to $E_{add} = \frac{q^2}{C} + \Delta E$ (ΔE is the energy difference between two discrete energy levels). This energy difference (E_{add}) is known as the addition energy.

To simplify the following discussion about transport through a quantum dot, a simple depiction is provided in Figure 3.1(c-d), where the quantum dot is represented by a ladder of electrochemical potentials connected to the source and drain contacts but separated by some tunneling barrier. The gate is also included to represent its ability to tune the quantum dot's electrochemical potential. The electrochemical potential of the source and drain contacts are given by $\mu_S = \mu_0 + eV_{SD}/2$ and $\mu_D = \mu_0 - eV_{SD}/2$ where we assume a symmetrically applied bias. μ_0 is the electrochemical potential of the charge reservoirs without an additional bias voltage. Consider the case where the system is at $T = 0$ K, and $\mu_{QD}(N) < \mu_S, \mu_D < \mu_{QD}(N+1)$ (Figure 3.1c). Then charge carriers will tunnel into the quantum dot until it reaches an occupation level of N charges. This N^{th} charge cannot tunnel to the drain reservoir because $\mu_D > \mu_{QD}(N)$. Similarly, the $N+1^{th}$ charge cannot tunnel onto the dot because $\mu_{QD}(N+1)$ is higher than the potentials of the reservoirs. This is known as Coulomb Blockade. By changing the applied gate voltage, the electrochemical potential $\mu_{QD}(N+1)$ can be lowered such that it lies between μ_S and μ_D (Figure 3.1d). Now, a charge carrier can tunnel into the quantum dot from the source contact (since μ_S

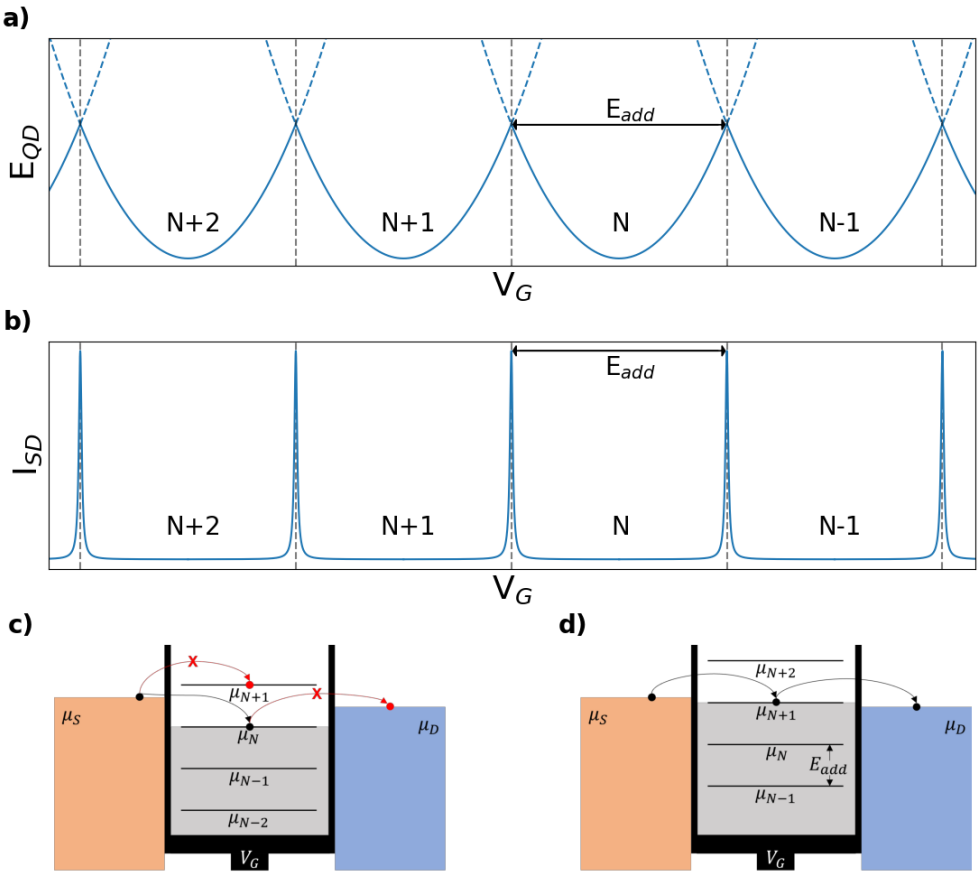

Figure 3.1: (a) Electrostatic energy of a quantum dot as a function of gate voltage for a various population of charged holes. The solid line represents the minimal energy of the quantum dot whereas the dashed line is the continuation of the parabola obtained from equation 3.1. (b) Current as a function of the gate voltage indicating periodic peaks occurring at the intersection of the parabolas from (a). (c-d) Illustration of a quantum dot showing the ladder of energy levels (horizontal lines). The thick vertical lines on either side of the quantum dot represent the tunneling barriers from the source to the drain reservoir. (c) Coulomb Blockade regime where injected carriers cannot tunnel into the drain reservoir due to the lack of available energy levels. (d) The gate voltage is tuned such that the energy level associated to a charge occupation of $N + 1$ lies between the source and drain electrochemical potentials resulting in the flow of current.

$> \mu_{QD}(N+1)$) resulting in an energy increase of $E_{add} = e^2/C + \Delta E$. Because $\mu_D < \mu_{QD}(N+1)$, the $N+1^{th}$ charge carrier will tunnel out of the quantum dot and into the drain, hence dropping the quantum dot's electrochemical potential back down to $\mu_{QD}(N)$, where the tunneling cycle then repeats itself. For a small applied bias voltage, the current spectrum as a function of the gate voltage appears as in Figure 3.1b.

From Figure 3.1, one can directly see that the energy between quantum dot energy levels can be directly extracted from a Current *vs.* Gate Voltage measurement by noting the difference between adjacent peaks. However, there is a proportionality constant involved, called the gate-lever arm ($\alpha_G = C_G/C$), which is not necessarily known.

$$E_{add} = \alpha_G \Delta V_G$$

Another measurement technique exists where, as a result, the addition energy is directly readout. To ease the explanation of this technique, we now refer to Figure 3.2. In experiment, Figure 3.2 is obtained by measuring the current as a function of both the bias voltage V_{SD} and the gate voltage V_G. When the bias voltage is zero, current peaks appear periodically in gate voltage as we have seen before (indicated by black circles in Figure 3.2). The white diamond indicates the region where the quantum dot's energy levels are not within the bias window, the energy spacing between the electrochemical potentials of the source and drain. The border of that diamond indicates moments where a quantum dot energy level aligns perfectly with the source or drain. The blue areas are then the regions where the occupation level of the quantum dot is fluctuating between $N-1$ and N. The green region represents an area where two charge carriers can tunnel in and out of the quantum dot at the same time. Finally, the red points represent the instant when the bias window is equal to the spacing between two consecutive electrochemical potentials in

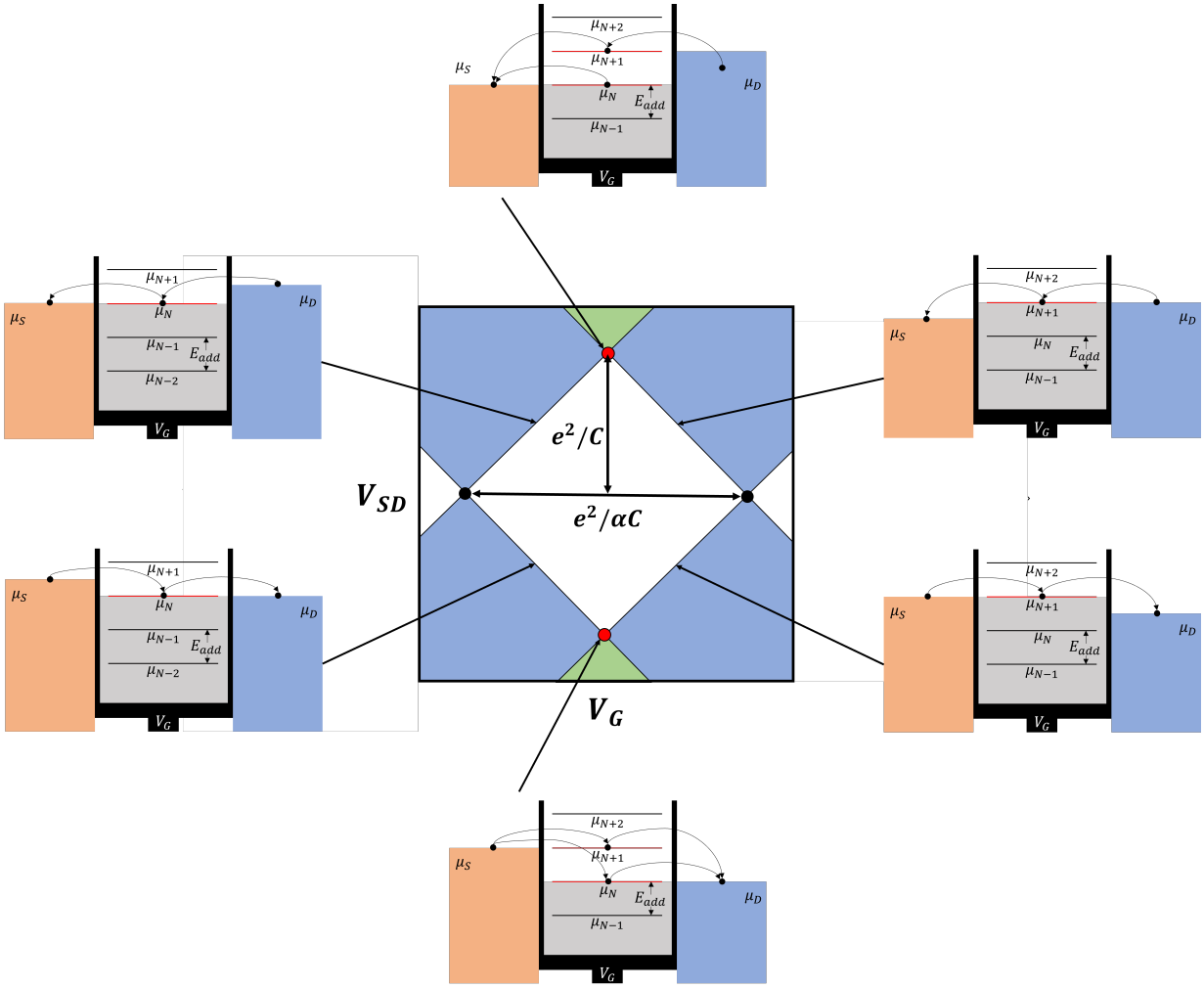

Figure 3.2: Illustration of Coulomb blockade diamonds. The current is blocked in the white diamond. Blue (green) areas represent single (two) charge carrier tunneling in and out of the quantum dot. Coulomb blockade peaks occur at the points where neighboring Coulomb diamonds touch and the addition energy can be calculated from their periodicity. The transport associated to these features is pictorially explained by the surrounding illustrations.

the quantum dot. Therefore, $e|V_{SD}| = |\mu_S - \mu_D| = \mu_{N+1} - \mu_N = E_{add}$. This kind of measurement leads to important information about the quantum dot such as its addition energy, the lever arms, and a good estimate for the quantum dot's size.

In this chapter, we present the fabrication and the resulting transport measurements of gate-controlled quantum dots in two different monolayer TMDs: molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2).

3.2 Device geometry

The device geometry used to achieve the results presented in this chapter rely on four main electrical components: the semiconducting TMD material, the electrical contacts, the global accumulation gate, and the local control gates.

Electrical contacts are achieved using the bottom contact architecture as discussed in chapter 2.3.2. For the MoS_2 device, the contacts consist of 10 nm of titanium (Ti) and 20 nm of gold (Au) whereas in the WSe_2 device, the contacts are made of 2 nm of chromium (Cr) and 8 nm of platinum (Pt). In these samples, only the contacts were cleaned using the AFM brooming technique. A global accumulation gate (top gate) is used to tune the contacts into the ohmic regime and reduce their contact resistance, and to inject charge carriers uniformly into the TMD layer. Local control gates are then used to locally tune the TMD flake's charge carrier density to create the quantum confinement.

The fabrication of these devices begins by patterning the local control gates (Ti (2.5 nm) / Au (2.5 nm)) on a degenerately p-doped silicon (Si) substrate with 285 nm of thermally grown silicon oxide (SiO_2) using standard electron beam lithography procedures. A false color scanning electron microscope image of the local control gates is found in Figure 3.3b

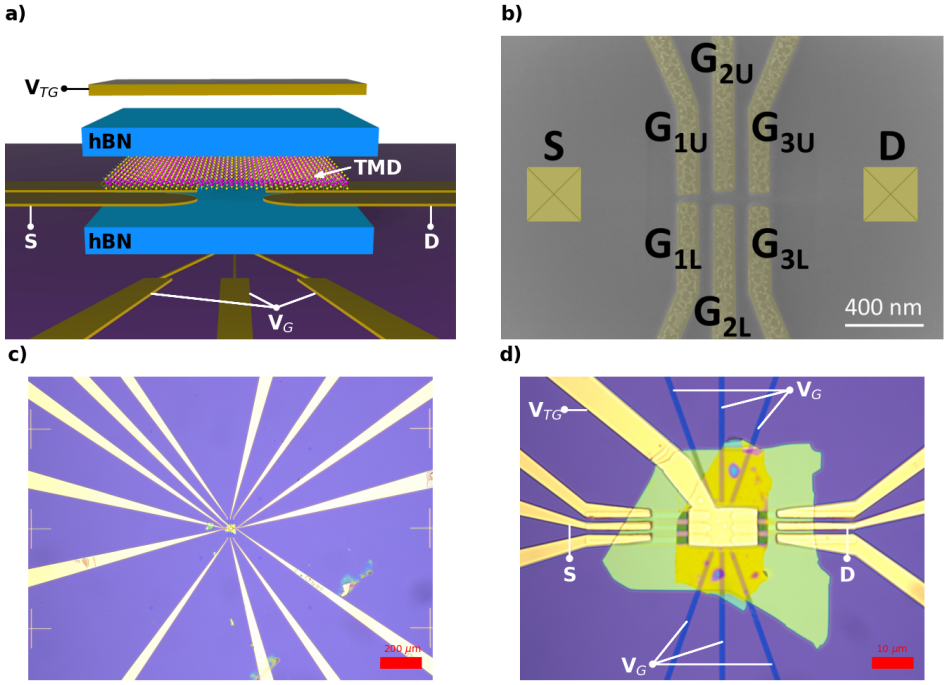

Figure 3.3: (a) Schematic of the device structure used to study quantum dots in transition metal dichalcogenide monolayers. False color scanning electron micrograph of the local control gates (V_G in (a)). Source and drain contacts are added to the figure simply for orientation purposes. (c) Optical micrograph of the completed device taken with a 5X magnification lens where the extension of the electrical connections are visible. (d) Optical micrograph of the same device as in (c) taken with a 100X magnification lens.

where the pattern includes three sets of gates separated by 50 nm, 100 nm, and 75 nm (from left to right). The transfer methods discussed in chapter 2.1 are used to transfer a previously identified exfoliated flake of hexagonal boron nitride on top of the local control gates. This hBN flake serves as a smooth substrate for the TMD flake and as a dielectric layer, insulating the semiconducting material from the local control gates. On top of the hBN, the electrical contacts are patterned, deposited, and cleaned. Using van der Waals heterostructure fabricating techniques, we sequentially pick-up a second flake of hBN, then a monolayer of TMD, and precisely place the stack on top of the electrical contacts. This

second hBN flake serves as an encapsulating layer and as a dielectric between the TMD flake and the top gate. Finally, using electron beam lithography techniques, the top gate is patterned on top of the hBN. A schematic of the device and a completed device are shown in Figure 3.3 (a, c-d).

3.3 Quantum dots in molybdenum disulfide

In this section, we concentrate on the electrical transport results we obtained on molybdenum disulfide (MoS_2) using the device presented in Figure 3.3 d. All electrical measurements were performed while the sample was submerged in a bath of liquid helium resulting in a measuring temperature of 4.2 K. Throughout the experiments, the middle leftmost and middle rightmost contacts were used as the source and drain contact respectively as indicated in Figure 3.3 d. Furthermore, the silicon back-gate was grounded during the course of the measurements.

Initial tests consisted of applying a bias voltage (10 mV) to the source contact and monitoring the drain current while sweeping the top gate voltage (Figure 3.4 a). The top gate was used to populate the MoS_2 sheet with charge carriers where we observed the current turning on at a voltage $V_{TG} = 5$ V, indicating that electrons are responsible for transport through the device. Reproducible current oscillations were observed suggesting the presence of localized states near the contacts caused by disorder in the sample.

The control gates' influence on transport across the device was then studied by sweeping the voltages on opposite gates simultaneously (G_{nL} and G_{nU} where $n = 1, 2, 3$). Figure 3.4 (b-d) presents these current traces for various top gate voltages ranging from 7 V (blue curve) to 5.2 V (pink) in intervals of 0.3 V. As can be seen in panels 3.4 (c-d), when the voltage is made more negative, the current reduces until it finally reaches zero. This can

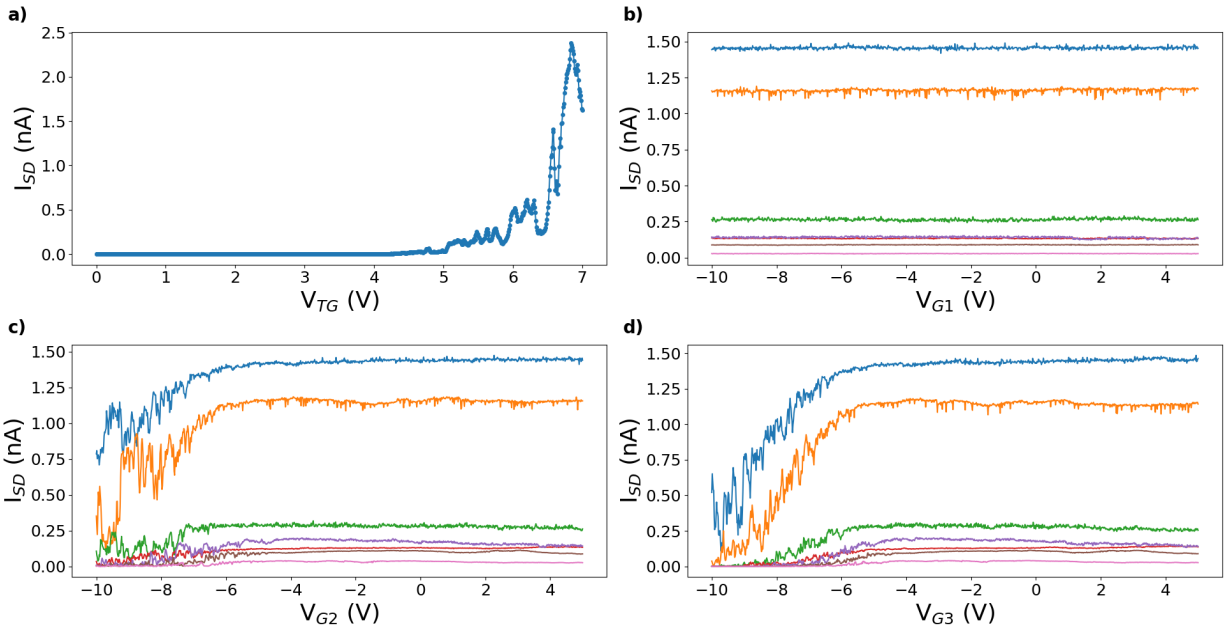

Figure 3.4: (a) Source-drain current as a function of the top gate voltage. Current begins to increase at $V_{TG} \approx 5$ V indicating electron conduction. (b-d) Source-drain current as a function of pairwise local control gate voltages. In (b), voltage was applied to the local control gates G_{1U} and G_{1L} simultaneously. In (c), voltage was applied to the local control gates G_{2U} and G_{2L} simultaneously. In (d), voltage was applied to the local control gates G_{3U} and G_{3L} simultaneously. A DC bias voltage of 10 mV was applied between the source and drain contacts and measurements were taken at T = 4 K for all panels.

be understood by the local gates first depleting the MoS_2 of electrons in the area above the gates resulting in the formation of a channel between the gates and a reduction of current. Eventually, the voltages on the gates are made negative enough such that the area between the gates is also depleted resulting in the pinch-off of the channel. This trend is true for the two sets of gates G_{2L}/G_{2U} and G_{3L}/G_{3U}, however, G_{1L}/G_{1U} have no influence on the current as seen in Figure 3.4 (b) indicating that these gates are most likely broken. Furthermore, we note that the current curves in 3.4 (c-d) agree well with the lithographic dimensions of the local control gates. Gates G_{2L} and G_{2U} are separated

by 100 nm implying that they should pinch-off at a higher voltage compared to gates G_{3L} and G_{3U} which are separated by 75 nm. The current traces associated with the pair of gates G_2 and G_3 also exhibit fluctuations which are attributed to quantum dots formed near the gates.

To demonstrate that these fluctuations are reproducible, the current traces taken in Figure 3.4 (c-d) are repeated for a large range of top gate voltages with a 15 mV resolution Figure 3.5 (a, b). The resulting current is plotted as a function of the voltage applied to the set of gates (G_{3U} and G_{3L} in Figure 3.5 (a), G_{2U} and G_{2L} in Figure 3.5 (b)) and the top gate voltage. In both plots, we can again identify the regime where the gates pinch-off the channel and the current is zero (lower left corner). We can also identify the regime where the gates have not yet depleted the MoS_2 of electrons in the region above them resulting in high current (top right corner). In between these two regimes, we observe multiple continuous diagonal lines demonstrating the reproducibility of the current oscillations observed in Figures 3.4c-d. These oscillations, which we attribute to resonant tunneling through quantum dots in the device, were further studied by applying independent voltages to individual control gates at a fixed top gate voltage. In Figure 3.5 (c), the source-drain current was monitored at a constant top gate voltage of $V_{TG} = 7$ V as the control gates G_{3U} and G_{3L} were independently changed. In Figure 3.5 (d), the effect of control gates G_{2U} and G_{2L} on the source-drain current was studied at a top gate voltage of $V_{TG} = 4.2$ V.

In Figure 3.5 (c), multiple horizontal, vertical, and diagonal current peaks are visible which provide information about the location of the quantum dots that are responsible for these resonant transport peaks. In more detail, a vertical line suggests that the quantum dot is only tunable by the voltage applied to G_{3L}, indicating that it must be located above that gate. Using that same logic, the presence of horizontal lines imply that there are quantum

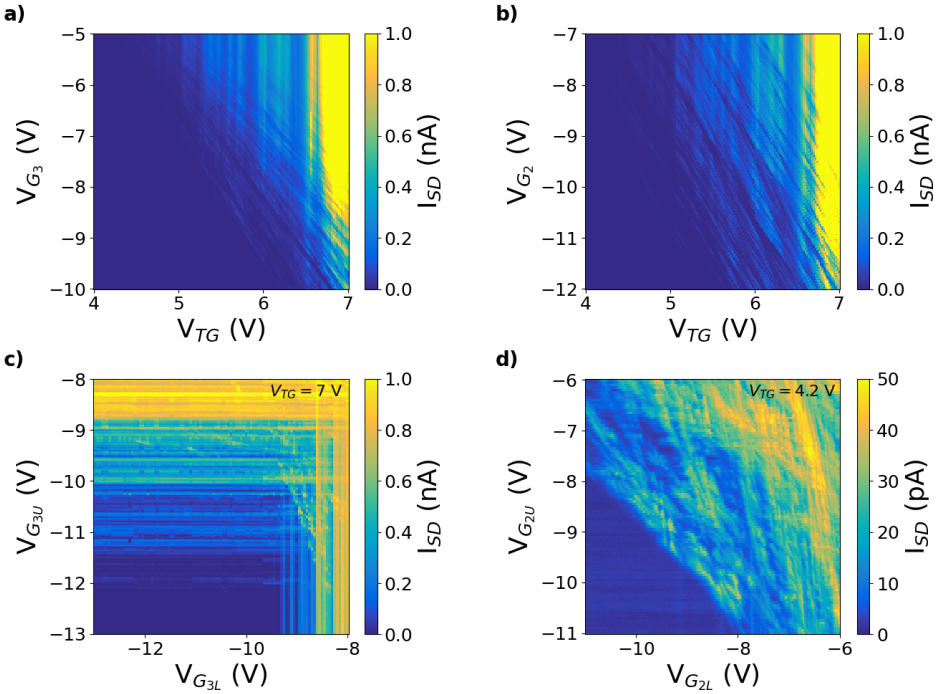

Figure 3.5: (a-b) Source-drain current as a function of the top gate voltage and the voltage applied simultaneously to the local control gates G_{3U} and G_{3L} in (a) (G_3 in the panel) and G_{2U} and G_{2L} in (b) (G_2 in the panel). (c-d) Source-drain current as a function of the individual control gates G_{2U} and G_{2L} in (c) and G_{2U} and G_{2L} in (d) at constant top gate voltages as indicated. A DC bias voltage of 10 mV was applied between the source and drain contacts and measurements were taken at T = 4 K for all panels.

dots above G_{3U}. Diagonal lines suggest that quantum dots are capacitively coupled to both gates and that they lie between them. Figure 3.5 (d) tells a similar story concentrating on an area where there are multiple diagonal lines with various slopes. This suggests that there are multiple quantum dots between the gates G_{2U} and G_{2L}, with some of the dots being closer to one gate than the other.

The number of quantum dots formed in the MoS_2 device suggested by the charge stability diagrams in Figure 3.5 indicate that these dots are not formed by the local control gates but are instead created by the local minima of the non-uniform potential landscape governed by

defects and disorder in the device. Although some of the quantum dots are formed directly above or near single gates, the large number of dots make it impossible to individually study them. Further material and device optimisation is required to realize a more tunable quantum dot circuit.

3.4 Quantum dots in tungsten diselenide

Scanning tunneling microscopy (STM) has been used to image defects in various semiconducting TMD materials and extract their defect densities (Figure 3.6). More specifically, for the case of MoS_2, chemical vapor deposition grown crystals have demonstrated defect densities ranging from 8×10^{12} cm^{-2} [71] to 2×10^{13} cm^{-2} [72], and natural crystals have been reported to have defect densities ranging from 5.1×10^{11} cm^{-2} [73] to 5×10^{13} cm^{-2} [74]. STM work has also been performed on tungsten diselenide (WSe_2), another semiconducting TMD, and lower defect densities have been published. For example, WSe_2 crystal grown using molecular beam epitaxy has reported a defect density of 2.19×10^{11} cm^{-2} [75], flux grown WSe_2 reported a defect density of 7.0×10^{10} cm^{-2} [52], and mechanically exfoliated WSe_2 reported a defect density of 1.1×10^{12} cm^{-2} [76].

The fact that WSe_2 has been demonstrated to have a lower defect density compared to MoS_2, similar devices were fabricated and studied using WSe_2 as the TMD layer. Furthermore, the spin splitting described in chapter 1 is larger in both the conduction and valence band for monolayer WSe_2 compared to MoS_2 which can be an attractive property for spin qubits. The experimental results from the transport measurements performed on these devices are the subject of the following letter[1].

[1] **J. Boddison-Chouinard**, A. Bogan, N. Fong, K. Watanabe, T. Taniguchi, S. Studenikin, A. Sachrajda, M. Korkusinski, A. Altintas, M. Bieniek, P. Hawrylak, A. Luican-Mayer, and L. Gaudreau. Gate-controlled quantum dots in monolayer WSe_2. *Applied Physics Letters*, 119, 2021.

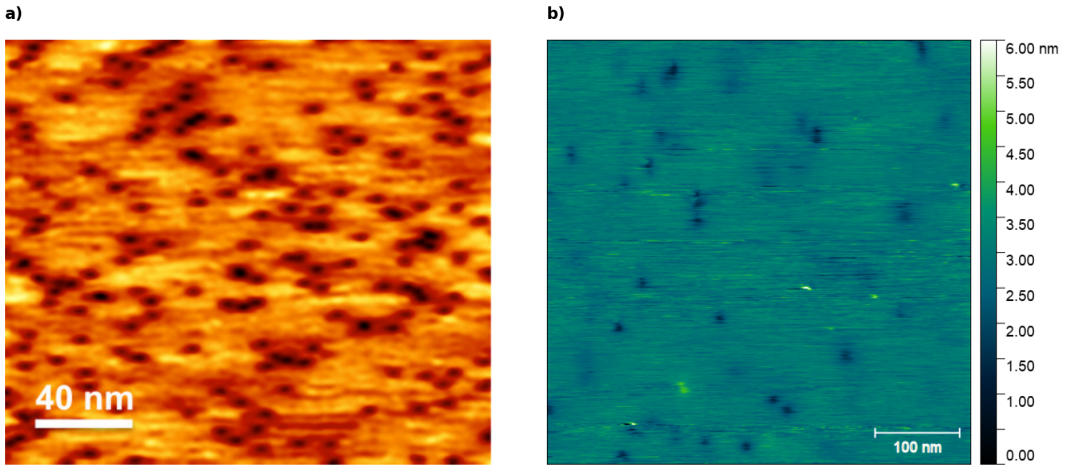

Figure 3.6: (a) STM image of exfoliated MoS_2 crystal indicating a defect density of 5.1×10^{11} cm^{-2} ($V_b = 1.5$ V, $I_t = 0.3$ nA). Image adapted from Ref. [73] (b) STM image of exfoliated WSe_2 crystal indicating a defect density of approximately 1×10^{10} cm^{-2} ($V_b = -1$ V, $I_t = 0.250$ nA). This WSe_2 crystal comes from the same "mother" crystal used for the transport measurements presented in this thesis. Image taken in the Adina Luican-Mayer lab by Ryan Plumadore.

3.4.1 Gate controlled quantum dots in monolayer WSe_2

Statement of contributions

ALM, Louis Gaudreau (LG) and Pawel Hawrylak (PH) envisioned the idea for the work presented in this letter. JBC, ALM, LG, and Alex Bogan (AB) designed the device architecture. Norman Fong (NF) fabricated the local control gates and JBC fabricated the remainder of the sample. JBC and AB performed the experiments, and JBC analyzed the data. JBC wrote the first draft of the manuscript (excluding the theoretical calculations) which was completed alongside LG, ALM, and AB. The theoretical component of the manuscript was completed by Marek Korkusinski (MK), Abdulmenaf Altintas (AA), Maciej Bieniek (MB), and PH. KW and TT grew and provided the hexagonal boron nitride.

Gate controlled quantum dots in monolayer WSe_2

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Quantum confinement and manipulation of charge carriers are critical for achieving devices practical for quantum technologies. The interplay between electron spin and valley, as well as the possibility to address their quantum states electrically and optically, make two-dimensional (2D) transition metal dichalcogenides an emerging platform for the development of quantum devices. In this work, we fabricate devices based on heterostructures of layered 2D materials, in which we realize gate-controlled tungsten diselenide (WSe_2) hole quantum dots. We discuss the observed mesoscopic transport features related to the emergence of quantum dots in the WSe_2 device channel, and we compare them to a theoretical model.

One of the most promising solid-state platforms for implementing qubits is based on semiconductor spin qubits utilizing the spin degree of freedom of electrostatically confined electrons in semiconductors [1, 2]. This topic has been extensively studied in materials such as GaAs and SiGe, in which researchers have been able to create circuits from one to up to nine quantum dots [3–6], and have successfully demonstrated coherent quantum operations using the spin of the confined carriers[7, 8].

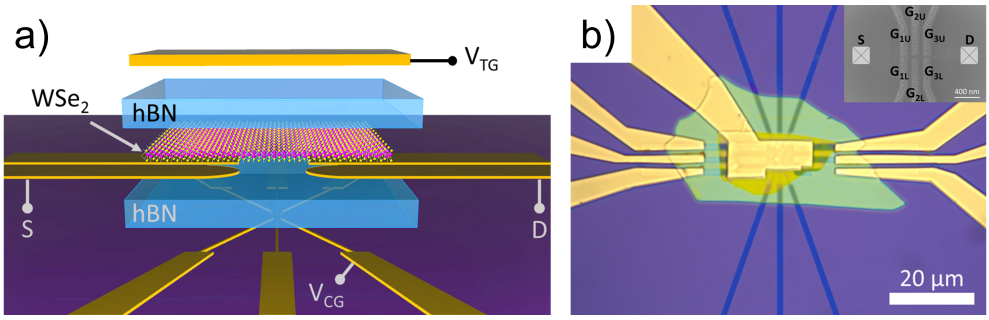

Figure 1. (a) Schematic of the monolayer WSe_2 device structure. Cr (2 nm) / Pt (8 nm) contacts are used to contact monolayer WSe_2 from the bottom. HBN encapsulates the WSe_2 layer, while a top gate (V_{TG}) and bottom control gates (V_{CG}) are used to control the carrier density in the WSe_2 layer. (b) Optical micrograph of a competed device. The inset represents a scanning electron micrograph depicting the layout of the control gates.

Despite significant progress, material specific challenges continue to hamper the development of complex quantum devices. For example, GaAs spin qubits suffer from short coherence times mainly due to hyperfine interaction with nuclei [9]. SiGe devices have significantly higher qubit coherence times when using purified ^{28}Si[10], which has zero nuclear spin. However, the indirect band gap in Si prevents such devices from performing coherent photon to spin conversion, necessary for long distance quantum network communications [11].

With the development of advanced methods for fabricating 2D materials heterostructures, devices based on atomically thin semiconducting transition metal dichalcogenides (TMDs)[12] are emerging as a promising platform in the field of quantum information science [13, 14]. Semiconducting TMDs typically exhibit a direct band gap at the K-point in the Brillouin zone[15]. Moreover, they have potential for realizing spin qubits with long coherence time due to spin-valley locking, caused by the strong spin-orbit interaction and the symmetries of their 2D lattice [16]. These promising properties motivated recent efforts to understand charge transport through quantum dots in 2D materials [17–21]. Gated structures were used to create many-electron single and double quantum dots in eight layers of molybdenum disulfide (MoS_2)[18], in monolayer MoS_2[19], as well as in monolayer and bilayer tungsten diselenide (WSe_2)[21]. In these low dimensional structures, defects and disorder affect the

transport properties of real devices, where they alter the electrostatic environment experienced by the charge carriers [22, 23]. Effects of such a potential landscape have been seen in experiments reporting resonant transport through quantum dots that form in local minima [24, 25]. These experiments underscore not only the promise of the 2D materials platform for quantum devices, but also the remaining challenges in material purity, device fabrication and ultimate electrical and optical control over the charge, spin and valleys degrees of freedom of the quantum states. Here, we address some of these questions and present measurements of hole transport through a monlolayer WSe_2 quantum dot. Our approach, which differs from similar reported devices [21], allows us to identify and control, using gates, quantum dots formed in the local minima of electrostatic potential fluctuations in monolayer WSe_2 at a temperature of 4K. We estimate the charging energy and diameter of the dot using a simple capacitive model and we present a numerical model of quantum dots in this material.

The WSe_2 device was assembled using standard dry transfer methods [26–28] on a Si/SiO_2 wafer with 285 nm SiO_2 and degenerately doped Si. A schematic representation and an optical micrograph of a completed device are shown in Figure 1. Hexagonal boron nitride (hBN) (38nm), used as an insulating dielectric, was transferred on top of pre-patterned local control gates (Ti (2.5 nm) / Au (2.5 nm)), followed by patterned bottom electrical contacts (Cr (2 nm) / Pt (8 nm))[29] using e-beam lithography. To minimize the contact resistance, we mechanically removed the polymer residues using an atomic force microscope tip in contact mode[30, 31]. Following this key step, we used dry transfer techniques to position a WSe_2 monolayer encapsulated by a hBN flake ($\approx$ 30 nm) onto the mechanically cleaned bottom contacts. In a final lithographic step, we deposited a top gate (Ti (5 nm) / Pd (20 nm) / Au (100 nm)), which covered the entire WSe_2 flake. This gate was used to modify the charge carrier density in the WSe_2 and to achieve a regime of ohmic contact. Details of device fabrication and cleaning are presented in the supplementary material.

Experimental characterisation of this device was initially performed by applying a small DC voltage to the source contact and monitoring the drain current, while sweeping a DC voltage on the top gate (Figure 2a). The increase in current for negative top gate voltages indicates the successful population of holes in the channel, consistent with the doping levels found in previous experiments [21, 29]. Furthermore, as the temperature is lowered from room temperature to 4K, a larger negative voltage on the top gate is necessary to activate the conducting channel, as the microscopic crystal

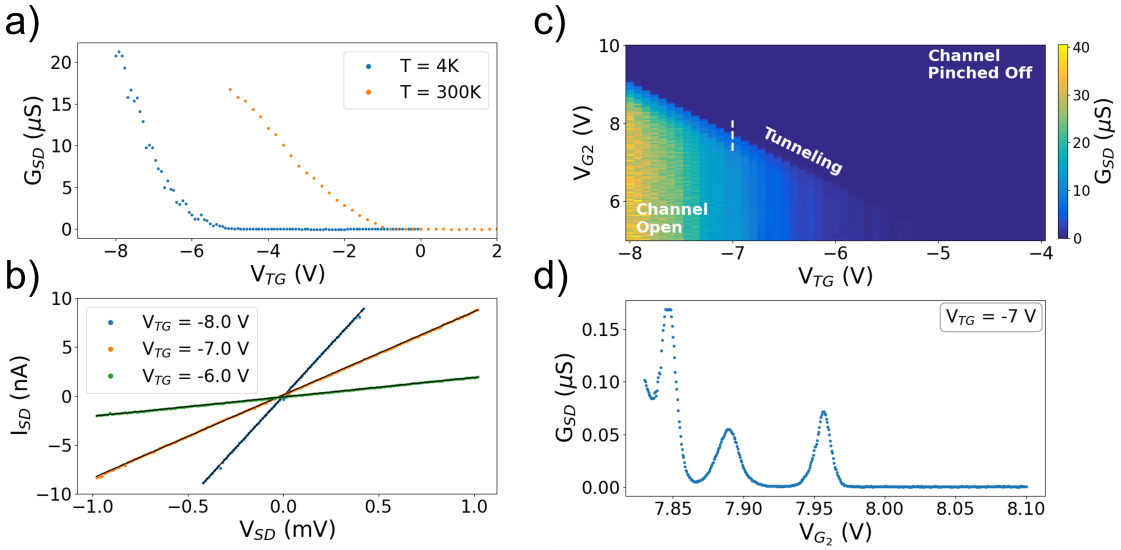

Figure 2. (a) Source-drain conductance as a function of top gate voltage where the black (blue) curve was taken at room temperature (4K). (b) Source-drain current versus source-drain voltage taken at various top gate voltages, while all control gates are grounded. (c) Source-drain conductance versus top gate and control gates V_{G2} (upper-middle and lower-middle in inset 1b). The conductance across the channel operates in three distinct regimes: an open channel, a tunneling regime, and a pinched-off regime. (d) Source-drain conductance versus the control gate voltage V_{G2} at a constant top gate voltage of -7 V.

defects decrease the device mobility especially at low temperatures [32]. The remaining measurements shown in this letter are performed at 4K. Figure 2b shows current-voltage characteristics obtained at different values of top gate voltage, as indicated. We note that in our device ohmic contacts are achieved when the top gate is tuned below -5 V, as evidenced by the linear behaviour of the $I_{SD} - V_{SD}$ curves. A total resistance of 47 kΩ is observed at a top gate voltage of V_{TG}=-8 V.

Next, we investigated the influence of the local control gates on the transport proprieties of the device, by applying identical voltages to pairs of control gates (upper (U) and lower(L)), while keeping the remaining control gates grounded. Figure 2c shows the conductivity G_{SD} across the WSe_2 channel as a function of top gate voltage V_{TG} and the voltage applied to both control gates in the pair G_{2U} and G_{2L} simultaneously, V_{G2}. We distinguish three regimes. When the channel is activated by the top gate and the control gate voltages are below a certain threshold, the channel

is open (conductive), and a finite current is measured. As we increase the local control gate voltage V_{G2}, the channel crosses over to a resonant tunneling regime and is eventually completely pinched-off with sufficiently large control gate voltages. For clarity, Figure 2d shows a line trace along the range of voltages indicated by the dashed line in Figure 2c, taken at a top gate voltage V_{TG} = -7 V. The presence of resonant transport peaks in the tunneling regime suggest the presence of quantum dots in the device.

We can further explore the characteristics of the quantum dots in the channel by varying the voltages on the local control gates. Figure 3a shows the changes in the source-drain current I_{SD}, when we vary the voltages on G_{2U} and G_{2L}, at a fixed top gate voltage $V_{TG} = -5.5$V. In this charge stability diagram, we identify horizontal lines and vertical lines, corresponding to different transport resonances through quantum dots. Vertical lines indicate that the quantum dot is capacitively coupled only to gate G_{2U} and, therefore, that its location is under the gate G_{2U} or very close to it. Similarly, horizontal peaks are entirely controlled by gate G_{2L}. We can also identify quantum dots formed in between gates as depicted by the G_{3L} - G_{3U} stability diagram in Figure 3b, where in addition to having horizontal and vertical lines, we find diagonal lines with various slopes, indicating the presence of quantum dots forming at various locations between the two gates. In this situation, we observe avoided crossings as the one highlighted in the inset of Figure 3b, suggesting capacitive coupling between such quantum dots. The results presented in both Figure 3a and Figure 3b imply that the potential landscape of the WSe_2 varies across the sample, creating local quantum dots that are identified by transport resonances near depletion. The control gates can therefore be used to study individual quantum dots.

We explore the properties of the quantum dot associated with the vertical lines in Figure 3a, by sweeping the bias voltage V_{SD} for different values of G_{2L} and G_{2U} as indicated by the dashed line, while the top gate voltage is kept constant $V_{TG} = -5.5$ V. The variation of the source-drain current I_{SD} while the bias and control gate voltages are varied, is shown in Figure 3c. We note the presence of diamond-shaped features (Coulomb diamonds) characteristic of quantum dot behaviour, where regions with zero source-drain current represent a regime of Coulomb blockaded transport. From the plot of Figure 3c we can estimate the size and charging energy of the quantum dot. From the height of the first Coulomb diamond, the charging energy $U \sim 3.4$ meV, value consistent with

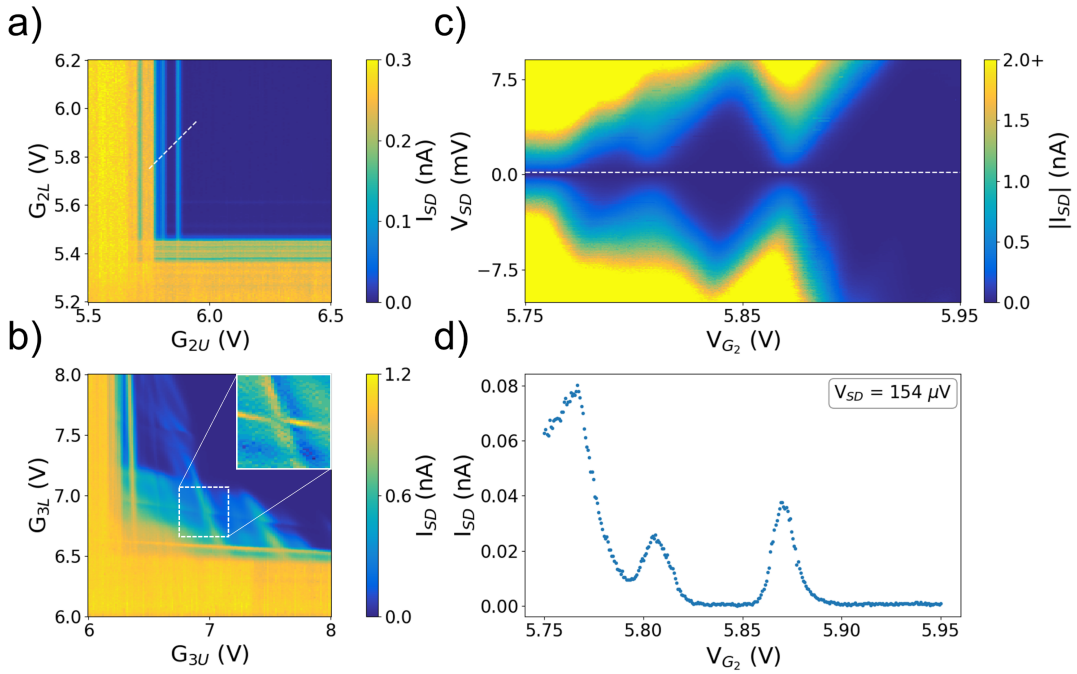

Figure 3. (a) Source-drain current I_{SD} as a function of individual control gates G_{2L} and G_{2U} taken at $V_{TG} = -5.5$ V and $V_{SD} = 0.5$ mV. (b) Source-drain current I_{SD} as a function of two other individual control gates G_{3L} and G_{3U} taken at $V_{TG} = -6.0$ V and $V_{SD} = 0.5$ mV. The inset represents the derivative $\partial I_{SD}/\partial G_{3L}$ of the white dashed box. (c) Source-drain current I_{SD} as a function of bias voltage V_{SD} and control gate V_{G2} voltage corresponding to the white dashed line in (a). (d) Source-drain current I_{SD} as a function of $G_{2L\&R}$ taken at a $V_{SD} = 154\ \mu V$ corresponding to the white dashed line in (c).

previous reports in gated QD structures in WSe_2 [21, 24]. Figure 3d shows a line cut through the map of Figure 3c, taken at a source-drain voltage $V_{SD} = 154\ \mu V$. The energy separation between the peaks is $\Delta V_G \approx 65$ mV. We can estimate the size of the quantum dot by approximating the quantum dot and the control gate as a parallel plate capacitor, as detailed in the supplementary material. Using $\epsilon_{hBN} = 4$ as hBN's relative permittivity[33] and its thickness $t_{hBN} = 38$ nm, the gate capacitance is approximated to be $C_G = \epsilon_0 \epsilon_{hBN} \pi d^2/4t_{hBN}$, where d is the quantum dot diameter. The gate capacitance can also be expressed as $C_G = e^2/\Delta V_G$. From these two equations, we estimate the quantum dot diameter to be $d \approx 58$ nm.

To understand the nature of electronic states available for holes that are confined in a WSe_2

quantum dot as well as the interplay of valley, spin and orbital degrees of freedom, we performed tight binding and ab-initio calculations (using ABINIT) of valence holes in single layer WSe_2 [34, 35] and confined to a gated quantum dot [35–37]. A single layer of WSe_2 consists of two triangular sublattices: sublattice A, having d orbitals from W atoms and, sublattice B, consisting of a pair of Se atoms, with p-orbitals below and above the metal layer. A WSe_2 monolayer with such a hexagonal lattice is a direct gap semiconductor with energy minima at the two nonequivalent valleys in the Brillouin zone. Figure 4a shows the calculated energy spectrum of holes in a single layer of WSe_2 around the two non-equivalent valleys, $+K$ and $-K$, where strong spin-orbit interaction leads to splitting of hole spin up and spin down states by 470 meV. This implies that the spin degree of freedom of the hole ground states is locked to the valley index with spin up locked to $+K$ and spin down locked to $-K$. In addition, the hole wavefunction changes its orbital character, at $+K$ valley it is built of $m = +2$ W d-orbital, where d-orbital corresponds to state with angular momentum l=2 and z-projections m=0,+/-2 [34], while at $-K$ valley it is built of $m = -2$ W d-orbital. The energy bands reflect the massive Dirac fermion description of the energy bands in WSe_2, where close to the top of the upper valence band the dispersion is approximately parabolic with effective mass $m^* = 0.28$, but it quickly becomes linear.

We consider hole states localised in a WSe_2 quantum dot, similar to those leading to the observed Coulomb blockade spectrum in our device. Figure 4b represents an idealized Gaussian potential profile generated by an external gate [35, 37] with $V_0 = 100$ meV and diameter of 60 nm, assumed to confine hole states in a WSe_2 layer. The calculated spectrum for this quantum dot is shown in Figure 4c, where the zero energy is at the top of the valence band and the confining potential leads to discrete quantum dot levels in the energy gap of the WSe_2 layer. As a result of confinement, we find several energy shells, separated by energy $\omega_0 = 5$ meV. The lowest hole energy s-shell is doubly degenerate, corresponding to $(+K, \uparrow, m = +2)$ and $(-K, \downarrow, m = -2)$ states. The next energy p-shell is almost fourfold degenerate, followed by a six fold degenerate d-shell. The predicted hole energy spectrum is similar to the energy spectrum of carriers confined to semiconductor parabolic quantum dots[38], except for lifting the degeneracy of hole shells by topological magnetic moments inherent to massive Dirac fermions [35–37]. To estimate the charging energy U needed to add a hole to the lowest state, we consider a parabolic quantum dot, so that $U = Ry^*\sqrt{\pi}\sqrt{\omega_0/Ry^*}$ [39], where Ry^* is

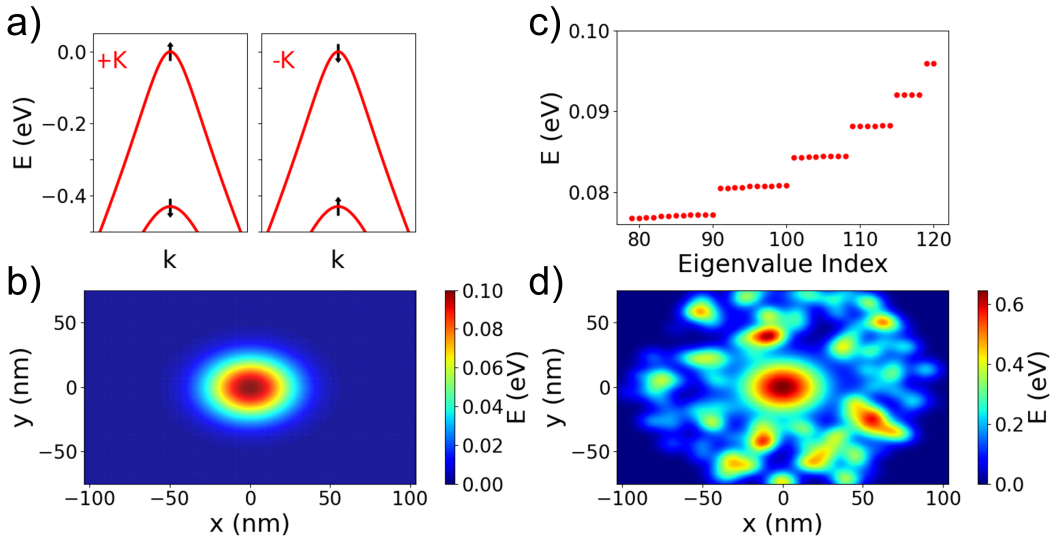

Figure 4. (a) Electronic band dispersion for WSe_2 around the top of the valence band for the two valleys $+K$ and $-K$, emphasizing the spin structure. (b) Schematic view of a simulated Gaussian potential for a quantum dot in WSe_2. (c) Energy spectrum of hole states in a WSe_2 quantum dot confined by the potential shown in (b). (d) Schematic representation of a quantum dot generated by a gate and surrounded by a random electrostatic potential.

an effective Rydberg, given by $Ry^* = Ry \times m^*/(\epsilon^2)$, where m^* is the effective mass and ϵ the effective dielectric constant. For typical parameters $\epsilon = 10$ and $m^* = 0.28$ characteristic of holes in WSe_2, the resulting charging energy is found to be $U = 20$ meV. We note that the discrepancy between this simple model and the measured experimental results are likely due to the presence of random electrostatic potential below the semiconducting channel or the gate, as schematically illustrated in Figure 4d. This suggests that to fully take advantage of the unique properties of quantum confined states in 2D semiconductors, more effort is needed to optimize the materials homogeneity and purity, as well as to improve electrical contacts.

In summary, we demonstrated electrical control of WSe_2 hole quantum dots in gated devices based on 2D heterostructures. Electrical transport measurements revealed a Coulomb blockade regime, from which we estimated the charging energy and size of the formed quantum dots. Additionally, charge stability diagrams using control gates indicate that the quantum dots are likely generated by

the inherent electrostatic fluctuations of the device and that they can be coupled. Our theoretical calculations reveal that the ground state of holes in such a quantum dot is not fourfold degenerate as expected and found in bilayer graphene quantum dots [17], due to the spin and valley degrees of freedom, but doubly degenerate due to valley-spin locking. These results shed light on mesoscopic transport features in 2D semiconducting quantum dot devices, paving the way for the development of quantum devices based on electrostatically confined WSe_2 quantum dots.

SUPPLEMENTARY MATERIAL

See the supplementary material for details on device fabrication and AFM cleaning as well as for quantum dot size calculations.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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3.5 Conclusion

The electrical transport measurements performed on both the monolayer MoS_2 and monolayer WSe_2 devices revealed the presence of many quantum dots formed in the minima of the non-uniform potential landscape created by defects and disorder. From charge stability diagrams, we observed that the number of incidental quantum dots in the monolayer MoS_2 was too large to isolate and study single dots. However, due to the lower defect densities found in WSe_2, the local control gates were used to study individual quantum dots in this material where Coulomb blockade and Coulomb diamonds were observed.

Evident by transport measurements taken at low-temperatures, quality electrical contacts were achieved and gates were successfully used to globally and locally tune carrier densities. However, to achieve *gate-defined* quantum dots in monolayer TMDs, improvements must be made to further reduce the disorder and defects by improving the material, or by altering the device architecture (see chapter 5).

Chapter 4

Charge detection in monolayer tungsten diselenide

4.1 Quantum point contacts for charge detection

In an ideal and uniform system, the local gate pattern described in chapter 3 (Figure 3.3) can be used to create narrow constrictions between two opposite gates, commonly referred to as a quantum point contact (QPC). For example, voltages can be applied to gates G_{1U} and G_{1L} in our device architecture such that the semiconducting material directly above the gates are depleted of carriers, and flow of current occurs only through the channel defined by the two gates.

Transport through such a channel is discussed in detail in chapter 5, where we see that the conductance is quantized and given by the Landauer formula [77, 78]:

$$G = \frac{ge^2}{h}N$$

where e is the elementary charge, h is Planck's constant, N is the number of available channels (or subbands), and g is the degeneracy of the channels.

The energy spacing between subbands is a function of the width of the constriction, W, therefore, as the width is reduced, the number of contributing subbands is also reduced, thus reducing the conductance. An important aspect of gate-defined constrictions is that the constriction's width is tunable by the potentials applied to the gates ($W \propto V_G^{-1}$), therefore, the channel conductance as a function of the gate potential should vary in a step like fashion such that it respects the Landauer formula. This staircase pattern has been observed and confirmed in various systems [79–82].

An advantage of this conductance pattern is its sensitivity to nearby potentials. One can tune the constriction width such that the conductance is at a value that corresponds to the transition from n to $n+1$ subbands, or in between two conductance plateaus. As a result, a nearby potential fluctuation will result in a small change in the constriction width and a large change in conductance. For this reason, quantum point contacts have been used as extremely sensitive charge sensors in complex quantum circuits. The QPC is placed in the circuit near a quantum dot such that it is sensitive to the change in charge occupation of the quantum dot. This detection scheme is especially practical in multiple quantum dot systems where it has been used to detect the charge in each dot separately without having the need to flow current directly through the quantum dots [26, 83–90].

4.2 Results

QPCs and charge detection have been proven to be a vital component of complex quantum circuits, however, non-invasive charge detection has never been implemented in TMD based quantum devices due to the challenges related to material and device cleanliness.

In the following article, we demonstrate that a gate-defined nano-constriction fabricated in monolayer WSe_2 can be used to detect the change in occupation of a nearby quantum dot[1].

4.2.1 Charge detection using a monolayer WSe_2 van der Waals heterostructure

Statement of contributions

AB initiated the work presented in this article. The local control gates were patterned by NF, Pedro Barrios (PB), and Jean Lapointe (JL). Sample fabrication including heterostructure assembly, electrical contacts patterning, and top gate fabrication were done by JBC. JBC and AB conducted the experiments. JBC analyzed the data and wrote the first draft of the manuscript which was completed in collaboration with LG and ALM. KW and TT grew and provided the hexagonal boron nitride.

[1] **J. Boddison-Chouinard**, A. Bogan, N. Fong, P. Barrios, J. Lapointe, K. Watanabe, T. Taniguchi, A. Luican-Mayer, and L. Gaudreau (in press). Charge detection in a WSe_2 van der Waals heterostructure. *Physical Review Applied*, 2022

Charge detection using a monolayer WSe_2 van der Waals heterostructure

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Charge detection is a crucial component used in semiconductor quantum circuits. It allows the non-invasive readout of charge and spin qubits in quantum information protocols and can also be leveraged for new quantum sensing applications. In this work, we demonstrate that van der Waals heterostructure devices with gated nano-constrictions in monolayer WSe_2 can be used as charge detectors for nearby quantum dots. This is the first demonstration of charge detection using transition metal dichalcogenides, and we find that the detection sensitivity is comparable to other 2D material charge detectors based on graphene. These results open the possibility of implementing charge detection schemes based on 2D materials in complex quantum circuits.

The detection and manipulation of individual charges and spins is at the heart of developing quantum technologies. In particular, the detection of individual charges in a quantum dot (QD) can be realized by placing a quantum point contact (QPC) in its vicinity and detecting changes in the conductance through the QPC current as a result of the altered

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electrostatic environment around the QD. While transport directly through a single quantum dot and charged detection are equivalent this is not the case for circuits containing more than a single quantum dot. In that situation direct transport only occurs under specific resonance conditions between dots which becomes severely restrictive as additional quantum dots are added. This is in contrast to charge detection techniques which are able to identify the charge in each dot separately without current flowing directly through the circuit. As a result, charge detection technology is a requirement for complex spin qubit quantum circuits[1–3]. The implementation of this approach was initially successfully demonstrated in GaAs two-dimensional electron gas (2DEG) devices[4]. More recently, two-dimensional (2D) materials including graphene and semiconducting transition metal dichalcogenides (TMDs) emerged as a novel platform to realize electrostatically confined quantum circuits. Within the 2D materials platform, QPC's have been demonstrated in TMDs[5–10], and more specifically, QPC charge detection has been demonstrated in monolayer and bilayer graphene (BLG) devices [11–16]. However, charge detection has not yet been implemented in semiconducting TMDs. The direct band gap in TMDs, along with the interplay of the spin and valley degrees of freedom, makes them an appealing platform for realizing hybrid quantum circuits with optical and solid state qubits[17–19]. Additionally, the strong spin-orbit coupling in TMDs could enable fast spin qubit manipulation with AC electric fields[20] and lead to the spin-valley locking, by which qubits could be more robust against electro-magnetic noise. Although the first gated quantum dots in TMDs have been recently realized[5, 6, 8, 21–23], charge detection using gated nano-constrictions is yet to be implemented. In this work, we realize a nano-constriction in a monolayer WSe_2 channel and, demonstrate for the first time, charge detection of a gate controlled WSe_2 quantum dot.

The charge detector device used in this work is based on monolayer WSe_2, schematically described in Figure 1a. Its optical micrograph is shown in Figure 1b. The device was assembled on a $p-Si/SiO_2$ (285 nm) substrate using standard dry transfer methods. Local control gates [Ti (2.5 nm) / Au (2.5 nm)] were first deposited on the substrate using electron beam lithography (Fig 1b inset). They are 100 nm in width, with a lateral spacing of 50 nm, and varying gap spacing (50 nm, 100 nm, and 75 nm). The local control gates are responsible for locally depleting the carriers in the monolayer WSe_2 flake. A flake of hexagonal boron nitride (hBN) with 44 nm thickness was transferred on top of the pre-patterned gates and electrical contacts [Cr (2 nm) / Pt (8 nm)] were subsequently lithographically patterned on

top of the hBN. To increase sample cleanliness and, consequently, reduce contact resistance, the device was cleaned in a vacuum furnace (10^{-7} Torr) at 300 °C for 30 minutes. Additionally, remaining polymer residues were removed using an atomic force microscope (AFM) tip in contact

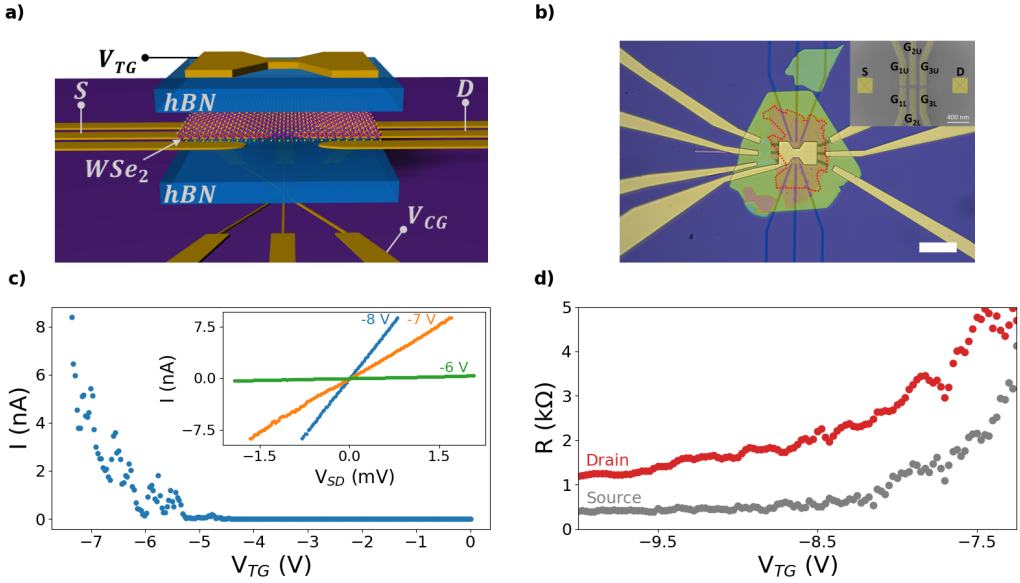

FIG. 1. (a) Schematic architecture of the charge detection device based on monolayer WSe_2. (b) Optical micrograph of the completed device used in this work. The WSe_2 flake is outlined in red for clarity. Scale bar: 20 μm. Inset: false-color scanning electron micrograph of the control gates. (c) Source-drain current as a function of the top gate voltage (V_{TG}) showing the activation curve of the device. Inset: linear I-V characteristic observed when $V_{TG} < -6$ V. The temperature of these measurements was T = 4 K. (d) Contact resistance of the source and drain contacts as a function of the top gate voltage V_{TG}, as indicated. The grey (red) curve represents the resistance associated to the source (drain) contact. The temperature of these measurements was T = 1.5 K.

mode[23–25]. A WSe_2 monolayer and a 37 nm thick hBN flake were exfoliated and identified on independent substrates. Using dry transfer techniques, the hBN flake was first picked-up an then used to pick-up the WSe_2 flake; subsequently, the WSe_2/hBN stack was precisely placed on top of the cleaned electrical contacts. We note that prior to the deposition of the hBN/WSe_2 stack, the WSe_2 surface was also mechanically cleaned using an AFM tip. A last lithographic step was performed to deposit a top gate [Ti (5 nm) / Pd (20 nm) / Au (100 nm)] used to globally modify the charge carrier density of the WSe_2 flake and to

achieve ohmic contacts.

In a first measurement step, the source-drain current was monitored as a function of the top gate voltage (V_{TG}) at a temperature of T = 4 K as shown in Figure 1c. The current increases at higher negative values of V_{TG}, indicating hole conduction across the WSe_2 channel. At top gate voltage values below – 6 V, the current voltage characteristics across the source-drain contacts show a linear behaviour, as presented for select values of (V_{TG}) in the inset of Figure 1c. One of the principal challenges in developing quantum devices in 2D semiconductors is realizing good electrical contacts. Thus, when the temperature was further reduced (T = 1.5 K), by using a three-terminal measurement scheme, the contact resistance of the source and drain were individually measured as a function of (V_{TG}) as seen in Figure 1d. The importance of the top-gate for achieving high quality contacts is evidenced by the low contact resistance measured when $V_{TG} = -10$ V. At this top-gate voltage, a contact resistance of 404 Ω was measured for the source contact and 1240 Ω for the drain contact.

We then investigated the influence of the local control gates on the transport properties of the device in a dilution refrigerator with a base temperature below 10 mK. Specifically, the pair of gates $V_{G_{3L}}$ and $V_{G_{3U}}$ (right-most control gates in the inset of Figure 1b) were studied while all other control gates were grounded (Figure 2). A bias voltage of 500 μV was applied to the source contact, while the drain contact was grounded. A gradually increasing voltage was applied to both $V_{G_{3L}}$ and $V_{G_{3U}}$ to create a channel by locally depleting the WSe_2 flake of holes in the areas directly above the two control gates. Keeping $V_{G_{3L}}$ at 15.12 V, $V_{G_{3U}}$ was varied, while the source-drain current I was monitored, as shown in Figure 2a (blue dotted curve). The source-drain current decreased as a function of $V_{G_{3U}}$ until $V_{G_{3U}} = 15.6$ V, when it suddenly increased, and, as $V_{G_{3U}}$ is further increased, the current eventually pinches off. We demonstrate below that it is related to the nano-constriction acting as a non-invasive probe of the charge of a nearby incidental quantum dot formed by the potential landscape created by impurities and defects in the environment around the WSe_2 layer[23, 26].

Figure 2b illustrates the model for the blue current trace characteristics observed in Figure 2a. A nearby

quantum dot has an initial population of N holes. As a larger positive voltage is applied to the local control gate $V_{G_{3U}}$, the width of the channel formed between $V_{G_{3U}}$ and $V_{G_{3L}}$

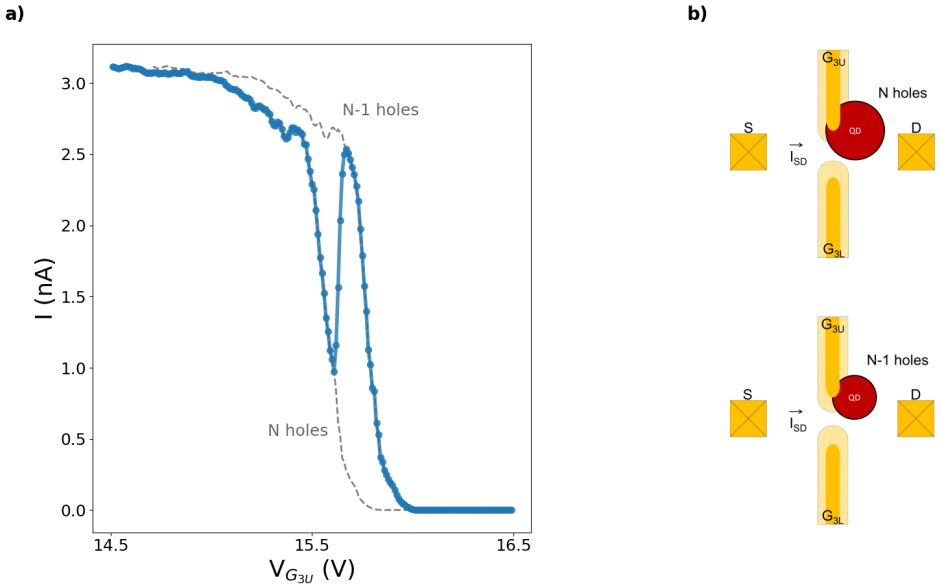

FIG. 2. (a) The blue dotted curve is the source-drain current as a function of the local control gate G_{3U}, while the local control gate $G_{3L} = 15.12$ V. The grey dashed curves are guides for two distinct quantum dot populations N and N-1, as indicated. (b) Schematic explanation of the result observed in (a), where a change in the hole population of a nearby quantum dot affects the channel width and the source-drain current. T $<$ 10 mK.

decreases, resulting in a decrease of current. At the same time, $V_{G_{3U}}$ controls the chemical potential of the nearby quantum dot and can therefore remove holes from it by applying a larger positive voltage. At a specific gate voltage, the population of the quantum dot transitions from N holes to $N-1$ holes, resulting in a widening of the channel and, as a result, a sudden increase in current through the charge detector.

Assuming no change in the number of holes (N) in the quantum dot as a function of gate voltage, the current is expected to follow the leftmost grey dashed curve in Figure 2a. If a hole is removed from the quantum dot, which would be therefore populated by N-1 holes, a larger voltage applied to $V_{G_{3U}}$ would be needed to achieve the same result (rightmost grey dashed curve). Thus, the jump between the two gray curves indicates a switch between a nearby quantum dot population of N and N-1 holes.

To demonstrate that the observed step in the source-drain current of Figure 2 is caused by a change in the charge population of a nearby quantum dot, we studied the evolution of the

charge detection step as a function of $V_{G_{3U}}$ for different values of $V_{G_{3L}}$ between 15 V (dark red curve) and 15.4 V (dark blue curve) as shown in Figure 3a. We observe that as $V_{G_{3L}}$ increases, the constriction pinch-off voltage decreases as a function of $V_{G_{3U}}$, while the voltage at which the charge transfer step occurs remains mostly constant. This indicates that the origin of the step is distinct from the nano-constriction. In addition, we note that a current peak is still visible, but with considerably less amplitude, after the detector is pinched-off for higher $V_{G_{3L}}$ values. We attribute this behaviour to resonant tunneling through a single energy level in the nearby quantum dot in the Coulomb Blockade regime.

To investigate this further, we extract the position of three distinct events in each current trace of Figure 3a: the first pinch-off, the second pinch-off and the charge transfer step. The first pinch-off point is extracted by taking a linear regression of the initial downward slope of the current and obtaining its x-intercept. It represents the point in gate voltage where the current would be zero if there was no change in the hole occupation of the nearby quantum dot. Similarly, the second pinch-off point is the x-intercept of the linear regression of the current's second downward slope, which occurs because a hole has been ejected from the nearby quantum dot. The charge transfer step is taken to be the middle point between the current's local minimum and local maximum around the step. This represents the gate voltage at which the chemical potential of the quantum dot lies exactly at the midpoint between the source and drain leads. An example of this is illustrated in Figure 3b. This analysis is performed for all values of $V_{G_{3L}}$ and plotted in Figure 3c. The slope associated to the first pinch-off point and the charge transfer step are each constant as a function of $V_{G_{3L}}$ and have values of -1.7 ± 0.1 $V_{G_{3U}}/V_{G_{3L}}$

and -0.34 ± 0.03 $V_{G_{3U}}/V_{G_{3L}}$ respectively. The difference in slopes between the linear dependencies of these events (first pinch-off, and charge transfer) further indicate that the origin of the charge transfer step and the nano-constriction are independent. Looking at the extrapolations associated to the second pinch-off point, we observe a change in slope at $V_{G_{3L}} = 15.22$ V, the voltage where the charge transfer step transitions into a Coulomb blockade peak, associated to resonant tunneling through the quantum dot. The slope corresponding to the second pinch-off point in the charge detection regime (-1.6 ± 0.2 $V_{G_{3U}}/V_{G_{3L}}$) is similar to the slope associated to the first pinch-off point, suggesting its origin being the nano-constriction. However, in the Coulomb blockade regime, the slope corre-

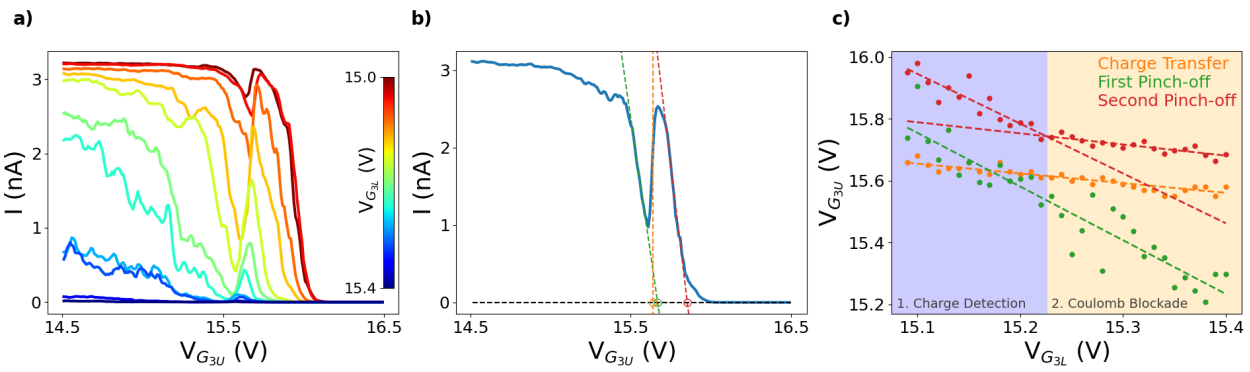

FIG. 3. (a) Source-drain current as a function of the local control gate V_{G3U}. Curves were taken for different values of V_{G3L} ranging from 15 V (dark red) to 15.4 V (dark blue). Experimentally, curves were taken at an interval of $\Delta V_{G3L} = 0.01$ V but for clarity, an interval of $\Delta G_{3L} = 0.05$ V is shown here. (b) An example of how the "position" of the first pinch-off (green), the second pinch-off (red) and the charge transfer step (orange) are obtained. The trace is taken when the voltage on $V_{G3L} = 15.12$. (c) The position of the first pinch-off (green), the second pinch-off (red) and the charge transfer step (orange) plotted as a function of V_{G3L} along with fitted linear regression. $T < 10$ mK.

sponding to second pinch-off (-0.35 ± 0.05 V_{G3U}/V_{G3L}) no longer follows the first pinch-off, but instead it follows the charge transfer step. This is due to the fact that at $V_{G3L} > 15.22$ V the constriction is completely pinched off and we are measuring only resonant tunneling through the quantum dot. We note that the quantum dot transport is still present in the charge detection regime, however the signal is dominated by the transport through the nano-constriction.

The sensitivity of the charge detector, defined as the change of conductance through the nano-constriction caused by the addition or subtraction of a single hole in the nearby quantum dot in units of e^2/h, was tuned as a function of the voltage applied to V_{G3L} as can be seen in figure 4. An optimal value of $0.09e^2/h$ is reached when $V_{G3L} = 15.17$ V. At this point, the derivative of the current with respect to the gate voltage, dI/dV_{G3L}, is maximum, indicating that the sensitivity of the constriction to its electrostatic environment is highest. Table 1 compares this sensitivity with previously reported charge detectors using graphene and bilayer graphene devices (dot-detector distances ranged from 35 nm to 150 nm), suggesting that TMDs show promising prospects of being used in charge detection

scheme based on nano-constrictions. We note that the high sensitivity of the TMD device in this work can be partially attributed to the close proximity of the incidental quantum dot to the detector.

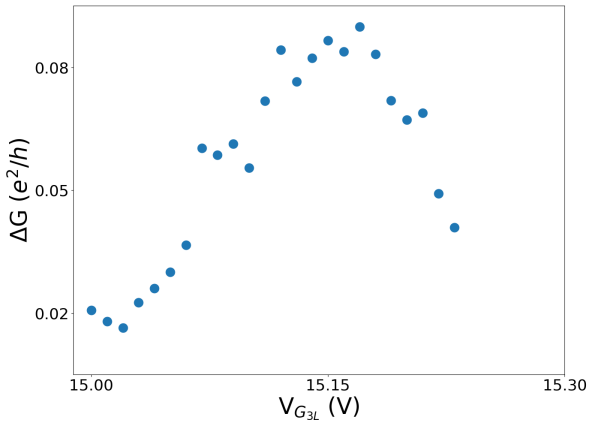

FIG. 4. The charge detection sensitivity (ΔG) of the measured device as a function of the voltage applied to G_{3U}.

In summary, we fabricated van der Waals heterostructure devices where we electrostatically define nano-constrictions in monolayer WSe_2. Our fabrication technique results in very low contact resistance, which allows the study of transport properties through the constrictions. By monitoring the current in a nano-constriction, we demonstrate for the first time using TMDs, the possibility of using such a device as a charge sensor for nearby quantum dots. The sensitivity of the WSe_2 is comparable to similar devices implemented in graphene and bilayer graphene. Further material and device optimisation is required to realize more tunable quantum circuits with highly sensitive charge detection using TMDs. These results pave the way for future the development of complex quantum circuits, where charge detectors can be integrated into gated quantum dot architectures.

TABLE I. Comparison of the charge detector sensitivity (ΔG) in various 2D material devices.

Reference	ΔG (e^2/h)	Material
Appl. Phys. Lett. (2008)[11]	10^{-4}	Graphene
Appl. Phys. Lett. (2010)[12]	< 0.1	Graphene
Phys. Status Solidi B (2011)[15]	0.005	BLG
Phys. Rev. B (2011)[13]	0.02	Graphene
Nat. Commun. (2013)[14]	0.002	Graphene
Nano Lett. (2019)[16]	0.2	BLG
This work (2022)	0.09	ML WSe_2

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4.3 Conclusion

In this chapter, we discussed the importance of charge detection and demonstrated that the local gate pattern described in chapter 3 can be used to create a nano-constriction in the WSe_2 flake to detect the change of charge occupation of a nearby quantum dot. The importance of this work comes from the fact that it constitutes the first demonstration of such devices in TMDs, an important goal towards realizing quantum circuits based on TMDs. Although this detection scheme was used to detect charge fluctuations in an incidental quantum dot, we anticipate that it is readily applicable to gate-defined TMD quantum dots.

Chapter 5

Quantized conductance in monolayer tungsten diselenide

5.1 Conductance across a 1D channel

The resistance of a classical two-dimensional conductor can be expressed using Ohm's law, $R = \rho L/W$, where ρ is material dependent and describes its resistivity, and L and W are geometric factors describing the length and width of the device, respectively. This definition for resistance is only applicable when the conductor is operating in the classical regime, when the characteristic length scales of the system (the mean free path for example) are much smaller than the device dimensions. In this regime, scattering events dictate the velocity at which charge carriers move in the material, and hence, they determine the resistivity and resistance. However, as the dimensions of the device (L and W) approach the size of these characteristic length scales and scattering events are limited, the resistance diverges away from Ohm's law.

In a regime where the mean free path of the charge carriers is larger than their distance travelled (ballistic regime), the conductance of the device obeys what is known as the Landauer formula and is given by [77, 78]:

$$G = \frac{ge^2}{h}N$$

where e is the elementary charge, h is the Plank constant, N is the number of transport channels, and g is the degeneracy of the available transport channels (for example, 2 for spin degenerate channels).

This formalism can be derived by considering charge carriers that are constrained in a well along the y and z directions, but free to move along the x-direction. The resulting confinement potential can be written as:

$$V(x,y,z) = \begin{cases} 0, & 0 < z < t,\ 0 < y < W,\ \text{and } \forall x \\ \infty, & \textit{otherwise} \end{cases}$$

This confinement potential can be thought of as a two-dimensional material with a thickness t, and an additional confinement which forces the charge carriers to move in a 1D channel with a width W. The energy eigenvalues of the resulting Hamiltonian are then $E = E_{y,z} + \hbar^2 k_x^2/2m^*$ where $E_{y,z}$ are the energies corresponding to a square well:

$$E_{y,z} = \frac{\hbar^2}{2m^*}\left[\left(\frac{n_z\pi}{t}\right)^2 + \left(\frac{n_y\pi}{W}\right)^2\right]$$

where n_y and n_z are positive integers representing the subband indices. In a 2DM, t is typically on the order of angstroms and is therefore much smaller than W. As a result, there exists many eigenstates corresponding to the cases where $n_z = 1$ with lower energies

than the eigenstate with $n_z = 2$ and $n_y = 1$. Therefore, we can ignore the n_z degree of freedom and consider a total energy of:

$$E = \frac{\hbar^2}{2m^*}\left(\frac{n_y \pi}{W}\right)^2 + \frac{\hbar^2 k_x^2}{2m^*}$$

Connecting this device to two electrical contacts at $x = \pm\infty$ and applying a voltage difference of $V = (\mu_1 - \mu_2)/e$ between the two results in a flow of current. To calculate this total current, let's evaluate the current carried by each subband, n_y, separately, call it i, and then add them up.

$$i = e\int_{\mu_2}^{\mu_1} D(E)v(E)T(E)dE$$

In this expression, $D(E)$ is the 1D density of states, $v(E)$ is the velocity of the charge carriers moving in 1D, and $T(E)$ is the transmission probability of the subband in question. When the bias voltage is small enough compared to the Fermi energy E_F, we can evaluate all of these terms at the Fermi energy which gives:

$$i = eD(E_F)v(E_F)T(E_F)(\mu_1 - \mu_2)$$

In a system with g-degeneracies, the 1D density of states is given by:

$$D_{1D}(E) = \frac{g}{h}\sqrt{\frac{m^*}{2E}}$$

The velocity of the electrons at energy E is defined as:

$$v(E) = \frac{1}{\hbar}\frac{dE}{dk_x} = \frac{1}{\hbar}\frac{2\hbar^2 k_x}{2m^*} = \frac{\hbar}{\hbar}\sqrt{\frac{2E}{m^*}} = \left(\frac{h}{g}D_{1D}(E)\right)^{-1}$$

Putting the expression for velocity and the density of states together, we obtain:

$$D_{1D}(E)v(E) = \frac{g}{h}$$

and the single subband current gives:

$$i = \frac{e}{h}T(E_F)(\mu_1 - \mu_2)$$

For the total current, we include the contributions from every occupied subband ($E(k_x = 0) < E_F$) where we denote this total number as N. This results in:

$$I = \frac{e}{h}\sum_{n_y=1}^{N} T_{n_y}(E_F)(\mu_1 - \mu_2)$$

If there is no backscattering, the transmission probability is unity, therefore $\sum_{n_y} T_{n_y} = N$, and the total current now reads as:

$$I = \frac{ge}{h}(\mu_1 - \mu_2)N = \frac{ge^2}{h}VN$$

We then find that the conductance $G = I/V$ is the Landauer formula as introduced earlier:

$$G = \frac{ge^2}{h}N$$

demonstrating that each occupied subband contributes ge^2/h to the conductance.

Devices can be fabricated such that they closely resemble the confinement potential described during the derivation of the Landauer formula, where the width of the confinement,

and hence the width of the 1D channel, is tunable by electrostatic gating. The first experimental results [79] showed that conductance across a quantum point contact in a two-dimensional electron gas of a gallium arsenide-aluminum gallium arsenide (GaAs-AlGaAs) heterostructure was quantized in steps of $2e^2/h$ as expected from the Landauer's formula and the degeneracy (2-fold spin degeneracy) of the heterostructure (Figure 5.1a). Demonstrations of quantized conductance have also now recently been reported in graphene and bilayer graphene [82, 91] where the intervals between conductance plateaus are spaced out by $4e^2/h$ (Figure 5.1b), corresponding to the expected 4-fold degeneracy coming from the 2 spin and 2 valley degrees of freedom in this material.

5.2 Observation of quantized conductance in TMDs

Although much progress has been made in the field of monolayer TMDs regarding sample cleanliness, it is still lagging behind other materials such as graphene or GaAs, making it hard to achieve the ballistic regime and observe phenomena such as quantized conductance. Nonetheless, quantized conductance has only been observed recently in few layer TMDs (MoS_2 [48, 92] and WSe_2 [49]), and once in monolayer MoS_2 [93]. For these particular TMDs, due to the spin and valley locking, one would expect conductance plateaus to occur at intervals of $2e^2/h$. Surprisingly, in all referred cases, the quantization was in intervals of e^2/h suggesting the lifting of the spin or valley degeneracy, however this observation was never adequately explained. In this chapter, we discuss the fabrication and design of a new device architecture which leads to quasi-ballistic transport across a long 1D channel. Using this device architecture, we can then explore the quantized conductance mystery in TMDs, more specifically, in monolayer WSe_2.

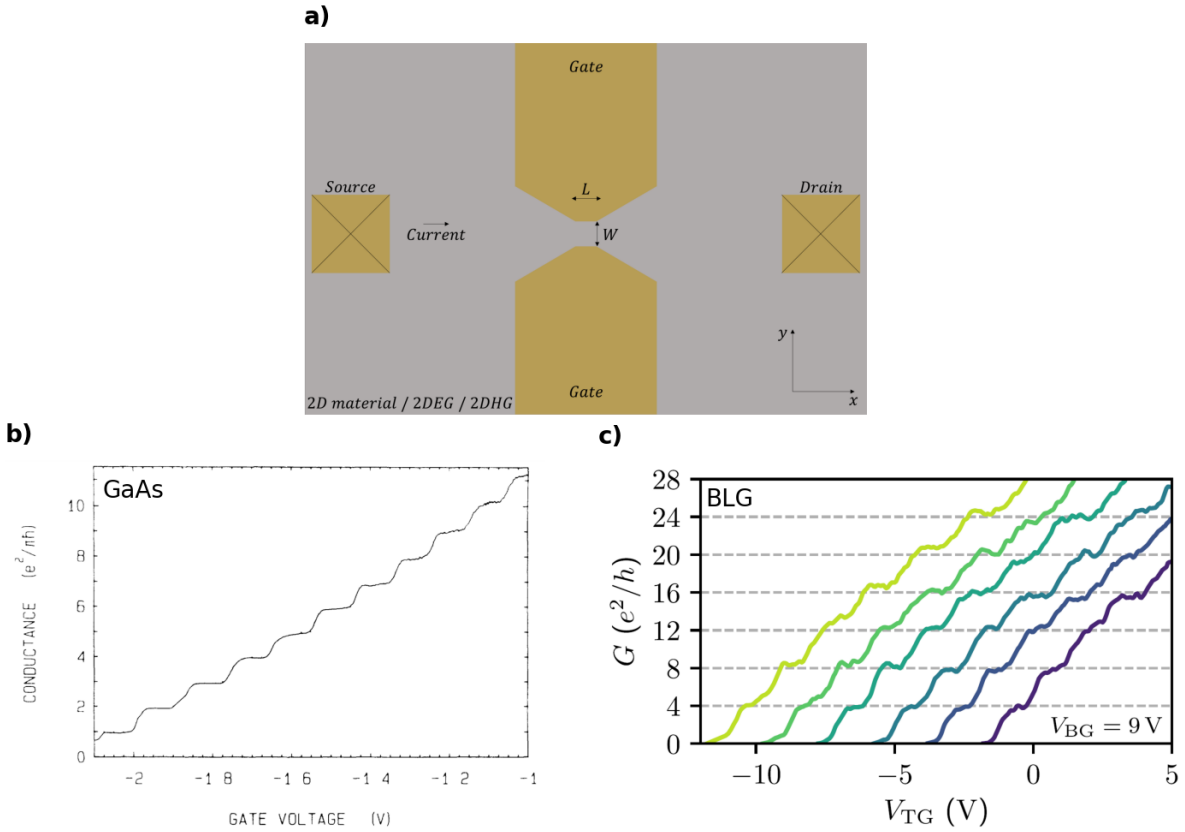

Figure 5.1: (a) Cartoon of a gate structure that could be responsible for the potential described in section 5.1. (b) Conductance as a function of gate voltage for a 2DEG in a GaAs/AlGaAs heterostructure showing clear quantization in steps of $2e^2/h$. Adapted from Ref. [79]. (c) Conductance as a function of gate voltage for a sheet of bilayer graphene at different carrier densities showing clear quantization in steps of $4e^2/h$. Adapted from Ref. [82].

5.3 Device architecture

In the previous two chapters, the studied nanostructures originate from quantum dots that have been formed in the device's local potential fluctuations. Although we have shown that

these incidental quantum dots are still controllable, the randomness of their position makes them impractical for quantum circuits. With the goal to create gate-defined quantum dots with well known dot locations, we altered the device structure.

The heart of the device architecture remains the same; a monolayer WSe_2 flake is encapsulated by two hexagonal boron nitride flakes and is bottom contacted by Cr/Pt contacts. This hBN/WSe_2/hBN heterostructure is fabricated on top of the same local gates as discussed in the previous chapters.

In the previous architecture as discussed in chapters 3 and 4, we used one single accumulation gate to globally introduce charge carriers in the WSe_2 sheet, which consequently populates all the potential minima in the WSe_2 flake resulting in multiple quantum dots (Figure 5.2a), and tangled transport data. To remedy this situation, we separated the one global accumulation gate into 3 main components: a global back gate, a split gate, and contact gates.

The entire device is fabricated on top of a degenerately p-doped silicon (Si) substrate with 285 nm of thermally grown silicon oxide (SiO_2). The silicon being conductive, is used as a global accumulation gate, and the silicon oxide is used as a gate dielectric. Therefore, by applying a potential difference between the silicon and the TMD flake, we can tune the global carrier density of the flake, as done before with the global top gate. Again, this results in many incidental quantum dots scattered across the device. To limit the number of quantum dots participating in the transport experiments, a two-piece global gate with a small separation (200 nm $\times$ 600 nm) is patterned on top of the fabricated device. These gates, which we call split-gates, are used to deplete the WSe_2 flake of carriers in the areas directly underneath the gates. When a bias voltage is applied between the source and drain contact, the charge carriers are then forced to pass through the gate-defined channel where there are fewer or zero incidental quantum dots (Figure 5.2b). A second set of global

accumulation gates are also patterned onto the top hBN flake such that they overlap the electrical contacts. These contact gates are used to bring the electrical contacts into the ohmic regime. A scanning electron micrograph of the top-gate structure is shown in Figure 5.2c where we have outlined the underlying contacts (blue) and local gates (red). The local gates extend past the split gate so that they may be used to create gate defined quantum dots.

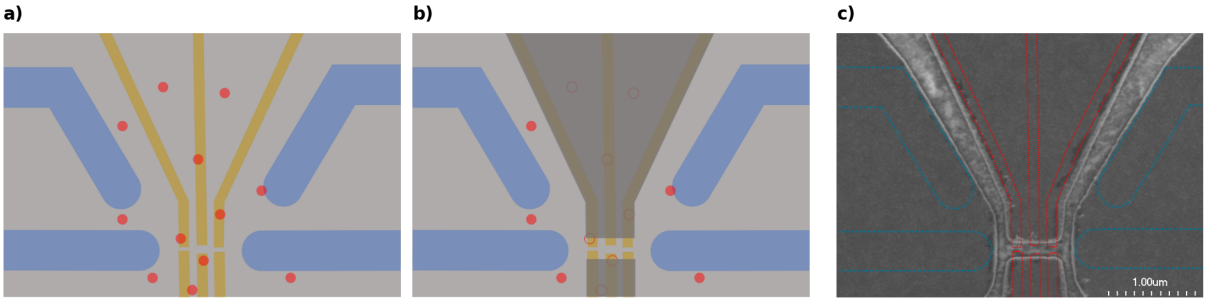

Figure 5.2: (a) Illustration of the device architecture and non-uniform 2DHG when a global accumulation gate is used to accumulate carriers into the WSe_2 layer (grey background). Current can flow from the source to the drain contacts (blue) while tunneling through quantum dots (red circles) and not necessarily between the local gates (gold) as desired. (b) Adding a split gate (dark grey) on top of the local gates forces the charge carriers to conduct in the channel defined by the gates. (c) SEM micrograph of the top gate structure where the contacts and the local gates are outlined in blue and red, respectively.

5.4 Results

The goal of the discussed architecture above is to create a clean and uniform two-dimensional hole gas where we can then use local control gates to create and study gate-defined quantum dots. The nature of the split-gate also creates a gate-defined one-dimensional channel with a lithographic width of 200 nm and a length of 600 nm. This allows us to study WSe_2

hole transport through a 1D channel and is the subject of the following article[1].

5.4.1 Anomalous conductance quantization of a one-dimensional channel in monolayer WSe_2

Statement of contributions

JBC, AB, and LG designed the device architecture which is presented in this manuscript. JBC, PB, and JL participated in the fabrication of the top gates (split gates and contact gates). JBC was responsible for the fabrication of the device, the experimental measurements, and the data analysis. The first draft (excluding the theory contribution) was written by JBC and LG, then edited with ALM's help. The theoretical component of the manuscript was completed by Jarosław Pawłowski (JP), Daniel Miravet (DM), MB, and PH. KW and TT grew and provided the hexagonal boron nitride.

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Anomalous conductance quantization of a one-dimensional channel in monolayer WSe_2

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Among quantum devices based on 2D materials, gate-defined quantum confined 1D channels are much less explored, especially in the high mobility regime where many body interactions play an important role. We present results of measurements and theory of conductance quantization in a gate-defined one dimensional channel in a single layer of transition metal dichalcogenide material WSe_2. In the quasi-ballistic regime of our high mobility sample, we report conductance

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quantization steps in units of e^2/h for a wide range of carrier concentrations. Magnetic field measurements show that as the field is raised higher conductance plateaus move to accurate quantized values and then shift to lower conductance values while the e^2/h plateau remains locked. Based on microscopic atomistic tight-binding theory, we show that in this material, valley and spin degeneracies result in 2 e^2/h conductance steps for non-interacting holes, suggesting that symmetry breaking mechanisms such as valley polarization dominate the transport properties of such quantum structures.

Realization of quantum devices based on two-dimensional (2D) materials has attracted significant interest in recent years [1, 2]; in particular, advances in fabrication techniques for devices based on transition metal dichalcogenides (TMDs) enabled the realisation of building blocks of quantum circuits such as gate-controlled quantum dots in monolayer and few layer MoS_2[3–5] and WSe_2[6, 7] as well as one-dimensional (1D) channels based on split gate technology[8–12]. 1D channels are of great interest in quantum information science because they have been established as valuable tools for non-invasive readout of semiconducting charge and spin qubits in GaAs[13], SiGe[14], graphene[15–18], bilayer graphene[19, 20] and WSe_2[21]. In 1D channels, the Landauer-Buttiker formalism explains the quantized conductance in units of n e^2/h, where n is the number of available transport channels, which depends on the degeneracies of the system; for example, 2-fold spin degeneracy for GaAs[22] and 4-fold spin and valley degeneracy for graphene[23]. Beyond this picture, much less is known about the mechanisms through which interaction effects can add complexity and play a role in transport anomalies [22]. Therefore, 1D channels based on high mobility 2D materials offer the possibility to access interaction regimes.

Here, we present results of investigation of the first 1D channel based on high mobility monolayer WSe_2, and find that the conductance is quantized in units of e^2/h. This is surprising since in monolayer TMDs, due to spin-valley locking, we expect conductance quantization for non-interacting holes in units of 2 e^2/h. Our results are in agreement with reports using few-layer MoS_2[8, 10], trilayer WSe_2[12] and monolayer MoS_2[9], but the origin of the e^2/h quantization remains unexplained. We attribute this broken valley and spin degeneracy to the formation of valley and spin polarised states of holes, which have been predicted for WS_2 [24, 25] and in laterally gated MoS_2 quantum dots [26, 27].

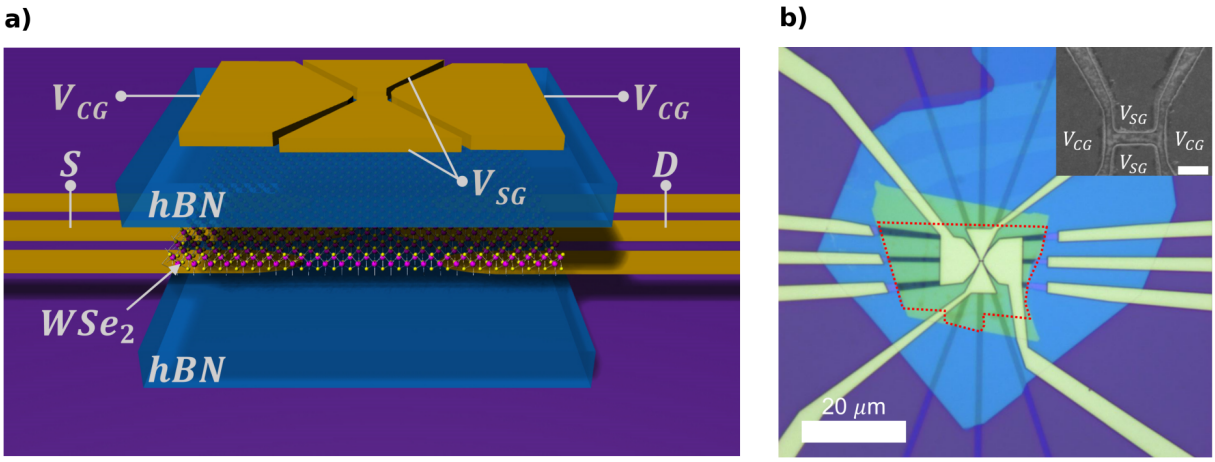

FIG. 1. (a) Schematic of the monolayer WSe_2 device structure. (b) Optical micrograph of the device used in this study. The WSe_2 monolayer flake is outlined in red for clarity. Inset: Scanning electron micrograph of the top gate structure (scalebar is 400 nm). The left and right gates are used to activate the contact region (V_{CG}). The top and bottom gates (V_{SG}) are used to form the 1D channel. The 1D channel is lithographically defined to have a width of 200 nm and a length of 600 nm.

Although there is already a substantial body of work explaining non-universal conductance quantization, a full understanding of the so called "0.7 anomaly" in quantum point contacts remains elusive and is assumed to be due to electron-electron interactions [28–37]. While the full theory of conductance in the presence of hole-hole interactions is in progress, here we show a complete single-particle model based on atomistic tight-binding theory for holes in a WSe_2 monolayer, confined in an electrostatically-defined 1D channel. It demonstrates that a channel potential does not break valley degeneracy and without hole-hole interactions conductance is expected to be quantized in units of 2 e^2/h. Hence the observed anomalous quantization in units of e^2/h can likely be explained in terms of broken symmetry valley-polarized ground state induced by interactions [24, 25, 38].

The device was assembled on a p-doped silicon substrate with 285 nm of thermally grown silicon dioxide (SiO_2). Using standard dry transfer methods[39, 40], a flake of hexagonal boron nitride (hBN) (26 nm) was picked-up with a polypropylene carbonate (PPC) coated polydimethylsiloxane (PDMS) stamp and transferred onto lithographically patterned local gates. Electrical contacts [Cr (2 nm) / Pt (8 nm)][41] were subsequently patterned on top of the hBN. To remove any contaminants on the surface of the hBN and the electrical

contacts, the sample was thermally annealed in a vacuum furnace (10^{-7} Torr) at 300 °C for 30 minutes and further cleaned mechanically using an atomic force microscope tip (AFM) in contact mode[7, 21, 42, 43]. A second polymer stamp was used to subsequently pick-up an hBN flake (34 nm) then a monolayer WSe_2 flake. To ensure proper contact to the electrical contacts, the stack of flakes and stamp were placed in an AFM such that the surface of the WSe_2 flake was exposed where it was then mechanically cleaned using an AFM tip. The hBN/WSe_2 stack was then dropped off onto the patterned contacts. At this stage, the device was thermally annealed in a vacuum furnace following the same recipe as before. A final lithographic step was performed to pattern the top gates which are separated into four components. Two of the top gates, labelled as V_{CG} in Figure 1a, cover the area where there is overlap between the WSe_2 flake and the electrical contacts, and are used to activate the electrical contacts. The two other top gates, labelled as V_{SG} in Figure 1a, are used to define the 1D channel in the WSe_2 with a lithographic width of 200 nm and length of 600 nm.

We first demonstrate that we can create a conduction region with sufficiently low resistance to study quantized conductance. Figure 2a is a 4-point measurement of the device resistance R_{SD} as a function of the split gate voltage V_{SG} at a source-drain bias of 20 μV and constant back-gate voltage $V_{BG} = -33\ V$. At low V_{SG}, when the voltages on the split gate are not sufficiently high to deplete the underlying WSe_2 regions from carriers, we measure a resistance of 480 Ω from which we are able to extract a contact resistance of 9.76 $k\Omega$ (see supplementary material section 1), a value that is comparable to others reported using more complex fabrication techniques[12, 44, 45]. As the voltage is increased on the split gates, we observe an increase in resistance indicating that a constriction has been formed and that holes are responsible for transport in the device.

The change in the conductance of the device in units of e^2/h as a function of the split gate voltage V_{SG} is shown in Figure 2b, from which we obtain a gate depletion value of $V_{SG} = 2.7\ V$. At this point, the 1D channel is formed, and the total measured resistance is 5030 Ω. When indicated, this back-gate dependent series resistance (see supplementary material section 3) is subtracted from the raw data to obtain the conductance related only to the 1D channel[9]. In Figure 2b, quantized conductance steps close to e^2/h and 2 e^2/h can be observed for a fixed hole concentration of 1.82×10^{12} cm^{-2} (see supplementary material section 2). Tuning the concentration allows us to reach two different regimes, as

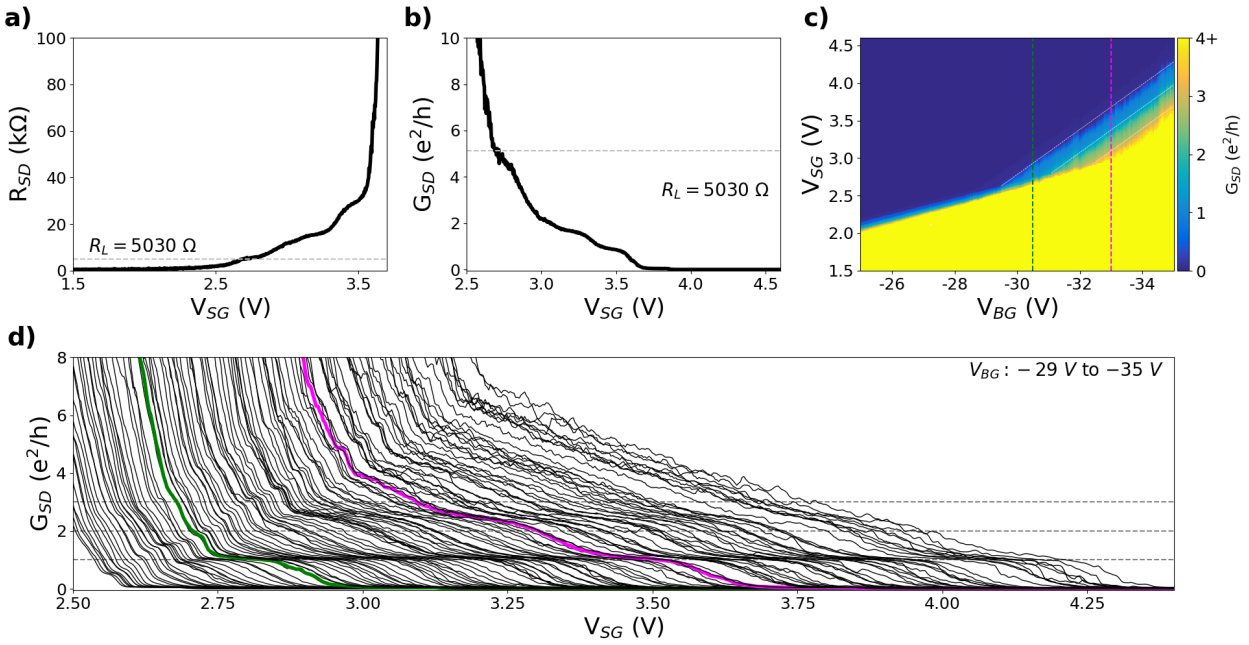

FIG. 2. (a) 4-point measurement of resistance vs. split gate voltage (V_{SG}) at $V_{BG} = -33$ V. The dashed line indicates the resistance where the channel is formed (at depletion). (b) Conductance in units of e^2/h vs. split gate voltage (V_{SG}) at $V_{BG} = -33$ V. The dashed line represents the conductance where the channel is formed (at depletion). (c) Color map of conductance as a function of split gate voltage V_{SG} and back-gate voltage V_{BG}. A lead resistance (resistance at depletion) is subtracted. (d) Line cuts from (c) plotted in a "waterfall" style indicating a first step at e^2/h and a second step around 2 e^2/h. The left most trace is taken at $V_{BG} = -29$ V and the right most trace is taken at $V_{BG} = -35$ V. The green and magenta lines are highlighted by similarly colored dashed lines in (c) and correspond to back-gate voltages of −30.5 V and −33 V respectively. These two curves feature the regimes where we observe the 1 e^2/h plateau (green), and the 1 e^2/h and 2 e^2/h plateaus (magenta).

demonstrated in Figure 2c. At higher hole concentrations, below $V_{BG} = -30\ V$, we see the appearance of the first conductance step at e^2/h. As the carrier concentration increases

(V_{BG} decreases), the difference between the depletion and pinch-off values also increases and we observe the appearance of a second conductance step at a value of 2 e^2/h. These conductance steps are more clearly observed in a waterfall plot as shown in Figure 2d. The observation of quantized conductance through the 600 nm long channel along with the high measured field effect carrier mobility of $\mu_{FE} = 7900\ cm^2/Vs$[12, 41, 45, 46] (see supple-

mentary material section 2), hints towards quasi-ballistic transport and demonstrates that a high quality monolayer WSe_2 sample has been achieved. At lower carrier concentrations, we observe the onset of a distinct transport regime that remains to be elucidated by further investigations (see supplementary material section 6).

We further investigate the quantized conductance features by applying a magnetic field perpendicular to the plane of the two-dimensional material. Due to the large hole spin and valley g-factor which has been reported to be up to 12 in monolayer WSe_2[47], we explore the low magnetic field regime between -100 mT and 100 mT (Figure 3a) to eliminate any possible spin or valley polarisation occurring due to a small magnetic field offset at 0 T. The quantization remains constant at low field even at a high resolution of 4 mT. We therefore conclude that the measured lifting of spin and valley degeneracies at low fields is inherent to this particular system leading to a ground state where only one conducting channel is available. At higher fields, as depicted in Figure 3b, we observe that the first plateau remains constant between -5 T and 8 T with a very small correction around 0 T which we attribute to magnetoresistance effects in the leads. This magnetoresistance correction is more significant at higher conductance, but after 1.5 T we observe the second and third quantization plateaus aligning with the values of 2 e^2/h and 3 e^2/h. This data set demonstrates that each conductance channel up to the third one allows transport for only one quantum of conductance. We cannot determine, however, what is the ground state in terms of spin or valley. Additionally, at higher magnetic fields, we observe an evolution of the second and third plateaus in which they lower in conductance and seem to merge into the first plateau. No such change in conductance is observed for the first plateau. Measurements performed at 10 mK in a dilution refrigerator show the same behaviour (see supplementary material section 4).

In order to determine whether the anomalous quantization behaviour originates from the spin-valley locking mechanism in TMD's, we developed a single-particle model of a 1D channel. To calculate single-hole states, we use a tight-binding model for WSe_2 monolayer [26, 48–50] in a basis of three d-orbitals localized on tungsten atoms and three p-like orbitals describing Se_2 dimers (6 even orbitals in total).

A single-particle channel wavefunction for a hole state s satisfies the Schrödinger equation

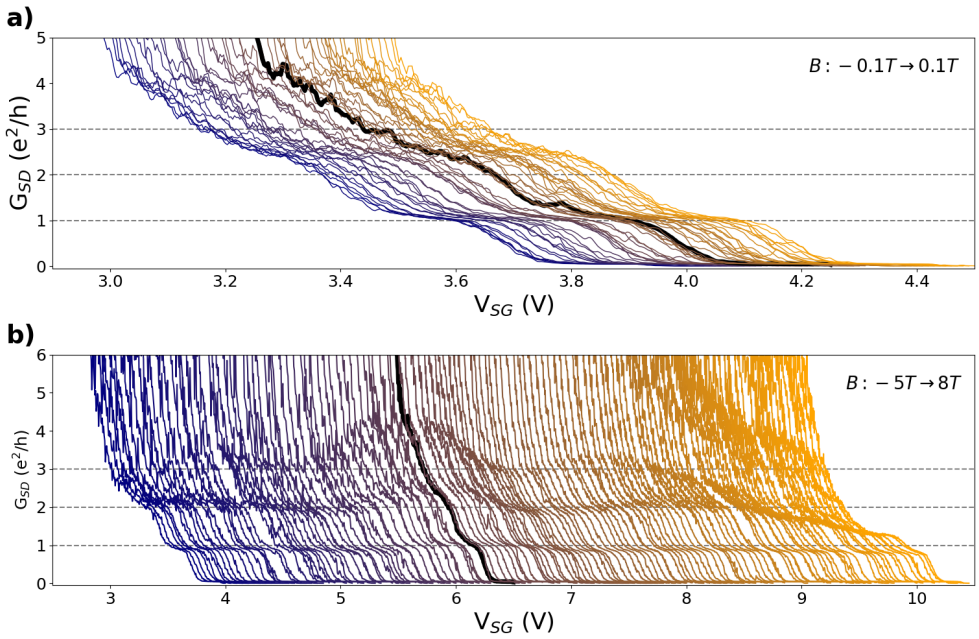

FIG. 3. (a) Dependence of the quantized conductance plateaus on a perpendicular low magnetic field ranging from −100 mT to 100 mT and a resolution of 4 mT. (b) Dependence of the quantized conductance plateaus on a perpendicular magnetic field ranging from –5 T to 8 T. In both panels, a horizontal offset is introduced between adjacent line traces for clarity. $V_{BG} = -33.2$ V for all runs with the corresponding lead resistance of $R_L = 5029\ \Omega$ subtracted.

[49, 50]:

$$\left(H_{\text{bulk}} + |e|U^{\text{ch}}\right)|\Psi^s\rangle = E^s|\Psi^s\rangle, \tag{1}$$

where the channel is defined within the WSe_2 monolayer lattice and oriented along the x-axis of the elongated, rhombohedral computational box presented in Fig. 4(a). The 1D electronic confinement is determined by an applied external gate-defined potential U^{ch}. A hole is free to move in the channel direction, while movement in the perpendicular direction is constrained by a Gaussian-like potential along the y-axis:

$$U^{\text{ch}}(y) = U_0\left(1 - \exp\left(-\frac{y^2}{2\sigma_y^2}\right)\right), \tag{2}$$

parametrized in our calculations by potential depth $U_0 = 100$ mV, and width $\sigma_y = 5$ nm (see Fig. 4(a)). Note that at the center of the channel, where holes localize, the potential is zero and increases as we move away from the center.

We define the finite computational box in a form of a rhomboid of the WSe_2 lattice. We wrap the computational box on a torus, apply the periodic (Born–von Karman) boundary

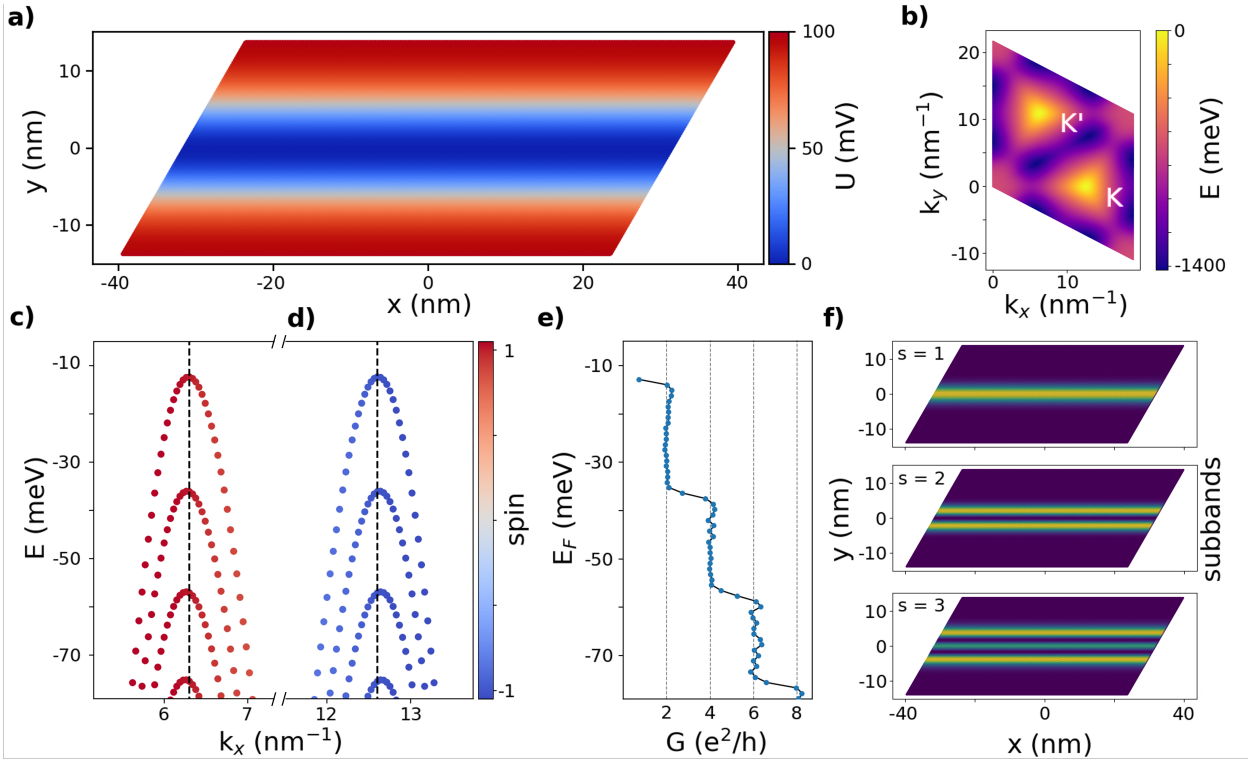

FIG. 4. (a) Computational rhombus representing WSe_2 monolayer with 1D gate-defined channel potential U^{ch} applied along the x-axis. (b) Valence band energy surface within the Brillouin zone with two maxima at K' and K points. (c,d) Single-particle states calculated within the tight-binding model for WSe_2 monolayer with applied 1D gate-defined channel potential U^{ch}. The hole eigenstates, characterized by their energy, wave vector k_x, and spin, form characteristic parabolic subbands located in (c) K' valley with spin-up (red dots), or (d) K valley with spin-down (blue dots). Subsequent subbands are used to calculate the channel conductance (d) via the Landauer formula. Resulting conductance curve has a characteristic stepped-like shape with subsequent plateaus at multiples of 2 e^2/h. Those states (numbered by s quantum number) are occupied by hole states with spatial densities (f) resembling harmonic oscillator modes.

conditions, and obtain a set of allowed, discretized k-vectors over which we diagonalize the bulk Hamiltonian H_{bulk}. The valence band (VB) wavefunction for each allowed k-vector is a linear combination of Bloch functions on the W and Se_2 dimer sublattices l ($l = 1, \ldots, 6$):

$$\left|\psi^{\text{VB}}_{k\sigma}\right\rangle = \sum_{l=1}^{6} A^{\text{VB}}_{k\sigma l} \left|\psi_{k,l}\right\rangle \otimes \left|\chi_{\sigma}\right\rangle , \tag{3}$$

where $|\chi_\sigma\rangle$ is the spinor part of the wavefunction, and

$$|\psi_{k,l}\rangle = \frac{1}{\sqrt{N}} \sum_{R_l=1}^{N} e^{i\mathbf{k}\cdot\mathbf{R}_l} \varphi_l(\mathbf{r} - \mathbf{R}_l) \tag{4}$$

are Bloch functions built with atomic orbitals φ_l. N is the number of unit cells, while $\mathbf{R}_l$ defines the position of atomic orbitals in the computational rhomboid. By diagonalising the 6 by 6 Hamiltonian H_{bulk} at each allowed value of k we obtain the bulk energy bands $E^{\text{VB}}_{k\sigma}$ and wavefunctions $A^{\text{VB}}_{k\sigma l}$. The topmost valence band energy surface is shown in Fig. 4(b), where two non-equivalent maxima, K and K' valleys, are clearly visible.

In the next step, we expand the channel wavefunction in terms of the lowest energy valence band states given by Eq. 3:

$$|\Psi^s_\sigma\rangle = \sum_k B^{\text{VB},s}_{k\sigma} \left|\psi^{\text{VB}}_{k\sigma}\right\rangle. \tag{5}$$

Finally, we solve the Schrödinger equation (1) with the potential term U^{ch} by converting it to an integral equation for the coefficients $B^{\text{VB},s}_{k\sigma}$, and obtain the single-hole eigenstates confined within the channel,

$$E^{\text{VB}}_{q\sigma} B^{\text{VB},s}_{q\sigma} + \sum_k B^{\text{VB},s}_{k\sigma} \sum_l \left(A^{\text{VB}}_{q\sigma l}\right)^* A^{\text{VB}}_{k\sigma l}\, U^{\text{ch}}_l(q,k) = E^s_\sigma B^{\text{VB},s}_{q\sigma}, \tag{6}$$

where $U^{\text{ch}}_l(q,k) = \frac{1}{N}\sum_{R_l=1}^{N} U^{\text{ch}}(\mathbf{R}_l) e^{i(\mathbf{k}-\mathbf{q})\cdot\mathbf{R}_l}$ is the Fourier transform of the channel confinement on each sublattice l. The structural and the tight-binding Slater-Koster parameters in the calculations are directly listed in the supplementary material, Section 7.

The channel states of energy E^s_σ are characterized by subband index s, by the spin σ, and also by the valley K or K' determined by the expectation value of the wave vector $\langle k_x\rangle \equiv k_x$ in the channel direction. They belong to two different valleys: K' with spin-up – Fig. 4 (c), and K with spin-down – Fig. 4 (d), creating degenerate spin-valley locked states. Characteristic parabolic subbands are formed due to the lateral quantization within the channel represented by different values of s quantum number.

We note that the VB maximum (for the free hole Hamiltonian H_{bulk}) is shifted to zero and the highest energy state (ground state for holes in the channel) is located below, at -12 meV. The second spin-valley pair (not presented) is split-off by 0.5 eV below on the energy scale by the strong intrinsic spin-orbit coupling present in this material.

After calculating the single-particle eigenstates of the Hamiltonian H, we are ready to numerically estimate the conductance through the 1D channel. For each subband s, we calculate the density of states within the given subband $\frac{dN_s}{dE}$, and then estimate the particle velocity as $v_s(E) = \frac{1}{\hbar}\frac{\partial E_s}{\partial k_x}$. The conductance, which combines contributions from states from different occupied subbands s filled up to the Fermi energy, is calculated using the 2-terminal Landauer formula [51]:

$$G(E_F) = \frac{e^2}{E_F}\sum_s \int_0^{E_F} dE \frac{1}{2}\frac{dN_s}{dE} v_s(E). \tag{7}$$

The factor 1/2 is due to the fact that we take only states with $k_x > K_x$ (or $k_x > K'_x$ for the second valley), i.e., active under the given source-drain bias. In the above formula we assume that no backscattering occurs. The calculated conductance is presented in Fig. 4(e). It has the conductance plateaus at multiples of 2 e^2/h. The corresponding charge densities for each subband are plotted in Fig. 4(f). The final result shows that a microscopic theory of a 1D channel predicts conductance steps in units of 2 e^2/h. Hence, we see that the measured e^2/h conductance quantization cannot be explained in the single-particle picture.

A possible explanation for the e^2/h conductance quantization can be obtained in terms of a broken symmetry valley-polarized ground state [24, 25, 38]. A valley polarized state is expected to be the ground state of a 2D hole gas in a single layer of WSe_2 for sufficiently strong interaction strength and hole density (in analogy to WS_2 [25]). The breaking of valley degeneracy naturally lifts the degeneracy of bands in the mean field picture. Therefore, conductance plateaus in conductance quantization are expected to be half of the degenerate system, giving e^2/h instead of 2 e^2/h steps as a function of Fermi energy. This might explain e^2/h plateau for large range of hole densities, as shown in Fig. 2(d).

In summary, we have fabricated high quality monolayer WSe_2 devices where an electrostatically confined 1D hole transport channel is formed. At low temperature, hole quasi-ballistic transport is observed, revealing an unexpected conductance quantization in steps of e^2/h instead of 2 e^2/h taking into account the electronic effects from the band structure of TMDs such as spin-valley locking. We have compared the experimental results to a single particle atomistic tight-binding model for holes in WSe_2 and demonstrated that a 1D confining potential does not reproduce the measured conductance quantization in units of e^2/h. Recent experiments[24] and theory[26] suggest the existence of a valley polarised state of the

hole gas in TMDs. Such a state would explain the measured plateau at e^2/h. A theoretical model which includes hole-hole correlations is therefore necessary to explain quantum transport in 2D TMDs. These results show that the electronic properties of monolayer TMDs are still insufficiently understood and require further research to elucidate.

ACKNOWLEDGMENTS

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Supplementary for anomalous conductance quantization of a one-dimensional channel in monolayer WSe_2

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Section 5: Reproducibility in a different measurement setup

Section 6: Transport in the low carrier density regime

Section 7: Tight-binding parameters

SECTION 1: 2-POINT MEASUREMENT AND CONTACT RESISTANCE

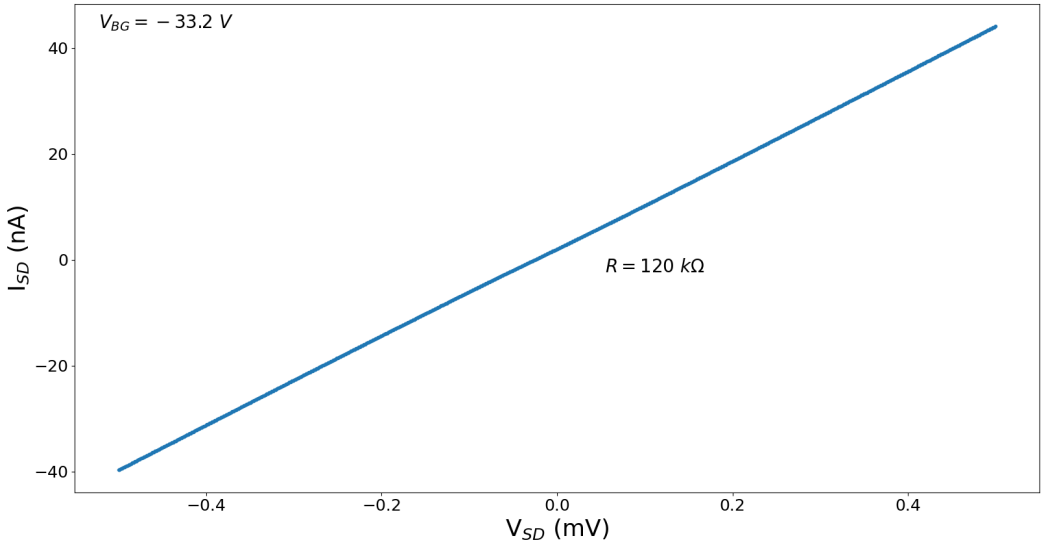

FIG. 1. 2-point measurement of the source-drain current as a function of the bias voltage indicating a total resistance of 120 kΩ. T = 4 K.

We performed 2-point IV measurements in addition to the 4-point measurements presented in the main text to obtain the contact resistance. The 2-point measurement yielded a resistance of 120 kΩ (Figure 1) which is a sum of the contact resistance (2 contacts), the RF line (connected to a single contact), and the channel resistance. From the 4-point measurement taken at a back-gate voltage of $V_{BG} = -33.2\ V$, the channel resistance is 480 Ω (Figure 2a in the main text). The RF line connected to one contact has a resistance of 100 kΩ. Therefore, the average contact resistance per contact is 9760 Ω.

$$R_C = \frac{1}{2}(R_{2-point} - R_{4-point} - R_{RF}) = 9760\ \Omega$$

SECTION 2: MOBILITY AND CARRIER DENSITY CALCULATION

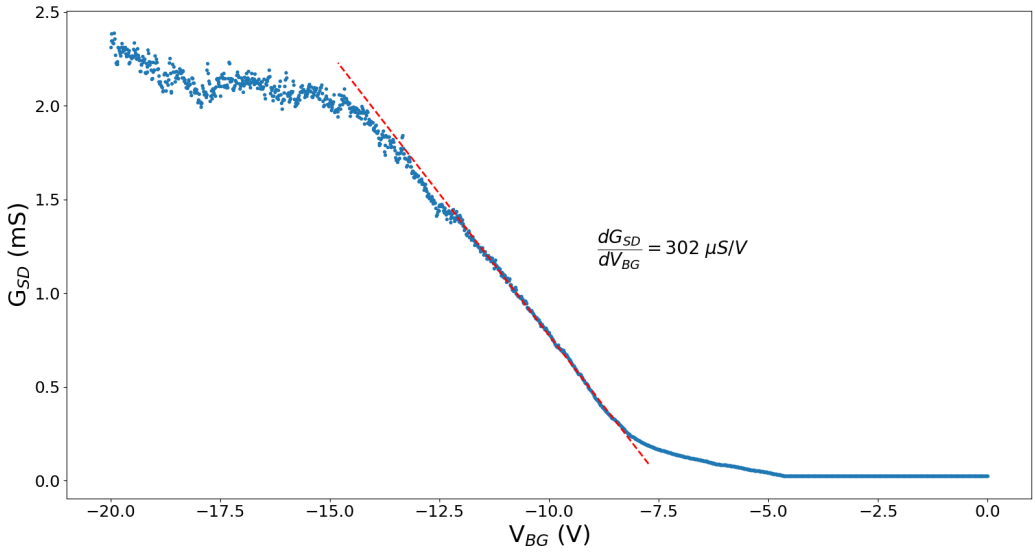

FIG. 2. 4-point measurement of the source-drain conductance as a function of back-gate voltage taken at 4K.

In a 4-point measurement scheme, we monitor the resistance as a function of back-gate voltage with the split gate turned off. The conductance (inverse of resistance) increases linearly as of $V_{BG} = -8\ V$. From this linear segment, we extract a slope of $-302\ \mu$S/V and a x-intercept of $V_{th} = -7.44\ V$, which corresponds to the threshold voltage. Using these values, we can estimate the field-effect mobility of our device and obtain the carrier concentrations for different values of V_{BG}. For calculating the mobility, we use:

$$\mu = \frac{dG_{SD}}{dV_{BG}} \frac{L}{w} \frac{1}{C_G}$$

where the ratio L/w is taken to be 1.3 (calculated from the geometry of the sample), and $\frac{dG_{SD}}{dV_{BG}} = -302\ \mu S/V$ (Figure 2). The gate capacitance per unit area, C_G, is obtained by considering that the dielectric between the WSe_2 and the back-gate is comprised of 285 nm of SiO_2 and 26 nm of hBN (confirmed by AFM). Therefore,

$$
\begin{aligned}
C_G &= \epsilon_0 \left(\frac{\epsilon_{SiO_2}\epsilon_{hBN}}{\epsilon_{hBN}t_{SiO_2} + \epsilon_{SiO_2}t_{hBN}} \right) \\
&= \epsilon_0 \left(\frac{(4)(4)}{4(285 \times 10^{-9}) + 4(26 \times 10^{-9})} \right) \\
&= 1.14 \times 10^{-4}\ F/m^2.
\end{aligned}
$$

With these values, we obtain a mobility of approximately $\mu_{FE} = 7900\ cm^2/Vs$ which is better than other high mobility values reported in WSe_2[1–4]. Additional values were extracted from similar curves taken at room temperature and at 1 K where we obtained $\mu_{FE}(T = 300K) = 297\ cm^2/Vs$ and $\mu_{FE}(T = 1K) = 16357\ cm^2/Vs$. This trend from low mobility to high mobility as temperature decreases further suggests that a clean and high mobility device has been fabricated.

The carrier concentration at any given back-gate voltage can be estimated by

$$
n(V_{BG}) = C_G \frac{V_{BG} - V_{Th}}{e}
$$

For example, at $V_{BG} = -33\ V$ (Figure 2 a-b in main text), the hole concentration is approximately $n = 1.82 \times 10^{12}\ \text{cm}^{-2}$.

SECTION 3: SERIES RESISTANCE CALCULATION

In Supplementary Figure 3(a), we plot the raw data (resistance vs. split gate voltage) for various values of the back-gate voltage. The leftmost curve corresponds to a back-gate voltage of $-25\ V$ and the rightmost curve corresponds to a back-gate voltage of $-35\ V$. The spacing between each curve is $50\ mV$. In Supplementary Figure 3(b), the conductance $(\frac{1}{R_{SD}})$ is plotted as a function of the split gate voltage for the same curves as in Supplementary Figure 3(a). In both Supplementary Figure 3(a-b), a red dotted line is plotted indicating the value of the series resistance that was subtracted to obtain Supplementary Figure 3(c) (Figure 2 c-d in the main manuscript). This series resistance represents the resistance at the point where the areas beneath the split gates are depleted and was obtained in a similar fashion to Marinov *et al.*[5]. As we can see, the series resistance decreases as a function of back-gate voltage because the WSe_2 sheets on either side of the split gates have more

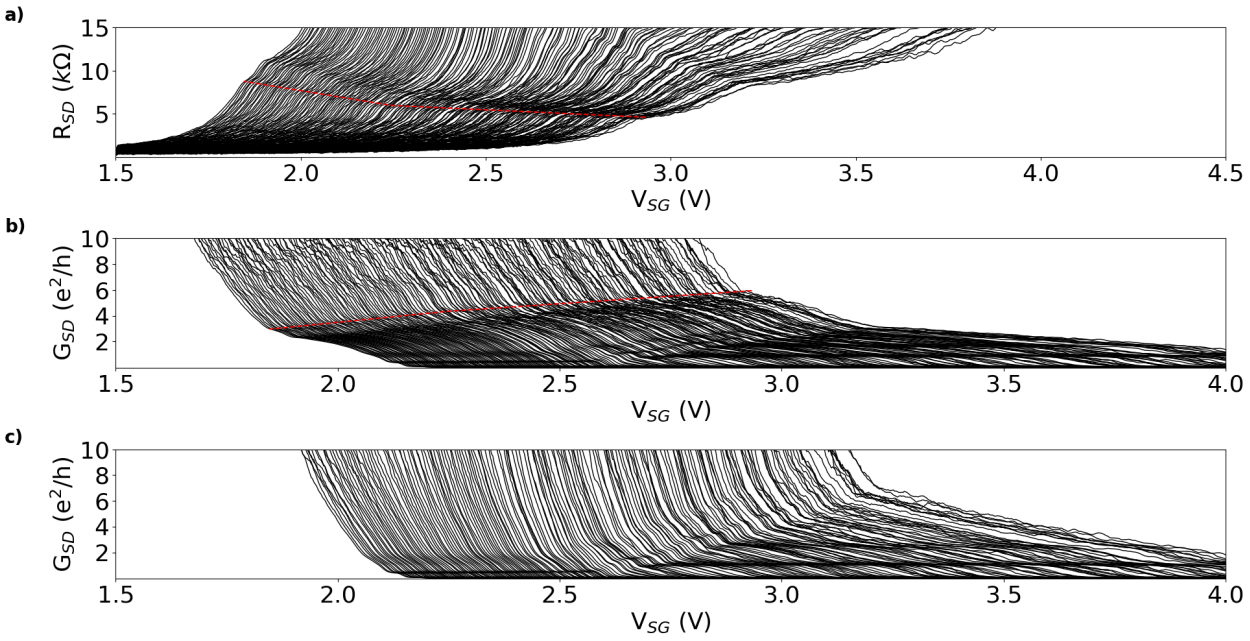

FIG. 3. (a) Resistance as a function of split gate voltage V_{SG} where each trace is taken at a different back-gate voltage V_{BG} ranging from -25 V (left) to -35 V (right). (b) Corresponding conductance curves plotted in units of e^2/h. The red lines in plots (a-b) correspond to the depletion of the split gates and consequently the series resistance. (c) The same traces as in (b) after subtracting the series resistance.

carriers and therefore less resistance. After removing the series resistance (Supplementary Figure 3(b)), we obtain the same plot as found in the main text (Supplementary Figure 2d).

SECTION 4: REPRODUCIBILITY AT 10 MK

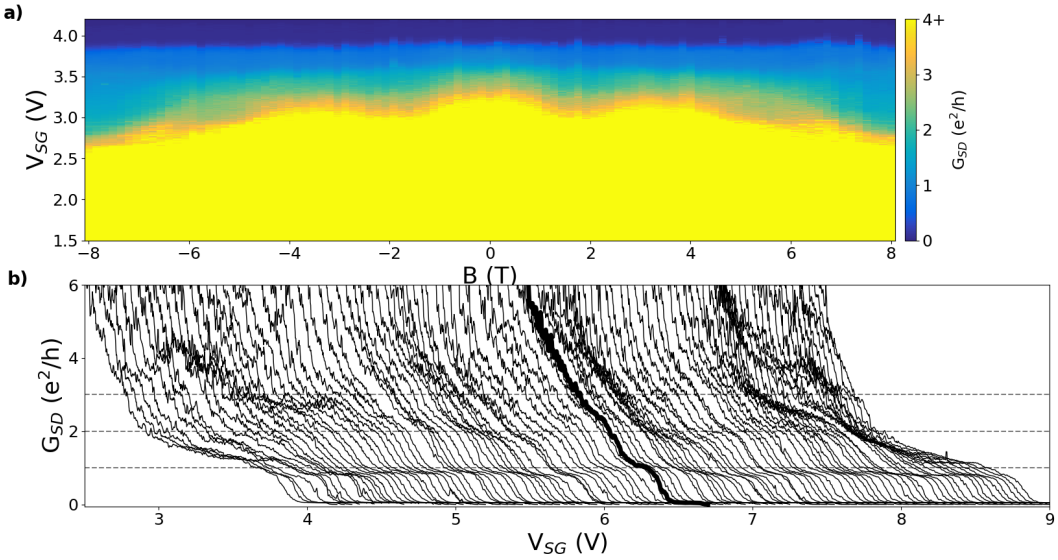

FIG. 4. (a) Dependence of the quantized conductance plateaus on a perpendicular magnetic field ranging from -8 T to 8 T. (b) Line cuts from (a) plotted in a "waterfall" style. A horizontal offset is introduced between adjacent line traces for clarity. A lead resistance of $R_L = 5083\ \Omega$ was subtracted. $V_{BG} = -33.2$ V.

The same set of measurements found in Figure 3 in the main manuscript was also performed at the base temperature of the dilution refrigerator (10 mK) (Supplementary Figure 4). A first plateau appears at e^2/h for all values of the magnetic field. Another plateau appears around 2 e^2/h at $B = 0$ T and quickly converges to 2 e^2/h as we turn on the magnetic field. This value away from 2 e^2/h at $B = 0\ T$ is attributed to magnetoresistance effects in the leads. At approximately ± 5 T, the 2 e^2/h plateau evolves towards the e^2/h plateau as seen at 4 K.

SECTION 5: REPRODUCIBILITY IN A DIFFERENT MEASUREMENT SETUP

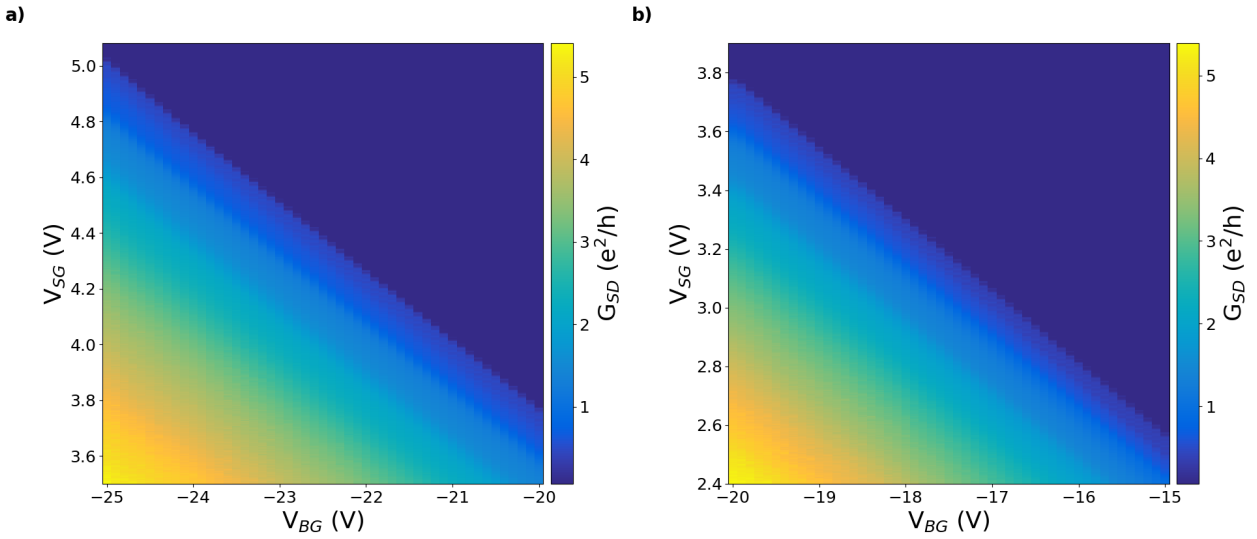

FIG. 5. Color map of conductance as a function of split gate voltage V_{SG} and back-gate voltage V_{BG}.

The device considered in the main manuscript was also studied in a 1K cryostat at 4 K. Similar results are observed where there are 3 robust plateaus each spaced by e^2/h for various carrier densities as seen in Supplementary Figure 5.

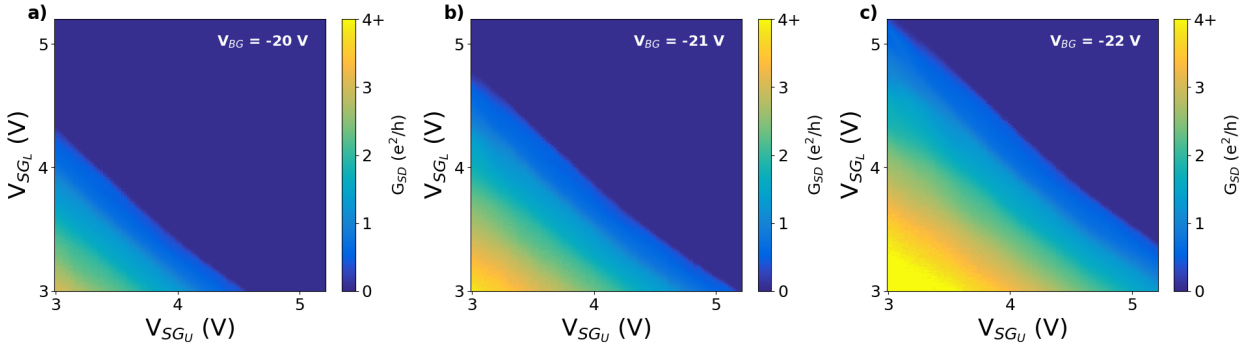

FIG. 6. Conductance as a function of individual split gates V_{SG_L} and V_{SG_U} taken at (a) $V_{BG} = -20$ V, (b) $V_{BG} = -21$ V, and (c) $V_{BG} = -22$ V

To ensure that the conductance plateaus are related to the gate-defined channel and not some resonances under the split gates, we measured the conductance as a function of each individual split gate (Supplementary Figure 6). V_{SG_L}/V_{SG_U} refer to the lower/upper split gates in the inset of Figure 1b in the main text. These plots were taken at 3 different

carrier concentrations (back-gate voltages) and we observed robust plateaus that are equally influenced by both gates (a slope of approximately 45°) indicating that the origin of the plateaus is located in between the two gates, hence the channel.

SECTION 6: TRANSPORT IN THE LOW CARRIER DENSITY REGIME

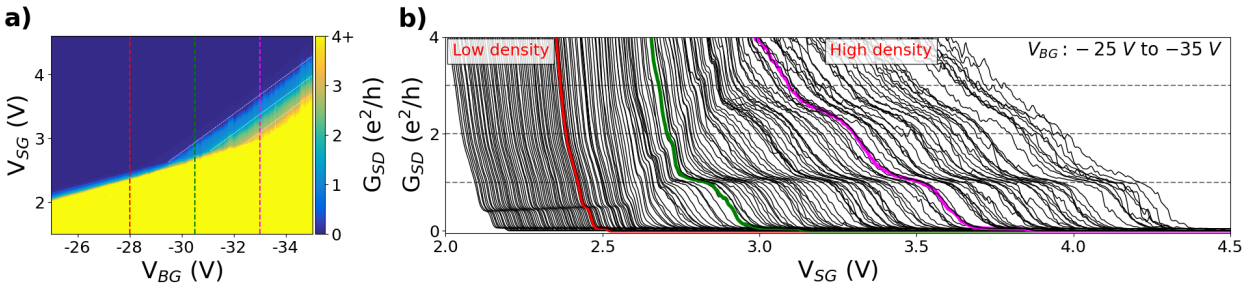

FIG. 7. (b) Color map of conductance as a function of split gate voltage V_{SG} and back-gate voltage V_{BG} as found in Figure 2c of the main manuscript. A lead resistance is subtracted. (b) Line cuts from (a) plotted in a "waterfall" style indicating a first step at e^2/h and a second step around $2e^2/h$ in the high density regime. An additional robust plateau is found at 0.5 e^2/h in the low density regime. The left most trace is taken at $V_{BG} = -25$ V and the right most trace is taken at $V_{BG} = -35$ V. The red, green and magenta lines are highlighted by similarly colored dashed lines in (a) and correspond to back-gate voltages of −28 V, −30.5 V, and −33 V respectively. These three curves feature the regimes where we observe the 0.5 e^2/h plateau (red), the 1 e^2/h plateau (green), and the 1 e^2/h and 2 e^2/h plateaus (magenta)

Transport through the 1D channel was studied at various back-gate voltages (-25 V to -35 V) which led to the observation of two distinct regimes as demonstrated in Supplementary Figure 7a. At higher hole concentrations ($V_{BG} < -30\ V$) we observed conductance plateaus at 1 e^2/h and 2 e^2/h as discussed in the main manuscript. Furthermore, Supplementary Figure 7b reveals that there is a robust plateau located at 0.5 e^2/h found at lower carrier densities corresponding to a back-gate raised above -30 V. This plateau is unexpected and demonstrates that further research needs to be conducted on monolayer TMDs to fully understand their electronic properties.

SECTION 7: TIGHT-BINDING PARAMETERS

In the tight-binding atomistic calculations we chose the following structural parameters: $d_{\parallel} = 1.9188$ Å (W-Se_2 dimer center distance), $d_{\perp} = 1.6792$ Å (Se atom distance from $z = 0$ plane). The tight-binding Slater-Koster parameters are given by (all in eV): $E_d = -0.4330$, $E_{p0} = -3.8219$, $E_{p\pm1} = -2.3760$, $V_{dp\sigma} = -1.58193$, $V_{dp\pi} = 1.17505$, $V_{dd\sigma} = -0.90501$, $V_{dd\pi} = 1.0823$, $V_{dd\delta} = -0.1056$, $V_{pp\sigma} = 0.52091$, $V_{pp\pi} = -0.16775$, together with characterising intrinsic spin-orbit couplings: $\lambda_W = 0.275$, $\lambda_{Se_2} = 0.08$. We note that these parameters are chosen to reproduce ab initio electronic band structure of two spinfull valence bands.

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5.5 Conclusion

In this chapter, a new device architecture is presented which demonstrates independent control of the charge carrier density in the WSe_2 (back-gate) and the contact resistance (contact-gate). This allows us to tune the charge carrier density into the low-carrier regime while maintaining an extremely low contact resistance, an important feature for reaching the few-hole regime in gate-defined quantum dot devices. Furthermore, a high field-effect hole mobility [49, 94–96] of $\mu_{FE} = 7\ 900\ cm^2/Vs$ was measured indicating that a high quality monolayer WSe_2 has been achieved.

This new architecture also features a split-gate which can be used to create a long and narrow 1D channel in the monolayer WSe_2 sheet. Transport across this channel resulted in the observation of conductance quantization suggesting that a quasi-ballistic regime has been achieved. This further suggests that the disorder in the channel has been reduced and that the use of the split-gates can be advantageous for creating truly gate-defined quantum dots. Interestingly, the conductance plateaus were observed at intervals of e^2/h instead of the expected $2e^2/h$ as the spin-valley locking would insinuate, suggesting a spontaneous valley polarised state of the hole gas in monolayer WSe_2. In the low carrier density regime, a robust plateau located at $0.5e^2/h$ was also observed. A single particle atomistic tight-binding model was insufficient for explaining both of these interesting features suggesting that hole-hole correlations need to be considered.

These findings show that further research needs to be conducted on monolayer TMDs to fully understand their electronic properties. Furthermore, these results demonstrate that the new device architecture is promising for achieving gate-defined quantum dots in the few-hole regime.

Chapter 6

Conclusion and outlook

In this work we presented the fabrication techniques necessary for properly contacting TMDs with low contact resistances. Using these techniques, devices in monolayer MoS_2 and WSe_2 were fabricated and the transport associated to three quantum structures were studied: quantum dots in monolayer MoS_2 and monolayer WSe_2, a gate-defined nanoconstriction used as a charge detector, and a gate-defined 1D channel. From those experiments, several conclusions can be drawn and improvements to the current device architecture can be proposed.

First, from the results presented in Chapter 3, we observed that disorder and defects in the environment around the TMD create a non-uniform potential landscape resulting in the formation of multiple quantum dots in the potential minima. Although the location of the quantum dots is by nature random, we found that when the density of quantum dots is low enough, such was the case in monolayer WSe_2, individual quantum dots can be controlled and studied by gates. Transport measurements such as bias spectroscopy led to the extraction of the addition energy of a particular quantum dot, 3.4 meV, and its

diameter (≈ 58 nm).

In chapter 4, towards developing the necessary elements for a TMD based quantum circuit, we demonstrated that our gate structure can define a nano-constriction which can be used as a charge detector for a nearby quantum dot. This was the first demonstration of non-invasive charge detection in TMD-based devices. Although the quantum dots studied in this chapter were incidental, this detection scheme is readily applicable to gate-defined quantum dots.

The transport associated to chapter 3 and 4 were mostly dominated by incidental quantum dots created by defects and disorder which made the need for cleaner materials or an alternate device architecture evident. There exists research which focuses on achieving cleaner TMDs [52], but in this 5^{th} chapter, we presented a device architecture that reduced the number of incidental quantum dots that participate in transport measurements. This was made evident by the measured high mobility and the observation of quantized conductance plateaus. The interval between the conductance plateaus was recorded to be e^2/h as opposed to the expected value of 2 e^2/h obtained from simple mode counting (spin-valley locking). The explanation for this spontaneous valley polarised state was discussed and hole-hole correlations was suggested as being a possible reason. Another advantage of this device architecture comes from the fact that it consists of three distinct gates: the back-gate which is responsible for controlling the 2DHG charge carrier density globally, the split-gate which is responsible for creating the 1D channel and reducing the number of participating quantum dots, and the contact gates which are used for achieving quality contacts. The independent control of all these electrical components allows us to tune the 2DHG into the low-density regime without compromising the quality of the electrical contacts.

Further improvements can be made to the current device architecture by using a graphite

back-gate instead of the silicon substrate. SiO_2 is known to host trapped charges which can contribute to the non-uniform potential landscape that influences the TMD layer [48]. A graphite/hBN gate/dielectric stack on the other hand, can be used as an atomically flat back-gate free of trapped charges. Fabrication of such a device is in progress at the time of writing (Figure 6.1).

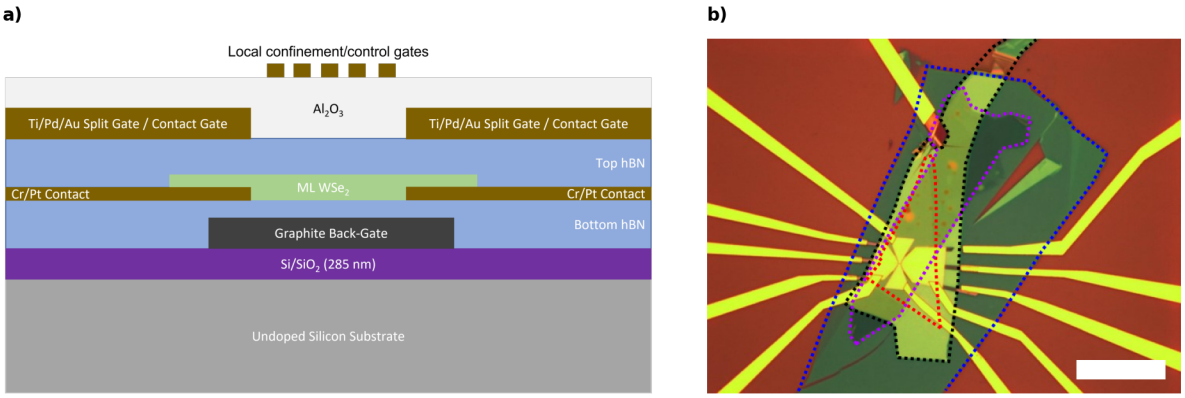

Figure 6.1: (a) Schematic of the device architecture including a graphite back-gate. Local confinement gates are moved to the top most layer of the device and separated by a 50 nm layer of aluminum oxide (Al_2O_3). (b) Optical image of the device structure from (a) up to the split gates/contact gates. The 2D materials are outlined in colored dashed lines (graphite = purple, bottom hBN = blue, monolayer WSe_2 = red, top hBN = black). The scale bar represents 20 μm.

Although this thesis presents fabrication techniques for achieving high quality ohmic contacts to TMDs and reports on unexplored quantum transport phenomena in quantum structures based on TMDs, there still exists many challenges associated with these materials. With a focus on the growth of cleaner materials with lower defect densities [52], the continuous improvement on the fabrication techniques, and the constant search for an optimal device architecture, TMD-based devices show promise in the field of quantum technologies and this thesis provides a step towards achieving these final goals.

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Appendix A

Sample catalogue

Table A.1 presents optical micrographs of the final devices which have been discussed throughout this dissertation.

Table A.1: Catalogue of the samples discussed in this thesis. All scale bars represent 20 μm.

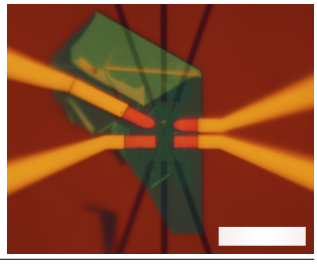
Sample ID	Material	Contact Architecture	Section	Optical micrograph
MoS_2 Batch 2, Sample E	Monolayer MoS_2	Top contacts	Chapter 2.3	

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Table A.1 – continued from previous page

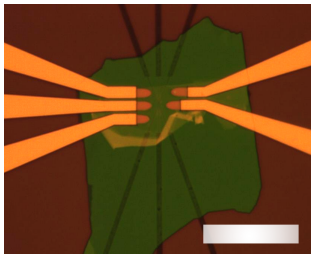
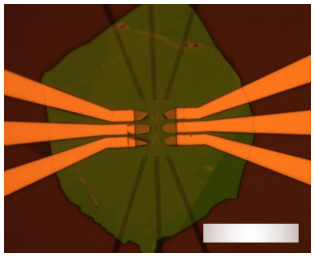
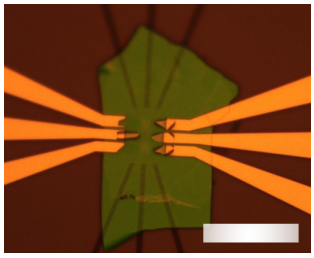
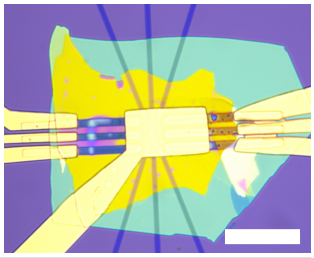
Sample ID	Material	Contact Architecture	Section	Optical micrograph
MoS_2 Batch 4, Sample B	Monolayer MoS_2	Top contacts	Chapter 2.3	
MoS_2 Batch 4, Sample D	Monolayer MoS_2	Top contacts	Chapter 2.3	
MoS_2 Batch 4, Sample E	Monolayer MoS_2	Top contacts	Chapter 2.3	
MoS_2 Batch 6, Sample E	Monolayer MoS_2	Bottom contacts	Chapter 2.3	

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Table A.1 – continued from previous page

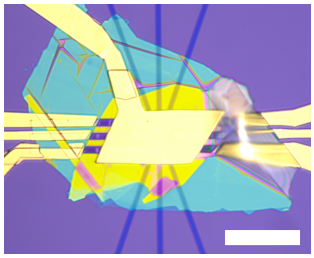
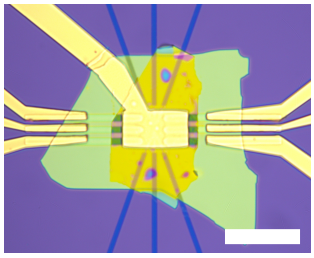
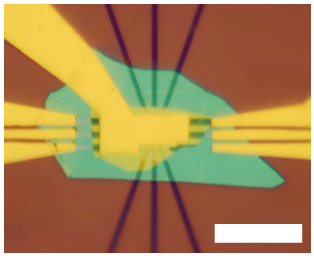
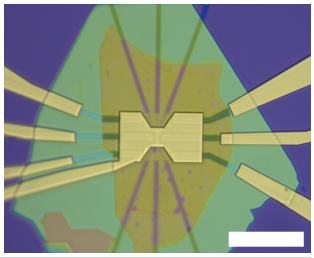
Sample ID	Material	Contact Architecture	Section	Optical micrograph
MoS_2 Batch 6, Sample F	Monolayer MoS_2	Bottom contacts	Chapter 2.3	
MoS_2 Batch 7, Sample C	Monolayer MoS_2	Bottom contacts	Chapter 3.2, 3.3	
WSe_2 Batch 1, Sample A	Monolayer WSe_2	Bottom contacts	Chapter 2.3, 3.4	
WSe_2 Batch 3, Sample B	Monolayer WSe_2	Bottom contacts	Chapter 2.3, 4.2	

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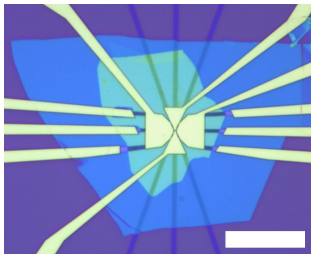
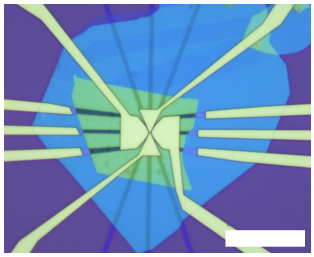
Table A.1 – continued from previous page

Sample ID	Material	Contact Architecture	Section	Optical micrograph
WSe_2 Batch 4, Sample B	Monolayer WSe_2	Bottom contacts, 4-piece top gate	Chapter 5.4	
WSe_2 Batch 4, Sample C	Monolayer WSe_2	Bottom contacts, 4-piece top gate	Chapter 5.4	

Appendix B

Detailed device fabrication process and characterization

In this chapter, we present the entire fabrication process, including the subtle techniques, that were used to fabricate the devices presented throughout this thesis.

B.1 Isolation and identification of 2D materials

Mechanical exfoliation is the technique used to isolate monolayer and few-layer thick flakes of materials from the bulk crystal [57, 58]. A standard technique was already discussed in section 2.1 but a modified version was used for isolating large monolayers of TMDs and large uniform flakes of hBN.

This technique begins just like the standard exfoliation technique, where the bulk crystal is cleaved using tweezers and placed on a piece of semiconductor-grade adhesive tape. A second piece of adhesive tape is then repeatedly attached and peeled-off from the initial

tape with the 2D material until it is covered with thinner crystal. The 2D material covered tape is gently placed onto a PDMS film such that the crystal is in direct contact with the PDMS. The tape is then removed leaving behind exfoliated flakes on the PDMS sheet. To transfer the exfoliated flakes on to a substrate, the PDMS sheet with crystal is placed in direct contact with a SiO_2/Si substrate and left on a hot plate at 80°C for 5 minutes. The substrate was then rapidly separated from the PMDS resulting in 2D materials being transferred onto the SiO_2 surface. This method proved to increase the overall yield of exfoliated monolayer TMDs, and resulted in much larger flakes compared to the direct exfoliation from tape to substrate (Figure B.1). All the hBN and TMD crystals were isolated using this technique. Better results for exfoliating graphite and graphene were achieved using the standard technique.

A silicon substrate with 285 nm of thermally grown SiO_2 is the standard choice of substrate for 2D materials due to the maximized optical contrast of monolayer flakes [97]. The thickness of exfoliated flakes on this substrate can optically be identified (monolayers in Figure B.1 d and f), however, additional characterisation techniques are used to confirm the thickness. In addition to the optical contrast, the thickness is confirmed using atomic force microscopy (AFM), and Raman spectroscopy.

The basic principle of AFM works by scanning a sharp tip over a surface and detecting the deflection of a cantilever where the size of the deflection is related to the interacting forces between the sample and the tip. For a flat and uniform surface, this deflection is always constant, however, if a step is introduced, the deflection will necessarily change. The deflection can be kept constant by raising and lowering the tip, from which the height of the sample can be determined. The AFM can also be used to verify the surface cleanliness

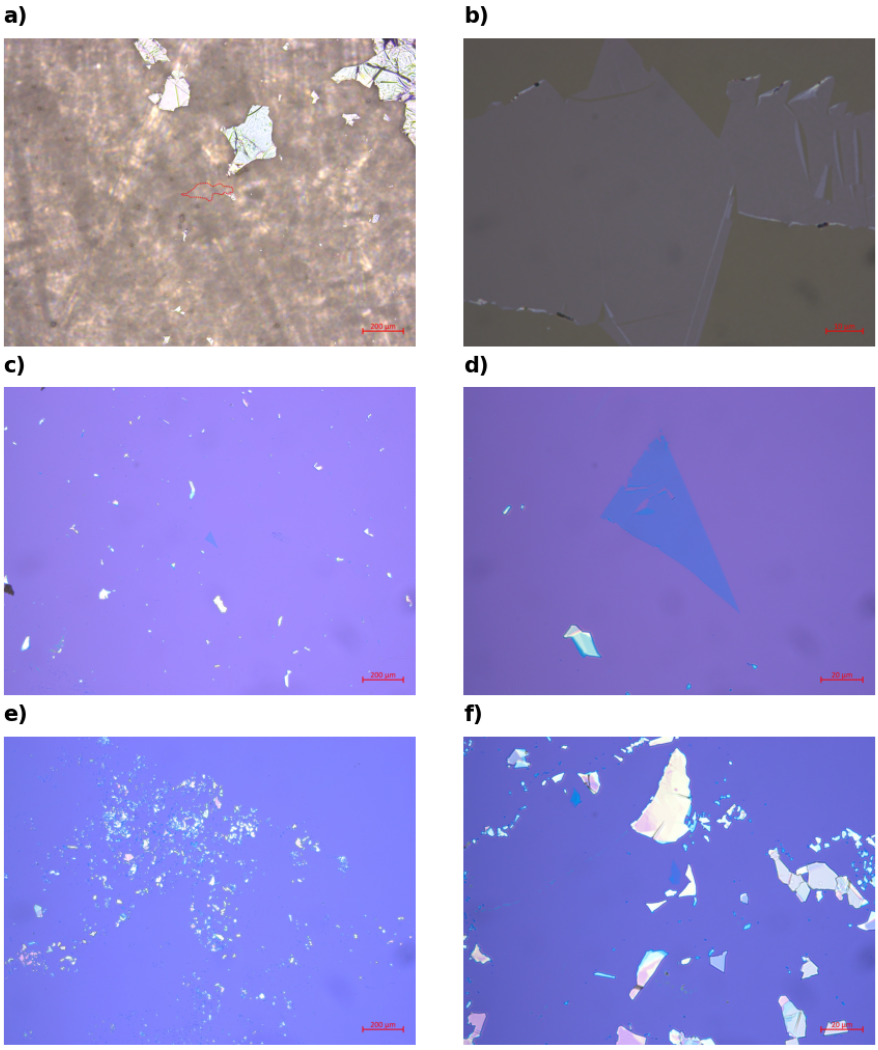


Figure B.1: (a-b) Optical micrographs of exfoliated MoS_2 directly on a PDMS sheet. (a) 5X magnification. Outlined in red is a large MoS_2 flake isolated from surrounding multilayered flakes. (b) Zoom-in (100X) of the same flake as in (a). (c-d) Optical micrographs of exfoliated MoS_2 using the PDMS sheet as an intermediary step resulting in large isolated monolayer flakes, a desirable detail for sample fabrication. Optical magnification of 5X and 50X for (c) and (d), respectively. (e-f) 5X (e) and 50X (f) optical micrographs of exfoliated MoS_2 using the standard tape technique. Comparing the (e-f) to (c-d), the density of flakes is larger however the overall area of individual flakes is much smaller. Furthermore, isolated monolayers are rare and hard to find when exfoliation is done directly from the tape. An example of an isolated monolayer is found at the center of (f).

of the flakes and ensure that it is free of cracks and residues.

The Raman spectra of TMDs show features that are strongly dependent on the number of layers [98,99], which can then be used to identify flake thicknesses. For example in molybdenum disulfide, in a standard back-scattering Raman measurement, two high frequency modes are detectable: E^1_{2g} and A_{1g}. The A_{1g} Raman mode blue-shifts when the number of layers is increased caused by the stiffening of the out-of-plane vibrations. The E^1_{2g} mode on the other hand experiences a red-shift when the material increases in thickness [98,99]. For WSe_2, there exists a Raman peak near 250 cm^{-1} (A_{1g}) which corresponds to the out-of-plane vibrations of the selenium atoms. A second peak labelled 2LA(M) is situated near A_{1g}, whose position and intensity with respect to the A_{1g} peak depends strongly on the material's thickness.

Optical contrast, AFM, and Raman spectroscopy were all used to confirm the thickness of the materials used in this dissertation. An example of AFM and Raman spectroscopy performend on WSe_2 is shown in figure B.2.

B.2 Nanofabrication

In this section we describe the nanofabrication steps used to fabricate the electrical components of the TMD devices of this thesis, focusing mainly on electron beam lithography (EBL).

Three main electrical components are patterned to achieve the devices found in this thesis: local control gates, electrical contacts, and top gates. Local control gates are patterned directly on the Si/SiO_2 substrate however, the contacts and top gates are patterned on top of 2D materials which leads to slightly different recipes.

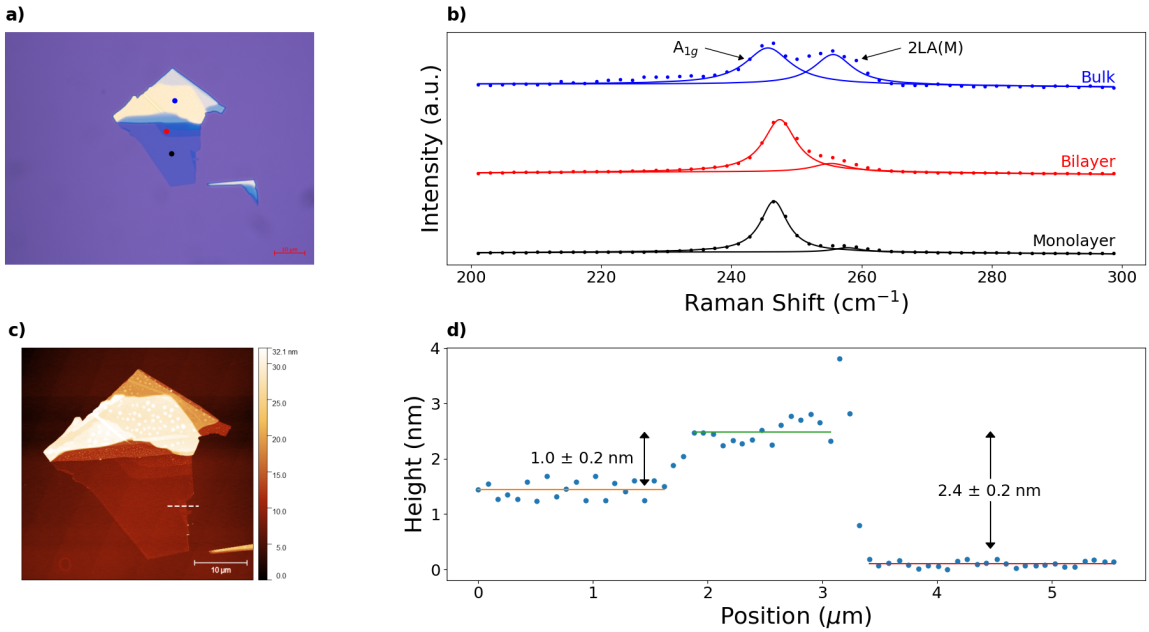


Figure B.2: (a) Optical micrograph of an exfoliated WSe_2 flake with various thicknesses. (b) Raman spectra taken at the points indicated in (a) demonstrating the evolution of the Raman peaks with respect to flake thickness. The spectra are consistent with what is expected for monolayer, bilayer and bulk WSe_2. (c) AFM topography map of the same flake as in (a). (d) Line profile of the dashed line indicated in (c). The heights extracted from this line profile confirm that the lower portion of the flake is monolayer.

EBL recipe for local control gates

The local control gate pattern presented in chapter 3 have features that are separated by 50 nm, and therefore require a high-resolution patterning technique such as electron beam lithography. The following recipe was used to achieve these gates.

1. Spin-coat the sample with PMMA (950K PMMA C4 - 370 nm)
   (a) Use acetone/IPA and a nitrogen (N_2) blow dry to clean the sample.
   (b) Spin the sample at 2000 rpm for 30 s.
   (c) Bake the sample at 180°C for 15 minutes.

2. In the ebeam, expose the pattern at an electron-beam accelerating voltage of 50 kV and a dose of $\approx 500\ \mu C/cm^2$.

3. Develop in a 1:3 solution of MIBK:IPA for 0 seconds followed by a 15 s IPA rinse, and N_2 blow-dry.

EBL recipe for electrical contacts

For the devices presented in this thesis, contacts are patterned directly on hBN. Initially, a similar recipe to the one used for the local control gates was used to pattern the electrical contacts. Patterning directly on top of hBN often led to thin cracks in the PMMA between nearby features as indicated in Figure B.3(a,c,d), presumably due to poor adhesion between the PMMA and the hBN. Upon metallization, this veining often led to shorts between adjacent electrical components (Figure B.3d). To remedy the situation, a thin layer of hexamethyldisilazane (HMDS) was deposited prior to the spin coating of PMMA to promote adhesion to the hBN. Furthermore, following the electron beam exposure, the samples were developed in a mixture of 7% H_2O and 93% IPA for 1 minute. The combination of these alterations led to well defined structures without the veining (Figure B.3e-f). Here we present the complete recipe.

1. Place the sample in an HMDS oven for 5 minutes.

2. Spin-coat the sample with PMMA (950K PMMA A6 - 600 nm)

   (a) Use acetone/IPA and a nitrogen (N_2) blow dry to clean the sample.

   (b) Spin the sample at 3000 rpm for 60 s.

   (c) Bake the sample at 180°C for 90 s.

3. In the ebeam, expose the pattern at an electron-beam accelerating voltage of 10 kV and a dose of $\approx 150\mu C/cm^2$.

4. Develop in a 7:93 solution of H_20:IPA for 1 minute followed by a 30 s IPA rinse, and N_2 blow-dry.

This recipe was also used to pattern the contact pads and their extensions.

EBL recipe for top gates The top gates were fabricated on top of hBN, therefore, the HMDS adhesion layer and H_2O/IPA developer was also used to prevent any veining. The process steps for this electron beam lithography procedure were as follows:

1. Place the sample in an HMDS oven for 1 minute.

2. Spin-coat the sample with PMMA (950K PMMA C2 - 168 nm)

   (a) Use acetone/IPA and a nitrogen (N_2) blow dry to clean the sample.

   (b) Spin the sample at 2000 rpm for 30 s.

   (c) Bake the sample at 150°C for 15 minutes.

3. In the ebeam, expose the pattern at an electron-beam accelerating voltage of 50 kV and a dose of $\approx 459\mu C/cm^2$.

4. Develop in a 7:93 solution of H_20:IPA for 15 seconds followed by a 15 s IPA rinse, and N_2 blow-dry.

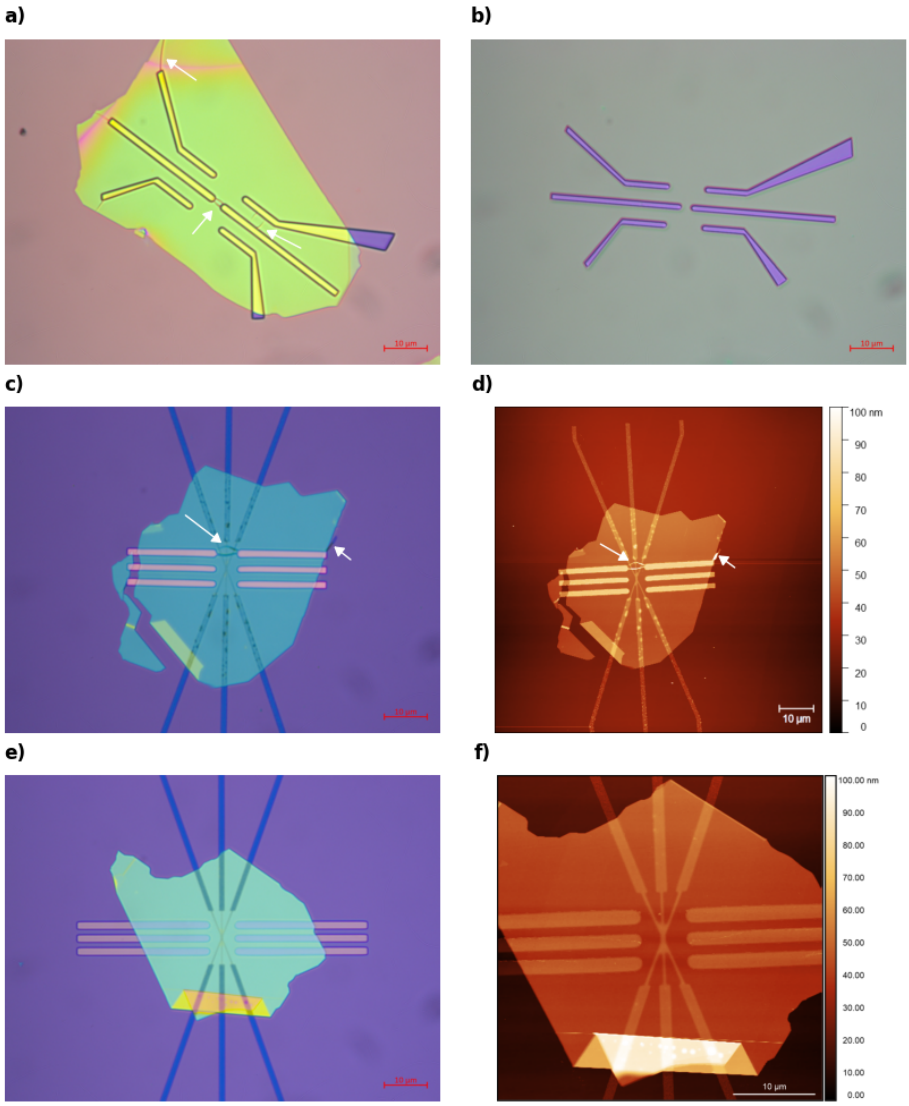


Figure B.3: (a-d) EBL patterning of contacts without the HMDS layer. (a) Optical micrograph of the contact pattern on hBN taken after development. White arrows indicate that veins formed in the PMMA. (b) Same contact pattern as in (a) defined directly on Si/SiO_2 where no cracks in the PMMA are noticeable. Optical micrograph (c) and AFM map (d) of the contact pattern taken after metallization demonstrating that the veins are also filled, which can lead to shorts between separate electrical components. (e-f) EBL patterning of the contacts using the HMDS layer. Optical micrograph (e) and AFM map (f) of the resulting contacts showing no signs of veining.

B.3 AFM Brooming Protocol

As discussed in section 2.2-2.3, AFM brooming is a key ingredient for achieving ohmic contacts, clean surfaces, and clean interfaces between 2D materials. Here we present a complete protocol for AFM brooming, specifically when using the Bruker Dimension Icon. This protocol can generally be adapted to be used with any AFM.

1. **Select the mode of operation**
   (a) To "broom" the sample, we employ the AFM in Contact Mode therefore select the "Contact Mode" option.
2. **Load the AFM tip**
   (a) A soft cantilever is typically used for AFM brooming. The tip used throughout this thesis was the OTR8-10 by Bruker, which is a silicon-nitride tip on a soft cantilever (0.15 N/m). This tip is loaded in the system.
   (b) Align the laser and the photosensitive diode (PSD)
3. **Approaching the surface**
   (a) While the tip is in focus, lower the tip until the surface also comes into focus.
   (b) Align the tip on an area next to the targeted sample.
4. **Engaging the tip**
   (a) In the **Check Parameters** window within the **Workflow Toolbar**, set the inital values to:
      i. Deflection Setpoint = 2 V

ii. Integral Gain = 2.000

iii. Proportional Gain = 5.000

(b) Attempt to engage the tip by pressing the **Engage** button in the **Workflow Toolbar**. A pre-engage check begins followed by motion of the Z-stage.

(c) From this first engate, two outcomes are possible:

i. Real engage

ii. False engage

(d) Note the type of engage and withdraw the tip by clicking **Withdraw** in the **Workflow Toolbar**.

i. If the outcome is a real engage: The goal is to determine the lowest deflection setpoint therefore reduce the current deflection setpoint and re-engage. Repeat the previous step until a false engage is recorded. The deflection setpoint that resulted in the last real engage is the minimum deflection setpoint and should be noted.

ii. If the outcome is a false engage: Increase the deflection setpoint and re-engage. The deflection setpoint that results in a real engage is the minimum deflection setpoint and should be noted.

5. Force Calibration

The force applied by the tip on the sample must be controllable therefore, the relation between this force and the tip deflection voltage must be determined. To obtain this information, a force curve is performed.

(a) Engage the tip.

(b) Click **Ramp** in the **Workflow Toolbar**

(c) In the **Ramp Parameter List**, adjust the **Ramp Size** to 1 μm and the **Scan Rate** to 0.5 Hz.

(d) Select **Ramp Continuous** and consistently observe a plot similar to Figure B.4.

(e) If the plots are consistent, select **Ramp Single**. Otherwise, the deflection setpoint may be too low and this step should be repeated with a slightly higher setpoint.

(f) Drag vertical cursors from the plot edge to points 2 and 3 in Figure B.4.

(g) Click **Ramp** > **Update Sensitivity** to calculate the slope corresponding to the straight line formed between points 2 and 3. This slope (force sensitivity) equates the relation between the deflection voltage and the Z-displacement.

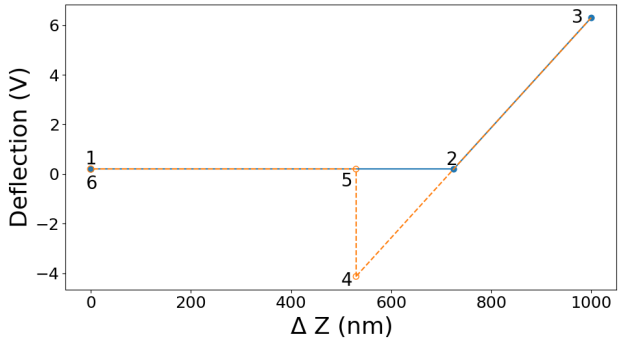


Figure B.4: A typical force curve highlighting key AFM tip positions. (1) The tip is far away from the sample where the deflection is near 0. (2) The tip contacts the sample and begins to bend as the z-displacement is increased, resulting in a positive increase in the deflection voltage. (3) At the end of the z-displacement range, the deflection reaches a maximum and the piezoelectric motors begin to retract the tip. The deflection voltage returns to its initial value then becomes smaller due to the tip "sticking" to the surface (4). (5) The tip is released and abruptly returns to the initial deflection voltage. (6) It continues to retract without any change in the deflection voltage.

6. Spring Constant Determination

The previous plot gives you a relation between the deflection voltage and the piezo Z-displacement. To obtain the applied force, the spring constant of the cantilever must be determined.

(a) Withdraw the tip.

(b) Click on **Thermal Tune**.

(c) Adjust the scanning range to **1 - 100 kHz**. The cantilevers used in these experiments have a nominal resonant frequency at 73 kHz.

(d) Select **Get data**.

(e) Drag the vertical cursors from the plot edge to either side of the peak.

(f) Click on **Calc. Spring K** and note the spring constant. A standard spring constant is in the range of 0.2 N/m.

7. Calculating the Contact Force

The contact force is defined as $F = k \times d$ where k is the spring constant and d is the cantilever deflection. From the force calibration done in step 5, we can obtain a relationship between the force and the deflection voltage.

$$F = k \times Force\ Sensitivity \times (Deflection\ Voltage - Minimum\ Deflection\ Setpoint)$$

8. AFM Brooming

(a) **Setting up the scanning**

i. Set the **Scan Size** and the **Aspect Ratio** to the desired values

ii. Set the **Scan Rate** to ≈ 0.5 Hz

iii. Set the resolution (**Samples**/**Line**) of the scans. The AFM microscope has an approximate tip radius ($\approx$15 nm for the tips used in this thesis), and should be considered when setting this resolution (**Samples**/**Line**). Overlap between consecutive line scans is ideal to ensure that the entire scan area gets cleaned. For example, a scan area of width W should have a resolution bigger than $W/2r$ where r is the tip radius.

iv. Set the **Deflection Setpoint** such that the contact force is approximately 100 nN, the typical force used to clean the samples presented in this thesis.

(b) **Engage the Brooming**

Monitor the deflection error channel and sweep until there is no noticeable change indicating that debris is no longer being dragged.

9. **Post-brooming scan**

A post-brooming scan is performed to ensure that the AFM brooming was successful. This is performed in tapping or non-contact mode to avoid dragging the debris back into the cleaned area.

B.4 Complete Sample Fabrication

With all the fabrication techniques now described in great detail, the entire fabrication process for WSe_2 Batch 4, Sample C is presented along with Figure B.5 as a reference for each step.

1. **Local control gate fabrication** (Figure B.5a)

(a) **Substrate preparation**: A p-doped Si/SiO_2 was cleaved into a 7 mm × 10 mm chip and cleaned using acetone/IPA, and dried with a N_2 gun.

(b) **Electron beam lithography:** Following the procedure described in *EBL recipe for local control gates*, local gates were patterned into the PMMA coated substrate.

(c) **Metallization:** Using electron beam metal deposition, the pattern was metallized with Ti (2.5 nm) / Au (2.5 nm).

(d) **Lift-off:** The substrate was placed in a bath of acetone held at 45°C where the residual metal film was detached from the substrate. To aid with lift-off, the substrate was gently sprayed with acetone using a pipette.

(e) **Cleaning:** The sample was cleaned using acetone/IPA and dried off using a N_2 gun.

2. **Bottom hBN transfer** (Figure B.5 b-e)

(a) **Substrate preparation**: A p-doped Si/SiO_2 was cleaved into a 7 mm × 10 mm chip and cleaned using acetone/IPA, and dried with a N_2 gun.

(b) **Mechanical exfoliation:** Following the procedure described in *Isolation and identification of 2D materials*, a large and flat hexagonal boron nitride (26 nm thick) was exfoliated on the previously cleaned substrate and identified (Figure B.5 b).

(c) **Transfer preparation:** A glass slide with a PDMS/PPC stamp was prepared.

(d) **Pick-up:** The hBN flake was picked-up using the PDMS/PPC stamp while the substrate was held at a temperature of 40°C. The flake on the stamp was then

optically inspected for cracks that may have formed during the pick-up step (Figure B.5 c).

(e) **Drop-off:** The hBN flake was dropped off onto the local control gates (Figure B.5 d).

(f) **Cleaning:** The substrate with local control gates and hBN was placed into the vacuum furnace ($< 10^{-7}$) Torr and was baked for 30 minutes at 300°C (Figure B.5 e).

3. **Electrical contacts fabrication** (Figure B.5 f-i)

(a) **Electron beam lithography:** Following the procedure described in *EBL recipe for electrical contacts*, contacts were patterned into the PMMA coated substrate above the hBN.

(b) **Metallization:** Using electron beam metal deposition, the pattern was metallized with Cr (2 nm) / Pt (8 nm).

(c) **Lift-off:** The substrate was placed in a bath of acetone held at 45°C where the residual metal film was detached from the substrate. To aid with lift-off, the substrate was gently sprayed with acetone using a pipette (Figure B.5 f).

(d) **Chemical cleaning:** The sample was cleaned using acetone/IPA and dried off using a N_2 gun.

(e) **Furnace cleaning:** The sample was placed into the vacuum furnace ($< 10^{-7}$ Torr) and was baked for 30 minutes at 300°C (Figure B.5 g).

(f) **AFM cleaning:** Following the procedure described in *AFM Brooming Protocol*, the contacts and underlying hBN were cleaned using an AFM tip in contact mode (Figure B.5 h-i).

4. **Device encapsulation** (Figure B.5 j-r)

   (a) **Substrate preparation**: Two p-doped Si/SiO_2 were cleaved into 7 mm $\times$ 10 mm chips and cleaned using acetone/IPA, and dried with a N_2 gun.

   (b) **Mechanical exfoliation:** Following the procedure described in *Isolation and identification of 2D materials*, a monolayer WSe_2 was exfoliated and identified (Figure B.5 l) on one chip. A slightly larger and flat hBN flake (34 nm thick) was exfoliated and identified on the other chip (Figure B.5 j).

   (c) **Transfer preparation:** A glass slide with a PDMS/PPC stamp was prepared.

   (d) **First pick-up:** The hBN flake was first picked-up using the PDMS/PPC stamp while the substrate was held at a temperature of 40°C. The flake on the stamp was then optically inspected for cracks that may have formed during the pick-up step (Figure B.5 k).

   (e) **Second pick-up:** The WSe_2 flake was then picked-up using the PDMS/PPC/ hBN stamp while the substrate was held at a temperature of 40°C. The flakes on the stamp were then inspected optically and with an AFM (Figure B.5 m-n).

   (f) **AFM cleaning:** Following the procedure described in *AFM Brooming Protocol*, the WSe_2 flake was cleaned using an AFM tip in contact mode (Figure B.5 o-p).

   (g) **Drop-off:** The hBN/WSe_2 stack was dropped off onto the contacts while the substrate was held at a temperature of 80°C(Figure B.5 q).

   (h) **Furnace cleaning:** The substrate with local control gates and hBN was placed into the vacuum furnace ($< 10^{-7} Torr$) and was baked for 30 minutes at 300°C (Figure B.5 r).

5. **Top gate fabrication** (Figure B.5 s-t)

(a) **Electron beam lithography:** Following the procedure described in *EBL recipe for top gates*, the top gates, extensions, and contact pads were patterned into the PMMA coated sample.

(b) **Metallization:** Using electron beam metal deposition, the pattern was metallized with Ti (5 nm) / Pd (25 nm) / Au (125 nm). This thick metal at the contact pads can help reduce the risk of punching through the oxide at the wire bonding step, hence reducing the leakage current to the back-gate.

(c) **Lift-off:** The substrate was placed in a bath of acetone held at 45°C where the residual metal film was detached from the substrate. To aid with lift-off, the substrate was gently sprayed with acetone using a pipette.

(d) **Chemical cleaning:** The sample was cleaned using acetone/IPA and dried off using a N_2 gun.

Figure B.5

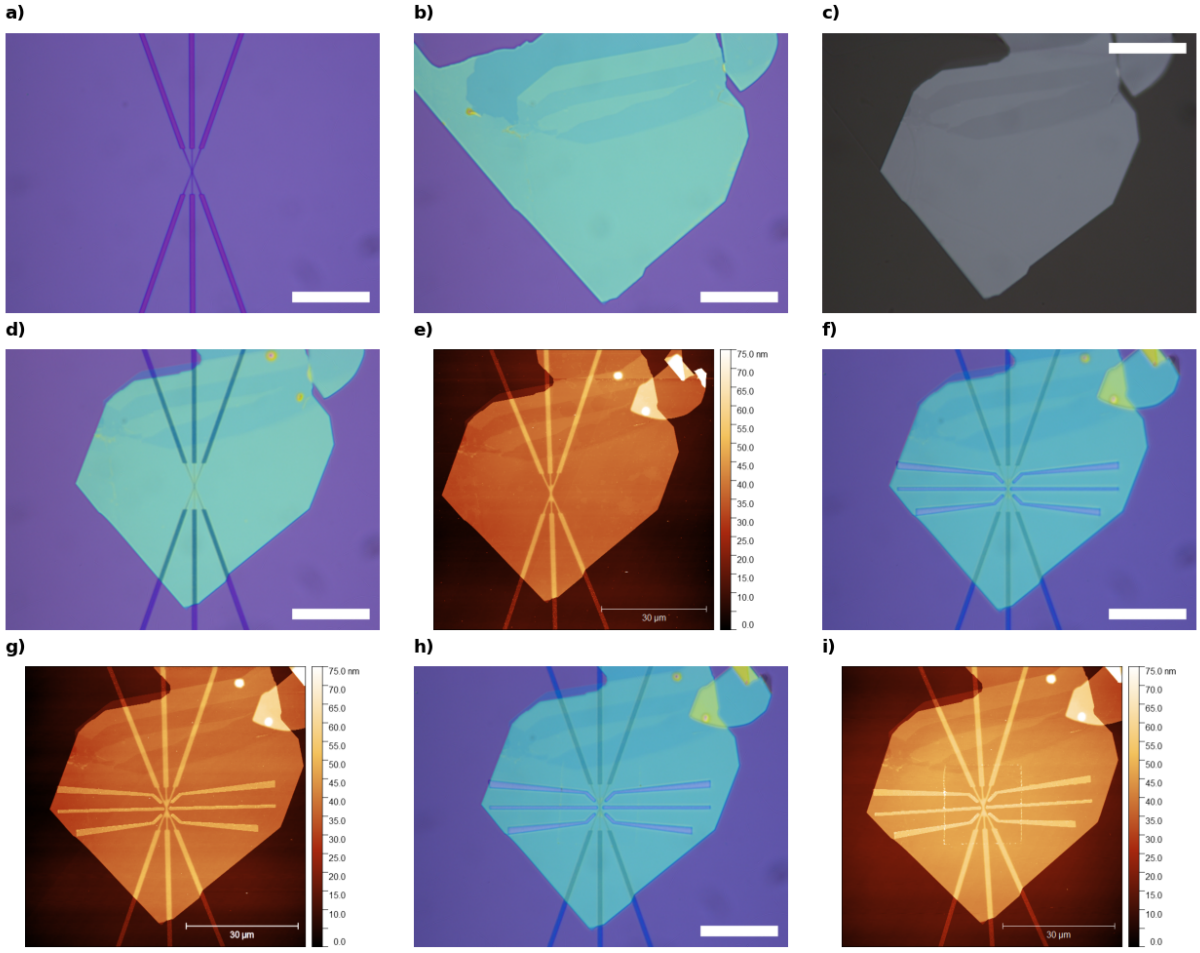

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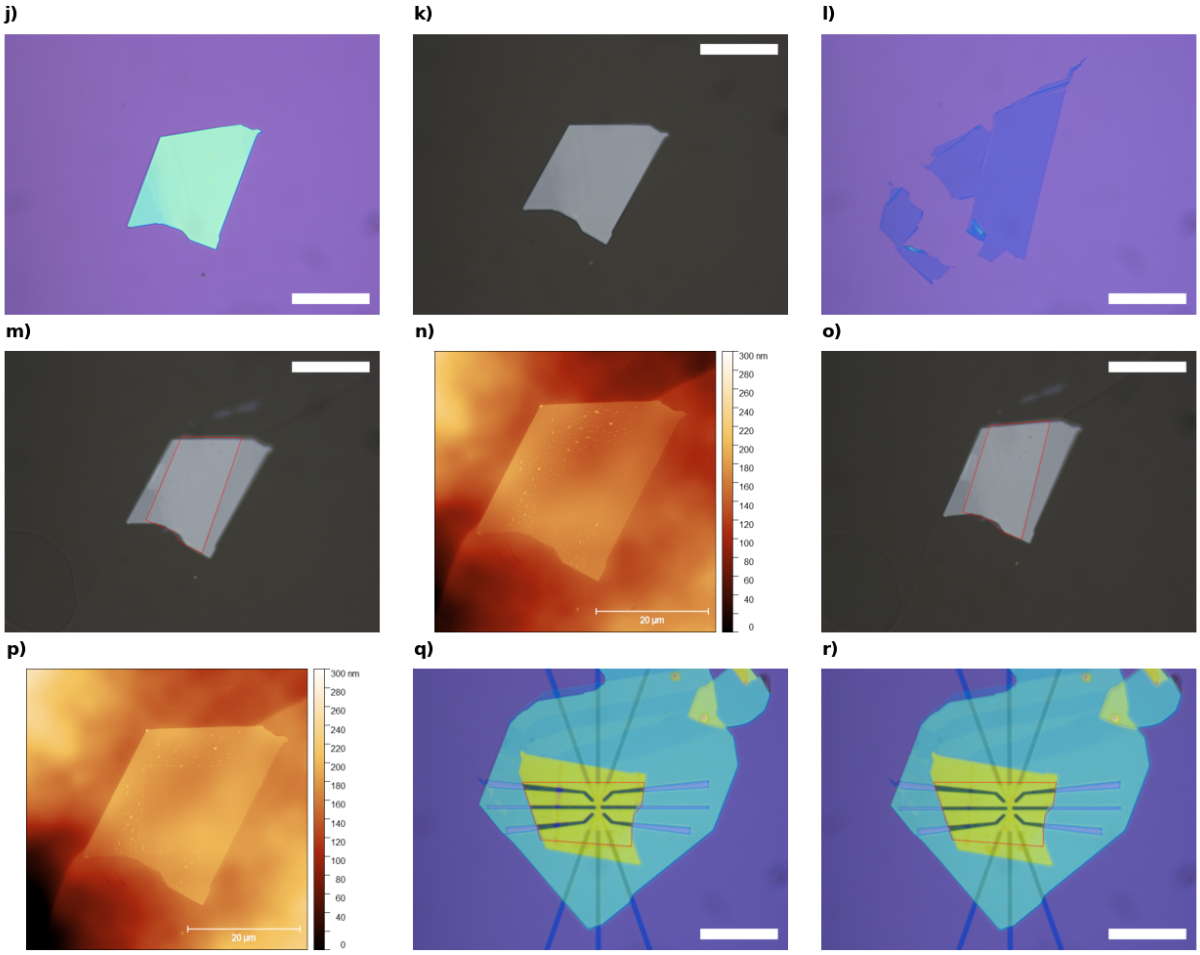
Figure B.5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20 µm

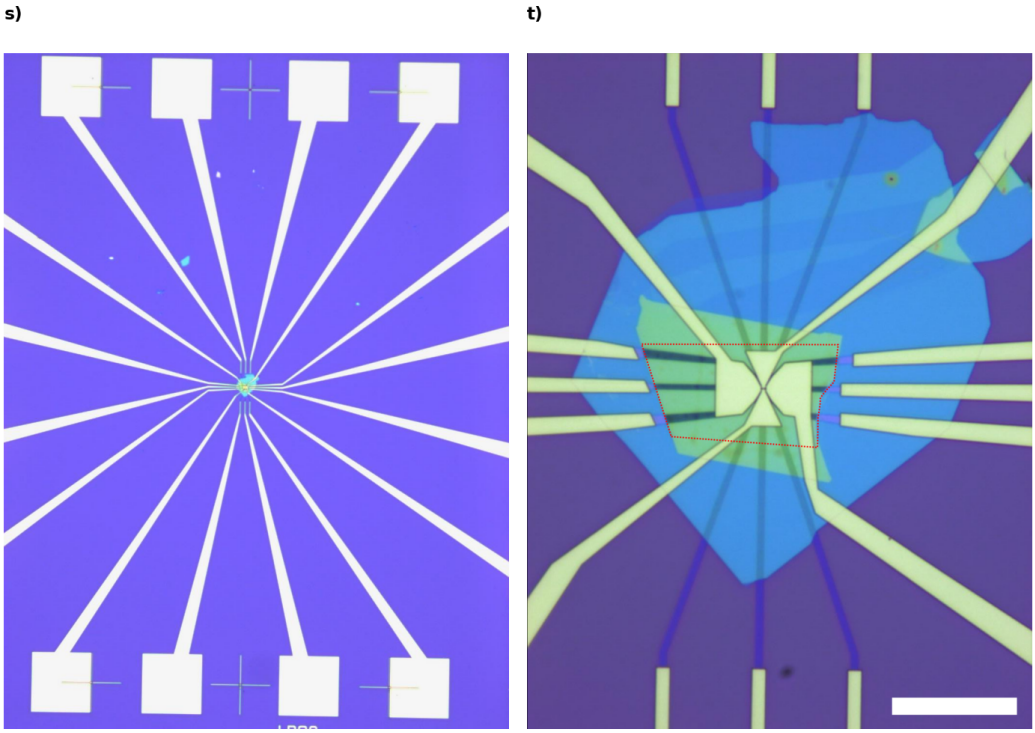

Figure B.5: Optical micrographs and AFM imgages of the complete fabrication process for WSe_2 batch 4, sample C. (a) Local control gates (Ti (2.5 nm) / Au (2.5nm)) are pre-patterned on a Si/SiO_2 substrate. (b) An hBN flake is exfoliated and identified (c) The hBN flake from (b) is picked-up using a PDMS/PPC stamp. (d) The same hBN flake is then transferred onto the local control gates. (e) Using a vacuum furnace, the hBN flake is cleaned for 30 minutes at 300°C. (f) Cr (2 nm) / Pt (8 nm) contacts are patterned onto the hBN flake. (g) The contacts are cleaned in the vacuum furnace for 30 minutes at 300°C. (h-i) Additionally cleaning is performed on the contacts by following the AFM brooming protocol. (j) An hBN flake is exfoliated and identified. (k) The hBN flake from (j) is picked-up using a PDMS/PPC stamp. (l) Monolayer WSe_2 is exfoliated and identified. (m-n) The WSe_2 flake is picked-up using the PDMS/PPC/hBN stack. A red-dashed line outlines the WSe_2 flake. (o-p) The WSe_2 surface is cleaned using the AFM brooming procedure. (q) The WSe_2/hBN stack is transferred onto the contacts. (r) The encapsulated sample is cleaned in the vacuum furnace for 30 minutes at 300°C. (s-t) Top gate electrodes and extensions going out to the contact pads are patterned to complete the device. All scale bars in the optical images are 20 μm.

Appendix C

Experimental setup

C.1 Low-temperature systems

To achieve the energy scales associated with the phenomena discussed in this thesis, the sample must be cooled to cryogenic temperatures. Based off the charging energy of 3.4 meV quoted in chapter 3, a temperature below 39 K is necessary to resolve this feature, and even lower temperatures may be desired to resolve additional features. To achieve these low temperatures, the measurements presented in this thesis were taken in three different cryogenic environments, each with their unique advantages.

The simplest and most time efficient method for measuring at low temperatures is by placing the sample in a large liquid helium (^{4}He) dewar which cools the sample down to 4.2 K. The sample is mounted on a chip carrier (Figure C.1) and attached to an insert (Fig. C.2a) which contains the electrical wiring necessary for connecting the pins from the chip carrier (and hence the sample) to an electrical box. The insert can slowly be lowered into the helium dewar until a temperature of 4.2 K is read by a temperature

sensor mounted near the sample. Going from room temperature to 4.2 K takes less than a couple of hours and measurements in this system can continue until all the helium in the dewar evaporates, typically on the order of weeks. This system is ideal for quick sample tests at low temperature due to the rapid sample turnaround.

Temperatures between 1.2 K– 4.2 K can be achieved by placing the same insert as before into a 1 K cryostat (Figure C.2a). This cryostat is separated into multiple compartments: the sample space, the inner vacuum chamber (IVC), the helium bath, and the outer vacuum chamber (OVC). The IVC thermally isolates the sample space from the helium bath while the OVC thermally isolates the helium bath from the exterior of the cryostat. A channel exists between the helium bath and the sample space where the flow of helium can be regulated by a needle valve. By opening the needle valve completely, liquid helium can occupy the sample space and cool the sample down to 4.2 K. To cool the sample even more, we utilize the fact that the boiling temperature of a liquid is a function of its vapor pressure. By pumping on the sample space and controlling the flow of the "warm" helium, the temperature of the liquid helium and the sample can be reduced to 1.2 K. A cool-down typically takes around 6 hours where the sample can then remain cold as long as the helium in the bath is not depleted. Because the sample space and the helium bath are separated, the helium bath can be replenished at any time without compromising the temperature of the sample.

Finally, a Bluefors LD250 dry dilution refrigerator (Figure C.2b-c) was used to achieve operating temperatures between 4.2 K and 10 mK. This system is considered a dry fridge because it does not require an external supply of cyogenic liquids to operate. A superconducting magnet can be mounted to the system capable of reaching magnetic fields of 8 T. The system is cooled down from room temperature to around 4 K by an in-series double pulse tube cryocooler, a process that takes 1-2 days depending on whether the magnet is

mounted or not. After the dilution refrigerator is cooled to 4 K, a mixture of ^{3}He and ^{4}He is circulated through the fridge via a scroll and turbo pump. A compressor is used to raise the pressure of the helium to about 2 bar which causes the mixture to condense and liquefy, filling the mixing chamber and part of the still. Pumping begins on the still resulting in evaporative cooling and a drop of temperature below 0.8 K. Below this temperature, the helium separates into two phases, the ^{3}He concentrated phase and the dilute phase, where the dilute phase accumulates at the bottom of the mixing chamber. The ^{3}He dilute phase pools up in the still, where in this state, the helium that is pumped away is almost pure ^{3}He as a result from the large difference in vapor pressures between the two isotopes. The evaporated ^{3}He is returned into the condensing line of the dilution refrigerator, introduced into the mixing chamber, and forced through the phase boundary which results in cooling. The evaporation of the ^{3}He in the still creates a concentration imbalance between the dilute phase in the still and the mixing chamber, resulting in the flow of ^{3}He from the mixing chamber to the still. This cycle is then repeated to achieve a base temperature of approximately 10 mK. The sample is mounted such that it is thermally coupled to the mixing chamber. An additional $\approx$ 5 hours is necessary to go from 4.2 K to 10 mK. From base temperature back to room temperature, it can take up to three days, therefore a total of 5 days should be reserved to exchange samples in this system.

Experiments in chapter 2 used all three systems. Experiments in chapter 3 were primarily performed in the 1 K cryostat while the initial tests were completed in the helium dewar. Experiments in chapter 4 were primarily conducted in the 1 K cryostat with the initial tests carried out in the helium dewar. The sample from chapter 5 was initially measured in the helium dewar and the 1K cryostat, but most of the results presented in this chapter were acquired while the sample was cooled in the dry dilution refrigerator.

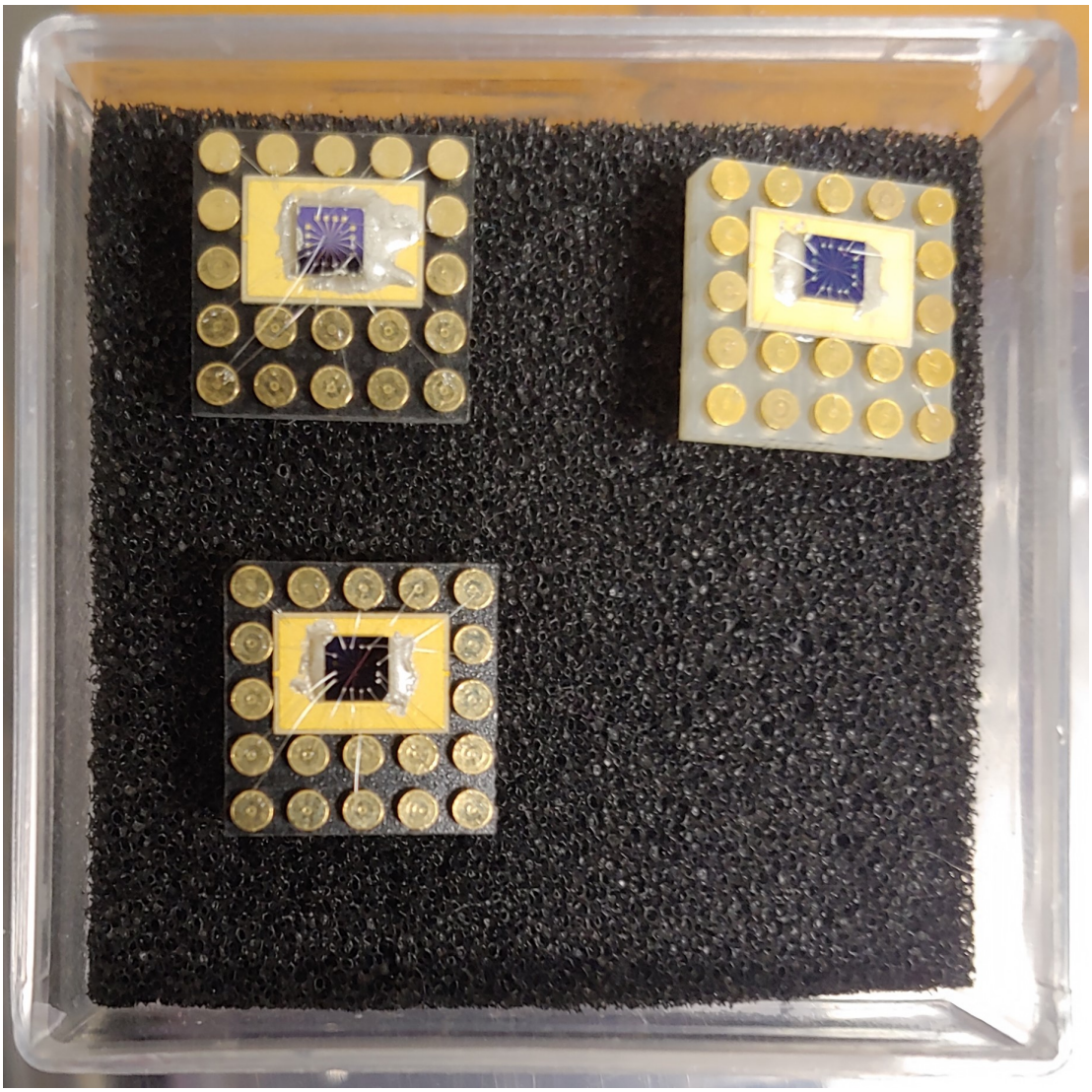

Figure C.1: Samples mounted to chip carriers which can be plugged in to the insert for the 1 K cryostat or the circuit board on the Bluefors LD250 dilution refrigerator. The samples are mounted on a gold plated pad which is also mounted on the chip carriers. Both are fixed using GE varnish. Silver epoxy is additionally used to electrically connect the silicon back gate to the gold plated pad. Using a wire bonder, the chip carrier's pins are connected to the contact pads on the sample by a thin gold wire.

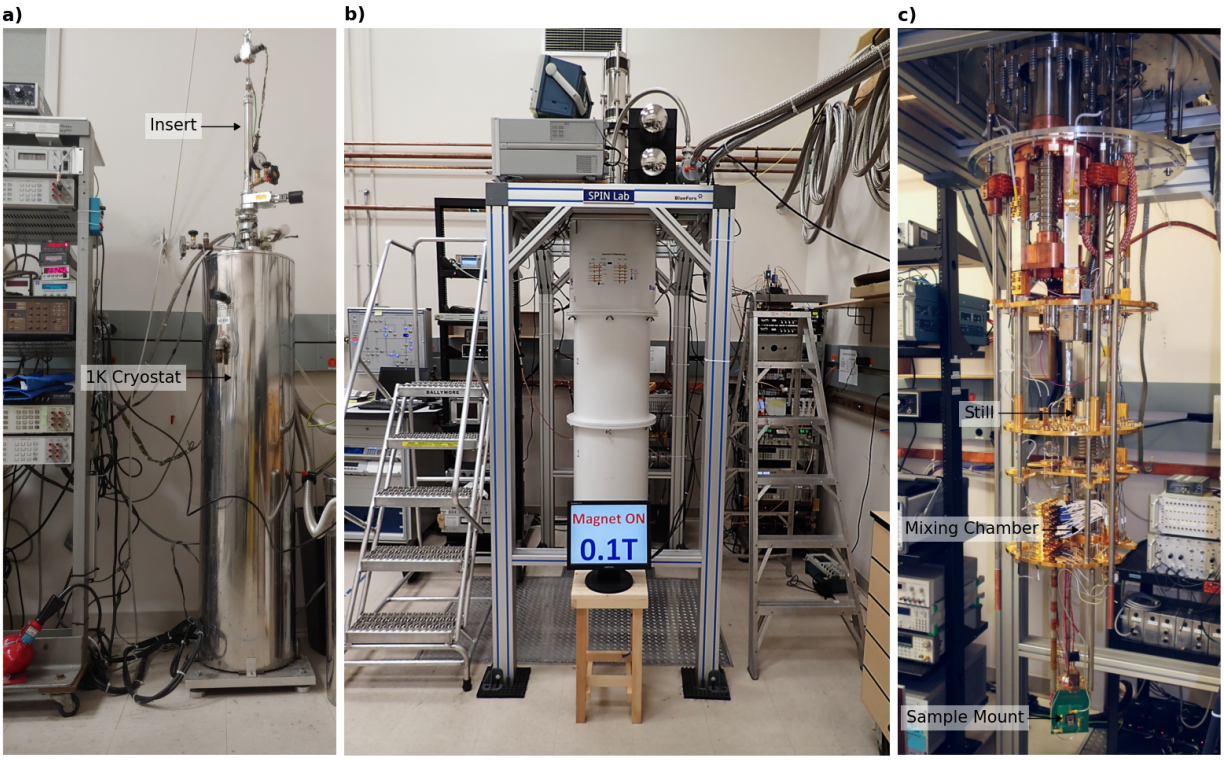

Figure C.2: (a) The 1K cryostat that was used in this thesis with the insert positioned inside the cryostat. The insert can be placed inside a helium dewar instead. (b) The closed and (c) opened Bluefors LD250 dry dilution refrigerator where the still, mixing chamber, and sample mount are clearly identified.

C.2 Electronics and measurement schemes

Sources of voltage and current were applied to two distinct types of electronic components in this thesis: the electrical contacts and the gates. Keysight 2900 source measuring units were used to simultaneously supply DC voltages to the gates and readout the current. The current was limited to 10 nA to avoid high leakage currents through the thin dielectrics and to prevent dielectric breakdown. The leakage current was measured and monitored during all electrical measurements. The source resolution of the voltage supply is between 100 nV and 1 μV and the measurement resolution of the current is between 10 fA and 100 fA, depending on the model used (2901/2902 vs. 2911/2912).

The Keysight 2900 source measuring units were also used to apply a source-drain DC voltage and to measure the source-drain current in a standard 2-point measurement scheme. An AVS-47 resistance bridge was further used to perform 2-point, 3-point, and 4-point measurements (Figure C.3). In a two-point measurement scheme, the measured resistance is a sum of the contact resistances and the channel resistance whereas the 4-point measurement resistance is sensitive to only the channel resistance. One can modify the 4-point measurement scheme by placing one of the voltage probes on the same contact used for the current source, resulting in a 3-point measurement. In this measurement setup, the resistance associated to the contact used as a current source and a voltage probe can be determined. These three measurement schemes are summarized in Figure C.3.

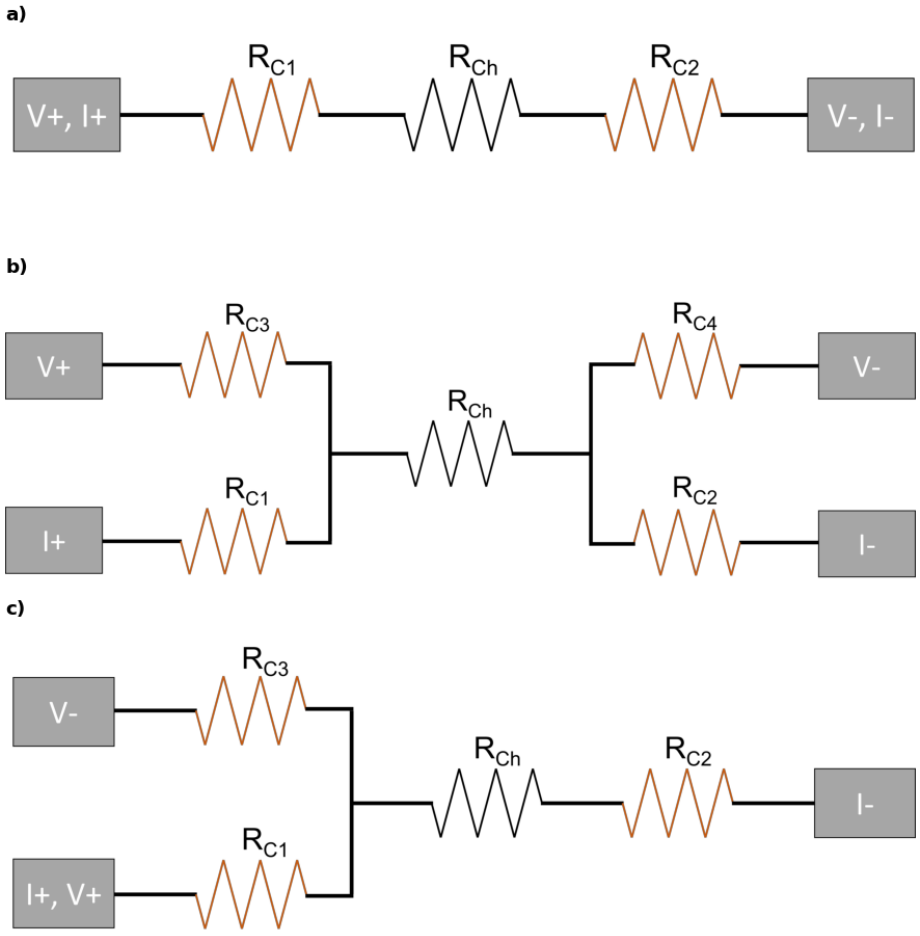

Figure C.3: Simplified circuit diagram of a 2-point measurement scheme (a), a 4-point measurement scheme (b), and a 3-point measurement scheme (c) where current flows from I_+ to I_- and V_+/V_- are voltage probes. R_{Ch} (black resistances) represents the channel resistance and R_{Ci} (orange resistances) represents the contact resistances. In the 2-point measurement scheme, the measured resistance is given by $R = \dfrac{\Delta V}{\Delta I} = \dfrac{V_+ - V_-}{I_+ - I_-} = R_{C1} + R_{Ch} + R_{C2}$. In the 4-point measurement scheme, the measured resistance is given by $R = \dfrac{\Delta V}{\Delta I} = \dfrac{V_+ - V_-}{I_+ - I_-} = R_{Ch}$. In the 3-point measurement scheme, the measured resistance is given by $R = \dfrac{\Delta V}{\Delta I} = \dfrac{V_+ - V_-}{I_+ - I_-} = R_{C1}$

Appendix D

Field-effect mobility calculation of WSe_2 device 4C

The characterization of TMD based devices via carrier mobility is a key metric to assess material quality and characterize the transport properties. A common and relatively simple method for extracting the carrier mobility can be done by varying the voltage applied to an accumulation gate while monitoring the conductance across the device. This type of measurement leads to an activation curve which contains a linear region at the beginning of the curve. From the slope of the linear regression taken across the linear region, the field-effect mobility may be obtained using the following relation:

$$\mu_{FE} = \frac{dG_{SD}}{dV_G}\frac{L}{W}\frac{1}{C_G}$$

where L and W are the length and width of the device channel, respectively, C_G is the capacitance per unit area of the dielectric separating the channel from the accumulation gate, and dG_{SD}/dV_G is the measured slope.

Typically, devices fabricated for mobility measurements are patterned to have very well defined lengths and widths. However, for the devices considered in chapter 5, the expression for the mobility was altered to conform to the unique device geometry. With that being said, the source and drain leads in these samples, where their dimensions are governed by the shape of the contact gates, form a channel that is geometrically friendly for the straightforward calculation of the L/W term (Figure D.1).

The L/W term can be thought of as a resistance ($R \propto L/W$), therefore, to calculate this term, we can break up the channel into individual components along the vertical axis and sum their contributions similar to the addition of resistors in parallel.

$$\frac{L}{W} = \left(\sum_i \frac{1}{R_i} \right)^{-1}$$

Here, $R_i = W_i/L_i$ are the individual components formed by breaking up the channel. To simplify the calculation, the channel is separated into 4 components as indicated by the shapes outlined in red in Figure D.1b. Defined by electron beam lithography, the rectangular pieces each have a width of 0.375 μm and a length of 1 μm. Then the equation above becomes:

$$\frac{L}{W} = \left(2 \left(\frac{0.375}{1} + \frac{1}{R_t} \right) \right)^{-1}$$

The factor of two appears because there are two sets of identical components. R_t is the contribution from the trapezoid. This value can be calculated by summing over all the infinitesimally narrow channels that add up to give the complete trapezoid.

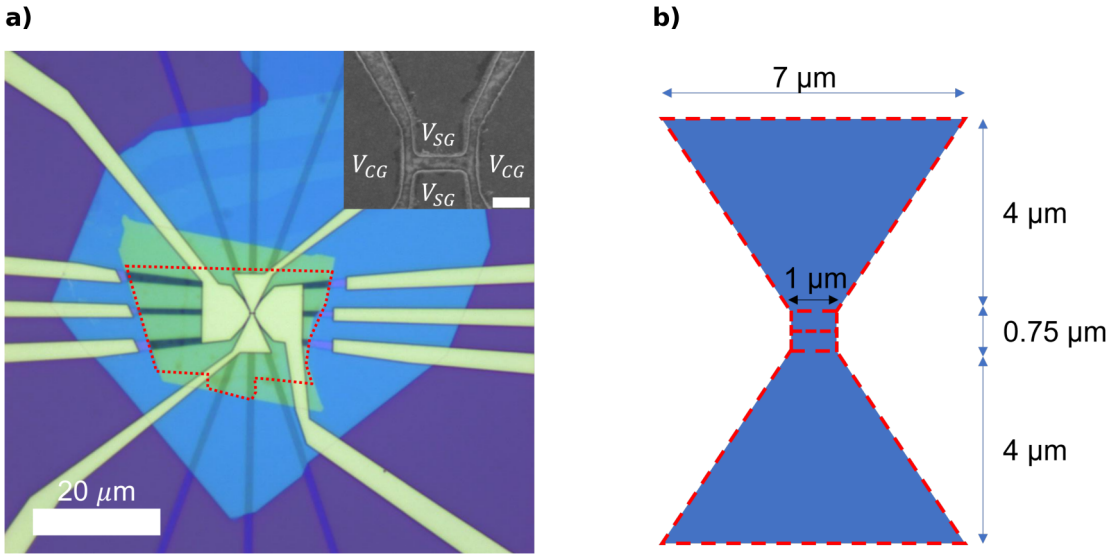

Figure D.1: (a) Optical micrograph of the device for which the hole mobility has been measured. Inset: Scanning electron micrograph of the top gate structure (scalebar is 400 nm). The geometry of the source and drain reservoirs are dictated by the contact gates (V_{CG}) resulting in a channel with the geometry described in (b).

$$R_t = \int_0^{W_t} \frac{dW}{L(W)} = \int_0^{W_t} \frac{dW}{L_0 + \frac{L - L_0}{W_t} W} = \frac{W_t}{L - L_0} ln \left(L_0 + \frac{L - L_0}{W_t} W_t \right)$$

where W_t, L_0, and L are the width, the short base, and the long base of the trapezoid, respectively. These values are lithographically defined to be 4 μm, 1 μm, and 7 μm, respectively resulting in $R_t = \frac{4}{6}\ln(7)$. Mobility of this device structure can now be calculated as:

$$\mu_{FE} = \frac{dG_{SD}}{dV_{BG}} \frac{1}{C_G} \left(2 \left(\frac{0.375}{1} + \frac{4}{6} \ln(7) \right) \right)^{-1}$$

For the device presented in chapter 5, the slope of the activation curve taken at 4 K was -302 $\mu S/V$ and the gate capacitance was 1.14×10^{-4} F/m^2 resulting in the reported

field-effect mobility of approximately 7 900 cm^2/Vs.

Appendix E

Interface thermal conductance calculation

In chapter 2, we presented a method for flattening large areas of van der Waals heterostructures based on localized thermal laser treatment. We proposed a model which suggests that the bubble content migrates when its kinetic energy overcomes its adhesion energy leading to the minimum bubble migration temperature:

$$T_{min} = \frac{4(d^2 - \pi a^2)}{k_B \rho \pi h(3a^2 + h^2)} \left(\frac{6E_{2D}h^4}{5a^4} + \gamma_w(cos\theta_{top\ material} + cos\theta_{substrate}) \right)$$

From AFM data acquired on graphene on rhenium disulfide samples, the above expression leads to a minimum migration temperature of $T_{min} = 430 \pm 60$ K, which was also confirmed with experimental data. From this migration temperature, we are able to extract the interface thermal conductance for a graphene/ReS_2 heterostructure, and find it to be $g = 0.725$ MW/m^{2}K. Here, we explain how this parameter is found.

In the system we are considering, a graphene/ReS_2 heterostructure is being locally heated by a 532 nm diode laser which can be thought of as a constant heat source. This heat can diffuse laterally through the graphene and also across layers into the ReS_2. This leads to the following steady state heat equations:

$$\frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r} + \frac{\alpha P}{\kappa_s t}\exp\left(-\frac{r^2}{r_0^2}\right) - \frac{g}{\kappa t}(T - T_A) = 0, \qquad \text{for } 0 \leq r \leq r_0$$

$$\frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r} - \frac{g}{\kappa t}(T - T_A) = 0, \qquad \text{for } r \geq r_0$$

where α is the percentage of absorbed light by graphene at 532 nm, P is the laser intensity, κ_s is the in-plane thermal conductivity of graphene, t is the thickness of monolayer graphene, g is the interface conductance between graphene and ReS_2, r_0 is the laser spot size, and T_A is the ambient temperature. We assume the laser follows a Gaussian distribution. Setting $\Theta = T - T_A$ and $z = \sqrt{\frac{g}{\kappa_s t}}r$, the differential equations become:

$$\frac{\partial^2 \Theta}{\partial z^2} + \frac{1}{z}\frac{\partial \Theta}{\partial z} - \Theta = -\frac{\alpha P}{g}\exp\left(\frac{z^2}{z_0^2}\right), \qquad \text{for } 0 \leq z \leq z_0$$

$$\frac{\partial^2 \Theta}{\partial z^2} + \frac{1}{z}\frac{\partial \Theta}{\partial z} - \Theta = 0, \qquad \text{for } z \geq z_0$$

These two equations are the non-homogeneous and homogeneous modified Bessel differential equations and have the following solutions:

$$\Theta(z) = C_1 I_0(z) + C_2 K_0(z) + \Theta_p(z), \qquad \text{for } 0 \leq z \leq z_0$$

$$\Theta(z) = C_3 I_0(z) + C_4 K_0(z) \qquad \text{for } z \geq z_0$$

$I_0(z)$ and $K_0(z)$ are the modified Bessel functions of the first and second kind, respectively, of order 0, and $\Theta_p(z)$ is a particular solution to the non-homogeneous modified Bessel differential equation. Using the variation of parameters methods, we find:

$$\Theta_p(z) = -\frac{\alpha P}{g} I_0(z) \int_0^z \frac{K_0(\bar{z})}{W(I_0(\bar{z}), K_0(\bar{z}))} \exp\left(-\frac{\bar{z}^2}{z_0^2}\right) d\bar{z} + \frac{\alpha P}{g} K_0(z) \int_0^z \frac{I_0(\bar{z})}{W(I_0(\bar{z}), K_0(\bar{z}))} \exp\left(-\frac{\bar{z}^2}{z_0^2}\right) d\bar{z}$$

where $W(x, y) = xy' - x'y$ is the Wronskian of x and y. To solve for the C_i's, we consider the following boundary conditions:

$$\lim_{z \to \infty} \Theta(z) = 0$$

$$\left.\frac{d\Theta(z)}{dz}\right|_{z=0} = 0$$

$$\Theta(z_0^-) = \Theta(z_0^+)$$

$$\left.\frac{d\Theta(z)}{dz}\right|_{z=z_0^-} = \left.\frac{d\Theta(z)}{dz}\right|_{z=z_0^+}$$

The first boundary condition states that the temperature of the graphene flake sufficiently far away from the laser is equal to the ambient temperature. This condition requires that $C_3 = 0$.

The second boundary condition ensures that hottest spot on the graphene flake is located at the center of the laser. This condition requires that $C_2 = 0$.

The third and fourth boundary conditions ensure that the temperature remains smooth and continuous at the edge of the laser spot. The third boundary then requires that:

$$C_4 = \frac{C_1 I_0(z_0) + \Theta_p(z_0)}{K_0(z_0)}$$

and the fourth boundary condition requires that

$$C_1 = \frac{\alpha P}{g} \int_0^{z_0} \frac{K_0(\bar{z})}{W(I_0(\bar{z}), K_0(\bar{z}))} \exp\left(-\frac{\bar{z}^2}{z_0^2}\right) d\bar{z}$$

Using these values for the constants, and the fact that $W(I_0(z), K_0(z)) = 1/z$, we can rewrite the solution as:

$$\begin{aligned}\Theta(z) = \frac{\alpha P}{g}(I_0(z) \int_z^{z_0} \bar{z} K_0(\bar{z}) \exp\left(-\frac{\bar{z}^2}{z_0^2}\right) d\bar{z}) \\ + K_0(z) \int_0^z \bar{z} I_0(\bar{z}) \exp\left(-\frac{\bar{z}^2}{z_0^2}\right) d\bar{z}, \qquad \text{for } 0 \le z \le z_0\end{aligned}$$

$$\Theta(z) = \frac{\alpha P}{g} K_0(z) \int_0^{z_0} \bar{z} I_0(\bar{z}) \exp\left(-\frac{\bar{z}^2}{z_0^2}\right), \qquad \text{for } z \ge z_0 \tag{E.1}$$

If we are interested in the temperature at the center of the laser, we can reorganize to find:

$$T(r=0) = T_A + \Theta(0) = T_A + \frac{\alpha P}{g} \int_0^{z_0} \bar{z} K_0(\bar{z}) \exp\left(-\frac{\kappa_s t}{g r^2} \bar{z}^2\right) d\bar{z}$$

From experiment, we found that the minimum migration temperature occurs at $T_{min} = 430 \pm 60$ K and at a laser power of 6 mW. Plugging those values in the above expression along

with $\alpha = 2.3\%$ [97], $r_0 = \dfrac{\lambda}{\pi N A} = 250$ nm, $P = \dfrac{6 \times 10^{-3}}{\pi r_0^2}$, $\kappa_s = 450$ $\mathrm{Wm^{-1}K^{-1}}$ [100, 101], and $t = 0.335$ nm [97], we extract a value of $g = 0.725$ $\mathrm{MW/Km^2}$.