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FACULTY OF GRADUATE AND
POSTDOCTORAL STUDIES

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Modeling of the Single- and Dual-Gate Microwave Field Effect Transistors for Computer Aided Design

by

Mohammad Abdeen

A dissertation submitted in partial fulfillment of the
requirements for the degree of

Doctor of Philosophy in Electrical and Computer
Engineering

Ottawa-Carleton Institute of Electrical Engineering
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List of Acronymes

ADS	Advanced Design System
ANN	Artificial Neural Networks
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CPU	Central Processing Unit
CPW	coplanar waveguide
DC	Direct Current
DG	Dual Gate
DGFET	Dual Gate Field Effect Transistor
DUT	Device Under Test
FET	Field Effect Transistor
GA	Genetic Algorithms
GaAs	Gallium Arsenide
GHz	Giga Hertz
GPIB	General Purpose Interface Bus
GRBF	Generalized-Radial Basis Function
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HP	Hewlett Packard
InP	Indium Phosphide

JFET	Junction Field Effect Transistor
MESFET	MEtal Semiconductor Field Effect Transistor
MISFET	Metal Insulator Semiconductor Field Effect Transistor
MLP	Multi-Layer Perceptron
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NEC	Nippon Electronic Corporation
RF	Radio Frequency
RBF	Radial Basis Function
SDD	Symbolically Defined Devices
SG	Single Gate
Si	Silicon
SOLT	Short-Open-Load through
SOM	Self-Organizing Maps
SOT	Small Outline Transistor
SPWL	Smoothed Piece-Wise Linear
TRL	Through-Reflect Line
TWT	Traveling Wave Tube
VLSI	Very Large Scale Integration

List of Symbols

A_0	Curtice model parameter
a_1	incident wave for port 1
A_1	Curtice model parameter
a_2	incident wave for port 2
A_2	Curtice model parameter
A_3	Curtice model parameter
α	Curtice model parameter
b_1	reflected wave for port 1
b_2	reflected wave for port 2
β	Curtice model parameter
C_{ds}	The drain-to-source capacitance of the field effect transistor
C_{gd}	The gate-to-drain capacitance of the field effect transistor
C_{gs}	the gate-to-source capacitance of the field effect transistor
C_{pds}	The parasitic drain-to-source capacitance of the field effect transistor
C_{pgs}	The parasitic gate-to-source capacitance of the field effect transistor
D	Drain terminal for the field effect transistor
D_{gd}	Gate-to-Drain diode
D_{gs}	Gate-to-Source diode
f_{max}	Maximum Oscillation Frequency
f_T	unity-gain frequency

G	Gate terminal for the field effect transistor
γ	Curtice model parameter
g_{ds}	The output conductance of the field effect transistor
g_m	The transconductance of the field effect transistor
I_{ds}	The DC drain-to-source current of the field effect transistor
I_{ds}^{DC}	The DC component of the drain-to-source current
I_{ds}^{RF}	The radio-frequency component of the drain-to-source current
I_{dss}	Zero-gate saturation drain current
L	Gate length of the field effect transistor
λ	Curtice model parameter
L_d	The drain inductance of the field effect transistor
L_g	The gate inductance of the field effect transistor
L_{pd}	drain packaging inductance
L_{pg}	gate packaging inductance
L_s	The source inductance of the field effect transistor
n	number of frequency data points
$n+$	heavily doped semiconductor with donor impurities
$Q(v_1)$	Stored charge for port 1 as a function of v_1
Q_d	Drain stored charge for the dual-gate MESFET
Q_{g1}	Gate1 stored charge for the dual-gate MESFET
Q_{g2}	gate2 stored charge for the dual-gate MESFET

Q_{gs}	the gate-to-source stored charge
R_{12}	inter-gate resistance of the dual-gate FET
R_d	the drain resistance of the field effect transistor
R_{ds}	The output resistance of the field effect transistor
R_{fd}	Gate-to-Drain diode differential resistance
R_{fs}	Gate-to-Source diode differential resistance
R_g	The gate resistance of the field effect transistor
R_i	The channel resistance of the field effect transistor
R_s	The gate resistance of the field effect transistor
S	Source terminal for the field effect transistor
S	The scattering matrix
S_{3P}	The three-port S-parameter matrix
σ	neuron activation function
T	Temperature in degrees Celsius
τ	The transconductance delay
T_r	Training data set
T_s	Testing data set
v_l	port 1 voltage as defined by ADS SDD
$V_{applied}$	Intrinsic applied voltage
V_{bi}	Built-in potential of the Schottky gate
V_{ds}	The DC drain-to-source voltage of the field effect transistor

v_{ds}	pulsed drain-to-source voltage amplitude
V_{ds0}	Drain-to-source model at model evaluation point
V_{gs}	The DC gate-to-source voltage of the field effect transistor
V_{gs0}	pinch-off voltage
V_{gs1}	The DC gate1-to-source voltage of the field effect transistor
v_{gs1}	pulsed gate1-to-source voltage amplitude
V_{gs2}	The DC gate2-to-source voltage of the field effect transistor
v_{gs2}	pulsed gate2-to-source voltage amplitude
V_{TO}	Curtice model threshold voltage
ω	the angular frequency
W	gate width for the field effect transistor
ω	neural network weights vector
Y	The admittance matrix
Z	The impedance matrix
z_j^l	The output of the j^{th} neuron at l layer

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They say first thing is first...

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Abstract

The increasing need for advanced communication technologies in the 21st century is leading to continuous development of new and more complex active devices and systems. Transistors such as BJTs, HBTs, FETs, and HEMTs are fundamental components in today's personal, corporate and global communication systems.

The single- and dual-gate MESFETs are widely used devices with wide areas of RF/Microwave applications. Due to their superior performance, MESFETs have been extensively used in high frequency, high-gain, and low-noise amplifiers, oscillator, mixers, and many other applications.

In this thesis, conventional and intelligent modeling methodologies are investigated for the applicability to today's computer-aided design methodologies and tools. Novel approaches of this work are applied to the area of small- and large-signal modeling of the GaAs MESFET (the single- and dual-gate.)

Optimal models for the single-gate MESFET are obtained using conventional techniques. A CAD tool called, TopFinder, is developed for optimal small and large-signal model generation. The tool has been successfully tested on a commercial single-gate MESFET and HEMT transistors.

Neural network modeling technique is applied to the modeling of the dual-gate MESFET. More specifically, neural network large-signal models for the dual-gate MESFET are developed. These models present the RF device performance behavior including temperature dependence. The neural network technique is successfully applied to two dual-gate MESFET devices; a discrete chip and an on-wafer chip. First, the drain current is modeled while presenting both isothermal (using pulsed measurements) and temperature dependent neural network model for the dual-gate MESFET. A comprehensive large-signal neural network model is also developed. This model includes the nonlinearity of conductances as well as those of the junction capacitances. The nonlinear dual-gate MESFET model is successfully incorporated into ADS. The model is verified by comparing the measurements of a nonlinear single-stage amplifier application based on the dual-gate MESFET to harmonic balance simulations in ADS showing satisfactory results.

Chapter 1

INTRODUCTION

1.1 *Motivation*

The increasing need for advanced communication technologies in the 21st century is leading to continuous development of new and more complex active devices and systems. Transistors such as BJTs, FETs, and HEMTs are fundamental components in today's personal, corporate and global communication systems.

The single- and dual-gate MEtal-Semiconductor FET (SG and DG MESFET) are popular devices with wide areas of RF/Microwave applications. Due to their superior performance over many other devices, MESFETs have been extensively used in high frequency, high-gain, and low-noise amplifiers, oscillator, mixers, and many other applications.

Modeling is an important step towards an efficient system design. Fast, accurate and efficient device modeling techniques are very important to enable the design community to catch-up with the ever-increasing demands for faster, feature rich and effective communication systems and applications.

Conventional, circuit based and empirical models have extensively been used in RF and microwave device modeling. Recently, techniques based on artificial intelligence have been introduced and have shown a significant success. Intelligent techniques include genetic algorithms, fuzzy logic and artificial neural networks.

The RF and microwave design process has been following a classical model for quite some time. In this model, one starts with the desired design specifications and arrives at an initial configuration for the circuit to be designed. Available design data and previous experience provide the help needed in selecting the initial design configuration. Analysis and synthesis procedures are used for deciding values of various parameters of the design. A prototype is constructed for the initial design and measurements are carried out for evaluating its characteristics. The prototype is modified if its performance is not with good agreement with the desired specifications. Adjustment, tuning, and timing mechanisms are incorporated in the design to carry out these modifications. Measurements are carried out again and the results are compared with the desired specifications. This process is repeated until the desired specifications are achieved. The final design is then sent to fabrication. This process has become increasingly difficult because of the increased complexity of modern systems, variety of active and passive components, and the difficulty to incorporate modifications in modules fabricated by integrated circuit technology.

The emergence of computer-aided design (CAD) methodologies revolutionized the way RF and microwave systems are built. With CAD techniques and with the enormous improvement in computer technology (speed, capacity and memory) the complete design process is performed on the desktop easier, faster and more efficiently. Today's commercially available CAD tools have built in libraries of numerical models of many RF and microwave devices and components. These models are ready to use in order to evaluate the performance of a given circuit. Moreover, many optimization techniques along with sensitivity analysis are also available to tune and optimize the design. When the full simulation of the design achieves the performance specifications, the design can then be sent to fabrication.

Artificial Neural Networks (ANNs) have emerged as a powerful technique for modeling input/output relationships. They have been used for many complex applications such as control, telecommunications, biomedical, and pattern recognition. In recent years, however, ANNs are being used more and more in the area of RF/microwave design. Neural-network techniques have been used for a wide variety of microwave applications such as modeling of transmission-line components, vias, coplanar waveguide (CPW) components, FETs, amplifiers, etc. Recently, the work on straight applications of standard neural networks techniques to microwave problems has led to advanced work in RF and microwave-oriented

neural network structures, training algorithms, knowledge-based networks, and methodologies for libraries of microwave neural models developments. Neural networks offer many advantages for nonlinear modeling. They are fast, accurate and more importantly have the ability to generalize. By “generalize” we mean the ability to respond correctly to new data that has not been used for model development.

In this work, conventional and intelligent modeling methodologies are investigated for the applicability to today’s computer-aided design approaches and tools. Novel approaches of this work are applied to the area of small- and large-signal modeling of the GaAs MESFET (the single- and dual-gate.)

1.2 *Thesis overview*

This thesis presents two major contributions for the modeling of gallium arsenide semiconductor field effect transistors. The first is to design and build a CAD tool that is able to construct optimal circuit based models. The second is to employ the state-of-the-art modeling techniques, i.e. neural networks, to achieve more accurate, fast and efficient models for the field effect transistor.

The approaches discussed in this work are applied to two of the most popular active devices in today’s communication and microwave systems, namely the single- and the dual-gate MESFET. The development of small- and large-signal models is the central issue discussed. Circuit based as well as neural network models are considered.

This thesis is organized in 7 chapters, including this one. In chapter 2, an overview of the single- and dual-gate MESFETs as well as the measurement and characterization methods is presented. Chapter 3 presents an overview of the RF and microwave device modeling techniques that will be used throughout this work along with a literature survey.

In chapter 4, conventional modeling techniques are used to obtain optimal transistor model. This is achieved through a computer-aided design tool developed in this work, TopFinder, for optimal small and large-signal model generation. The tool has been successfully tested on two practical examples of a commercial single-gate MESFET and HEMT transistors.

In chapters 5 and 6, device modeling with intelligent techniques for computer-aided design is presented. Neural network large-signal models are developed. These models present the RF device performance characterization including temperature dependence. In chapter 5, the technique is successfully applied to two dual-gate MESFET devices; a discrete chip and an on-wafer chip. Only drain current is modeled in this chapter while presenting both isothermal (using pulsed measurements) and temperature dependent neural network drain current model for the dual-gate MESFET.

In chapter 6, a comprehensive large-signal neural network model is developed. This model includes the nonlinearity of conductances as well as of the junction capacitances. The model is successfully incorporated in one of the most popular commercial circuit simulator, i.e. the Agilent Advanced Design System (ADS [8]). The model is verified by comparing the measurements of a nonlinear single-stage amplifier application based on the dual-gate MESFET to harmonic balance simulations in ADS and is shown to have a satisfactory accuracy.

Chapter 7 presents a thesis summary, conclusions and recommendations for future research works

1.3 Thesis Contributions

The following is a list of the original contributions of this work:

For the Single-Gate FET

In chapter 4, the author developed a CAD tool to enable the designer to find the optimal small-signal topology for a single-gate MESFET/HEMT given a set of S-parameter measurements. Optimal topology in the context of this thesis is defined as the topology that gives the minimal S-parameter fitting error so far reported in the literature. The details of this work are given in the following list.

1. Developed a CAD methodology for optimal small-signal topology generation for the GaAs MESFET. This methodology is implemented as a tool called TopFinder. This tool provides designers with important answers to questions such as: what is the most appropriate topology for the measurement in hand for a given FET?. The tool is demonstrated on the EFA018A GaAs MESFET [55],[58]. Furthermore, the versatility

of the tool is demonstrated by obtaining an optimal topology for a HEMT transistor. The demonstrated device is the EPB018A5 low noise high gain HEMT.

2. The tool is further enhanced to include the ability to select the best large-signal device model under given operating conditions. This capability is demonstrated on the NE71000 GaAs MESFET [56].

For the Dual-Gate GaAs MESFET

In chapters 5 and 6, models based on neural networks (henceforth called neural network models) for the dual-gate MESFET are developed. The models include isothermal (based on pulsed measurements) as well as temperature dependent RF and DC drain current models. A large-signal neural network model that includes nonlinear capacitances and output conductance is also developed within the context of this thesis. The complete large-signal neural network model for the dual-gate MESFET is successfully implemented in ADS. The model is verified through a nonlinear amplifier application based on the dual-gate MESFET. The model and the simulations showed reasonable agreement. Details of the work on the dual-gate MESFET are listed below:

1. Introduced for the first time the neural network approach to modeling the dual-gate MESFETs. An isothermal large-signal neural network model for the RF drain current of the dual-gate MESFET is developed. This model is based on pulsed measurements and is therefore isothermal. This is demonstrated on the NE25118 dual-gate GaAs MESFET [59][61]. Furthermore, a combined DC and RF large-signal drain-current neural network model for the dual-gate MESFET is developed. This model is valid across a wide range of DC bias conditions. This is also demonstrated on the NE25118 dual-gate GaAs MESFET [57].
2. Developed a temperature dependent large-signal neural network model for the dual-gate MESFET. This is demonstrated on an on-wafer dual-gate GaAs MESFET manufactured by Nortel Networks [60].

3. Developed a comprehensive large-signal neural network model for the dual-gate MESFET that includes conductances as well as junction capacitances [62]. The model is verified through an on-wafer single-stage nonlinear amplifier application. The model is also implemented in ADS and harmonic balance simulations are compared to the experimental harmonic content measurements with a satisfactory agreement.

Chapter 2

OPERATION AND CHARACTERIZATION OF THE FIELD EFFECT TRANSISTOR

2.1 Introduction

The Field Effect Transistor (FET) is a three terminal electronic device which controls the current flowing between two terminals with the voltage applied to the third. The current flows from one terminal (called the source, S) to another (called the drain, D). The controlling terminal is called the gate (G).

The field-effect transistor comes in several forms. In the junction FET (called a JFET) the control (gate) voltage varies the depletion width of a reverse-bias p-n junction. Alternatively, the metal gate electrode may be separated from the semiconductor by an insulator (metal-insulator-semiconductor FET, called MISFET). A common special case of this type uses an oxide layer as the insulator (MOSFET). A similar device to the JFET results if the p-n junction is replaced by a Schottky barrier (metal-semiconductor FET, called MESFET). The MESFET is very useful in high-speed digital or microwave circuits and applications. Particular advantages exist for the III-V compounds such as GaAs or InP due to the higher mobility and carrier drift velocities than Si.

Throughout this work, attention is focused on the GaAs MESFETs (both the single- and dual-gate) due to their important role in radio frequency (RF) and microwave applications.

2.2 The single-gate MESFET: structure, operation and applications

The single-gate MEtal Semiconductor Field Effect Transistor, or MESFET, is a semiconductor device that is used in switching and amplification applications. It consists of a undoped (semi-insulating) GaAs substrate to provide physical support for the device. The gate is formed by a metal-semiconductor contact (Schottky-barrier) in direct contact with the n-type GaAs that forms the channel region. The channel length, L , is defined by the length of the gate electrode and similarly for the width, W . To reduce the parasitic resistances between the drain and the source contacts and the channel, the two contacts are surrounded with a heavily doped n^+ GaAs. The structure of the MESFET and its circuit symbol are depicted in Figure 2.1.

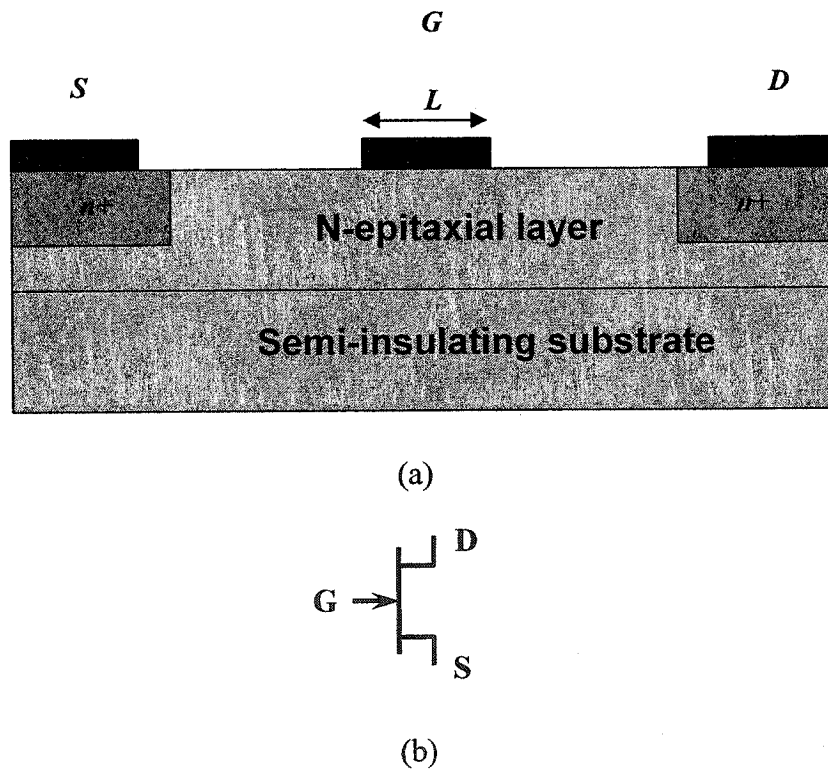
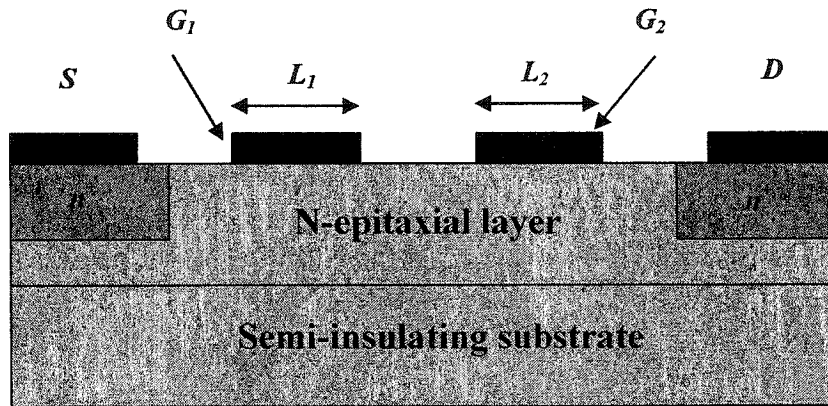


Figure 2.1 The n-channel GaAs MESFET: (a) structure, (b) circuit symbol

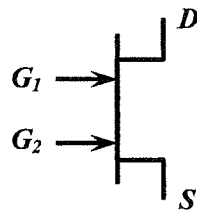
The MESFET has some very attractive applications in the RF/Microwave area due to its high switching speed (very small “on” resistance) and its relatively high cut-off frequency. A typical MESFET has a cut-off frequency of around 30 GHz and can go up until several tens of GHz.

2.3 The dual-gate MESFET: structure, operation, and applications

The dual-gate MESFET is a variation of the single-gate with a second gate between the first gate and the drain. The device is built on a semi-insulating GaAs substrate. An n-type epitaxial active layer is grown on the substrate forming a channel. The Source and Drain electrodes are surrounded with heavily doped n^+ GaAs regions to reduce the parasitic resistance between the electrodes and the channel. The electrodes of the two gates are formed on the n-channel and form two Schottky barrier contacts. The structure of the dual-gate MESFET can be symmetric, i.e. equal gate dimensions and equal spacing, or it can be asymmetric. Figure 2.2 depicts the structure of the dual-gate MESFET and its circuit symbol.



(a)



(b)

Figure 2.2 The n-channel dual-gate GaAs MESFET: (a) structure, (b) circuit symbol

Liechti [13] showed that the dual-gate MESFET can be approximated as two single-gate FETs, FET1 and FET2, in a cascode connection and having a constant drain current (Figure 2.3).

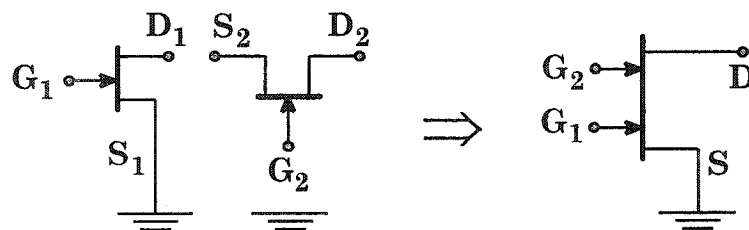


Figure 2.3 The dual-gate FET model as a cascode connection of two single-gate FETs

In general terms, there are four modes of operation of the DGFET based on the two FETs in cascode criteria:

1. Both FET1 and FET2 are in saturation region.
2. FET1 is in the triode region while FET2 is in the saturation region.
3. FET2 is in the triode region while FET1 is in the saturation region.
4. Both FET1 and FET2 are in the triode regions.

The advantages of the DGFET over the single gate of comparable size include higher gain, gain control, better input gate-to-drain isolation, and higher output impedance. That made it attractive for various nonlinear circuit applications such as mixers, frequency multipliers, and power combiners.

Building efficient RF/microwave circuits and systems can not be achieved without sufficient characterization of their components. Device characterization starts with the measurement of their behavior under various operating conditions (i.e. small- or large-signal) and then developing a suitable model for them. The remainder of this chapter is dedicated to present an overview of the essential measurement methods for RF/microwave devices. The chapter to follow presents their modeling techniques.

2.4 Measurement methods for the FET

This section presents a brief review of typical measurement methods for general transistor characterization. Selecting the appropriate measurement type depends on the characterization criteria. For example, load-pull measurements can be selected if large-signal transistor characterization is required. However, the availability of equipment may limit the type of measurement selected. Load-pull setups are usually very expensive and other measurement strategies might be used as a substitute to a more desirable measurement method.

2.4.1 Direct current-voltage (DC I-V) measurements

The DC I-V measurement is the most fundamental of all device measurement methods. In this type of measurement, the most significant current component of the device is plotted against its corresponding device terminal voltage with respect to the common terminal. DC

device measurement has the advantage of being easy to perform even in simple laboratories and yet provides relatively good estimates for many device parameters.

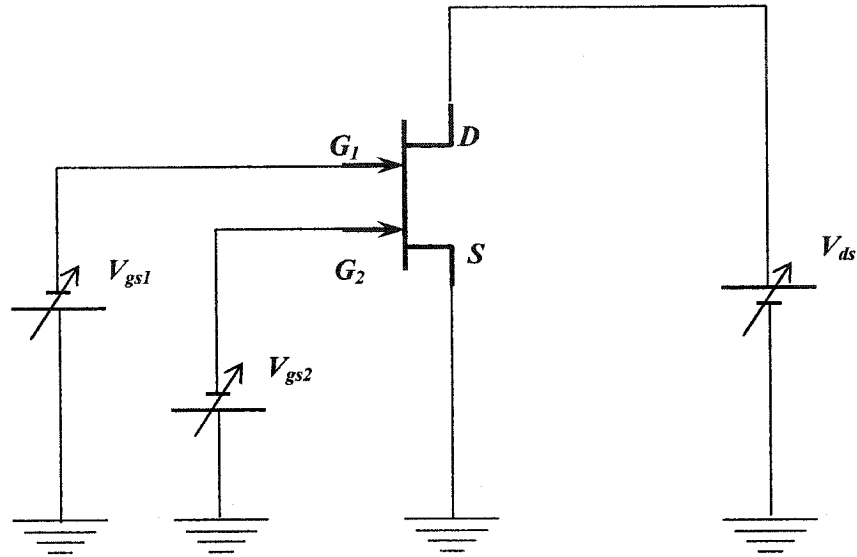


Figure 2.4 A schematic for the DC I-V measurement setup for the n-type dual-gate FET

Typically, microwave MESFETs are employed in the common source configuration. In the case of single-gate FET, the drain current I_{ds} is plotted against the drain-source voltage V_{ds} while the gate-source V_{gs} voltage is held at a fixed value. For the dual-gate MESFET, the drain current I_{ds} is measured against the drain-source voltage V_{ds} , while both gates are held at a fixed voltage, V_{gs1} and V_{gs2} . A DC I-V family of curves can be generated by changing the V_{gs} values (or V_{gs1} and V_{gs2} in the dual-gate case). As an illustration, a schematic for the DC I-V measurement setup for the dual-gate FET is depicted in Figure 2.4.

Modern laboratory equipments made it a fairly easy task to measure the DC I-V for a given device. With computer interfaces, such as the general purpose interface bus (GPIB), many power supplies and multi-meters can be programmed to automatically measure the device I-V curves with virtually no user intervention. For such automated measurements to be performed reliably, chip and discrete components should be mounted on a well designed test

fixture to provide a 50 Ohm environment and hence prevent device oscillation. On wafer devices, on the other hand, are mounted on microwave probe stations for DC and other high-frequency measurements. Those stations use coplanar transmission line probes, which bring 50 Ohm lines directly to the device terminals on the wafer.

2.4.2 S-parameter measurements

The DC measurements alone are not sufficient for microwave device characterization. As will be shown in Chapter 3, many small-signal model element values can not be determined from DC measurements and can only be determined from RF measurements.

Scattering parameter (S-parameter) measurements are the most popular RF device measurement technique. For a two port device, a four-tuple set (magnitude and angle) at each frequency value constitutes a complete set of S-parameter at a given bias point. Equation (2.1) is the defining formula for S-parameters for a two port device (Figure 2.5).

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (2.1)$$

where a_1 and a_2 are the normalized incident waves and b_1 and b_2 are the normalized reflected waves.

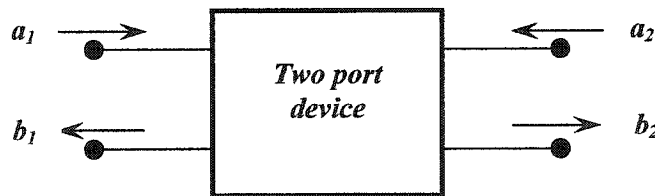


Figure 2.5 Two port S-parameter configuration

It is to be noted that S-parameter values depend on the DC bias condition of the device. In other words, if the bias point of the device changes, a new set of S-parameters will be required to characterize the device at the new bias point.

Automatic S-parameter measurement setups are readily available in most microwave laboratories. The measurement setup consists of computer controlled power supplies, multimeters, and most importantly the network analyzer. All the devices are connected to a computer through a general purpose interface and can be pre-programmed with a user friendly interface. Commercially available instrumentation software (e.g. LabView) can provide excellent environment for automated measurement. The device should be mounted on a suitably designed test fixture (for discrete or chip devices) with the accompanying calibration kit. The microwave S-parameter measurements can be very accurate even up to frequencies as high as 110 GHz (the Agilent 8510 Network Analyzer system). The accuracy of the measurements depends mostly on the calibration and the ability to de-embed the test fixture. The two most common calibration techniques are the through-reflect-line (TRL) and the short-open-load through (SOLT) [41].

2.4.3 Pulsed I-V measurements

Although DC I-V measurements are easy to perform, device parameters, such as the transconductance g_m and the output conductance g_{ds} , extracted from DC measurements are different from their RF counterparts. The DC parameter values can only be used as first approximations when seeking the device RF models. This is due to the low frequency dispersion characteristics of these parameters. Moreover, the DC measurements of the drain current are not performed under iso-thermal conditions. For high drain currents in particular, the channel of the device overheats and the device temperature rises. As a consequence, the drain current of the FET decreases when the channel temperature rises [88].

Pulsed I-V measurements are preferred over the DC ones. They have the advantage that the FET parameter values extracted from them are very close to the RF values [71]. Under pulsed measurements, the DC drain current of the device is constant and therefore the device is measured under iso-thermal conditions.

Pulsed I-V measurement of the MESFET is performed by applying pulsed voltage to either of the gate(s), the drain, or both of them while DC biasing the device in the cut-off region. The pulse serves to drive the device into saturation for a very brief period of time that is short enough that the device does not heat-up. The pulsed drain current is then measured by a current probe or any other measurement device (as will be shown in a later chapter). A schematic of a pulse measurement setup for the dual-gate FET is shown in Figure 2.6.

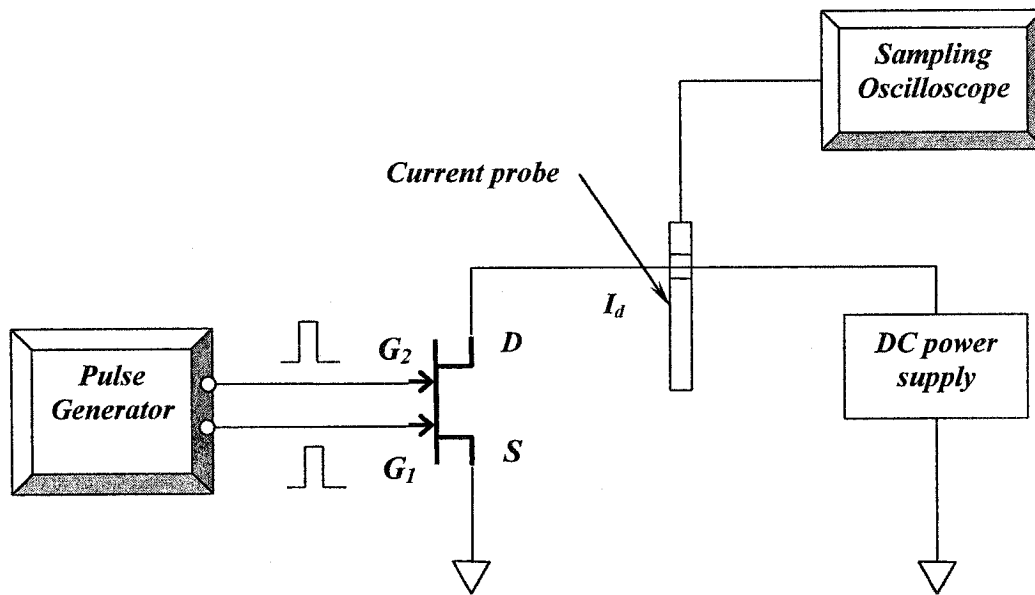


Figure 2.6 Pulsed I-V measurement equipment configuration for the dual-gate FET.

2.4.4 Load-pull measurements

In large-signal MESFET circuits, such as power amplifiers and oscillators, small-signal RF characterization techniques (e.g. S-parameters) are not suitable. Due to the high power levels of these applications, the device behaves as a nonlinear element and linear characterization techniques render inaccurate results. Alternatively, large-signal measurement techniques have been developed. The most popular of them is the load-pull measurement.

Load pull measurements involve embedding the device to be tested into measurement circuitry that can be impedance tuned. The measurement system simultaneously monitors the

tuned impedance of the characterization circuitry and the performance of the device. Device response is then recorded under the variable load conditions. The resulting loci of impedances required to obtain a constant performance parameter (i.e. output power or power added efficiency) are displayed on a smith chart in the form of closed contours. The load-pull contours are determined one frequency at a time. Also the load-pull contours apply to only one incident power level used in the measurement.

Load-pull equipment configurations can be classified into two general categories. *Traditional* and *active-load* pull systems.

Traditional load-pull systems utilize mechanical adjustments to change the circuit impedance. These include slide-screw tuners, dielectric slug tuned air lines, and microstrip tuning. Figure 2.7 illustrates an equipment configuration that can be used for load pull measurements.

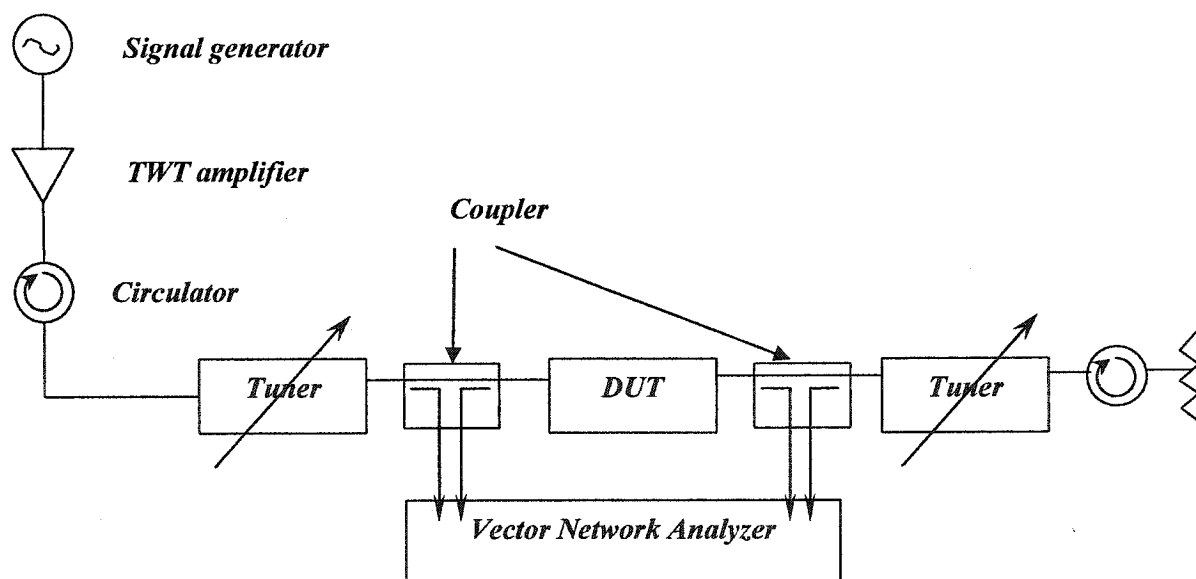


Figure 2.7 Typical test equipment configuration for traditional large-signal load-pull measurements

Active-load pull measurement systems overcome many of the problems associated with traditional load-pull systems. In this method, two phase- and amplitude-controlled RF signals are applied to the device. No physical impedance tuner is required. The major advantage of this system is that the load reflection coefficient obtained is not limited in magnitude. By independently adjusting the input attenuators, virtually any reflection coefficient can be synthesized [41].

2.4.5 Other measurement techniques

There exist several other large-signal measurement techniques for FET characterization. These techniques are not used in this research due to the unavailability of the measurement equipments. A list of some of them is given below:

1. Pulsed S-parameter measurements. Rather than using continuous wave (CW) S-parameter measurements DC bias conditions, Pulsed S-parameters under pulsed DC bias conditions can be a better alternative. Pulsed Bias/S-parameter measurements do not cause the device to overheat and therefore present better models under isothermal conditions.
2. Multi-bias S-parameter measurement. In this technique, small-signal S-parameter measurements are done at many bias conditions to generate large-signal models.
3. Two-tone harmonic content measurement. This technique is used to measure the nonlinear device behavior. In this technique, the output spectral content of the device is recorded while two input signals, closely spaced in the frequency and of equal magnitudes, are applied to the input of the device. The measurement is made for increasing input power levels.

2.5 Conclusions

In this chapter, a brief overview of FET measurement techniques is presented. Obtaining accurate measurements with a reliable measurement setup is the first step toward a successful design. Device modeling is important for models built for use in circuit and systems design and performance evaluations. This step required the availability of accurate measurement data. The following chapter is dedicated to reviewing modeling methodologies and techniques used for FET. Emphasis is given to those techniques relevant to this research.

Chapter 3

MODELING TECHNIQUES FOR THE RF/MICROWAVE FET

This chapter reviews various modeling techniques for RF and microwave devices. Conventional, or classical, modeling techniques are those that do not involve learning techniques, are extensively used in the field, and are proven robust and reliable. Other techniques are relatively more “modern” and have been recently introduced to the modeling of engineering problems and more specifically in the area of RF/microwave devices. The distinctive property of these modern techniques is that they are “intelligent”. An explanation of the term will be given within the context of this chapter. Emphasis is given to techniques (both conventional and intelligent) relevant to the research work discussed herein.

3.1 Device modeling with conventional techniques

3.1.1 Introduction

There are three categories of device models based on the type of performance predictions for which the models are used: the small-signal, the large-signal and the noise models. These models provide the device/circuit designer with a specific component behavior as linear (small-signal) or nonlinear (large-signal). Noise models are to predict the device noise performance in a circuit or a system. The following sections give an overview of the

small- and the large-signal models. Noise models for the FET are outside the scope of this work.

3.1.2 Small-signal circuit models and parameter extraction

When an electron device operates in its linear region or on small signals (e.g. small-signal amplifiers), it is modeled as a linear system. In this the linear model is a combination of linear circuit elements (resistors, capacitors, inductors, linear sources). A given configuration of such circuit elements is called a *topology*. The device model accuracy depends on the selected topology and the values of its elements.

A standard MESFET equivalent circuit topology [66][26] is shown in Figure 3.1.

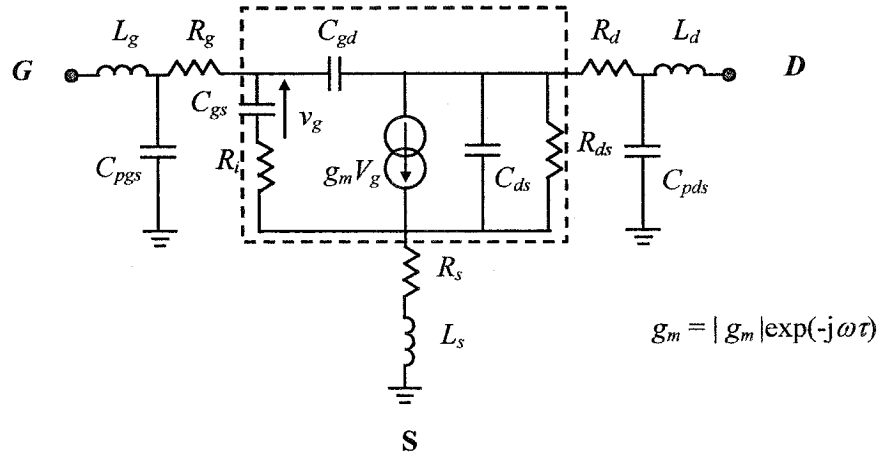


Figure 3.1 A standard equivalent circuit topology for MESFETs

The following is a list of the topology elements and their description:

L_s : is the source parasitic inductance.

L_d : is the drain parasitic inductance.

L_g : is the gate parasitic inductance.

R_s : is the source parasitic resistance.

R_d : is the drain parasitic resistance.

R_g : is the gate parasitic resistance.

C_{pds} : is the drain-to-source parasitic capacitance.

C_{pgs} : is the gate-to-source parasitic capacitance.

C_{gs} : is the gate-to-source depletion capacitance.

C_{gd} : is the gate-to-drain depletion capacitance.

C_{ds} : is the drain-to-source depletion capacitance.

R_i : is the charging resistance.

$|g_m|$: is the magnitude of the device transconductance.

τ : is the transconductance delay.

R_{ds} : is the output resistance.

Other topologies have also been described in the literature [4], [16],[86] but the standard topology provides a sufficient accuracy for frequencies around 26 GHz. The circuit topology is used to predict the device small signal behavior where measurement data are not available. The topology is divided into two groups of elements; the extrinsic (or parasitic) elements (ones outside the dotted line) and the intrinsic elements that represent the bulk of the device (inside the dotted elements).

The values of the elements of the equivalent circuit topology can be obtained by direct measurement, by using some physical device models, or by indirect measurements using a technique called *parameter extraction*.

Parameter extraction is a technique whereby element values of a transistor model topology are found. In this technique, a set of small-signal S-parameter measurements are performed for the device over the desired modeling frequency range. The values of the equivalent circuit elements are found such that they best fit the set of previously measured S-parameters. There are two approaches for parameter extraction. The first is mainly mathematical where optimization techniques, such as Quasi-Newton and Levenberg-

Marquardt, are used to fit the desired set of functions [43], [96]. In this approach, convergence to a physically meaningful solution strongly depends on the selection of a “good” starting point. Otherwise, the algorithm may either converge to a physically meaningless result or may not converge at all. The second approach depends on performing some simple experimental work to obtain the values of the extrinsic elements. The intrinsic elements can then be computed analytically subject to some assumptions [24] [26] [66]. Analytical formulas require the computation of the intrinsic admittances of the device. These are obtained by de-embedding the effects of the parasitic elements from the device impedance/admittance matrix. These matrices are easily calculated from the device S-parameter measurements [21]. As an example, the gate-to-source and gate-to-drain capacitances, C_{gs} and C_{gd} are obtained by the following relations:

$$C_{gs} = \frac{\text{Im}(Y_{11}) - \omega C_{gd}}{\omega} \left(1 + \frac{\text{Re}(Y_{11})^2}{(\text{Im}(Y_{11}) - \omega C_{gd})^2} \right) \quad (3.1)$$

$$C_{gd} = -\frac{\text{Im}(Y_{12})}{\omega} \quad (3.2)$$

where Y_{ij} are the Y -parameters of the intrinsic elements and ω is the angular frequency. A complete set of these relations can be referred to in [66], [41].

For the dual-gate MESFET, and as suggested by several researchers, the small-signal model is a combination of small signal models of two single-gate MESFETs connected in cascode [13][90]. The first FET (FET1) is in a common source configuration while the second (FET2) is in a common gate configuration. Figure 3.2 shows a schematic for this model.

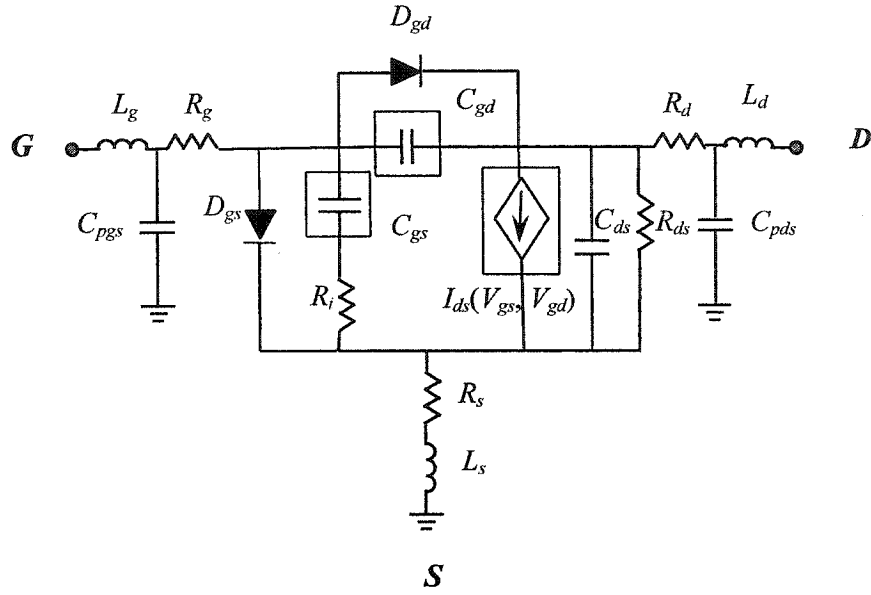


Figure 3.3 A large-signal equivalent circuit for the single-gate MESFET.

The main nonlinear elements of the circuit shown in Figure 3.3 are:

1. The drain-source current I_{ds} controlled by the voltages V_{gs} and V_{gd}
2. The gate-source capacitance C_{gs}
3. The gate-drain capacitance C_{gd}
4. The diodes D_{gs} and D_{gd} which are important in modeling the forward-bias gate current and the drain-gate avalanche current respectively.

Empirical modeling is a common technique in the area of electron devices. In this technique a given device characteristic (e.g. I-V) are fitted to a function. This function is in most cases nonlinear and depends on the parameters affecting the device characteristic under consideration. A typical procedure to develop a device model is to first measure the device characteristics (e.g. drain current). Then a mathematical function that behaves similarly is found. The mathematical function includes adjustable parameters that, when assigned proper values, will cause the function to approximate the measurement data.

Empirical models are widely used in large-signal FET modeling. One of the first such models was proposed by Van Tuyl and Liechti [87] and later modified by Curtice [97]. The quadratic Curtice model consists primarily of the voltage-controlled current source I_{ds} , gate-source C_{gs} capacitance, and gate-drain capacitance C_{gd} as the nonlinear elements. The modeling equations proposed by Curtice are:

$$I_{ds}(V_{gs}, V_{ds}) = \beta (V_{gs} - V_{TO})^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \quad (3.3)$$

where V_{gs} and V_{ds} are the intrinsic terminal voltages and β , V_{TO} , λ , and α are the model parameters, and

$$C_{gs, gd} = C_{gs0, gd0} \left(1 - \frac{V_{applied}}{V_{bi}} \right)^{-1/2} \quad (3.4)$$

where V_{bi} is the built-in potential of the Schottky gate, $V_{applied}$ is the intrinsic gate-source or gate-drain voltage, and $C_{gs0, gd0}$ is the zero-bias gate-source or gate-drain capacitance.

Statz *et al.* developed a more accurate model by introducing some modifications to the model proposed by Curtice. The square-law dependence of Curtice model on the term $(V_{gs} - V_{TO})$ is replaced with a new expression. In addition, the hyperbolic function turned out to be computationally intensive and is replaced with a polynomial. The complete Statz model is given by Equations (3.5) and (3.6)

$$I_{ds} = \frac{\beta(V_{gs} - V_{TO})^2}{1 + b(V_{gs} - V_{TO})} \left[1 - \left(1 - \frac{\alpha V_{ds}}{3} \right)^3 \right] (1 + \lambda V_{ds}) \quad \text{for } 0 < V_{ds} < \frac{3}{\alpha} \quad (3.5)$$

$$I_{ds} = \frac{\beta(V_{gs} - V_{TO})^2 (1 + \lambda V_{ds})}{1 + b(V_{gs} - V_{TO})} \quad \text{for } V_{ds} \geq \frac{3}{\alpha} \quad (3.6)$$

A complete set of current and capacitance Statz model is given in [41].

Curtice and Ettenberg altered the original Curtice model in order to produce a closer fit to the relationship between the drain-source current as a function of the gate-source voltage. The exponent of the $(V_{gs} - V_{TO})$ term took a value other than 2. A cubic approximation was used and the result was to have more freedom in matching the device characteristics. The

resulting model is called Curtice-Ettenberg or Curtice cubic model. The equations of this model are given by:

$$I_{ds} = (A_0 + A_1V_1 + A_2V_1^2 + A_3V_1^3) \tanh(\gamma V_{ds}) \quad (3.7)$$

with

$$V_1 = V_{gs} [1 + \beta(V_{ds0} - V_{ds})]$$

where V_1 is used to model the occurrence of pinch-off voltage increase with drain-source voltage, γ , β , and A_i 's are the model parameters, V_{ds0} is the drain-source voltage (in saturation) at which the A_i coefficients are evaluated.

Several other nonlinear models exist and they vary in the number of model parameters and the model accuracy. Adding more model parameters has the advantage of giving the designer more freedom to obtain better fitting for a given device. On the other hand, obtaining the values of a given model parameter might grow complex as the number of model variable increase, and therefore complicating the parameter extraction task. The Materka and the TriQuint Own Model (TOM) models [41] are examples of other large-signal FET models.

For the dual-gate FETs, some large-signal models have been reported in the literature, though not as many as those of the single-gate. This is because dual-gates are relatively more complex and are not as popular as the single-gate FET.

In [3], Madjar presented a model by extending another model developed for the single-gate FET. In this model, the electric field equations are solved to obtain the relation between the terminal currents and the applied voltages. This model is rather a physical model since it requires the device physical dimensions. These are not usually available and if so, their accuracy is poor. Moreover, Madjar's model did not agree well with the device measurement data.

Darling [84] proposed a distributed model by solving Poisson's equation numerically subject to the appropriate boundary conditions. However, the model computation time grows significantly as required accuracy increases. In addition, this model is not suitable for computer aided design tools.

There is currently two empirical models for the dual-gate FET, one suggested by Jenner [63] and another by Ibrahim [67]. In Jenner's model the nonlinear drain current is represented by a three-dimensional power series approximation. However, obtaining good accuracy can require as many as 165 parameters. Moreover, the model is generated from DC measurements and does not take into account the frequency dispersion of the transconductance and the output conductance. On the other hand, although the model developed by Ibrahim *et al.* required only 49 parameters, it still presents a significant amount of model extraction procedures. In addition, the RF current component in the model required the extraction of the transconductance from three-port S-parameter measurements. This presents a fairly complex and costly process.

From the above discussion, it is shown that there is hardly one large-signal dual-gate FET model that is sufficiently accurate and, more importantly, suitable for use in today's most versatile design methodologies, viz. the computer aided design. A need is therefore urgent to develop a model that fulfills both requirements.

3.1.4 Other Device Models

In addition to the aforementioned model types, others have been reported in the literature. These models are listed here without further details as they are outside the scope of this work. These models are:

- Physical models: which are based on the physical properties of the device, such as gate length, gate width, doping concentrations, carrier mobility, *et cetera*
- Table based models: use a table of measurement data to model the device characteristics. The size of the table grows exponentially with the number of elements being modeled. In addition, interpolation and extrapolation is needed to obtain element values not in the table which degrades the model accuracy. Table-based models are less computer-intensive than the physically based models.

3.2 Modeling with intelligent techniques

3.2.1 Introduction

Conventional modeling techniques have been the subject of research and study for several decades. Their applications include the fields of machine control, image and signal processing, circuit theory, RF and microwave circuits, and many other areas. Conventional techniques, however, sometimes lack the necessary flexibility to deal with problem variations and tuning issues. This restricts the problem solving capability of these methods to problems that are well understood. With today's computer speed and technology, processing power can be used to solve other problems that are not well understood and/or their solutions are not readily known.

Intelligent techniques have emerged as an alternative to conventional ones with significant successes. These techniques include Genetic algorithms, Neural Networks, and Fuzzy logic.

(a) Genetic Algorithms

Genetic algorithms (GAs) are search procedures that use the mechanics of natural selection and natural genetics. A genetic algorithm, first developed by John H. Holland in the 1960's [33], uses evolutionary techniques, based on function optimization and artificial intelligence, to develop a problem solution. The basic operation of a genetic algorithm is relatively straightforward. First a population of possible solutions to a problem is developed. Next, the better solutions are recombined with each other to form some new solutions. Finally the new solutions are used to replace the poorer of the original solutions and the process is repeated.

GAs are attractive in engineering design and applications because they are easy to use and are likely to find the *globally* best design or solution. This is because GAs are less susceptible to getting "stuck" in a local minima. Some of the GA applications include, structure design, process design, planning, VLSI design, control systems, electrical power systems, pattern recognition, classification problems, and many others. GAs are also suitable for multi-objective optimal design problems, involving multiple objectives. Optimization with Genetic algorithms can be conveniently used in CAD tools to solve optimization

problems. The focus of this research is to develop models suitable for CAD tools other than finding solutions for existing models. Therefore, genetic algorithms will not be considered in this research.

(b) Fuzzy logic

Fuzzy logic was introduced by Zadeh in the mid 1960's [52]. Classical logic is described as Boolean in the sense that it assumes that every element is either a member or a non-member. This imposes a restriction to express imprecise concepts, for example, whether the room is "hot" or "cold". Fuzzy logic, on the other hand, introduced for the first time the idea of partial set membership. It extends Boolean logic to handle the expression of vague concepts and, as a result, solve the preceding problem. To express imprecision in a quantitative fashion, fuzzy logic introduces a set membership function that maps elements to real values between zero and one (inclusive); the value indicates the "degree" to which an element belongs to a set. A membership value of zero indicates that the element is entirely outside the set, whereas a one indicates that the element lies entirely inside a given set. Any value between the two extremes indicates a degree of partial membership to the set.

Fuzzy logic is well-suited for systems that require the ability to handle vague data and/or model imprecise reasoning procedures. Many commercial applications of fuzzy logic relate to "process control", which refers to the management of a mechanical or environmental process. Examples of fuzzy logic technology include air conditioning, cruise control, and video cameras. Fuzzy techniques have been also used in the area of microwave application as a data processing front end for other modeling techniques (such as neural networks) [10].

From the above discussion, it is seen that fuzzy logic is not conveniently suitable for device modeling applications to be discussed in this work. Accordingly, intelligent techniques using fuzzy logic methods will not be further investigated.

(c) Artificial Neural Networks

Artificial Neural Networks (ANNs) have emerged as a powerful technique for modeling input/output relationships. They have been used for many complex applications such as control, telecommunications, biomedical, and pattern recognition. In recent years, however, ANNs are being used more and more in the area of RF/microwave design. Neural network

techniques have been used for a wide variety of microwave applications such as modeling of transmission-line components [23], [24], [93], vias [81], coplanar waveguide (CPW) components [80], FETs [1], [37], [94], amplifiers, [98] etc. Neural networks have also been used in impedance matching [74], and inverse modeling [76]. Recently, the work on straight applications of standard neural network techniques to microwave problems has now led to advanced work in RF and microwave-oriented neural network structures, training algorithms, knowledge-based networks, and methodologies for libraries of microwave neural models developments.

Due to their advantages and suitability to this research work, the ANN is selected to be the intelligent technique applied to modeling problems in this research proposal. The following section gives a background of the basics of the neural networks and their modeling methodologies and approaches.

3.2.2 Artificial Neural Networks

An artificial neural network is an information processing paradigm. It is inspired by the way the biological nervous systems, such as the brain, process information. It has two physical components; the processing elements (called neurons) and the connections between them (called links). Every neuron receives a stimulus from the neighboring neurons connected to it, processes the information, and produces an output. Each link has a weight parameter associated with it. Neurons that receive stimulus from outside the network (i.e. not from another neuron) are called input neurons. Neurons whose outputs are used externally are called output neurons. Other neurons outside those categories are called hidden neurons. Different neural network structures can be constructed based on the selection of the processing elements and the way they are connected. These structures include the multi-layer perceptron (MLP), the radial basis function networks (RBF), the self-organizing maps (SOM), and others [83]. In this research work, the MLP structure is considered as the main neural structure because it is relatively easy to use and at the same time is sufficient for the research objectives.

(a) The multi-layer perceptron

The multilayer perceptron (MLP) is the most popular neural-network structure in which the neurons are grouped into layers. The first and the last layers are called input and output layers, respectively and the remaining layers are called hidden layers. For example an MLP3 is a neural network of one input layer, one output layer, and one hidden layer. The “universal approximation theorem” states that a multilayer perceptron network (MLP) can approximate any arbitrary multidimensional function [46]. Figure 3.4 shows a typical MLP3 neural network. In this Figure, each circle represents a neuron, and an array of horizontally adjacent neurons represents a layer. The input layer is the first layer and the last layer is the output layer (bottom up).

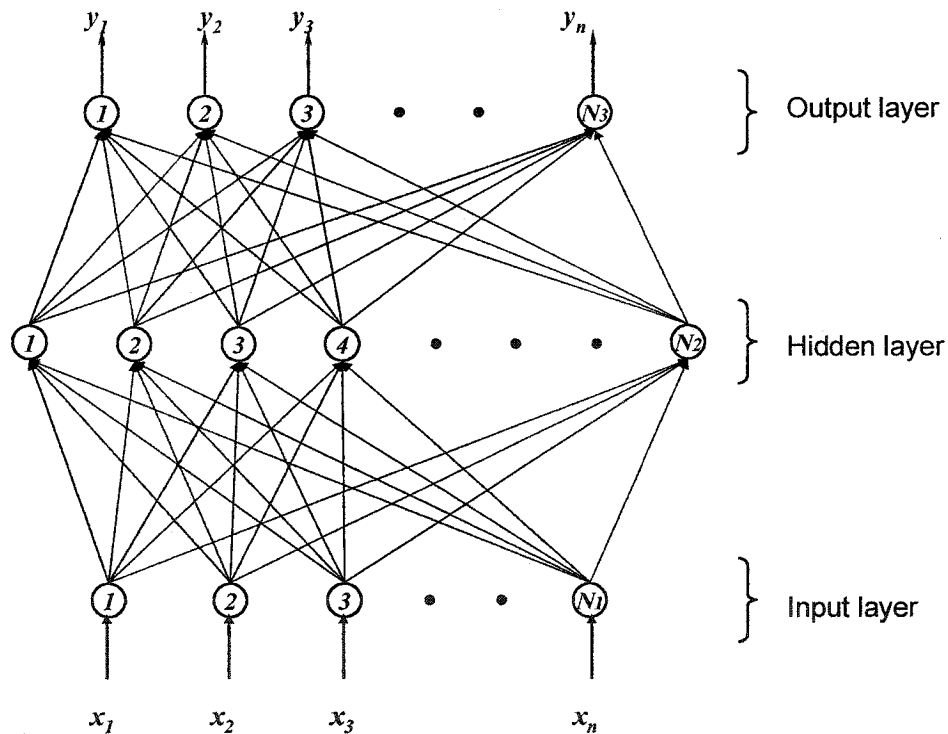


Figure 3.4 A three-layer neural network (MLP3)

(b) The activation function

An output z_j^l of the j^{th} neuron at a layer, l , is a weighted sum of all inputs from neurons of a previous layer, $l-1$, with weighting parameters, ω_{ij}^l . The summed output is passed through a function called a neuron activation function $\sigma(\cdot)$. The most commonly used activation function for hidden neurons is the sigmoid function given by

$$\sigma(\gamma) = \frac{1}{(1 + e^{-\gamma})} \quad (3.8)$$

where γ is given by

$$\gamma_i^l = \sum_{j=0}^{N_{l-1}} \omega_{ij}^l z_j^{l-1} \quad (3.9)$$

and

$$z_i^l = \sigma(\gamma_i^l) = \sigma\left(\sum_{j=0}^{N_{l-1}} \omega_{ij}^l z_j^{l-1}\right) \quad (3.10)$$

where z_j^{l-1} is the j 's output from layer $l-1$ and ω is the weights vector.

The output at the output layer y_i is given by

$$y_i = z_i^L = \sigma\left(\sum_{j=0}^{N_{L-1}} \omega_{ij}^L z_j^{L-1}\right) \quad (3.11)$$

where L is the index of the last (output) layer. The zero index accounts for a DC bias component of the neural network that might be necessary for some nonlinear functions.

Other possible activation functions include the arc-tangent and the hyperbolic-tangent functions. All activation functions share the properties of being bounded, continuous, monotonic, and continuously differentiable.

(c) Training process and algorithms

Neural networks need to be trained in order to represent a certain component characterization. Measurement data is usually split into two or three sets depending on the amount of data available. One set, called the training set T_r , is used to train the model.

Another set, called the verification set V , is used to guide the model during the model generation process. A third set is the testing set T_s , and is used for model testing. Ideally the three data sets should be mutually exclusive and uncorrelated. Depending on data availability, the appropriate percentages can be selected. A typical one is 50/50 split between the training/verification and the testing. In some other cases, 80/20 percentiles are used.

Gradient and non-gradient based techniques are used to minimize the training error E_{Tr} by adjusting the weights vector ω . Examples of gradient based algorithms are the back propagation, the conjugate-gradient, the Quasi-Newton, and the Levenberg-Marquardt algorithms. The Simplex method is considered as a non-gradient based method. Global optimization techniques such as simulated annealing can also be used [83].

(d) Neural network training

The training of a neural network is a process with which the weighing values are determined by feeding the network with a pre-determined input-output data pairs $\{(x_k, d_k)\}$, where x_k and d_k are the n - and m -vectors representing the inputs and desired outputs of the neural network. The neural network training error is defined as

$$E_{Tr} = \frac{1}{2} \sum_{k \in Tr} \sum_{j=1}^m |y_j(x_k, \omega) - d_{jk}|^2 \quad (3.12)$$

where d_{jk} is the j^{th} element of d_k and $y_j(x_k, d_k)$ is the j^{th} neural-network output for input x_k , Tr is the training data set.

(e) Number of layers and number of neurons

To date there exist no theoretical method to determine the required number of layers or the number of neurons in a given layer of a neural network model. It is mainly based on trial and experience although in theory the three layers are sufficient.

(f) Overlearning and underlearning

Overlearning is a case where the neural network memorizes perfectly the training data but fails to make generalizations, i.e. to predict the data values not included in the training data set. Excessive number of neurons of a neural model can lead to overlearning.

Underlearning is when the network is not even able to learn the training data. It is indicative of the use of insufficient number of neuron for the neural model or insufficient data.

3.2.3 Literature survey of neural network applications in microwave devices and circuit modeling

The use of the artificial neural network in microwave applications is relatively new. In 1992, Vai *et al.* [75] proposed the use of a neural network representation of Smith chart. With this approach, the inaccuracy of the estimation process associated with smith chart methodology is avoided. This technique is later extended and used for impedance matching [73].

In 1994, Zabaab *et al.* [1] first introduced the use of neural network in microwave circuit analysis and design at the device and circuit level. At the device level, they used a neural network FET model to replace the device physics based model. This made it easy for performance optimization since the device equations are not repeatedly solved. The training data for the FET used in their work was based on the physical dimensions rather than on measurements.

Shirakawa *et al.* [49] used a neural network approach to model the large-signal characteristics of an HEMT. They combined the circuit based model of the HEMT with a neural network representation of the nonlinear circuit elements (i.e. drain current and nonlinear capacitances). They also argued that the three-layer MLP model introduced in [1] requires a relatively large number of neurons and hence longer training time. By building a multi-layer (five layers) neural model, Shirakawa *et al.* managed to reduce the number of necessary neurons to only 26 neurons. This served to reduce the training time significantly.

Further work on MESFET/HEMT neural modeling have been carried out by Lazaro *et al.* [70]. They obtained a more accurate large-signal models by fitting both the I-V curves of the MESFET/HEMT devices, as well as their derivatives up until the third order. They also included valuable comparisons between the performance of various neural network architecture, namely the generalized-radial basis function (GRBF) network, the smoothed piece-wise linear (SPWL) network, and the well-know multilayer perceptron (MLP) network.

There have been no reports, however, and to the best of our knowledge, on using a neural network approach for modeling the small and/or large signal characteristics for the dual gate FETs. The neural network approach offers significant gains to the dual-gate FET modeling that other modeling methods do not. Detailed neural models for the dual-gate MESFET are covered in Chapter 5 and 6 of this research work.

3.3 Conclusions

In this chapter, an overview of the modeling techniques for the RF and microwave FET is presented. Both small- and large-signal models for the single- and dual-gate FET have been considered. Conventional (circuit based and empirical) as well as intelligent techniques are reviewed. Neural network modeling technique is reviewed in more details as it will be the base for the research work presented in chapter 5.

The chapters to follow in this research proposal presents the novel contributions achieved using conventional as well as neural techniques with highlights to their relevance to today's computer-aided design techniques.

Chapter 4

OPTIMAL MODELING OF THE SINGLE-GATE FET

4.1 Introduction

In the previous chapters, a review of conventional as well as intelligent techniques for modeling the field effect transistor was presented. The proposed focus of this research work is to determine, study, and enhance design techniques suitable for the today's widely used computer aided design tools. This can be achieved by either enhancing classical techniques to be more suitable for computer aided design or by using modern ones that readily lend themselves to computer aided design methodologies. The common denominators of the two approaches are speed, accuracy, and most importantly, suitability for automation.

This chapter shows how conventional modeling techniques can be appropriately enhanced for computer aided design with application to the small- and large-signal modeling of the single-gate MESFET. It is shown that not only accurate small and large-signal single-gate MESFET models are automatically generated, but those models are also optimal subject to a given criterion.

4.2 An optimal small-signal circuit based FET model for computer-aided design

In today's ever evolving technological age, device modeling and characterization play an important rule in systems design complying with international standards. With better device

models and modeling tools, significant improvement in performance predictions of systems built with these devices can be achieved. Efficient device modeling is therefore a central issue in building today's communications systems.

A small signal transistor model consists of a circuit topology and the values associated with its elements. A standard topology used in most of the FET small-signal models as well as in commercial circuit simulators was introduced in Chapter 3 (Figure 3.1). This topology provides good performance predictions till a frequency of 26 GHz. However, for some devices and for higher frequency range this topology does not provide good accuracy [41]. Designers often have to “tweak” the topology by adding other components to compensate or account for some physical phenomena. As an example, Materka [4] added inductances at the drain and the gate terminals (L_{pd} , L_{pg}) to account for the packaging inductances. Berroth [64] added differential resistances of the gate to source R_{fs} , and gate to drain R_{fd} , diodes to account for the operating points of forward gate bias. Menozzi [86] added resistances R_{gs} and R_{gd} to account for reverse gate currents for some high performance devices such as InP-based MODFET with rather leaky gates. He also added a drain to gate capacitance C_{pgd} to account for padding.

In summary, device modeling as it stands today, starts by assuming a given topology and then finding its element values that fit a given set of S-parameter data in a specific frequency range. For the cases where the result is not satisfactory, an experienced designer is required to add several more elements to the topology to improve fitting results. Clearly, this modeling procedure is lengthy, tedious, and requires significant expertise. It is also not optimal in that the final topology is specific to a given device and similar steps have to be repeated for another device even if it is of a similar type. Moreover, this procedure is based on manual, trial and error process that requires a fair amount of expertise whose level is not sustained for devices obtained through a new or updated technology.

The development of a computer aided design tool is of a significant benefit in such a scenario. The tool can help speed up the characterization/design process with significant improvement in accuracy. The main objective of such a tool is to automatically determine the topology that best fits a given measurement data and to attain its parameter values (parameter

extraction).

In the following sections, a new computer aided design tool is presented with which an optimal topology is generated through a recursive process rather than assuming a fixed topology *a priori*. The proposed CAD tool is called TopFinder [58]. The obtained topology is optimal in the sense that it best fits a given set of measurement data (e.g. S-parameters.) The core optimization algorithm of the tool is based on error criteria according to the following relationship[41]:

$$E_{ij} = \sum_{k=1}^n \frac{|S_{ij\text{meas}}^k - S_{ij\text{mod}}^k|}{|S_{ij\text{meas}}^k|} \quad (4.1)$$

where E_{ij} is the error in a given S-parameter (e.g. S_{11}), n is the number of data points, and S_{meas} and S_{mod} are the measured and modeled S-parameters, respectively. The overall error criteria for is given by:

$$E = \sum_{j=1}^2 \sum_{i=1}^2 w_{ij} E_{ij} \quad (4.2)$$

where w_{ij} are weighting factors and E_{ij} is the error value of S_{ij} S-parameter.

TopFinder requires a set of S-parameter measurements as inputs and produces the topology that best fits this set as its output.

4.2.1 The optimal topology construction procedure

The prime goal of TopFinder is to be able to construct an optimal RF/Microwave transistor small signal topology with minimal (or hardly any) user expertise. The only reliable information in hand is the S-parameter data obtained from simulations or measurements.

The small signal model topology construction process starts by assuming a kernel topology. By a kernel topology we mean a “bare-bone” small signal model for microwave transistors. An important characteristic of the kernel topology is that it should be simple and easy to evaluate its parameters using the available measurement data. Although several variations of the kernel topology might be constructed, a given kernel topology should

include some essential elements that are characteristic of a specific transistor type. For example, a kernel topology for a MESFET should include elements such as the gate-to-source capacitance, C_{gs} , the gate-to-drain capacitance, C_{gd} , the trans-conductance g_m , and some others. For simplicity and without loss of generality, the kernel topology in this work is chosen to be the standard topology.

To obtain initial values of the kernel topology elements, an initial parameter extraction process is performed. Topology element values are obtained by curve fitting the S-parameter measurements. A smaller portion of the frequency range of the S-parameter might be used to get quick values of the kernel topology. Parameter extraction of the final topology uses S-parameter measurements over the whole frequency range. The tool for parameter extraction is developed as part of the TopFinder CAD tool.

The evolution of the kernel topology into a full optimal topology is obtained incrementally. Initially, a structure that contains all potential circuit elements that might exist in the topology is initialized. The optimality metric is calculated and sensitivity of this metric to all the topology elements is computed. Elements are then sorted in an descending order according to their sensitivity value. Element sensitivity is calculated by changing the element value by 5% and then computing the difference between the old and the new values of the sensitivity metric. Top two or three elements depending on the sensitivity of S-parameters to those elements are considered in the new topology. After every step of adding an element, the optimality metric, as given by (4.1), is computed and stored with its corresponding configuration. The topology with the best metric value is designated as the optimal topology.

The tool is written in C programming language and runs on both Unix and MS-Windows operating systems. The overall run time for obtaining the optimal topology varies from a device to another but the average time is about 5 minutes. The tool outputs the optimal topology in a form of a text file with element names and values. This file can be used as an input to a graphical user interface output. A high-level flow chart of the algorithm used to develop the tool is shown in Figure 4.1 below.

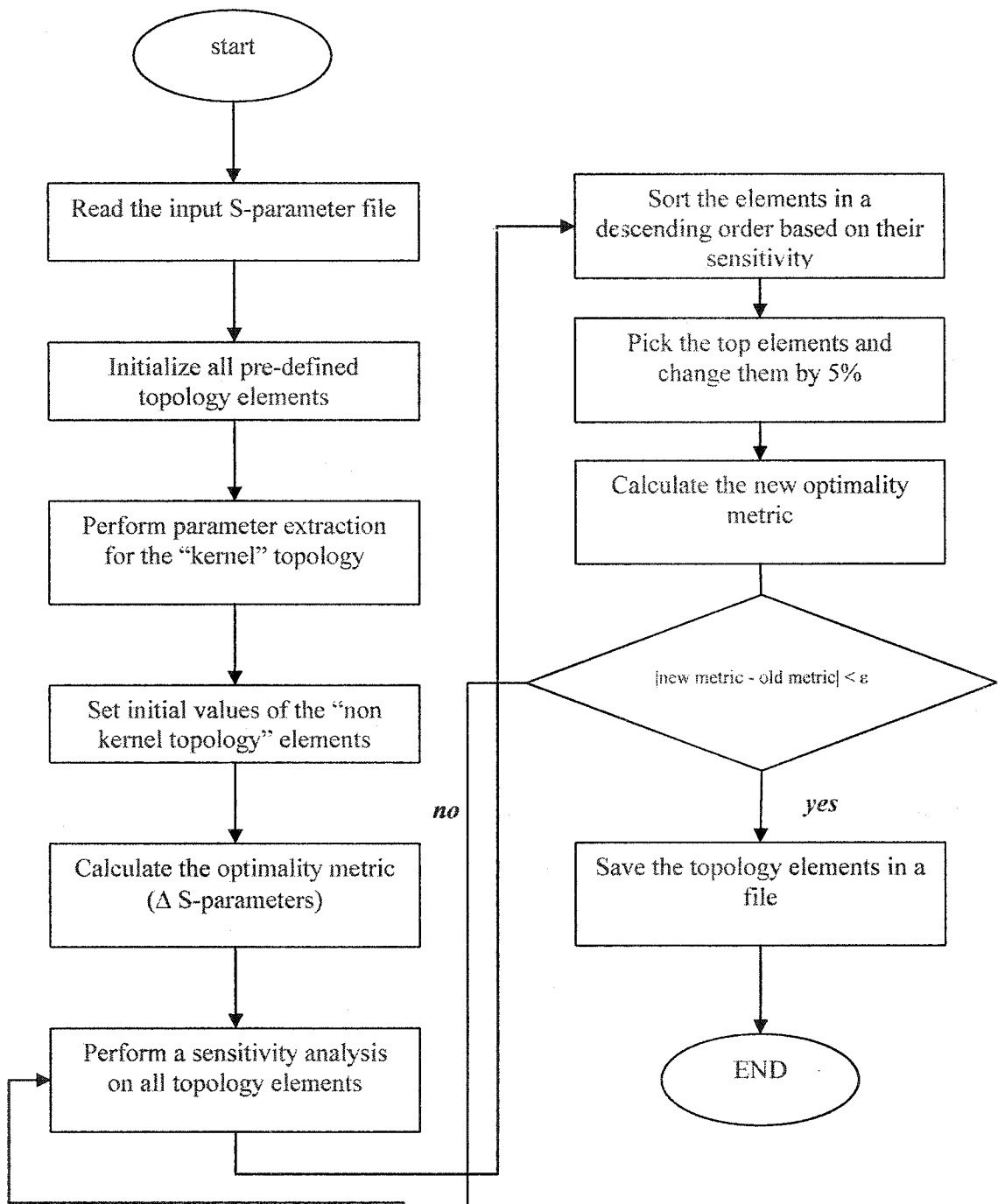


Figure 4.1 A high-level flowchart of TopFinder CAD tool

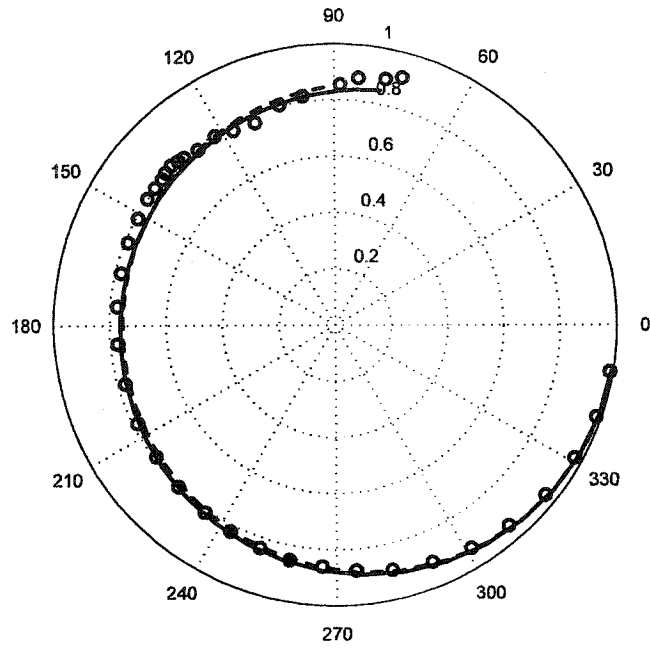
4.2.2 Demonstration of the CAD tool (TopFinder)

In this section, TopFinder is demonstrated on two examples. The first is demonstrated on a GaAs MESFET till a frequency of 40 GHz. In this example it is shown that TopFinder generates an optimal circuit-based FET model that fits better the measured S-parameters than the standard topology [55][56]. In the second example, however, the tool is demonstrated on a HEMT device till a frequency of 40 GHz. Although the tool was initially designed for FET devices, it is shown in this example that the tool can also be used for HEMTs due to the similarities of the circuit-based models between the FETs and HEMTs.

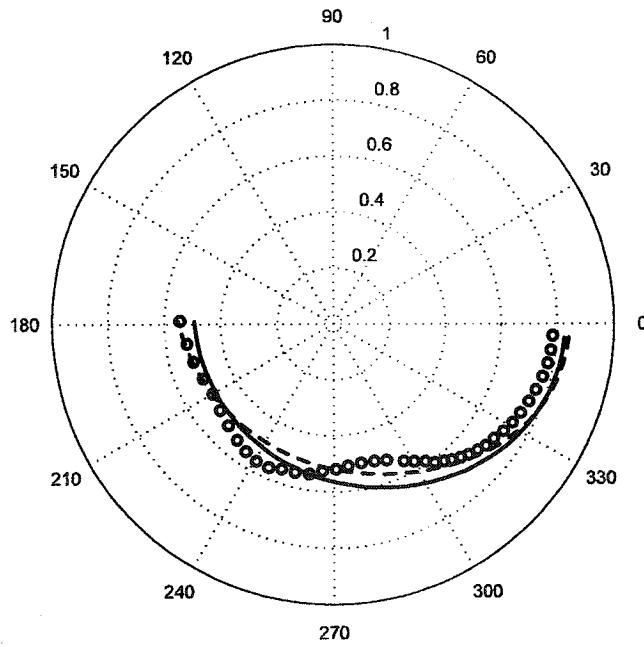
(a) Example 1: The EFA018A GaAs MESFET

This example is an application of TopFinder for high performance devices. The test device is the EFA018A GaAs power MESFET from Excilics Semiconductors [20]. S-parameter for this device up to a frequency of 40 GHz at a bias of $V_{ds} = 6$ V and $I_{ds} = 0.5 I_{dss}$ ($I_{dss} = 50$ mA) are obtained from the device manufacturer. The optimal topology is generated in less than 5 minutes on a typical Solaris workstation. The optimal topology is shown in Figure 4.4.

The input and output reflection coefficients (S_{11} and S_{22}) are shown in Figure 4.2. The forward and reverse S-parameters (S_{21} and S_{12}) are shown in Figure 4.3. Both figures show S-parameters for the optimal topology (produced by the tool), the standard topology, and the measurement data. They also show that the optimal topology fits the measurement data better than the standard topology. Table 4.1 summarizes the extracted element values of the optimal and the standard topologies for this example.

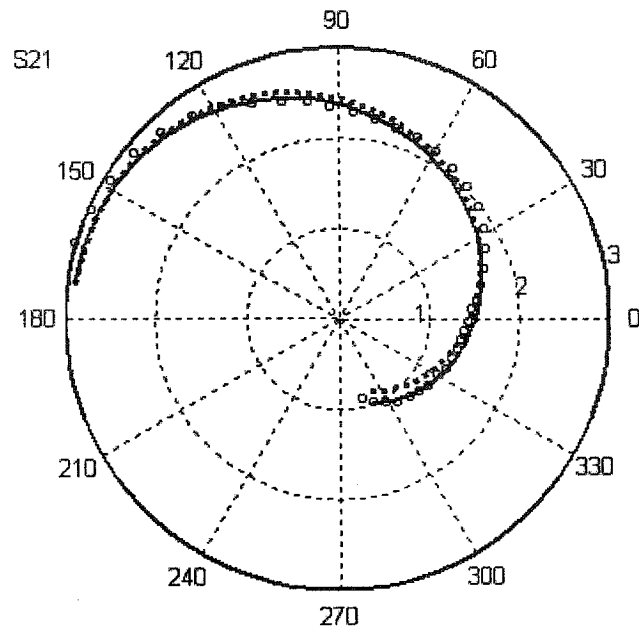


(a)

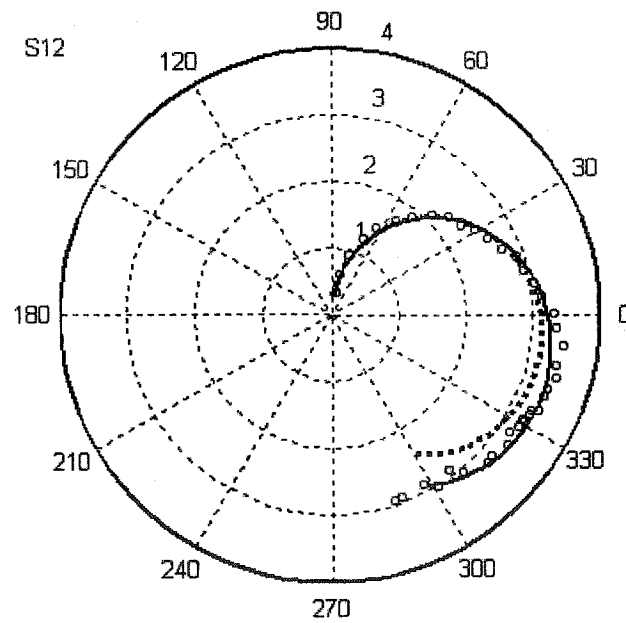


(b)

Figure 4.2 (a) S_{11} (b) S_{22} for measured ($\circ$), standard topology (...), and tool produced optimal topology (—)



(a)



(b)

Figure 4.3

(a) S_{21} (b) S_{12} (scale 0.033/Div) for measured ($\circ$), standard topology (...), and tool produced optimal topology (—)

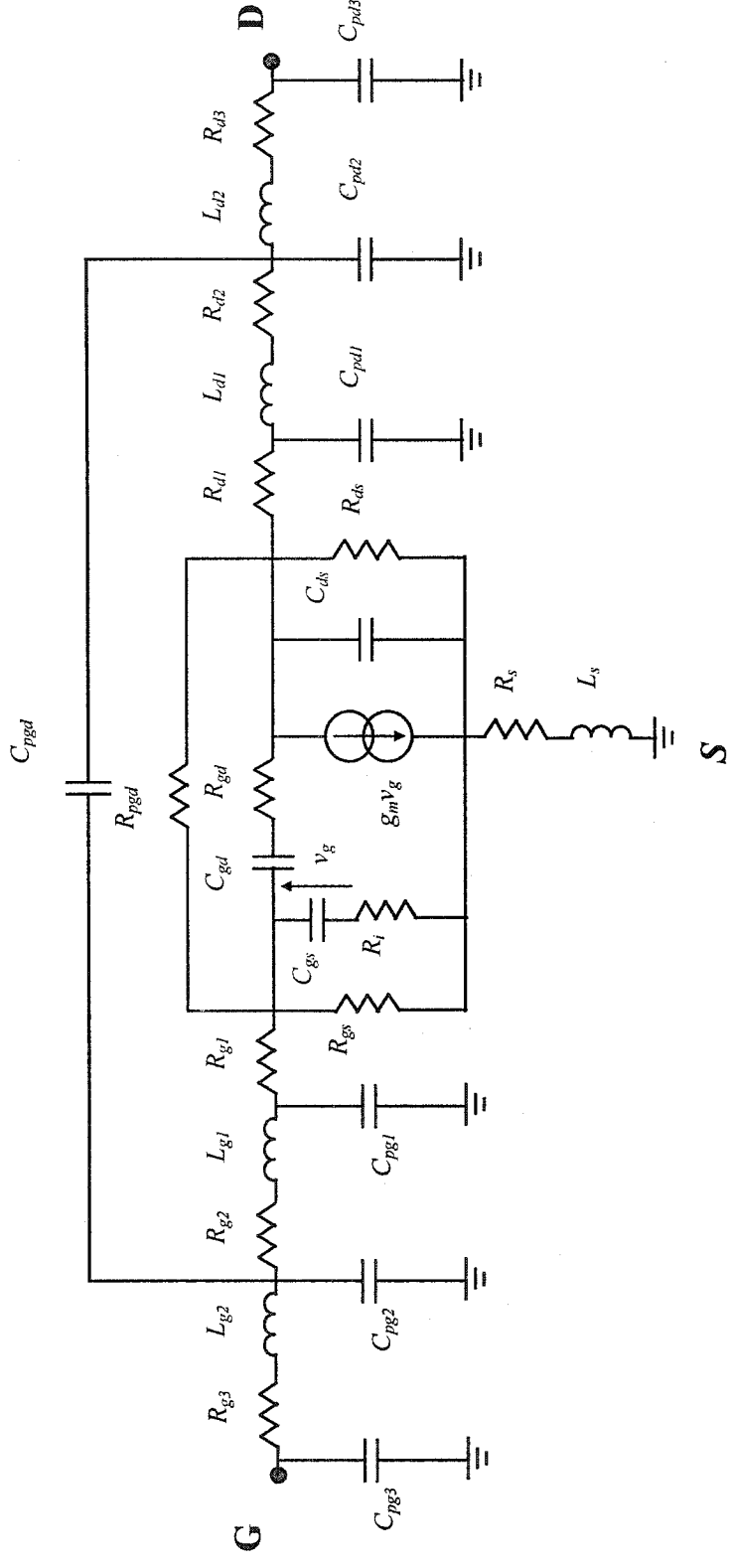


Figure 4.4 Optimal topology for the EFA018A GaAs MESFET

Table 4.1 Element values for the Optimal and Standard topologies for the EFA018A

Equivalent circuit element	Optimal Topology	Standard Topology
$C_{gs} (fF)$	166.88	170.00
$g_m (mS)$	32.00	30.50
$g_{ds} (mS)$	1.65	1.70
$C_{ds} (fF)$	6.00	6.00
$C_{gd} (fF)$	16.00	16.00
$L_g (nH)$	0.14	0.23
$L_d (nH)$	0.19	0.22
$L_s (nH)$	0.06	0.06
$R_i (Ohms)$	0.47	0.53
$R_s (mOhms)$	320.00	230.00
$\tau (pS)$	2.36	2.40
$R_{d1} (Ohms)$	2.20	1.00
$R_{g1} (mOhms)$	680.00	500.00
$C_{pd1} (fF)$	43.00	50.00
$C_{pg1} (fF)$	39.66	50.00
$C_{pg2} (fF)$	2.00	0.00
$C_{pd2} (fF)$	8.00	0.00
$R_{g2} (Ohms)$	0.165	0.00
$R_{g3} (Ohms)$	0.245	0.00
$L_{pg} (nH)$	0.062	0.00
$L_{pd} (nH)$	0.059	0.00
$C_{pg3} (fF)$	12.99	0.00
$C_{pd3} (fF)$	6.13	0.00
$R_{d2} (mOhms)$	0.0215	0.00
$R_{d3} (mOhms)$	39.00	0.00
$C_{pgd} (fF)$	0.98	0.00
$R_{gdp} (MOhms)$	1.35	Infinity
$R_{gs} (MOhms)$	2.92	Infinity
$R_{gd} (Ohms)$	1.12	0.00

(b) Example 2: The EPB018A5 low noise high-gain Heterojunction FET (HEMT)

In the previous example the author showed the effectiveness of the tool for developing optimal topologies for the GaAs MESFETs. Although this tool was developed specifically for the GaAs MESFETs, it can be easily applied to other transistors since the process of developing the optimal topology is generic to a great extent. This is especially true for transistors with large degree of similarity to the MESFET. An example of transistors similar to the MESFET is the heterojunction FET, or the HEMT.

In this example, the TopFinder tool is applied to the EPB018A5 low noise, high gain HEMT from Excelics Semiconductors. The device is $0.3 \times 180 \mu\text{m}$ with an f_{max} of 120 GHz. S-parameter measurements of the device are up to a frequency of 40 GHz at a bias of $V_{ds} = 2.0$ V and $I_{ds} = 15.0$ mA.

The standard topology of MESFETs and HEMTs are similar and no modifications/tuning are needed for the TopFinder CAD tool. The TopFinder is applied on the two-port S-parameter file of the HEMT and the optimal topology is generated in less than 5 minutes. The tool is run on a typical Solaris workstation. The resulting optimal topology is shown in Figure 4.5.

The input and output reflection coefficients (S_{11} and S_{22}) are shown in Figure 4.6. The forward and reverse S-parameters (S_{21} and S_{12}) are shown in Figure 4.7. Both figures show S-parameters for the optimal topology (produced by the tool), the standard topology, and the measurement data. They also show that the optimal topology fits the measurement data better than the standard topology. Table 4.2 summarizes the extracted element values of the optimal and the standard topologies for this example.

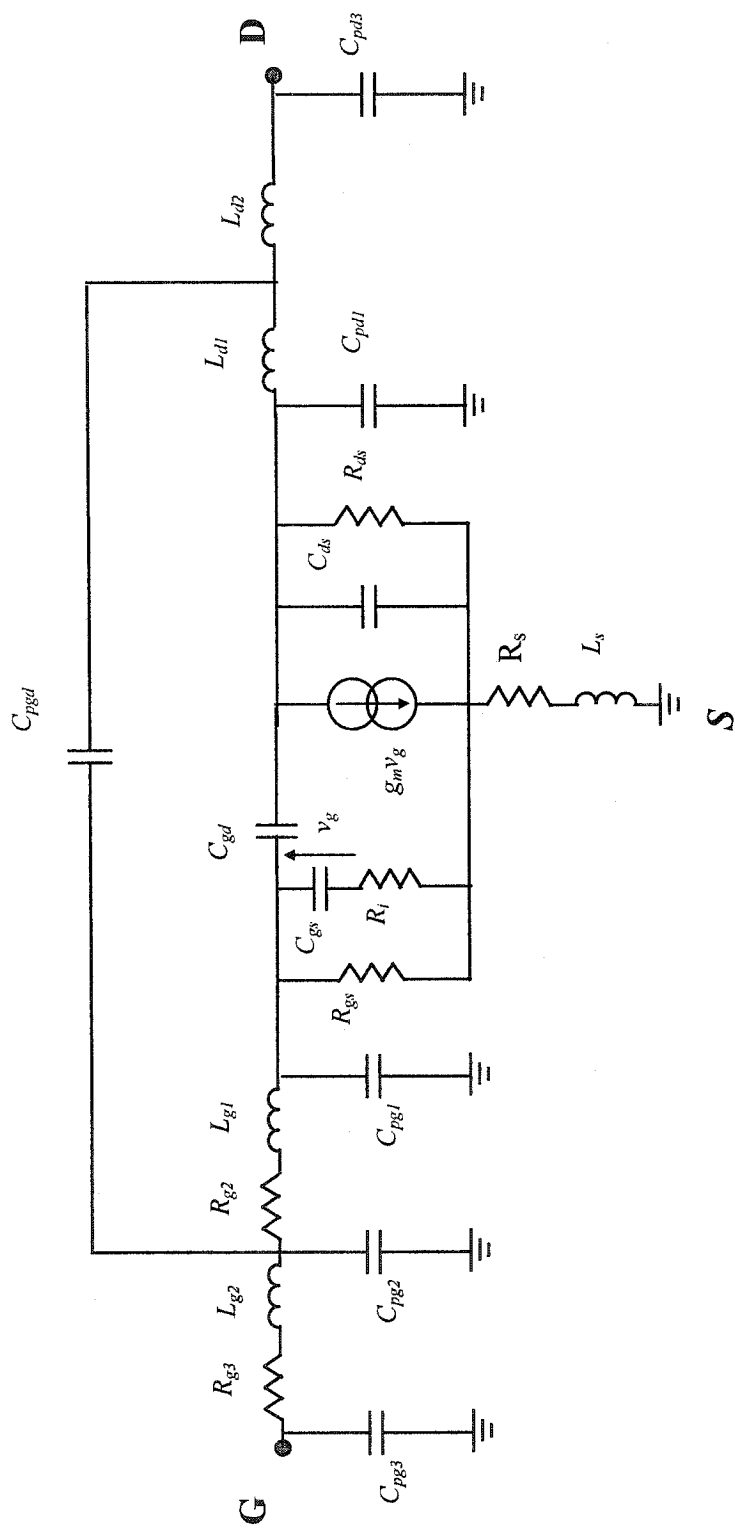
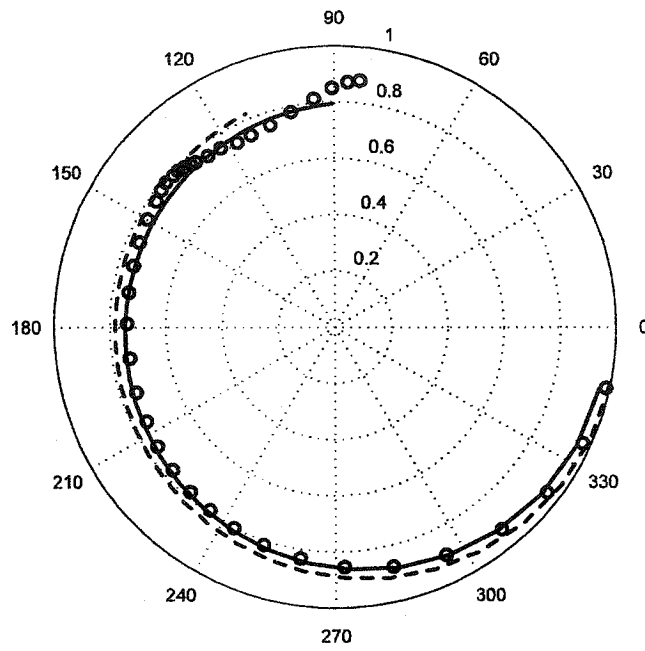
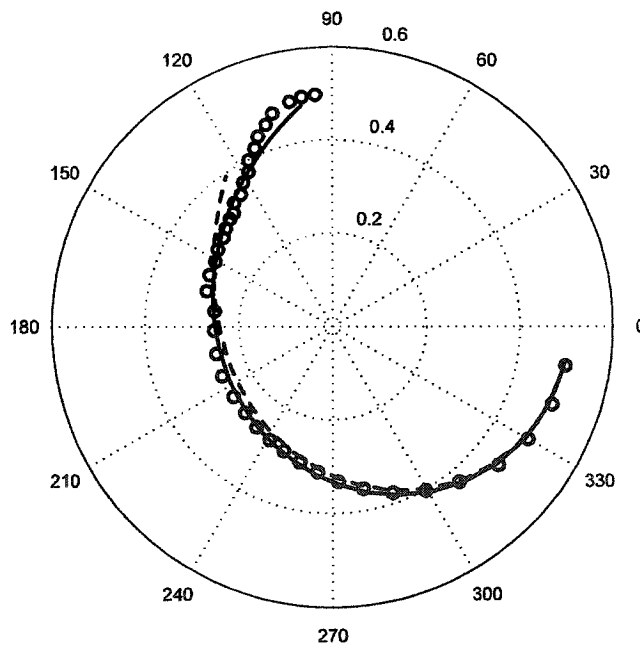


Figure 4.5 Optimal topology for the EPB0185A heterojunction FET (HEMT)



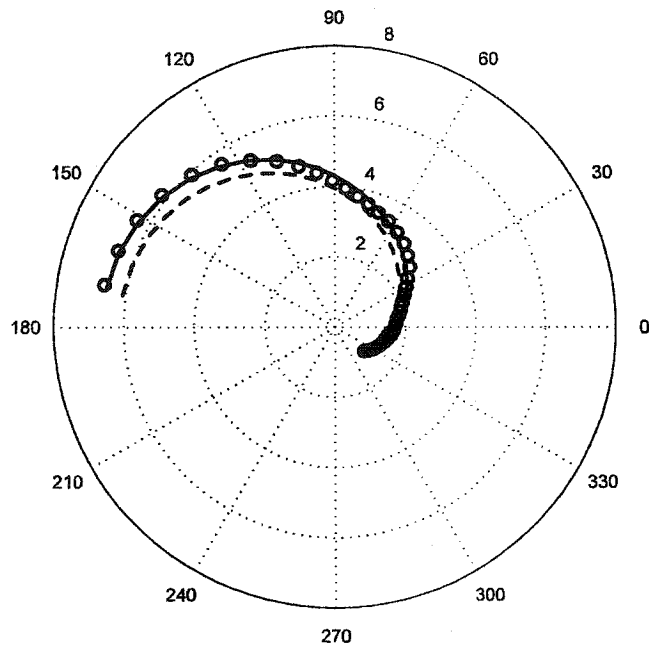
(a)



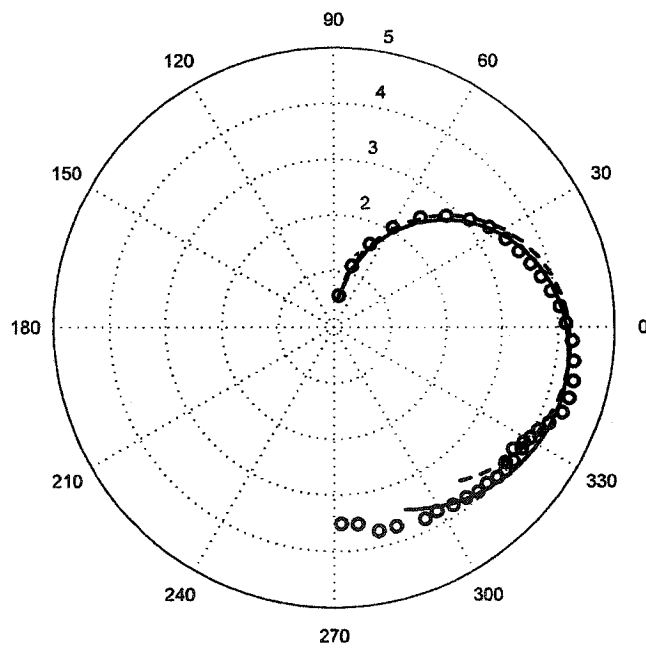
(b)

Figure 4.6

(a) S_{11} (b) S_{22} for measured ($\circ$), standard topology (...), and tool produced optimal topology (—) for the EPB018A5 HEMT



(a)



(b)

Figure 4.7

(a) S_{21} (b) S_{12} (scale 0.033/Div) for measured ($\circ$), standard topology (...), and tool produced optimal topology (—) for the EPB018A5 HEMT

Table 4.2 Element values for the optimal and standard topologies for the EPB018A5 HEMT

Equivalent circuit element	Optimal Topology	Standard Topology
C_{gs} (fF)	152.40	150.00
g_m (mS)	94.00	85.00
g_{ds} (mS)	6.9	3.70
C_{ds} (fF)	22.1	15.00
C_{gd} (fF)	34.3	40.00
L_g (nH)	0.17	0.22
L_d (nH)	0.17	0.19
L_s (nH)	0.02	0.018
R_i (Ohms)	1.52	1.6
R_s (Ohms)	0.50	0.61
τ (pS)	1.0	2.0
R_{d1} (Ohms)	0.0	1.60
R_{g1} (Ohms)	0.0	1.90
C_{pd1} (fF)	36.56	41.00
C_{pg1} (fF)	42.30	80.00
C_{pg2} (fF)	9.3	0.00
C_{pd2} (fF)	0.0	0.00
R_{g2} (Ohms)	0.16	0.00
R_{g3} (Ohms)	0.245	0.00
L_{g2} (nH)	0.02	0.00
L_{d2} (nH)	0.04	0.00
C_{pg3} (fF)	3.8	0.00
C_{pd3} (fF)	5.8	0.00
R_{d2} (Ohms)	0.0	0.00
R_{d3} (Ohms)	0.0	0.00
C_{pgd} (fF)	3.4	0.00
R_{gdp} (MOhms)	Very Large	Infinity
R_{gs} (KOhms)	2.8	Infinity
R_{gd} (Ohms)	0.0	0.00

4.3 Efficient Determination of the optimal large-signal model for the FET

In the previous section, the importance of developing small-signal models both accurately and quickly is highlighted. One contribution of this research is to develop a CAD tool for building the optimal small-signal FET models.

But developing accurate large-signal device models is as important when reliable system design is considered. Furthermore, automating the model generation process serves to improve the design cycle and minimize the required user expertise [17], [79], [41].

A large signal device model is a set of empirical functions with parameter values that can be appropriately assigned to best fit the performance of the nonlinear circuit elements in the device large-signal model. Some of the most commonly used large-signal device models are the Curtice, Statz, and the Materka models. An overview of these models is given in Chapter 3.

An optimal large-signal device model is closely linked to its small-signal counterpart. In essence, optimal large-signal models can be constructed from multiple optimal small-signal models obtained at different DC bias points[38], [30], [22]. This section shows how to automatically determine the optimal large-signal FET model associated with the small signal one. Starting with a set of measured S-parameters at different DC bias points, the optimal large signal model is produced and its parameter values extracted with minimal user expertise. Currently the widely used Materka, Curtice, and Statz large-signal models are fully supported.

4.3.1 Optimal large-signal model

The process of finding the most accurate large-signal model is essentially to find the model that “best-fit” the measured characteristics of the device nonlinear elements. In other words, measured values of nonlinear elements such as the device transconductance g_m , gate-to-drain capacitance C_{gd} , and gate-to-source capacitance C_{gs} , should be available first. Although this can be done through direct measurements, the experimental setup is complex and the values might not be accurate. Another alternative is to perform small-signal S-parameter measurements at many DC bias points (V_{ds} , V_{gs}). For each bias point, small signal

parameter extraction is performed. This process provides element values at a given bias point. Repeating this process gives the dependence of element values on bias.

Generally, it is sufficient to optimize the large-signal model fitting for the DC I-V characteristics. It is the view of this research that this approach, namely to “best fit” only DC I-V device characteristics, is not sufficient. Rather, the optimal large-signal model is found by fitting both the I-V characteristics as well as their derivatives. The derivatives of the DC I-V characteristics give the device small-signal transconductance and output conductance as follows:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \quad (4.3)$$

and

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \quad (4.4)$$

In this work we focus on the transconductance since it is the most important nonlinear element in the FET model.

To be able to make a comparison between large-signal models, an “optimality” metric is introduced. This metric combines the evaluation of fitting both the I-V curves as well as the current derivative. Addition of the two terms is selected as a common form of multi-objective optimization cost function. This metric is given as follows:

$$O_m = \sum_{\text{all DC points}} w_1 \cdot \frac{\{I_{ds}(\text{mod}) - I_{ds}(\text{meas})\}^2}{\{I_{ds}(\text{meas})\}^2} + \sum_{\text{all DC points}} w_2 \cdot \frac{\{g_m(\text{mod}) - g_m(\text{meas})\}^2}{\{g_m(\text{meas})\}^2} \quad (4.5)$$

where O_m is the optimality metric, I_{ds} is the drain current, $X(\text{mod})$ is the model value of a given parameter and $X(\text{meas})$ is the measured value of the parameter (X stands for either I_{ds} or g_m). The summation is taken over all the DC measurement points. The factors w_1 and w_2 are for weighting purposes and to normalize the relative magnitudes of the individual metric expressions.

The computation of this metric involves two terms. The first is to compute least-square fitting error of the DC I-V characteristics of the device under consideration. This is an optimization problem where an empirical large-signal model (e.g. Curtice, Statz, or Materka) are tested for best fit of the measurement values. Nonlinear optimization methods are usually used to find the coefficients for those models. In this work a C implementation of the Levenberg-Marquardt method is used [96]. This implementation is modified such that a “good” starting point of models elements is calculated and is fed to the optimization program. Figure 4.8 shows the fitting results of the three models for the NE71000 GaAs MESFET.

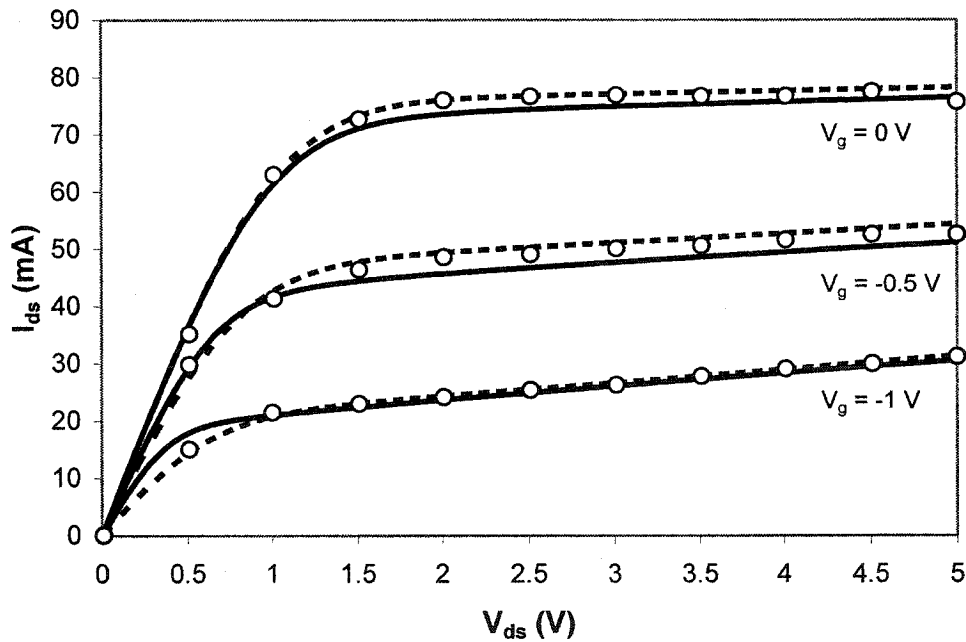


Figure 4.8 I-V curves for the MESFET with large signal fitting models: measurements ($\bullet$), Curtice cubic (...), Materka model (—)

From the figure above it is shown that the Curtice cubic model provides better fitting for the experimental DC I-V characteristics than the Materka model. This conclusion will be reexamined below and after the optimality metric is computed.

To compute the second term, the optimal topology is first generated by fitting a set of S-parameter measurement data to the small-signal model. S-parameter values used here are taken in the typical operating device DC bias points ($V_{ds} = 3$ V and $V_{gs} = -0.5$ V). Multiple S-parameter measurements at various bias points are then obtained. Bias values are 0 ~ 4 V with a step of 0.5 for V_{ds} , and 0 ~ -1.8 V with a step of 0.2 V for V_{gs} . The dependence of the transconductance g_m on the DC bias is then calculated. In this step a parameter extraction program developed in this work is used. Figure 4.9 shows the measured, standard and optimal topology of the transconductance of the NE71000 MESFET.

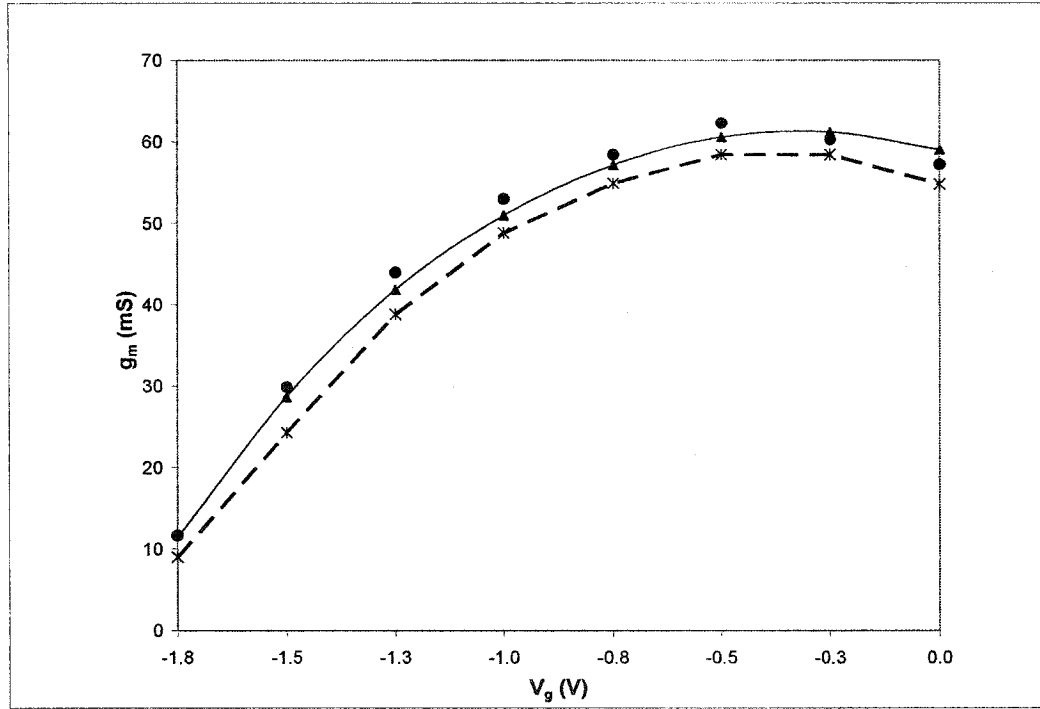


Figure 4.9 Transconductance variation with V_{gs} at $V_{ds} = 3$ V: RF measurement data ($\bullet$), standard topology ($\blacktriangle$), optimal topology (x).

The transconductance metric is then computed using Equation 4.2 and the overall optimality metric is obtained.

Based on the optimality metric suggested in Equation 4.5 the result for the optimal topology showed that the Materka model achieves a combined fitting metric of 0.236 while

that of Curtice model achieved about 0.57. This means that the Materka model achieved about 50% reduction in the optimality metric over the Curtice model (the smaller the metric the better the fit).

4.4 Conclusions

In this Chapter, a CAD tool is demonstrated, that enables designers to obtain a circuit-based topology for RF/Microwave transistors that best fits a set of measured S-parameter values. Compared to existing techniques, the proposed tool is fully automated and requires minimal expertise from the external user. This is especially important when characterizing new devices. The tool starts with a kernel topology that evolves into a full optimal topology. The results showed that the final and optimal topology fits the measured S-parameter data better than the standard topology.

The tool bears an amount of generality enough to apply to different types of transistors. As shown in this Chapter, the tool is useful for MESFETs as well as HEMTs. In addition, the tool can be easily expanded to include BJTs as well as other transistors. Moreover, the topology presented in this paper is for small signal operation with element values independent of the applied voltages. In reality, several elements, particularly C_{gs} and g_m , are function of the external voltage, V_{gs} and V_{ds} . Building a topology with nonlinear elements requires several sets of measurements of S-parameters under various bias conditions.

In addition, TopFinder is expanded to automatically determine the optimal large-signal model based on DC I-V measurements as well as a set of small-signal S-parameter measurements taken at different bias points. Optimal topology is generated first, using TopFinder. By fitting the DC I-V curves and keeping their partial derivative with respect to the bias V_{gs} (i.e. g_m) consistent with the values extracted from the S-parameter measurements, a best-fitting DC I-V large-signal model is obtained.

It is to be noted here that there are currently a significant number of publications on the neural network models of the single-gate FET (as referred to in Chapter 3). No further neural models for the single gate FET need to be introduced in this research.

Chapter 5

NEURAL NETWORK MODELING OF THE DRAIN CURRENT OF THE DUAL-GATE MESFET

5.1 Small-signal circuit based models for the dual-gate FET

Generally, the small signal DG MESFET model can be obtained by combining the models of two single-gate FETs in a cascode connection. Due to the complexity of the single-gate FET circuit model (some topologies can have more than 20 elements), the resulting DGFET circuit model will be far more complex. In addition, the amount of work to develop an optimal DGFET topology is significant and is not paralleled with an equivalent interest from the design community. On the other hand, neural network approaches have not been applied to the modeling of the DGFET. With a device as complex as the DGFET, neural networks offers an excellent modeling alternative. Neural network approaches for modeling the dual-gate MESFET are therefore adopted in this research. The details of the research contributions in this area are presented in the following sections.

5.2 Large signal neural network models for the Dual-Gate MESFET

The dual-gate MESFET has some significant advantages over the single gate of comparable size. These advantages include higher gain, better input gate-to-drain isolation, and higher output impedance. That made it attractive for various *nonlinear* circuit

applications such as mixers, frequency multipliers, and power combiners. There is a need, therefore, for further research towards the development of efficient nonlinear models for such transistors.

Most existing MESFET nonlinear modeling techniques use DC I-V measurements to represent nonlinear drain current and to obtain large-signal device model parameters such as the transconductance and the output conductance. However, the values obtained from DC measurements are not with a good agreement with their counterparts obtained from RF S-parameter measurements. This is mainly due to low frequency dispersion, self-heating, and trap effects [41].

Various MESFET researches [6], [15], [47], have shown that pulsed I-V characterization renders better device parameters than the ones produced by DC I-V ones. Paggi *et al.* [71], for example, showed that the value of the output resistance, R_{ds} , ($R_{ds} = 1/g_{ds}$) extracted directly from pulsed I-V curves is closer to the actual microwave values than the value taken from DC I-V curves. Pulsed measurements are, therefore, preferred if more accurate RF device characterization is desired.

Several works on large-signal DGFET models currently exist. Except for Ibrahim [68] and Jenner's models [63], other models dealt with the DGFET as two single gate FETs connected in cascode. This approximation did not result in a very good agreement between the simulation and the measurement data.

In Jenner's model [63] the nonlinear drain current is represented by a three-dimensional power series approximation. However, obtaining good accuracy can require as many as 165 parameters. Moreover, the model is generated from DC measurements and does not take into account the frequency dispersion of the transconductance and the output conductance. On the other hand, although the model developed by Ibrahim *et al.* required only 49 parameters, it still presents a significant amount of model extraction procedures. In addition, the RF current component in the model required the extraction of the transconductance from three-port S-parameter measurements. This presents a fairly complex and costly process.

Neural modeling of devices and circuits is one of the most recent trends in microwave CAD. Fast, accurate and reliable neural network models can be trained from measured or simulated data. Once developed, these neural models can be used in place of CPU-intensive

physics/EM models of active/passive devices to speed up microwave design. Neural network techniques have been used to model a wide variety of microwave devices and circuits [1][81] with significant successes.

In this chapter, large-signal modeling of the dual-gate MESFET using neural network approach is presented for the first time.

In the first section, an RF large-signal drain current model is presented. This is achieved by utilizing the data from pulsed I-V measurements rather than the usual DC I-V measurements. This is demonstrated on the NE25118 dual-gate MESFET chip manufactured by NEC.

In the second section, a combined DC and RF neural network large-signal drain current model is presented. The RF current is modeled at various DC bias points. This is demonstrated also on the NE25118 dual-gate MESFET chip manufactured by NEC.

In the third section of this chapter a temperature dependent neural network drain current model is presented. This is demonstrated on an on-wafer dual-gate MESFET manufactured by Nortel Networks.

5.2.1 A large-signal neural model for the dual-gate FET with pulsed I-V measurements (isothermal)

(a) The large-signal circuit model

The large signal model for the dual gate FET accounts for the nonlinearity in the input-output characteristics for large signal input values. A new dual-gate large-signal model is developed in [67]. A schematic of this model is shown in Figure 5.1 and is adopted in this work. In this model, drain current, I_{ds} , as well as the stored charges, Q_{g1} , Q_{g2} , and Q_d represent the nonlinear dual-gate FET elements. The author considers mainly the modeling of the drain current since it is the prime source of nonlinear device behavior.

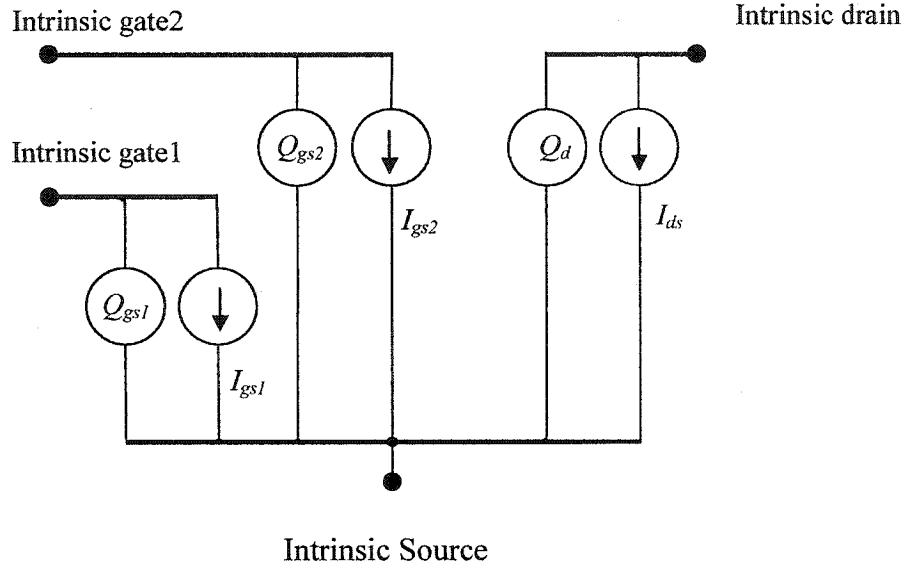


Figure 5.1 The intrinsic large-signal dual-gate FET model

(b) The dual-gate neural network model

As mentioned in Section 3.2.2, an artificial neural network is a collection of neurons that are interconnected in a certain way to form an input-output relationship. The multilayer perceptron (MLP) is the most popular neural-network structure in which the neurons are grouped into layers. The first and the last layers are called input and output layers, respectively and the remaining layers are called hidden layers. For example an MLP3 is a neural network of one input layer, one output layer, and one hidden layer. Figure 3.4 shows a typical MLP3 neural network. In this Figure, each circle represents a neuron, and an array of horizontally adjacent neurons represents a layer. The input layer is the first layer and the last layer is the output layer (bottom up).

In this section we show the effectiveness of neural network approach in modeling the nonlinear behavior of the dual-gate MESFET. We have modeled the NE25118, $1 \times 1.5 \times 400$ μm dual-gate MESFET manufactured by NEC [77]. This chip is commercially available as a discrete component in the form of a small outline transistor (SOT) package. An appropriate

test fixture to measure the chip pulsed I-V characteristics is designed for that purpose. Figure 5.2 shows the NE25118 dual-gate MESFET and the test fixture used in the measurements.

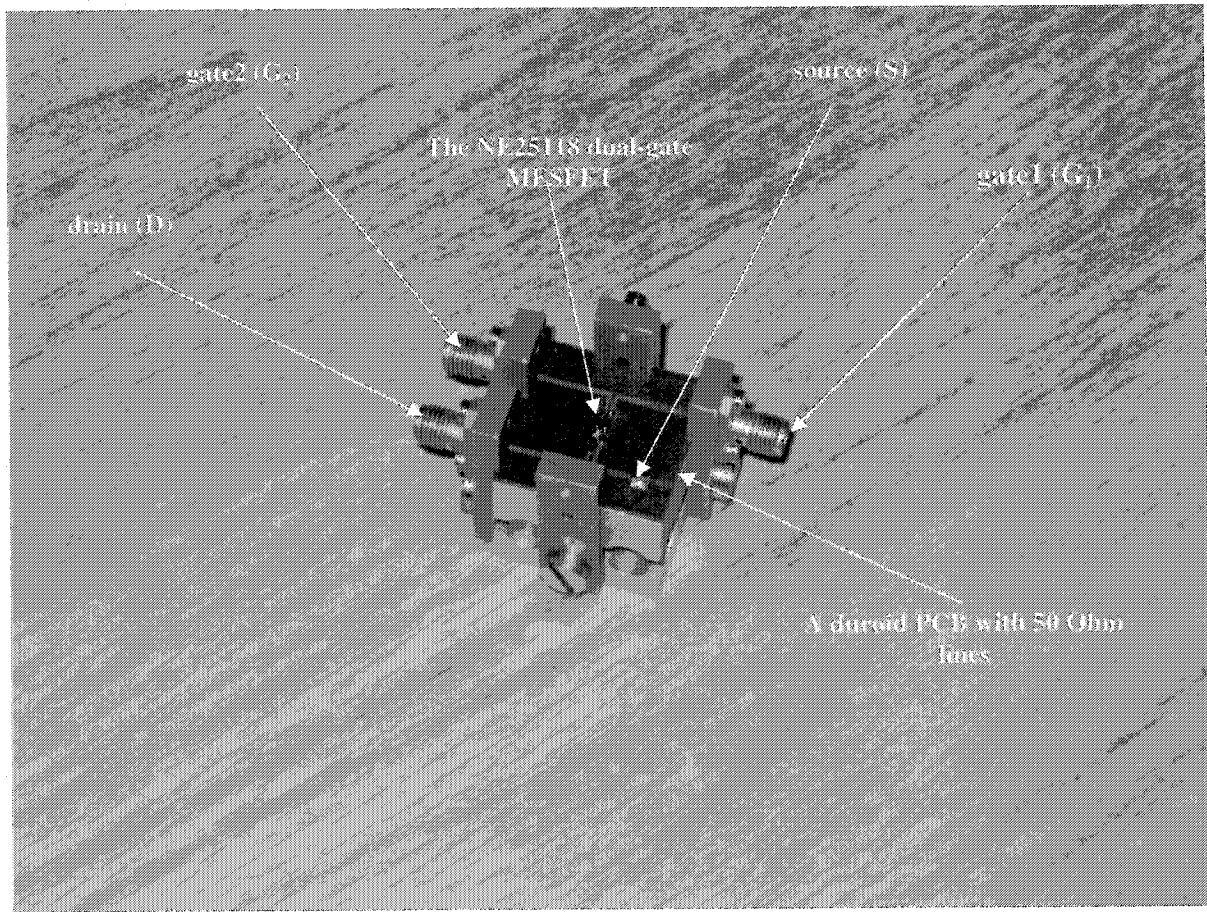


Figure 5.2 The test fixture for pulsed I-V measurements for the NE25118 dual-gate MESFET

Pulsed measurements are performed by a programmable DC/pulse measurement setup. A schematic of this setup is depicted in Figure 5.3. The drain and the gates are pulsed simultaneously. Gate voltage levels are varied from -1.0 to 0.5 V (step of 0.3 V), while the drain voltage levels are varied from 0.0 to 10.0 V (step of 0.5 V). The drain current is averaged over many reading points under the same measuring conditions. This process is software driven from a user interface. The selection of the pulse width is important to achieve reliable measurements. Long pulse widths can cause undesirable channel heating effect while excessively short pulses might not be long enough to turn on the device. For most devices, however, a $1\mu\text{s}$ pulse width is sufficient [34]. For this experiment, a pulse width of $1\mu\text{s}$ with pulse separation of 1ms (a duty cycle of 0.1 %) is selected. The measurements are performed at a bias point of $(V_{gs1}, V_{gs2}, V_{ds}) = (-1.0\text{ V}, -1.0\text{ V}, 0.0\text{ V})$.

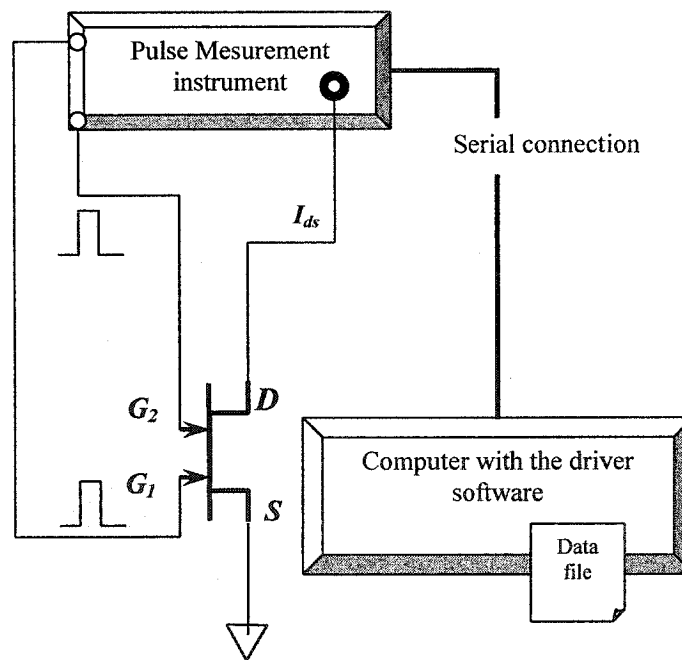


Figure 5.3 The DGFET pulse measurement setup schematic

The measurement setup is computer driven and is assembled at Nortel Networks and is based on the GaAsCODE pulse measurement instrument. This instrument is connected to a computer through an RS-323 interface. A user interface is available that enables the designer to configure the parameters of the experiment. Configurable parameters are: pulse width, pulse duty cycle, number of times a measurement is averaged over, DC operating point, pulse voltage range and step, maximum device power. After a measurement session is performed, measurement data is stored in a user defined file. This data file is used in the neural network model generation process.

The neural network model generation process starts by assuming an initial model configuration. The “universal approximation theorem” states that a multilayer perceptron network (MLP) can approximate any arbitrary multidimensional function. We started with a three layer neural network. The number of layers and neurons per layer are then changed until an optimal model is reached.

Measurement of data points are performed such that they cover the desired parameter range. The obtained data is divided into two sets, a training and a testing set. The testing data set is independent of the training set (never used in training).

Various neural model configurations have been tested. Three-, four-, and five-layer models with various numbers of neurons in each layer are constructed. The resulting model is trained and tested with the same data set. The five-layer model was found to produce the lowest model error. The dual gate model developed in this work is therefore of five layers; one input layer, one output layer, and three hidden layers. The input layer has three input parameters, the pulsed gates voltages, v_{gs1} and v_{gs2} , and the pulsed drain-source voltage, v_{ds} .

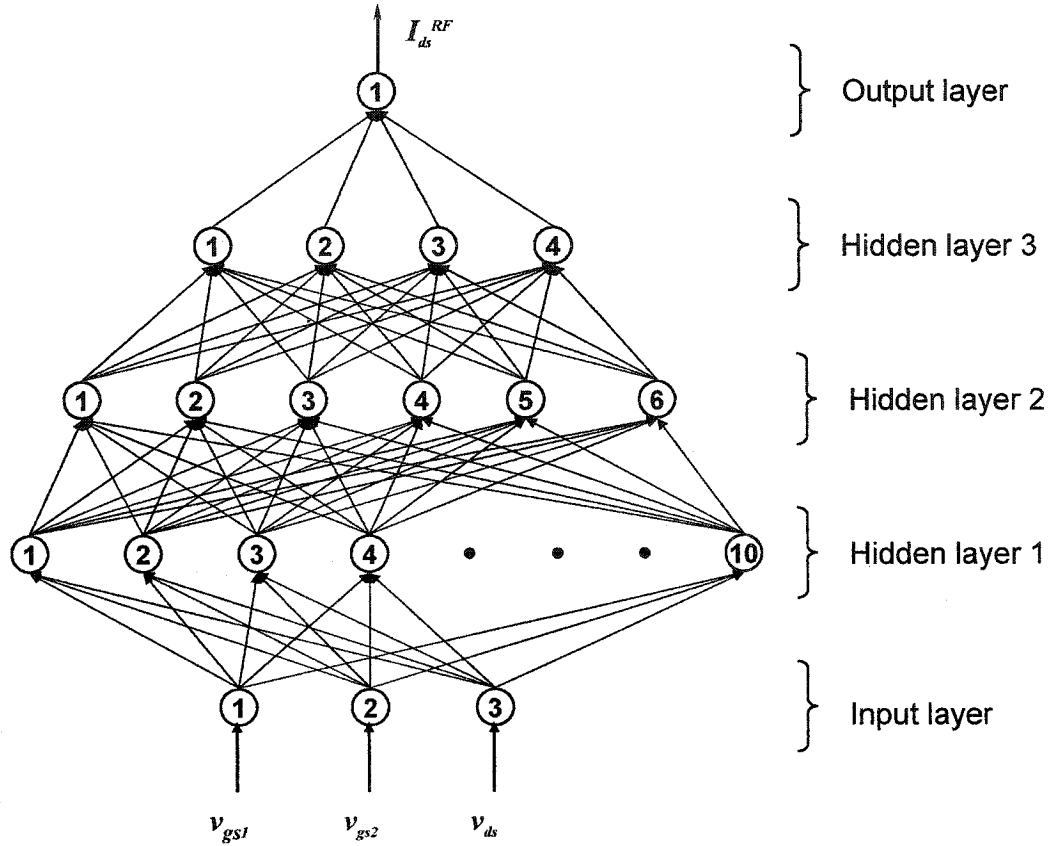


Figure 5.4 The Five-layer Neural Network model of the Dual gate FET drain current

The output layer has one output, the drain current, I_{ds}^{RF} . The number of model neurons for each layer is: 10 for the first, 6 for the second, and 4 for the third hidden layer. The total number of hidden neurons is 20 neurons. A schematic representation of the model is shown in Figure 5.4.

(c) Results

The number of pulsed measurement data points is 1147 in total. This bulk data should be randomized before being used in the neural model generation process. A randomization program is developed for this purpose. The data is then split into training and testing parts. The randomization step is important to ensure the model training and testing data are well spread in the data range of interest. Of the 1147 data points, 800 are used to train the model.

The remaining 347 data points are used in testing. The quasi-Newton method is used to minimize the training error of the neural model.

Figure 5.5 below shows the modeled (solid line) and the measurement data (solid circles) for the pulsed drain current, I_{ds}^{RF} , of the DGFET as a function of the pulsed drain voltage, v_{ds} , for gate voltage of $v_{gs1} = -0.3$ volts with different voltage values of the second gate, v_{gs2} . The Figure shows an excellent agreement between the model and measurement data.

The neural model developed in this work has an average model error of less than 1% with data correlation of 0.99. Statistical analysis on measurement and modeled data showed negligible data scattering. This model is generated using the *NeuroModeler* software [83]. The process of generating this specific neural model lasted a few minutes on a typical computer.

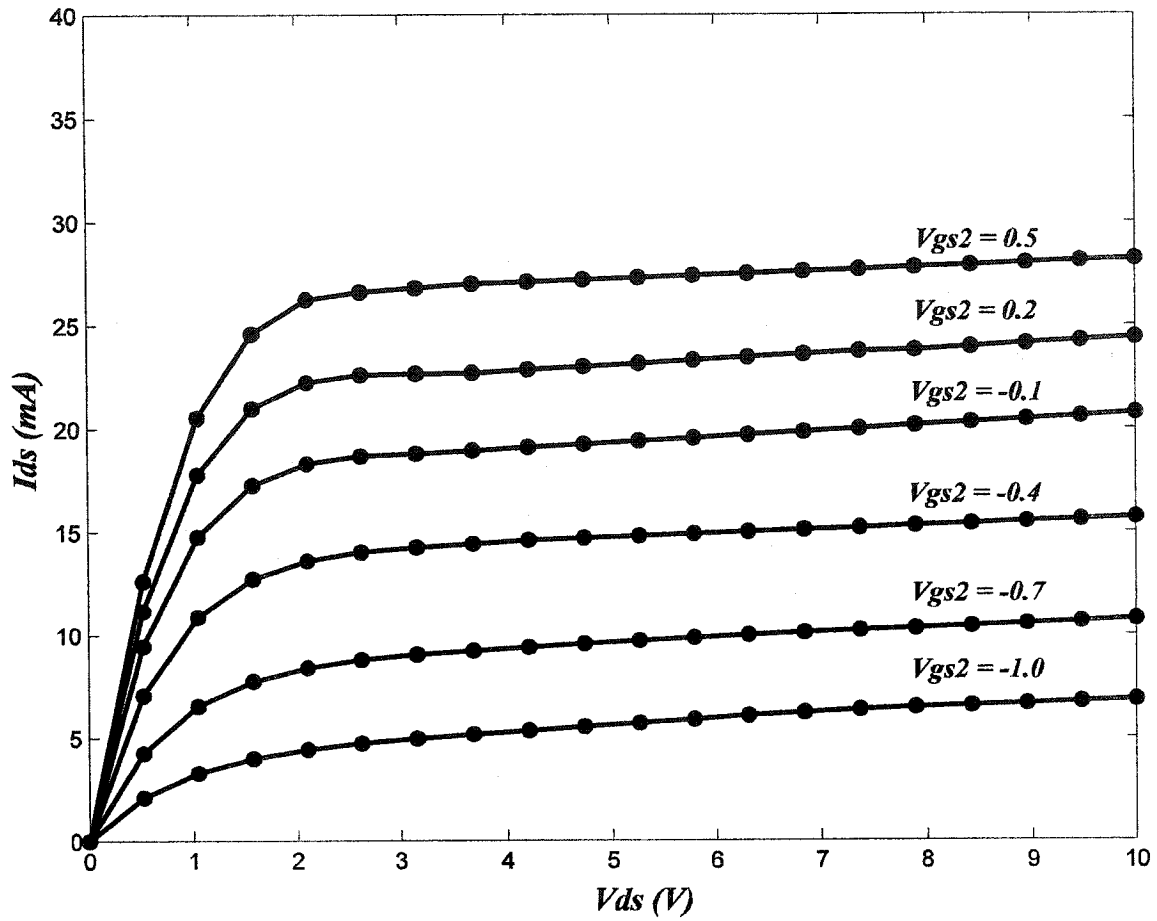


Figure 5.5 Pulsed IV curves (•: measurement, —: modeled) for the NE25118 dual-gate FET ($v_{gs1} = -0.3$ V and $v_{gs2} = -1.0 \sim 0.5$ V)

5.2.2 A Combined DC and RF Neural model for the Dual-Gate MESFET

Section 5.2.1 presented for the first time an RF drain current neural network model for the dual-gate MESFET [59]. The advantage of introducing the neural network approach is that the model can be trained with measurement data and then used directly for other data values not used by the training data set without having to run an intensive computation cycle every time the model is invoked. This presents a potential advantage for the computer aided design tools when obtaining overall circuit performance characteristics or during circuit optimization. Another advantage of the model presented in Section 5.2.1 is that it is based on pulsed I-V data rather than DC ones. This is advantageous when computing the small-signal device parameters such as g_m . Small-signal device parameters obtained from pulsed I-V data

agree better, with RF measurement values, than the ones obtained from DC I-V curves. However, pulsed I-V measurements depend on the DC bias of the device and there exist a complete set of such measurements for every bias point. The validity of this model then is restricted to the bias point at which the pulsed measurements were performed.

In this section, a complete large-signal drain current model for the dual-gate MESFET is presented. This model is represented by a combined neural network of two separate ones. The first represents the DC component of the drain current while the second represents the RF component. The inputs of the model include both the DC bias values as well as the pulsed values. This is advantageous in the sense that the bias dependence of the pulsed I-V characteristics can be accounted for in the model.

(a) Description of the model

The dual-gate MESFET drain current model developed in this work has two components, a DC and an RF. Static current component is modeled using the DC IV characterization. For the RF component, however, dynamic characterization is required. Most published works on the single and dual-gate FET approximate the dynamic behavior of the device with the static IV curves [68], [63], [97]. This results in significant errors in calculating the trans- and output conductances of the device. Pulsed measurements, on the other hand, provide a better representation of the RF large-signal behavior of the transistor [89].

The total dual-gate MESFET drain current is then given by [68]:

$$I_{ds} = I_{ds}^{DC} h(f) + I_{ds}^{RF} (1 - h(f)) \quad (5.1)$$

where I_{ds}^{DC} is the DC component of the drain current, I_{ds}^{RF} is the RF component, and $h(f)$ is a function that ensures a smooth transmission from DC to RF characteristics. For the model developed here, and for simplicity, $h(f)$ is chosen to be the unit-step function, i.e., the model represents either the DC or the RF current model.

$$h(f) = \begin{cases} 1 & f = 0 \\ 0 & f > 0 \end{cases} \quad (5.2)$$

where f is the frequency.

The DC current is a function of the static potential of the two gates and the drain, V_{gs1} , V_{gs2} , and V_{ds} respectively. On the other hand, pulsed I-V characteristics depend on the bias point as well as the pulse amplitudes applied [89]. Therefore, the RF drain current is a function of the bias point (V_{gs1} , V_{gs2} , V_{ds}) as well as the pulsed voltages (v_{gs1} , v_{gs2} , v_{ds}) applied over the bias point. In other words:

$$I_{ds}^{DC} = I_{ds}^{DC}(V_{gs1}, V_{gs2}, V_{ds}) \quad (5.3)$$

$$I_{ds}^{RF} = I_{ds}^{RF}(V_{gs1}, V_{gs2}, V_{ds}, v_{gs1}, v_{gs2}, v_{ds}) \quad (5.4)$$

(b) Results

The NE25118 1x1.5x400 μm GaAs dual-gate MESFET is modeled in this work. The DC and pulsed measurements are performed by a programmable DC/pulse measurement setup. Each measurement set is performed in a separate session. For the DC measurements, the bias range for the two gates is -1.0 ~ 0.25V (in steps of 0.25V) while that of the drain is 0 ~ 8V (steps of 0.25 V). For the pulsed measurements, the DC bias point is scanned from ($V_{gs1} = -1.0\text{V}$, $V_{gs2} = -1.0\text{V}$, $V_{ds} = 0.0\text{ V}$) to ($V_{gs1} = 0.2\text{ V}$, $V_{gs2} = 0.2\text{ V}$, $V_{ds} = 5.0\text{ V}$) in steps of ($\Delta V_{gs1} = 0.3\text{ V}$, $\Delta V_{gs2} = 0.3\text{ V}$, $\Delta V_{ds} = 1.0\text{ V}$). The drain and the gates are pulsed simultaneously. The pulsed gate voltage levels are varied from -1.0 to 0.2V (in steps of 0.3V), while the drain pulsed voltage levels are varied from 0 to 8V (in steps of 0.4V). The drain current was averaged over many reading points under the same measurement conditions. This is all software programmed from a software user interface. The width of pulse is 1 μs with pulse separation of 1 ms (a duty cycle of 0.1 %).

(c) The DC neural model

The DC neural model developed here is a three layer. We found no significant improvement of the model accuracy if more layers are used since the model is relatively simple. Ten hidden neurons were sufficient to obtain a very good accuracy of less than 1%. The input layer has 3 input parameters, the static voltages, (V_{gs1} , V_{gs2} , V_{ds}). The output layer has one output, the DC drain current, I_{ds}^{DC} . Figure 5.6 shows the measured and modeled data at $V_{gs1} = 0.0\text{ V}$ for different gate voltage (V_{gs2}).

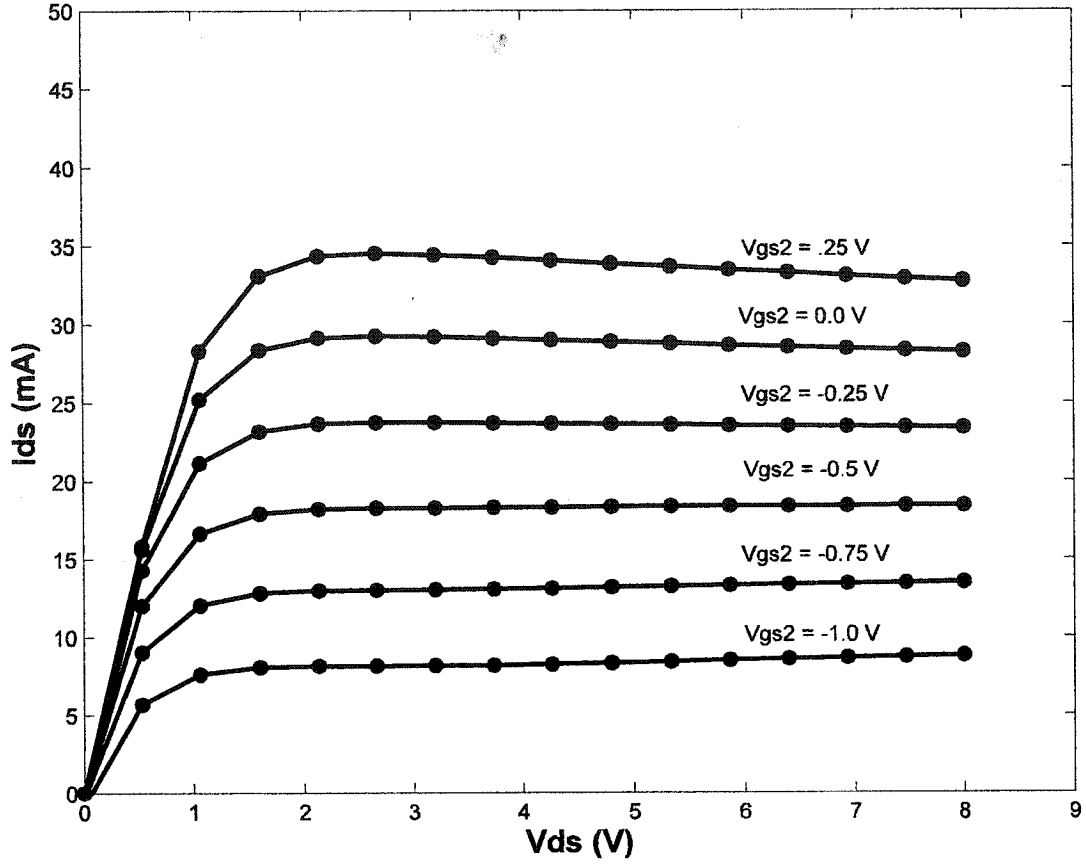


Figure 5.6 DC IV curves ($\bullet$: measurement, $-$: modeled) for the dual-gate FET ($V_{gs1} = 0.0$ V and $V_{gs2} = -1.0 \sim 0.25$ V)

(d) The RF neural model

We have tested three different neural models for the RF current; a three-, a four-, and a five-layer models. We found a significant improvement of the four-layer model over the three-layered one. On the other hand, the model error improvement presented by the five-layer model did not justify the model complexity over the four-layered model. The model presented here is therefore of four layers; one input layer, one output layer, and two hidden layers. The input layer has 6 input parameters, the static voltages, (V_{gs1} , V_{gs2} , V_{ds}), and the dynamic voltages (v_{gs1} , v_{gs2} , v_{ds}). The output layer has one output, the RF drain current, I_{ds}^{RF} . The total number of hidden neurons is 25 (19 and 6 neurons for the first and second layer respectively). Figure 5.7 shows an illustration of the model. Figures 5.8, 5.9, and 5.10, show

the measured and modeled pulsed data for the dual gate FET for various DC and pulsed voltages. The model shows very good fitting of the data. The model error is less than 1%.

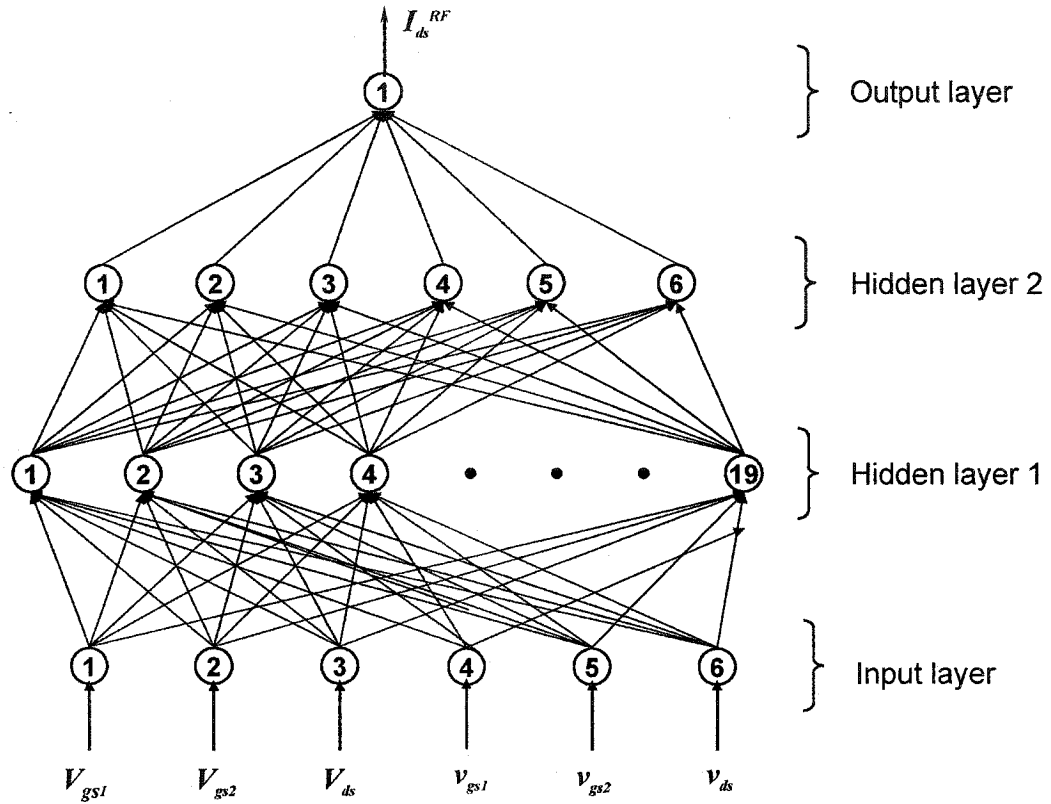


Figure 5.7

A Four-layer Neural Network model of RF current component of the Dual gate FET

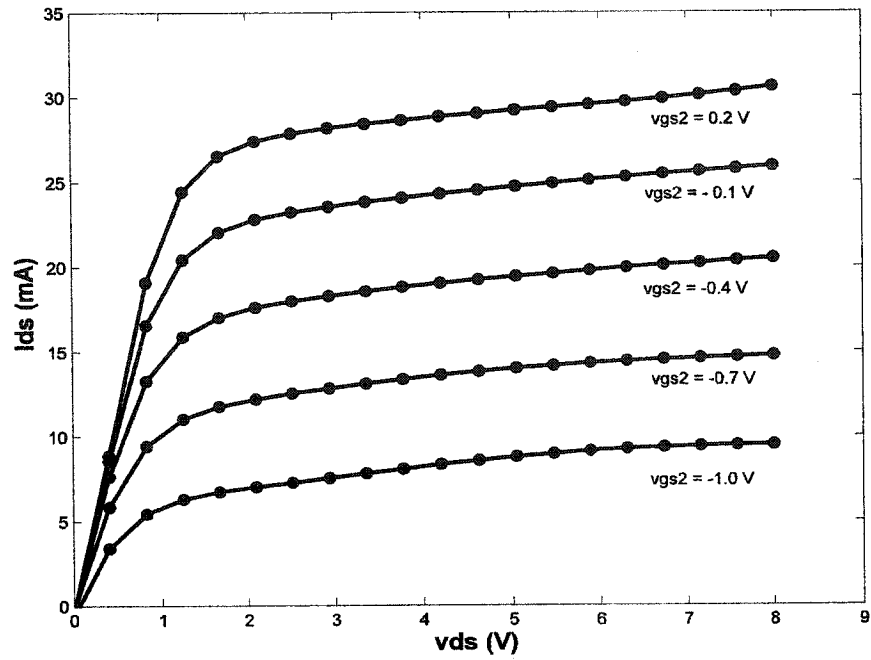


Figure 5.8 Pulsed IV curves (● : measured,— : modeled) for the dual gate FET at different gate pulse amplitudes (v_{gs2})

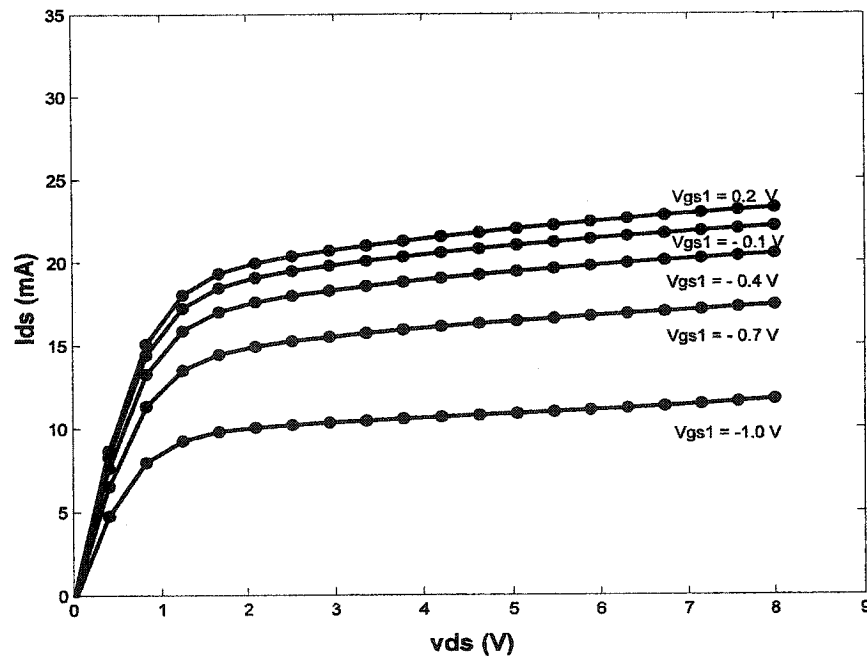


Figure 5.9 Pulsed IV curves (● : measured,— : modeled) for the dual gate FET at different gate bias voltages (V_{gs1})

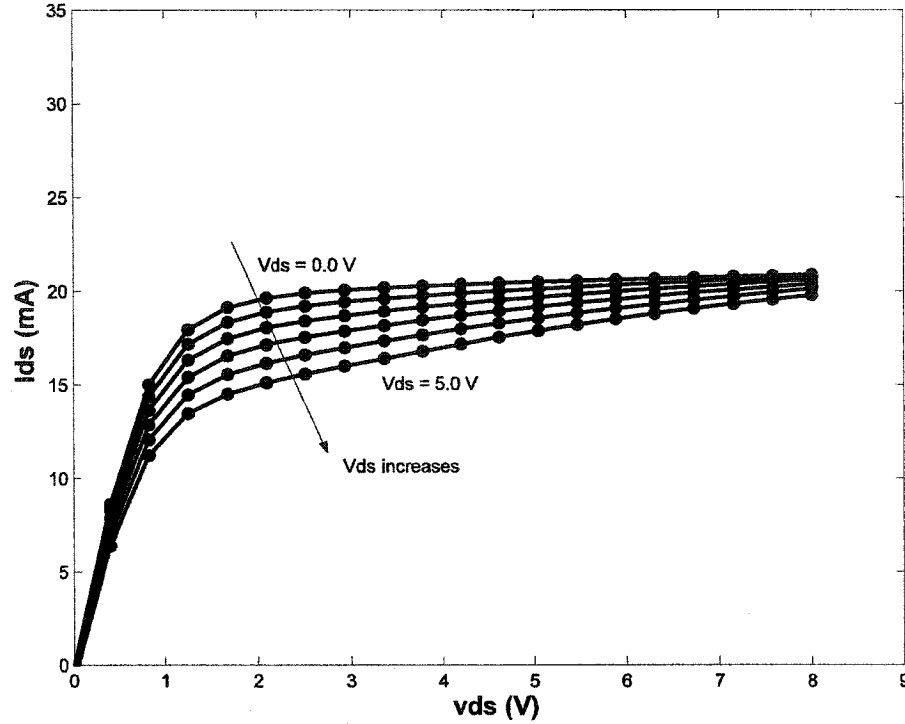


Figure 5.10 Pulsed I-V curves showing variation of pulsed drain current with the drain pulse voltage amplitude (● : measured, — : modeled) for the dual gate FET at different V_{ds} DC bias points

(e) The combined large-signal neural network model

The large-signal drain current neural model is a combination of the two individual neural submodels developed in the previous two sections, i.e., the DC and RF neural models. A schematic of the model is depicted in Figure 5.11.

Before training, the measurement data is first randomized. It is then split into training and testing parts. This step is important to ensure the model training and testing data are well spread in the data range of interest. About 70% of the measurement data points are used to train the model. The remaining 30% data points are used in model testing. Backpropagation with quasi-Newton algorithm is used for model training.

The final model showed a very good agreement between the simulations and the measurement data. The average model error was less than 1%. The overall model generation takes only a few minutes on a typical computer.

It is to be noted that the pulsed I-V characteristics do not show a negative output resistance effect. Negative resistance effect is mainly due to the decrease of the DC drain current with the increase of the DC drain bias. At high drain current values, the device temperature increases and so does the carrier scattering rate, which leads to a drop in the carrier mobility. This effect leads to a drop in the drain current and is called the channel “self-heating” effect. Pulsed characteristics are isothermal (due to having a fixed DC bias current and hence constant DC power). The channel temperature is therefore constant for one given set of bias points. In addition, the pulsed IV characteristics change appreciably with the DC drain bias. As the DC drain bias increases, the drain saturation current decreases and the knee of the curve moves closer to the zero drain voltage. Similar effects have been noticed for the single gate FETs.

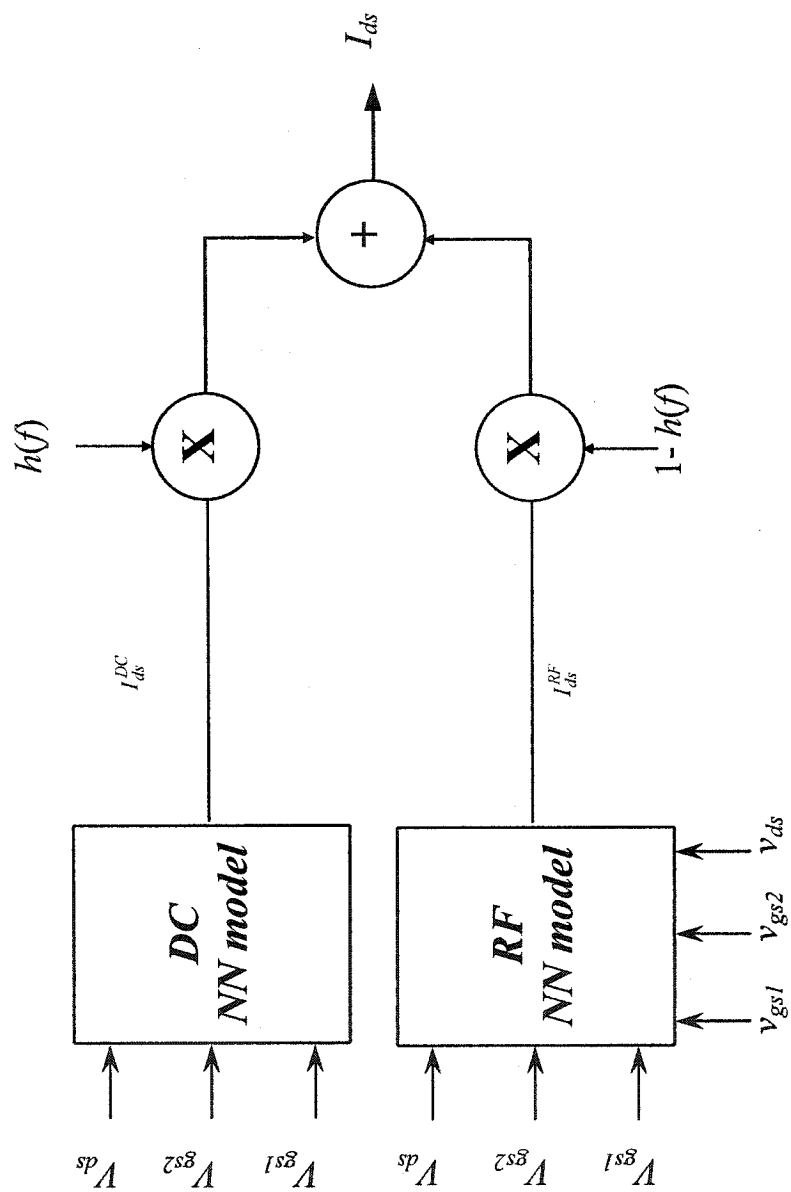


Figure 5.11 The combined large-signal drain current neural model for the dual-gate MESFET

5.2.3 A Thermal large-signal drain-current neural model for the dual-gate MESFET

In the previous sections, a neural network approach for large-signal modeling of the dual-gate MESFET is presented. The model is isothermal and the channel self-heating effect is pacified.

The development of efficient models of single- and dual-gate MESFETs with thermal effects are important to assure accurate electrical performance and reliable operation [72]. Modeling of the drain current is the focus of the majority of the existing nonlinear transistor models, e.g. Curtice, Statz, and Materka [41], since it is the prime cause of the nonlinear transistor behavior. While there exist a number of works on large-signal DGFET models [68], [63], [90], no model, to the author's knowledge, accounts for the effect of device temperature.

Empirical large-signal device modeling including temperature effects, especially for the dual-gate MESFET, is complex and of relatively poor accuracy. The success of neural modeling of devices and circuits has been demonstrated in previous sections. Neural network models are fast, accurate and reliable.

In this section, a temperature dependent large-signal drain current model for the dual-gate MESFET using neural networks is presented.

(a) Description of the model

The modeling technique is demonstrated on an on-wafer symmetric $6 \times 100 \mu\text{m}$ dual gate MESFET manufactured by Nortel Networks. Device characteristics are measured by mounting the wafer on a propping station. The power supplies and the multimeters are connected to the device. These instruments are computer programmed by a central computer with GPIB interface bus and using LabView software. Measurements of the drain current were taken in the ranges: gate voltages, V_{gs1} is $-1.6 \sim 0.6$ (step of 0.2) Volts, V_{gs2} is $-1.6 \sim 0.6$ (step of 0.2) Volts, and drain voltage, V_{ds} is $0.0 \sim 6.0$ (step of 0.1) Volts. The measurement procedure is repeated for various device temperatures ($T = 15, 25, 45$, and 65°C). The device temperature is varied by mounting the wafer on a temperature controlled thermal chuck. A schematic of this measurement setup is shown in Figure 5.12

After the measurement session is complete, measurement data are stored in data files for further processing.

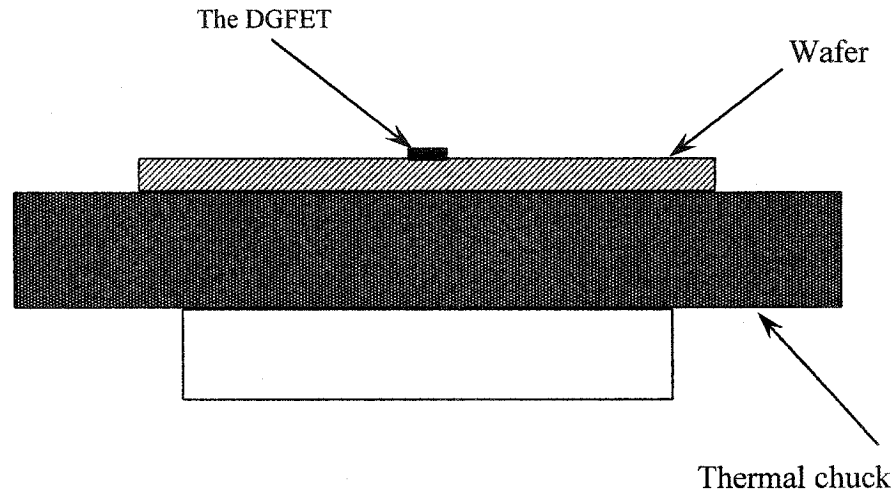


Figure 5.12 Schematic of the thermal measurement environment for the DGFET

(b) Results

The measurement data produced with the measurement setup introduced before are formatted appropriately for use by the *NeuroModeler* [83]. Data files are concatenated into one data file consisting of five columns. The first four columns represent the measurement values of the DC voltages (V_{ds} , V_{gs1} , V_{gs2}) and the temperature T . The final column represents the output current I_{ds} . The total number of measurement data points used in this model is 34,652. About 70% of the available data is used to train the model while the remaining 30% were used for testing.

Three neural models were tested in this case; three-, four-, and five-layer models. It was found that the five-layer model provides the best model accuracy with similar number of neurons as the other models. The five-layer model has one input, one-output and three hidden layers. The total number of model neurons is 21 (10, 7, and 4 neurons for the first, second,

and third hidden layer). The five-layer model showed an excellent fit to the measurement data. The model error is less than %1. Figure 5.13 shows a schematic of this neural network model.

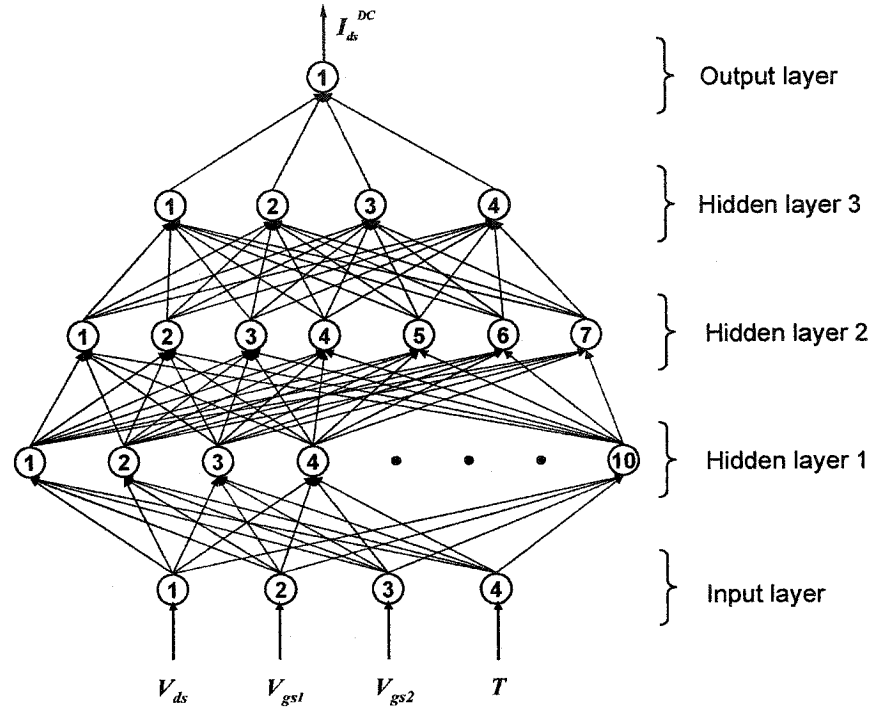


Figure 5.13 The temperature dependent neural network model for the drain current of the dual-gate MESFET manufactured by Nortel Networks

The following results show the modeled and the measurement data of the dual-gate drain current and its dependence on temperature. Figure 5.14 and 5.15 show the variation of the drain current with the drain voltage at several device temperatures. These measurements are taken for values of the $V_{gs1} = V_{gs2} = -0.5$ V (Figure 5.14) and for $V_{gs1} = V_{gs2} = 0.3$ V (Figure 5.15).

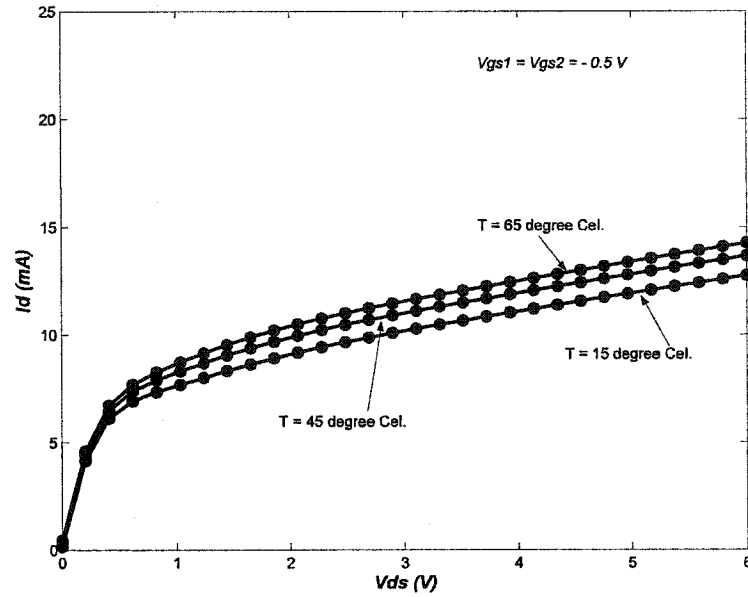


Figure 5.14 Variation of the drain current for the dual-gate MESFET with the drain-to-source voltage V_{ds} at various device temperatures at gate voltages ($V_{gs1} = V_{gs2} = -0.5$ V)

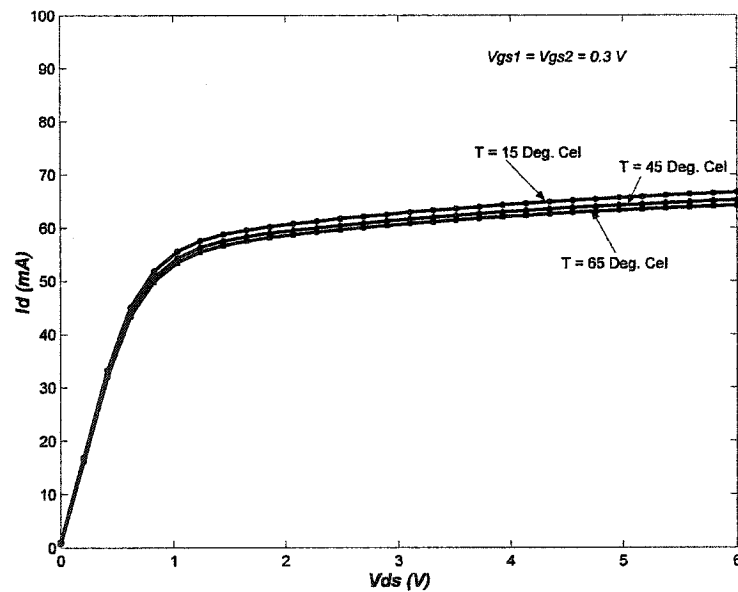


Figure 5.15 Variation of the drain current of the dual gate MESFET with the drain voltage for different values of the device temperature at constant gate voltages ($V_{gs1} = V_{gs2} = 0.3$ V)

Figure 5.16 below shows the temperature dependence of the drain current of the dual-gate MESFET with temperature at various drain voltage (V_{ds}).

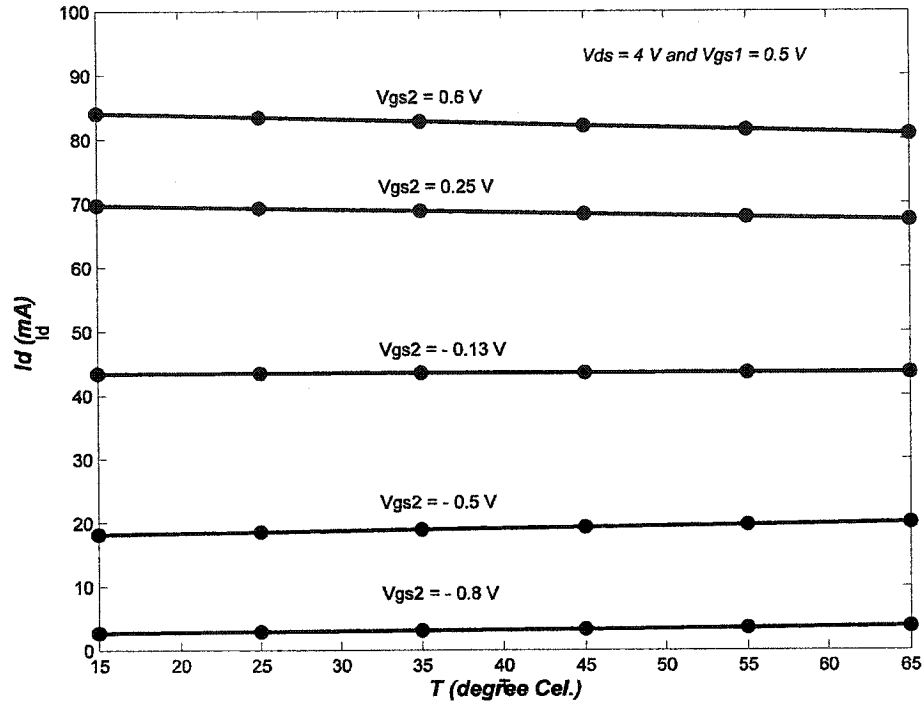


Figure 5.16 Variation of the drain current with temperature at various gate-to-source voltages (V_{gs2}).

Clearly the dependence of the drain current on temperature for a given value of V_{gs1} and V_{gs2} is linear. The Figure also indicates two main effects.

1) The drain current *increases* with temperature when the gate-to-source voltage is less than zero. This result is consistent with previously reported DC measurements for the single-gate MESFET [51] and can be modeled in terms of the threshold voltage.

2) The drain current *decreases* for gate-to-source voltage values above zero. The decrease of the drain current with temperature is mainly as a consequence of reduced mobility and saturation velocity [88].

5.3 Conclusions

In this chapter, MESFET modeling with neural networks is presented. The focus was on the dual-gate large-signal modeling due to the lack of such an important treatment in previous

literature. A neural large-signal RF drain current model for the dual-gate MESFET based on pulsed I-V measurements is presented. The use of pulsed measurement rather than the common DC I-V ones allowed for the elimination (or in the least minimization) of dual-gate channel self-heating effects. This model can thus be considered as an isothermal model.

Also, a complete large-signal neural network drain current neural model for the dual-gate MESFET is presented in this chapter. The static behavior of the device is represented by the DC I-V characteristics while the RF behavior is modeled using pulsed I-V measurements at different bias points.

The model generation is relatively fast (a few minutes on a typical computer). The final model showed very good agreement between the measured and simulated data. The model average error is less than 1%. This model paves the way to including the device model in commercial circuit simulators with the help of “user defined models” capability. This will be demonstrated in details in Chapter 6.

Finally, the dual-gate large-signal neural model is augmented by including the temperature dependence. This serves to widen the model applicability to areas such as power amplifiers, mixers and oscillators.

Chapter 6

SEMI-AUTOMATIC GENERATION OF LARGE-SIGNAL NEURAL NETWORK MODEL OF THE DUAL-GATE MESFET

6.1 *Introduction*

In chapter 5, large-signal neural network models of the drain current of the dual-gate MESFET are introduced. Drain current is considered as the main nonlinear element in the single- and dual-gate MESFETs. Although this assumption provides a relatively good accuracy in lower RF frequency range, but better accuracy is obtained by taking into account the nonlinearity of the junction capacitances and the output conductance.

In this chapter, a large-signal (nonlinear) model of the dual-gate MESFET that takes into account the nonlinearity of the junction capacitances and the output conductance is presented. In essence, the dual-gate MESFET is modeled as two single-gate FETs connected in cascode; each of which contains nonlinear representation of the junction capacitances and the output conductance. This is in addition to the nonlinear transconductance.

Later in this chapter, the generated large-signal dual-gate MESFET model is verified through a nonlinear circuit application. Out of the few possible nonlinear circuit applications, the author chose the nonlinear single-stage amplifier for reasons that will be mentioned later.

6.2 Semi-automatic generation of the large-signal neural network model for the dual-gate MESFET

Developing a large-signal model for a device as complex as the dual-gate MESFET is a demanding task. Existing models [63][67] focus mainly on the drain current. The drain current is modeled by a three dimensional series with variable coefficients. A parameter extraction procedure is required to obtain the coefficients that model the characteristics of a specific device. The number of model parameters in both cases is high (59 and 165) and requires significant extraction efforts.

In this work, the author adopts a neural network technique for reasons that have been detailed in previous chapters. Essentially, the process of producing a large-signal model for the dual-gate MESFET relies on measuring small-signal three-port S-parameters for the dual-gate MESFET at many bias conditions. A one set of three-port S-parameters (at a specific bias point) is then used to obtain other sets of two-port S-parameters of the two cascaded single-gate FETs that constitute the dual-gate MESFET. A two-port parameter extraction process is started for each single-gate FET at a given bias point thereby obtaining a bias dependence of the junction capacitance and conductances for each of the FETs. Neural network models for the nonlinear elements can now be generated using the result from the previous step as the training data. The generated neural network model can then be exported to commercial simulators, e.g. ADS, with the help of the user-defined models. The steps to build the large-signal neural network model for the dual-gate MESFET are detailed in the following sections.

6.2.1 Three-port S-parameter measurements

One way to characterize a large-signal device is to measure the S-parameters at many bias points. For a four-terminal device such as the dual-gate MESFET, three port S-parameter measurements are required. Three port network analyzers are expensive devices and are rare to find due to their high level of sophistication. An alternative to obtain three-port S-parameters is to perform multiple two-port S-parameter measurements between a given set of two ports while terminating the third in its characteristic impedance. For the three-port dual-gate MESFET, three two-port S-parameter measurements are needed to obtain a one-set of three-port S-parameters. Redundant S-parameters resulting from multiple two-port S-

parameter measurements can be ignored. Equation (6.1) shows a typical three-port S-parameters matrix.

$$S_{3P} = \begin{pmatrix} s_{11} & s_{12} & s_{13} \\ s_{21} & s_{22} & s_{23} \\ s_{31} & s_{32} & s_{33} \end{pmatrix} \quad (6.1)$$

As an example, gate₁, gate₂, and the drain of the dual-gate MESFET are assigned as port₁, port₂, and port₃ respectively. At a given DC bias point, three sets of two-port S-parameter measurements are obtained. The first is between gate₁ (port₁) and the drain (port₃, but will be port₂ in this two-port S-parameter set). Gate₂ (port₂) is matched with a 50 Ω impedance. This gives the first set of the two-port S-parameter measurements, which will be called here Set₁. Similarly, the remaining S-parameter sets (Set₂, and Set₃) can be obtained. These sets are related to the three-port S-parameters as follows:

$$Set_1 = \begin{pmatrix} s_{11} & \bullet & s_{13} \\ \bullet & \bullet & \bullet \\ s_{31} & \bullet & s_{33} \end{pmatrix} \quad (6.2)$$

$$Set_2 = \begin{pmatrix} \bullet & \bullet & \bullet \\ \bullet & s_{22} & s_{23} \\ \bullet & s_{23} & s_{33} \end{pmatrix} \quad (6.3)$$

$$Set_3 = \begin{pmatrix} s_{11} & s_{12} & \bullet \\ s_{21} & s_{22} & \bullet \\ \bullet & \bullet & \bullet \end{pmatrix} \quad (6.4)$$

In other words, when performing two-port S-parameter measurements between gate₁ and the drain while gate₂ is terminated, the following relation holds:

$$\begin{aligned} s_{11}(3p) &= s_{11}(2p) & s_{13}(3p) &= s_{12}(2p) \\ s_{31}(3p) &= s_{21}(2p) & s_{33}(3p) &= s_{22}(2p) \end{aligned} \quad (6.5)$$

where $s_{11}(3p)$ is the three-port s_{11} , and $s_{11}(2p)$ is the two-port s_{11} with the assumption that gate₁ is port₁ and drain is port₂.

As a demonstration of obtaining a three-port S-parameter set from three sets of two-port S-parameters, Figure 6.1 below shows a three-port S-parameters for the dual-gate MESFET at a DC bias of ($V_{gs1} = -0.4$ V, $V_{gs2} = 0.2$ V, and $V_{ds} = 5.0$ V) for a frequency range of 0.1 – 26.0 GHz.

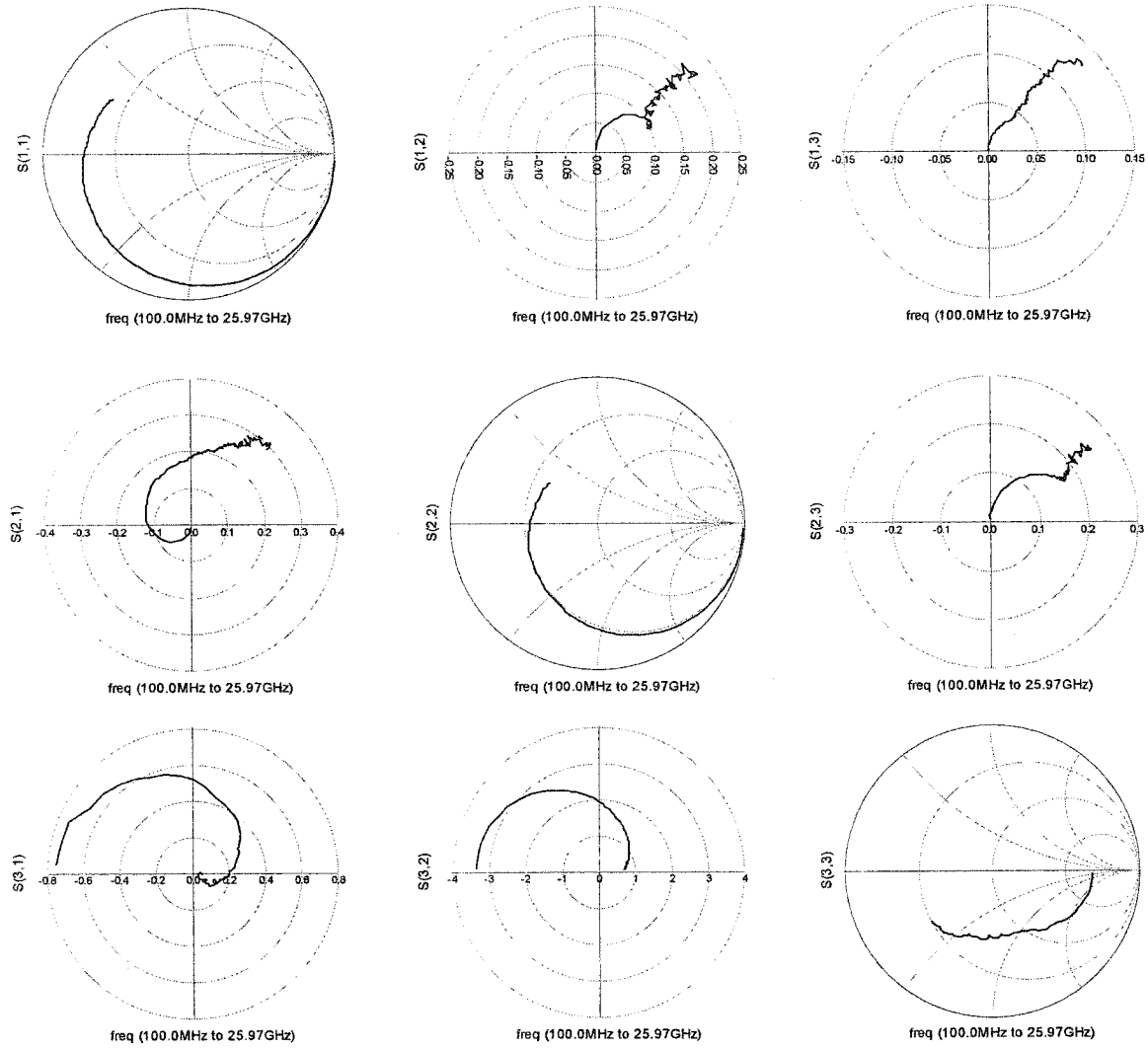


Figure 6.1

A three-port S-parameters of the dual-gate MESFET at DC bias of ($V_{gs1} = -0.4$ V, $V_{gs2} = 0.2$ V, and $V_{ds} = 5.0$ V) at a frequency range of 0.1 – 26.0 GHz.

6.2.2 Obtaining two-port S-parameters for the individual cascoded single-gate FETs

In the previous section, it was shown how three-port S-parameters for the dual-gate MESFET at many bias conditions are obtained from three-sets of two-port S-parameter measurements performed at the same bias. In this section the author shows how these three-port S-parameter data are used to obtain a full large-signal model for the dual-gate MESFET. As mentioned earlier in this chapter, the dual-gate MESFET can be modeled as two single-gate FETs connected in cascode. In this case, the problem of obtaining a large-signal model for the dual-gate MESFET is solved by obtaining the nonlinear dependence of the elements of each of the two single-gate FETs connected in cascode. To be able to do that, the technique described in [67] are adopted. In that technique, the two-port S-parameters for each of the single-gate FETs at various bias points is obtained. Model elements of each single-gate FET, i.e. C_{gs} , C_{gd} , C_{ds} , g_m , and g_{ds} are then obtained by performing parameter extraction using the two-port S-parameters at each bias point. The result in this case gives the nonlinear dependence of FET parameters with the DC bias, i.e. V_{gs1} , V_{gs2} , and V_{ds} . For our modeling purposes we adopt a simplified dual-gate MESFET model as shown in Figure 6.2.

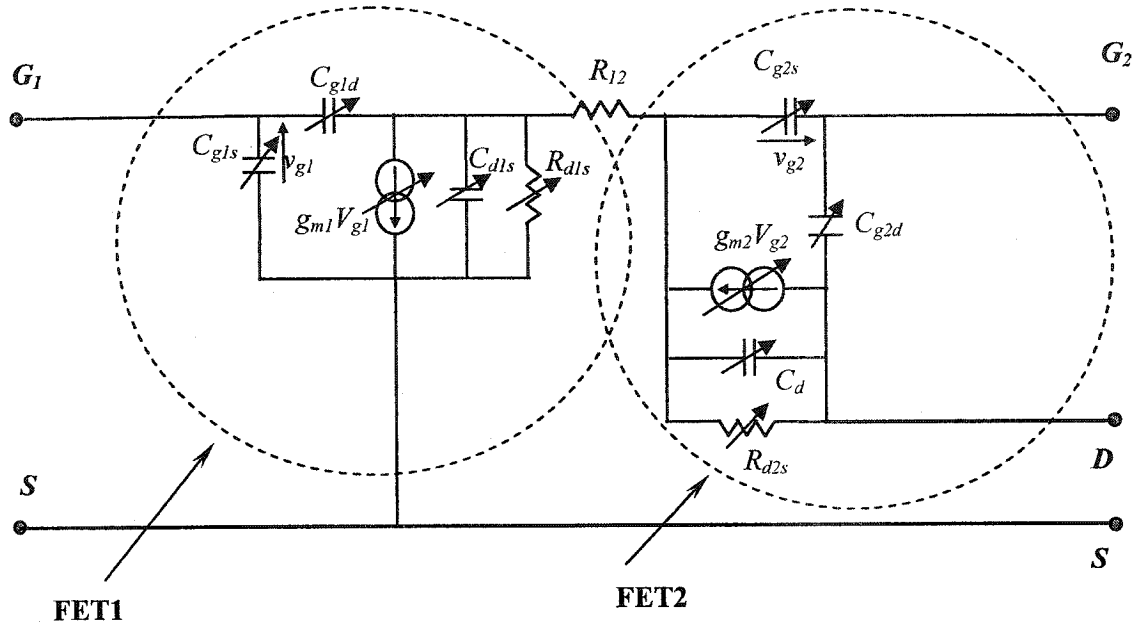


Figure 6.2 A Simplified nonlinear dual-gate MESFET model

The following equation relates the three-port z-parameter matrix $[Z]$ of the dual-gate MESFET (which may be derived from the measured three-port S-parameter as in [45]) to the individual two-port z-parameters of the single-gate FET's:

$$\begin{aligned} Z_{11} &= Z_{11}^I & Z_{12} &= Z_{12}^I & Z_{13} &= Z_{12}^I \\ Z_{21} &= Z_{21}^I & Z_{22} &= \left(Z_{22}^I + Z_{11}^{II} \right) & Z_{23} &= \left(Z_{22}^I + Z_{12}^{II} \right) \\ Z_{31} &= Z_{21}^I & Z_{32} &= \left(Z_{22}^I + Z_{21}^{II} \right) & Z_{33} &= \left(Z_{22}^I + Z_{22}^{II} \right) \end{aligned} \quad (6.6)$$

where Z^I and Z^{II} are the two-port z-parameters of the FET1 and FET2 respectively.

It can be shown from (6.6) that three of the four two-port z-parameters of FET1 (i.e. Z_{11}^I , Z_{12}^I , and Z_{21}^I) are given explicitly. The fourth z-parameter is given under the assumption that $Z_{12}^{II} \ll Z_{22}^I$ by [67]:

$$Z_{22}^I \approx Z_{23} \quad (6.7)$$

The equations for FET2 are also detailed in [67].

However, the dual-gate MESFET currently being modeled (manufactured by Nortel Networks) is symmetric and hence the author assumes that the two single-gate FETs are identical. This assumption is reasonably accurate up to a frequency of around 10 GHz [67].

A program to obtain two-port S-parameters for FET1 from a set of three-port S-parameters is written by the author. This program accepts a list of all the three-port S-parameter files (each file corresponds to a given bias point). It then produces a corresponding list of two-port S-parameter files at the corresponding bias point. The program is written in Matlab. Figure 6.3 below shows a sample of the two-port S-parameters for the FET1 obtained from a corresponding three-port S-parameters for the dual-gate MESFET and at DC bias of $V_{gs1} = -0.6$ V, $V_{gs2} = 0.6$ V, and $V_{ds} = 3.5$ V.

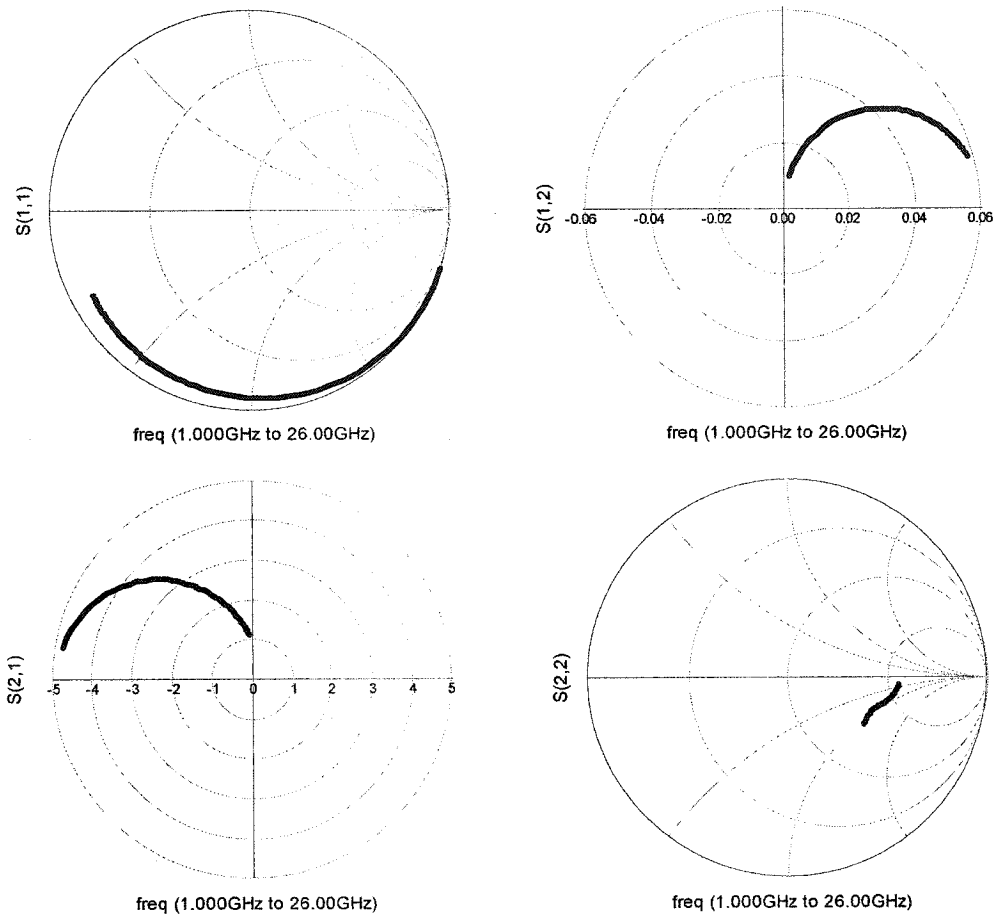


Figure 6.3 Two-port S-parameters for FET1 at bias point of ($V_{gs1} = -0.6$ V, $V_{gs2} = 0.6$ V, and $V_{ds} = 3.5$ V) in the frequency range of 1 – 26 GHz.

6.2.3 Parameter extraction of the nonlinear elements of FET1 and FET2

The two-port S-parameter data for both FET1 and FET2 obtained in the previous section are used by a parameter extraction program developed in this thesis and introduced in chapter 4. The values of the nonlinear elements at each bias point are obtained by performing a bulk parameter extraction over the list of all the two-port S-parameter files at various bias points. Parameter extraction of each S-parameter file provides the values of C_{gs} , C_{gd} , C_{ds} , g_m , and g_{ds} , at DC bias point associated with this particular file. The bulk parameter extraction provides the required nonlinear dependence of the dual-gate parameters with bias in a “numerical” form. This data is used in the following section as the training data to produce a nonlinear neural network model for the dual-gate MESFET.

6.2.4 Generating a large-signal neural network model for the dual-gate MESFET

For the bias ranges of interest mentioned previously there is a total of 1573 bias points. At each bias point there is a set of two-port S-parameters for each of the two single-gate MESFETs, resulting in 1573 S-parameter files (for each FET). Applying parameter extraction on each S-parameter file produces a set on nonlinear elements (C_{gs} , C_{gd} , C_{ds} , g_m , g_{ds}) at the given bias point. The result is that there are 1573 data points representing the nonlinear dependence of each element on V_{gs1} , V_{gs2} , and V_{ds} . This data is used to generate a neural network model for each FET.

The data (1573 data points) is split into two sets, a training set and a testing set. About 75% of the data is used for neural model training. The remaining 25% are used to test the validity of the produced neural model.

Three neural models were tested: a three-layer, a four-layer, and a five-layer perceptron models (MLP3, MLP4 and MLP5 respectively). With roughly similar number of neurons, the four-layer model error was 1.2% while that of the three-layer model was 2.7%. No significant improvement is noticed with a five-layer neural model. The four-layer dual-gate MESFET neural model, Figure 6.4, has a total of 35 neurons, 22 neurons for the first hidden layer and 13 neurons for the second hidden layer

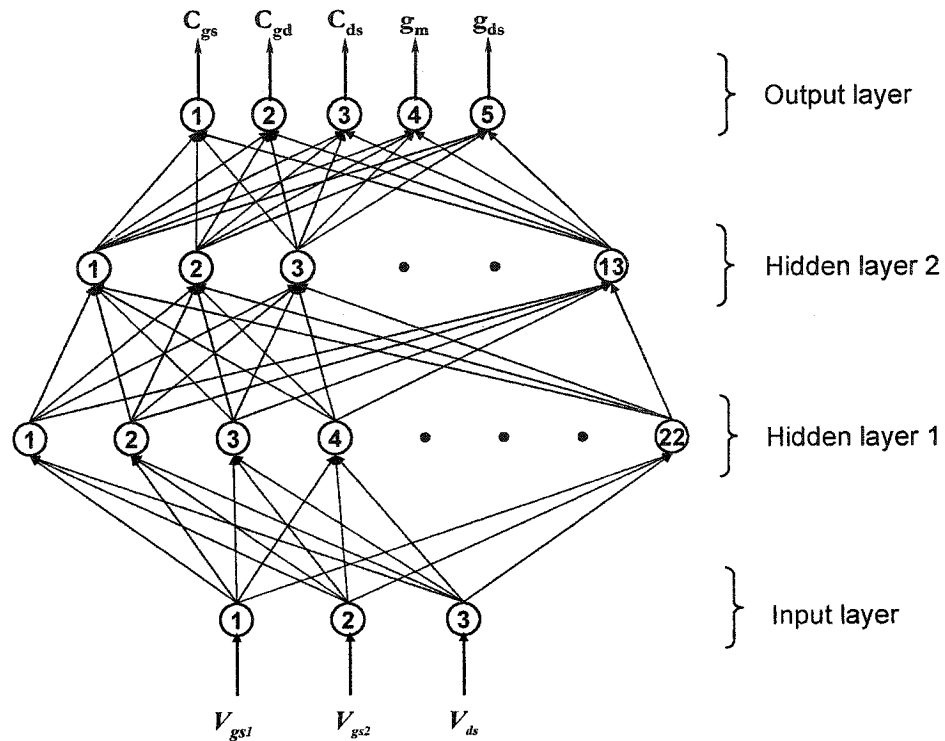


Figure 6.4 The four-layer large-signal neural network model for FET1

To illustrate the model results, Figures 6.5 and 6.6 show the modeled and measurement (extracted) values for two nonlinear elements. Figure 6.5 shows the modeled and the extracted values of the gate-to-source capacitance at various bias conditions. Figure 6.6 shows similar results for the transconductance. Both Figures have very good agreement between modeled and measured data.

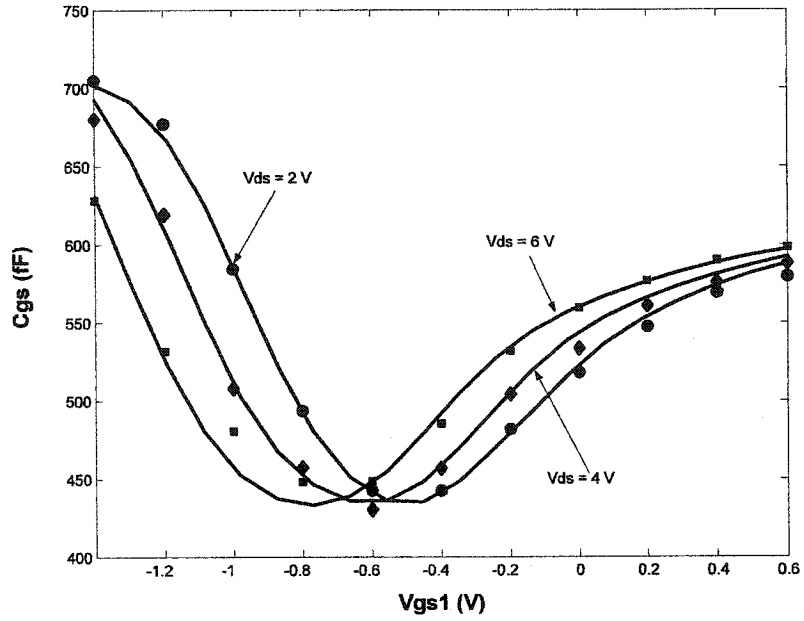


Figure 6.5 Modeled (line) and extracted values (from three-port S-parameter measurements) of the gate-to-source capacitance, C_{gs} vs. V_{gs1} for $V_{ds} = 2\text{V}$, 4V , and 6V

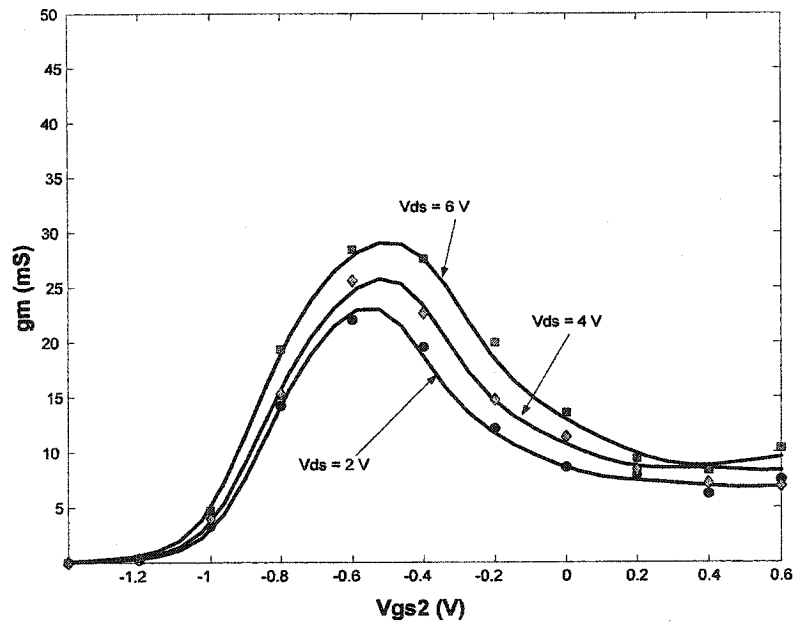


Figure 6.6 Modeled (line) and extracted values (from three-port S-parameter measurements) of the transconductance, g_m vs. V_{gs2} for $V_{ds} = 2\text{V}$, 4V , and 6V

6.2.5 Implementing the large-signal dual-gate MESFET model in commercial circuit simulators

Developing a large-signal model for the dual-gate MESFET is one thing; developing a large-signal model that can be easily used in commercial circuit simulators is another. Nowadays, CAD tools can reduce design efforts significantly by accurately predicting circuits and systems' responses before fabrication. This is only possible if component models, used in a given circuit or system, exist in the given simulator.

The purpose of this section is to demonstrate the implementation of the large-signal dual-gate MESFET model in commercial circuit simulators. The author chose the Advanced Design System (ADS) simulator since it is one of the most powerful and popular commercial microwave circuit simulators available today.

The dual-gate MESFET large-signal model is implemented in ADS with the help of user-defined models. More specifically, the Symbolically Defined Devices (SDD) modeling approach is followed [9]. For the large-signal dual-gate MESFET, a three port nonlinear model is used. To fully characterize a device in an SDD representation, currents and charges have to be defined at each device port. This includes linear and nonlinear components. Appropriate weighting factors $\{0,1\}$ are used for DC or time derivative operators. After completely defining currents and charges at each port, the model is ready to be used as a plug-in component in higher level circuit design.

The following steps describe the process of transforming the neural network nonlinear model developed in the previous sections into an SDD ADS model.

1. Obtain the nonlinear function representation of the neural network model for each model component (i.e. C_{gs} , C_{gd} , g_m , etc...).
2. Perform function integration, when applicable, to obtain the drain current (from g_m) and the charges (from capacitances). It is to be noted that capacitances are assumed to be a weak function of V_{ds} and integration of a capacitance to obtain the corresponding charge is performed over V_{gs} only. In addition, the limits of integrations are to be observed to obtain correct results. In our case, integration is performed analytically using Maple software package [53].

3. The resulting currents and charges are copied to the corresponding ports in ADS.

These steps are demonstrated for the drain current I_{ds} , one of the nonlinear capacitances namely the gate-to-source capacitance, C_{gs} , and the output conductance g_{ds} .

(a) Obtaining a large-signal model for the drain current (using g_m)

The generated neural network model for the transconductance (g_m), is exported as a C-language function. An analytic expression of the neural function of the transconductance is given in the Appendix.

The general form of the neural function of g_m is of the form:

$$g_m = \sigma \left(\sum_{j=0}^{N_L-1} \omega_{ij}^L z_j^{L-1} \right) \quad (6.8)$$

where the defining equations of σ , ω , z , N , and L are given by equations (3.8) – (3.11) in Chapter 3.

The ADS SDD model requires port currents rather than conductances. Therefore, the current corresponding to the transconductance given by (6.8) should be obtained. The transconductance is related to the drain current by the relation:

$$g_m = \frac{\partial}{\partial V_{gs}} I_{ds}(V_{gs}, V_{ds}) \quad (6.9)$$

Therefore, the drain current is obtained from g_m by integration of (6.9) as follows:

$$I_{ds} = \int_{V_{gs0}}^{V_{gs}} g(V_{gs}, V_{ds}) dV_{gs} \quad (6.10)$$

where V_{gs0} is the pinch off voltage (-1.1 V).

The integration of (6.10) is performed analytically using the *Maple* software package. The drain current expression for FET1 resulting from (6.10) is given in the Appendix. A three dimensional plot of the drain current as a function of both V_{gs} and V_{ds} is shown in Figure 6.7 below.

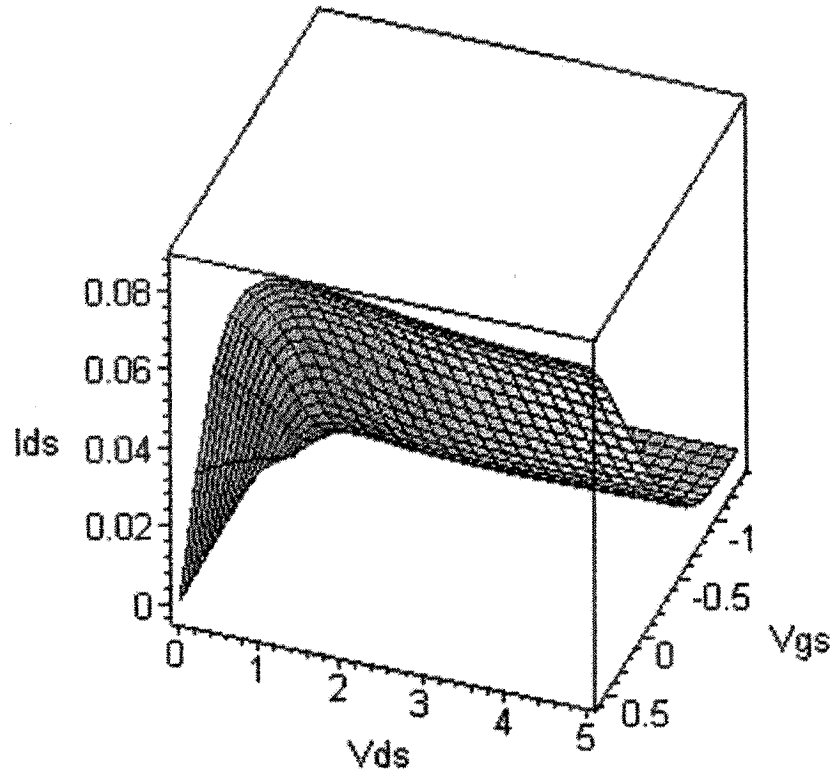


Figure 6.7 A three dimensional plot for the drain current I_{ds} (A), as a function of the gate voltage, V_{gs} , (V) and the drain voltage V_{ds} , (V) obtained by (6.10)

(b) Obtaining a large-signal model for the gate-to-source charge (using C_{gs})

As mentioned previously, the ADS SDD large-signal model requires the charge values at each of its ports. Normally, charges are not directly available but capacitance values are. Charges can be obtained from the capacitance values by integration over the appropriate voltage values. As an example, the gate-to-source charge is obtained from the gate-to-source nonlinear capacitance (and assuming that the capacitance $C_{gs}(V_{gs}, V_{ds})$ is a weak function of V_{ds}) as follows:

$$Q_{gs} = \int_{V_{gs0}}^{V_{gs}} C_{gs}(V_{gs}, V_{ds}) dV_{gs} \quad (6.11)$$

where V_{gs0} is the pinch off voltage (-1.1 Volt).

The nonlinear expression of the gate-to-source capacitance is given by the neural network nonlinear function (given in the Appendix). The integration in (6.11) is performed analytically using *Maple* software package. The final expression is also given in the Appendix. Figure 6.8 shows a three dimensional plot of the nonlinear charge function $Q_{gs}(V_{gs}, V_{ds})$.

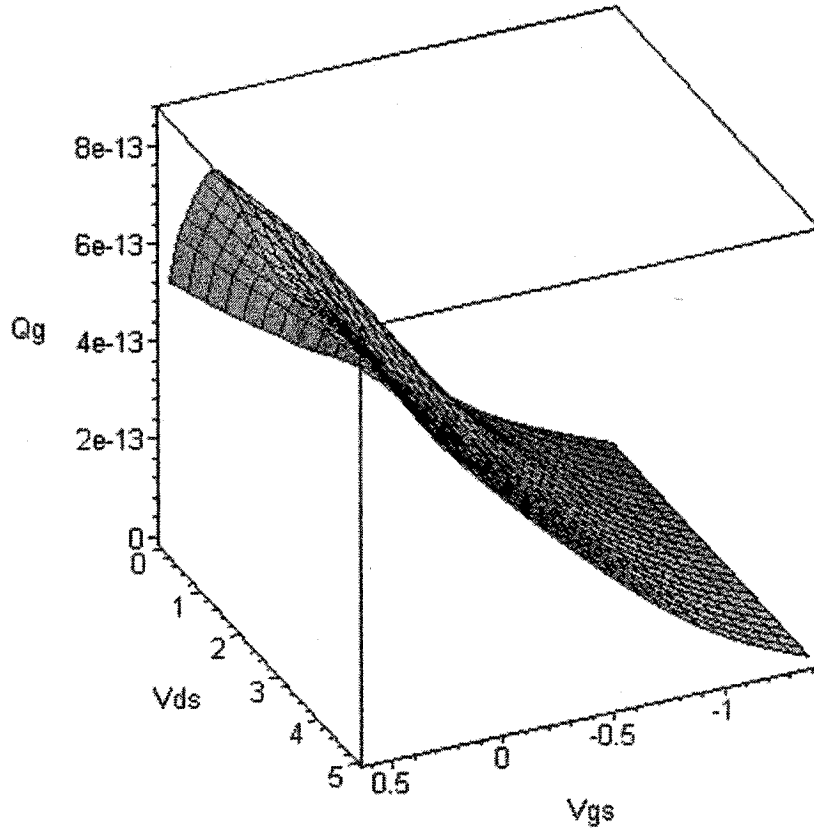


Figure 6.8

A three dimensional plot for the gate-to-source charge Q_g (C) , as a function of the gate voltage, V_{gs} , (V) and the drain voltage V_{ds} , (V) obtained by (6.11)

Similar procedures are applied to the gate-to-drain (C_{gd}) and the drain-to-source (C_{ds}) capacitances. The analytic expressions for C_{gd} and C_{ds} and their corresponding charges are given in the Appendix.

(c) Obtaining a large-signal model for the output conductance (g_{ds})

The nonlinear dependence of the output conductance, g_{ds} , is simpler to obtain since it is directly given by the neural network function obtained from the *NeuroModeler* software. The analytic form of the neural function of g_{ds} is given in the Appendix.

Figure 6.9 shows a three dimensional plot of the nonlinear dependence of the output conductance on the gate-to-source and drain-to-source voltages.

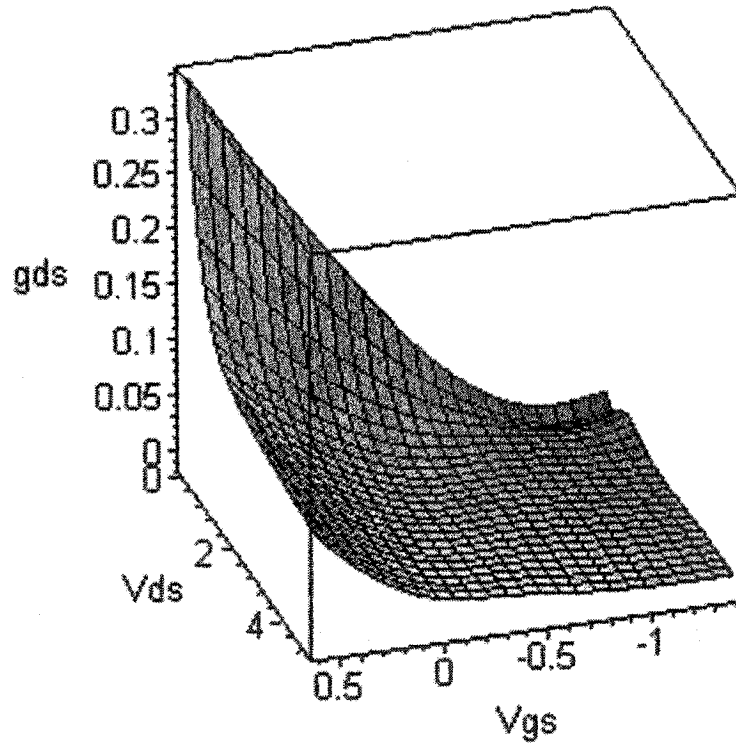


Figure 6.9

A three dimensional plot for the output conductance g_{ds} (S) , as a function of the gate voltage, V_{gs} , (V) and the drain voltage V_{ds} , (V)

6.2.6 Constructing the ADS model for the single-gate FET

In the previous sections, the nonlinear elements composing the single-gate FET nonlinear model are obtained. In this section the ADS model for that single-gate FET is constructed from those elements. Figure 6.10 below shows the terminals and the currents used in developing the ADS SDD model.

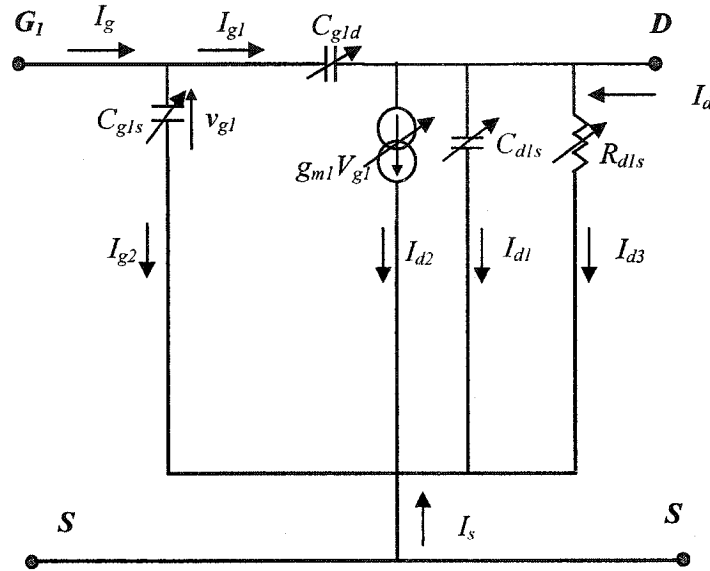


Figure 6.10 Simplified circuit model for FET1 used in the SDD model

The process of creating an SDD model in ADS requires writing of at least one equation at each port. For nonlinear resistors, current-voltage equations are written while for nonlinear capacitors charge-voltage equations are written as follows:

$$I[1,0] = f(v_1) \quad (6.12)$$

$$I[1,1] = \frac{d}{dt} Q(v_1) \quad (6.13)$$

where the first digit in the square bracket refers to the current port number (port "1") and v_1 is the voltage across this port. The second number in the square bracket is referred to in ADS

SDD as “weighting functions”. A weighing function is a frequency-dependent expression used to scale the spectrum of a port current. They are evaluated in the frequency domain. A value of “0” for the weighting function is defined to be identically one. It is used when no weighing is desired. A weighing function of “1” is defined as “ $j\omega$ ” and is used when a time derivative is desired [9].

Based on the rules above, the SDD model for the FET1 is written as follows:

$$\begin{aligned} I_g &= I_{g1} + I_{g2} \\ &= \frac{\partial}{\partial t} Q_{gd}(V_{gs}, V_{ds}) + \frac{\partial}{\partial t} Q_{gs}(V_{gs}, V_{ds}) \end{aligned} \quad (6.14)$$

$$\begin{aligned} I_d &= I_{d1} + I_{d2} + I_{d3} - I_{g1} \\ &= \frac{\partial}{\partial t} Q_{ds}(V_{gs}, V_{ds}) + \int_{V_{gs0}}^{V_{gs}} g_m(V_{gs}, V_{ds}) dV_{gs} + g_{ds} V_{ds} - \frac{\partial}{\partial t} Q_{gd}(V_{gs}, V_{ds}) \end{aligned} \quad (6.15)$$

$$I_s = -(I_{d1} + I_{d2} + I_{d3} + I_{g2}) \quad (6.16)$$

The complete ADS SDD model with equations is shown in Figure 6.11 below.

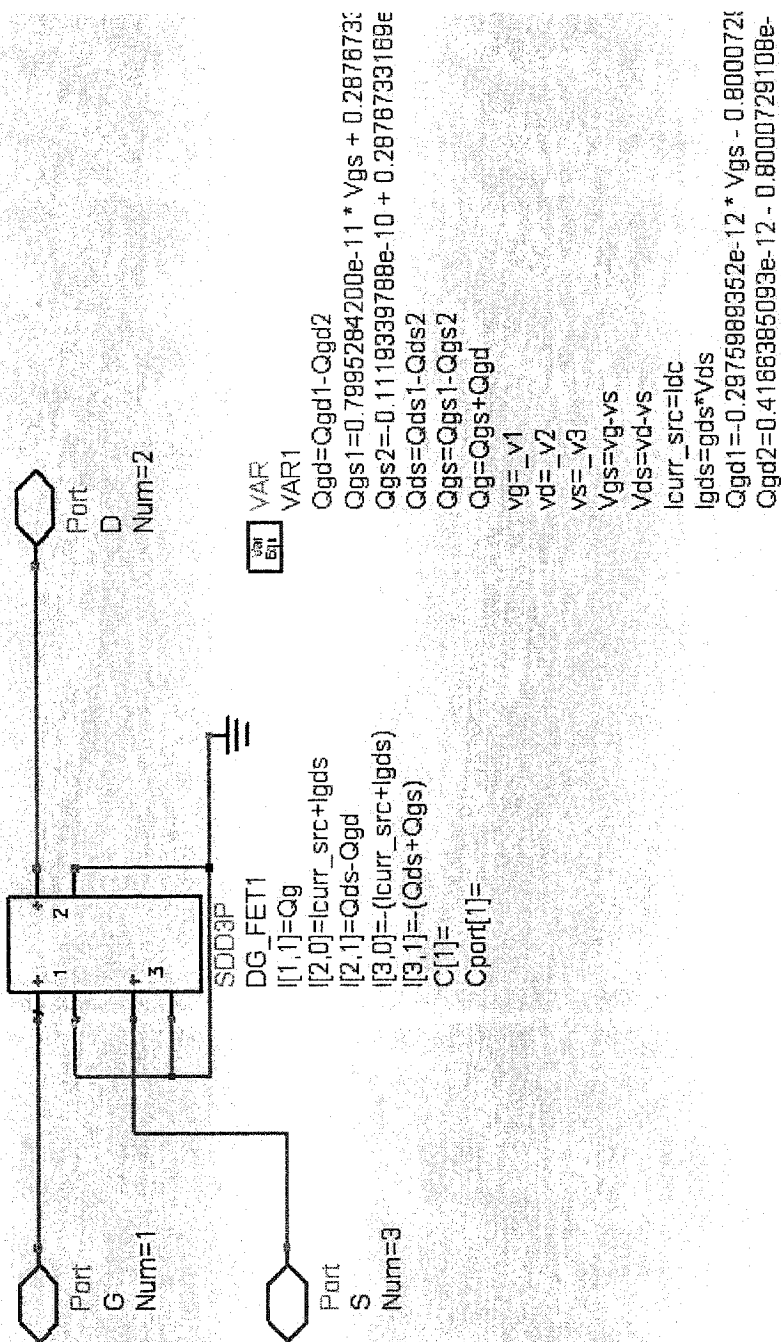


Figure 6.11 The ADS SDD nonlinear model for FET1.

6.3 Verification of the dual-gate large-signal neural network model: A single-stage nonlinear amplifier

Model verification is an essential step in the model generation process to ensure model accuracy and feasibility. The choice of the application for the purpose of model verification depends on the nature of the model. Linear applications provide sufficient platform for linear model verifications. Nonlinear models, however, require developing nonlinear applications to fully verify the model accuracy.

In the previous sections of this chapter, the author developed a neural network based nonlinear model for the dual-gate MESFET. Verification for such model can be achieved through one of several options of dual-gate nonlinear applications. Examples of such applications are nonlinear amplifiers, mixers, and frequency converters. In this work, the dual-gate large-signal model verification is performed through a nonlinear amplifier application due to the availability of such application in an on-wafer form at Nortel Networks (where the author performed most of the experimental work).

6.3.1 Description of the nonlinear dual-gate MESFET application

The application used in model verification is a variable-gain nonlinear amplifier. Figure 6.12 shows its circuit diagram. It consists of six dual-gate MESFETs of various sizes connected in parallel. The sizes of the six dual-gate FETs are: $1 \times 10 \mu\text{m}$, $1 \times 20 \mu\text{m}$, $1 \times 40 \mu\text{m}$, $1 \times 80 \mu\text{m}$, $2 \times 80 \mu\text{m}$, $4 \times 80 \mu\text{m}$. The first digit refers to the number of device gates while the second refers to the gate width (W). The six terminals of the first gate are connected together. Similarly for the drains of the six transistors. Input power is connected to the first gate terminal (gate_1) while output power is taken on the common drain. The second gate of each transistor can be independently connected to a DC bias source. This gate controls whether or not the individual transistor is turned on. Setting the DC bias of this gate to approximately 2.0 V turns on the individual transistor, while connecting a DC voltage of -1.0 V or less to the same gate turns a given transistor off. The overall gain of this stage can therefore be controlled by the number of dual-gate FETs that are turned on. The area of each dual-gate FET in the array of six dual-gates is a power of 2. The value of the overall gain is therefore proportional to a binary number of six digits. In other words, if all dual-gate FETs are turned

on the overall gain is a constant multiplied by the binary number 111111, while the gain is half of that of the full gain if the most significant dual-gate MESFET is turned off (corresponding to 011111). Figure 6.13 shows the layout of the nonlinear amplifier implementation used in this work.

For our verification purposes, this variable-gain amplifier will be used as a constant gain amplifier with its gain set to a maximum. In other words, all the six transistors are turned on and therefore the output gain is at its maximum. In addition, to simplify the model verification, the combination of the six transistors is represented in our model by *one single* dual-gate FET with similar area. Figure 6.14 depicts such an arrangement. More accurate, but rather fairly complex, verification can be obtained by modeling the variable-gain amplifier as six dual-gates connected in parallel. It is the author's opinion that the gain in accuracy is unparalleled with the effort involved. As will be shown later, this approximation shows satisfactory results and is sufficient for the verification purposes



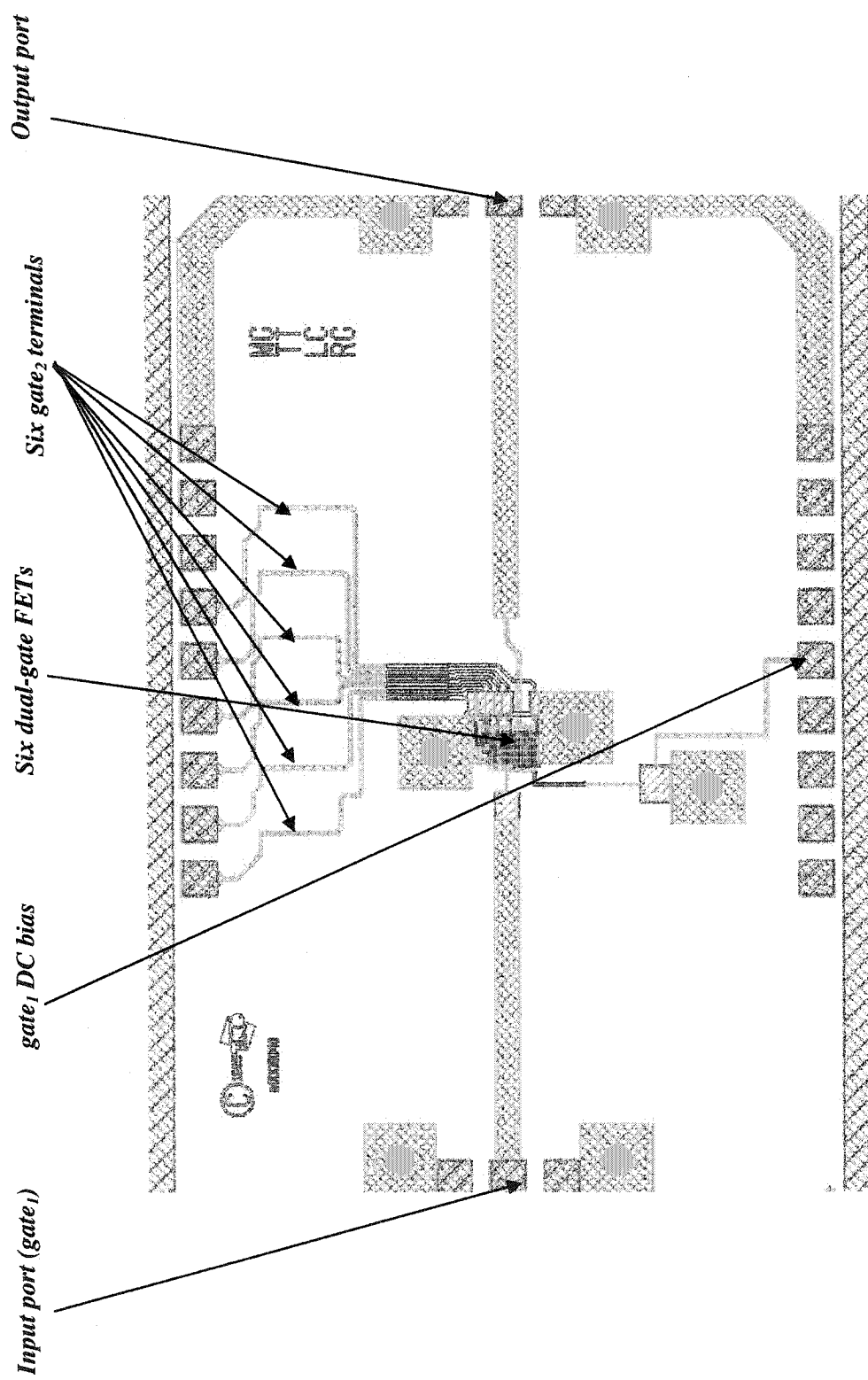


Figure 6.13 The layout of the variable-gain amplifier stage.

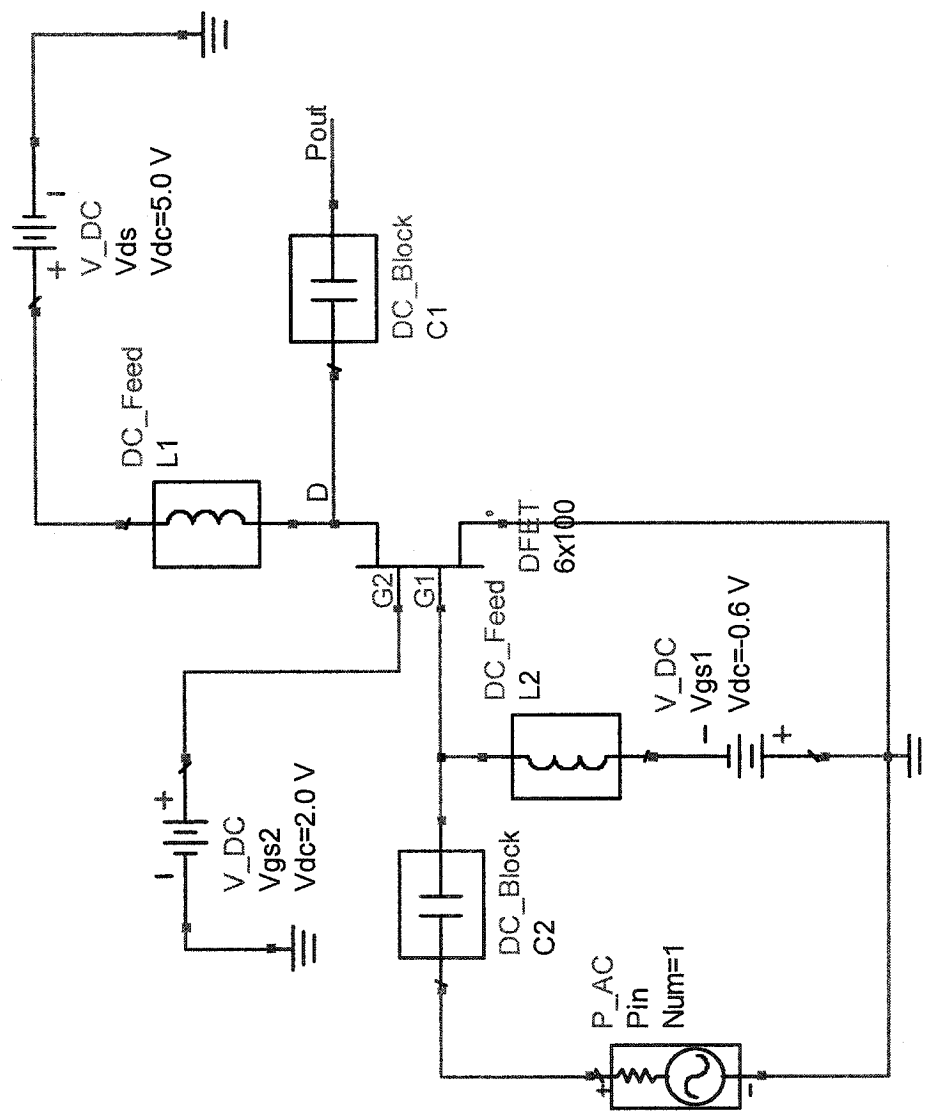


Figure 6.14 The schematic of the variable-gain amplifier stage operated as a fixed-gain amplifier.

6.3.2 The measurement system

The objective of the nonlinear amplifier measurements is to obtain the harmonic contents of the output power when the input large-signal power changes over a given input power range. The measurement setup that achieves this objective consists of:

1. An on-wafer amplifier stage.
2. An on-wafer probing station.
3. An input signal generator with variable power.
4. A spectrum analyzer.
5. DC power supplies.

The author used a probing station, the HP 8662A synthesized signal generator, and the Agilent 8565EC spectrum analyzer as the main components of the measurement setup. The measurement setup and the environment are all provided by Nortel Networks. The measurement setup is shown in Figure 6.15 below.

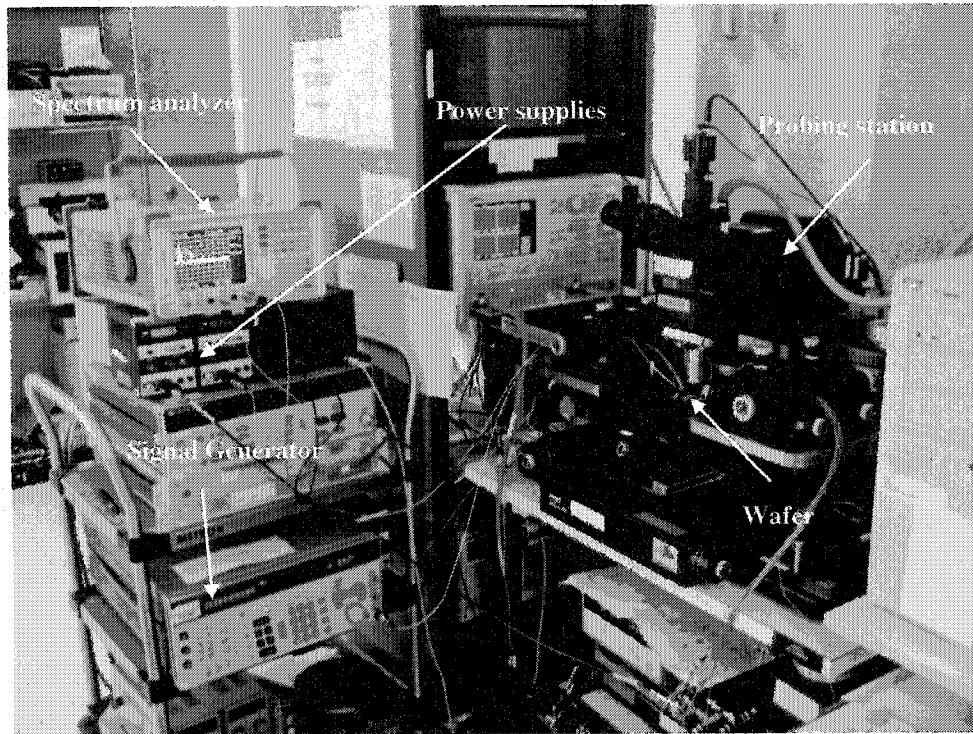


Figure 6.15 On-wafer harmonic content measurements for the variable-gain amplifier stage

6.3.3 Experimental results

The bias conditions for the input/output power measurements are: gate₁ DC bias, V_{gs1} is set to -0.6 V, the gate₂ DC bias, V_{gs2} is set to 2.0 V, the DC drain bias, V_{ds} is set to 5.0 V. The input power is varied from -10.0 dBm till 15.0 dBm in steps of one dBm. The frequency of the input signal is set to 1.2 GHz (maximum frequency of the available signal generator). The spectrum analyzer is set to measure the fundamental and the higher harmonics of the output power. Measurements are recorded for the fundamental, the second, and the third harmonics. Figure 6.16 shows the measured input/output power for the nonlinear amplifier stage till the third harmonic.

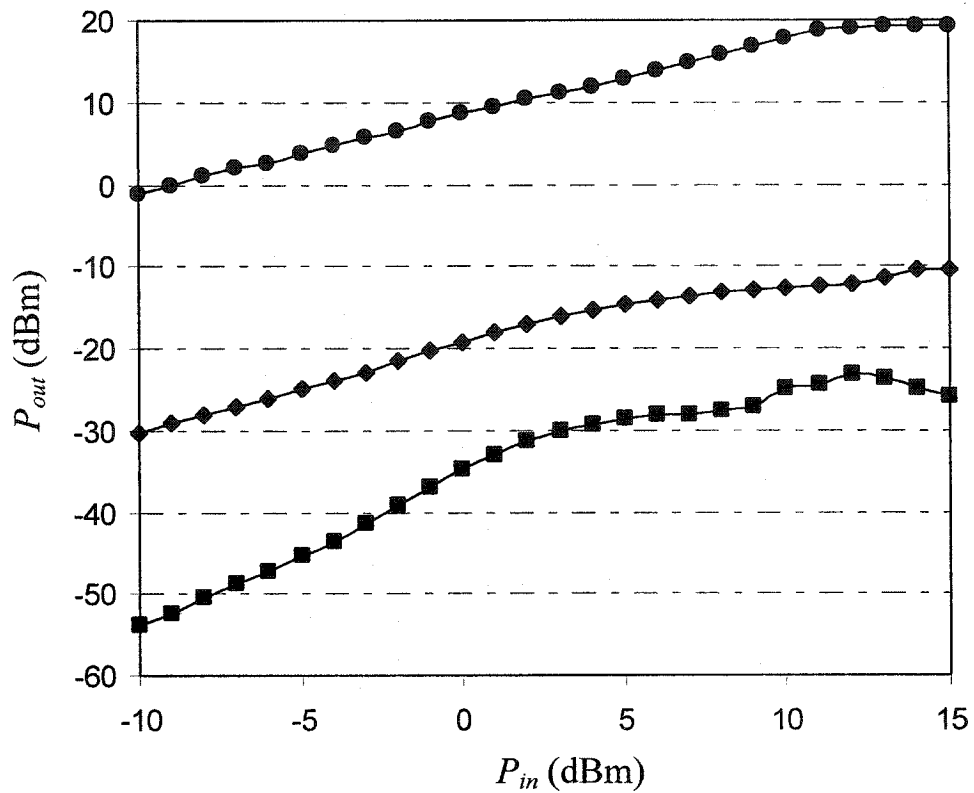


Figure 6.16 The measured input/output power for the nonlinear amplifier stage for first harmonic (●), second harmonic (◆), and third harmonic (■).

The Figure shows an overall gain of approximately 10.0 dB for the amplifier stage. The output power of the fundamental harmonic saturates at higher power levels while more power is “transferred” to the second and the third harmonics.

Figure 6.17 below shows the spectrum analyzer output at an input power of -10.0 dBm. A second harmonic distortion of 30.0 dBm is also shown.

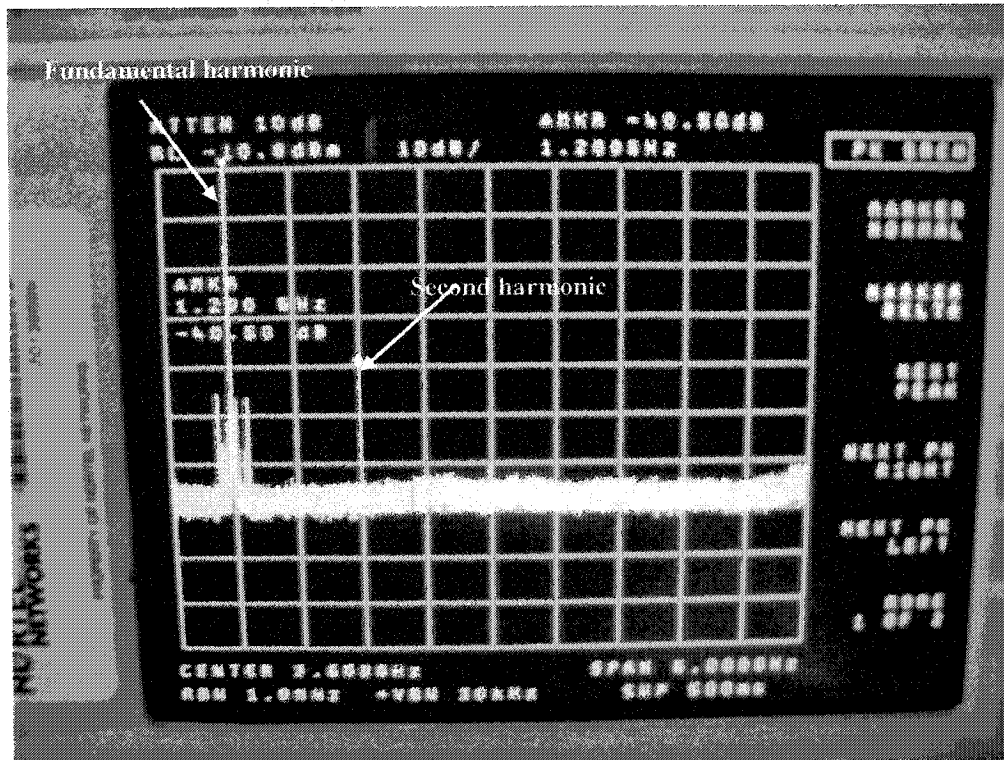


Figure 6.17 The output of the spectrum analyzer at input power of -10.00 dBm

6.3.4 Simulation results

In the previous section, the large-signal measurement results are shown for the nonlinear amplifier stage. In this section harmonic balance simulations are shown for the modeled nonlinear amplifier stage. The core device in this stage is the dual-gate MESFET. The simulation is implemented in ADS and the large-signal dual-gate MESFET model produced earlier in this section is used. Essentially, the dual-gate MESFET is represented as a cascode combination of two single-gate FETs whose neural network large-signal models are developed earlier in this chapter. Figure 6.18 below shows a schematic of the harmonic balance simulation implemented in ADS.

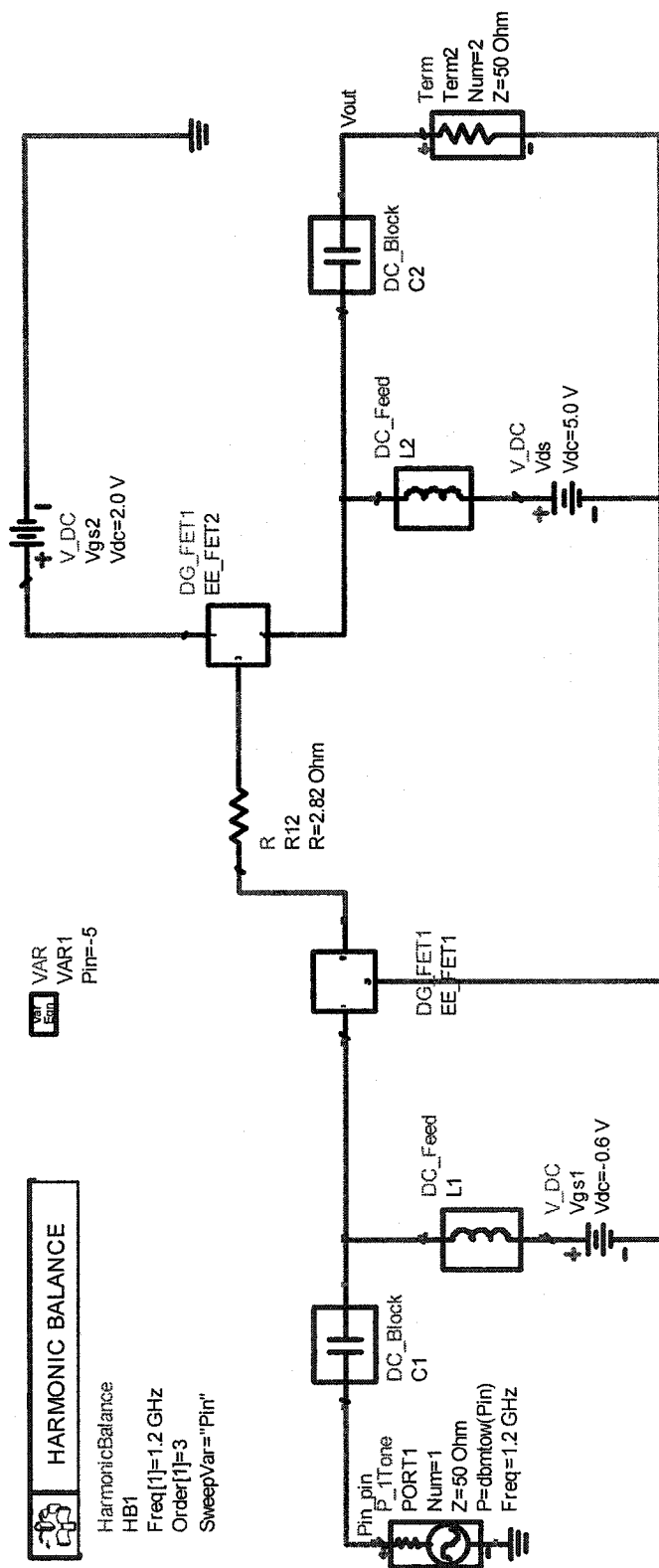


Figure 6.18 A schematic of the harmonic balance simulation of the large-signal amplifier using the dual-gate MESFET model.

In Figure 6.18, the harmonic balance simulation is setup with a variable input power source. Input power level is varied from -10.00 dBm to 15.00 dBm. The frequency of the input power source (single tone) is set to 1.2 GHz. The Figure also shows that the dual-gate MESFET is modeled as a cascode connection of two single-gate FETs. Each FET is “linked” to its ADS nonlinear model. It is to be noted that the two single-gate FETs are connected through a resistor R_{I2} . This resistor models the inter-gate resistance. The value of R_{I2} is obtained from a previous work on a similar device on the same wafer [67][69]. DC bias voltages are also shown on the schematic and are: $V_{gs1} = -0.6$ V, $V_{gs2} = 2.0$ V, and $V_{ds} = 5.0$ V. The values match the bias conditions under which the experimental measurements are performed.

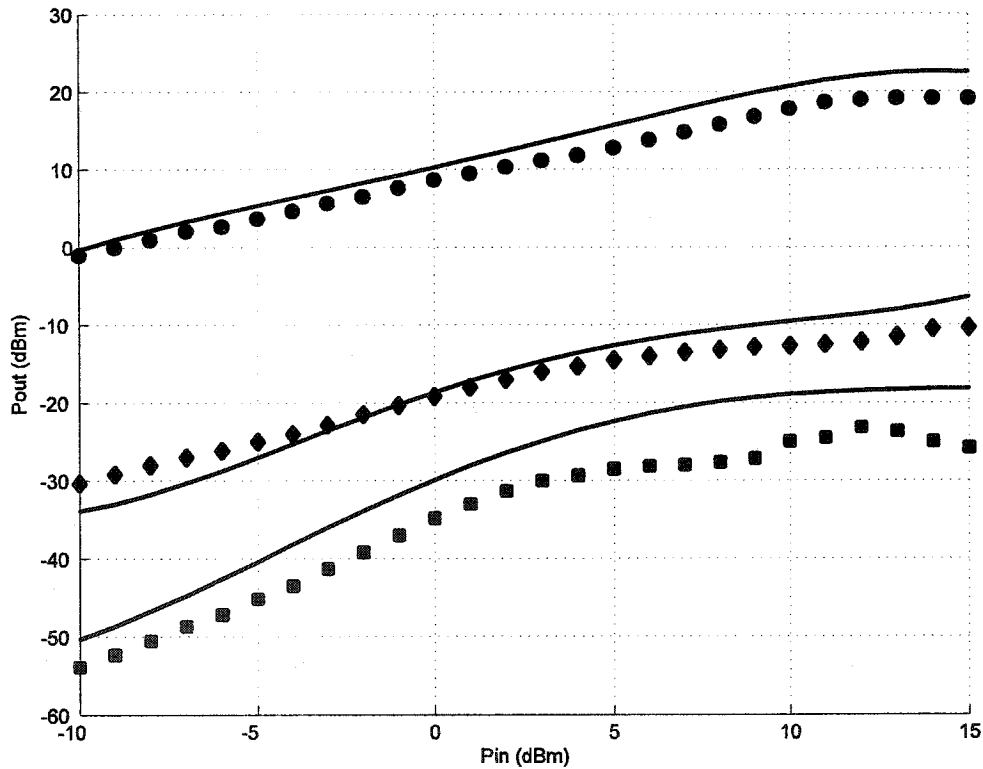


Figure 6.19

The measured and simulated harmonic contents (output power vs. input power) of the nonlinear amplifier stage. (a) measured (●) and simulated (—) fundamental harmonic, (b) measured (◆) and simulated (—) second harmonic, (c) measured (■) and simulated (—) third harmonic.

Figure 6.19 shows the measurements and the harmonic balance simulation of the input/output power transfer characteristics for the single stage dual-gate MESFET amplifier. The results agree to a reasonable degree with the experimental results obtained in the previous section. A maximum gain of about 12 dB is obtained in this case, which is two dB above the experimental results. This can be attributed to some model simplifications. Other discrepancies between the experimental results and the simulations can be attributed to the following reasons.

1. The use of a simplified circuit model of the dual-gate MESFET (Figure 6.2).
2. Neural network modeling errors.
3. The assumption used to develop the nonlinear model from the neural network model. These include the assumption that the nonlinear capacitances are a weak function of V_{ds} .
4. The assumption that the two single-gate FETs comprising the dual-gate FET are identical.
5. The simplification of the six dual-gate MESFETs connected in parallel by a single dual-gate MESFET of similar area.

Overcoming errors due to these assumptions can be a fairly complex and demanding task. For the verification purposes, it is the author opinion that the agreement between the experimental and the simulation result is satisfactory. Future work should include further investigations to identify the prime reasons.

6.4 Conclusions

In this chapter a complete large signal model for the dual-gate MESFET is developed. The model is based on neural networks. The model takes into account the nonlinearity of the transconductance as well as the junction capacitances and output conductance. For the model to be of value to the design community, it is exported to the popular commercial circuit simulator, ADS. This is performed using the powerful ADS symbolically defined devices (SDD) modeling approach. In order to verify the model correctness, a large-signal amplifier application based on the dual-gate MESFET is setup and measured. Also harmonic balance simulation is setup in ADS with similar conditions. The experimental and simulation results

show a satisfactory agreement. Intuitively, causes for some disagreements between the measurements and the simulations are attributed to some assumption regarding the symmetry of the dual-gate and other simplifications while in the process of developing the model.

Chapter 7

SUMMARY, CONCLUSIONS AND FUTURE WORKS

7.1 *Summary*

In the context of this thesis, novel CAD tools and techniques to model the GaAs MESFET with conventional and neural network techniques are presented. These techniques are demonstrated on single- and dual-gate MESFETs in both chip and on-wafer forms. Small and large-signal models for both devices are studied.

TopFinder, a CAD tool for optimal small-signal topology generation is developed in order to facilitate the topology selection process for the designer and to overcome the disadvantages of the trial-and-error model tuning procedures currently being followed. The tool is demonstrated on the EFA018A single-gate GaAs MESFET. Although the tool was designed mainly for the FET transistors, due to the similarities between the GaAs MESFET and the HEMT, the tool was tested on the EPB0185A HEMT with very good results.

Novel neural network large-signal and temperature models for the drain current of the dual-gate GaAs MESFET are also presented in this thesis. It is shown that neural techniques offer significant advantages of speed, accuracy, and suitability to computer-aided design. This is demonstrated on a chip dual-gate GaAs MESFET, the NE25118, and on the on-wafer dual-gate MESFET manufactured by Nortel Networks. The results showed excellent agreement between the model and the experimental data.

A large-signal neural network model for the dual-gate MESFET including the nonlinear capacitances is also introduced in this work. This model is exported to the popular commercial simulator by Agilent Technologies (ADS). The model is then verified through a single-stage nonlinear amplifier. Comparison of the harmonic contents and the harmonic balance simulation done in ADS showed reasonable agreement.

7.2 Recommendation for future work

The nanotechnology is now emerging as the leading edge in semiconductor development arena. With this technology, HEMTs can be fabricated with an f_{max} frequency as high as several hundred GHz. Moreover, InP/InGaAs heterojunction bipolar transistors (HBT) can be manufactured with sub-micron techniques to have a unity-gain frequency (f_T) of over 200 GHz and sometimes an f_{max} as high as 1.0 THz. With this frequency of operation, conventional models need to be looked at closely. Significant changes of existing standard topologies for these devices might be required. Parasitic components should also be looked at since they will be of significant effect at such high frequencies.

Due to the complexity of the dual-gate MESFET, more work is still required to provide fully automated and more accurate small and large-signal models. The large-signal dual gate MESFET model generated in this work required some manual intervention between two successive automatic operations (e.g. changing the format of the neural function exported by the *NeuroModeler* to a Maple compatible format). Other similar situations exist that presents some hurdles to a fully automated model generation process. These hurdles can be overcome if more tool integration is provided. The researcher can also design a tool-integration strategy by using proper communication channels and protocols between various commercial software packages.

In addition, a more accurate large-signal dual-gate MESFET model can be obtained by including the parasitic well as the nonlinear elements in the model. Although this make the model fairly complex, but it provides significant improvement to the model accuracy at higher frequency ranges of operations (above 25 GHz).

Temperature dependent large-signal models for the dual-gate MESFETs are also essential especially in power applications. The development of such models that include

capacitances and conductances requires the measurements of three-port S-parameters at various device temperatures. Repeating the technique followed in this thesis at each device temperature can lead to a full temperature dependent large-signal dual-gate MESFET model. This process can be fairly time consuming without appropriate automation strategies.

A potential alternative to the dual-gate large-signal modeling techniques used in this thesis is to use pulsed S-parameter measurements and/or load-pull measurements to extract the large-signal device parameters. This technique is efficient but requires a sophisticated experimental setup.

Noise performance of devices is essential for efficient communication systems (especially low power hand held devices). This calls for the development of device models that incorporates the noise effects (noise models). Dual-gate MESFET noise models are non-trivial and require further work and investigation.

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Appendix

Calculation of the nonlinear drain current, $I_{ds}(V_{gs}, V_{ds})$.

The transconductance as a nonlinear function of V_{gs} and V_{ds} is given by:

$$\begin{aligned}
 gm := & -0.2934462660 - \frac{.1358954320}{1.0 + e^{(2.043146000 + 3.587460000 V_{gs} + .1391226667 V_{ds})}} \\
 & + \frac{.2574305540e-1}{1.0 + e^{(-.827096000 - 6.760230000 V_{gs} + .8318799999e-1 V_{ds})}} \\
 & + \frac{.4394760060}{1.0 + e^{(-1.14453120 - .6038280000 V_{gs} - 3.988766666 V_{ds})}} \\
 & - \frac{.5315933320}{1.0 + e^{(2.116408800 - .3558930000 V_{gs} - .1035120000 V_{ds})}} \\
 & + \frac{.7095113000}{1.0 + e^{(2.58948800 + 1.102470000 V_{gs} + 3.991466666 V_{ds})}} \\
 & - \frac{.2975021760}{1.0 + e^{(-2.189498000 - 4.178970000 V_{gs} + 1.171093333 V_{ds})}} \\
 & + \frac{.2419217560}{1.0 + e^{(-2.790052000 - 3.988530000 V_{gs} + 1.332976667 V_{ds})}} \\
 & + \frac{.2601199020}{1.0 + e^{(4.084395000 + 1.160270000 V_{gs} - .1238190000 V_{ds})}}
 \end{aligned}$$

Integration of g_m w.r.t. V_{gs} gives the drain current I_{ds} as follows:

$$\begin{aligned}
 Idc := & -0.03788068215 \ln(e^{(2.043146000 + 3.587460000 V_{gs} + 0.1391226667 V_{ds})}) \\
 & + 0.03788068215 \ln(1. + e^{(2.043146000 + 3.587460000 V_{gs} + 0.1391226667 V_{ds})}) \\
 & - 0.003808014727 \ln(e^{(-.8270960000 - 6.760230000 V_{gs} + 0.08318799999 V_{ds})}) \\
 & + 0.003808014727 \ln(1. + e^{(-.8270960000 - 6.760230000 V_{gs} + 0.08318799999 V_{ds})}) \\
 & - 0.7278165405 \ln(e^{(-1.144531200 - 0.6038280000 V_{gs} - 3.988766666 V_{ds})}) \\
 & + 0.7278165405 \ln(1. + e^{(-1.144531200 - 0.6038280000 V_{gs} - 3.988766666 V_{ds})}) \\
 & + 1.493688642 \ln(e^{(2.116408800 - 0.3558930000 V_{gs} - 0.1035120000 V_{ds})}) \\
 & - 1.493688642 \ln(1. + e^{(2.116408800 - 0.3558930000 V_{gs} - 0.1035120000 V_{ds})}) \\
 & + 0.6435651764 \ln(e^{(2.589488000 + 1.102470000 V_{gs} + 3.991466666 V_{ds})})
 \end{aligned}$$

$$\begin{aligned}
& -0.6435651764 \ln(1 + e^{(2.589488000 + 1.102470000 V_{gs} + 3.991466666 V_{ds})}) \\
& + 0.07119031149 \ln(e^{(-2.189498000 - 4.178970000 V_{gs} + 1.171093333 V_{ds})}) \\
& - 0.07119031149 \ln(1 + e^{(-2.189498000 - 4.178970000 V_{gs} + 1.171093333 V_{ds})}) \\
& - 0.06065436539 \ln(e^{(-2.790052000 - 3.988530000 V_{gs} + 1.332976667 V_{ds})}) \\
& + 0.06065436539 \ln(1 + e^{(-2.790052000 - 3.988530000 V_{gs} + 1.332976667 V_{ds})}) \\
& + 0.2241891129 \ln(e^{(4.084395000 + 1.160270000 V_{gs} - 0.1238190000 V_{ds})}) \\
& - 0.2241891129 \ln(1 + e^{(4.084395000 + 1.160270000 V_{gs} - 0.1238190000 V_{ds})}) \\
& + 0.03788068215 \ln(e^{(-2.979298000 + 0.1391226667 V_{ds})}) \\
& - 0.03788068215 \ln(1 + e^{(-2.979298000 + 0.1391226667 V_{ds})}) \\
& + 0.003808014727 \ln(e^{(8.637226000 + 0.08318799999 V_{ds})}) \\
& - 0.003808014727 \ln(1 + e^{(8.637226000 + 0.08318799999 V_{ds})}) \\
& - 0.7278165405 \ln(1 + e^{(-0.2991720000 - 3.988766666 V_{ds})}) \\
& - 1.493688642 \ln(e^{(2.614659000 - 0.1035120000 V_{ds})}) \\
& + 1.493688642 \ln(1 + e^{(2.614659000 - 0.1035120000 V_{ds})}) \\
& - 0.6435651764 \ln(e^{(1.046030000 + 3.991466666 V_{ds})}) \\
& + 0.6435651764 \ln(1 + e^{(1.046030000 + 3.991466666 V_{ds})}) \\
& - 0.07119031149 \ln(e^{(3.661060000 + 1.171093333 V_{ds})}) \\
& + 0.07119031149 \ln(1 + e^{(3.661060000 + 1.171093333 V_{ds})}) \\
& + 0.06065436539 \ln(e^{(2.793890000 + 1.332976667 V_{ds})}) \\
& - 0.06065436539 \ln(1 + e^{(2.793890000 + 1.332976667 V_{ds})}) \\
& - 0.2241891129 \ln(e^{(2.460017000 - 0.1238190000 V_{ds})}) \\
& + 0.2241891129 \ln(1 + e^{(2.460017000 - 0.1238190000 V_{ds})}) - 0.2934462660 V_{gs} \\
& - 0.4108247724 + 0.7278165405 \ln(e^{(-0.2991720000 - 3.988766666 V_{ds})})
\end{aligned}$$

Calculation of the nonlinear gate-to-source charge, $Q_{gs}(V_{gs}, V_{ds})$.

The nonlinear gate-to-source capacitance $C_{gs}(V_{gs}, V_{ds})$ is given by:

$$\begin{aligned}
 C_{gs} := & .7995284200e-11 - \frac{.1028808960e-12}{1.0 + e^{(-23.99914000 - 35.76310000 V_{gs} + 22.62800000 V_{ds})}} \\
 & - \frac{.2157529480e-11}{1.0 + e^{(.89897000 - 30.25100000 V_{gs} + 1.779343333 V_{ds})}} \\
 & - \frac{.4352037040e-11}{1.0 + e^{(-2.009838600 + .3669310000 V_{gs} - .3707966666e-1 V_{ds})}} \\
 & - \frac{.3636800860e-11}{1.0 + e^{(-2.629192000 + 1.213720000 V_{gs} + 2.390350000 V_{ds})}} \\
 & - \frac{.1469415020e-12}{1.0 + e^{(3.570460000 + 6.283900000 V_{gs} + .4868300000 V_{ds})}} \\
 & - \frac{.4033402240e-12}{1.0 + e^{(14.31112000 - 21.38880000 V_{gs} - .4509133333 V_{ds})}} \\
 & - \frac{.3609382780e-11}{1.0 + e^{(2.810354000 - 1.084240000 V_{gs} - 2.399736666 V_{ds})}} \\
 & + \frac{.2220008860e-11}{1.0 + e^{(.78744000 - 31.96060000 V_{gs} + 1.881573333 V_{ds})}} \\
 & - \frac{.6715613200e-12}{1.0 + e^{(2.68717640 - .5378090000 V_{gs} + 10.94040000 V_{ds})}} \\
 & - \frac{.2380946680e-12}{1.0 + e^{(-2.089980000 - 13.55660000 V_{gs} + 2.198376666 V_{ds})}}
 \end{aligned}$$

Integrating the capacitance w.r.t. V_{gs} with the appropriate limits of integration gives the gate-to-source charge as follows:

$$\begin{aligned}
 Q_{gs} := & .6946080049e-13 \ln(e^{(45.53228000 + 1.881573333 V_{ds})}) \\
 & - .1885754339e-13 \ln(1. + e^{(14.31112000 - 21.38880000 V_{gs} - .4509133333 V_{ds})}) \\
 & - .1186064148e-10 \ln(1. + e^{(-2.523542000 - .3707966666e-1 V_{ds})}) \\
 & - .2876733169e-14 \ln(1. + e^{(-23.99914000 - 35.76310000 V_{gs} + 22.62800000 V_{ds})}) \\
 & + .2876733169e-14 \ln(e^{(-23.99914000 - 35.76310000 V_{gs} + 22.62800000 V_{ds})}) \\
 & - .7132093088e-13 \ln(1. + e^{(.8989700000 - 30.25100000 V_{gs} + 1.779343333 V_{ds})})
 \end{aligned}$$

$$\begin{aligned}
& + .7132093088e-13 \ln(e^{(.8989700000 - 30.25100000 V_{gs} + 1.779343333 V_{ds})}) \\
& + .6946080049e-13 \ln(1. + e^{(.7874400000 - 31.96060000 V_{gs} + 1.881573333 V_{ds})}) \\
& - .6946080049e-13 \ln(e^{(.7874400000 - 31.96060000 V_{gs} + 1.881573333 V_{ds})}) \\
& - .1248698553e-11 \ln(1. + e^{(2.687176400 - .5378090000 V_{gs} + 10.94040000 V_{ds})}) \\
& + .1248698553e-11 \ln(e^{(2.687176400 - .5378090000 V_{gs} + 10.94040000 V_{ds})}) \\
& - .1756300754e-13 \ln(1. + e^{(-2.089980000 - 13.55660000 V_{gs} + 2.198376666 V_{ds})}) \\
& + .1756300754e-13 \ln(e^{(-2.089980000 - 13.55660000 V_{gs} + 2.198376666 V_{ds})}) \\
& + .1186064148e-10 \ln(1. + e^{(-2.009838600 + .3669310000 V_{gs} - .3707966666e-1 V_{ds})}) \\
& - .1186064148e-10 \ln(e^{(-2.009838600 + .3669310000 V_{gs} - .3707966666e-1 V_{ds})}) \\
& + .2996408447e-11 \ln(1. + e^{(-2.629192000 + 1.213720000 V_{gs} + 2.390350000 V_{ds})}) \\
& - .2996408447e-11 \ln(e^{(-2.629192000 + 1.213720000 V_{gs} + 2.390350000 V_{ds})}) \\
& + .2338380655e-13 \ln(1. + e^{(3.570460000 + 6.283900000 V_{gs} + .4868300000 V_{ds})}) \\
& - .2338380655e-13 \ln(e^{(3.570460000 + 6.283900000 V_{gs} + .4868300000 V_{ds})}) \\
& + .1885754339e-13 \ln(e^{(14.31112000 - 21.38880000 V_{gs} - .4509133333 V_{ds})}) \\
& - .3328951874e-11 \ln(1. + e^{(2.810354000 - 1.084240000 V_{gs} - 2.399736666 V_{ds})}) \\
& + .3328951874e-11 \ln(e^{(2.810354000 - 1.084240000 V_{gs} - 2.399736666 V_{ds})}) \\
& + .2876733169e-14 \ln(1. + e^{(26.06920000 + 22.62800000 V_{ds})}) \\
& - .2876733169e-14 \ln(e^{(26.06920000 + 22.62800000 V_{ds})}) \\
& + .7132093088e-13 \ln(1. + e^{(43.25037000 + 1.779343333 V_{ds})}) \\
& - .7132093088e-13 \ln(e^{(43.25037000 + 1.779343333 V_{ds})}) \\
& + .1186064148e-10 \ln(e^{(-2.523542000 - .3707966666e-1 V_{ds})}) \\
& - .2996408447e-11 \ln(1. + e^{(-4.328400000 + 2.390350000 V_{ds})}) \\
& + .2996408447e-11 \ln(e^{(-4.328400000 + 2.390350000 V_{ds})}) \\
& - .2338380655e-13 \ln(1. + e^{(-5.227000000 + .4868300000 V_{ds})}) \\
& + .2338380655e-13 \ln(e^{(-5.227000000 + .4868300000 V_{ds})}) \\
& + .1885754339e-13 \ln(1. + e^{(44.25544000 - .4509133333 V_{ds})}) \\
& - .1885754339e-13 \ln(e^{(44.25544000 - .4509133333 V_{ds})}) \\
& + .3328951874e-11 \ln(1. + e^{(4.328290000 - 2.399736666 V_{ds})}) \\
& - .3328951874e-11 \ln(e^{(4.328290000 - 2.399736666 V_{ds})}) \\
& - .6946080049e-13 \ln(1. + e^{(45.53228000 + 1.881573333 V_{ds})})
\end{aligned}$$

$$\begin{aligned}
& + .1248698553\text{e-}11 \ln(1. + e^{(3.440109000 + 10.94040000 V_{ds})}) \\
& - .1248698553\text{e-}11 \ln(e^{(3.440109000 + 10.94040000 V_{ds})}) \\
& + .1756300754\text{e-}13 \ln(1. + e^{(16.88926000 + 2.198376666 V_{ds})}) \\
& - .1756300754\text{e-}13 \ln(e^{(16.88926000 + 2.198376666 V_{ds})}) + .1119339788\text{e-}10 \\
& + .7995284200\text{e-}11 V_{gs}
\end{aligned}$$

Calculation of the nonlinear gate-to-source charge, $Q_{ds}(V_{gs}, V_{ds})$.

The nonlinear drain-to-source capacitance $C_{ds}(V_{gs}, V_{ds})$ is given by:

$$\begin{aligned}
C_{ds} := & .1183792800\text{e-}11 + \frac{.7721571000\text{e-}11}{1.0 + e^{(2.673884000 - 5.198290000 V_{gs} + 2.064933333 V_{ds})}} \\
& - \frac{.7509959600\text{e-}14}{1.0 + e^{(1.904769000 + 2.018570000 V_{gs} - .5175099999 V_{ds})}} \\
& - \frac{.9996472200\text{e-}12}{1.0 + e^{(-3.833662000 + 2.361380000 V_{gs} + .2513613333 V_{ds})}} \\
& - \frac{.3184924600\text{e-}11}{1.0 + e^{(-2.229202000 - 1.773430000 V_{gs} + 1.176580000 V_{ds})}} \\
& + \frac{.1108681860\text{e-}11}{1.0 + e^{(-3.011174000 - 1.728710000 V_{gs} + 1.237370000 V_{ds})}} \\
& - \frac{.1703679120\text{e-}10}{1.0 + e^{(1.148798000 - 1.920680000 V_{gs} + 1.139550000 V_{ds})}} \\
& + \frac{.3914567800\text{e-}11}{1.0 + e^{(-1.938878000 - 2.122520000 V_{gs} + 1.406903333 V_{ds})}} \\
& - \frac{.2003810380\text{e-}11}{1.0 + e^{(3.500087600 - 5.040070000 V_{gs} - .2678853333 V_{ds})}}
\end{aligned}$$

Integrating the capacitance w.r.t. V_{gs} with the appropriate limits of integration gives the drain-to-source charge as follows:

$$\begin{aligned}
Q_{ds} := & .1485405970\text{e-}11 \ln(e^{(9.951490000 + 2.064933333 V_{ds})}) + .1183792800\text{e-}11 V_{gs} \\
& - .4233317890\text{e-}12 \ln(1. + e^{(-7.139594000 + .2513613333 V_{ds})}) \\
& + .4233317890\text{e-}12 \ln(e^{(-7.139594000 + .2513613333 V_{ds})}) \\
& - .3720435556\text{e-}14 \ln(1. + e^{(-.921229000 - .5175099999 V_{ds})}) \\
& + .3720435556\text{e-}14 \ln(e^{(-.921229000 - .5175099999 V_{ds})}) \\
& - .1485405970\text{e-}11 \ln(1. + e^{(9.951490000 + 2.064933333 V_{ds})})
\end{aligned}$$

$$\begin{aligned}
& - .6413347872e-12 \ln(1. + e^{(-.590980000 + 1.237370000 V_{ds})}) \\
& + .6413347872e-12 \ln(e^{(-.590980000 + 1.237370000 V_{ds})}) \\
& + .1795912215e-11 \ln(1. + e^{(.253600000 + 1.176580000 V_{ds})}) \\
& - .1795912215e-11 \ln(e^{(.253600000 + 1.176580000 V_{ds})}) \\
& + .8870187225e-11 \ln(1. + e^{(3.837750000 + 1.139550000 V_{ds})}) \\
& - .8870187225e-11 \ln(e^{(3.837750000 + 1.139550000 V_{ds})}) \\
& + .1485405970e-11 \ln(1. + e^{(2.673884000 - 5.198290000 V_{gs} + 2.064933333 V_{ds})}) \\
& - .1485405970e-11 \ln(e^{(2.673884000 - 5.198290000 V_{gs} + 2.064933333 V_{ds})}) \\
& - .1844301962e-11 \ln(1. + e^{(1.032650000 + 1.406903333 V_{ds})}) \\
& + .1844301962e-11 \ln(e^{(1.032650000 + 1.406903333 V_{ds})}) \\
& + .3975759027e-12 \ln(1. + e^{(10.55618560 - .2678853333e-1 V_{ds})}) \\
& - .3975759027e-12 \ln(e^{(10.55618560 - .2678853333e-1 V_{ds})}) \\
& + .3720435556e-14 \ln(1. + e^{(1.904769000 + 2.018570000 V_{gs} - .5175099999 V_{ds})}) \\
& - .3720435556e-14 \ln(e^{(1.904769000 + 2.018570000 V_{gs} - .5175099999 V_{ds})}) \\
& - .4233317890e-12 \ln(e^{(-3.833662000 + 2.361380000 V_{gs} + .2513613333 V_{ds})}) \\
& + .4233317890e-12 \ln(1. + e^{(-3.833662000 + 2.361380000 V_{gs} + .2513613333 V_{ds})}) \\
& - .1795912215e-11 \ln(1. + e^{(-2.229202000 - 1.773430000 V_{gs} + 1.176580000 V_{ds})}) \\
& + .1795912215e-11 \ln(e^{(-2.229202000 - 1.773430000 V_{gs} + 1.176580000 V_{ds})}) \\
& + .6413347872e-12 \ln(1. + e^{(-3.011174000 - 1.728710000 V_{gs} + 1.237370000 V_{ds})}) \\
& - .6413347872e-12 \ln(e^{(-3.011174000 - 1.728710000 V_{gs} + 1.237370000 V_{ds})}) \\
& - .8870187225e-11 \ln(1. + e^{(1.148798000 - 1.920680000 V_{gs} + 1.139550000 V_{ds})}) \\
& + .8870187225e-11 \ln(e^{(1.148798000 - 1.920680000 V_{gs} + 1.139550000 V_{ds})}) \\
& - .1844301962e-11 \ln(e^{(-1.938878000 - 2.122520000 V_{gs} + 1.406903333 V_{ds})}) \\
& + .1844301962e-11 \ln(1. + e^{(-1.938878000 - 2.122520000 V_{gs} + 1.406903333 V_{ds})}) \\
& + .3975759027e-12 \ln(e^{(3.500087600 - 5.040070000 V_{gs} - .2678853333e-1 V_{ds})}) \\
& - .3975759027e-12 \ln(1. + e^{(3.500087600 - 5.040070000 V_{gs} - .2678853333e-1 V_{ds})}) \\
& + .1657309920e-11
\end{aligned}$$

Calculation of the nonlinear gate-to-drain charge, $Q_{gd}(V_{gs}, V_{ds})$.

The nonlinear gate-to-drain capacitance $C_{gd}(V_{gs}, V_{ds})$ is given by:

$$\begin{aligned}
 C_{gd} := & -2.975989352e-12 - \frac{.1027013592e-11}{1.0 + e^{(3.226760000 + 1.283650000 V_{gs} - .3395733333 V_{ds})}} \\
 & + \frac{.1528137798e-11}{1.0 + e^{(5.833342000 - 2.014920000 V_{gs} - .7508333333 V_{ds})}} \\
 & + \frac{.1535551578e-11}{1.0 + e^{(-1.899785000 + 4.201800000 V_{gs} + .1413816667 V_{ds})}} \\
 & - \frac{.8952375960e-12}{1.0 + e^{(-.371898800 - .5987470000 V_{gs} - .4569733333 V_{ds})}} \\
 & - \frac{.5725693842e-12}{1.0 + e^{(-2.312052000 + .1447450000 V_{gs} + 1.460586667 V_{ds})}} \\
 & + \frac{.2791879695e-11}{1.0 + e^{(2.152148000 - 1.538070000 V_{gs} - .7312866666 V_{ds})}} \\
 & + \frac{.4447392543e-11}{1.0 + e^{(1.184506000 - 2.658300000 V_{gs} + .2371913333 V_{ds})}} \\
 & - \frac{.3057600612e-11}{1.0 + e^{(1.069199000 - 1.910740000 V_{gs} - .5282966666 V_{ds})}}
 \end{aligned}$$

Integrating the capacitance w.r.t. V_{gs} with the appropriate limits of integration gives the gate-to-drain charge as follows:

$$\begin{aligned}
 Q_{gd} := & -.1815183766e-11 \ln(e^{(2.152148000 - 1.538070000 V_{gs} - .7312866666 V_{ds})}) \\
 & + .1815183766e-11 \ln(1. + e^{(2.152148000 - 1.538070000 V_{gs} - .7312866666 V_{ds})}) \\
 & - .1673021308e-11 \ln(e^{(1.184506000 - 2.658300000 V_{gs} + .2371913333 V_{ds})}) \\
 & + .1673021308e-11 \ln(1. + e^{(1.184506000 - 2.658300000 V_{gs} + .2371913333 V_{ds})}) \\
 & + .1600218037e-11 \ln(e^{(1.069199000 - 1.910740000 V_{gs} - .5282966666 V_{ds})}) \\
 & - .1600218037e-11 \ln(1. + e^{(1.069199000 - 1.910740000 V_{gs} - .5282966666 V_{ds})}) \\
 & + .1495185105e-11 \ln(e^{(-.371898800 - .5987470000 V_{gs} - .4569733333 V_{ds})}) \\
 & - .1495185105e-11 \ln(1. + e^{(-.371898800 - .5987470000 V_{gs} - .4569733333 V_{ds})}) \\
 & - .3955710969e-11 \ln(e^{(-2.312052000 + .1447450000 V_{gs} + 1.460586667 V_{ds})}) \\
 & + .3955710969e-11 \ln(1. + e^{(-2.312052000 + .1447450000 V_{gs} + 1.460586667 V_{ds})}) \\
 & + .8000729108e-12 \ln(1. + e^{(3.226760000 + 1.283650000 V_{gs} - .3395733333 V_{ds})}) \\
 & - .7584111518e-12 \ln(e^{(5.833342000 - 2.014920000 V_{gs} - .7508333333 V_{ds})})
 \end{aligned}$$

$$\begin{aligned}
& + .7584111518\text{e-}12 \ln(1. + e^{(5.833342000 - 2.014920000 V_{gs} - .7508333333 V_{ds})}) \\
& + .3654508968\text{e-}12 \ln(e^{(-1.899785000 + 4.201800000 V_{gs} + .1413816667 V_{ds})}) \\
& - .3654508968\text{e-}12 \ln(1. + e^{(-1.899785000 + 4.201800000 V_{gs} + .1413816667 V_{ds})}) \\
& - .8000729108\text{e-}12 \ln(e^{(3.226760000 + 1.283650000 V_{gs} - .3395733333 V_{ds})}) \\
& - .3654508968\text{e-}12 \ln(e^{(-7.782305000 + .1413816667 V_{ds})}) \\
& + .7584111518\text{e-}12 \ln(e^{(8.654230000 - .7508333333 V_{ds})}) \\
& - .7584111518\text{e-}12 \ln(1. + e^{(8.654230000 - .7508333333 V_{ds})}) \\
& + .8000729108\text{e-}12 \ln(e^{(1.429650000 - .3395733333 V_{ds})}) \\
& - .8000729108\text{e-}12 \ln(1. + e^{(1.429650000 - .3395733333 V_{ds})}) \\
& - .1600218037\text{e-}11 \ln(e^{(3.744235000 - .5282966666 V_{ds})}) \\
& + .1600218037\text{e-}11 \ln(1. + e^{(3.744235000 - .5282966666 V_{ds})}) \\
& + .1673021308\text{e-}11 \ln(e^{(4.906126000 + .2371913333 V_{ds})}) \\
& - .1673021308\text{e-}11 \ln(1. + e^{(4.906126000 + .2371913333 V_{ds})}) \\
& + .1815183766\text{e-}11 \ln(e^{(4.305446000 - .7312866666 V_{ds})}) \\
& - .1815183766\text{e-}11 \ln(1. + e^{(4.305446000 - .7312866666 V_{ds})}) \\
& + .3654508968\text{e-}12 \ln(1. + e^{(-7.782305000 + .1413816667 V_{ds})}) \\
& - .1495185105\text{e-}11 \ln(e^{(.4663470000 - .4569733333 V_{ds})}) \\
& + .1495185105\text{e-}11 \ln(1. + e^{(.4663470000 - .4569733333 V_{ds})}) \\
& + .3955710969\text{e-}11 \ln(e^{(-2.514695000 + 1.460586667 V_{ds})}) \\
& - .3955710969\text{e-}11 \ln(1. + e^{(-2.514695000 + 1.460586667 V_{ds})}) - .4166385093\text{e-}12 \\
& - .2975989352\text{e-}12 V_{gs}
\end{aligned}$$

Obtaining the nonlinear output conductance, $g_{ds}(V_{gs}, V_{ds})$.

The output conductance is given by:

$$\begin{aligned}
 g_{ds} := & -0.5670746438 + \frac{1.282051950}{1.0 + e^{(2.604740000 - 1.355050000 V_{gs} + .3895000000e-1 V_{ds})}} \\
 & - \frac{.2980638751e-1}{1.0 + e^{(-4.809786000 - 7.169320000 V_{gs} + .7722999999 V_{ds})}} \\
 & + \frac{.8691668358}{1.0 + e^{(1.745498500 + .2380800000 V_{gs} + .3158450000e-1 V_{ds})}} \\
 & + \frac{.6195600192}{1.0 + e^{(4.46224200 + 3.356730000 V_{gs} + 1.991516666 V_{ds})}} \\
 & + \frac{.4118302173}{1.0 + e^{(-3.407814000 - 1.654810000 V_{gs} - .6434933333 V_{ds})}} \\
 & + \frac{1.822725388}{1.0 + e^{(1.949294800 - .1989380000 V_{gs} + 2.316073333 V_{ds})}} \\
 & + \frac{.3459144530}{1.0 + e^{(5.163292000 - 1.714890000 V_{gs} - .2498426666 V_{ds})}} \\
 & - \frac{.7787578005}{1.0 + e^{(2.24654800 + 1.820370000 V_{gs} + 2.705116666 V_{ds})}}
 \end{aligned}$$