A C-Band Compact High Power Active Integrated Phased Array Transmitter Module Using GaN Technology

By

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Abstract

In this research, an innovative phased array antenna module is proposed to implement a high-power, high-efficient and compact C-band radio transmitter. The module configuration, which can be integrated into front-end circuits, was designed as planar layers stacked up together to form a metallic cube. The layers were fabricated by using a Computer Numerical Control (CNC) milling machine and screwed together. The antenna parts and the amplifier units were designed at two opposite sides of the cube to spread the dissipated heat produced by the amplifiers and act as a heat sink. Merging the antenna parts with the amplifier circuits offers additional advantages such as decreasing the total power loss, mass, and volume of the transmitter modules by removing the extra power divider and combiner networks and connectors between them as well as reducing the total signal path.

To achieve both a maximum possible radiation efficiency and high directivity, the aperture waveguide antenna was selected as the array element. Four antenna elements have been located in a cavity to be excited equally and the cavity is excited through a slot on its underside so a compact subarray is formed. Antenna measurements demonstrated a 15.5 dBi gain and 20 dB return loss at 10 % fractional bandwidth centered around 5.8 GHz and with more than 98% radiation efficiency. The total dimensions of the subarray are approximately 8*12*4 cm^3.

The outcoming signal from the amplifiers is transferred into the slot exciting the subarray through a microstrip-to-waveguide transition (MWT). A novel and robust MWT structure was designed for the presented application. The MWT was also integrated with a microstrip coupler to monitor the power from the amplifier output. The measured insertion loss of the MWT along with the microstrip coupler was less than 0.25 dB along with more than 20 dB return loss within the same bandwidth of the subarray. The microstrip coupler shows 38 dB of coupling and more than 48 dB of isolation with negligible effects on the amplifier output signal and the insertion/return loss of the MWT.

The amplifier subcomponents consist of power combiners/dividers (PCDs), high power amplifiers (HPAs) and bias circuitry. A Monolithic Microwave Integrated Circuit (MMIC) three-stage HPA was designed in a commercially available 0.15 um AlGaN/GaN HEMT technology provided by National Research Council Canada (NRC) and occupies an area of 4.7*3.7 mm^2. To stabilize the HPA, a novel inductive degeneration technique was successfully used. To the best of the author's knowledge, this is the first time this technique has been used to stabilize HPAs. Careful considerations on input/output impedances of all HEMTs were taken into account to prevent parametric oscillations. Other instability sources, i.e. odd-mode, even-mode,

and low frequency (bias circuit) oscillations were also prevented by designing the required stabilization circuits. The electromagnetic simulation of the HPA shows 35 W (45.5 dBm) of saturated output power, 26 dB large signal gain and 29% power added efficiency within the same operating bandwidth as the subarray. The output distortion is less than 27 dB, indicating that the HPA is highly linear. The PCD was designed by utilizing a novel, enhanced configuration of a Gysel structure implemented on Rogers RT-Duroid5880. The insertion loss of the Gysel is less than 0.2 dB while return loss and isolation are greater than 20 dB over the entire bandwidth. The same subarray area (8*12 cm^2) has been used for the amplifier circuits and up to eight HPAs can be included in each module. All the above parts of the transmitter module were fabricated and measured, except the MMIC-HPA.

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List of Acronyms

2-D	Two Dimensional
3-D	Three Dimensional
3dB-BW	Three Decibel-Beamwidth
3D-EM	Three Dimensional Electromagnetic
5G	Fifth Generation
ADS	Advanced Design System
AlGaN	Aluminum Gallium Nitride
BeO	Beryllium Oxide
cm	centimeter
CNC	Computer Numerical Control
CO	Coupling
CPU	Center processor unit
CST	Computer Simulation Technology
CW	Continues wave
dB	Decibel
dBi	Decibel isotropic
dBm	Decibel milli
DC	Direct Current
DI	Directivity
DRC	Design Rule Check
fF	femto Farad
FNBW	First Nulls Beamwidth
FSLL	First Side Lobe Level
EM	Electromagnetic
GaAs	Gallium Arsenide
GA	Genetic Algorithm
GaN	Gallium Nitride
GHz	Giga Hertz
HEMT	High Electron Mobility Transistor
HFSS	High Frequency Structural Simulator
HPA	High Power Amplifier
HPBW	Half Power Beam Width
IEEE	Institute of Electrical and Electronic Engineers
IL	Insertion Loss
IMN	Input Matching Network
I/O	Input/Output
IS	Isolation
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LNA	Low Noise Amplifier
LRL	Line- Reflect-Line
LS	Large Signal
kW	Killo Watt
MAG	Maximum Available Gain
MC	Microstrip Coupler
MESFET	Metal- Semiconductor Field-Effect Transistor
MHz	Mega Hertz

MMIC	Monolithic Microwave Integrated Circuit
MMIC-HPA	Monolithic Microwave Integrated Circuit-High Power Amplifier
MMN	Middle Matching Network
MPT	Microwave Power Transmitting
MSG	Maximum Stable Gain
MWT	Microstrip-to-Waveguide Transition
MWT&MC	Microstrip-to-Waveguide Transition& Microstrip Coupler
nH	nano Hanry
NRC	National Research Council Canada
OMN	Output Matching Network
PA	Power Amplifier
PCB	Printed Circuit Board
pHEMT	P-channel High Electron Mobility Transistor
PMN	Prea-input Matching Network
mA	milli Amper
mm	millimeter
mW	milliwatt
mΩ	milliOhm
PAE	Power Added Efficiency
PCD	Power Combiner Divider
RL	Return Loss
RF	Radio Frequency
RADAR	RAdio Detection And Ranging
SiC	Silicon carbide
SIW	Substrate Integrated Waveguide
SLL	Side Lobe Level
SOLT	Short-Open-Load-Through
SPDT	Single-Pole Dual-Through
SSPA	Solid-State Power Amplifier
TFC	Thin Film Capacitor
TFR	Thin Film Resistor
THD	Total Harmonic Distortion
TRL	Through-Reflect-Line
TWT	Travelling-Wave Tube
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Ratio
W	Watt
WCA	Waveguide-to-Coaxial Adapter
WLAN	Wireless Local Area Networks
μm	micrometer
$\frac{1}{sq}$	per square

Chapter 1

Introduction

1.1 Introduction

In this research, a high-power, high-efficiency and compact size transmitter module is proposed. Each part of the transmitter module was designed with new ideas as well as these parts are combined together with an innovative scheme. The amplifiers were designed with GaN technology that is new and reliable as well. The demand for high power transmitters has risen considerably but their design remains complex; it is even more challenging when high efficient miniaturized modules are needed. Microwave transmitters are working in different frequency ranges from about 1 GHz to 100 GHz. There are different technologies and techniques available to design the transmitters at different frequency bands.

1.2 Motivations and background

In today's communications systems, there are many applications requiring high-power, high-efficiency transmitters implemented onto a small footprint and with minimum cost. All these criteria, i.e. power, efficiency, size and cost, cannot be improved simultaneously and trade-offs are usually needed to best reach the desired values. For example, when the output power is the most important criterion, efficiency and size will be usually sacrificed to achieve the highest power. Therefore, producing such transmitters to meet all the mentioned specifications is a serious requirement for the industry. This challenge has motivated researchers to design high-power, high-efficiency and compact transmitters by presenting new concepts, techniques and technologies. The transmitters considered here are to be utilized in RADAR systems, base-stations of mobile communication and aerospace or satellite sites. Thus, the proposed design must be robust enough for long-term use and easy to assemble for future maintenance.

This motivation leads the researcher to select the AlGaN/GaN HEMT technology. In the last decade, GaN has proven to provide more power density and power added efficiency (PAE) in comparison with other available technologies such as GaAs and SiC. Several Microwave Monolithic Integrated Circuit (MMIC) High Power Amplifiers (HPAs) have been designed and reported recently [1]. These HPAs can provide up to 40 W output power and 40% PAE for frequencies up to the K-band. These achievements have not been matched by any other competing technology. Presenting novel combining networks [2] by RF/microwave designers has resulted in more powerful and more efficient solid-state power amplifiers (SSPAs). The SSPAs can work in both continuous wave (CW) and pulsed-mode, which is a worthwhile advantage over the Travelling-Wave Tube (TWT) amplifiers.

Also, designing high-directive and high-efficient antenna and array implemented in a compact, low-weight and durable structure is one of the most challenging topics for antenna researchers and designers. To achieve a high directive antenna, the antenna surface must be enlarged. Therefore, finding the methods that can increase the antenna gain while keeping a compact size is always an interesting challenge for antenna designers. The proposed methods to overcome this challenge usually sacrifice other features of the antenna performance such as radiation efficiency.

An additional motivation for carrying this research is on the difficulties in integrating and assembling the antenna with active circuitry, particularly for robust, reliable, long-term use. Feeding an antenna array with 1,000 elements or even more by a mighty power amplifier is not at all efficient. A large portion of the produced power will be dissipated in distributing networks. Therefore, designers are motivated to employ active integrated antenna arrays. In this way, each element or group of elements has its own power amplifier. The drawbacks of this technique is that connecting the antenna elements to their active circuitry will increase the configuration complexity due to the required wiring and cooling systems. More importantly, in long-term use, the active circuits will need regular maintenance and repairing. Accordingly, special type of connectors must be used so that different parts of the transmitter can be assembled or separated easily and quickly without degrading their performance for a long time. This issue will be more critical when the high power must be delivered to the antenna. Hence, in this thesis a novel structure is proposed that significantly resolve the problem of assembling the antenna with active circuitry in the active integrated antenna array.

In this research, all the essential elements of a transmitter (Antenna, power amplifier, power combiner/divider networks and connections) were designed making use of novel and unique concepts to satisfy these requirements driven by industrial applications. Furthermore, a highly suitable configuration is proposed to integrate the parts as a compact transmitter module.

Microwave frequency range has been divided into different bands as mentioned in Table 1-1. Lower frequency bands, mostly L and S, are used for longer range transmission due to lower free space loss. However, higher frequency bands, mostly K and Ka, are used for high-resolution detection (in RADAR applications) and for high-rate and wide-band data transferring (in SAT-com and mobile radio communications). Transmitters and receivers can be implemented in a smaller size at higher frequency bands that causes lower cost. However, producing high power transmitters will be more difficult by increasing the frequency as well as their performance are more sensitive to the weather conditions. For example, meteorological RADARs are mainly designed in three different bands [3], [4]. S-band weather RADARs operate between 2.7 to 2.9 GHz to detect heavy rain at the range up to 300 km. C-band weather RADARs operate between 5.6 to 5.65 GHz to detect the rain at the range up to 200 km and can provide a good compromise between range, resolution, accuracy and cost. X-band weather RADARs operate between 9.3 to 9.5 GHz and are used for short-range observation up to 50 km; they are more accurate than S or C-bands. The typical peak power of a transmitter in pulse mode with a duty cycle of about 0.1 % [3] for S-band weather RADAR is 750 kW, for C-band is up to 270 kW and for X-band is from 100 W to 25 kW.

Table 1-1: Microwave frequency range

band	L	S	C	X	Ku	K	Ka	U	E
Frequency (GHz)	1 to 2	2 to 4	4 to 8	8 to 12	12to 18	18 to 26.5	26.5 to 40	40 to 60	60 to 90

Therefore, a transmitter designed at C-band can provide good accuracy and/or resolution as well as it can be employed for long-range applications. C-band communication satellites often use the frequency range from 5.92 to 6.42 GHz for their up-links. The frequency range for C-band weather RADARs is from 5.25 to 5.72 GHz, but most of them fall within the 5.6 to 5.65 GHz range [3], [4]. Synthetic Aperture RADARs (SAR) use the frequency range of 5.3 GHz to 5.4 GHz while C-band military RADARs usually use 5.25 to 5.92 GHz. Also, the IEEE 802.11a standard allocates the frequency range from 5.15 to 5.72 GHz to Wireless Local Area Networks, WLAN. Microwave Power Transmitting, MPT, has recently demonstrated applications to transfer the solar power collected by a satellite to a power station on the earth [5]. ISM bands (Industrial, Scientific and Medical) i.e. 2.45 GHz [6] or 5.8 GHz [7]-[10] are used for the MPT application with 3 % bandwidth. 5G mobile radio communication is moving to higher frequencies, particularly at 5.8 GHz, in order to send more data at faster rates. Accordingly, the proposed transmitter is designed at 5.8 GHz to support many of the applications operating at this frequency range. To achieve a transmitter that can be used for all aforementioned applications, the transmitter and all its parts is designed for more than 10% fractional bandwidth.

1.3 Objectives

The proposed transmitter module was designed at 5.8 GHz and it covers at least 10% fractional bandwidth of all defined parameters for each part of the transmitter. This large bandwidth is wide enough for all the mentioned applications and the designed transmitter will be suitable for all those applications.

In RADAR applications, the transmitter and receiver antenna is usually the same but for the applications such as satellite and MPT, the transmitter and the receiver use separate antennas. To achieve a high directive antenna, there are two options, dish or any kinds of reflector antenna and phased array (Fig. 1-1). Reflector antennas are too bulky for the desirable criteria and need mechanical equipment to rotate the beam and scan the space so they are not energy efficient. Phased arrays can provide very small Side Lobe Level (SLL) and Half Power Beam Width (HPBW) and very high directivity [9], [11].

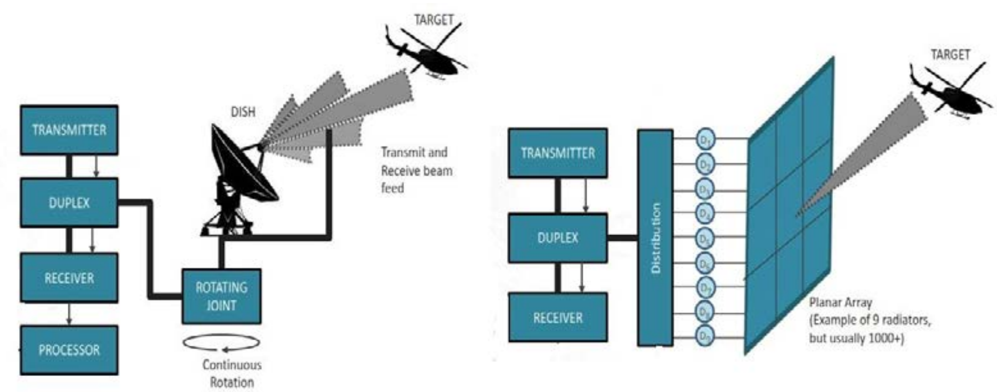


Fig. 1-1: Reflector and phased array Antenna [12]

In this research, the most important feature for choosing the array elements was the radiation efficiency thus, all microstrip-based antenna configurations structures [13], [14] are ignored. In fact, because of dielectric and surface wave losses, any configuration of microstrip antennas is not usually able to provide radiation efficiency beyond 70% in practice [15]-[17]. Some techniques have been reported to improve the radiation efficiency of microstrip antennas i.e. using Dielectric Resonator Antenna (DRA) [15] or Genetic Algorithm (GA) [18], [19] but they are not robust enough or easy to implement in a compact array. Radiation efficiency will be worsened when microstrip antennas are configured into an array due to the loss added by the dividing network [16], [20] and [21].

Slot array antennas have widely been used among the metallic structure of antennas [11]. They can provide higher radiation efficiency than microstrip array antennas, about 80 % [22]. They are also a suitable structure for millimeter wave frequencies [23]. The major drawback with slot antennas is the mutual coupling [24], [25] and difficulties to produce high gain antenna, which often requires multiple slots thus leading to larger array.

To achieve an antenna with more than 95 % radiation efficiency and very high directivity, both aperture and horn antennas were considered. The major issue regarding these configurations is their size. They are usually massive and difficult to fulfill in arrays. Cavity-backed waveguide aperture antenna [26] is a good solution to reduce the size. This technique is also applicable to the slot antennas [27], [28]. This technique has been used for different frequencies from Ku-band to U-band or even E-band [29]-[31]. Therefore, this configuration was adopted for the antenna in the proposed transmitter module at the C-band. In this research, many modifications were added to this structure so that it can be efficiently merged with active circuits as well as to improve the antenna radiation performance. Some techniques were also applied to design a compact structure and manufacture it properly.

The most important part of a transmitter module, to accomplish simultaneous high power and high-efficiency transmitters, is the High Power Amplifier (HPA). There are several technologies available to implement the HPAs. A complete list of monolithic integrated-circuit technologies is presented in Table 1-2 [32]. LDMOS has demonstrated to be the most suitable technology to achieve HPAs at L-band and S-band because they can provide the larger power in comparison with other technologies [33], [34]. Transistors fabricated in AlGaN/GaN are ideal for high power and high-efficiency operation due to their high break-down voltage, high saturated electron drift velocity and high thermal conductivity [35]. GaN HEMTs also offer greater power density and wider bandwidths. One of the drawbacks of AlGaN/GaN HEMTs is their relatively low values of the electron and hole mobility, which limits the use of these transistors for higher millimeter frequencies.

Table 1-2: Comparison of monolithic integrated-circuit substrates [32]

Technology Property	Silicon	SiC	GaAs	InP	GaN
Semi-insulating	No	Yes	Yes	Yes	Yes
Resistivity (Ω-cm)	10^3-10^5	$>10^{10}$	10^7-10^9	$\sim10^7$	$>10^{10}$
Dielectric constant	11.7	9.7	12.9	14	8.9
Electron mobility (cm^2/Vs)	1450	500	8500	4000	800
Saturation electrical velocity (cm/s)	$9*10^6$	$2*10^7$	$1.3*10^7$	$1.9*10^7$	$2.3*10^7$
Radiation hardness	Poor	Excellent	Very good	Good	Excellent
Density (g/cm^3)	2.3	3.1	5.3	4.8	6.1
Thermal conductivity (W/cm-°C)	1.45	3.5	0.46	0.68	1.3
Operating temperature (°C)	250	>500	350	300	>500
Energy gap (eV)	1.12	2.86	1.42	1.34	3.39
Breakdown field (kV/cm)	≈300	≥ 2000	400	500	≥5000

In this research, a MMIC-HPA was designed in the 150 nm AlGaN/GaN HEMT technology provided by National Research Council (NRC) of Canada. The HPA proposed here was designed as a three-stage amplifier. To achieve at least 30 W output power with a small area of HPA, eight 8×100μm cells were designated to form the output stage. Because the input power of the HPA must not exceed 25 dBm to saturate the HPA, the HPA was designed to provide a large signal gain, greater than 20 dB. Because the HPA may be used as a satellite transmitter, the linearity of the HPA was enhanced by careful design of the matching networks and the addition of harmonic suppressors to the matching networks.

The initial simulations of the HEMTs from the available design kit showed that they are prone to oscillation, particularly parametric oscillations. Because the conventional stabilization methods were not able to stabilize the HPA properly, a new technique was presented and utilized. Careful investigation was also performed to verify the stability of the HPA in different situations. The maximum number of the HPAs in each transmitter module is eight but alternative arrays of 1, 2 or 4 elements can be also employed in each module when an array with non-uniform amplitude distribution is needed.

Combining the HPAs was carried out using a microstrip board. The Gysel structure was used as a microstrip power combiner. High power load resistors, with large size, can be embedded in this structure. Low insertion loss with the same power division over a wide bandwidth are other advantages of this structure. Some modifications have been also fulfilled to create a more compact configuration with better performance.

A compact and low loss microstrip-to-waveguide transition (MWT) was designed and presented. The MWT was creatively equipped by a microstrip coupler to monitor the output power from the HPAs going to the Antenna. This technique not only has removed the coupler insertion loss from the HPA outputs but also it is needless from the extra space for microstrip coupler.

1.4 Objectives summary

Based on the aforementioned specifications of the proposed transmitter module (with more than 10% fractional bandwidth of 5.8 GHz), the objectives of this thesis are summarized as follow:

- Designing an antenna with the following features:
    - nearly 100% radiation efficiency,
    - greater than 20 dB return loss (to provide approximately 100% total efficiency),
    - must have the capability to be employed as an element in a large array,
    - must have the capability to be fed effectively and easily particularly when utilized in an array,
    - must be robust for long-term and outdoor (or even aerospace) applications,
    - must be very compact so, its aperture efficiency must be greater than 75% and its height must be considerably smaller than other available antennas,
    - must exhibit very high directivity so that a planar array of the designed antenna with the aperture size of 10 times of the wavelength by 10 times of the wavelength can provide about 30 dBi gain.
- Designing a MMIC-HPA with the following features:
    - more than 45 dBm (31.5 W) saturated output power,
    - designed in small die, less than 25 mm^2,
    - greater than 25% efficiency,
    - completely stable against the different kinds of oscillations in both large and small-signal regimes,
    - more than 20 dB large signal gain, so that the input power must be less than 25 dBm to get 45 dBm output power,
    - about 30 dB of total harmonic distortion (THD) at saturation where 45 dBm output power is produced.
- Designing a microstrip-to-waveguide transition (MWT) with the following features:

- insertion loss must be less than 0.3 dB,
- return loss must be greater than 20 dB,
- must be very compact,
- must be compatible with the transmitter module to provide an easy and robust connection between the RF-circuits and the antenna.

- Designing a power monitor system with the following features:
  - greater than 20 dB return loss,
  - less than 0.1 dB insertion loss,
  - very compact,
  - about 40 dB coupling,
  - about 10 dB directivity.
- Designing the required microstrip power combiner/dividers (PCD) with the following features:
  - all the designed PCDs must be very compact,
  - their load resistors must be large enough to tolerate the unbalance power in the worst case,
  - insertion loss must be less than 0.2 dB,
  - return loss of all ports must be greater than 20 dB,
  - isolation between splitting ports must be more than 15 dB,
  - the splitting ports must be approximately of equal phase and amplitude; the phase and amplitude difference between the splitting ports must be less than 3^{o} and 0.05 dB, respectively.

Based on the above requirements, the transmitter module must have the following capabilities:

- must be robust for long-term and outdoor applications,
- energy efficient and cost effective,
- easy to fabricate, assemble and maintain,
- Low-profile and compact.

1.5 Research Contributions

- *Proposing and demonstrating an innovative stabilization technique for the HPAs by using the degeneration inductor*.

Degeneration inductor is commonly used to match the input impedance of low noise amplifiers to their optimum noise impedance. In this research, degeneration technique was successfully utilized for the first time to stabilize the HPAs. Conventional stabilization methods are either unable to stabilize the available HEMTs or will significantly degrade the HPA performance. Commercially available HEMTs are highly prone to parametric oscillations and the degeneration inductor proved to be the best available technique to prevent this type of oscillations. To assure stability, the real part of the input impedance of the transistors was considered at different input powers, up to saturation, as well as for the entire frequency bandwidth.

- *A 35 W 3-stage MMIC HPA was proposed and designed using a 0.15 um AlGaN/GaN HEMT technology, fitted in a compact size of 4.7*3.7 mm^2.*

  The entire layout was simulated by Keysight ADS momentum. Although the HPA was biased in class-AB with 30% power added efficiency, the HPA is highly linear so that the output voltage and current are nearly the same as their inputs. The linearity of the HPA is due to its designed matching networks and utilizing the third harmonic suppressor.

- *A new modified Gysel structure is presented along with its efficient design algorithm.*

  Designing the low loss power combiner/divider (PCD) is very critical on the overall efficiency of a transmitter module that combines many power amplifiers. The fabricated prototypes demonstrated that the modified Gysel exhibits very low loss. In comparison with standard PCDs, which typically have 0.5 dB insertion loss, the proposed Gysel PCD can decrease the total insertion loss by about 1 dB in a module including eight parallel amplifiers. To achieve the smallest possible combining network, three different configurations of the modified Gysel PCDs as well as one compact Wilkinson PCD were designed for different locations of the combining network. The Gysel PCD at the final stage was designed for the 100 W load resistor with the size of 6*6 mm^2. This size of high power resistor cannot be embedded into a standard Wilkinson PCD.

- *An efficient and innovative structure of MWT was developed to excite the antenna.*

  The proposed structure is very compact and with very low loss. The MWT was implemented as a planar-layered structure, which is suitable for implementation using CNC machines. Assembling and/or separating the antenna and active circuitry from each other is, therefore, more convenient.

- *To save space as well as adding no more loss to the signal path, a microstrip coupler was merged with the proposed MWT making use of novel ideas developed in this research.*

  For long term use and easy maintenance, the performance of the transmitter modules must be always monitored. This was achieved by using a $\frac{\lambda}{4}$ open-ended microstrip line available in the

MWT. By this way, there is no extra space required for the coupler as well as the coupler does not affect the MWT performance.

- *A novel antenna configuration was designed and implemented.*
  The proposed antenna has been designed as a subarray consisting of four waveguide apertures mounted in a cavity. To improve the antenna gain (up to 15 dBi) and return loss (up to 20dB), the size of apertures was increased to slightly larger dimensions in three steps by using an original scheme. The waveguide height connected to the antenna input port was reduced (to one third of its standard value), using novel techniques developed in this research, to achieve a compact structure. The proposed antenna achieves close to 100% radiation efficiency, making it an excellent candidate for high efficiency applications. The proposed antenna can be effectively employed in the arrays, as a subarray, to increase the gain. Planar arrays with different amplitude/phase distribution were designed and simulated by employing the proposed antenna. A uniform amplitude/phase distribution array with 5*5 elements is capable of providing 29 dBi gain, making this array suitable for high directive applications e.g. MPT, tracking RADAR and aerospace applications. Notwithstanding its high gain (15.5 dBi), the antenna size is very compact (8*12*4 cm^3) in comparison with a horn antenna with the same aperture size (8*12 cm^2) and electrical features at the desirable frequency range. In fact, the height of the proposed antenna (4 cm) is approximately 20% of that of the horn antenna. Comparison with commercial products [36]-[38] demonstrates the advantages of this antenna. Indeed, the referred devices show about 15dBi gain with almost the same aperture area but with a return loss of about 10 dB, i.e., a radiation efficiency less than 90%. Furthermore, the length of those antennas is about 5 times of the proposed antenna. Finally, the gain flatness of the designed antenna is much better than the one of the referred products.

A complete list of published and/or submitted papers is listed below,

1- **M. Gholami**, M. C. E. Yagoub; "New Compact E-Plane Microstrip-to-Waveguide Transition with Slotted Ground Plane Coupling", *Microwave and Optical Technology Lett.*, Vol. 56, No.3, pp. 615-619, 2014.

2- **M. Gholami**, R.E. Amaya and M.C.E. Yagoub, "Low-loss compact power combiner for solid state power amplifiers with high reliability", *IET, Microwave, Antennas & Propag.*, Vol. 10, No. 3, pp. 310-317, 2015.

3- **M. Gholami**, R.E. Amaya and M.C.E. Yagoub, "Improved Meandered Gysel Combiner/Divider Design with Stepped-Impedance Load Line for High-Power Applications", *Progress in Electromagnetics Research C*, Vol. 70, PP. 53-62, 2016.

4- **M. Gholami**, R.E. Amaya and M.C.E. Yagoub, "Compact High-Gain High-Efficiency Cavity Backed Aperture Antenna", *submitted to Trans. on Antenna and wave propag.*.

5- **M. Gholami**, R.E. Amaya and M.C.E. Yagoub, “A Novel Compact structure of Integrated Microstrip-to-waveguide Transition with microstrip coupler”, *in preparation.*
6- **M. Gholami**, R.E. Amaya and M.C.E. Yagoub, “A 35 W AlGaN/GaN MMIC High Power Amplifier with New stabilization technique at C-Band”, *in preparation*.

1.6 Thesis Outline

In the next chapters, each part of the proposed transmitter module is explained separately. In each chapter, an exhaustive review of the literature is presented, the proposed structure is presented with its novelty and originality in its design. The accurate simulation and/or measurement results are also presented and will compare if applicable. This thesis is structured as follows,

Chapter 2 deals with the design of the MMIC HPA. The biasing classes of the amplifiers and different kinds of oscillation along with the stabilization schemes are briefly reviewed. A systematic design procedure is presented and employed to design the proposed HPA. The techniques used to stabilize the HPA as well as the simulation results are also presented.

In chapter 3, the structure of the combining network is practiced. In this chapter, Gysel power combiner/divider will be examined. In chapter 4, first, an original microstrip-to-waveguide transition is presented then an innovative configuration is proposed to merge the presented microstrip-to-waveguide transition with a microstrip coupler.

In chapter 5 after a short review of aperture waveguide antenna and planar arrays, the designed antenna is proposed. The simulation results, obtained by various simulators, are compared with measurement results of the antenna. In addition, different sizes of antenna array are simulated and the simulation results are presented.

Chapter 2

High power amplifier design

2.1 Introduction

One of the most challenging parts in designing a transmitter is the power amplifier and even more challenging when the power amplifier block is expected to simultaneously work at both high-power and high-efficiency [39]. In this chapter, a short review of the AlGaN/GaN HEMTs technology is first presented. Then, transistors classes of operation based on biasing conditions are briefly introduced, the effects of possible undesired oscillations examined, and stabilization techniques presented. Afterward, a step-by-step design procedure is detailed and the obtained simulated results discussed.

2.2 MMIC-HPA

The use of Microwave Monolithic Integrated Circuit (MMIC) High Power Amplifiers (HPAs) is rapidly growing in radio communication systems. They lead to lower weights and smaller size transmitters as well as the ease and cost-saving of mass production volumes in contrast with other bulky devices such as Travelling-Wave Tube (TWT) amplifiers. Many applications mentioned in chapter 1, i.e. Sat-com, active phased antenna arrays in RADARs, 5G mobile radio communications, Microwave Power Transmission (MPT) trend to utilize MMIC HPA. MMIC-HPAs can also be effectively combined to make Solid-State Power Amplifiers (SSPAs) [40], [41]. All aforementioned applications operate in the C-band, centered around 5.8 GHz.

Recently, several HPAs have been reported on various GaN foundries and operating in different frequency ranges. To compare these products, a few state-of-the-art MMIC HPAs mostly operating in the C-band were reviewed. Qorvo (Triquint) has released two die MMIC HPAs. TGA2578 and TGA2590 fabricated by 0.25 μm GaN on SiC process with 30 W saturated power and 40% PAE. The both products cover most of the C-band frequencies [42]. Triquint has also released two new packaged MMIC HPAs, TGA2576-(FS and 2-FL), with 40 W saturated power and 35% PAE [42]. In addition, the latest MMIC generation of HPAs presented by Cree, i.e. CMPA5585025D, fabricated by 0.25 μm GaN on SiC, is suitable for the upper half of the C-band, with 40% PAE and about 40 W saturated power [43]. By using 0.25 μm GaN HEMT process of United Monolithic Semiconductors (UMS), [44], [45], [46] and [47] have reported 20 W, 40 W, 40 W, and 50 W HPA, respectively, with more than 40% PAE. MMIC GaN HPAs described in [48]-[50] have been published without mentioning the producer foundry. MMIC GaN HPA in [49] reported a 52% PAE and 46 dBm saturated power. At the other frequency bands, valuable designs have also been reported such as in [51], fabricated by Fraunhofer IAF with 0.25 μm AlGaN/GaN HEMTs at K-band, that can provide 10 W power and 30 % PAE. A survey of GaN foundry and GaN future can be found in [52]. The features of referred HPAs are summarized in Table 2-1.

Table 2-1: State-of-the-art of GaN-based MMIC-HPAs at C-band

Ref.	Frequency (GHz)	Power (dBm)	PAE (%)	Large Signal Gain (dB)	Size (mm^2)	Size of cells
[42]	2-6	45	40	22	6.4*5	**8*250um/150nm**
[43]	5.5-9	46	40	22	3.7*4.8	**?*?/250nm**
[45]	5-5.8	46	41	22	4.5*4	**?*?/250nm**
[46]	5.4-6.1	46	36	17	3.8*3.9	**6*200um/250nm**
[47]	5.2-6	48	46	20	4.7*3.8	**8*250um/250nm**
[48]	3.6-4	50	64	10	15.2*14.3	**6*200um/?nm**
[49]	5.2-6.8	46	52	22	3.3*3.8	**6*200um/250nm**
[50]	5-6	47.8	40	25	3.2*5.3	**8*100um/150nm**
This work	**5.4-6.1**	**45**	**28**	**26**	**4.7*3.7**	**12*210um/250nm**

2.3 AlGaN/GaN HEMTs technology

GaN technology is the most suitable process to design power amplifiers due to its features in comparison with other available technologies. Compared to commonly used semiconductor materials (Table 2-2 [35]), GaN exhibits high breakdown voltage, which allows large drain voltages to be used. In fact, high breakdown voltage causes higher doping voltage and denser device, which results in higher power density in the device as well as increased transconductance, power gain, transition frequency f_T (the frequency for which the short-circuit current gain h_{21} is equal to 1), and maximum oscillation frequency f_{max} (the frequency for which the maximum available power gain is equal to 1) [35].

Table 2-2: Material properties of common microwave semiconductors [35]

Property	Units	Silicon	GaAs	4H-SiC	GaN
Bandgap	EV	1.11	1.43	3.2	3.4
Breakdown field	V/cm	$7*10^5$	$7*10^5$	$35*10^5$	$35*10^5$
Saturation velocity	Cm/sec	$1*10^7$	$1*10^7$	$2*10^7$	$1.5*10^7$
Saturation field	V/cm	$8*10^3$	$3*10^3$	$25*10^3$	$15*10^3$
Thermal conductivity	W/cm-K	1.5	0.46	4.9	1.7/substrate
Electron mobility	Cm^2/V-sec	1350	6000	800	1000
Hole mobility	Cm^2/V-sec	450	330	120	300

The thermal conductivity of a semiconductor material relates to its capability of removing the heat generated from unconverted DC power. GaN on SiC substrate has the biggest thermal conductivity. Bandgap determines the upper-temperature limit of device operation. Higher temperature operation makes possible to design the transistor smaller and denser that will withstand the heat it generates under bias [35].

The frequency performance, e.g. f_T, of a device is mainly determined by the electron velocity. The electric field at which electron velocity saturates, saturated field, is also important. It determines how quickly the charge carriers can be accelerated to their saturation values. GaN on SiC offers the largest value for both parameters resulting in devices with higher knee voltages and moving the optimal performance to higher voltage levels [35]. The high saturated drift velocity leads to high saturation current densities and larger watts per unit gate periphery. In turn, this leads to lower capacitances per watt of output power. Low output capacitance and drain-to-source resistance per watt also make GaN HEMTs suitable for switch-mode amplifiers [53].

The electrical conductivity of the device substrate is a very important material property for higher frequency operation of RF transistors. AlGaN/GaN HFET fabricated on semi-insulated SiC have much better microwave performance than other substrates [35].

These attractive features in amplifier applications, enabled by its superior semiconductor properties, make the GaN-based HEMT a very promising candidate for microwave power applications [1].

However, one of the limitations of AlGaN/GaN, related to wide bandgap semiconductors, is the relatively low values of electron and hole mobility in these materials. Low mobility results in increased parasitic resistance, increased losses, and reduced gain. Fortunately, the electron mobility in a 2D-gas in an AlGaN/GaN heterostructure typically remains close to 1000 cm^2/Vs, which is almost close to SiC. The hole mobility in both SiC and GaN is very low and it severely limits the use of p-type SiC in RF transistors that are intended for operation above about 1 GHz [35].

2.4 Transistors classes of operation

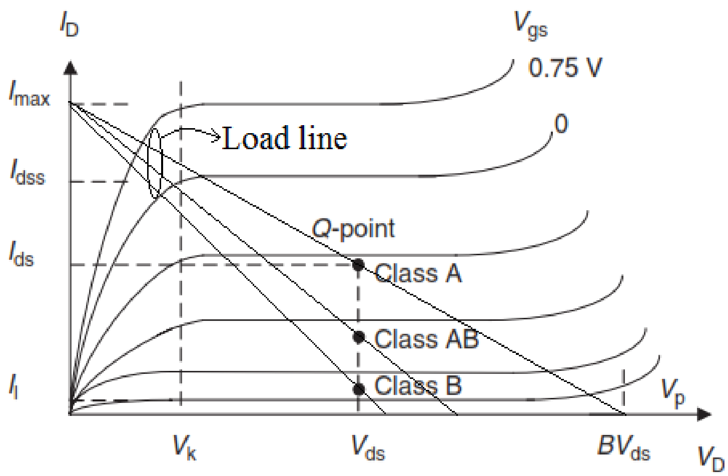
There are many resources in the literature describing RF/Microwave amplifier classes such as A, B, AB, C, D, E, and F [54], [55]. These classes are implemented by selecting proper transistor bias conditions and designing the input/output matching networks to meet the system requirements in terms of noise figure, output power, efficiency (or DC power consumption), linearity conditions (modulation schemes), frequency range, size, and cost. The main difference between classes is the conduction angle of the amplifier, determined by the bias point (Fig. 2-1.a and .b).

In class-A, the quiescent point is selected approximately at the center of the I-V curves and the linear output power is maximized by properly selecting the load match. The class-A amplifier is designed essentially as a small-signal linear amplifier and has the same characteristics in that the output signal is an amplified replica of the input signal. In a small-signal amplifier, the transistor is usually conjugately matched at the input and output for maximum gain and good input and output VSWR. A class-A power amplifier differs from a small-signal amplifier in the power level. The class-A amplifier can be designed to operate in saturation by properly selecting the output match for the device [56].

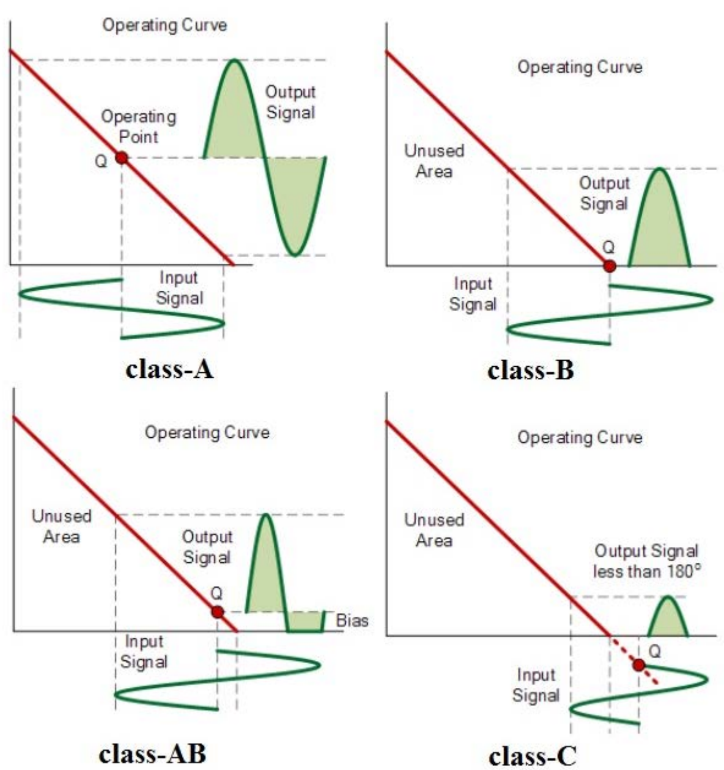
In the case of Class-B, the Q-point is set at the cut-off of the device current (at pinch-off, with negligible current without the RF signal). The load match is designed to obtain the best gain, maximum output power, and maximum efficiency. Single-ended Class-B amplifiers have poor linearity performance. At RF, Class-B amplifiers are usually realized in push–pull configurations (two single-ended stages). However, the linearity characteristics are not as good as for the class A due to the nonlinear transition between the two stages during a full RF cycle [56].

In class-AB, the Q-point current is 5% to 30% of the total device current depending on the frequency of operation, noise figure, efficiency, and linearity requirements. This class is commonly used in single-ended power amplifiers and has higher efficiency than class A and better linearity than class B [56].

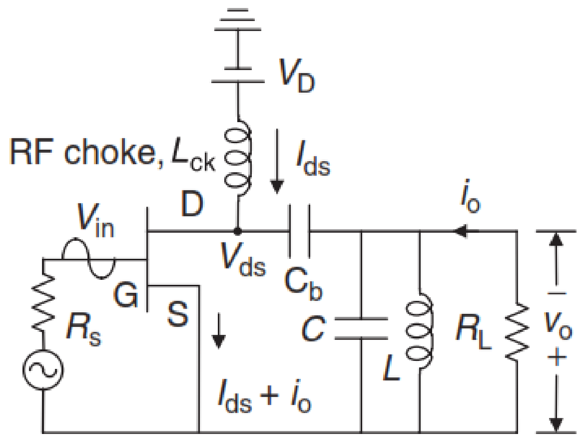
In a Class-C amplifier, the Q-point is set well below the cut-off point of the device current. These amplifiers are highly nonlinear because of producing large amplitude harmonics which leads the output waveform is quite different from the input signal. The bias topology for class-A, -B, -AB and –C is almost the same, as shown in Fig. 2-1.a.



(a) Output I-V curve of a FET, Imax: drain peak current, I_{dss}: drain-source saturated current, Ids: drain-source bias current, I_1: leakage current, V_{gs}: gate-source voltage, V_{ds}: drain-source voltage, V_D: drain supply voltage, BV_{ds}: drain-source break down voltage, V_p: pinch off voltage and V_k: knee voltage [56]



(b) Input and output voltage waveforms for different classes [57]



(c) A simple typical bias topology for a FET in class-A, -B, -AB and C

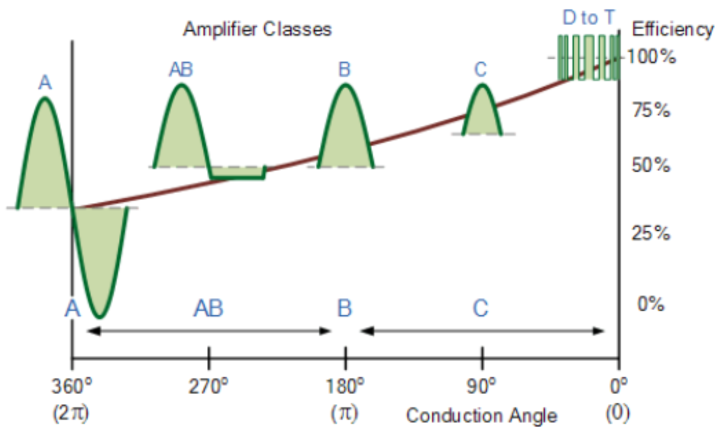
Fig. 2-1: Comparison between class-A, -B, -AB and -C

Class-D, -E, and -F amplifiers work as a switch. They must provide very low resistance in the "ON" state and very high impedance in the “OFF” state with respect to the load impedance value. In this case, the voltage and current waveforms at the output show a 180 phase difference. If the ON resistance is negligible, there is no power dissipation in the device, and if the OFF impedance is very large, there is no current flow through the device [56]. The power amplifier’s efficiency as a function of its conduction angle for different classes of operation is shown in Fig. 2-2.

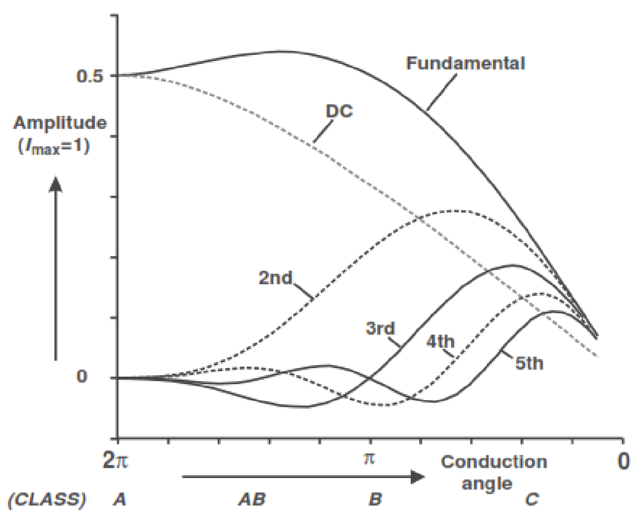
The transistor classes of operation discussed so far can all be “inverted,” which means that the current and voltage waveforms could be reversed. For example, an inverted Class B mode consists of a device having a sinusoidal current waveform and a half-wave rectified voltage waveform [58].

In the Class-F amplifier configuration, the reduced power dissipation is achieved by employing an impedance matching technique (such as resonant circuits) to terminate harmonic frequencies in desired loads. In a Class-F amplifier, the efficiency is improved by using output matching networks using multiple resonators to control the harmonic power levels and shape the drain voltage and/or drain current waveforms [59]. In an ideal design, at the device output, all even harmonics are short-circuited to reproduce a half-sine-wave current waveform while the odd harmonics are open circuited to shape the output voltage to a square wave. Class-F amplifiers, in particular, are currently of interest since they appear to be feasible at microwave frequencies. A Class-F amplifier is designed in essentially the same way as a class-AB/B amplifier, except that the output circuit is designed to present a short circuit to the second harmonic and an open circuit to the third harmonic.

In practice, often only the short at the second harmonic is employed due to the difficulty in designing suitable matching circuits over extremely wide bandwidths [56]. Fig. 2-3 shows a simple circuit topology for the class-F amplifier. In a multistage amplifier, harmonic termination can also be selected.



(a) Conducted waveform and efficiency versus conduction angle reduction [57]



(b) Different harmonics level versus conduction angle reduction [32]

Fig. 2-2: Comparison of different classes in terms of reduction of conduction angle

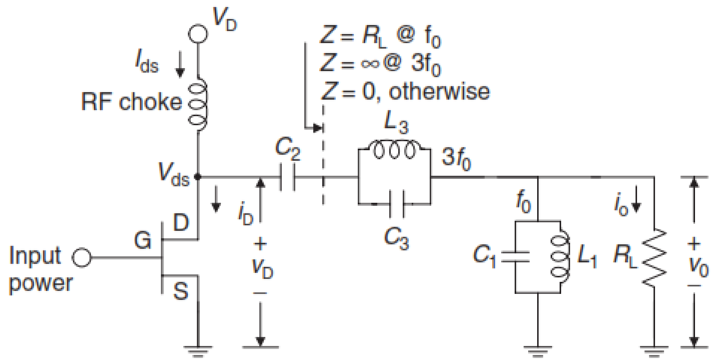


Fig. 2-3: Simple typical Class-F circuit topology [56]

To design a Class-F power amplifier, the input is matched for maximum gain (conjugately matched). The transistor is biased almost the same way as in class-B/AB, $V_o = \frac{9}{8}V_{ds}$ and $I_o = \frac{I_{max}}{2}$, and the load resistance is obtained by $R_L = \frac{V_o}{I_o} = \frac{9}{4}\frac{V_{ds}}{I_{max}}$. The parallel L_1, C_1 network (shunt) is resonant at f_0 and the parallel L_3, C_3 network (series) is resonant at the third harmonic $3f_0$. Capacitor C_2 is a blocking capacitor and can also be used as matching element [56].

2.5 Oscillations and stabilization techniques

The design should be unconditionally stable and also odd-mode, parametric, and low-frequency oscillation conditions must be prevented [60]. At microwave frequency unavoidable parasitics are often sufficient to cause oscillation if care is not taken in the design and fabrication of the amplifier. Oscillation may occur at frequencies that do not propagate out the amplifier because they are filtered or blocked by bias capacitors or matching networks. It is not unusual for microwave amplifiers to oscillate anywhere between 1 MHz and 30 GHz or higher [60]. Once an oscillation has been identified, it is usually not difficult to correct it in many cases at a slightly lower gain. In most microwave systems, conditional stability is usually acceptable in the frequency band where component impedances are defined. The main oscillation sources in MMIC HPA are even-mode, odd-mode, parametric, and low frequency (bias).

Any device, which is not unconditionally stable, can give rise to even-mode oscillations. This occurs when the device is connected between the input/output matching networks or bias networks. The oscillation can be examined by using two-port S-parameters through calculating the stability factor, K, and stability measurement, B.

In a multistage amplifier, internal transistors are terminated by passive matching networks followed by active devices, which can give rise to negative resistance. A series of stable two-amplifier stages will be stable, but if additional feedback (e.g. biasing circuitry) is introduced, the new circuit must also be analyzed. Even-mode oscillations can happen even without applying a RF/microwave signal [60]. Even-mode oscillations can be prevented by using stabilization circuits such as the one depicted in Fig. 2-4.

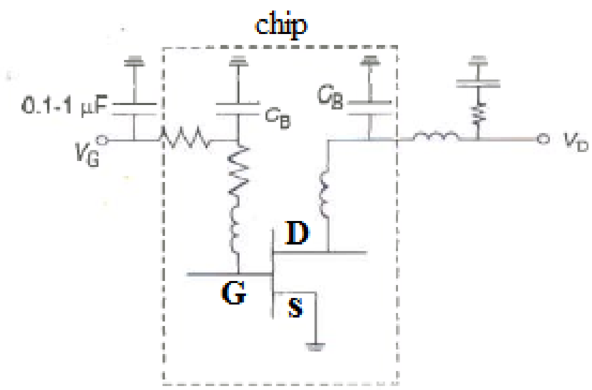


Fig. 2-4: Stabilization scheme for even-mode oscillations [60]

The major source of odd-mode oscillations in a MMIC PA is the matching networks, which may provide different impedance values for the input/output of the paralleled transistors due to coupling between circuit elements and T- or cross-junctions. Thus, the paralleled transistors in the PA may not necessarily see the same match and accordingly, different RF voltage levels are developed at the gate/drain locations of the paralleled transistor. This leads to negative resistance or odd-mode oscillations. These oscillations are also called parallel transistor oscillations [60]. The frequency of oscillations is usually in the operating band; so to minimize the possibility of odd-mode oscillation, a resistor, called isolation resistor, must be connected between gate feeds as well as drain feeds (Fig. 2-5). The value of the isolation resistor is generally between 10 to 50 ohms [60]. This resistor can damp out these oscillations.

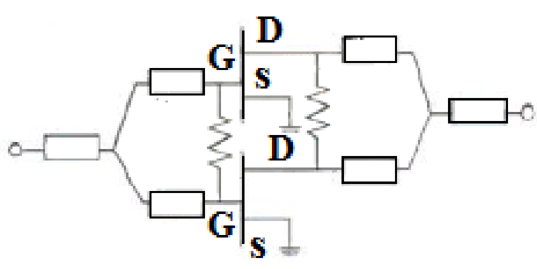


Fig. 2-5: Stabilization scheme for odd-mode oscillations [60]

When transistors are driven in a nonlinear region, a parametric subharmonic oscillation occurs due to pumping of a nonlinear reactance by RF voltage at a multiple of the oscillation frequency (In MESFETs and pHEMTs, such pumped nonlinear reactance is constituted by C_{gs} and C_{gd} [60]). In this case, a subharmonic frequency is injection-locked to the fundamental frequency, resulting in a negative resistance at the operating frequency [60]. One way to suppress the parametric oscillation is using lossy matching and biasing networks (Fig. 2-6), which switches the negative resistance at device port to a positive value.

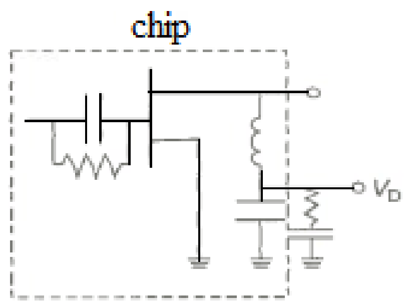


Fig. 2-6: Stabilization scheme for parametric oscillations [60]

Low frequency, or bias, oscillations are generally observed in high power amplifiers with large gate periphery devices and occur in the frequency range of 10 MHz to 50 MHz [60]. Fig. 2-7 shows effective techniques to prevent low-frequency oscillations.

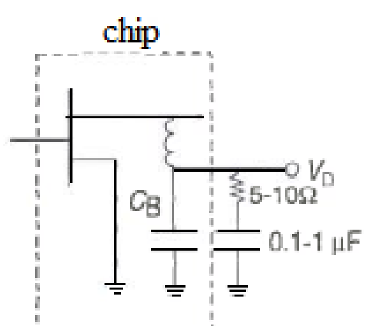


Fig. 2-7: Stabilization scheme for low frequency oscillations [60]

2.6 Design procedure of the MMIC HPA

The *first step* to design an amplifier begins by choosing the amplifier type and fabrication technology. The main reasons for choosing a particular technology are the operating frequency, the cost, and the capability to satisfy the design requirements such as maximum power density, noise figure (for LNAs), and robustness. Although the GaN/AlGaN is not as cheap as GaAs or Sic, it was chosen for this research due to its excellent electrical features as described above.

In the *second step*, the size of the transistor should be selected, i.e., the number of fingers and the gate width. The total gate width, obtained by multiplying the gate width with the number of fingers, must be determined with regards to the desired operating frequency, the output power, and the gain. The MSG (Maximum Stable Gain) and the break-point frequency of the MAG (Maximum Available Gain), where the K-factor becomes equal to unity, are shifted to higher frequency with decreasing gate length [61]. Although shorter gate width can increase the gain, it often results in lower output power. To minimize the power loss along the gate finger, the gate width should be smaller than a value that leads signal phase rotation to be smaller than $\frac{\pi}{16}$ along the gate finger [62].

The *third step* should be dedicated to transistor biasing. Small signal amplifiers (with an exception for LNAs, which are biased in class-AB) are usually implemented in Class-A. Other classes are used for power amplifiers with the trade-off between efficiency and linearity [56]. HPAs are mostly biased in Class-AB by using harmonic suppressing techniques [63]-[65] from Class-F to achieve the best linearity features, high output power, and quite a large signal gain.

In the *fourth step*, the stability of the selected transistor(s) must be examined. If a transistor is not unconditionally stable, it must be stabilized using stabilization techniques. There are several techniques reported in the literature used to stabilize a transistor [66]. The stability must be examined first by using the small signal techniques and S-parameter data [66]. Stability factor (K), and stability measurement (B), should be calculated for a very wide frequency range (i.e. from 30 MHz to 30 GHz) and must satisfy the following conditions $K > 1,\ B > 0$ [66] for unconditional stability. The input/output stability circles can also be plotted in the smith chart to obtain the impedances that ensure stability [66]. Beside the small-signal stability, large-signal stability of PAs must be examined not only before designing the matching networks but also after designing the matching networks. A transistor is stable in a large-signal mode when the real part of the input and output impedances are positive [66]. To examine this condition, the I/O impedances of the transistor must be obtained when the transistor is excited by an input power as large as 1dB-compression gain (P1dB).

The *fifth step* is designing the input/output matching networks. PAs must be applied by such an input power that can be driven into saturation while the maximum output power and Power Added Efficiency (PAE) are achieved. When large input power is applied to a transistor, nonlinear features of the transistor result in changes to its output impedance. Therefore, designing the Output Matching Network (OMN) is not possible by using the S-parameters. Thus, to find the optimum OMN, load-pull simulations must be performed. In load-pull simulations, a variable load is connected to the biased transistor and output power, gain and PAE are calculated for different values of the load. Then, these parameters are plotted as contours on the smith chart for their maximum values as well as few values smaller than their maxima. By this way, the optimum load is a point on the smith chart that is close to the center of all contours (Fig. 2-8).

The Input Matching Network (IMN) can be either similarly designed (with source pull) or using conjugated matching techniques. Note that the optimum obtained OMN must be included in the circuit before designing the IMN. Also, it can be helpful to tune the OMN by including the obtained IMN in order to achieve more precise load impedance.

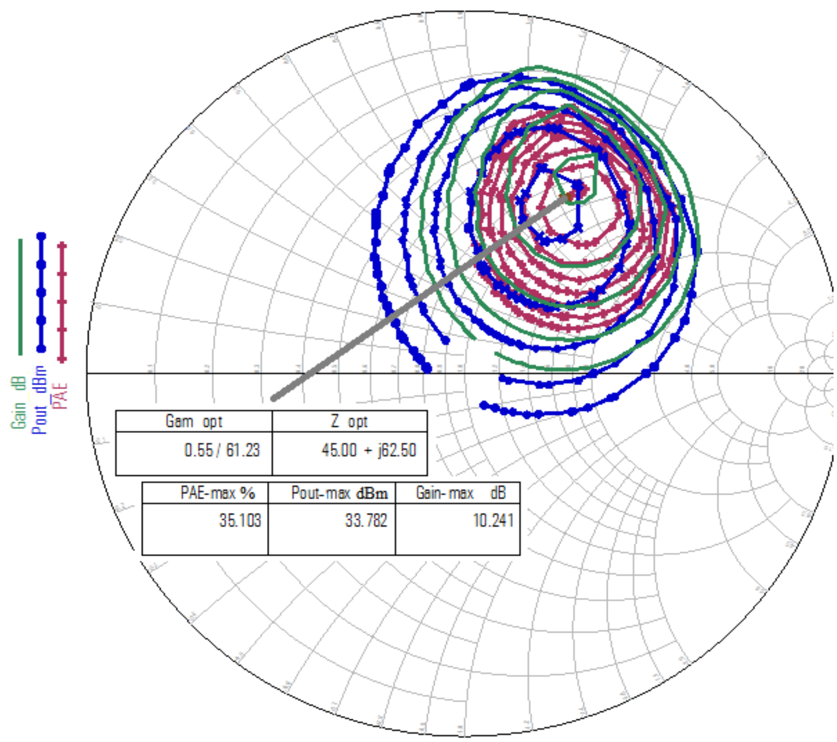


Fig. 2-8: A sample Load pull simulation graphs

In the sixth step, several transistors must be combined to provide enough power at the output along with few stages to reach acceptable gain. Therefore, power combining and cascading techniques must be used in designing a MMIC HPA. Hence in the *sixth step*, a line-up plan should be prepared for power and gain from the HPA input to the HPA output. Based on the required gain and power, the number of stages and the number of transistors per stage should be determined.

In the *seventh step*, some practical issues should be taken into account such as the amount of heat produced by the transistors due to the dissipated DC power or the heat produced by the high current flowing on the non-zero resistivity biasing lines. Thus, using through vias to circulate the heat to the ground plane or sufficiently wide strip to reduce resistivity could be ways to investigate.

In the *eighth step*, the matching networks together with biasing lines and combining/splitting networks must be designed using the optimum impedance of the transistor output obtained by load-pull simulations and the conjugate of the transistor input impedance. The Output Matching Network is the most important matching part to provide the required power. It is usually designed by either binary T-combiners [39, [44], [45] or bus-bar techniques [67]-[69]. MMIC designers use also other combiners instead of simple Tee junctions to create a balanced amplifier and improve the Input/Output (I/O) return loss. The most attractive combiner in MMIC design is the Lange coupler although the coupling arms are very thin, thus are not very suitable for very high powers [70]. MMIC HPAs are usually designed in two or three stages. Cascading more than three stages [71] may raise instability due to adding external positive feedback. Drain and gate bias lines must be included in the matching network to achieve a compact design [72], [73]. Furthermore, microstrip lines and lump elements, i.e., TFRs (Thin Film Resistors), TFCs (Thin Film Capacitors) and spiral inductors, can be used at frequencies up to the Ka-band. Different network topologies can be employed, to create a matching network between two impedances so careful consideration of the network topology will prevent designing large matching networks [74], [75].

In the ninth step, after achieving acceptable simulated performance, the layout of matching networks must be updated to achieve a compact size and wisely configuration. No ideal elements must be used, all capacitors, inductors, and resistors must be utilized from the available design kit.

In the tenth step, early design iterations of the circuits are typically performed only in schematic but as designs progress, it is always necessary to simulate the matching networks (distributed passive sections) by using an electromagnetic (EM) simulator to accurately estimate losses and include coupling effects. Many commercial microwave simulators including Keysight ADS, have the capability to simulate the layout of distributed elements using a built-in EM engine which is invoked when a simulation is executed in the schematic environment. This capability is called co-simulation. Therefore, *in this step*, the final design must be simulated by using the co-simulation technique. If the co-simulation results are not satisfactory, the designed circuit must be optimized to achieve the expected results from the co-simulation.

Finally, in the *eleventh step*, the required Pads for signal I/O and bias voltages as well as extra through vias, ground pads, and outer frame must be added to the layout and Design Rule Check (DRC) must be performed. In the case of appearing any violation of design rules, all the errors must be removed by modifying the designed layout.

2.7 Designed MMIC HPA

The proposed HPA in this chapter is appropriate and usable for most of the applications mentioned in chapter 1. The HPA is designed at 5.8 GHz and with greater than 10% fractional bandwidth. The HPA is expected to exhibit variations of less than $\pm 0.5\ dB$ in gain or power over the desirable frequency range. The maximum output power must be achieved by considering the maximum allowable chip size fixed by the foundry. The HPA gain must be large enough so that an input power of less than 25 dBm (maximum power of the signal sources) can saturate the HPA conveniently. The PAE of the HPA must be close to the PAE of a single chosen cell. The HPA must work sufficiently linear so that the output waveform of both current and voltage are the replica of their input waveforms. The HPA input/output ports must be perfectly matched to the 50 Ω source/load impedances when the HPA is derived into the large signal mode. Furthermore, the MMIC HPA must be designed as small as possible without degrading its electrical performance.

As the first step, a 0.15 μm commercial GaN process provided by NRC (National Research Council of Canada) [76] is employed to produce the Monolithic Microwave Integrated Circuit (MMIC). NRC also offers a 0.5 µm long metal Gate, a GaN500, and a 0.150 µm long metal Gate, GaN150, on silicon carbide wafers of 75 µm thickness. These processes have two metal layers, with 50 Ω/sq nichrome resistors and MIM capacitors of 0.19 fF/(µm^2). The process is capable of gold back side and through via thus using microstrip line is feasible. Some electrical features of the process are summarized in Table 2-3 [76].

Table 2-3: Major electrical features of the NRC GaN process [76]

maximum Drain voltage bias	30 V
Maximum power level	7 W/mm
Minimum Drain-source break down voltage	80 V
maximum current density	1000 mA/mm
maximum long-term operating Drain current density	350 mA/mm
Gate source voltage	between -8 to 2 V
The unity gain frequency, f_T	35 GHz
Maximum tolerable current for a track made by two layers and via between those	24 mA/μm width
Maximum operating voltage of capacitors	40 V
maximum breakdown capacitor voltage	180 V

In the second step, to achieve the maximum output power and power gain, different sizes of cell transistors were examined. Based on the details given in second step in section 2.6, for the C-band frequency, the gate width should be less than 200 μm. The performed simulations showed that 100 μm gate width can provide more gain than 150 μm or 200 μm in expense of losing a little of the output power. Eight fingers were chosen for each cell to provide maximum gain. A cell with more than eight fingers would be risky because they cannot provide the same voltage and current for all the sources of a cell. In addition, the cells with more fingers are more deficient to transfer the heat produced by dissipated power. Therefore, cells with a size of 8×100 μm were chosen. Eight cells were designated to form the output stage of the amplifier. Because lower power is required for the driver stage and also to achieve higher gain while avoiding degrading the total efficiency, a 4×100 μm HEMT cell was chosen as the driver stage.

In the third step, the HEMTs are biased in class AB with +28 V at the Drain and -3.5 V at the Gate. Drain bias voltage was chosen close to its maximum allowable value because lower drain bias voltage decreases the output power and PAE.

In the fourth step, the stability of the HEMT was first examined by S-parameter simulations when the chosen cell was biased to the desired values. A 8×100 μm single cell HEMT was stabilized by using the both schemes depicted in Fig. 2-4 and Fig. 2-6. Fig. 2-9 shows the schematic as well as the simulation results of the small-signal stability criteria and gains. To limit the gate current and improve stability, an inductor is usually used in gate bias lines [77], [78].

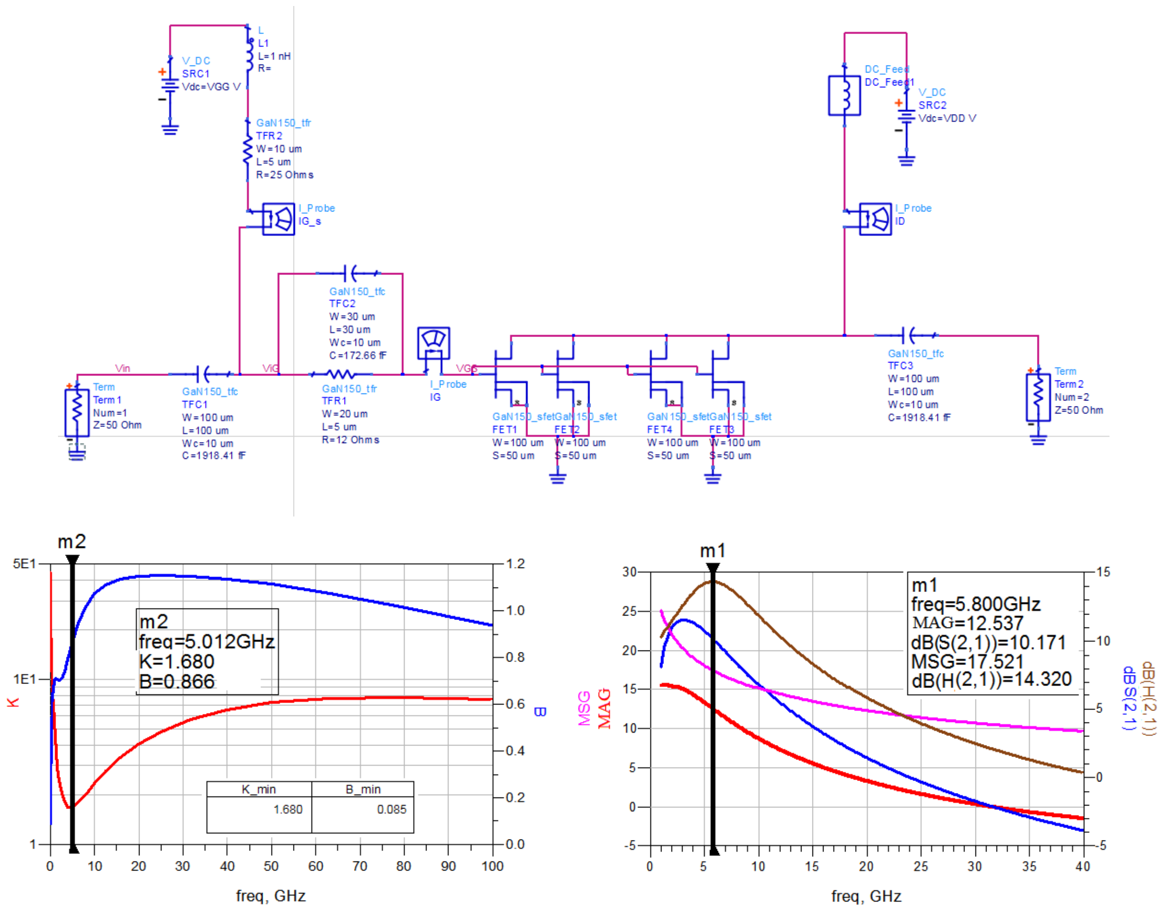


Fig. 2-9: Stabilizing circuit of the HEMT cell as an amplifier (top), and small signal stability criteria and gain features (bottom)

K is the stability factor, B is the stability measurement, MAG is the maximum available gain in dB, MSG is the maximum stable gain in dB, dB(S(2,1)) is the S_{21} in dB and dB(H(2,1)) is the h_{21} in dB versus frequency.

When the HEMT was driven into the nonlinear regime by a large-signal input, parametric oscillation was observed by performing harmonic-balance simulation. The real part of the input impedance of the HEMT became negative when the input power reached the 1dB compression point. Such situation can be avoided by using a large series resistor at the gate, but this will lead to a significant decrease of the gain.

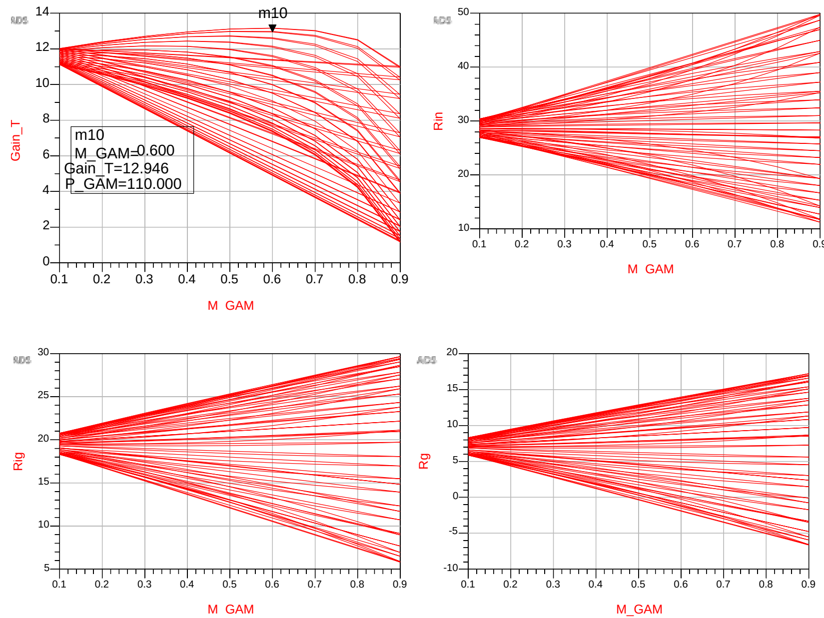
More investigations on the behavior of the available HEMTs show that this instability is happened when the HEMT is terminated with some specific load values. In other words, the oscillation happens when load value is located in some areas of the smith chart. By increasing the input power to the saturation point, the instability area is expanded and covers most of the smith chart. Therefore, not only the HEMT will be unstable under large signals (non-linear regime) but also there is no guarantee that HEMT would be stable for small signals (linear regime). In this case, the output signal would be so large that the ADS harmonic balance simulator was not able to converge.

To describe this situation more clearly, the amplifier shown in Fig. 2- 9 was simulated for different values of the load termination, and with two different values of the signal source power, i.e., 10 dBm for small signal and 25 dBm for large signal (Fig. 2-10). The input saturation power is about 27 dBm and the small signal gain (linear gain) is about 12 dB for the selected HEMT. The drain and gate biases are of 24 V and -3.5 V, respectively. Let R_{in}, R_{ig} and R_g be the real parts of the impedances at the point indicated by V_{in}, V_{iG} and V_{GS} in Fig. 2-9. Also let Gain_T be the transducer gain at the fundamental frequency, and M_GAM and P_GAM the magnitude and phase of the reflection coefficient of the load termination. Fig. 2-10.b shows that the HEMT is unstable for loads with reflection coefficient magnitude higher than 0.6 and phase between 80^o to 130^o. As aforementioned, the resistor at the gate, which is 12 Ω in Fig. 2-9, was increased to stabilize the HEMT. The minimum value of the resistor that can stabilize the HEMT is 45 Ω but as shown in Fig. 2-11 the transducer gain would be 5.5 dB which is not enough for the designed amplifier. Also, by this stabilization method, the maximum output power and PAE are of 30.5 dBm and 13.5%, respectively.

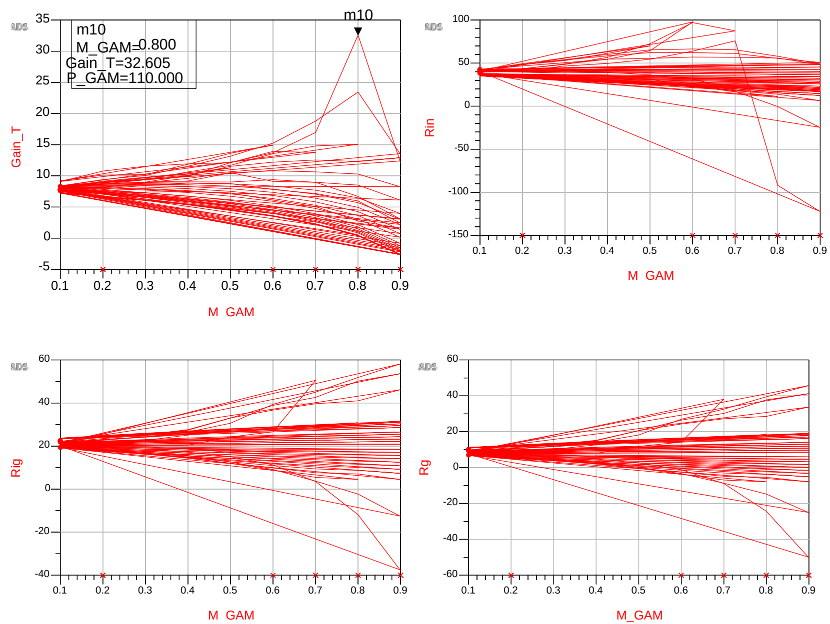
Therefore, different stabilization circuits were used to avoid oscillation [79]. However, simulations demonstrated that the stabilization schemes reported in the literature could not effectively stabilize the available AlGaN/GaN HEMT.

Finally, inductive degeneration technique was found to be the best option to stabilize the available AlGaN/GaN HEMT. Inductive degeneration techniques were formerly used in low-noise amplifiers to match the input impedance to the optimum source impedance. *To the best of our knowledge*, inductive degeneration was successfully utilized for the first time to stabilize a HPA. An inductor at the transistor source increases the real part of its input impedance with no significant degradation of the HEMT performance. Fig. 2-12 shows the proposed schematic of the stabilization circuit as well as simulation results of the small-signal stability criteria and gains.

The only adverse effect of the proposed scheme is a relatively small reduction of the maximum sweeping drain-source voltage due to the voltage drop across the inductor. Using inductive degeneration instead of connecting the transistors’ source directly to the ground is also somehow risky. In fact, utilizing inductors at transistors’ source can increase instability. That is why, traditionally, power amplifier designers would like to connect transistors’ source to ground. The stability of designed HPA were examined very carefully for both small and large-signal and for a very wide frequency range. In addition of considering the small signal criteria (stability factor and measurement), stability was examined by watching the input/output impedance of each transistor as well as each stage of the HPA for all input powers from small signal to saturation. This technique has been rarely used/reported by other designers.



(a)



(b)

Fig. 2-10: Load-pull simulation results of the HEMT shown in Fig. 2- 9

versus the magnitude of the reflection coefficient (M_GAM) of the load termination and for different phases of load reflection coefficient (P_GAM), (a) Small-signal, when the input power is 10 dBm and (b) large-signal, when the input power is 25 dBm.

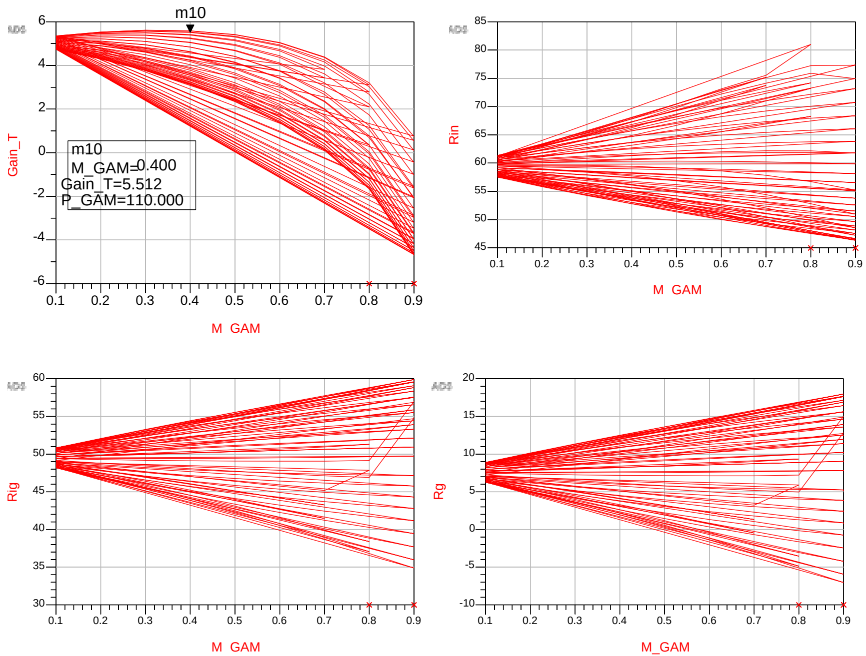


Fig. 2-11: Large-signal load-pull simulation results of the stabilized HEMT shown in Fig. 2-9.

Another issue, that must be considered carefully, is the maximum operating current flowing from source to ground through the inductors. This value must be smaller than the maximum allowable current of the employed inductors. The last issue is that inductors typically have massive layout and placing two of them for each cell needs a large area. In the designed HPA, the inductors are located at unused areas to achieve a compact design.

Two parallel inductors with values between 0.2 to 0.3 nH can adequately stabilize the 8×100µm single cell HEMT without significant degradation of the power gain. Choosing larger inductor values can produce more positive resistance at the transistor input but the gain will decrease accordingly. On the other side, choosing the inductor values close to their minimum values will make the HPA more prone to oscillations due to fabrication tolerances. So, enough margin must be taken into account to assure stability. Two parallel inductors were chosen to connect the both sides of the HEMT's source that carry the drain current to ground through source. In this way, inductors with narrower track widths can be used to withstand the maximum drain-source current. Also, the HEMT layout would be completely symmetrical and equal ground reference can be provided for all the sources in each cell (Fig. 2-13).

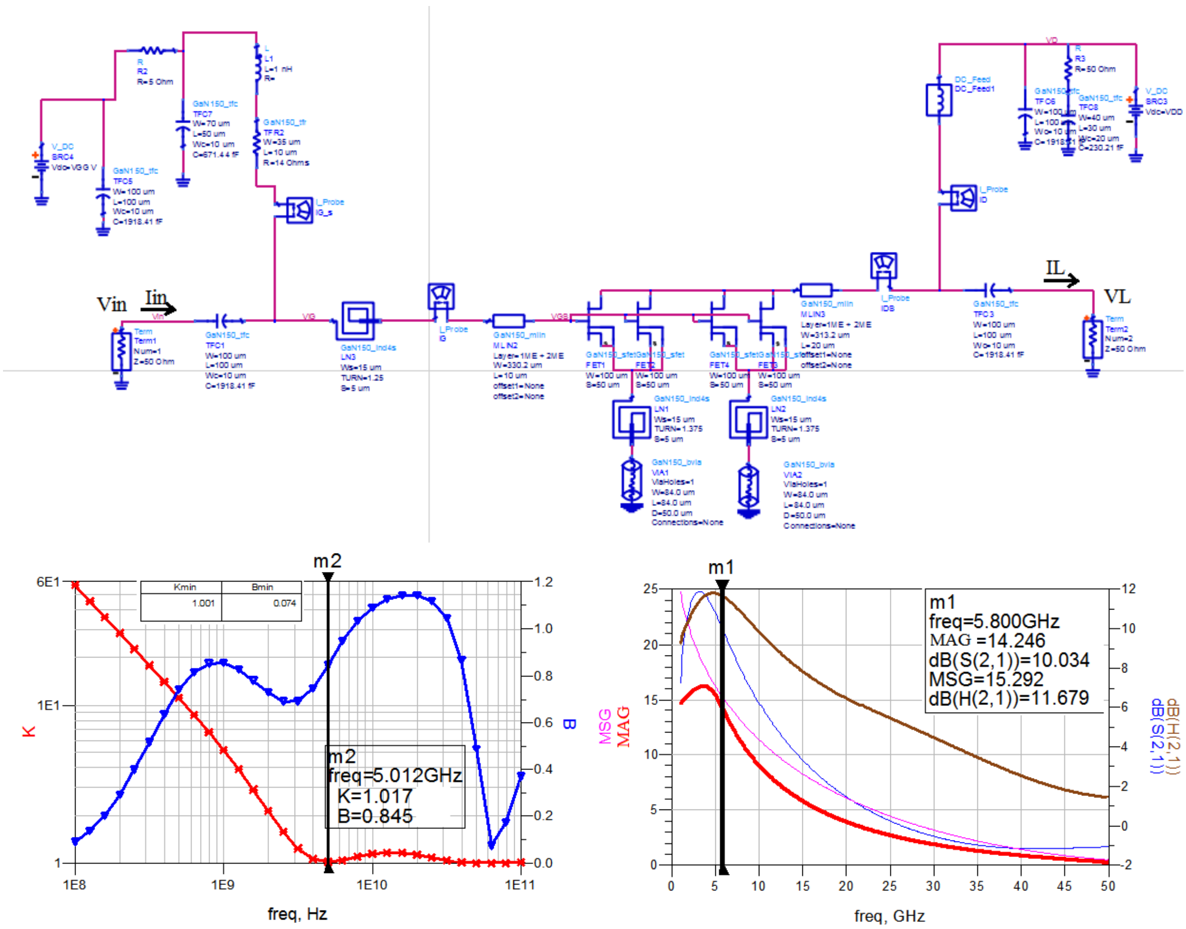


Fig. 2-12: stabilizing circuit of the HEMT cell as an amplifier (top), and small signal stability criteria and gain features (bottom), K is the stability factor, B is the stability measurement, MAG is the maximum available gain in dB, MSG is the maximum stable gain in dB, dB(S(2,1)) is the S_{21} in dB and dB(H(2,1)) is the h_{21} in dB versus frequency

The minimum value of K is very close to one but K will have enough margin from one in the final HPA design due to the extra loss added by microstrip lines in the matching networks. The enhanced stable HEMT was simulated by harmonic balance when it was undergone by a high power input signal. By optimizing the values of a series inductor at the gate and series RL at the gate bias, the parametric oscillations were effectively prevented and the input resistance of the HEMT remained positive even for very large input powers. Large-signal simulations demonstrated that the drain bias of HEMTs must not be more than 24 V for a reliable operation. Drain bias voltage bigger than 24 V will increase the risk of oscillation when the HEMTs are terminated by a load which is far from the location of the optimum load on the smith chart. However, the value of the gate bias does not have significant impact on the stability of the HEMTs. Low-frequency (bias) oscillations are also avoided in the amplifier of Fig. 2-12 by adding large capacitors parallel to the drain and gate bias supply.

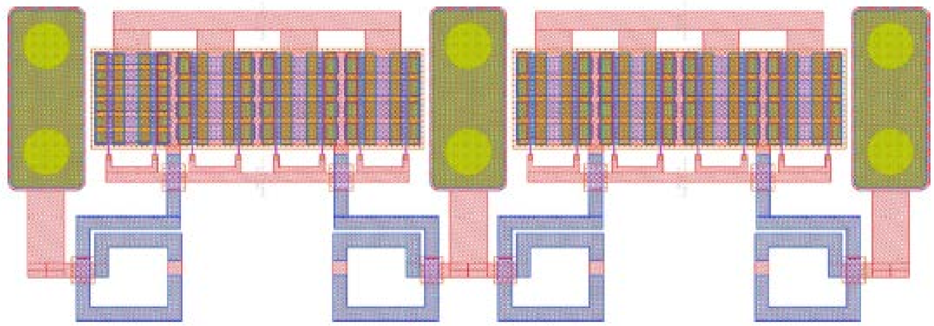


Fig. 2-13: The layout of two 8×100µm cells with degeneration inductor at the source

In the fifth step, the load-pull simulation of a single cell was performed to find the optimum output load and the large-signal (LS) gain. It must be done by taking into account all stabilization and bias circuitry. The obtained optimum output load of a 8×100µm HEMT cell was found to be about (40+j20) Ω. Fig. 2-14 displayed the harmonic balance simulation results. The cell can provide 36.5 dBm output power with 9 dB large signal transducer gain and 34% PAE when it is derived from 27.5 dBm input power and terminated to its optimum load.

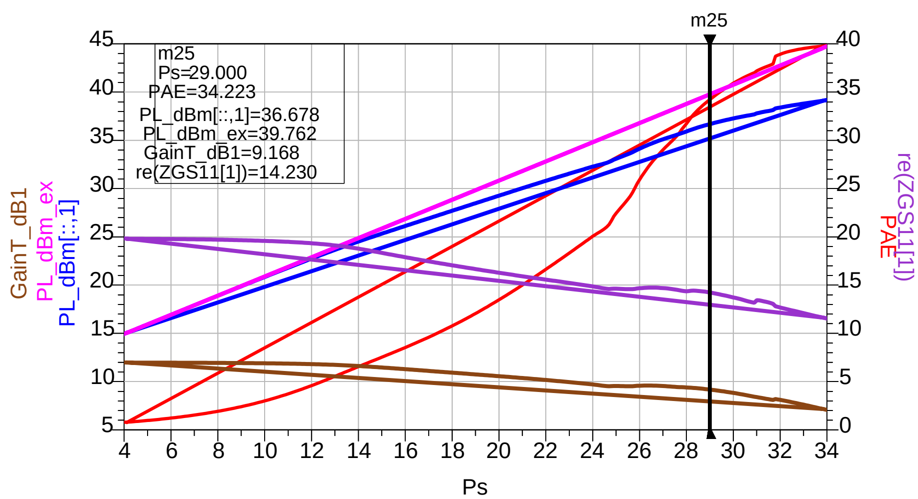


Fig. 2-14: Simulation results of a 8×100µm stabilized HEMT cell terminated by an optimum load.

Ps is the power of the signal source in dBm, PL_dBm[::,1] is the fundamental harmonic of the output power in dBm at the load, PL_dBm_ex is the virtual extension of the linear part of the output power in dBm, GainT_dBm1 is the transducer gain in dB at the fundamental harmonic, PAE is the power added efficiency in %, and re(ZGS11[1]) is the real part of transistor input impedance at the fundamental harmonic (in ohms)

In Fig. 2-14, the HEMT was simulated without the input matching network (the same as in the schematic shown in Fig. 2-12) with approximately 1.5 dB of loss between the power of the signal source (Ps) and the power available at the HEMT's gate. Fig. 2-14 also shows that the small signal transducer gain is 12 dB and the output power is 36.7 dBm at 3-dB compression gain where the input power, Ps, is 29 dBm.

The real and imaginary parts of the input impedance of the HEMT is displayed in Fig. 2-15. The input resistance of the HEMT is positive even for large input powers, thus demonstrating the stability of the HEMT. Therefore, the optimum input impedance of the HEMT must be (13-j27) Ω.

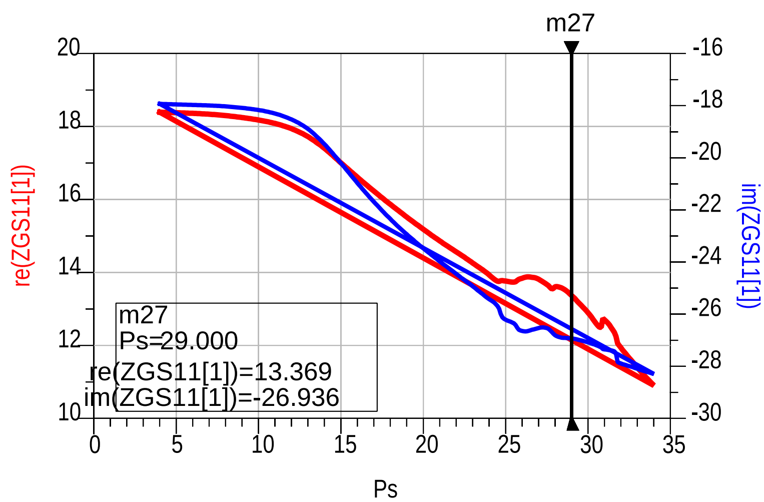


Fig. 2-15: Simulation results of a 8×100μm stabilized HEMT cell terminated by the optimum load,

Ps is the signal source power in dBm, re(ZGS11[1]) is the real part of transistor input impedance at fundamental harmonic in ohms, and im(ZGS11[1]) is the imaginary part of transistor input impedance at the fundamental harmonic in ohms

Fig. 2-16 shows the power level of the harmonics delivered to the optimum load, and the ratio of the fundamental frequency power level to other harmonics power level summation. Fig. 2-17 shows the time waveforms of voltage and current at the input and output as well as the dynamic load-cycle depicted on the I-V characteristic curve of the HEMT.

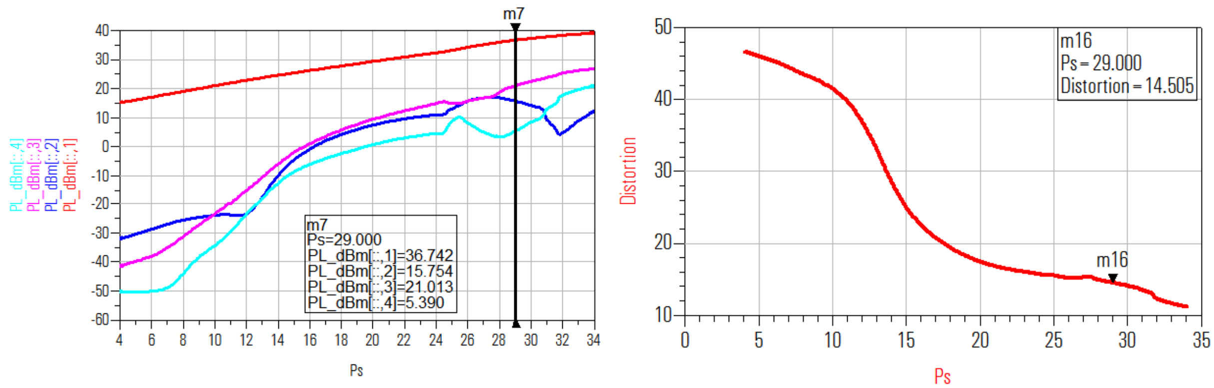


Fig. 2-16: Simulation results of a 8×100µm stabilized HEMT cell terminated by the optimum load,

Ps is the signal source power in dBm, PL_dBm[::,1] is the power at the load at the fundamental harmonic, PL_dBm[::,2] is the power at the load at the second harmonic, PL_dBm[::,3] is the power at the load at the third harmonic, and PL_dBm[::,4] is the power at the load at the forth harmonic

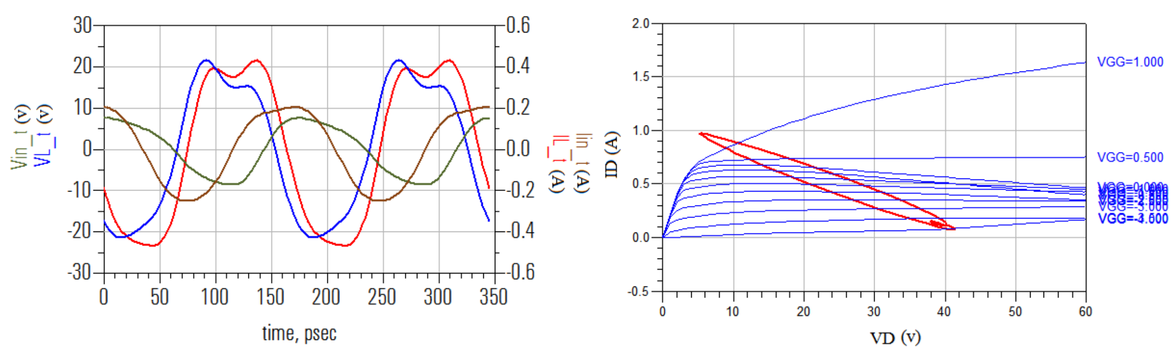


Fig. 2-17: Simulation results of a 8×100µm stabilized HEMT cell terminated to optimum load,

voltage and current time wave-forms of the input/output (left) and dynamic load-cycle over the I-V curve (right)

The obtained optimum output load of the 4×100µm HEMT cell was about (50+j30) Ω. When this cell is terminated by its optimum output load without input matching network, according to Fig. 2-18, the small signal transducer gain is almost 14 dB. In addition, the output power is 34 dBm, the large signal transducer gain is 10 dB, the PAE is 34%, and the input impedance is about (18-j65) Ω, at around the 3-dB compression gain (Fig. 2-18). Because the HEMT was simulated without input matching network so, there was about 0.8 dB loss between the power of the source (Ps) and the power available at the HEMT's gate. As a result, the 3-dB compression gain in Fig. 2-18 corresponds to a power of 24.2 dBm at the gate of the transistor.

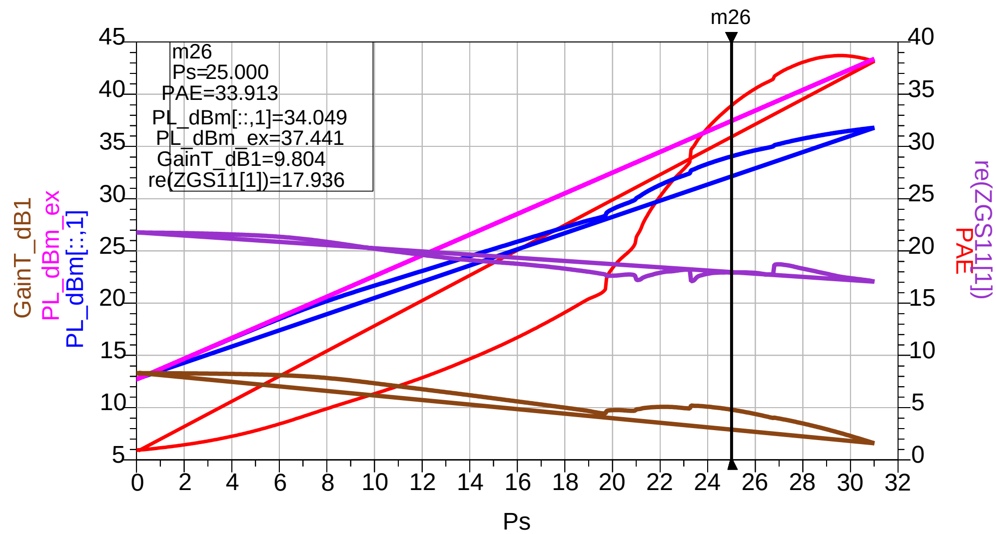


Fig. 2-18: Simulation results of a 4×100μm stabilized HEMT cell terminated to its optimum load.

Ps is the signal source power in dBm, PL_dBm[::,1] is the fundamental harmonic of the output power in dBm at the load, PL_dBm_ex is the virtual extension of the linear part of the output power in dBm, GainT_dBm1 is the transducer gain in dB at the fundamental harmonic, PAE is power added efficiency in %, and re(ZGS11[1]) is the real part of the transistor input impedance at the fundamental harmonic in ohms

In the sixth step, based on the results obtained in the previous step, the configuration of the HPA was designed as a three-stage amplifier using eight 8×100 μm parallel HEMTs at the output stage (stage#1), two 8×100 μm HEMTs at the middle stage (stage#2) and one 4×100 μm HEMT at the input stage (stage#3). The HPA configuration along with a line-up power gain map was depicted in Fig. 2-19. So, The HPA provides 45 dBm output power with large signal gain of 25 dB.

In the seventh step, the line widths for the different parts of the HPA are calculated. The available technology has two metal layer, namely 1ME and 2ME. The thickness of 1ME is 1 μm and 2ME is 3 μm. 2ME can be landed on 1ME through a via layer, VIA2, to make a low resistance line. The lines fabricated by this way have 4 μm thickness and can provide 6.75 $\frac{m\Omega}{sq}$, thus the maximum current that this line can withstand is 24 $\frac{mA}{\mu m}$. The width of the lines and inductors were determined based on the maximum tolerable current and the maximum required current for each line. Same as in Fig. 2-13, two vias were placed between HEMT cells not only to make a perfect ground for the HEMT cells but also to distribute the heat dissipated by the HEMTs to the bottom ground plate. In the worst case, the capacitors in the OMN must withstand 24 DC bias voltage plus 45 dBm power. Because the maximum operating voltage of the capacitors is 40 V, two series capacitors were used at the OMN that can operate reliably.

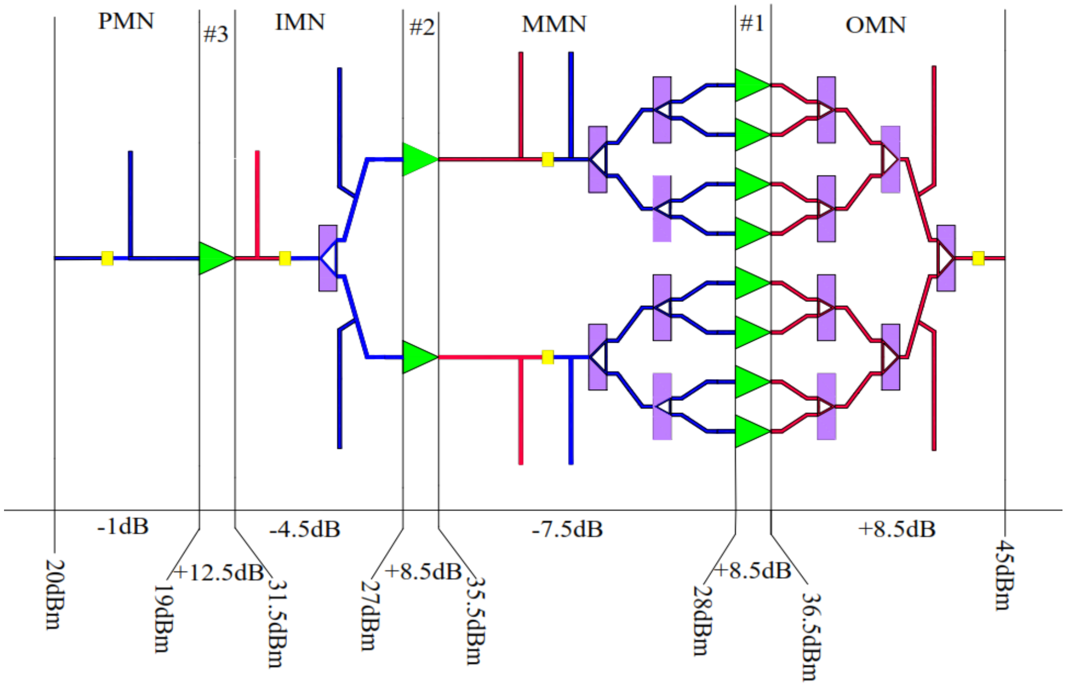


Fig. 2-19: HPA configuration and power/gain line-up

In the eighth step, four matching networks OMN, MMN, IMN, and PMN must be designed (as displayed in Fig. 2- 19). The matching networks not only must match the input/output of the HEMTs to their optimum impedances but also must properly combine, split and transfer the power among the HEMT cells in the three stages. The matching networks must also provide the required bias voltage to the gate/drain of the HEMTs. The OMN was designed to match the optimum output load of each cell at Stage#1 to the 50 Ω output port of the HPA as well as to achieve the maximum output power. MMN and IMN were designed to match the optimum output load of each cell at Stage#2 and Stage#3 to the conjugated input impedance of the cells in Stage#1 and Stage#2, respectively. The PMN has been used to match the 50 Ω input port of the HPA to the conjugated input impedance of the cell in Stage#3.

The matching networks were designed so that, at least, 10% variations of the utilized elements do not degrade the responses of the matching networks.

In the line-up power/gain map shown in Fig. 2-19, 0.5 dB loss for OMN, 1.5 dB for MMN and IMN, and 1 dB for PMN, were set. The T-junction was used for all the combiners and dividers. Each matching network was designed separately then assembled together along with the HEMTs to get the full HPA.

A simplified topology of the matching networks in a full HPA is shown in Fig. 2-20. The required stabilization circuits required to prevent the even-mode and parametric oscillations were included in the matching networks. The circuits required to prevent the low frequency (or bias) oscillations were also added to the matching networks in Fig. 2-20. To achieve more linear amplification, a third harmonic suppressor has been added to the output matching network. The harmonic balance simulation results of the schematic in Fig. 2-20 are displayed in Fig. 2-21. The results show 34 dB for the small signal transducer gain while the large signal transducer gain is about 25.5 dB (with 20 dB input power) and the output power is 45.5 dBm, which completely meet the line-up power/gain map depicted in Fig. 2-19. The PAE is a little smaller than expected, probably because the designed matching networks or the harmonic suppressor need more tuning. Fig. 2-21 also shows the input resistance of the HEMT cells at different stages, which demonstrates the stability of the HPA.

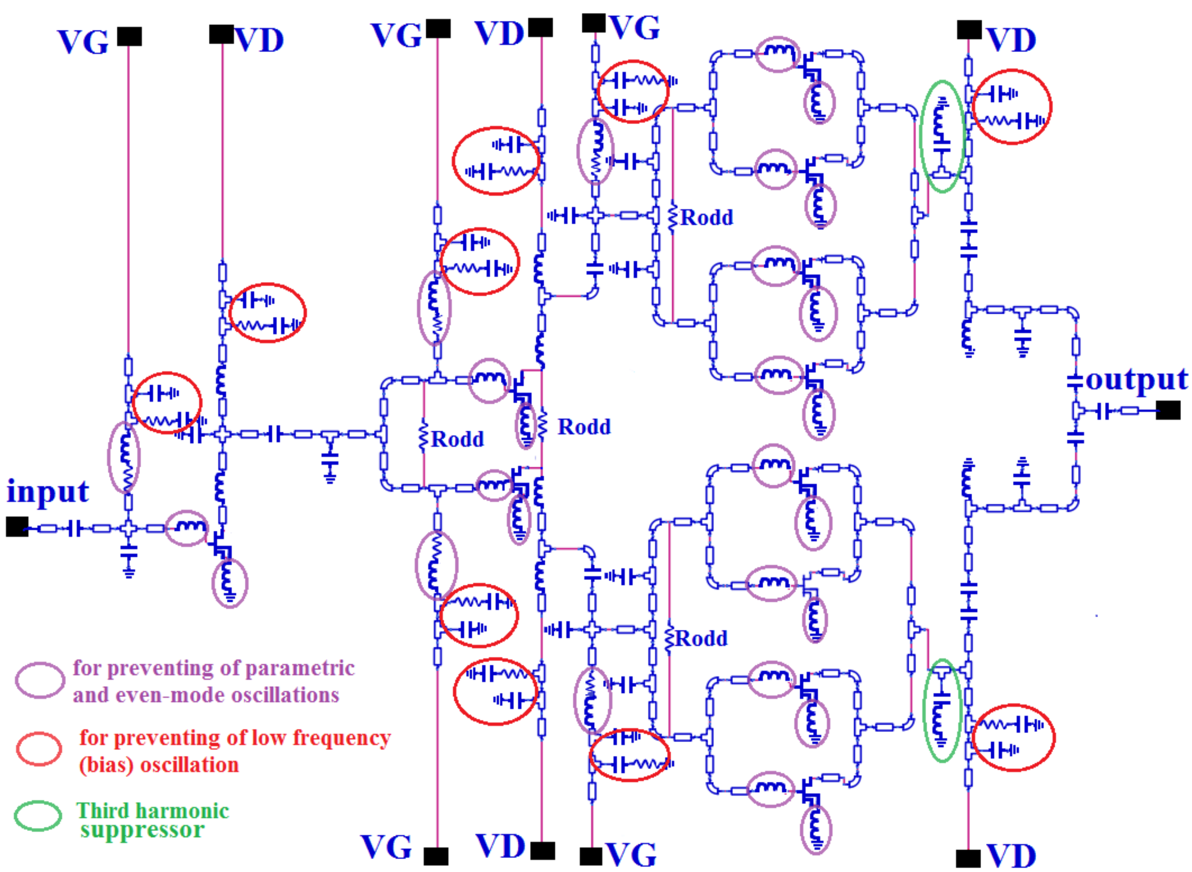


Fig. 2-20: Simplified circuit schematic of the MMIC-HPA

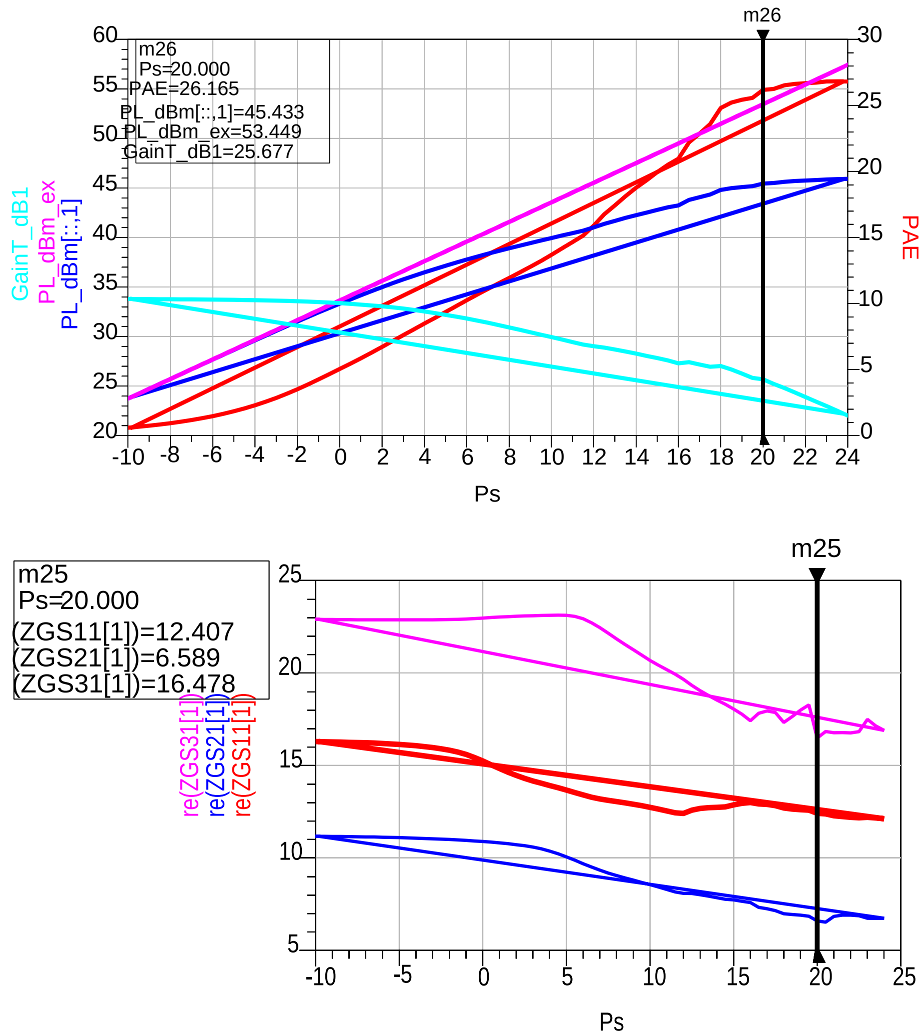


Fig. 2-21: schematic simulation results of the MMIC HPA.

Ps is the signal source power in dBm, PL_dBm[::,1] is the fundamental harmonic of output power in dBm at the load, PL_dBm_ex is the virtual extension of the linear part of the output power in dBm, GainT_dBm1 is the transducer gain in dB at the fundamental harmonic, PAE is the power added efficiency in %, and re(ZGS11[1]), re(ZGS21[1]), re(ZGS31[1]) are the real part of the transistors input impedance (in ohms) at the fundamental harmonic at stage#1, stage#2 and stage#3, respectively.

In the ninth step, the layout of each matching network is generated. By effectively meandering the lines, a compact layout was obtained for each matching network. All the components of the matching networks must be selected from the design kit. The lines or components should not be located very close together due to undesirable coupling between the lines and components.

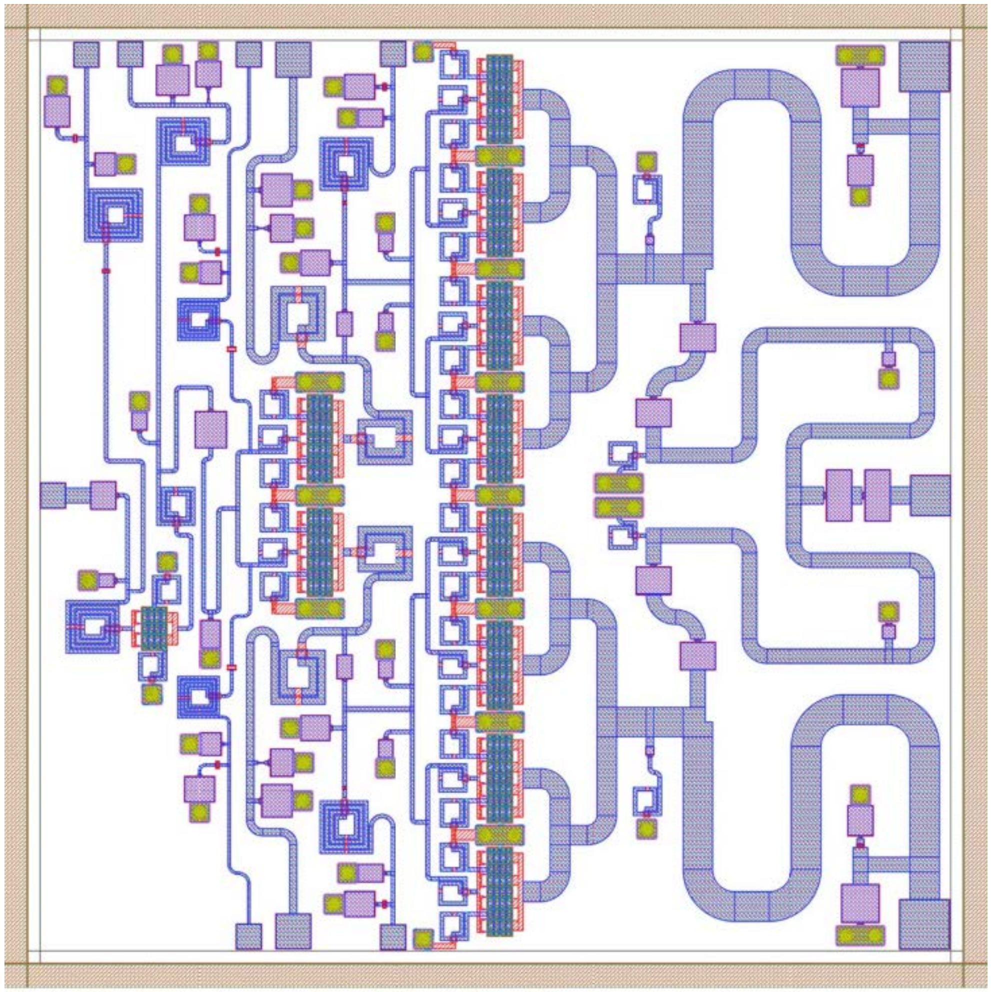


Fig. 2-22: HPA Layout (3.7 mm by 3.7mm)

In the tenth step, the layout of the matching networks obtained in the last step was simulated in Keysight ADS Momentum and co-simulation technique was performed to obtain the whole HPA performance. A HPA with the size of 3.7*3.7 mm^2 was first designed (Fig. 2-22). Due to large couplings between the adjacent lines/components, the responses of the matching networks varied and the HPA performance degraded. A new HPA layout was then designed with a larger size of 4.7*3.7 mm^2 (Fig. 2-23), to lower the undesirable couplings to an accepted level and accordingly, to enhance the HPA performance.

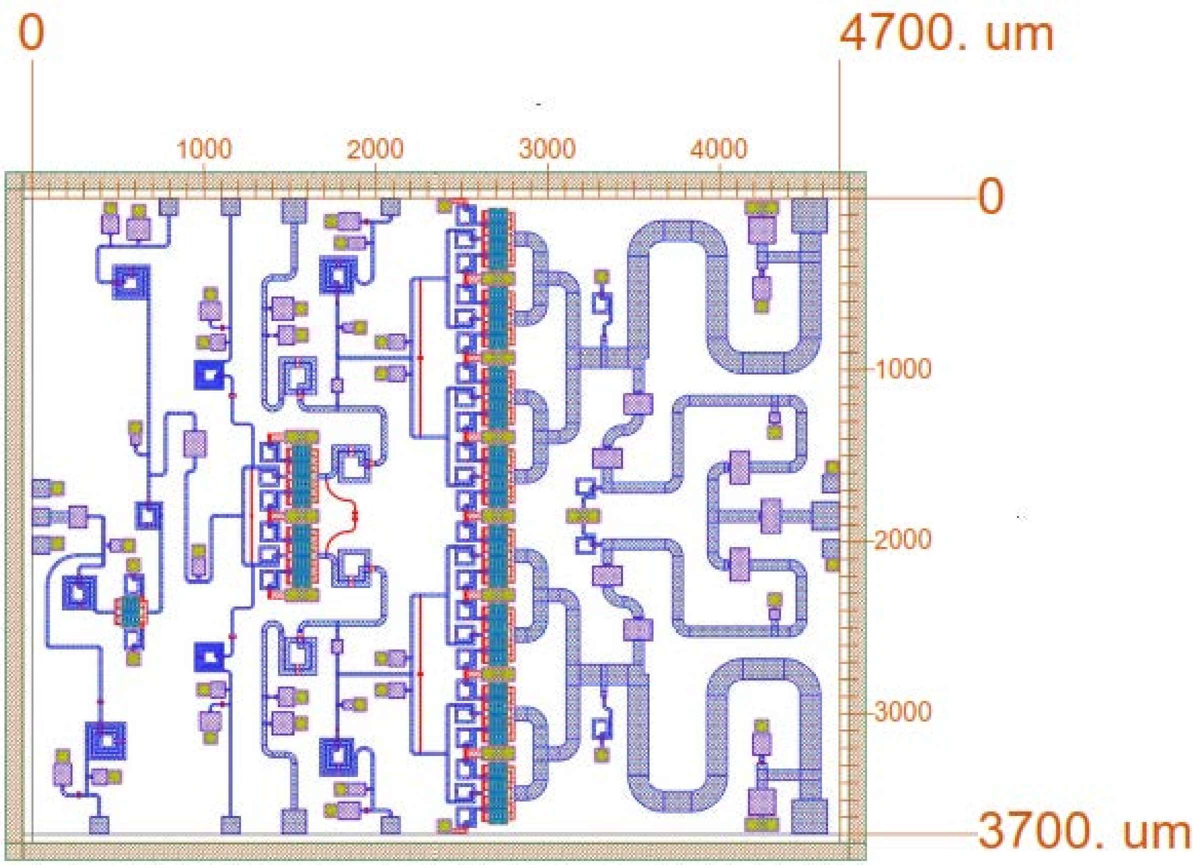


Fig. 2-23: New HPA Layout (4.7 mm by 3.7mm)

When the whole HPA was co-simulated, odd-mode oscillations were observed causing convergence issues during simulation. In fact, the matching networks were not able to provide the exact same impedance for all parallel HEMT cells due to unavoidable coupling between adjacent elements. Isolator resistors are usually used for all outputs and inputs of the HEMT cells. In this design, some specific locations were found to place the isolator resistors without requiring additional layout area. These isolator resistors, R_{odd}, of about 15Ω, are indicated in Fig. 2-20 as well as in the HPA layout shown in Fig. 2-23. Therefore, the final HPA shown in Fig. 2- 23 is completely stable. Fig. 2-24 shows the input and output impedance at the fundamental frequency, which demonstrates the stability of the HEMTs. At 20 dB source power, the input/output impedances of the HEMTs calculated in the fifth step (desired) and their corresponding values from Fig 2-24 (obtained) in each stage of the HPA are summarized and compared in Table 2-4, demonstrating that the designed matching networks were accurately designed.

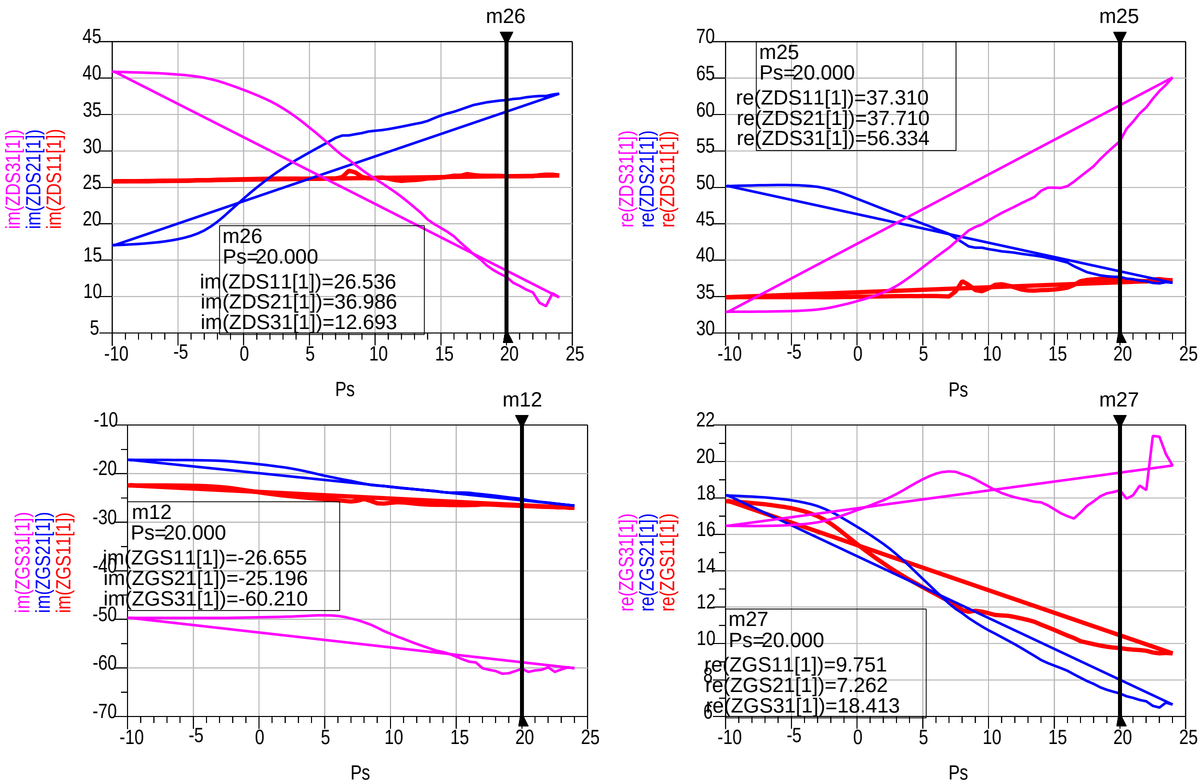


Fig. 2-24: Input/output impedances of the HEMT cells at fundamental frequency versus signal source power (Ps).
re(ZDS11[1]), re(ZDS21[1]) and re(ZDS31[1]): real part of the output impedance of the HEMTs at stage 1, 2, and 3, respectively.
re(ZGS11[1]), re(ZGS21[1]) and re(ZGS31[1]): real part of the input impedance of the HEMTs at stage 1, 2, and 3, respectively.
im(ZDS11[1]), im(ZDS21[1]) and im(ZDS31[1]): imaginary part of the output impedance of the HEMTs at stage 1, 2, and 3, respectively.
im(ZGS11[1]), im(ZGS21[1]) and im(ZGS31[1]): imaginary part of the input impedance of the HEMTs at stage 1, 2, and 3, respectively.

Table 2-4: Input/output impedances of the HEMTs

Input impedance at stage#1 (desired)	13 - j27	Output impedance at stage#1 (desired)	40 + j20
Input impedance at stage#1 (obtained)	9.8 - j26.7	Output impedance at stage#1 (obtained)	37.3 + j26.5
Input impedance at stage#2 (desired)	13 - j27	Output impedance at stage#2 (desired)	40 + j20
Input impedance at stage#2 (obtained)	7.3 - j25.2	Output impedance at stage#2 (obtained)	37.7 + j37
Input impedance at stage#3 (desired)	18 - j65	Output impedance at stage#3 (desired)	50 + j30
Input impedance at stage#3 (obtained)	18.4 - j60	Output impedance at stage#3 (obtained)	56.3 + j12.7

Fig. 2-25 shows 31% PAE, 46 dBm output power, and 26 dB large-signal transducer gain when the source power is 20 dBm. These values can satisfy all the design specifications. Also, the small signal transducer gain is 36 dB.

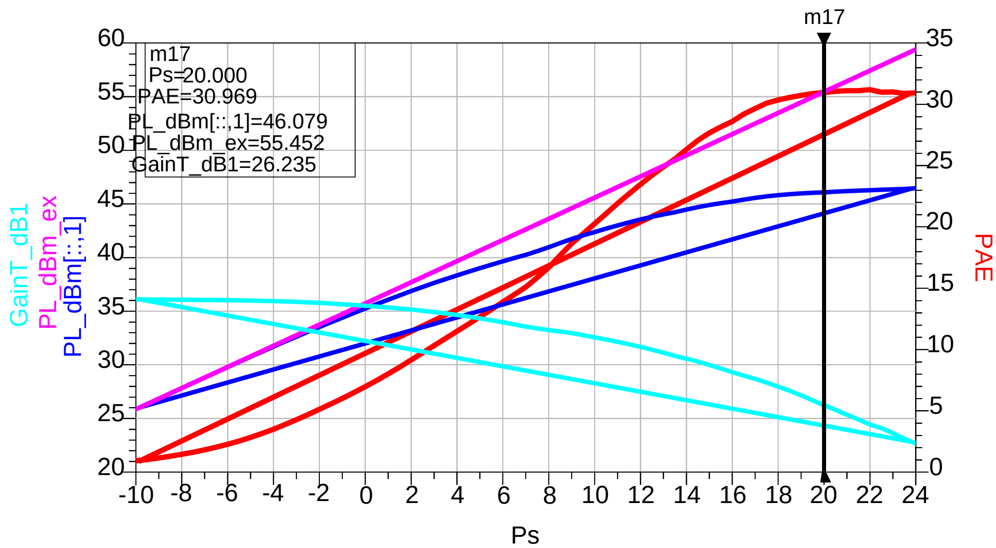


Fig. 2-25: Output power, transducer gain and PAE of the final HPA at fundamental frequency versus signal source power (Ps) in dBm,

PL_dBm[::,1] is the fundamental harmonic of the output power in dBm at the load, PL_dBm_ex is the virtual extension of the linear part of the output power in dBm, GainT_dBm1 is the transducer gain in dB at the fundamental harmonic, PAE is the power added efficiency in %.

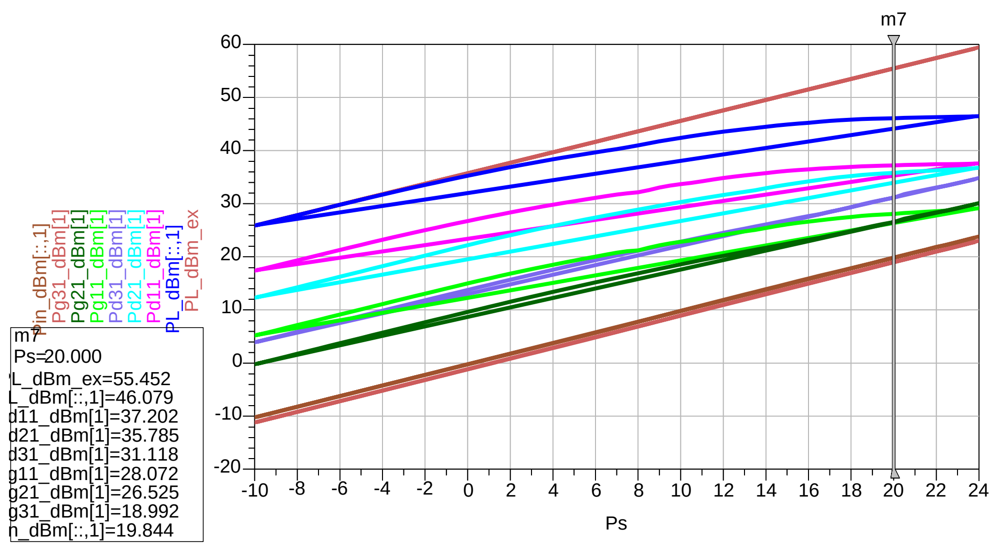


Fig. 2-26: Typical power (in dBm) of fundamental frequency at gate and drain of different stages of the HPA versus the signal source power (Ps) in dBm.

PL_dBm[::,1] is the power at the load, PL_dBm_ex is the virtual extension of the linear part of the output power, Pd11_dBm[1] is the power at the drain of stage 1, Pd21_dBm[1] is the power at the drain of stage 2, Pd31_dBm[1] is the power at the drain of stage 3, Pg11_dBm[1] is the power at the gate of stage 1, Pg21_dBm[1] is the power at the gate of stage 2, Pg31_dBm[1] is the power at the gate of stage 3, Pin_dBm[::,1] is the power at the input of the HPA.

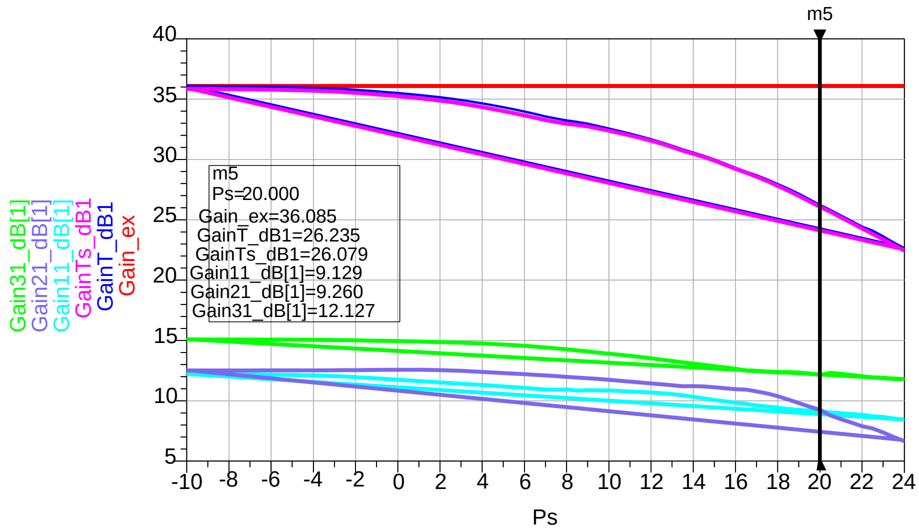


Fig. 2-27: Typical gain in dB of the different stages of the HPA at fundamental frequency versus the signal source power (Ps) in dBm,
GainT_dB1 is the transducer gain, Gain_ex is the virtual extension of the small signal gain, GainTs_dB1 is the output power minus the source power, Gain11_dB[1] is the gain of stage 1, Gain21_dB[1] is the gain of stage 2, Gain31_dB[1] is the gain of stage 3.

The powers at the gate and drain of the HEMTs at each stage are displayed in Fig. 2-26 while the gain of the three stages are displayed in Fig. 2-27 to follow up the power/gain line-up map depicted in Fig. 2-19. Fig. 2-26 and Fig. 2-27 demonstrate that the desired values of the power/gain line-up indicated in Fig. 2-19 have been fulfilled. In Fig. 2-28, the total consumed DC power is compared with the AC power delivered to the load at the fundamental frequency, showing that the output power is 5 dB less than the overall consumed DC power. In other words, the output power is 31.6% of the total consumed DC power. Therefore, the total efficiency of the HPA is slightly larger than the PAE by 0.6%.

The output power at different harmonics is shown in Fig. 2-29. The level of the third harmonic is reduced (see Fig. 2-16) due to the effect of the third harmonic suppressor used at the output matching network. Fig. 2-29 also shows the total harmonic distortion (THD), defined as the ratio of the fundamental frequency to the summation of other harmonics. THD is about 28 dBm, thus demonstrating that the HPA is highly linear.

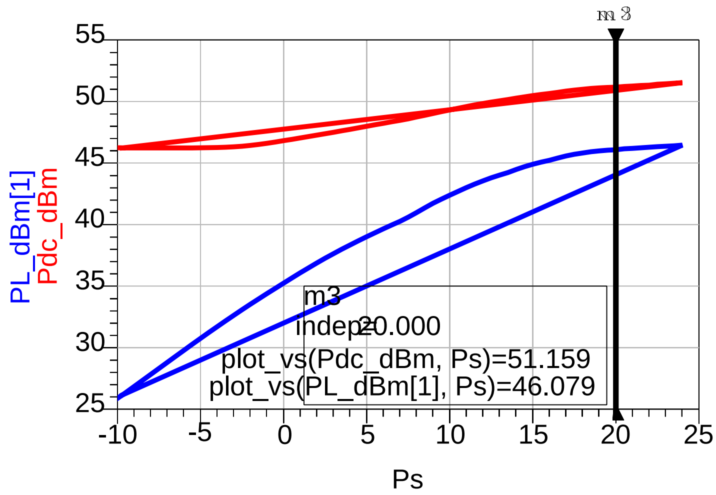


Fig. 2-28: Power consumed and produced by HPA,
Pdc_dBm is the total consumed DC power in dBm of the HPA and PL_dBm[1] is the power of fundamental frequency at the load in dBm versus the source power (Ps) in dBm,

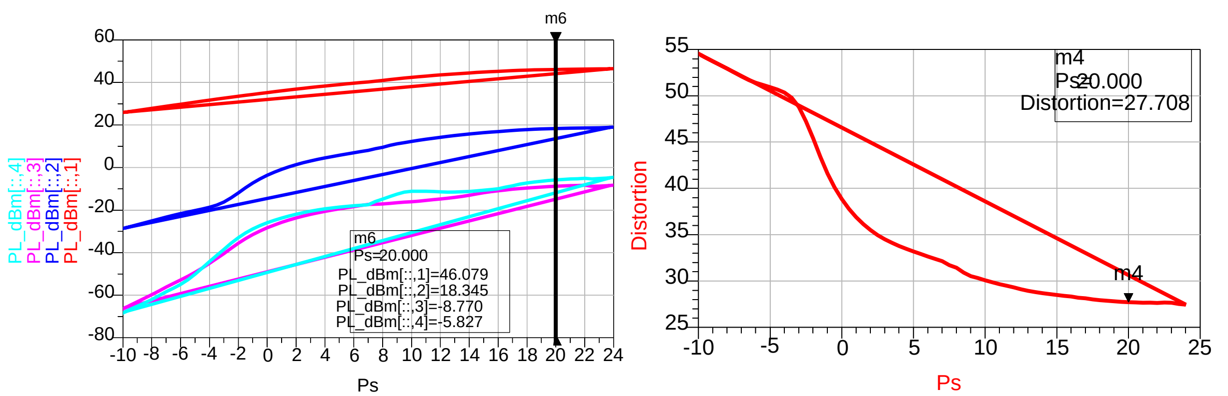


Fig. 2-29: Output power of different harmonics in dBm (left) and distortion (THD) of the HPA in dB (right), versus the signal source power (Ps) in dBm,
PL_dBm[::,1] is the power at the load of the fundamental, PL_dBm[::,2] is the power at the load of the second harmonic, PL_dBm[::,3] is the power at the load of the third harmonic, and PL_dBm[::,4] is the power at the load of the forth harmonic

Fig. 2-30 shows the voltage and current at the gate and drain of a typical HEMT cell in each stage. Fig. 2-31 shows the total current consumed by the HPA from different bias voltage supplies at each stage. The time waveforms of the voltage and current of the load are displayed in Fig. 2-32 and the dynamic load-cycle over the I-V characteristic curve of the HEMTs are displayed in Fig. 2-33.

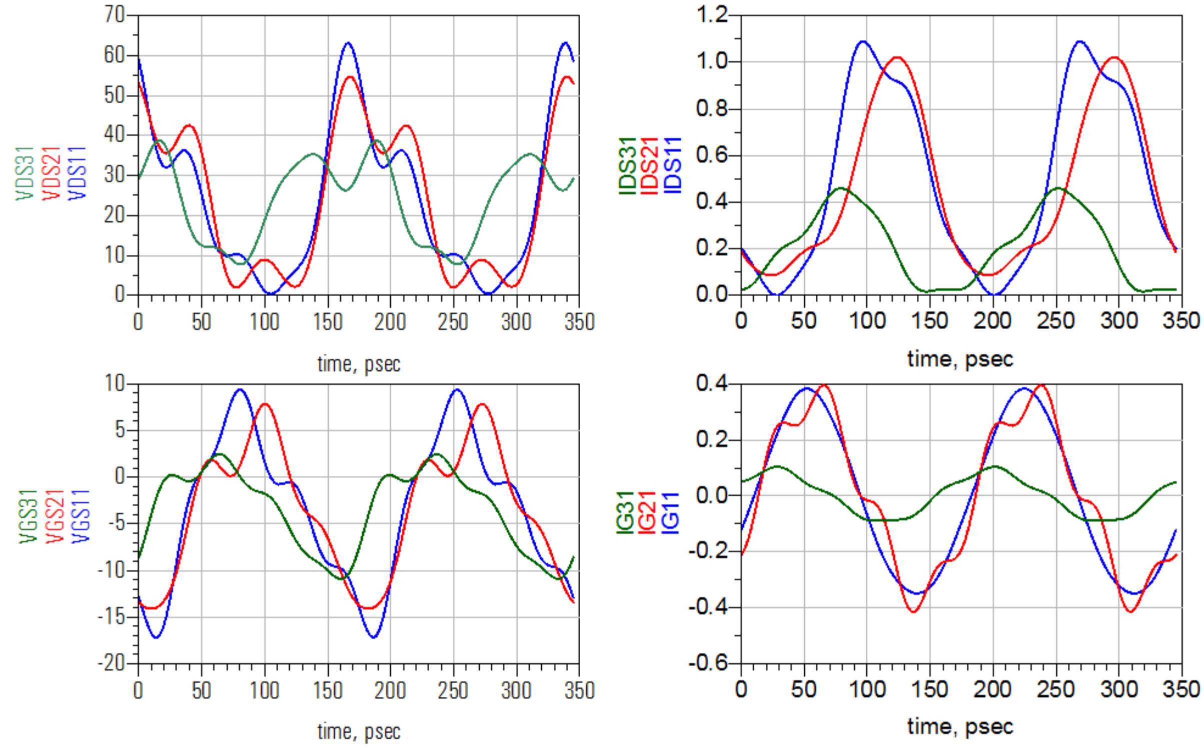


Fig. 2-30: Time wave-form of the voltage and current of drain and source of each HEMT at each stage,
VDS11, VDS21, VDS31 are the voltage at drain of each HEMT at stage 1, 2, and 3, respectively,
VGS11, VGS21, VGS31 are the voltage at the gate of each HEMT at stage 1, 2, and 3, respectively,
IDS11, IDS21, IDS31 are the current at drain of each HEMT at stage 1, 2, and 3, respectively,
IG11, IG21, IG31 are the current at the gate of each HEMT at stage 1, 2, and 3, respectively,

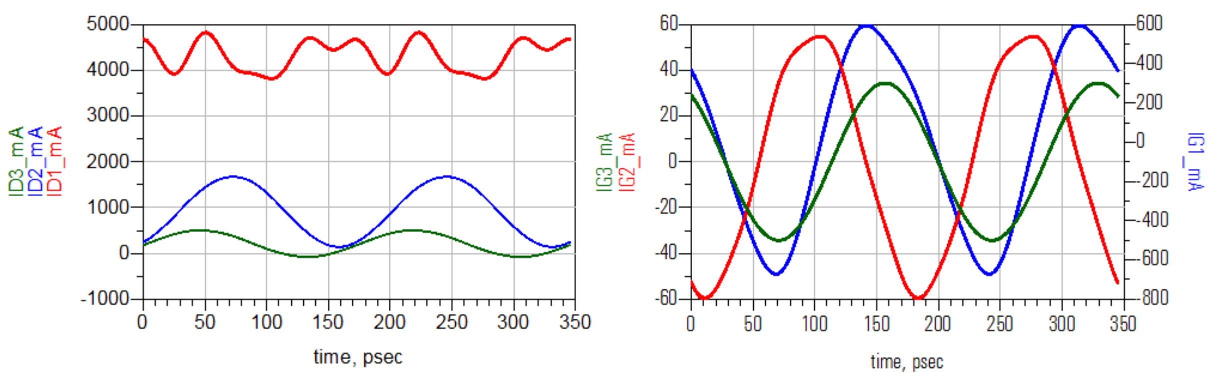


Fig. 2-31: Time wave-form of the current drawn from the bias voltage supplies,
ID1_mA is the current drawn from drains at stage 1 in mA, ID2_mA is the current drawn from drains at stage 2 in mA, ID3_mA is the current drawn from drains at stage 3 in mA, IG1_mA is the current drawn from gates at stage 1 in mA, IG2_mA is the current drawn from gates at stage 2 in mA, and IG3_mA is the current drawn from gates at stage 3 in mA

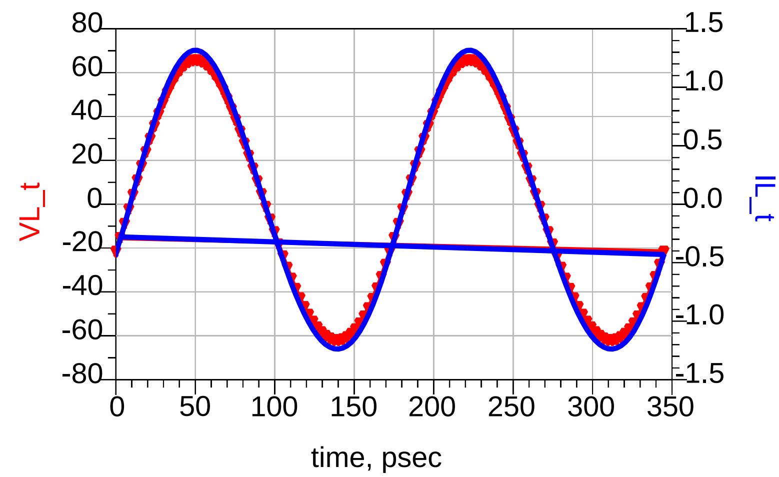


Fig. 2-32: Time waveforms of the output voltage (V) and current (A)

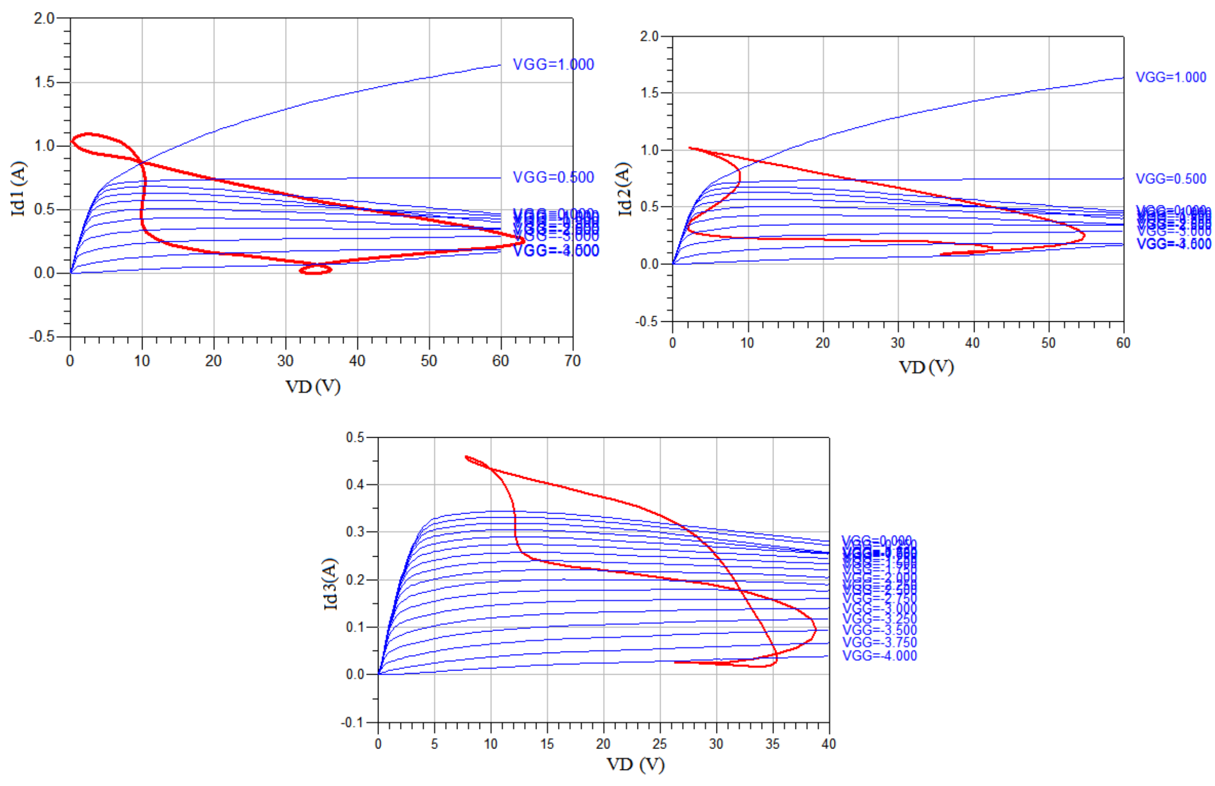


Fig. 2-33: Dynamic load-cycle over the I-V curves of the HEMTs at each stage,
Id1 is the drain current of a HEMT cell in stage 1, Id2 is the drain current of a HEMT cell in stage 2, and Id3 is the drain current of a HEMT cell in stage 3

All presented simulation results were performed when the frequency of the signal source was 5.8 GHz. At the end, the HPA was simulated by sweeping the frequency of the signal source. Fig. 2-34 shows the PAE, the large signal gain and the output power versus frequency when the power of signal source was set to 20 dBm.

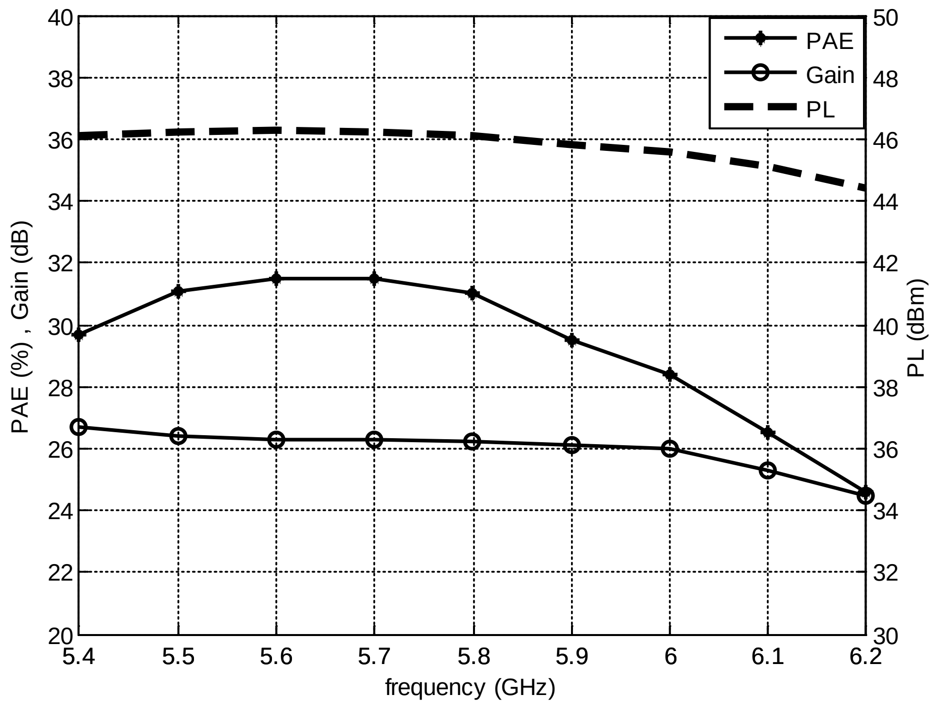


Fig. 2-34: PAE, large signal transducer gain, and output power of the final HPA versus frequency

Finally, in the eleventh step, design rule check was performed and all errors removed by a little tuning of the layout. The layout shown in Fig. 2-23 has all the required pads and outer frame for sawing.

2.8 Conclusion

In this chapter, a MMIC HPA based on AlGaN/GaN HEMT technology has been designed. A brief review of GaN technology as well as a discussion for various types of transistor biasing and stabilization schemes has been presented. An eleven-step design procedure was presented to design the MMIC HPA. The designing procedure was reviewed for the proposed HPA by focusing on the innovative proposed stabilization technique. A detailed, complete and useful set of the simulation results was presented. The results demonstrate the stability of the MMIC HPA. The main features of the HPA performance were satisfied with 31% power added efficiency, 46 dBm saturated output power and 26 dB large-signal gain. Also, The HPA shows 12% fractional bandwidth. Although GaN technology provided by NRC is not mature yet, based on Table 2-1, the performance of the designed HPA can be successfully compared to existing recent designs.

Chapter 3

Power combining networks

3.1 Introduction

To achieve a high power transmitter module, several units of the high power amplifier designed in chapter 2 must be combined. Therefore, a power combiner and/or divider structure is required. Since the proposed transmitter module should combine up to eight HPAs, only compact configurations can be retained among the wide panel of possible power combiners/dividers (PCD) available in the literature. Also, because efficiency is the key design parameter of the proposed transmitter module, the insertion loss of the designed PCD should be the most important feature of its performance.

In this chapter, the design of the PCD is first described. Then, a suitable PCD configuration is proposed by modifying the conventional Gysel structure. Finally, a technique based on even-odd mode analysis is proposed to efficiently design the proposed structure.

3.2 Main features of existing PCD

A PCD is a specific type of couplers. Couplers can be implemented through different media, e.g. microstrip, waveguide, stripline …. In this chapter, microstrip couplers will be discussed because this structure has the most compact size and can be implemented easier in comparison with other structures. There are different kinds of microstrip couplers e.g. Wilkinson, Gysel, branch-line, Lange coupler, rate race and so on. Note that if the power is divided equally between the splitting ports, i.e. direct and coupling ports, a 3-dB coupling is achieved [66].

Microstrip couplers can be divided into two groups: in-phase and quadrature-phase. Quadrature-phase couplers are not suitable for the purpose of high power amplifier modules due to unavoidable unbalanced power division at the desirable frequency range. This issue becomes worse when a PCD with wider bandwidth is required. Fig. 3-1 shows that quadrature couplers have a large unbalanced amplitude at the center frequency. On the other side, in-phase PCDs, such as Wilkinson, exhibit negligible unbalance amplitude over a wide bandwidth, making them good candidates for high-power applications.

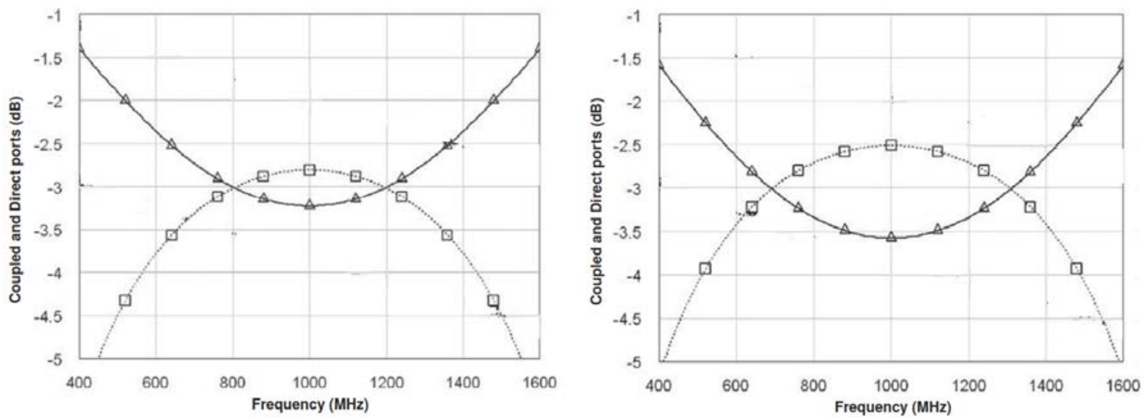


Fig. 3-1: Insertion loss of two different responses of quadrature PCDs with different bandwidths [32]

Microstrip Wilkinson PCD can provide low insertion Loss (IL) as well as high isolation (IS) and return loss (RL) over acceptable bandwidths [80], while also exhibiting the most compact configuration over other PCDs. However, in most cases, the load resistor is too close to the body of the structure, resulting in Wilkinson PCDs that are prone to unwanted radiations from adjacent resistors, leading to a drastic degradation in their performance [32]. High-power RF resistors still occupy large areas although RF components providers are implementing smaller high-power RF devices. Thus, implementing Wilkinson PCDs with high power resistors on a Printed Circuit Board (PCB) remains a challenge. One way to include a high power RF resistor with minimum unwanted radiations would be to add a half-wavelength impedance sections to each arm and also between the load resistor ends and the Wilkinson's arms [81] (Fig. 3-2). However, this scheme will obviously increase the size and severely degrade the total insertion loss. During the last few years, several improvements have been made on Wilkinson PCD design but most of them are not still able to address these drawbacks [82]-[84].

In 1975, Gysel proposed a configuration for high-power in-phase PCDs [85]. In this structure, two load resistors have been used outside the structure body so large size resistors can be used with minimum concern about unwanted radiations. Note that this structure is still an in-phase PCD but if one of the loads is removed, the remaining configuration would be close to a rat race structure. The main drawback of the Gysel structure is that it is relatively bulkier (Fig. 3-3).

From there, many modifications to the original configuration have been suggested [88]-[93]. The measurement results of the referred works are summarized in Table 3-1.

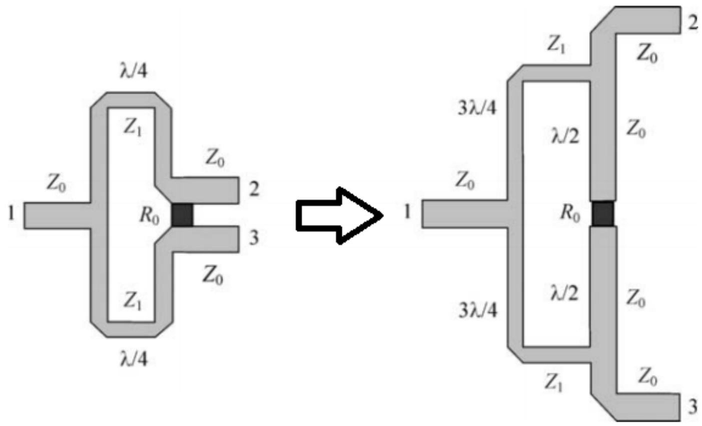


Fig. 3-2: Wilkinson PCD with extra half wavelength [81]

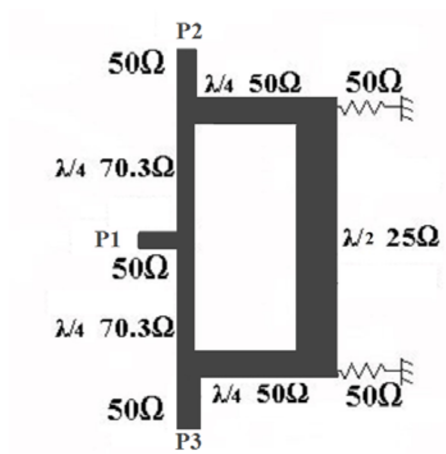


Fig. 3-3: Original configuration of Gysel combiner [85]

Therefore, the most important parameters to consider in this research in terms of PCD performance are insertion loss and size. To achieve a reliable and high-efficiency transmitter module, the IL was limited to 0.2 dB with a maximum 0.05 dB unbalance power between two splitting ports for the whole desirable frequency range. The size of any microstrip component is related to the relative permittivity of the substrate board. Rogers RT-Duroid 5880 substrates were used to design the RF circuits of the transmitter module. This substrate has a relative permittivity of 2.2, 0.381 mm thickness and 0.0009 loss tangent. The free space quarter wavelength at 5.8 GHz is almost 13 mm and the quarter wavelength of guided wave in the selected substrate is 8.8 mm. Hence, a PCD with a size no more than 20*20 mm^2 is small enough. For the PCDs supposed to operate just as a divider in the transmitter module, Wilkinson structure may be used to save more space. The input power for the HPA designed in chapter 2 is about 20 dB. Thus, 1-watt resistors, that are small enough, can be utilized in the Wilkinson structure as power dividers of the transmitter module.

Table 3-1: Comparison between measurement results of the reported Gysel structures

Bandwidth (GHz)	[86]	[88]	[89]	[90]	[91]	[92]	[93]
< 0.25 dB IL	0	0	0	0	0	0	1.6-2.2
< 0.5 dB IL	0	0	0	0	0	2.9-3.3	1.5-2.4
> 20 dB RL of port 1	4.5-7.7	1.3-1.7 &2.3-2.7	Not presented	1-1.4 &1.6-1.9	0.8-1.2	2.8-3.3	1.9-2.4
> 15 dB RL of port 2 or 3	5-7.6	1.3-2.6	Not presented	1.1-1.9	Not presented	2.9-3.2	1.7-2.5
> 15 dB IS	4-8.2	0-5	0.9-2.3	1.1-2	0.4-1.6	2.6-3.3	1.5-2.3
< 0.1 dB unbalance power between splitting ports	0	2.7-2.9	0.5-2.3	Not presented	Not presented	0	1.5-2.6

The next important parameter to consider is RL. A return loss greater than 20 dB was set as a design goal for the PCDs, i.e., the reflected signal power would be less than 1% of the incident signal power. Isolation is less important in power amplifiers combining. Isolation of typically 15 dB or even 10 dB is enough for PCDs in amplifiers but for applications such as signal mixing, higher isolation may be required. Note that there are no concerns about phase difference of the splitting ports of the Wilkinson or Gysel PCDs (They are the same).

3.3 Design and analysis of modified Gysel PCD

In this research, an enhanced Gysel PCD configuration is presented by inserting a meandered load lines to a conventional configuration, where the 50 Ω load resistors are directly connected to the Gysel PCD ring. This aims to add three additional degrees of freedom to the structure compared to standard ones, leading to low insertion loss and high return loss over a wider bandwidth, as well as facilitating design flexibility for the load location. The three additional degrees of freedom, compared to the standard structures, are to include the value of the load resistor as well as the length and width (or characteristic impedance) of the meandered load line.

At first glance, adding an extra load line would increase the overall device size but, as demonstrated in this research, careful meandering of the additional lines helped making our design more compact without degrading performance. Additional design flexibility to the Gysel structure allows for narrower transmission lines. Microstrip lines with narrower widths not only reduce the size of the Gysel PCD but are also easier to meander thus, leading to a more compact design in comparison with the original configuration of Gysel PCD. The proposed configuration also shows a wider frequency response with approximately 10% fractional bandwidth for 20 dB return loss. In contrast, conventional Gysel PCDs have demonstrated fractional bandwidths of 5% or less [32].

To understand the theory of operation of the proposed Gysel PCD, an even-odd mode analysis was used while all the design steps are refined by using commercial circuit/EM simulators such as Keysight ADS Momentum. Fig. 3-4 shows the schematic of the proposed Gysel PCD in which all characteristic impedances ($\mathbb{Z}_a, \mathbb{Z}_b, \mathbb{Z}_c$, and $\mathbb{Z}_d$) and load values (R_L) have been respectively normalized to z_a, z_b, z_c, z_d, and r_L, relative to the system impedance $\mathbb{Z}_0 = 50\ \Omega$. Due to symmetry, the configuration of Fig. 3-4 can be analyzed using the even-odd mode equivalent circuits as shown in Fig. 3-5. Due to the narrowband nature of the quarter-wave lines including their non-negligible parasitic effects, low or high impedance terms are used instead of the desired short and open circuits. The seen impedances from different nodes shown in Fig. 3-5 are reported in Table 3-2 for both even and odd modes.

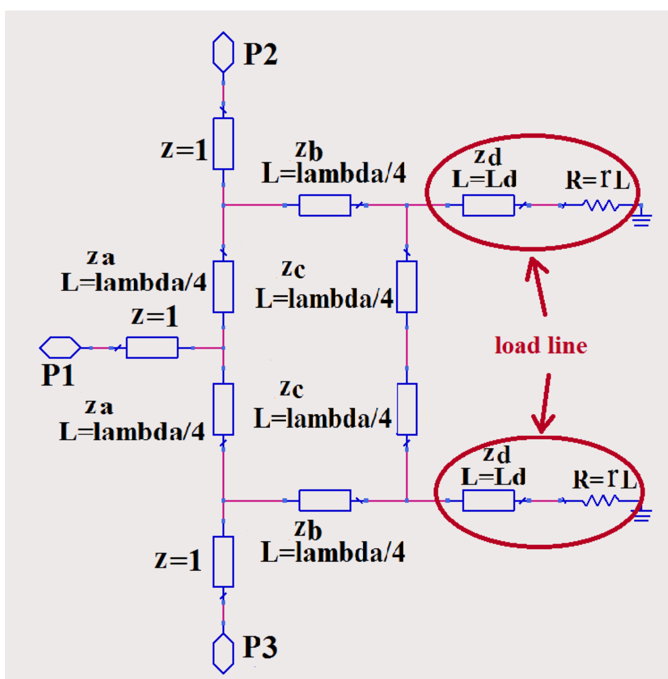


Fig. 3-4: Proposed modified Gysel with stepped impedance load lines

Perfect matching between ports 1 and 2 from even mode analysis implies that [66],

$$z_{6,e} = z_{5,e} \Rightarrow \; z_a = \sqrt{2} \tag{3-1}$$

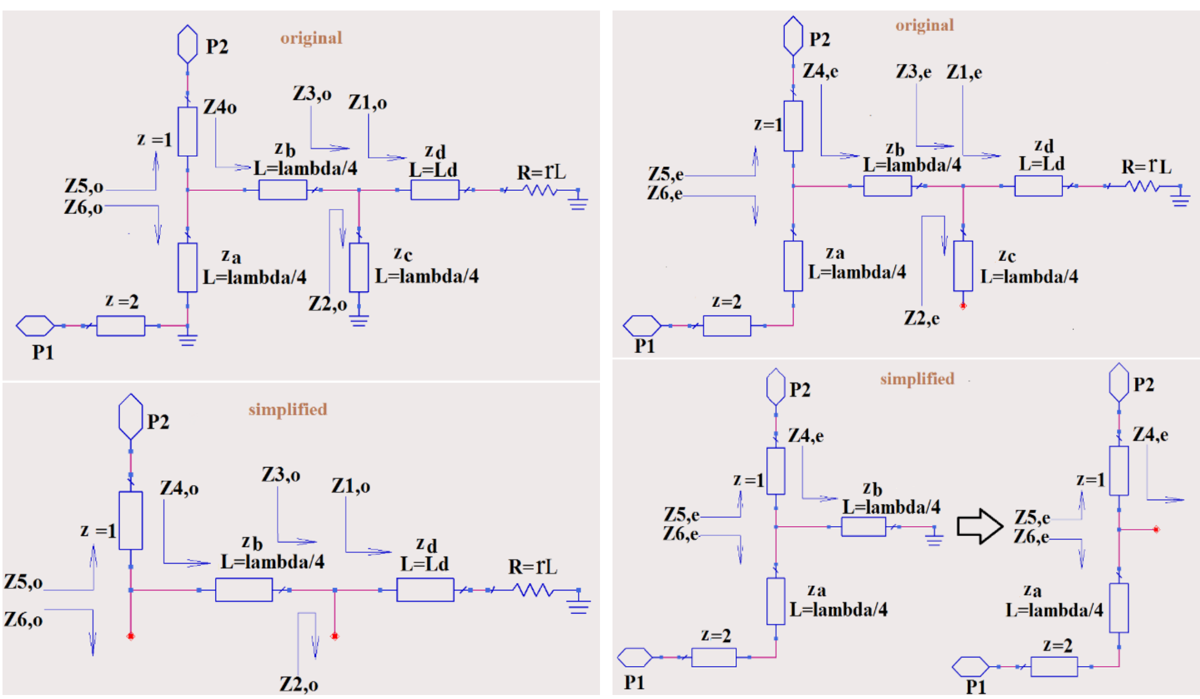
whereas odd mode analysis leads to

$$z_{5,o} = z_{4,o} \Rightarrow z_{3,o} = (z_b)^2 \; \Rightarrow z_{1,o} = (z_b)^2 \tag{3-2}$$

As extracted from the even mode analysis, impedance $\mathbb{Z}_a$ corresponds to 70.7 Ω while any arbitrary value can be chosen initially for $\mathbb{Z}_b$ and $\mathbb{Z}_c$. Therefore, to simplify the designing process and reduce the PCD size, impedance $\mathbb{Z}_b$ has been set to 70.7 Ω ($z_b = \sqrt{2}$) whereas $\mathbb{Z}_c$ was set to smaller values to achieve wider bandwidth and higher isolation. Hence

$$z_{1,o} = 2 \; or \; \mathbb{Z}_{1,o} = 100 \; \Omega \tag{3-3}$$

$$z_d \frac{r_L + j z_d \tan(\beta L_d)}{z_d + j r_L \tan(\beta L_d)} = 2 \tag{3-4}$$



(a) (b)

Fig. 3-5: Equivalent circuit and its simplified configuration (a) odd-mode and (b) even-mode

Table 3-2: Impedances "seen" from the nodes of even & odd mode equivalent circuits

Input impedance	Even mode	Input impedance	Odd mode
$z_{1,e}$	Any value	$z_{1,o}$	$z_d \dfrac{r_L + jz_d \tan(\beta L_d)}{z_d + jr_L \tan(\beta L_d)}$
$z_{2,e}$	Short circuit/ low impedance	$z_{2,o}$	Open circuit/ high impedance
$z_{3,e}$	Short circuit/ low impedance	$z_{3,o}$	$z_{1,o}$
$z_{4,e}$	Open circuit/ high impedance	$z_{4,o}$	$\dfrac{(z_b)^2}{z_{3,o}}$
$z_{5,e}$	1	$z_{5,o}$	1
$z_{6,e}$	${z_a}^2/2$	$z_{6,o}$	Open circuit/ high impedance

Optimal values for all other unknown variables z_d, L_d, and r_L, in (3-4), can be obtained by using Keysight ADS momentum through the following algorithm (Fig. 3-6).

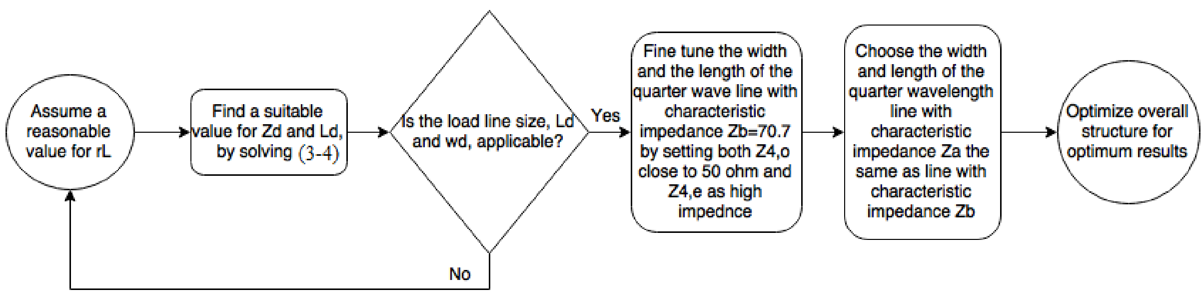


Fig. 3-6: Flowchart of the proposed design process

Design algorithm of the proposed Gysel PCD

1- Design process started by solving (3-4). With its three unknown variables, our first approach is to assume a reasonable value for r_L and then find the smallest applicable length, L_d, and the most suitable characteristic impedance, z_d realized with a line width of w_d in order to satisfy (3-4). Note that, solving (3-4) or equivalently fitting $\mathbb{Z}_{1,o}$ into 5% tolerance of 100 Ω i.e. [95, 105] Ω, for the whole desirable frequency range, is adequate in most practical situations.

2- If the obtained load line size is not suitable, change the load value, r_L, and start again from step 1. In this work, r_L was assumed to be 50Ω for the first two designs while a smaller value was chosen for the last design in order to obtain a practical load line width.

3- The required half wavelength line with characteristic impedance $\mathbb{Z}_c$ has no constraints to its width but it should also not be too wide to impede meandering to reduce size. Also, the following conditions must be verified: $z_{3,o} = z_{1,o} = 2$ and $z_{3,e}$ should correspond to a low impedance value by tuning the width of $\mathbb{Z}_c$ (Fig. 3-5). Note that for these applications, impedances less than 5 Ω can be approximated as low impedances while impedances higher than 1000 Ω can be approximated as high impedances.

4- The width and length of the quarter wave line with characteristic impedance $\mathbb{Z}_b$ = 70.7 Ω should be finely tuned by setting both $\mathbb{Z}_{4,o}$ close to 50Ω and $\mathbb{Z}_{4,e}$ as high impedance.

5- Verify that the width and length of the quarter wavelength line with characteristic impedance $\mathbb{Z}_a$ are the same as those of $\mathbb{Z}_b$ found in step 4.

6- After connecting and shaping all parts in layout design, the entire structure should be optimized and/or fine-tuned to achieve optimum results.

All these steps were closely followed by schematic and electromagnetic co-simulations using Keysight ADS Momentum to take into account the high-frequency behavior of all components used. Through the algorithm described in Fig. 3-6, the presented process also aims to scale and accommodate the proposed improved Gysel PCD for any desirable frequency range.

3.4 Capabilities and scalability of the proposed Gysel PCD

To demonstrate the capabilities of the proposed PCD, a few PCDs were implemented and their measured results compared to expected simulated results [2]. Rogers RT-Duroid 5880 substrates with a relative permittivity of 2.2 and 0.381 mm thickness and Rogers TMM10i substrate with a relative permittivity of 9.8 and with 0.381 mm thickness were used to design the Gysel PCDs operating at Ku and X bands. Here, the Gysel PCD designed and implemented only at Ku-band by Rogers RT-Duroid 5880 is reviewed.

Proposed Gysel PCD at Ku-band

The modified Gysel PCD was designed at the center frequency of 16.5 GHz using an RT-Duroid 5880 substrate. Fig. 3-7 shows the schematic view used to determine the even and odd modes of $\mathbb{Z}_4$and its momentum co-simulation results.

For $\mathbb{Z}_{4,o}$, a 20% tolerance margin and for $\mathbb{Z}_{4,e}$, any value larger than 500 Ω in the entire desirable frequency range was found acceptable to achieve the expected performance for the designed Gysel PCD. The complete layout view of the Gysel PCD design is shown in Fig. 3-8. After fabrication, the structure was experimentally validated. The measured results are compared with simulation data in Fig. 3-9. Insertion loss is less than 0.25 dB from 15.5 to 17.3 GHz while the RL is greater than 20 dB and isolation is greater than 15 dB. Also, there is no observable difference between the insertion loss of port 2 and port 3.

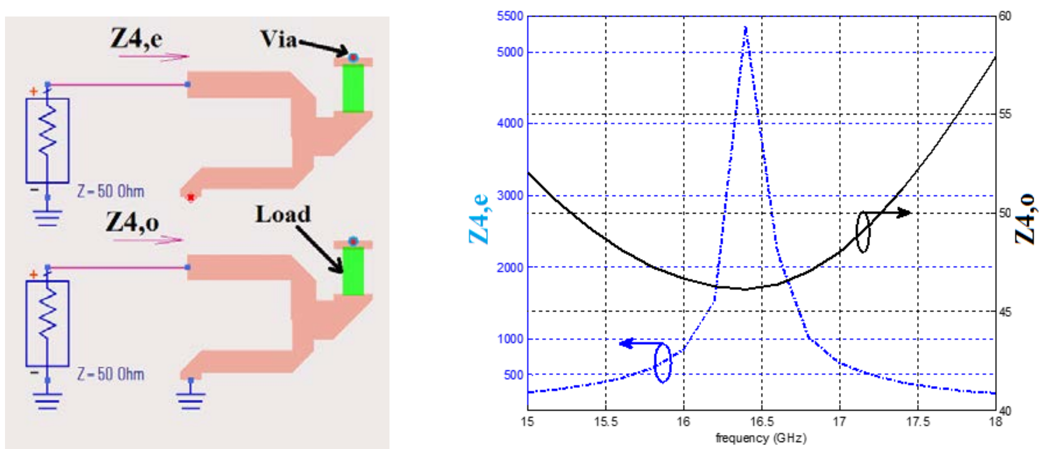


Fig. 3-7: Even-odd mode simulation to determine $\mathbb{Z}_4$, co-simulation schematic view (left) and even and odd mode impedance magnitude simulation results (right)

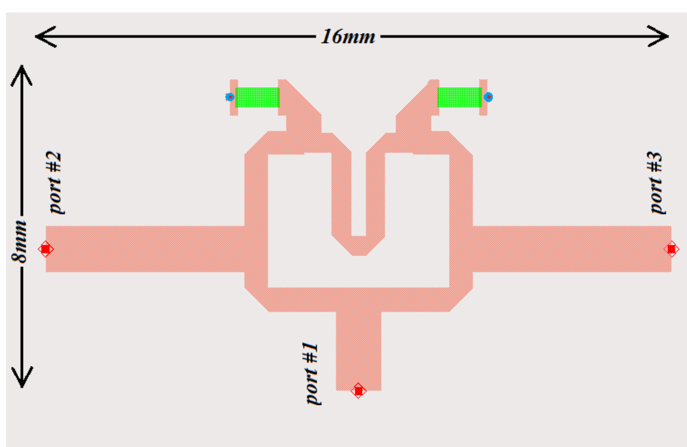


Fig. 3-8: Layout of proposed Ku-band Gysel PCD on RT-Duroid 5880

Fig. 3-10.a shows an implemented power amplifier module capable of combining four power amplifiers to measure the performance of the proposed Gysel PCD when connected sequentially.

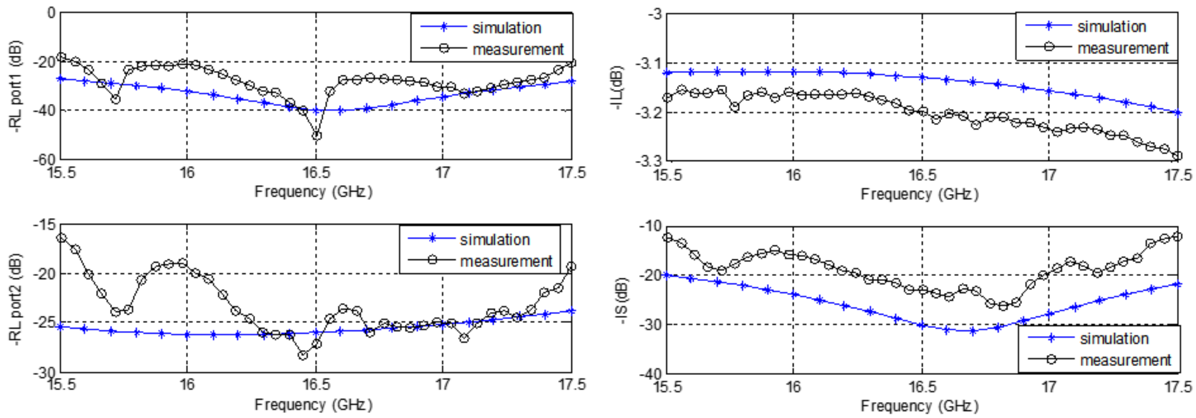
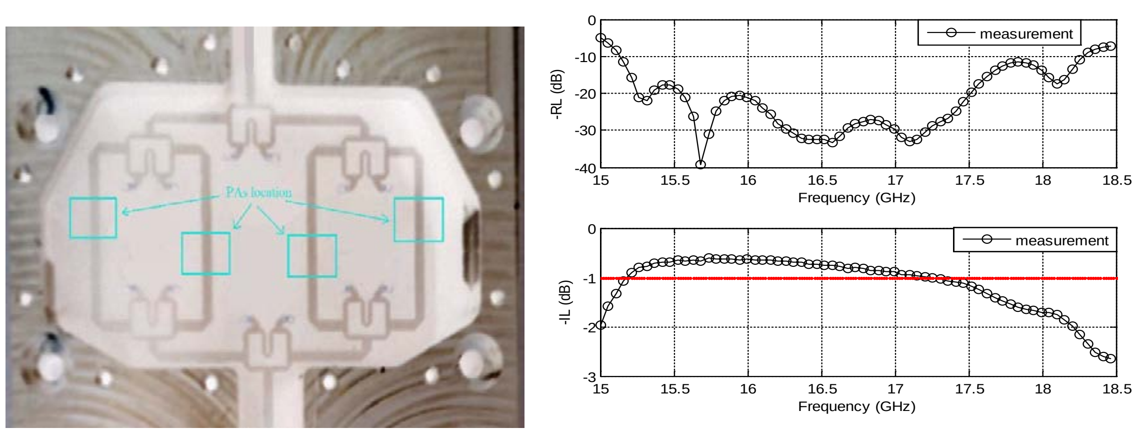


Fig. 3-9: Comparison between simulated and measured results of Ku-band Gysel PCD on RT-Duroid 5880

Through lines have been used in the place of PAs to measure the values of IL and RL of the Gysel PCD without the effects of power amplifiers. The measured S-parameters are shown in Fig. 3-10.b indicating a 12% fractional bandwidth with 20 dB return loss or better and operating at a center frequency of 16.5 GHz. The total insertion loss for the overall structure containing four Gysel PCDs was measured to be less than 1 dB, corresponding to 0.25 dB for each of the proposed Gysel PCD.



(a) (b)

Fig. 3-10: 4-PA combiner Ku-band module on RT-Duroid 5880 (a) photograph (45*55 mm^2), (b) measurement results

3.5 Designing the Power combining network

As aforementioned, the transmitter module is supposed to combine up to eight HPAs. Therefore, for each input and output of the combining network, seven PCDs in three stages are needed. Recall that in order to design a compact transmitter module, very small PCDs are required. The HPA designed in chapter 2 can provide an output power of 35 W when driven by 20 dBm (100 mW). Thus, the required input power for the transmitter module is about 1 W (30 dBm). To explain why so high level of isolation between the splitting ports is required, consider the situation when identical amplitude or equal phase signals are not combined. The effect of amplitude and phase imbalance between the two splitting ports on the combined ports is plotted in Fig. 3-11. In the case of amplitude, when two identical signals are applied (i.e., 0 dBm each) the combined power is 3 dBm and no power is dissipated in the isolation resistor(s). But if one of the signals is 1 dB less, then the combined power is reduced by approximately 0.5 dB and the rest is dissipated across the isolation resistor(s). In the case of phase, when two identical signals are applied (i.e., 0 dBm each) the combined power is 3 dBm and no power is dissipated in the isolation resistor(s). But if one of the signals is 30° out of phase, then the combined power is reduced by approximately 0.3 dB compared to the identical phase case and the rest is dissipated across the isolation resistor(s) [32].

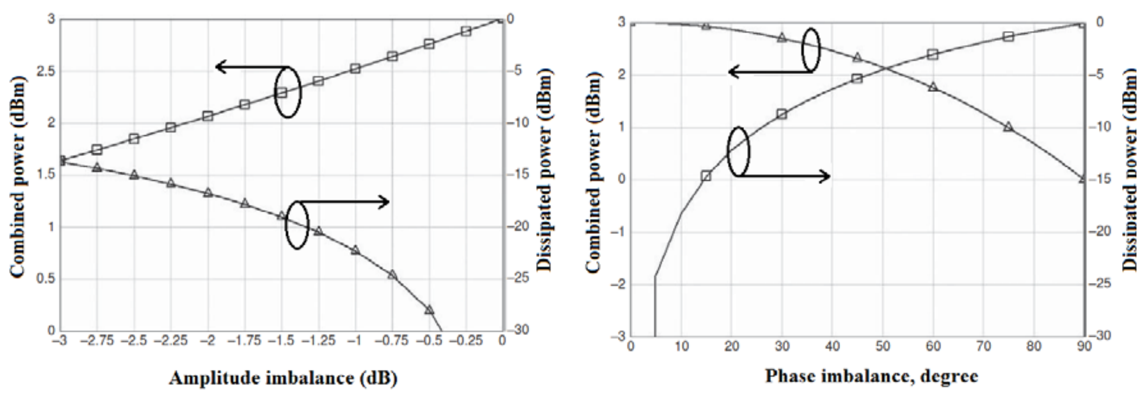


Fig. 3-11: Simple structure of single section Wilkinson PCD [32]

Hence Wilkinson structure is used for the PCDs at the input of the combining network because it is the most compact structure among the PCDs. Also, the maximum power delivered to the PCDs at the input of combining network is 1 W, so small size and medium power resistors can be safely used in Wilkinson structure. A typical single section Wilkinson PCD is displayed in Fig. 3-12.

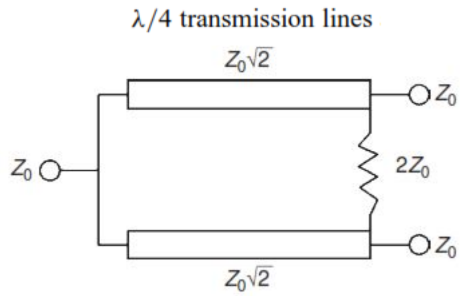


Fig. 3-12: Simple structure of single section Wilkinson PCD [32]

A full wraparound power chip resistor manufactured by beryllium oxide (BeO) material from US Microwave [94] has been utilized as an isolation resistor for the Wilkinson. The size of this resistor is 1.4 mm by 0.7 mm with 0.42 mm distance between its two pads. The resistor can operate up to 200 GHz and can dissipate 1 W power. A microstrip Wilkinson PCD was designed based on the selected isolation resistor. The configuration is displayed in Fig. 3- 13. The approximate size of the designed Wilkinson is 10 mm by 17 mm. The achieved simulation results by Keysight ADS Momentum is shown in Fig. 3-14. They demonstrate 34% fractional bandwidth for 0.15 dB insertion loss and/or 20 dB return loss.

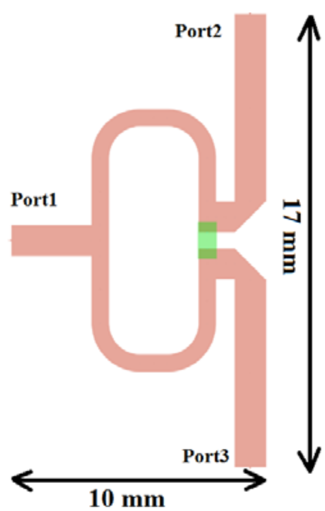


Fig. 3-13: Designed configuration of Wilkinson PCD

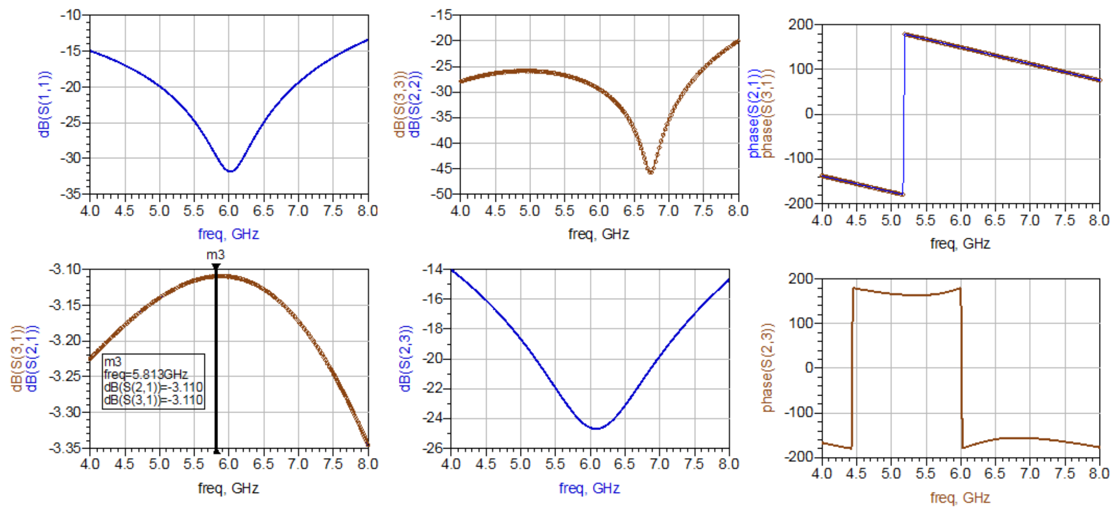


Fig. 3-14: Electromagnetic simulation results of designed Wilkinson PCD

Gysel structure is employed for the PCDs as the combining network. The suitable resistor for the Gysel PCD of the combining network should be single wraparound. This kind of resistors is terminated from one end to its metallic bottom plate. The bottom plate must be connected directly to the metallic carrier instead of the substrate. This scheme improves distributing the heat produced at the resistor when unbalance situation happens. US Microwaves [94] and Barry [95] have produced a variety of terminations from beryllium oxide (BeO) material suitable for this application. Two terminations from Barry were chosen. The first one operates up to 18 GHz and 40 W with a size of 3 mm x 1.5 mm. It is utilized for the first and second stage of the power combining network. The second one operates up to 8.4 GHz and 100 W with the size of 6.35 mm x 6.35 mm and employed for the third stage.

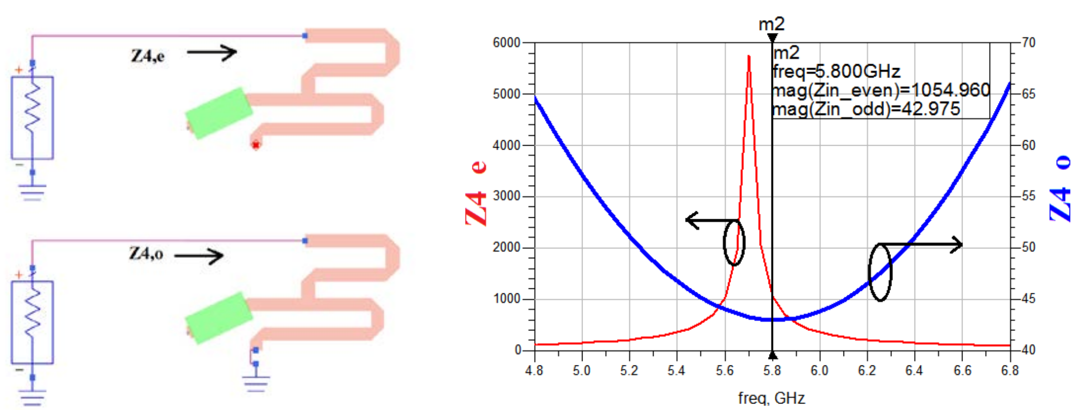


Fig. 3-15: Even-odd mode simulation to determine $\mathbb{Z}_4$, co-simulation schematic view (left) and even and odd mode impedance magnitude simulation results (right)

The schematic needed to perform the co-simulation of the even and odd mode of the $\mathbb{Z}_4$ of the first kind of the Gysel PCD is shown in Fig. 3-15 along with its simulation results. Subsequently, the whole Gysel PCD was created and tuned to achieve the best results in the desirable frequency range. The configuration of the designed Gysel PCD for the first stage of the combining network is displayed in Fig. 3-16 and its simulation results obtained by Keysight ADS Momentum plotted in Fig. 3-17. The IL is less than 0.25 dB from 5.1 GHz to 6.4 GHz with about 22% fractional bandwidth. At the same frequency range, the RL is greater than 20 dB. Isolation is also greater than 15 dB from 5 GHz to 7GHz. The second version of the Gysel PCD for the second stage of the power combining along with its electromagnetic simulation results are displayed in Fig. 3-18 and Fig. 3-19. This version shows better results with 20 dB return loss of the combining port (port1). Fig. 3-19 also shows the seen impedance of the even and odd mode of $\mathbb{Z}_4$.

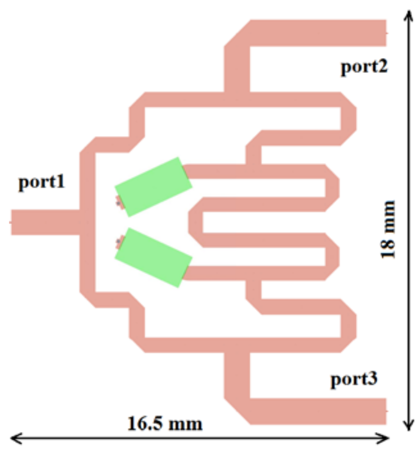


Fig. 3-16: Designed configuration of Gysel PCD for the first stage

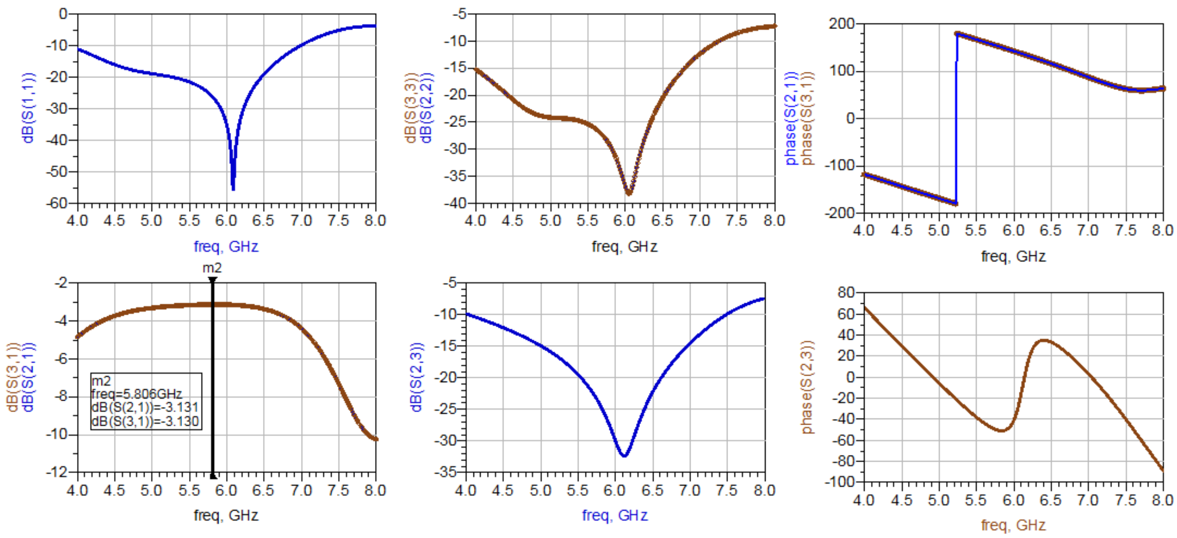


Fig. 3-17: Electromagnetic simulation results of designed Gysel PCD shown in Fig. 3-16

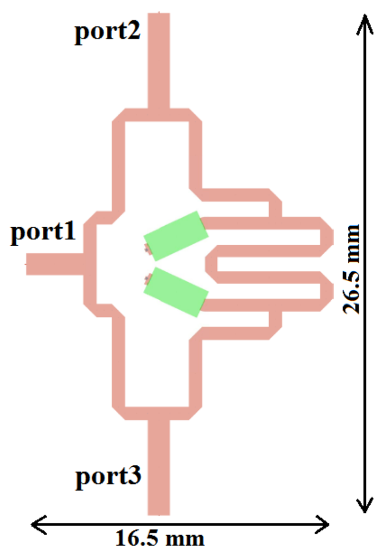


Fig. 3-18: Designed configuration of Gysel PCD for the second stage

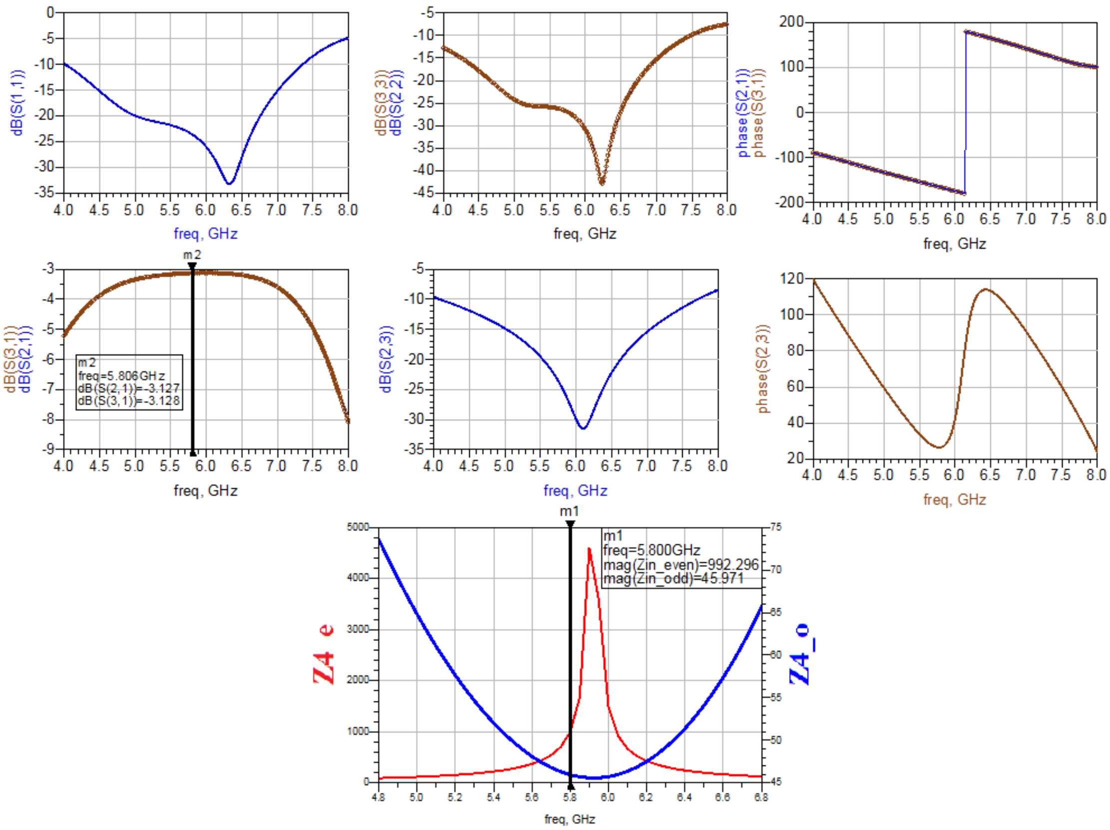


Fig. 3-19: Electromagnetic simulation results of designed Gysel PCD shown in Fig. 3-18

The third version of the Gysel PCD was designed using the larger resistor. The schematic used to carry out the co-simulation of the even and odd mode of the $\mathbb{Z}_4$ of this kind of the Gysel PCD is shown in Fig. 3-20 along with its simulation results. The entire layout of this Gysel PCD is shown in Fig. 3-21. The height of the third version is almost twice of the first stage. The electromagnetic simulation results obtained by Keysight ADS Momentum are displayed in Fig. 3-22. The bandwidth for the IL less than 0.25 dB is the same as the last two versions as well as the RL of combined port (port1). The bandwidth for RL greater than 20 dB at splitting ports (ports 2 and 3) and isolation greater than 15 dB, is limited in this case.

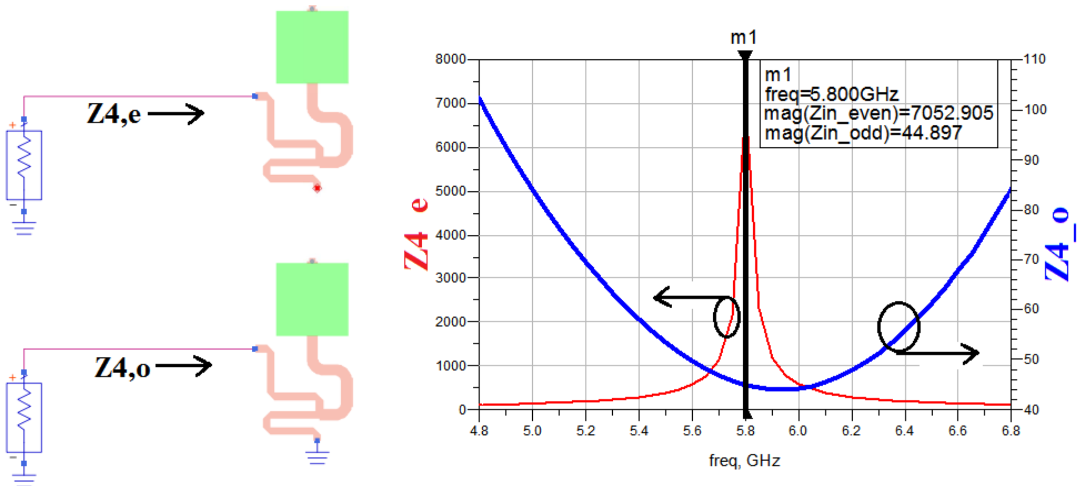


Fig. 3-20: Even-odd mode simulation to determine $\mathbb{Z}_4$, co-simulation schematic view (left) and even and odd mode impedance magnitude simulation results (right)

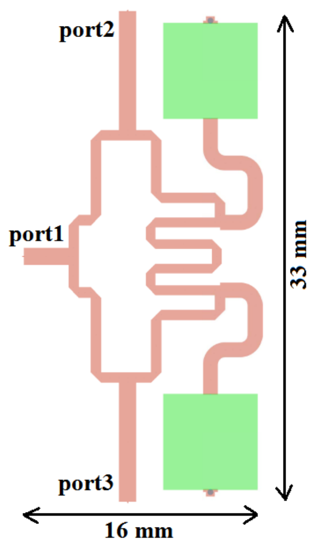


Fig. 3-21: Designed configuration of Gysel PCD for the third stage

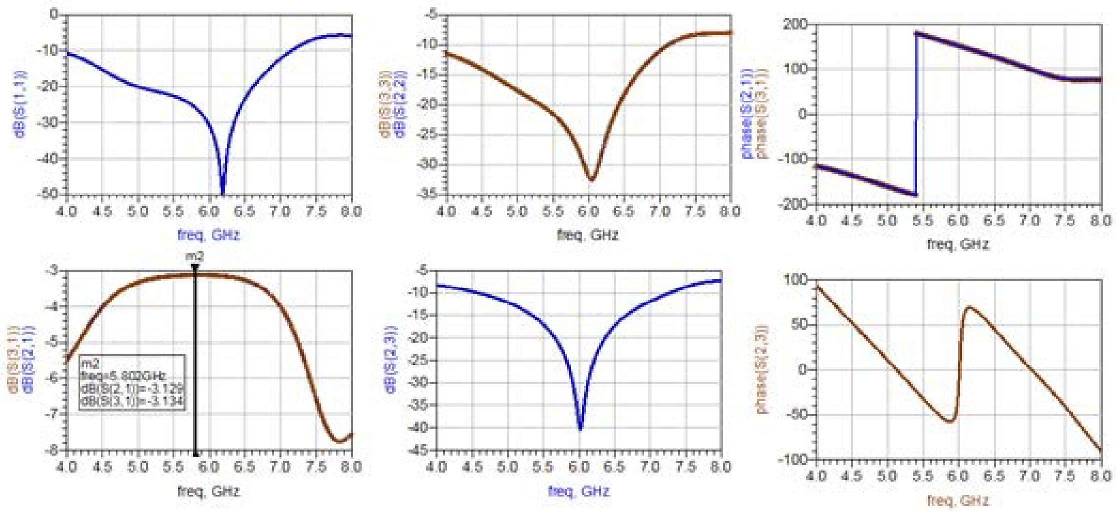


Fig. 3-22: Electromagnetic simulation results of the third designed Gysel PCD shown in Fig. 3-21

3.6 Conclusion

In this chapter, the required PCDs for the power combining network were introduced. The power combining network is supposed to combine up to eight HPAs. It consists of three stages at the input and three stages at the output. One Wilkinson PCD and three different Gysel PCDs were designed to achieve a small combining network. The designed Wilkinson PCD is utilized for the input of the combining network. Each of the three designed Gysel PCDs is used at one stage of the power combining output.

The employed Gysel PCD is a modified configuration of its conventional version. A design method based on even-odd mode analysis was also performed for the proposed Gysel configuration and a design algorithm provided to control the design process.

Each of the PCDs provides more than 20% fractional bandwidth for greater than 20 dB return loss, less than 0.25 dB insertion loss and greater than 15 dB isolation. Their amplitude and phase imbalance is very negligible. All these structures are more compact in comparison with other counterparts with the same power handling.

Chapter 4

Microstrip-to-waveguide transition integrated with a microstrip coupler

4.1 Introduction

Transitions are key elements in communication systems when different kinds of transmission media are used. Among transitions, microstrip-to-waveguide transitions (MWT) are extensively used. In fact, recent developments in microwave circuits and solid-state technology have led to the ever-increasing use of planar circuit packages, highlighting microstrip lines as ones of the most widely used transmission media in RF/microwave system design. On the other side, waveguides are present in front-end of transmitters and receivers due to their low losses and high power capabilities. Therefore, it is necessary to use reliable microstrip-to-waveguide transitions to optimize the transmission chain. In this chapter, a robust and suitable MWT structure was designed for the transmitter module and innovative design approaches applied to make it more compact and efficient.

Also, a transmitter without a power monitor is not reliable. Any degradation/dysfunction in the transmitter performance must be detected during the normal operation of the transmitter. To monitor the power of a transmitter, a coupler is required to get a sample of the main signal power. Couplers are usually implemented using waveguides or planar lines. The main advantages of waveguide couplers are their very high power handling and very low insertion loss, but they are very bulky. To design a compact transmitter, planar (microstrip) couplers remain the only choice. In this research, an innovative design is proposed to significantly reduce the insertion loss of the coupler from the main signal power.

4.2 MWT structures

In the last few years, different MWT transitions have been reported in the literature [96]-[107]. Although most of them exhibit excellent performance, they present several disadvantages: difficulty in manufacturing [96]-[98], [101], [102], high sensitivity to fabrication tolerances [96], [98], not sufficiently robust [100], [103], [104], inappropriate if the waveguide should be easily separated from the dielectric board [105], and incomplete sealing and waterproofing [106], [107].

Also, a key feature to classify MWT structures is how the microstrip line can be inserted into the waveguide. The microstrip board can be located perpendicular to the waveguide propagation direction and inserted through a window devised in the waveguide wider wall, as shown in Fig. 4-1. In this method (referred to perpendicular patch transition), the transition is performed by a microstrip patch antenna [103], [108] when one end of the waveguide is closed by a metallic plate at a distance of about a quarter wavelength of the center operation frequency. In an other method (parallel patch transition), the microstrip board is parallel to the waveguide propagation direction, at about a quarter of the wavelength away from the back-short end of the waveguide [103], [104], [109] as in Fig. 4-2. The major disadvantage of these two techniques is that they are not sealed because of the window created on the waveguide wall.

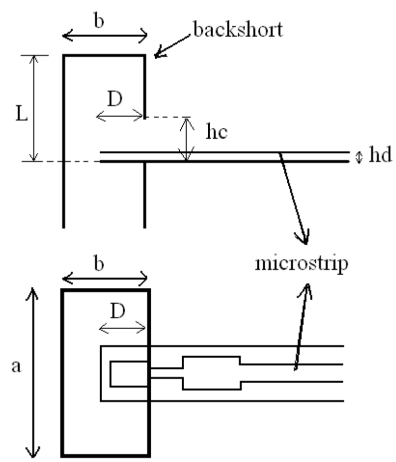


Fig. 4-1: Perpendicular patch transition [103]

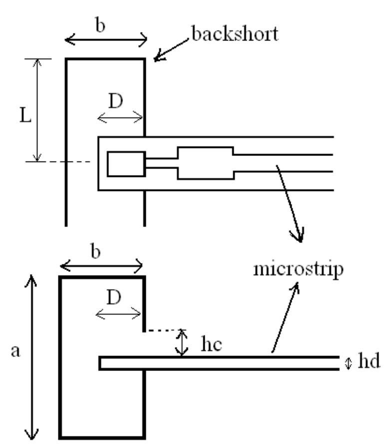


Fig. 4-2: Parallel patch transition [103]

To overcome this disadvantage, one can use a coaxial line as interface [105]. In this scheme, microstrip board lies on the wider waveguide wall. A coaxial line transfers the signal into the waveguide through its wall thickness. The internal metal of the coaxial line is soldered to the microstrip line through a via and comes down into the waveguide to operate as a probe (Fig. 4-3). A metallic ring (bush) is usually used to match the MWT for a wider bandwidth. Although this kind of MWTs is sealed and can provide low insertion loss due to its metallic structure, it is not a suitable design because of its sensitivity to the fabrication tolerances and difficulty of taking apart the sections including the microstrip board and the waveguide.

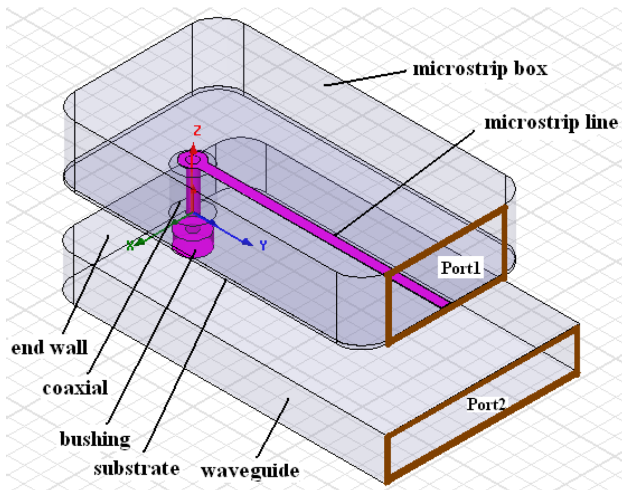


Fig. 4-3: Coax interface transition [105]

Another way to implement the transition between the microstrip and the waveguide is fulfilled by the quasi-Yagi antenna as displayed in Fig. 4-4. In this scheme, the microstrip board is inserted into the waveguide from one of its ends [106].

Due to low radiation efficiency of microstrip antennas, MWTs designed by using a microstrip antenna have relatively large insertion loss. Therefore, to enhance the efficiency of the MWT and consequently the transmitter module, other mechanisms of transitions were investigated. Designing the MWT by using the slotted ground plane is the best technique that can achieve the minimum insertion loss [110], [111]. In these structures, the coupling is done through a slot created in the ground plane of the substrate and the end of the microstrip line must be shorted to the edge of the slot line. The MWT proposed in [110] and shown in Fig. 4-5 is very suitable for power amplifier applications. This design is very robust and very stable with respect to manufacturing and assembly variations. The mechanical aspects of the transition’s implementation are so that seamless integration into the overall package manufacturing and assembly process can be achieved without sacrificing the electrical performance. The structure proposed in [111] is also innovative but there is a limitation that the thickness of the waveguide's wall underneath the substrate must be narrow, no more than 2 mm.

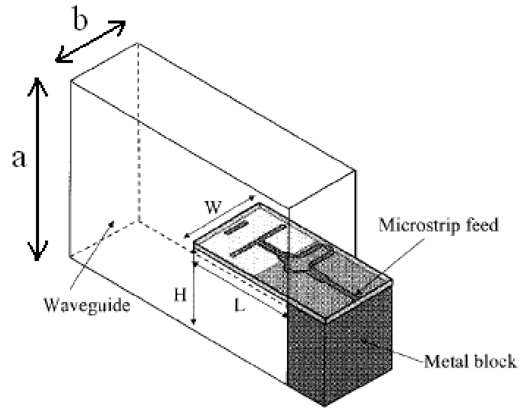


Fig. 4-4: Inserting microstrip board into the waveguide [106]

There are also other different techniques to design MWTs, e.g. using a substrate integrated waveguide (SIW) as an interface between the waveguide and the microstrip [112], [113] or utilizing a dielectric waveguide [114] but they do not have low loss performance as well as compact size.

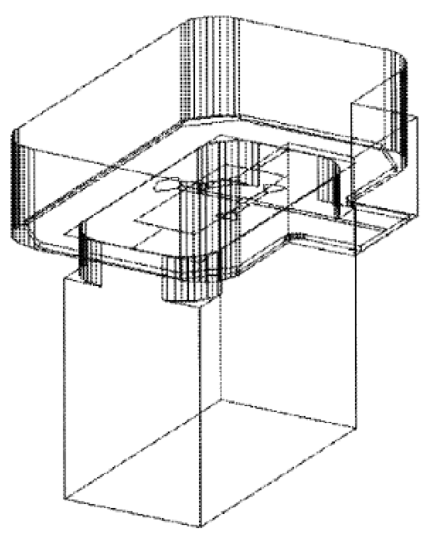


Fig. 4-5: Slotted ground plane transition [110]

4.3 Proposed MWT structure

In this work, we started with the structure reported in [110] (Fig. 4-5) using a microstrip board above the open end of the waveguide, where the coupling is achieved by a slot etched in the ground plane. The microstrip line is crossed above the waveguide aperture at the middle of it and then shorted to the edge of the slot through a quarter-wavelength open-ended stub. The structure is enclosed by a cavity and the microstrip inserted to the cavity through a channel.

This configuration exhibits important advantages. First, it is not sensitive to reasonable manufacturing tolerances. It can be also easily assembled to or separated from the waveguide section. Note that the microstrip section is sealed to avoid exposing the HPAs from dust, moisture or other damaging factors. Also, the waveguide can be directed in parallel with the substrate by using a waveguide bend at any desirable distance from the substrate. All these features make the selected structure an excellent candidate for the transmitter module. However, rescaling the structure reported in [110] for frequency ranges less than 30GHz and dielectrics with lower permittivity will come out with undesirable large-size structures, mainly due to the quarter-wavelength open-ended stub and the large waveguide aperture.

Hence, this structure needs to be largely modified. The modifications presented here, make the structure more compact and efficient, thus suitable for the proposed transmitter module. More parameters were introduced that need to be optimized. To save time, an efficient design process has been setup by dividing all the parameters into three groups and optimizing the parameters of each group separately instead of optimizing them in a single step.

In the proposed approach, in order to minimize the size, the $\lambda/4$ open stub at the end of the microstrip line has been bent to be directed along the slot instead of being perpendicular to it. The $\lambda/4$ open stub can be bent toward both sides as a Tee-shape (Fig. 4-6) or only bent toward one side. Several alternatives can be retained instead of rectangular shape slot and many configurations were examined and simulated. Finally, a "+" shape slot located at the center of the waveguide aperture has been retained to achieve the maximum bandwidth and coupling between the microstrip line and the waveguide.

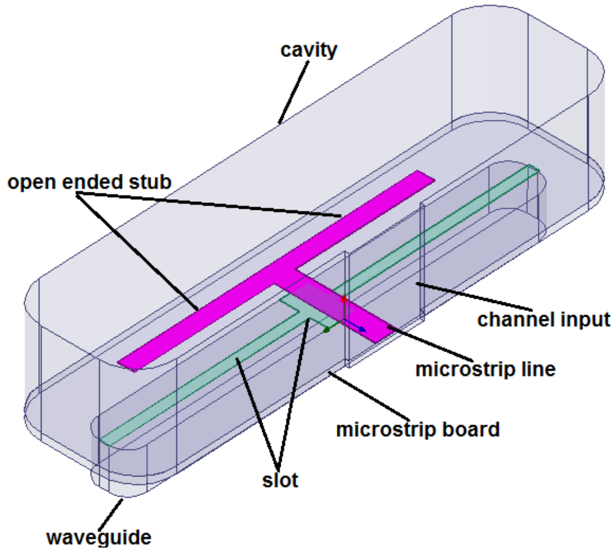


Fig. 4-6: The structure used in the first design step

Another improvement has been accomplished by reducing the waveguide height. Reducing the waveguide height (b) has two advantages. Not only a more compact configuration is obtained but also based on equation (4-1), the characteristic impedance of the waveguide (Z_0) is decreased [115]. Therefore, it would be closer to the characteristic impedance of the microstrip line (usually 50Ω). Hence microstrip line can be matched more conveniently with a reduced height waveguide. The waveguide aperture can be converted to its standard dimensions by designing a couple of waveguide capacitance steps.

$$Z_0 = 465 \frac{b}{a} \sqrt{\frac{\mu_r}{\varepsilon_r}} \frac{1}{\sqrt{1-(f_c/f)^2}} \ \Omega \qquad (4\text{-}1)$$

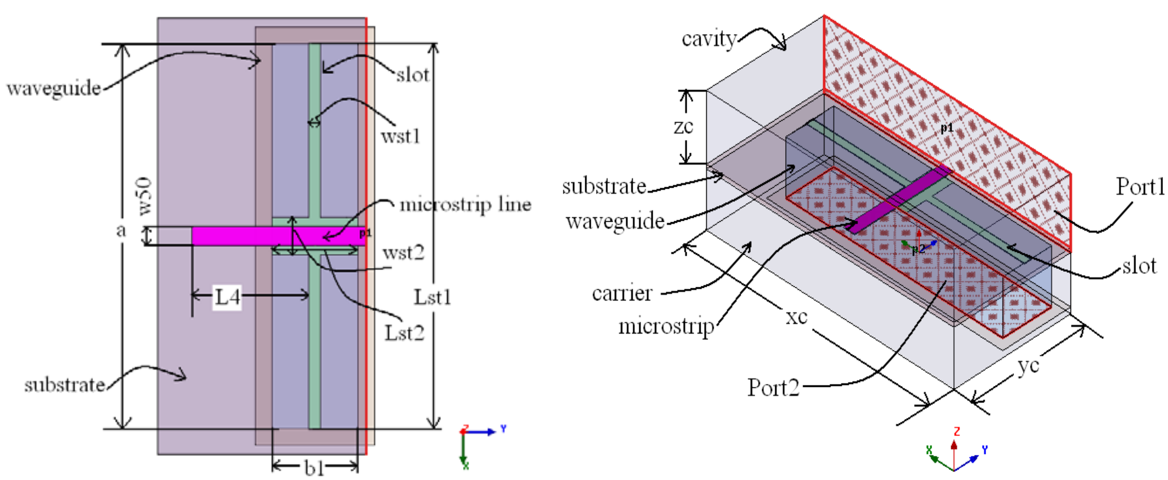
where a is the waveguide width, μ_r and ε_r the respective relative permeability and permittivity of the propagating medium inside the waveguide, and f_c the cut-off frequency.

The substrate must be enclosed in a box called cavity, as depicted in Fig. 4-6. The cavity dimensions should be designed so that the unwanted resonances are prevented in the operating frequency range. The height of cavity should be around 5 mm for the range from 4 GHz to 40 GHz. The microstrip line is inserted into the cavity through a small channel.

To increase the bandwidth, a two-stub matching circuit was used instead of one stub while the matching circuit was placed in the channel to reduce the cavity size and accordingly the MWT size. Note that including the matching network in the cavity not only increases the cavity size but also can cause undesirable resonances in the operating frequency band and degrade the structure performance.

As for the design procedure itself, there are many useful parameters that can be optimized. Hence, we designed the MWT step-by-step to reduce the required optimization time. In the first step, we designed a transition between a straight microstrip line and a waveguide with a reduced height, the same as in Fig. 4-6. Thus, the parameters depicted in Fig. 4-7, i.e., the dimensions of the slot (wst1, wst2, Lst1, Lst2), the dimensions of the cavity (xc, yc, zc), the length of the open-ended microstrip line to be continued after the slot (L4), and the initial height of the waveguide (b1), must be optimized to achieve high return loss and small insertion loss. Because the open-ended stub operates as a short-circuit at the edge of the slot, the structure performance is relatively insensitive to the width of the open-ended stub. Also, at this stage, it is not necessary to set the width of the input microstrip line to 50 ohms because a matching network will be included afterward.

Note that, as already mentioned, the initial height of the waveguide (b1) was specified to a value less than its standard height (b). In the second step, a waveguide of height b1 was adapted to a waveguide of height b. This was performed through designing a couple of capacitive steps in a separate design procedure by optimizing the values of Lw1, Lw2, and b2, as shown in Fig. 4-8.

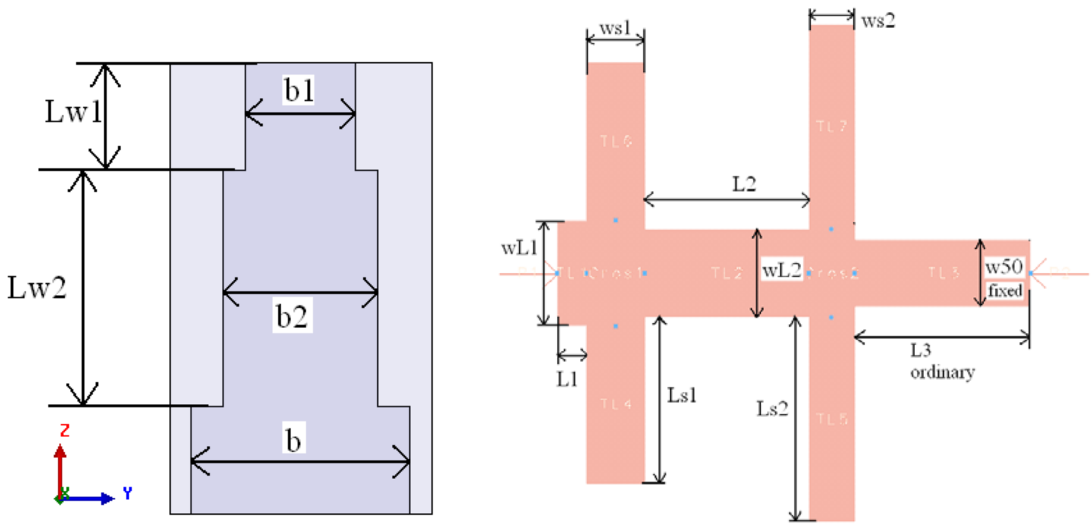


(a) (b)

Fig. 4-7: The structure used in the first design step (a) top view and (b) 3-D view

In the third step, a microstrip matching network at the beginning of the microstrip line was designed. As shown in Fig. 4-8, a double stub matching network was designed by optimizing the eight parameters, wL1, L1, ws1, Ls1, wL2, L2, ws2, and Ls2.

The simulations of the first and second step must be performed in a 3-D electromagnetic simulator. In this research, both Ansys HFSS and CST Microwave studio commercial software were utilized. Note that optimizing the matching network along with the already designed parts of the transition structure in a 3D-EM simulator will require a huge CPU time. Therefore, the microstrip matching network can be independently optimized by a 2-D electromagnetic simulator, like Keysight ADS Momentum, and using the S-parameters obtained from the first step.



(a) (b)

Fig. 4-8: The structure used in the second design step (a) and third design step (b)

Although many parameters must be determined, the proposed procedure, which consists to split the whole structure into three parts, will significantly reduce the required simulation time. Therefore, 9, 3, and 8 parameters must be optimized separately for, respectively, the first, second and third steps instead of simultaneously optimizing 20 parameters of the whole structure. In other words, the three different steps lead to $9!*3!*8! \sim 88e^{9}$ permutations for each optimization iteration in the EM simulator while the whole structure will require $20! \sim 24e^{17}$ permutations. Also a smaller structure reduces the total number of meshes and consequently the simulation time. Finally, the whole structure must be simulated in a 3-D electromagnetic simulator for final tuning and trimming.

The proposed MWT can be scaled and designed for different frequency ranges [116] and [40]. Fig. 4- 9 shows a photograph of the back-to-back MWT implemented in X-band and Fig. 4- 10 displays the S-parameters results of the implemented proposed MWT in X-band and Ku-band. As shown in Fig. 4- 10, a good agreement between simulated and measured data is observed for both the X- and Ku-band MWT structures. Also, both MWTs exhibit an insertion loss less than 0.2 dB (for a single MWT) as well as a return loss greater than 20 dB at 12 % of their center frequency. The last point about the proposed MWT is its low sensitivity to the manufacturing tolerances [116].

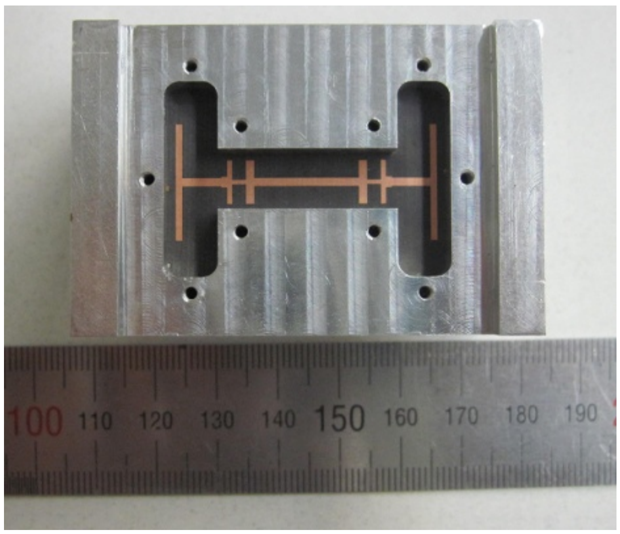
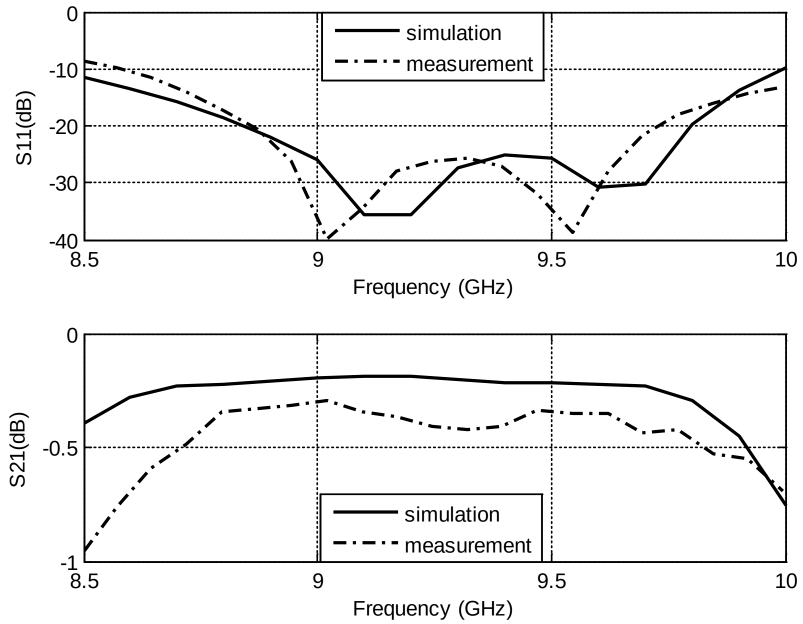
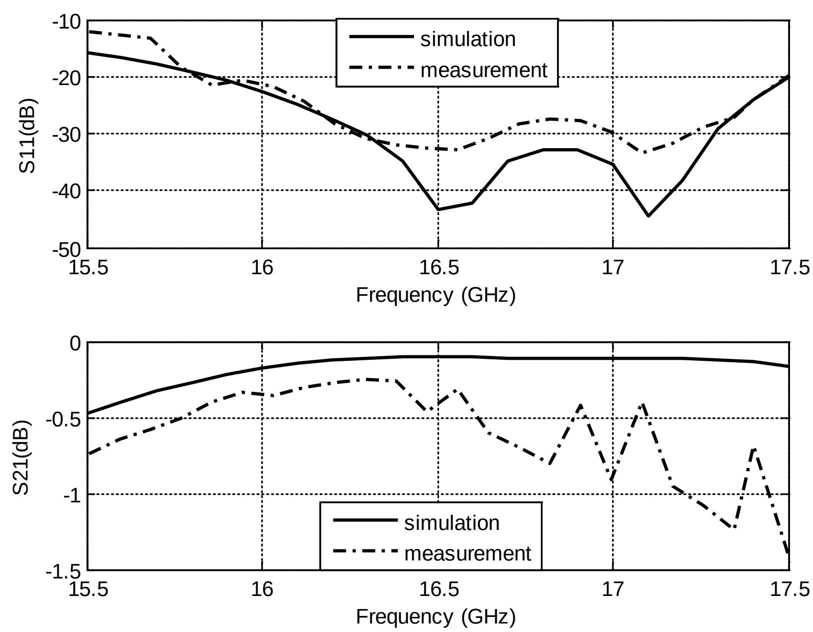


Fig. 4-9: A photograph of the manufactured X-band transition



(a)



(b)

Fig. 4-10: Simulation and measurement results of the proposed MWT implemented in X-band (a) and Ku-band (b)

4.4 Microstrip coupled line coupler

The main purpose of couplers is sampling a signal to monitor some features, e.g. power level or voltage level. Each system, particularly for long-term uses, must have at least one coupler at the output of the transmitter to monitor the power level delivered to the antenna. The coupled line couplers, or more simply couplers, can be usually implemented by using waveguides [117] or planar techniques such as microstrip lines [66]. Microstrip couplers (MC) are more compact but they may produce more losses in comparison with waveguide couplers. On the other side, although waveguide couplers exhibit very low losses, they are very massive for many radio-communication systems. For each kind of couplers, in addition to having all ports matched, three parameters must be considered namely, coupling (CO), directivity (DI), and isolation (IS). In regard to Fig. 4-11, these parameters can be defined as

$$CO^{dB} = 10\log_{10}\left(\frac{P_1}{P_3}\right) = -|S_{31}|^{dB} \tag{4-2}$$

$$IS^{dB} = 10\log_{10}\left(\frac{P_1}{P_4}\right) = -|S_{41}|^{dB} \tag{4-3}$$

$$DI^{dB} = 10\log_{10}\left(\frac{P_3}{P_4}\right) = 10\log_{10}\left(\frac{P_3}{P_1}\right) + 10\log_{10}\left(\frac{P_1}{P_4}\right) = |S_{31}|^{dB} - |S_{41}|^{dB} = -CO^{dB} + IS^{dB} \tag{4-4}$$

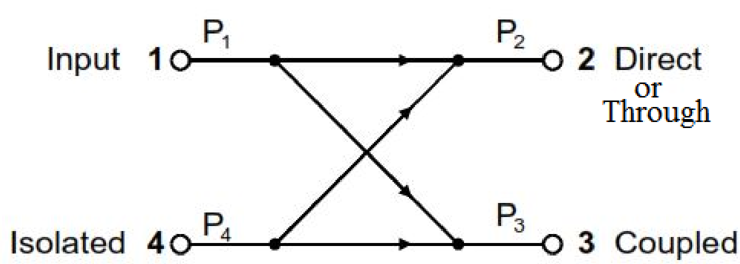


Fig. 4-11: Signal flowchart of a coupled line coupler [118]

Waveguide couplers cannot be employed for the proposed transmitter because they cannot be fitted in the available space of the proposed compact transmitter module thus MC is the only choice.

MCs are usually designed by using two $\frac{\lambda}{4}$ parallel lines close to each other (Fig. 4-12). The separation distance between the two lines determines the coupling level.

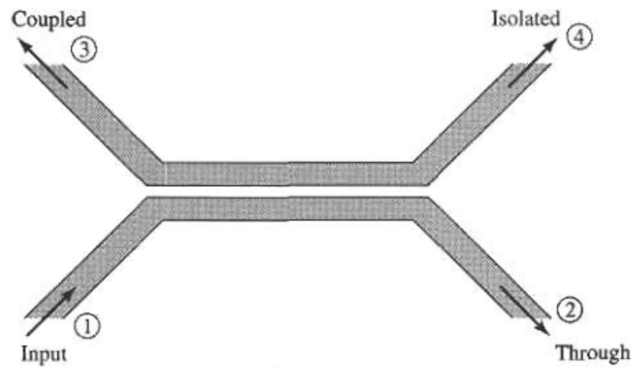


Fig. 4-12: A typical layout of the microstrip coupled line coupler [118]

Another drawback of the MC is its low directivity. The directivity of the MCs is typically around 6 dB and it would be even lower when a larger coupling coefficient is required. Improving the directivity cannot be achieved without sacrificing the other features of the MC [119]. To show a rough relation between the coupling, directivity and isolation values, a typical microstrip coupler was simulated when the gaps between two lines of the MC was varied. Simulations was performed with a specific substrate. The obtained simulation results around 5.8 GHz are summarized in Table 4-1.

Table 4-1: Rough comparison between several of features of a simple MC based on different gaps between two lines

CO	11	12.5	14	16	21	24	25	27	29	31	33	37
IS	24	25	25	26	28	30	30.5	32	33	35	36	40
DI	13	12.5	9	8	7	6	5.5	5	4	4	3	3

The quarter wavelength of the guided wave in the selected substrate is 8.8 mm. Hence the MC will add about 1 cm to the length of the transmitter module opposite to the goal of being compact.

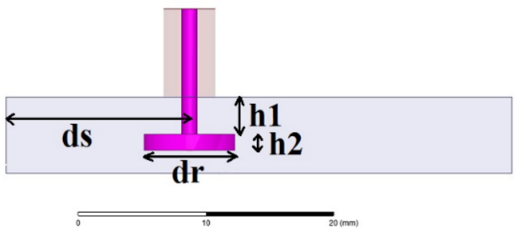
In this research, an innovative and very compact configuration is then proposed and implemented with a directivity greater than 10 dB for 10% fractional bandwidth.

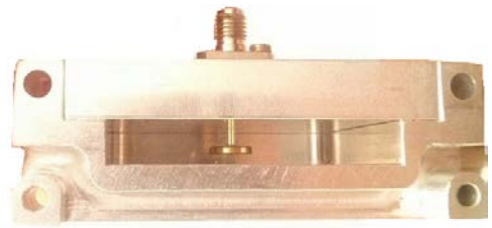
This technique was developed by integrating the MWT and the MC. As aforementioned, the microstrip line in the MWT must be extended by a length of $\frac{\lambda_g}{4}$ in order to be shorted to the edge of the slot. In the proposed MWT, the $\frac{\lambda_g}{4}$ line was bent to achieve a more compact configuration. Here, the $\frac{\lambda_g}{4}$ line was not bent to both sides, as in Fig. 4-9, but just bent to one side to improve the directivity.

This $\frac{\lambda_g}{4}$ line is also used as part of the MC. By using this technique, because the coupling starts from the point where the through line becomes a short-circuit, the MC does not have any effect on the MWT performance and, consequently, on the output signal from the HPAs going to the antenna. As mentioned, the width of the $\frac{\lambda_g}{4}$ line has a negligible effect on the MWT performance. Therefore, the width of the $\frac{\lambda_g}{4}$ line is used to enhance the directivity of the MC. By adjusting the width of the $\frac{\lambda_g}{4}$ line, high directivity and isolation can be achieved when a coupling coefficient higher than 30 dB is needed. Adjusting the width of the $\frac{\lambda_g}{4}$ line cannot improve the directivity of a conventional MC without sacrificing the return loss and insertion loss of the through path. Another advantage of the proposed technique is that the required space for MC and MWT is shared, thus a more compact transmitter module is achieved.

4.5 Waveguide-to-coaxial adapter

To measure the performance of the designed MWT by a Vector Network Analyzer (VNA), a Waveguide-to-coaxial adapter (WCA) is required to convert the waveguide port to a coaxial port. As described earlier, to match more conveniently the microstrip line to the waveguide as well as to achieve a more compact design, the height of the waveguide must be reduced. The height of the waveguide was chosen to be 6 mm. An height smaller than 6 mm can be theoretically chosen to achieve more compact design but many difficulties may appear during the fabrication process and the measurement procedure. Therefore, a waveguide-to-coaxial adapter (WCA) with the aperture size of 40 mm * 6 mm was retained (Fig. 4-13). The coaxial connector has a dielectric diameter of 4.1 mm (Teflon with $\varepsilon_r = 2$) and a metal diameter of 1.28 mm. The height of the metal pin inserted into the waveguide (h_1) as well as its distance from the waveguide back-shorted (d_s) are the effective parameters to match the ports. The value of d_s should be close to a quarter of the wavelength at the center of the desirable frequency range. To improve the matching, a ring was also added at the end of the metal pin inside the waveguide. It is possible to obtain a broadband matching by optimizing the height (h_2) and the diameter (d_r) of the ring.





(a) (b)

Fig. 4-13: Structure of the waveguide to coaxial adapter, (a) simulation drawing (side view) and (b) manufactured prototype (front view)

A WCA called WCA#1 was designed and fabricated achieving greater than 20 dB return loss for about 20% fractional bandwidth. However, it was too sensitive to the fabrication tolerances. Therefore, the structure was redesigned to extend the bandwidth, leading to less sensitivity to the fabrication tolerances. Increasing the ring diameter to an optimum value is a good way to achieve the widest possible bandwidth. Table 4-2 shows the parameter values of the two designed and fabricated WCAs while Fig. 4-14 compares the return loss of both designed WCAs. The bandwidth of the second prototype (WCA#2) is 2.7 GHz for 20 dB return loss (46% of fractional bandwidth), i.e., more than twice of the bandwidth of WCA#1. The fabricated WCA#2 was then used to measure the MWT performance through the VNA.

Table 4-2: The parameters of both implemented WCAs (all dimensions are in mm and with reference to Fig. 4-13)

	h1 (mm)	h2 (mm)	Ds (mm)	Dr (mm)
WCA #1	3.4	1.5	9.8	4
WCA #2	2.9	1.3	14.5	7.2

However, there are different ways to calibrate the VNA. SOLT (Short-Open-Load-Through) [120] calibration method, also called full 2-ports, is suitable for nondispersive transmission lines although it is also usually employed for nondispersive media. TRL (Through-Reflect-Line) [121] and LRL (Line-Reflect-Line) [122] calibration methods are more suitable for dispersive transmission lines such as waveguides. With these approaches (TRL or LRL), the effects of WCAs were completely removed from the responses of the device under test thus more accurate results will be obtained. The Agilent VNAs have the options to calibrate with the TRL method [123] while the Anritsu VNAs have the options to calibrate with the LRL method [124]. Both VNAs as well as their nondispersive calibration methods (LRL and TRL) were then used in this research.

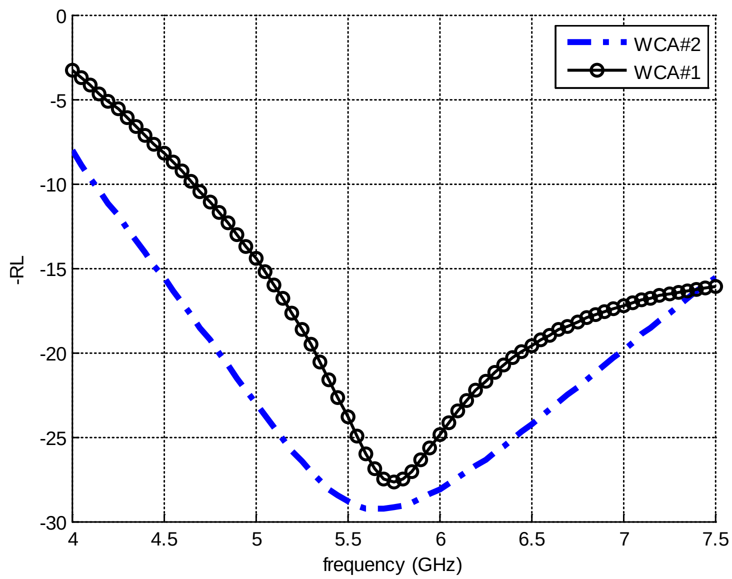
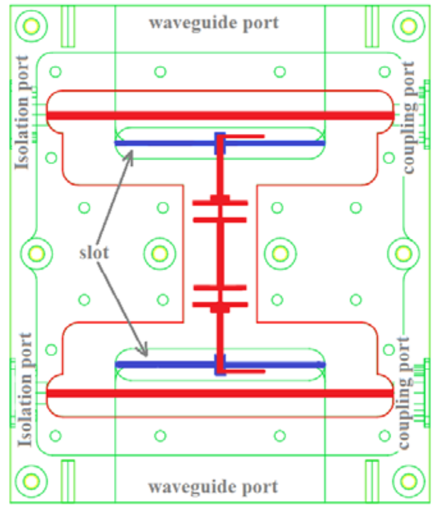


Fig. 4-14: Return loss of both designed WCAs

4.6 Integrated microstrip-to-waveguide transition and microstrip coupler

Based on the proposed structure, a microstrip-to-waveguide transition combined with a microstrip coupler (MWT&MC) was designed at 5.8 GHz with more than 10% fractional bandwidth. The standard waveguide proper to the targeted frequency range is the WR159, operating from 3.7 GHz to 7.4 GHz, with dimensions of 40.38 mm * 22.19 mm. Because the proposed MWT&MC is assumed to excite a custom-designed antenna in a unit module and also to be more convenient, the dimensions of 40 mm * 20 mm were chosen for the waveguide aperture.

The designed structure was simulated in both Ansys HFSS and CST Studio Suite. A back-to-back version of integrated MWT&MC was also simulated and then implemented to verify its performance. The manufactured prototype along with its drawing map is displayed in Fig. 4-15.



(a) (b)

Fig. 4-15: (a) manufactured prototype of the MWT&MC and (b) its drawing map

The results of the return loss and insertion loss of the designed MWT&MC are compared in Fig. 4-16 and Fig. 4-17, respectively. It is observed that the return loss is greater than 20 dB and the insertion loss (for a single MWT&MC) is less than 0.2 dB over about 15% fractional bandwidth.

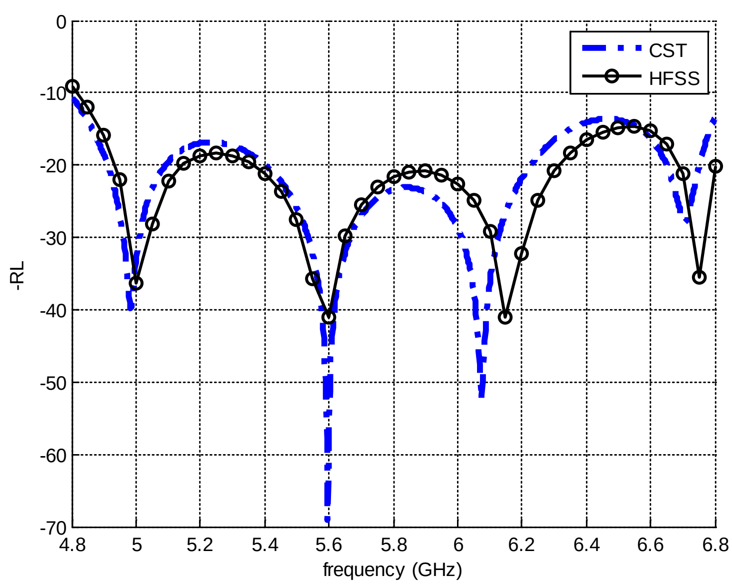


Fig. 4-16: Comparison of the return loss of the designed MWT&MC

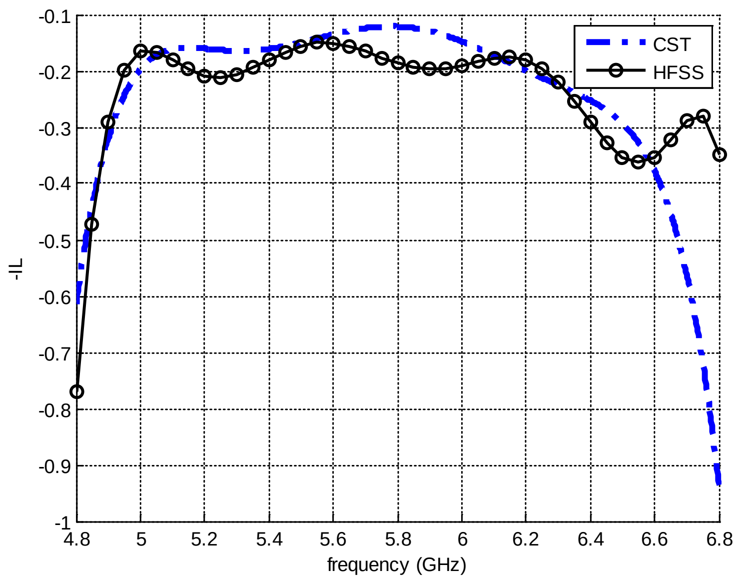


Fig. 4-17: Comparison of the insertion loss of the back-to-back MWT&MC

The two notches observed in Fig. 4-16 at 5 GHz and 6.7 GHz are caused by the package of the back-to-back MWT&MC structure. For a single MWT&MC, these notches are not observed. Also, coupling, isolation, and directivity of MWT&MC are displayed in Fig. 4-18, Fig. 4-19, and Fig. 4-20, respectively. The coupling factor is about 37.5 dB. The variation of the coupling factor for 10% fractional bandwidth is 0.5 dB and 1.5 dB for 25% fractional bandwidth. Thus, the coupling flatness of the proposed MWT&MC in regard to microstrip couplers is very good. Greater than 10 dB directivity was achieved from 5.6 GHz to 6.2 GHz (10% fractional bandwidth). The directivity factor is more than triple of a conventional microstrip coupler with regard to Fig. 4-12. The HFSS and CST simulation results, shown in Fig. 4-16 to 4-20, confirm each other. For example, the bandwidth of 20 dB return loss of HFSS simulation is 100 MHz wider than CST simulation (equivalent to 10%), the bandwidth of 0.25 dB insertion loss of both simulators are the same, or the discrepancies between the directivity of HFSS and CST simulations are less than 2%.

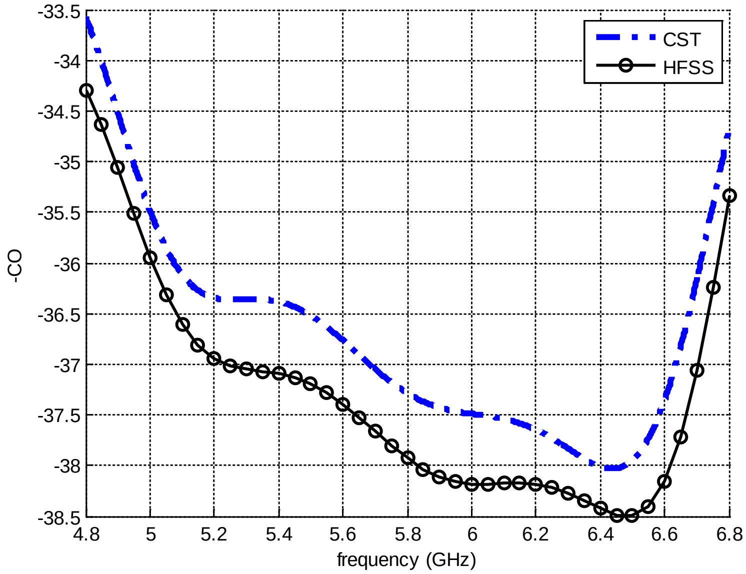


Fig. 4-18: Comparison of the results of coupling of the MWT&MC

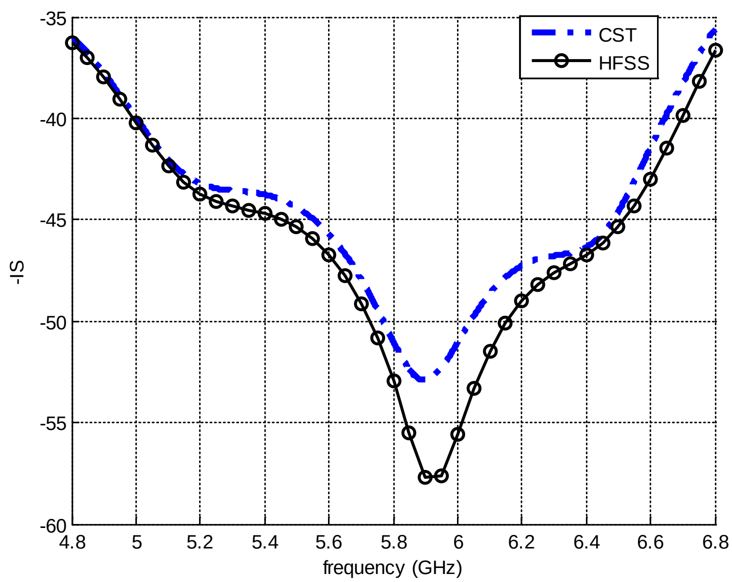


Fig. 4-19: Comparison of the results of the isolation of the MWT&MC

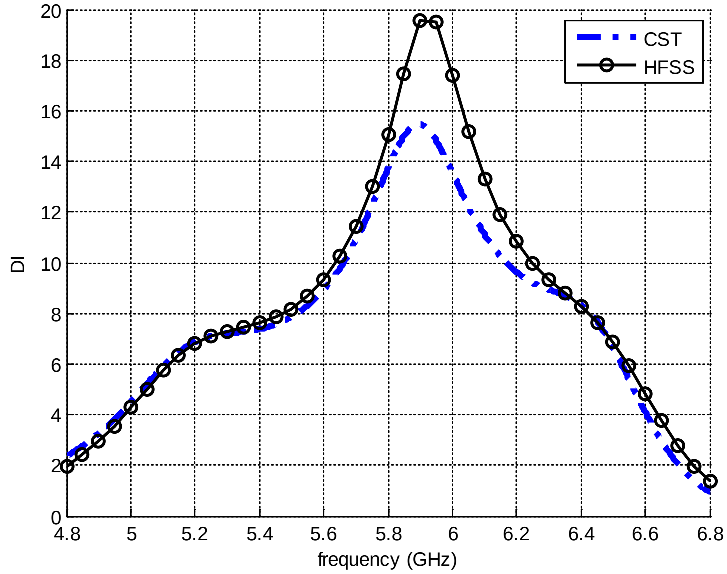


Fig. 4-20: Comparison of the results of the directivity of the MWT&MC

As claimed, the structure has low sensitivity to the tolerances due to fabrication process. Because the metallic body of the structure is manufactured by CNC milling machine, there is no serious concern about its fabrication errors. The main reason of the errors is caused by likely small shift of the printed circuit board (PCB) of the substrate when attaching it on the metallic body. Therefore, according to Fig. 4-21, a simulation was performed by shifting the PCB toward the $\pm$x-direction. The amount of shift along the +x-direction (with the name of xms) was varied from -0.2 mm to 0.2 mm. Fig. 4-22 shows the negative of return loss and Fig. 4-23 shows the negative of the insertion loss of the structure displayed in Fig. 4-21 when the microstrip board was shifted along the x-direction but other parts were remained fixed. The results demonstrated that the bandwidth of 20 dB return loss and the bandwidth of 0.25 dB insertion loss is in a very good agreement.

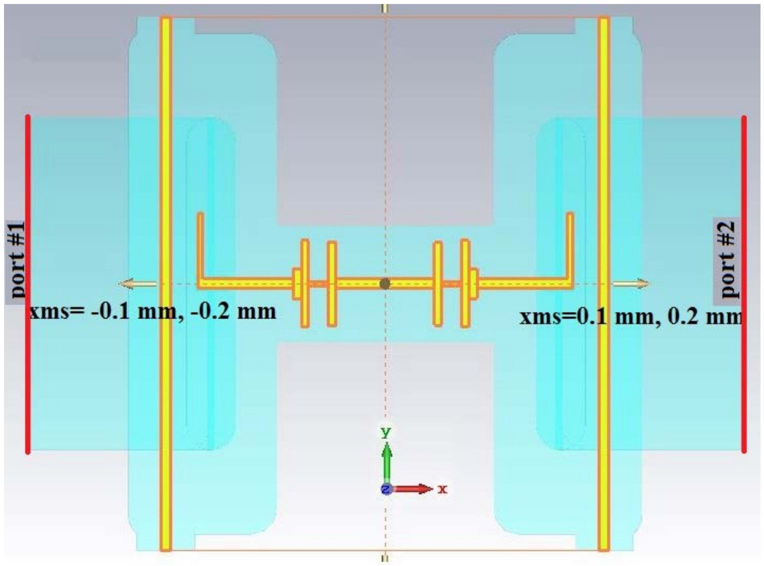


Fig. 4-21: Shifting the microstrip board toward the x-direction

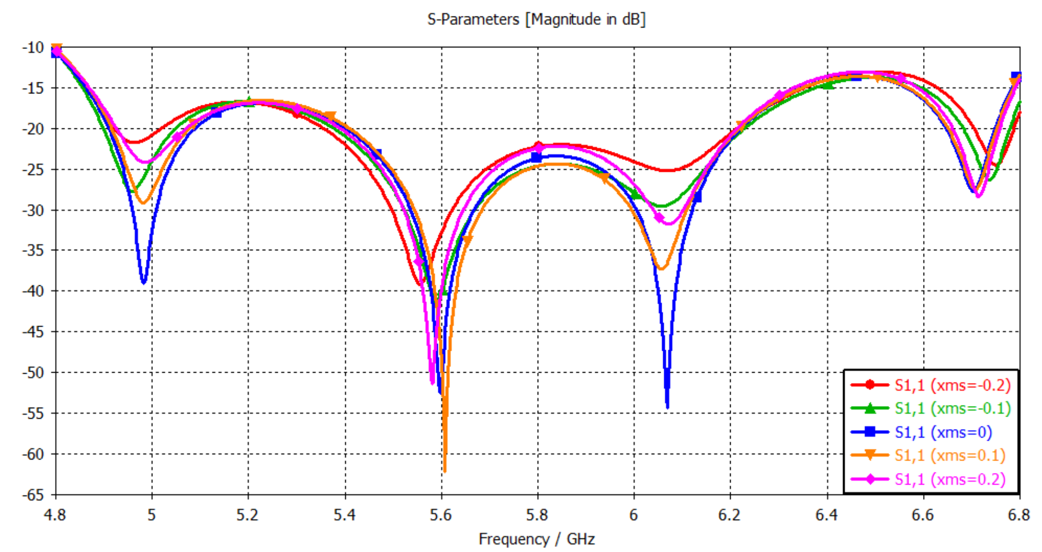


Fig. 4-22: The simulated negative return loss of MWT&MC when the microstrip board is shifted along the x-direction

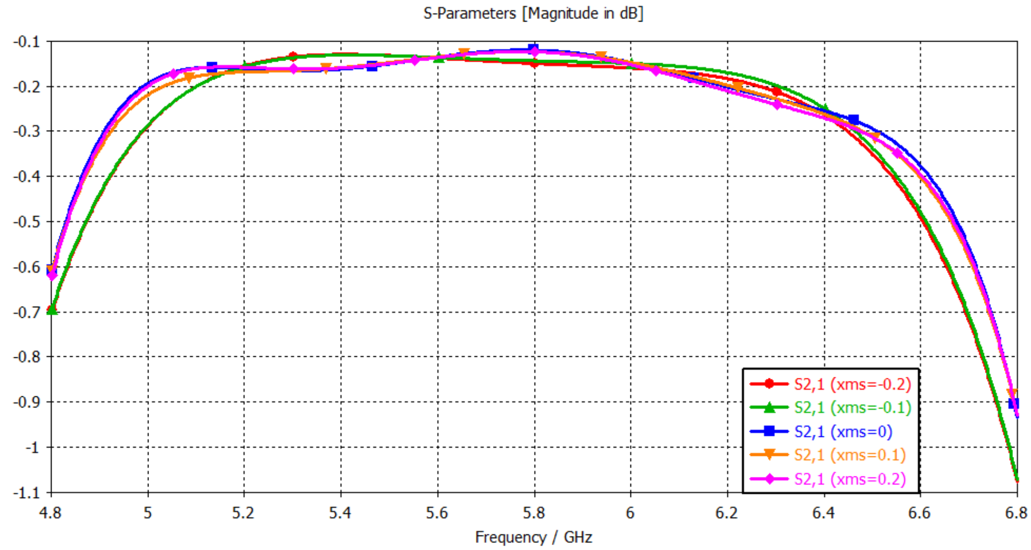


Fig. 4-23: The simulated negative insertion loss of MWT&MC when the microstrip board is shifted along the x-direction

Fig. 4-24 shows the simulation results of the MWT without the MC. In other words, the microstrip coupler was removed from the designed structure shown in Fig. 4-15.b. These results demonstrated that the microstrip coupler does not have any effect on the MWT performance.

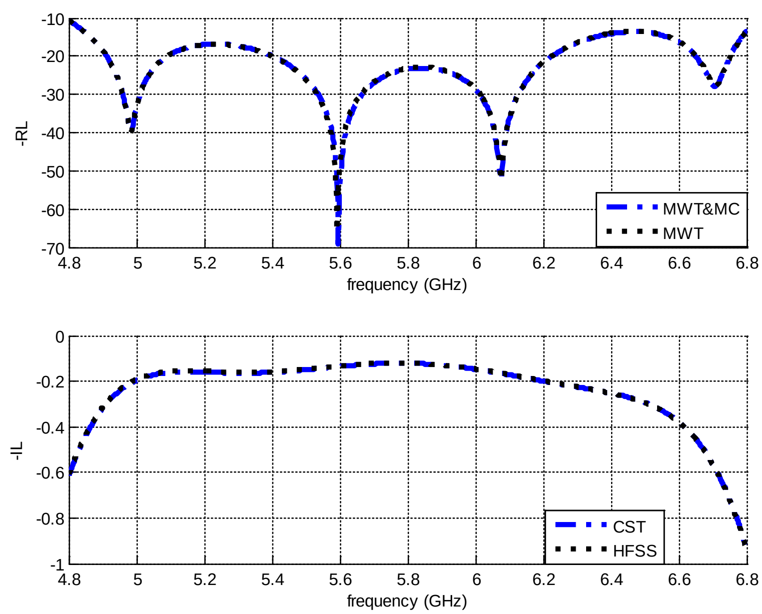


Fig. 4-24: The simulated results of MWT&MC structure when the microstrip coupler has been removed

4.7 Conclusion

In this chapter, an innovative microstrip-to-waveguide transition combined with a microstrip coupler was designed. The proposed configuration is very compact, robust, low sensitive to fabrication variations and suitable for the intended transmitter module. Low insertion loss (less than 0.25 dB) and large return loss (greater than 20 dB) have made it as a reliable and efficient device for the transmitter module. The proposed microstrip coupler, included in this design, shows around 37.5 dB coupling. The directivity of the microstrip coupler is also greater than 10 dB for 10% fractional bandwidth, three times of a conventional microstrip coupler. To achieve a compact configuration, the height of the utilized waveguide was set to approximately a quarter of its standard value. Hence a wideband waveguide to coaxial adapter was designed with 46% fractional bandwidth.

Chapter 5

Antenna design and implementation

5.1 Introduction

In this chapter, a suitable antenna for high power, high-efficiency, and compact transmitter module is introduced. Some features of the antenna, e.g., side lobe level and gain, can be improved by constructing an array of the antenna. Thus, the most important feature of the antenna for the proposed transmitter module is the radiation efficiency that must be as higher as possible because this parameter usually got worse when the antenna is employed in an array. As aforementioned in chapter 1, waveguide antennas are the best choice for the stated applications. Among the available types of waveguide antennas, aperture antennas were chosen to provide very high radiation efficiency while occupying a relatively small space. In addition to the radiation efficiency, the antenna's gain, return loss and size are other important parameters to consider during the design. The gain and size of the antenna are related oppositely. Hence, based on the waveguide aperture antenna, an original antenna structure is proposed in this chapter that not only increases the gain but also keeps the size as compact as possible. Therefore, instead of employing a simple aperture antenna, a more advanced configuration will be introduced by using innovative techniques proposed in this chapter.

Furthermore, the antenna should be implemented in such a way it can be merged with the amplifiers in a very convenient way. Also, the antenna should operate as a heatsink for the HPAs because each high power amplifier needs a cooling system. In fact, dynamic cooling systems (e.g. fan, fluid radiator) are not suitable in this work because they reduce the overall efficiency of the transmitter module. However, to let the antenna operate as a heatsink, the overall size and weight of the transmitter module are decreased significantly due to removing the extra heatsink for cooling the power amplifiers.

In this chapter, after a brief review of the waveguide aperture antenna theory, the proposed antenna with all the performed modifications is presented. The achieved measurement and simulation results are compared and presented at the end of the chapter.

5.2 Waveguide aperture antenna

The dominant mode to radiate wave from a rectangular waveguide aperture on a ground plan is TE_{10}, as shown in Fig.5-1. With regard to the rectangular coordinate system (x,y,z), plotted in Fig. 5-1, and corresponding components of the spherical coordinate system (r, θ, φ), the electric field on the aperture surface (a*b) is

$$E_a = \hat{a}_y E_0 \cos\left(\frac{\pi}{a}x\right),\ -\frac{a}{2} \leq x \leq \frac{a}{2}, -\frac{b}{2} \leq y \leq \frac{b}{2} \tag{5-1}$$

and the far field electric and magnetic field components would be [125],

$$E_r = H_r = 0 \tag{5-2}$$

$$E_\theta = -\frac{\pi}{2} C \sin(\varphi) \frac{\cos X}{X^2 - \left(\frac{\pi}{2}\right)^2} \frac{\sin Y}{Y} \tag{5-3}$$

$$E_\varphi = -\frac{\pi}{2} C \cos(\theta) \cos(\varphi) \frac{\cos X}{X^2 - \left(\frac{\pi}{2}\right)^2} \frac{\sin Y}{Y} \tag{5-4}$$

$$H_\theta = -{E_\varphi}/{\eta}, H_\varphi = {E_\theta}/{\eta} \tag{5-5}$$

$$X = \frac{ka}{2}\sin(\theta)\cos(\varphi),\ Y = \frac{kb}{2}\sin(\theta)\sin(\varphi),\ C = j\frac{abkE_0 e^{-jkr}}{2\pi r} \tag{5-6}$$

Note that in the above equations, η is the intrinsic impedance and k is the wave number of the medium. The E-plane pattern is on the YZ-plane ($\varphi = \frac{\pi}{2}$) and the H-plane is on the XZ-plane ($\varphi = 0$) for the aperture shown in Fig. 5-1. The electric and magnetic field in these two main planes are,

E-plane, ($\varphi = \frac{\pi}{2}$)

$$E_r = E_\varphi = 0\ , E_\theta = -C\frac{\sin\left(\frac{kb}{2}\sin\theta\right)}{\frac{\pi kb}{4}\sin\theta} \tag{5-7}$$

H-plane, ($\varphi = 0$)

$$E_r = E_\theta = 0\ , E_\varphi = \frac{\pi}{2} C \cos\theta \frac{\cos\left(\frac{ka}{2}\sin\theta\right)}{\left(\frac{ka}{2}\sin\theta\right)^2 - \left(\frac{\pi}{2}\right)^2} \tag{5-8}$$

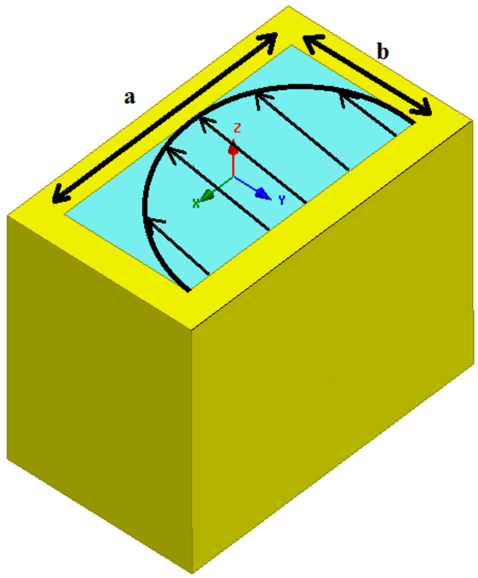


Fig. 5-1: Rectangular aperture antenna

The maximum directivity and first side lobe level (FSLL) can be approximately obtained [125] as,

$$D_{max} = 10.18\frac{ab}{\lambda^2} \tag{5-9}$$

$$FSLL\ in\ E - plane = -13.26\ dBc \tag{5-10}$$

Directivity and effective aperture area A_{em} are related as

$$D_{max} = 4\pi\frac{A_{em}}{e_{rad} \times \lambda^2} \tag{5-11}$$

In (5-11), e_{rad} is the antenna radiation efficiency. With a physical aperture area $A_p = a * b$, the aperture efficiency is

$$E_{ap} = \frac{A_{em}}{A_p} = \frac{8}{\pi^2} = 0.81 \tag{5-12}$$

Free space wavelength, λ_0, at 5.8 GHz is 51.7 mm. The aperture size of a waveguide should satisfy $0 < b < 0.5$ and $\lambda_0 < a < \lambda_0$ over the entire targeted frequency range to propagate the dominant mode (TE_{10}) without the evanescent modes [66]. Therefore, in order to maintain sufficient margin for the desired frequency range, i.e. from 4.8 GHz to 6.8 GHz, 40 mm and 20 mm were selected for *a* and *b*, respectively.

As a result, the design parameters were inserted into (5-9), yielding to a maximum theoretical directivity of 3.1 dBi for single aperture elements. This gain is not enough for an array element to implement a high gain array antenna with all desired features mentioned in chapter 1. In addition, it is not suitable for a single proposed transmitter module. Hence, some techniques to improve the antenna gain were investigated, i.e., increasing the aperture size according to (5-9). This can be obtained by either increasing the antenna width (H-plane sectoral horn) or height (E-plane sectoral horn) or both width and height, which leads to a pyramidal horn configuration [125]. However, to achieve a high gain at the desired frequency range, the size of the horn antenna will be prohibitively large, so this method is not applicable for the proposed applications. Using dielectric [126] and fractal shapes [127] are other ways to raise the gain but radiation efficiency will be decreased and these configurations are not robust enough.

Employing a waveguide aperture antenna in a typical array with traditional feeding network, e.g. T-junctions, has two disadvantages. First, this kind of feeding networks is very bulky thus not suitable for a compact module. Second, an array of aperture waveguide antennas cannot provide a large gain because the gain of its elements is not high enough (about 3dBi for each). For example, a 2*2 array of this kind of antennas will increase the gain to around 6 dBi. Therefore, to implement an array suitable for the targeted application with a large gain, e.g. 20 dBi, the proposed antenna should address these two issues. However, before introducing the proposed antenna, a short antenna array review is first presented.

5.3 Antenna Array

A planar array is designed to obtain higher gain and SLL and narrower main beam. For each kind of antenna array with equal or different phase/magnitude excitation and space between elements, the total electric field is obtained by (5-13),

$$E_{total} = E_{single\ element\ at\ reference\ point} \times AF \quad (5\text{-}13)$$

where the array factor *AF* depends on the array configuration and excitations of the elements. A planar array is considered with rectangular form, as shown in Fig. 5-2. β_x, β_y are the phase shifts along the x- and y-axis, respectively, and I_{mn} is the excitation magnitude for the element at point (m, n). The array factor would be,

$$\text{AF}= \sum_{n=1}^{N} \sum_{m=1}^{M} I_{mn} e^{j(m-1)(kd_x \sin\theta \cos\varphi+\beta_x)} e^{j(n-1)\left(kd_y \sin\theta \sin\varphi+\beta_y\right)} \quad (5\text{-}14)$$

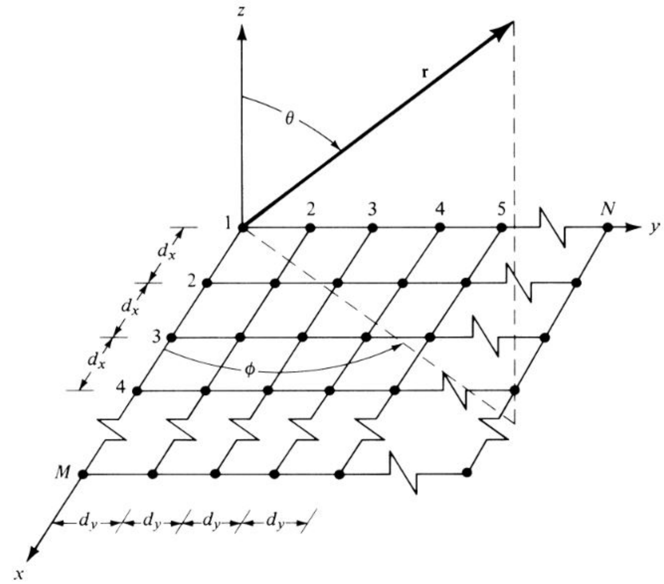


Fig. 5-2: Planar array [35]

Uniform magnitude excitation ($I_{mn} = I_0$) can provide minimum high power beam width (HPBW) but to achieve maximum SLL, unequal magnitude excitation (particularly binomial) must be designed. With uniform magnitude excitation, (5-14) will be reduced to (5-15) [125].

$$AF(\theta,\varphi) = I_0 \frac{\sin\left(\frac{M}{2}\psi_x\right)}{\sin\left(\frac{\psi_x}{2}\right)} \times \frac{\sin\left(\frac{N}{2}\psi_y\right)}{\sin\left(\frac{\psi_y}{2}\right)} \tag{5-15}$$

$$\psi_x = kd_x \sin\theta \cos\varphi + \beta_x \,,\, \psi_y = kd_y \sin\theta \sin\varphi + \beta_y \tag{5-16}$$

$$AF_{max}(\theta = 0,\varphi) = M \times N \qquad , \qquad {AF_{max}}^{dB} = 20log_{10}(AF_{max}) \tag{5-17}$$

Also to avoid the grating lobes, the distance between the elements must be smaller than a half wavelength, $d_x < \frac{\lambda}{2}$ and $d_y < \frac{\lambda}{2}$. If it is desired to have only one main beam directed along $\theta = \theta_0$ and $\varphi = \varphi_0$, the progressive phase shift between the elements in the x- and y- directions must be equal to

$$\beta_x = -kd_x \sin\theta_0 \cos\varphi_0 \quad \text{and} \quad \beta_y = -kd_y \sin\theta_0 \sin\varphi_0 \tag{5-18}$$

By solving the system of two equations in (5-18), the direction of the main beam can be obtained in terms of the specific progressive phase shifts β_x and β_y [11].

$$\tan(\varphi_0) = \frac{\beta_y d_x}{\beta_x d_y}, \sin^2\theta_0 = \left(\frac{\beta_x}{kd_x}\right)^2 + \left(\frac{\beta_y}{kd_y}\right)^2 \quad (5\text{-}19)$$

Maximum directivity of a large planar array, which is nearly broadside, will obtained by (5-20),

$$D_{max} = \pi\cos(\theta_0) D_x D_y \quad (5\text{-}20)$$

Here D_x and D_y state for the maximum directivity of the linear broadside array along x- and y-directions, respectively [125]. Directivity of a linear broadside array as well as a linear end-fired array with equal magnitude excitation (uniform array) are given, respectively, as

$$D_{max} = 2N\frac{d}{\lambda}, \text{ linear broadside array} \quad (5\text{-}21)$$

$$D_{max} = 4N\frac{d}{\lambda}, \text{ linear end-fired array} \quad (5\text{-}22)$$

Also for a linear broadside array with uniform excitation, a relation between HPBW (in terms of degree) and maximum directivity can be expressed as [125]

$$D_{max} \times HPBW \simeq 101.5 \simeq 100 \quad (5\text{-}23)$$

Equation (5-23) can be used as a good approximation between HPBW and directivity for most linear broadside arrays with practical distribution.

The binomial arrays do not exhibit any minor lobes provided the spacing between the elements is equal or less than one-half of a wavelength. For a binomial linear array with $\frac{\lambda}{2}$ spacing between elements, the HPBW and maximum directivity can be approximately related by [125]

$$\text{HPBW} \simeq \frac{1.06}{\sqrt{N-1}} \simeq \frac{0.75}{\sqrt{L/\lambda}} \quad (5\text{-}24)$$

$$D_{max} \simeq 1.77\sqrt{N} \simeq 1.77\sqrt{1 + 2\,L/\lambda} \quad (5\text{-}25)$$

L is the length of the array and N is the number of elements, $L = (N-1)d$

While binomial arrays have very low-level minor lobes, they exhibit larger beamwidths. A major practical disadvantage of binomial arrays is the wide variations between the amplitudes of the different elements of an array, especially for an array with a large number of elements. This leads to very low efficiencies for the feed network.

Maximum directivity for a Dolph-Tschebyscheff array scanning around broadside is obtained by [125]

$$D_{max} \simeq \frac{2R_0^2}{1+(R_0^2-1)f\frac{\lambda}{L+d}} \tag{5-26}$$

with:

$$f = 1 + 0.636\left(\frac{2}{R_0}\cosh\left(\sqrt{(\cosh^{-1}R_0)^2 - \pi^2}\right)\right)^2$$

R_0 is the corresponding voltage ratio of the major lobe to side lobe. Therefore, for a planar array with uniform excitation and $\frac{\lambda}{2}$ distance between elements, the maximum directivity is obtained from (5-20) and (5-21),

$$D_{max} = \pi \times M \times N \text{ or } D_{max}^{dB} = 4.97 + 10 \times \log_{10}(M \times N) \tag{5-27}$$

Thus for a 10× 10 array, the maximum theoretical directivity is $D_{max}^{dB} \cong 25\ dB$.

Among the three most widely used amplitude distributions, (uniform, binomial and Tschebysceff), a uniform amplitude array yields to the smallest half-power beamwidth. It is followed, in order, by the Dolph-Tschebyscheff and binomial arrays. In contrast, binomial arrays usually possess the smallest SLL followed, in order, by the Dolph-Tschebyscheff and uniform arrays [125].

It has been analytically shown that for a given SLL the Dolph-Tschebyscheff array produces the smallest first nulls beamwidth between (FNBW). Conversely, for a given FNBW, the Dolph-Tschebyscheff design leads to the smallest possible side lobe level [125].

Uniform arrays usually possess the largest directivity, except that of super-directive arrays. The directivity of a Dolph-Tschebyscheff array, with a given SLL, increases when the array elements number is increased but for a given number of array elements, the directivity is not inversely proportional or related to SLL [125]. Note that there are other amplitude distributions presented in the literature (e.g. Taylor) [11].

5.4 Proposed Antenna

The proposed technique enhances the antenna gain without degrading the radiation efficiency while maintaining a compact size. In addition, this design has the ability to achieve greater than 20 dB for larger than 10% fractional bandwidth. These improvements were achieved through modifying the feeding method of the antenna in an array as well as improving the antenna structure.

Therefore, four apertures have been placed close together to create a subarray. The apertures are excited by a cavity to keep the minimum size and maximum radiation efficiency. This technique is called cavity-backed antenna [26]-[28], [128], [129]. The cavity-backed structure can also be incorporated by substrate integrated waveguide (SIW) technique to design the low profile antennas in the expense of degrading the radiation efficiency [130]-[132]. The polarization of the rectangular aperture antenna is linear so, the polarization of the subarray is linear. If a circular polarization is needed, it would be possible to convert the antenna polarization to circular [133], [134]. In this method, there is a rectangular cavity. On top of the cavity, the apertures are constructed symmetrically to the center of the cavity. Hence, the cavity operates as a compact interface to excite the apertures equally, instead of using three T-junctions.

In the conventional cavity-backed configuration, the cavity is fed through a slot at a special location of its bottom surface but in the proposed design, the cavity is fed by a narrow aperture located at the center of its bottom surface. The cavity surface must be extended enough to include the four apertures, thus its dimensions would be too large for the desirable frequency range. As a result, unwanted resonances will emerge at the operating frequency of the antenna. Therefore, two couples of walls have been added into the cavity to limit the cavity size and consequently, avoid the undesirable resonances. The dimensions of these added walls are wx1, wy1, wx2, and wy2. Fig. 5-3 displays the described subarray configuration.

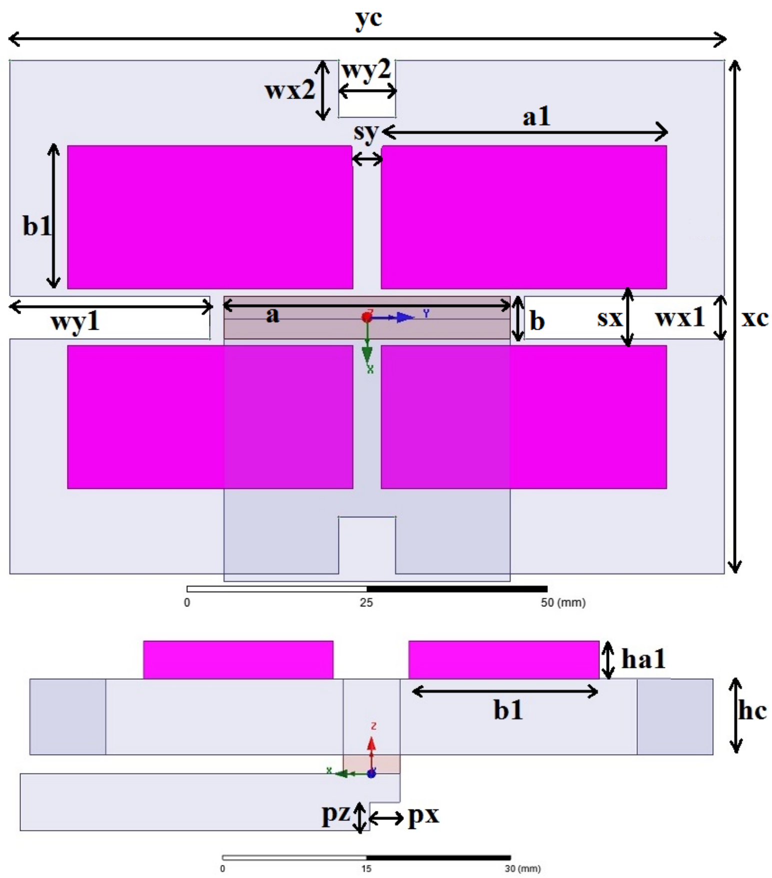


Fig. 5-3: Top and side views of the cavity-backed antenna

In Fig. 5-3, a_1 and b_1 are the aperture dimensions, equal to 40 mm and 20 mm, respectively. x_c and y_c are the cavity surface dimensions and h_c its height, which should be about $\frac{a}{4}$, so that the subarray can resonate in the desired frequency range.

The variables named *a* and *b* are related to the size of the narrow aperture exciting the cavity, referred to the slot in this thesis. They were chosen equal to the size of the output port of the microstrip-to-waveguide transition designed in chapter 4, i.e., a = 6 mm and b = 40 mm.

The slot was directed to the one side of the proposed subarray by using a designed bend, as depicted in Fig. 5-3. This bend is very compact and suitable for the subarray configuration and manufacturing process in comparison with the typical mitered bends [40]. The bend performance is optimized by designing a step in its corner, with dimensions pz and px. The bend was designed separately and then added to the structure.

The distances between the apertures, sx and sy, must be optimized to avoid the grating lobe and to achieve maximum gain. The variable called ha_1 is the height/depth of the aperture but at this stage of designing process, it is very small (about 1 mm).

Thus, there are nine variables (sx, sy, wx_1, wy_1, wx_2, wy_2, xc, yc, and hc) that must be optimized to achieve the desired antenna gain and return loss. However, this structure, which is almost the conventional structure of a cavity-backed antenna, can only provide about 6.5 dBi of gain. This gain is not enough to build a compact and high-directive antenna array.

To increase the gain as well as to improve the return loss, the aperture sizes were extended toward the outside of the antenna in a couple of stages. As displayed in Fig. 5-4, not only the apertures dimensions were extended but also a specific height/depth was given to each extension. The antenna gain is improved by optimizing the apertures height, ha_1, ha_2, and ha_3 whereas the antenna bandwidth can be adjusted by optimizing the values of $a1$, a_2, a_3, b_1, b_2, and b_3.

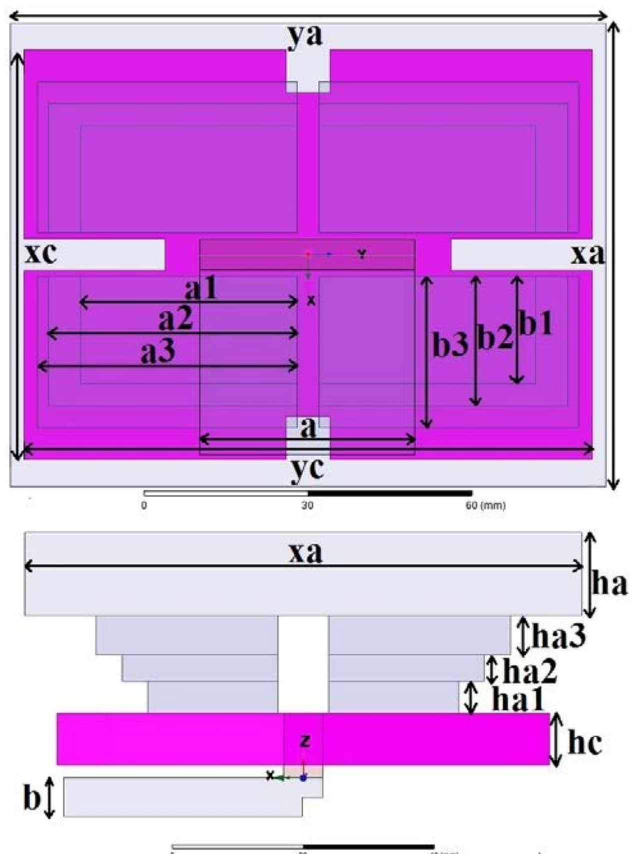


Fig. 5-4: Top and side views of the proposed subarray

Further increasing of the gain was accomplished by uniting the four apertures into a single larger aperture, as depicted in Fig. 5-4 as well in Fig. 5-5. Again, the variable *ha* (Fig. 5-4) mainly improves the gain while *xa* and *ya* adjust the antenna bandwidth. The final uniting aperture on top of the apertures will also improve the mutual coupling when the proposed subarray will be used in an array.

These twelve added parameters were optimized to achieve a large gain and a wide bandwidth for a great return loss. These achievements were obtained in the expense of increasing the height of the subarray structure by only 28 mm. In fact, if a horn antenna, with the same aperture size and input port as the proposed cavity-backed antenna, was designed and simulated to achieve the same level of gain and return loss, the height of the horn antenna must be about 200 mm, approximately five times the proposed antenna height

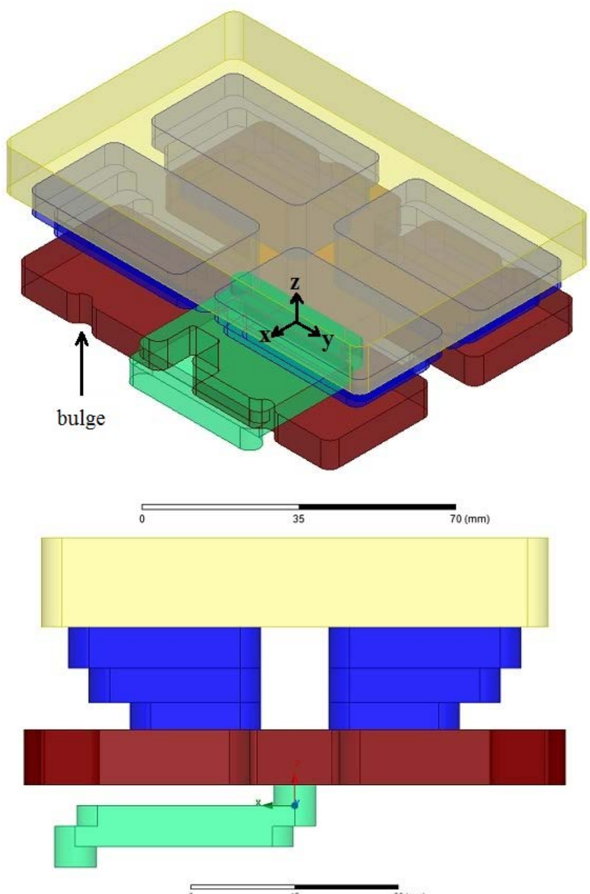


Fig. 5-5: 3-D and side views of the final proposed subarray

The last advantage of the proposed subarray is that its configuration can be implemented as planar layers by Computer Numerical Control (CNC) machines. Hence, the subarray structure was designed in three planar layers. These layers are tightened altogether by screws. The final optimized structure is shown in Fig. 5-5. In this Figure, four bulges were added to the cavity sides to provide the required space for extra screws.

Based on the proposed plan to manufacture the subarray by a CNC machine, a drawing map of the optimized structure was prepared (Fig. 5-6). The overall size of the fabricated antenna is 126 mm × 86 mm × 48 mm. Because the subarray is a part of the transmitter module that must be fed by the HPAs through the MWT&MC, the input port of the subarray has been moved to the outer surface of layer #1 close to the edge of the subarray by utilizing another bend.

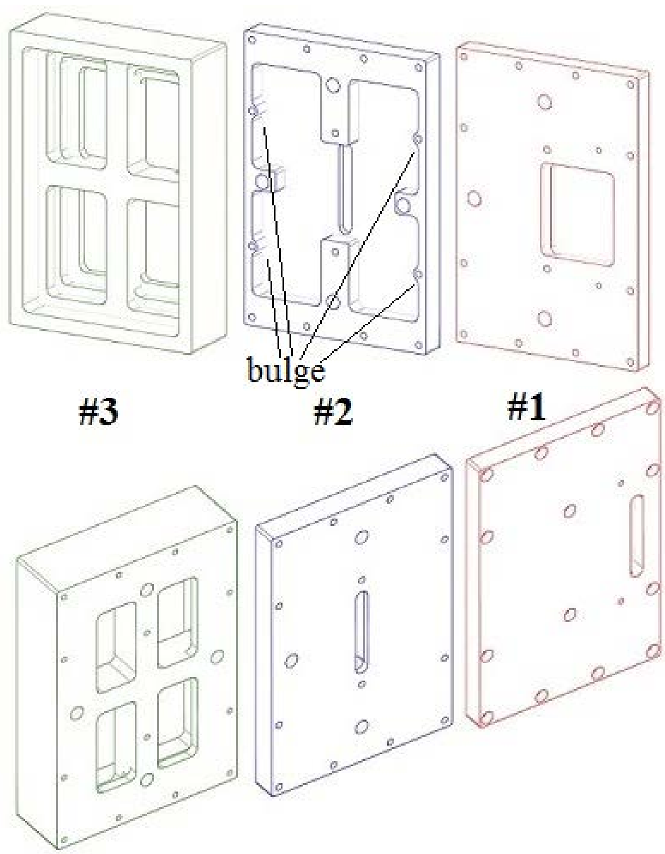


Fig. 5-6: Drawing map of the subarray

In fact, the layer #1 is a common layer between the amplifier circuitry and the subarray. The HPAs and the combining networks are located behind layer #1. Therefore, the metallic structure of the subarray can operate as an effective heatsink for the HPAs with no extra cost.

5.5 Simulation and measurement results of the antenna

All the design simulations were performed in Ansys-HFSS but the optimized structure was also simulated in CST Microwave Studio and EMSS FEKO for further validation. The results from the three commercial EM simulators were virtually identical with slight discrepancies less than 5 %. Regard to Fig. 5-5, the E-plane is the XZ-plane ($\varphi = 0$) and the H-plane is the YZ-plane ($\varphi = \frac{\pi}{2}$). The radiation efficiency of the subarray obtained by the three simulators is a straight line, approximately of 100%.

A prototype of the proposed subarray was manufactured and measured by using the WCA designed in Chapter 4 (Fig. 5-7).

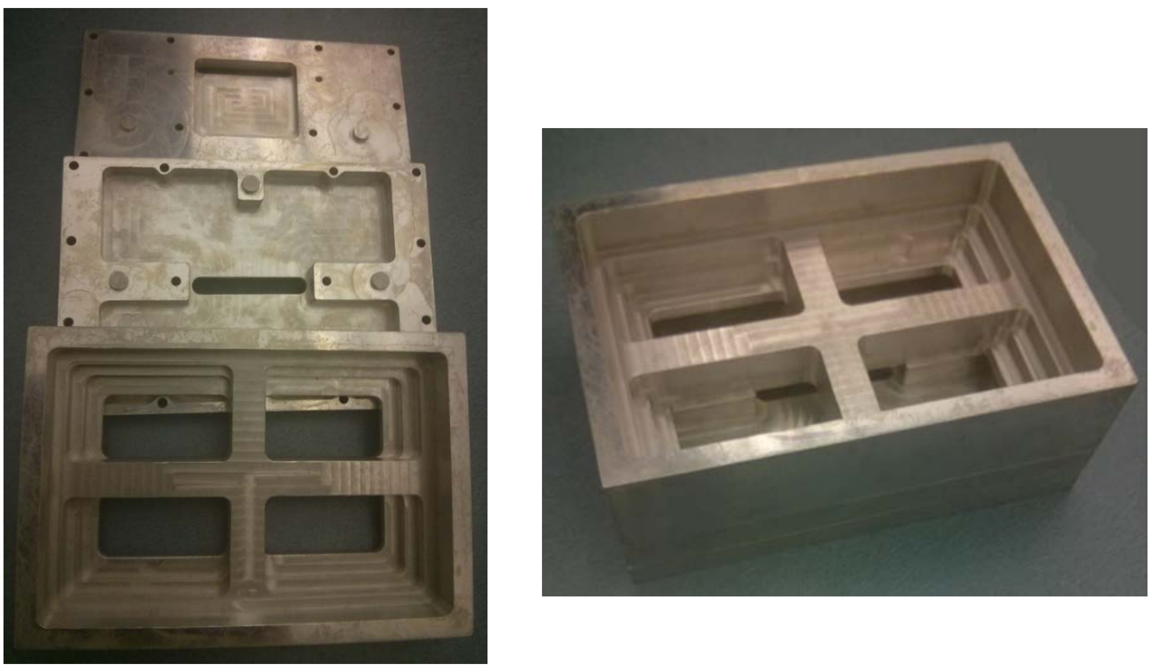


Fig. 5-7: The manufactured prototype of the subarray

The return loss response of the subarray is displayed in Fig. 5-8. The measured return loss not only meets the simulation results but also demonstrates wider bandwidth: it is greater than 20 dB from 5.45 GHz to 6.3 GHz (14.5% fractional bandwidth) and greater than 10 dB from 5.18 GHz to 6.45 GHz (22% fractional bandwidth). A 3-D view of the radiation pattern, at 5.8 GHz, obtained by CST is displayed in Fig. 5-9, which also includes the information about the maximum gain, radiation efficiency, and phase center.

Fig. 5-10 shows the polar graph of the antenna gain patterns in two principal planes at 5.8 GHz obtained by HFSS. HFSS shows the minimum gain in comparison with other simulators. Fig. 5-11 shows the polar graph of the gain pattern in two principal planes at 5.8, 5.6 and 6.0 GHz obtained by CST. It also displays the amount of the side lobe level and the half power beam width. The average of the SLL is about 15 dB at E-plane and 9.7 dB at H-plane. In addition, the average of the HPBW is about 2*33=66^{o} at E-plane and 2*22=44^{o} at H-plane. Fig. 5-12 shows the gain pattern at 5.8 GHz at three different planes ($\varphi = 0°, 45°, and\ 90°$) in the form of a polar and rectangular graph obtained by FEKO. It also displays the information about SLL and HPBW.

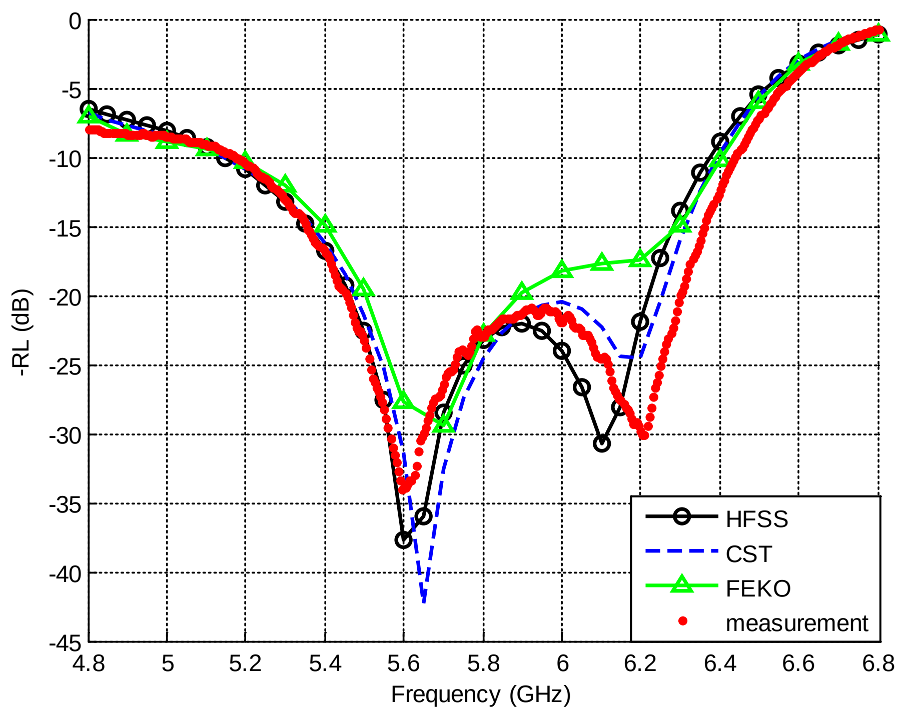


Fig. 5-8: The return loss of the subarray

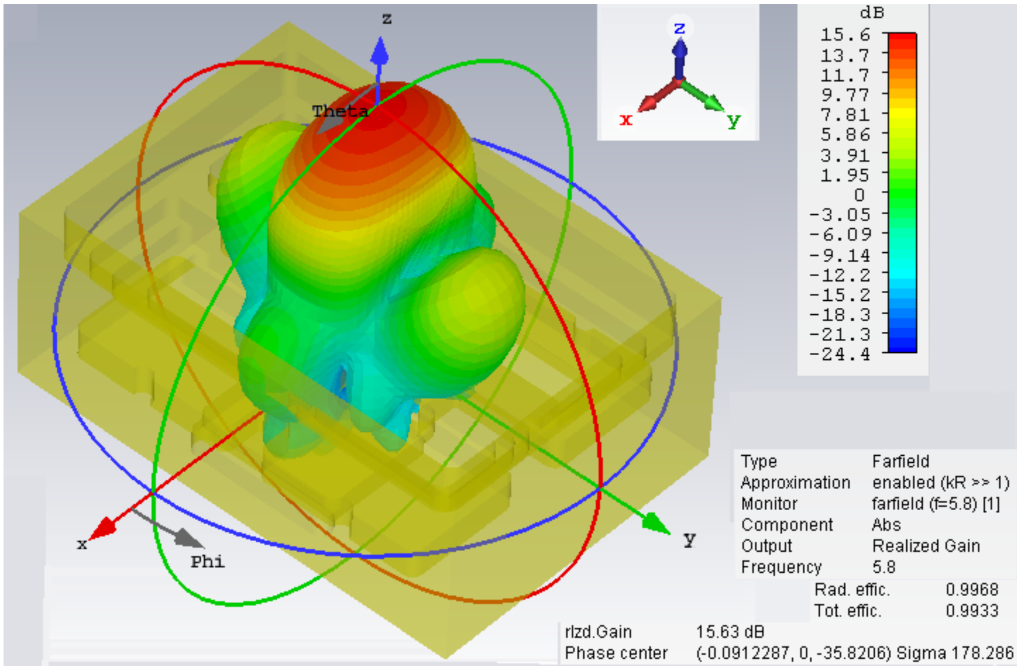


Fig. 5-9: The return loss of the subarray

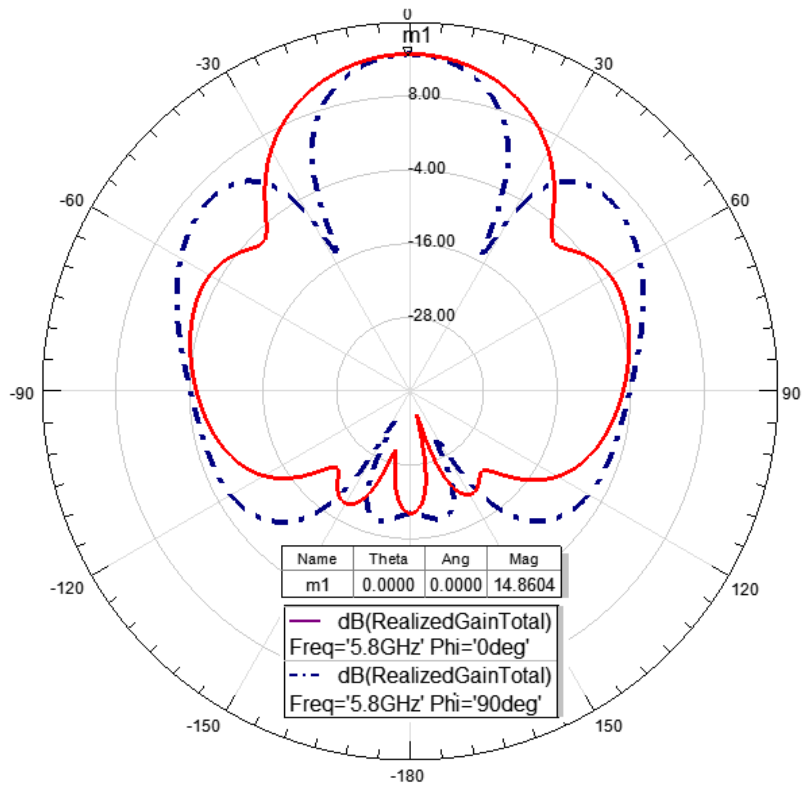


Fig. 5-10: Polar graph of gain pattern for both E- and H-plane at 5.8GHz by HFSS

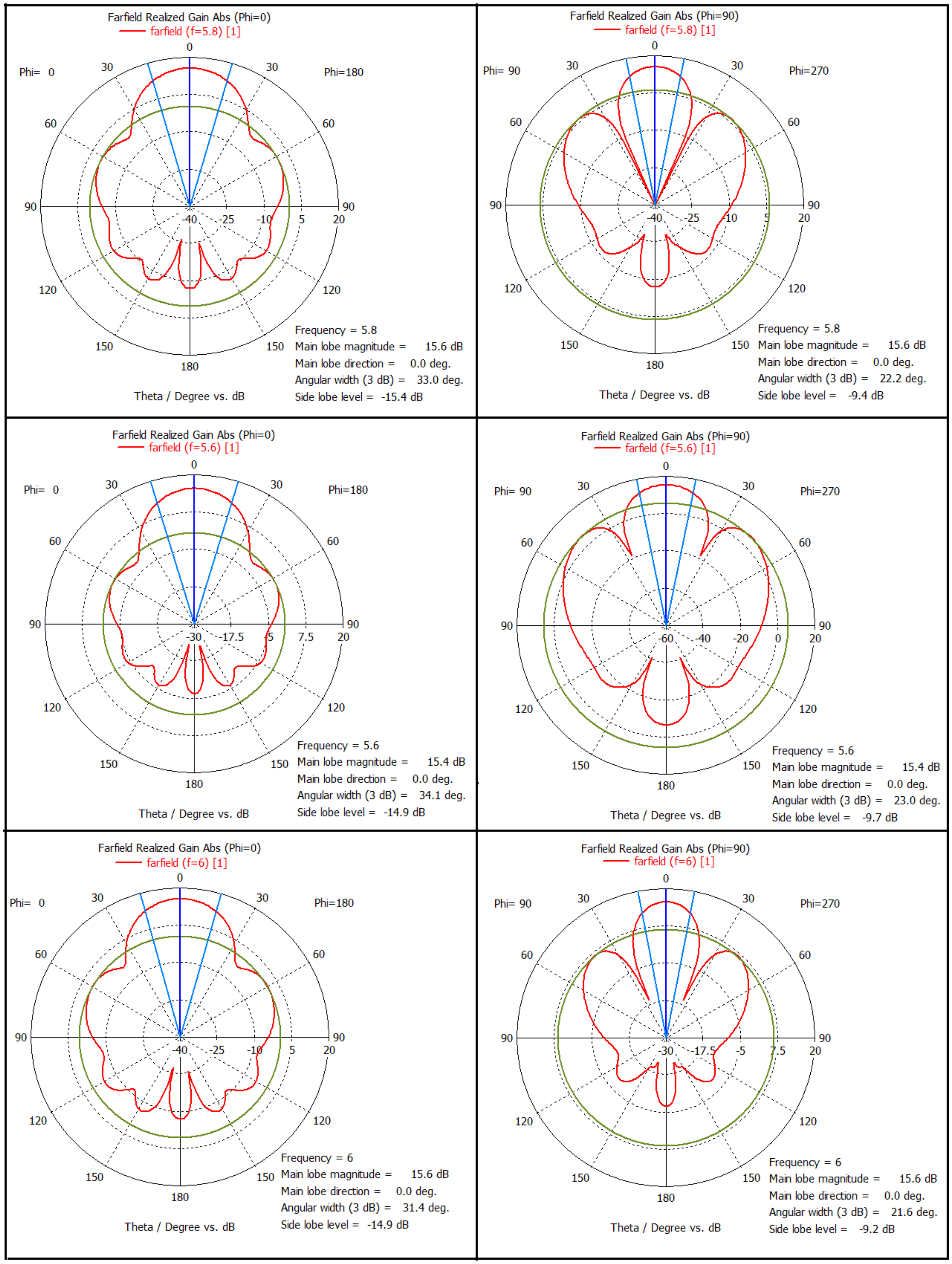


Fig. 5-11: Polar graph of gain for both E- and H-plane at 5.8, 5.6 and 6 GHz by CST

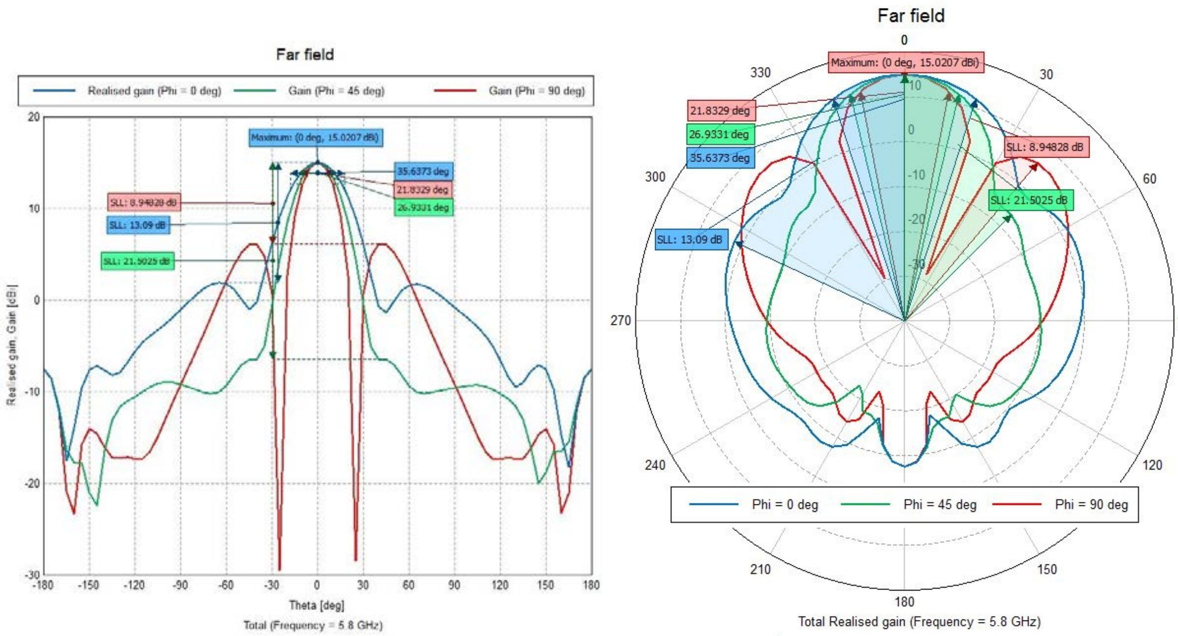


Fig. 5-12: Rectangular (left) and polar (right) graphs of the gain pattern for different planes at 5.8GHz by FEKO

The antenna radiation performance was measured in an anechoic chamber (Fig.5-13). There are usually three ways to measure the antenna gain, identical two-antenna absolute-gain method, three-antenna absolute-gain method, and gain transfer (or gain-comparison) method [135]. Because only one prototype has been fabricated and the available gain standard antenna did not have an accurate gain list, the second method was utilized.

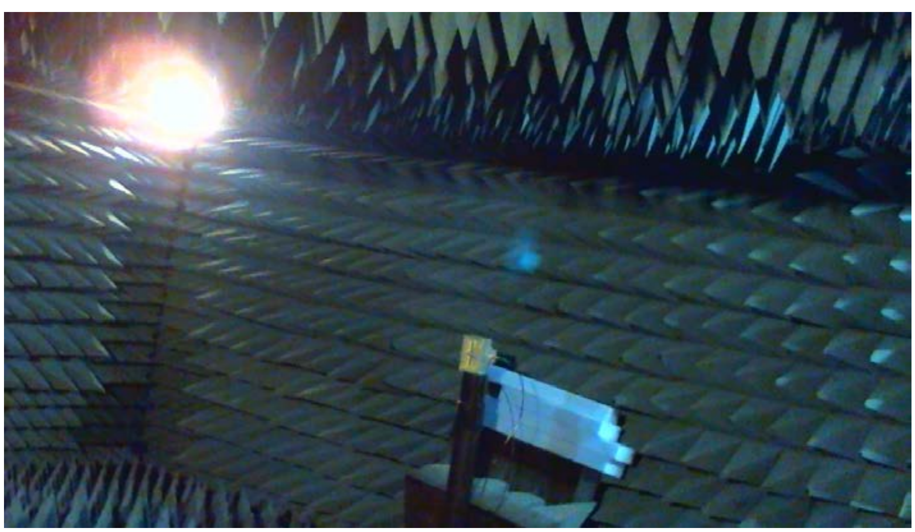


Fig. 5-13: Anechoic chamber

In the three-antenna absolute-gain method, there are three antennas with unknown gain. Then, any other two antennas can be used to perform three measurements, which allow calculating the gains of all three antennas. All three measurements were performed at a fixed known distance R between the radiating and the transmitting antennas. It does not matter whether an antenna is in a transmitting or in a receiving mode. What matters is that the three measurements involve all three possible pairs of antennas: antenna #1 and antenna #2; antenna #1 and antenna #3; antenna #2 and antenna #3 [135]. Based on Friis transmission equation,

$$\begin{cases} G_1^{dB} + G_2^{dB} = 20\log_{10}\left(\frac{4\pi R}{\lambda}\right) + P_{r_{12}}^{dB} - P_{t_{12}}^{dB} \\ G_1^{dB} + G_3^{dB} = 20\log_{10}\left(\frac{4\pi R}{\lambda}\right) + P_{r_{13}}^{dB} - P_{t_{13}}^{dB} \\ G_2^{dB} + G_3^{dB} = 20\log_{10}\left(\frac{4\pi R}{\lambda}\right) + P_{r_{23}}^{dB} - P_{t_{23}}^{dB} \end{cases} \tag{5-28}$$

The right-hand sides of the equations in (5-28) are known if the distance R, the transmitted power ($P_{t_{ij}}^{dB}$), and the received power ($P_{r_{ij}}^{dB}$) are known. Thus, the following system of three equations with three unknowns is obtained and the solution to the system of the equations is given in (5-30) [135].

$$\begin{cases} G_1^{dB} + G_2^{dB} = A \\ G_1^{dB} + G_3^{dB} = B \\ G_2^{dB} + G_3^{dB} = C \end{cases} \tag{5-29}$$

$$\begin{cases} G_1^{dB} = \frac{A+B-C}{2} \\ G_2^{dB} = \frac{A-B+C}{2} \\ G_3^{dB} = \frac{-A+B+C}{2} \end{cases} \tag{5-30}$$

Based on the above method, the antenna gain was measured and compared with simulation ones in Fig. 5-14. It shows that the measured gain is greater than 15 dBi from 15.37 GHz to 6.32 GHz. The measured results are very close to the simulation results obtained by CST.

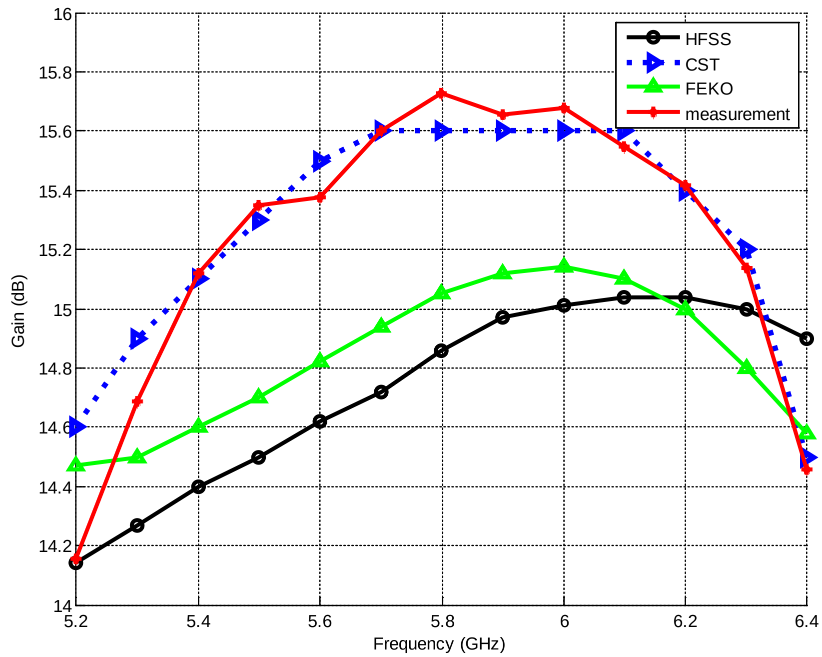


Fig. 5-14: The measured and simulation gain of antenna versus frequency

To measure the radiation efficiency, directivity must be measured based on (5-31).

$$e_{rad} = \frac{Gain}{Directivity} \tag{5-31}$$

The directivity measurements are directly related to the pattern measurements. Once the pattern is found over a sphere, the maximum directivity can be determined using the following expression

$$D_{max} = 4\pi \frac{F_{max}(\theta_0,\varphi_0)}{\int_0^{2\pi}\int_0^{\pi} F(\theta,\varphi)\sin\theta d\theta d\varphi} \tag{5-32}$$

where $F(\theta,\varphi)$ is the power pattern of the test antenna and (θ_0,φ_0) is the direction of maximum radiation. Generally, $F(\theta,\varphi)$ is measured by sampling the field over a sphere of constant radius R. The spacing between the sampling points depends on the directive properties of the antenna and the desired accuracy. The integral in (5-32) can be calculated numerically, e.g,

$$\Pi \approx \frac{\pi}{N}\frac{2\pi}{M}\sum_{j=1}^{M}\left[\sum_{i=1}^{N} F\left(\theta_i,\phi_j\right)\sin\theta_i\right] \tag{5-33}$$

Measuring the field over a sphere is usually difficult or even impossible. Therefore, the 3-D pattern of the antenna is estimated by using some 2-D pattern cuts. For high-directivity antennas, only two orthogonal 2-D elevation patterns often suffice. Assuming that the antenna boresight is along the z-axis, these are the patterns at $\varphi = 0°/180°$ and $\varphi = 90°/270°$. The 3-D field function on the directional angles can be approximated from the 2-D functions as [135].

$$\boldsymbol{E}(\theta,\varphi) \approx j\beta \frac{e^{-j\beta r}}{4\pi r}[\cos\varphi \,.\, \boldsymbol{E}(\theta,0) + \sin\varphi \,.\, \boldsymbol{E}(\theta,90°)] \tag{5-34}$$

For high-directivity antennas, the angles θ, at which the antenna has significant pattern values, are small. Thus, the approximation of the 3-D pattern in terms of two orthogonal 2-D patterns can be reduced to the following simple expression [135].

$$|E(\theta,\varphi)| \approx \sqrt{cos^2\varphi . |\boldsymbol{E}(\theta,0)|^2 + sin^2\varphi . |\boldsymbol{E}(\theta,90°)|^2} \tag{5-35}$$

Based on the proposed method, the directivity and, consequently, the radiation efficiency were calculated by using the measured data and plotted in Fig. 5-15. The radiation efficiency displayed in this Figure also includes the loss due to the return loss of the antenna and the WCA. That is why, the displayed radiation efficiency is 2% less than its ideal value at desirable frequency range and it was fallen sharply at the out-of-band. As a result, the radiation efficiency at desirable frequency range is greater than 98%.

The physical aperture area is $A_p = 85\ mm \times 125\ mm = 10625\ mm$. Effective aperture, A_{em} was also calculated by using (5-11) and consequently the aperture efficiency E_{ap} was calculated by (5-12). The measured results of the aperture efficiency are displayed in Fig. 5-16. Because the effective aperture is proportional to wavelength, the aperture efficiency shown in Fig. 5-16 has more descending slope at higher frequencies. Aperture efficiency of typical antennas vary from 35% to 70%. For horn and reflector antennas, the aperture efficiency is typically in the range of 50% to 80%. The aperture efficiency of the designed antenna is more than 70% from 5.3 GHz to 6 GHz, which is high compared to other antennas.

The normalized E-plane and H-plane patterns obtained by the three simulators as well as the measured ones are plotted in Fig. 5-17 and Fig. 5-18. The gain pattern is closer to the CST simulation. Different simulated/measured features of the antenna radiation pattern are summarized in Table 5-1.

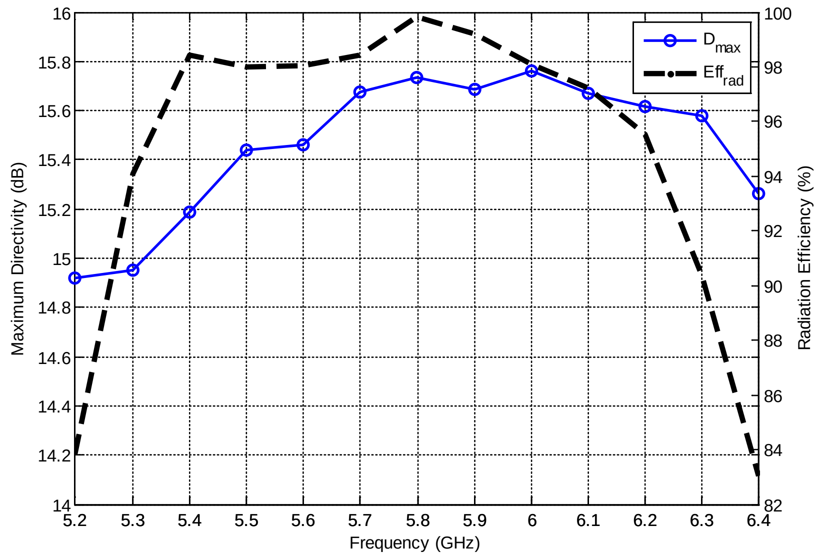


Fig. 5-15: The measured directivity and radiation efficiency of antenna versus frequency

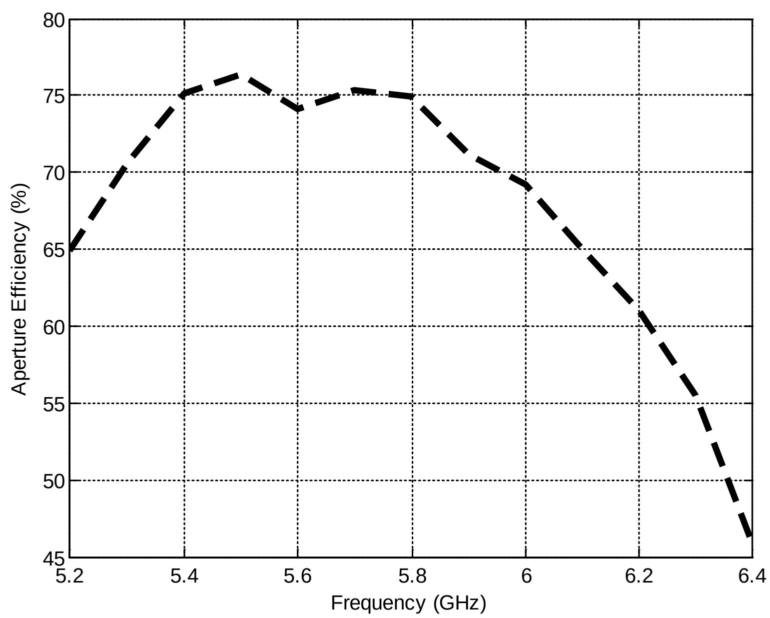


Fig. 5-16: The measured aperture efficiency of antenna versus frequency

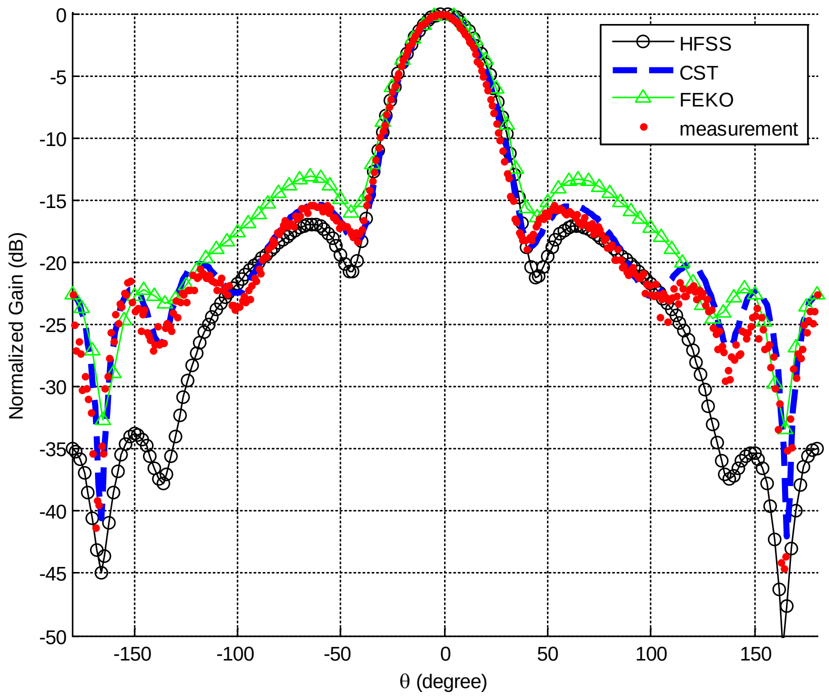


Fig. 5-17: Normalized E-plane($\varphi = 0$) gain patterns

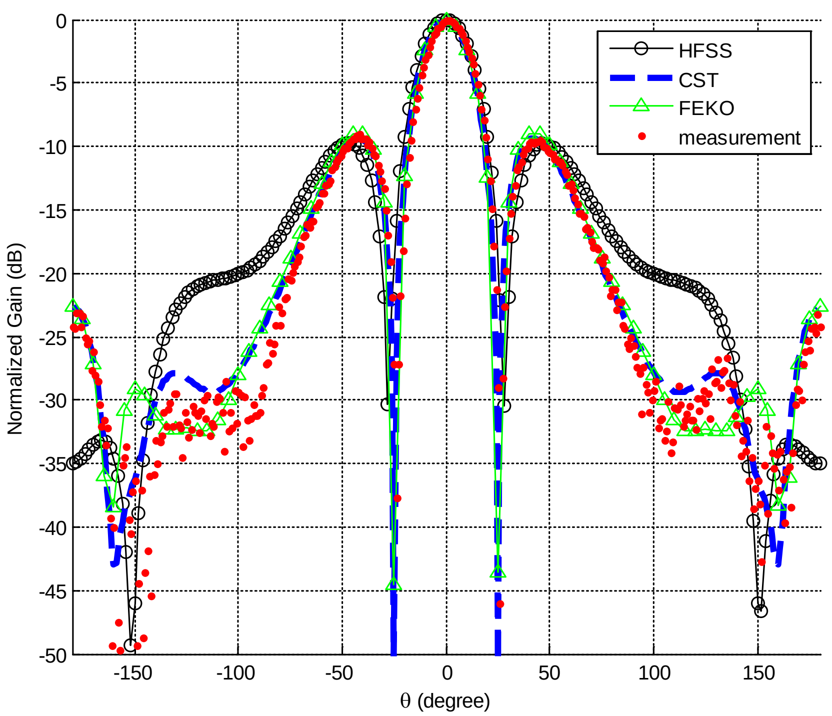


Fig. 5-18: Normalized H-plane ($\varphi = 90$) gain patterns

Table 5-1: Different features of the antenna radiation pattern

	Measurement	CST	HFSS	FEKO
SLL on E-plane	17 dBc @ 56°	15.5 dBc @ 61°	17 dBc @ 64°	13 dBc @ 65°
SLL on H-plane	9.5 dBc @ 41°	9.4 dBc @ 41°	9.8 dBc @ 46°	9 dBc @ 40
3dB-BW on E-plane	32.6 °	33	36	35.6
3dB-BW on H-plane	21.5°	22	24	21

5.6 Antenna array simulations

The proposed subarray antenna was finally used as element of the array. The uniform planar arrays with different numbers of elements were simulated in HFSS. Fig. 5-19 shows a 5×5 array configuration. The center-to-center distance between the subarrays in x- and y-directions, are respectively 90 mm and 130 mm. The rectangular graph of the gain pattern for the arrays with the size of 2×2 and 5×5 are shown in Fig. 5-20 and Fig. 5-21, respectively. Furthermore, the maximum gain, FSLL, and HPBW of the different simulated arrays are summarized in Table 5-2. As expected, the gain was increased by 3dB by doubling the number of elements. In other words, the gain of 2×2 array is greater than 6 dB compared to the single element array and less than 6dB as compared to the 4×4. Except for the single element array, the E-plane FSSL is about 12.5 dBc at around 30° and the H-plane FSSL is about 10 dBc at around 52°. Another conclusion is that, the HPBW of the E-plane is $\frac{3}{2}$ of the H-plane HPBW for all size of arrays.

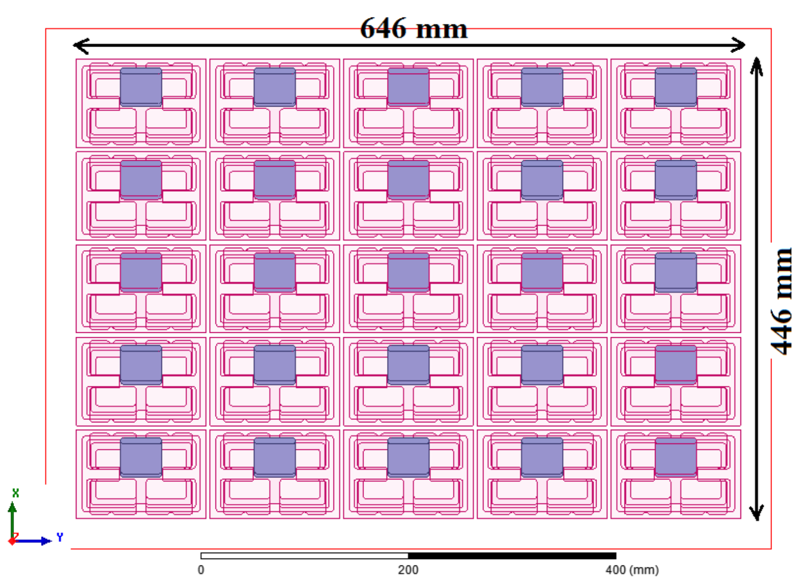


Fig. 5-19: 5×5 array configuration

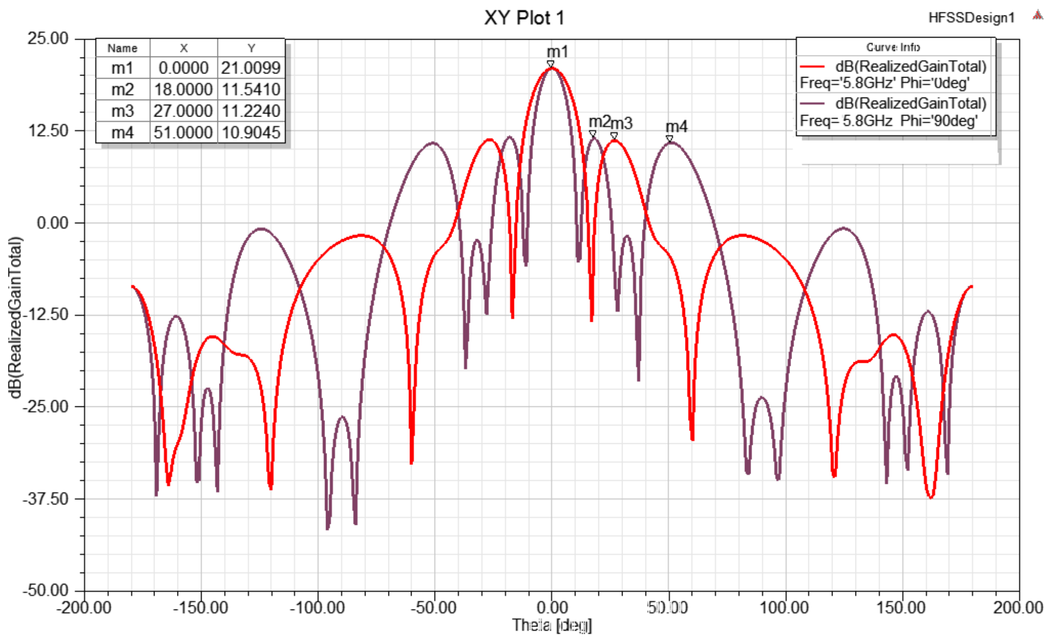


Fig. 5-20: Gain pattern in principal planes of the 2 × 2 array obtained by HFSS

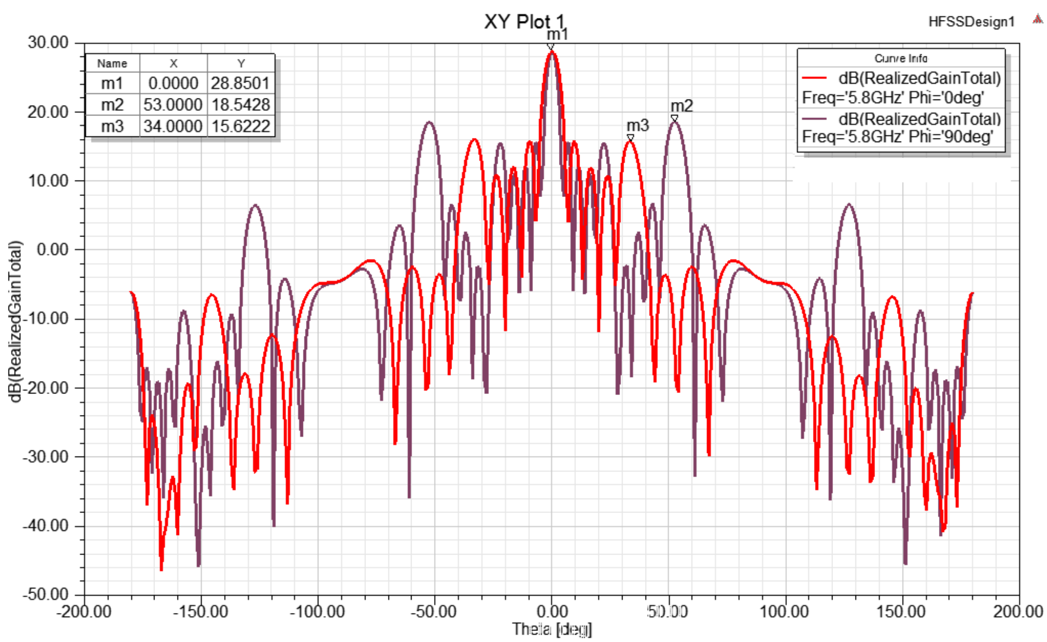


Fig. 5-21: Gain pattern in principal planes of the 5 × 5 array obtained by HFSS

Table 5-2: Features of the uniform antenna arrays obtained by HFSS for different sizes

Array Size	Maximum gain (dB)	FSLL on E-plane	FSLL on H-plane	3dB-BW on E-plane	3dB-BW on H-plane
1	14.86	12.6dBc@64º	9.8 dBc@ 46º	36 º	24º
2×2	21	10dBc@27º	9.5dBc@18º,51º	15 º	10 º
3×3	24.4	12dBc@31º	10dBc@52º	10 º	7 º
4×4	26.9	13dBc@34º	10dBc@53º	7	5.7
4×5	27.9	13dBc@34º	10dBc@52º	6	5.5
5×5	28.9	12dBc@34º	10dBc@53º	6	4

There are several parameters e. g. phase progression and distance between elements that must be determined to design a phased array for a specific application. To exhibit the phase scanning capabilities' of the built array, a progressive phase (β_x, β_y) was assigned to array elements' in both x and y-directions. Hence, the 5*5 array displayed in Fig. 5-19 was simulated with different phase shifts β_x (in x-direction) and β_y (in y-direction). Fig. 5-22 shows the gain pattern in both principal planes when $\beta_x = 90$ and β_y=0. The E-plane gain pattern shows 8º shifts and 0.6 dB reduction of maximum gain. Naturally, there is no shift on the H-plane gain but it was reduced by half. Fig. 5-23 shows the gain pattern when $\beta_x = 0$ and β_y= -90. The H-plane gain pattern shows 6º shifts and 0.7 dB reduction of maximum gain.

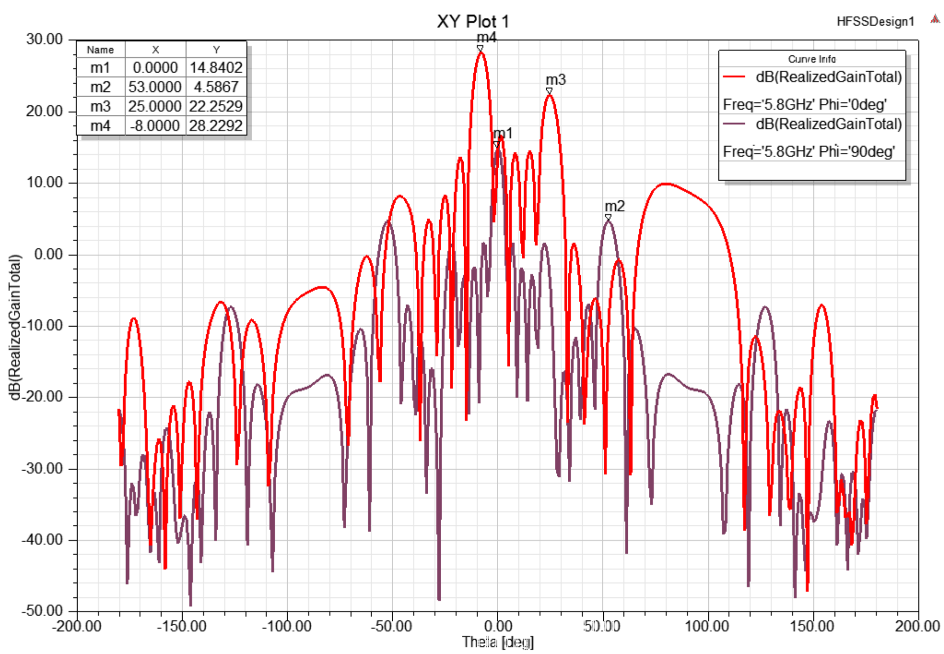


Fig. 5-22: Gain pattern in principal planes of the 5 × 5 array obtained by HFSS when $\beta_x = 90^o$, β_y=0

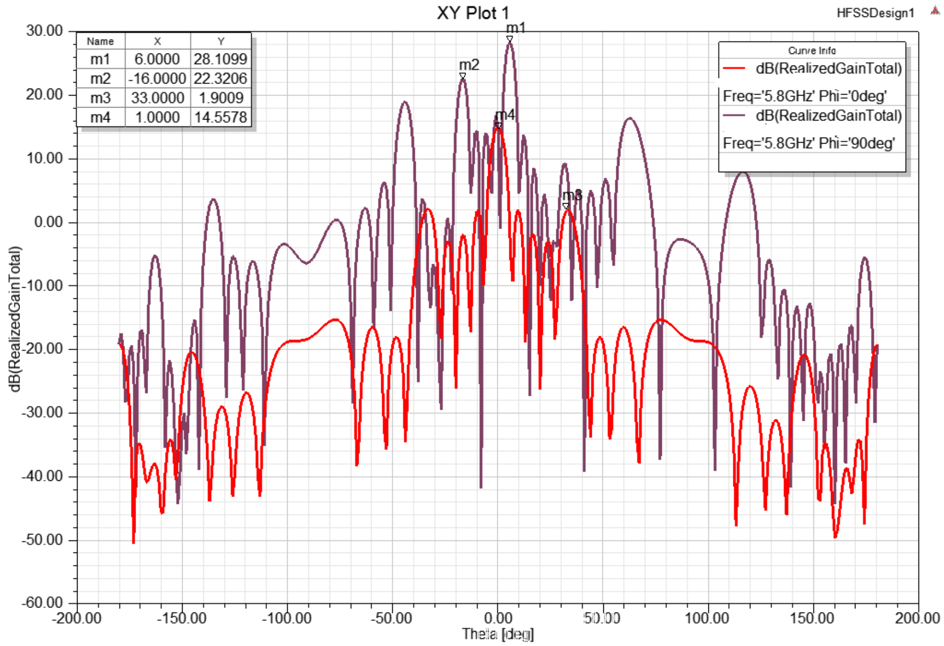


Fig. 5-23: Gain pattern in principal planes of the 5 × 5 array obtained by HFSS when $\beta_x = 0$, β_y=-90°

Fig. 5- 24 displays a 3-D pattern corresponding to Fig. 5-23 to show the different aspects of this array with more details.

An amplitude Dolph-Chebyeshev distribution with 5 elements and -20 dB side lobe level was simulated. The relative magnitude of the currents is 1, 1.61, 1.93, 1.61, 1 [11] so, the relative coefficient of the power is square of the current magnitude (depicted in Fig. 5-24). The two principal gain patterns are shown in Fig. 5-24. As explained, the gain decreased a little, about 0.5 dB. The major discrepancies with uniform array is the position of the first side lob, which was shifted from 9° to 22° at the E-plane and from 8° to 33° at the H-plane. The main beam width was slightly increased and the maximum side lobe level was slightly decreased (1 dB). All the side lobe levels are not exactly the same but they are limited to -20 dB of main beam.

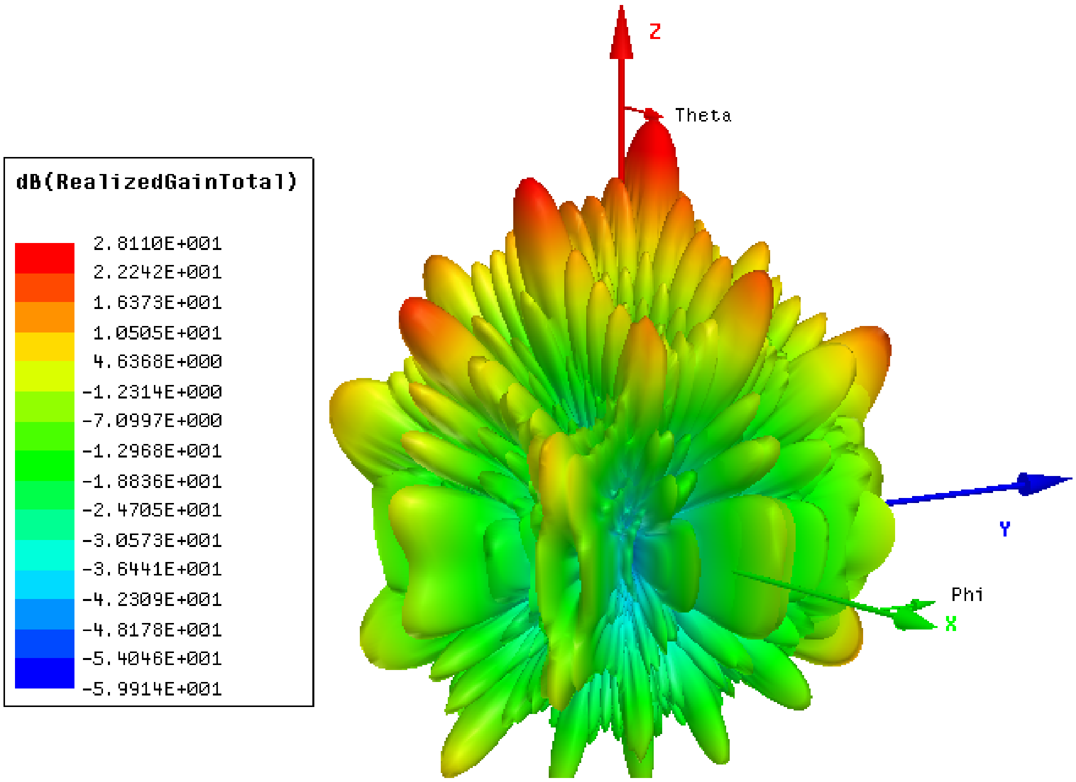


Fig. 5-24: Gain pattern in principal planes of the Dolph-Chebyeshev 5 × 5 array obtained by HFSS

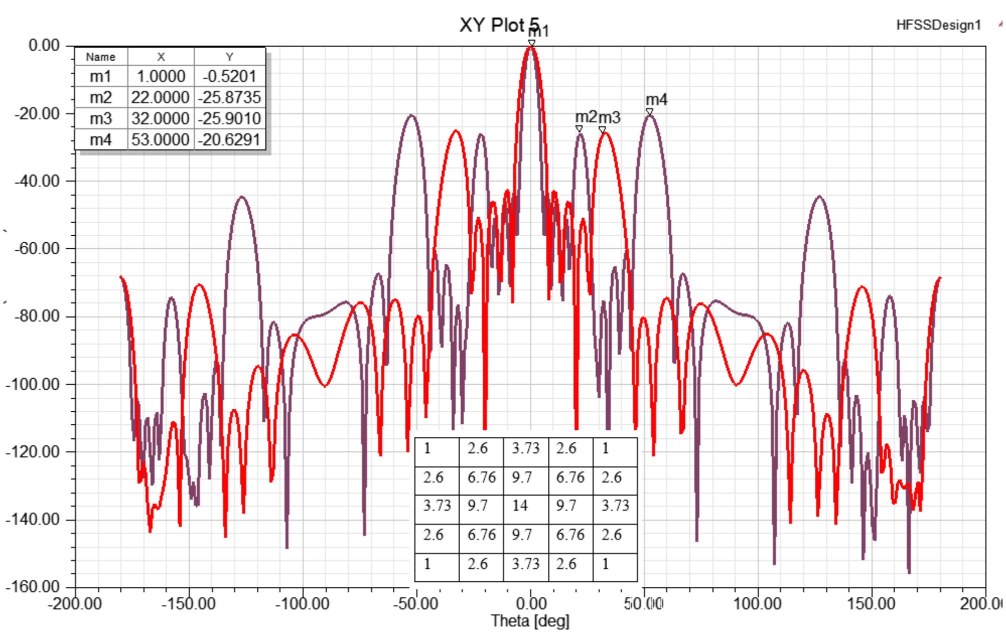


Fig. 5-25: Gain pattern in principal planes of the Dolph-Chebyeshev 5 × 5 array obtained by HFSS

5.7 Conclusion

In this chapter, a novel antenna structure was designed. This structure was simulated in three commercial simulators and then fabricated. The achieved simulated and measured results are in excellent agreement. The measured results demonstrate an antenna suitable for applications that need a compact, high-efficiency and high-gain transmitter. The antenna can be appropriately integrated with the amplifier circuitry to construct a compact module and can operate as the heatsink for the amplifiers. The antenna gain is between 15 dBi to 15.7 dBi for 15% fractional bandwidth. In addition, its return loss is greater than 20 dB for 12% fractional bandwidth. The calculated radiation efficiency of the antenna was found approximately equal to 100% by using the measured data. This antenna was also employed in a uniform array. A 2 x 2 array can enhance the gain to 21 dBi while a 5 x 5 array of 65 x 45 cm^2 can increase the gain up to 29 dBi.

Chapter 6

Conclusions and Future works

6.1 Conclusions

In this thesis, a high-efficiency, high-power and compact transmitter module was designed. Centered at 5.8 GHz with an operating frequency range of 10%, the proposed module can be utilized as a single transmitter or as an element in an active integrated antenna array. To enhance the efficiency and output power as well as to achieve a compact configuration, several innovative designs were introduced.

The proposed transmitter module consists of four essential parts namely, MMIC-HPAs as amplifier units, combining networks to split the input signal between the HPAs and combine the amplified output signal from the HPAs, a waveguide antenna as subarray, and a microstrip-to-waveguide transition (MWT) to transfer the signal into the waveguide from a microstrip line.

A metallic structure was used for the antenna to provide a radiation efficiency greater than 90% as required in the design specifications. Furthermore, the antenna can play the role of a heatsink for the HPAs, thus allowing a significant reduction in size and weight of the transmitter module.

A cavity-backed structure was designed and fabricated to feed four waveguide apertures. The original configuration allowed building a compact antenna (8*12*4 cm^3) with excellent measured performance, with greater than 20 dB return loss and 15 dBi gain.

To design the MMIC-HPA, a novel technique was proposed and successfully utilized to stabilize the AlGaN/GaN HEMTs. This scheme is based on the inductive degeneration technique. The performance of the designed HPA is competitive with state-of-the-art reported MMIC-HPA designs with an output power greater than 45 dBm, a power added efficiency of 30%, and a transducer large signal gain of 22dB. To achieve a high-power transmitter module, up to eight units of the designed MMIC-HPA can be combined. Moreover, the proposed HPA shows excellent linearity behaviour.

As for the combining network, very compact and low loss power combiners/dividers (PCDs) were designed, i.e. Wilkinson and Gysel. The output combiners were designed to include a large resistor as isolator and/or terminator. To achieve a high-efficiency transmitter module, careful consideration was given to reduce the insertion loss of the PCDs such that the total insertion loss of the combining network consisting of three consecutive PCDs is less than 0.7 dB.

The designed MWT has a key feature that can effectively merge the antenna with the active circuits in a compact module. Furthermore, its measured results show an excellent performance, i.e., less than 0.25 dB insertion loss and more than 20 dB return loss. The proposed MWT not only transfers the signal into the waveguide but also makes a sample of the signal to monitor the performance of the transmitter module.

The whole structure was fabricated as planar layers by a CNC milling machine as depicted in Fig. 6-1. The layers must be tightened to each other by screws. Fig. 6-1 and 6-2 show the completed transmitter module.

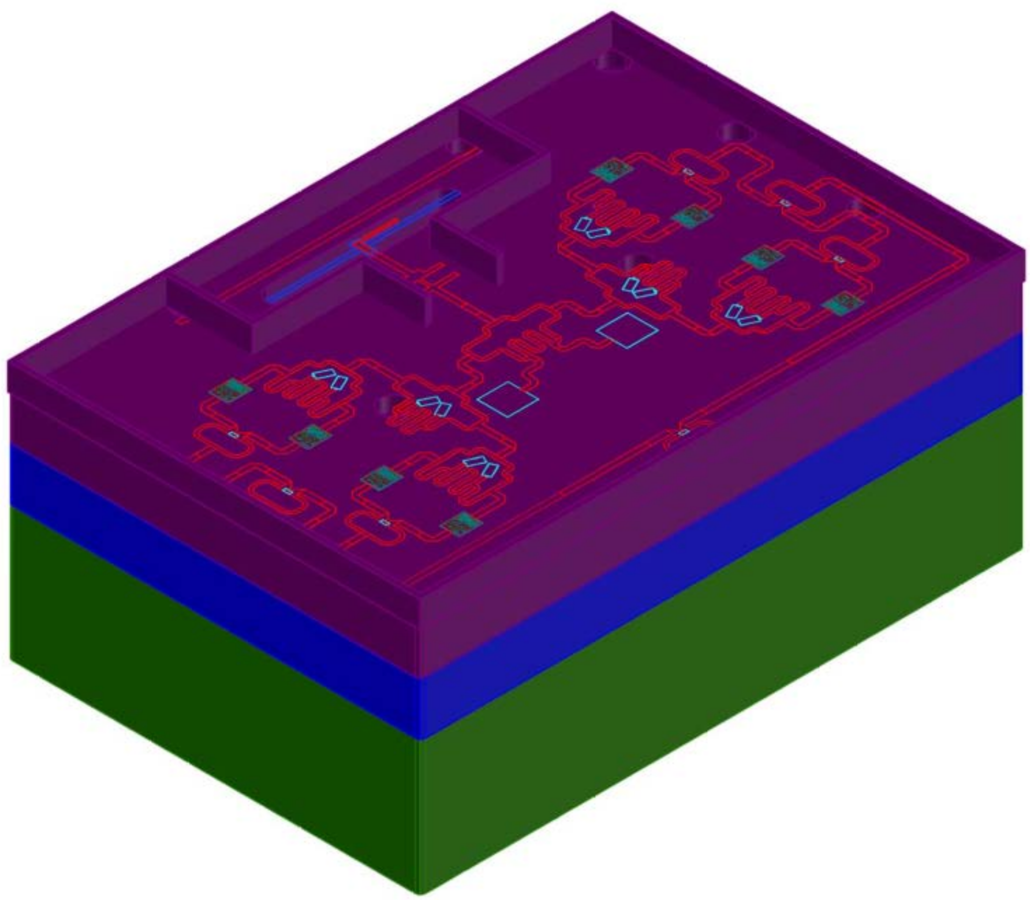


Fig. 6-1: 3-D view of the transmitter module

Because the antenna is almost lossless, the total loss between the HPAs' output and the antenna output is less than 1 dB (0.75 dB for the output part of the combining network and 0.25 dB for the MWT).

Thus, a transmitter module of eight HPAs can provide about 53.5 dBm (≅220 W) output power, by considering 45.5 dBm (≅35 W) for each HPA. Also, there is 0.6 dB loss at the input of the combining network. Hence, the total loss of the passive circuits/components is about 1.6 dB. The total consumed power for each HPA is about 51 dBm (125 W) (Fig. 2-26). Therefore, the total consumed power for the transmitter module including the eight HPAs is 1 kW, which means 22% total efficiency for the whole transmitter module.

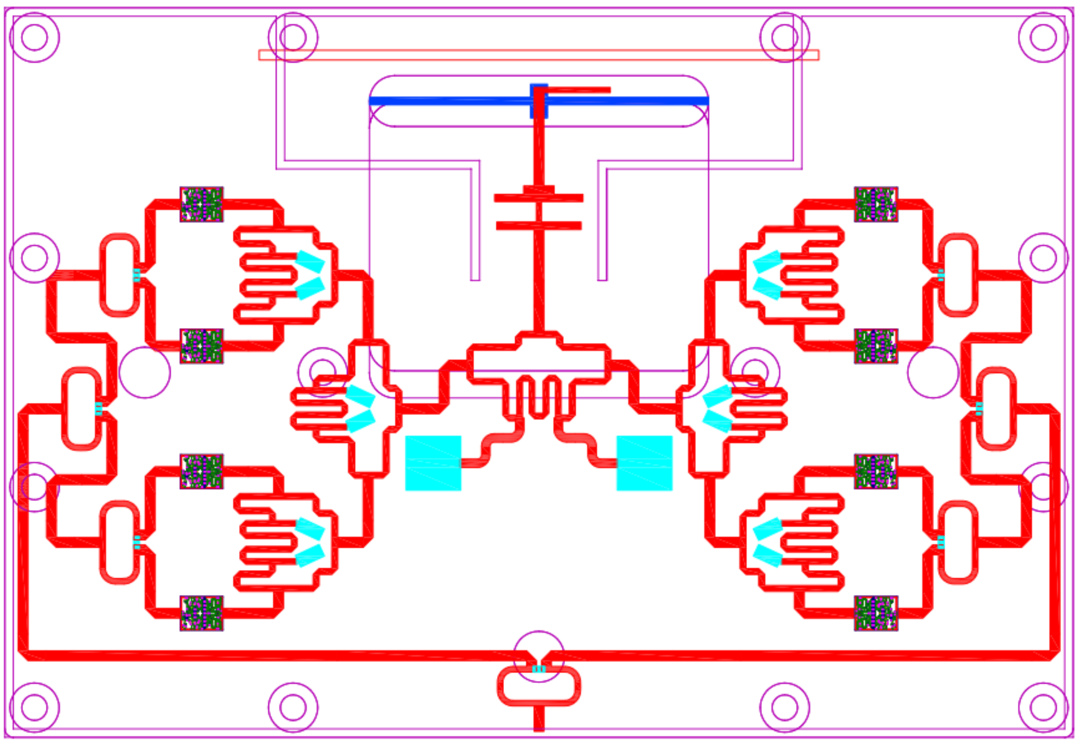


Fig. 6-2: Top view (RF section) of the transmitter module

It is worth to mention that each of the above four essential parts of the transmitter module does not have a significant impact on the performance of the three other subsystems. The RF circuits are located on the back side of the antenna where the antenna radiation efficiency, back lobe level, is about 27 dBc less than the main lobe (Fig. 5-10, Fig. 5-11, and Fig. 5-12). In addition, the RF circuits as well as their bias circuits are enclosed in a metallic box. Antenna, MWT&MC, HPA, and PCDs were designed to have 20 dB return loss. Therefore, cascading these blocks will not affect their performance or limit the bandwidth of the whole transmitter module. Fig. 3-10 and the cited papers confirm this issue. Furthermore, chip isolators can be employed before or even after the HPAs to obtain more reliability.

6.2 Future works

Some of the works that can be undertaken as future works can be listed as follows:

- Improving the MMIC-HPA PAE. This can be achieved by modifying the class/bias operation point of the HEMTs as well as redesigning the matching networks by choosing another optimum load, source impedance, or a matching circuitry topology.
- Performing yield or Monte-Carlo simulations before the fabrication of the HPA is a good way to confirm how much percentage of the fabricated HPAs will have the expected performance.
- All the microstrip lines of the HPA were designed by considering the maximum currents that they can handle, and the capacitors were utilized by considering the maximum operating voltage across them. However, performing derating analysis and simulations are necessary to demonstrate the reliability of the HPA before fabrication to confirm that all the microstrip lines current and capacitors voltage as well as transistors voltage and current are located in the safe range.
- Performing a 3-D electromagnetic simulation of the whole module including the MMIC-HPAs by a 3-D electromagnetic simulator such as Keysight Empro. This simulation could include thermal issues to better predict the module behavior before its fabrication.
- Designing a power amplifier as driver to increase the transmitter module capability to operate in a microwave system. Each MMIC-HPA needs an input power about 20 dBm to be fully saturated. Thus, the input power of the transmitter module including eight HPAs must be about 30 dBm (1 W). Therefore, utilizing a power amplifier with 1 W output power and a gain around 20 dB as driver will avoid providing this large power at the input of the transmitter module
- For RADAR applications, the transmitter and receiver antennas are usually the same. Thus, a device will be needed to separate transmit and receive signal paths to/from the antenna. Waveguide circulators can be a suitable choice due to their power handling, low insertion loss and high isolation. Therefore, an H-plane circulator can be designed between layer#1 and layer#2 of the subarray (Fig. 5-6).
- RF GaN SPDT (single-pole dual-through) switches have been recently designed [136]. Since such devices can handle large powers, one can replace the ferrite circulator by a GaN-based MMIC switch, resulting in a massive size reduction of the area on the module level [137]. Furthermore, GaN switches can provide a higher isolation in comparison with circulators.

The electrical and thermal properties of GaN on SiC HEMT technology are well suited to high power control circuit applications [136]. Their high breakdown voltage will allow the use of higher control voltage and correspondingly, larger RF voltage swings for off-state transistor. Power handling is also limited by device on-state current capability. High maximum current capability of GaN HEMTs reduce the channel resistance and increase RF current swing for the on-state device [136]. Thus, designing and including a GaN SPDT before the designed MWT&MC can enhance the capability of the transmitter module to share its antenna with a receiver.

- In phased array applications that scan beams, the transmitter module must be equipped with phase shifters. Thus, designing a phase shifter and including it at the input of the designed combining network can be a promising research work. MMIC GaN phase shifters can provide accurate phase shifts with low insertion loss and large 1-dB compression point [138]. Furthermore, to find the optimum phase shift for each module in the array, it will be worth to simulate the array based on the features of the transmitter module (e.g., using the Keysight SystemVue simulator).
- To achieve a practical transmitter, the proposed module must be accompanied by a bias circuit to provide the required voltages and currents for the HPAs. It can be placed over the transmitter module as a roof for the HPAs and combining networks.
- Design the feeding networks for the transmitter module when used as array, particularly when the array is going to operate with non-uniform amplitude distributions.

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