

LINEAR CIRCUIT TECHNIQUES
FOR INSULATED GATE
INTEGRATED FIELD-EFFECT
DEVICES

by

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ABSTRACT

The application of MOS integrated circuits has been primarily limited to the digital field because the requirement for high packing densities is more pressing than in linear circuits and there are fewer problems resulting from lack of dc operating point stability and because of device non-linearities. In addition, the stray capacitances associated with integrated circuit coupling capacitors introduce severe bandwidth limitations. The paper discusses circuit design techniques, suitable for p-channel single diffusion enhancement type all-MOS circuits, which provide solutions for some of the above problems.

ACKNOWLEDGEMENTS

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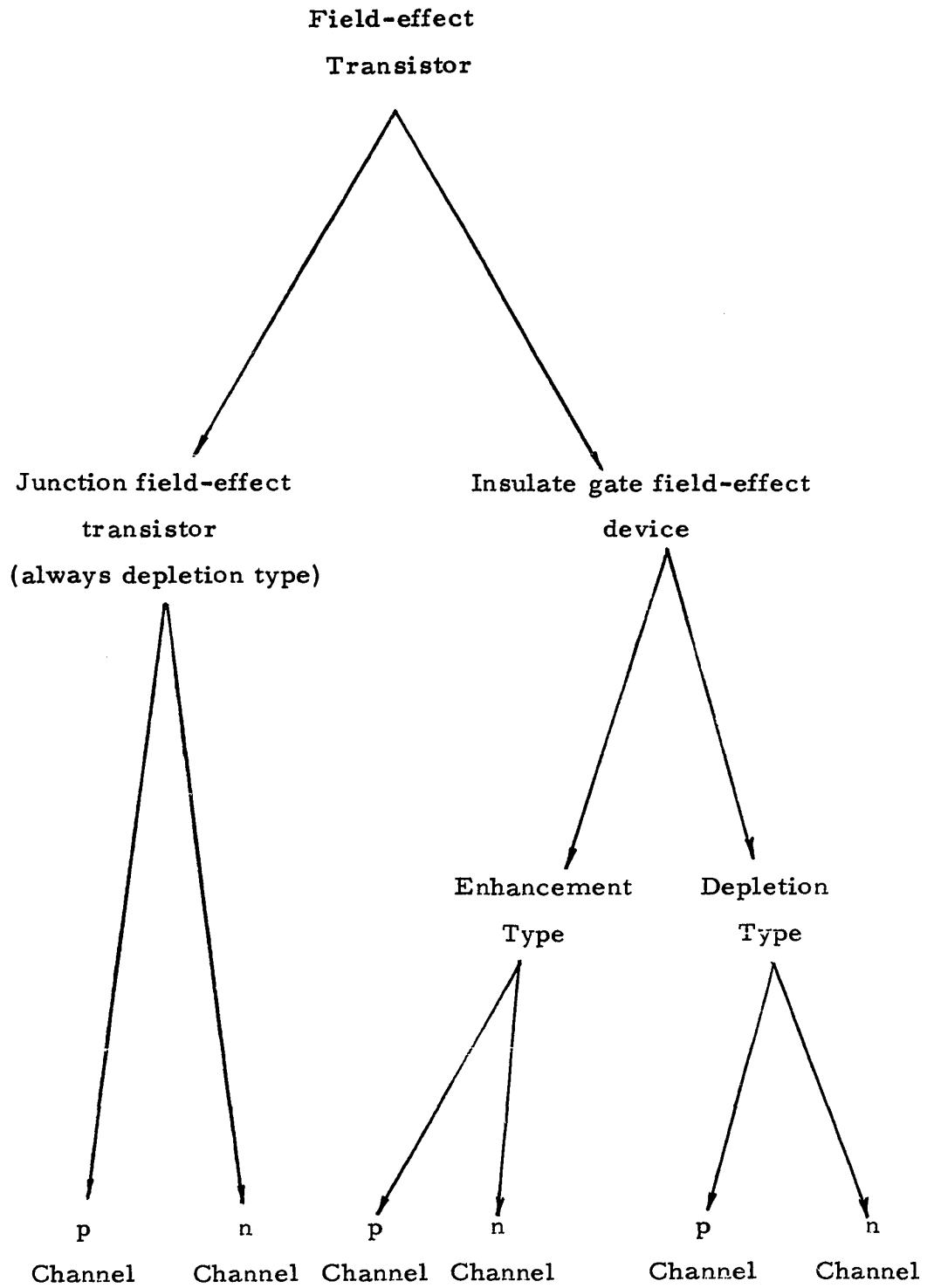
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Terminology of Field Effect Devices

There are two types of field effect or unipolar device ; junction and insulated gate. In both types, the flow of majority carriers through their conducting region or channel is controlled by the gate voltage. There are ohmic contacts to the channel, referred to as the source and drain. In a junction gate device, the gate is isolated from the conducting channel by the depletion layer of a reverse biased junction, while in an insulated gate device, a layer of insulator is used. Typically, in an MOS device, the gate is metal, the insulator silicon dioxide and the conducting material lightly doped semiconductor. The junction field effect device utilizes the depletion region of a reverse biased p-n junction to control the effective cross section of the channel area, while in an MOS device, the control of the channel conduction is achieved by changing the surface carrier density by an electric field normal to the surface of the semiconductor.

Insulated gate devices may be subdivided in two ways; depletion or enhancement and p or n devices. The depletion device is distinguished from the enhancement device by there being conduction in the channel at zero gate bias, while in an enhancement device, there is no conduction at zero gate bias. An organizational chart of this terminology is given below.



Organization Chart of Field-effect Devices

LIST OF SYMBOLS

1. A Gain of amplifier
2. C_c Channel capacitance
3. C_{gd} Gate to drain capacitance
4. C_o Oxide capacitance per unit area
5. E Voltage per unit width
6. V_c Voltage across channel capacitance
7. V_g Gate signal voltage
8. f Frequency
9. g_m Transconductance
10. I_{ds} Drain current at saturation per unit channel width
11. l Channel length
12. R_L Load resistance
13. r_c Channel resistance
14. r_d Drain resistance
15. R_F Feedback resistance
16. r_{gd} Gate to drain leakage resistance
17. r_{gs} Gate to source leakage resistance
18. t_{ox} Thickness of the oxide layer
19. V_D Drain voltage with respect to the source
20. B Reverse admittance
21. Z_{in} Input impedance
22. Z_{out} Output impedance

- 23. V_T Threshold voltage
- 24. W Channel width
- 25. X Distance along the channel from source to drain
- 26. ϵ_{ox} Dielectric permittivity
- 27. δ Channel sheet conductance
- 28. ρ Channel sheet charge density
- 29. U Amplification factor
- 30. μ_o Carrier mobility
- 31. C_{in} Input capacitance

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I Introduction

A recent development in integrated circuits has been the successful application of metal-oxide-semiconductor field effect devices. These have advantages over bipolar and junction gate field effect devices, in that, only a single diffusion process is required in their fabrication, no special isolation processes are needed and they yield a much higher packing density. Their practical application has been in digital circuits rather than linear circuits because, in addition to the immediate economic gains, the requirement for high packing densities is more pressing and the present lack of dc stability of their operating point is less of a problem. The main objections to applying MOS devices in linear integrated circuits are:

- (1) The square law characteristic of MOS devices distorts the signal being amplified.
- (2) Instabilities of threshold voltage.
- (3) Bandwidth limitations due to stray capacitances between integrated elements and the substrate and inherent device limitations.

All these will be discussed in detail later. However, there are economic advantages to be gained from their use in linear integra-

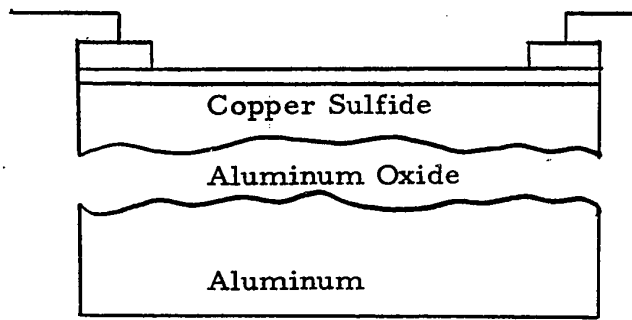
grated circuits and it is possible to design stable MOS circuits to meet a variety of linear applications.

The thesis starts with a brief history of field effect device development and is followed by a discussion of the theory of their operation, their electrical characteristics and equivalent circuits. Then, circuit designs directed towards integrated circuits with several useful circuit configurations are presented. The thesis concludes with an assessment of the position of insulated gate field effect devices in semiconductor integrated circuits.

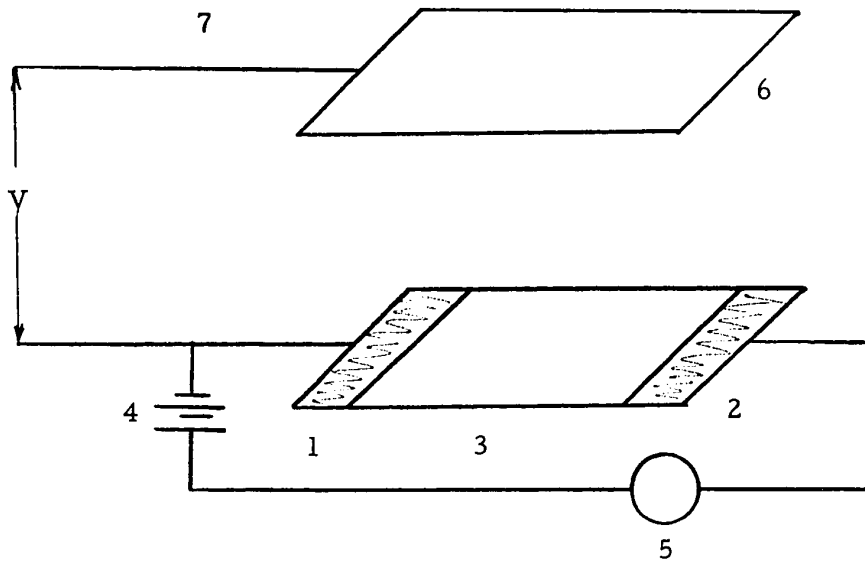
II A Survey of MOS Device Operating Principles

II-1 History

Early efforts to realize semiconductor devices operating on field effect principles were undertaken by J. D. Lilienfeld¹ in 1928. By 1935, patents had been issued both to Lilienfeld and Heil² for their independent efforts in United States and Great Britain respectively. These devices are shown in Fig. 1 (a) and (b). The light area marked 3 in Fig. 1 (b) is described as a thin layer of semiconductor such as tellurium, iodine, cuprous oxide, or vanadium pentoxide; 1 and 2 designate ohmic contacts to the semiconductor. A thin metallic layer marked 6, immediately adjacent to but insulated from the semiconductor layer, serves as control electrode. Heil describes how a signal on the control electrode modulates the resistance of the semiconductor layer so that an amplified signal may be observed by means of the current meter, marked 5. In modern terminology, one might describe this device as a unipolar field effect device with insulated gate. A slight modulation in the current through the device was observed, but because of the limited knowledge of the physics of surfaces and thin films at that time, little advance in the development of these devices was made and interest in them faded with the continued development of the vacuum tube.



(a)



(b)

Fig. 1 The historical field effect device structures (a) The metal oxide semiconductor device proposed by Lilienfeld (b) The metal oxide semiconductor thin device proposed by Heil

Later in 1948, Pearson and Shockley revived the interest in "Field effect" devices. The device geometry in the experiments of Pearson and Shockley was similar to that proposed by Lilienfeld and Heil. They also attempted to modulate the resistivity of a piece of semiconductor material by means of an external field plate, but failed to demonstrate the changes in conductance expected from the number of additional charge carriers in the semiconductor material calculated from the capacitance of the structure. The reason for this lack of correlation between the simple theory and experiment was that most of the charge induced in the semiconductor was trapped in surface states and only a small percentage of the additional carriers added were free to move. In 1952, Shockley proposed a field-effect transistor structure which bypassed the problem of surface states. Shockley used a reverse-biased p-n junction to modulate the mobile charge in the relatively lightly doped n-type portion of the junction. The electric field was now almost completely immersed in the semiconductor bulk and the problem of surface states was avoided. While these experiments were not successful in making a practical insulated gate field-effect device, they did lead to the invention of the bipolar and junction field-effect transistors. Accordingly, for several years, there was no further work on device structures with external field plates.

It is only recently that a significant effort has been refocused on the insulated gate field-effect device. In 1960, Kahng and Atalla proposed a silicon structure in which an insulated gate was used to induce conduction between two normally reverse-biased junctions, and in 1961, Weimer described the development of a thin film insulated gate device utilizing cadmium sulfide as the semiconductor material. In 1962, Hofstein and Heiman described the use of metal oxide semiconductor structure in a field-effect device with an insulated gate fabricated on single crystal silicon. Unlike the junction gate field-effect transistor, the new device allowed both enhancement and depletion of the charge in the channel, and permitted operation with zero bias.

II-2 Physical Construction of MOS Devices

A perspective and cross-sectional view of a typical MOS device are shown in Fig. 2 and Fig. 3. The heavily doped regions are the source and the drain electrodes. The gate is separated from the channel by an insulating layer. The insulator of the silicon device is thermally grown silicon dioxide; hence the name metal-oxide-semiconductor field effect device. These devices can be made on either p or n-type silicon giving complementary types. However, for simplicity, only those constructed on n-type silicon will be considered.

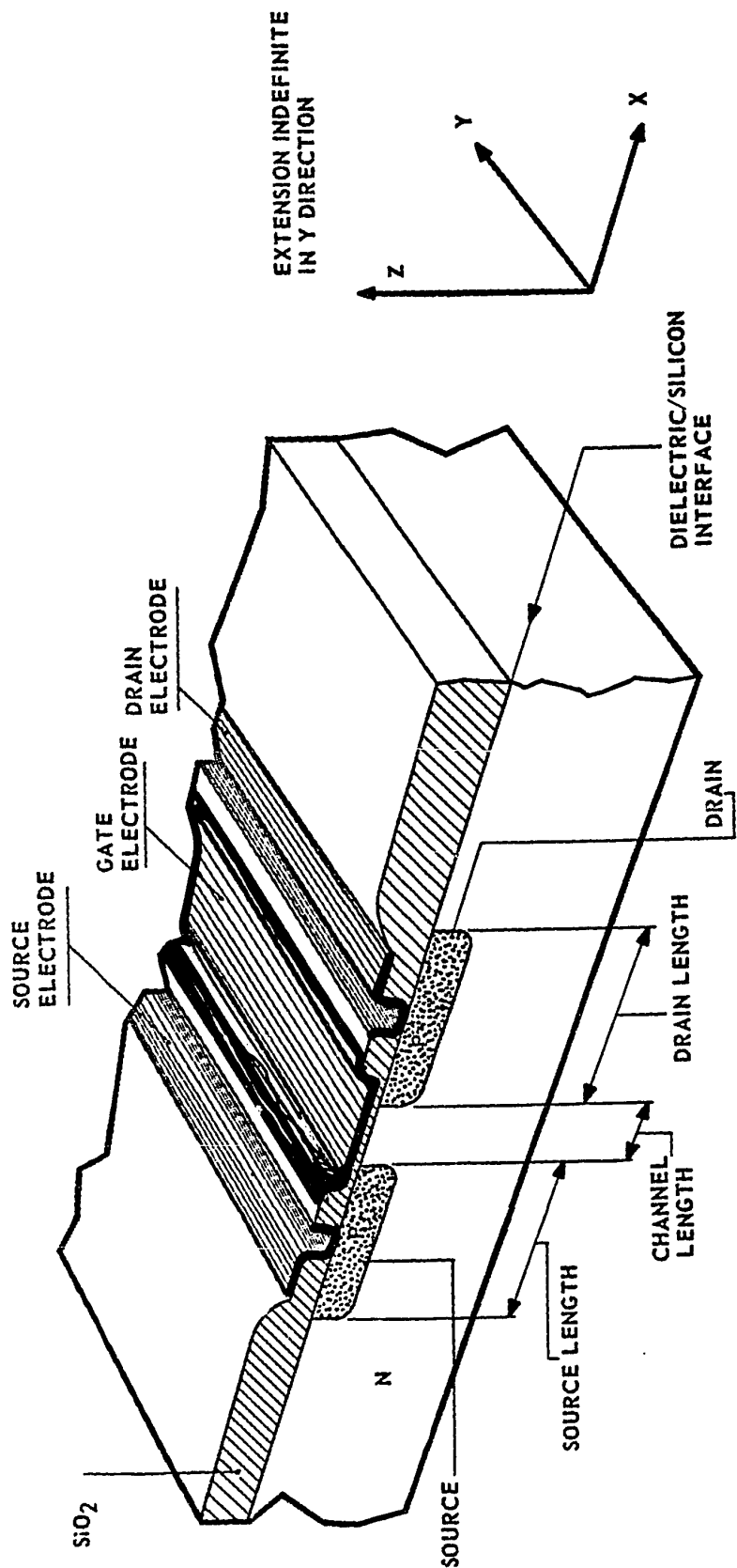


Fig. 2 A perspective view of an MOS device

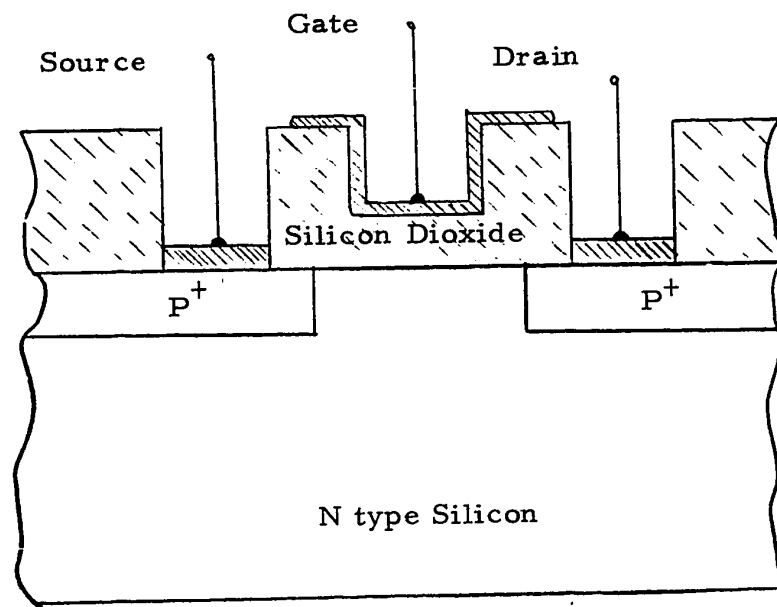


Fig. 3 Cross-sectional view of P channel enhancement type MOS device showing raised oxide over source and drain regions to reduce capacitances from gate to source and to drain









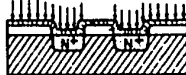




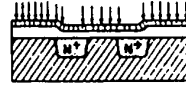

Contacts are made to the substrate, the two p^+ diffused regions and the isolated aluminium layer or gate. The aluminium layer, the silicon dioxide layer and the semiconductor form a parallel plate capacitor. Hence if a negative voltage is applied to the aluminium gate relative to the substrate, there will be a negative charge at the surface of the semiconductor. The positive charge at the surface of the semiconductor is obtained by repelling electrons from the surface of the semiconductor and attracting holes either from the p^+ regions or from those formed by thermal generation in the n-type silicon bulk. The positive charge induced in the semiconductor will fill any negative states at the silicon-dioxide/semiconductor interface and neutralize any negative impurity centres at the surface of the semiconductor. Excess holes will form free carrier centres. Thus, if a field is applied to the holes along the surface, conduction will occur. The transverse field can be obtained by applying a voltage between the two p^+ regions. If the right-hand region (or drain) is made negative with respect to the left-hand region (or source) there will be a hole flow from the source to the drain. Thus, a charge on the gate results in a charge near the surface of the semiconductor which is free to move at right angles to the electric field producing it and the quantity of charge, hence the conductivity of the channel thus produced, is controlled by the gate voltage. Such a transistor in which conduction is by holes is known as a p-channel MOS device. The complementary type in which conduction is by electrons is known as an n-channel MOS device.

II-3 Fabrication

The fabrication techniques used to produce MOS devices are similar to those used for modern high speed silicon bipolar transistors. The substrate material for an n-channel device is a lightly doped p-type silicon wafer. (Reversal of n-type and p-type materials referred to in this description produces a p-channel device.) After the wafer is polished and oxidized in a furnace, photolithographic techniques are used to etch away the oxide coating and expose bare silicon in the source and drain regions. The source and drain regions are then formed by diffusion in a furnace containing an n-type impurity (such as Phosphorus). If it is to be an enhancement type device, no channel diffusion is required and if a depletion type device, an n-type channel is formed in a separate diffusion to bridge the space between the diffused source and drain.

The wafer is then oxidized again to cover the bare silicon regions, and a second photolithographic and etching step is performed to remove the oxide in the contact regions. After metal is evaporated over the entire wafer, another photolithographic and etching step remove all metal not needed for the ohmic contacts to the source, drain and gate.

A series of illustrations of the process is shown in Fig. 4

- (a)  The P-type wafer is cut, lapped, and polished.
-
- (b)  The silicon dioxide masking layer is grown.
-
- (c)  Photoresist is applied over the silicon dioxide.
-
- (d)  The photoresist is exposed to ultraviolet light through a mask to form the drain-source diffusion window pattern.
-
- (e)  The resist is developed and the unexposed resist is removed. Then, using an etching solution, the windows are cut through the masking oxide.
-
- (f)  The remaining photoresist is removed.
-
- (g)  The N^+ drain and source regions are diffused into the wafer through the windows.
-
- (h)  The wafer is covered with photoresist again.
-
- (i)  The photoresist is exposed to ultraviolet light through a mask that leaves the area above the channel region unexposed.
-
- (j)  The resist is developed and the unexposed resist is removed. The oxide directly above the channel region is then etched away.
-
- (k)  The remaining photoresist is removed.
-
- (l)  The insulating oxide layer is grown with safeguards to prohibit ionic drift.
-
- (m)  Once again, the wafer is coated with photoresist.
-
- (n)  The photoresist is exposed to ultraviolet light through a mask to form the drain-source contact window pattern.
-
- (o)  The resist is developed and the unexposed resist is removed. Then, the contact windows are cut through the insulator oxide, using the etching solution.

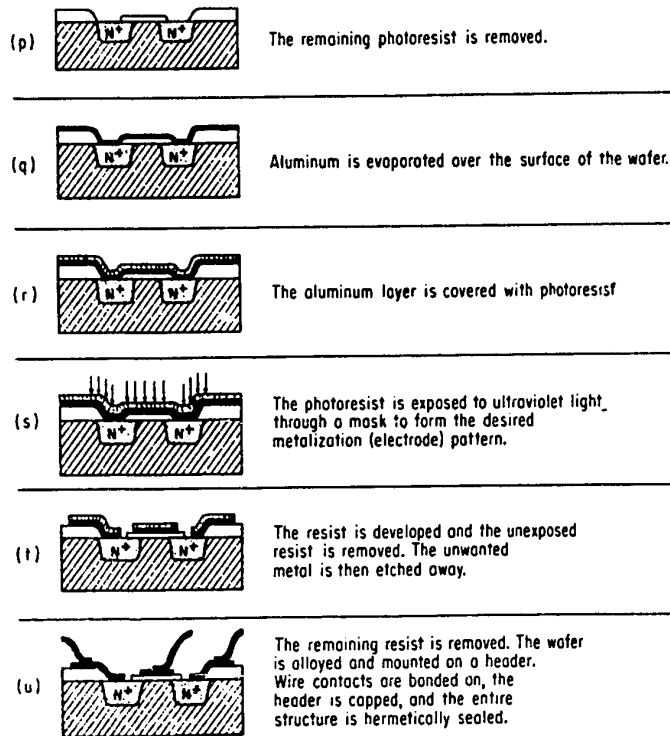


Fig. 4 The process of fabricating MOS devices

II-4 Types of MOS Field Effect Device

The properties of the two basic types of MOS field effect device introduced in the section on terminology are now considered in detail.

- (1) **Enhancement-type:** The gate must be forward biased to produce active carriers and permit conduction through the channel. No useful channel conductivity exists at either zero or reverse gate bias. Charges induced by the gate voltage below the threshold value are immobile and do not contribute to currents that eventually flow in the channel except for leakage current. These are sometimes called threshold devices.

In an enhancement-type device the gate electrode covers the entire channel, overlapping both source and drain regions. Any channel region which is left exposed contributes a very high series resistance to the device since there are few carriers in the channel at zero gate bias. The overlap results in a substantial capacitance from gate-to-source and gate-to-drain unless special provisions are made.

From now on, for the sake of simplicity, only p-channel enhancement-type MOS devices will be discussed if not otherwise specified. The principles of operation and the

design techniques that follow can also be applied to its complementary types except for the change of battery supply voltage direction.

- (2) Depletion type: The channel region between the source and drain is made of material of the same conductivity type. Charge carriers are present in the channel when no bias voltage is applied to the gate. A reverse gate voltage is one which depletes this charge and thereby reduces the channel conductivity. A forward gate voltage draws more charge carriers into the channel and thus increases the channel conductivity.

Unlike the enhancement device, the depletion unit does not require the gate electrode to overlap both source and drain regions as illustrated by the offset gate geometry shown in Fig. 5 for a high-frequency unit. The unmodulated portion of the channel near the drain electrode introduces some series resistance in the saturation region. The addition of a series drain resistance merely increases the drain voltage at which drain current saturates. So long as the small signal output resistance of the device is large, with respect to the unmodulated drain resistance, there will be little deterioration in circuit gain. However, any series source resistance introduces degeneration and

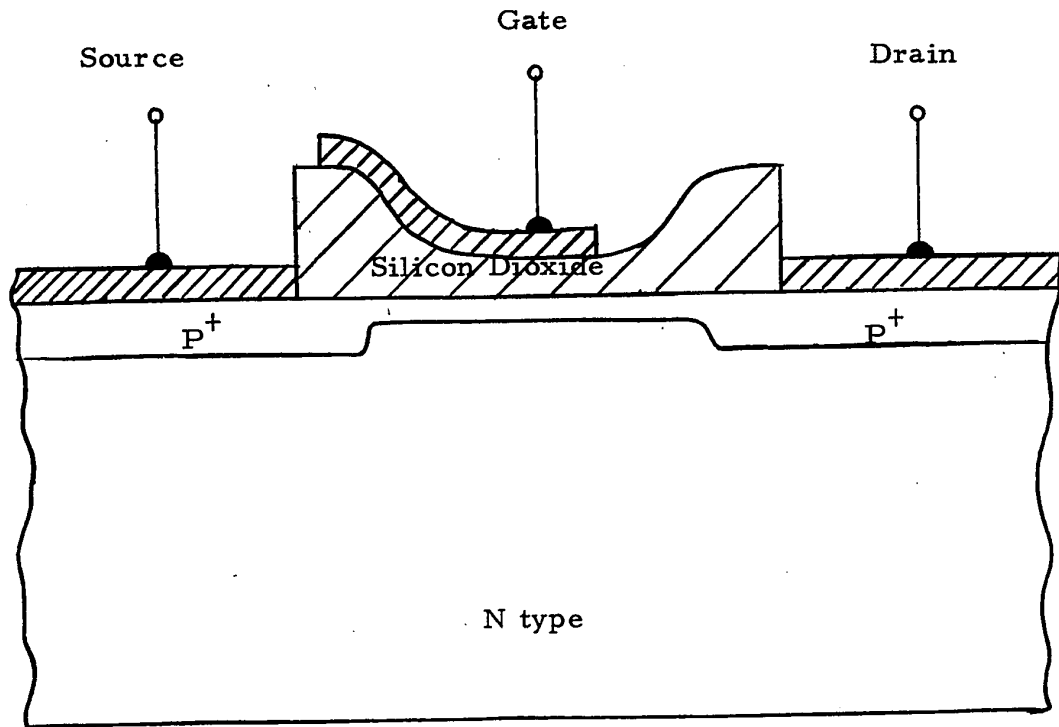


Fig. 5 In depletion type field effect device, the gate need not overlap source and drain. Offset geometry reduces feedback capacitance from drain to gate when the device is operated in current saturation region

is undesirable. Thus, the gate electrode is frequently allowed to overlap the source region.

When the gate electrode is offset, in this way, the feedback capacitance is reduced, since the active channel length is forced to coincide with the portion of the gate electrode which lies over the channel. The only inactive part of the input capacitance results from the overlap of the source electrode. The exact distribution of active gate capacitance between source and drain is difficult to determine, but the depletion of majority carriers near the drain end of the active channel considerably reduces the feedback capacitance, when the device is in saturation.

II-5 Theory Of Operation

To derive a simplified theory of the operation of insulated gate field effect devices, certain assumptions will be made. These are:

- (1) All the carriers induced in the semiconductor are free carriers
- (2) The induced charge is determined only by the capacitance of the silicon dioxide structure
- (3) The mobility of the carriers is constant.

The channel sheet conductance δ , at a point, X along the channel is a function of the channel voltage at that point, $V(X)$, the applied gate voltage V_g , and the threshold voltage, V_T

$$\begin{aligned} \delta &= f(V_g, V_T, V(X)) && \text{when } (V_g - V(X)) > V_T \\ \delta &= 0 && \text{when } (V_g - V(X)) \leq V_T \end{aligned} \quad (1)$$

The channel current per unit width, I , at this point in the channel is therefore:

$$I = \delta E = f(V_g, V_T, V(X)) \frac{dV}{dX} \quad (2)$$

Since the current must be constant from the source to drain, integration yields;

$$I_{ds} = \frac{1}{l} \int_0^{V_D} f(V_g, V_T, V(X)) dV_X \text{ for } V_D < V_g - V_T \quad (3)$$

where l is the channel length, V_D is the applied drain voltage, and I_{ds} is the drain current per unit channel width.

MOS devices are constructed with a shallow channel (the channel depth in the silicon is much less than the oxide thickness), which is about 1000 \AA . The voltage drop from the surface through the channel into the semiconductor is small compared with the voltage drop across the oxide and may be neglected. The channel sheet charge density, ρ , is then given by:

$$\rho = C_o [V_g - V_T - V(X)] \quad \text{for } V(X) \leq (V_g - V_T) \quad (4)$$

Where X is the distance along channel from source to drain. The channel sheet conductance is given by:

$$\sigma = \mu_o \rho = C_o \mu_o [V_g - V_T - V(X)] \quad (5)$$

Where C_o is the oxide capacitance per unit area and μ_o is the carrier mobility. Combining equations (3) and (5) yields:

$$I_{ds} = \left[\frac{C_o \mu_o}{2l} \right] [(V_g - V_T)^2 - (V_g - V_T - V_D)^2] \quad (6)$$

For $V_D = V_g - V_T$, the saturated current I_{ds} is :

$$I_{ds} = \frac{C_o \mu_o}{2l} (V_g - V_T)^2 \quad (7)$$

As V_D approaches $V_g - V_T$ space charge dominated currents are generated in the drain region. This space charge region becomes dominant over the gate controlled charge at the point in the channel, where the voltage is essentially $V_g - V_T$. From this point it extends to the drain where the voltage is V_D . The current appears to saturate because the length of the space charge region is generally much smaller than the over-all channel length. The source region of the channel, or that region from the source to the junction with the drain space charge region, therefore predominates in determining the current. Since the region length is fairly constant and the voltage drop across it is fixed at $V_g - V_T$ the current flow is essentially fixed as shown

in Fig. 6. Further increases in drain voltage above $V_g - V_T$ are absorbed across this drain region with only a slight modulation of the source region length. The saturation of drain current is therefore basically dependent on geometry.

If the saturated current is differentiated with respect to gate voltage, the transconductance g_m is obtained:

$$g_m = \frac{C_o \mu_o}{l} (V_g - V_T) \quad (8)$$

Equations (4) through (8) apply for shallow devices.

II-6 Electrical Characteristics

Output characteristic curves for the four types of MOS device are shown in Fig. 7. In the saturation or pinch-off region, the dynamic output resistance of the device may be approximated from the slope of the output characteristic curves at any given set of conditions.

Typical transfer characteristics for p-channel MOS devices are shown in Fig. 8. The threshold voltage shown is a critical parameter in circuit designs. One type of MOS device currently on the market has its threshold voltage specified between -1.5 to -6 volts. This can result in a considerable variation of channel current. The reasons for the instabilities of the threshold voltage are discussed in section II-8.

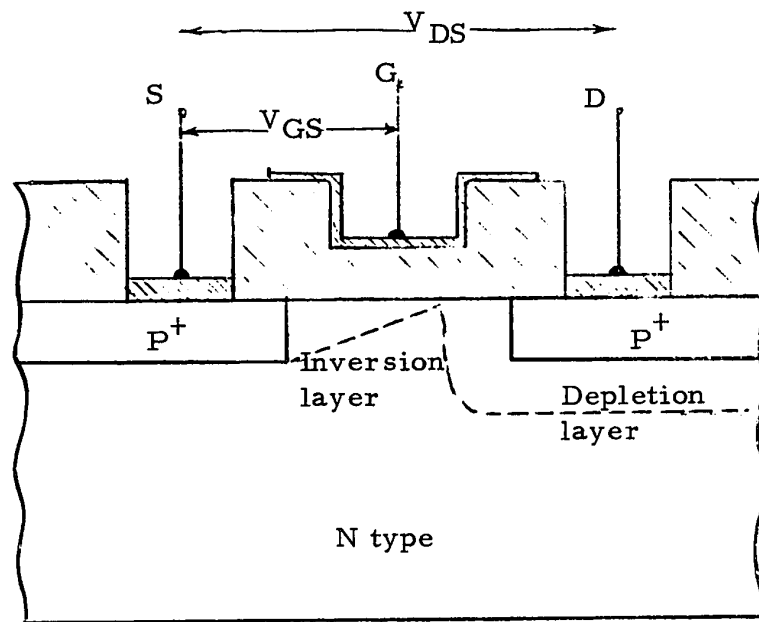


Fig. 6 Cross sectional view of MOS device showing the inversion layer depletion layer

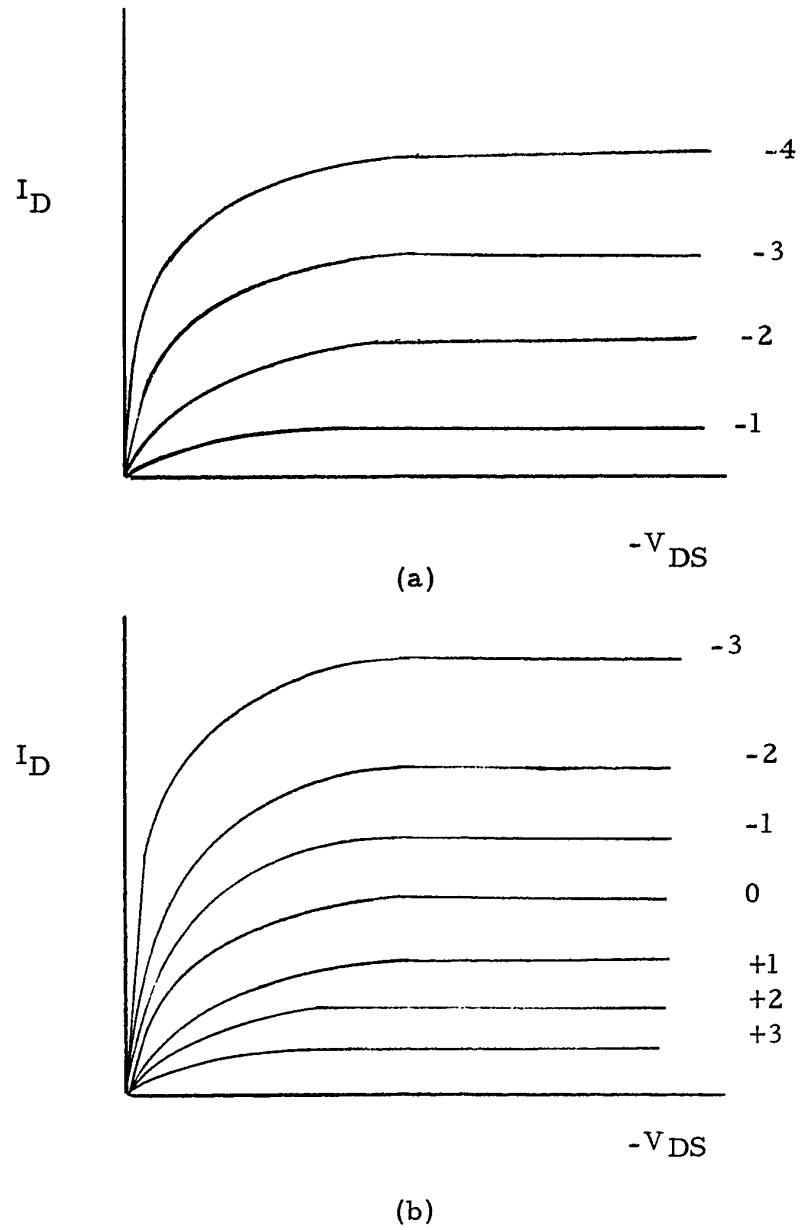
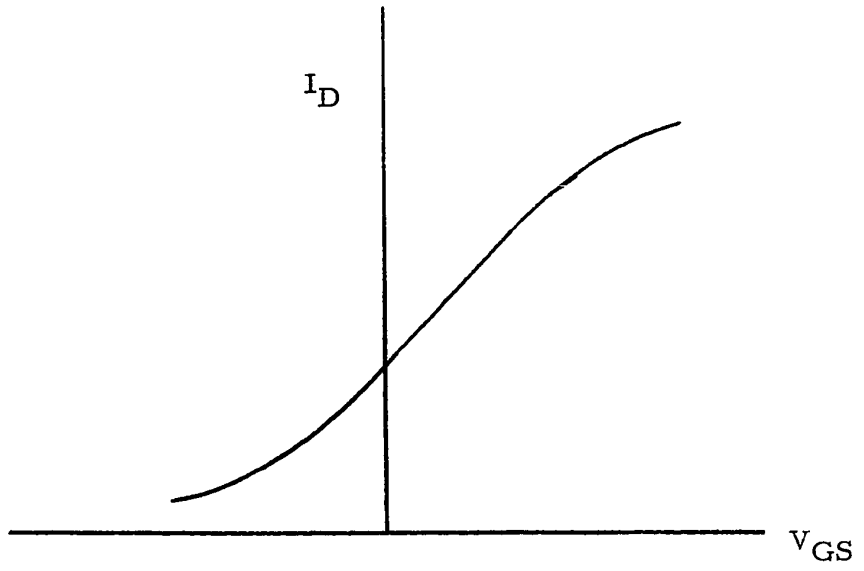
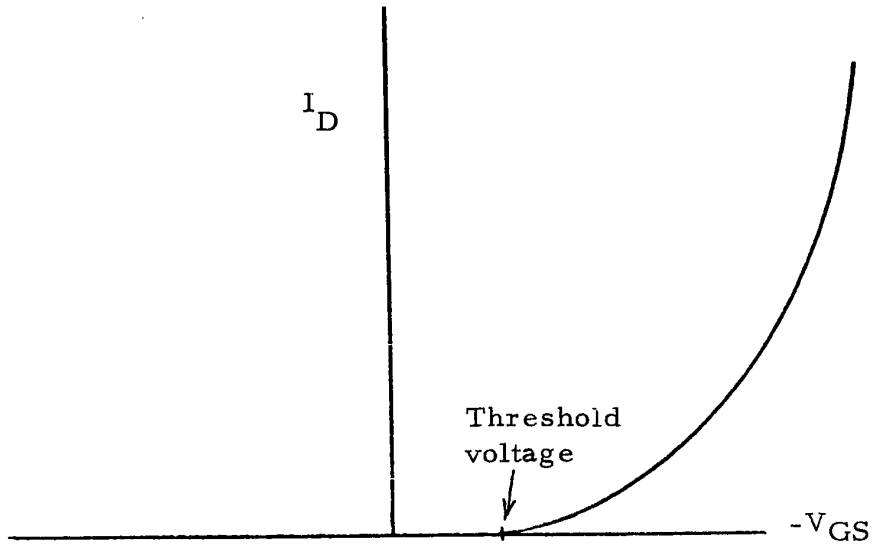


Fig. 7 Output characteristic curves for n-channel MOS device
(a) Enhancement type (b) Depletion type



(a) Depletion type



(b) Enhancement type

Fig. 8 Typical transfer characteristics for n-channel MOS device

II-7 Regions of Operation

The basic current-voltage relationship for a p-channel enhancement type MOS device, operating in the common source configuration, is shown in Fig. 9. At low drain to source potentials and with the gate bias large enough to produce channel conduction, the resistance of the channel is essentially constant and the current varies linearly with voltage, as illustrated in region A-B. As the current is increased beyond point B, the voltage drop IR in the channel produces a progressively greater voltage difference between the gate and points in the channel successively closer to the drain. As this potential difference between gate and channel increases, the drain current increases much more slowly with the further increases in drain to source voltage and saturation is reached, region B-C. Further increases in drain to source voltage beyond point C produce no significant change in drain current until point D, when the device enters the breakdown region, and the drain current may increase rapidly.

The saturation region between points B and D in Fig. 9 is the region in which MOS devices are especially useful as high impedance voltage amplifiers. In the ohmic region, between A and B,

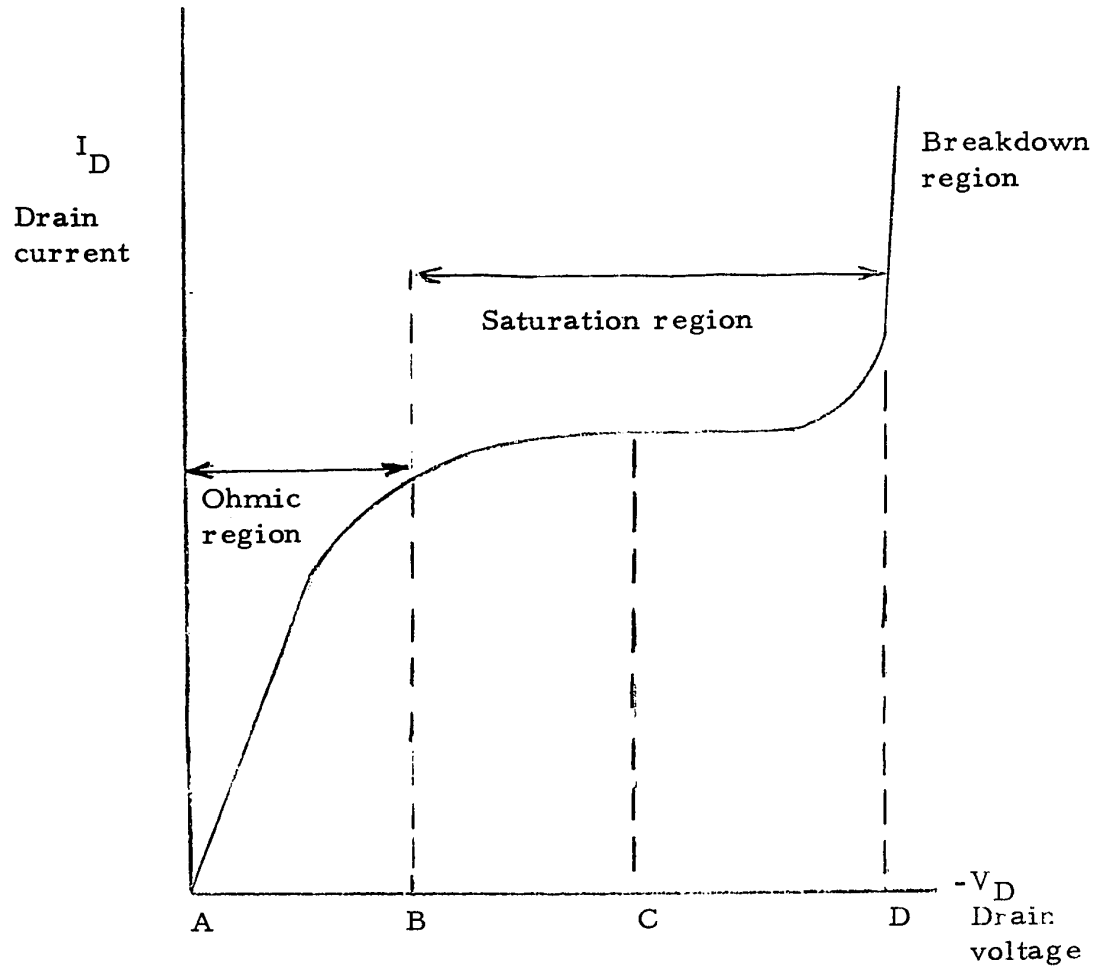


Fig. 9 Current-voltage characteristic of an MOS device showing the three possible operating regions

the linear variation in channel resistance makes them useful in voltage controlled resistor applications such as the chopper unit at the input of some dc amplifiers.

The maximum allowable drain voltage is limited by avalanche multiplication of channel current. The gradual breakdown becomes greater for increasing gate voltage and drain current. The soft gradual breakdown characteristic is caused by the generation of hole electron pairs in the high field of the drain region by impact ionization. Since these holes and electrons act partially as a shielding plasma, the onset of severe avalanching is spread out over a wider voltage range than the asymptotic sharp breakdown to the substrate.

Possible applications of this gate modulated breakdown phenomenon have been considered by Atalla⁹, Hofstein and Warfield¹⁰, Nathanson, Szedon and Jordan¹¹ and Shockley and Hooper¹².

II-8 Instabilities in MOS devices

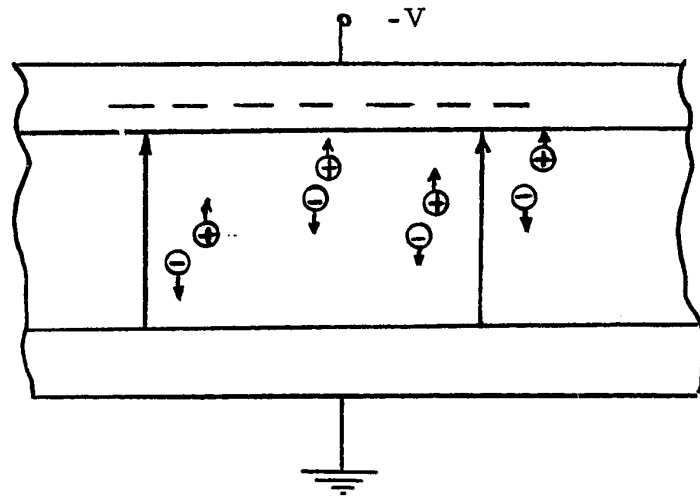
MOS devices operating with electric fields in the order of 10^6 V/cm in the oxide have shown instabilities of characteristics

which have been related to the motion of ions and molecules in silicon dioxide and other insulating films.

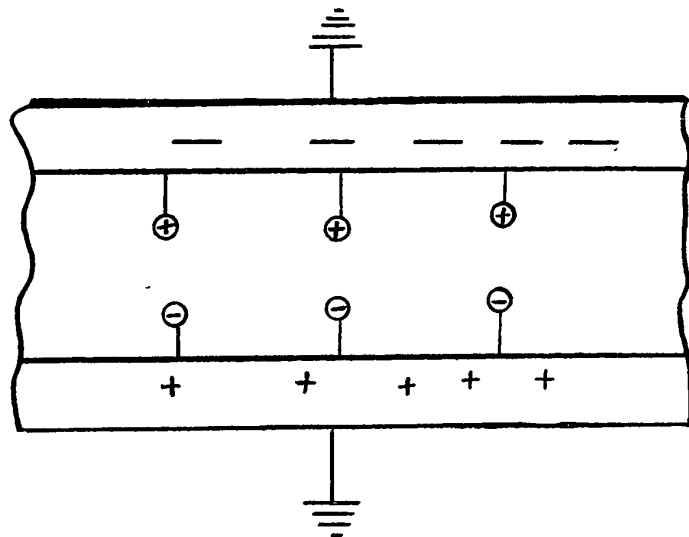
The suggested mechanism of this instability is as follows. Assume that the oxide layer contains mobile polyatomic molecules, which may be easily dissociated. The application of a negative potential to the gate electrode of a p-channel device will tend to move the positive ions toward the gate electrode and the negative ions toward the silicon surface. When the gate bias is removed from an enhancement device a field in the oxide layer remains which is opposite to the original field that caused the migration, as shown in Fig. 10.

The details of this mechanism are not well understood. However, the foregoing discussion indicates qualitatively, in schematic form, what might be happening. It has been suggested that the type of ion moving in the silicon dioxide layer is a positively charged oxygen vacancy, which allows only positive charge in insulating layer.

This effect may be observed by examining the transfer characteristic of a p-channel enhancement device before and after the application of a large negative gate bias for an extended period of time. Initially, the transfer characteristic appears as shown in the right hand curve of Fig. 11. After the application of gate voltage, the



(a)



(b)

Fig. 10 Migration of ions in the bulk of the silicon dioxide layer can cause a drift in the device characteristics. (a) Oxide field causes ions to drift (b) Finite electric field exists when gate potential is reduced to zero

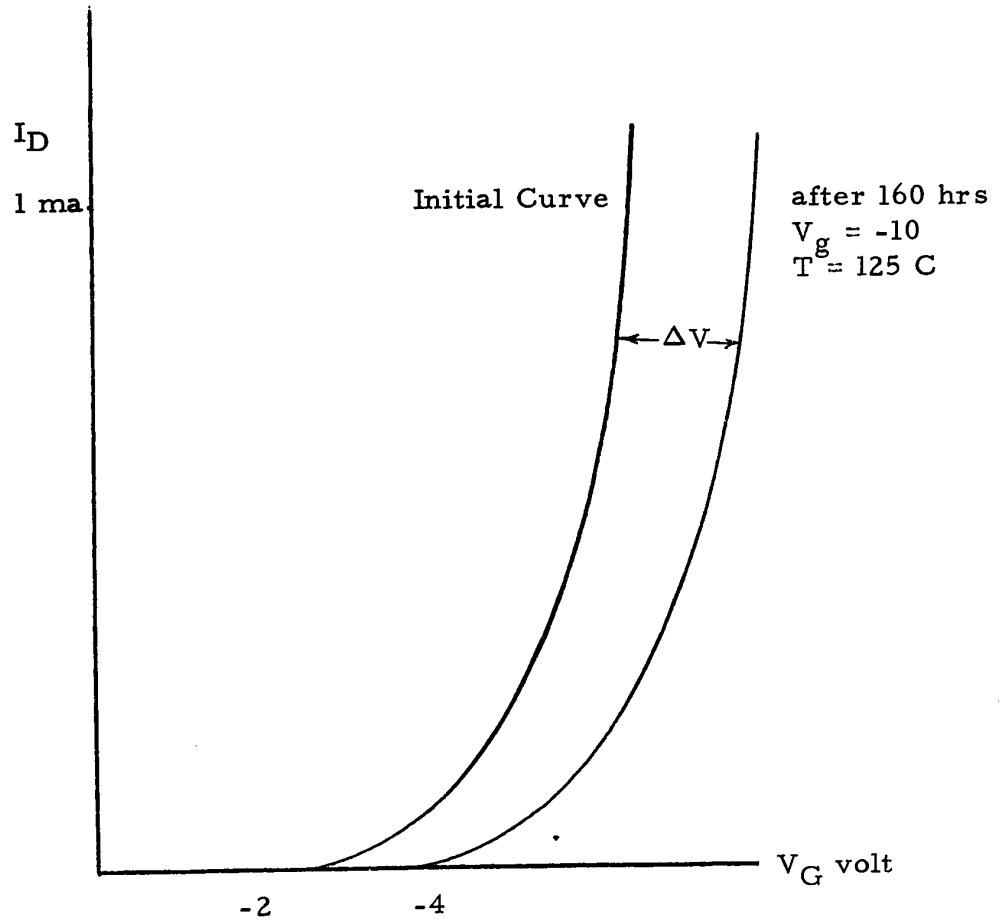


Fig. 11 Transfer characteristic curve shifting of p-channel MOS device due to drift

curve drifts to the right and the instability can be quantitatively characterized by the voltage shift ΔV . This quantity increases with temperature, time of application, and electric field strength. In some units, drift is observed until a maximum value of ΔV is observed, while in other, ΔV seems to increase continually with time.

Recently, there have been considerable fabrication improvements aimed at reducing this drift, that is, when this type of instability was first observed values of ΔV as large as 5 or 6 V were observed; now it is possible to limit the drift to less than 0.5 V by diffusing Phosphorus into the oxide layer before metalization of the device. Silicon dioxide is an open lattice structure having a mean lattice spacing of about 8 Å. The addition of Phosphorus forms a glass like structure which is more dense than silicon dioxide. This may reduce the mobility of the ions, producing a more stable oxide. More recent work has indicated that many of the impurity ions are introduced when the gate electrodes are fabricated and that stability can be improved by clean processing alone.

II-9 Comparisons

MOS devices presently offer a number of advantages and disadvantages compared with double diffused integrated circuits.

Advantages include:

- (1) Low power consumption in switching circuits, especially when complementary switching pairs are employed.
- (2) Extremely high input impedance (10^{14} ohms).
- (3) Good square law behavior. Although the device is non-linear, its law is accurately known and can be compensated.
- (4) It is possible to make devices with desired levels of operating bias.
- (5) The input impedance stays high and constant both inside and outside the normal operating range.
- (6) Resistors, capacitors and cross-overs can be readily fabricated as part of MOS arrays.
- (7) Outstanding packing density. An MOS device generally occupies one square mil compared with 24 mils for a typical double diffused integrated circuit transistor.
- (8) Low input capacitance. This can be in the fractional picofarad range for arrays.
- (9) Choice of operation in the enhancement or depletion modes.
- (10) Fewer manufacturing steps. One diffusion is required for MOS circuits compared with at least four for double diffused bipolar integrated circuits.

Disadvantages include:

- (1) Delicate gate insulation. e. g. Electrostatic charges accumulated by walking in crepe or rubber soles on a dry day are sufficient to permanently rupture the silicon dioxide layer between the gate metal and the silicon bulk. This happens if the accumulated electrostatic voltage exceeds the breakdown voltage (130V) of the gate and poses a serious production handling problem.
- (2) Limited compatibility with non-MOS elements. High output impedances can cause either speed or power loss in cases of extreme mismatch. Special circuit techniques are necessary to eliminate such problems.
- (3) Power limitation. Present MOS devices cannot handle large powers.
- (4) Dc drift. The instabilities of MOS devices pose major problems in dc biasing and ac gain of linear amplifiers.

III Equivalent Circuits for MOS Devices

In this chapter, equivalent circuits consisting of linear elements and ideal rectifier diodes for MOS devices are presented. First, piecewise linear models are developed from graphical terminal characteristics. Then, nonlinearity is removed for the small signal model by considering the diode operating states and remaining parameters adjusted to give a more accurate representation of the operating principle of the device. Frequency dependence is also taken into account.

III-1 Piecewise Linear Circuit Model

Typical I_D - V_D characteristics of an MOS p-channel enhancement type device are shown in Fig. 12. The curves can be divided into three portions: (A) Operation below saturation (B) Operation at saturation and (C) Breakdown, as shown in Fig. 12. At low drain to source potentials, the channel resistance is essentially bilateral. This linear resistance varies as a function of gate voltage. Above the threshold voltage, the device is useful as a high impedance voltage amplifier. We are therefore interested in portions (A) and (B). Circuit models will be developed for these two portions separately.

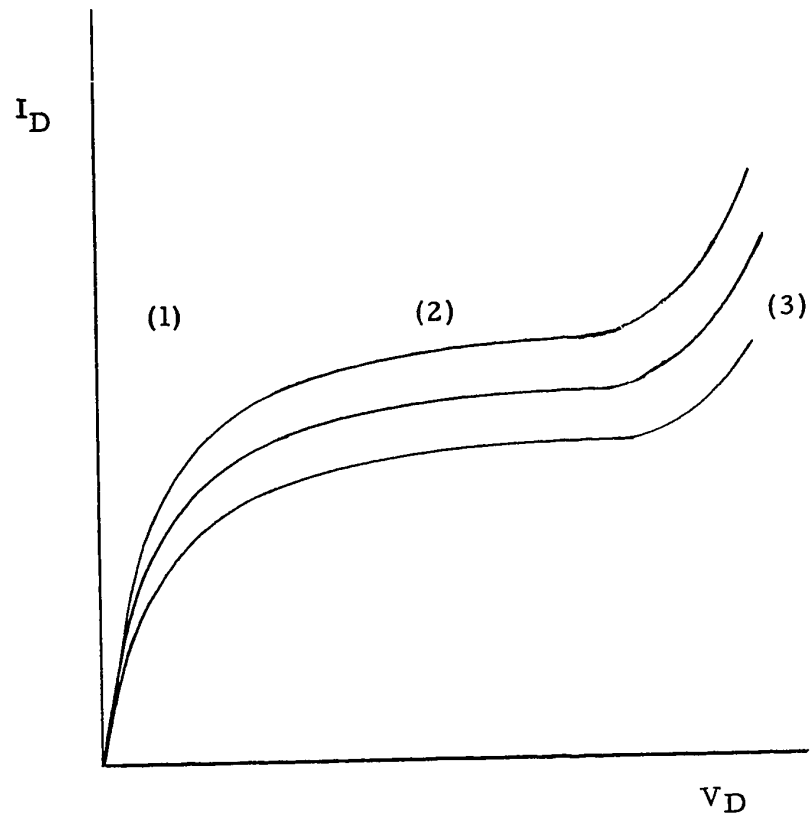


Fig. 12 Regions of Operation

(A) Operation below saturation

As presented in section II-5, the input of the device may be represented as a capacitor. Below the threshold voltage, the device acts like a resistor, the resistance being a function of the gate voltage V_g and a simple equivalent circuit is shown in Fig. 13. Before saturation is reached the drain current I_D , is given by

$$I_D = \mu_o C_o ((V_g - V_T)V_D - V_D^2/2) \quad (6)$$

consequently,

$$R_D = 1 / \mu_o C_o (V_g - V_T - V_D/2)$$

Thus in the region under consideration

$$A = 1 / \mu_o C_o$$

(B) Operation in the saturation region

The main feature of interest in these characteristics is that I_D is function of V_g and nearly independent of V_D . This suggests a circuit model of the type shown in Fig. 14. D_{sb} and D_{db} are the p-n junctions formed between drain and source and the bulk n silicon. The gate voltage is identified as the control variable. The proportionality constant for the controlled source is the transconductance of the model, defined by:

$$g_m = \partial i_d / \partial v_g \quad \text{where } V_D \text{ is a constant held}$$

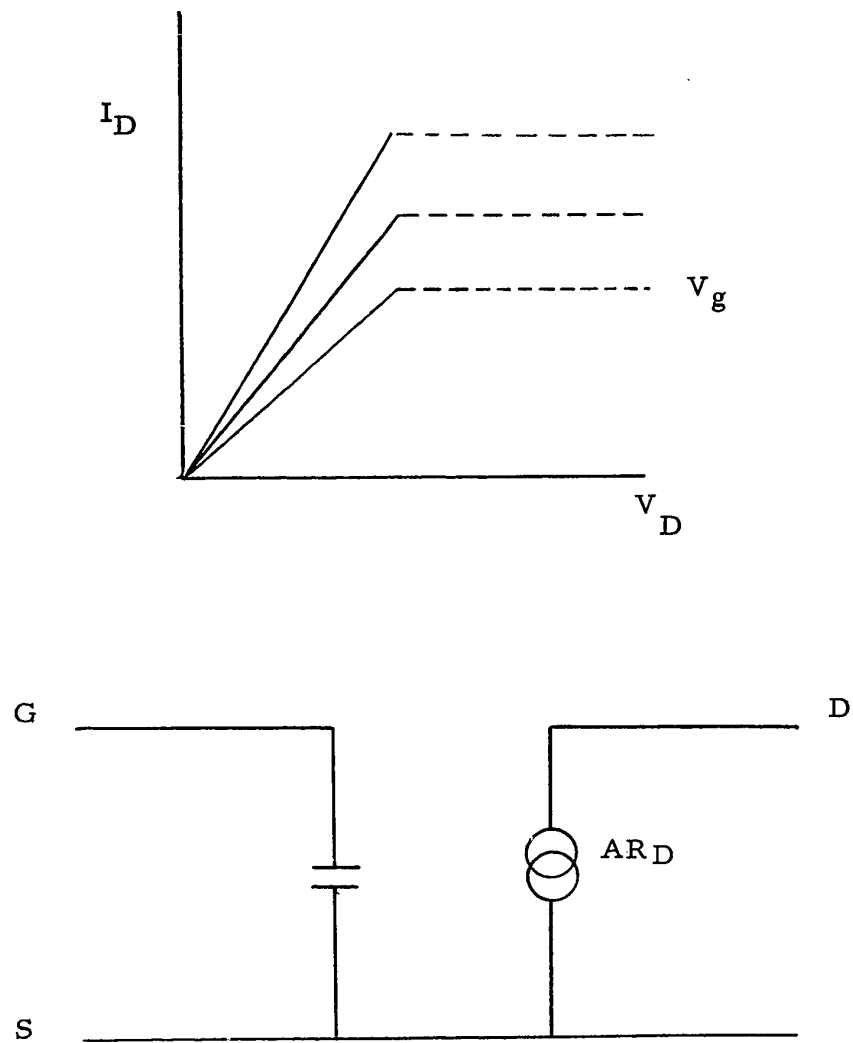


Fig. 13 Equivalent circuit of MOS device before saturation

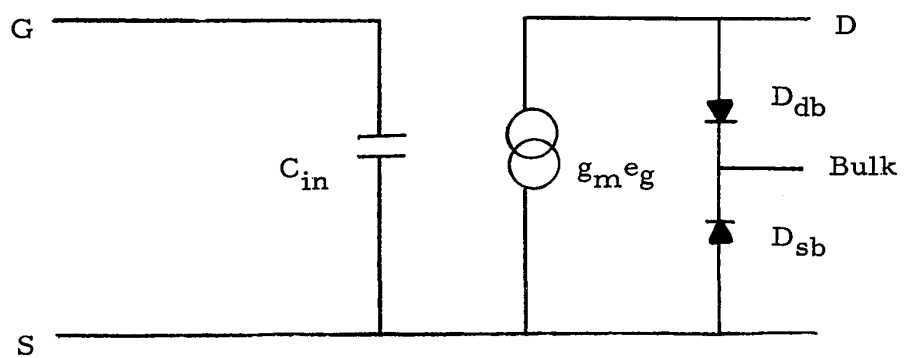
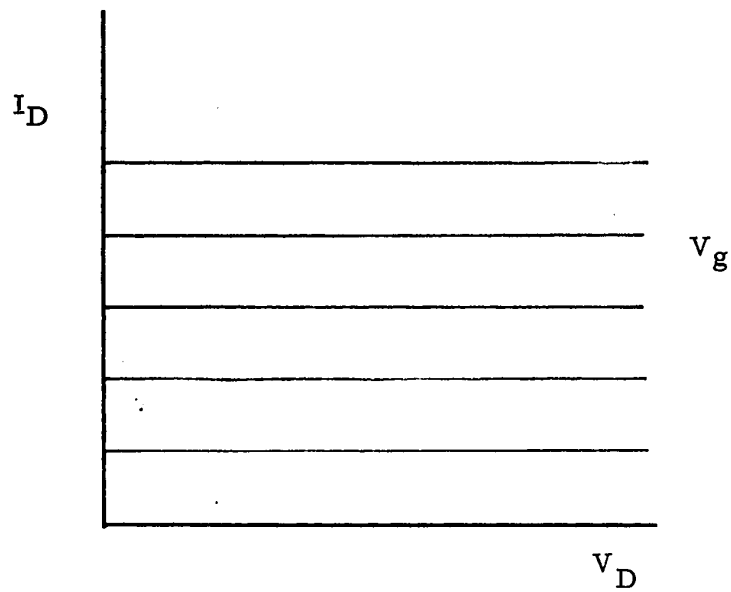


Fig. 14 Piecewise linear equivalent circuit of MOS device

The circuit model shown in Fig. 14 is useful in problems where a simple representation of $V_D - I_D$ characteristics of the device is adequate. If a better approximation is required, a large resistance r_d placed across drain and source will give the output characteristics a constant slope, as shown in Fig. 15.

III-2 Small Signal Model

Up to this point, the discussion of the device characteristics has been concerned with graphical representations of the terminal characteristics and equivalent circuits which include non-linear elements. In this section, specific operating points will be selected and small signal equivalent circuits will be developed.

Consider the large signal models in Fig. 15. Diode D_{db} and D_{sb} can be eliminated by postulating that the bulk is usually connected to the source and the diode D_{db} is back biased. Since the resistances from gate to source and gate to drain, in practical cases, are never infinite, there are leakage resistance paths across the insulating oxide from gate to source and gate to drain. These can be represented by r_{gs} and r_{gd} , as shown in Fig. 16. Furthermore, if the bias point in the saturation region is known, we may choose values of g_m and r_d which reflect the local behavior of the graphical characteristics.

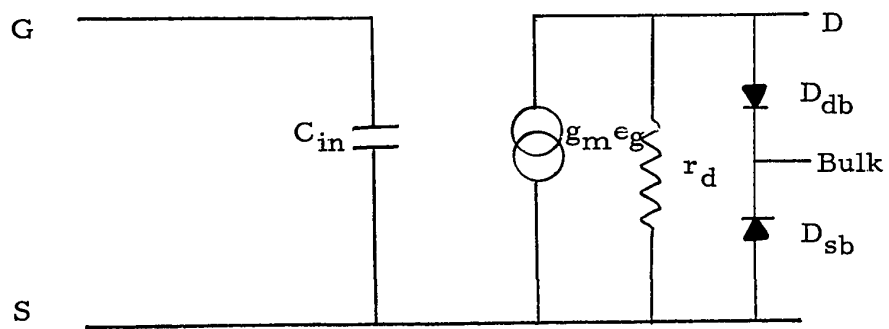
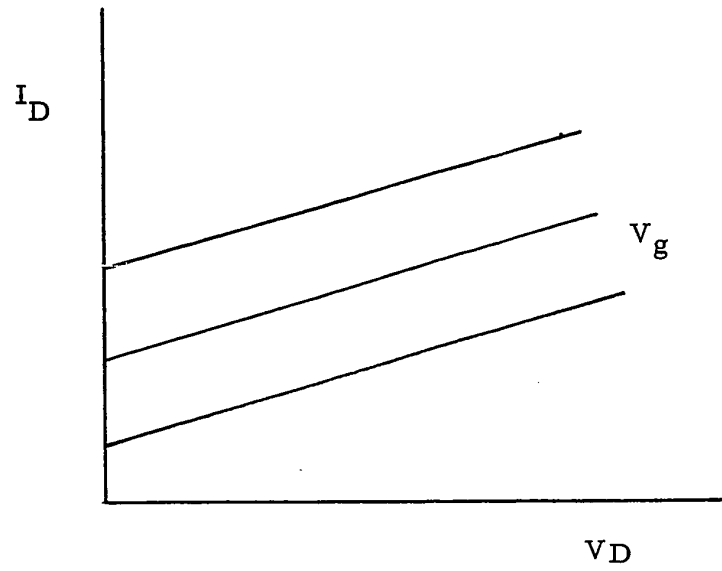


Fig. 15 Incorporating r_d in the equivalent circuit

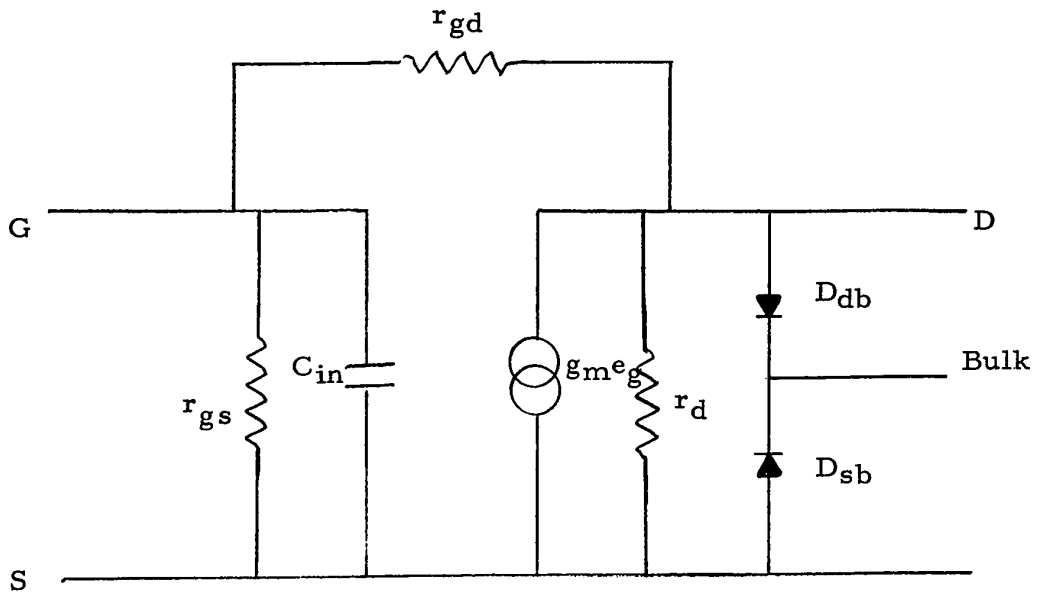


Fig. 16 Equivalent circuit of MOS device

Now considering the operating mechanisms, there is capacitance distributed along the metalized gate and the conducting channel. The capacitance distributed along the active channel resistance must charge and discharge through the channel resistance. This distributed network can be lumped in the form of series capacitance C_C and resistance r_C connected across gate and source as shown in Fig. 17. The voltage across C_C controls the mobile charge ^{which} ~~and~~ is the most important modulation parameter and the series resistance r_C is the lossy element. Thus, the equivalent circuit can be further improved by changing the controlled source. That is, the controlled source is dependent on the voltage across the channel capacitance, which in turn controls the charge. Consequently, the high frequency performance is a function of the time constant associated with r_C and C_C . The capacitance C_{gd}' is the intrinsic gate to drain capacitance.

The small signal equivalent circuit of the MOS device obtained by the above method is similar to the one given by Heiman and Hofstein¹³. Charge control characterization of field effect devices has been presented by Boothroyd²¹. The equivalent circuit of Boothroyd is similar to the circuit of Fig. 16 simplified. The two equivalent circuits are related in Fig. 18. The small signal equivalent circuit will be employed to calculate the gain, input and output impedance etc., in Chapter V.

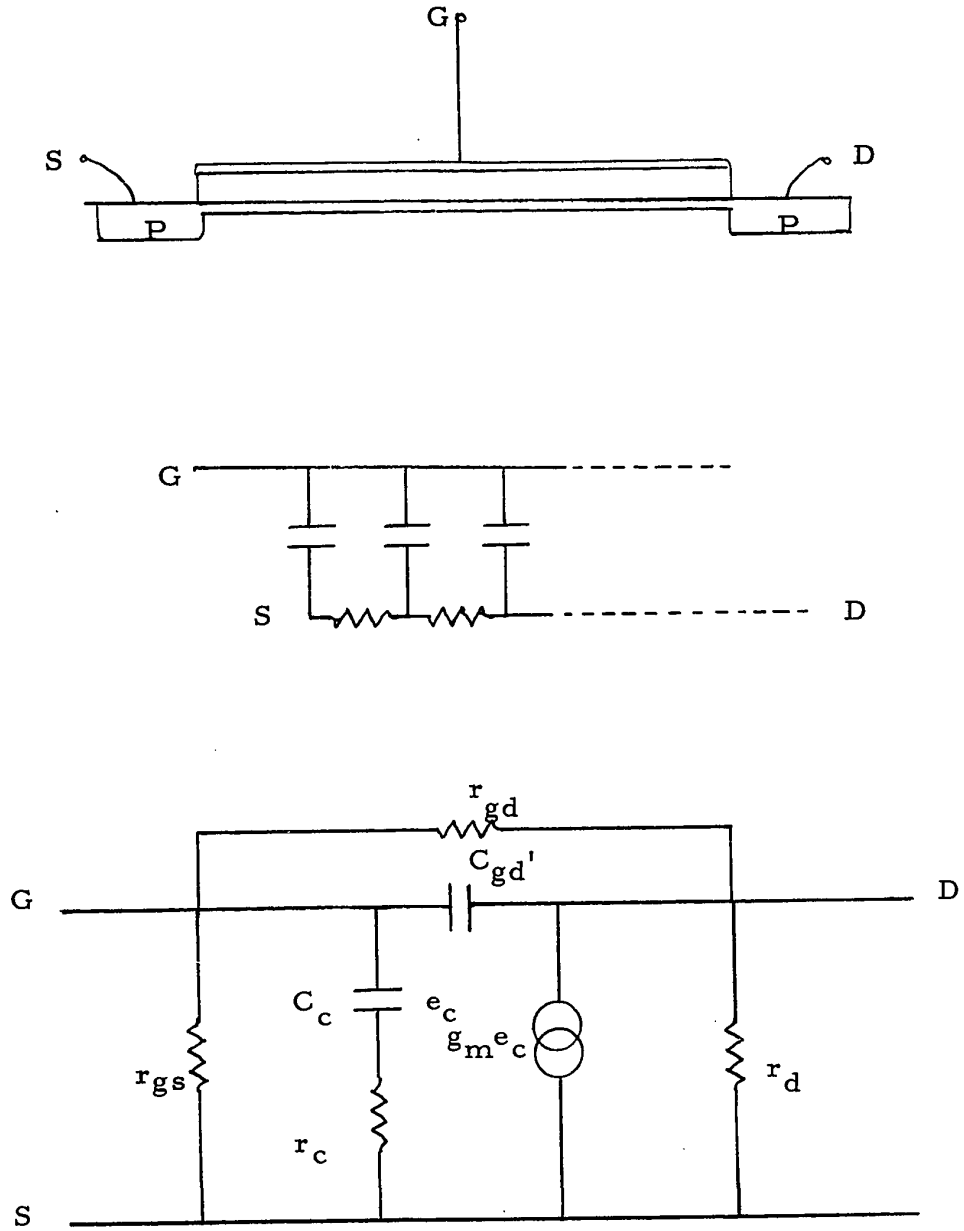
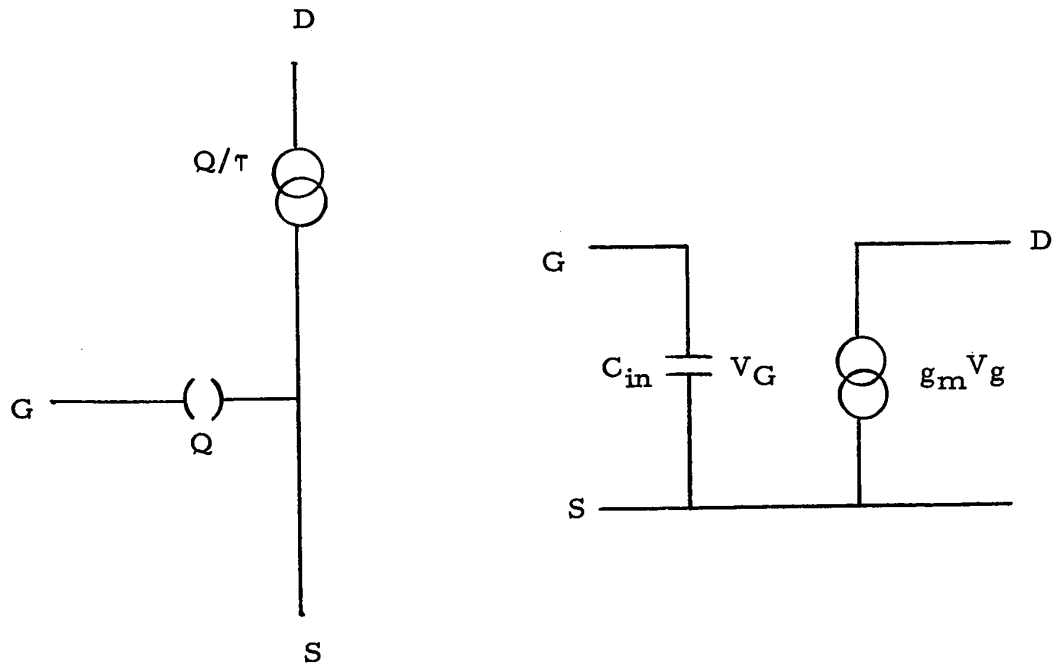


Fig. 17 Improved equivalent circuit of MOS device



$$I_D = (Q_o + Q_G + Q_D) / \tau = Q / \tau$$

$$I_D = g_m V_g$$

$$Q / \tau = g_m V_g$$

$$1 / \tau = g_m / C_{in}$$

Fig. 18 Charge control model

III-3 Gain Bandwidth

The upper frequency limit of semiconductor devices is closely related to τ , the transit time of the carrier²². In a field effect device, current is carried by majority carriers which drift across the channel under the drain to source field. Using the simplest type of analysis, τ can be calculated for the field effect device under the assumption of constant channel mobility μ_o .

$$\tau = l/v_d$$

$$v_d = \mu_o V_d/l$$

$$\tau = l^2/\mu_o V_D$$

where v_d is the average drift velocity in the channel and V_D/l is the drift field.

The gain-bandwidth product is defined as

$$GBW = C_{in}/2\pi g_m$$

However,

$$g_m = \mu_o C_{in} V_d/l^2$$

$$g_m/C_{in} = \mu_o V_d/l^2$$

Therefore

$$GBW = g_m/2\pi C_{in} = 1/2\pi\tau$$

Although parasitic elements and external circuits may reduce the actual speed of operation, C_{in}/g_m for an ideal field effect device is a useful figure of merit. An MOS field effect device of 10 μ m channel length typically will have an upper frequency limit in the range of hundreds of MHerz.

IV Amplifier Design and Stability

The preceding chapters have been concerned with the physics and electrical characterization of MOS devices. In this chapter, the design of simple amplifiers is discussed. As indicated in the introduction, the most significant single problem results from dc instabilities of the device (treated in section II-8). The MOS device is treated both as an active element and a load. Then solutions to the dc instability problems are presented. The chapter concludes with a discussion of the stability of multiple stage amplifiers.

IV-1 Basic Amplifier Configurations

There are three basic single stage amplifier configurations for field effect devices: common source, common drain, common gate. Each has characteristics which recommend it for use in particular applications. In the examples which follow, a p-channel MOS device is used for illustration, but all the results, except those relating to polarity, apply equally to n-channel MOS devices.

The three basic amplifier configurations are tabulated below:

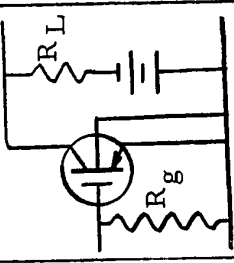
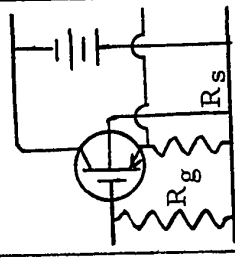
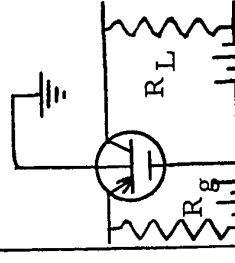
Amp. conf.	Ckt. diagrams	Voltage gain	Comments
<p>Common Source</p>		$\frac{g_m r_d R_L}{r_d + R_L}$	<p>1 High input resistance and several pf of input capacitance 2 Medium to high output impedance 3 Voltage gain greater than unity 4 Polarity reversal Application: Most frequently used configuration due to voltage gain larger than unity.</p>
<p>Common Drain</p>		$\frac{R_s}{((U+1)/U)R_s + 1/g_m}$	<p>1 Input resistance is similar to above, but the input capacitance is an order lower 2 Output impedance is low 3 Voltage gain is less than one 4 No polarity reversal Application: Reduced input circuit capacitance, downward impedance transformation, increased input signal handling capability, & low distortion</p>
<p>Common Gate</p>		$\frac{(g_m r_d + 1)R_L}{(g_m r_d + 1)R_g + r_d}$	<p>1 The input resistance is the same value as the output resistance of source follower, and capacitance is smaller 2 High output impedance 3 Voltage gain greater than unity 4 No polarity reversal Application: Transformation of low input impedance to a high output impedance, used in high frequency circuits because neutralization of feedback is not necessary in most applications</p>

Table I Basic Amplifiers

IV-2 Realization of load resistor using MOS devices

Three ways of connecting an MOS device as a load resistor are shown in Table II and the choice of the particular configuration is governed by the application and area of silicon available. A and B are the preferred connections because of the small area used, but the higher impedance of type C sometimes justifies its use.

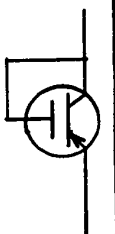
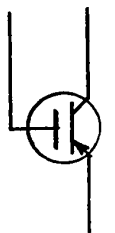
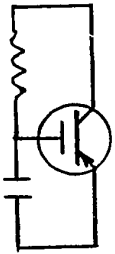
Ty.	Con.	R_L	Application	Comments
A		$\frac{2I^2}{\mu_0 C_0 V_D}$	Common source inverting amplifier	Small area used, but small signal value of resistance is lower than large signal value
B		r_d	Common drain amplifier	Large resistance in the order of r_d Similar area to above Small signal resistance is larger than large signal value
C		r_d	Common source amplifier	Large resistance in the order of r_d . But because of capacitor C, it requires a much larger area than A and B. The resistor R can be of the type in A.

Table II MOS devices as load resistors

IV-3 DC stability of Amplifiers

As indicated in section II-8, the threshold voltage of MOS devices drifts with time, temperature and bias voltage. Since the common source and common gate configurations have voltage gain, precautions must be taken to stabilize the working point in these configurations. Two methods will be discussed below, (a) source current stabilization and (b) output voltage stabilization. Both of these methods can yield equally stable amplifiers, but they differ in their power supply voltage requirements.

The dc stability of a circuit depends on the supply voltage, the threshold voltages and their respective stability. This is illustrated in Fig. 19 where

$$i = (V_S - nV_T + V_N) / R_L$$

V_S - Supply voltage

V_N - Total of all the variable voltage components
i. e. supply and threshold voltages in series

n - Number of threshold voltages in series

The stability is improved by arranging that $V_S - nV_T$ is much larger than V_N . Then $i = (V_S - nV_T) / R_L$. Hence it is preferable to use a configuration where there is a minimum number of threshold voltages in series and where this total voltage is small compared with the supply voltage.

(a) Source current stabilization

The source current may be stabilized by a similar technique to that used for emitter current stabilization of bipolar transistor. A typical circuit is shown in Fig. 20. The analysis of this circuit is as follows:

$$I_S = I_D$$

$$I_S = (V_{SS} - V_G) / R_S$$

$$V_{SS} - V_G \gg \pm 1 \text{ V}$$

The source current is equal to the drain current and since the effective gate voltage drifts with the threshold voltage $V_{SS} - V_G$ must be large. Source current stabilization presents a further difficulty, in that, when integrated, the source by pass capacitor must be large if the amplifier has a low frequency pass band, because the significant time constant is that of R_S and the by pass capacitor. Furthermore, there are several resistors in the circuit all of which suffer the above mentioned limitations of MOS devices. In this circuit, there are three MOS device threshold voltages in series.

(b) Output voltage stabilization

A simple and effective way to stabilize the output voltage is by dc feedback to the gate. This technique is applicable to any inverting amplifier, but the single stage, illustrated in Fig. 21, will

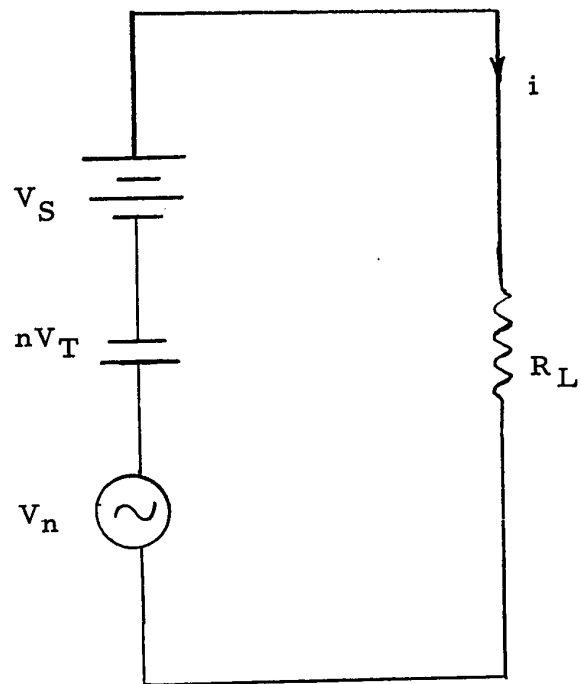


Fig. 19 Equivalent dc circuit of MOS amplifier

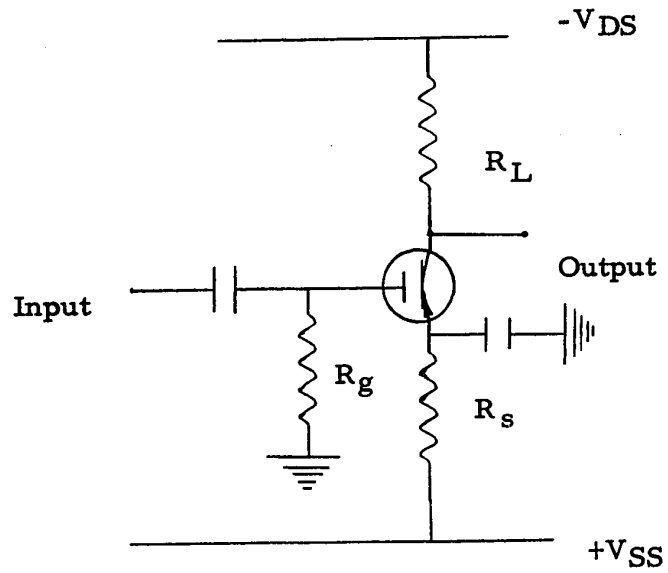


Fig.20 Source current Stabilization

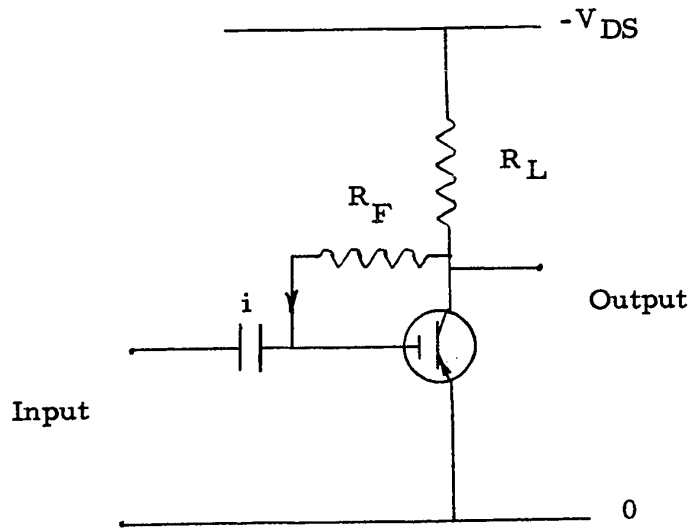


Fig. 21 Output voltage stabilization

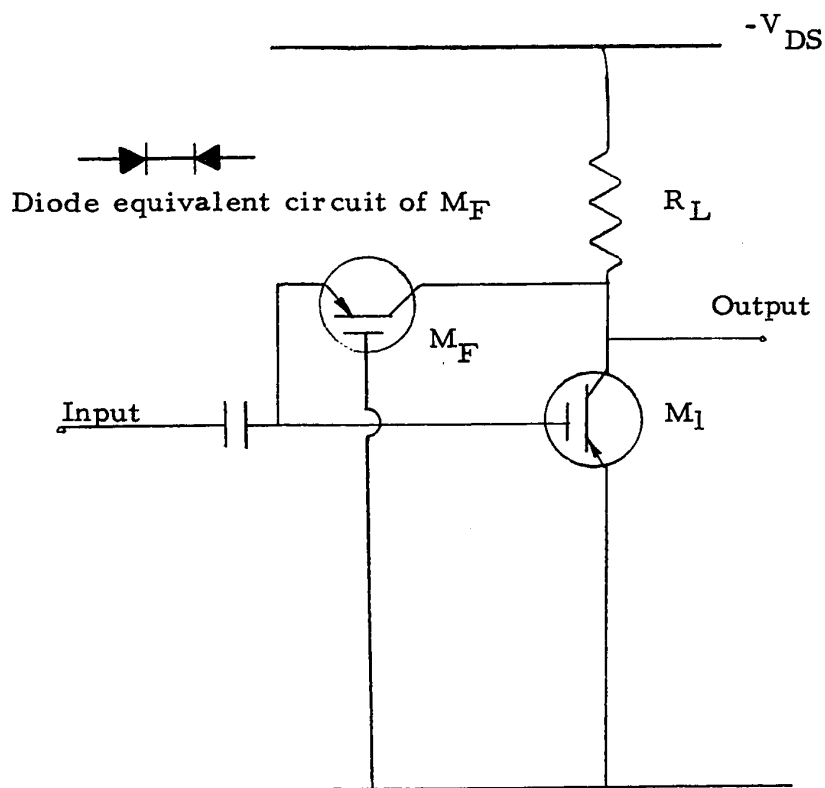


Fig. 22 Feedback circuit using type B resistor

be discussed first. The circuit, as shown, stabilizes the dc output voltage to the same value as the gate voltage at the chosen value of drain current.

$$V_{\text{out}} = V_T + \Delta V_T + i_F R_F$$

$$i_F = 0$$

$$V_{\text{out}} = V_T + \Delta V_T$$

Thus, variations in gate threshold voltage are reproduced without amplification at the output. Only one capacitor, a coupling capacitor, is used and its value is determined by the feedback resistor R_F and the ac gain. Since the current is of the order of 10^{-14} amperes, R_F can be many megohms, hence the coupling capacitor can be small.

$$C = (A + 1) / 2\pi R_F f$$

Several MOS realizations of the feedback resistor are possible:

- (a) An MOS resistor with a long narrow gate may be constructed. However, this presents several fabrication problems outside the scope of this thesis.
- (b) An MOS device, of conventional geometry operated with the gate at circuit ground, has a diode equivalent circuit shown in Fig. 22. This technique of realizing a high value resistance requires electrical isolation from the n-bulk of the amplifier. Air and dielectric insulation are satisfactory, but add steps to an otherwise simple manufacturing process.

(c) A solution which overcomes many of the disadvantages of (a) and (b) above is illustrated in Fig. 23. The feedback resistor is a conventional geometry MOS device with the gate and drain connected together (Table II type A) and constructed in the same bulk as the amplifier. There are two current paths connected to the gate of the amplifier, the leakage current of the source p-n junction to the bulk or circuit ground and the source to drain current of the feedback resistor. In normal operation, these two currents are equal and of the order of 10^{-9} amperes at room temperature. The feedback resistor is thus operated close to its threshold voltage, see Fig. 24. As the amplitude of the input signal of the amplifier is increased, the dc value of the output voltage changes to keep the average value of the two gate currents equal. This effectively holds the maximum negative excursion of the output voltage at the quiescent value of the dc output level. The transfer characteristic at two levels of input signal are shown in Fig.25. The effective value of the feedback resistor with $V_T = -5V$ and a junction leakage current of 10^{-9} amperes is of the order of 5×10^9 ohms. Thus, if the coupling capacitor is 20 pF and the gain 9, the low frequency cut-off is in the order of 20 Herz.

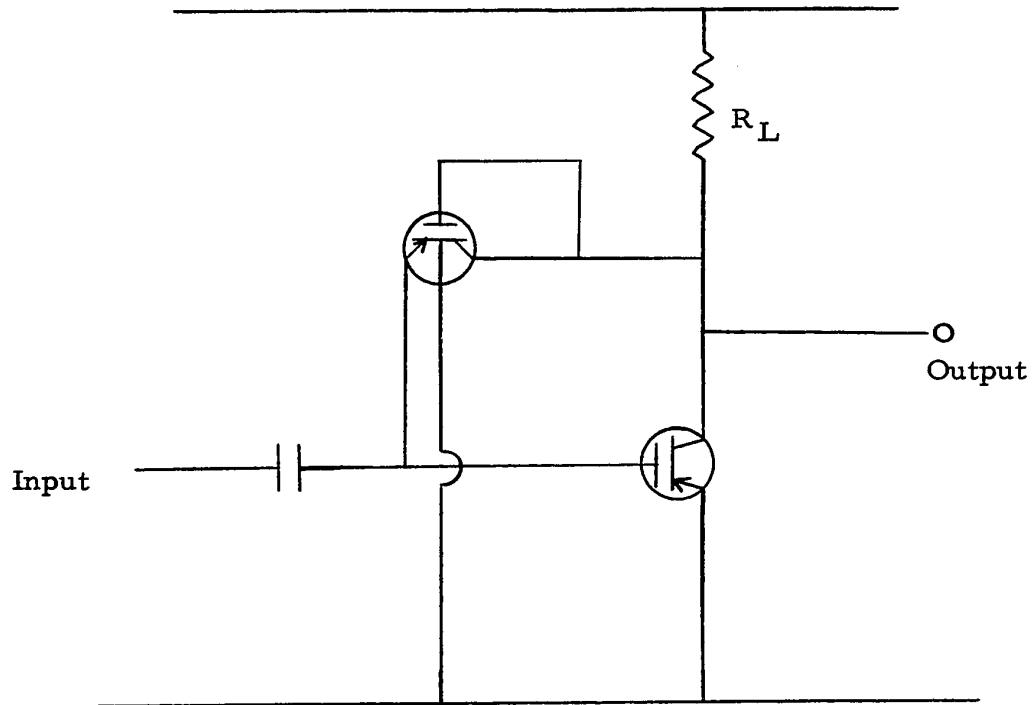


Fig. 23 Feedback circuit using type C resistor

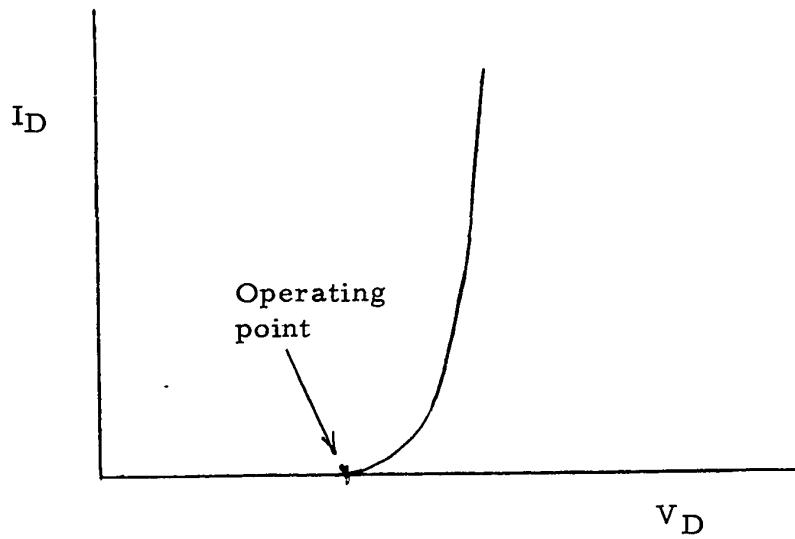


Fig. 24 Operating point of type C resistor

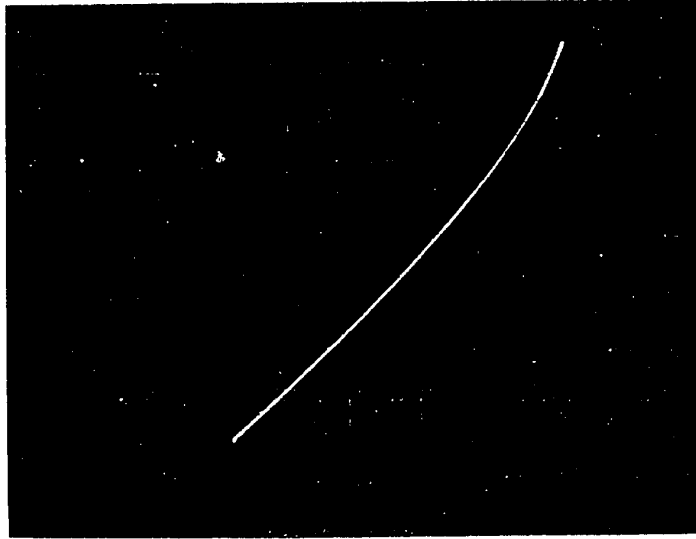


Fig. 25 Transfer characteristic of MOS amplifier
(Scale H - lv/cm V - lv/cm)

IV-4 A dc Feedback Stabilized MOS Linear Amplifier

The MOS device is a square law device, i. e. drain current is proportional to the effective gate voltage square. The transconductance g_m varies directly with the gate voltage $g_m = \mu_0 C_i V_g / 2l$. If a linear resistor is used as a load, distortion will arise. A solution is to use another MOS device as a load as shown in Fig. 26. The non-linearity of the transconductance will be compensated by the non-linearity of the MOS load in such a way as to maintain the voltage gain to a constant. The proof is as follows:

$$g_m = (2I_{ds}\mu_0 C_{oa} / l_a^2)^{1/2}$$

$$R_L = (l_L / 2I_{ds}\mu_0 C_{oL})^{1/2}$$

$$A = - g_m R_L \quad C_o = KE_{ox} l_w / t_{ox}$$

$$A = - (l_L w_a E_{oxa} t_{oxL} / l_a w_L E_{oxL} t_{oxa})^{1/2}$$

If M_1 and M_2 were made identical except for the width, then

$$A = - (w_a / w_L)^{1/2}$$

Gate voltage is the parameter most likely to change due to the drift of threshold voltage and the reasons why the threshold voltage drifts have been discussed. As can be seen from the equation above, the voltage gain is independent of the gate voltage V_g . An amplifier can be designed with stable voltage gain that depends only upon the geometry of the devices used. The gain is proportional to the square root of the channel

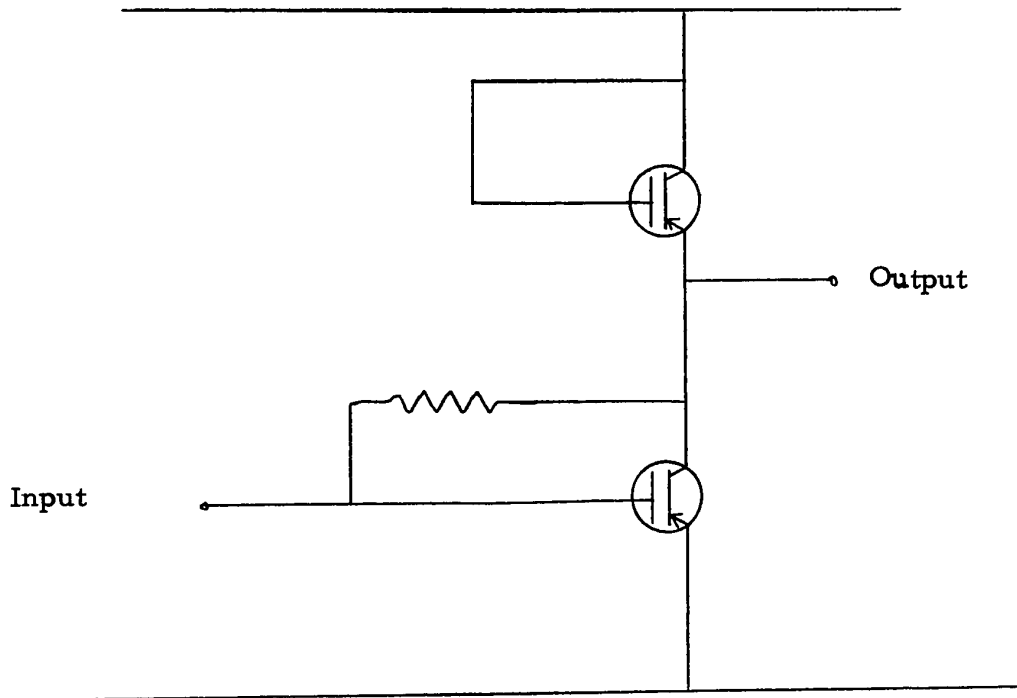


Fig. 26 A dc feedback stabilized MOS linear amplifier

widths ratio of the active device and load provided other parameters are identical. If the channel widths are equal, the circuit becomes a linear inverter with a gain of one. A feedback resistor from the load to the gate will accomplish the dc biasing. Since all the components of the amplifier can be made by MOS techniques, manufacturing can be relatively simple.

IV-5 Multiple Stage Amplifiers

As stated above, dc output voltage stabilization may be applied to multiple stage inverting amplifiers, such as the three stage amplifier of Fig. 27. However, the increased gain demands the use of a larger coupling capacitor e. g. in a typical amplifier, each stage may have a gain of 10, resulting in the coupling capacitor of approximately 100 times the capacitance of that required for a single stage, thus using 100 times the area. Since the physical dimensions of the feedback resistor can be small, an integrated MOS amplifier, dc stabilized stage by stage as shown in Fig. 28, is more economical of area than one stabilized over several stages at a time. Furthermore, the parasitic shunt capacitance of an MOS feedback resistor limits the overall gain, in addition to causing ac stability problems.

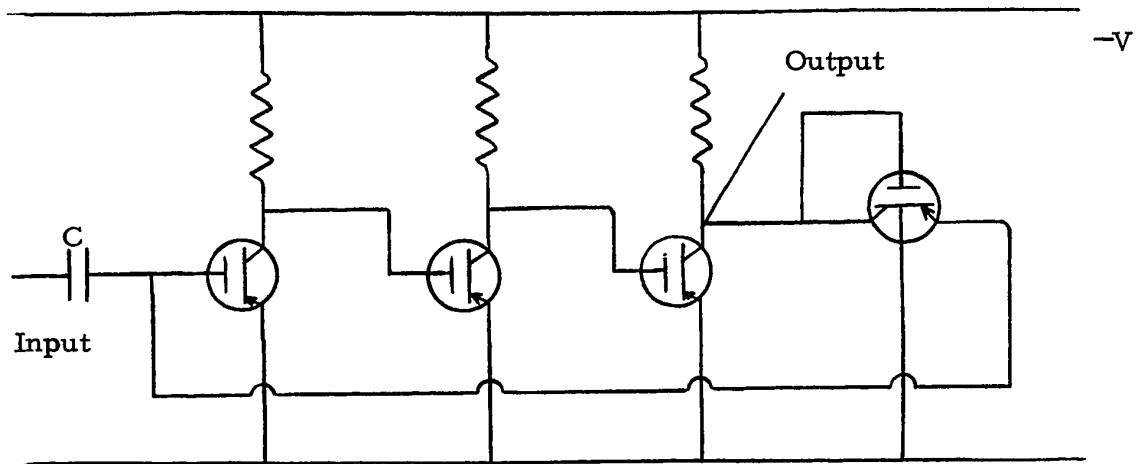


Fig. 27 Multiple stage MOS amplifier using only one feedback resistor for dc stabilization

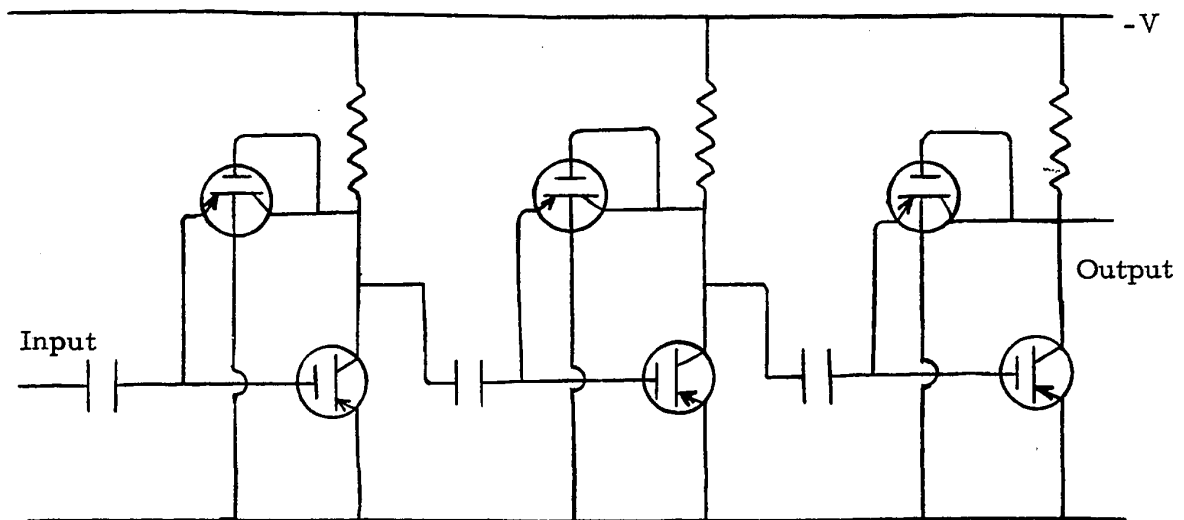


Fig. 28 Multiple stage MOS amplifier using dc feedback stabilization stage by stage

V Pair Circuits

Amplifiers can be made from cascade connections of the single stages discussed previously. However, a coupling capacitor is needed between each stage. The stray capacitance introduced by the integrated realization of the coupling capacitor, as shown in Fig. 29, will severely limit the bandwidth. With a single stage gain of around 10, this results in a small gain-bandwidth product. In order to improve the gain-bandwidth product, two stages per coupling capacitor must be considered. Two stages of MOS device will have a possible gain of a 100 which may be traded in favor of bandwidth. Thus it is worthwhile to explore the possibilities of pair circuits.

All possible combinations of basic amplifier configurations, i. e. , common gate, common drain and common source, can be examined as a three dimensional matrix form, shown in Fig. 30 (a). The first device is represented in columns and second device in rows. The third dimension is in terms of cascade, series and parallel.

The three dimensional matrix simplifies into the two dimensional cascade matrix, since the matrices for series and parallel connections consist only of two basic pairs as shown in Figs. 30 (b) and (c). These connections increase the I_D (maximum) and V_{DS} (maximum)

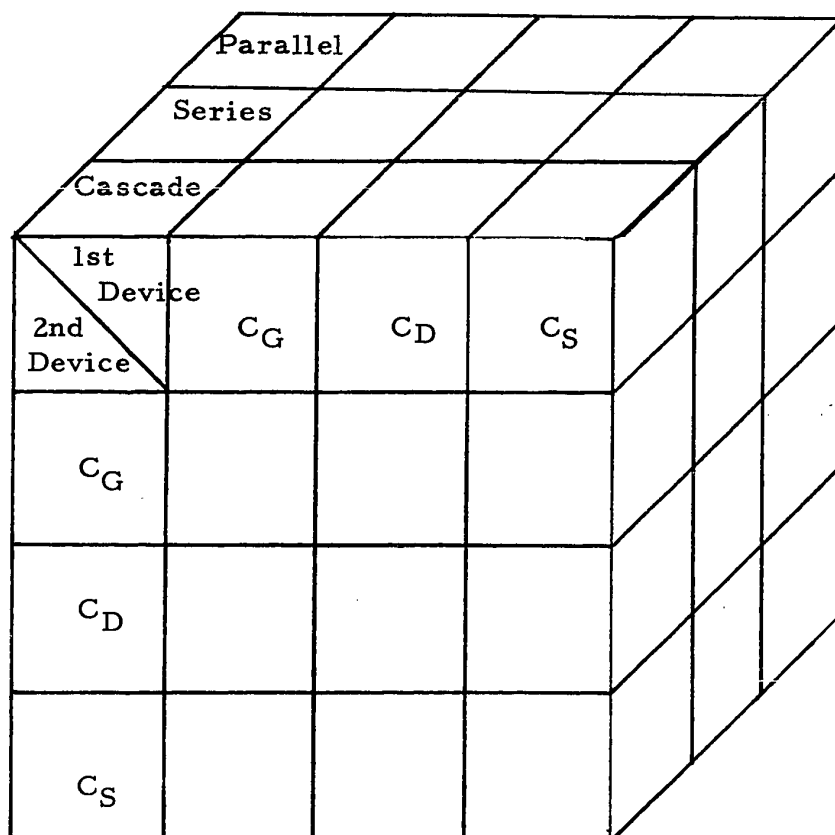


Fig. 30 (a) Matrix showing all possible combination of two MOS devices

Series

1st Device 2nd Device	C_G	C_D	C_S
C_G			
C_D			
C_S			

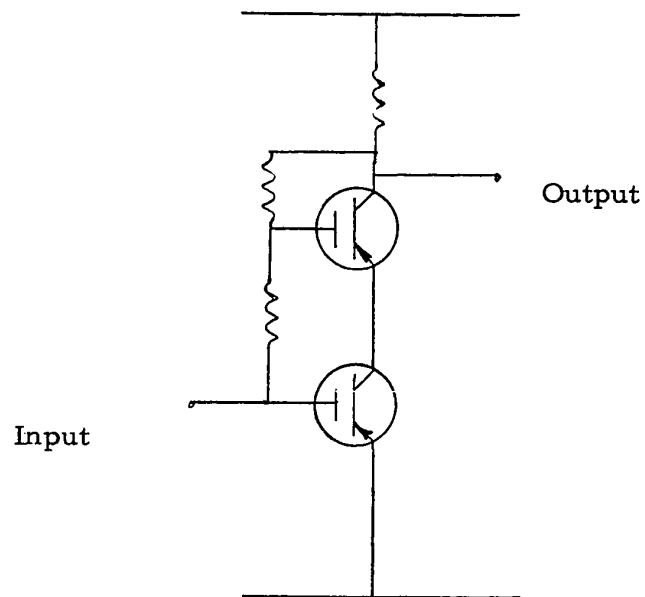


Fig. 30 (b)

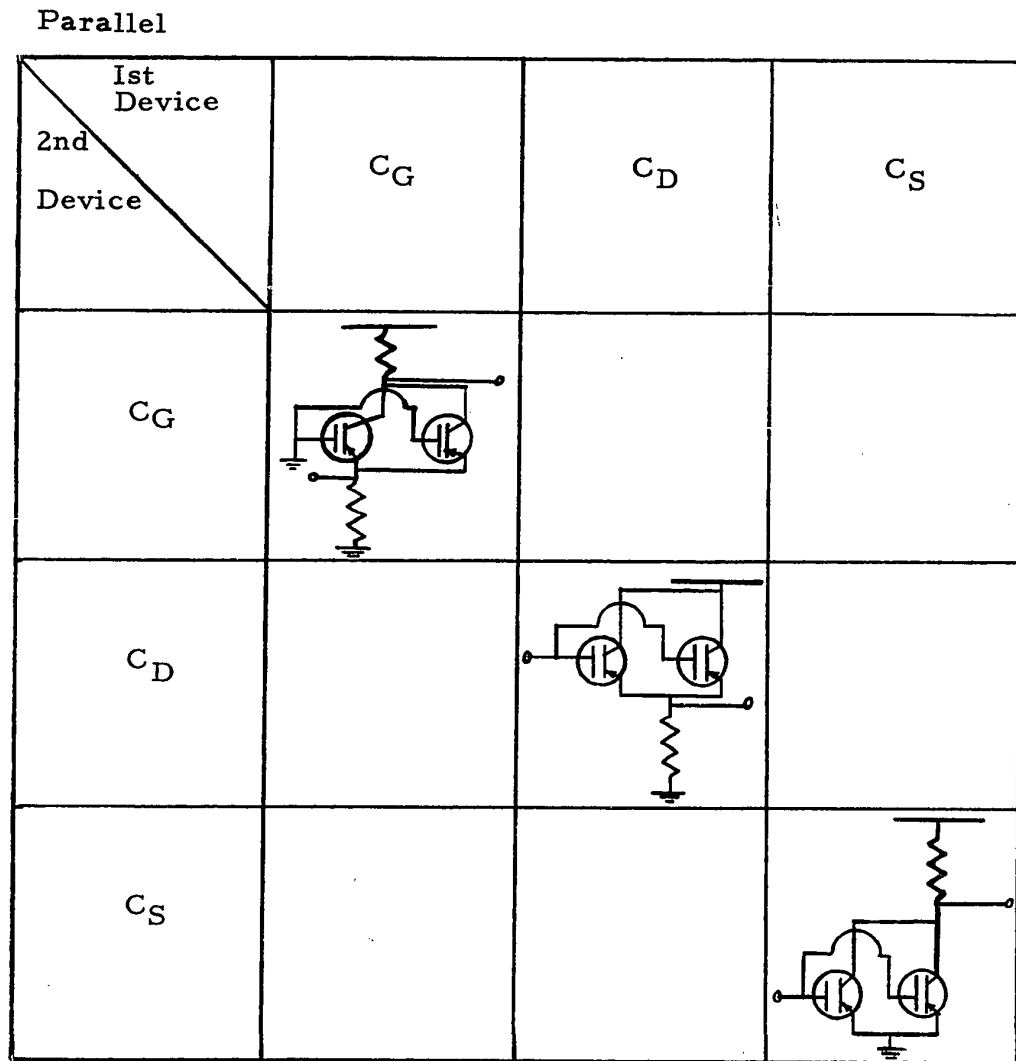


Fig. 30 (c)

handling capacity of the devices, respectively. In integrated circuits, this is equivalent to increasing the channel width or length. Thus, these connections are trivial and will not be considered further. Strickly speaking, the series and parallel pairs are only a subcase of the cascade connections.

The cascade matrix, shown in Fig. 31, will now be considered case by case:

- (11) Common gate followed by common gate circuit - A slight manipulation of this circuit shows that it is equivalent to two MOS devices in series and thus, is trivial.
- (12) Common drain driving a common gate circuit - This can be recognized as a conventional differential pair shown in Fig. 32.

If the parameters of the two MOS devices are alike and if the external gate circuits are also alike, there will be perfect symmetry and balance. Then, so far as dc is concerned, the common source resistance R_S can be replaced by a resistance of $2R_S$ in series with each source. This gives a stability factor close to unity, for each side, provided R_S is sufficiently large. Similar changes in Q_1 and Q_2 will balance in any output taken between the two drains.

Although some degree of balance might be expected from devices fabricated on the same chip, it is preferable to establish the dc operating point of each half of the differential pair separately.

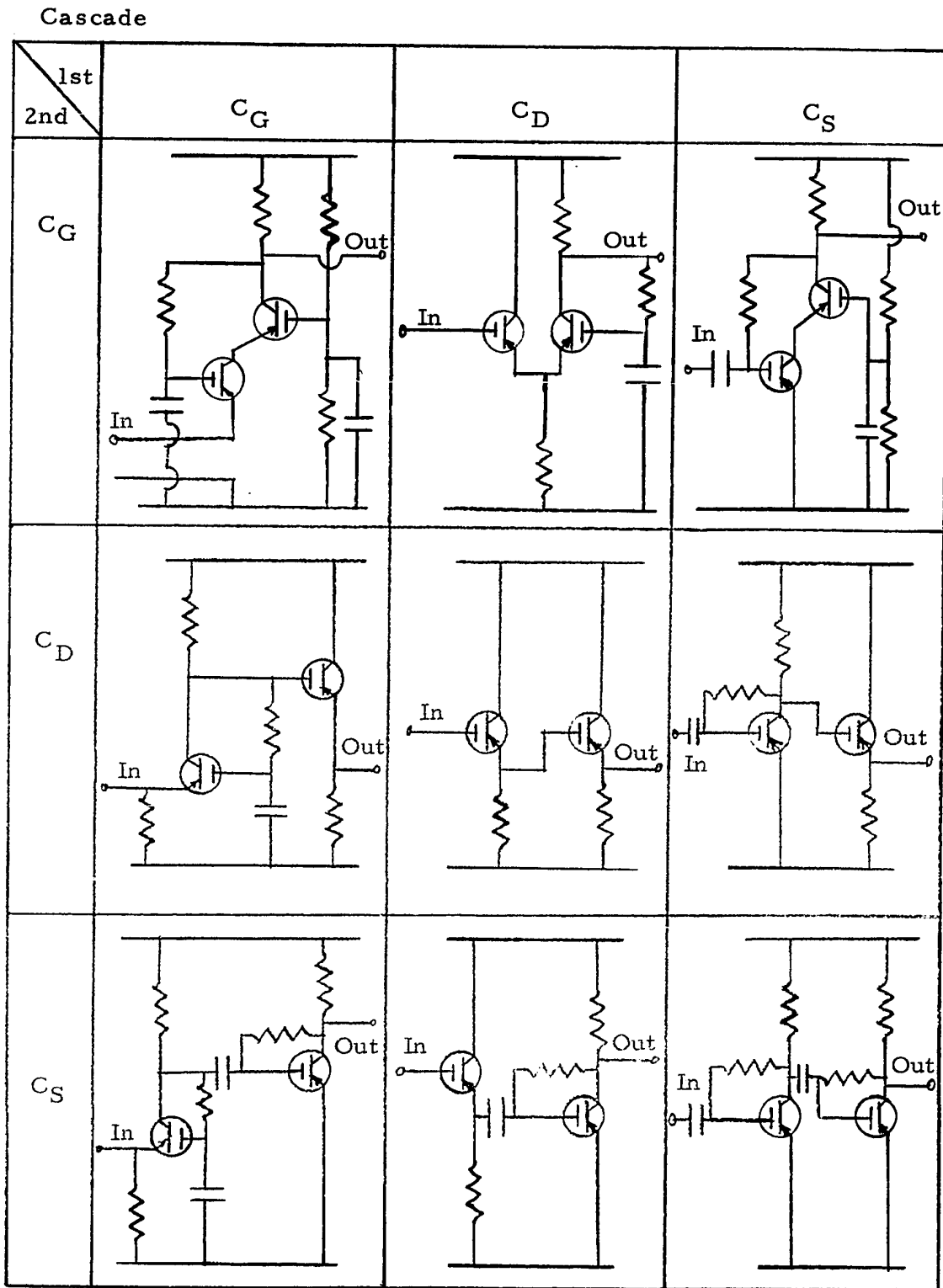


Fig. 31 Pair circuits with biasing

Typical circuits are shown in Fig. 33 (a) and (b). In circuit (a) R establishes the current for the sources of Q_1 and Q_2 , and the circuit operation is similar to any conventional differential amplifier. A third MOS device in type B or C connections (see Table II) can serve as a current source instead of a resistance and this will improve the common mode rejection.

These differential amplifier configurations are compatible with single diffused fabrication techniques. Few, if any, capacitors are needed, the key to economy in integrated fabrication. Furthermore, the primary parameters of the differential amplifiers are functions of ratios between device parameters, eliminating the need for close tolerances in individual components.

(13) Common source driving a common gate circuit - This can be recognized as a conventional "cascode" amplifier as shown in Fig. 34. The transconductance of the pair is determined by the transconductance of the driving unit providing that the driven unit does not limit the overall current. The "cascode" amplifier may be used to improve the signal to noise ratio and reduce the feedback capacitance of an amplifier stage.

The input impedance of the pair is determined by the input device and the output impedance by the driven unit. If the conductivity of the driven unit is kept above that of the driving unit, so that no current limiting occurs, the output impedance of the pair will

always be equal to, or greater than, the normal output impedance of the driven unit operating alone. If, alternatively, the driven unit begins to limit, the output impedance of the pair may be increased by several orders of magnitude. This limiting results from the degenerative action of the input device when the pair is operated in series.

The possibility of tailoring the transfer characteristic of the "cascode" pair, by biasing the gate of the driven unit, is perhaps the most significant feature of this circuit configuration. Excessive limiting by the driven unit drastically reduces the dynamic range of the cascode drain current - gate voltage transfer characteristic. Alternatively, by careful selection of the gate bias of the driven unit, the high current end of the cascode transfer characteristic can be varied over a wide range. In addition, improved signal to noise ratio and reduced feedback capacitance are advantages.

(21) Common gate driving a common drain - This is a useful amplifying pair because:

- (a) The gain of the circuit depends on the values of passive components rather than the device itself.
- (b) The output impedance is low.
- (c) The feedback capacitance C_{ds} is small.

(22) Common drain driving a common drain - This circuit exhibits high input impedance and low output impedance and is essentially an impedance converter, with no voltage gain and a high current gain. The input capacitance can be decreased by using a smaller channel

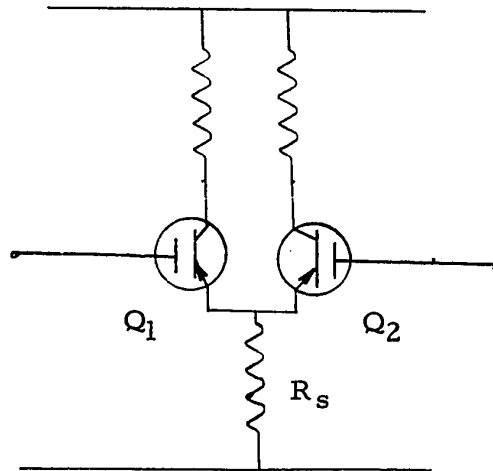


Fig. 32 MOS differential pair

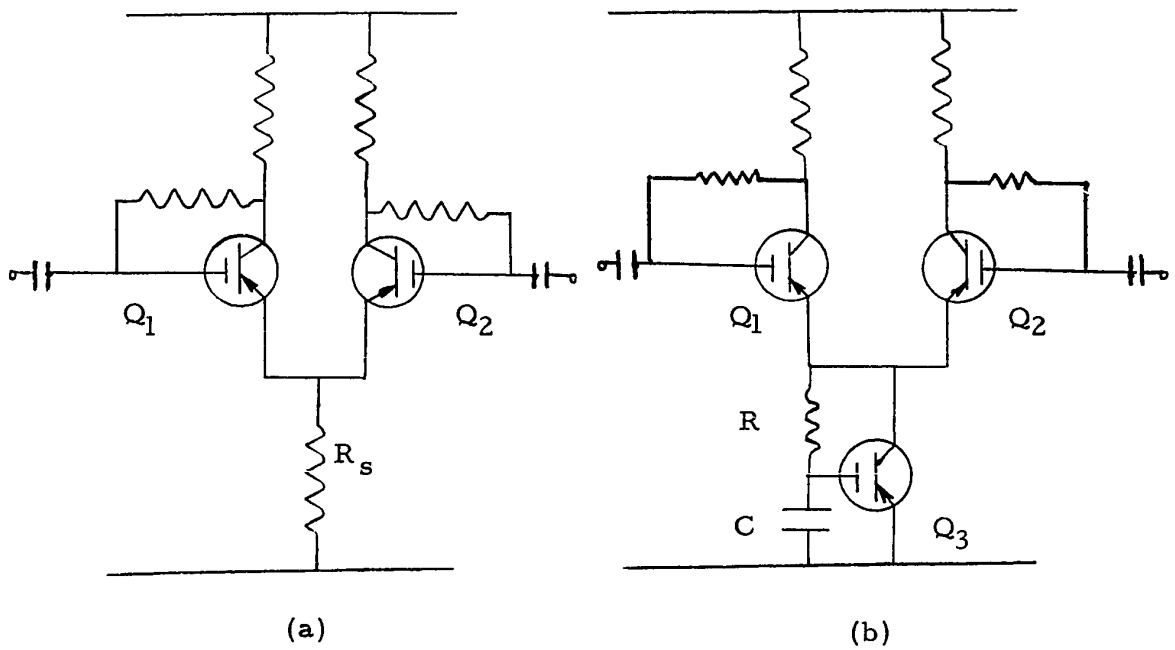
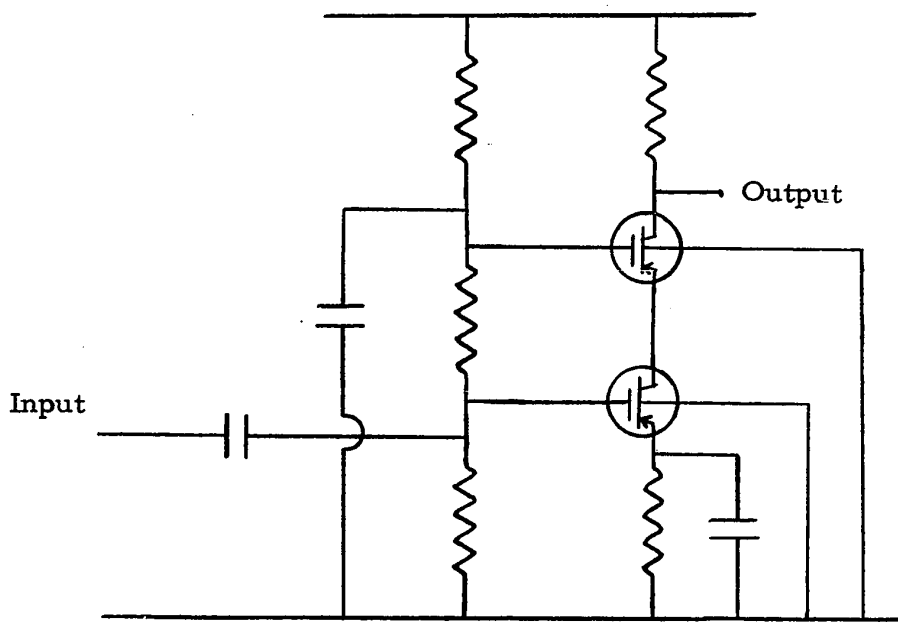
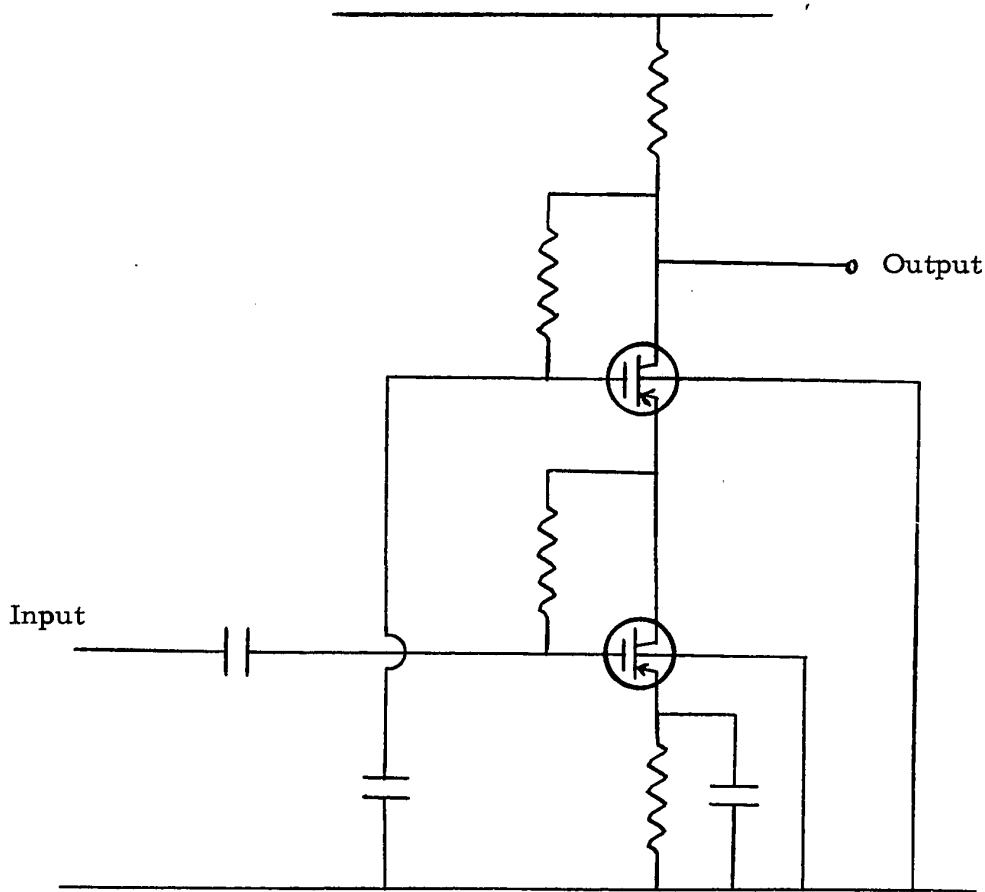


Fig. 33 MOS differential pair using another MOS device as current source



(a)



(b)

Fig. 34 MOS cascode circuits

width for the first device than for the second. The primary application for this circuit is where high output current is required.

(23) Common source driving a common drain - This circuit has voltage gain in the first stage and current gain in the second. It is similar to the circuit of (21) and differs only in the input connection. Circuit (23) is an inverting amplifier while circuit (21) is non-inverting. Also in circuit (23) the coupling capacitor becomes a decoupling capacitor and there is no large shunt capacitance at the input. A practical circuit using circuit (23) and (21) is shown in Fig. 35.

(31) Common gate driving a common source - The most important feature of this circuit is its low feedback admittance. It has voltage gain in both stages but there is only one phase inversion. Since gain in the second stage requires a high output impedance, it is preferable to follow this pair with a common drain stage to reduce the output resistance and increase the bandwidth.

(32) Common drain driving a common source - The low output impedance of the first stage can be used to drive a large gate MOS device in the common source configuration without sacrificing bandwidth. It exhibits a high input impedance and a moderately high output impedance. There is one phase inversion and feedback from output to input can be used.

(33) Common source driving a common source - This connection is merely a cascade of two common source stages, see section IV-5.

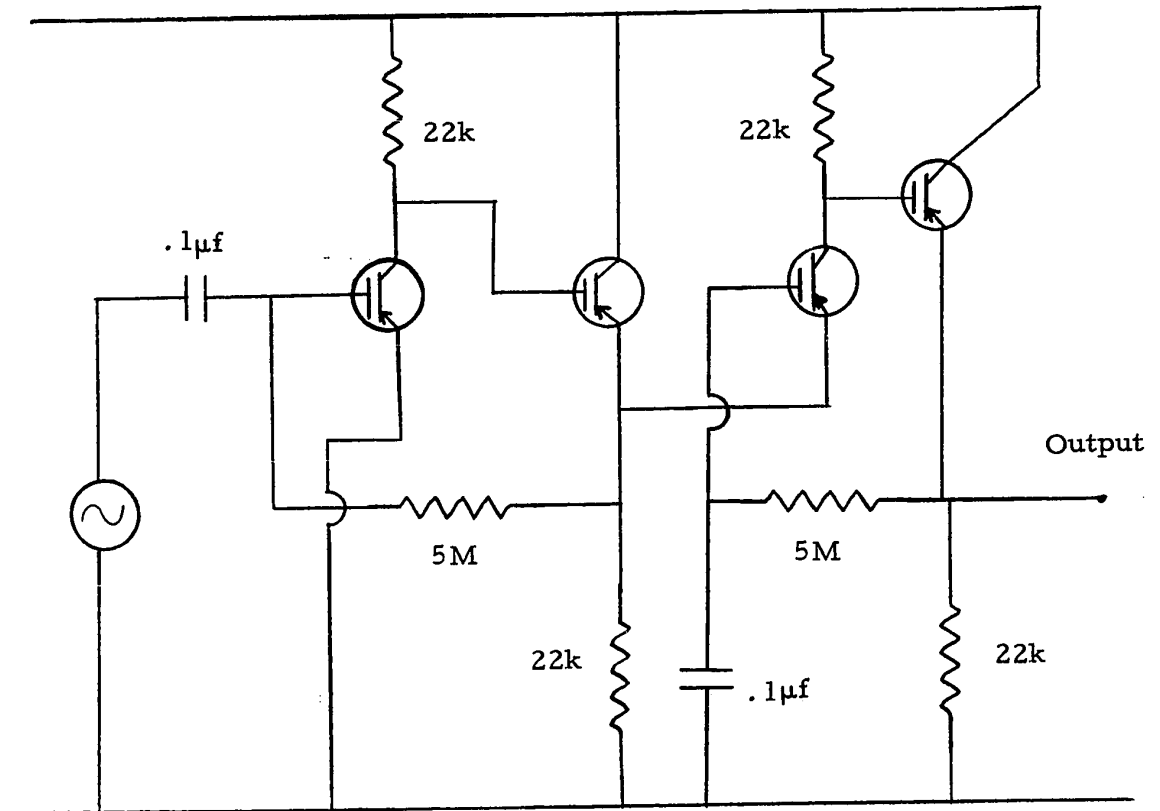


Fig. 35 Practical circuit using (23) and (21)

The gain, inverse admittance^{and} input-output impedance have been tabulated in Table III.

1st Device	2nd Device	C_G	C_D	C_S
		$B_{GG} = \frac{R_{s2} R_{L1}}{R_{L2} R_{L1}}$ $A_T = \frac{(1+g_m r_d) R_{L1}}{R_1 (1+g_m r_d) + r_d + R_{L2}}$ $Z_{in} = R_{s1} \parallel \frac{R_{L1} Z_{in C} + r_d}{1 + g_m r_d}$ $Z_{out} = [(g_m r_d + 1) R_{s2} + r_d] \parallel R_{L2}$	$B_{DG} = \frac{1}{r_d g_m} - \frac{r_d X}{R_{s1} r_d} \frac{r_d + X}{g_m r_d} \frac{r_d + X}{g_c} R_s$ $A_T = \frac{g_m R_{s2}}{1 + g_m R_{s2} (1 + g_m r_d) R_{L1} + r_d + R_{L2}}$ $Z_{in} = (1 + g_m R_{s2}) \parallel Z_{C} \parallel X_{C_{in}} \parallel g_c$ $Z_{out} = [(g_m r_d + 1) R_{s2} + r_d] \parallel R_{L2}$	$B_{GG} = \frac{R_{s2}}{(j\omega C_{gd} R_{L1} - g_m) R_{L2}}$ $A_T = \frac{-g_m r_d R_{L1} (1 + g_m r_d) R_{L2}}{r_d + R_{L1} R_1 (1 + g_m r_d) + r_d + R_{L2}}$ $Z_{in} = r_{gs}$ $Z_{out} = [(g_m r_d + 1) R_{s2} \parallel R_{L1}] \parallel R_{L2}$
		$B_{GD} = \frac{R_{s1} R_{L1}}{R_{L2} R_{L1}} \frac{r_d + X}{r_d} \frac{r_d + X}{g_c}$ $A_T = \frac{g_m R_{s1}}{1 + g_m R_{s1} (1 + g_m r_d) R_{L1} + r_d + R_{L2}}$ $Z_{in} = (1 + g_m R_{s1}) X_{C} \parallel g_c$ $Z_{out} = \frac{r_d R_{s2}}{(g_m r_d + 1) R_{s2} + r_d}$	$B_{DS} = \frac{1}{r_d g_m} - \frac{r_d X}{R_{s1} r_d} \frac{r_d + X}{g_m r_d} \frac{r_d + X}{g_c}$ $A_T = \frac{g_m R_{s1}}{1 + g_m R_{s1} (1 + g_m r_d) R_{L1} + r_d + R_{L2}}$ $Z_{in} = (1 + g_m R_{s1}) X_{C} \parallel g_c$ $Z_{out} = \frac{r_d R_{s2}}{(g_m r_d + 1) R_{s2} + r_d}$	$B_{SD} = \frac{1}{r_d g_m} - \frac{r_d X}{R_{s2} r_d} \frac{r_d + X}{g_m r_d} \frac{r_d + X}{g_c}$ $A_T = \frac{-g_m r_d R_{L1}}{r_d + R_{L1} R_1 (1 + g_m r_d) + r_d + R_{L2}}$ $Z_{in} = r_{gs}$ $Z_{out} = \frac{r_d R_{s2}}{(g_m r_d + 1) R_{s2} + r_d}$

1st Device 2nd Device	C_G	C_D	C_S
C_X	$B_{GS} = \frac{R_{s1}}{R_{L1} (j\omega C_{gd} R_{L2} - g_m)}$ $A_T = - \frac{(1+g_m r_d) R_{L1}}{R_1 (1+g_m r_d) + r_d R_{L2}} \cdot \frac{g_m r_d R_{L2}}{r_d + R_{L2}}$ $Z_{in} = R_{s1} \parallel \frac{R_L + r_d}{1+g_m r_d}$ $Z_{out} = \frac{r_d R_L}{r_d + R_L}$	$B_{DS} = \frac{1}{r_d g_m - R_{s1}} \cdot \frac{\frac{r_d X_{gd}}{r_d + X_{gd}} [g_m + \frac{r_d + X_{gd}}{r_d - X_{gd}}]}{X_{gd} [r_d g_m (1 - \frac{X_{gd}}{r_d + X_{gd}}) (j\omega C_{gd} R_{L2} - g_m)]}$ $A_T = \frac{g_m R_s}{1+g_m R_s} \cdot \frac{g_m r_d R_L}{r_d + R_L}$ $Z_{in} = (1+g_m R_s) X_{cgc}$ $Z_{out} = \frac{r_d R_L}{r_d + R_L}$	$B_{SS} = \frac{1}{(j\omega C_{gd} R_{L2} - g_m) (j\omega C_{gd} R_{L1} - g_m)}$ $A_T = \left(\frac{g_m r_d R_{L1}}{r_d + R_{L1}} \right) \left(\frac{g_m r_d R_{L2}}{r_d + R_{L2}} \right)$ $Z_{in} = r_{gs}$ $Z_{out} = \frac{r_d R_{L2}}{r_d + R_{L2}}$

TABLE III (a) Pair Circuits.

VI Typical Application

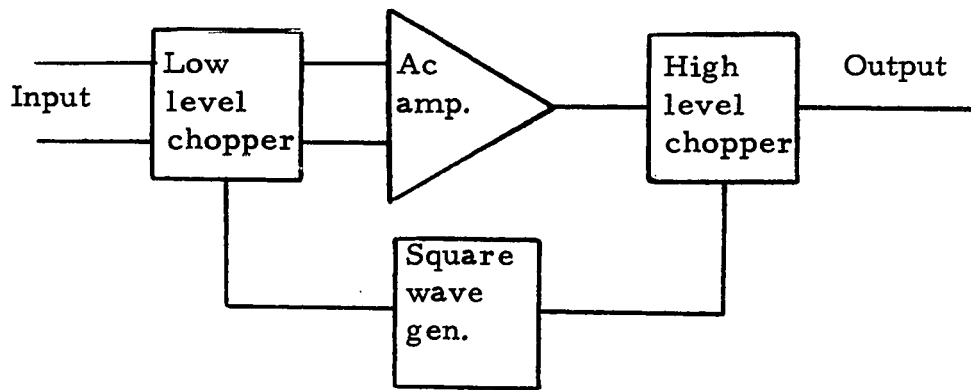
As an example of the above design techniques, a dc amplifier for biological applications is designed in this chapter. This example is chosen because the variable impedance of biological systems requires high input impedances for voltage measurements and because MOS devices, by their nature, have high input impedances.

VI-1 System Design

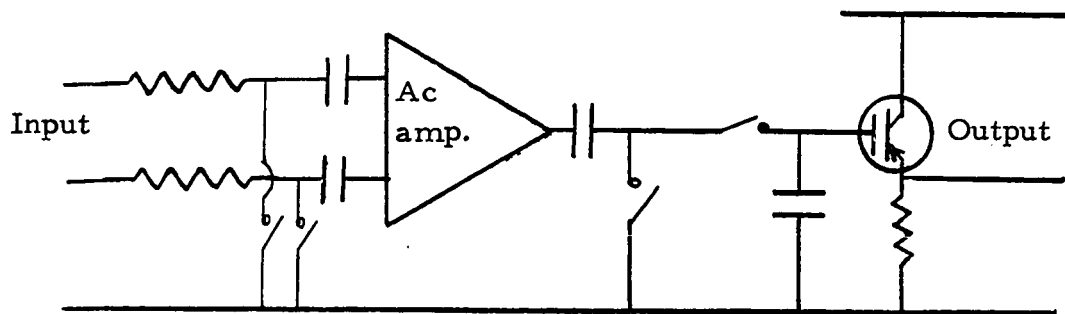
Dc Amplifier Specification:

- (a) Input- ≈ 10 microvolts
(source impedance for biological applications is variable over a wide range)
- (b) Output- ≈ 1 volt
(output impedance less than 1 k)

A schematic block diagram of a chopper type dc amplifier is shown in Fig. 36. The small dc signal is first converted to ac by means of a chopper circuit. After amplification the dc is restored by higher level choppers. Both choppers can be driven by a reference signal (in this case, a square wave generator).



(a)



(b)

Fig. 36 Block diagram of chopper type dc amplifier

The design of the dc amplifier will be discussed below, but since the purpose of this chapter is to demonstrate the design techniques developed above, the design of the ac amplifier will be treated in detail, while the ancillary circuits, such as the choppers and square wave generator will be discussed only briefly.

VI-2 Ancillary Circuits

Low level chopper - The type of low level chopper adopted in this application is the dual collector transistor²³. There is little coupling between the switching signal applied to the emitter and the small signal circuit. In addition, it is suitable for high input impedance applications and has a low differential off-set voltage.

High level chopper - A high level chopper is needed to restore the dc and this can be done by two MOS high level switches as shown in Fig. 37. The capacitor C_2 is provided to smooth the output and if the bandwidth of the overall system is to be maintained, capacitor C_1 must be much larger than C_2 .

Square wave generator - The choppers are driven by an MOS multivibrator and buffer amplifier.

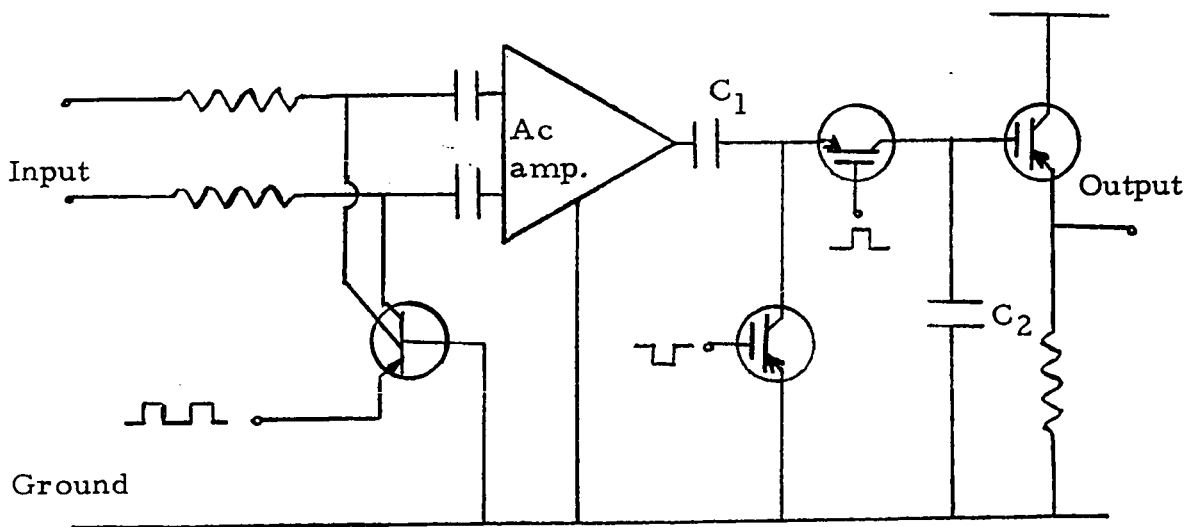


Fig. 37 Chopper type ac amplifier using dual collector transistor as low level chopper and MOS series-shunt chopper as higher level chopper.

VI-3 Ac Amplifier

In this section a design procedure, which uses the above techniques, is applied to the ac amplifier. First, the system for the ac amplifier is designed, followed by the detailed design of a single stage.

From section VI-2 the specification for the ac amplifier is as follows:

Ac Amplifier Specifications:

- (a) Input- $\approx 10 \mu V$ p. p.
(The amplifier must have adequate common mode rejection for the chopper circuit employed)
- (b) Output- $\approx 1 V$
(Suitable impedance to drive the high level chopper)
- (c) Bandwidth- Sufficient to maintain the edges of chopped signal.
- (d) Gain- 10^5 .

From the above it is clear that at least five stages of amplifications are required, because it is difficult to obtain a single stage voltage gain greater than 10, as demonstrated in section IV-4. Since the chopper requires common mode rejection, a differential amplifier is used for the first stage, see Fig. 32. The common mode rejection may be further improved by an additional stage of differential amplification. This is followed by at least three stages of single ended

amplification. An extra stage, without voltage gain, may be required to match the output of the ac amplifier to the high level chopper. A block diagram of the system is shown in Fig. 38. Now, the design of the single stage amplifier will be considered in detail. For simplicity, a single ended amplifier will be discussed, we will consider the case where the three stages are similar. It is now possible to write the specification for one of these stages.

Single Stage Specification:

- (a) Input- Dynamic range from μ l milivolt to μ l volt.
(Suitable to be driven by a source similar to its own output)
- (b) Output- Adequate to drive a load similar to its own input.
- (c) Bandwidth- Large enough to preserve the edges of the chopped signal.
- (d) Gain- 10.

We now examine Table I of single stage amplifier configurations.

The common source configuration meets input impedance and voltage gain requirement, but it may, in monolithic form, lack the bandwidth requirement. Thus, we must consider the pair circuits of Table III and we find that the following meet the specifications:

- (1) Common drain driving a common gate (differential pair)
- (2) Common gate driving a common drain

- (3) Common source driving a common drain
- (4) Common drain driving a common source

From Fig. 39, we see that (1) is similar to (2) and (3) is similar to (4) in a cascaded circuit depending on which pair is examined. Thus, these four circuits can be reduced into two types only. Here we note that both (2) and (3) do not require a matching stage at the output, because the common drain already has an adequately low output impedance to match the high level chopper.

It seems that both circuits meet the specifications. However, analysis of the dc levels and number of threshold voltage drops in each circuit with feedback biasing reveals that direct coupling of similar circuits will result in a progressive decrease in the dc level of successive stages shown in Fig. 40 and 41 and a solution is to combine the two types of circuits with a coupling capacitor as shown in Fig. 42.

We now consider in detail one of the stages, shown in Fig. 43. For dc stabilization, a feedback resistor is used from drain to gate. The all MOS circuit is shown in Fig. 44. The bold lines represent the metal on the surface and the thin lines p regions. R_1 and R_2 are large value resistances and type B of Table II is suitable. The feedback resistor must be of extremely large value and this is realized by a type A of Table II operating in the region shown in Fig. 45. As demonstrated

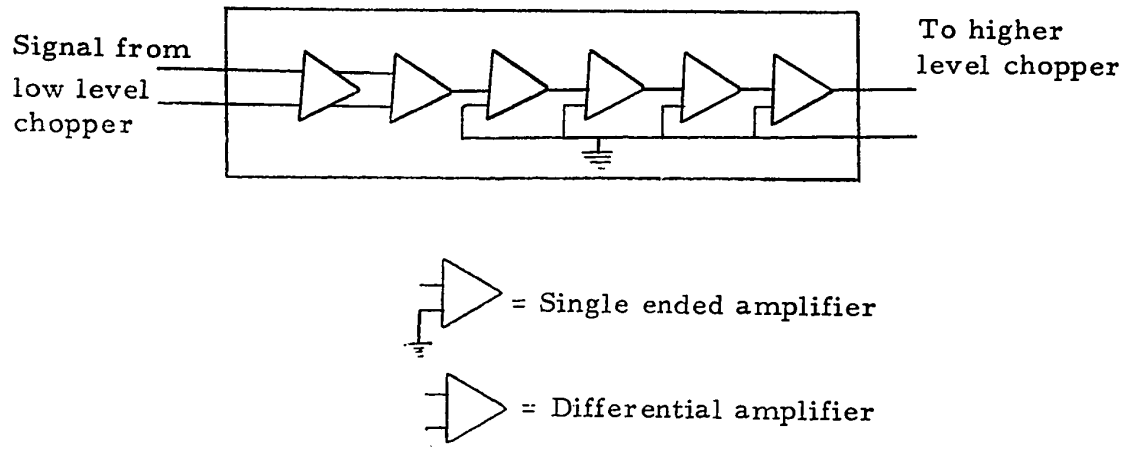


Fig. 38 Block diagram of ac amplifier

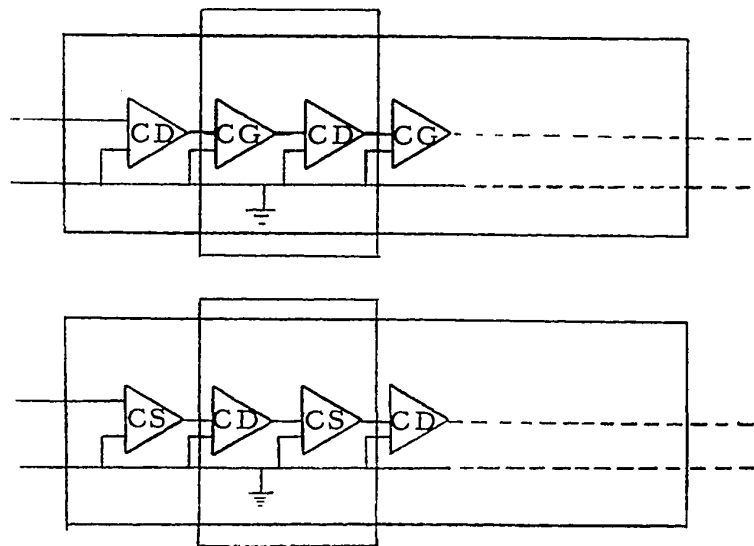


Fig. 39 Cascading of pair circuits

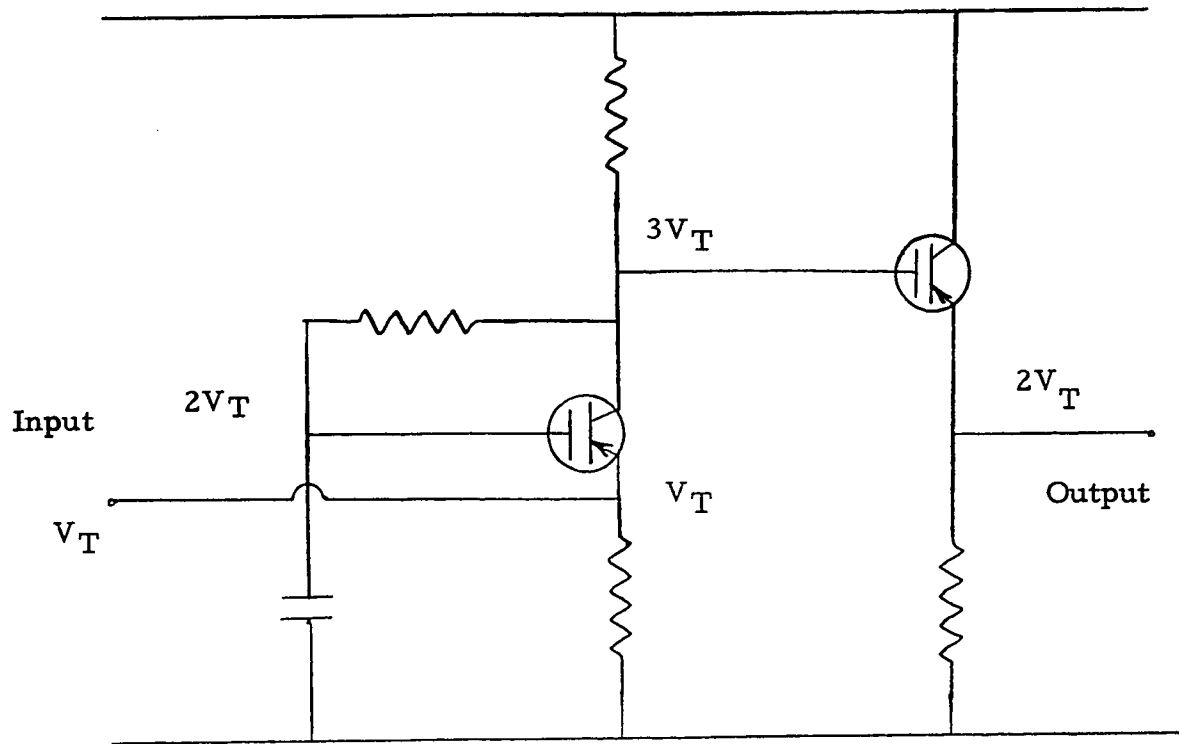


Fig. 40 Dc level of circuit (2)

(Note negative shift of dc level between input and output)

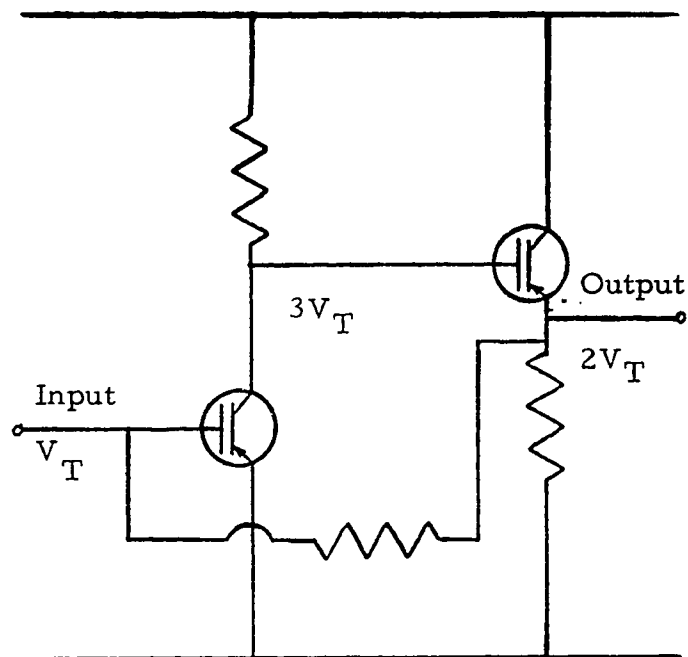


Fig. 41 Dc level of circuit (3)

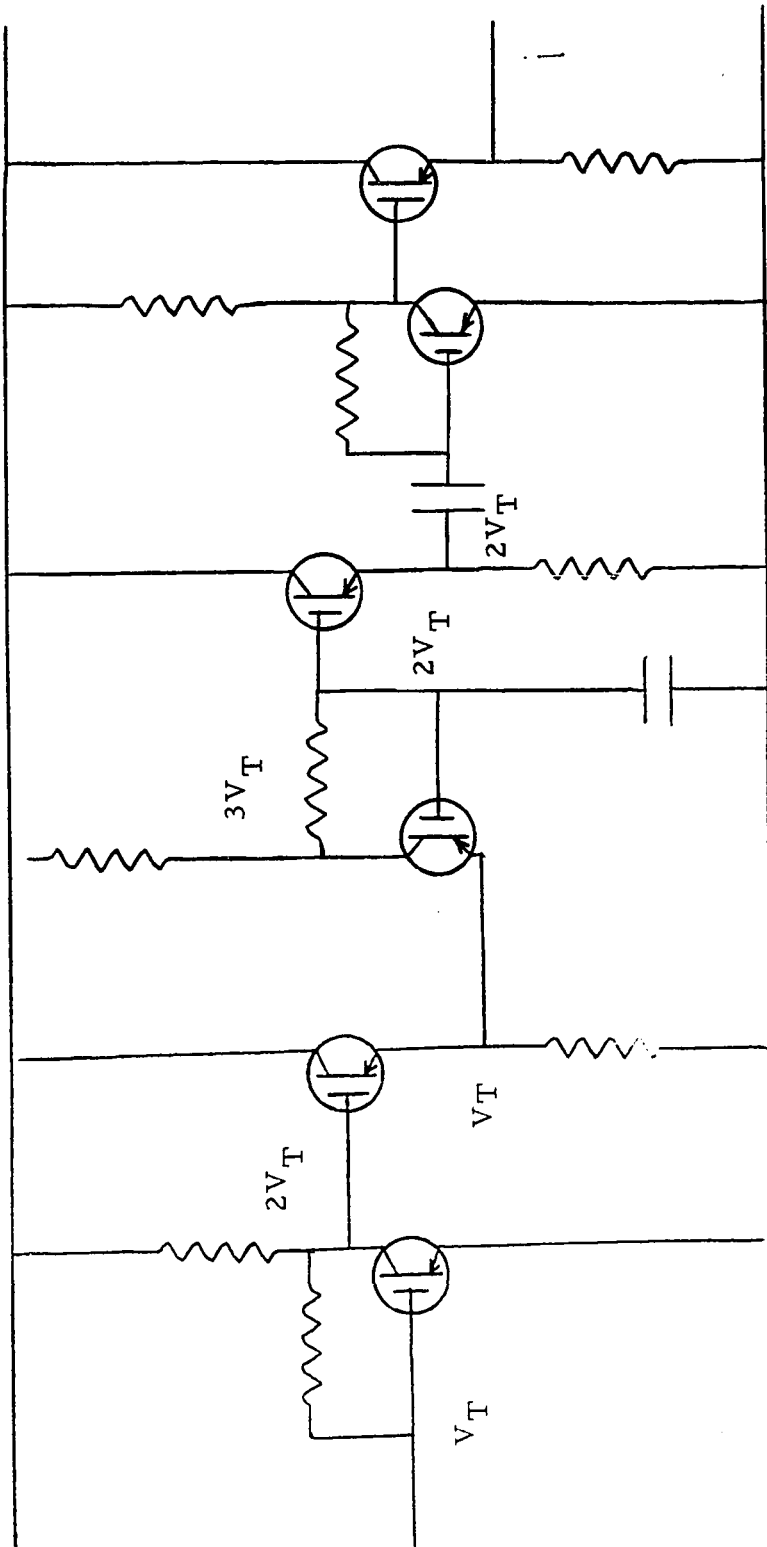


Fig. 42 Cascading of (2) and (3)

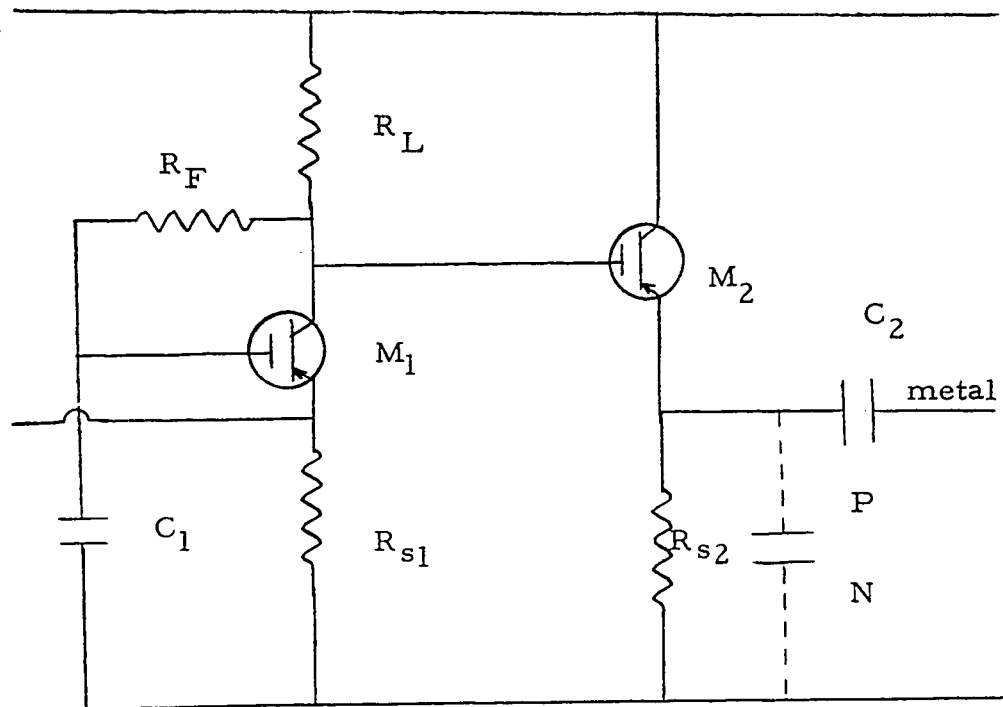


Fig.43 Circuit (2) showing the stray capacitance introduced by C_2

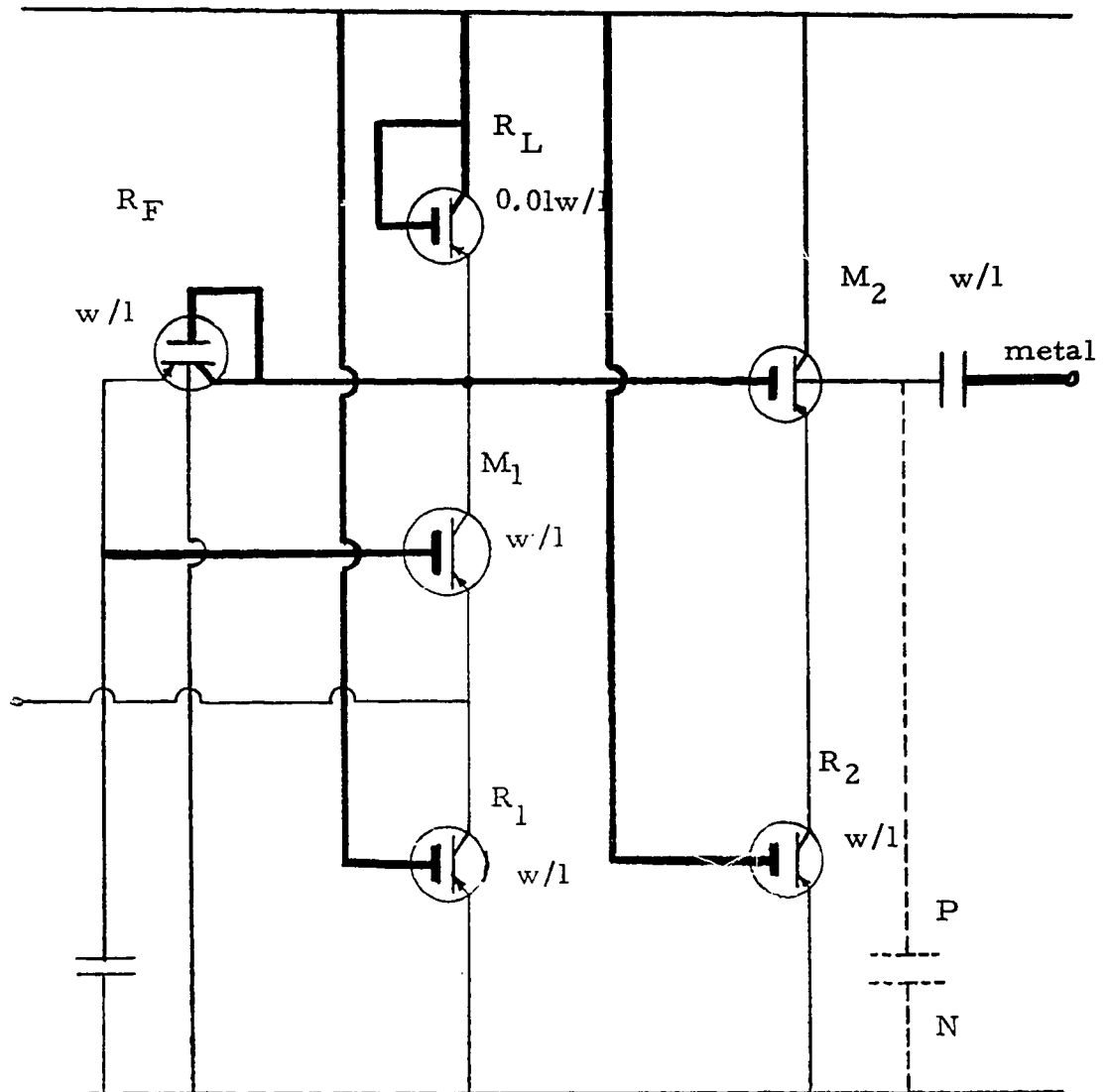


Fig. 44 All MOS amplifier circuit with bold line representing the metalization

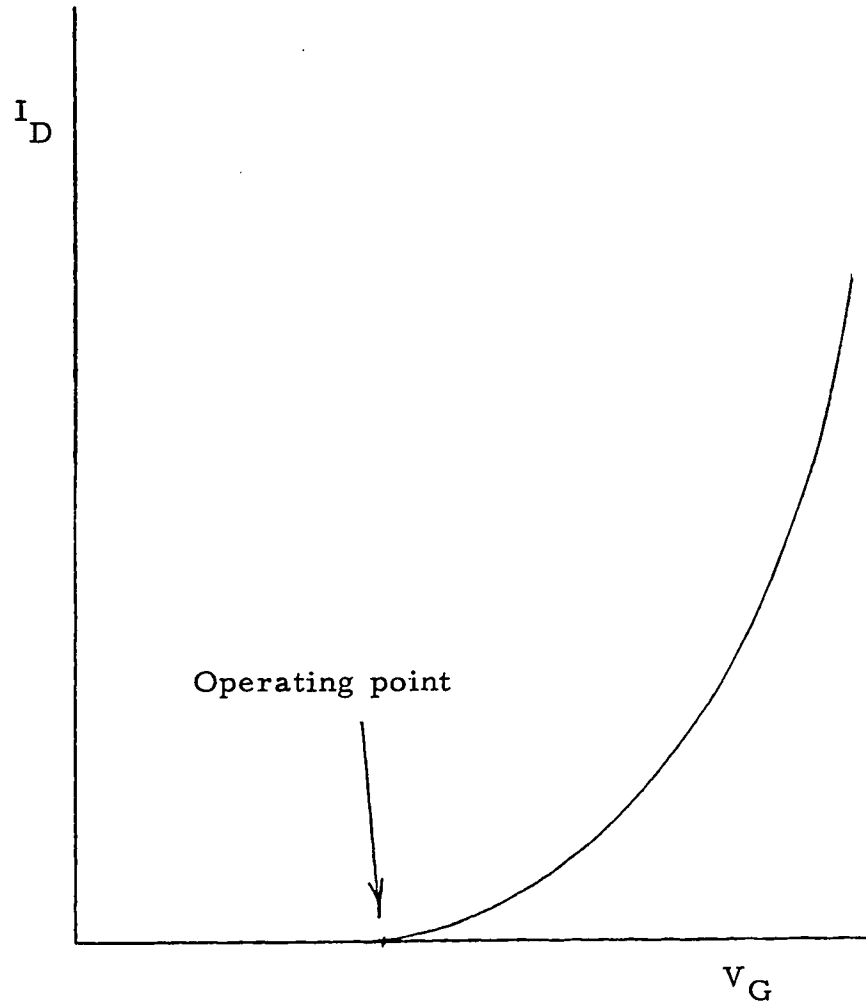


Fig. 45 Operating region for type A resistor of Table II

in section VI-2 a type A resistor may be used for R_L . Since each stage must have a voltage gain of 10, R_L should be an MOS device of channel width/length 0.01 times that of the active device M_1 , assuming other device parameters to be equal. Although the coupling capacitance C_2 to the next stage presents a stray capacitance from the p^+ region to the bulk silicon, the bandwidth can be maintained because the common drain has a low output impedance.

An overall circuit of the ac amplifier is shown in Fig. 46. Since MOS devices occupy a smaller area than bipolar, the complexity of the circuit will not prevent its fabrication as a monolithic unit.

This circuit has not yet been fabricated as an integrated unit, although the circuit design techniques employed have been tested separately.

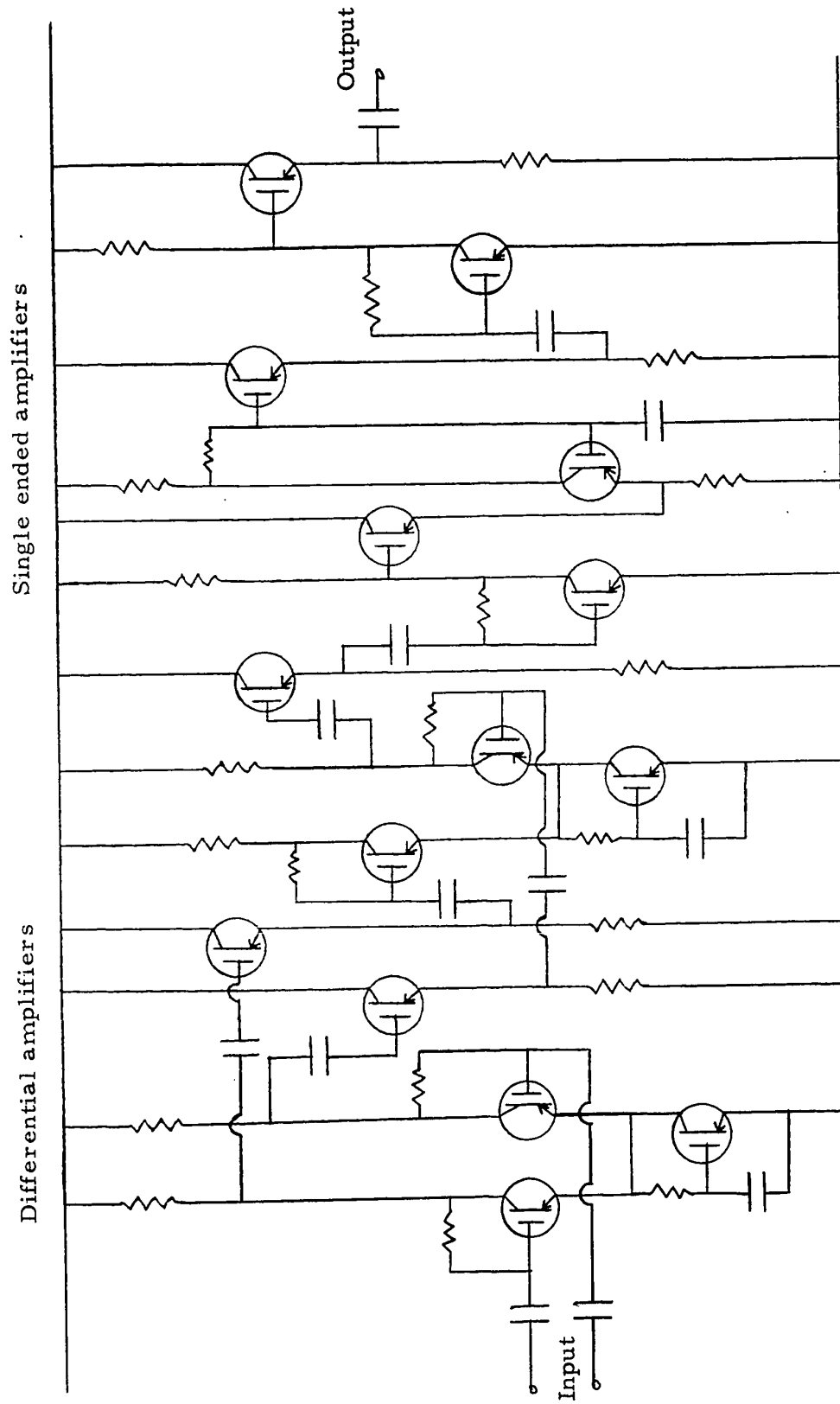


Fig. 46 The overall circuit of the ac amplifier

VII Conclusion

As indicated in the introduction, the major difficulties in applying MOS devices to linear integrated circuits are device nonlinearities, dc instabilities and bandwidth limitations. The thesis has shown that many of these limitations can be overcome, particularly:

- (1) Non-linearities can be removed by matching the characteristic of an MOS load to the characteristic of an active device.
- (2) Dc instabilities can be greatly reduced by the appropriate feedback techniques.
- (3) There are two distinct sources of bandwidth limitations, inherent device limitations and stray capacitances in the integrated realization of the circuit.

The inherent device limitations can be improved only by device development. However, the effect of the stray capacitances can be reduced by placing them at low impedance nodes. Because of the small gain-bandwidth of a single MOS amplifying stage, particularly when these stray capacitances are considered, it is useful to consider active devices in pairs. A matrix of all possible pair combinations has been examined and it has been shown that some of them are useful in linear

amplifier design, in that, although the gain is not increased over that of single stage, the effect of stray capacitances in dc stabilized integrated realizations can be significantly reduced.

The study has been limited to circuits suitable for integration using a single diffusion technology because of the apparent economic advantages. It is clear that additional flexibility will result from more sophisticated techniques such as multiple diffusion technology and complementary devices, and further work is required to explore the possibilities.

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