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Via Walled Cavities as Vertical Transitions in Multilayer Microwave and Millimeter Wave Circuits

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VIA WALLED CAVITIES

AS VERTICAL TRANSITIONS

IN MULTILAYER MICROWAVE & MILLIMETERWAVE CIRCUITS

by

Tom Swierczynski

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ABSTRACT

This thesis describes the development and realization of a novel method of transferring energy vertically through any number of substrate layers of a printed circuit board at microwave and millimeter wave frequencies.

The motivation for this thesis has been the need for a high performance, small size and low cost vertical interconnect circuit which can be used in wireless applications. In particular, array antenna applications often require vertical interconnects in beam forming networks or to couple signals from the beam forming network to the radiating elements. Therefore, the transfer of energy vertically through several layers of printed circuit board is an essential means to pass information for further processing.

This thesis initially discusses and evaluates recent developments produced within the microwave industry on this topic through a concise review of the literature. Shortcomings of current techniques to transfer energy vertically at microwave and millimeter wave frequency are identified and discussed.

The main objective of this thesis was to determine vertical interconnect solutions to operate at any microwave and millimeter wave frequencies, that can be easily implemented using current printed circuit board (PCB) technology and to provide flexibility to construct multiple substrate layer transitions between two microstrip lines by the use of via walled cavities. This was done through the undertaking of both the simulations and practical realization of a vertical interconnect design.

With this objective, the techniques and methodology as well as design guidelines are developed and discussed. Various cavity types and circuit configurations are presented with tradeoff analyses. Also, a manufacturing tolerance study is presented to show that this novel

method of transferring energy can be used in applications at microwave and millimeter wave frequencies.

PUBLICATIONS

[1] T. Swierczynski, D.A. McNamara, "Solutions of switched element array synthesis problems using the parallel generalized projection algorithm", Microwave and Optical Technology Letters, vol. 40, no. 6, pp. 465-471, March 20, 2004.

[2] T. Swierczynski, D.A. McNamara, M. Clenet, "Via-walled cavities as vertical transitions in multiplayer millimetrewave circuits", IEE Electronics Letters, vol. 39, no. 25, pp.1829-1831, December 11, 2003.

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1. INTRODUCTION

With the rising demand for low cost, low profile indoor smart antennas as well as increasing digital data rate requirements in transmission channels, interconnect circuits are becoming vital, integral parts in a successful antenna design. A multilayer printed circuit board (PCB) provides a low-cost, low profile solution for many of today's wireless applications. More complex circuitry is being developed where PCBs of many substrate layers are used to fulfill design requirements. Transfer of energy vertically through several layers of printed circuit board is used to pass information for further processing. In the array antenna applications this includes vertical interconnects in beam forming networks and also coupling signals from the beam forming networks to the radiating elements. At microwave and millimeter wave frequencies these transitions have to be carefully designed as traditional, low frequency techniques do not work effectively.

Frequency bands have been assigned for future broadband indoor wireless systems where the required bandwidths are on the order of 3% to 5%, and at times as much as 10%, when two separate frequency bands are used for transmit and receive channels [1]. In order to be able to realize intelligent antenna arrays whose cost makes them suitable for use in such commercial wireless systems, as much integration as possible is needed. This integration of radiating elements, active microwave integrated circuit (MIC) packaging technology as well as signal processing hardware necessitates the use of vertical RF transitions that pass through many, rather than one or two, substrate layers. This thesis addresses the topic of vertical interconnections between mircrostrip lines on multiple PCB substrate layers.

1.1 PROBLEM STATEMENT

The increasing popularity of microwave and millimeter wave applications has created many challenges for interconnect and MIC packaging technologies. Good vertical transitions for a single substrate layer have been designed using vias [2] and coupling slots [3]. These are

usually not suitable if vertical transitions are required to pass through several PCB substrate layers that may be electrically thick.

Electrically thick ground planes and waveguides have been successfully used to provide vertical transitions, as in [4] and [5], respectively. Unfortunately, these techniques can not be applied to microwave circuits designed using printed circuit board technology. Alternative and novel solutions are considered in this thesis to provide vertical interconnections between multiple PCB layers.

1.2 THESIS OBJECTIVE

The objective of this thesis is to determine vertical interconnect solutions that can be easily implemented using current PCB technology to provide multiple substrate layer transitions between two microstrip lines. Design guidelines are to be provided in order to make simple vertical transitions that RF designers can use. To this end, various coupling configurations and types of vertical interconnects, that would allow high integration, are simulated and discussed. An example of a vertical transition has been designed and built. Its measured performance is examined.

1.3 THESIS OUTLINE

This thesis documents the specifications, design and implementation of a vertical interconnect microwave circuit.

Following this introduction, Chapter 2 provides an overview of existing means of transferring energy vertically on a printed circuit board as applied to microwave and millimeter wave circuits. Various published results are reproduced to establish a baseline for using commercially available electromagnetic simulation tools, such as HFSS [6] and Ensemble [7], in the design of newly proposed vertical interconnect circuits.

In Chapter 3, background information on transmission line and cavity theory is presented. Initial designs of the proposed novel vertical interconnect circuit follow next. This serves as a

learning step in the design and a baseline for a higher performance circuit that is presented in Section 3.6. Various cavity shapes and coupling methods are analyzed to determine the best-suited configuration and the flexibility one has in a design of this kind. Manufacturing tolerances are analyzed in Section 3.7 to provide a better understanding of how performance of the circuit is affected with imperfections of the printed circuit board manufacturing process.

Chapter 4 discusses a design of a vertical interconnect circuit which has been built and tested. Measured results are presented and discussed.

With the completion of the research and development of the novel vertical transition via walled cavity circuit designs, a solution not available with existing design techniques, Chapter 5 presents the final conclusions and discusses the overall results of the thesis.

Also, Appendix A contains detailed manufacturing circuit schematics for the two vertical interconnect designs whereas Appendix B outlines background information pertaining to the simulation tools used in the thesis. It also details the electromagnetic solving techniques that are used by the commercially available tools, HFSS and Ensemble. The high level methodologies of the finite element method (FEM) and the method of moments (MoM) are presented.

Finally, in this thesis, we use the following definitions for return loss (RL) and insertion loss (IL):

RL = 20 * $\log_{10}|S_{nn}|$ [dB] and IL = 20 * $\log_{10}|S_{nm}|$ [dB] where ***n*** and ***m*** can take on integer values of 1 or 2 for a two port network.

1.4 REFERENCES FOR CHAPTER 1

[1] C.A. Fernandes, "Shaped dielectric lenses for wireless millimeter-wave communications", IEEE Antennas and Propagation Magazine, Vol. 41, No. 5, pp. 141-151, October 1999

[2] R.Ito, R.Carrillo-Ramirez & R.W.Jackson, "RF modeling of vertical interconnection between power-ground plane combined with 2D TLM", Proceedings of the 2001 10th Topical Meeting on *Electrical Performance of Electronic Packaging*, pp.339-342 (IEEE Product No. TH8565-TBR).

[3] E. Pillai & W. Wiesbeck, "FDTD analysis of wideband aperture coupled interconnect," Electronics Letters , vol. 31, no. 12, pp. 982-983, 8 June 1995.

[4] M. Davidovitz, R.A. Sainati & S.J. Fraasch, "A non-contact interconnection through an electrically thick ground plate common to two microstrip lines", IEEE Transactions on Microwave Theory and Techniques, vol. 43, no. 4, pp.753-759, April 1995.

[5] M. Coutant & K. Chang, "Broadband, electrically long vertical waveguide interconnect", Electronics Letters, vol. 36, no. 25, pp. 2076-2078, 7 December 2000.

[6] *HFSS*™ (High Frequency Structure Simulator), Ansoft Corporation, Four Station Square, Suite 200, Pittsburgh, PA 15219-1119, USA.

[7] *Ensemble*™, Ansoft Corporation, Four Station Square, Suite 200, Pittsburgh, PA 15219-1119, USA.

2. A REVIEW OF MICROWAVE VERTICAL INTERLAYER TRANSITIONS

2.1 INTRODUCTORY REMARKS

Several methods have been used to provide vertical transition in microwave circuits. Most common means of transferring energy vertically on a printed circuit board includes the use of a via or a coupling slot. For longer vertical transitions, thick conducting ground planes or waveguides can be used to provide vertical interconnections between two transmission lines. These techniques are discussed in the following sections of this chapter. Various published results are reproduced to establish a baseline for using commercially available electromagnetic simulation tools, such as HFSS [1] and Ensemble [2].

2.2 VERTICAL TRANSITION USING A SINGLE VIA

A via is a conducting cylindrical structure that is often used to connect or isolate printed circuits. A typical vertical via transition between two microstrip lines is shown in Figure 1.

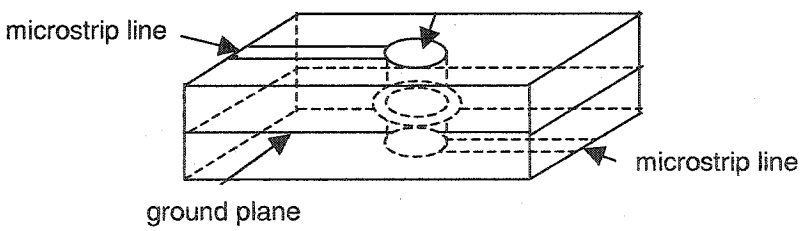

Figure 1: Vertical Via Interconnect

In the recent years, vias have been extensively analyzed to better understand and predict their performance at microwave frequencies. Research has shown [3-14] that vias, although widely used as interconnects up to microwave frequencies, are not well suited to be used in circuits that operate at millimeter wave frequencies. In particular, the performance of such vertical interconnects is very much dependent on the size of via used, i.e. its diameter and length. As the transition becomes longer, not only does the corresponding via length increase, but also

its diameter. This, in turn, causes the interconnect to be inefficient and less adaptable to varying length requirement, as will be demonstrated in Section 2.2.1. This limits this type of vertical interconnect circuit to applications involving one or two substrate layers only.

To demonstrate these limitations when a single via is used as a vertical interconnect, the interconnect in [3] has been analyzed in more detail. In [3], a technique is developed to find a lumped element model for a via interconnection. The accuracy of the modified two-dimensional transmission line matrix method (2D-TLM) is measured against the three-dimensional finite element method (FEM) obtained using HFSS.

2.2.1 Single Via Vertical Transition Geometry of Reference [3]

Using HFSS via was modeled as per [3, Fig. 2.b], where via radius a=10mil, length d=15mil, via pad radius b=20mil, g=5mil, and ε_r=9, no conductor or dielectric losses were used.

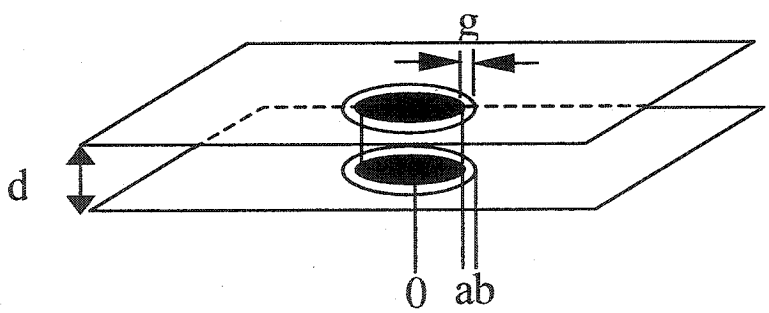

Figure 2: Via Geometry of [3]

For convenience, the results have been reproduced and are presented in Figure 3 and Figure 4. It is clear that this via performs quite poorly above 10GHz, as the return loss reaches –5dB. However, in order to fully understand how well this two port device works, one needs to look at the magnitude of the insertion loss in addition to the return loss over a band of frequencies, as consideration given to only one parameter can be misleading.

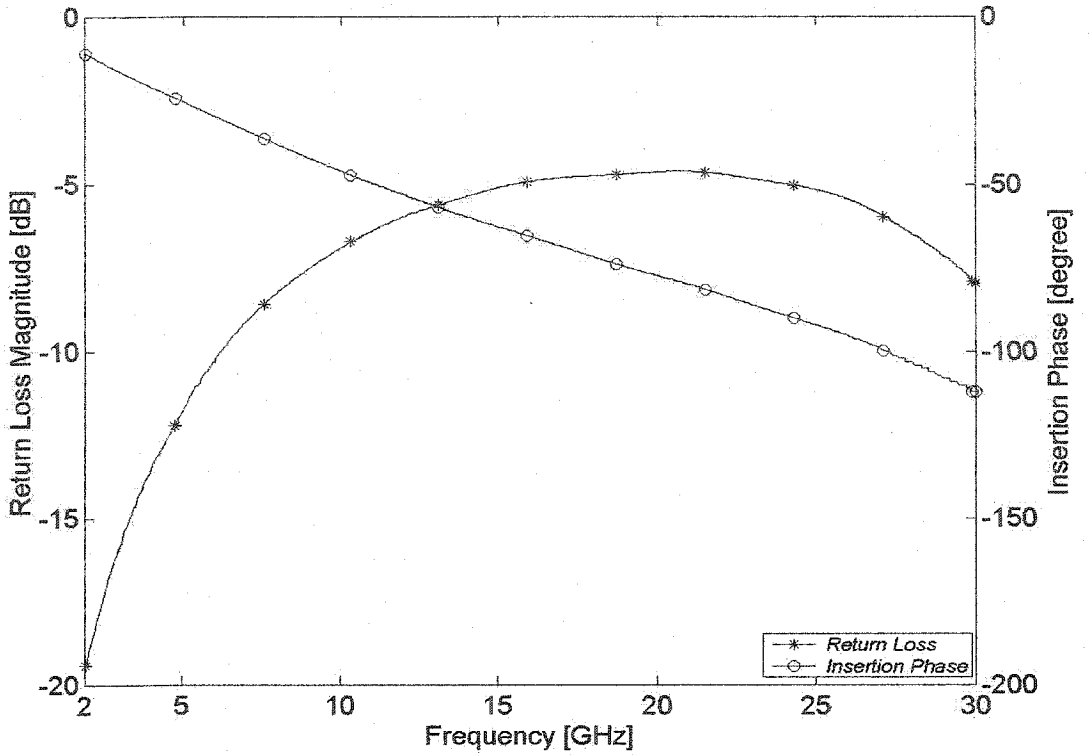

Figure 3: Computed Return Loss Magnitude and Insertion Phase of the Via in Figure 2.

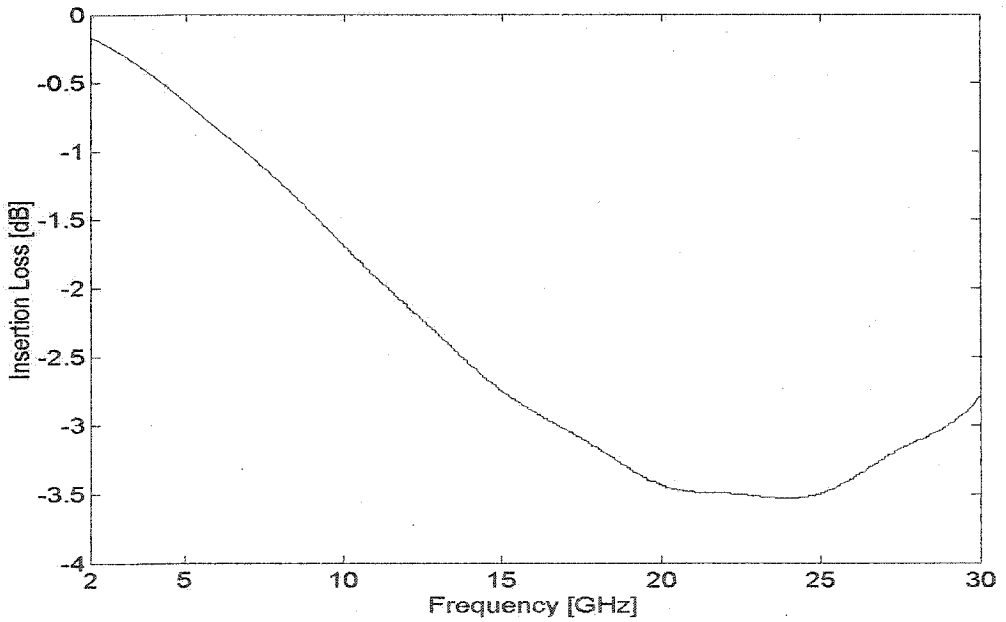

Figure 4: Computed Insertion Loss Magnitude of the Via in Figure 2.

Bandwidth criteria are often dependent on the type of application in which the circuit is being used. If the insertion loss is to be better than –3dB and the return loss less than –10dB, it is clear that a single via presented in [3] can not be used as a mean to transfer energy vertically at frequencies above 8GHz. To further illustrate the limitations of vias at microwave and millimeter frequencies, one can vary the length of the vertical transition. Keeping all other circuit parameters constant, via length was varied from 15mil to 75mil. As demonstrated in Figure 5 and Figure 6, the performance of the transition circuit gets worse with increasing vertical length of the interconnect.

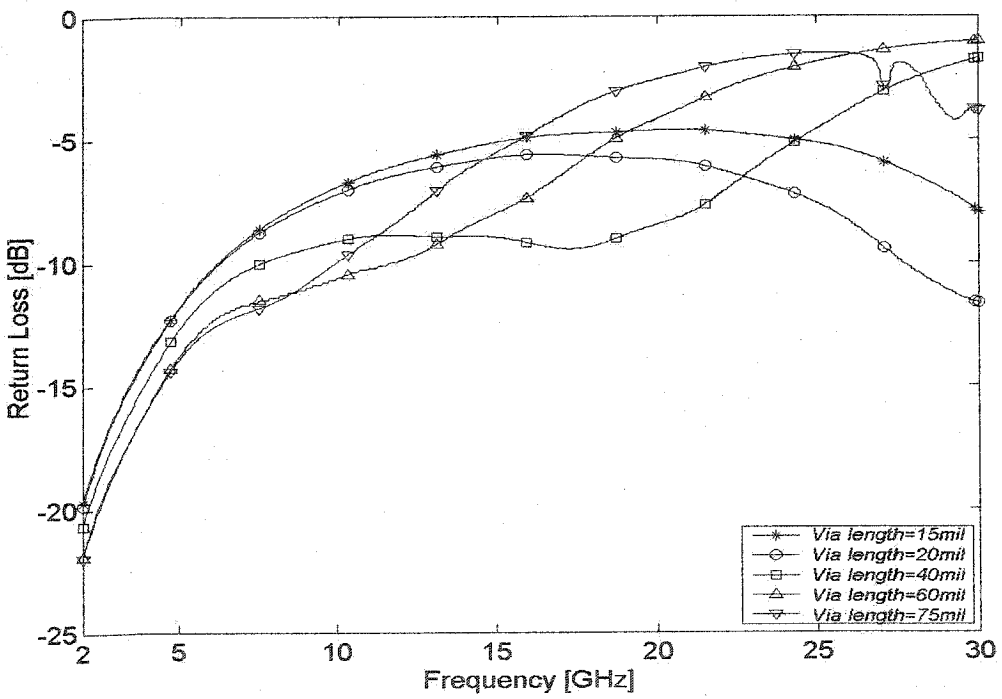

Figure 5: Computed Return Loss Magnitude Versus Frequency. Via length is a parameter.

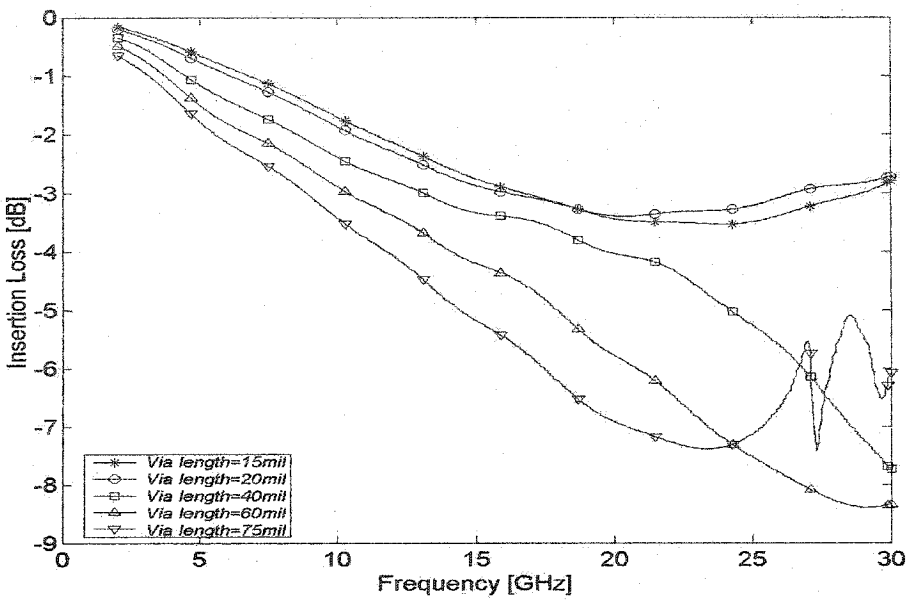

Figure 6: Computed Insertion Loss Magnitude Versus Frequency. Via length is a parameter

Using vias as a means to transfer energy vertically has another practical limitation. The most common manufacturing processes where through hole vias (vias extending the entire thickness of the PCB), blind vias (vias which start at the outer PCB layer and end at an internal substrate layer), or buried vias (vias which are not visible after the PCB has been laminated and which constitute vertical transitions on internal substrate layers) are made to extend through multiple substrate layers, require that the vias be larger in diameter for longer vertical transitions. This is dictated by what is commonly referred to as the "aspect ratio", which is defined as the ratio of PCB thickness to via diameter. For example, the aspect ratio of 5:1 means that a via diameter of 5mil can be used in printed circuit board of a thickness up to 25mil. Boards thicker than this require vias that are larger in diameter. Currently aspect ratios of 10:1 and higher are achievable. Also, packaging technology such as the low temperature cofired ceramics (LTCC) can use small vias on fairly thick PCBs, as the lamination process is such that via holes are drilled through a single layer rather than multiple substrate layers. This, however, results in vias being staggered, which leads to undesirable effects which need to be carefully considered if such geometries are used.

Designs which use through hole, blind or buried vias are dependent on the size of the via for a given vertical transition. In general, the longer the vertical transition, the larger the via diameter needs to be. Therefore, it is necessary to study the effects of via diameter on the performance of the interconnect. In the case of reference [3], exact setup was used as that in Figure 2, with the exception of via radius *a* which was varied from 2.5mil to 10mil. Figure 7 and Figure 8 show that as via diameter increases, even for a small vertical transition of 15mil, this circuit can not be used as a vertical interconnect at microwave and millimeter wave frequencies. This is further demonstrated in [4] for four and ten substrate layer printed circuit boards. In practice, conductor and dielectric losses would further degrade the performance of this type of interconnect circuit.

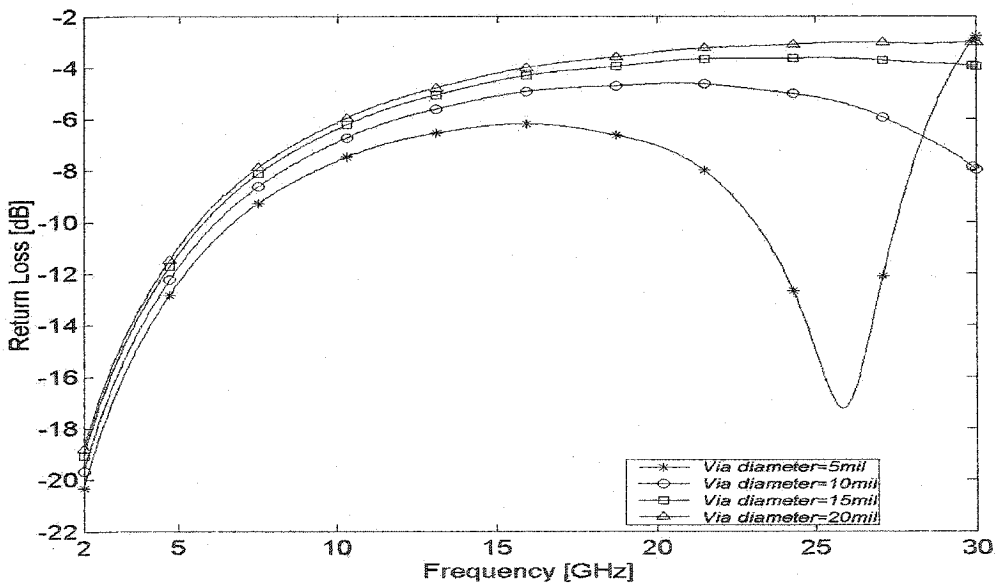

Figure 7: Computed Return Loss Versus Frequency for the Interconnect of [3].

Via Diameter is a Parameter

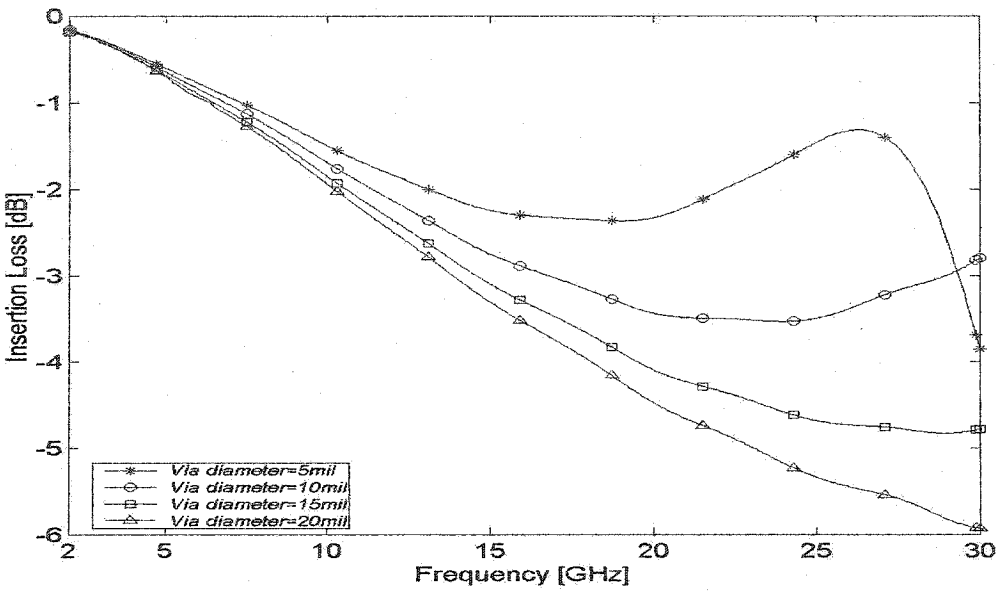

Figure 8: Computed Insertion Loss Versus Frequency for the Interconnect of [3].

Via Diameter is a Parameter

2.2.2 Microstrip to Microstrip Vertical Transition Using a Single Via

The analysis carried out in the previous section suggests that a via does not provide a good means of transferring energy from one substrate layer to another. It is fair to assume that if a single via does not show good performance for energy transfer, then a vertical interconnect built with a via will show even worse characteristic. However, to complete this discussion, it is useful to connect transmission lines on both sides of the via to create a vertical interconnect circuit.

One such example is made by adding 10 mil substrate (ε_r = 9) on both sides of the original circuit depicted in Figure 2. In order to provide 50 Ω matching, the conductor width must be 10.57 mil. The performance computed using HFSS is shown in Figure 9. As for the case of the via geometry in Figure 2, the performance is unsatisfactory at the higher frequencies.

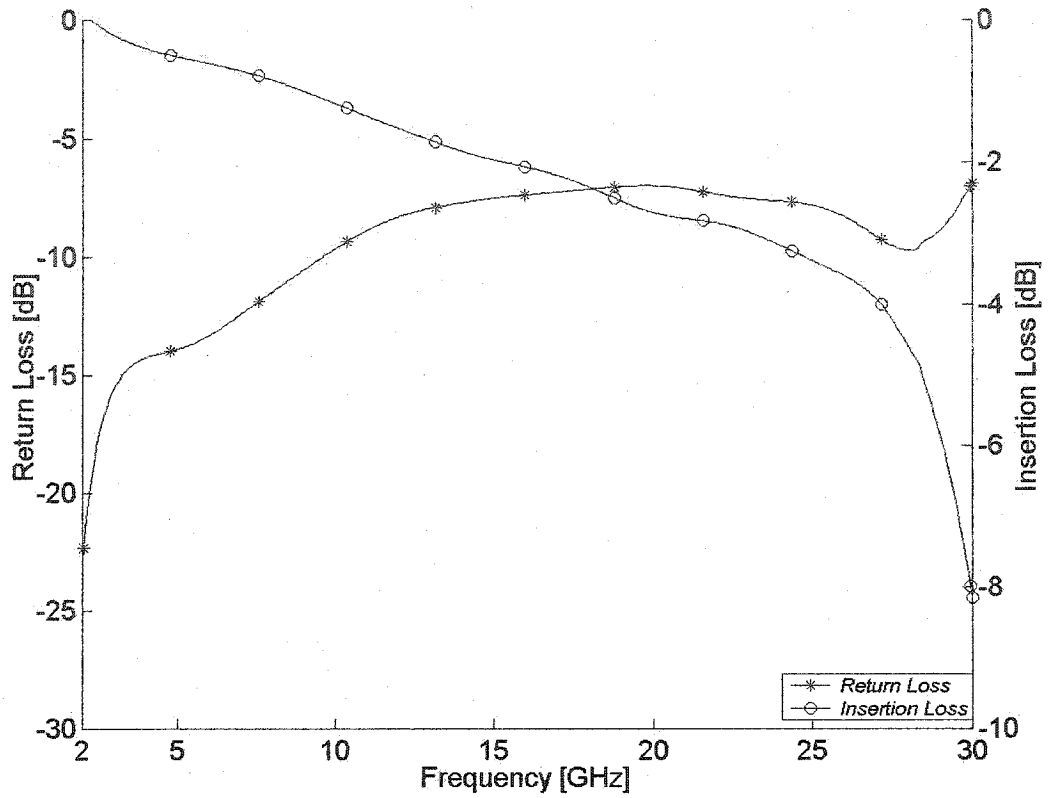

Figure 9: Computed Response of Vertical Transition Between Microstrip Lines Using a Single Via of Figure 2

2.3 APERTURE COUPLED VERTICAL INTERCONNECTS

With the advent of printed circuit board technology, a lot of research has been done to develop printed antennas. With requirements for more compact designs, several techniques have been developed to provide efficient feeding methods for printed microstrip patch and slot antennas. One of the techniques uses aperture coupled microstrip lines, and is thoroughly analyzed in [15-21]. With the inherently narrow bandwidth of patch antennas, research then progressed to the development of structures that would improve printed antenna performance. Two common techniques are the use of a thick substrate, or stacked patches, as well as using a novel aperture shapes, as described in [22-28]. Also, microstrip lines that are offset relative to the center of the slot can provide good coupling of energy, as demonstrated in [29-31]. This adds

flexibility in designing microwave circuits as space constraints may not always allow for inline coupled interconnects to be used.

It is only a natural step in the printed microwave circuits that aperture coupling gets used not only to transfer energy into a radiating element, but also to vertically transfer energy to a non-radiating microwave circuit for further processing. Numerous studies have been carried out to better understand slot coupled vertical interconnects between microstrip lines, striplines, or combination of the two, as in [32-46]. Other types of transmission lines, such as co-planar waveguides, can also be used to build vertical interconnects as the principle of energy coupling remains the same in all cases. The limitation of this type of transition is the inability to transfer energy through more than one substrate layer.

The above mentioned studies are instrumental in the development of vertical interconnects that do operate at microwave and millimeter wave frequencies. As will be shown in Chapter 3, these are the fundamental building blocks of vertical transitions, where good coupling, bandwidth, and minimization of radiation losses are essential performance parameters. Slot coupling techniques, inline and offset coupling configurations, as well as different shape slots serve as a guidance to a good vertical interconnect design.

2.3.1 Aperture Coupled Vertical Interconnect Geometry of Reference [32]

Aperture coupling between two microstrip lines has been investigated by Pillai in [32]. For convenience, the circuit configuration is shown in Figure 10.

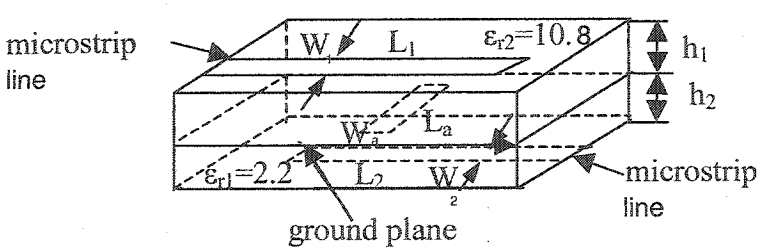

Figure 10: Aperture Coupled Interconnect Configuration (After [32, Figure 1])

The circuit parameters are as follows:

1. W_a = 0.5mm, L_a = 7mm
2. W_1 = 1.545mm, W_2 = 0.554mm
3. h_1 = 0.508mm, h_2 = 0.635mm
4. L_1 and L_2 are open circuit stub lengths, measured from the center of the coupling slot, to be optimized

The author of [32] applied the finite difference time domain (FDTD) method to the above problem in order to obtain the computed performance shown in Figure 11 and Figure 12. We have used Ensemble to reproduce the results. These agree closely with these provided in [32] for the same transition.

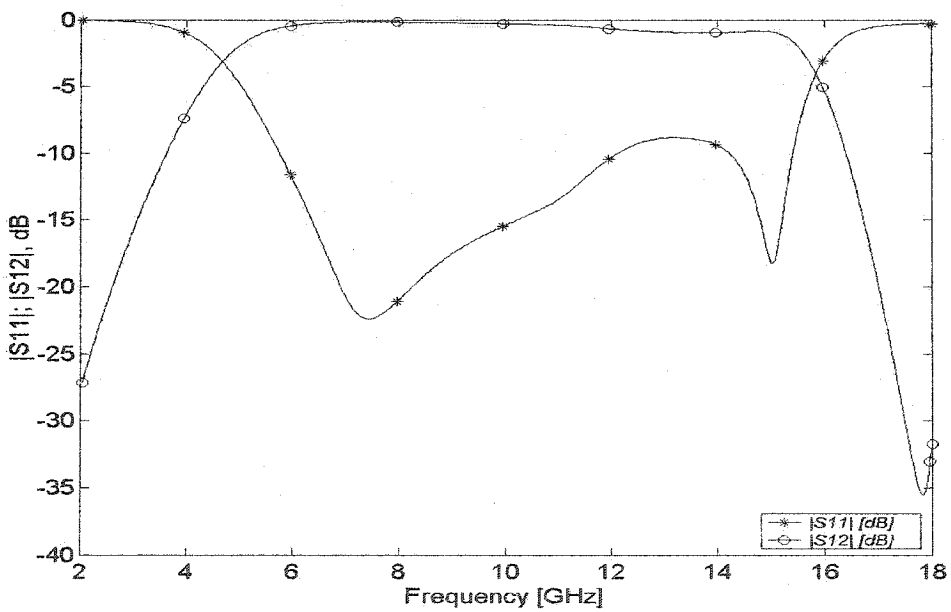

Figure 11: Computed Return Loss and Insertion Loss Magnitudes Versus Frequency (After [32, Figure 2])

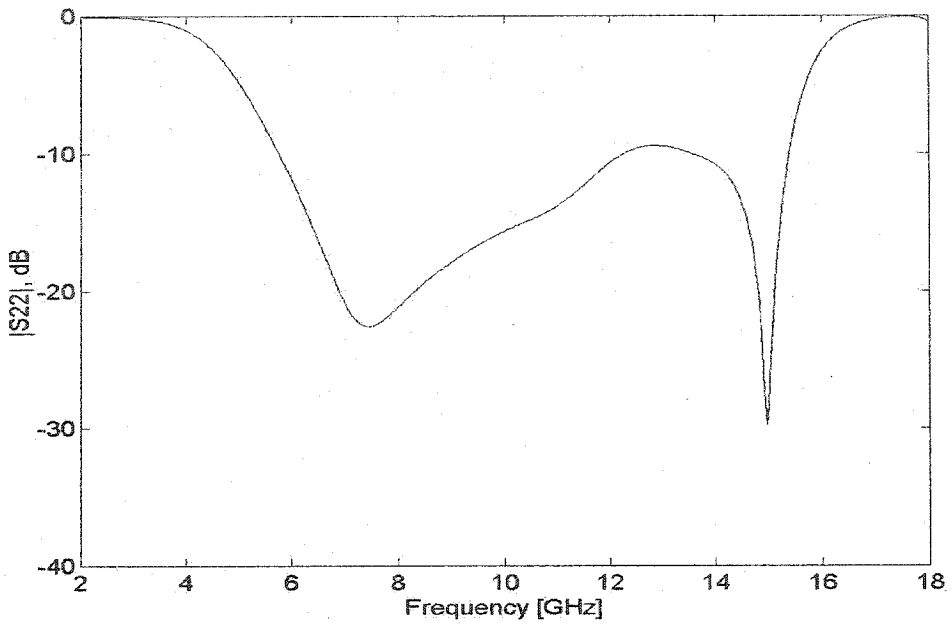

Figure 12: Computed Return Loss Magnitude Versus Frequency

(After [32, Figure 3])

The design was carried out to operate at 9.6 GHz. Figures 11 and 12 show very good agreement with the published data. Figure 12 shows a second resonance at about 15 GHz. Data obtained in [32] using the FDTD method also shows a second resonance but not as pronounced. This can be accounted for by the fact that the Ensemble simulation was carried out using over two thousand sample frequency points, thus allowing for a sharp response to be visible. Return loss, |S11| may not exactly be the same as |S22|, as the structure is not reciprocal.

In the final step, the author of [32] optimized the design by reducing the stub length. This was reproduced using HFSS.

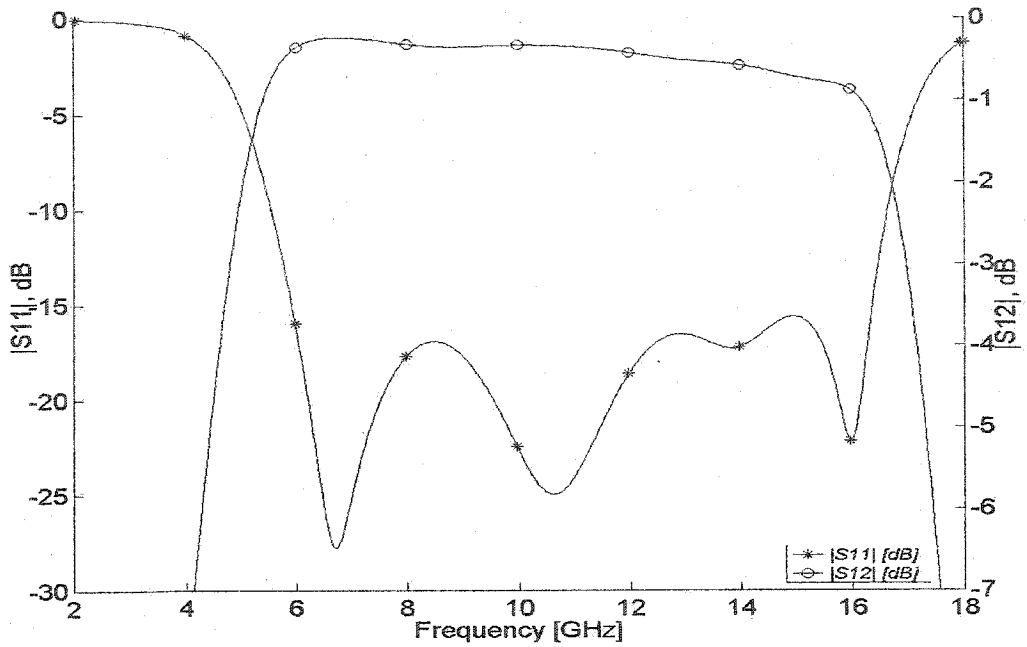

Figure 13: Computed Return Loss and Insertion Loss Magnitudes Versus Frequency (After [32, Figure 4])

All simulations have been carried out using lossless dielectric and conducting media.

2.3.2 Bandwidth Consideration and Analysis

In order to analyze vertical interconnects, one needs to establish criterion for determining the transmission bandwidth. This is often dictated by the application in which the circuit is being used. Suppose we define the impedance bandwidth of the interconnect as that frequency range over which $|S_{11}| < -A$ and $|S_{21}| > -B$. Reference [32] in fact assumes B = 2 dB. Reference [47] uses B = 1.5 dB, while [6] suggests the use of B = 3.0 dB. Both references [22] and [23] identify A = 10 dB.

Based on the information provided in the referenced material, this thesis assumes bandwidth criterion for which B = 2.5 dB and A = 10dB for a lossless circuit configuration.

It is evident that the vertical interconnect presented by Pillai in [32] provides a very wide band transition which can be used to transfer energy vertically through one substrate layer. This technique can be used successfully at microwave and millimeter wave frequencies. Unfortunately, this method lacks the flexibility of providing the microstrip to microstrip vertical transition when several substrate layers separate the microwave circuits. It is common practice to build PCBs of layer counts far exceeding 10 or even 20 layers. In this case, RF circuits may be present on every intermediate copper layer and transitions between several layers are necessary.

2.4 VERTICAL INTERCONNECTION THROUGH ELECTRICALLY THICK GROUND PLANE

Vertical interconnections have also been made using thick ground planes (as opposed to multiple substrate layers) as a means to guide the energy vertically, as in [48-53]. Structures of this type can be used for millimeter wave integrated circuits and phased arrays, as indicated in [49]. With a proper design of the metallic cavity, one can also obtain a wide bandwith response, as in [49,50].

Unfortunately, the cavity orientation used by Pozar in [49] lacks the flexibility of adapting to specified vertical interconnect dimensions for operation at a set design frequency. This, in turn, may not be suitable for some applications where the frequency is low and the design in [49] results in physically large structures. Nonetheless, this type of vertical interconnects serves as a good example of the type of vertical interconnects circuit solutions currently used at microwave and millimeter wave frequencies. In order to exercise the modeling tools on vertical transitions through thick ground planes we will consider the transition in [48] in some detail.

The media for the transition is a thick ground plane with a rectangular slot, which operates in the fundamental waveguide mode, TE_{10}. The transition is made between two microstrip lines. In the analysis carried out in [48], there are no conductor or dielectric losses taken into account. Thickness of the ground plane is varied and performance is analyzed. For convenience, the configuration is shown in Figure 14.

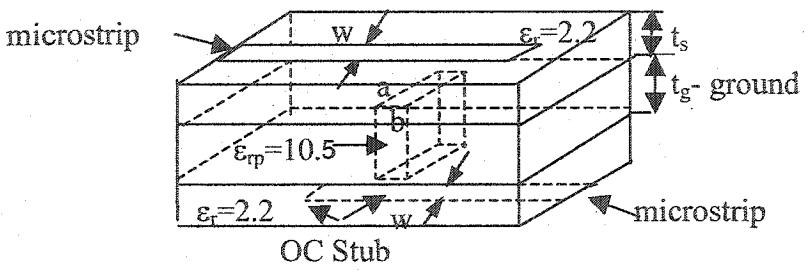

Figure 14: Thick Ground Plane Vertical Interconnect Circuit Configuration

The length of the open circuit stub (OC Stub) is measured from the center of the slot and it is the same for both microstrip lines, i.e. 650 mil that is about one quarter of guided wavelength for a microstrip line at 3.1GHz, or $\lambda_g/4$. The perfectly conducting cavity is filled with a dielectric with a permittivity of ε_{rp}=10.5. Both microstrip lines are constructed using dielectric substrate of ε_{rs}=2.2, substrate thickness of t_s = 62mil, and a conductor width of w = 196mil. The dimensions of the cavity are a = 500mil and b = 100mil. The only dimension that is varied is the vertical height of the cavity, t_g.

Using Ensemble, the published results have been reproduced and are shown in Figure 15, Figure 16 and Figure 17. The obtained data reveals that coupling is very poor when the ground plane is 50 mil thick (Figure 15). This is due to the fact that the waveguide is operating below cutoff, thus severely diminishing circuit performance. As the length of the cavity increases, the resonant behaviour of the lowest order cavity mode (TE_{101}) is dominant, thus providing a coupling structure of very narrow band (Figure 16). The cavity length of 1000mil indicates that more than one resonant cavity mode exists in the transition, indicated by the individual resonances (Figure 17). One could use this concept to broaden the response of the interconnect, the circuit could be optimized in such a way that the resonant frequencies are spaced very close together in frequency.

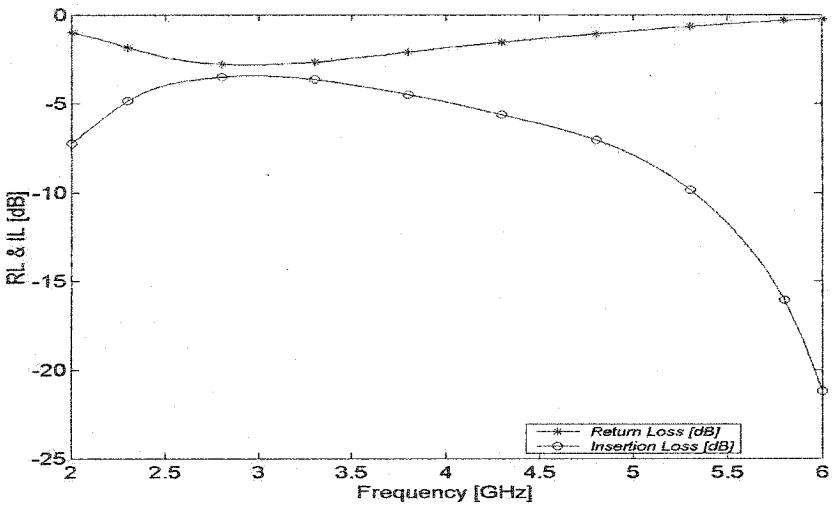

Figure 15: Computed Return Loss (RL) and Insertion Loss (IL).

These results are very similar to these presented in [48, Figure 3]

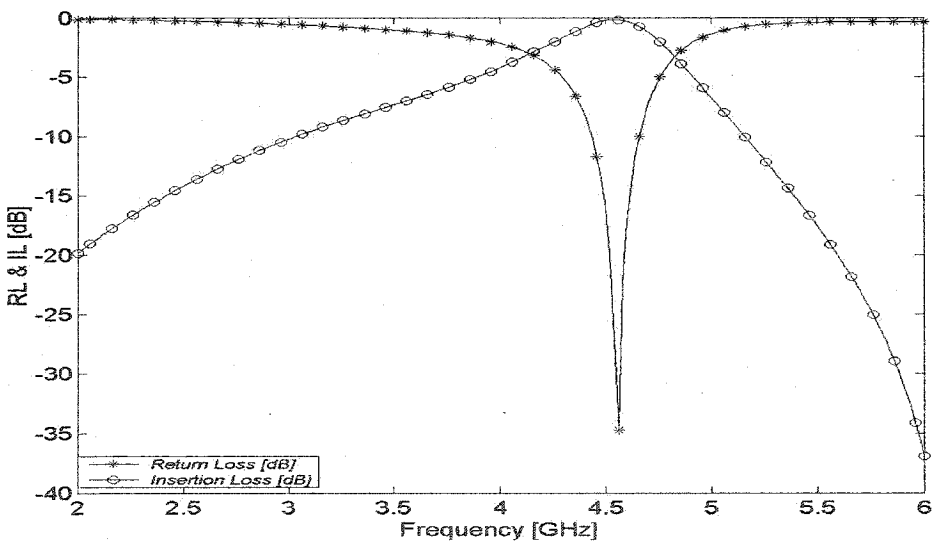

Figure 16: Computed Return Loss (RL) and Insertion Loss (IL).

These results are very similar to these presented in [48, Figure 4]

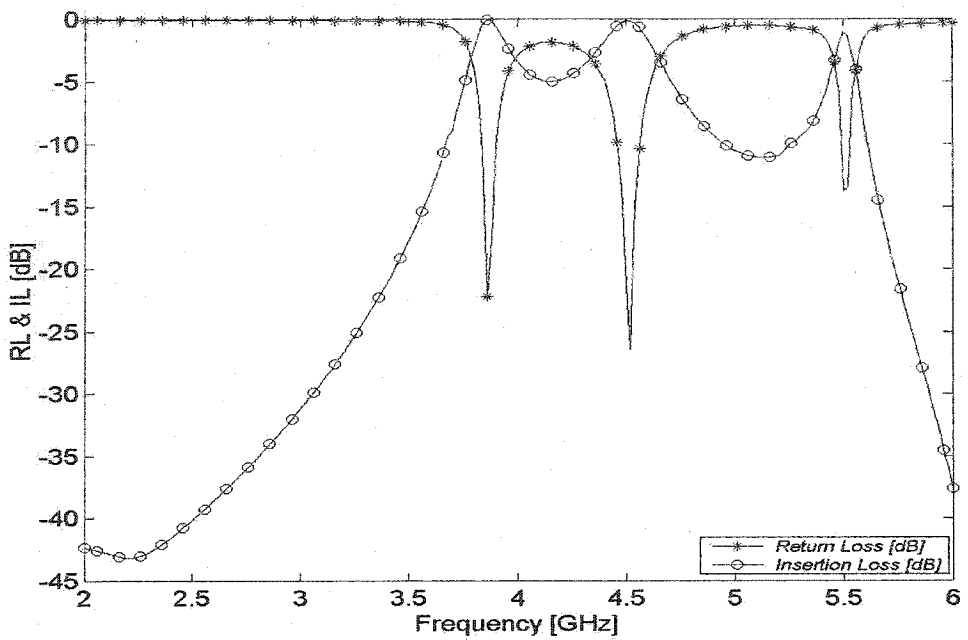

Figure 17: Computed Return Loss (RL) and Insertion Loss (IL).

These results are very similar to these presented in [48, Figure 5]

Using a thick ground plane as a means of vertical transition is not practical for implementation in the printed circuit board technology as it is not feasible to build PCBs with solid, conducting, vertical walls which are rectangular in shape. Furthermore, if these walls were to be broken up into segments, represented by vias, (as will be demonstrated in Chapter 3), this interconnect would not work since there would not be wall current continuity. Finally, the configuration mentioned here exhibits large radiation losses due to the excessively large cavity openings. One can overcome this by coupling into smaller, rectangular slots that are interfacing the much larger cavity.

2.5 ELECTRICALLY LONG, VERTICAL WAVEGUIDE INTERCONNECTS UTILIZING DOUBLE RESONANCES

Similar to that in Section 2.4, but specifically utilizing double resonance behaviour for wider bandwitdth, in reference [47], a vertical interconnect between two microstrip lines was

constructed by including a waveguide filled with a dielectric material and placing it between the two transmission lines. The circuit configuration is shown in Figure 18.

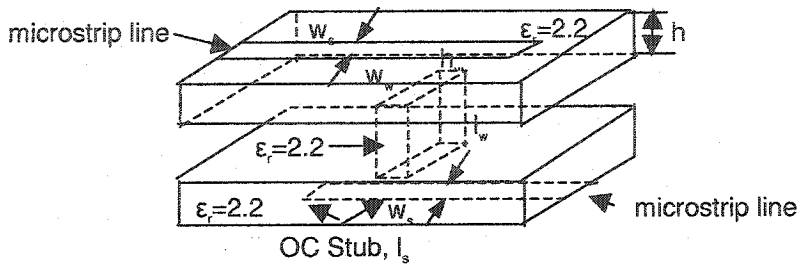

Figure 18: Rectangular Waveguide Interconnect Circuit Configuration of Reference [47]

The following parameters have been used in the construction of the interconnect:

1. w_s = 92.42mils (omitted in publication, calculated based on 50Ω system)
2. l_s = 175mil, h = 30mil
3. l_w = 800mil, w_w = 600mil, and h_w = 62mil

Ensemble was used in the reproduction of the simulation results. Configuration was setup using perfect electric conductors and lossless dielectric material, as in [47]. Circuit performance is shown in Figure 19.

The proposed interconnect seems to support two lowest order, resonant modes. In the attempt to check this hypothesis, one can evaluate resonant frequencies for the TE_{101} and TE_{102} rectangular cavity modes, [54], as follows:

$$f_{TE101} = \frac{c}{2\pi\sqrt{\mu_{rc}\varepsilon_{rc}}}\sqrt{\left(\frac{\pi}{w_w}\right)^2+\left(\frac{\pi}{l_w}\right)^2},\quad f_{TE102} = \frac{c}{2\pi\sqrt{\mu_{rc}\varepsilon_{rc}}}\sqrt{\left(\frac{\pi}{w_w}\right)^2+\left(\frac{2\pi}{l_w}\right)^2} \tag{1}$$

where c is the speed of light in free space, μ_{rc} = 1 is the relative permeability of the material filling the cavity and ε_{rc} = 2.2 is the relative permittivity of the dielectric material.

Applying the above expressions to the current configuration of Figure 18, one finds f_{TE101} = 8.29GHz, and f_{TE102} = 11.96GHz. These resonant frequencies only apply to a rectangular, unloaded cavity. By loading the cavity with two slots and microstrip lines, the resonant frequencies will be different. However, these calculations serve well in determining the electromagnetic field behaviour inside a much more complex structure, such as the microstrip to microstrip vertical interconnect.

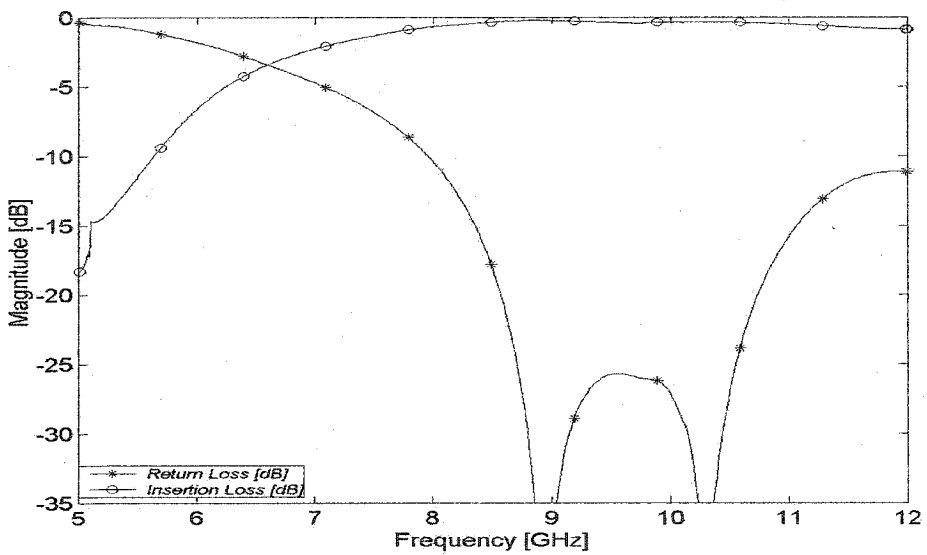

Figure 19: Computed Performance of the Rectangular Waveguide Interconnect in [47, Figure 3]

Finally, this interconnect, although of wide bandwidth, can not be used in integrated designs implemented using printed circuit board technology. This is because the orientation of the currents is such that the cavity must be made with solid conducting walls. This is illustrated in Figure 20.

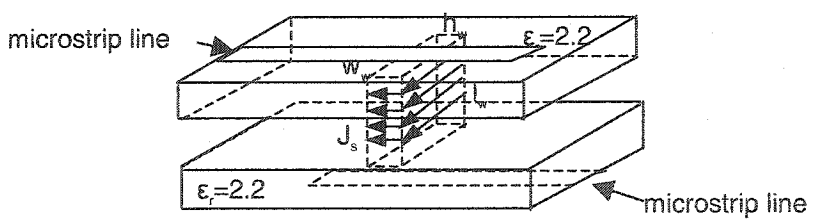

Figure 20: Current Distribution Along Vertical Cavity Walls

J_s represents the surface current density distribution along the vertical walls of the cavity for the TE_{101} and TE_{102} resonant modes.

If this vertical interconnect were to be integrated using PCB technology, the vertical walls would have to be replaced by vertical, cylindrical conductors, or vias. In that case, the coupling presented by this structure would be very poor since the 'effective' vertical walls of the cavity would be broken up into segments, thus drastically disturbing the current density distribution along the walls. Therefore, this approach cannot be used to construct vertical interconnects in the applications of PCB microwave integrated circuits.

2.6 CONCLUDING REMARKS

Three different types of vertical transitions have been considered in this chapter. Section 2.2 dealt with transitions that use single vias between microstrip lines. It was shown that the performance of such transitions is unsuitable at both microwave and millimeter wave frequencies. Section 2.3 discussed vertical interconnects which utilize aperture coupling. While it was shown that these interconnects exhibit good high-frequency performance when used in single-substrate layer configurations, their performance deteriorates rapidly as the number of layers increases. Vertical transitions through electrically thick ground planes (as opposed to those through substrate layers) were discussed in Sections 2.4 and 2.5. While these geometries represent long interconnects, they are unsuitable for use with printed circuit board technologies. In Chapter 3 we will discuss a novel vertical interconnect which overcomes the above limitations.

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3. MULTILAYER VERTICAL TRANSITIONS USING VIA WALLED CAVITIES

3.1 INTRODUCTION

Chapter 3 develops the novel via walled aperture coupled cavity interconnect which is the principal contribution of this thesis. Section 3.2 discusses the geometry of this interconnect. We will see that in order for the proposed interconnect to be compatible with printed circuit board technologies, it is necessary to "construct" one or more of the cavity walls using a "fence" of vias. Thus the use of via-fences (in applications other than vertical interconnects) is reviewed in Section 3.3.

Sections 3.4 through 3.8 deal with vertical interconnects between microstrip lines, using via walled cavities of rectangular shape only. These sections represent a very detailed study of such interconnects. A design procedure for such interconnects is developed in Section 3.4. Parametric studies of two design examples, using electromagnetic simulation, are conducted in Sections 3.5 and 3.6. The effect of manufacturing tolerances on such interconnects is carefully considered in Section 3.7. Section 3.8 demonstrates that it is also possible to design such interconnects for those cases where the intput/output microstrip lines are not "in-line".

The use of alternative via walled cavity shapes in the vertical interconnects is the subject of Section 3.9 (circular cavity shapes) and Section 3.10 (loaded cavity shapes).

While all the above sections of this chapter involve input/output ports consisting of microstrip lines, Section 3.11 deals briefly with the possibility of using striplines instead.

Section 3.12 concludes the chapter.

3.2 CONFIGURATION OF THE PROPOSED VERTICAL INTERCONNECT

The core of the vertical interconnection is a cavity, which is built from conducting cylinders, or vias. Vias are very common in printed circuit board designs. They range in size, often depending on the thickness of the board. In general, vias are larger in diameter when the

number of substrate layers is increased. This is governed by the "aspect ratio", which is a ratio of the thickness of the printed circuit board to the via diameter. Today, it is achievable to build designs with aspect ratio of 10:1 or higher. As will be demonstrated, unlike the vertical interconnects which use a single via, the proposed solution is quite independent of the via diameter.

Thus, the most important building block, i.e. the core of the design is graphically represented in Figure 21.

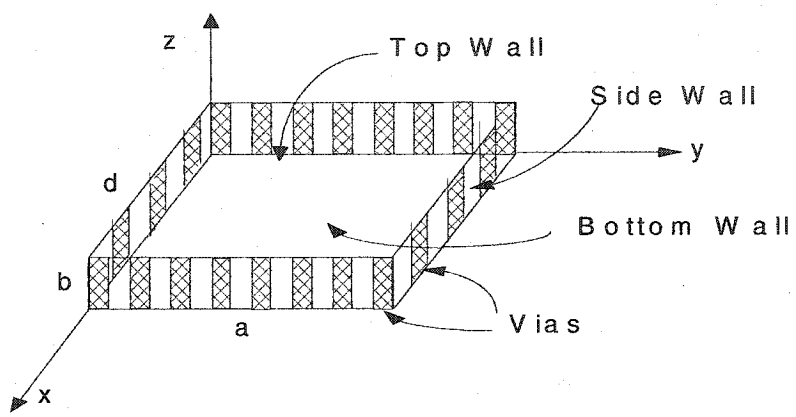

Figure 21: Rectangular Cavity with a Via Fence Forming the Sidewalls.

The shape of the cavity need not be rectangular. Section 3.9 clearly demonstrates that cylindrical shaped cavities may also be considered in the design of vertical interconnect circuits as the design guidelines remain the same.

Although the sketch shows via strips, in practice and in the electromagnetic modelling discussed in this thesis they have a circular cross section, and are modelled using ten rectangular segments. Conducting ground planes containing apertures where the electric field couples energy through the use of the microstrip lines form the top and bottom walls of this cavity. Dimension ***b*** is the vertical distance, which allows transitions to be made, equivalent to several substrate layers.

A complete sketch of the interconnect along with parameter designations is shown in Figures 22 and 23.

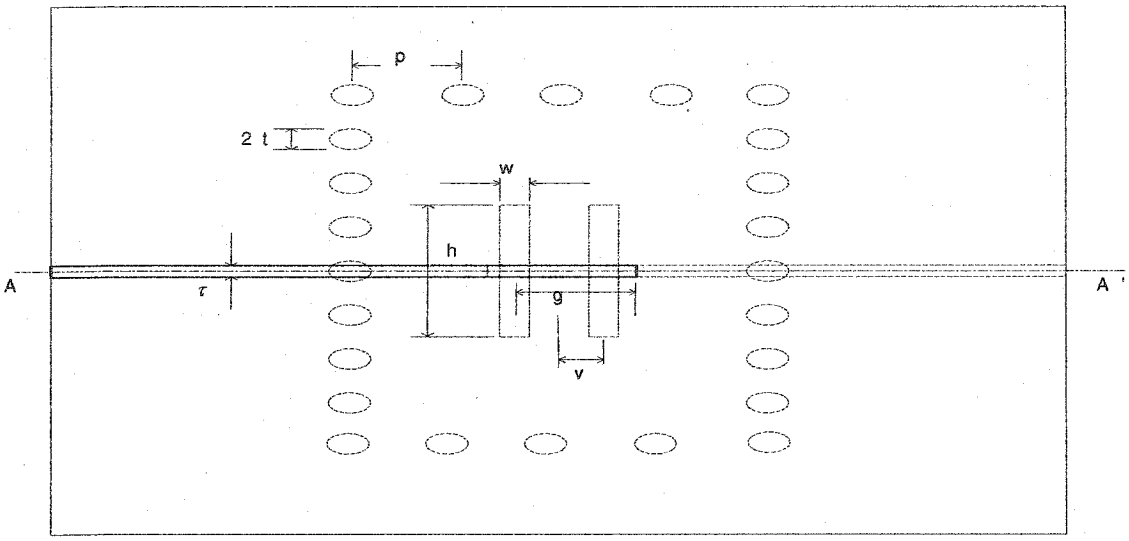

Figure 22: Top View of the In-line Vertical Transition Geometry.

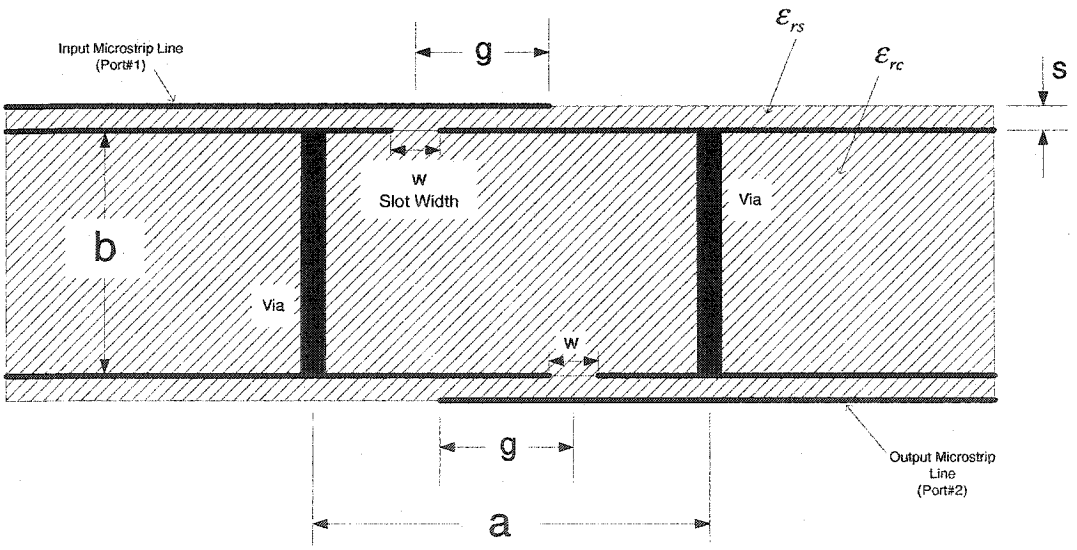

Figure 23: Section (through AA') of the vertical transition in Figure 22

All parameters shown will be considered in this chapter and chapter 4 of this thesis.

3.3 LITERATURE REVIEW ON THE USE OF VIA FENCING

Microwave printed circuits have been used for many years. The idea of using via fencing to create waveguide structures to operate at microwave and millimeter wave frequencies has

been researched since the early 1970s. At that time, work was done to build compact waveguides, circulators and filters in a planar form, as in [1-3]. This new approach of realizing small, integrated circuits was finding a very wide range of applications, from the military electronic countermeasures, radars to commercial wireless communications systems (i.e. hand held communicators), sensors and radiometry (i.e. astronomy, meteorology) just to name a few, as suggested in [2].

Today, the operating frequencies of every day appliances such as computers, wireless phones, stereo systems and others, are continuously increasing. Digital designers are becoming more aware of RF phenomena and design guidelines. With the increasing complexity of the systems and a desire to reduce the physical size of the products, circuits need to be built in isolation from one another to reduce crosstalk. This is why the ideas of via fencing from as far as the 1970s is used today to provide isolation between circuits, as suggested in [4-5]. Naturally, purely RF designs face equal challenge. Antenna arrays need to be small and hidden. The wireless solutions that enter regular households and small businesses require systems which are a lot more integrated than ever before. This is why there is so much effort spent in developing solutions for printed circuits.

Due to the phenomenal technology boom in recent years, via walled waveguide analysis has been resurrected and enhanced to address concerns of today. There is always a concern that replacing a solid conducting wall with a via fence, to allow for the circuit to be manufactured, may result in undesired effects, such as energy leaking out and coupling to adjacent circuits. However, several filters have been successfully designed using the technique of substrate integrated waveguides, as in [6-10].

These publications give a great insight into the design of via walled waveguides and their performances. For example, [6] shows a transition that can be used to feed a planar antenna element. For that purpose, the planar transition exhibits a bandwidth of about 6 – 7 % for a return loss of 15dB and insertion loss of about 4dB. This can serve to establish a bandwidth criteria, previously discussed in chapter 2. As well, one can expect that the predicted

performance parameters might vary considerably from the measured data, as in [8]. It is, therefore, imperative, that one considers manufacturing tolerances when designing these types of microwave circuits.

Finally, the most useful studies that this thesis draws design guidelines from, are the substrate integrated rectangular cavities where designs have been carried out to provide low cost, high quality factor (narrow bandwidth) resonators [11-15]. These circuits also show the type of manufacturing tolerances [11], one can expect and possible frequency shifts of the predicted response [12].

3.4 DEVELOPMENT OF A DESIGN PROCEDURE FOR VERTICAL INTERCONNECTS USING VIA-WALLED RECTANGULAR CAVITY SHAPES

The most commonly used cavity resonator is the rectangular cavity. Substrate integrated rectangular cavities providing low cost, high quality factor (narrow bandwidth) resonators have been used to construct various microwave circuits [11-15]. In all cases, these resonators were designed to operate in the lowest order cavity mode, TE_{101}.

3.4.1 Electromagnetic Aspects of Solid-Wall Rectangular Cavities

The unloaded resonant frequency of the TE_{101} mode of the cavity, with all solid, conducting walls, is given in [16] as

$$f_{TE101} = \frac{c}{2\pi\sqrt{\mu_{rc}\varepsilon_{rc}}}\sqrt{\left(\frac{\pi}{a}\right)^2+\left(\frac{\pi}{d}\right)^2} \qquad (2)$$

where ***c*** is the speed of light in free space, μ_{rc} is the relative permeability of the material filling the cavity, and ε_{rc} its relative permittivity.

It is worth noting that the resonant frequency does not vary with dimension ***b***. As well, the electric field of the TE_{101} mode is constant in the vertical direction, a fact that provides some design flexibility in the height of the vertical transition (and thus the number of substrate layers) for which the present vertical transition design can be obtained. In practice, transitions

ranging from two layers to as many as twenty are feasible, as long as ***b*** < ***a***, as outlined in [16].

The next step in designing a vertical interconnect is to place apertures such that transmission lines (microstrip lines or striplines) can be used to couple energy in and out of the cavity. In order to do this successfully, one needs to understand the current density distribution on the cavity surface for the lowest order mode. Such pictorial representation can be found in [16] and it is repeated here for convenience in Figure 24.

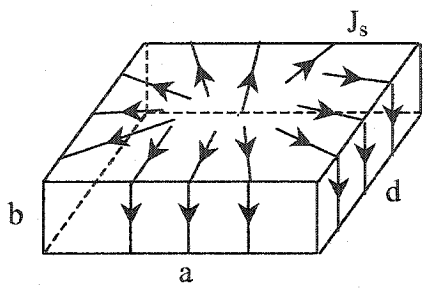

Figure 24: Current Density Distribution of a Rectangular Cavity Operating in the TE_{101} Resonant Mode

On top and bottom surfaces of the cavity (planes ***a-d*** in Figure 24) the current is at its maximum along the edges of the cavity and it declines to zero at the center. Therefore, coupling slots should be placed where the maximum current is, i.e. close to the edge of the cavity. Because of the symmetry of the current distribution, the coupling apertures may be placed along any one of the four edges. This adds flexibility in the design, since one is not forced to position the cavity in only one way, but coupling can be made in variety of ways. Even though the currents are maximum right at the cavity edge, it is impractical to place the apertures there. In fact, when the solid wall cavity is replaced with vias, manufacturing rules will often dictate how far away from the vias an object such as the coupling slots can be placed. Nonetheless, understanding this behaviour aids in the design and optimization of a good vertical interconnect.

Following the design of the solid wall cavity and a rough placement of the coupling slots, one needs to design a microstrip line to establish appropriate two port connection and sufficient coupling.

3.4.2 Microstrip Line Design

In the design of the vertical interconnects, the most commonly used means of energy transfer between two substrate layers is accomplished by using either two microstrip lines (connection between outside printed circuit board layers) or two striplines (connection between inner circuit layers). The design of interconnects remains the same in principal. This is why most of the analysis is carried out using vertical interconnect circuits between two microstrip lines. One example of stripline to stripline coupling is also demonstrated in Section 3.11.

Almost every undergraduate textbook on electromagnetic theory deals with the microstrip lines and striplines. Chapter 3 of [17] is used here as a basis for the following discussion.

A microstrip line is a transmission line that is etched on a slab of a dielectric substrate that has a conducting plane on the opposite side. Microstrip lines support quasi-TEM modes because the dielectric to air interface has a discontinuity in the phase velocity of the fields, i.e. the phase velocity in the dielectric region, $\frac{c}{\sqrt{\varepsilon_r}}$, is different from the phase velocity in air, *c*. Thus, phase match at the dielectric – air interface is impossible to obtain for a TEM type wave. However, good static or quasi-static solutions may be applied, as usually the substrate is electrically very thin.

With a given permittivity of the dielectric material, chosen substrate thickness and characteristic impedance of the line, one can use the approximate closed form solutions outlined in chapter 3 of [17] to obtain desired conductor width. For convenience, these relationships are outlined in equation (3).

$$\frac{W}{d}=\begin{cases}\dfrac{8e^{A}}{e^{2A}-2} & for\ W/d<2\\ \dfrac{2}{\pi}\left[B-1-\ln(2B-1)+\dfrac{\varepsilon_r-1}{2\varepsilon_r}\left\{\ln(B-1)+0.39-\dfrac{0.61}{\varepsilon_r}\right\}\right] & for\ W/d>2\end{cases} \qquad (3)$$

where

$A=\dfrac{Zo}{60}\sqrt{\dfrac{\varepsilon_r+1}{2}}+\dfrac{\varepsilon_r-1}{\varepsilon_r+1}\left(0.23+\dfrac{0.11}{\varepsilon_r}\right)$, $B=\dfrac{377\pi}{2Zo\sqrt{\varepsilon_r}}$, and ***W*** is the conductor width, ***d*** is the substrate thickness.

Surface waves are electromagnetic waves, which are totally reflected from a dielectric interface. In the design of microstrip lines, consideration must be given to the TE and TM surface waves that can be excited along a grounded dielectric slab. In reference [17], Pozar derives the cutoff frequency of the TM_n mode to be $f_c=\dfrac{nc}{2d\sqrt{\varepsilon_r-1}}$, n = 0, 1, 2, ... and the TE_n mode to be $f_c=\dfrac{(2n-1)c}{4d\sqrt{\varepsilon_r-1}}$, for n = 1, 2, 3, ... In both formulations, ***c*** is the speed of light, ***d*** is the thickness of the dielectric slab, and γ_r is the relative permittivity of the dielectric material. Note that the dominant TM mode is the TM_o mode for which the cutoff frequency is zero.

In the current design, ***d*** = 6 mil = 152.4 :m and ε_r = 7.1. The cutoff frequencies of the TM_1 and TE_1 modes are 398.51 GHz and 199.25 GHz, respectively. Therefore, there is no danger of launching a surface wave when the operating frequency is 20 GHz, which was chosen more or less arbitrarily. This is because the design methodology can be easily applied to circuits operating at other microwave or millimeter wave frequencies. Finally, to complete the design of the microstrip line, the corresponding line width of the transmission line can easily be evaluated using equation (3). In this example, the line width, ***w*** = 7.8 mil = 198.12 :m.

In order to couple energy in and out of the cavity, one needs to understand how the transmission line (microstrip or stripline) must be positioned relative to the coupling slot.

When a transmission line is terminated in an open circuit, the standing wave produced can be seen to have a maximum voltage wave at the end of the line, and minimum (zero) current (corresponding to infinite load impedance). Rotating one quarter wavelength or one half around a Smith Chart, one finds minimum voltage (zero) and maximum current. It is that point on the transmission line that needs to be lined up with the center of the coupling slot. This short analysis is only valid when the system is solely comprised of a transmission line, be it microstrip or stripline. In proposed configuration, the loading aperture presents a series impedance and as a result it will change the behaviour slightly. However, positioning of the transmission line with a stub of one quarter wavelength from the center of the coupling slot is a good starting point in the design. Once this is done, the design can be optimized for best performance.

3.4.3 Via-Walled Equivalents of Solid Wall Rectangular Cavities

In the previous sections, design guidelines have been set to allow a vertical transition to be designed and optimized with a solid wall rectangular cavity. This is very useful because simulations required to solve this type of configuration are much shorter than ones where solid wall cavity is replaced with vias. Since one needs to not only optimize the coupling slot dimensions ***h*** and ***w*** (see Figure 22) but also the open circuit stub length, ***g***, many parametric sweeps of different values need to be run to obtain the optimum design (sometimes in excess of 200 or 300 hundred simulations). This process can take as little as 24 – 48 hours on a computer containing a Pentium 3, 2.4 GHz microprocessor with 512 Mbytes of RAM (Read Access Memory). In comparison, vertical interconnect circuits where the cavities are made of vias result in simulations that can take several hours each. In order to perform the same number of simulations, one would need several weeks to obtain an optimum design. This is because the problem results in many more unknowns that need to be computed. In the case of HFSS [18], the solution converges much faster when the solid wall cavity is used. This is

because the current distribution along the vertical walls is constant in the vertical direction. In comparison, when vias form the cavity, the fields are more complex and require more meshing in the area where they are placed. On the other hand, Ensemble [19], allows for rectangular cavities to be used because the Green's function that is used already takes into account the presence of the cavity. This means that solid wall rectangular cavity does not need to be meshed and the number of unknowns is drastically reduced. Once the vias are placed, the method of moments used by Ensemble can no longer use that same Green's function, thus every via needs to be meshed and currents solved for. This results in many more unknowns and increased simulation time.

Once the circuit is optimized using a solid cavity wall, the vertical walls of the cavity are replaced by a via fence. Although [7] and [9] deal only with rectangular waveguides constructed of the via fences, they, for the specific manner in which the cavity is being used here, provide some useful guidelines as to how the via wall dimensions must be related to those of the original solid walls. Reference [8] suggests that, to decrease leakage through the via walls (in other words, better approximate the solid wall with vias) one should use $2t/p \approx 0.5$, where $2t$ is the via diameter and p the pitch (that is, center to center spacing) between vias, as per Figure 22. Translated into the cavity framework of interest here, [7] further suggests that the dimensions a and d, obtained from the solid wall cavity considerations, must each be increased by an amount $(2t)^2 / 0.95p$, and the center of the vias then be placed along the boundary contour of the enlarged cavity. In order to structure this process, vias are placed at each corner and then the remaining vias inserted in such a way as to achieve $2t/p \approx 0.5$ as closely as possible. This new configuration will result in performance very close or identical to that obtained by solid wall cavity.

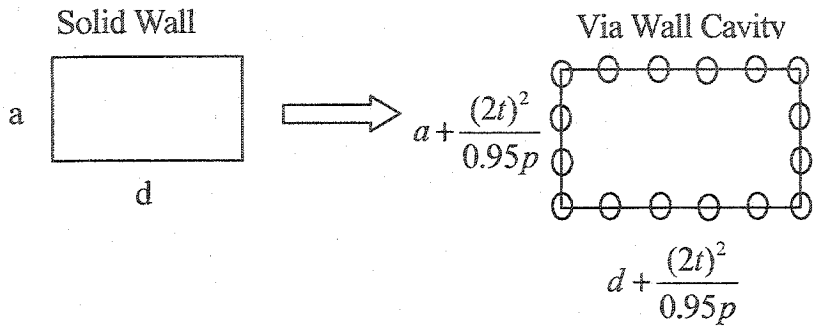

Figure 25: Top View of the Solid Wall Cavity to Via Wall Cavity Design Transformation

One way to understand why the effective cavity dimensions are enlarged in the presence of via fence to obtain the same resonant response as the solid wall cavity is to envision a scenario where to replace the solid walls, ***a*** and ***d***, vias are placed such that center of each conducting cylinder lies along the cavity outline. If vias are placed closer and closer together the resulting wall will be such that the effective dimensions a_{eff} and d_{eff} will be much smaller than the original solid wall cavity dimension, ***a*** and ***d***. Smaller cavity results in higher resonant frequency, as per equation (2). Therefore, to make this work, the via fence cavity must be moved further away in order to bring the resonant frequency of the unloaded cavity down to the desired value. This is illustrated in Figure 26.

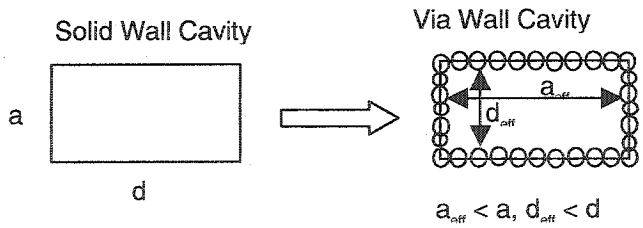

Figure 26: Top View of the Solid Wall Cavity to Via Wall Cavity Transformation

Design Rule Review

3.4.4 Vertical Interconnect Design Steps

It is always useful to have the above design procedure summarized for a quick reference. The steps are outlined next:

1. Determine dimensions ***a*** and ***d*** of a solid wall unloaded cavity as per equation (2) keeping in mind that the vertical distance ***b*** must satisfy ***b*** < ***a*** and ***a*** < ***d*** (lowest order TE_{101} cavity mode).
2. In the case of microstrip to microstrip vertical interconnect circuit, determine conductor width of the transmission line, τ, as per equation (3), ensuring that no higher order mode surface waves can propagate.
3. Determine the location of the rectangular coupling slots (rectangular shape slots are easiest to analyze). Position slots as close to the edge of the cavity as possible ensuring manufacturing rules are obliged.
4. Position transmission lines in such a way that open circuit stub length of $\lambda_g/4$ (one quarter of guided wavelength) is set from the center of the aperture.
5. Perform full 3D electromagnetic simulations to optimize the design with solid wall cavity and no conductor or dielectric losses. The parameters in question are the coupling slot dimensions, ***h*** and ***w***, and the open circuit stub length, ***g***, as depicted in Figure 22.
6. Once the design is optimized, replace vertical solid cavity walls with via fences. This can be easily done by increasing both ***a*** and ***d*** cavity dimensions by the amount $(2t)^2 / 0.95p$, where ***2t*** is the via diameter and ***p*** the pitch , and the center of the vias then be placed along the boundary contour of the enlarged cavity. In order to structure this process, place vias at each corner and then insert the remaining vias in such a way as to achieve $2t/p \approx 0.5$ as close as possible.
7. Perform a simulation of the new structure. If the circuit resonates at a slightly different frequency, adjust new cavity dimensions, ***a*** or ***d***, to obtain desired response.
8. Once a desired response is obtained, include conductor and dielectric losses in the simulation.

As will be pointed out in later sections of this chapter, step # 7 will be limited to adjusting only one dimension, i.e. ***d***. This will simplify the design process even further.

3.4.5 Application of the Design Procedure

The design procedure developed in this section will be applied in Section 3.5 and Section 3.6. Section 3.5 will provide a rapid means of understanding the behaviour of such interconnects. Electromagnetic simulations will be used to predict the performance of the interconnect, and how this performance varies with changes in the physical dimensions (i.e. slot size, stub length, interconnect height). With the understanding provided by the above exercise, the design procedure is applied, in Section 3.6, to a second example, yielding improved interconnect performance and a circuit which is less sensitive to manufacturing tolerances.

3.5 DESIGN OF A VERTICAL INTERCONNECT WITH A VIA-WALLED RECTANGULAR CAVITY: APPLICATION #1

3.5.1 Present Aims

A vertical interconnect design is presented in this section. Electromagnetic simulations are used to predict circuit behaviour and understand effects of various circuit dimensions on the performance of the vertical interconnect. This interconnect serves as a basis to develop orthogonal coupling vertical interconnect circuit configuration, as described in Section 3.8. In Section 3.6, cavity dimensions will be optimized to obtain a design with a much larger impedance bandwidth and remove circuit performance sensitivity to one cavity dimension.

3.5.2 Basic Design

Without much insight into the design of vertical interconnects, a rectangular cavity vertical interconnect design was produced. First, dimensions a and d were selected such that the unloaded cavity would resonate at around 20 GHz. There are infinitely many possibilities when selecting these two values. For no particular reason other than to ensure that $a < d$ for propagation of TE_{101} mode, a solid wall cavity was selected to be of dimensions a = 150 mil, d = 164 mil. The dielectric material was chosen to have $\varepsilon_r = 7.1$ since this is a typical value for LTCC material, DuPont 943 or 951 process, likely to be more commonly used for multilayer circuits in the future, as suggested in [20-21]. Since the vertical dimension of the cavity can be, in theory, of any value as long as it is less than a, b was selected to equal 75 mil. This is

much larger than the vertical transitions used with the single via circuits, considered in Chapter 2, thus providing a good test for this type of a vertical interconnect.

With the cavity dimensions set, the next step in the design is to determine microstrip line parameters. With a characteristic impedance of 50 Ω and substrate thickness of 6 mil, the conductor width was calculated to be τ=7.8 mil, using equation (3). The guided wavelength for this microstrip line equals 264 mil ($\lambda_g = \frac{\lambda_o}{\sqrt{\varepsilon_{eff}}}$, where $\lambda_o = \frac{c}{f}$ and effective dielectric constant is $\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/W}}$, where ***d*** is the thickness of the dielectric material and ***W*** is the conductor width, as per chapter 3 of [17]). Therefore, the open circuit stub length is set at one quarter of the guided wavelength, i.e. ***g*** = 66 mil.

Next, rectangular slots are positioned v = 50 mil from the center of the cavity. This is illustrated in Figure 27.

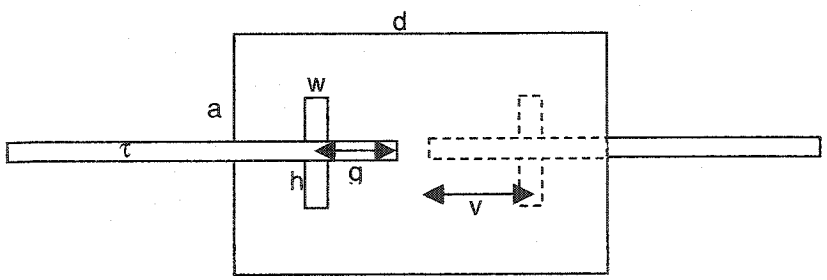

Figure 27: Top View of the Solid Wall Rectangular Cavity Vertical Interconnect

The design was optimized for ***w*** = 8 mil, ***h*** = 70 mil, and ***g*** = 51 mil. It so happens that the optimum open circuit stub is shorter than the predicted value of 66 mil. One could argue that due to fringing effect, the transmission line appears longer than it really is, as suggested by Edwards in chapter 7 of [22]. Unfortunately, the loading presented by the entire circuit is much more complex and more difficult to predict. As will be demonstrated

in later sections, the optimum open circuit stub may actually be much longer than the predicted, $\lambda_g / 4$ value.

The final design step is to replace the solid wall cavity with a via fence. For via diameter of 10 mil and desired pitch of 20 mil, the amount by which ***a*** and ***d*** must increase is 5.26 mil. This becomes the new outline for the vias to be placed. Once the corner vias are placed, one places the remaining vias with equal spacing between them. In this configuration, 8 vias have been placed along side ***a*** with 22 mil spacing between them, and 9 vias were placed along side ***d*** with 21 mil spacing. Figures 28 and 29 show the comparison between solid cavity and via fenced cavity designs (lossless case). The results have been obtained using Ensemble. There is a slight frequency shift in the two responses of about 80MHz. One can change this by moving via walls ***a*** or ***d*** in order to match the two responses. However, this is difficult to do as 80MHz frequency change is very small compared to the operating frequency and slight changes to the cavity size will result in larger separation of the two curves.

The insertion loss shows that there is no energy lost when solid cavity wall is replaced with via fence. This further suggests that the design rules outlined by Cassivi et al, [7], are very accurate to approximate the solid cavity wall.

Finally, the bandwidth of the response is very narrow, about 100 MHz or 0.5 %, corresponding to high quality factor. This is not a desirable result, as bandwidths of 3% to 5% are usually sought for in an interconnect design. Nonetheless, this first design serves well as a means to better understand the networking of microwave vertical transitions.

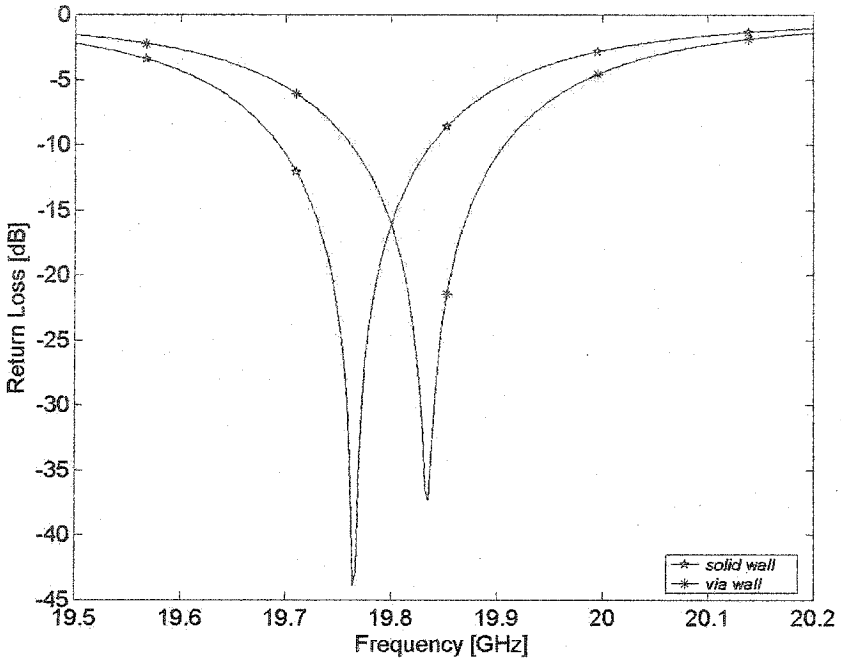

Figure 28: Return Loss vs. Frequency for a Solid and Via Wall Cavity Interconnects

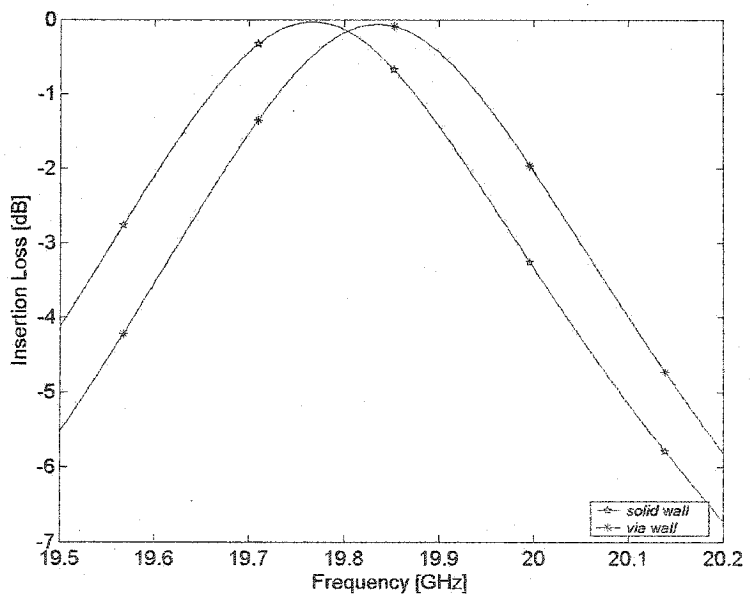

Figure 29: Insertion Loss vs. Frequency for a Solid and Via Wall Cavity Interconnects

3.5.3 The Effects of Dielectric and Conductor Losses

To complete any design, one must include any imperfections to better predict the response of a "real life" microwave circuit. This is usually done by including losses in the final analysis. The most common losses which are easily modeled are the conductor (Ohmic) losses and dielectric losses.

The most commonly used conductor material is copper, although other materials are also used to lower ohmic losses, especially since they are the more dominant of the two, as pointed out by Edwards in chapter 5 [22]. This includes silver and gold, much more expensive than copper.

Next, conductivity of $\sigma = 5.8 \times 10^7$ S/m and a loss tangent for the dielectric material of $\tan\delta = 0.0025$ (slightly worse than the lowest loss LTCC material currently available and reflective of Ceramic Low Temperature Expansion, CLTE, material used to build a prototype design [23] outlined in Chapter 4), were used in order to allow the model to predict the transition's performance in the presence of losses.

The simulation results shown in Figures 30 and 31 were obtained using HFSS.

Insertion loss clearly indicates the expected performance degradation when conductor and dielectric losses are included in the analysis. In the small frequency band where impedance bandwidth is defined, aggregate losses of about 2 to 2.2 dB are expected.

In the following sections, different circuit parameters are varied to see what effect they may have on the overall performance of the interconnect. This will serve as a good basis to design interconnects of various configurations and better performance as well as understand circuit performance sensitivity to various parameter changes.

Finally, because the circuit is reciprocal, all parameter changes are done to both sides of the vertical interconnect at the same time. Also, performance measurements of interest are the magnitude (in dB) of the return loss and and the magnitude (in dB) of the insertion loss.

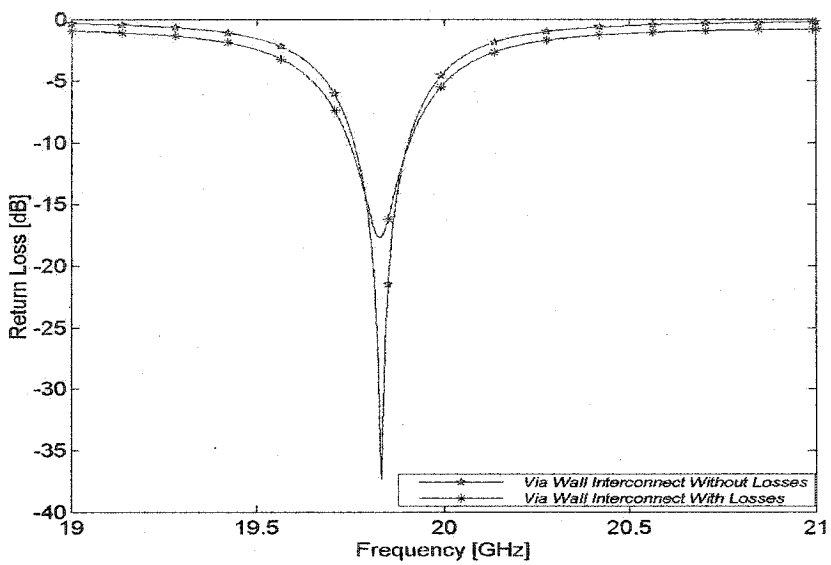

Figure 30: Return Loss vs. Frequency for a Via Wall Cavity Interconnect with Losses

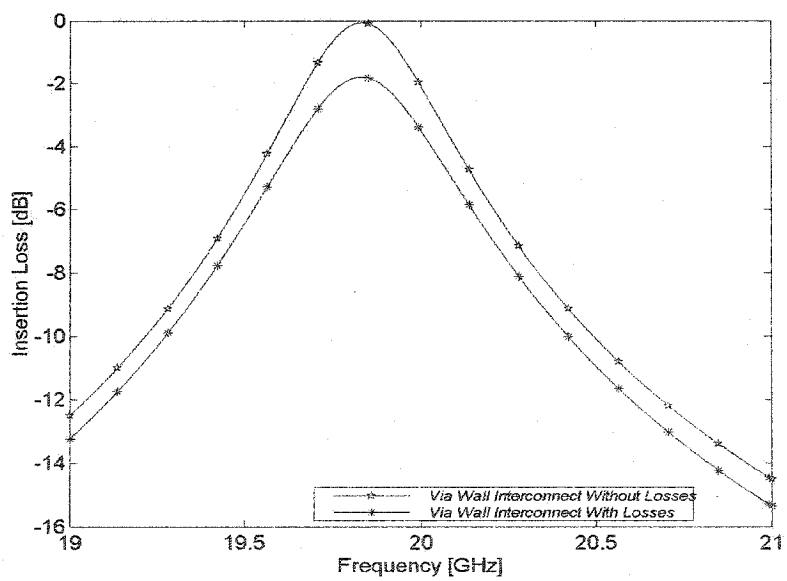

Figure 31: Insertion Loss vs. Frequency for a Via Wall Cavity Interconnect with Losses

3.5.4 The Effect of Coupling Slot Size (h And w)

Varying the coupling slot size reveals interesting properties that a designer can use in the creation of the vertical interconnect microwave or millimeter wave circuits. With all other parameters being constant and no losses included, the simulation results are shown in Figures 32 and 33.

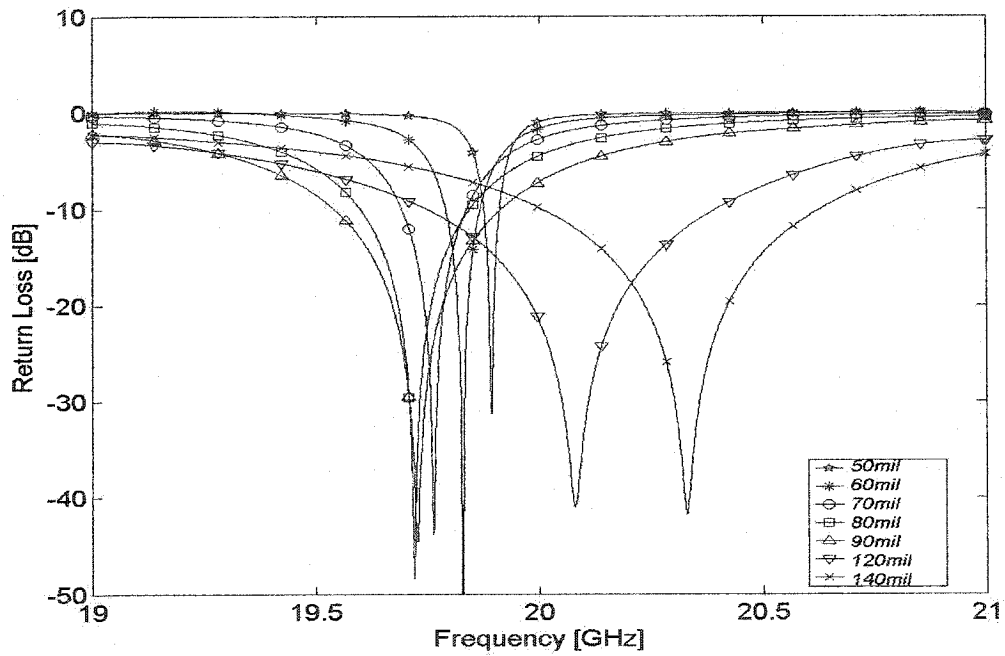

Figure 32: Return Loss vs. Frequency for a Via Walled Interconnect where Aperture Length is a Parameter

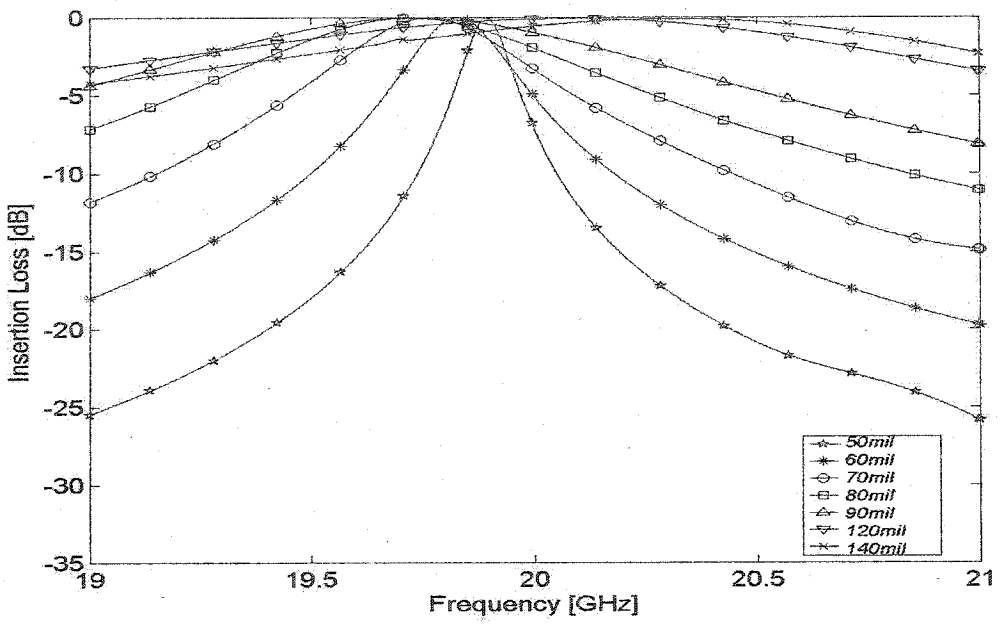

Figure 33: Insertion Loss vs. Frequency for a Via Walled Interconnect where Aperture Length, h, is a Parameter

Next, the width of the coupling slot is varied, ***w***, keeping all other parameters at their optimum design values, including the open circuit stub length. The slot is kept at ***v*** = 50 mil from the center of the cavity to the center of the aperture. The above exercise reveals that slot length increases both coupling and bandwidth. The centre frequency of the response changes, however, not very much. On the other hand, changes in aperture width are directly related to changes in frequency of the response. Very little changes in bandwidth are observed. This observation is also supported by Pozar in [24], where slot dimensions have been analyzed in the frequency selective surfaces using coupled microstrip patches and [25] where an aperture coupled cavity antenna was analyzed. Therefore, as a general rule, larger coupling slots exhibit wider bandwidth.

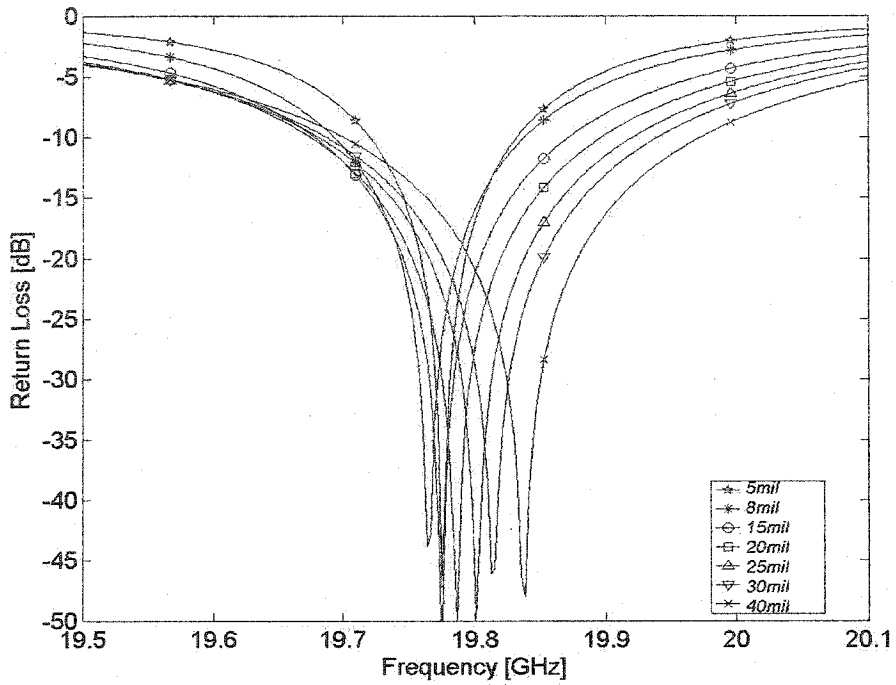

Figure 34: Return Loss vs. Frequency where Aperture Width is a Parameter

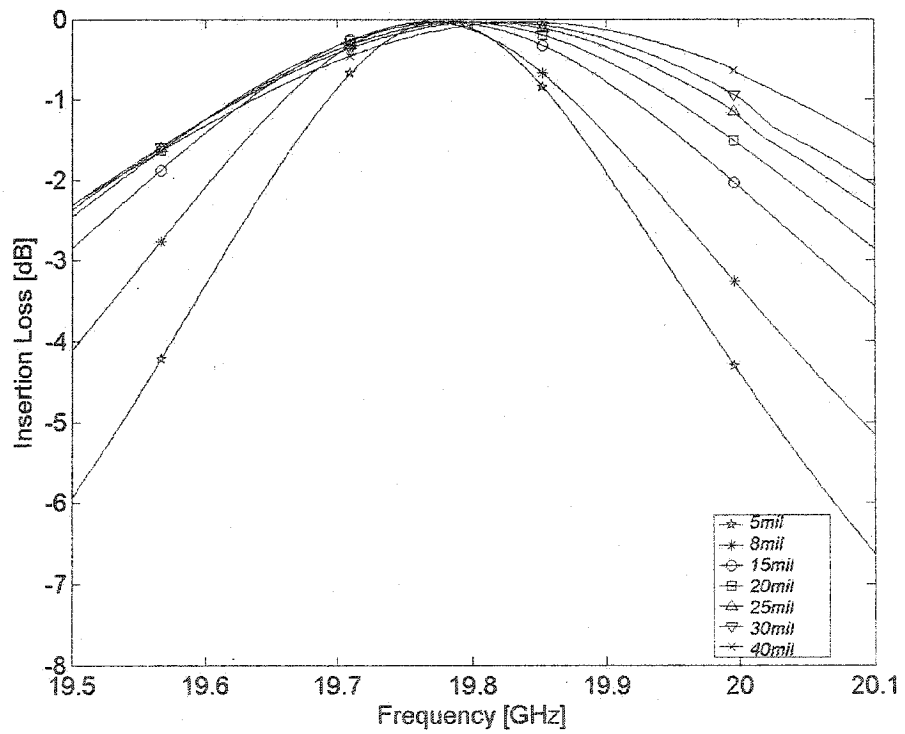

Figure 35: Insertion Loss vs. Frequency where Aperture Width is a Parameter

3.5.5 The Effects of the Open Circuited Stub Length (g)

During the optimization process, one also varies the open circuit stub length to obtain the best circuit performance. It is then of interest to see what happens as the stub length is changed and all other parameters are kept at their optimum values.

As shown in Figures 36 and 37, the amount of coupling is also controlled by the open circuit stub, as pointed out in [26]. An optimum design results in the maximum energy coupling in and out of the cavity. This is when the slot resonance and the cavity resonance are as close to one another as possible. The small shift in centre frequency is due to the change in the overall complex impedance that the circuit presents at the input, i.e. open circuit stub in series with a complex load representing the aperture.

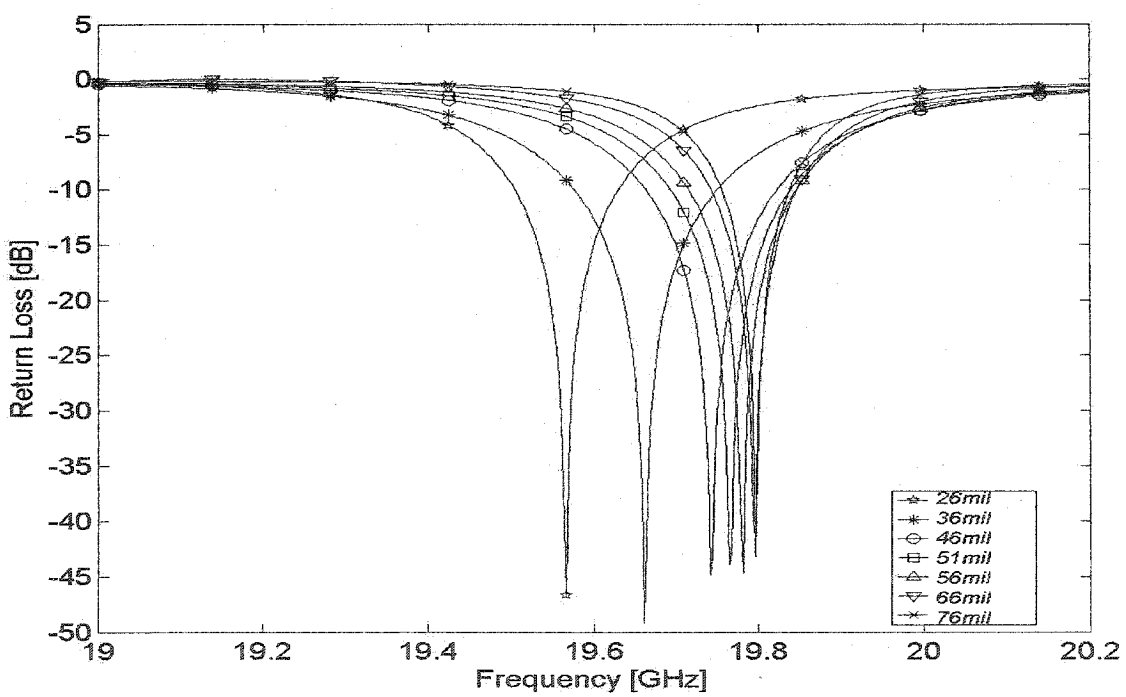

Figure 36: Return Loss vs. Frequency for the Via Walled Interconnect where the Open Circuit Stub Length, g, is a Parameter

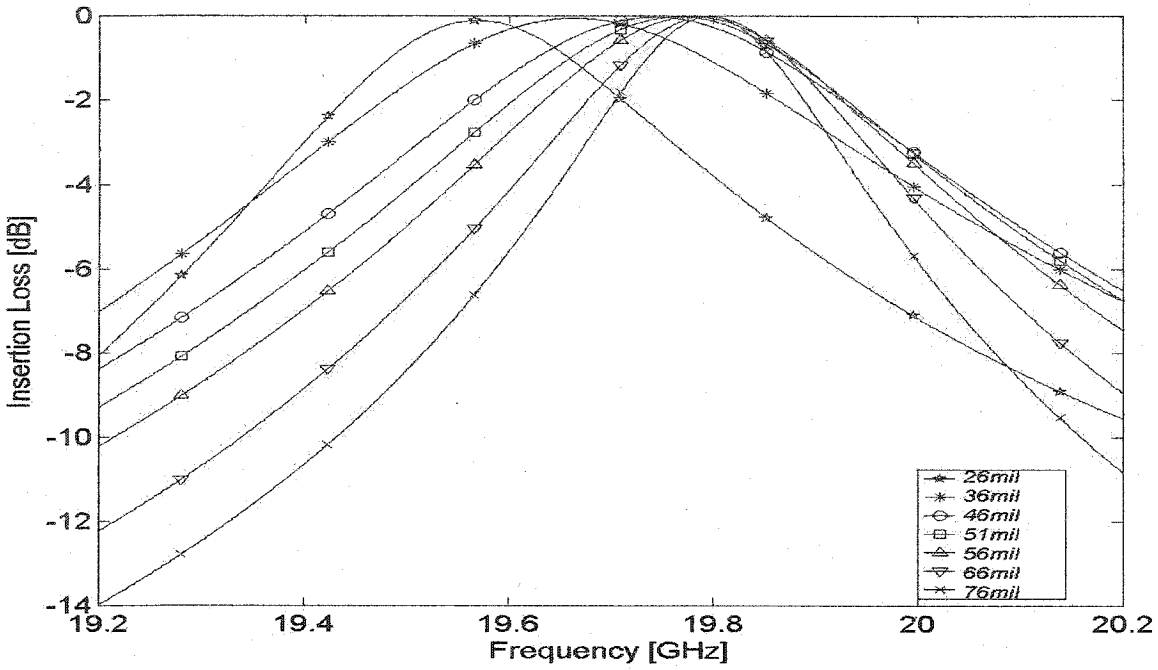

Figure 37: Insertion Loss for the Via Walled Interconnect where the Open Circuit Stub Length, g, is a Parameter

3.5.6 The Effect of the Interconnect Height, *b*

In Section 3.4.1 of this chapter, the resonant frequency formulation was given for the lowest order unloaded cavity mode, TE_{101}. Since the vertical dimension does not enter the calculation, it would appear that dimension ***b*** can be of any value as long as it satisfies ***b*** < ***a***. It is worth performing simulations on the optimized via wall cavity to see if that is indeed the case.

As it turns out, the vertical interconnect performs as expected as long as ***b*** < ***a***, i.e. there is almost no frequency shift in the response. This gives an RF designer a lot of flexibility, as there seem to be very little restriction on this dimension. As well, any manufacturing tolerances or temperature expansions that would change the vertical dimension will not cause any performance degradation. Once the vertical dimension approaches or extends passed the dimension ***a***, there is likely to be another mode present in the cavity, i.e. TE_{101} may not be the lowest order mode, and the frequency response degrades and shifts more noticeably.

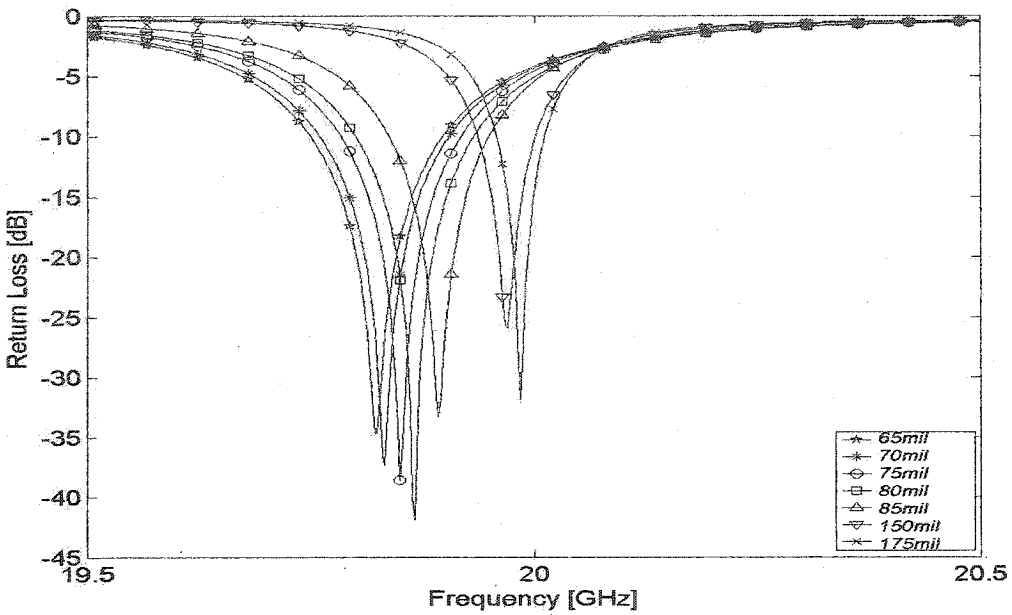

Figure 38: Return Loss vs. Frequency for the Via Walled Interconnect where the Vertical Transition Distance is a Parameter

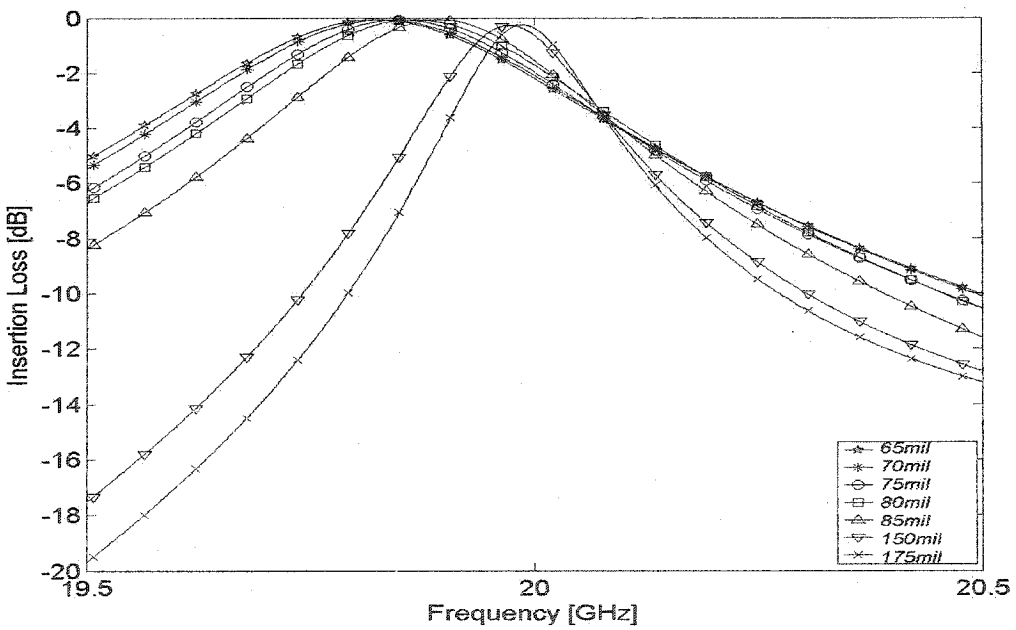

Figure 39: Insertion Loss vs. Frequency for the Via Walled Interconnect where the Vertical Transition Distance is a Parameter

3.5.7 Insight Gained

This first design was made to establish a benchmark and gain a better understanding of how this type of circuit works. It was found that the impedance bandwidth is very small, on the order of 0.5 %. This factor alone renders this vertical interconnect from being useful in the intended applications. However, it serves well in the understanding of the various physical circuit dimensions.

In general, the size of the coupling slot has a direct impact on the overall bandwidth of the vertical transition. Extending slot length increases bandwidth where as increasing slot width shifts the response in frequency. This behaviour is supported by Pozar in [24-25] where slot coupling microwave structures are considered.

Open circuit stub also controls the amount of energy coupling to and from the cavity, as pointed out in [26]. Small shifts in centre frequency are expected since changing the stub creates different complex load impedance transferred to the input. It is important to optimize it for best performance.

Finally, the circuit performance does not seem to be sensitive to changes in the vertical distance, ***b***. This might seem obvious when one considers that this dimension does not enter in the determination of the resonant frequency for an unloaded rectangular cavity resonator. It would then suggest, that this dimension is not sensitive to manufacturing tolerances or temperature variations resulting in different vertical dimension. This, unfortunately, may not always be the case, as demonstrated in Section 3.6.

3.6 DESIGN OF A VERTICAL INTERCONNECT WITH A VIA-WALLED RECTANGULAR CAVITY: APPLICATION #2

3.6.1 Present Aims

The knowledge gained in Section 3.5 can now be applied to an improved vertical interconnect design where much larger impedance bandwidth is to be obtained. Also, in the effort to consider manufacturing tolerances, presented in Section 3.7, the rectangular cavity can be

designed better to remove the performance sensitivity to manufacturing tolerances placed on the cavity dimension, ***d***.

3.6.2 Basic Design

Although the first design was quite useful in demonstrating several important concepts that a designer can use in creating vertical interconnects, the overall impedance bandwidth was unfortunately very small. In order to fulfill the bandwidth requirement of 3 % to 5 %, a new design is required.

In the analysis of the first design, it was determined that the size of the coupling aperture determines the amount of energy coupled in and out of the cavity. In particular, the length of the slot, ***h***, seems to increase the impedance bandwidth more than the width of the slot, ***w***. Therefore, the natural step forward is to design an interconnect such that a large slot can be implemented.

It was demonstrated in Section 3.5 that the coupling slots may be positioned along either sides of the cavity, namely ***a*** or ***d***. Also, the resonant frequency of the unloaded cavity for the TE_{101} mode is sensitive to slight variations in ***a*** or ***d*** when these dimensions are similar in size, much like the first design. This poses a problem when manufacturing tolerances are taken into consideration. In order to address this issue and still ensure TE_{101} cavity mode, one can make dimension ***d*** much larger than ***a***. This will result in a cavity design that will not be sensitive to changes in ***d***, but only in ***a***, and it will allow for much longer coupling slots which ultimately should enhance impedance bandwidth.

With these facts in mind, equation (2) was used to obtain new cavity dimensions. The design of the microstrip lines, vertical dimension, ***b***, and dielectric material used remain the same as in the first design. The only changes made are to the ***a*** and ***d*** dimensions of the cavity, and coupling aperture configuration.

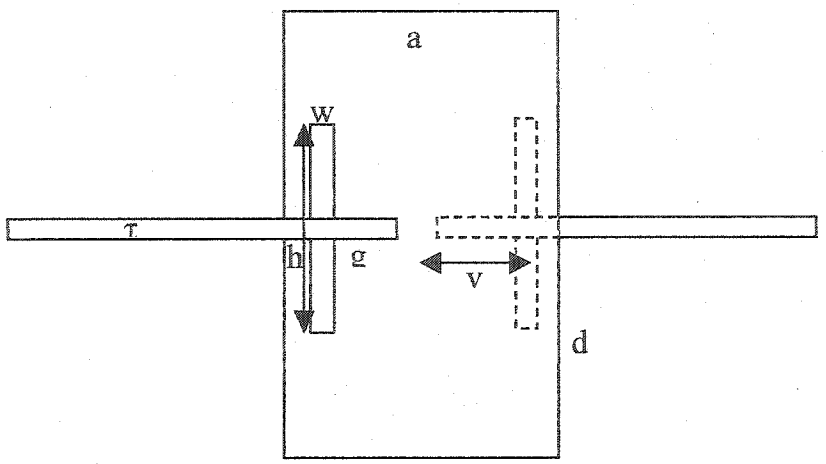

Figure 40: Top View of the Improved Solid Wall Cavity Interconnect Design

The chosen dimensions for the solid wall cavity are ***a*** = 115.7 mil and ***d*** = 380 mil. Once again, simulations were performed to optimize the above design. Optimum performance was achieved for ***h*** = 180 mils, ***w*** = 10mils, ***g*** = 81 mils, and a distance from the slot centerline to the cavity centerline ***v*** = 30 mils. The simulation results for a lossless configuration were obtained using both HFSS and Ensemble modeling tools.

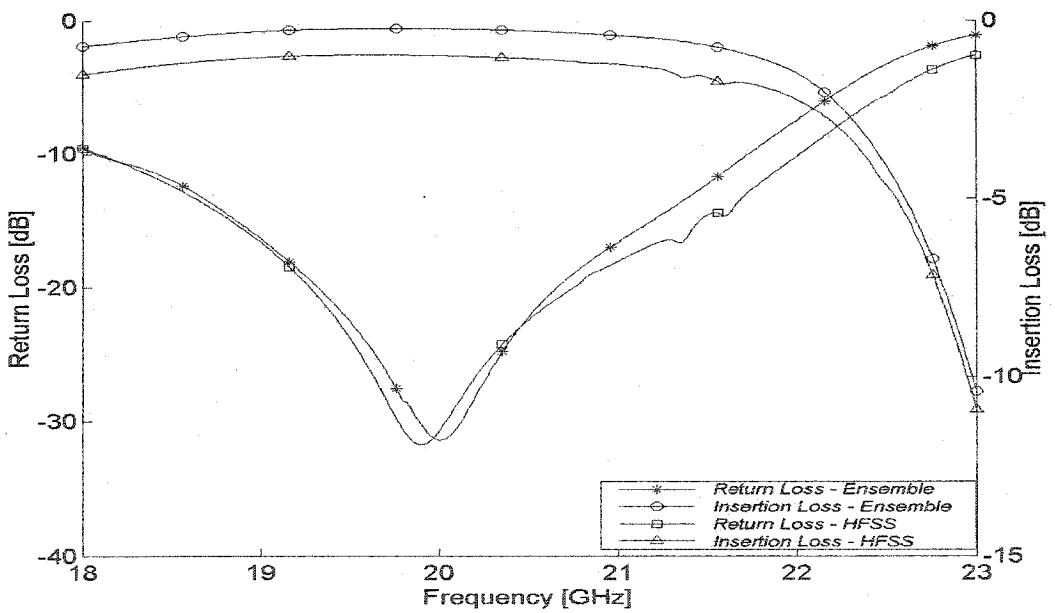

Figure 41: Simulation Results of the Improved Solid Wall Rectangular Cavity Interconnect

With impedance bandwidth criteria of S_{11} < -10dB and S_{21} > -2.5dB for a lossless configuration, bandwidth of about 18 % is achieved. This result is highly desirable, as requirements of 3 % to 6 % can be easily met, allowing for manufacturing tolerances.

Also, a good agreement is obtained between both methods despite their very different approaches to solve for electromagnetic fields, as described in Appendix B. However, a difference of about 1dB can be seen in the insertion loss between the finite element method (employed by HFSS) and the method of moments (employed by Ensemble). This may possibly be attributed to the numerical approximations as well as problem setup differences between the tools that include port definition where rectangular waveguide is used in HFSS to launch the electromagnetic wave. This waveguide is setup by the user. In contrast, the incident field in Ensemble is predetermined by the tool and can not be altered. Finally, Ensemble uses infinite ground planes and substrate layers to solve for electromagnetic fields whereas HFSS uses finite size structures enclosed in a radiating box where absorbing boundary conditions are applied. These differences all contribute to the small differences in the results.

Next, to complete the design, dimensions ***a*** and ***d***, obtained from the solid wall cavity considerations, must each be increased by an amount $(2t)^2 / 0.95p$, and the center of the vias then be placed along the boundary contour of the enlarged cavity. In order to structure the process, vias are placed at each corner and the remaining vias are then inserted in such a way as to achieve $2t/p \approx 0.5$ as closely as possible.

In the present example ***2t*** = 10 mils, ***a*** = 120.96 mils and ***d*** = 385.26 mils. The pitch ***p*** is 20.16 mils along the wall of dimension ***a***, and 20.27 mils along the wall of dimension ***d***. In order to include dielectric and conductor losses, conductivity of $\sigma = 5.8 \times 10^7$ S/m and a loss tangent for the dielectric material of $\tan\delta = 0.0025$ are used, same as in the case of the first interconnect design of Section 3.5. No changes were made to the slot-related dimensions.

As in the case of the first design, losses contribute to performance degradation of about 2 to 2.5 dB, as shown in Figure 42. Once again, the impedance bandwidth of the improved design is well within the requirement, allowing for further degradation made due to manufacturing tolerances.

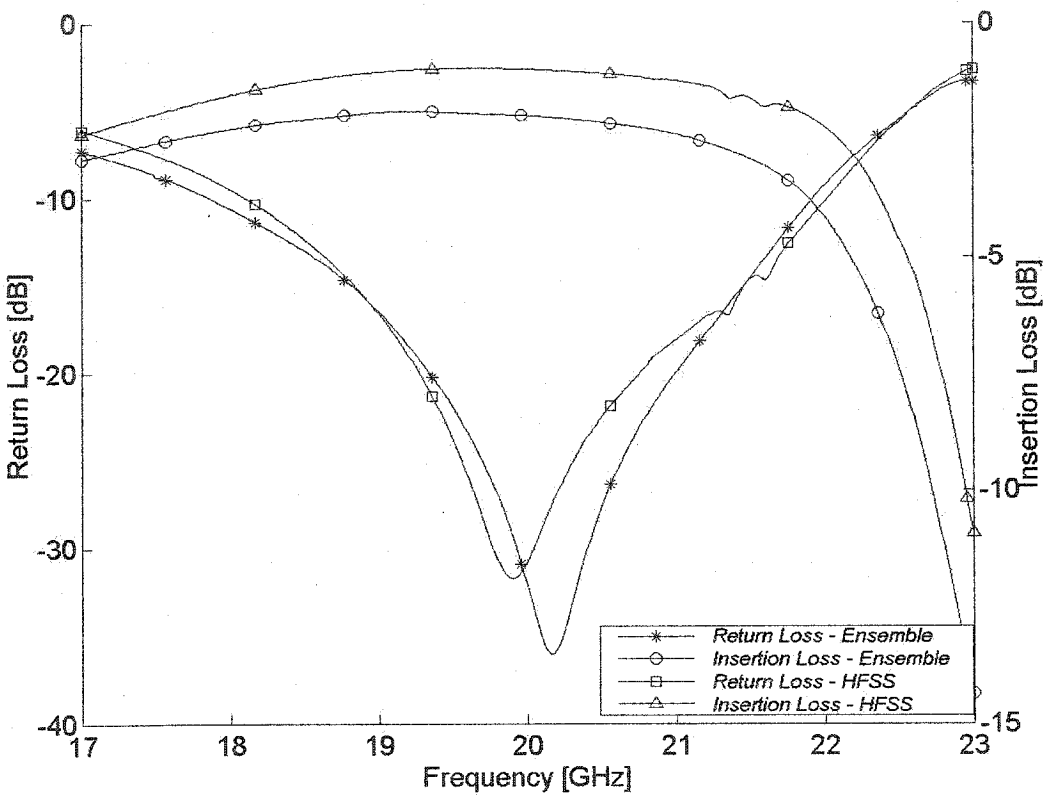

Figure 42: Computed Results of the Improved Via Wall Rectangular Cavity Interconnect

To further depict whether conductor or dielectric losses are dominant, the optimum design was once again simulated with the individual losses included separately in the circuit.

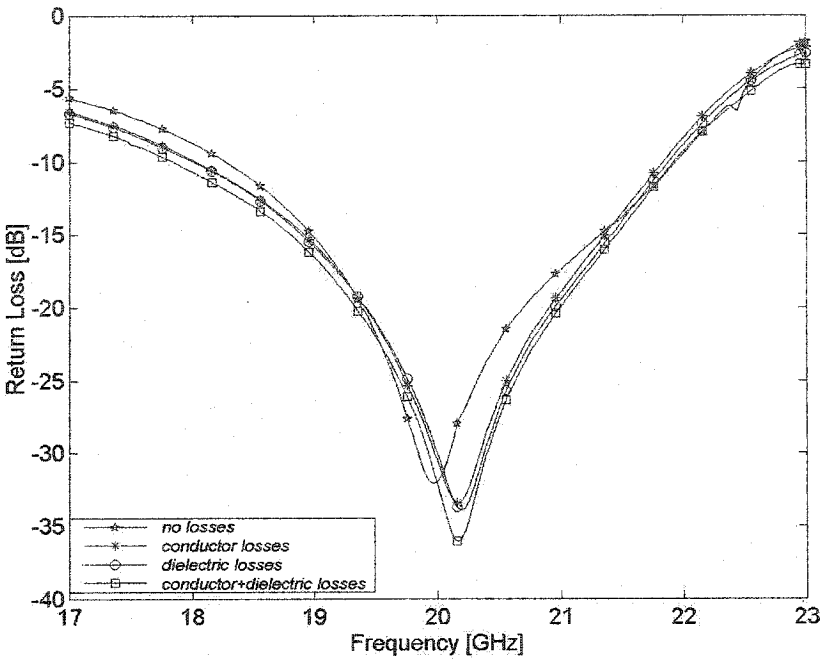

Figure 43: Return Loss of the Via Walled Interconnect when Losses are Under Consideration

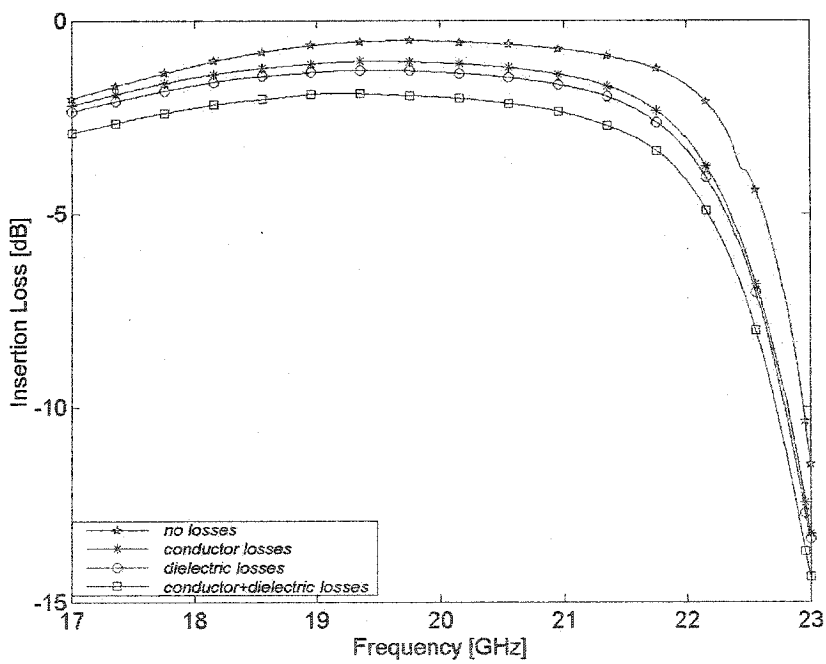

Figure 44: Insertion Loss of the Via Walled Interconnect when Losses are Under Consideration

Both losses appear to contribute equally although insertion loss shows dielectric loss to be slightly more dominant. This is expected as the electromagnetic energy is predominantly passed through the dielectric media of the vertical interconnect rather than the conducting vias. This is particularly true as vertical transitions using metallic vias as a means of transferring energy were proven unsuccessful in Chapter 2.

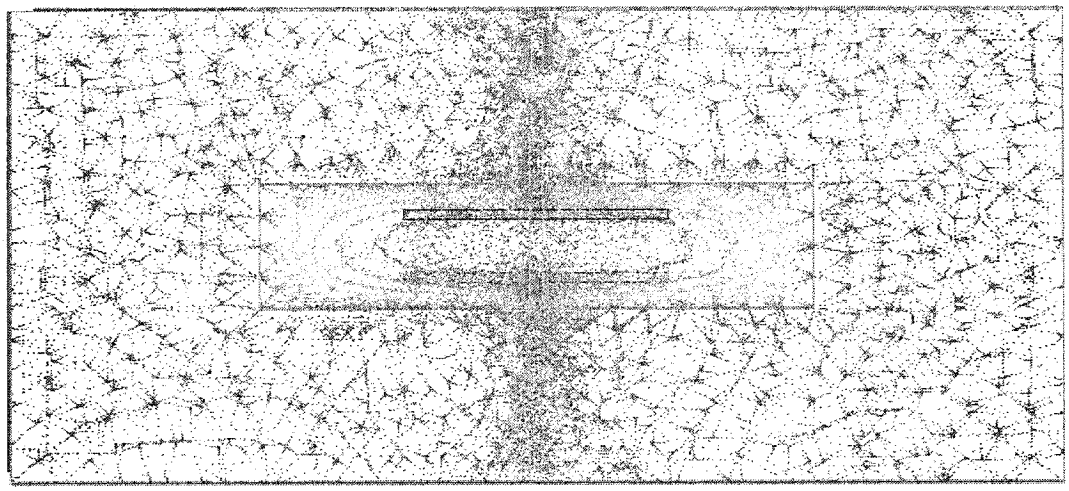

Figure 45: Magnitude of the Electric Field Distribution of the Solid Walled Cavity Interconnect

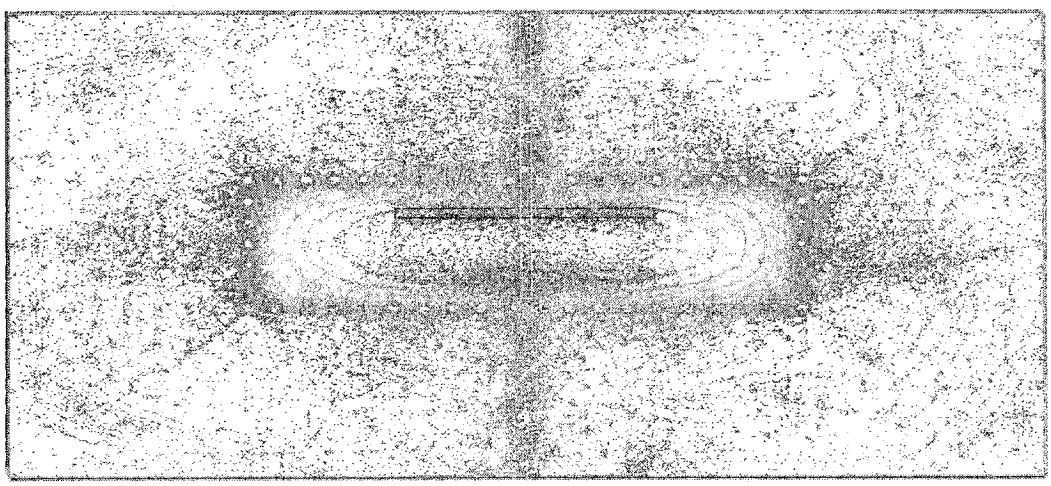

Figure 46: Magnitude of the Electric Field Distribution of the Via Walled Cavity Interconnect

Figures 45 and 46 show the energy flow through the vertical interconnect circuit, solid cavity walled and via walled cavities, respectively. More dense shading indicates stronger field presence where as darker regions show very weak presence of the electric field. It is clear that as energy enters the cavity, the dielectric media is used as a means to carry energy from one side of the cavity to the other. The via wall is there to limit energy leaks. It is evident that the less space is left between each via, the better insertion loss performance can be achieved, i.e. closer to the performance of the solid walled cavity interconnect. Therefore, dielectric losses are more dominant, but still allow for a good vertical interconnect circuit to be made.

In the next sections, the effect of parameter variations on the overall performance of the vertical interconnect is analyzed. This is done to show that some generalizations made in the first design may not entirely be applicable to the improved vertical transition microwave circuit.

3.6.3 The Effect of Slot Size (h And w)

Keeping all other parameters constant, coupling slot length was varied to understand the effects on the circuit performance. The via walled configuration was used without conductor and dielectric losses.

As shown in Figures 47 and 48, the length of the coupling slot allows for energy to be coupled more or less effectively, depending on its size. In the case of the first design, it seems as though making the length as large as possible would result in larger bandwidth. Unfortunately, this is not the case here. Clearly, there is an optimum slot length where the impedance bandwidth is largest. This occurs when the slot resonance and the cavity resonance take place at the same frequency thus resulting in maximum energy transfer. Any other configuration provides complex impedance that is resonant at different frequencies resulting in a worse response. Lastly, various slot lengths produce responses that are shifted in frequency. This is more pronounced only when the dimension is changed drastically, i.e. small changes in slot length do not result in vast changes of the frequency response, as was observed in the first design depicted in Section 3.5.

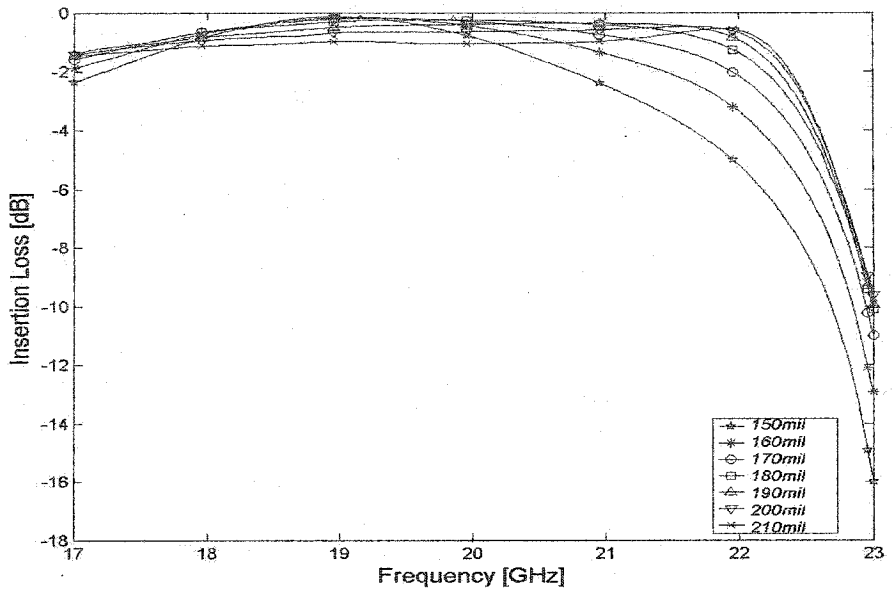

Figure 47: Insertion Loss of the Via Walled Interconnect where the Coupling Slot Length, h, is a Parameter

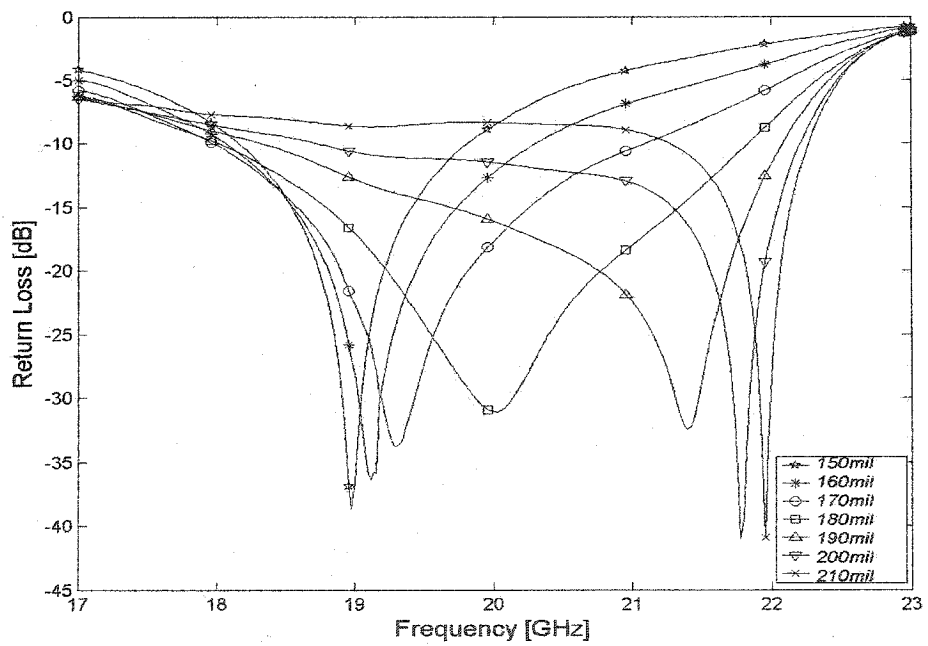

Figure 48: Return Loss of the Via Walled Interconnect where the Coupling Slot Length, h, is a Parameter

Next, the coupling aperture slot width, ***w***, is varied and its effect noted in the Figures 49 and 50.

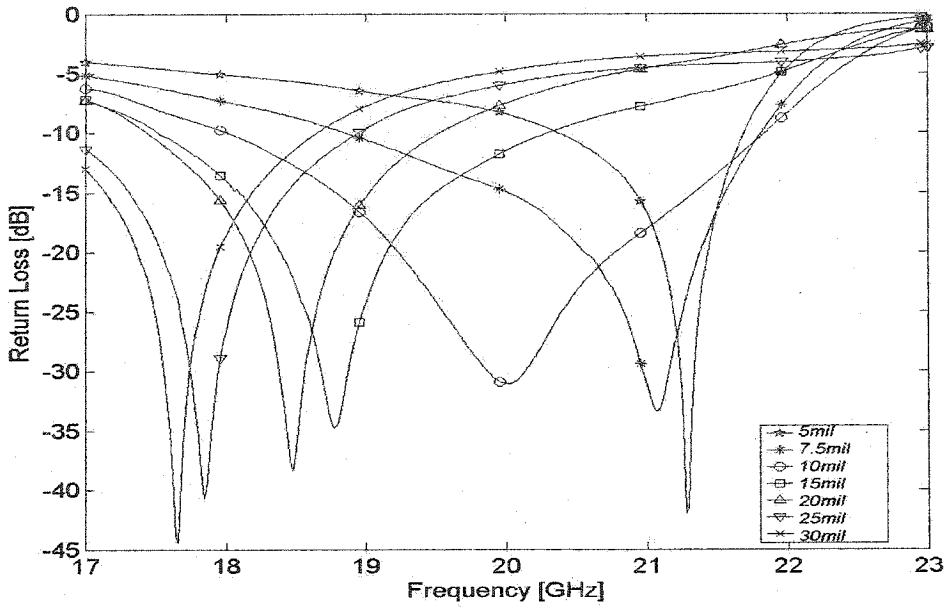

Figure 49: Return Loss of the Via Walled Interconnect where the Coupling Slot Width, w, is a Parameter

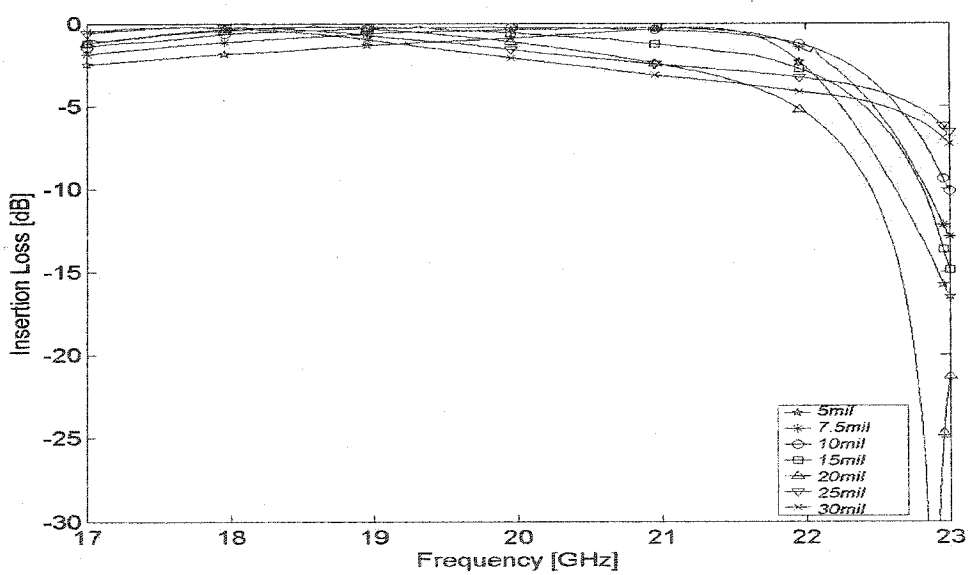

Figure 50: Insertion Loss of the Via Walled Interconnect where the Coupling Slot Width, w, is a Parameter

Small changes in the aperture width produce relatively large changes in the centre frequency response. This observation is also supported by Pozar in [24], where slot dimensions have been analyzed in the frequency selective surfaces using coupled microstrip patches and [25] where aperture coupled cavity antenna was analyzed. However, much like the variations in the slot length, changes in the aperture width also give rise to different values of impedance bandwidth. This is expected, as resonant behaviour is altered every time the circuit parameter is changed.

3.6.4 The Effect of the Open Circuit Stub Length, *g*

Much like the case of the first design, the open circuit stub controls the amount of energy coupling in and out of the cavity, as explained in Section 3.5. A designer needs to optimize it for best performance, starting with a length of $\lambda_g/4$. For completeness of this analysis, the open circuit stub length is varied and the simulation results are presented in Figures 51 and 52.

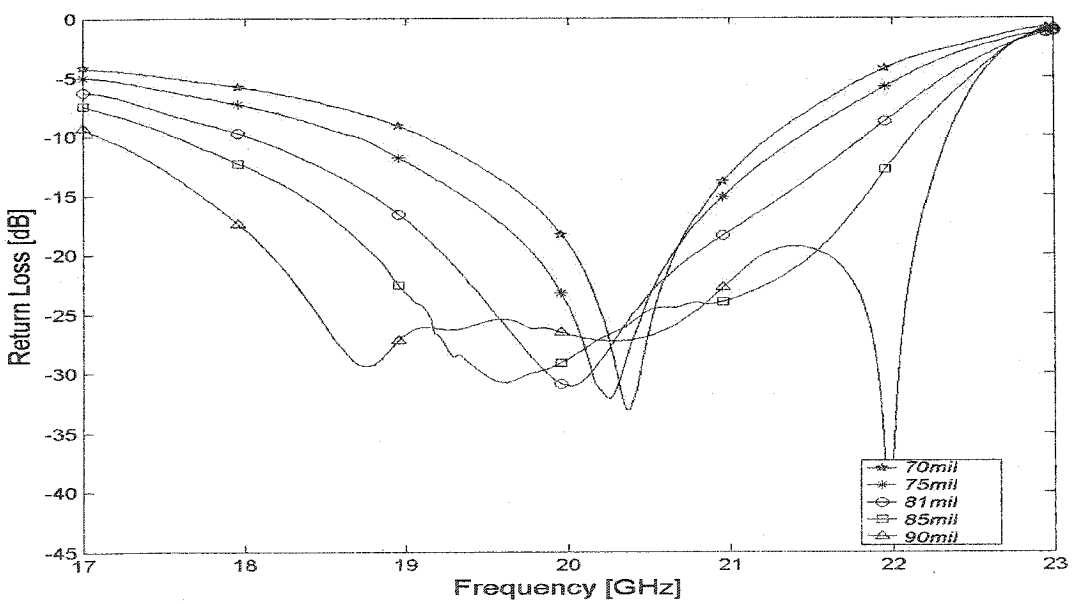

Figure 51: Return Loss of the Via Walled Interconnect where the Open Circuit Stub Length, g, is a Parameter

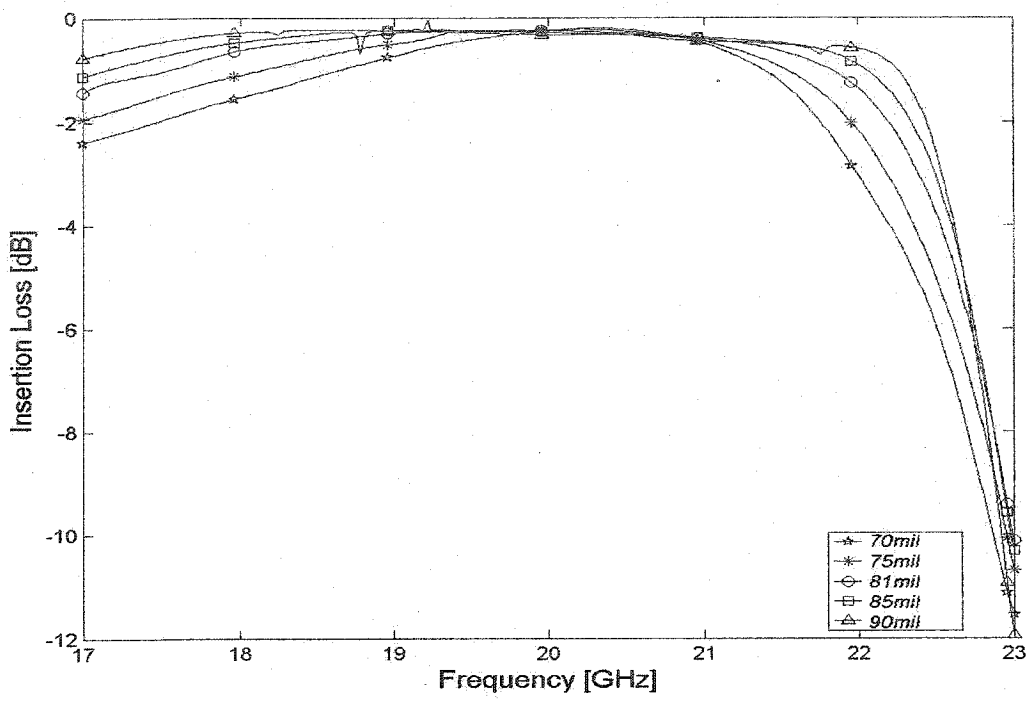

Figure 52: Insertion Loss of the Via Walled Interconnect where the Open Circuit Stub Length, g, is a Parameter

3.6.5 The Effect of the Cavity Height, *b*

Last parameter worth analyzing at this time is the vertical dimension, ***b***. Unlike the first design which showed no performance degradation with changes to dimension ***b*** as long as ***b*** < ***a***, this design results in frequency shifts up to 1 GHz, as shown in Figures 53 and 54. This clearly indicates that even though the unloaded cavity resonant behaviour is independent of the vertical dimension for the TE_{101} resonant mode of operation, the loaded band-pass filter changes its resonant behaviour with the vertical dimension. Also, once the vertical dimension approaches or exceeds the dimension ***a***, there is likely to be another mode present in the cavity. TE_{101} may not be the lowest order mode, and frequency response degrades to a point where the circuit is of no use.

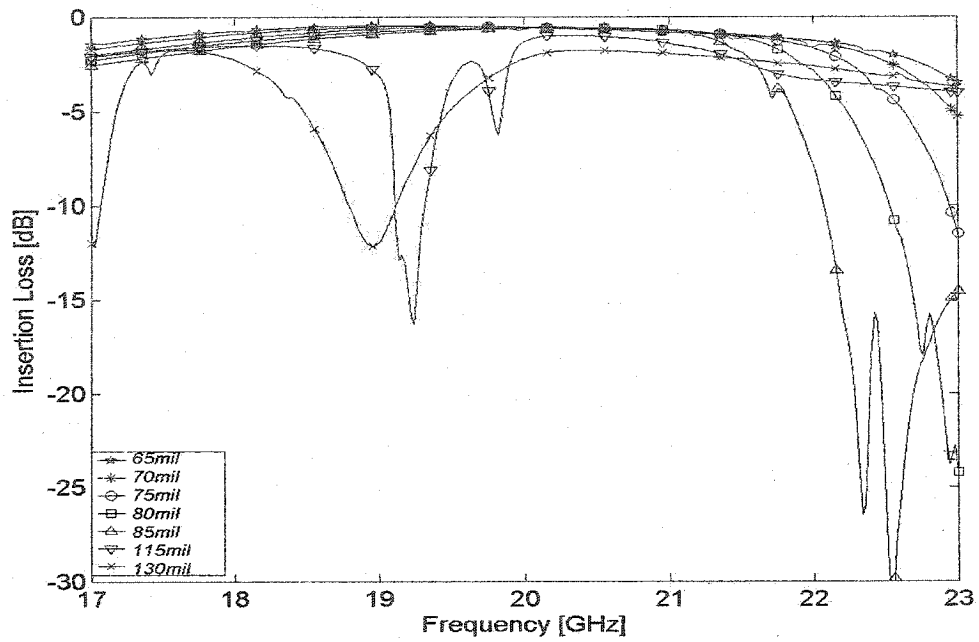

Figure 53: Insertion Loss of the Via Walled Interconnect where the Vertical Transition, b, is a Parameter

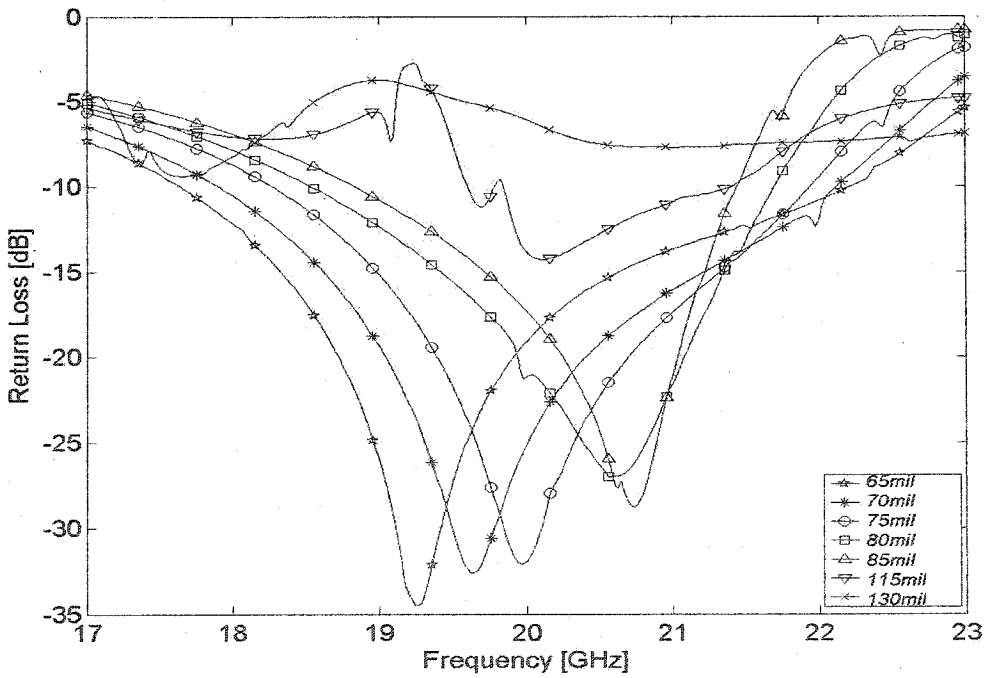

Figure 54: Return Loss of the Via Walled Interconnect where the Vertical Transition, b, is a Parameter

3.6.6 The Effect of the Diameter of the Vias Used to Form the Cavity Wall

The via diameter is yet another parameter which can be varied. The manufacturing design capabilities often set out minimum via dimensions for a specific vertical interconnect. For instance, Filtran Microcircuits Inc., [27], suggests aspect ratio of 10:1 as being the limit of what they can currently achieve. This means that the ratio of printed circuit board thickness to the via diameter is at most 10:1. For example, if the via diameter is 10 mil, the thickest board that one can use in the vertical transition is 100 mil. Anything beyond that can not be manufactured. So, if the vertical transition exceeds 100 mil, larger via must be used.

In Section 2.1 a single via was considered as a means to transfer energy vertically between two transmission lines. It was concluded that this type of vertical interconnect does not work well at microwave and millimeter wave frequencies. In fact, performance degrades rapidly not only with the increased vertical distance but also with larger via diameter.

It is then worth analyzing the optimum rectangular cavity design with fence walls constructed with vias of various diameters. Once again, in order to substitute solid cavity walls with via fence and obtain similar response to the optimum solid wall cavity interconnect design, the cavity is enlarged before vias are placed in accordance with design rules outlined in Section 3.4.4. The following Figures 55 and 56 show the simulated results for lossless vertical interconnects:

Clearly the proposed vertical interconnect operates very well at microwave frequencies. There is no restriction on how large via diameter needs to be. Because the electric field resides inside the cavity, the energy transfer is not directly reliant on the via walls. This adds flexibility to the design, allowing one to not only design vertical interconnects of various lengths but also to use less expensive manufacturing processes which might only allow for larger vias to be used.

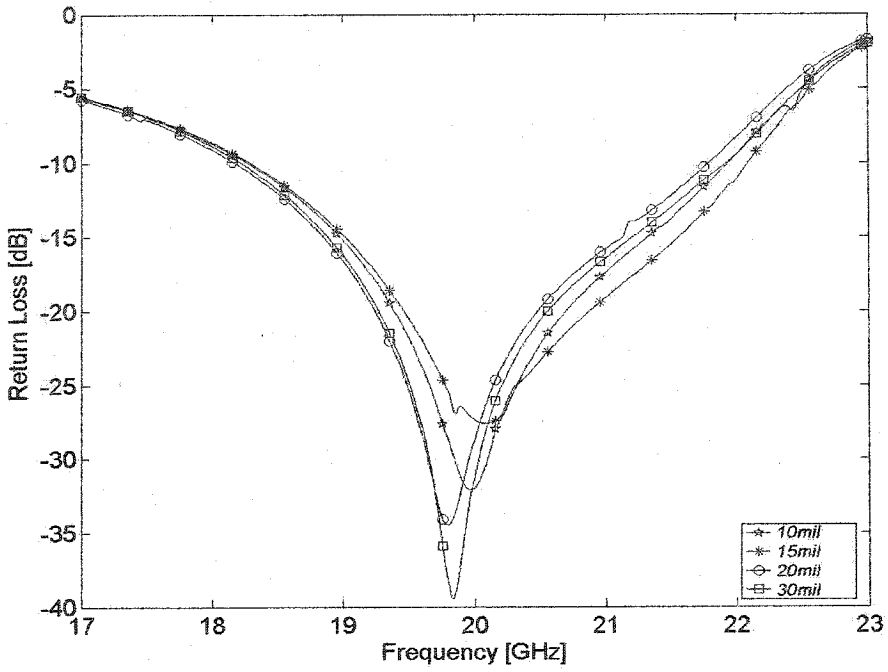

Figure 55: Return Loss of the Via Walled Interconnect where the Via Diameter is a Parameter

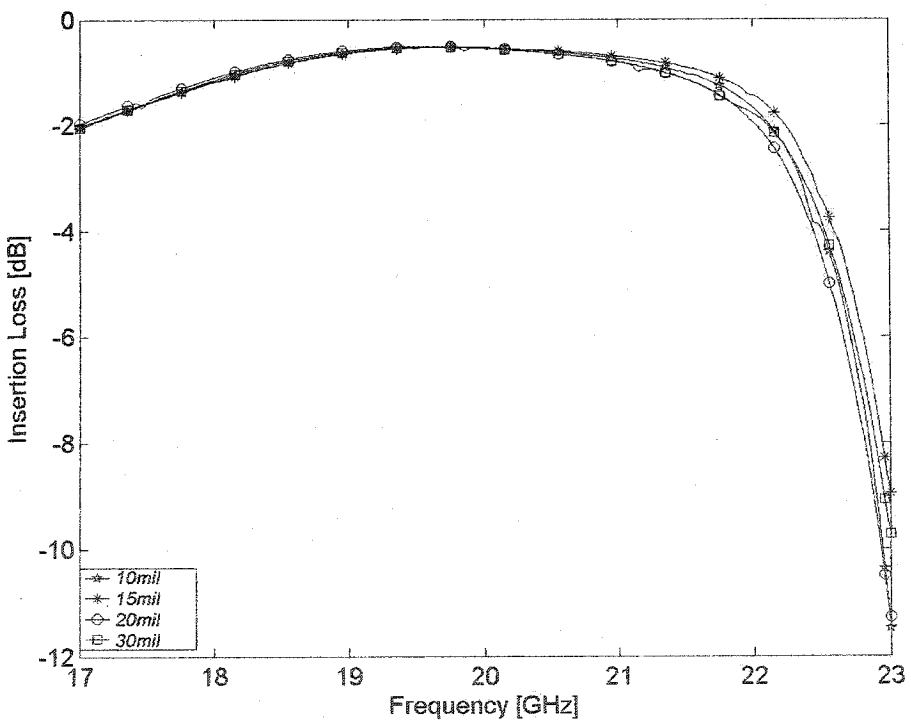

Figure 56: Insertion Loss of the Via Walled Interconnect where the Via Diameter is a Parameter

Finally, one can also use double wall cavities to potentially improve the performance of an interconnect circuit. For instance, when using large vias, the distance between the vias increases. This has a potential to result in a design where energy leaks out through the cavity walls and circuit performance degrades. To compensate for the excessive space between vias and still satisfy the manufacturing guidelines, one can place a second row of vias directly behind the original via wall, staggering each via. This concept is illustrated in Figure 57.

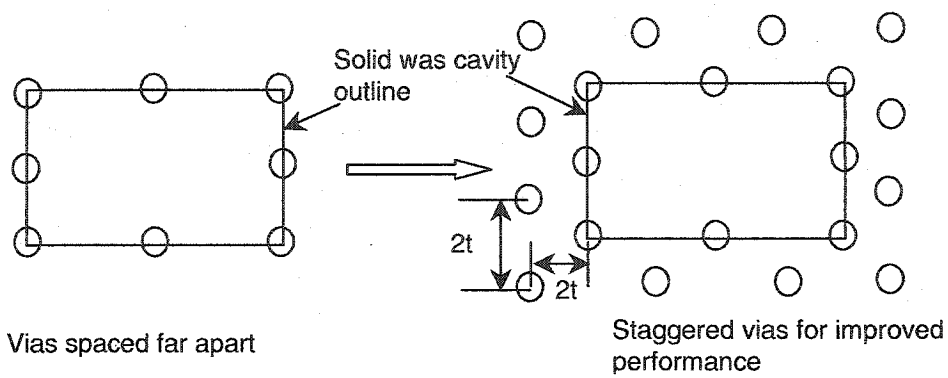

Figure 57: Top View of the Staggered Via Cavity Transformation

In order to simplify the design, one can space the second row of vias minimum distance of twice the via diameter away from the original via wall and have vias within a row spaced in the same manner, as shown in Figure 57. To illustrate this principle, a design was taken where vias of 30 mil in diameter were used. Using spacing of about 60 mil between adjacent vias and lossless configurations, the computed data is presented in Figures 58 and 59.

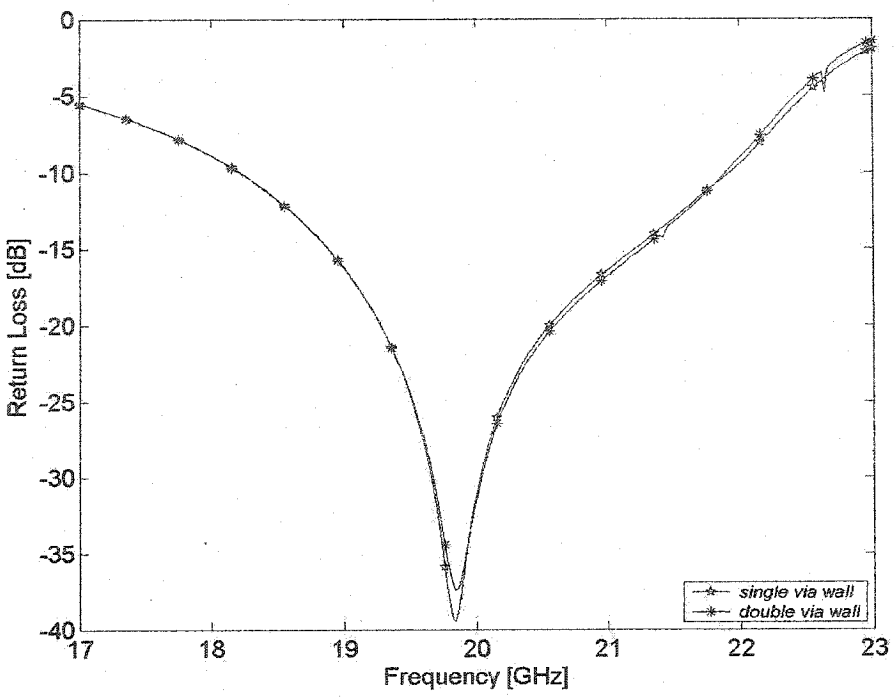

Figure 58: Return Loss of the Via Walled Interconnect where Single and Double Via Walled Cavities are Used

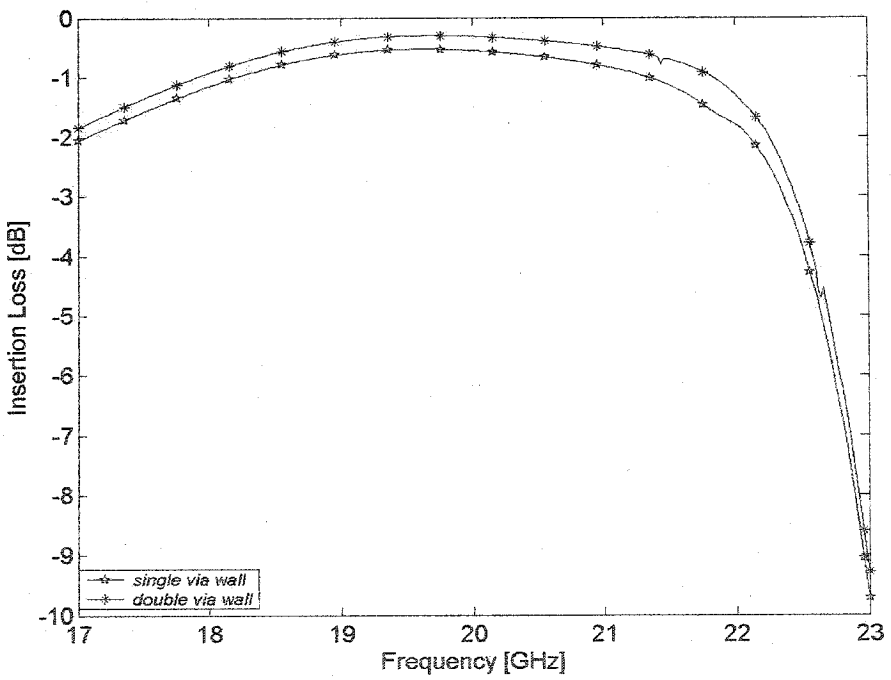

Figure 59: Insertion Loss of the Via Walled Interconnect where Single and Double Via Walled Cavities are Used

The improvement is seen in the insertion loss data. Clearly, this is due to the fact that the electromagnetic field is confined more in the cavity with when two via walls are used in the design. This also provides better isolation to adjacent circuits. The method of placing rows of vias to provide isolation has been extensively used, as demonstrated in [4-5]. Double via walls have also been used in the cavity filter designs, as shown in [11-13].

3.6.7 The Effect of Finite Thickness Ground planes and Microstrip Conductors

Until now, all analysis have been carried out with conductors of zero thickness. This includes both microstrip lines and ground planes. However, when circuits get built, all conductors are three dimensional having finite thickness that is often selected based on the current carrying capacity requirements. For most microwave circuits, 0.5 oz./sq. ft. conducting materials are used, i.e. the amount of conductor per square foot of a printed circuit board is 0.5 oz, as recommended by Filtran Microcircuits Inc. [27]. This translates to a thickness of 0.7 mil. With this new addition to the optimum design, HFSS simulation was performed to see the effect of the finite conductor thickness.

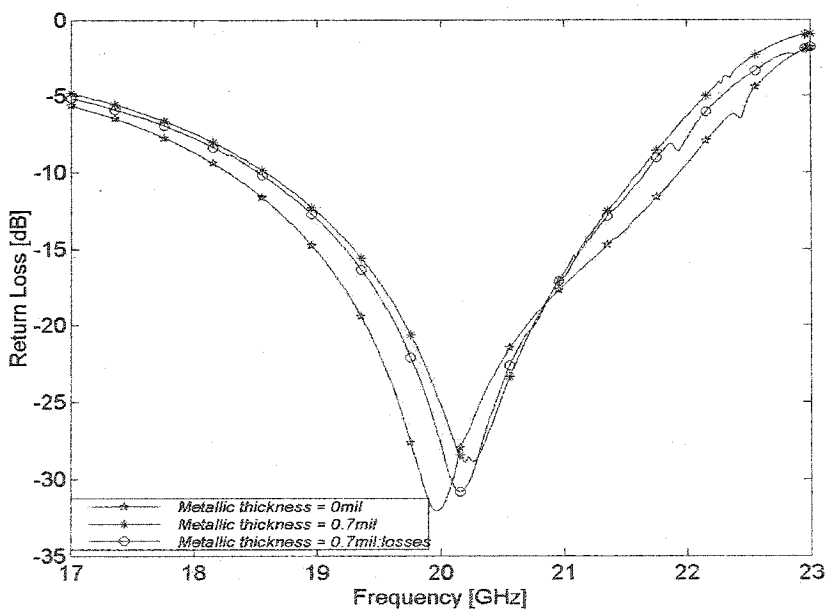

Figure 60: Return Loss of the Via Walled Interconnect where Finite Conductor Thickness is Used

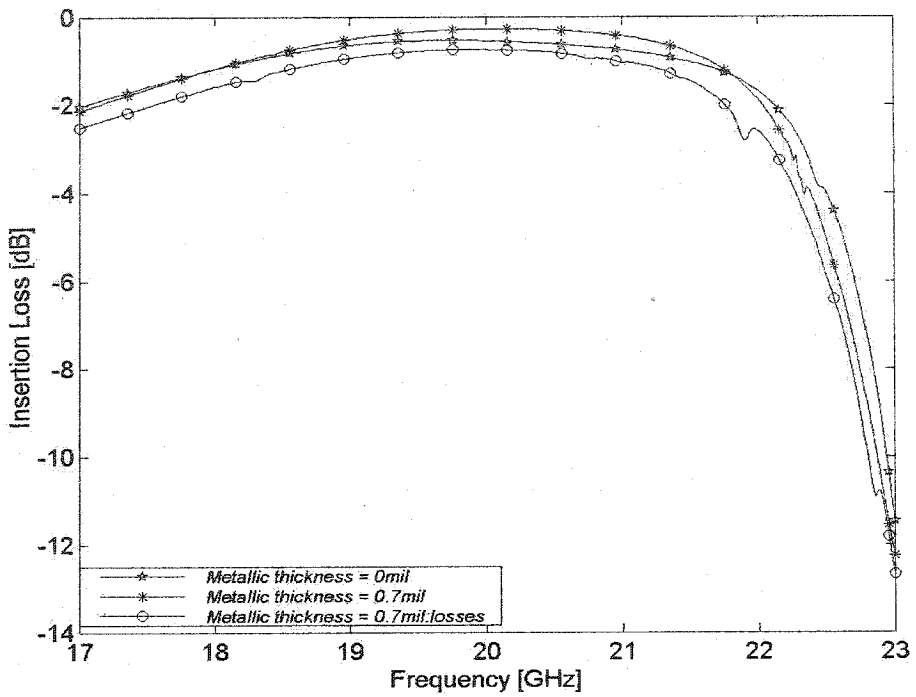

Figure 61: Insertion Loss of the Via Walled Interconnect where Finite Conductor Thickness is Used

Return loss indicates a bandwidth reduction of about 2 % when finite conductor thickness is included in the analysis. Insertion loss is unaffected by the added conductor thickness. Conductor and dielectric losses have negligible effect in this configuration on the circuit performance. Overall, the circuit performs very well and meets the original impedance bandwidth criteria of 3 to 5 %.

3.6.8 Review of the Complete Interconnect Design

This improved design was made to ensure that originally stated performance requirements can be met. Unlike the first design, where the impedance bandwidth was found to be in the order of 0.5 %, this design shows a bandwidth of about 18 %. This result allows for surface roughness, temperature expansion and manufacturing tolerances, elements which degrade performance for any microwave circuit.

Much like the first design, analysis was performed to see how the circuit performs when various parameters are changed.

In general, the size of the coupling slot has a direct impact on the overall bandwidth of the vertical transition. Both the slot length and width affect the performance of the circuit. There is an optimum set of values such that largest impedance bandwidth can be achieved. To a larger extend, lengthening the slot length increases bandwidth where as increasing slot width shifts the response in frequency more pronouncedly. This behaviour is supported by Pozar in [24-25] where slot coupling microwave structures are considered.

Open circuit stub length also controls the amount of energy coupling to and from the cavity, as pointed out in [26]. Centre frequency shifts are expected since changing the stub creates different complex load impedance transferred to the input. It is important to optimize it for best performance.

Also, the performance of the vertical transition does seem to be sensitive to changes in the vertical distance, ***b***. Unlike the first design which showed no performance degradation with changes to dimension ***b*** as long as ***b*** < ***a***, this design results in frequency shifts up to 1 GHz. This clearly indicates that even though the unloaded cavity resonant behaviour is independent of the vertical dimension for the TE_{101} mode of operation, the loaded band-pass filter changes its resonant behaviour with the vertical dimension. Also, once the vertical dimension approaches or exceeds the dimension ***a*** of the cavity, there is likely to be another mode present in the cavity, i.e. TE_{101} may not be the lowest order mode, and frequency response degrades to a point where the circuit is of no use.

Finally, finite conductor thickness has a small effect on the impedance bandwidth, on the order of about 2 %. This is not very significant as 16 % bandwidth vertical interconnect circuit easily meets original bandwidth requirement and allows for manufacturing tolerances.

3.7 THE EFFECTS OF MANUFACTURING TOLERANCES

3.7.1 Introductory Remarks

The previous section of this chapter has already dealt with parameter changes. These parameter changes contribute to altered circuit performance. In any microwave or millimeter wave designs, it is critical to be able to realize circuits with as little variation to the circuit dimensions as possible. Unfortunately, it is expected to have various dimensions altered from the optimized design parameters as manufacturing tolerances are unavoidable. It is therefore in the hands of a good designer to not only perform paper analysis and optimization, but also introduce parameter variations with accordance to specified manufacturing guidelines to see how the circuit will behave when parameter tolerances are introduced.

3.7.2 The Effect of Variations in Interconnect Cavity Dimensions, *a* & *d*

In this section we deal with manufacturing tolerances of the cavity dimensions, ***a*** and ***d***. Equation (2) clearly shows that the resonant frequency of an unloaded rectangular cavity operating in the TE_{101} mode strongly depends on the two cavity dimensions, ***a*** and ***d*** and has no dependence on the vertical dimension, ***b***. The optimum design presented here resulted in the dimension ***d*** being much greater than the dimension ***a***, still satisfying the condition for the TE_{101} mode, i.e. $a < d$ and $b < a$. This was done purposely to remove the sensitivity of parameter ***d*** changes which could quickly affect the resonant behaviour of the cavity. As a result, only small changes to dimension ***a*** make the cavity resonant response change swiftly. This, of course, is the theoretical analysis of the unloaded cavity. As presented in previous section, depending on the configuration of the vertical interconnect using rectangular cavity resulting circuit may in fact be sensitive to changes in the vertical dimension, ***b***. As this has already been analyzed, it is worth considering the remaining cavity dimensions. Before doing so, one needs to understand what these tolerances are so that unnecessary worries can be avoided. Reference [11], in Table I shows that a via hole positioning precision of $\pm$ 7.9 μm = $\pm$ 0.311 mil can be achieved. With a filter design operating at 20 GHz and built using a rectangular cavity made of vias, this accuracy translated to a operating frequency shift of $\pm$

201 MHz, as outlined in [11]. Also, the design guidelines of Filtran Microcircuits Inc. [27] indicate via hole accuracy of ± 0.5 mil and as high as ± 1.5 mil for less sensitive designs. This means that in the absolute worst case, the distance between two vias defining a particular cavity dimension can be changed by twice the accuracy of via placement.

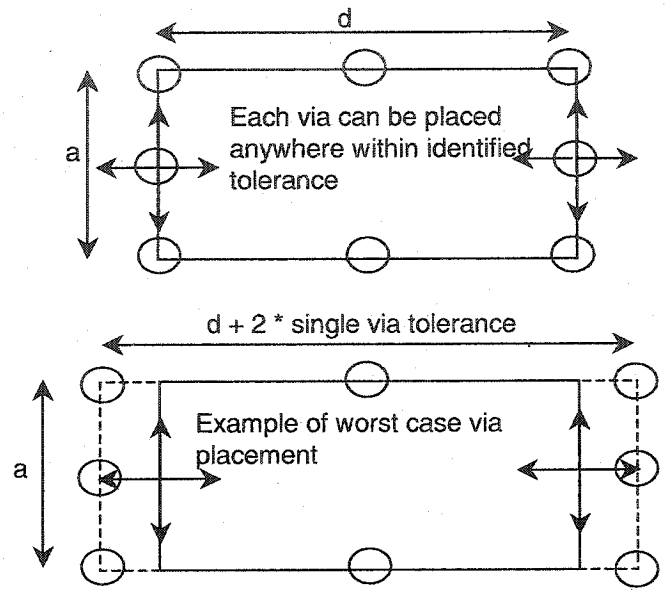

Figure 62: Pictorial Representation of Via Position Accuracy – Top View of the Cavity

It is the optimum via interconnect design that is used with no dielectric or conductor losses, and zero conductor thickness, as per Section 3.6. Analysis was carried out using HFSS.

A. The Influence of Cavity Dimension *d*

Manufacturing tolerances may result in the dimension *d* being smaller or larger at the extremes. It is therefore interesting to investigate both cases.

For the case where the via walled cavity is made smaller, the resonant behaviour is captured in Figures 63 and 64.

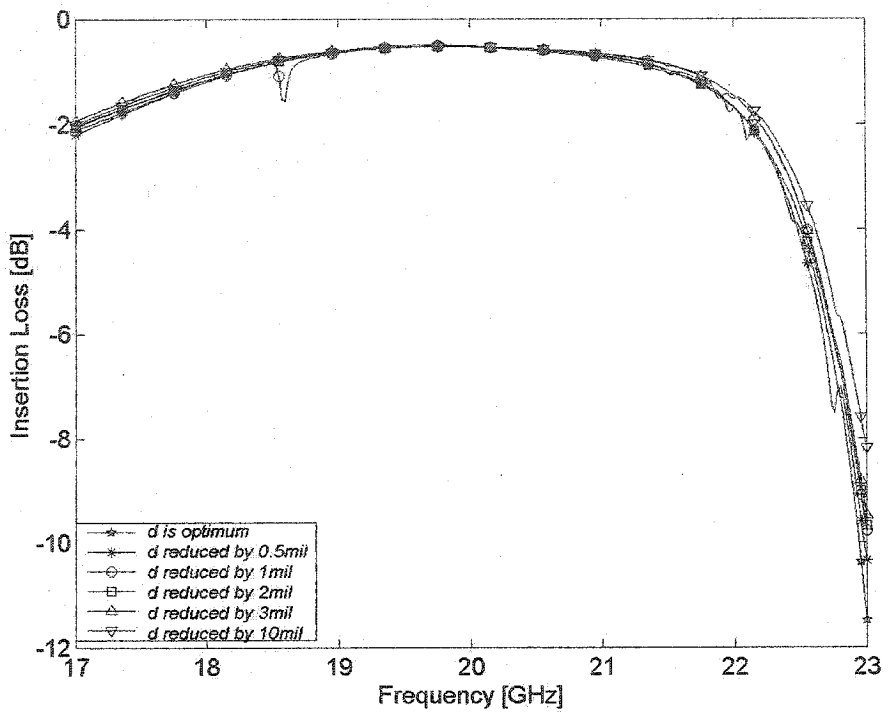

Figure 63: Return Loss of the Via Walled Interconnect where the Via Cavity Dimension, *d*, is Made Smaller

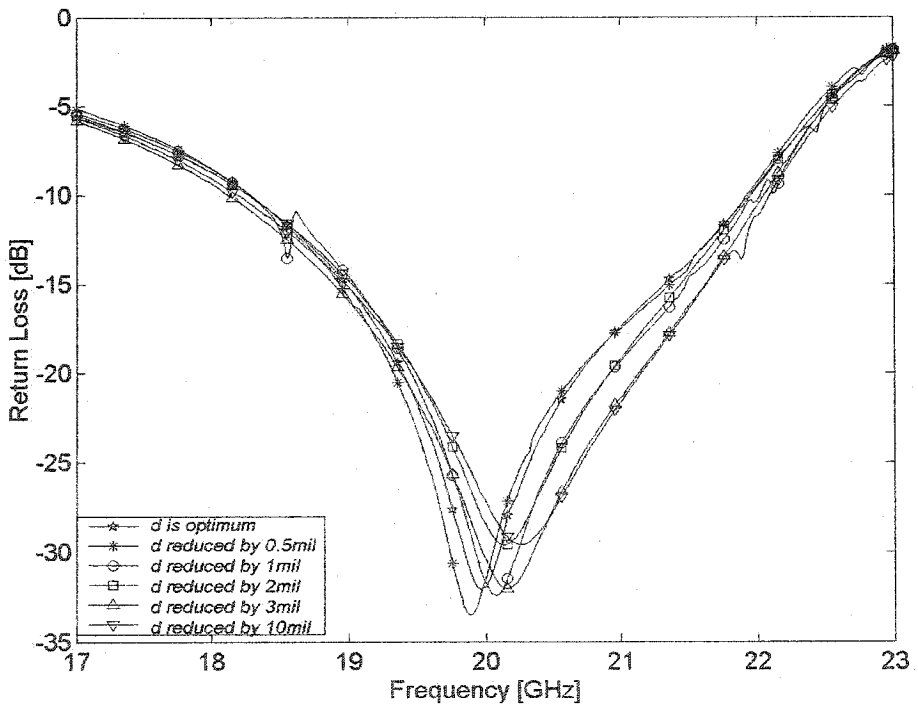

Figure 64: Insertion Loss of the Via Walled Interconnect where the Via Cavity Dimension, *d*, is Made Smaller

It is evident that moving via walls such that the overall dimension, ***d***, is reduced by as much as 10 mil, has no significant effect on the performance of the circuit. This stems from the analysis of Section 3.6 where making this dimension much larger than ***a*** would make this design less sensitive to manufacturing tolerances. One can also see this when observing the resonant frequency shift of an unloaded rectangular cavity with the changing dimension ***d***, using equation (2).

Next, via walls are extended out to increase overall dimension, ***d***.

Once again, any changes in the via cavity dimension, ***d***, result in insignificant changes in the circuit performance. This confirms that manufacturing tolerances do not diminish circuit performance when applied to this parameter.

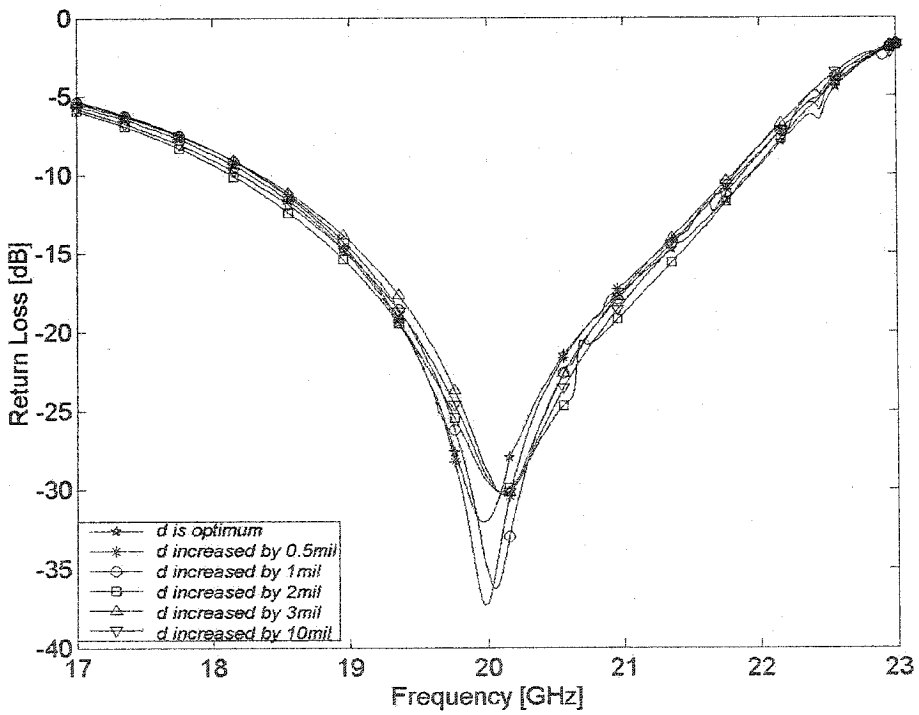

Figure 65: Return Loss of the Via Walled Interconnect where the Via Cavity Dimension, *d*, is Made Larger

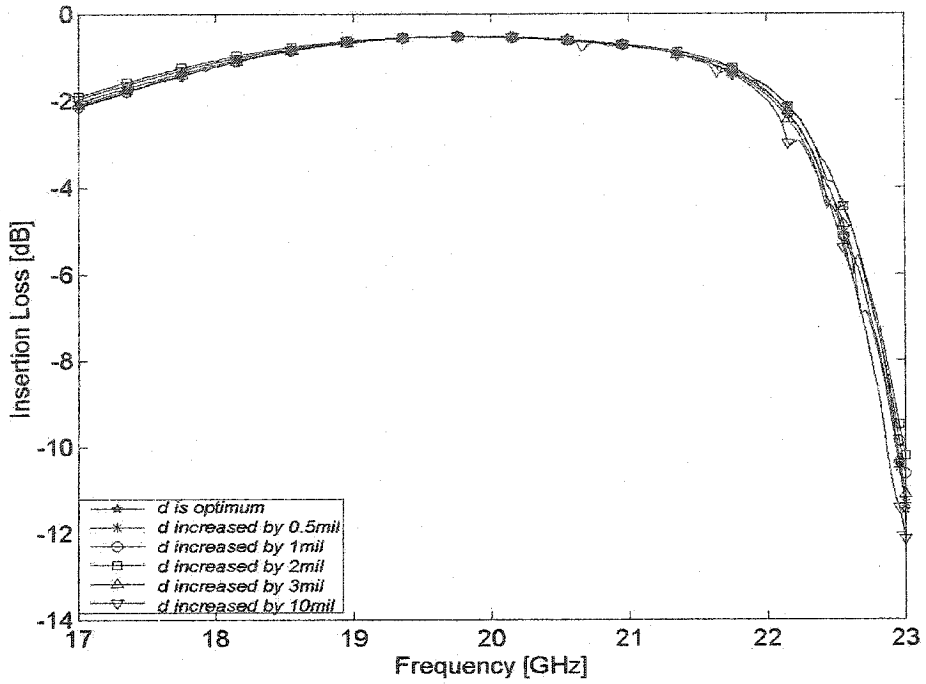

Figure 66: Insertion Loss of the Via Walled Interconnect where the Via Cavity Dimension, *d*, is Made Larger

B. The Influence of Cavity Dimension *a*

Unlike the ***d*** dimension of the via cavity, changes in this parameter are likely to affect the resonant frequency of the cavity. This can be seen by analyzing equation (2), where it is observed that the resonant frequency of an unloaded rectangular cavity operating in the TE_{101} mode is sensitive to the variations in the ***a*** parameter. Therefore, it is expected that in the design of a vertical interconnect similar behaviour will be obtained. The only uncertainty is how much of a disturbance would result when an optimally designed circuit was built with the tolerances stated previously. Much like the case of altering the ***d*** cavity dimension, this parameter can also be made smaller or larger in the extreme cases. Parameter resulting in smaller cavity is considered first. From equation (2) it follows that making ***a*** smaller will result in higher resonant frequency of an unloaded cavity. However, even at the extreme of 3 mil reduction in this parameter, the unloaded cavity predicts a frequency shift of about 0.5 GHz. Unfortunately, the vertical interconnect circuit gives rise to a centre frequency shift of about 2 GHz, limiting impedance bandwidth to about 10 %, as illustrated in Figures 67 and 68. This is still acceptable performance that easily meets the original bandwidth requirement of 5 %.

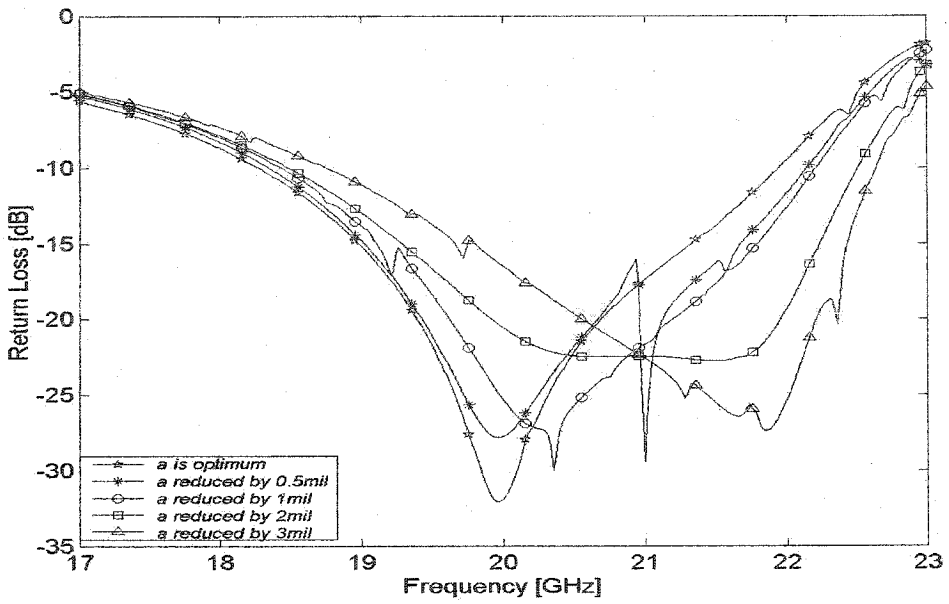

Figure 67: Return Loss of the Via Walled Interconnect where the Via Cavity Dimension, *a*, is Made Smaller

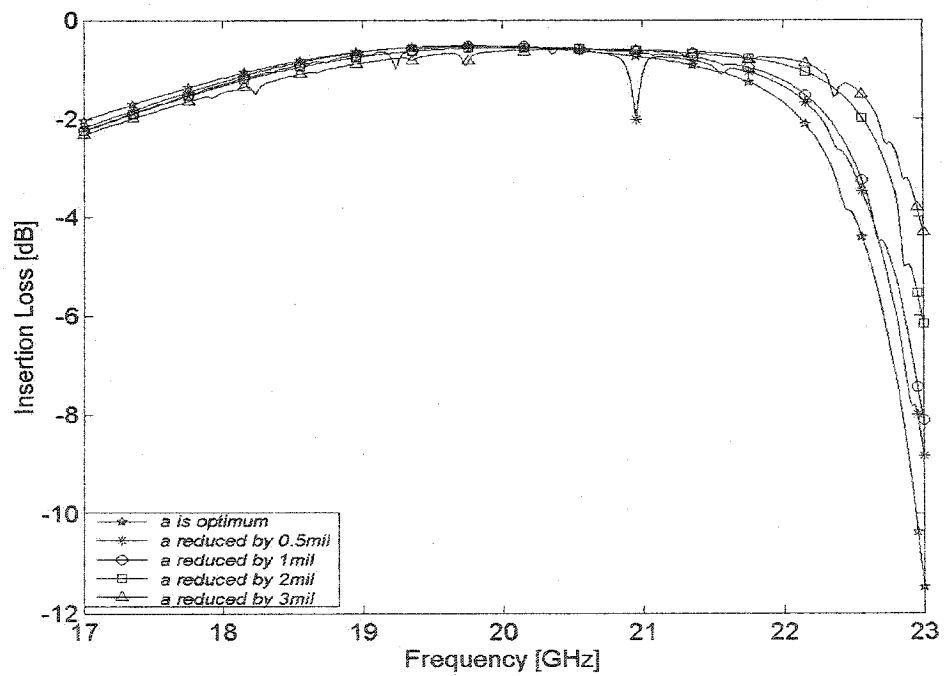

Figure 68: Insertion Loss of the Via Walled Interconnect where the Via Cavity Dimension, *a*, is Made Smaller

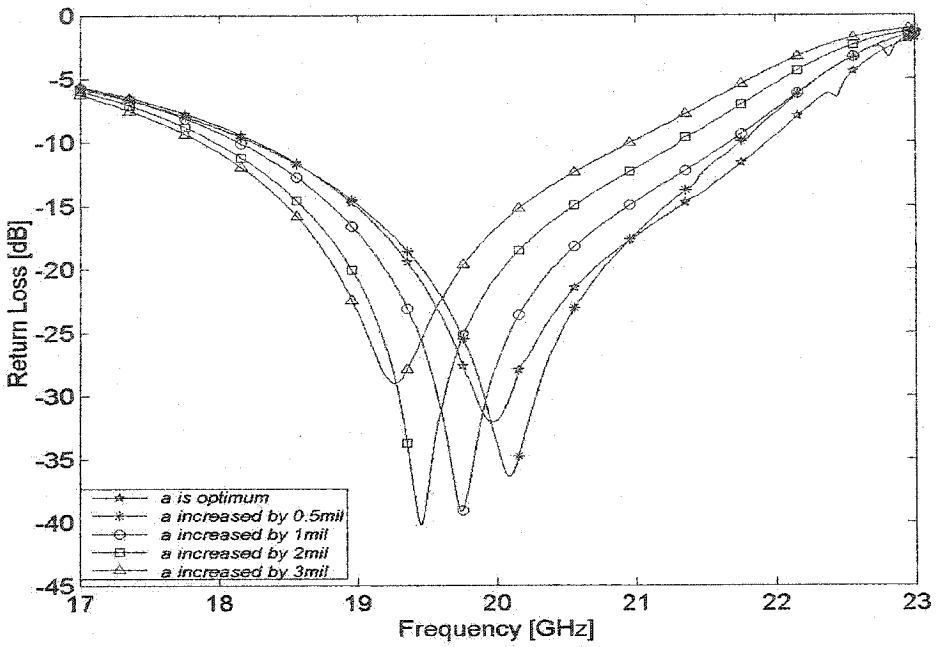

Figure 69: Return Loss of the Via Walled Interconnect where the Via Cavity Dimension, *a*, is Made Larger

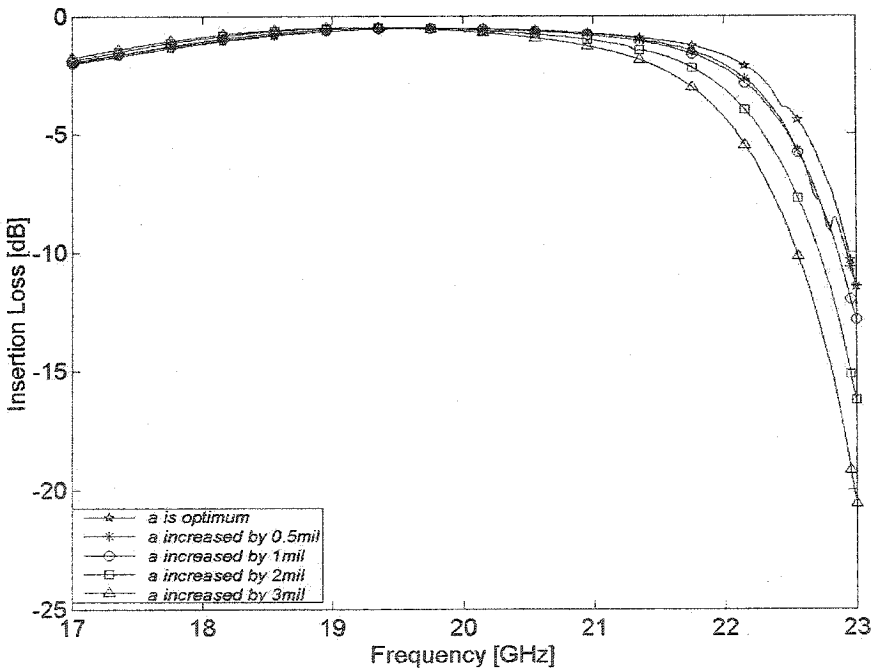

Figure 70: Insertion Loss of the Via Walled Interconnect where the Via Cavity Dimension, *a*, is Made Larger

The results of via cavity dimension, ***a***, made larger are shown in Figures 69 and 70.

Once again the bandwidth is limited by the response of the return loss. In the worst case of manufacturing tolerances, the impedance bandwidth is limited to about 8 %. However, if tolerances of ± 0.5 mil are applied, bandwidth of about 15 % is achievable with this design. Finally, larger cavity corresponds to a shift in the frequency response to a lower frequency band, as is the case of an unloaded resonant cavity.

3.7.3 The Effect of the Coupling Slot Location

In Section 3.6 analysis was carried out to better understand the effect aperture coupling slot dimensions, ***h*** and ***w***, have on the overall performance of the vertical interconnect circuit. One other aspect to consider is the accuracy with which these slots are placed relative to other objects, such as cavity walls, microstrip lines, as illustrated in Figure 71.

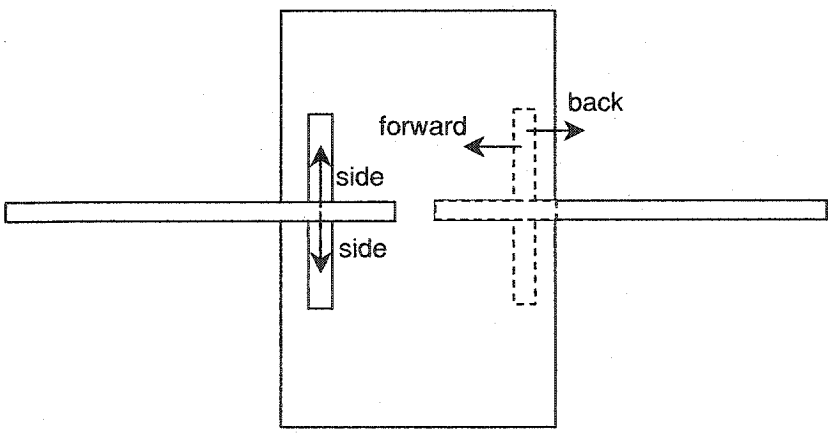

Figure 71: Coupling Aperture Slot Position Variation

Figure 71 introduces terminology that identifies the type of change in the configuration. The manufacturing accuracy to place slots where it is designed to be is the same as the one of placing objects, such as vias. Therefore, one can expect worst cases to be when both slots are shifted together backward or forward. The apertures can also be placed such that they are both shifted to one side or one slot is shifted to one side and the other will shift to the opposite side. There are many combinations and most of them are being looked at next. The optimum

via interconnect design is used with no dielectric or conductor losses, and zero conductor thickness, as per Section 3.6. Analysis was carried out using HFSS. Also, no other parameters are varied with the exception of the ones under consideration, depicted in Figures 72 and 73.

The circuit performance is noticeably affected when both slots are moved either forward or backward. This is because the optimum coupling set up by the open circuit stub was changed. As well, the slots were positioned in a new area where the current density distribution is different from what it was, i.e. the current is maximum at the edge of the horizontal cavity wall and it decreases to zero at the center of the cavity. In order to obtain better results, new open circuit stub length would have to be determined. This would likely result in a change in open circuit stub length which would be much different than 3 mil.

When the slots are placed to one side or opposite sides, circuit performance is not affected greatly because the current distribution on the cavity wall has not changed and the same, optimum open circuit stub still operates well to establish the best energy coupling.

Finally, it can also happen that only one of the two slots is moved from its optimum location and the second kept as per design guidelines. This is investigated in Figures 74 and 75.

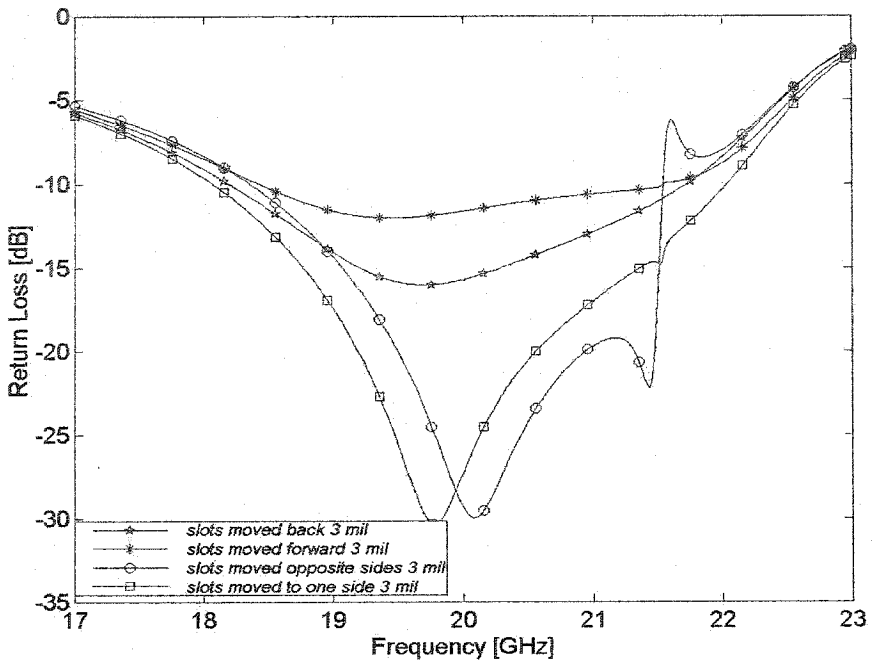

Figure 72: Return Loss of the Via Walled Interconnect where Both Coupling Slots are Moved in the Same Direction

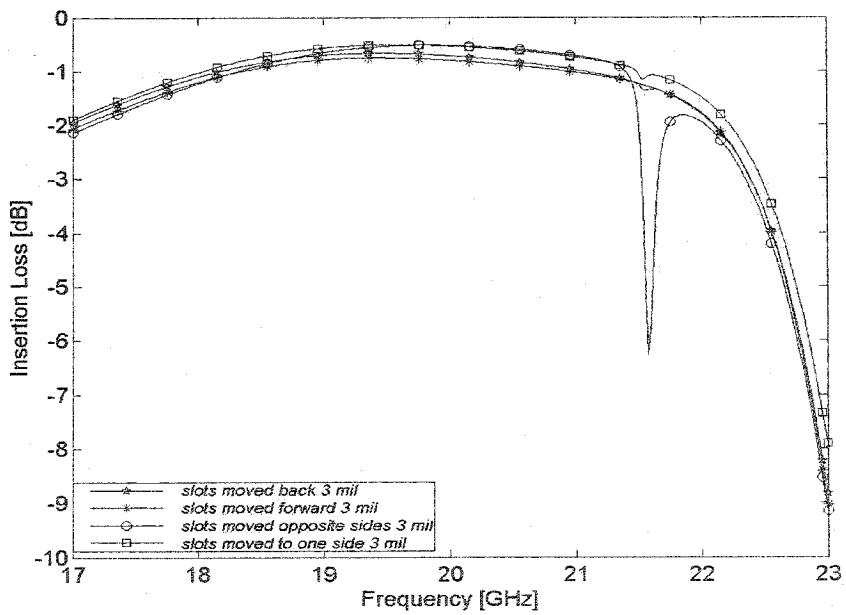

Figure 73: Insertion Loss of the Via Walled Interconnect where Both Slots are Moved in the Same Direction

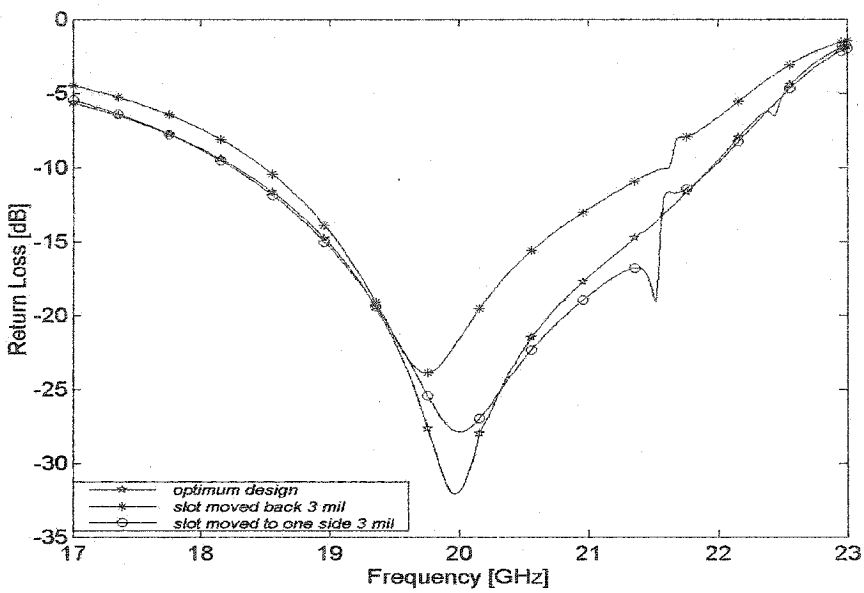

Figure 74: Return Loss of the Via Walled Interconnect where Only One Coupling Slot is Moved from Its Designed Location

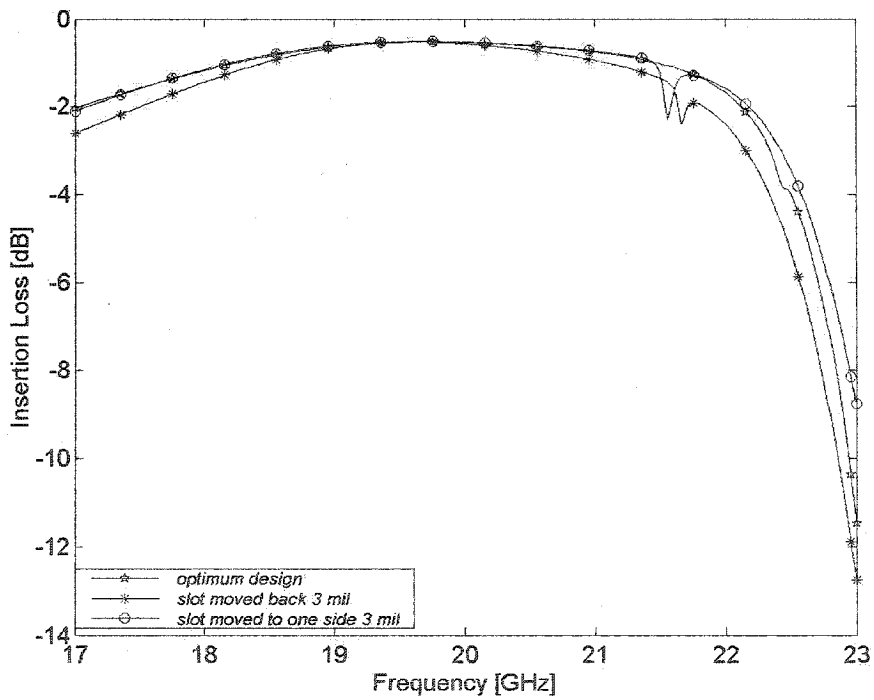

Figure 75: Insertion Loss of the Via Walled Interconnect where Only One Coupling Slot is Moved from Its Designed Location

The performance of the vertical interconnect circuit is not affected by manufacturing tolerances when only applied to one slot. This is clearly not the worst case. However, it is interesting to note that only the extreme parameter changes result in performance degradation.

3.7.4 The Effect of Substrate Dielectric Constant Variations

The resonant frequency of an unloaded rectangular cavity operating in the dominant cavity mode, TE_{101}, is inversely proportional to the relative permittivity of the dielectric material. Since this relationship also applies to the dimensions of the cavity, it follows that loading a cavity with material of high dielectric constant will result in a smaller cavity design. This is a simple way of making any circuit more compact. However, dielectric constant of any substrate material varies in frequency due to manufacturing imperfections. For that, one needs to take into account the effects that this inaccuracy may have on the overall circuit performance. From design guidelines available by DuPont [20] and Filtran Microcircuits Inc. [27], one can obtain information as to how dielectric materials change their properties with frequency and manufacturing tolerances. For this design, where $\varepsilon_r = 7.1$, representative variation at both extremes are $\varepsilon_r = 6.9$ and $\varepsilon_r = 7.3$. In both cases, entire dielectric material was changed, not just the portion where the via cavity resides. This means that the impedance of the microstrip lines will change, accordingly. As chapter 3 of [17] outlines approximate closed form expressions to design microstrip transmission lines, characteristic impedance of a microstrip line is inversely proportional to the relative permittivity of the dielectric material. Finally, optimum via interconnect design is used in this analysis with no dielectric or conductor losses, and zero conductor thickness, as per Section 3.6. Analysis was carried out using HFSS.

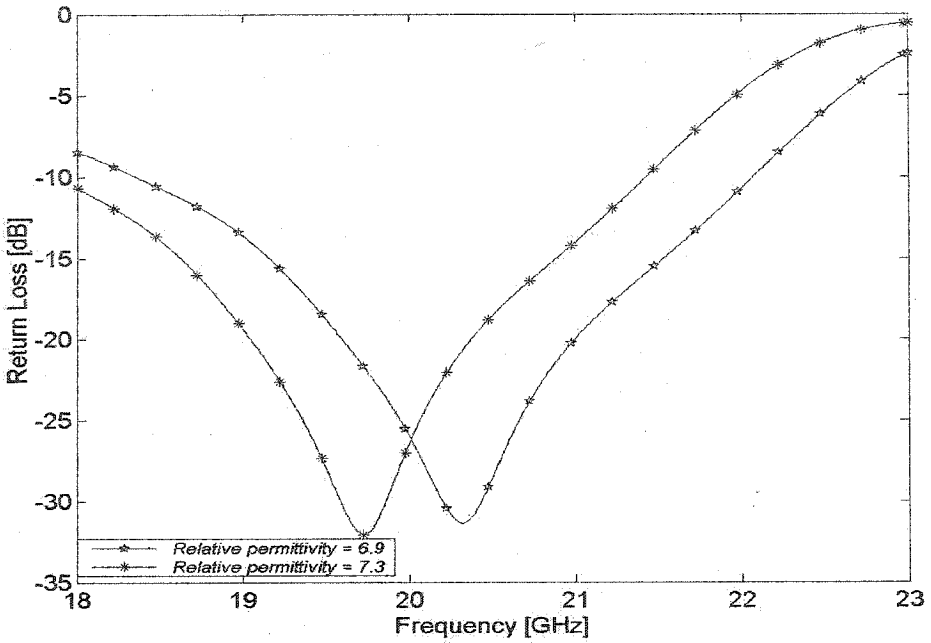

Figure 76: Return Loss of the Via Walled Interconnect where the Via Dielectric Constant is a Parameter

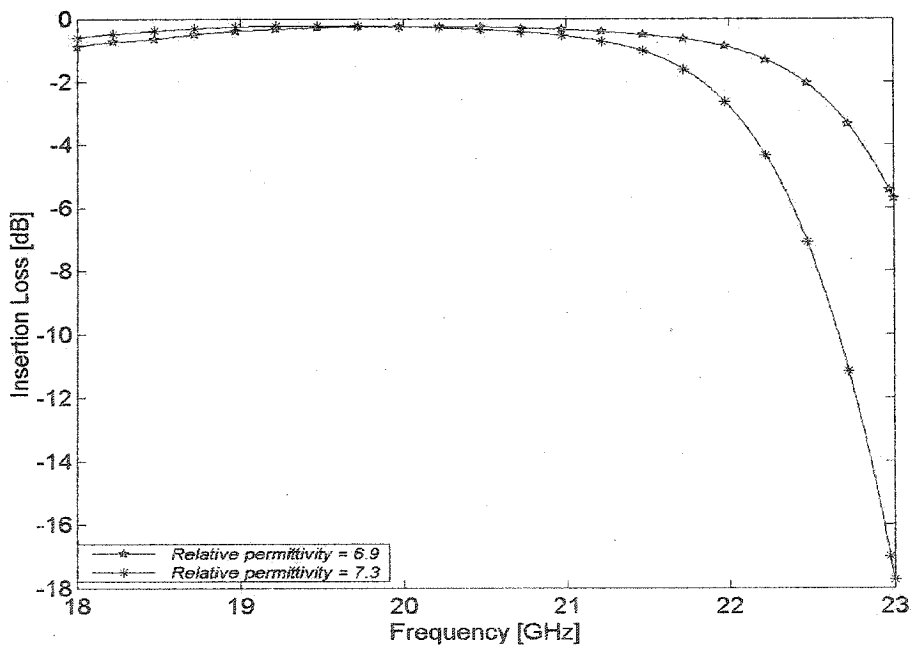

Figure 77: Insertion Loss of the Via Walled Interconnect where the Dielectric Constant is a Parameter

The impedance bandwidth is reduced by about 3% to approximately 15%. The behaviour is easily predicted by considering equation (2) which shows the resonant frequency relationship for an unloaded rectangular cavity operating in its dominant mode. Clearly, dielectric constant variations do not have a great effect on the performance of the optimum vertical interconnect circuit.

3.7.5 The Effect of the Dimensions of the Input/Output Microstrip Lines

Most printed circuit board manufacturers guarantee impedance of any line with a tolerance of ± 10%. This can be achieved by either altering the line width or changing the substrate thickness where the microstrip line resides. This assumes that the dielectric constant of the substrate material does not change. In some cases, the manufacturer may use a combination of both to provide proper characteristic impedance of a transmission line. Here, the change in characteristic impedance is accomplished by changing the conductor width. Therefore, 45 Ω and 55 Ω lines are under consideration. Using equation (3), the conductor width resulting in a 45 Ω transmission line placed on a 6 mil substrate with $\varepsilon_r = 7.1$ is 9.45 mil, where as 55 Ω line gives rise to conductor width of 6.53 mil.

Finally, optimum via interconnect design is used in this analysis with no dielectric or conductor losses, and zero conductor thickness, as per Section 3.6. Analysis was carried out using HFSS. The simulation results of Figures 78 and 79 show what happens when both microstrip lines change impedance to the same value, i.e. both are at either 45 Ω or 55 Ω.

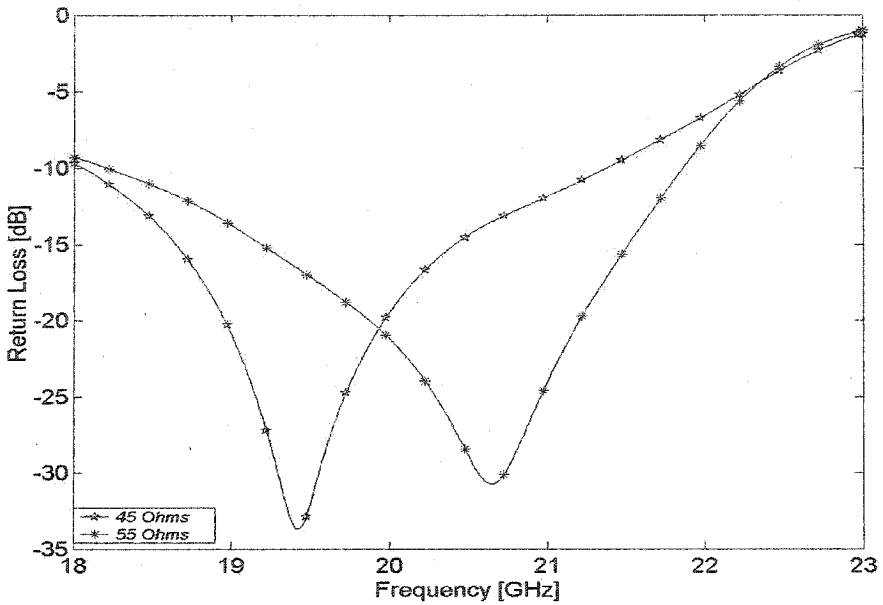

Figure 78: Return Loss of the Via Walled Interconnect where the Microstrip Line Impedance is Varied

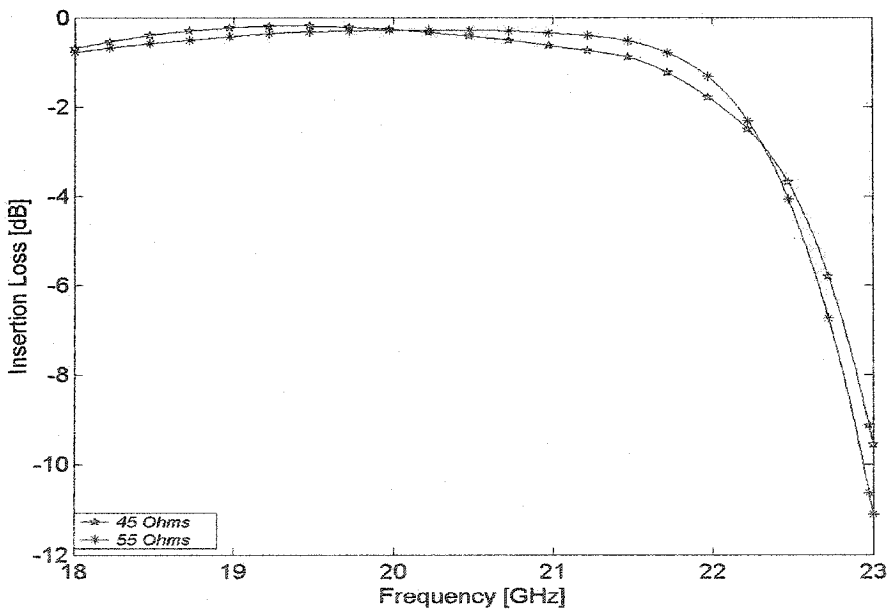

Figure 79: Insertion Loss of the Via Walled Interconnect where the Microstrip Line Impedance is Varied

Lower impedance line results in wider conductor but shorter guided wavelength. Conversely, higher impedance transmission line gives narrower conductor and longer guided wavelength. This, in turn, results in electrically longer or shorter open circuit stub lengths, respectively. This is why the return loss responses are shifted in frequency. Section 3.6.4 shows analysis where the circuit performance is changed due to varying open circuit stub length, *g*. The results are identical. One can then conclude that the impedance change of the microstrip lines is equivalent to changing the open circuit stub length by altering the electrical length of the stub, thus changing the amount of coupling in and out of the via walled cavity which results in response shifted in frequency and possible reduction of impedance bandwidth. In this example, the bandwidth is not affected by the manufacturing tolerances.

Also, HFSS simulation engine ensures maximum coupling between wave ports and the microwave structure, so that circuit performance is unaffected by any impedance mismatch. This also applies to Ensemble. This is why no degradations in return loss are observed.

Finally, one can realize a design where one microstrip line is of higher impedance than the other. The effect of that configuration is presented Figures 80 and 81.

The response does not shift in frequency when one of the transmission lines has a characteristic impedance of 45 Ω and the other of 55 Ω. Impedance bandwidth is not affected and circuit performs very well with these tolerances.

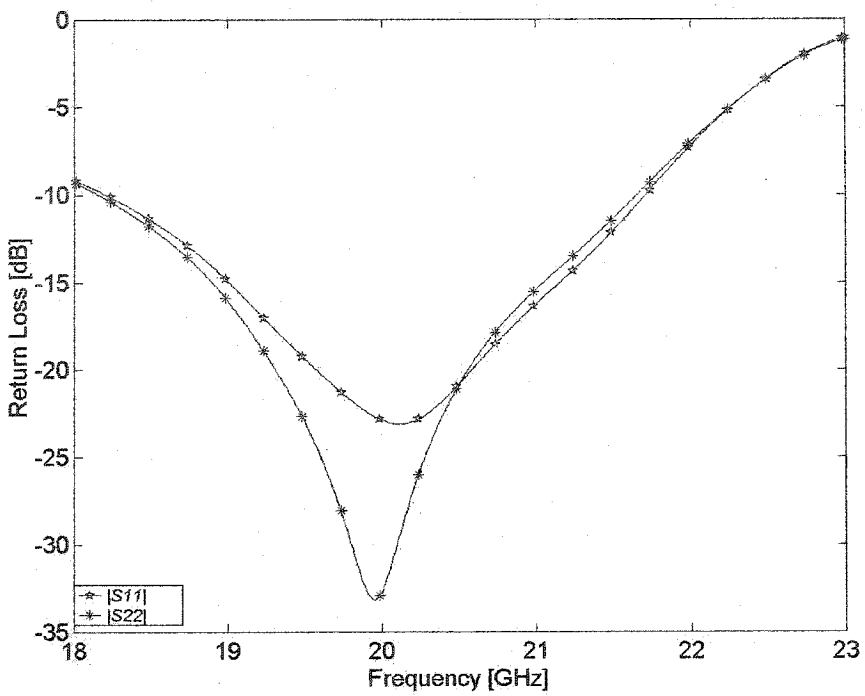

Figure 80: Return Loss of the Via Walled Interconnect where the Microstrip Lines Have Different Characteristic Impedances

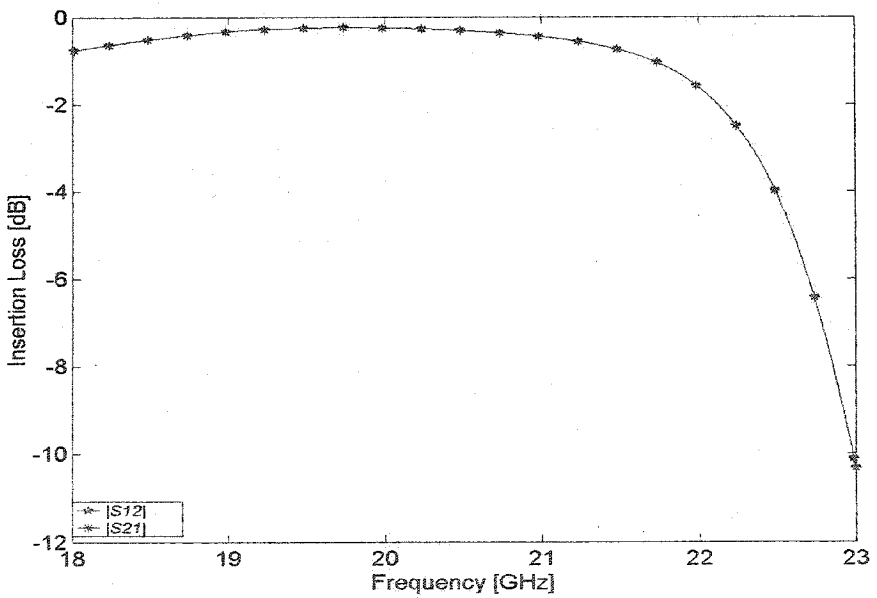

Figure 81: Insertion Loss of the Via Walled Interconnect where the Microstrip Lines Have Different Characteristic Impedances

3.7.6 Concluding Remarks on the Effects of Fabrication Variations

It is very important to consider manufacturing tolerances in any printed circuit board design. Circuits designed to operate at microwave or millimeter wave frequencies should be given even more consideration as certain parameters may change the performance drastically or even render the design useful.

The improved rectangular via walled cavity design resulted in the dimension ***d*** being much larger than ***a***. This was done purposely to remove the effect manufacturing tolerances can have on the circuit performance when this dimension is changed and still maintain the configuration such that TE_{101} mode remains the lowest cavity mode. As a result, changing the overall dimension, ***d***, did not alter the response noticeably.

Unfortunately, small changes to dimension ***a*** of the cavity, will result in potentially large frequency shifts of the response. This can be easily observed by analyzing equation (2). Fortunately, with the tolerances outlined by Cassivi et al in Table I of [11], circuit performance of about 15 % impedance bandwidth can be achieved. This is very satisfactory result allowing for other manufacturing tolerances and still meeting general bandwidth requirements of 5 %.

As the circuit operates in such a way that energy is coupled through rectangular slots into the cavity, it is very important to position both coupling slots in such a way as to provide the best performance. Moving coupling slots forward or backward, along the axis of microstrip lines can have detrimental effects. This occurs simply because the optimized open circuit stub length is no longer maintained and as a result, energy is not efficiently coupled in and out of the cavity. Circuit with the impedance bandwidth in excess of 10 % can still be achieved. When slots are placed off center, little effect is observed. Energy is still coupled optimally as maximum current is maintained at the aperture since open circuit stub length has not changed.

Dielectric constant variation can be easily predicted through the analysis of equation (2). The resonant frequency of an unloaded rectangular cavity shifts down with increasing relative

permittivity and the opposite is true when the parameter decreases. However, overall performance is well maintained and impedance bandwidth in excess of 15 % can be achieved.

The impedance of a microstrip line is yet another parameter that is often under the scrutiny of manufacturing tolerances. Changing the conductor width, altering the thickness of the substrate or changing the dielectric constant of the material can alter the impedance of a transmission line. Here, line impedances were varied by changing the width of the conductor. Lower impedance line results in wider conductor but shorter guided wavelength. Conversely, higher impedance transmission line gives narrower conductor and longer guided wavelength. This, in turn, results in a electrically longer or shorter open circuit stub, respectively. This is why the response of the return loss is shifted in frequency. Section 3.6.4 shows analysis where the circuit performance is changed due to varying open circuit stub length, ***g***. The results are identical. One can then conclude that impedance change of the microstrip lines is equivalent to changing the open circuit stub length by altering the electrical length of the stub, thus changing the amount of coupling in and out of the via walled cavity which results in the response shifted in frequency and possible reduction of the impedance bandwidth. In this design, the bandwidth is not affected noticeably by the manufacturing tolerances.

3.8 VERTICAL INTERCONNECTS WITH DIFFERENT INPUT/OUTPUT MICROSTRIP LINE DIRECTIONS AND COUPLING SLOT SHAPES

3.8.1 Introduction

Until now, all analysis has been carried out using vertical interconnect circuits which use in-line coupling. That is, both microstrip ports are positioned along the same line of symmetry.

It is then interesting to see whether a circuit could be built such that the coupling configurations are different. If this were possible, it would add flexibility to the design. This is because most of the time, designs have a lot of circuitry and printed circuit board space is always at a premium. Being able to position the vertical transition circuits in various coupling configurations may mean the difference between having the circuit done within allowed space or not being able to do it at all.

Even though the following coupling methods are new, the design considerations and circuit parameter tolerances already identified are the same as previously stated in Sections 3.6 and 3.7.

3.8.2 Interconnects with Spatially Orthogonal Input/Output Microstrip Lines

Orthogonal coupling is made when both microstrip lines are at ninety degrees from one another. This means that the coupling slots must be orthogonal, residing on opposite ends of the cavity. This poses a problem. It was determined that the length of the coupling aperture, ***h***, to large extend controls the impedance bandwidth. Since both slots are at ninety degrees from one another, it follows that the rectangular cavity should have both ***a*** and ***d*** sides of comparable lengths. It follows, then, that the improved vertical interconnect design should not be used as the dimension ***d*** is much larger than ***a***. Therefore, one can use the very first design where ***a*** = 150 mil, ***d*** = 164 mil in order to support the TE_{101} resonant mode in the cavity. Target operating frequency as well as printed circuit board parameters all remain the same as depicted in Section 3.5, i.e. f_{res} = 20 GHz, ε_r = 7.1, ***b*** = 75 mil, and microstrip lines are designed on a 6 mil substrate giving conductor width of 7.8 mil, using equation (3). As before, it is easier to optimize a design with solid, perfectly conducting cavity walls rather than attempt to optimize the final via walled interconnect design.

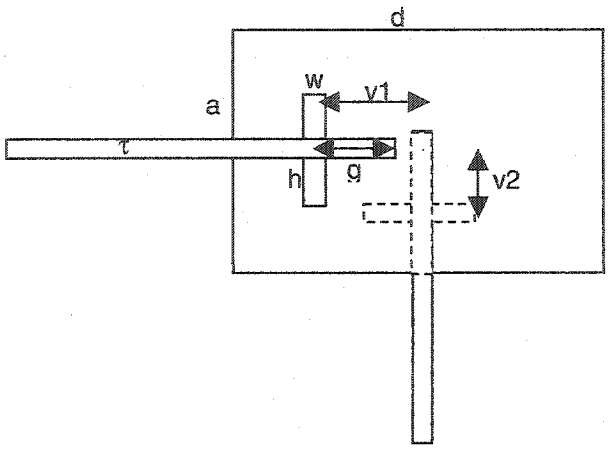

Figure 82: Solid Wall Rectangular Cavity Vertical Interconnect, Orthogonal Coupling - Top View

The design was optimized for ***w*** = 5 mil, ***h*** = 120 mil, and ***g*** = 66 mil, ***v1*** = 75 mil, ***v2*** = 70 mil.

Simulations have been carried out using Ensemble.

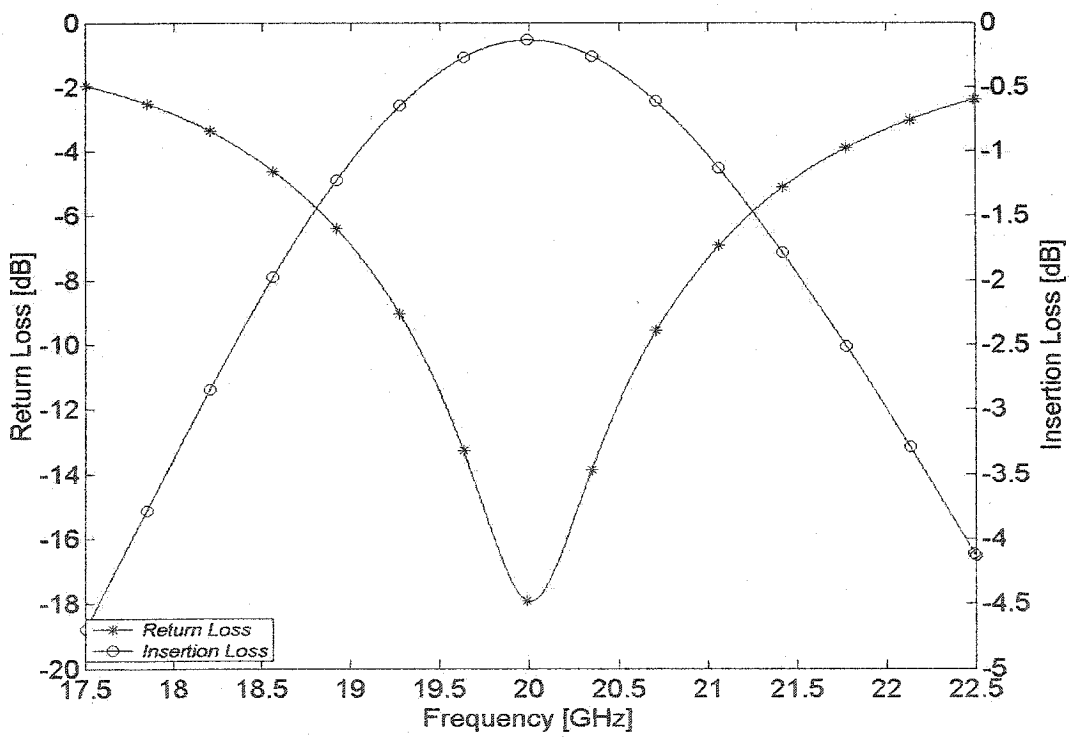

Figure 83: Simulation Results for the Solid Cavity Wall Interconnect Design with Microstrip Lines in the Orthogonal Configuration

The circuit simulation did not include any conductor or dielectric losses. Compared to the in-line configuration, thoroughly analyzed in Section 3.5, this cavity shows favorable performance, although small in comparison to the improved design of Section 3.6. The increase in bandwidth is likely due to the enlarged slot length, ***h***. Bandwidth of about 7 % is achievable with this particular design.

To complete the design, it is essential to replace the solid wall cavity with the via fence. For a via diameter of 10 mil and desired pitch of 20 mil, the amount by which ***a*** and ***d*** must increase is 5.26 mil. This becomes the new outline for the vias to be placed. Once the corner vias are placed, one places the remaining vias with equal spacing between them. In this configuration, 8 vias have been placed along side ***a*** with 22.1 mil spacing between them, and 9 vias were placed along side ***d*** with 21.15 mil spacing. The simulation results in Figures 84 and 85 show both lossless and lossy configurations. For the case where losses are included, both finite conductivity of $\sigma = 5.8 \times 10^7$ S/m and dielectric loss of $\tan\delta = 0.0025$ were used.

The final design confirms the performance of this vertical transition circuit. It is evident that there is the flexibility of using a circuit in this type of configuration. However, one needs to remember that choosing cavity dimensions that are almost the same results in a design which is sensitive to parameter variations in both cavity sides ***a*** and ***d***. This may not be desirable unless manufacturing processes are used that can accommodate very small tolerances, such as those outlined by Cassivi et al in Table I of [11].

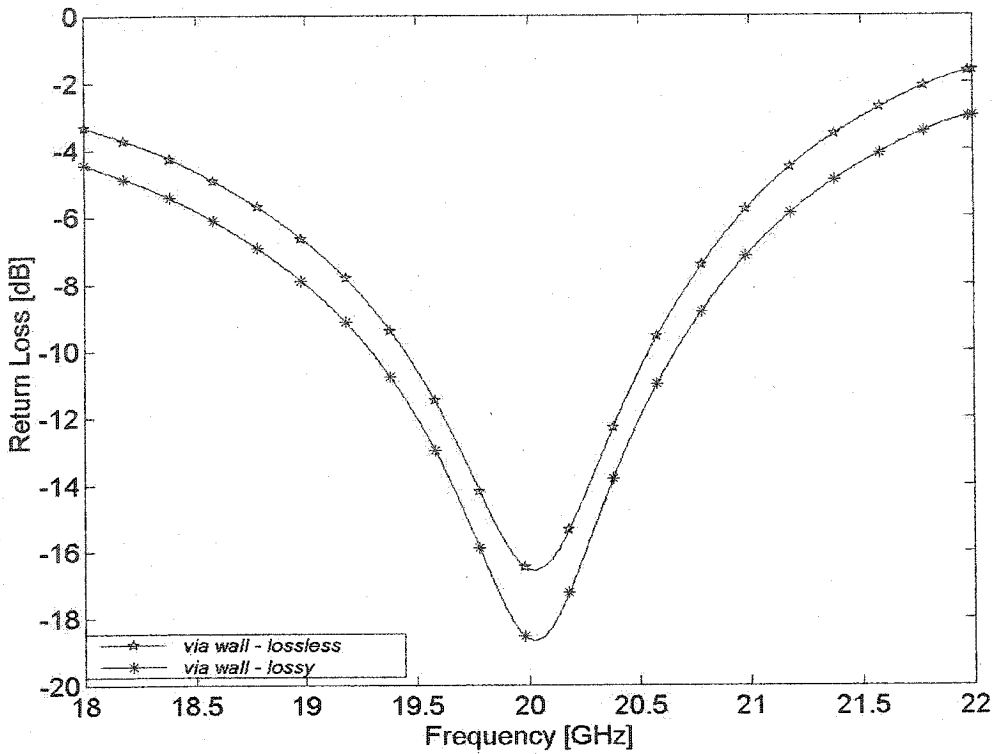

Figure 84: Return Loss of the Via Walled Interconnect in the Orthogonal Coupling Configuration

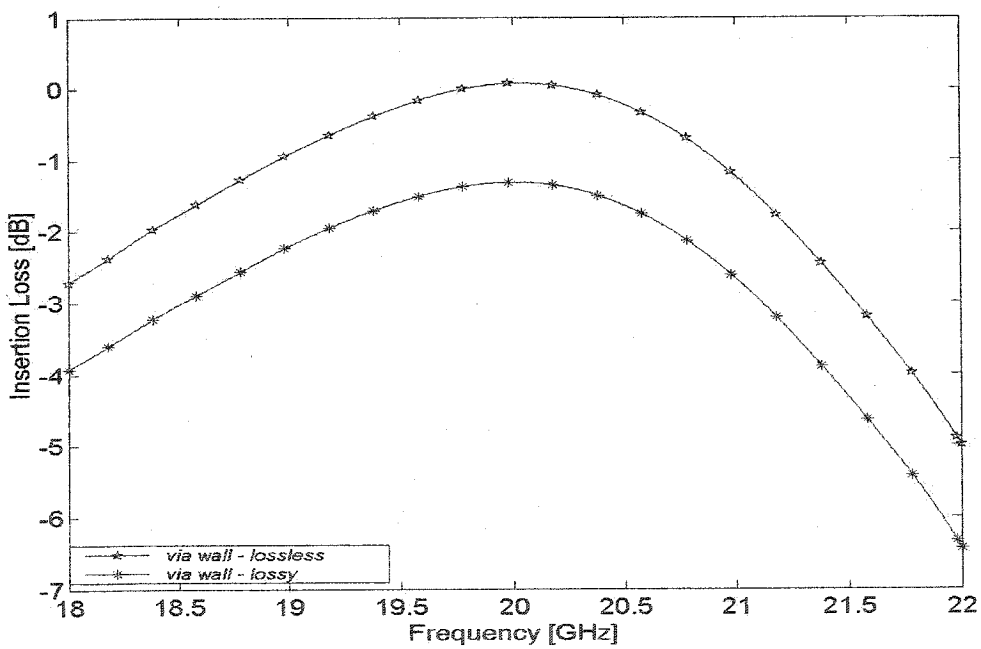

Figure 85: Insertion Loss of the Via Walled Interconnect in the Orthogonal Coupling Configuration

A fair amount of research has been dedicated to improving impedance bandwidth and reducing mutual coupling between microwave circuits by using different shapes of the coupling slots. References [28-29] are good examples of the type of work others have done on this subject. Among other slots like the 'H' shaped or 'hour glass' shaped coupling apertures, it seems the bowtie slot shows most superiority. Alexopoulos et al in [29] explain that "at the center frequency, bowtie and H-shaped slots twist the polarization direction of the out-going electromagnetic wave (the cause of mutual coupling).... the mutual coupling is reduced ..." and "in the upper and lower band, bowtie slot couples more energy than rectangular and H-shaped slots". It is therefore worth considering this type of aperture coupling as a mechanism to transfer energy vertically.

Since there is a possibility of increasing impedance bandwidth, it is worth using this aperture in the orthogonal configuration as it is the design with the smallest bandwidth.

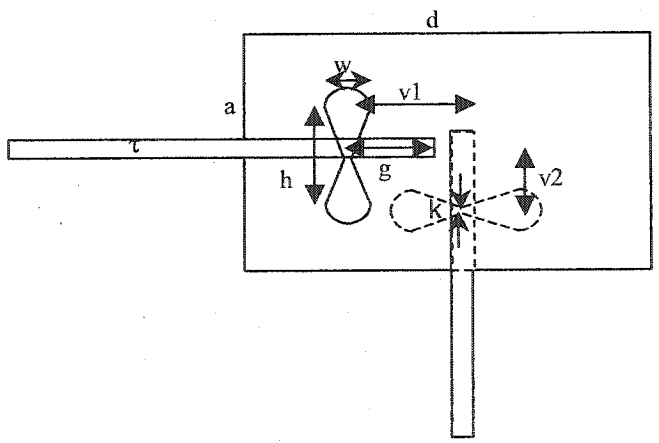

Figure 86: Top View of the Solid Walled Cavity Interconnect in the Orthogonal Coupling Configuration with Bowtie Apertures

The design was made such that all parameters have remained the same as in the previous sections except for the following: h = 110 mil, w = 28.5 mil, k = 6 mil, $v1$ = 60 mil, $v2$ = 52 mil, g = 66 mil, and the arc is 30 degrees.

The results in Figure 87 indicate no bandwidth improvements, although slightly shorter slots were used. Since the apertures are more complex to manufacture, it seems that there is little gained in using this type of a coupling slot as the rectangular slots are much easier to manufacture and take less time to optimize.

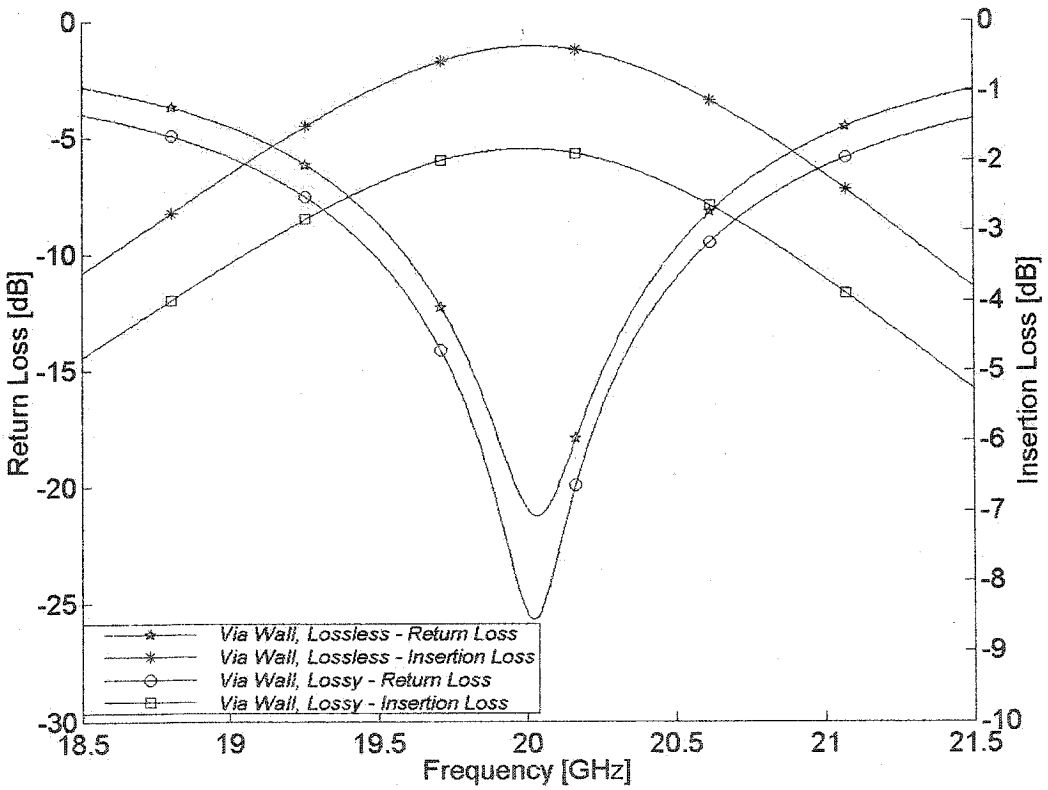

Figure 87: Simulation Results of the Via Wall Cavity in the Orthogonal Coupling Configuration with Bowtie Apertures

3.8.3 Interconnect with Offset Input/Output Microstrip Lines

The offset transmission line coupling configuration is one where both microstrip lines are offset relative to the center of the cavity. In this case, there is no restrictions on the cavity shape, as there was in the case of the orthogonal coupling interconnects. Therefore, one can start with the optimum vertical interconnect in-line coupled design, described in Section 3.6 and optimize it for the new coupling configuration. This cavity size is preferred as manufacturing tolerances do not affect circuit performance when applied to the cavity dimension, ***d***. Once again, one should start with a solid wall cavity interconnect and then replace the outer walls with the via fences. The final dimensions of the offset vertical transition are ***a*** = 130.96 mils, ***d*** = 395.26 mils, ***h*** = 180 mils, ***w*** = 10 mils, ***v*** = 30 mils, ***g*** = 75 mils, ***r*** = 70 mils, ***2t*** = 10mils, ***p*** = 21.82 mils along the walls of length ***a***, and ***p*** = 20.8 mils along the walls of length ***d***. Ensemble simulation tool was used to optimize this design.

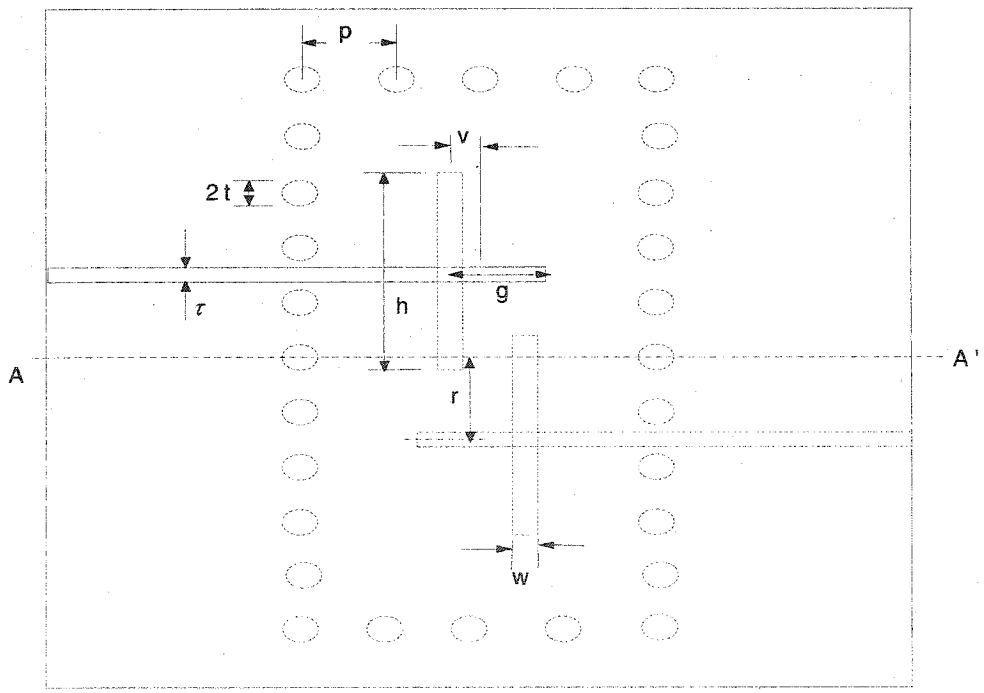

Figure 88: Top View of the Offset Coupling Vertical Interconnect

Using the previously mentioned performance criteria this transition has a bandwidth of 12.5% as shown in Figures 89 and 90.

From the results, it appears that there are two resonant modes residing in the cavity. Unfortunately, this does not seems to be visible when the same circuit is simulated using HFSS. Since the obtained values of return loss where this is seen are below –30 dB, simulation results can change depending on the convergence criteria, approximations made by the tools, variations in meshing of the structure, all of which may contribute to differences in results when very small numbers are to be calculated. For completeness, HFSS results are also included.

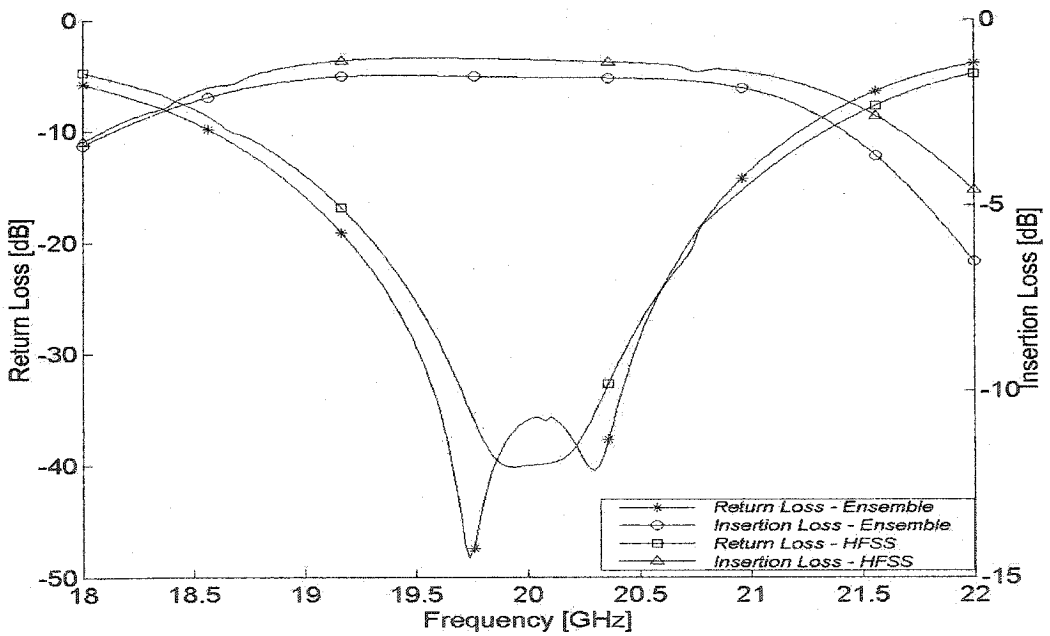

Figure 89: Ensemble Simulation Results of the Offset Coupled Vertical Interconnect

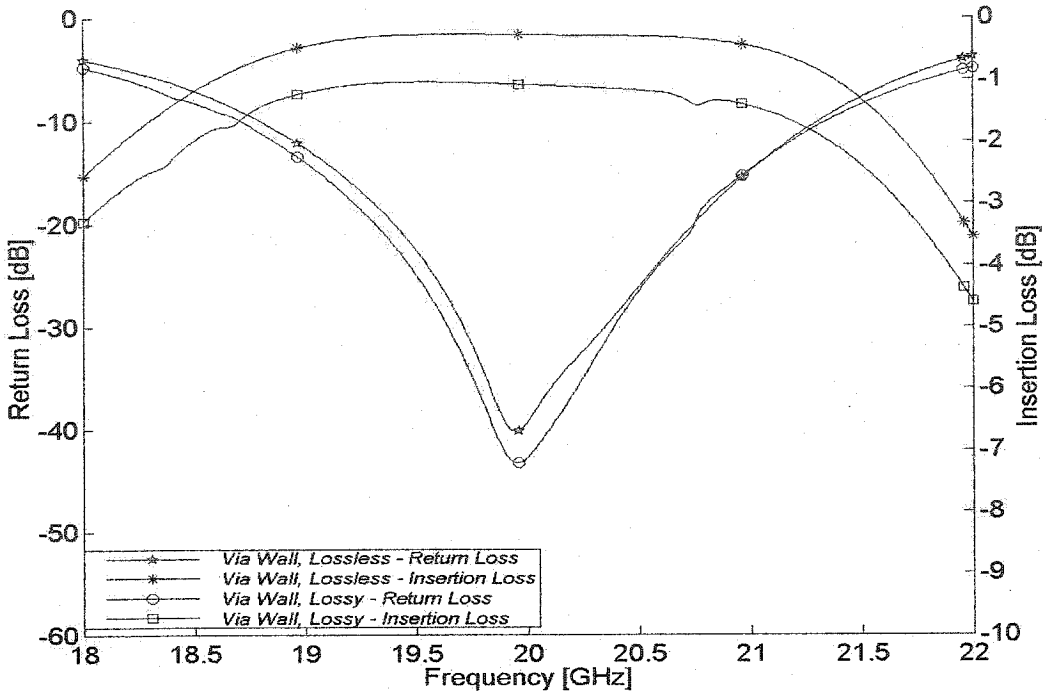

Figure 90: HFSS Simulation Results of the Offset Coupled Vertical Interconnect

Offset coupling provides yet another way of accommodating various design constraints. With impedance bandwidth of 12.5 % there is enough room to allow for manufacturing tolerances.

3.8.4 Concluding Remarks on the Different Vertical Interconnect Configurations

When novel ideas are put forward, it is always desirable to have it applicable in many different ways. This results in added flexibility that designers like to have. With the demand of producing smaller products and including more functionality into existing products, the vertical interconnect circuit may not always be used in the in-line configuration due to space constraints or proximity to other circuit which may not allow for the in-line coupling. Therefore, other coupling configurations are necessary.

Orthogonal coupling is a configuration in which both microstrip lines are orthogonal to one another. This configuration requires that the cavity be more square, rather than a long

rectangle. This is because one needs to maximize slot length for both ports. This is not possible when the parameter ***d*** is much larger than ***a***. As a consequence, the design has more parameters which are sensitive to manufacturing tolerances as changes to both ***d*** and ***a*** affect the performance of the interconnect circuit. As well, impedance bandwidth of about 7 % can be achieved, which is considerably better than the same cavity used in the in-line coupling configuration. Finally, bowtie coupling slots have been identified in [28-29] to enhance bandwidth and reduce mutual coupling between circuits. It was determined that smaller bowtie shaped aperture could in fact result in response similar to that of a longer rectangular slot. However, since the benefits in this type of application do not seem to stand out and the added complexity of the design is great, it is concluded that rectangular aperture is best suited for this application.

As microstrip lines come from different printed circuit board layers, it may be difficult to position them such that they both align with the center of the cavity. If that is challenging in a given design, it might be useful to have two microstrip lines offset relative to the center of the cavity. In that case, one can use the optimum design configuration where ***d*** is much larger than ***a*** thus removing rapid performance changes when manufacturing tolerances are applied to the dimension ***d***. Impedance bandwidth of 12.5 % can be achieved with this configuration allowing for losses and manufacturing tolerances to further reduce performance and still meet the target bandwidth of 3 - 5 %.

3.9 VERTICAL INTERCONNECTS USING VIA-WALLED CYLINDRICAL CAVITIES

3.9.1 Preliminary Comments

In the brief literature review, there seems to be absolutely no consideration given to designing circular via walled cavities. In chapter 2, when the current vertical interconnection techniques were reviewed, Pozar in [30] and Lee in [31] have used circular cavities, operating in their lowest order TE_{111} mode, to design vertical interconnections between two microstrip lines through a thick ground plane. It is then fair to assume that one should consider this type of cavity as a potential candidate for vertical interconnection using via walls.

Unfortunately, chapter 3 of [17] shows that the lowest order mode of a circular waveguide has all three components of the magnetic field, thus resulting in current density distribution which not only has a vertical component, but also circumferential. In the case of a solid circular cavity, this is not critical. However, when the solid wall is replaced with vias, the gaps between vias disturb the current flow, thus rendering the device useful. This is illustrated in Figure 91.

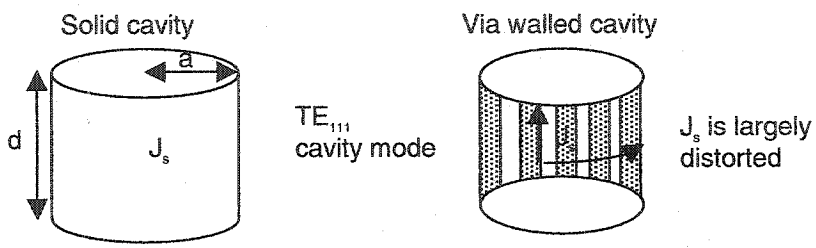

Figure 91: Current Density Distribution of the Circular Cavity Operating in the TE_{111} mode

One could ask the question of whether there is a cavity mode that would result in vertical currents only, along the cavity walls. As it turns out, cavity mode TM_{011} gives currents only in the vertical direction. It is then worth considering a cavity operating in that mode.

The TM_{011} cavity mode results in currents only along vertical walls. It is then fair to assume that a vertical interconnect constructed with a cavity supporting this particular mode might work when the solid cavity is later replaced with vias. In order to design this type of an interconnect, one needs to obtain the length of the vertical interconnect along with corresponding cavity radius. In Chapter 6 of [17], Pozar derives an expression for the resonant frequency of a circular cavity operating in TM_{nml} mode as $f_{nml} = \frac{c}{2\pi\sqrt{\mu_r\varepsilon_r}}\sqrt{\left(\frac{p_{nm}}{a}\right)^2+\left(\frac{l\pi}{d}\right)^2}$, where p_{01} = 2.405 for the TM_{011} mode under consideration. Clearly for this cavity mode, the vertical dimension plays an important role in establishing the resonant behaviour of the unloaded cavity. That means that with any changes to the vertical dimension, the resonant frequency will be affected accordingly. Also, the combination of dimensions *a* and *d* results in a cavity

which is quite large for a given resonant frequency. For instance, in order to design a cavity which operates at 20 GHz, one set of dimensions could be ***a*** = 125.87 mil, ***d*** = 142.5 mil. The above equation reveals that there is only a limited set of values that give dimensions which can be used for a given design frequency. This can be illustrated by solving the above equation for the cavity radius ***a***, as follows: $a = \frac{p_{nm}}{\sqrt{\left(\frac{2\pi f_{nml}\sqrt{\mu_r \varepsilon_r}}{c}\right)^2 - \left(\frac{l\pi}{d}\right)^2}}$.

This relationship shows that for a given design frequency, only specific values of the vertical dimension will result in a real value of the cavity radius, ***a***. This is a limitation as very few vertical interconnects can be designed at a given operating frequency. Nonetheless, it is worth testing the above formulation to see if one can actually make it work as a vertical interconnect using printed circuit board technology.

In the present example, ***d*** = 142.5 mil, ***a*** = 125.87 mil. The substrate material used has a relative permittivity of ε_r = 7.1. The microstrip design remains the same as in the case of a rectangular cavity interconnect circuit, giving a transmission line τ = 7.8 mil wide, built on 6 mil thick substrate and an open circuit stub length of ***g*** = 66 mil is used as a starting point in the optimization ($\lambda_g/4$). Once the optimization was completed, the optimum open circuit stub length of ***g*** = 65 mil resulted. Also, the coupling aperture was found to be of the following dimensions, ***h*** = 180 mil, ***w*** = 10 mil, and offset from the center of the cavity to the center of the slot, ***v*** = 70 mil.

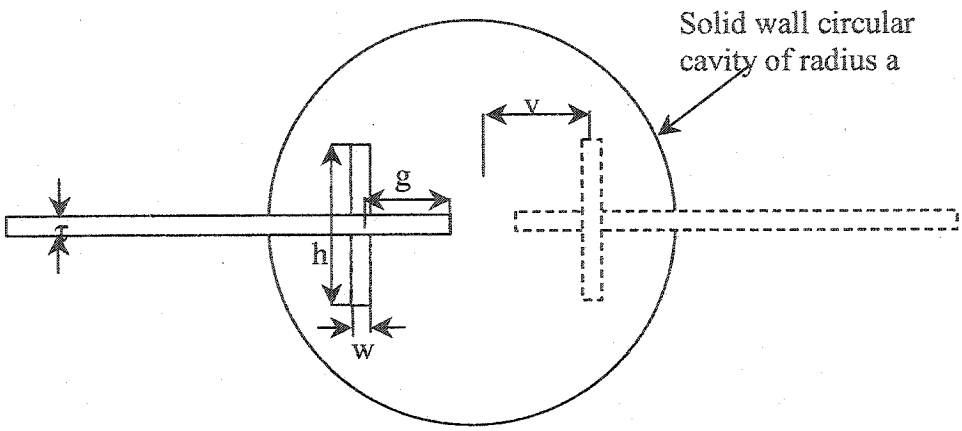

Figure 92: Top View of the Solid Wall Circular Cavity Interconnect

Much like the rectangular cavity interconnect circuit, the vertical transition using a circular cavity is reciprocal. This does not have to be the case, but it simplifies the design and analysis.

Once the design is finalized using solid wall circular cavity, design rules outlined in Section 3.4.4 are applied to replace the solid cavity wall with vias of 10 mil in diameter. The simulated results using HFSS are presented in Figures 93 and 94.

For a relatively large vertical distance of 142.5 mil, the solid wall cavity interconnect exhibits good performance where impedance bandwidth of about 8% was obtained. This is for a lossless case. Once the solid wall cavity is replaced with vias, performance deteriorates to less than 5 % of impedance bandwidth. Conductor and dielectric losses contribute further to an additional loss of about 0.5 dB. This sudden change in the performance might be contributed to the way in which the solid wall was approximated by vias. It is not an easy task to place vias in a circle, thus making the optimization task a little more challenging. Some vias result in further spacing than others and energy begins to leak out affecting the overall performance of the circuit.

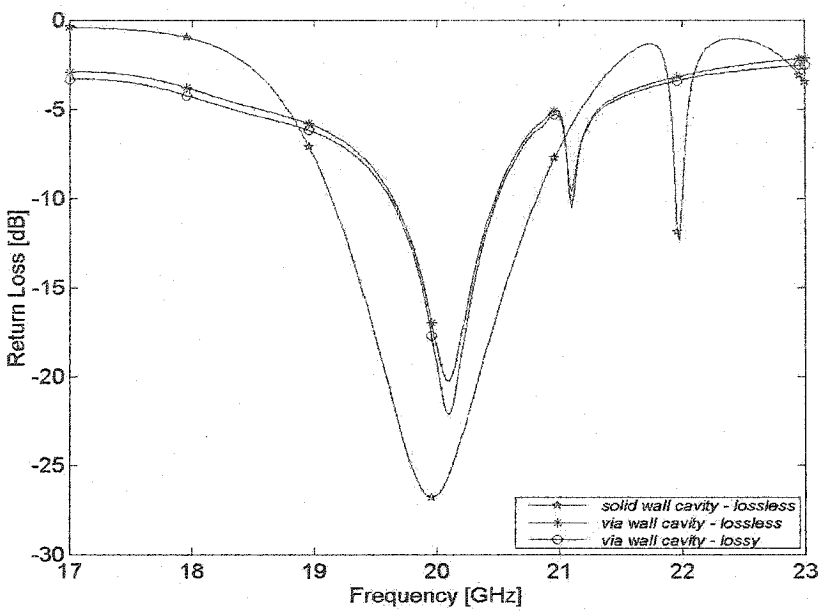

Figure 93: Return Loss of the Circular Cavity Interconnect

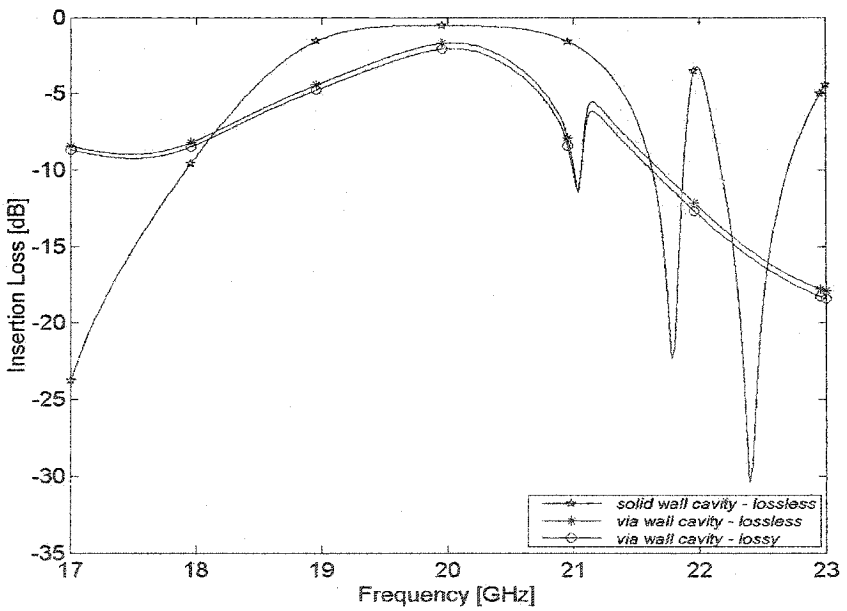

Figure 94: Insertion Loss of the Circular Cavity Interconnect

It is clear that a design can be carried out using vias forming a circular cavity operating in the TM_{011} mode. A designer choosing this type of an interconnect must take into account that this

mode of propagation is not the lowest cavity mode and as a result, other cavity modes may be excited if the circuit is not properly designed.

In summary, circular cavity can be considered as an integral part in designing vertical interconnect circuits. The lowest cavity mode, TE_{111}, results in surface current density distribution which has vertical as well as circumferential components. Even though this is not a problem for a solid wall cavity designs, via walled cavity does not work in this mode as current distribution is interrupted by lack of circumferential continuity in the via wall. However, TM_{011} mode gives currents that are only oriented in the vertical sense along the vertical cavity walls. As this is not the lowest cavity mode, one must ensure that no other cavity mode can exist, otherwise poor performance design will result. With that in mind, a vertical interconnects can be built with impedance bandwidth of about 5 %. Optimization process becomes more tedious as vias are not easily placed in a circular configuration.

Also, circular cavities are limited in their cross-sectional area, limiting the size of the coupling aperture, which plays an important role in establishing the bandwidth.

Finally, in order to design a circular cavity to operate at a given resonant frequency, there are only discrete values of cavity height, ***d***, and radius, ***a***, that will give the desired resonant frequency response, as outlined in chapter 6 [17]. This, in turn, removes the flexibility of designing vertical transitions for any number of substrate layers.

3.10 VERTICAL INTERCONNECTS USING A LOADED CAVITY

It is recognized that the performance of the vertical interconnect is affected by small changes in dimension ***a***. This is a direct consequence of how a rectangular cavity resonator operates in the lowest order mode, namely the TE_{101} mode. With the optimum design set forth, it has been shown that small variations to the dimension ***a*** may result in large centre frequency shifts. This is not a problem when the manufacturing tolerances as outlined by Cassivi et al in Table I of [11] are applied. Unfortunately, achieving these tolerances is not easy, nor is it inexpensive. It

is then desirable to investigate vertical interconnect circuits a little further to see if there is a particular cavity that would be insensitive to changes in the dimension of concern.

In reference [32], Elliott has looked at the properties of a rectangular waveguide which contains a T-septum attached to one of its side walls. In doing so, the resulting waveguide can support two modes with equal phase velocities. This structure, in turn, is likely to be resistant in its behaviour to minor dimensional changes.

Taking this idea into the design of a vertical interconnect microwave circuit, one immediately realizes that placing any structure inside the rectangular cavity adds to the complexity of the design and also results in a structure which is substantially larger than the optimum rectangular cavity design, presented in Section 3.6. This can be explained by considering the "effective" area of the cavity set out by parameters ***a*** and ***d*** for the operation in the TE_{101} mode. When the cavity is made physically smaller, the resonant frequency of the lowest order cavity mode increases. One can also think of the area made smaller when any objects are placed inside the cavity. Therefore, the resonant frequency of the cavity, which will no longer be a pure TE_{101} mode, will also increase. This is particularly true when T-septa are added to the cavity of optimum vertical interconnect design, as per Section 3.6. As in the case of the original design, it is easier to start with a solid cavity wall and T-septa, optimize the design for best performance and then replace solid walls with vias so that the design can be manufactured. With this in mind, the solid wall cavity design is depicted in Figure 95.

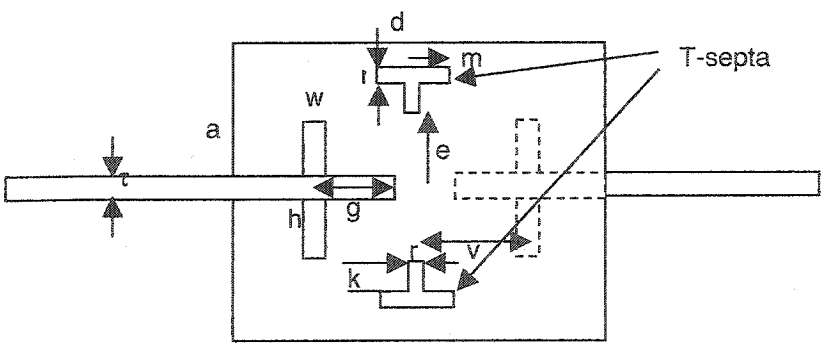

Figure 95: Top View of the Solid Wall Rectangular Cavity Interconnect with T-septa

The vertical distance was chosen to equal 75 mil as previously depicted. The microstrip line design remains the same also, since dielectric constant is 7.1. The T-septa extend the length of the cavity, or the dimension, ***b***. All other parameters are as follows:

1. ***a*** = 390 mil, ***d*** = 380 mil
2. ***h*** = 190 mil, ***w*** = 35 mil
3. ***g*** = 82.5 mil, ***v*** = 100 mil
4. ***e*** = 70 mil, ***r*** = 15 mil, ***m*** = 30 mil, ***k*** = 50 mil

The following optimum circuit performance was obtained for a lossless configuration using HFSS, and it is shown in Figure 96.

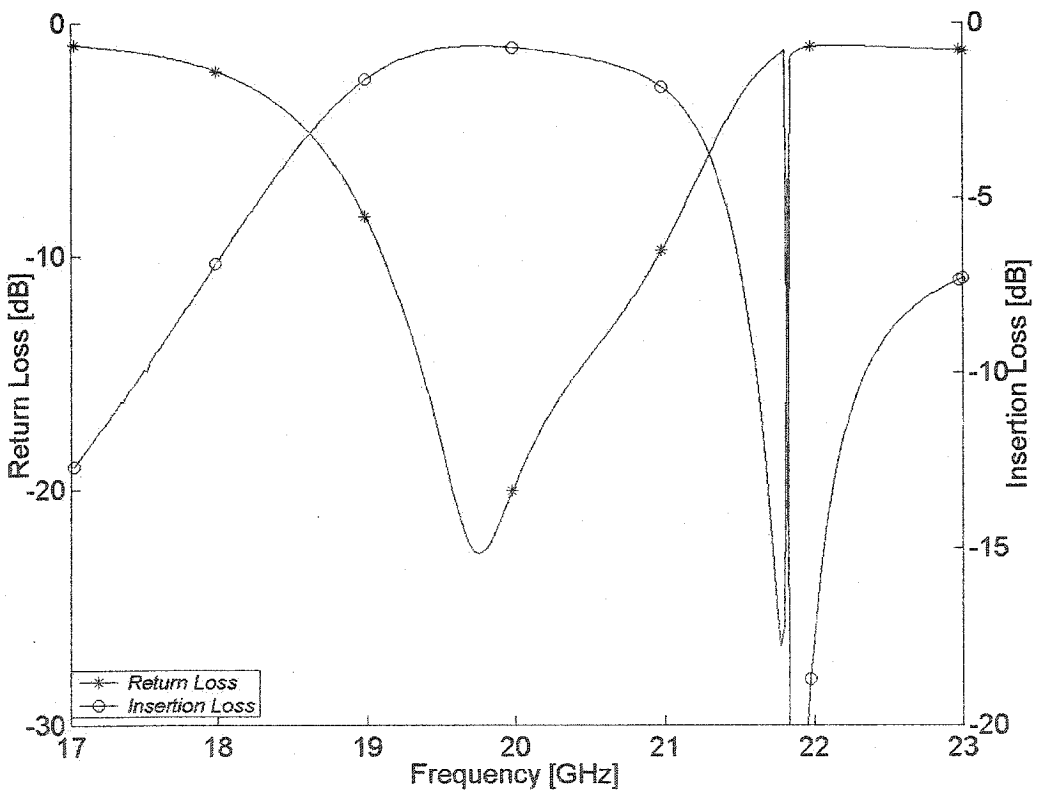

Figure 96: Simulation Results of the Solid Wall Rectangular Cavity Model with T-septa

The resulting vertical interconnect circuit shows impedance bandwidth in excess of 10 %. Due to the presence of the T-septa inside the cavity, the existing cavity mode is not likely to be the TE_{101} mode. Since the cavity mode is no longer that of the TE_{101} mode, it is uncertain whether the current density distribution along the vertical cavity walls and the T-septa will be vertical as it is in the case of a TE_{101} mode inside a rectangular cavity. This is required if this design is to be realized using current printed circuit board technology. In order to check this, solid cavity walls and T-septa are replaced with vias. In order to replace the outer cavity walls with vias, design rules of Section 3.4.4 were applied and vias of 10 mil in diameter were used. It is more difficult to replace the T-septa with vias and still maintain similar circuit performance. In this example, vias with a diameter of 8.25 mil were placed to form the T-septa, as shown in Figure 97.

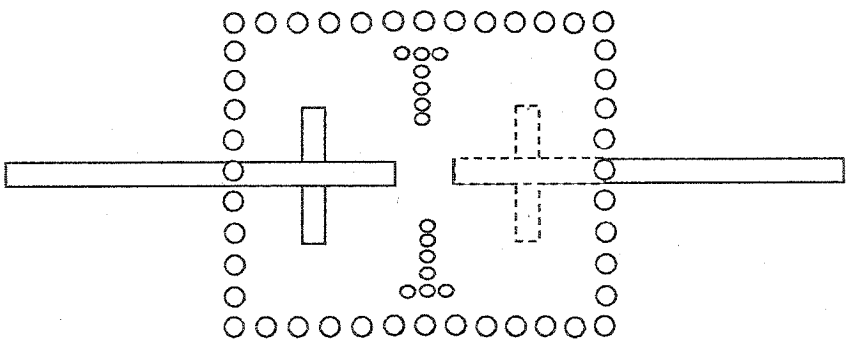

Figure 97: Top View of the Via Walled Rectangular Cavity Model with T-septa

The purpose of looking at this configuration was not just a consideration of yet another cavity shape. The main goal was to search for a vertical interconnect such that its performance is insensitive to changes in the cavity dimension ***a***. This is due to the fact that many printed circuit board manufacturers continue to build circuits, which may result in the dimension changes as much as ±3 mil. That being the case, it was demonstrated that such tolerances result in drastic performance changes of the vertical transition circuit.

As depicted in Figures 98 and 99, it is evident that the cavity modes that exist in this particular circuit support vertical current density as the performance is not affected by replacing the solid walls with vias. More importantly, the centre frequency of the response only shifts a maximum of about 300MHz when the cavity dimension *a* is changed by 3 mil. This is a vast improvement in the design as previous configuration shows changes in centre frequency in excess of 2 GHz. This is likely due to the fact that there are two resonant modes present in the cavity, as suggested by Elliott [32]. Clearly, one can use this configuration if manufacturing tolerances are of this order. The disadvantages include larger circuit and more complex design that includes the T-septa.

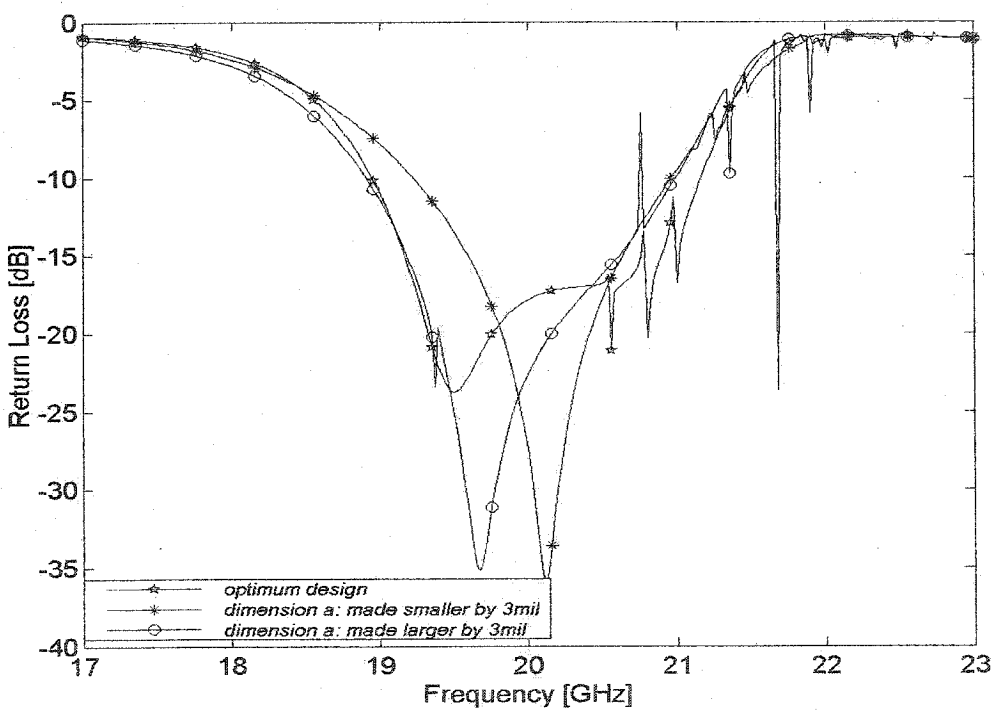

Figure 98: Return Loss of the Via Walled Rectangular Cavity Model with T-septa

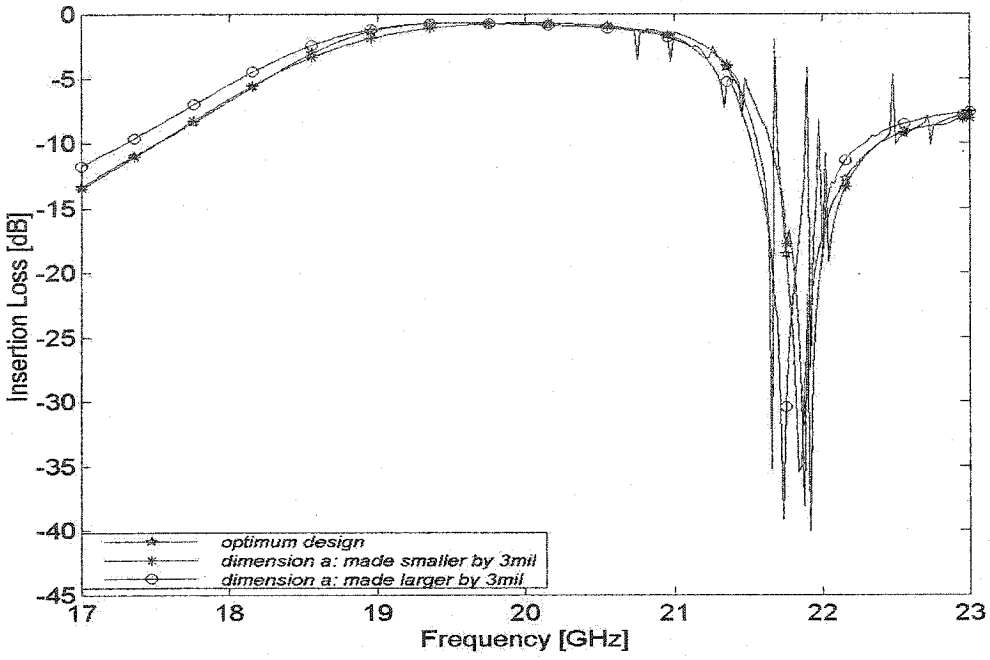

Figure 99: Insertion Loss of the Via Walled Rectangular Cavity Model with T-septa

In summary, inserting any objects inside a rectangular cavity results in smaller occupied volume which, in turn, increases the centre frequency of the circuit. In order to maintain the resonant behaviour at a desired frequency, the cavity needs to be enlarged. This is one disadvantage in inserting T-septa into the rectangular cavity. Also, the circuit is made more complex. However, as depicted by Elliott in reference [32], T-septa may contribute to a new design where two modes are supported within the cavity. In this case, the circuit is less sensitive to manufacturing changes. This is indeed the case. Therefore, one can use this approach to design a circuit that can be implemented using printed circuit board technology where T-septa and cavity walls are made of vias and manufacturing tolerances are less stringent than those outlined by Cassivi et al in Table I of [11].

3.11 STRIPLINE TO STRIPLINE VERTICAL INTERCONNECTS

3.11.1 Introductory Remarks

Until now, all analysis have been carried out for a microstrip to microstrip vertical interconnect circuits. When dealing with multi-layer printed circuit board designs, there is a possibility of wanting to transfer energy within the printed circuit board, i.e. on internal layers. For that, stripline to stripline vertical interconnect circuit is desired. Although this thesis is primarily focused on vertical transitions between two microstrip lines, a short discussion on vertical transition circuit involving striplines follows.

3.11.2 STRIPLINE DESIGN AND CONSIDERATION

A stripline is formed when a metallic conductor is placed between two substrates of equal thickness and having ground planes on either side of the structure. This is illustrated in Figure 100.

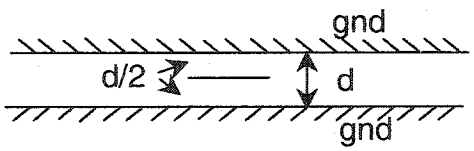

Figure 100: Cross-Sectional View of the Stripline Transmission Line

Unlike microstrip lines, the stripline has two conductors that are part of a homogeneous dielectric, and it can support propagation of a TEM electromagnetic wave. This is the usual mode of operation. However, higher TE and TM modes can also propagate resulting in unwanted parallel plate modes of wave propagation. One can suppress these modes by either shortening the two plates with vias, thus forming a 'boxed' stripline, or by ensuring that the two ground planes are separated at least one quarter of guided wavelength, as suggested by Pozar in [17]. The latter is often impractical, as circuits are made smaller resulting in more space-confined circuit integrations. Therefore, one can rely on via shortening the two plates to suppress parallel plate modes and also provide better isolation between circuits. The cutoff frequencies for TE and TM parallel plate modes can be deduced as

$f_c = \frac{n}{2d\sqrt{\mu\varepsilon}} = \frac{n \cdot c}{2d\sqrt{\varepsilon_r}}$, where ***c*** is the speed of light, ***d*** is the separation between ground planes, γ_r is the relative permittivity of the dielectric material, and n = 1, 2, 3 ... When d = 20 mil = 508 :m and γ_r= 7.1, the cutoff frequency for the lowest order TE, and TM_1 modes are 41.58 GHz. Of course, this formulation only applies to a structure comprised of a single stripline, i.e. it does not take into account any type of aperture loading. It does, however, indicate that parallel plate modes are more likely to be present in designs reaching these frequencies, unlike the cutoff frequencies of the surface wave modes possibly present when microstrip lines are used, that were in excess of a 100 gigahertz.

With a given permittivity of the dielectric material, chosen substrate thickness and characteristic impedance of the line, one can use the approximate closed form solutions outlined in chapter 3 of [17] to obtain desired conductor width. For convenience, these relationships are shown in equation (4).

$$\frac{W}{d} = \begin{cases} x & for\ \sqrt{\varepsilon_r} Z_o < 120 \\ 0.85 - \sqrt{0.6 - x} & for\ \sqrt{\varepsilon_r} Z_o > 120 \end{cases} \tag{4}$$

where

$x = \frac{30\pi}{\sqrt{\varepsilon_r} Z_o} - 0.441$, and ***W*** is the conductor width, ***d*** is the substrate thickness and Z_o is the characteristic impedance of the stripline.

In this case, ***d*** = 20 mil = 508 :m, γ_r = 7.1 and ***W*** = 5.5 mil = 139.7 :m for Z_o = 50 Σ. Note that the thickness of the dielectric substrate was increased from that used in the design of the microstrip line. This is because if ***d*** were selected to equal 12 mil (2 times 6 mil), the resulting conductor width would have to equal about 3 mil which is rather small and difficult to realize.

3.11.3 Interconnect Design and Predicted Performance

Taking the well established design approach of using the solid wall cavity with dimensions ***a*** = 114.7 mil, ***d*** = 380 mil, ***b*** = 75 mil, ***h*** = 180, ***w*** = 10 mil, ***g*** = 75 mil, and ***v*** = 35 mil, the following results shown in Figure 101 are obtained with the help of HFSS. All simulations have been carried out without including the ohmic and dielectric losses.

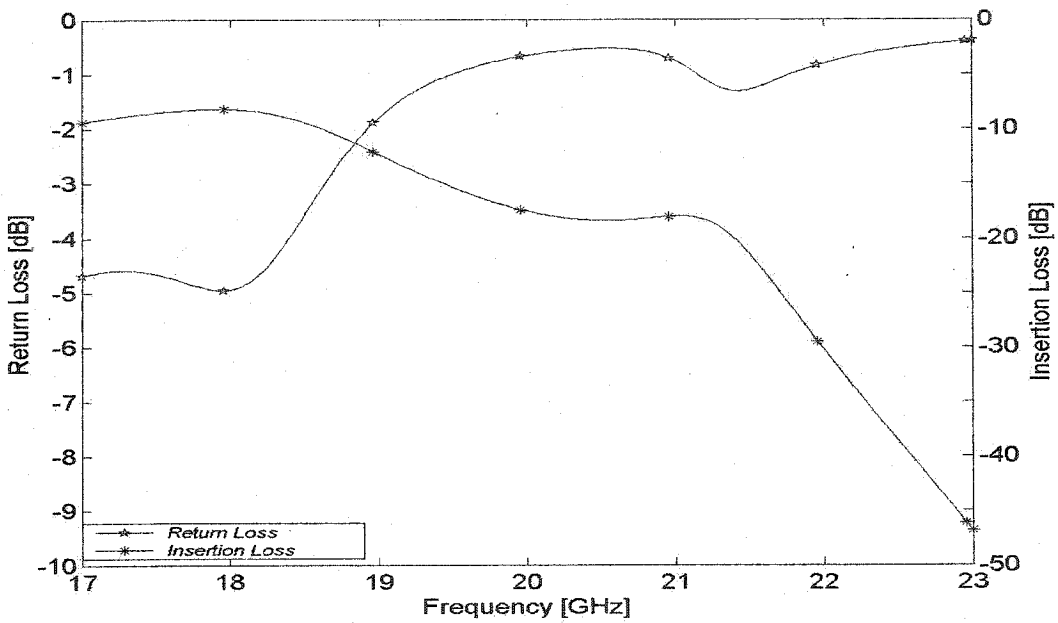

Figure 101: Simulation Results of the Stripline Solid Walled Cavity Interconnect

Clearly there is absolutely no coupling through this vertical interconnect. This may suggest that the energy is lost due to higher order modes, the parallel plate modes. In order to verify this, both striplines are boxed in with rows of vias, 20 mil in diameter and 40 mil spacing. The solid cavity is replaced with 10 mil vias as per design rules outlined in Section 3.4.4. This results in 7 vias along dimension ***a***, separated by 20 mil, and 20 vias along dimension ***d***, separated by 20.2 mil.

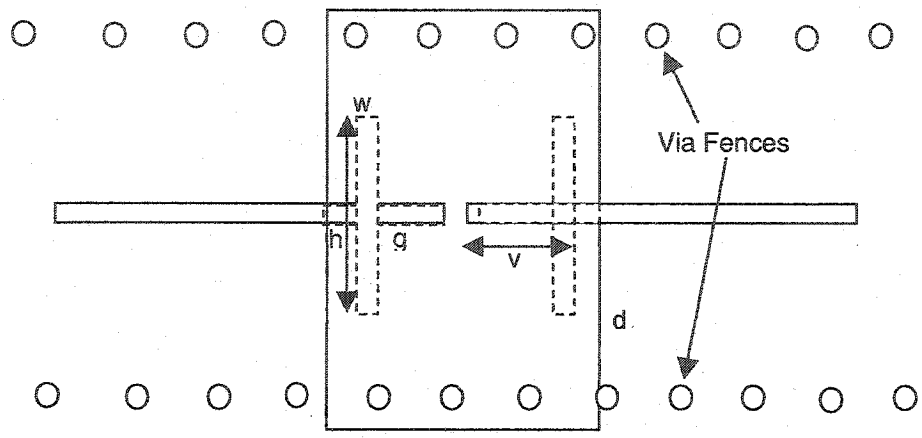

Figure 102: Top View of the Boxed Stripline Solid Cavity Interconnect Design.

Note that the via fencing is placed between the ground planes that define the stripline configuration. The vias are placed 115mil away from the center of the cavity. There is no interference between the vias and the cavity as the rectangular cavity is on a different substrate layer and it is separated from the boxed striplines.

As illustrated in Figure 103, good coupling was quickly established once both striplines have been boxed in with the via fencing. This confirms the presence of higher order modes at the design frequency of interest. Although this interconnect does not show high bandwidth, it illustrates that vertical interconnect circuits can be designed using stripline configuration, provided proper care is applied to eliminate higher order modes from propagating and diminishing the effectiveness of the microwave circuit.

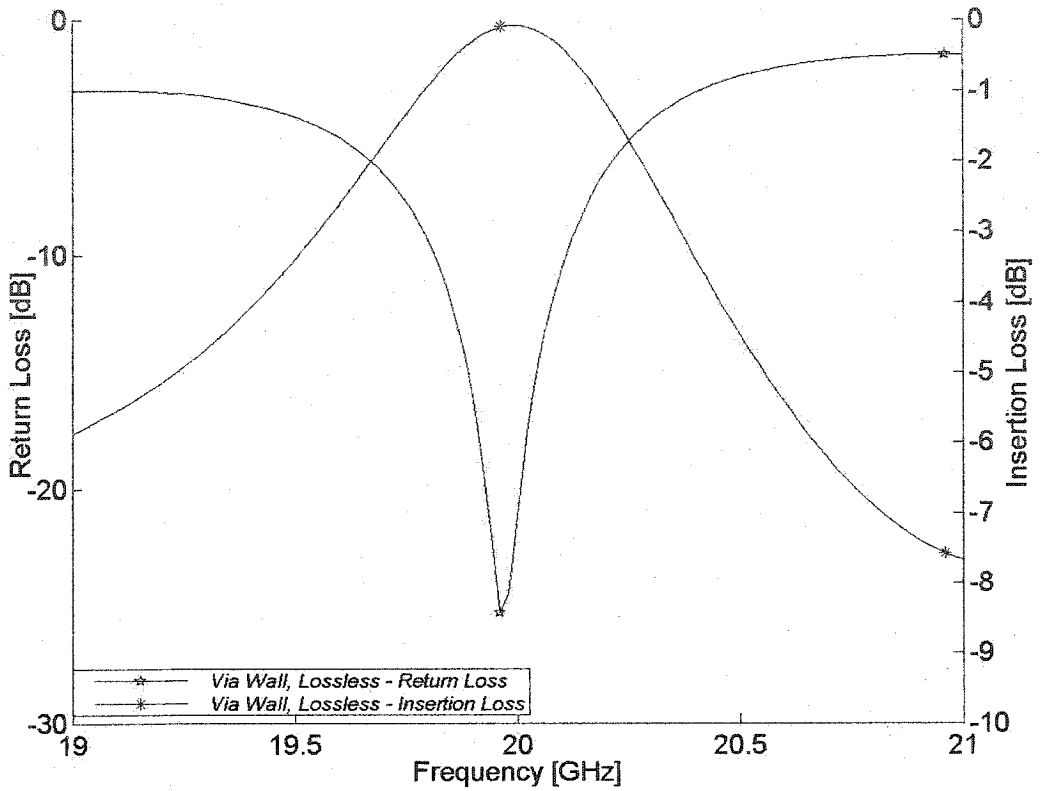

Figure 103: Simulation Results of the Via Walled Stripline Vertical Interconnect

3.11.4 Final Remarks on the Stripline to Stripline Interconnect

The design rules of creating a vertical transition between two striplines is very much the same as the one applied to the microstrip lines. As a matter of fact, everything that relates to the cavity design, slot positioning and the optimization of the open circuit stub length is identical. The only difference is the design of the stripline and ensuring higher order modes do not propagate. At microwave and millimeter wave frequencies, there is a high chance of launching parallel plate modes when stripline interconnects are designed. To suppress these TE_n and TM_n modes, via fences extending the length of the structure are placed between both sets of ground planes that define both input and output ports. Once the 'boxed' stripline structure is created, higher order modes are suppressed and the vertical interconnect design can be

completed. This is yet another degree of freedom a designer has to accommodate to various challenges of designing RF circuits.

3.12 CONCLUSIONS

In this chapter a novel vertical interconnect that uses a via walled aperture coupled rectangular cavity geometry has been developed. This interconnect is compatible with printed circuit technologies and is able to transfer a signal through many substrate layers. The geometry of the interconnect has been defined, and a design procedure formulated and applied. Detailed parametric studies of the behaviour of such interconnects (when used with microstrip input/output lines), and of the effect of dimensional variations on the performance, have been conducted using electromagnetic simulation. In addition, it has been demonstrated that such interconnects can be designed for those cases where the intput/output lines are not "in-line". Furthermore, the use of alternative via walled cavity shapes in the vertical interconnects has been discussed, as well as the possibility of using such interconnects with striplines as input/output lines. Chapter 4 describes the experimental implementation of a vertical interconnect.

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4. EXPERIMENTAL REALISATION OF A VIA-WALLED APERTURE-COUPLED CAVITY VERTICAL INTERCONNECT

4.1 INTRODUCTORY COMMENTS

This chapter is concerned with the experimental implementation of a vertical interconnect of the type discussed in Sections 3.2 through 3.8. Fabrication considerations are considered in Section 4.2. Measurement difficulties are discussed and illustrated in Section 4.3. A comparison of measured and predicted performance is provided in Section 4.4. The chapter is concluded in Section 4.5.

4.2 FABRICATION CONSIDERATIONS

The material used was CLTE (ceramic low thermal expansion) substrate material supplied by Arlon Microwave Materials [1]. The CLTE material has a relative dielectric constant of 2.94 and a loss tangent of 0.0025 at 10 GHz. We refer to the longitudinal section through the vertical interconnect, previously shown as Figure 23 in Section 3.2, and repeated here for convenience as Figure 104.

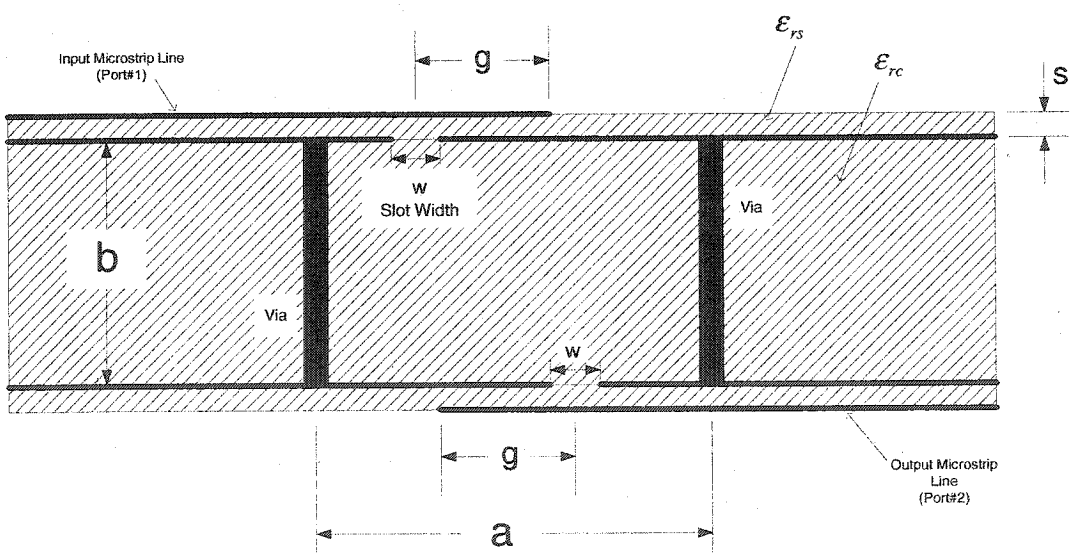

Figure 104: Section (through AA') of the vertical transition in Figure 22

In order to illustrate how the vertical interconnect is fabricated we suppose that the height is such that it can be realized using four substrate layers, as shown in Figure 105.

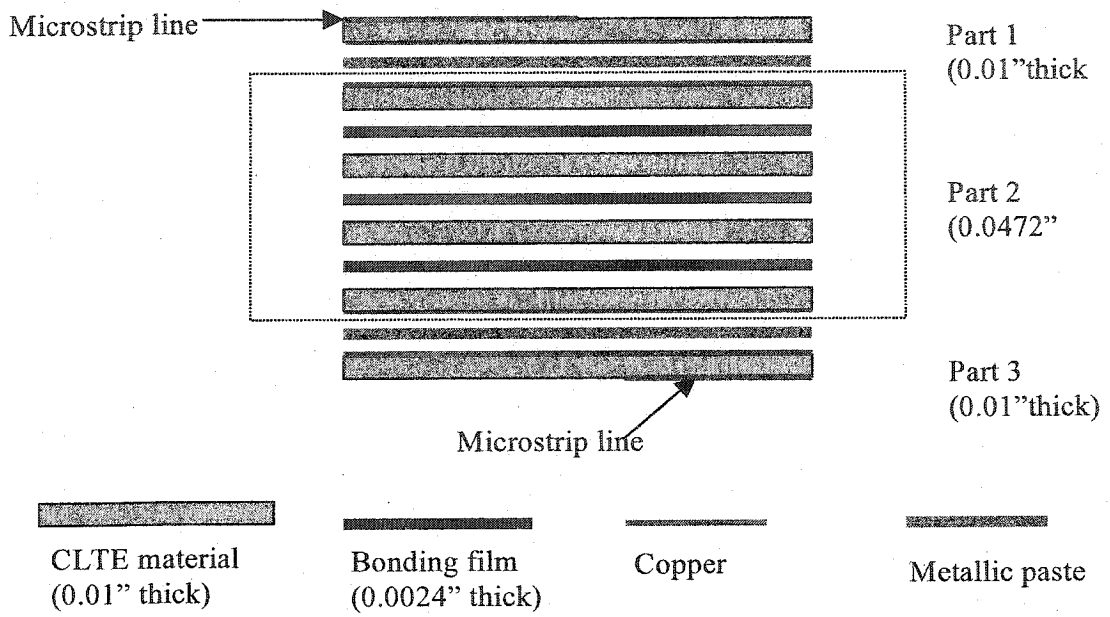

Figure 105: Formation of the Vertical Interconnect with the CLTE Material

Parts 1 and 3 are single layers of CLTE material (0.01" thick) with etched conductor on both sides. Part 2 is realized with four layers of CLTE material laminated using three CLTE-P bonding films. Parts 1, 2 and 3 are fabricated separately, and then are laminated together using a conductive paste.

Prior to lamination, a conductive paste was used to make contact between ground planes of the cavity and the microstrip lines.

An interconnect fabricated in the manner described in Figure 105 was realized. This is shown in Figure 106.

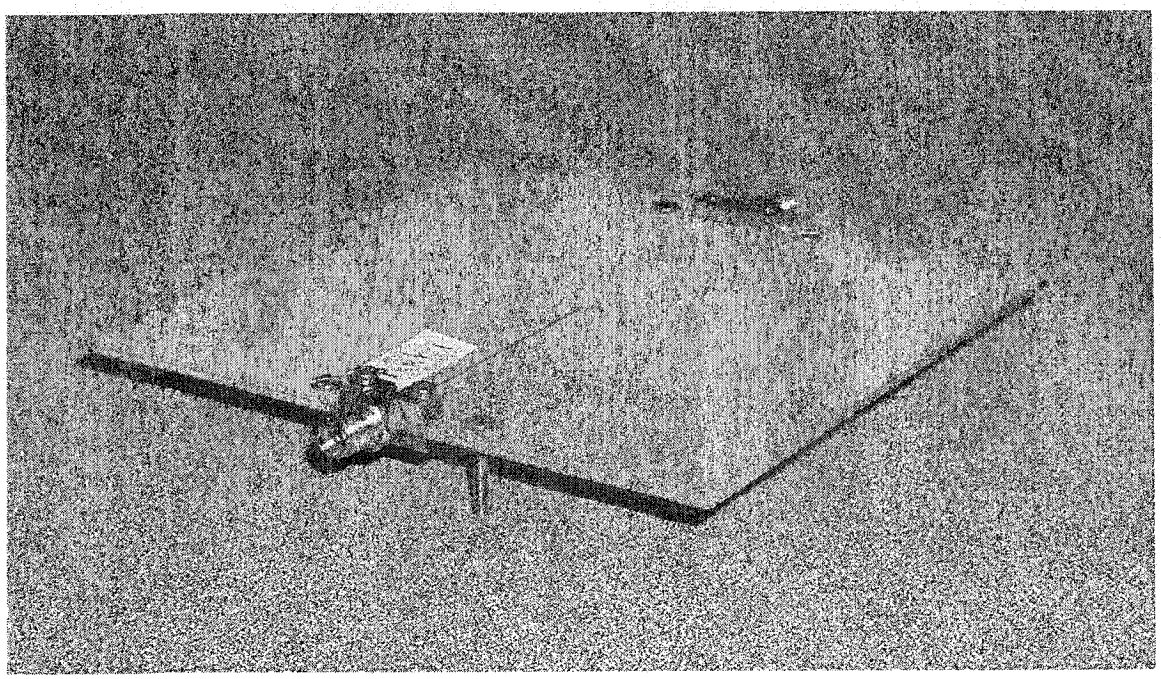

Figure 106: Fabricated Short Vertical Transition Circuit

Furthermore, X-ray imaging was done [2] in order to determine the success of the fabrication process. These are shown in Figures 107 through 109.

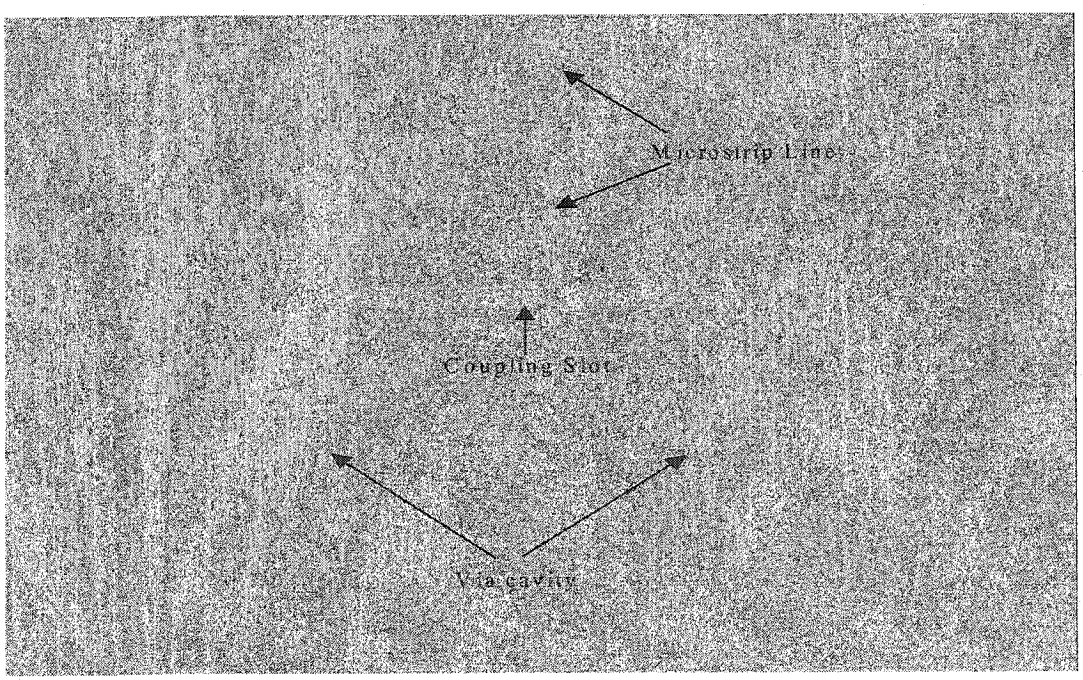

Figure 107: Top View of the Vertical Interconnect Circuit

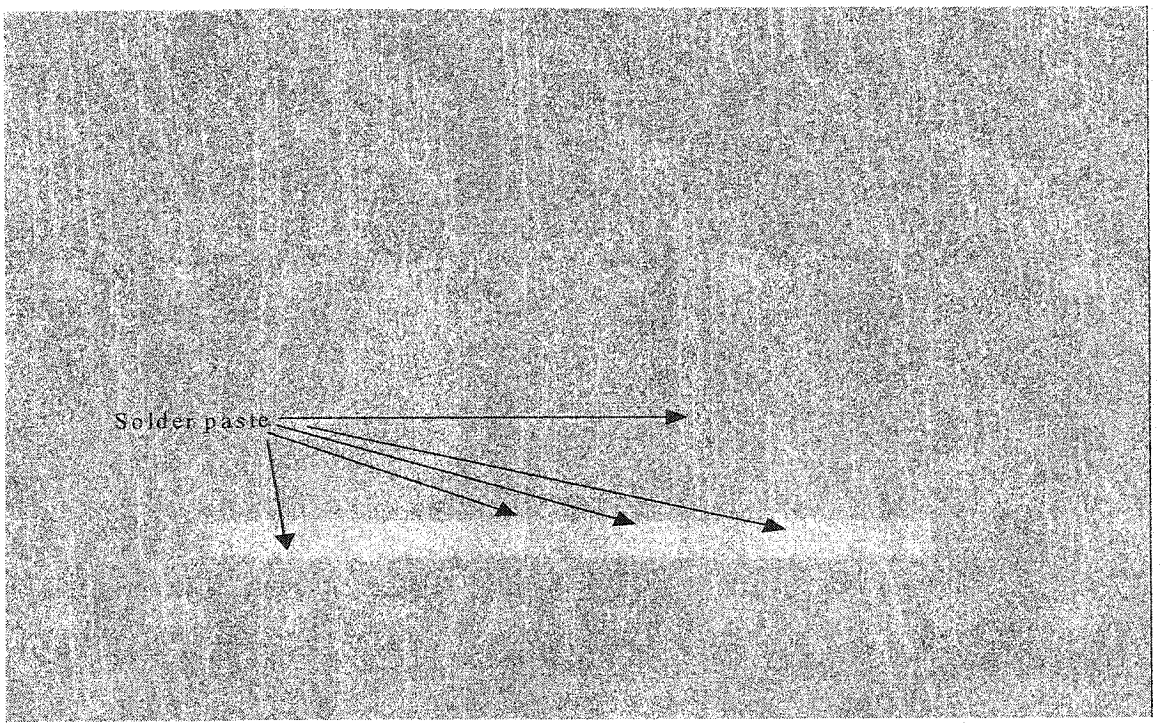

Figure 108: Cross-Section of the Microstrip Ground Plane

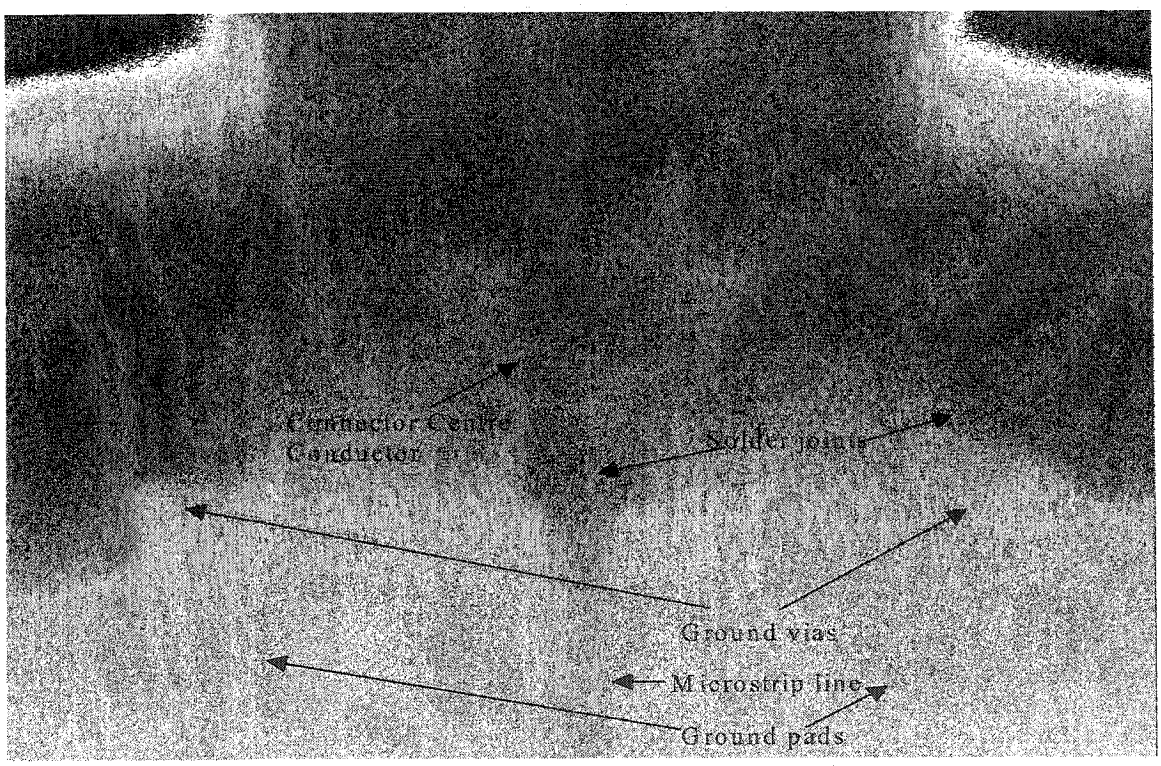

Figure 109: SMA Connector to Microstrip Line Transition

The following comments can be made about the fabricated vertical interconnect:

- The conductive paste has not been distributed consistently throughout the structure. As a result, there are irregularities in the final conducting structure, as can be seen in the form of dark spots in Figure 108. The inconsistent thickness of the paste in the vicinity of the coupling slots can lead to air gaps in what is supposed to be a single conducting layer. These imperfections can lead to a significant deterioration in the performance of the interconnect.

- Some of the paste is also present inside the coupling slots. This could significantly influence the interconnect performance.

- As indicated, the constructed ground planes are fabricated by joining two separate ground planes using conductive paste. The individual ground planes used here were 0.7 mil thick, so that when they are joined the final ground plane should be 1.4 mil think. However, the X-ray images showed that the final ground plane thicknesses were on the order of 4 mil. The conclusion is that there has been a lot of conducting paste placed "inside" the circuit.

- The position of the vias and the slots have been very well manufactured, within the tolerance of about $\pm$ 1 mil.

4.3 MEASUREMENT CONSIDERATIONS

Measurement of the performance of the vertical interconnect is a difficult task. It is necessary to use coaxial connectors in such measurements, as shown in Figures 106 and 110.

We note from Figure 104 that the ground planes of the input/output microstrip lines are not easily accessible. In order to provide ground connections between the outer conductors of the coaxial connectors and the ground planes of the microstrip lines, ground pads have been placed near the edge of the board with a single via making the connection between the pads

and the groundplane. This is depicted in Figure 110 and also in Figures A 2 and A 4 of Appendix A.

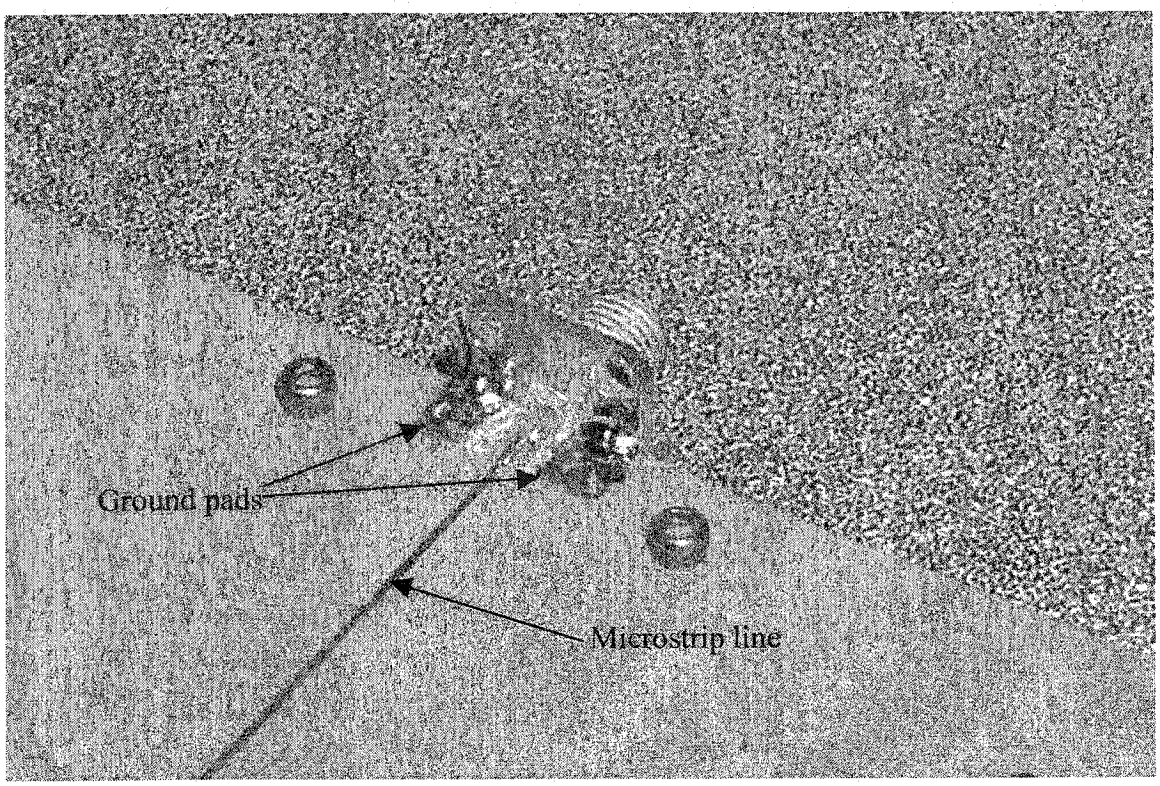

Figure 110: SMA Connector to Microstrip Line Transition

In order to establish the extent of the effect of the connectors and the above connector/microstrip transition on the measured performance, measurements of return loss and insertion loss were done for two different types of coaxial connectors. These were both of the SMA type, the one rated to 27 GHz and the other to 40 GHz. The measured return loss and insertion loss of the interconnect plus connectors are shown in Figures 111 and 112, respectively. There is a significant difference between these measured responses. The 40Ghz connector provides the better response.

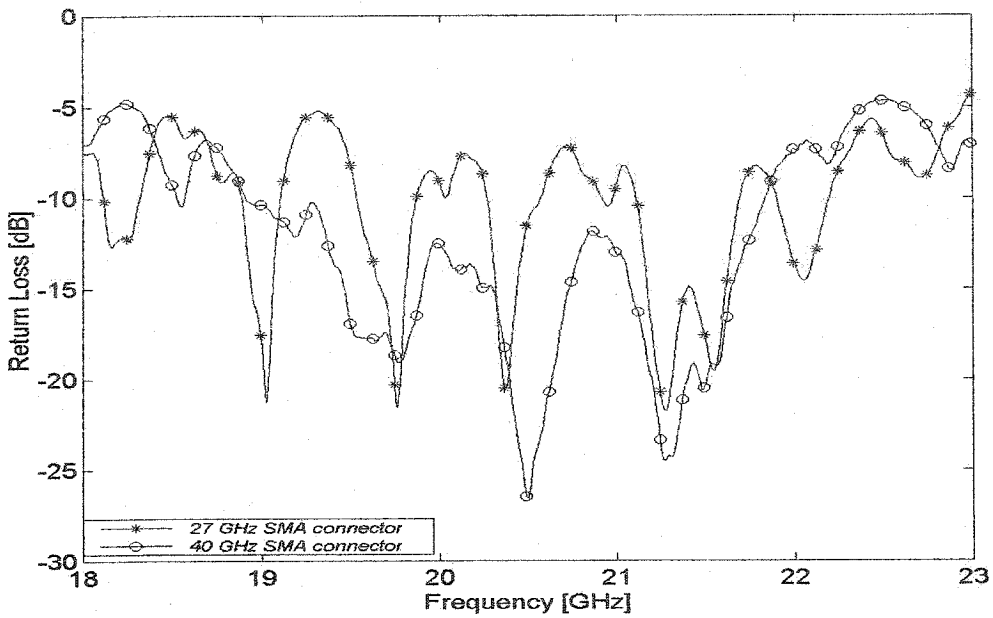

Figure 111: Measure Return Loss of the Fabricated Vertical Interconnect Circuit

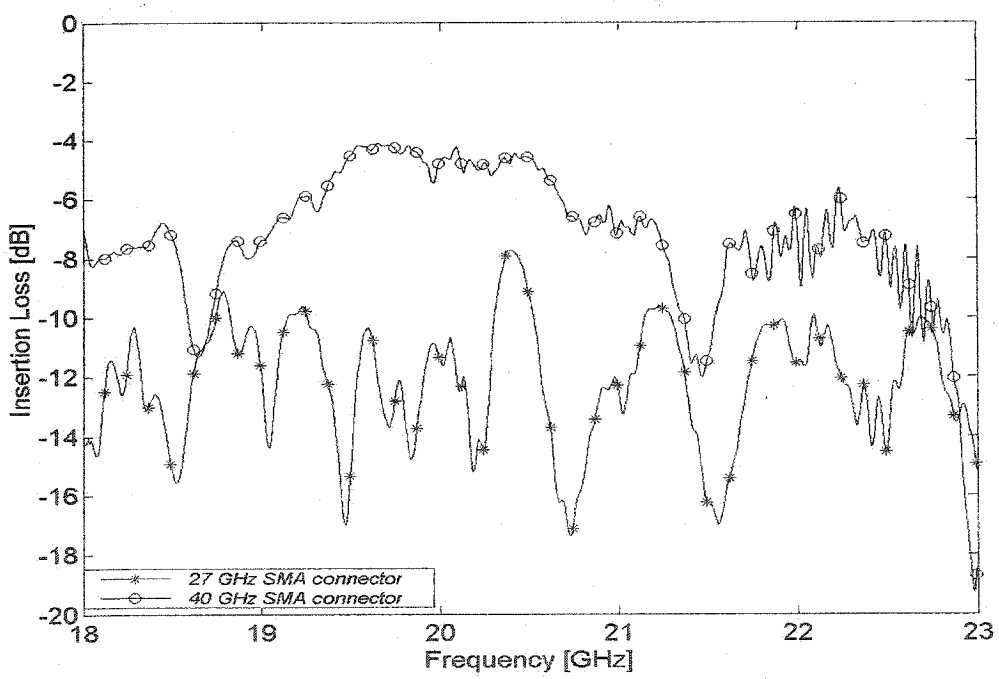

Figure 112: Measured Insertion Loss of the Fabricated Vertical Interconnect Circuit

4.4 EXPERIMENTAL VERTICAL INTERCONNECT DESIGN

The reader is once again referred to Figure 104, as well as to Figure 113, for the symbols used to denote the dimensions of the vertical interconnect.

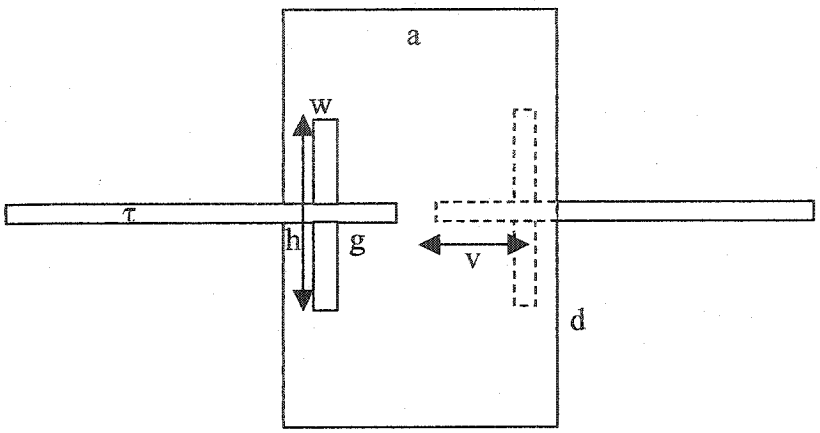

Figure 113: Top View of the Solid Cavity Wall Vertical Interconnect

The vertical interconnect selected for experimental verification was chosen to have the vertical dimension ***b*** = 52 mil. The material used was the CLTE substrate material previously mentioned in Section 4.2. The copper layers on this material have a thickness of 0.7 mil, and the substrate layers a thickness of 10 mil.

If a center frequency of 20.7GHz is chosen, the design steps outlined in Section 3.2 provide initial values for the cavity dimensions of ***a*** = 176 mil and ***d*** = 500 mil; recall that these are based on an unloaded cavity analysis and will need to be altered later in the design process. With an ***s*** = 10 mil substrate, the conductor width of a microstrip line is determined to be 25.48 mil for a characteristic impedance of 50Ω. This can be used to compute the λ_g on the microstrip lines and hence find the initial length ***g*** = $\lambda_g/4$ = 149.58mil of the open circuit stubs.

The above interconnect was modeled using HFSS. The model included the fact that the ground planes are 0.7 mil thick. In order to have a computationally feasible model the connectors were not included, and thus the details of the connector/microstrip line transition were not included either.

The vertical interconnect design was "manually" optimized using the above electromagnetic model with a solid wall rectangular cavity specified. The optimized design had the following dimensions: a = 160 mil, d = 500 mil, h = 200 mil, w = 40 mil, g = 95 mil, v = 60 mil.

As outlined in Section 3.2, the last step in the design is to replace the solid cavity walls with via fences. Vias having a diameter of 20 mil were used. The outline of the cavity where vias are to be placed needed to be increased by a factor of 10.52 mil, as per design guidelines of Section 3.2. Vias were placed 42.8 mil apart (center to center distance) along dimension a (total of five vias) and 39.4 mil along dimension d (total of 15 vias).

The computed performance of the above interconnect is shown in Figure 114.

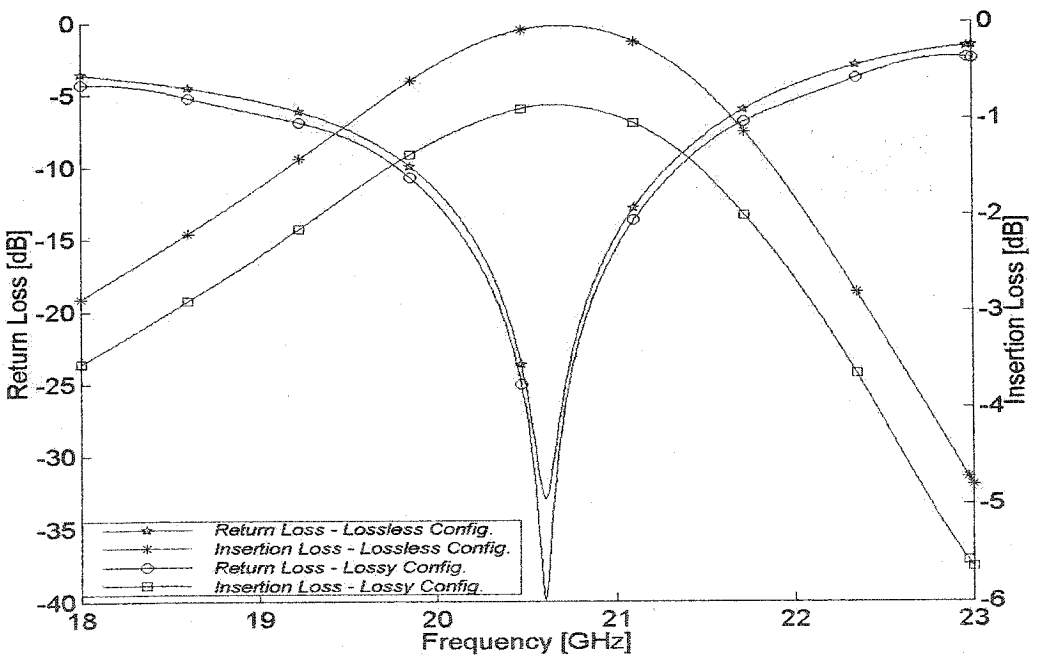

Figure 114: Computed Results for the Via Walled Cavity Interconnect

These reveal that the vertical interconnect design has an impedance bandwidth of about 7 %. The effects of dielectric and ohmic losses are clear from the computed performance shown.

The above vertical interconnect was realized with four layers of CLTE material laminated using five CLTE-P bonding films of identical dielectric properties and thickness of 2.4 mil. The microstrip lines were fabricated separately and then laminated to the "internal" layers using a conductive paste.

X-ray images were taken of the fabricated interconnect. These revealed that the dimension ***b*** was about 47.2 mil instead of the specified 52 mils. However, the electromagnetic simulation shows that the effect on the predicted performance is small, as illustrated in Figure 115.

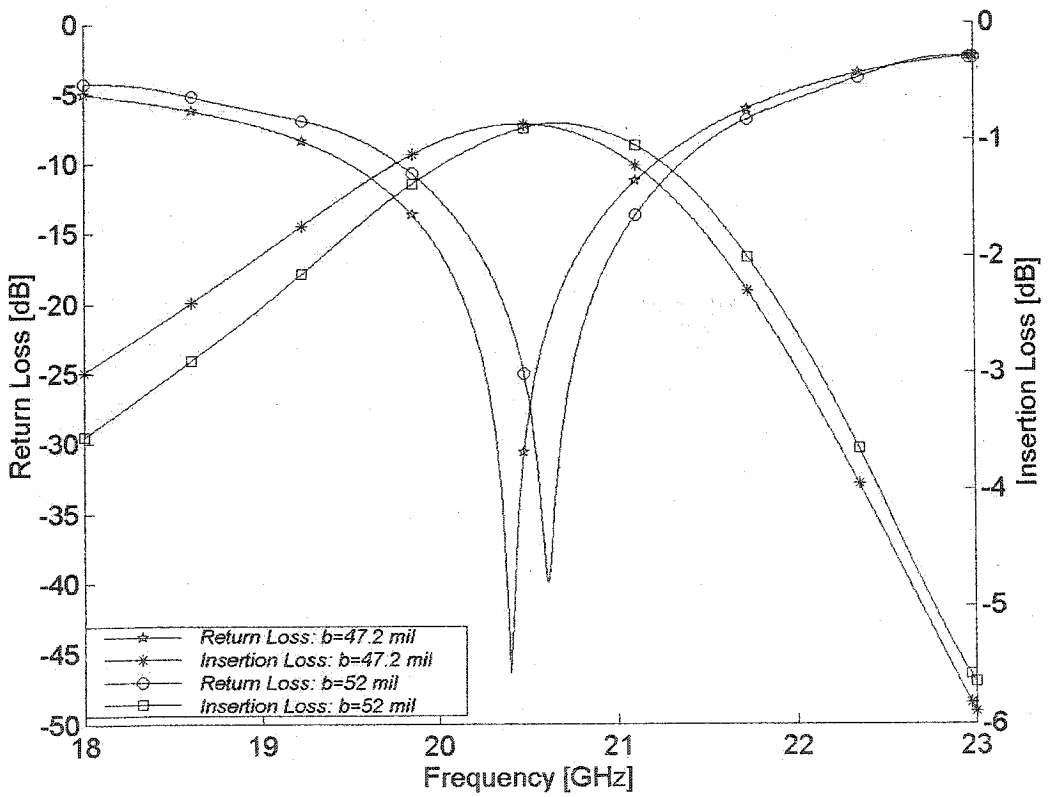

Figure 115: Computed Results Comparison between the two Via Walled Interconnects with Different Vertical Dimension, *b*, and with Losses Included in the Simulations

It is clear that the only effect this has on the design is a small shift in the centre frequency from 20.7GHz to 20.4 Ghz. Furthermore, the fabricated circuit revealed that the dimension ***d*** was 3 mil below the specified 510.25 mil. Simulation once again shows that (as expected from

Section 3.7.2) this dimension change does not have a profound effect on circuit performance. The widths of the microstrip lines were found to be 24 mil, which is about 1.5 mil less than that intended and hence results in a slightly higher line impedance.

A comparison of the predicted and measured performance (using the 40GHz connectors referred to in Section 4.2) for this vertical interconnect is shown in Figures 116 and 117.

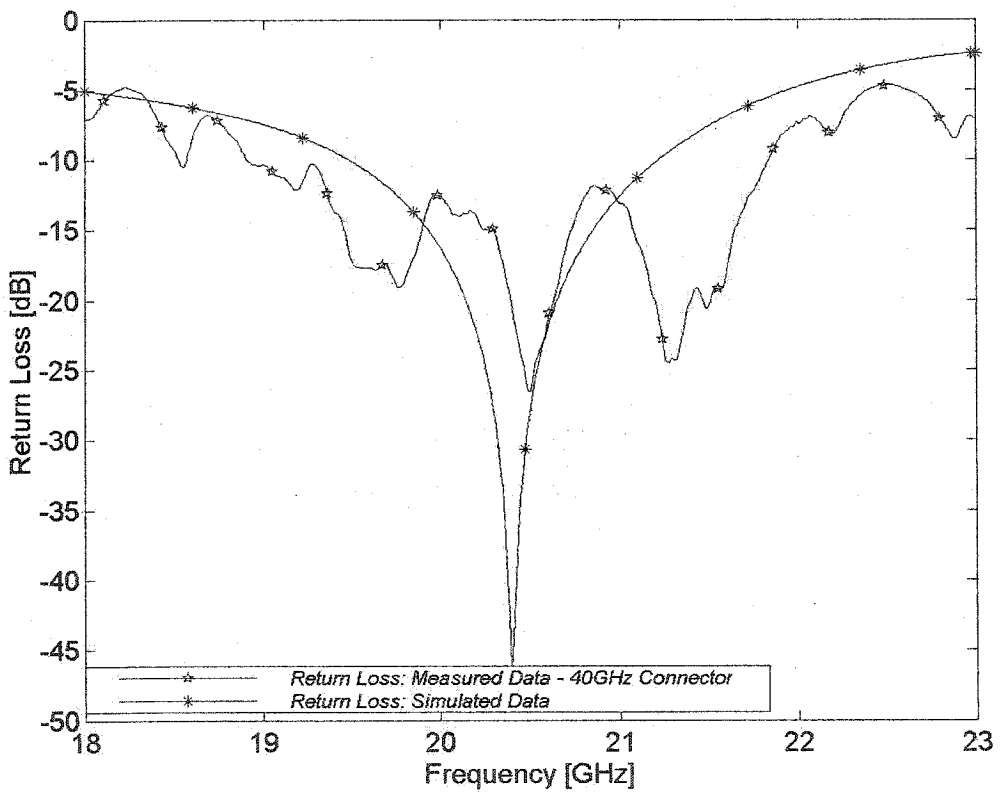

Figure 116: Return Loss of the Simulated and Measured Data for the Via Walled Cavity Interconnect

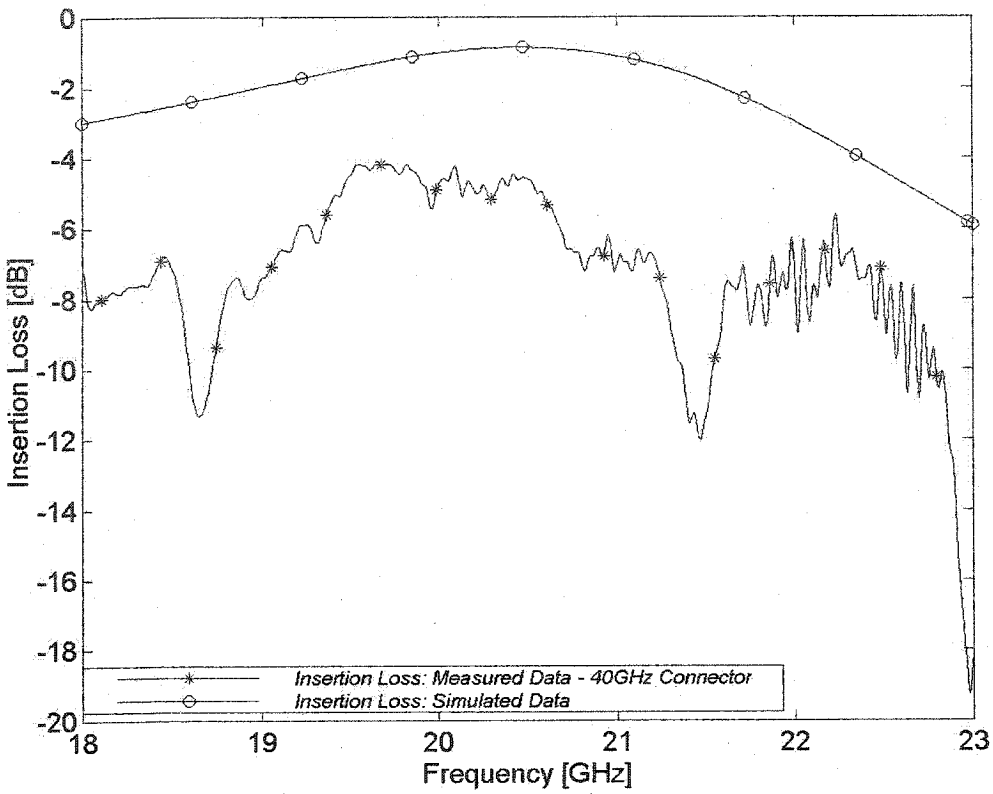

Figure 117: Insertion Loss of the Simulated and Measured Data for the Via Walled Cavity Interconnect

The predicted performance is that obtained with the values of ***b*** and ***d***, as well as the microstrip line widths, set equal to the observed values mentioned in the previous paragraph. There is reasonable agreement between the computed and measured return loss. The predicted centre frequency was 20.4 GHz, while the measured value is 20.5 GHz. This shift could be due to the fact that we used a permittivity value for the substrate material that was quoted at 10GHz; a decrease in this value at higher frequency would cause an increase in the centre frequency.

The comparison between the predicted and measured insertion loss is not as good. Initially it was thought that the presence of the ground pads might be partly responsible for the degraded performance, these not having been included in the original simulations. However, when added to the electromagnetic simulation model these were observed to have little effect

on the interconnect performance. There could be several other reasons for the discrepancy between the simulated and measured insertion loss. Firstly, the fabrication effects mentioned in Section 4.2 were present on this interconnect, and will influence the measured performance. Perhaps most important is the fact that the connector effects were not included in the simulation, and we have been unable to "calibrate them out" [3] or "gate them out" [4] in the measurements obtained here. An attempt was therefore made to estimate such effects. Data on the 40GHz connectors [5] suggests that, at 20.5 GHz, each connector contributes an insertion loss of 0.5433 dB. If the loss tangent of 0.0025 at 10GHz is extrapolated to 20.5 GHz, the additional interconnect loss can be estimated at 1.1dB. Lastly, the lengths of the input/output microstrip lines were larger on the measured interconnect than that which was simulated. It is possible to estimate that this increased length leads to an insertion loss increase of 0.236 dB per microstrip line. If the above insertion loss contributions are added to the curve in Figure 117 we obtain a "corrected" measured insertion loss shown in Figure 118.

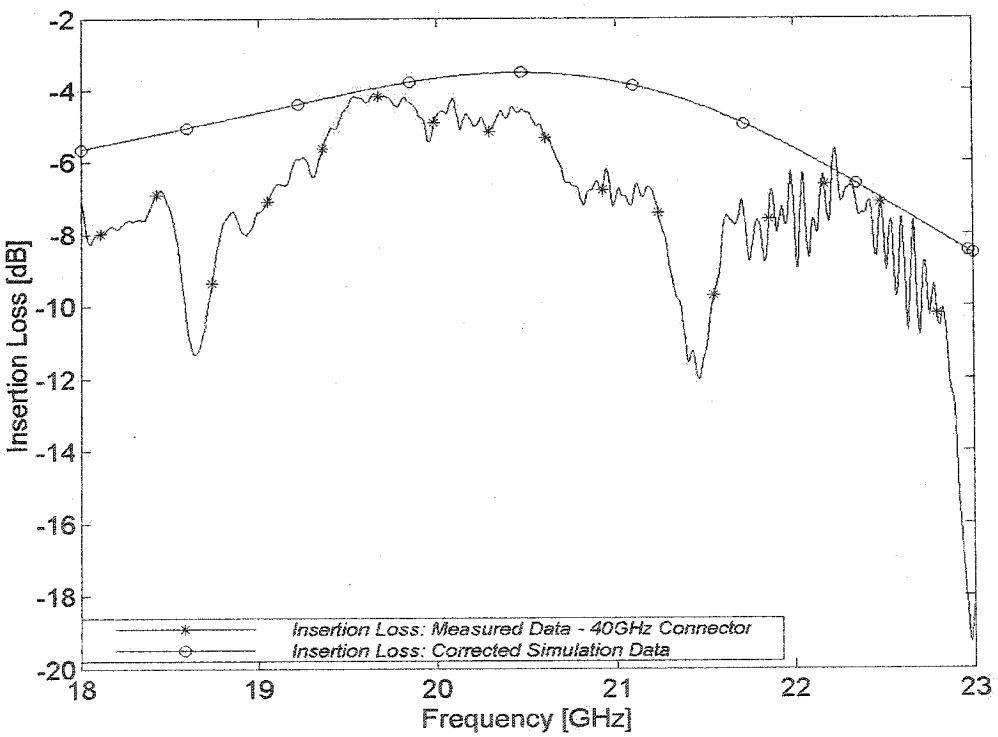

Figure 118: Insertion Loss of the Measured and Corrected Simulated Data for the Via Walled Cavity Interconnect

4.5 CONCLUSIONS

This chapter has presented the design, predicted performance, and measured performance of a vertical interconnect that was fabricated. The fabrication imperfections were discussed, and the measured performance was compared to that obtained using electromagnetic simulation. The measurement difficulties were pointed out. Although commercial test fixtures exist for removing connector effects in standard single-layer microstrip structure measurements, these cannot be used directly for the situation here where the input/output microstrip lines are on different layers of a multilayer structure. A completely satisfactory experimental measurement of the interconnect behaviour was not possible.

4.6 REFERENCES FOR CHAPTER 4

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[2] *Breconridge*, 500 Palladium Drive, Ottawa, Ontario K2V1C2, Canada.

[3] Product Note 8510-8A, *Network Analysis : Applying the 8510 TRL Calibration for Non-Coaxial Measurements*, Agilent Technologies.

[4] *Time Domain for Vector Network Analyzers*, Application Note, Anritsu, Microwave Measurements Division, 490 Jarvis Drive, Morgan Hill, CA 95037-2809, USA (www.us.anritsu.com).

[5] Microminiature Coaxial Connectors, SBMO Series, Radiall S.A., 300 Long Beach Blvd, Stratford, CT 06615.

5. GENERAL CONCLUSIONS AND FUTURE WORK

The principal contributions of this thesis are as follows:

- A new via walled cavity vertical interconnect has been described for the first time. It is compatible with microwave/millimeter wave circuit fabrication technology already in use or under development (eg. LTCC). In addition to the case where the input/output transmission lines of the interconnect are parallel and in-line, it has been shown that it is possible to realize interconnects where these are parallel but offset from each other, or even spatially orthogonal to each other. This ads a significant amount of flexibility to this novel vertical interconnect.

- A parametric study of the effect of the interconnect dimensions on the insertion loss and return loss performance has been undertaken using detailed electromagnetic simulation. The modeling methods have been validated by comparing the predictions of methods based on different mathematical approaches (*viz.* integral equation based methods versus differential equation based methods).

- A structured design procedure for the vertical interconnect has been developed.

- Electromagnetic simulation has been used to determine the effects of dimensional and positional tolerances on the performance of the interconnect. In this manner, it has been possible to establish that such interconnects are viable at microwave and millimeter wave frequencies.

- A specific vertical interconnect has been fabricated and its performance measured.

Future work might include the following:

- The development of an improved measurement technique (for input/output microstrip lines on different layers of a multilayered structure) in order to remove the effects of connectors.

- A study of the coupling between two vertical interconnects closely located on the same printed circuit board.

APPENDIX A – Detailed Manufacturing Circuit Schematics of the Vertical Transition

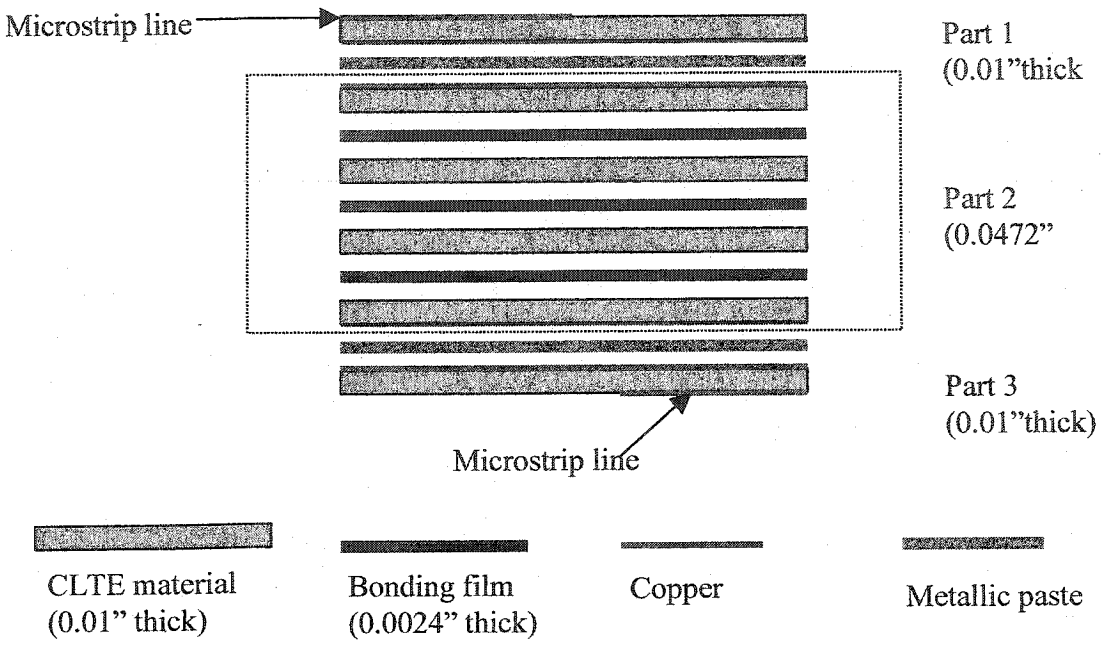


Figure A 1: Composition of the Vertical Interconnect Circuit; Formation of the *b* dimension

Parts 1 and 3 are single layer of CLTE material (0.01" thick) with the etched conductor on both side. Part 2 is realized with four layers of CLTE material laminated using three CLTE-P bonding films. Parts 1, 2 and 3 are fabricated separately, and then are laminated together using a conductive paste.

Next, we illustrate the cross sectional views of all the layers of the printed circuit board along with all manufacturing details in required to build the vertical interconnect circuit, i.e. part 1, part 2, and part 3 of Figure A 1.

Part 1

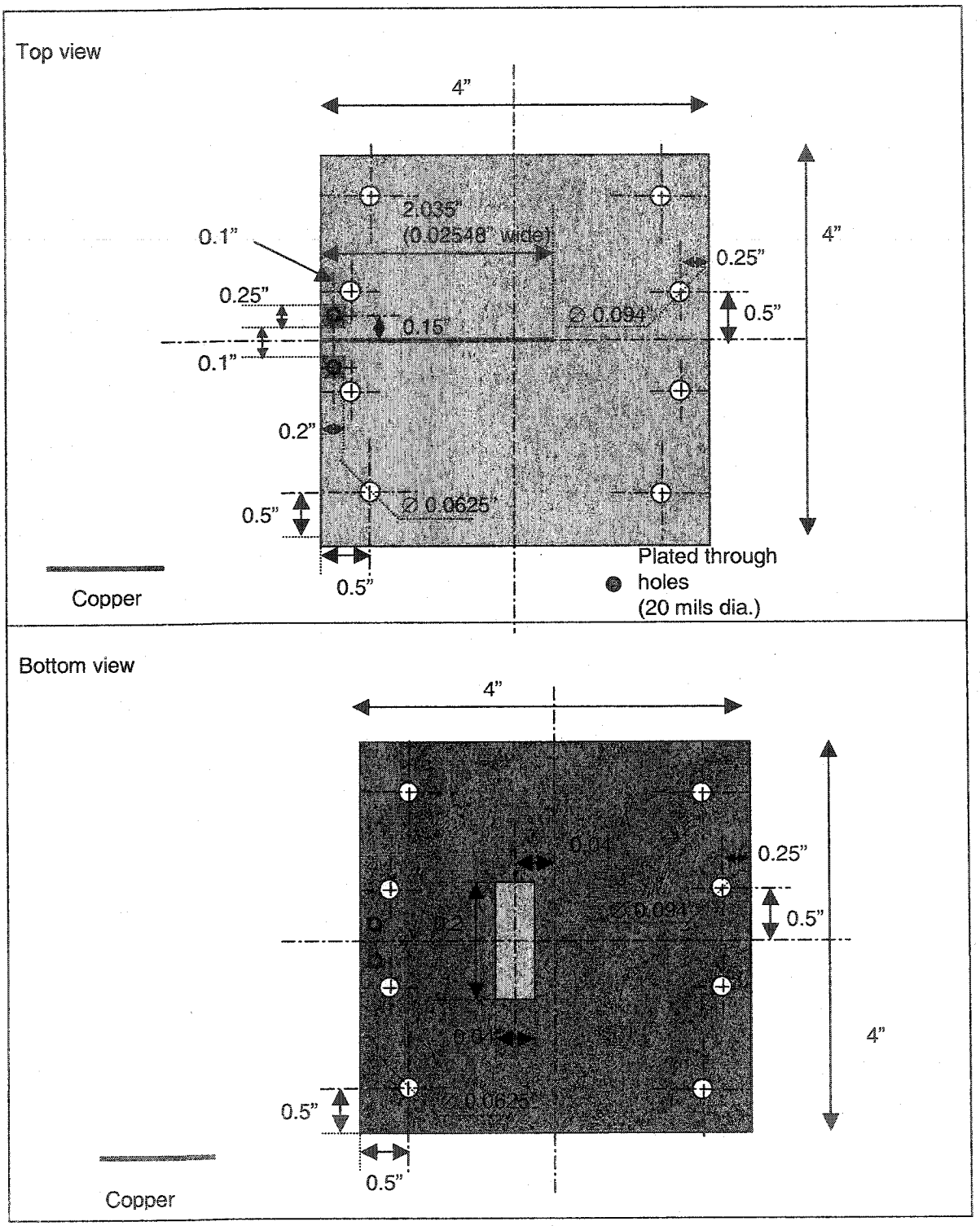
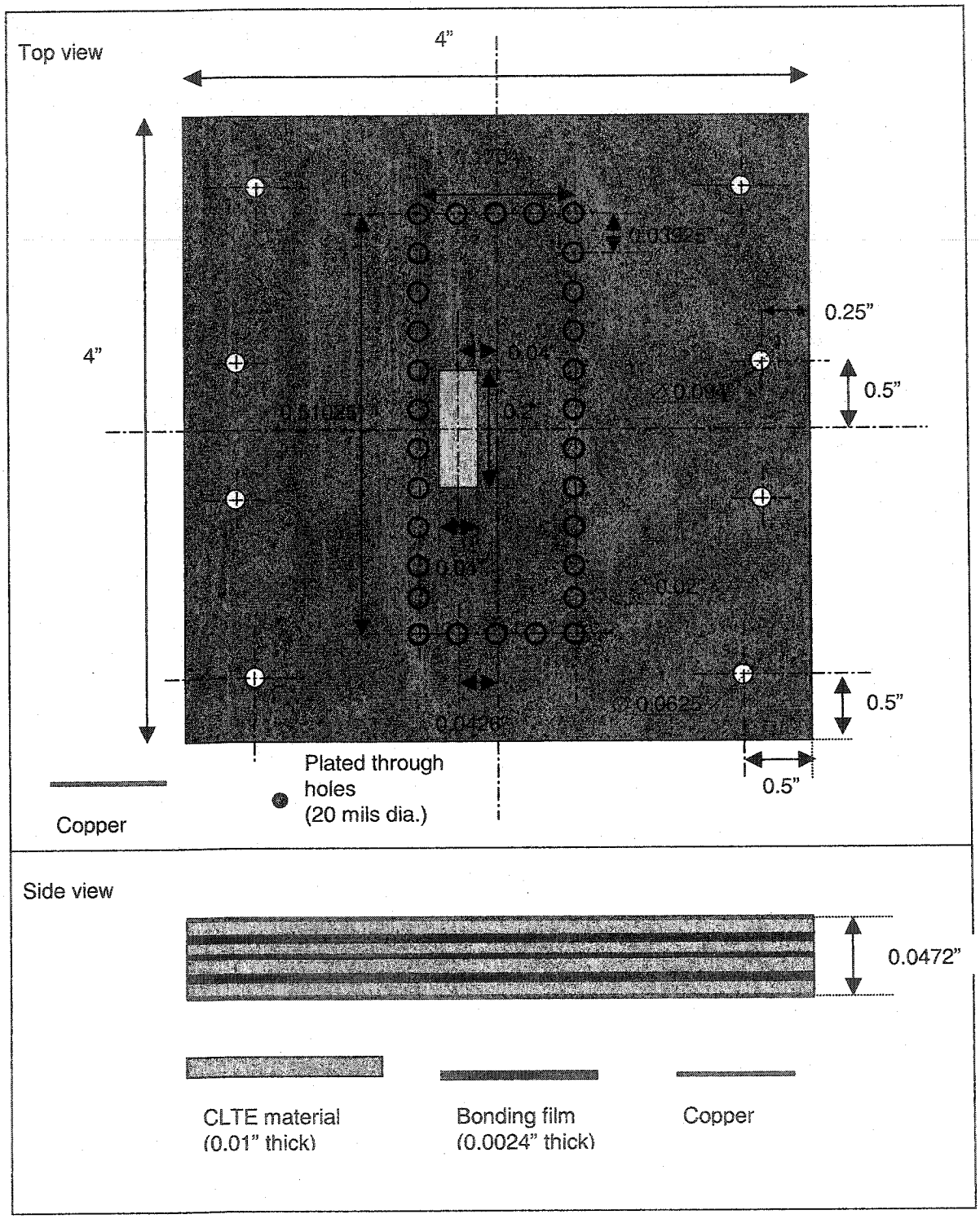


Figure A 2: Manufacturing Details of the Part 1 Vertical Interconnect Design

Part 2


Top view
4"
4"
0.25"
0.5"
0.5"
0.5"
Plated through holes (20 mils dia.)
Copper
Side view
0.0472"
CLTE material (0.01" thick)
Bonding film (0.0024" thick)
Copper

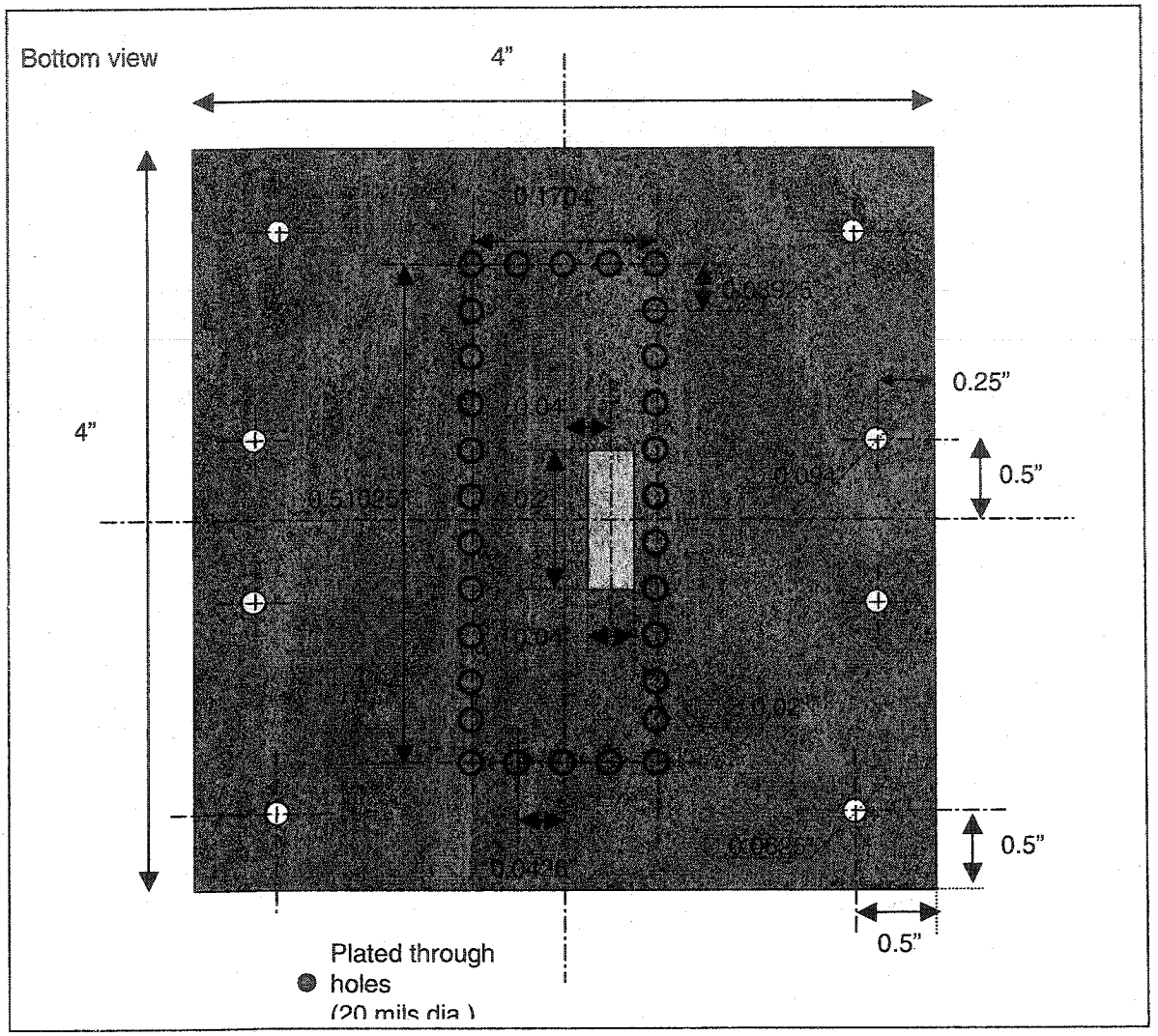


Figure A 3: Manufacturing Details of the Part 2 Vertical Interconnect Design

Part 3

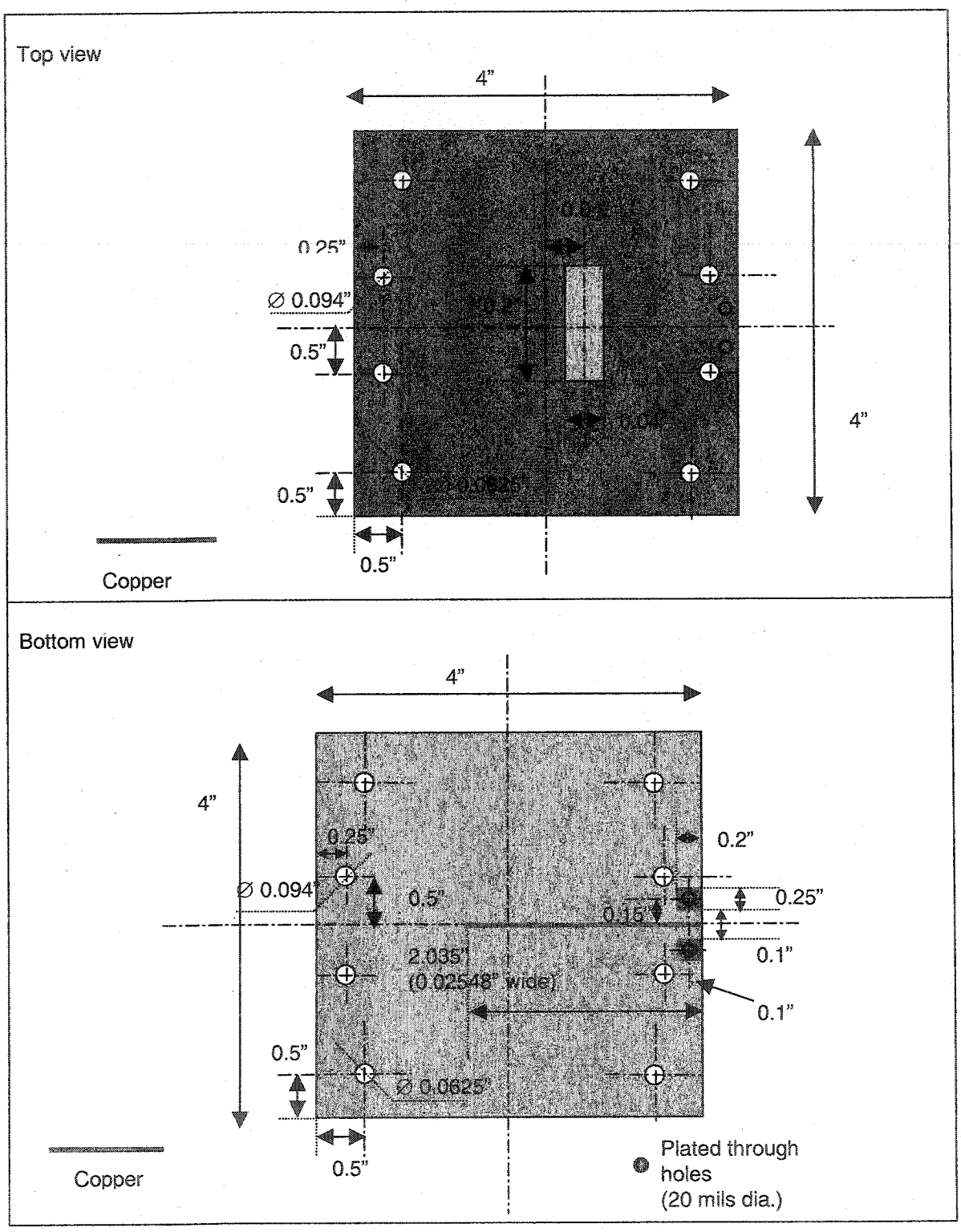


Figure A 4: Manufacturing Details of the Part 3 Vertical Interconnect Design

Metallic rectangular pieces

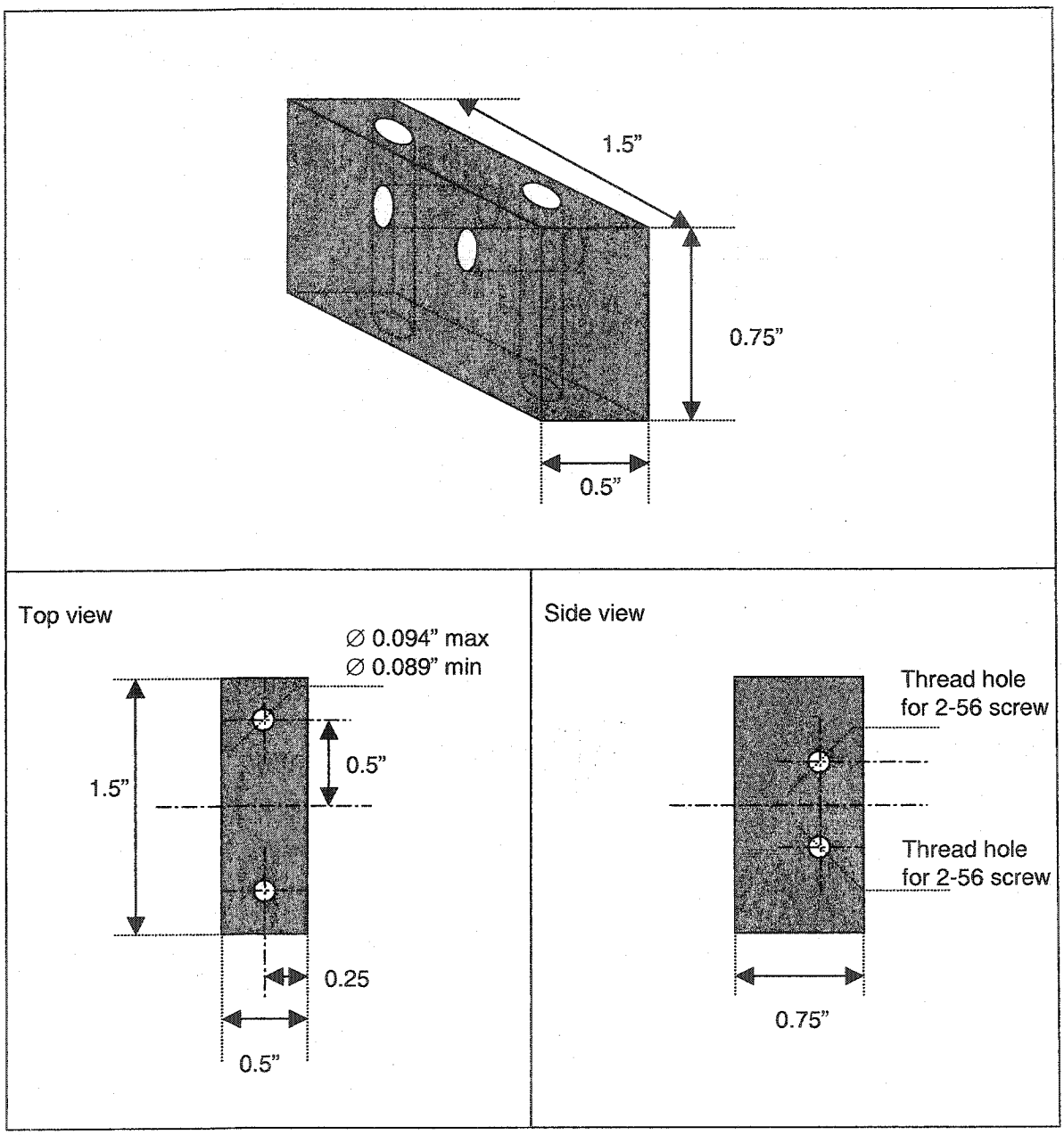


Figure A 5: Manufacturing Details of the Metallic Parts used to Fix the SMA Connectors to the Board

APPENDIX B - ELECTROMAGNETIC MODELING OF INTER-LAYER TRANSITIONS

In this thesis, two methods are used in determining electromagnetic field solutions and providing scattering parameters for all vertical interconnect configurations. First, the finite element method (FEM) is applied in all problems solved using HFSS [1]. The FEM method has a differential equation approach as its basis. Second, the method of moments (MoM) is employed in all problems solved using Ensemble [2]. This method is based on an integral equation approach. Since these are the only simulation tools used in this study, it is worth presenting a high level description of each of the methods used and the way in which the scattering parameters are extracted from field solutions.

B.1 FINITE ELEMENT METHOD (FEM)

This method is based on solving the Maxwell's equations in a point form, i.e. the differential form. In this form, the electric and magnetic fields can be determined by solving the vector wave equation subject to physical and absorbing boundary conditions. This method provides a complete solution of the electromagnetic fields. For open problems, such as the configuration presented in this thesis, in which radiating waves propagate outward to infinity, the finite element method can only be used once the infinite domain is finite. Therefore, an artificial rectangular boundary is constructed which encloses the structure on which the absorbing boundary or perfectly matched layer/absorber conditions are imposed, as described in [3-5]. A rectangular enclosure for the inhomogeneous vertical interconnect structure must be formed for HFSS to perform the analysis. This defines where the absorbing boundary conditions are set.

In this thesis, the absorbing radiation boundary extends passed the interconnect structure about one quarter of the guided wavelength in all three dimensions. The top and bottom excess space is air, whereas the lateral plane contains the printed circuit board where the vertical interconnect circuit resides. This is the optimum size of the fictitious enclosure so that computation time is minimized and the simulation results are not compromised.

In order to find the optimum simulation setup, it is a good practice to run a simulation using HFSS and then setup exactly the same problem in Ensemble, where different method (method of moments) is used to produce the same results. When both sets of electromagnetic fields data converge, one is reassured that the size of the circuit enclosure is largely adequate and does not affect the final result. Alternatively, one can make the box very large (many wavelengths long), thus ensuring that the field solution is accurate. This, however, may result in excessive computation time, which may not be practical when a design is to be developed in a timely manner.

The vertical interconnect circuit presented in this thesis is classified as a driven problem where input/output ports are formed by waveguides through which the incident fields are applied. Weighting and expansion functions are applied to the vector wave equation to form the "weak form" of the differential equation. The structure is then meshed and the electromagnetic fields are approximated using selected vector expansion functions along with the corresponding unknown coefficients. For 3D problems, a tetrahedron is commonly used as an element that makes up the overall region where the field solution is sought. Also, higher order vector elements are often used to form the expansion and weighting functions in order to better approximate the electromagnetic field solutions, as described in [6-7]. Sparse matrix equations result and unknown electric or magnetic fields are determined. Once the solution is obtained, scattering parameters may be computed or simply extracted from the resultant matrix equations, as presented in [6]. The analysis must be repeated with the incident field at another port if the scattering parameters are to be computed for that port. In this case, only the excitation vector changes in the repeated analysis.

B.2 METHOD OF MOMENTS (MOM)

Using an integral equation approach, this method uses the electric and magnetic current sources to evaluate the electromagnetic fields in a specified region, as in [8-11].

Ensemble implements this method to solve the electromagnetic field problems. It is designed specifically to work with printed circuits. It also uses conducting ground planes and substrate layers that are infinite in extent. This is because the selected Green's function takes into account the presence of these planes and layers. As a result, conducting planes and substrate layers do not need to be meshed. This leads to a problem of less unknowns and therefore shorter computation time.

In the application of the MoM, the equivalence principle is applied, where the conducting or dielectric scatterers (any objects placed in an unbounded medium) are replaced by equivalent electric or magnetic sources radiating in the unbounded region. The equivalent sources radiate in the presence of the embedding medium that constitutes the original environment. In this circuit configuration, the equivalent electric currents are placed along via walls and equivalent magnetic currents represent the coupling apertures. The microstrip lines are also replaced with the equivalent electric currents in the analysis. Both input/output ports of the two-port network constitute the impressed sources that generate the incident electric and magnetic fields. Once this is done, boundary conditions are applied and the integral equations are formulated. The remainder of the analysis is quite similar to that of the finite element method where surfaces are meshed, unknown currents are assigned and expansion functions are selected. The integral equation is then discretised by applying the weighting functions and forming a full system matrix. Once the solution is obtained, the electromagnetic fields can be determined.

For this particular circuit configuration, the MoM is computationally more advanced than the FEM. This is simply due to the fact that there are fewer unknowns to be solved when only the conductor and aperture surfaces are being meshed, rather than having to mesh an entire 3D region, as implemented in HFSS. This conclusion is also supported by the comparative analysis by Pozar in [12]. In this thesis, however, these methods are used for the purpose of validating some of the results and establishing a good baseline for the analysis of the proposed vertical interconnect.

B.3 CONVERGENCE OF THE SIMULATION RESULTS

Numerical analysis is only valid when the final solution satisfies Maxwell's equations. In order to ensure that the meshing is sufficient to obtain the correct results, a certain convergence criterion needs to be met. It is unclear as to what type of measure for convergence is employed by Ansoft, as it is information that can not be easily obtained. However, one can assume that certain parameters (such as the electric or magnetic fields, or scattering parameters) are being evaluated every time the meshing is enhanced. Sophisticated tools such as HFSS and Ensemble must have an adaptive meshing where the regions containing large errors are meshed more finely than those that reach convergence much faster. In either case, all simulation results presented in this thesis have been obtained by performing adaptive sweeps with convergence criterion of 1%. This is adequate as known results have been successfully reproduced in Chapter 2.

B.4 SCATTERING PARAMETERS

The scattering parameters are used in evaluating the performance of an N-port network. In this thesis, N = 2. These parameters relate the voltage waves incident on the ports to those reflected from the ports, as detailed in Chapter 4 of [13]. In the case of a reciprocal two port network, the return loss (reflection coefficient looking into one port, and a matched load terminating the second port) S_{11} and S_{22} are the same in theory. This argument also applies to the insertion loss (transmission coefficient from one port to the other), S_{21} and S_{12}.

In order to apply these concepts, Figure B 1 shows the location of the input and output ports.

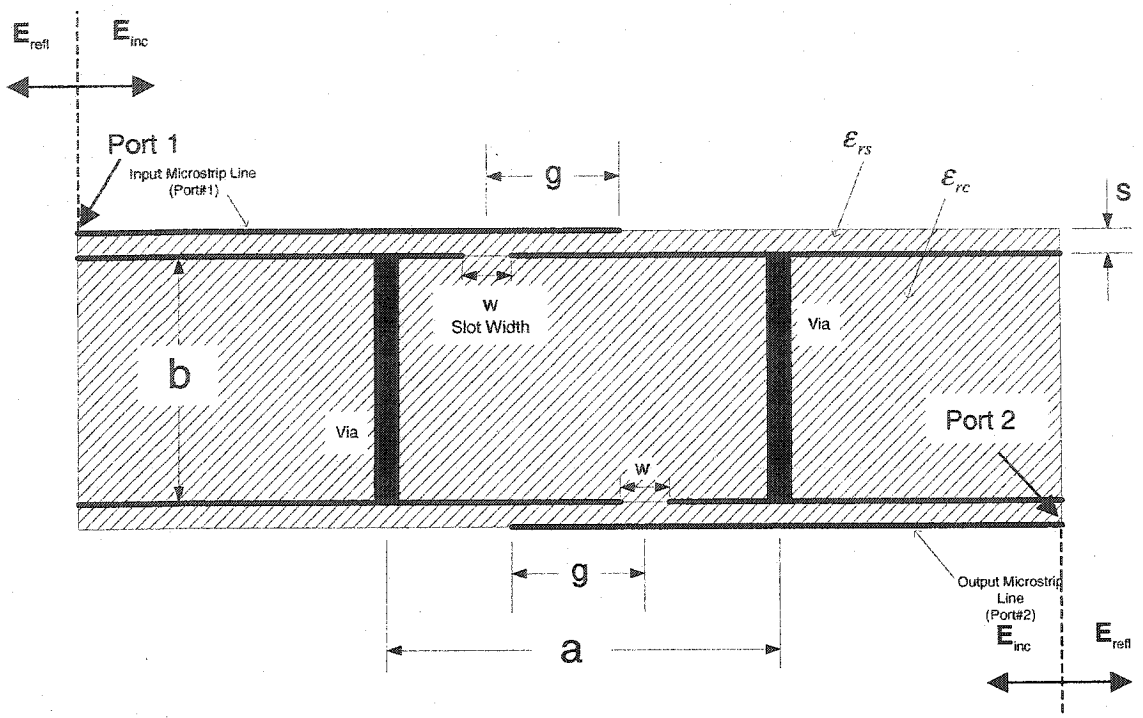


Figure B 1: The Definition of Ports of the Vertical Interconnect

With the electromagnetic fields computed using either the finite element method or the method of moments, one can compute the reflection and transmission coefficients by evaluating the incident and reflected electric fields at ports 1 and 2, as shown in Figure B 1 and performing a simple calculation, as pointed out in Chapter 4 of [13]. If the microstrip line is long enough, a measure of current standing wave at each port will lead directly to the scattering matrix, as depicted in [8]. This is often applied when the method of moments is used as the engine in the analysis. When FEM is used, scattering parameters may be extracted from the resultant matrix equations, as presented in [6].

Also, the return and insertion losses are most often expressed in decibels by performing the following calculation: $S_{11/22} = 20 \cdot \log_{10}(\Gamma)$ and $S_{21/12} = 20 \cdot \log_{10}(T)$.

Finally, the phase of the scattering parameters depends heavily on the reference plane chosen for a particular measurement. In the lossless case, this results in a rotation of the response on a Smith chart. In this work, the concern is not in the phase rotation, but the magnitude of a parameter and its variation with frequency.

B.5 REFERENCES FOR APPENDIX B

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