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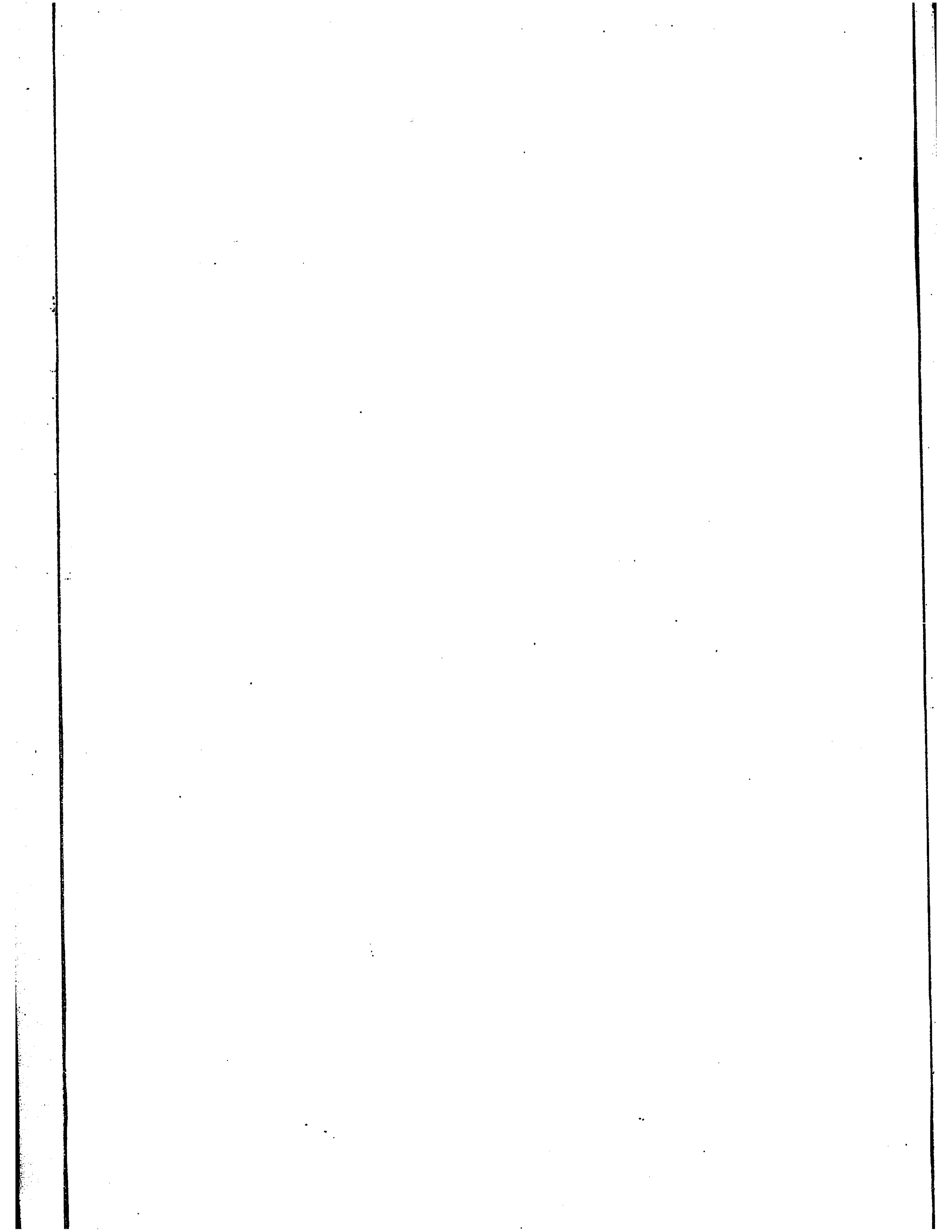

ARCS-THESES

Yield Study of GaAs VLSI Circuits

By

Younes Djadi, Dipl. of Eng.

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Department of Electrical Engineering
Faculty of Engineering
University of Ottawa

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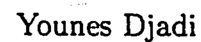

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Abstract

In this thesis a comparison of two gallium arsenide digital logic families, direct-coupled FET logic (DCFL), and source-coupled FET logic (SCFL) is presented. Then, a study of the electrical yield characteristics of gallium arsenide SCFL circuits is done according to the following parameters: The maximum frequency of operation, the compatibility with ECL in terms of logic levels, the circuit architecture, and the complexity. This study is carried out taking into account the presence of parametric variations as obtained from measurements from a typical wafer.

The compatibility with ECL is found to be the determinant factor on the maximum achievable yield. The circuit architecture and complexity, on the other hand, are found to have a significant effect on the maximum circuit speed that can be achieved for the maximum yield.

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Contents

1 Introduction 1

1.1 Advantages of Gallium Arsenide . . . 1

1.2 Limitations of Gallium Arsenide . . . 3

1.2.1 Material limitations . . . 3

1.2.2 Process limitations . . . 3

1.2.3 MESFET limitations . . . 4

1.3 Motivation . . . 4

1.4 Outline of the Thesis . . . 5

2 Gallium Arsenide Device Modeling 6

2.1 Schottky Barrier Diode Model . . . 6

2.2 Gallium Arsenide MESFET Model . . . 8

2.2.1 Modeling of Low-Frequency Anomalies . . . 11

3 Common Gallium Arsenide Digital Circuits 17

3.1 Depletion Mode Logic Circuits . . . 17

3.1.1 Source Coupled FET Logic . . . 18

3.1.2 Limitations of Output Cell . . . 22

3.2 Enhancement Mode Logic Circuits . . . 23

3.2.1 Direct Coupled FET Logic . . . 23

3.3 Noise-Margin Limitations of GaAs VLSI . . . 26

3.3.1 Effect of Parameter Variations on Yield . . . 29

3.3.2 Contributions of Long 32

4 GaAs Processing Data and Yield analysis **33**

4.1 GaAs Processing Data 33

4.1.1 Model Parameter Extraction 33

4.1.2 Wafer characterization 37

4.2 Yield Analysis 41

4.2.1 Yield of SCFL Inverters 41

4.2.2 Effect of Circuit Architecture on Yield 42

4.2.3 Effect of latency on the Maximum Frequency of Operation 45

4.2.4 Effect of Complexity on Yield 52

5 Conclusion **58**

References **61**

A Transistor and Diode Model Parameter Extraction **64**

A.1 Process Parameter Distribution 64

A.2 Transistor Model Parameter Extraction 68

A.2.1 Extraction of λ and β 68

A.2.2 Extraction of α 69

A.3 Diode Model Parameter Extraction 70

A.4 SCFL Gate Load Resistance Extraction 70

A.5 Temperature Scaling 70

List of Figures

2.1 SBD equivalent circuit 8
2.2 Diode current versus voltage for a nominal diode 9
2.3 MESFET equivalent circuit 13
2.4 Ids versus Vds characteristics for the MESFET described above 14
2.5 DCFL inverter 14
2.6 DCFL inverter step response 15
2.7 DCFL inverter frequency response 15
2.8 FET Output Conductance vs Frequency. 16

3.1 SCFL inverter gate 20
3.2 SCFL DC transfer characteristics for different FET threshold voltages . . . 21
3.3 SCFL inverter delay versus FET threshold voltage 21
3.4 SCFL inverter power dissipation versus FET threshold voltage 22
3.5 SCFL Output Cell 24
3.6 Output cell voltage levels versus FET threshold voltage 25
3.7 DCFL inverter gate 26
3.8 DCFL inverter transfer characteristics for different Vt's 27
3.9 DCFL inverter noise margin versus threshold voltage 27
3.10 DCFL inverter delay versus threshold voltage 28
3.11 DCFL inverter dissipated power versus threshold voltage 28
3.12 Maximum Width and Maximum Square noise margins [Long] 30
3.13 Yield of GaAs circuits with N gates [Long]. 32

4.1 A typical GaAs wafer fabricated in BNR. 34
4.2 Inverter chain for maximum frequency measurements 38
4.3 Maximum frequency of operation vs. Site position 39
4.4 Test circuit for output voltage level measurements 39
4.5 Output High logic level vs. Site position 40
4.6 Output Low logic level vs. Site position 40
4.7 ECL-Nonfunctional sites in the wafer 42
4.8 Yield of SCFL inverters vs. Frequency 43
4.9 Parity generator circuit 43
4.10 Ideal Input and output signals 44
4.11 Input and output signals with latency 45
4.12 Maximum XOR frequency of operation vs. Site position 48
4.13 Yield of XOR circuits without latency vs. Frequency 48
4.14 Maximum input frequency of parity generator circuits vs. Site position . . 49
4.15 Yield of Parity generator circuits vs. Frequency 50
4.16 Yield of XOR circuits vs. Frequency 51
4.17 Yield of n-level-XOR circuits vs. Frequency 53
4.18 Functional sites with double complexity 54
4.19 Functional sites with triple complexity 55
4.20 SCFL Parity circuit Yield vs. Frequency for different complexities without output cell 55
4.21 SCFL Parity circuit Yield vs. Frequency for different complexities with output cell 56

A.1 V_{to} spread across the wafer 65
A.2 I_{Dss} spread across the wafer, at $V_{GS} = 0$ 65
A.3 R_{DS} spread across the wafer 66
A.4 C_{DS} spread across the wafer 66
A.5 V_{on} spread across the wafer at $I_s = 150\mu A/\mu M$ 67

A.6 $R_\square$ spread across the wafer 67
A.7 V_{to} spread across the wafer at 150 degrees C 72
A.8 λ spread across the wafer at 150 degrees C 73
A.9 β spread across the wafer at 150 degrees C 73
A.10 α spread across the wafer at 150 degrees C 74
A.11 I_S spread across the wafer at 150 degrees C 74
A.12 R_L spread across the wafer at 150 degrees C 75

List of Tables

2.1 Hspice diode model parameters used for GaAs Schottky diode 9

2.2 Hspice model parameters for GaAs MESFET 12

3.1 Projected number of functional gates at the 50 percent yield level [Long] . 31

4.1 The extracted parameter values across the wafer 36

4.2 The extracted parameter sensitivity 37

Chapter 1

Introduction

Since the early days of semiconductor technology a number of different materials have been studied with a view to investigating phenomena that may lead to significant new devices. Since silicon is the most widely used and reliable semiconductor material, then any new material must be significantly better than silicon, or else must possess some desirable property not found in silicon. Of all new materials the one that has received most attention to date is gallium arsenide (GaAs) which is regarded as the second most important electronic material after silicon [1].

1.1 Advantages of Gallium Arsenide

Since the late 1960s, gallium arsenide technology has been used in the areas of monolithic microwave and millimeter wave devices. In 1974 the use of GaAs MESFETs in digital ICs began with some relatively high power, high speed SSI divider circuits and has developed over the years to well established LSI technology with some inroads into the VLSI arena [3]. The reason for the interest in gallium arsenide for digital integrated circuits lies in the nature of its basic band structure. Compared to silicon, several technical advantages may be identified [2], [3], [6]:

- Gallium arsenide can be fabricated in a semi-insulating (SI) form, because it has a larger bandgap (1.43eV) than silicon (1.1eV). A direct result of this is the reduction

in capacitive parasitics and superior high temperature performance.

- Gallium arsenide is a direct band gap semiconductor meaning that the minimum separation between the valence band and the conduction band occurs at the same momentum. As a result of this gallium arsenide can be used very efficiently in converting electron-hole pairs into light. Therefore it is a very good optoelectronic material.

- Gallium arsenide has a low field electron mobility which is about 6 times higher than that of silicon which means that at low electric fields the electron drift mobility is quite high providing low resistivity in thin film layers and high electron velocity at low applied voltage. This results in the reduction of parasitic resistance and time delay.

In addition to the above advantages gallium arsenide has [4]:

- High speed and low power.
- Low thermal noise.
- Extreme temperature operation.
- High radiation tolerance.
- Integration with detection.

1.2 Limitations of Gallium Arsenide

Although gallium arsenide has many advantages over silicon it still has its own limitations which represent the main obstacles that stop it from being competitive to silicon. These limitations are [2], [3], [4]:

1.2.1 Material limitations

- Poor native oxide.
- High defect density.
- Lower thermal conductivity.
- Relatively volatile.
- Expensive.

1.2.2 Process limitations

The processing problems inherent to gallium arsenide come from the fact that it is a compound semiconductor. As compared to silicon:

- Ion implantation is harder to control in gallium arsenide.
- Gallium arsenide has substitutional sites, therefore an implanted ion may act as a donor or acceptor.
- The annealing of an implanted layer is more complicated since the group III and V impurities have different vapor pressures, chemical properties, and melting points.
- The electrical behavior of the background impurities and defects in the substrate is less predictable.

1.2.3 MESFET limitations

- Frequency dependent small signal conductance.
- Drain current transients with time constants on the order of seconds.
- Poor absolute accuracy and pair matching.
- Backgating and sidegating between devices.
- Piezoelectric effects and light sensitivity.

1.3 Motivation

As a result of the imperfections described above, gallium arsenide devices exhibit more variations in their electrical properties from ingot to ingot and wafer to wafer than would be acceptable in the silicon MOS process. This will cause variations in the circuit characteristics: e.g. signal levels, noise margin, rise time, fall time, and delay, from wafer to wafer and across the wafer itself. This nonuniformity in circuit characteristics will set a limit on GaAs VLSI circuit complexity. However, further increases in complexity will be necessary if gallium arsenide is to play a major role in very high speed computers. Thus a close study of the effect of parameter nonuniformity on complexity and yield of gallium arsenide circuits is needed.

This thesis will investigate the effect of variations in process parameters on the performance of GaAs SCFL circuits, and give an estimation of the Yield versus Speed for different complexities and circuit architectures using real data obtained from a typical wafer. The yield under consideration here is the electrical and not the process yield, which means that the predicted yield will be the maximum yield that can be achieved assuming no deffects, and no interconnect problems.

1.4 Outline of the Thesis

In chapter 2, the MESFET transistor and Schottky barrier diode models used throughout the thesis are described.

In chapter 3, a description of the widely used gallium arsenide digital circuit families is given along with a comparison of the most important characteristics of the two widely used gallium arsenide logic families, the Direct Coupled FET Logic (DCFL) and the Source Coupled FET Logic (SCFL).

In chapter 4 a discussion of sample wafer data from BNR[1] is presented with a description of the methods used in model parameter extraction. Also, the characteristics of the SCFL gates from the 25 sites on the wafer are described. Then, a detailed study of the yield of SCFL circuits is presented.

In the last chapter a summary of the most important steps in yield prediction is given, then some ideas for future work are presented. The thesis is completed with a conclusion about the contributions of this work, and possibilities for future work.

[1] BNR: Bell-Northern Research Ltd. P.O.Box 3511, Station C, Ottawa, Ontario, Canada, K1Y 4H7

Chapter 2

Gallium Arsenide Device Modeling

The accuracy of device models used in circuit simulation is the most critical aspect of circuit design. Inaccuracies will lead to incorrect prediction of circuit performance. Computer simulation is in fact only as accurate as the equations used for circuit elements. These equations must be a compromise between accuracy and excessive computation time. In this thesis HSPICE[1] will be used as the simulation tool for the research, and in the following pages the models of the two gallium arsenide devices used in our circuits will be described: The Schottky barrier diode, and the MESFET.

2.1 Schottky Barrier Diode Model

The Schottky barrier diode (SBD) is widely used in the design of gallium arsenide digital circuits and it is especially used as a level shifting element in SCFL circuits. The main characteristic that distinguishes the Schottky barrier diode from the p-n junction diode is that the SBD is a majority carrier device, while the p-n junction diode is a minority carrier device. In spite of this major difference, the current-voltage relationship is still accurately described by the ideal diode equation [5]:

[1] HSPICE: Circuit simulation software, a product of Meta-Software, Inc. 1300 White Oaks Road, Campbell, CA 95008

$$I_D = I_S \left[\exp\left(\frac{qV_{D,i}}{nKT} \right) - 1 \right] \tag{2.1}$$

Where:

I_s: is the diode saturation current.

n: is the ideality factor.

K: is Boltzmann's constant.

T: junction temperature in Kelvin.

The above equation is for an ideal diode. Since any practical diode has a series resistance due to the contacts, neutral n-GaAs, and current crowding at the edges of the contacts, the above equation is modified to incorporate this series resistance by defining $V_{D,i}$ as:

$$V_{D,i} = V_D - I_D R_S \tag{2.2}$$

Where:

I_D: is The current through the diode.

V_D: is the voltage across the actual diode.

R_S: is the total parasitic diode resistance.

The equivalent circuit used in the Hspice model is shown in Fig. 2.1. The nonlinear dependent current source provides the functional relationship of eq. 2.1. The resistor models the voltage drop caused by R_S. The voltage dependent capacitor C_D models the charge stored in the depletion region of the S.B.D junction. This capacitance is modeled by:

$$C_D = C_{j0}\left(1 - \frac{V_{D,i}}{V_{B,i}}\right)^{-m} \tag{2.3}$$

Where:

C_{j0}: represents the zero bias junction capacitance.

$V_{B,i}$: is the effective built-in potential.

m: is the grading coefficient.

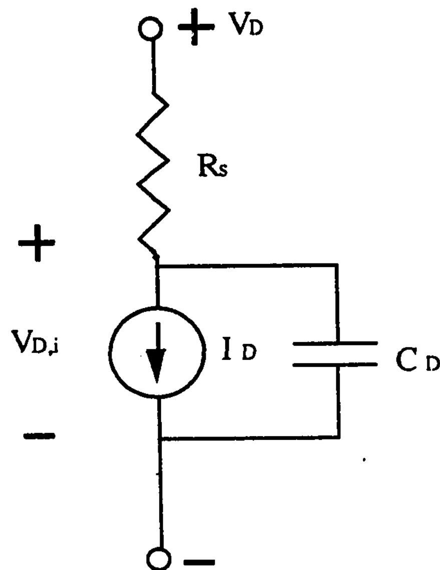

Figure 2.1: SBD equivalent circuit

Fig. 2.2 shows the diode DC characteristics for a diode 25μm in width and 1μm in length, and whose model parameters are shown in table 2.1.

2.2 Gallium Arsenide MESFET Model

There have been many attempts to find an accurate and simple model for the field effect transistor in general and GaAs FETs in particular as GaAs integrated circuits are becoming more and more sophisticated and complicated [7], [8], [9]. The difficulty with MESFET devices is that they are extremely complex internally, and simple external models cannot accurately describe this behavior under all conditions. Conversely a detailed two-dimensional internal model although more accurate, is not suitable for use with circuit simulation programs. The solution is then to develop a model which will describe as closely as possible the internal device behavior without being too complicated for simulation.

Name	Parameter	Units	Value
I_S	Saturation current	A	$1.5e-12$
n	Ideality factor	-	1.18
m	Grading coefficient	-	0.5
C_{J0}	Zero bias junction capacitance	F	2.8e-15
V_{BI}	Built-in potential	V	0.9
R_S	Ohmic resistance	Ω	400

Table 2.1: Hspice diode model parameters used for GaAs Schottky diode

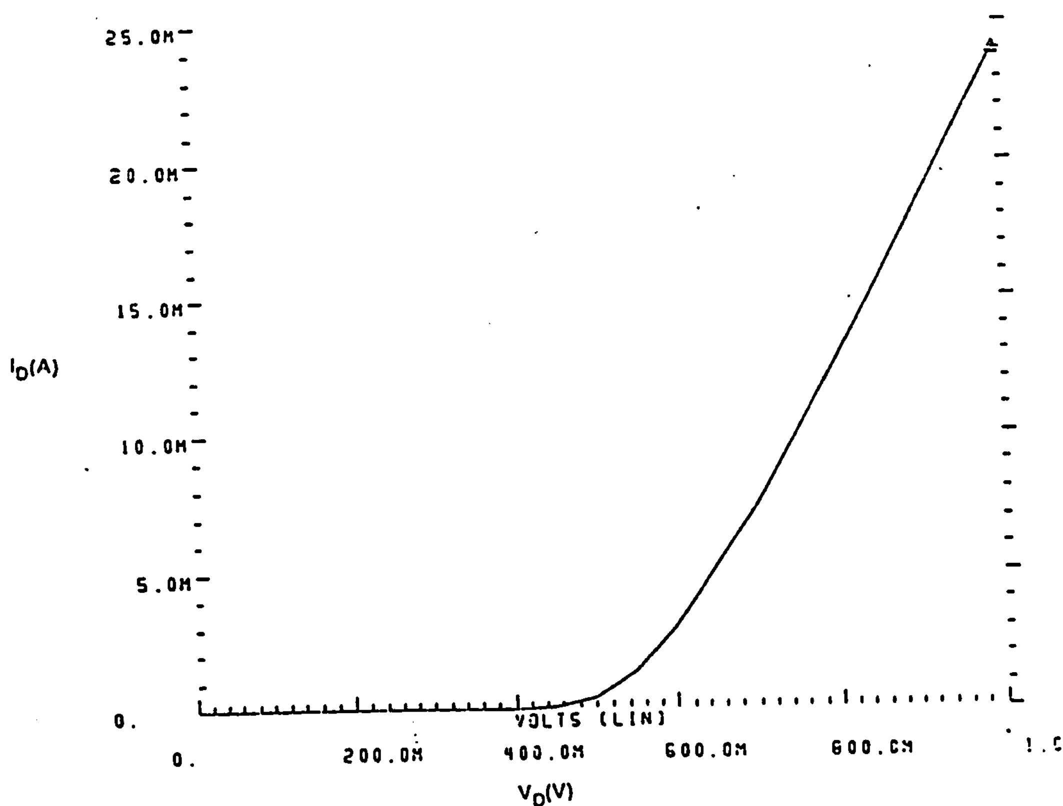

Figure 2.2: Diode current versus voltage for a nominal diode

Fig. 2.3 represents a schematic diagram of the equivalent circuit used in Hspice to represent the GaAs MESFET. The controlled current source $I_D(V_{GS,i}, V_{DS,i})$ is the key element for the DC model. It produces a drain current that depends on the internal gate-to-source (GS) and gate-to-drain (GD) voltages $V_{GS,i}$ and $V_{DS,i}$ respectively. The GS and GD diodes in Fig. 2.3 represent the gate junctions. The forward bias current flow is modeled with individual Schottky barrier diodes within the MESFET model. Time dependent effects are simulated through charge storage elements C_{GS}, C_{GD}, C_{DS}, and C_{RDS}.
A detailed description of the transistor model used throughout the thesis is given below:
The transistor model is based on the Statz model [8] which is a cubic approximation of the Curtice model [7] with gate field degradation [10].
Let:

$$V_{GST} = V_{GS} - (V_{to} + \gamma_{DS} \cdot V_{DS}) \tag{2.4}$$

Where:
V_{to}: is the threshold voltage.
γ_{DS}: is the drain voltage induced threshold voltage lowering coefficient.

The drain current is given by:

For: $V_{GST} < 0$

$$I_{DS} = 0. \tag{2.5}$$

For: $V_{GST} > 0, V_{DS} < \frac{3}{\alpha}$

$$I_{DS} = \beta_{eff} V_{GST}^2 (1 + \lambda V_{DS}) \left[1 - (1 - \frac{\alpha V_{DS}}{3})^3\right] \tag{2.6}$$

For: $V_{GST} > 0, V_{DS} > \frac{3}{\alpha}$

$$I_{DS} = \beta_{eff} V_{GST}^2 (1 + \lambda V_{DS}) \tag{2.7}$$

Where:

$$\beta_{eff} = \frac{\beta \cdot W \cdot M}{L(1 + ucrit \cdot V_{GST})} \tag{2.8}$$

And:

β: is the transconductance parameter gain.

α: is the saturation voltage parameter.

λ: is the channel length modulation parameter.

ucrit: is the critical field parameter for mobility degradation.

W: is the MESFET width.

L: is the MESFET length.

M: is a multiplying factor to simulate multiple MESFETs in prallel.

Fig. 2.4 shows the MESFET output DC characteristics for a MESFET 40μm in width and 1μm in length, and whose model parameters are shown in table 2.2.

2.2.1 Modeling of Low-Frequency Anomalies

Gallium arsenide MESFETs have been known to exhibit low frequency anomalies which affect the system performance, and the Hspice model for the GaAs MESFET does not accurately describe these characteristics. These anomalies are referred to as "drain lag" and "frequency dependence of output conductance" which are just the time and frequency-domain description of the same phenomena [11], [12].

Fig. 2.6 shows the effect of drain lag on the response of the DCFL inverter of Fig. 2.5. Note that there are two time constants: 1- An initial very short time constant. 2- A second long time constant of the order of tens of microseconds producing a long settling tail referred to as drain lag.

The DCFL inverter gain is shown in Fig. 2.7. Note that there are two cutoff frequencies: 1- The lowest one, on the order of KHz is due to the frequency dependence of the output conductance. 2- The highest one on the order of GHz is due to the usual parasitic elements.

The low frequency anomalities described above are due to electron traps in the substrate

Name	parameter	Units	Value
V_{to}	Threshold voltage	V	-1.128
β	Transconductance parameter	A/V^2	120.3e-6
λ	Channel length modulation parameter	1/V	-23.62e-3
α	Saturation voltage parameter	1/V	3.732
R_G	Gate ohmic resistance	Ω	8.3
R_S	Drain ohmic resistance	Ω	774
R_S	Source ohmic resistance	Ω	774
γ_{DS}	Drain voltage, induced threshold voltage lowering coefficient	-	-67.16e-3
ucrit	Critical field for mobility degradation	1/V	0.288
I_S	Gate junction saturation current	A	73.0e-15
n	Gate junction ideality factor	-	1.14
C_{GS}	Zero bias GS junction capacitance	F	906e-18
C_{GD}	Zero bias GD junction capacitance	F	150e-18
C_{DS}	Drain to source parasitic capacitance	F	220e-18
V_{BI}	Gate diode built-in voltage	V	0.9

Table 2.2: Hspice model parameters for GaAs MESFET

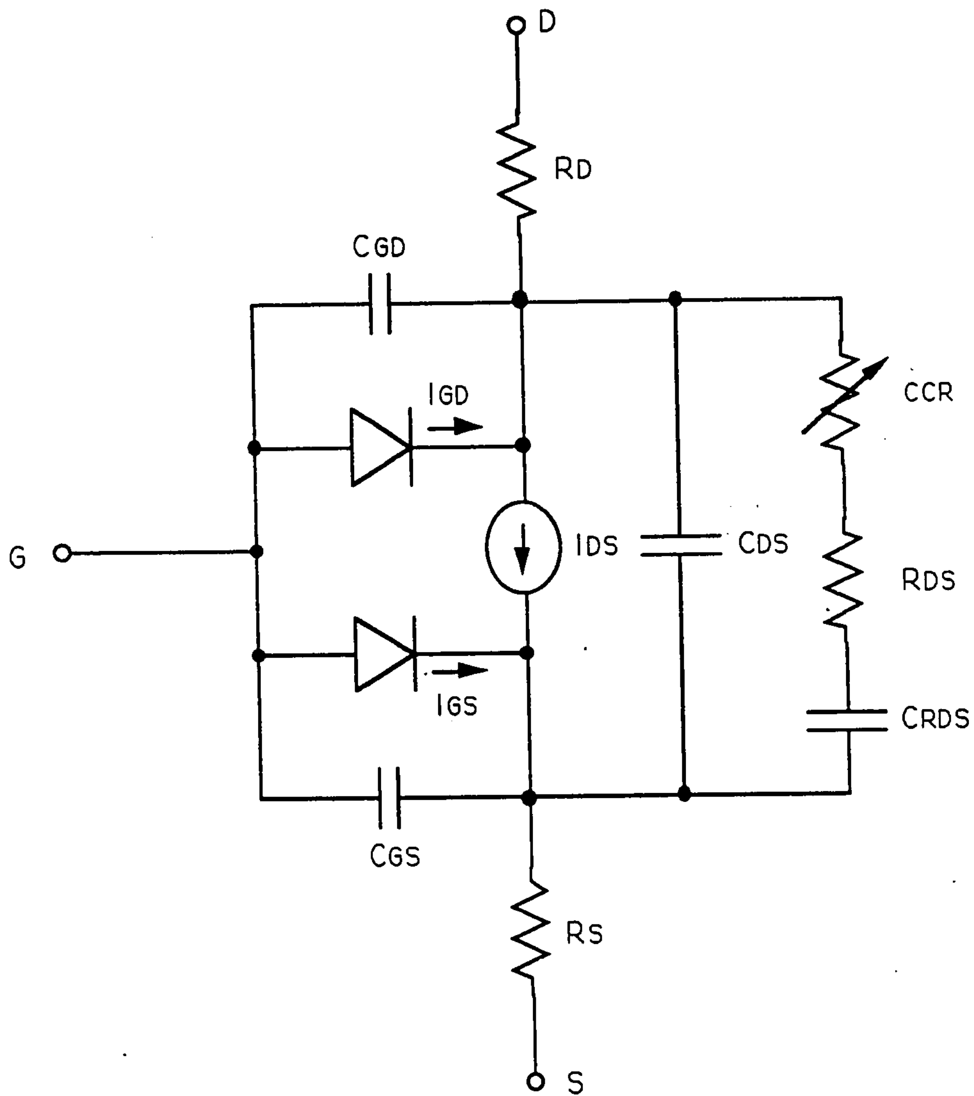

Figure 2.3: MESFET equivalent circuit

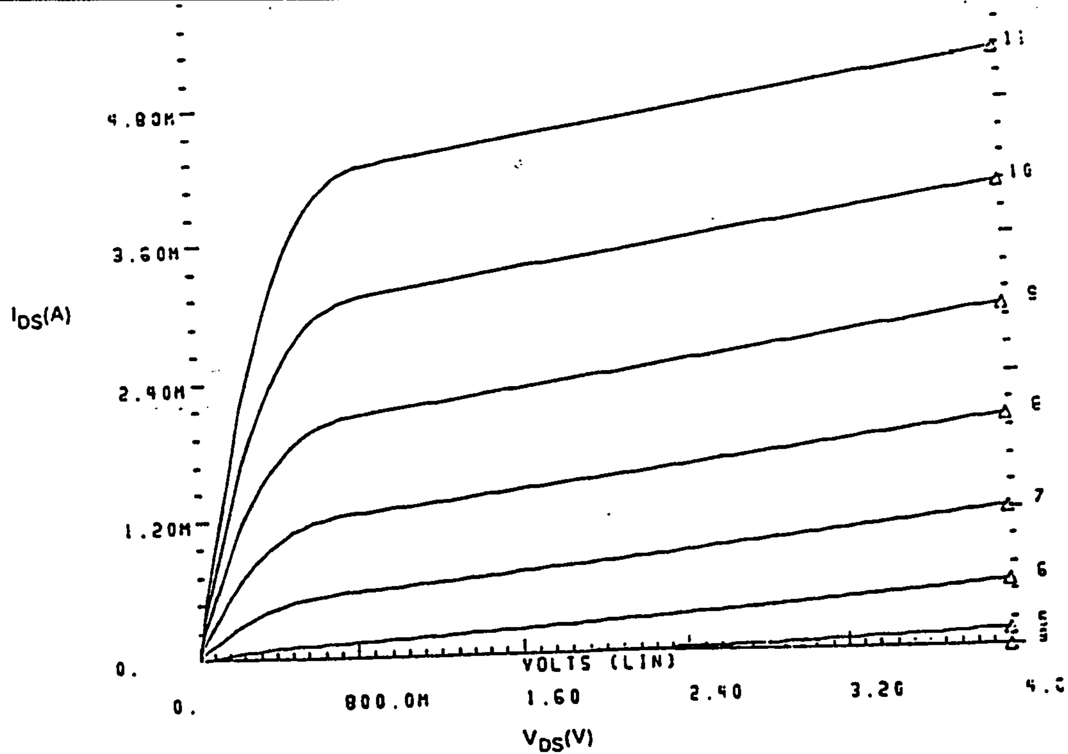

Figure 2.4: Ids versus Vds characteristics for the MESFET described above

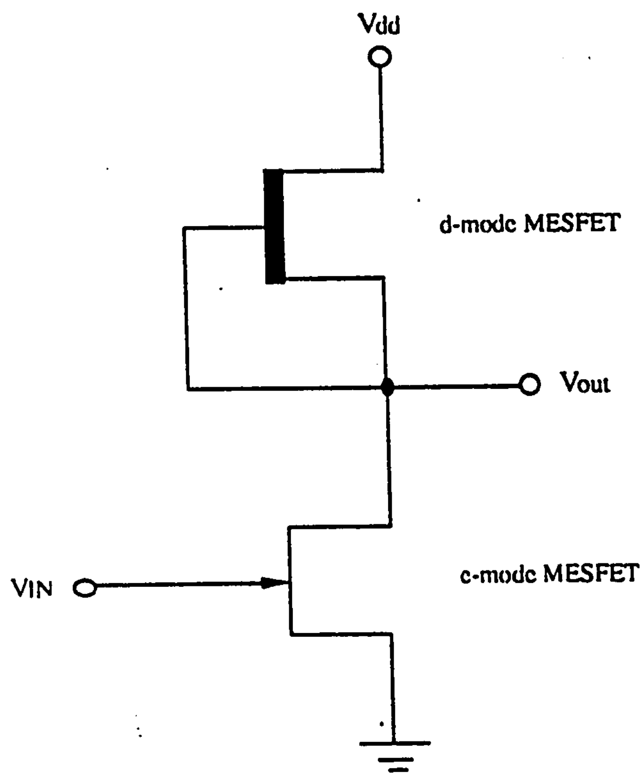

Figure 2.5: DCFL inverter

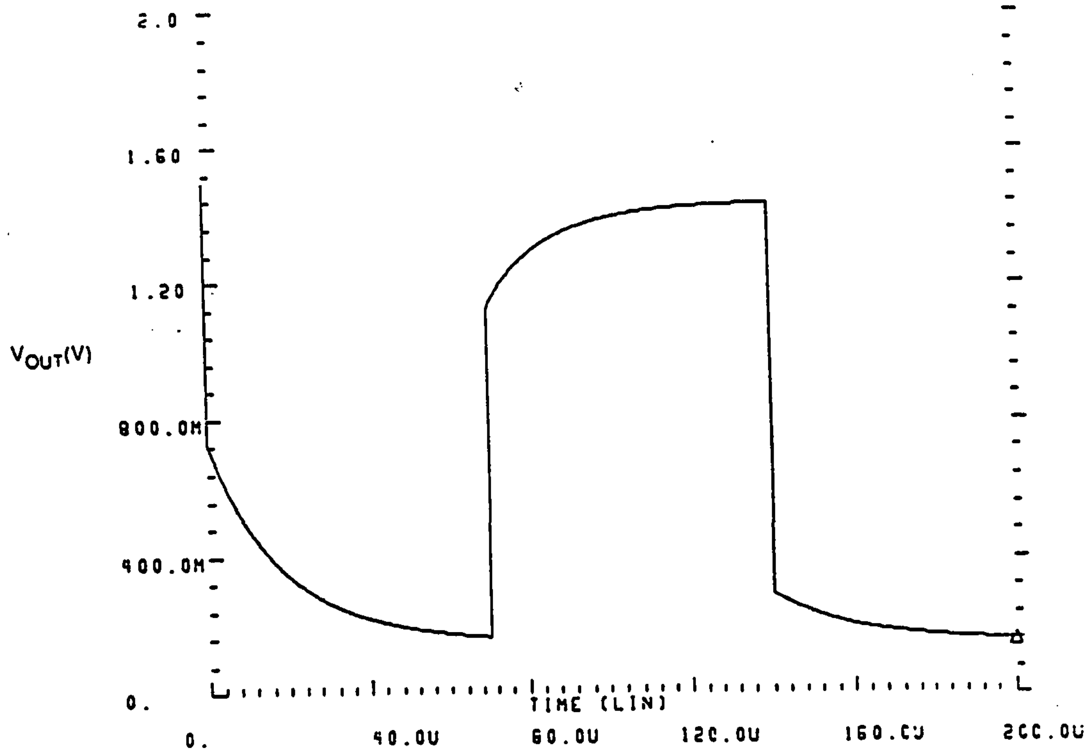

Figure 2.6: DCFL inverter step response

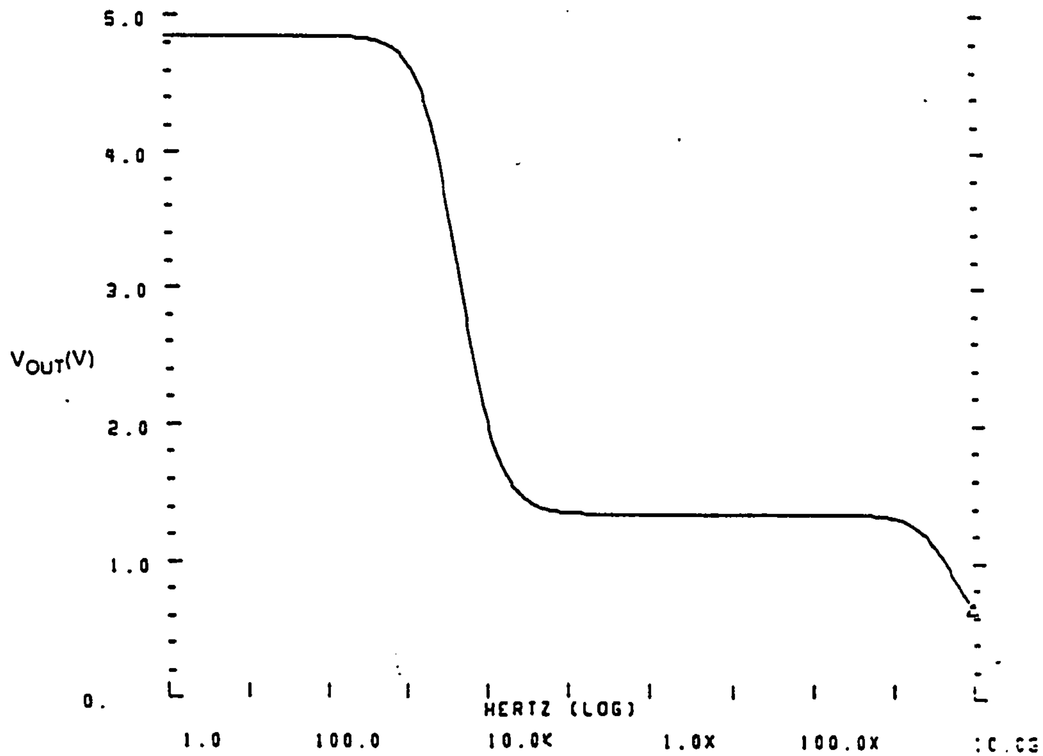

Figure 2.7: DCFL inverter frequency response

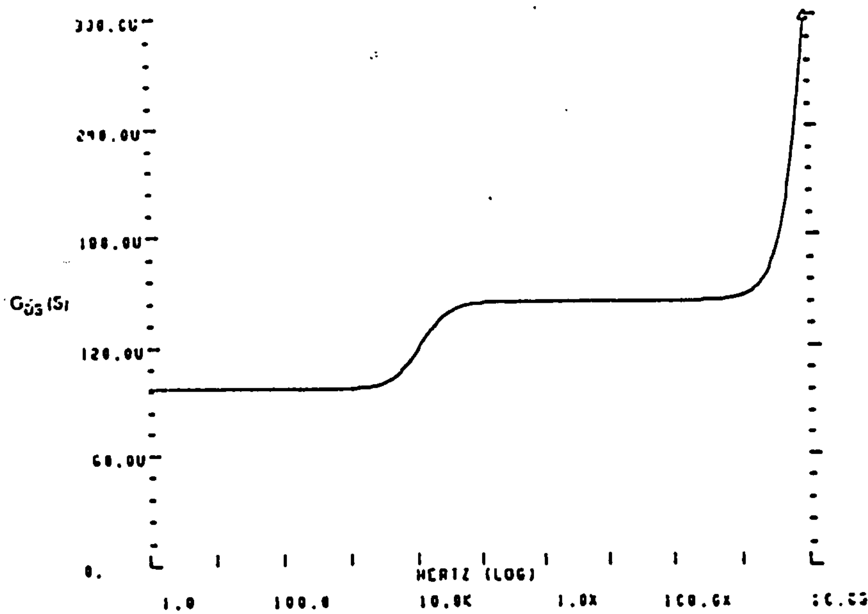

Figure 2.8: FET Output Conductance vs Frequency.

defects [12] which happens only when the FET is on, therefore the frequency dependence on the output conductance is modeled by a series RC network connected between the drain and source of the MESFET through a current controlled resistor (CCR) which is controlled by the FET drain current. When the FET is in saturation the drain current is different from zero, so the CCR represents a zero resistance and the RC network is directly connected to the FET. However, when the FET is OFF the drain current is zero, so that the CCR represents a very high resistance and the RC network is practically disconnected from the FET. See Fig. 2.3.

Fig. 2.8 shows the FET output conductance as a function of frequency.

Chapter 3

Common Gallium Arsenide Digital Circuits

The first section of this chapter discusses the properties and performance of depletion mode gallium arsenide circuits, taking as an example for this study a source coupled FET logic (SCFL) circuit. Then, it concludes by giving the advantages and limitations of this kind of circuit. The second section offers a similar study concerning enhancement mode gallium arsenide circuits by taking as an example a direct coupled FET logic (DCFL) circuit. In the third section, a discussion of a paper written by Long [13] concerning the yield characteristics of GaAs VLSI circuits, is presented. Finally, the fourth section gives the limitations of Long's technique, and presents the requirements and objectives of this work.

In GaAs MESFET circuits we have two types of static logic circuits: Depletion logic circuits, and enhancement logic circuits.

3.1 Depletion Mode Logic Circuits

Depletion mode logic circuits refer to circuits designed with depletion mode (d-mode) MESFETs. These kinds of circuits are characterized by unequal input and output voltage levels because V_{GS} must be negative in order to cut off the FET, while V_{DS} must be positive

at all times. Consequently level-shifting networks typically composed of forward-biased Schottky diodes, are necessary. In addition since both positive and negative signals are required, two power supply voltages, a positive V_{DD}, and a negative V_{SS} are needed. Therefore additional power is dissipated in the circuit. On the other hand larger logic voltage swings can be obtained, because the gate electrode of the d-mode FET varies from a negative voltage close to the threshold voltage to a positive voltage close to 0.7V. The high logic voltage swing of the d-mode circuits lead to larger drive currents, and increased noise margins giving higher yields [14].

There are many logic families in depletion logic circuits [13]: e.g. Unbuffered FET logic, Buffered FET logic, Capacitive coupled logic, Schottky diode FET logic, and Source coupled FET logic (SCFL) [15]. SCFL circuits will be considered as an example:

3.1.1 Source Coupled FET Logic

Source coupled FET logic (SCFL) is the equivalent in gallium arsenide of bipolar ECL or CML in silicon [16], [17]. In this kind of circuits we use differential amplifier circuit structures. One of the most important reasons for using SCFL circuits is to account for the spread in the threshold voltage of GaAs FETs, because the circuitry is such that only the relative variation of the threshold voltage is important [18]. The SCFL circuit includes a FET differential amplifier and a pair of buffer stages. Fig. 3.1 shows an SCFL inverter designed in BNR.

The operation of the SCFL gate may be explained by the following analysis which is similar to the one done by Shur [15]:

Consider the two following cases:

a- The transistor FET1 is ON and the transistor FET2 is OFF. Then we should have:

$$V_{INa} - V_S > V_{t1} \tag{3.1}$$

$$\overline{V_{INa}} - V_S < V_{t2} \tag{3.2}$$

b- The transistor FET1 is OFF and the transistor FET2 in ON. Then we should have:

$$V_{INb} - V_S < V_{t1} \tag{3.3}$$

$$\overline{V_{INb}} - V_S > V_{t2} \quad (3.4)$$

Where:

V_{INa} and V_{INb}: are the input voltages required for switching in cases (a) and (b) respectively.

$\overline{V_{INa}}$: and $\overline{V_{INb}}$ are the complimentary signals of V_{INa} and V_{INb} respectively.

V_{t1} and V_{t2}: are the threshold voltages of FET1 and FET2 respectively.

V_S: is the common source voltage for FET1 and FET2.

By substituting eq. 3.2 into eq. 3.1, and eq. 3.4 into eq. 3.3, we obtain the following conditions required for the SCFL gate operation:

$$V_{INa} - \overline{V_{INa}} > V_{t1} - V_{t2} \quad (3.5)$$

$$V_{INb} - \overline{V_{INb}} < V_{t1} - V_{t2} \quad (3.6)$$

From eq 3.5 and 3.6 we see that the input levels required for switching are only dependent on the difference between the threshold voltages of the FETs. In most cases the threshold voltage difference $V_{t1} - V_{t2}$ between neighboring FETs on a chip is very small. Therefore it can be ignored.

The DC transfer characteristic curves, delay times and power dissipation versus FET threshold voltage are shown in Fig. 3.2, 3.3, and 3.4 respectively. These results were obtained using Hspice circuit simulation, and assuming for simplicity that the other FET model parameters are constant. The simulation results show that the SCFL circuits can operate over a wide range of FET threshold voltages.

The power consumption of an SCFL inverter is considerably larger than the power consumption of inverters implemented using other logic families because of a more complicated circuit configuration and larger values of Vdd and Vss required for an optimum output voltage swing. However, total power consumption may still be comparable to those for other logic families, because of the high functionality of SCFL gates. A D flip-flop for example may be implemented using only two SCFL gates. If standard individual

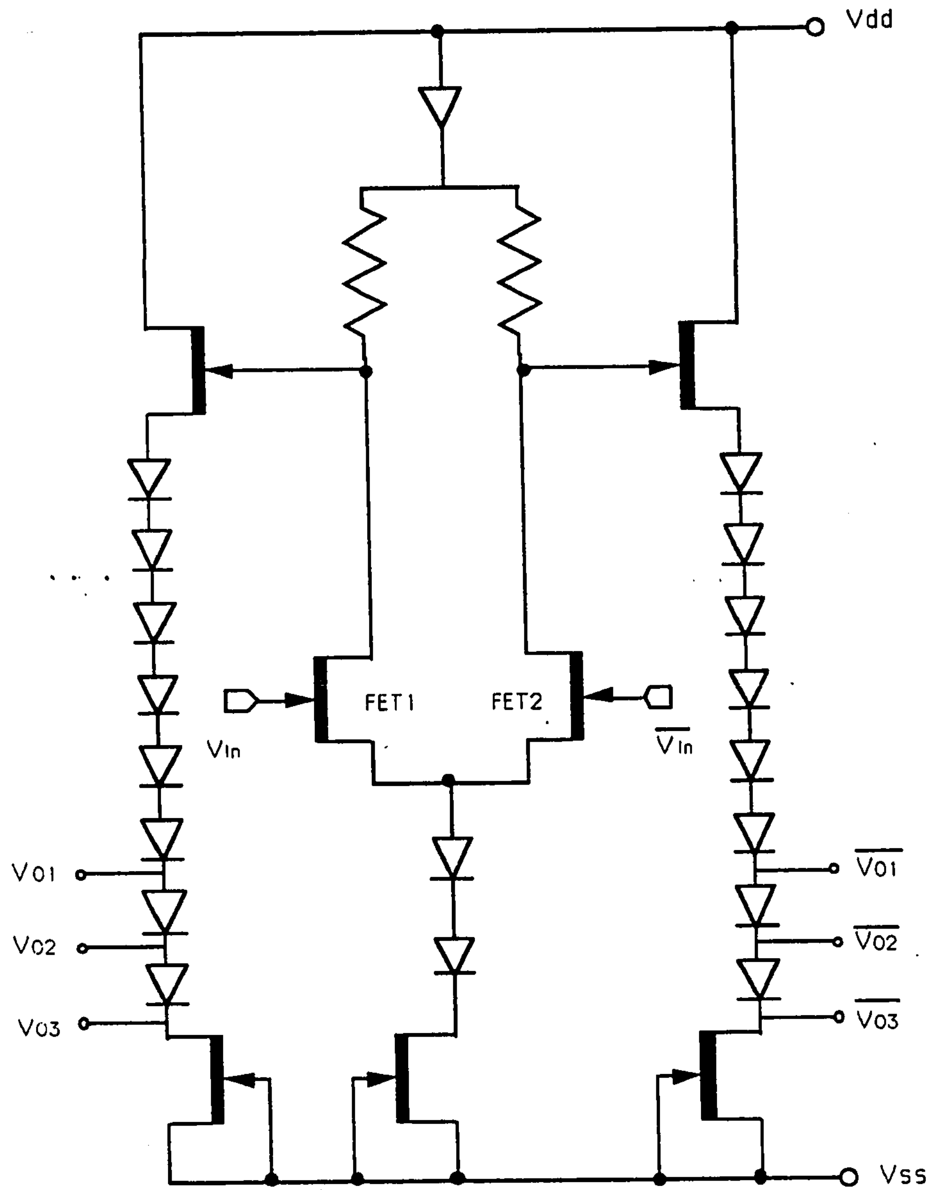

Figure 3.1: SCFL inverter gate

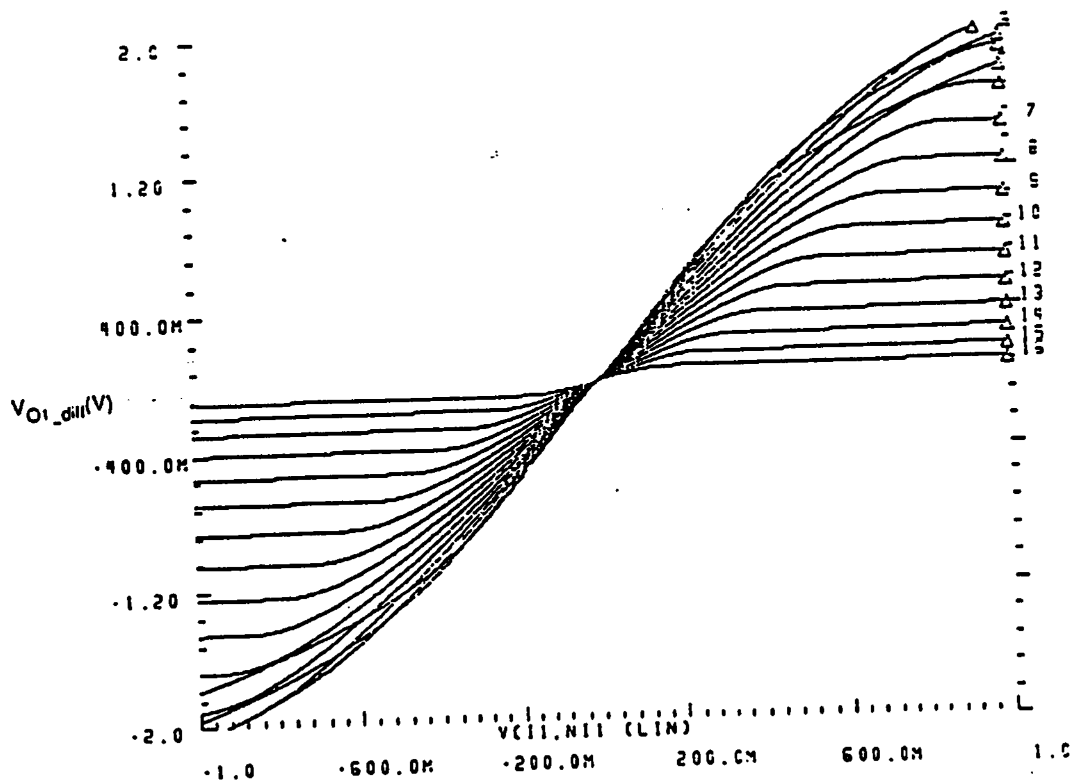

Figure 3.2: SCFL DC transfer characteristics for different FET threshold voltages

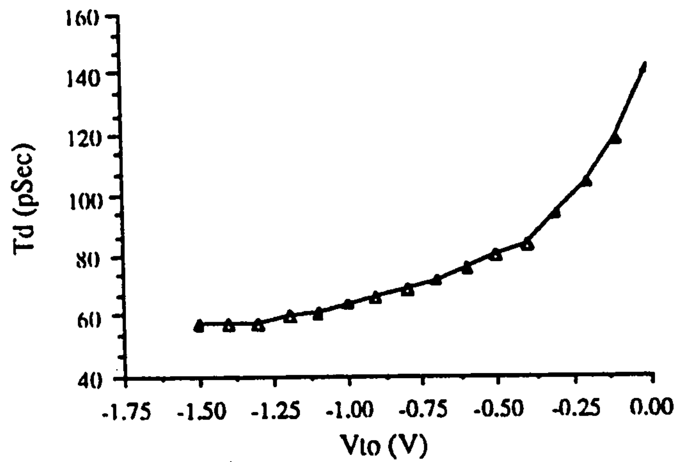

Figure 3.3: SCFL inverter delay versus FET threshold voltage

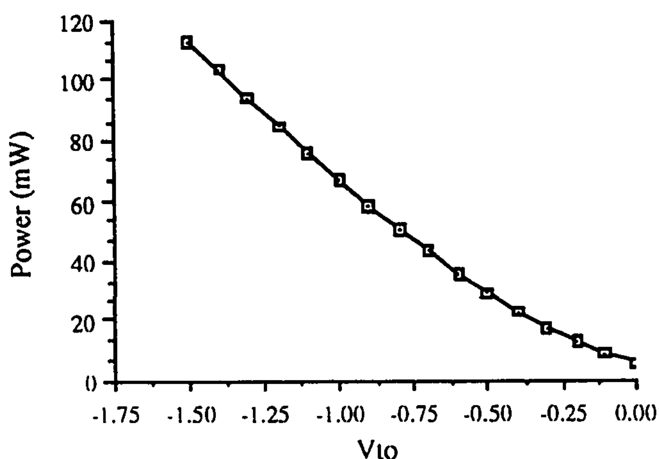

Figure 3.4: SCFL inverter power dissipation versus FET threshold voltage

NOR gates were to be used, at least eight gates would be needed to achieve the same function [14].

The reduced sensitivity to model parameter variation, high speed, and high functionality give SCFL strong advantages when compared with many of the other circuit possibilities.

3.1.2 Limitations of Output Cell

Internally SCFL circuits are very robust in the sense that even if the voltage levels change considerably from gate to gate, the logic levels are still recognizable as long as their difference is large enough. However, the internal signal has to be somehow passed to the outside world which is usually in ECL levels. So there is a need to interface the varying SCFL levels to fixed ECL levels. This is done by the output cell. Fig. 3.5 shows an output cell used in BNR which is similar to the one suggested by Shimizu [19]. The output ECL levels and the SCFL levels versus FET threshold voltage are shown in Fig. 3.6. Note that a large percentage of output levels fall outside the minimum acceptable ECL range [-1.62V,-0.98V]. This is the most important problem with SCFL circuits, and it has a

severe effect on the yield which will be discussed in a later chapter.

3.2 Enhancement Mode Logic Circuits

Enhancement mode logic circuits are implemented using enhancement mode (e-mode) MESFETs as switching devices. Since both V_{GS} and V_{DS} are always positive, no level shifting from output to input is needed, and a single power supply is sufficient. Also, the saturation voltage $V_{DS,sat}$ of an enhancement mode FET is less than that of a depletion mode FET. Thus, the power supply voltage can be lower for e-mode circuits than their d-mode equivalent. The above properties will save a lot of power and layout area [14]. However the e-mode circuits have their own disadvantages: 1- The gate-to-source voltage will swing from a minimum of 0V to a maximum of 0.7V which is the forward conduction limit of the gate-to-source diode. This will result in a small voltage swing. 2- For a high voltage gain in Vout vs. Vin transfer characteristics, resistors are not suitable to be used as loads. Therefore an active load should be used. While an e-mode MESFET can be used as an active load by connecting its gate and drain together, it is not suitable for high speed application because its drain current diminishes as the output load voltage increases. Therefore there is a need to use d-mode MESFETs which will further complicate the fabrication process

3.2.1 Direct Coupled FET Logic

Direct coupled FET logic (DCFL) is the first, simplest, and most widely used e-mode gallium arsenide logic circuit. Fig. 3.7 shows the schematic diagram of a DCFL inverter gate with a fan-out of 1 [14]. Note the similarity to the E/D nMOS circuits. The simplicity and the small number of circuit elements per gate result in lower interconnect parasitics, higher density, lower power consumption, and higher speed than for other gallium arsenide logic families. The operation of a DCFL gate may be explained as follows:

1- When the applied voltage Vin to the gate of the switching transistor is low (smaller than the threshold voltage Vt of this transistor) The transistor is off.

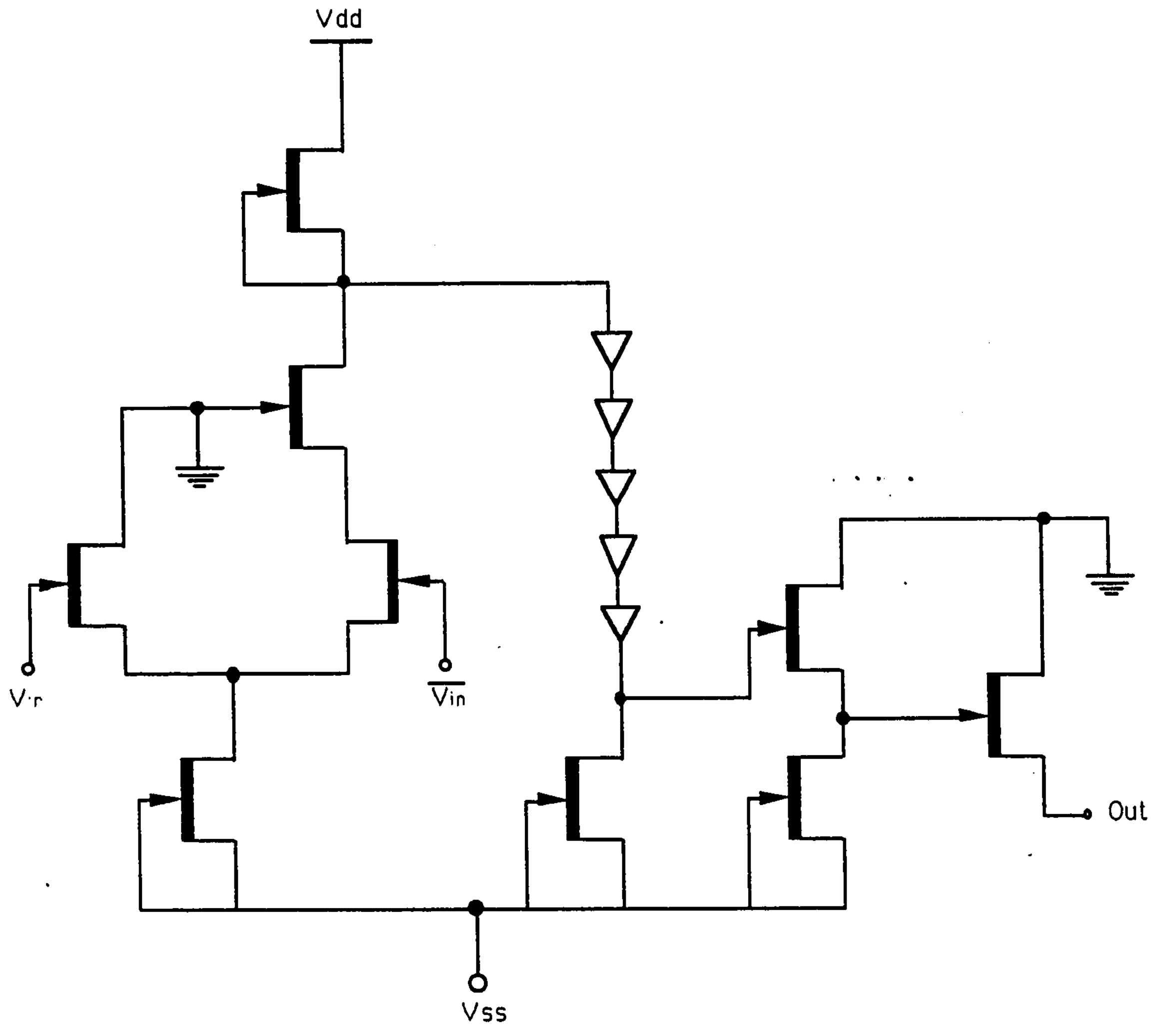

Figure 3.5: SCFL Output Cell

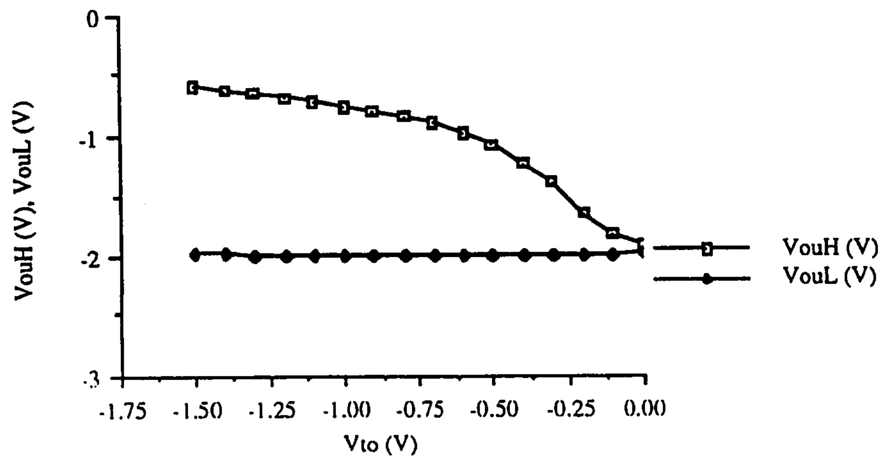

Figure 3.6: Output cell voltage levels versus FET threshold voltage

For a zero fan-out case i.e. no logic gates are connected to the output, Vout is nearly equal to Vdd. In a more realistic situation when other DCFL gates are connected to the output, the voltage Vout is determined by the gate turn-on voltage of the next stage i.e. about 0.7V.

2- When the input voltage Vin is high, the switching transistor is on and the output voltage Vout is low and equal to the drop across the source parasitic resistance. Fig. 3.8 shows the DC transfer characteristics of the DCFL inverter of Fig. 3.7 with a fan-out of 1. Note the rise in the output voltage as Vin increases beyond 0.7V. This is due to the drop across the source parasitic resistance due to the gate-to-source diode current.

From the above analysis, we can see that the noise margin of DCFL circuits is relatively small, because it is limited on the high side by the forward gate conduction of the next stage, and on the low side by the drop across the parasitic source resistance of the e-mode FET. The low (200mV or less) noise margins which are obtained with standard MESFET DCFL circuits places much emphasis on the uniformity of material and process

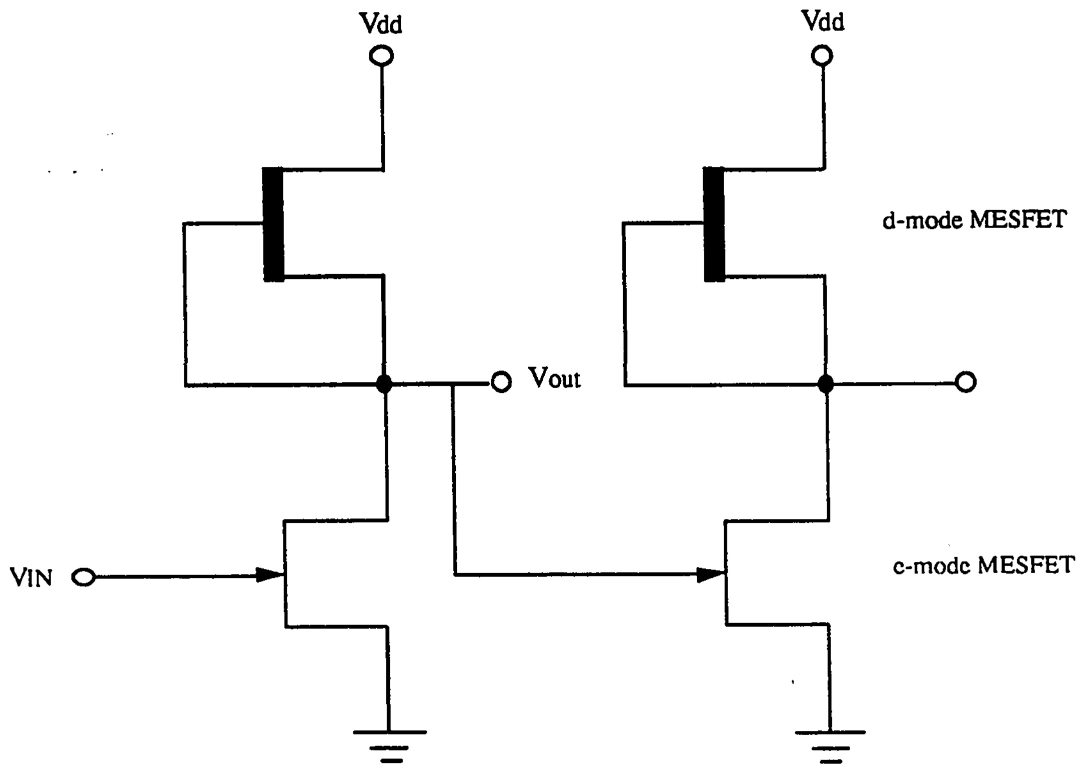

Figure 3.7: DCFL inverter gate

parameters. As will be discussed later, small variations in threshold voltage can reduce the noise margin even further as the circuit complexity increases. Fig. 3.9 shows the noise margin as a function of threshold voltage Vto for the DCFL inverter of Fig. 3.7. Fig. 3.10, and Fig. 3.11 give the delay times and power dissipation vs. threshold voltage. These results were obtained using Hspice circuit simulation. Note the large relative variations in these characteristics as compared to the results obtained for SCFL gates.

3.3 Noise-Margin Limitations of GaAs VLSI

This section discusses the technique used by Long to predict the yield of GaAs VLSI circuits, by taking into account the effect of parameter nonuniformity on the noise mar-

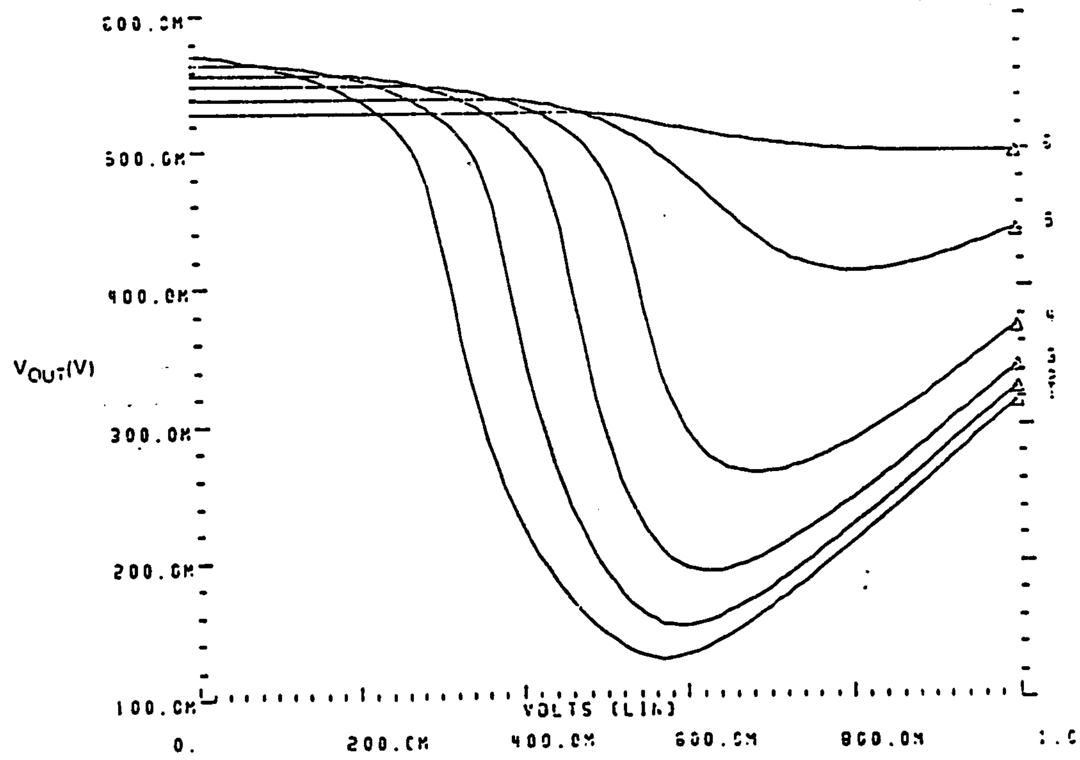

Figure 3.8: DCFL inverter transfer characteristics for different Vt's

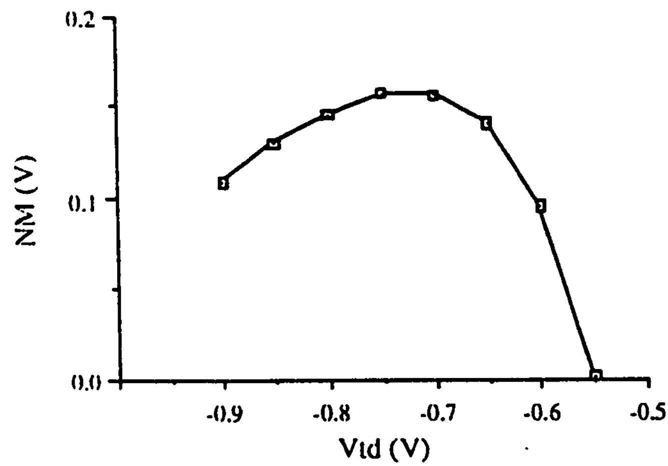

Figure 3.9: DCFL inverter noise margin versus threshold voltage

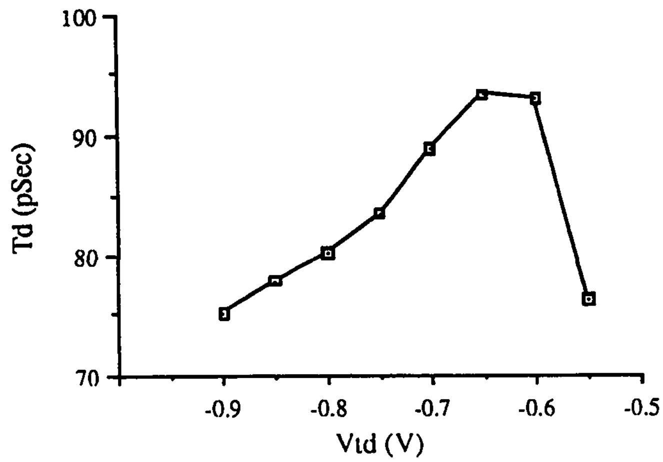

Figure 3.10: DCFL inverter delay versus threshold voltage

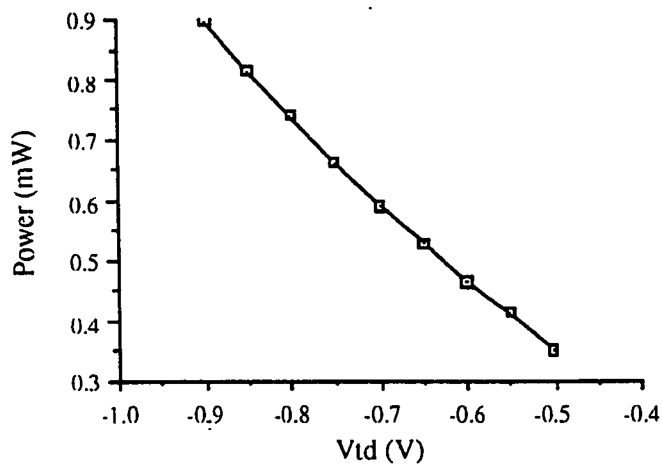

Figure 3.11: DCFL inverter dissipated power versus threshold voltage

gin [13].

The greatest single difference between silicon nMOS design and n-channel GaAs MESFET design is imposed by the Schottky barrier junction gate of the MESFET. The logic low output voltage for both types is limited by the drop across the parasitic source resistance of the switch FET which is about 0.1V to 0.2V, and the logic high output voltage in the nMOS inverter is Vdd while nMESFET inverter is limited by the forward voltage conduction limit i.e. about 0.7V. Hence, the logic swing for the nMOS inverter is 5V-0.1V while for the nMESFET inverter it is 0.7V-0.1V. This substantial reduction in logic swing makes GaAs MESFET digital circuits susceptible to errors when operated in a noisy environment, in other words the noise margin is said to be small. The noise margin can be increased by selecting a clever circuit topology. However, this may result in a larger layout area, more power dissipation, and delay. Therefore an appropriate circuit topology and optimum parameters must be carefully selected depending on the circuit specifications and projected production yield. The role of noise margin and circuit parameter variations on the yield will be explained in the next section.

3.3.1 Effect of Parameter Variations on Yield

The electrical yield is determined by considering two limiting factors:

1- The logic gate parameter variation resulting from process variation.

2- The noise margin which is the tolerance window available for high and low levels.

There are many definitions for noise margin, two of these are: The maximum width V_{MW} and the maximum square V_{MS} noise margin which represents the worst case [21], see Fig. 3.12. The method used to predict the electrical yield is as follows [13], [20]: The circuit under consideration is analyzed to determine the noise margin M^*. Then, it is analyzed for the sensitivities of the noise margin to variations in device parameters. The model parameters to be considered would include:

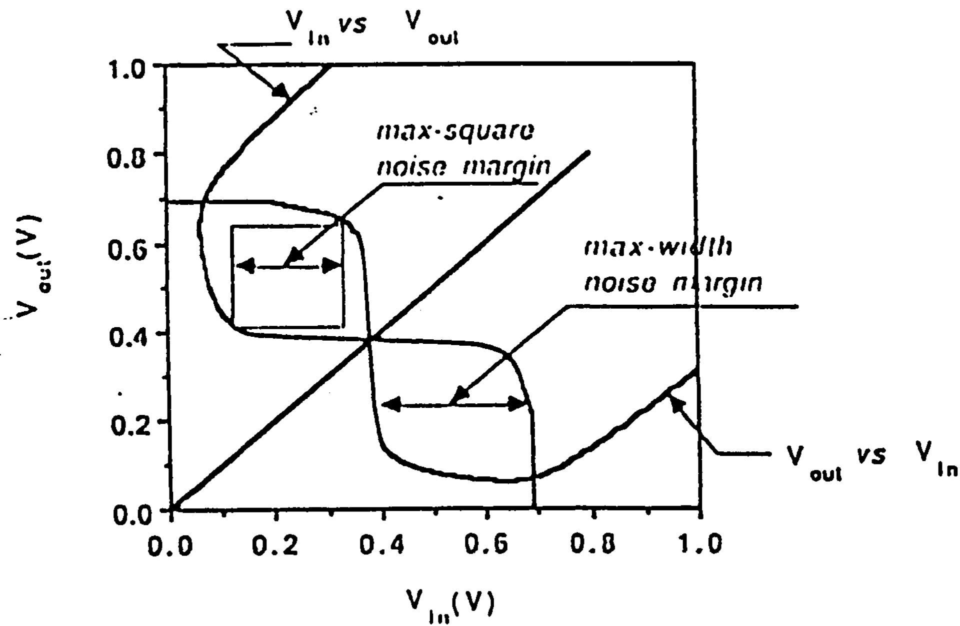

Figure 3.12: Maximum Width and Maximum Square noise margins [Long]

V_{to}: The FET threshold voltage.

β: The transconductance parameter gain.

R_S: The ohmic source resistance.

However, the most sensitive parameter for many circuits is found to be V_{to}. The parameters are assumed to vary independently of each other. Therefore the standard deviation of the noise margin, M_σ is given by:

$$M_\sigma^2 = \sum_{i=1}^{n} (R_i \sigma_i)^2 \tag{3.7}$$

Where R_i represents the sensitivity of the NM to each device parameter x_i, and σ_i is the associated variance.

Finally the available noise margin is computed as:

$$\Delta M = M^* - M_{min} \tag{3.8}$$

Where M_{min} is the minimum acceptable noise margin (arbitrarily assumed 0.1V).

The electrical yield is given as a function of the ratio of the available noise margin to the standard deviation of the noise margin and is defined as the probability of N inverters per circuit which has a noise margin within $\pm\Delta M$, as given by the following probability

$V_{TE}(V)$	$V_{TD}(V)$	NM(V)	$\sigma_{Vt}(mV)$	$\Delta M/M_\sigma$	# Gates
0.2	-0.9	0.22	53	4	10K
0.3	-0.8	0.16	53	2	10-100
0.3	-0.8	0.16	25	4	10K

Table 3.1: Projected number of functional gates at the 50 percent yield level [Long]

distribution function:

$$P(N) = P(X)^N \tag{3.9}$$

Where:

$$P(-X_1 < X < X_1) = \frac{1}{\sqrt{2\pi}} \int_{-X_1}^{X_1} exp(-\frac{X^2}{2})dX \tag{3.10}$$

$$X = \frac{M}{M_\sigma} \tag{3.11}$$

$$X_1 = \frac{\Delta M}{M_\sigma} \tag{3.12}$$

From the above expressions we see that if the available noise margin is high as is the case for Si CMOS, or if the noise margin variation is small as is the case for Si Bipolar circuits then the value of X_1 will be high, and the value of the integral will approach unity i.e. there will be a high yield. Fig. 3.13 describes the maximum yield that can be obtained in a circuit of N gates which have a noise margin window centered at M^* with a width of $2\Delta M$. Table 3.1 shows that the projected number of functional gates at 50 percent yield level for DCFL inverters with 0.22V noise margin at V_{TE} (enhancement threshold voltage) of 0.2V and V_{TD} (depletion threshold voltage) of -0.9V, is 10,000 gates. But if the mean threshold voltages are changed by only 0.1V then the projected number of functioning circuits is seen to be very small (10 to 100) in Fig. 3.13. So, in order to restore the previous yield of 50 percent, the variance on the threshold voltage must be reduced.

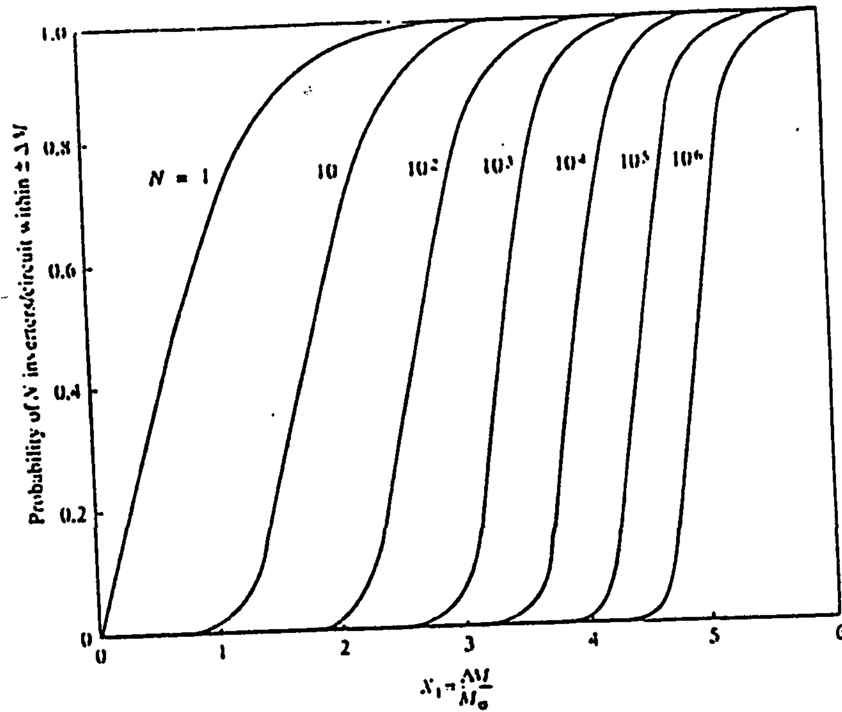

Figure 3.13: Yield of GaAs circuits with N gates [Long].

3.3.2 Contributions of Long

The work done by Long showed us that the parameter uniformity is the limiting factor that stands in the way of attaining the maximum power-limited complexity. This study was done by considering noise margin i.e. DC characteristics only. Although this is a very important step in IC design, it is just a prerequisite because the ultimate goal is to operate the IC at its full speed. Therefore, a similar study should be done taking into account the dynamic characteristics.

The purpose of this thesis is to study the effect of parameter uniformity on the yield of gallium arsenide digital IC's by taking into account the dynamic characteristics of GaAs VLSI circuits using real measurements obtained from a typical wafer.

Chapter 4

GaAs Processing Data and Yield analysis

4.1 GaAs Processing Data

In this chapter the measurement data used in the yield study and their spread over a typical wafer will be studied. Then the general characteristics of the wafer as SCFL gates will be given.

4.1.1 Model Parameter Extraction

In order to perform a practical study of gallium arsenide circuit yield, measurement data were obtained from a typical BNR fabricated wafer. The measurement data were obtained at 25 sites regularly spaced across the wafer. Note that two sites, site 5 and site 21 were discarded because of the inability to measure some parameter values. Therefore, they are considered as bad sites Fig. 4.1. The supplied parameters are:

- The transistor threshold voltage V_{to}
- The transistor saturated drain current I_{Dss}
- The linear drain to source resistance R_{DS}

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25

Figure 4.1: A typical GaAs wafer fabricated in BNR.

- The transistor output conductance G_{DS}
- The diode turn-on voltage V_D
- The sheet resistance $R_\square$

Apart from the threshold voltage V_{to} which is a direct parameter, all the other model parameters have to be derived analytically as discussed in appendix A.

The extracted model parameters to be used in the diode and transistor models described in chapter. 2, are:

- The transconductance gain parameter β
- The saturation voltage parameter α
- The channel-length modulation parameter λ
- The diode saturation current I_S
- The SCFL gate load resistance R_L

The distributions of these parameters at 150 degrees Celsius are shown in table 4.1. The 150 degree temperature was chosen as the worst operating temperature because at this temperature the circuit operates at its worst performance. If any circuit under investigation passes the tests at 150° C then it is considered as a good one, otherwise it will be discarded. The last row of table 4.1 gives the typical values of the model parameters used in BNR circuit design. Note that most of the extracted parameters are close to these typical values.

Table 4.2 gives the sensitivity of the SCFL circuit characteristics to the extracted parameters. The sensitivity S of the response y to the model parameter x is defined as follows:

$$S \simeq \frac{\Delta y/y}{\Delta x/x} \tag{4.1}$$

Where Δx denotes a small change in the model parameter x around its mean value, and Δy denotes the corresponding change in the response y, which is measured using simulation.

Note that the most sensitive parameters are the threshold voltage V_{to} and the transconductance gain parameters β. The 4th column in the table gives the ratio of the variance to the mean value. This ratio gives us a relative measure of the spread of the corresponding parameter across the wafer which is as important as the sensitivity. Some parameters, such as the diode saturation current are not as sensitive as the threshold voltage or the transconductance parameter but have variance to mean value ratios which are about 4 times larger than the transconductance ratio. This means that these parameters have more variations from the mean than the other parameters. Therefore there will be significant effects on the circuit performance across the wafer. The DC sensitivity shown in the table gives the sensitivity of the high output logic voltage level of the output cell to the extracted model parameters. The sensitivity of the low voltage level is much smaller, as can be seen later, that is why it is neglected. Note that, some parameters such as β and V_{to} are more sensitive in AC than DC, while other parameters such as I_S and α are more sensitive in DC than AC. From this we can conclude that taking the threshold voltage as the only sensitive parameter for yield analysis is not a realistic approach.

Site	$V_{to}(V)$	$\beta(\mu A/V^2$	$\lambda(10^{-3}V^{-1})$	$\alpha(V^{-1})$	$I_S(10^{-10}A)$	$R_L(\Omega)$
1	-0.667	129.08	-98.56	3.525	7.56	1088.67
2	-1.111	96.06	-50.89	2.879	5.46	1150
3	-1.111	96.06	-50.89	2.879	5.46	1180.67
4	-1.111	97.02	-55.68	2.851	5.46	1119.33
6	-1.022	101.28	-59.23	2.635	6.42	1180.67
7	-1.111	95.10	-46.00	2.909	6.42	1242
8	-1.289	78.67	-26.94	3.132	5.46	1242
9	-1.200	91.46	-43.43	2.829	6.42	1211.33
10	-1.022	101.28	-59.23	2.970	7.56	1150
11	-0.933	106.00	-63.11	2.667	8.90	1303.33
12	-1.111	95.10	-46.00	2.909	7.56	1272.67
13	-1.200	90.61	-38.78	2.663	5.46	1272.67
14	-1.289	78.67	-26.94	3.132	5.46	1303.33
15	-0.845	112.63	-73.36	2.734	6.42	1272.67
16	-0.933	120.02	-68.85	2.616	10.47	1180.67
17	-1.022	101.28	-59.23	2.792	6.42	1242
18	-1.111	95.10	-46.00	2.724	6.42	1272.67
19	-1.111	96.06	-50.89	2.879	7.56	1242
20	-0.667	105.17	-88.91	4.333	10.47	1180.67
22	-0.933	106.00	-63.11	2.809	8.90	1180.67
23	-0.933	107.23	-68.61	2.776	8.90	1242
24	-0.756	102.51	-84.03	3.527	10.47	1180.67
25	-0.933	109.72	-79.19	2.713	20.08	1119.33
Typical	-1.027	120.30	-30.00	3.604	10.63	1150

Table 4.1: The extracted parameter values across the wafer

Parameter	Mean value	Variance	Variance/Mean	AC Sensitivity	DC Sensitivity
$V_{to}(V.)$	-1.018	0.169	0.166	1.09	0.60
$\beta(\mu V/A^2)$	100.53	11.41	0.113	2.05	1.83
$\alpha(V^{-1})$	2.951	0.378	0.128	0.07	0.22
$\lambda(10^{-3}V^{-1})$	-58.60	17.86	0.305	0.10	0.04
$I_S(10^{-10}A)$	7.81	3.095	0.400	0.01	0.04
$R_L(\Omega)$	1210	59.63	0.049	0.47	0.19

Table 4.2: The extracted parameter sensitivity

4.1.2 Wafer characterization

The extracted model parameters were used to model an SCFL inverter (Fig. 3.1) and the output cell. The criteria used to characterize the wafer are:

- The max frequency of operation for an SCFL inverter
- The output voltage levels of the output cell

These two parameters were considered the most important ones, and the DC characteristics of SCFL cells were not considered. Because on one hand there are no standard voltage levels for SCFL cells, on the other hand SCFL cells are very robust from the DC point of view as discussed in chapter 3. The only DC problem arises when we want to interface the SCFL gates to ECL gates, because of the incompatibility of DC voltage levels. This is the role of the output cell which is considered in the second parameter.

Frequency characterization

In order to measure the maximum frequency of an SCFL inverter a chain of 3 inverters (Fig. 4.2) is simulated to account for the input and output loading, then AC analysis was performed to find the maximum operating frequency which is defined as the frequency at

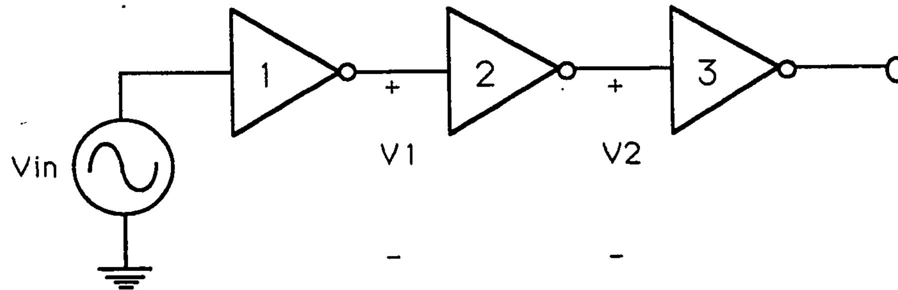

Figure 4.2: Inverter chain for maximum frequency measurements

which the voltage gain of the second inverter drops to one.

The extracted model parameters from each site were used to simulate the SCFL inverter chain described above, and the measured maximum frequencies are plotted in Fig. 4.3. Note that, even though the model parameters vary widely from site to site, most of the maximum frequencies of operation vary closely around 2.9Ghz. This is one of the characteristics of SCFL circuits.

From table 4.2 we can see that the variation in frequency is mainly due to the variation in the transconductance parameter β, and the threshold voltage V_{to}.

DC characterization

As discussed before, the main DC problem with SCFL circuits is in the output voltage levels of the output cell. To demonstrate this, the model parameters from each site were used to simulate an inverter in cascade with an output cell Fig. 4.4. The measured output high and low logic voltage levels are shown in Fig. 4.5 and 4.6 respectively. From these figures we can see that the low logic voltage level does not vary a lot, while the high voltage level varies considerably as we move from one site to another. From table 4.2 we see that the most sensitive parameters are β, V_{to}, α, and I_S if we consider the variance to mean ratio.

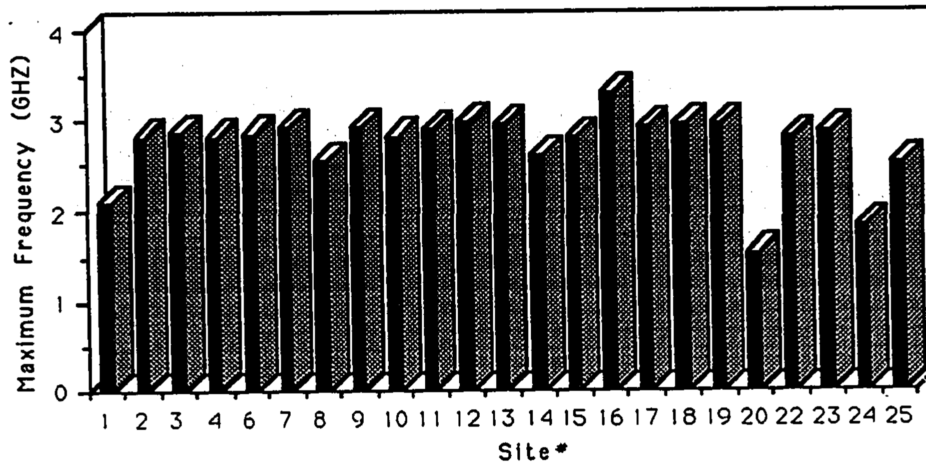

Figure 4.3: Maximum frequency of operation vs. Site position

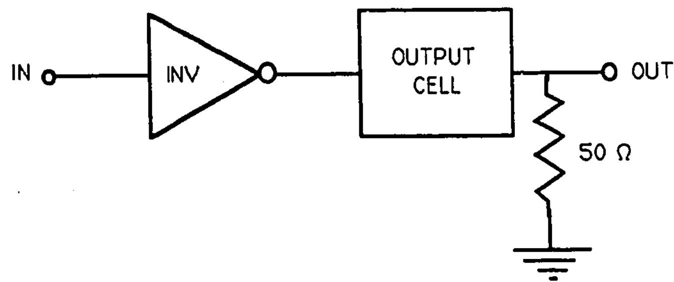

Figure 4.4: Test circuit for output voltage level measurements

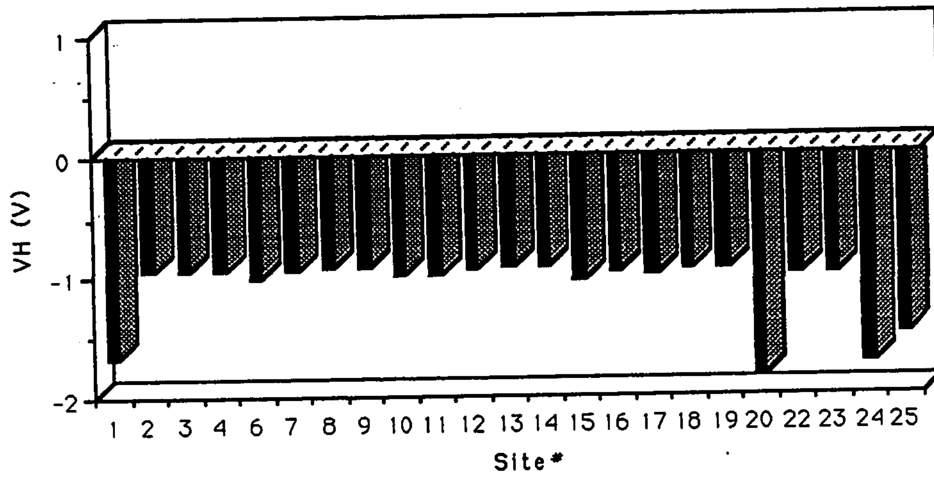

Figure 4.5: Output High logic level vs. Site position

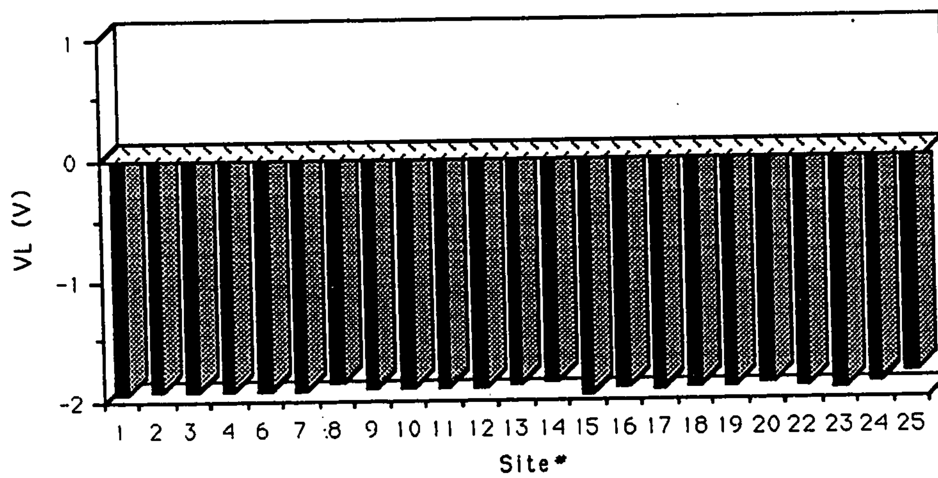

Figure 4.6: Output Low logic level vs. Site position

4.2 Yield Analysis

4.2.1 Yield of SCFL Inverters

The yield at a certain frequency f_0 will be defined as the ratio of the number of sites whose inverters can operate at a frequency greater or equal to f_0, to the total number of sites which is 25 in our case. From this definition we can see that the maximum yield that can be obtained cannot be greater than 92 percent (23/25) since 2 sites were rejected from the beginning.

The yield versus frequency characteristics for gallium arsenide circuits constituting only of SCFL inverters can be deduced directly from Fig. 4.3, This is shown as $Yield1$ curve in Fig. 4.8.

This yield versus frequency curve is valid only if we intend to work just with SCFL circuits. However, since in most of the cases we have to interface the low frequency part of the GaAs SCFL system to a silicon system, usually an ECL circuit, then we have to consider the output cell as well. An output cell is considered to be good if its output logic voltage levels lie in the ECL interval, which is:

From -0.98V to -0.5V for the High logic voltage level.

From -2V to -1.62V for the Low logic voltage level.

From Fig. 4.5 and 4.6 we see that all of the Low voltage levels lie in the ECL interval and that only the High level will determine whether an output cell is good or not. In addition to the two sites 5 and 21 which were initially discarded, there are 11 other sites which do not fulfill the ECL level requirement: 1, 6, 10, 11,15, 17, 20, 22, 23, 24, and 25 (shaded sites in Fig 4.7). Note that as can be expected, most of the bad sites are in the edges of the wafer. So, after discarding all of these, we can construct a new yield versus frequency curve which takes into account the ECL interfacing problem. This is shown as $Yield2$ in Fig. 4.8. We can notice a very important characteristic from the yield curve, which is that most of the discarded sites in the yield2 curve are situated in the low frequency part of the frequency axis which means that if a site is good from the ECL interfacing point

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25

Figure 4.7: ECL-Nonfunctional sites in the wafer

of view, then there is a big chance that it will have a high frequency of operation.

4.2.2 Effect of Circuit Architecture on Yield

So far, the circuit used in the yield study was a simple chain of inverters, although this will give us a quick method of estimating the system performance it does not give a realistic estimate. A more realistic estimate will be obtained if we use a more complex combinational circuit for instance. The circuit to be used in the yield study will be a 4-input parity generator (Fig 4.9), then the results will be extrapolated for more complex combinational circuits.

In dealing with multi-input circuits such as the parity generator circuit we face a problem called latency, which arises when the circuit inputs toggle at different frequencies. The latency problem becomes critical mainly when we are working at very high frequencies close to the maximum operation frequency of the gate. This can be explained as follows: Suppose that we have a 2-input XOR gate with inputs V1 and V2, and that the input signal at V1 is running at a very high frequency 4 times faster than the signal at input V2,

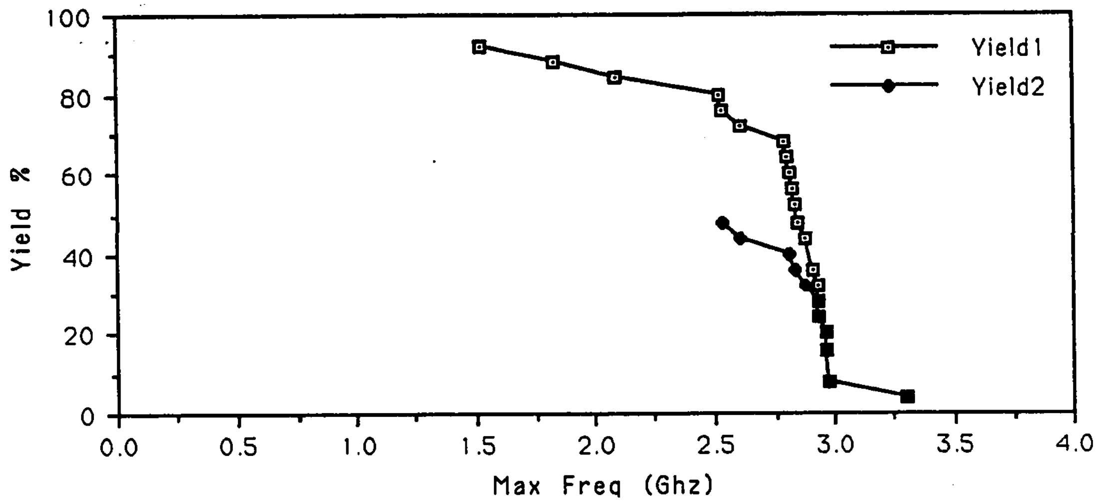

Figure 4.8: Yield of SCFL inverters vs. Frequency

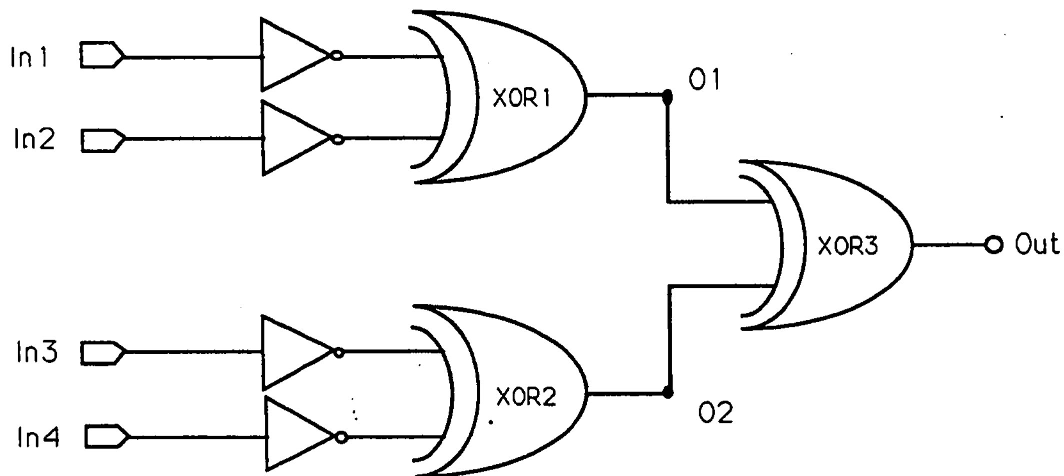

Figure 4.9: Parity generator circuit

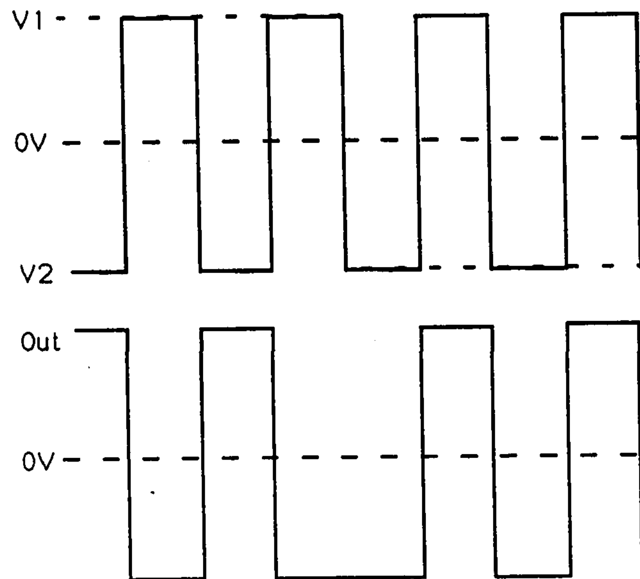

Figure 4.10: Ideal Input and output signals

then the voltage at node V2 will have enough time to reach its maximum and minimum values, while the signal at node V1, cannot reach those values, because it will be forced to change states before reaching its maximum value, therefore they will cross the 0V axis at different times separated by a time interval ΔT, as shown in Fig 4.11. During this time, the XOR output will produce a false pulse of duration ΔT, see Fig 4.10 and 4.11. Therefore the performance of the SCFL circuit will be affected not only by the gate delay time, but also by the latency of the gate.

From the previous analysis we can see that the effect of latency on the circuit performance is related to the number of gates we use in series. If, for example, we connect another 2-input XOR gate to the output of the XOR in the previous example, the second gate output will be affected by the latency of the first gate plus its own latency. Which means that there will be a false pulse of duration $2\Delta T$.

Hence, as a rule of thumb, we can say that for a circuit of n-levels of XOR gates the total

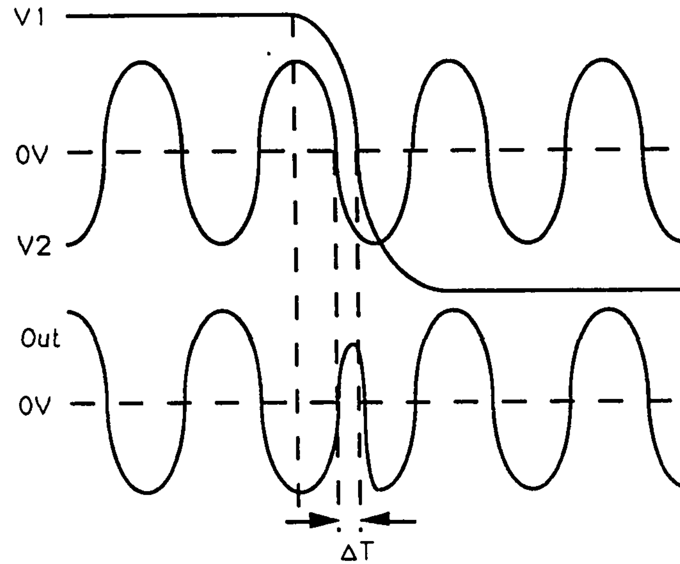

Figure 4.11: Input and output signals with latency

latency time T_{Lat} will be:

$$T_{Lat} = n\Delta T. \tag{4.2}$$

Where ΔT is the latency for one XOR gate.

4.2.3 Effect of latency on the Maximum Frequency of Operation

Assume that the high frequency input for a XOR gate has a pulse width of T_{PIN} seconds, then the output pulse width will be:

$$T_{POUT} = T_{PIN} - T_{Lat} \tag{4.3}$$

So, for an input signal of period T_{IN}, where:

$$T_{IN} = 2T_{PIN} \tag{4.4}$$

The output signal period will be T_{OUT}, where:

$$T_{OUT} = 2T_{POUT} = 2T_{PIN} - 2T_{Lat} \tag{4.5}$$

By replacing equation 4.4 into 4.5 we end up with:

$$T_{IN} = T_{OUT} + 2T_{Lat} \tag{4.6}$$

In terms of frequency, equation 4.6 can written as:

$$f_{IN} = \frac{f_{OUT}}{1 + 2T_{Lat} f_{OUT}} \tag{4.7}$$

Where: $f_{IN} = \frac{1}{T_{IN}}$, and $f_{OUT} = \frac{1}{T_{OUT}}$

Since, the SCFL gate has a maximum frequency of operation f_{MAX}, then the maximum input frequency taking the latency into account can be obtained from equation 4.7 by replacing f_{OUT} by f_{MAX}, which yields:

$$f_{InMAX} = \frac{f_{MAX}}{(1 + 2T_{Lat} f_{MAX})} \tag{4.8}$$

By replacing equation 4.2 in 4.8 we can find the maximum frequency of operation for a circuit of n-levels of XOR gates, to be:

$$f_{InMAX} = \frac{f_{MAX}}{1 + 2n\Delta T f_{MAX}} \tag{4.9}$$

The decrease Δf in the maximum frequency of operation as more XOR levels are added is:

$$\Delta f_n = f_{MAX} - f_{InMAX} \tag{4.10}$$

By replacing equation 4.9 in 4.10 we obtain:

$$\Delta f_n = \frac{2n\Delta T f_{MAX}^2}{1 + 2n\Delta T f_{MAX}} \tag{4.11}$$

From the above analysis it can be seen that the yield versus frequency characteristic for an n-level XOR circuit can be obtained by left shifting the yield-versus-frequency curve for a XOR circuit without latency by Δf_n on the frequency axis . In other words, if Y_0

is the yield of a 1-level XOR circuit without latency, then the yield Y_n of an n-level XOR circuit with latency is given by:

$$Y_n(f) = Y_0(f + \Delta f_n) \tag{4.12}$$

The maximum frequency of operation for a XOR gate

A similar analysis to the one done to find the maximum frequency of operation of an inverter is done to measure the maximum frequency of a XOR gate, by using the circuit shown in Fig 4.9. Fig. 4.12 shows the spread of the maximum frequency of operation of a XOR across the wafer. Note that, as would be expected, these frequencies are smaller than the inverter maximum frequencies shown in Fig. 4.3, due to the fact that we are using two transistors in series for switching rather than one for the inverter, therefore decreasing the transistor transconductance.

Yield of XOR gate circuits

The yield of a XOR circuit without latency can be obtained directly from Fig 4.12. See Fig 4.13.

In order to observe the effect of latency on yield, the 2-XOR-level parity generator circuit shown in Fig 4.9 was used as a test circuit. The highest frequency of operation was measured at each site by simulating the test circuit at its maximum frequency as measured from the inverter chain circuit, then the input frequency is decreased by small steps until the output signal is correct. Fig. 4.14 shows the spread of the maximum frequency of the parity generator circuit across the wafer.

As for the inverter circuits the yield of parity generator circuit can be obtained from Fig. 4.14. This is shown as *Yield*1 curve in Fig 4.15. This yield is calculated without considering the ECL interfacing problem. After considering the ECL interfacing problem,

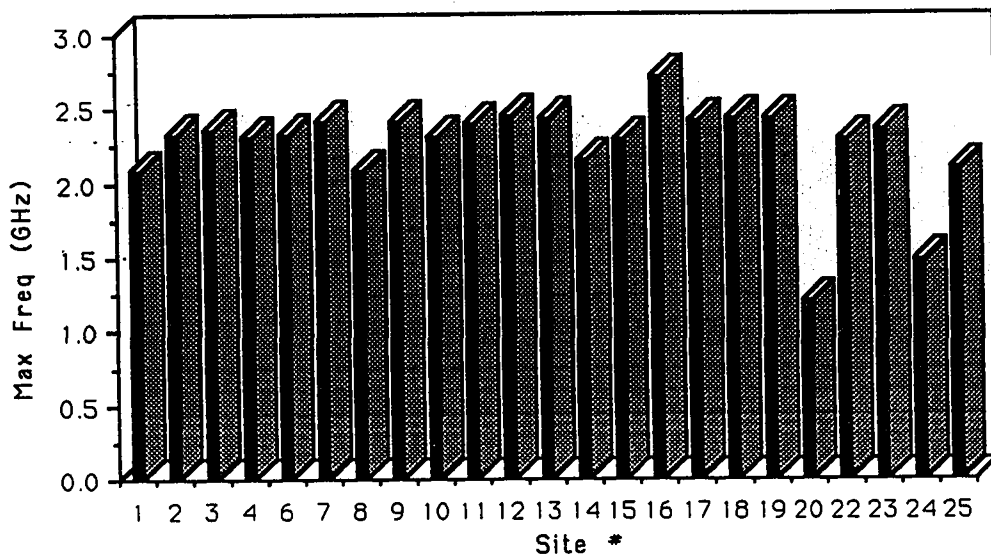

Figure 4.12: Maximum XOR frequency of operation vs. Site position

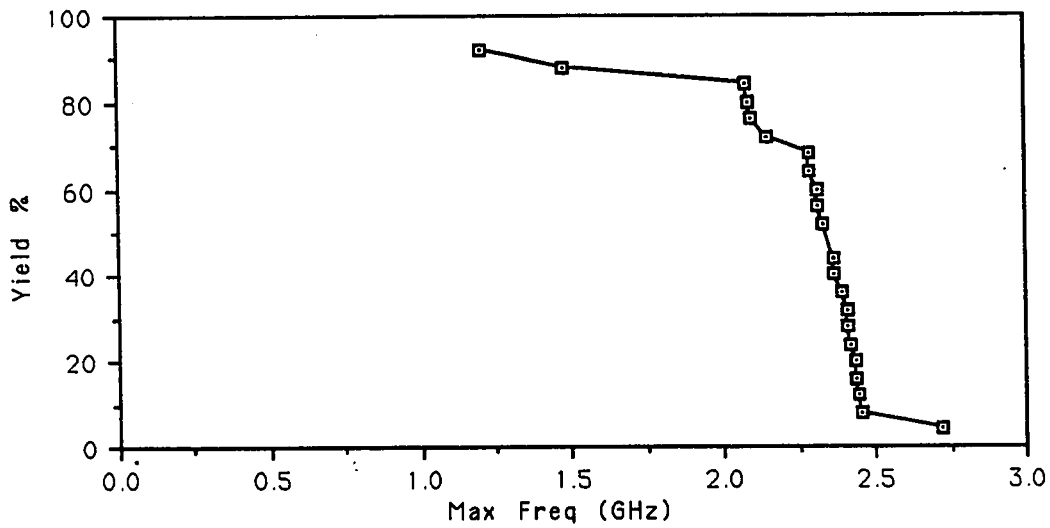

Figure 4.13: Yield of XOR circuits without latency vs. Frequency

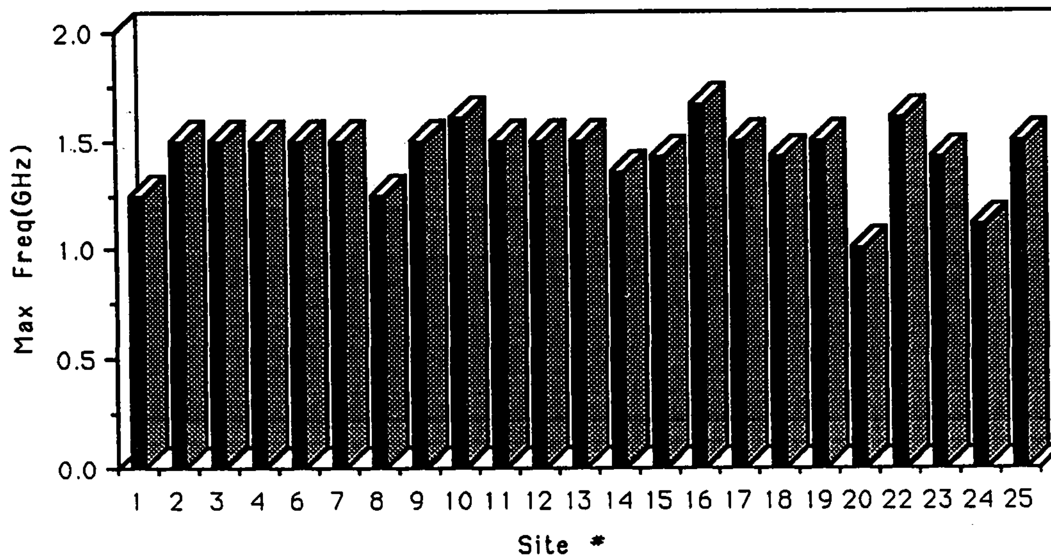

Figure 4.14: Maximum input frequency of parity generator circuits vs. Site position

a new yield versus frequency curve is obtained and depicted as $Yield2$ curve in Fig. 4.15. Note that as for inverter circuits, the ECL interfacing criterion is the main thing that causes the large drop in the yield.

As stated by equation 4.12 the yield of the 2-level-XOR circuit can be obtained directly from the XOR without latency yield shown in Fig. 4.13. The yield for the XOR circuit without latency ($Yield0$ curve), the yield of the parity circuit as obtained by simulation ($Yield1$ curve), and the yield for the parity circuit as obtained from equation 4.12 ($Yield2$ curve), are shown in Fig 4.16. Note that equation 4.12 gives us a close, though optimistic, yield as compared to the simulation results.

From the analysis presented above a general yield versus frequency characteristics can be drawn for an n-level-XOR circuit according to equation 4.12. See Figure 4.17. Where the $Yieldn$ curve gives the yield of SCFL circuits consisting of n-levels of XOR gates without considering the ECL interfacing problem. When the ECL compatibility is taken

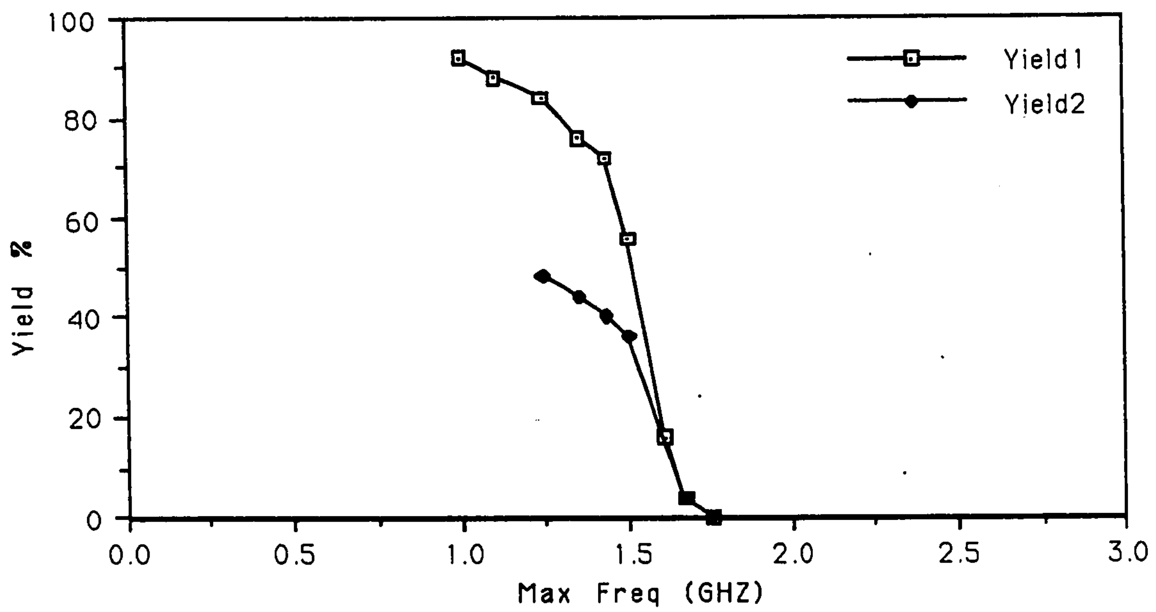

Figure 4.15: Yield of Parity generator circuits vs. Frequency

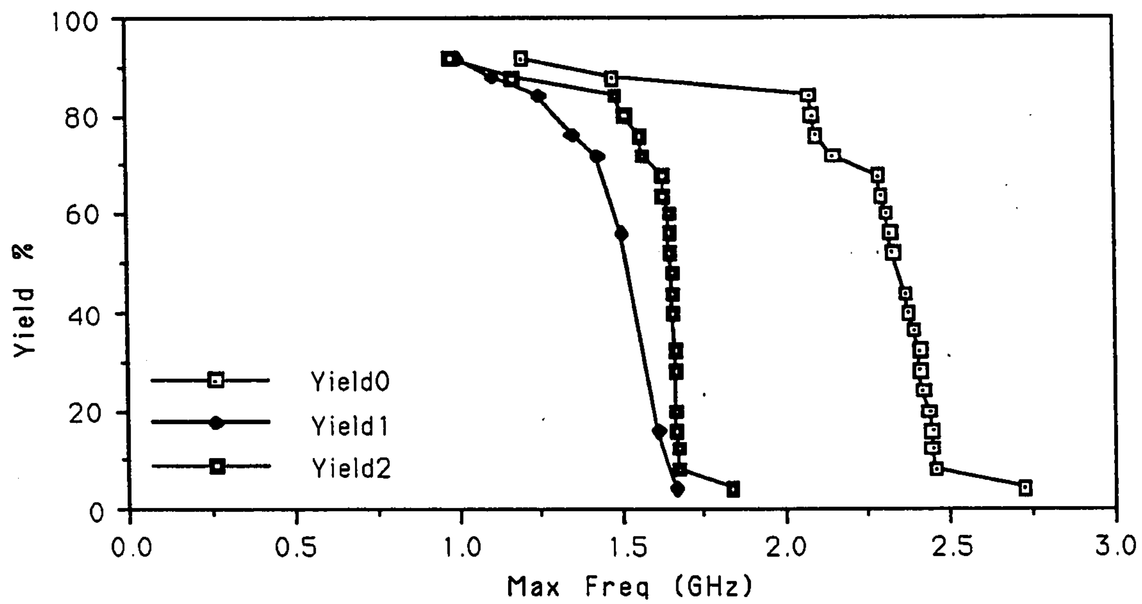

Figure 4.16: Yield of XOR circuits vs. Frequency

into consideration we will have similar yield curves, except that they will have smaller maximum values. Therefore, we'll be considering just the yield without ECL interfacing problem. Fig. 4.17 reveals a very important characteristic of SCFL circuits which is that at the highest frequencies of operation, the circuit yield drops drastically as the number of XOR levels is increased. For example, consider a 4-level XOR circuit operating at 1.25 GHz, from Fig.4.17 we can see that the maximum yield we can have is 80%. If we want to use a 5-level-XOR circuit instead, then the maximum yield that can be achieved at 1.25 GHz will drop to less than 5%. This indicates that the circuit architecture is a very important factor in determining the maximum yield that can be obtained. Therefore the predicted yield presented above can be improved by a creative architecture that will minimize the effect of latency on the yield. This can be done either at the transistor level by improving the design of SCFL gates, to be less sensitive to the latency effect, for instance, or at the gate level by introducing some retiming circuits whose role will be to retime the signals after each certain number of gates, to eliminate the latency accumulated from the previous gates.

4.2.4 Effect of Complexity on Yield

In the yield study done so far, only one site at a time was taken into consideration, and the yield was estimated according to the number of functional sites. Each site contains about 100 SCFL cells, if we assume a functionality of 4 for SCFL cells, this will be equivalent to 400 gates.

Suppose that we want to fabricate SCFL circuits of 200 cells, then we will be obliged to take two sites at a time. In doing so, many of the individual ECL functional sites will be nonfunctional when taken with a nonfunctional site. Therefore the yield is expected to drop drastically, as the complexity increases. From Fig 4.18 we see that the maximum number of functional circuits with ECL interface will be 4 out of 12 that's the best yield will be 33% instead of 48% when taking one site at a time. The yield versus frequency characteristics for the new complexity is shown as $Yield2$ curve in Fig 4.20 when not considering the ECL interfacing problem, and as $ECLYield2$ graph in Fig 4.21 when the

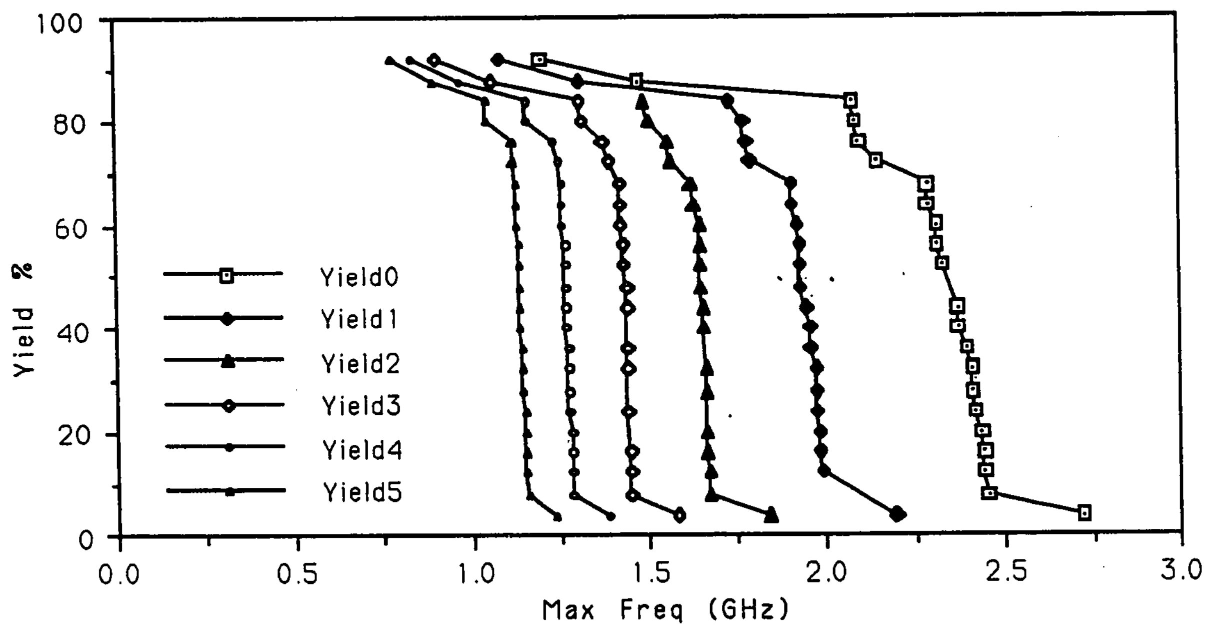

Figure 4.17: Yield of n-level-XOR circuits vs. Frequency

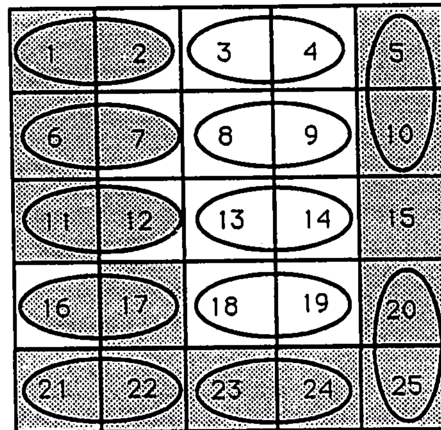

Figure 4.18: Functional sites with double complexity

ECL interfacing problem is taken into consideration. These results are obtained using the maximum frequency versus site position curve shown in Fig. 4.14. The idea used in drawing these characteristics is that if we take two sites with different maximum operating frequencies, then the maximum operating frequency of the new higher complexity site will be equal to the minimum of the maximum frequencies of the two sites.
When we increase the complexity and take three sites at a time which will be equivalent to 1200 equivalent gates, there will be 7 ECL nonfunctional sites out of 8, as shown by the shaded sites in Fig. 4.19. Consequently, the maximum yield that can be achieved will be 12.5%. Using the same idea as for the previous case, a new yield versus frequency characteristic is drawn as $Yield3$ curve in Fig. 4.20 when not considering the ECL interfacing problem, and as $ECLYield3$ curve in Fig 4.21 when the ECL interfacing problem is taken into consideration. By comparing the yield characteristics for the 1-site complexity (graph ECL Yield1), 2-site complexity (graph ECLYield2), and 3-site complexity (graph ECL Yield3) in Fig. 4.21 it can be seen that each time the complexity is increased the maximum yield drops drastically (by 31% when the complexity is doubled, and 64% when the complexity is tripled). The sharp drop in the maximum yield is due mainly to the ECL interfacing criterion set on the output cell, as can be concluded by comparing

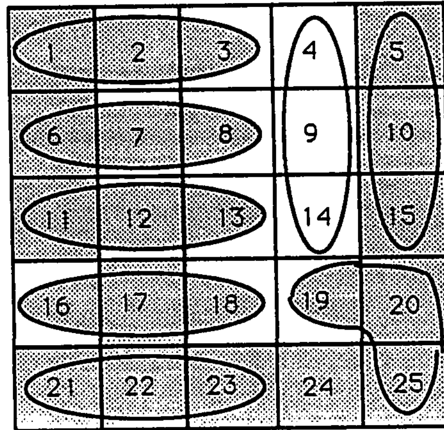

Figure 4.19: Functional sites with triple complexity

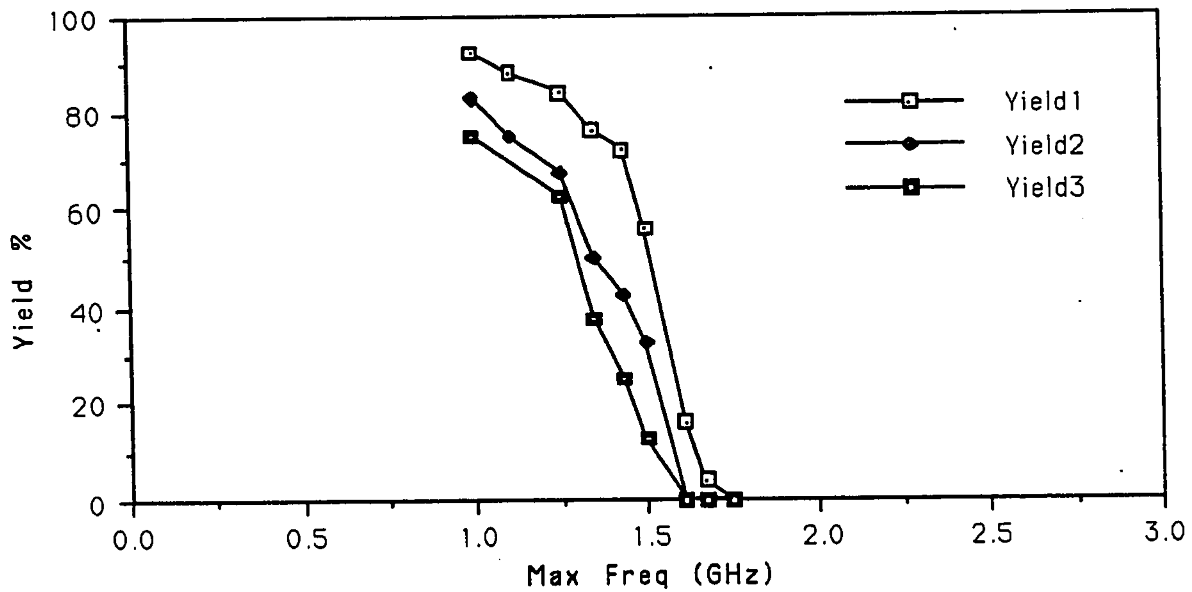

Figure 4.20: SCFL Parity circuit Yield vs. Frequency for different complexities without output cell

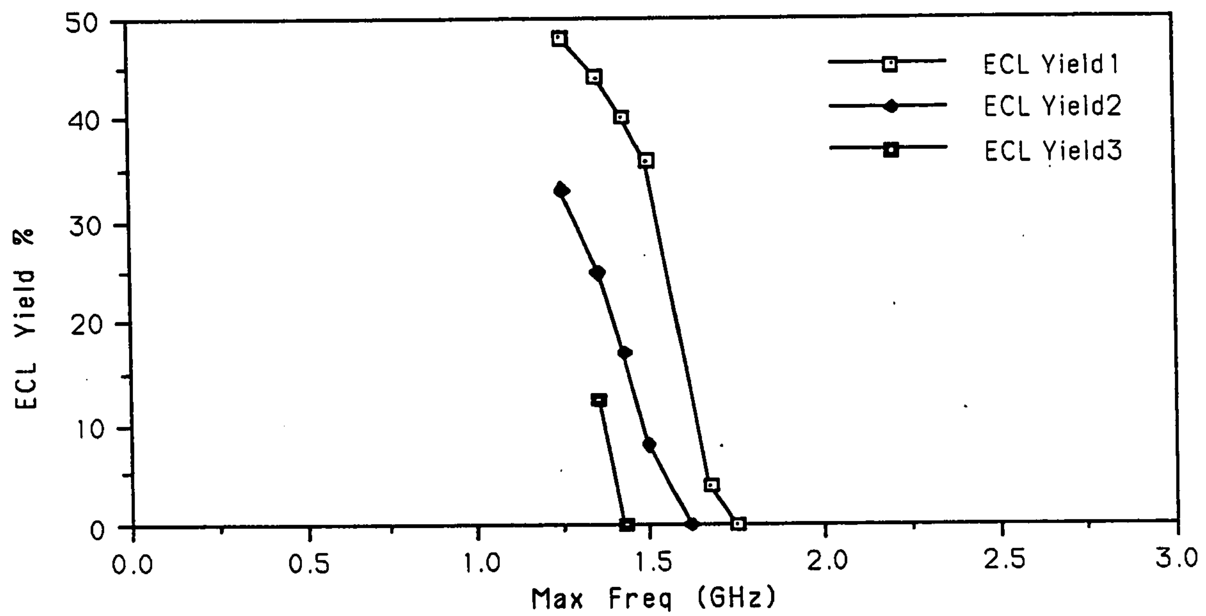

Figure 4.21: SCFL Parity circuit Yield vs. Frequency for different complexities with output cell

the yield characteristics of Fig. 4.20 and 4.21.

The conclusion of this chapter is that, given the large variations in process parameters, the yield of gallium arsenide SCFL circuits is limited by two factors:

1- The circuit architecture:

Because of the latency problem, as the circuit becomes complicated and more gate levels are used, the latency accumulates on the propagating signal which will result in erroneous output signals. This situation can be improved by a better design of the SCFL gate, and by introducing special timing circuits to synchronize the internal signals, and prevent the accumulation of latency.

2- The ECL interfacing criterion set on the output cell:

As can be concluded from the previous analysis, the ECL interfacing problem affects not only the yield for simple complexities, but it has also a severe effect on the yield as the complexity increases. This effect can be minimized by a better design of the output cell.

Chapter 5

Conclusion

In this research the effect of parametric uniformity, ECL compatibility, circuit architecture, and complexity on the yield versus speed characteristics of gallium arsenide SCFL circuits was studied.

The yield study was done as follows:

1- The circuit model parameters were extracted from a typical wafer composed of 25 sites, to account for their variations across the wafer.

2- An SCFL inverter chain from each site was simulated to measure the maximum speed of an inverter. Then, the yield versus frequency characteristic curve was derived.

3- An SCFL output cell from each site was simulated to measure the output logic voltage levels. All the output cells which are not ECL compatible were discarded. Then, a new yield versus speed characteristic curve which takes into account the ECL compatibility criterion, was derived.

4- A multi-input gate (2-input XOR) from each site was simulated. Then the maximum operating frequency was measured. From these measurements the yield versus frequency characteristic curve for multi-input gates was constructed.

5- The yield versus speed characteristic curve for SCFL multi-level gate circuits was theoretically predicted from the previous results. Then it was validated

by simulating a 2-level XOR gate parity generator circuit.

6- The SCFL circuit complexity was increased by a factor of 2, then 3 to account for the effect of complexity on the yield. The yield versus characteristics for different complexities were derived directly from the previous results assuming that when many sites are taken together then:

a- The maximum speed of the resulting site will be the minimum of the maximum speeds of the original sites.

b- The resulting site will be considered ECL compatible, only if all of the original sites are ECL compatible.

This yield study results show that given the actual spread in the model parameters, the maximum achievable yield is limited by: 1- The ECL compatibility, 2- The complexity. The circuit architecture is also an important factor. However, while the ECL compatibility constraint puts a limit on the maximum achievable yield, the circuit architecture can improve the yield versus speed characteristics only within the ECL compatibility limit. This suggests that the yield can be improved in two directions:

1- Tighter control of the process parameters to maximize the number of ECL compatible circuits. The SCFL circuits showed greatest sensitivity to the threshold voltage, the transconductance parameter, and the diode reverse saturation current, and particular attention should be given to the control of these.

2- Improving the circuit architecture to improve the yield to its maximum value allowed by the ECL compatibility constraint.

This study was done on typical process parameter measurements to study the yield of SCFL circuits, a similar study can be done for other gallium arsenide logic families, following the steps described above. Another way of doing this would be by assuming random variations of the circuit model parameters instead of extracting them from a typical wafer (typical means and variances of the model parameters are given in this

thesis). Then the yield would be predicted statistically, by monte-carlo analysis, for instance.

This study was very simplistic in considering the circuit architecture. A more in-depth analysis can be done to study the effect of circuit architecture on yield, and how it can be improved.

These can constitute interesting subjects for further research.

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Appendix A

Transistor and Diode Model Parameter Extraction

The transistor model used is the SAT 2, Level 3 of HSPICE MESFET model [10] which is the Cubic approximation of Curtice model, as indicated in chapter 2. The transistor and diode model parameters and the SCFL gate load resistance were extracted from the process parameters which were measured from the test structures used for process monitoring in IC fabrication in BNR.

A.1 Process Parameter Distribution

The supplied parameters are: V_{to}, I_{Dss}, R_{DS}, G_{DS}, V_D, and $R_\square$, as described in chapter 4. The spreads of these parameters at room temperature (27 degrees Celsius) across the wafer are shown in fig. A.1, A.2, A.3, A.4, A.5, and A.6 respectively. Note that these parameters are not independent, which is consistent with theory. We can notice for instance that V_{to}, I_{Dss}, and G_{ds} graphs have very similar patterns.

The model parameters λ, β, α, I_S, and R_L, were extracted as follows:

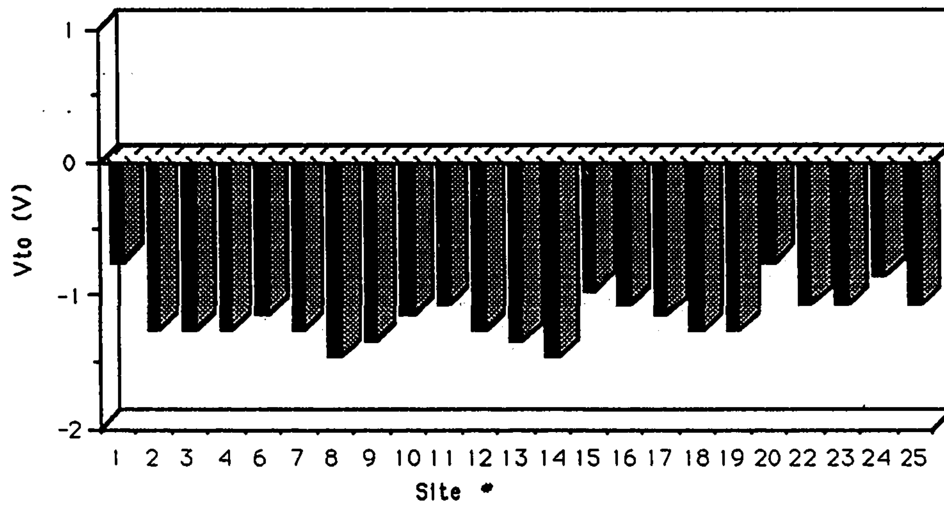

Figure A.1: V_{to} spread across the wafer

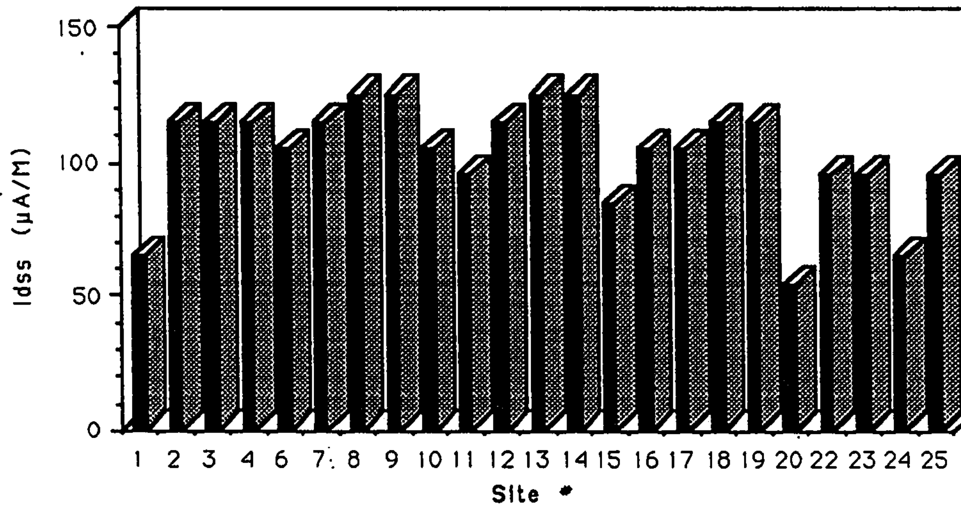

Figure A.2: I_{Dss} spread across the wafer, at $V_{GS} = 0$

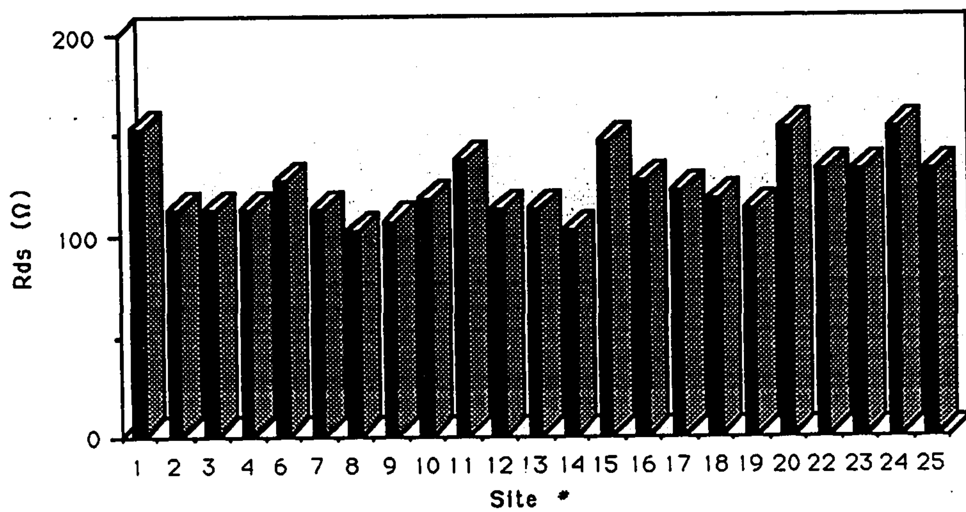

Figure A.3: R_{DS} spread across the wafer

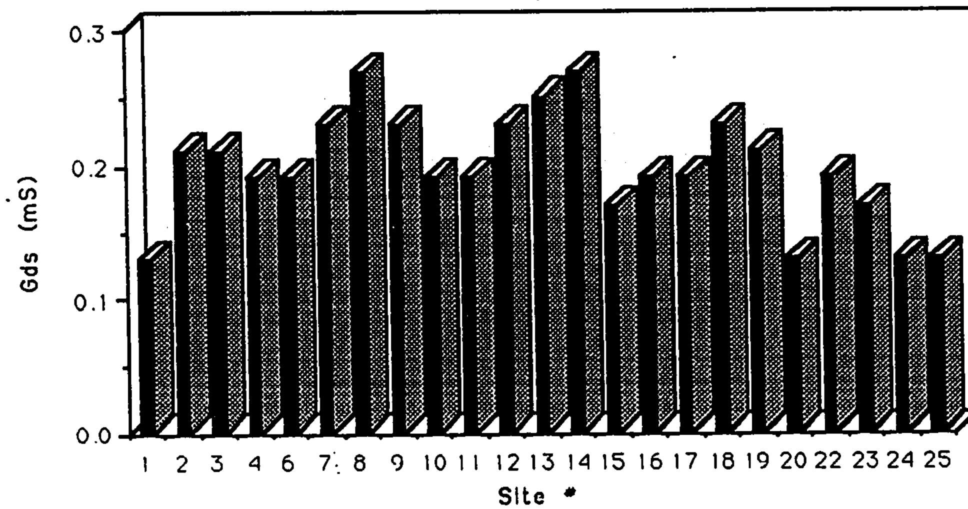

Figure A.4: G_{DS} spread across the wafer

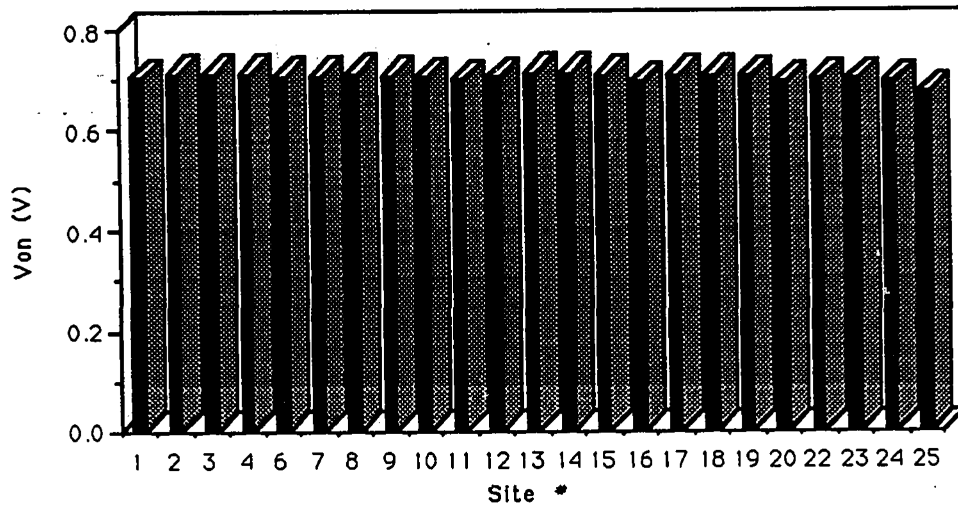

Figure A.5: V_{on} spread across the wafer at $I_s = 150\mu A/\mu M$

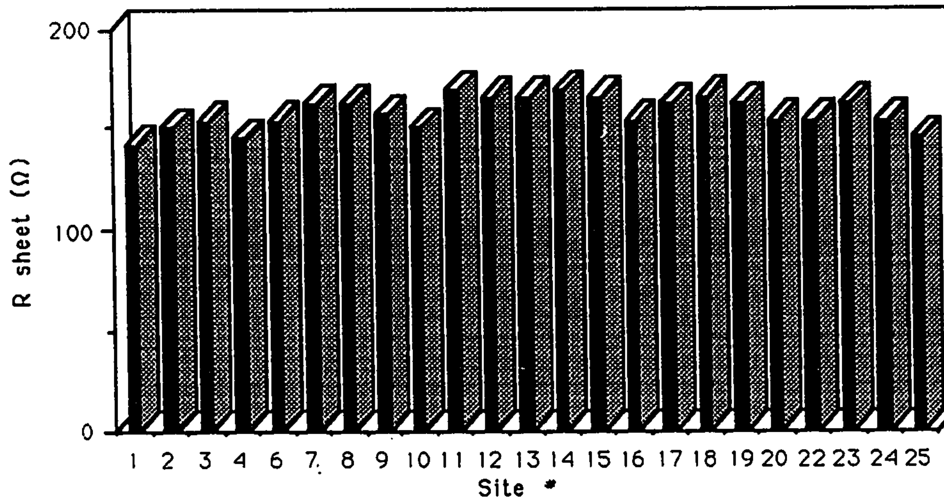

Figure A.6: $R_\square$ spread across the wafer

A.2 Transistor Model Parameter Extraction

A.2.1 Extraction of λ and β

The two model parameters λ and β can be extracted using the supplied parameters G_{DS}, I_{Dss}, and V_{to} as follows:

The transistor output conductance is defined as:

$$G_{DS} = \frac{dI_{DS}}{dV_{DS}} \quad (A.1)$$

When the transistor is in saturation.

From chapter 2 we know that the drain current I_{DS} is given by:

$$I_{DS} = \beta_{eff} V_{GST}^2 (1 + \lambda V_{DS}) \quad (A.2)$$

Where β_{eff} and V_{GST} are defined as:

$$\beta_{eff} = \frac{\beta \cdot W \cdot M}{L(1 + ucrit \cdot V_{GST})} \quad (A.3)$$

$$V_{GST} = V_{GS} - (V_{to} + \gamma_{DS} V_{DS}) \quad (A.4)$$

And:

$\gamma_{DS} = -67.16e - 3$

$ucrit = 0.288V^{-1}$

$V_{DS} = 2.5V$

By replacing equation A.2 into A.1 we obtain:

$$G_{DS} = \frac{d\beta_{eff}}{dV_{DS}} V_{GST}^2 (1 + \lambda V_{DS}) + \beta_{eff} \frac{d(V_{GST}^2)}{dV_{DS}} (1 + \lambda V_{DS}) + \beta_{eff} V_{GST}^2 \frac{d(1 + \lambda V_{DS})}{dV_{DS}} \quad (A.5)$$

On the other hand the transistor drain saturation current I_{Dss} is obtained by replacing V_{GS} with 0 in equation A.4 which yields:

$$I_{Dss} = (V_{to} + \gamma_{DS} V_{DS})^2 (1 + \lambda V_{DS}) \quad (A.6)$$

After manipulating the two equations A.5 and A.6 we obtain:

$$\beta = \frac{(1 + ucrit \cdot V_{GST})L}{WV_{GST}^2}\left[\frac{I_{Dss}}{V_{GST}^2}\left(\frac{ucrit \cdot \gamma_{DS}V_{GST}^2V_{DS}}{1 + ucrit \cdot V_{GST}} - 2\gamma_{DS}V_{GST}V_{DS} + V_{GST}^2\right) - \gamma_{DS}V_{DS}\right] \tag{A.7}$$

And:

$$\lambda = \frac{G_{DS} - B_{eff}\left[\frac{\gamma_{DS} ucrit V_{GST}^2}{1+ucrit \cdot V_{GST}}\right]}{\beta_{eff}\left[\frac{ucrit \cdot \gamma_{DS} \cdot V_{GST}^2 V_{DS}}{1+ucrit \cdot V_{GST}} - 2\gamma_{DS}V_{GST}V_{DS} + V_{GST}^2\right]} \tag{A.8}$$

A.2.2 Extraction of α

The model parameter α can be extracted using the linear drain to source resistance R_{DS}, which is defined as:

$$R_{DS} = \frac{V_{DS}}{I_{DS}} \tag{A.9}$$

For $V_{DS} \simeq 0$.

The drain I_{DS} current is given by:

$$I_{DS} = \beta_{eff}V_{GST}^2(1 + \lambda V_{DS})\left[1 - \left(1 - \alpha\frac{V_{DS}}{3}\right)^3\right] \tag{A.10}$$

After expanding equation A.10 and neglecting the terms that include V_{DS} assuming that V_{DS} is small and close to 0 (in the linear region of the transistor) we obtain the following equation:

$$I_{DS} = \beta_{eff} \cdot \alpha \cdot V_{GST}^2 \cdot V_{DS} \tag{A.11}$$

This yields:

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\beta_{eff} \cdot \alpha \cdot V_{GST}^2} \tag{A.12}$$

Since β is known from equation A.7 then α will be:

$$\alpha = \frac{1}{\beta_{eff} \cdot R_{DS} \cdot V_{GST}^2} \tag{A.13}$$

A.3 Diode Model Parameter Extraction

The diode model parameter I_S is extracted using the diode turn-on voltage V_D. The diode current equation is given, as in chapter 2, by:

$$I_D = I_S \left[\exp(\frac{qV_{D,i}}{nK_T}) - 1 \right] \tag{A.14}$$

Where $V_{D,i}$ is given by:

$$V_{D,i} = V_D - I_D R_S \tag{A.15}$$

And:

$I_D = 150\mu A/\mu M$

$R_S = 400\Omega \cdot \mu M.$

$n = 1.18$

Therefore I_S will be:

$$I_S = \frac{I_D}{\exp(\frac{qV_{D,i}}{nK_T}) - 1} \tag{A.16}$$

A.4 SCFL Gate Load Resistance Extraction

The load resistance R_L is extracted from the sheet resistance $R_\square$. Since the load resistance is linearly proportional to the sheet resistance, then the load resistance will be given by:

$$R_L = \frac{R_{LN}}{R_{\square N}} \cdot R_\square \tag{A.17}$$

Where:

$R_{LN} = 1150\Omega$, is the nominal load resistance.

$R_{\square N} = 150\Omega/\square$, is the nominal sheet resistance.

A.5 Temperature Scaling

The supplied process parameters were measured at room temperature (27 degrees Celsius). However, the circuit simulation for yield study has to be done at 150 degrees Celsius.

Therefore, all the model parameters have to be scaled to the simulation temperature, i.e. 150 degrees Celsius. The temperature scaling as done in BNR is as follows: Except for the model parameter I_S which has an exponential dependence on temperature, all the other parameters have a simple first order linear dependence, as shown below:

1- For I_S:

$$I_S(T) = I_S \cdot \exp\left[T_{CIS} \cdot \left(\frac{1}{T} - \frac{1}{TNOM}\right)\right] \quad \text{(A.18)}$$

2- For all other parameters:

$$parameter(T) = parameter \cdot [1 + (T - TNOM) \cdot TCparameter] \quad \text{(A.19)}$$

Where T is the operating temperature in Kelvin (equal to 423 degrees K in our case), $TNOM = 298$ degrees K, and $TCparameter$ is defined as follows:

a- Transistor Parameters:

$TCIS = -8.968e3K^{-1}$

$TCRG = 327.7e - 6K^{-1}$

$TCRD = 1.617e - 3K^{-1}$

$TC\gamma_{DS} = 182.6e - 6K^{-1}$

$TC\beta = 0$

$TCucrit = 5.172e - 3K^{-1}$

$TCV_{to} = -891.8e - 6K^{-1}$

$TC\alpha = -341.7e - 6K^{-1}$

$TC\lambda = 2.702e - 3K^{-1}$

$TCCGS = 500e - 6K^{-1}$

$TCRDS = 0$

b- Diode Parameters:

$TCIS = -8.968e3$

$TCRS = 1.4e - 3$

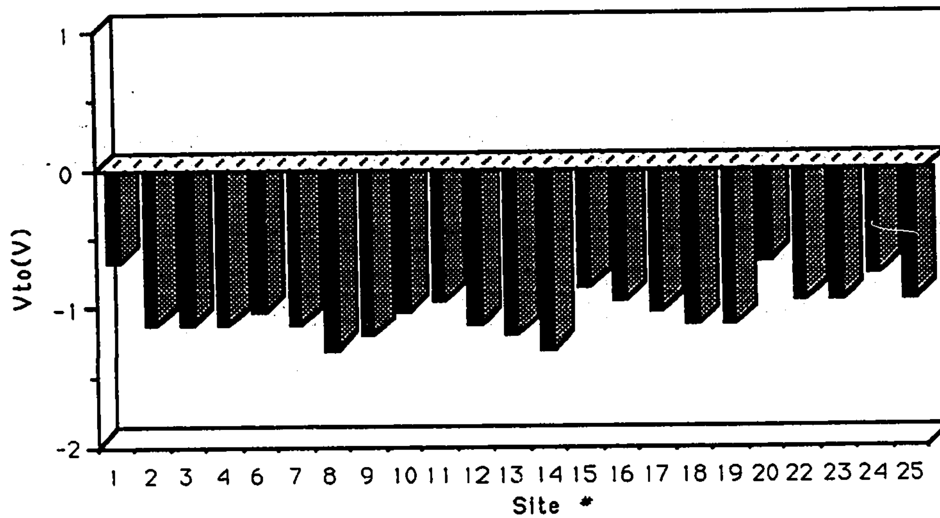

Figure A.7: V_{to} spread across the wafer at 150 degrees C

c- Load resistance:

> The load resistors used in the SCFL gates are fabricated using ion implantation. The temperature coefficients can be as low as 100 $ppm/°C$, which are well below those obtained for diffused resistors [22]. Therefore their variations with temperature are neglected in the simulations.

The spread of the extracted parameters V_{to}, λ, β, α, I_S, and R_L across the wafer, at 150 degrees C, are shown in Fig A.7, A.8, A.9, A.10, A.11, and A.12 respectively.

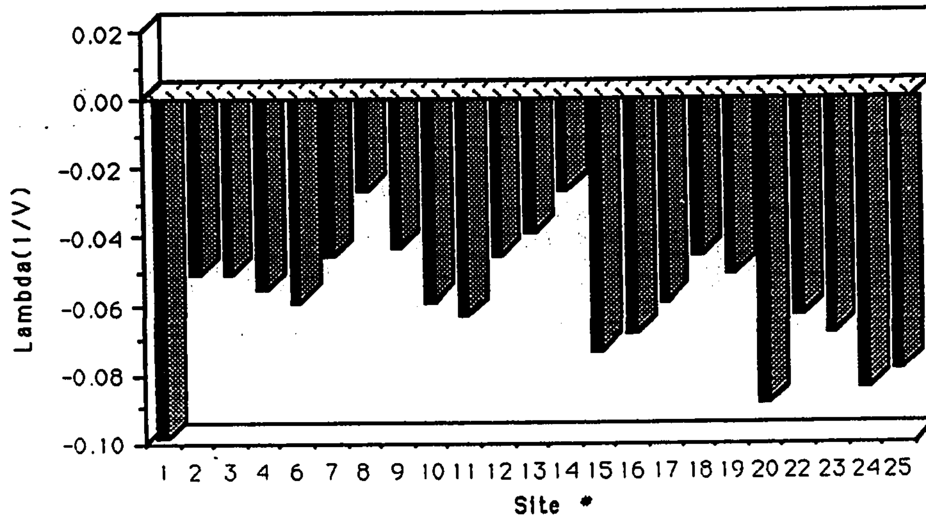

Figure A.8: λ spread across the wafer at 150 degrees C

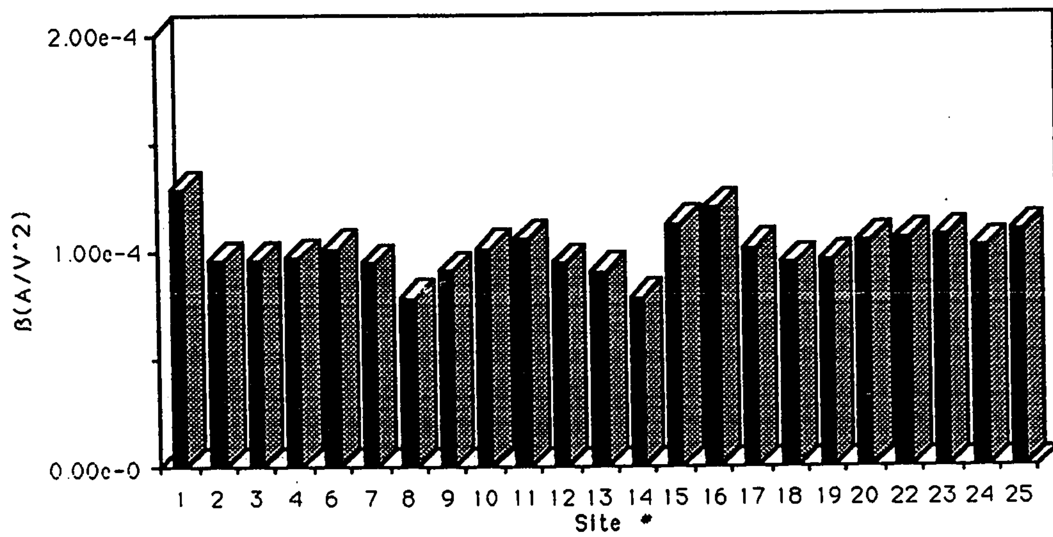

Figure A.9: β spread across the wafer at 150 degrees C

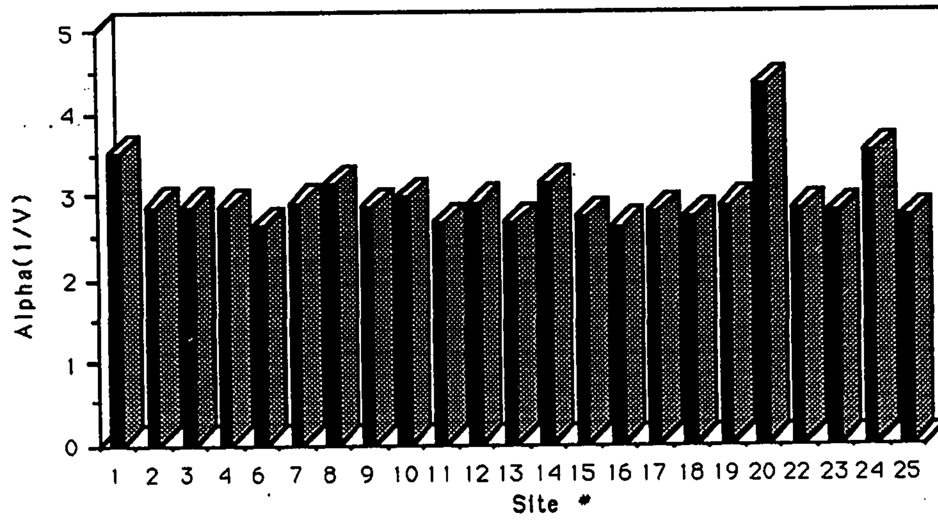

Figure A.10: α spread across the wafer at 150 degrees C

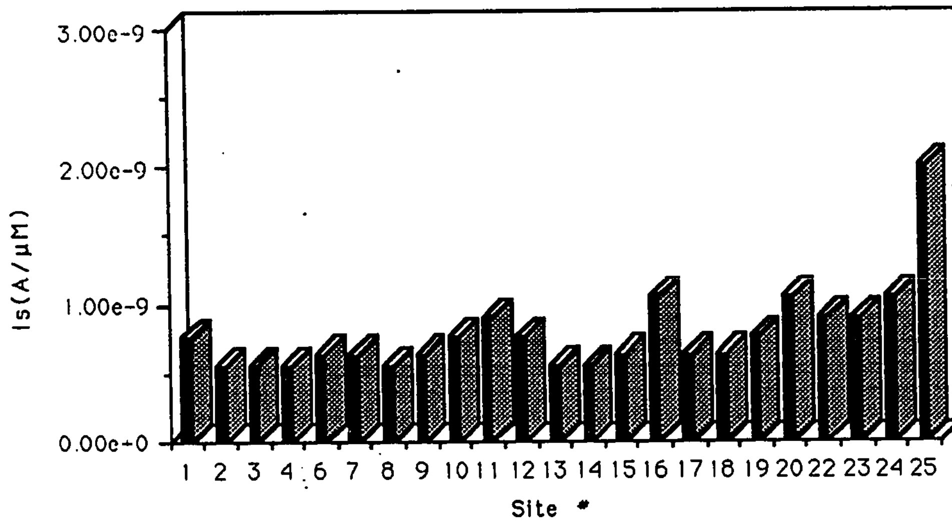

Figure A.11: I_S spread across the wafer at 150 degrees C

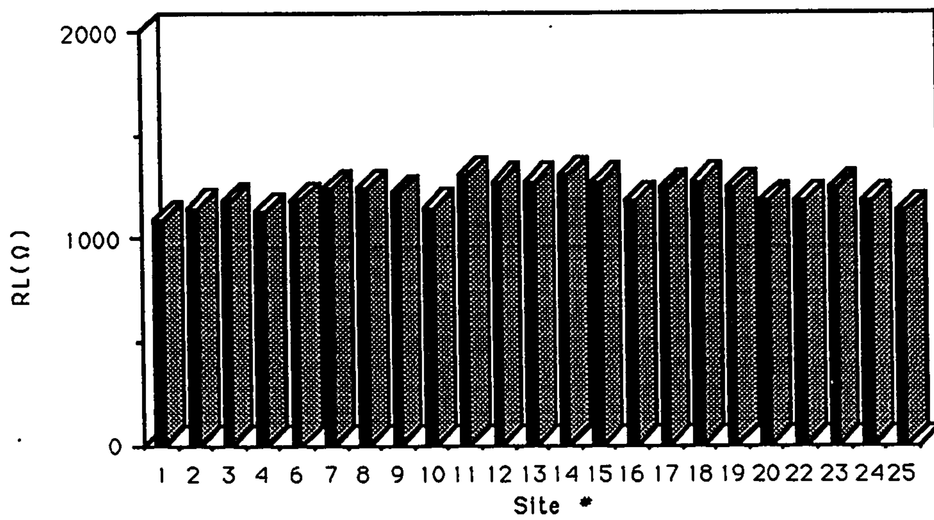

Figure A.12: R_L spread across the wafer at 150 degrees C