

POWER AND NOISE AS PHYSICAL SIZE LIMITATIONS
TO MICROELECTRONIC ELEMENTS

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ABSTRACT

There are several reasons for decreasing component size or for microminiaturization in general. Some of these are reliability, cost, and weight and volume limitations. Reliability can be improved by reduction of solder connections and by the possibility of redundancy. By reducing labour and the uncertainty of manual assembly and by increasing the yield of circuits, it is believed that the cost per circuit would be greatly reduced. Finally, weight and volume savings are of great importance in military and space electronics.

This thesis examines extensively two factors which could limit component size, specifically, power dissipation and inherent device noise. These two factors will be treated independently, since the first will determine the maximum power which an element can withstand before thermal breakdown occurs, while the second will influence the minimum signal power that one can have.

It has been found that a 50-micron square silicon monolithic transistor with a 20-micron square emitter can dissipate a maximum of 30 milliwatts. Also, the minimum signal power required to overcome the inherent transistor noise power is in the order of picowatts even for MHz. bandwidth.

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INTRODUCTION

1.1: Historical Review

Since the invention of the transistor, people have strived to reduce the physical size of these new elements envisaging, as already mentioned, not only a saving of space but also of cost and reliability improvement. However, it has only been within the past nine years, since 1958, that any significant progress has been made.

Research was begun as early as 1953 in both the United States and England to try to produce then, so called, solid microcircuits; that is, circuits contained entirely within one block of semiconductor material having no wires or discrete components as such, but with these components forming an integral part of the semiconductor chip. However, it was not until 1958 that actual progress in fabricating these was reported. At present, the state of the art is such that 0.5 cm. square monolithic integrated circuits have been produced and are commercially available such as, for instance, the Motorola operational amplifier MC 1433. Further miniaturization is being approached in research where the units produced are at least ten times smaller than those commercially available. Manufacturing difficulties have been the major obstacle to size reduction; however, improvements in photosensitive materials have, in part, resolved these difficulties.

Moreover, the theoretically known potential of the scanning electron microscope to define line widths in the Angstrom range, may be of major importance to future size reduction.

1.2: Physical Size Limitation Problem

In the late 1950's J.T. Wallmark [1] considered this size problem as being one of packing density and hinted that some means other than that of discrete components must be envisaged in order to further decrease circuit size. For such a system, he gave an empirical upper bound for the packing density as that of the human brain - approximately 10^7 parts per cm^3 .

One of his limitations to size was that of heat dissipation; however, his consideration was one of average power dissipation per element, the whole system being taken as some kind of sphere containing a number of identical elements in which the temperature rise was considered. He suggested that heat dissipation will be a major problem in increasing the packing density since a bulk of material can dissipate only a fixed amount of heat, the quantity of heat dissipated being a function of the surface area of the system. His other factors of size limitation were concerned with the manufacturing stage in which there is a high probability of breakage, of contamination of elements, etc.

J.J. Suran in 1961 pointed out five basic problems [2] associated with microcircuits, the first two of which, power dissipation and thermal generation, cannot be really separated. He further made the important statement that a certain minimum power is generally required to overcome the non-linearities of the circuit components at very low current and voltage levels and consequently power and bandwidth are directly related. This factor brings out an important point that one cannot reduce size merely by reducing the power dissipated in the circuit - assuming power to be a major factor in size limitation.

He then showed that if one were to reduce power dissipation by operating at lower voltages and currents these low energy circuits would be more susceptible to noise and component variations. His treatment of heat produced and dissipated is similar to that of Wallmark in that they both assumed a spherical source of heat and using this consideration, they obtained a temperature difference between the hottest point in the system considered and the outer surface of the system.

In 1962, Wallmark and Marcus [3] proposed that there exists an absolute lower limit to device size and an absolute upper limit to packing density based on statistical variations in impurity distribution, maximum resolution of semiconductor

fabrication methods, influence of radiation, and power density. It should be noted that the first two factors are strictly associated with manufacturing technology while the latter is innate to all circuits in any system.

Cosmic radiation, which has been extensively treated by these authors, would seem to be more a limitation of the reliability of fabricated circuits. However, it would seem that the probability of a cosmic ray hitting some element in a complete system should decrease with decreasing size. This probability of component damage should be very small since cosmic rays hit the earth at the rate of approximately one to two particles per cm^2 - min. at sea level. It would further seem that, even considering these occurrences, one would get an increase in generation-recombination noise rather than actual component failure. However, more study is needed in this field in order to come to some definite conclusion regarding its effect on component size and failure.

Power is again treated as a major limiting factor by these authors but in a different way. They treat temperature as being a limitation in packing density in so far as it limits the doping of the material in the active region of semiconductor devices rather than considering the effect which too much or too little power will have on each element.

Very large power densities, approximately 10^5 watts/cm³. for a unit similar to that considered in the first part of this thesis, are obtained by these authors. This figure compares with the value of 1.2×10^5 watts/cm³. encountered in this thesis.

A more recent approach [4] is that thermal failure limits the performance of thin film devices by lowering its figure of merit or gain-bandwidth product. In this approach each element is treated separately from the whole circuit with regards to its heat dissipation and this may seem to be the most applicable to microcircuits.

This approach of individually treating the elements as to power dissipation will also be followed in this thesis although for a different purpose - that of seeing how power limits the size of microelectronic components and hence of systems. It will be shown that transistors of micron dimensions can withstand milliwatt powers before thermal breakdown of the unit occurs.

Most of the factors outlined by the authors quoted can be improved by improving technology. For instance, the performance of microcircuits which was limited by the large parasitic capacitances between the substrate and the components and which decreased the bandwidth appreciably, need only be little affected. This is so because thin film or monolithic

components deposited or diffused such that they are isolated from the substrate (EPIC by Motorola [5]) do not seem to suffer from this effect and these have been found to be as fast in switching as their hybrid counterparts.

Moreover, not considering cooling apparatus, power dissipation and almost all types of transistor noise cannot be improved with improved technology. Power dissipation requirements will be a definite limitation in all types of both active and passive devices, while noise may limit some devices more than others. The latter factor becomes more pronounced as size decreases since surface effects might play a more important part.

The type of transistor and the mode of operation of the circuit will be important in noise considerations. For instance, in the case of active devices, the bipolar transistor has a different noise figure from the unipolar devices. Moreover, noise will have a greater influence in amplifier design than in switching network design where the important factor is merely to have the signal power larger than the noise power, the latter being below the switching threshold.

In the following it will be shown that quite large powers, in the milliwatt range, are capable of being dissipated even by micron-sized elements. It is further shown that the effect of transistor noise is negligible if such factors as source

resistance are optimized with the result that the minimum signal power required to overcome this noise power is in the picowatt range even for MHz. bandwidth.

Moreover, an attempt will be made to relate power dissipation and noise power to monolithic component dimension. That is, the power capabilities of a unit of certain given dimensions will be shown to have an upper limit imposed by power dissipation and a lower signal power limit imposed by the noise of the device.

Disregarding the dissipation limitation of the package, it will be seen that the minimum dimensions of a unit will be dictated by its maximum power dissipation capabilities. Also, using the derived formulas and the curves obtained in the first part of this thesis, one may obtain the minimum dimensions of an element given the maximum power or vice versa.

POWER CONSIDERATIONS

2.1: Introductory Comments

In order to obtain a minimum system size considering power and noise, one must first find out how are the individual components limited by these two factors. If the system is considered as a bulk, the temperature distribution throughout will vary because the component density will not be uniform throughout. In order to properly treat the subject, therefore, one must consider the construction of a real system in which the elements making up the system are treated individually.

2.2: System Under Consideration

The components considered will be those which are already in production today - monolithic integrated circuits. Although only this type of element (See Fig. 1) will be discussed, the theory of heat dissipation developed applies to any component in which the element thickness is small compared to the substrate thickness and where heat flow is mostly due to conduction through the substrate. Hence, this theory could be applied to other devices such as FET's or MOS transistors.

It should be noted also that a single element has been removed from a large system (See Fig. 2) in order to reduce the problem to one of solving for the maximum power density that this individual component can withstand.

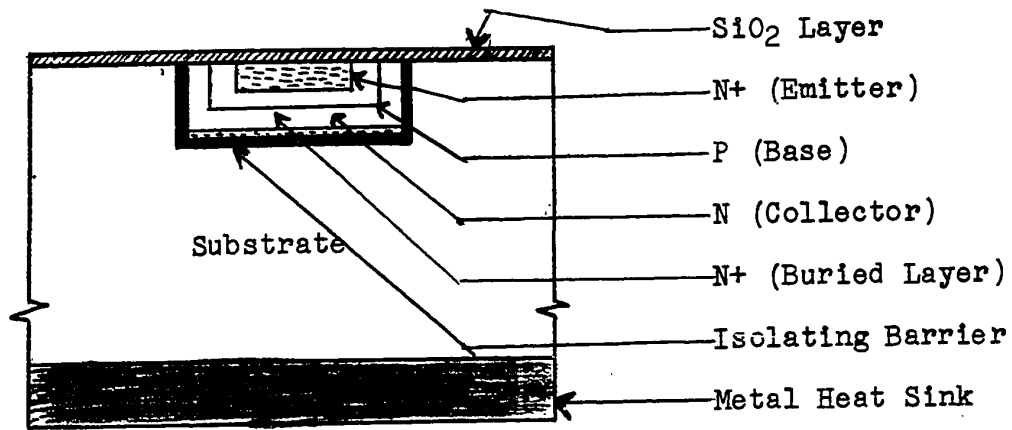


Fig. 1: Typical Monolithic Integrated Transistor

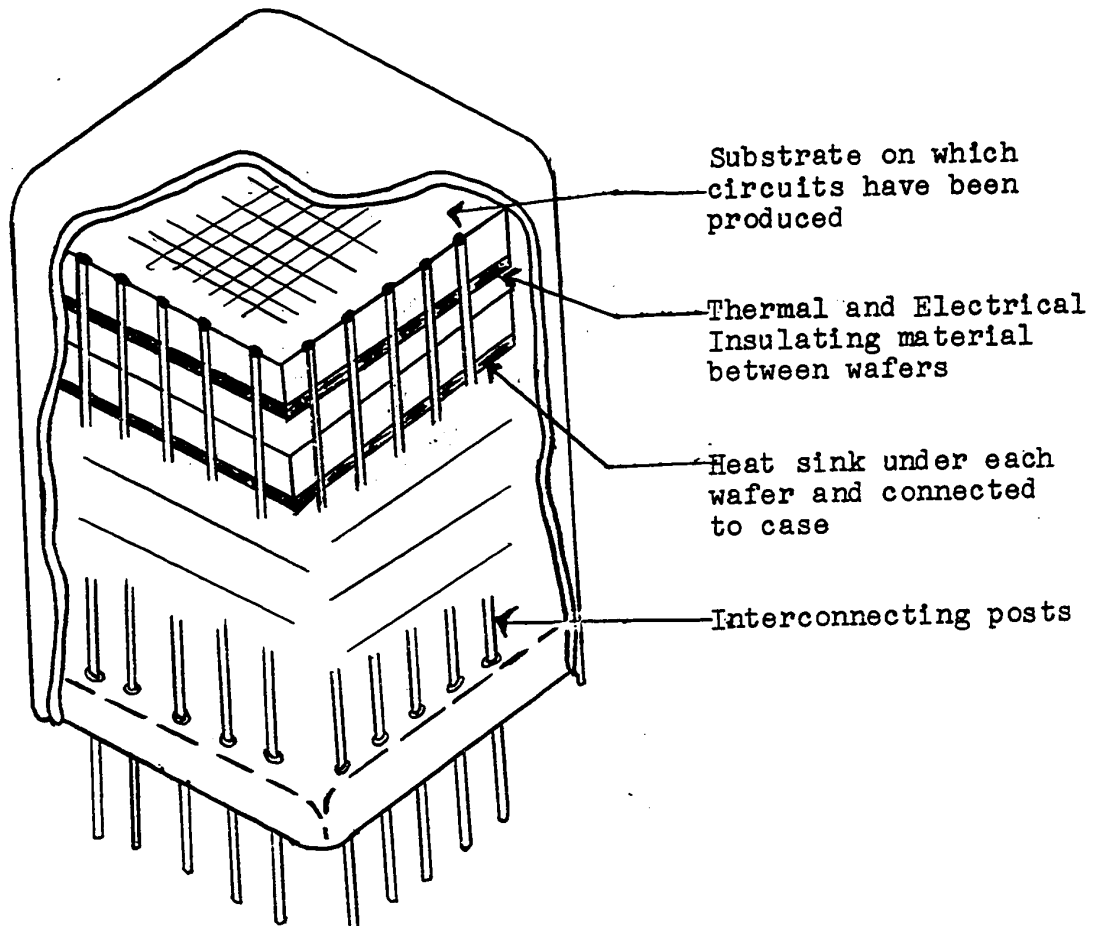


Fig. 2: System sketch showing wafers, interconnecting posts and casing.

2.3: Assumptions

2.3.1: Physical Dimensions

An early assumption that must be made is that the substrate thickness " t_s ", (See Fig. 3), is large compared to the element produced on it. In other words, the substrate makes up the bulk of the total system with the elements forming the various circuits being only of negligible thickness as compared to the substrate.

This is a reasonable assumption to make since present substrate thickness is of the order of six mils (.006 in.) for silicon while epitaxially grown or diffused thickness can be a fraction of micron [25 microns (μ) = 1 mil]. So transistors and diodes can be made which are approximately 10 microns thick while resistors can be made much thinner. This can be seen to represent a thickness ratio of approximately 15:1.

With technological improvements, substrate and element thickness can possibly be brought down further; however, very thin silicon wafers become extremely hard to handle with the result that breakage is very high. So the practical limit has been set at approximately six mils. Nevertheless, it will be assumed here that further size reduction is possible due to improved manufacturing methods and a best possible practical limit of substrate thickness will be set at 100μ (or approximately four mils).

The component width, taken as 20 microns, is assumed to be available with present day technology. The resolution of integrated circuit lithographic process is limited to the wavelength of the ultraviolet light used which can at best be taken as 1000 Angstroms ($1 \text{ \AA} = 10^{-8} \text{ cm.}$). Improvements to this figure will come about with improvements in electron beam machining whose ultimate resolution has been suggested [6] to be accurate to within 100 \AA . However, assuming for the present a resolution of 1000 \AA and assuming a maximum deviation of 1% in length and width dimensions, then the minimum value of film width should be:

$$\begin{aligned} \text{Max. possible deviation} &= 2 \times 1000 \text{ \AA} \\ 1\% \text{ width} &= 2 \times 10^3 \text{ \AA} \\ \therefore \text{width} &= 20 \times 10^{-4} \text{ cm.} \\ &= 20 \text{ microns} \end{aligned}$$

2.3.2: Dissipation Assumption

The second assumption made is that, in the structure considered (See Fig. 3), the heat loss or dissipation is due to conduction through the substrate only. This is not unreasonable because the system considered has been assumed to have a thermal and electrical insulating material of suitable thickness separating every wafer from each other.

In actual fact, existing circuits not having insulating material still rely on the same assumption since the heat lost by convection and radiation is negligible compared to that lost by conduction through the substrate and the metal case used.

Associated with this assumption is the fact that we are taking the thermal resistance between the parts of the component and the substrate to be negligible and hence, there is no temperature differential between them.

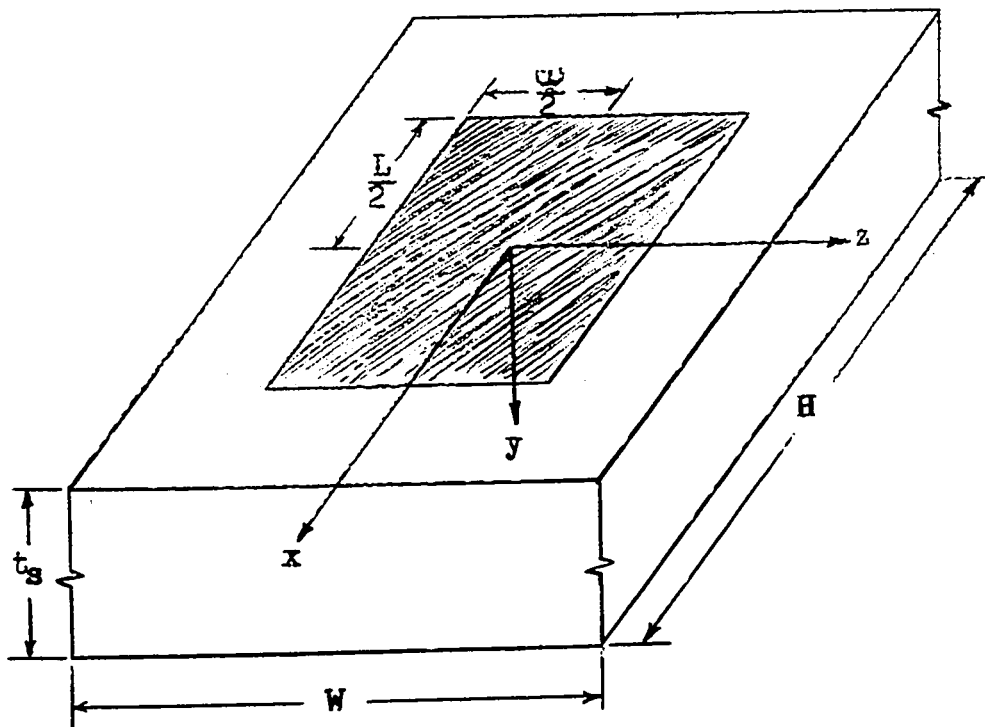


Fig. 3: Minute part of the wafer containing only one component and showing the dimensions and the axes used.

A further point in this assumption is that the element is taken as being a uniform constant source of heat at the component-substrate interface. This again is reasonable if the heat is considered to be produced by a current flowing uniformly through the element which is considered as a one dimensional flat surface. By using this assumption, the temperature at the interface can be found by means of Laplace's equation and by using further the first assumption of the element thickness being negligibly small, the solution can be used as being representative of the temperature of the element for any reasonable power input.

2.3.3: Boundary Conditions

Before proceeding to the actual mathematical treatment of the subject certain boundary conditions must be stated.

(i) It will be assumed that the bottom of the substrate (i.e. at $y = t_s$) has settled to some steady state temperature T_1 . This condition implies a continuous removal of heat from the heat sink attached to the substrate and the case (Shown in Figs. 1 and 2).

(ii) The second boundary condition that must be satisfied is that which concerns the periphery of the area surrounding the element. In Fig. 3 this periphery has been taken to be at $x = \pm \frac{H}{2}$ and $z = \pm \frac{W}{2}$.

Since a number of devices placed on a uniform substrate in a regular array are being dealt with, then there must be no heat flow across the boundary at these points; that is, the heat produced in one element will not affect the element next to it.

(iii) Finally, the steady state solution is the only one which will be dealt with.

2.4: Heat Flow Problem

Taking into consideration the above assumptions and using the arrangement shown in Fig. 3, the maximum operating temperature of the element (shaded) must be related to the power dissipation capabilities of this component. This may be done by solving the heat conduction equation for the given configuration taking into account the element and substrate geometries and the given boundary conditions.

Thus the problem is represented by Laplace's equation [7] as follows:

$$\nabla^2 T(x, y, z) = 0 \quad (1)$$

where ∇^2 has the usual form $\left[\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} \right]$ and

where $T(x, y, z)$ is the temperature at any point (x, y, z) . The solution to equation (1) can be obtained by using the standard procedure of separation of variables [8].

Using this technique

$$T(x, y, z) = X(x) Y(y) Z(z) \quad (2)$$

Performing the necessary operations on (2) and substituting into equation (1), Laplace's equation becomes:

$$\frac{1}{X} \frac{\partial^2 X}{\partial x^2} + \frac{1}{Y} \frac{\partial^2 Y}{\partial y^2} + \frac{1}{Z} \frac{\partial^2 Z}{\partial z^2} = 0 \quad (3)$$

Each term of equation (3) is a function of only one independent variable and so each term may be equated to some constant (p^2 , $-q^2$, and r^2 say) such that

$$p^2 + r^2 = q^2 \quad (4)$$

Thus one has the following three equations to solve:

$$\frac{1}{X} \frac{\partial^2 X}{\partial x^2} = -p^2 \quad (5)$$

$$\frac{1}{Y} \frac{\partial^2 Y}{\partial y^2} = q^2 \quad (6)$$

$$\frac{1}{Z} \frac{\partial^2 Z}{\partial z^2} = -r^2 \quad (7)$$

These equations have well known solutions which can be written as follows:

$$X = [A \cos px + B \sin px] \quad (8)$$

$$Y = [C \cosh qy + D \sinh qy] \quad (9)$$

$$Z = [E \cos rz + F \sin rz] \quad (10)$$

Substituting equations (8), (9), and (10) into (2) one finally gets

$$T(x,y,z) = [A \cos px + B \sin px][C \cosh qy + D \sinh qy][E \cos rz + F \sin rz] \quad (11)$$

Now using the given boundary conditions one can solve for the constants of equation (11).

$$\text{At } x = \pm \frac{H}{2} \quad U = -K \frac{\partial T}{\partial x} = 0 \quad (12)$$

Where U is the heat flow across the boundary.

$$\frac{\partial T}{\partial x} = Y(y)Z(z) \left[-A p \sin px + B p \cos px \right]_{x=\pm \frac{H}{2}} = 0 \quad (13)$$

Since $Y(y)$ and $Z(z)$ are not in general zero at $x = \pm \frac{H}{2}$ then in order to satisfy equation (13) one must have

$$A \sin \frac{pH}{2} - B \cos \frac{pH}{2} = 0$$

$$\text{and } A \sin \frac{pH}{2} + B \cos \frac{pH}{2} = 0$$

In evaluating p one must also consider that $T(0,0,0) \neq 0$ and hence A will not be zero. But, to satisfy the above equations one must have

$$B = 0 \text{ and } A \sin \frac{pH}{2} = 0$$

$$\text{or } p = \frac{2(n-1)\pi}{H} \quad n = 1, 2, 3, \dots$$

$$\text{Hence } X(x) = \sum_{n=1}^{\infty} A_n \cos \frac{2(n-1)\pi x}{H} \quad (14)$$

$$\text{Similarly, at } z = \pm \frac{W}{2} \quad U = -K \frac{\partial T}{\partial z} = 0$$

Thus one finds that $F = 0$ and

$$r = \frac{2(m-1)\pi}{W} \quad m = 1, 2, 3, \dots$$

$$\text{So } Z(z) = \sum_{m=1}^{\infty} E_m \cos \frac{2(m-1)\pi z}{W} \quad (15)$$

Substituting (14) and (15) into (11) one gets:

$$T(x, y, z) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} A_n E_m \cos \alpha_n x \left[C_{mn} \cosh q_{mn} y + D_{mn} \sinh q_{mn} y \right] \cos \beta_m z \quad (16)$$

$$\text{Where } \alpha_n = \frac{2(n-1)\pi}{H} \quad (17)$$

$$\beta_m = \frac{2(m-1)\pi}{W} \quad (18)$$

$$q_{mn} = 2\pi \left[\left(\frac{n-1}{H} \right)^2 + \left(\frac{m-1}{W} \right)^2 \right]^{\frac{1}{2}} \quad (19)$$

Equation (16) can be rewritten as:

$$T(x, y, z) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} (A_m G_{mn} E_m) \cos \alpha_n x \left[\cosh q_{mn} t_s + \frac{D_{mn}}{C_{mn}} \sinh q_{mn} y \right] \cos \beta_m z \quad (20)$$

Using the condition that at $y = t_s$, $T = T_i = \text{constant}$ after steady state has been achieved. Hence

$$T_i = \sum_m \sum_n A_{mn} \cos \alpha_n x \cos \beta_m z \left[\cosh q_{mn} t_s + \frac{D_{mn}}{C_{mn}} \sinh q_{mn} t_s \right] \quad (21)$$

T_i is constant, therefore all variables of x and z must disappear from the above equation. Noting that for $m = 1, n = 1$ one merely gets the constant a_{11} , then (21) can be rewritten as:

$$T_i = a_{11} + \sum_m \sum_n a_{mn} \cos \alpha_n x \cos \beta_m z \left[\cosh q_{mn} t_s + \frac{D_{mn}}{C_{mn}} \sinh q_{mn} t_s \right] \quad (21a)$$

Where the following condition must exist for the sum, $m = n \neq 1$. For this equation to hold, the sum or the second part of the right hand side of (21a) must be equal to zero. Thus

$$\frac{D_{mn}}{C_{mn}} = - \frac{\cosh q_{mn} t_s}{\sinh q_{mn} t_s}$$

Therefore equation (20) becomes

$$T(x, y, z) = T_1 + \sum_{m=1}^{\infty} \sum_{\substack{n=1 \\ m \neq n}}^{\infty} a_{mn} \frac{\cos \alpha_n x \sinh \alpha_{mn} (t_s - y) \cos \beta_m z}{\sinh \alpha_{mn} t_s} \quad (22)$$

Using now the condition that the heat flux Q flowing through the active device per cm^2 , per sec. is given by

$$Q = -K \frac{\partial T}{\partial y} \text{ at } y = 0 \quad (23)$$

Then the value of a_{mn} in terms of the constants Q and K can be obtained. Differentiating (22) and using equation (23) for $y = 0$

$$-\frac{Q}{K} = - \sum_{m=1}^{\infty} \sum_{\substack{n=1 \\ m \neq n}}^{\infty} \frac{a_{mn} \alpha_{mn} \cosh \alpha_{mn} t_s \cos \alpha_n x \cos \beta_m z}{\sinh \alpha_{mn} t_s}$$

or more conveniently

$$\frac{Q}{K} = \sum_{m=1}^{\infty} \sum_{\substack{n=1 \\ m \neq n}}^{\infty} b_{mn} \cos \alpha_n x \cos \beta_m z \quad (24)$$

$$\text{Where } b_{mn} = \frac{a_{mn} \alpha_{mn} \cosh \alpha_{mn} t_s}{\sinh \alpha_{mn} t_s} \quad (25)$$

Now using Fourier's method [7] on equation (24) first multiply both sides by $\cos \alpha_n x$ and then integrate over the whole period. That is

$$\frac{Q}{K} \int_{-\frac{H}{2}}^{\frac{H}{2}} \frac{\cos 2(k-1)\pi x dx}{H} = \sum_m \sum_n b_{mn} \cos \beta_m z \int_{-\frac{H}{2}}^{\frac{H}{2}} \frac{\cos 2(n-1)\pi x \cos 2(k-1)\pi x dx}{H}$$

The right hand integral will be zero for all $k \neq n$

while the left hand integral is the same as

$$\frac{Q}{K} \int_{-\frac{H}{2}}^{\frac{H}{2}} \frac{\cos 2(k-1)\pi x dx}{H}$$

This can be assumed to apply because, if the surface plane is under consideration then heat is produced only within the interval $-\frac{L}{2} \leq x \leq \frac{L}{2}$ and $-\frac{W}{2} \leq z \leq \frac{W}{2}$ while at the rest of the surface $Q = 0$. In other words, on the surface at $y = 0$ heat is given off through the substrate only by the thin film component while the rest of the surface has zero heat (See Fig. 4).

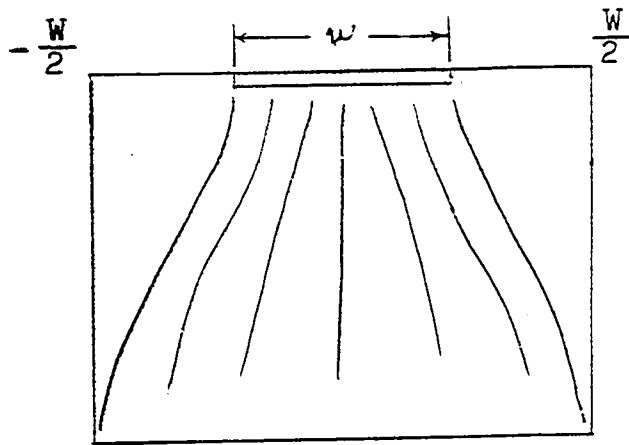


Fig. 4: Assumed heat flow from element through substrate; in the area between $-\frac{w}{2}$ and $\frac{w}{2}$, $-\frac{W}{2}$ and $\frac{W}{2}$, $Q = 0$

Hence changing the limits for the left hand integral and putting $k = n$ one gets

$$\frac{Q}{K} \left(\frac{1}{\alpha_n} \left[\sin \alpha_n x \right]_{-1/2}^{1/2} \right)^{1/2} = \sum_m b_{mn} \cos \beta_m z \left(\frac{1}{2} \right) \left[\frac{1}{\alpha_n} \sin \alpha_n x + x \right]_{-1/2}^{1/2}$$

Thus $\frac{2Q}{K\pi(n-1)} \sin \frac{\alpha_n L}{2} = \sum_m b_{mn} \cos \beta_m z$ (26)

Performing a similar operation for z and using the reasoning outlined in Fig. 4 one gets finally

$$b_{mn} = \frac{4Q}{K\pi^2(n-1)(m-1)} \sin \frac{\alpha_n L}{2} \sin \frac{\beta_m \omega}{2} \quad (27)$$

Using (27) in equation (25) one gets

$$a_{mn} = \frac{4Q \sin \frac{\alpha_n L}{2} \sin \frac{\beta_m \omega}{2}}{2 K\pi^2 q_{mn}(n-1)(m-1)} \tanh q_{mn} t_s \quad (28)$$

Thus equation (22) becomes

$$T(x, y, z) = T_i + \sum_{\substack{m=1 \\ m \neq 1}}^{\infty} \sum_{\substack{n=1 \\ n \neq 1}}^{\infty} \frac{4Q \sin \frac{\alpha_n L}{2} \sin \frac{\beta_m \omega}{2} \cos \alpha_n x \sinh q_{mn}(t_s - y) \cos \beta_m z}{K\pi^2 q_{mn}(n-1)(m-1) \cosh q_{mn} t_s} \quad (29)$$

Equation (29) gives the temperature distribution throughout the substrate including that at the component-substrate interface. The latter holds since it was assumed that there was no thermal resistance at the interface.

Having obtained the temperature distribution one must be concerned only with the maximum or critical temperature at the element or substrate surface.

Clearly from equation (29), the maximum temperature at the surface ($y = 0$) occurs at $x = 0$ and $z = 0$. Therefore, inserting these values in (29) it becomes

$$T_c = T_i + \sum_{\substack{m=1 \\ m \neq 1}}^{\infty} \sum_{\substack{n=1 \\ n \neq 1}}^{\infty} \frac{4Q \sin \frac{\alpha_n L}{2} \sin \frac{\beta_m \omega}{2}}{K\pi^2 q_{mn}(m-1)(n-1)} \tanh q_{mn} t_s \quad (30)$$

In most practical cases, one usually has the maximum temperature difference between the element and the substrate base available (ΔT_c).

$$\begin{aligned} \Delta T_c &= (T_c - T_i) \\ &= \frac{4Q}{K\pi^2} \sum_m \sum_n \frac{\sin \frac{\alpha_n L}{2} \sin \frac{\beta_m \omega}{2}}{q_{mn}(n-1)(m-1)} \tanh q_{mn} t_s \end{aligned} \quad (31)$$

Equation (31) can be put in a more suitable form for computing by removing the restriction $m = n \neq 1$ and thus it becomes (See Appendix A)

$$\begin{aligned} \frac{\Delta T_c K}{Q} &= \frac{2H\omega}{\pi^2 W} \sum_{n=2}^{\infty} \frac{\sin \frac{\alpha_n L}{2}}{(n-1)^2} \tanh \alpha_n t_s + \frac{2WL}{\pi^2 H} \sum_{m=2}^{\infty} \frac{\sin \frac{\beta_m \omega}{2}}{(m-1)^2} \tanh \beta_m t_s + \\ &+ \frac{4}{\pi^2} \sum_{m=2}^{\infty} \sum_{n=2}^{\infty} \frac{\sin \frac{\alpha_n L}{2} \sin \frac{\beta_m \omega}{2}}{(n-1)(m-1)q_{mn}} \tanh q_{mn} t_s \end{aligned} \quad (32)$$

Since Q has been assumed constant throughout the component or thin film element, the total power dissipation " P_M " can be incorporated into equation (32):

$$\begin{aligned} \Psi &= \frac{\Delta T_c K}{P_M} \\ &= \frac{2W}{\pi^2 \omega H} \sum_{m=2}^{\infty} \frac{\sin \frac{\beta_m \omega}{2}}{(m-1)^2} \tanh \beta_m t_s + \frac{2H}{\pi^2 \omega L} \sum_{n=2}^{\infty} \frac{\sin \frac{\alpha_n L}{2}}{(n-1)^2} \tanh \alpha_n t_s + \\ &+ \frac{4}{\pi^2 \omega L} \sum_{m=2}^{\infty} \sum_{n=2}^{\infty} \frac{\sin \frac{\alpha_n L}{2} \sin \frac{\beta_m \omega}{2}}{(n-1)(m-1)q_{mn}} \tanh q_{mn} t_s \end{aligned} \quad (33)$$

Where $P_M = Q\omega L$ is the total maximum power produced and dissipated and where Ψ is the "Thermal Factor".

2.5: Approximations and Computations

In Section 2.3 certain quantities have been assumed constant - specifically K , t_s and ω , the first has been assumed constant and independent of temperature while the latter two have been specified by the present best available technology.

With equation (33), then, if one is given the type of substrate material and the film and substrate dimensions, one can determine the maximum power which the element can tolerate.

As can be seen, this equation has too many variables; however, by fixing some of them and varying one, the variation in Ψ can be observed. However, it is of more interest to plot the inverse of the thermal factor.

Two variables have already been fixed by the existing technology

$$t_s = 100 \mu$$

$$\omega = 20 \mu$$

Next, suitable ranges for the other variables are chosen: W must be chosen such that $W > \omega$ otherwise the derivation of Ψ is affected. Thus, for ease of computation the following ranges are chosen

$$W = [25, 30, 35, 40, 50, 60] \text{ in microns}$$

$$H = RW, R = [1, 2, 3, 5, 7, 9] \text{ dimensionless}$$

$$L = PH, P = [0.4, 0.5, 0.6, 0.7, 0.8] \text{ dimensionless}$$

Where, as with W , H must be greater than but not equal to L .

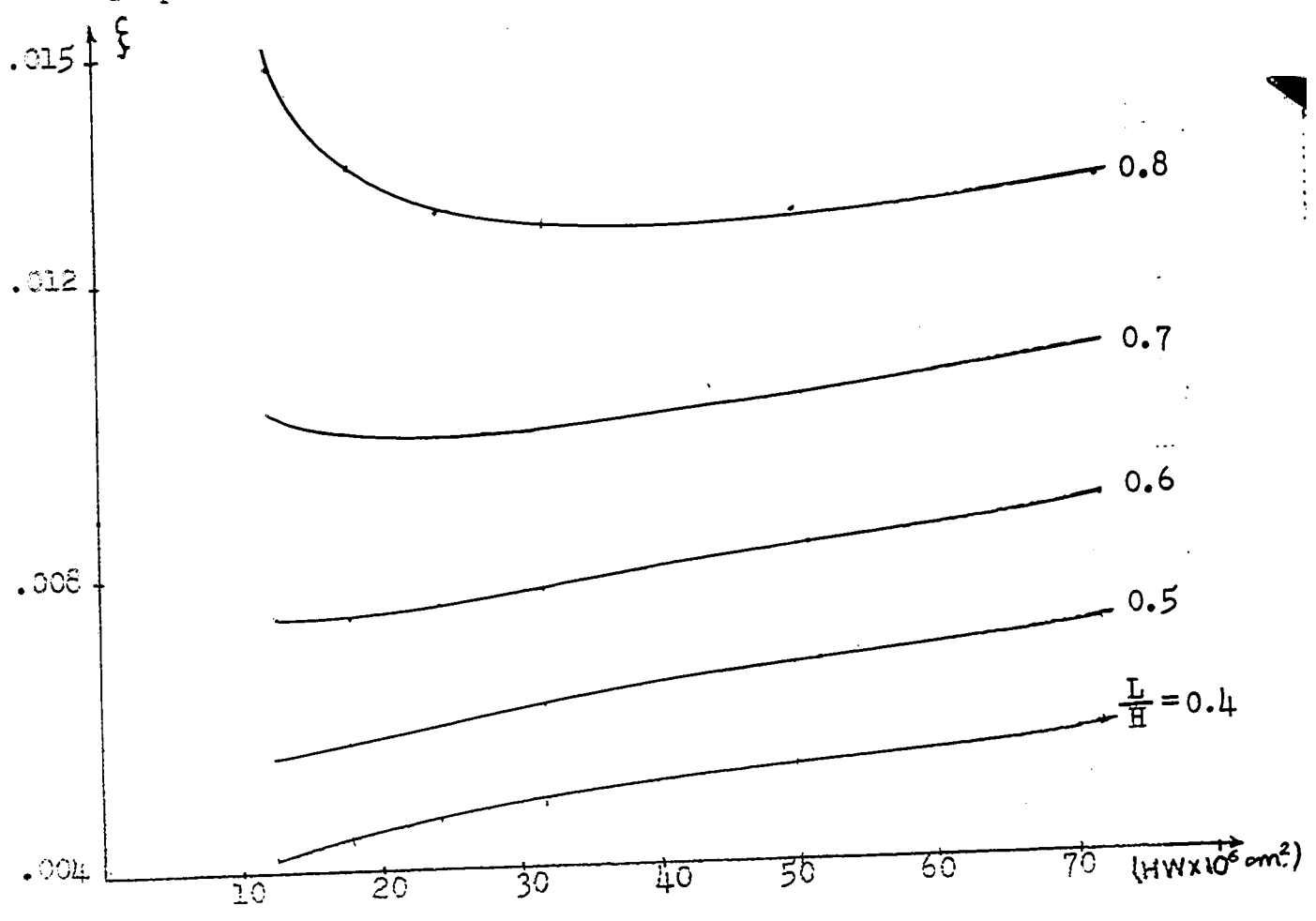
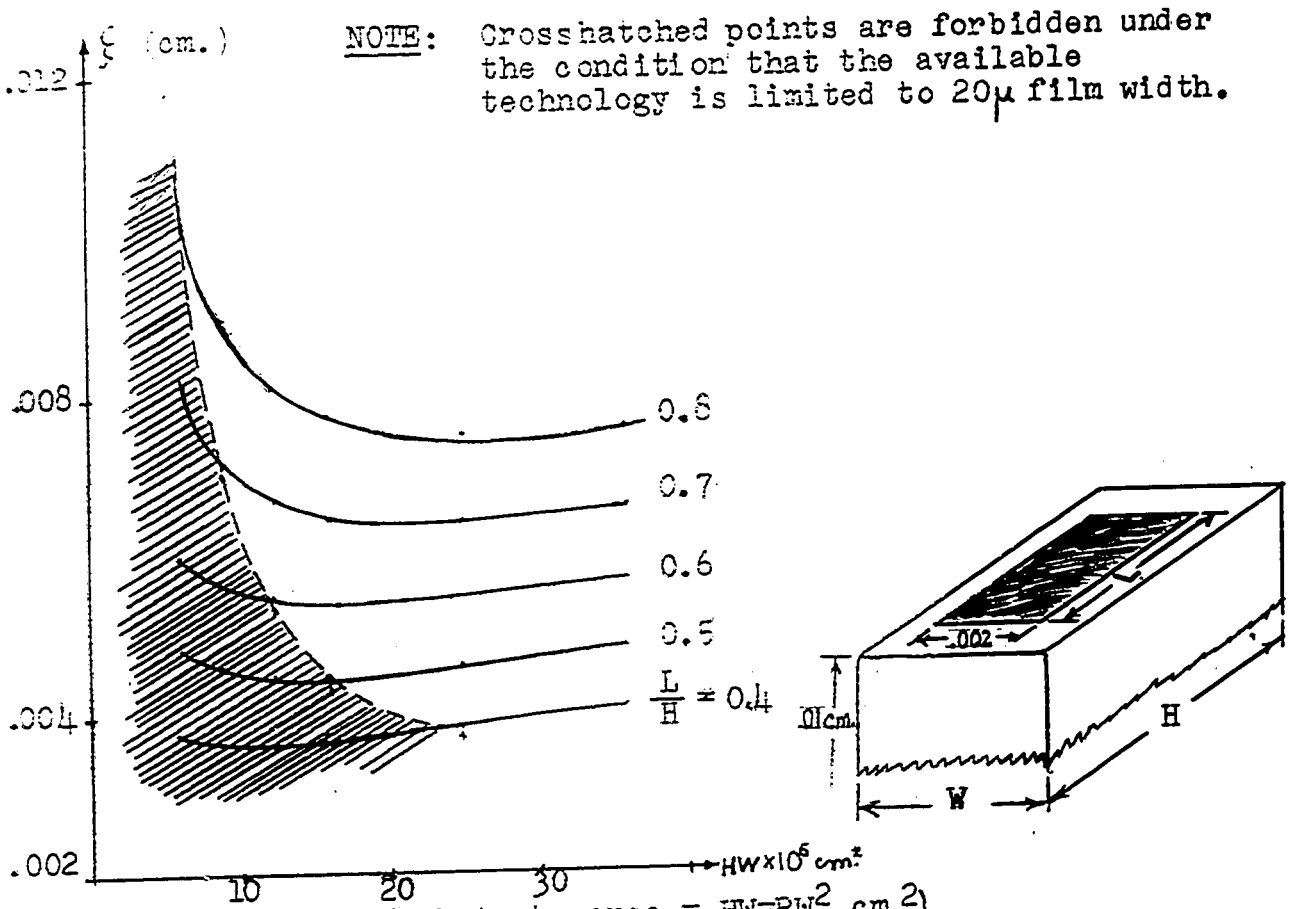
Substituting these parameters into equation (33) one gets

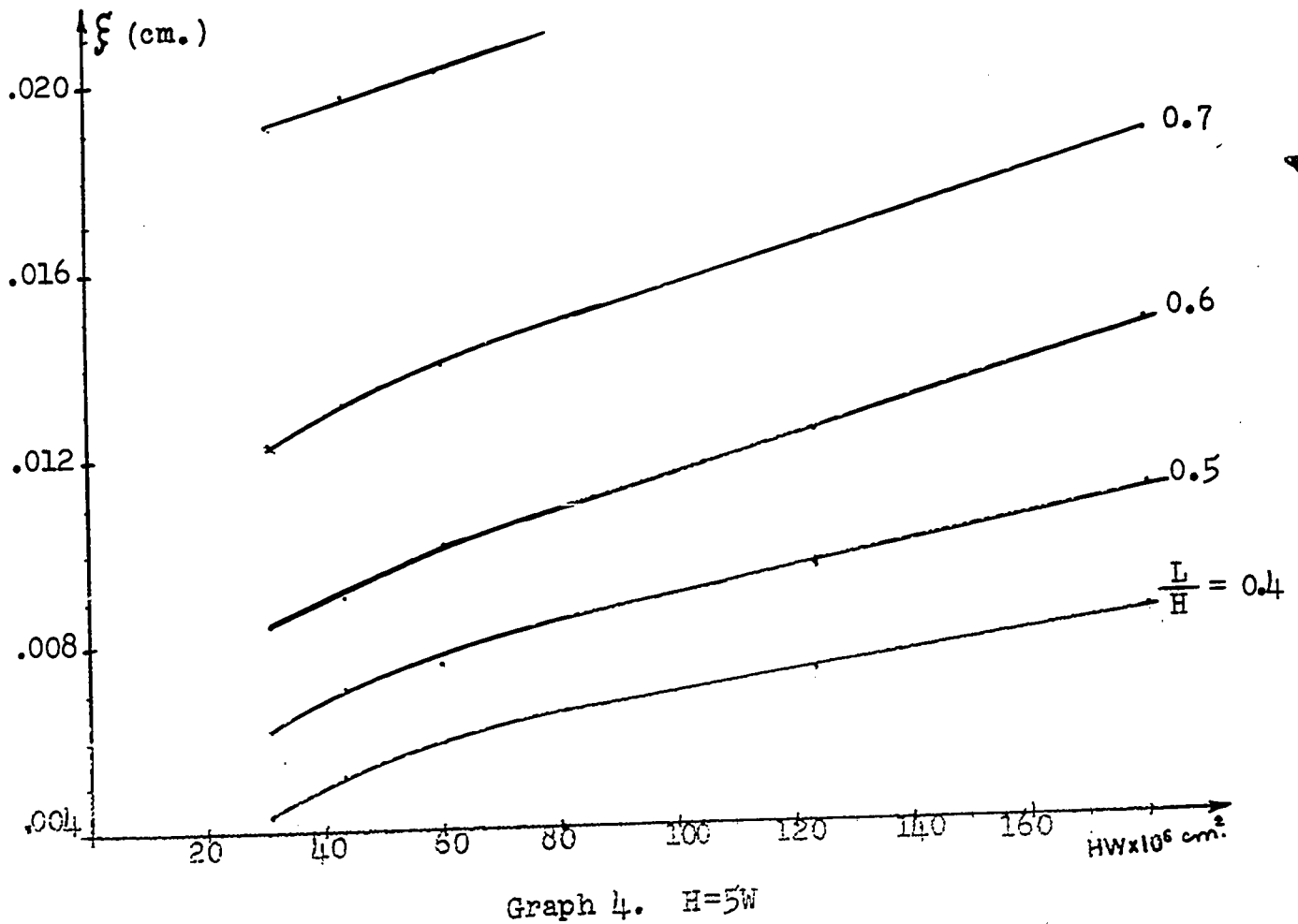
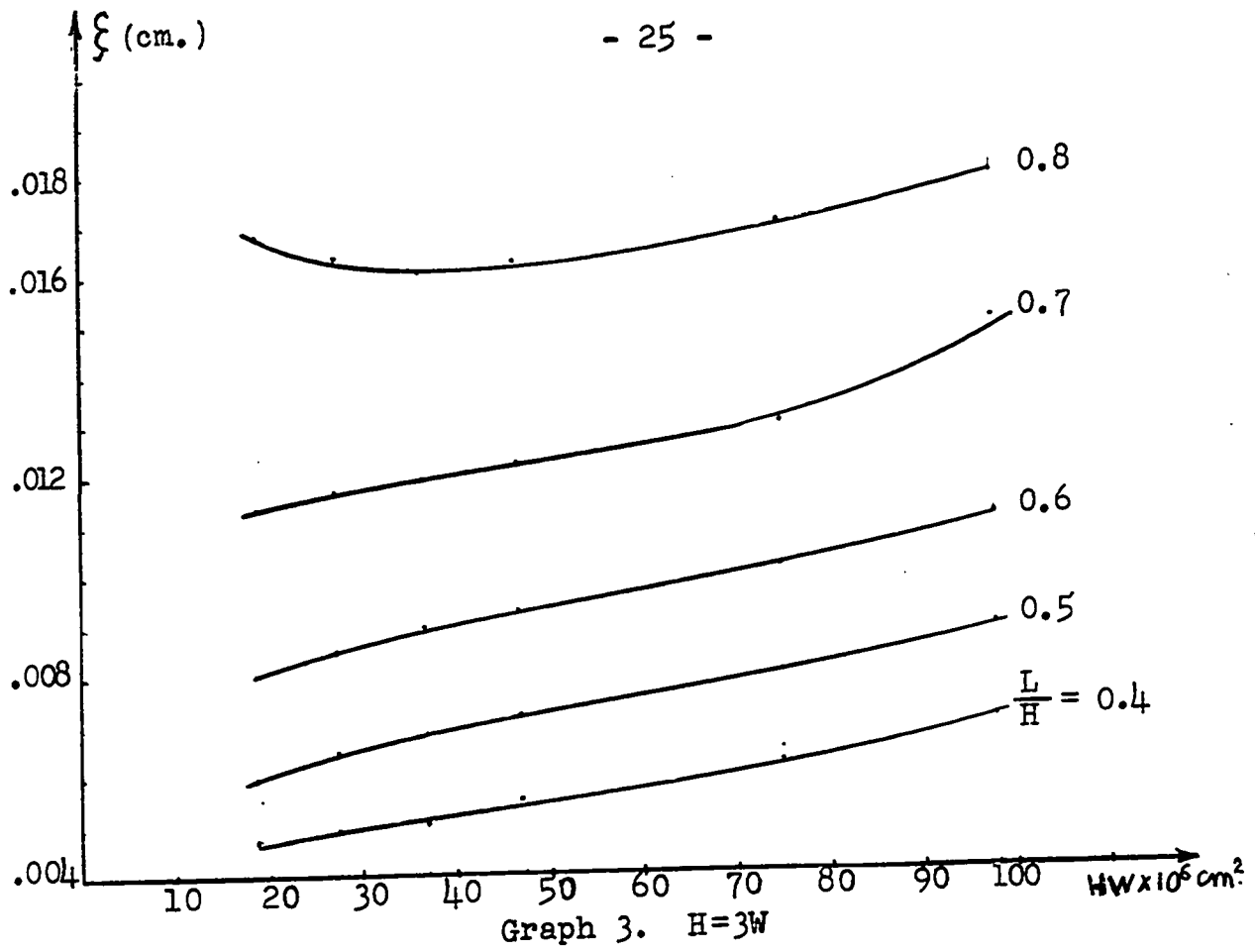
$$\begin{aligned} \Psi = & \frac{12250}{121R} \sum_{m=2}^{\infty} \frac{\sin \frac{0.044(m-1)}{7W}}{(m-1)^2} \tanh \frac{.44(m-1)}{7W} + \\ & + \frac{49}{242WP} \sum_{n=2}^{\infty} \frac{\sin \frac{22P(n-1)}{7}}{(n-1)^2} \tanh \frac{0.44(n-1)}{7RW} + \\ & + \frac{42875}{1331PR} \sum_{m=2}^{\infty} \sum_{n=2}^{\infty} \frac{\sin \frac{22P(n-1)}{7} \sin \frac{.044(m-1)}{7W}}{(n-1)(m-1) \left[\left(\frac{n-1}{R} \right)^2 + (m-1)^2 \right]^{\frac{1}{2}}} \tanh \frac{.44}{7W} \left[\left(\frac{n-1}{R} \right)^2 + (m-1)^2 \right]^{\frac{1}{2}} \end{aligned} \quad (34)$$

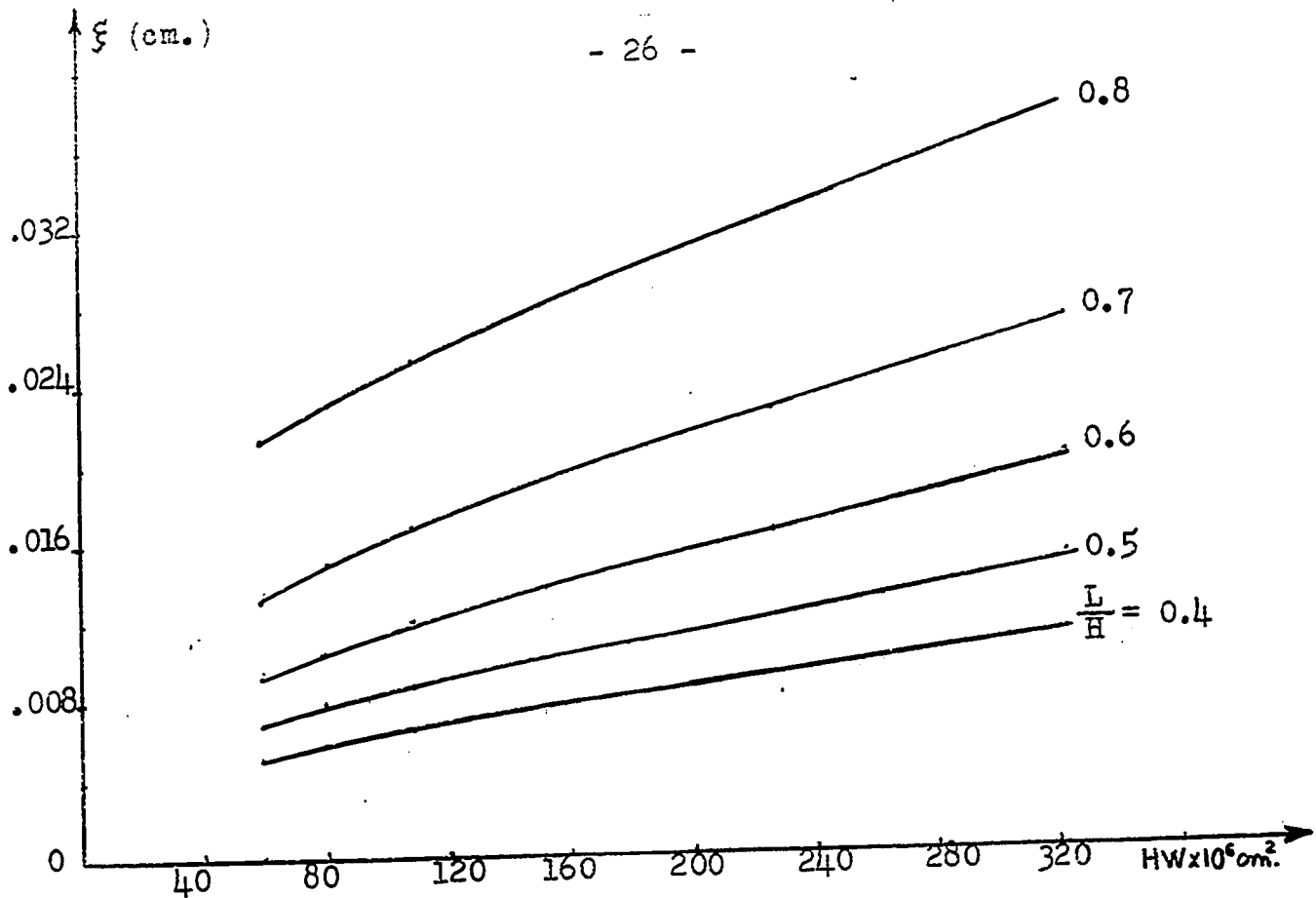
This function will be approximated for several values of P, R, and W.

Equation (34) was used to compute Ψ for various ranges of variables on the IBM 360 digital computer. The program used is shown in Appendix "D". From the thermal factor obtained, its inverse was taken, denoted as ξ , in order to see directly the variation in power with variations in substrate area. The following sets of curves are such plots of ξ versus substrate area for various constants. (Computer results are given in Appendix "E".)

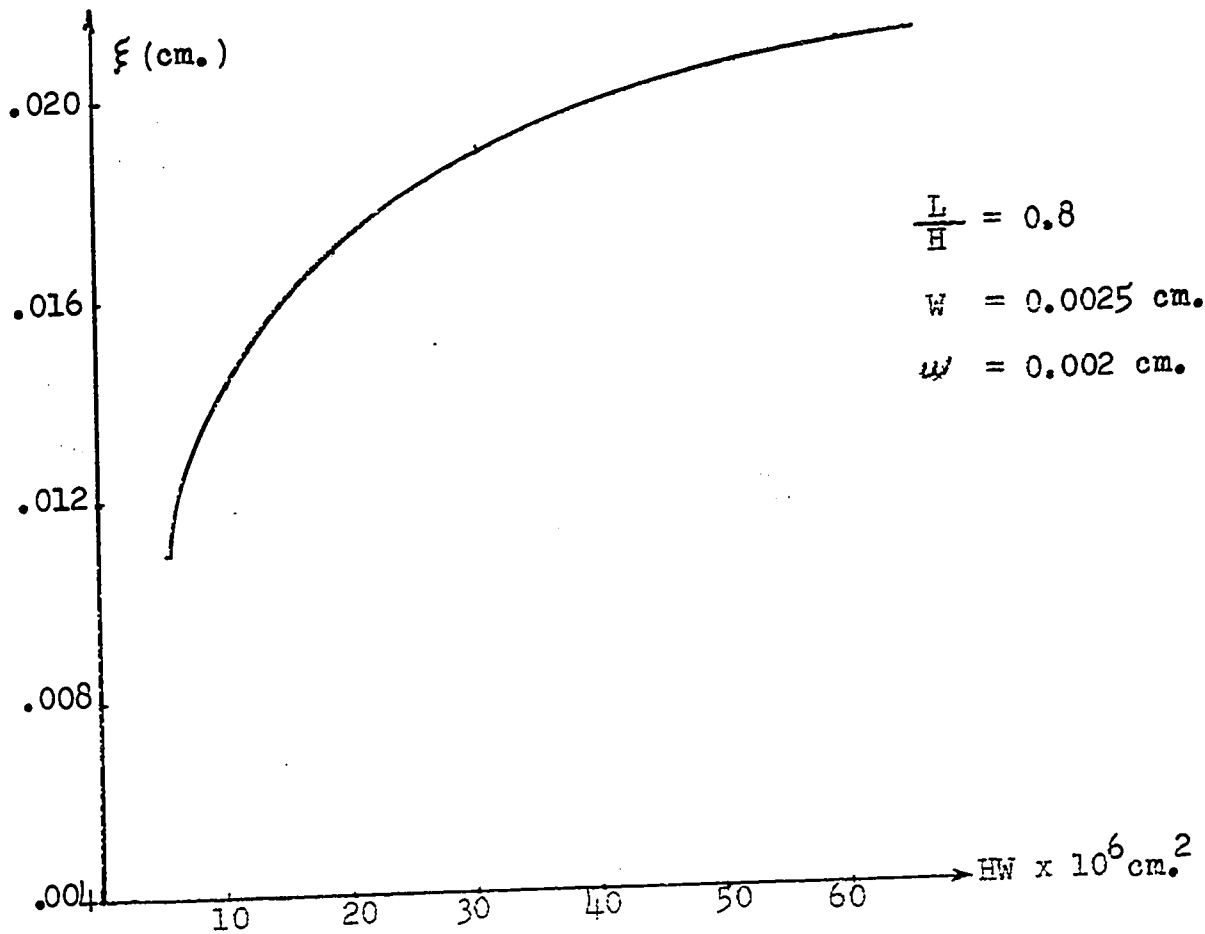
Graph 1 represents the case where the substrate length and width are equal. For this case, it can be seen that the maximum value of ξ and hence of power, within the assumptions made, is obtained for the $\frac{L}{H}$ ratio of 0.8. Moreover, the highest ξ value is obtained for a substrate area of $6.5 \times 10^{-6} \text{ cm}^2$, which is the case where the thin film element is 20μ square and the substrate is approximately 25μ square.







Graph 5. $H=9W$



Graph 6.

The remaining curves, Graphs 2 to 5, are similar plots in which the substrate length is taken as an integral number of substrate widths. These curves, again, show that as the $\frac{L}{H}$ ratio increases so also does the I.T.F. These curves further show that as the substrate length, and consequently the element length, increases, this factor and hence the amount of power which the element can safely dissipate increases at a faster rate. Taking Graph 5 as an example, one can see that the difference between the curves $P = 0.7$ and $P = 0.8$ is greater than that between $P = 0.6$ and $P = 0.7$ whereas in Graph 1 this difference is practically unnoticeable.

Now, if one were to consider the minimum size possible but taking also maximum power into account, one would be restricted to the case where $P = 0.8$. Graph 6 shows this case where the substrate and film widths have been fixed respectively at 25μ and 20μ . The Graphs 2 to 5 may be used to calculate the maximum power allowable for long elements (such as resistances). Graph 6 is especially suited for doing this because, for this case, the length ratio must be as large as possible. In other words, assuming a 20μ width for the resistor element and knowing the maximum power requirement, one can easily find the allowable length.

However, one notes that, as the length of the element increases, so also does the maximum allowable power. This suggests that the transistor, which has the lowest length ratio, will have the least allowable maximum power and hence this unit will be dealt with in more detail.

Taking typical transistor dimensions one would have the following results. Having assumed a minimum dimension of 20μ width and knowing that the emitter area of a transistor will occupy the least space, we take the emitter as being 20μ square. Using the ratio $\frac{L}{H} = 0.4$ we obtain a substrate length of 50μ . Thus the smallest transistor or diode unit possible using all the given assumptions is as shown in Fig. 5.

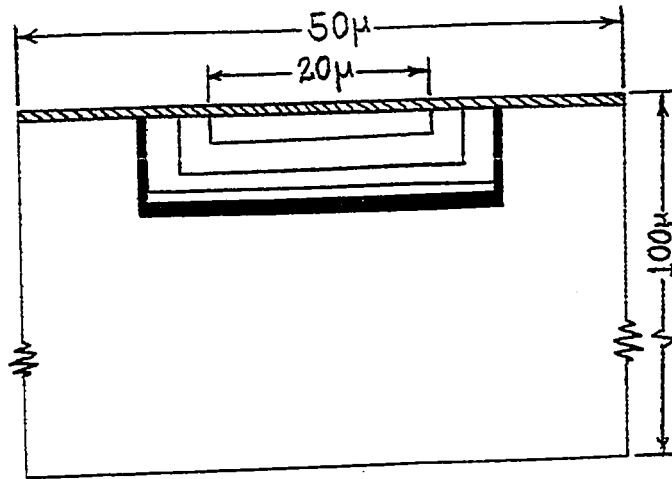


Fig. 5: Monolithic transistor under consideration.

From Graph 1, for these dimensions, the ξ value is

$$\xi = \frac{P}{\Delta T_c K} = 0.0039 \text{ cm.}$$

Using the usual value of K for silicon of $0.8 \text{ watts}/^{\circ}\text{C-cm.}$ and a maximum temperature rise of 10°C between element and substrate base, then the maximum allowable power for such a unit will be

$$\begin{aligned} P_M &= (.0039)(.8)(10) \\ &= 31 \text{ milliwatts.} \end{aligned}$$

This means that as long as we operate some circuit which uses resistors, transistors and diodes at such a power level so that the total power to any one transistor unit is less than this P_M figure, then there is no fear of thermal breakdown occurring. If this condition is applied, then one can find the density of components possible.

Assume that a typical resistor occupies four times the substrate area that a transistor or diode occupies and assume further that there are at most twice as many resistors as transistors or diodes combined. Then, from basic principles, the number of components per cm^3 is

$$\begin{aligned} \text{No. Components/cm}^3 &= \frac{1}{\left[\frac{\text{No. unit elements}}{\text{component}} \right] \left[\frac{\text{Volume}}{\text{unit}} \right]} \\ &= \frac{1}{(2 \times 4 + 1)(2t_s)(HW)} \end{aligned}$$

Twice t_s allows for the spacing between wafers, including the metal heat sink.

$$\begin{aligned} \text{No. components per cm}^3 &= \frac{1}{(18)(10^{-2})(50 \times 50 \times 10^{-8})} \\ &= 2 \times 10^5 \end{aligned}$$

If one were to consider existing cases where the heat dissipation of the case itself is limited to some maximum value P_c , then, on the average, each component cannot dissipate more than $(P_c/2 \times 10^5)$ watts of power. For example, existing flat packages enclosing microstructures have a $P_c = 500$ milliwatts, without using special cooling, and so

one can see that the average power per component for the example considered cannot be more than 2.5 microwatts. However, it should be noted that the limit is set by the outer case and not by the elements themselves.

Thus, it is seen that large packing densities are possible provided the average power per element is kept small (in the microwatt range) and provided the maximum power to any one element does not exceed that obtained from the graphs (for the case considered 31 milliwatts).

Moreover, since in most practical circuits only a small fraction of the transistors actually dissipate any significant power, then, if one were given an actual circuit with element power requirements, one could easily determine the minimum size of the units, from the given graphs, and hence the packing density.

Since it has been shown that the majority of the transistors must operate at low power levels, the transistor noise might become more pronounced. This will, therefore, be examined next in order to see what effects will noise power have at these low signal powers.

NOISE CONSIDERATIONS

In the following survey only the noise occurring in a transistor will be considered since resistor noise is similar to that occurring in the base resistance. It is felt that the noise found in a monolithic integrated transistor is similar to that found in a common junction transistor since both have similar type of p-n regions.

There are three known kinds of noise in these transistors: thermal noise, ~~shot~~ noise, and ~~Flicker~~ or $1/f$ noise, each of which will be separately considered. Once noise currents or voltages are determined, a total transistor noise figure (F) may be found and required the signal level established.

3.1: Thermal Noise

This type, first studied by Johnson [9] and mathematically defined by Nyquist [10], as early as 1928, is known to occur in any material that has a resistance and is at some finite absolute temperature. Its cause is believed to be due to the random thermal motion of electrons. Also, it has a flat frequency spectrum up to 3×10^{10} Hz.

For the transistor considered, the most important thermal noise source is the true base spreading resistance R_b . The noise power due to this resistance is independent

of the actual resistance value and is given by:

$$P_{nb} = kT p(f) \Delta f \quad (35)$$

where $p(f) = \frac{hf}{kT} \frac{1}{\left[\exp\left(\frac{hf}{kT}\right) - 1\right]} \approx 1$ for ordinary tempera-

tures and for frequencies up to 3×10^{10} Hz and where

h is Planck's constant

k is Boltzman's constant

T is the absolute temperature

Δf is the bandwidth or frequency range over which the transistor can be used.

The mean squared noise voltage, however, is given by:

$$\langle e_{nb}^2 \rangle = 4 kT R_b' \Delta f \quad (36)$$

Thus, using the generally accepted equivalent circuit for a transistor, one can place this thermal noise voltage in the base region as shown in Fig. 6.

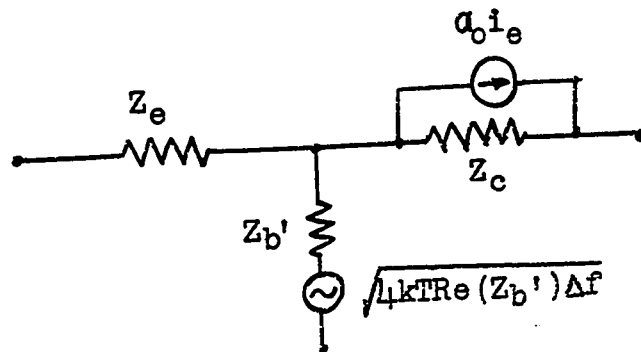


Fig. 6: Transistor equivalent circuit showing thermal noise voltage.

The real part of the impedance Z_b' for reasonably low frequencies, is the base spreading resistance R_b' but at high frequencies other factors must be included. This thermal noise voltage is actually due to the series resistances of the junctions which, at low frequencies, are lumped into one term R_b' .

3.2: Shot Noise

The approach used for this type of noise is similar to that used by Petritz [11] in 1952 and later used and modified by Van der Ziel [12] in 1958.

If the transistor is properly biased, the currents flowing across the junctions would have terms which would fluctuate at random. This random fluctuation or noise is believed to arise from the corpuscular nature of the current flow and from the fluctuations in concentration of the carriers and is, like thermal noise, independent of frequency at low frequencies.

Assuming the noise to arise from carrier density fluctuations, then the noise currents must be functions of the emitter and collector currents. Suppose that these currents are termed I_e and I_c respectively and consider the collector to be reverse biased (this is a natural assumption to make because the transistor is operated in this mode) so that there is no majority carrier injection from the collector into the base region, then the emitter current can be said

to be composed of $(I_e + \Delta I_e)$ and $(-\Delta I_e)$ where the first term is partly due to holes injected from the emitter into the base and partly to electrons injected from the base into the emitter and where the second term is similarly caused partly by holes flowing from the base into the emitter and partly by electrons flowing from the emitter into the base (for a p-n-p transistor).

Both of these currents fluctuate independently and each shows full shot noise. Thus, if the emitter noise is represented by a current generator i_{se} in parallel to the emitter junction, then

$$\langle i_{se}^2 \rangle = 2q (I_e + \Delta I_e) \Delta f + 2q \Delta I_e \Delta f \quad (37)$$

In the collector junction all holes move in the same average direction and so full shot noise would be expected for the current I_c only (hole current injected from the collector into the base is zero because of the existing bias conditions). Therefore, the shot noise due to this current can be represented by a current generator i_{sc} in parallel with the collector junction

$$\langle i_{sc}^2 \rangle = 2q I_c \Delta f \quad (38)$$

Thus, the transistor equivalent circuit showing both shot and thermal noise is shown in Fig. 7.

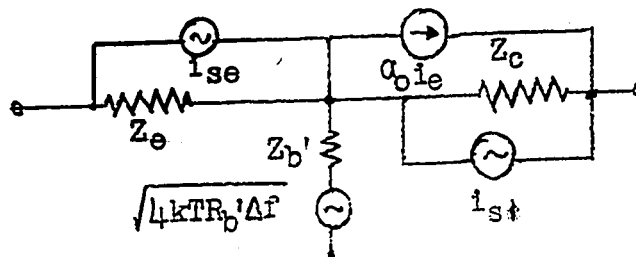


Fig. 7: Transistor equivalent circuit showing shot and thermal noise.

When considering shot noise there is a third factor that must be accounted for. This is a term due to the current common to both the emitter and the collector. Suppose that the part of the emitter current due to holes injected into the base by the emitter is given by

$$\gamma_0 (I_e + \Delta I_e) \quad (39)$$

where γ_0 is the d.c. emitter efficiency.

Suppose also that a part β_0 of these holes is collected by the collector, then the emitter and collector have in common a current

$$\gamma_0 \beta_0 (I_e + \Delta I_e) \quad (40)$$

and this shows full shot noise.

Next define, for convenience, the d.c. amplification factor of the transistor α_0 such that

$$\alpha_0 = \gamma_0 \beta_0 \quad (41)$$

Hence the total collector current may be written as:

$$I_c = \alpha_0 (I_e + \Delta I_e) + \Delta I_c \quad (42)$$

where ΔI_c is the current generated in the base region and collected by the collector.

Since (40) is common to both emitter and collector, then the cross-correlation $\langle i_{se} * i_{sc} \rangle$ is caused by fluctuation in this current which shows as shot noise.

$$\text{Thus } \langle i_{se} * i_{sc} \rangle = 2q \alpha_0 (I_e + \Delta I_e) \Delta f \quad (43)$$

Equation (42) can be placed in a more convenient form

$$I_c = (\alpha_o I_e + I_{co}) \quad (44)$$

where $I_{co} = (\alpha_o \Delta I_e + \Delta I_c)$ (45)

I_{co} is called the collector saturated current and is the collector current for open emitter.

Taking the approximate characteristic equation for junction diodes at low frequencies as representative also of the transistor junction

$$I = I_o \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \quad (46)$$

Then for the emitter junction

$$I_e = \Delta I_e \left[\exp\left(\frac{qV_e}{kT}\right) - 1 \right] \quad (47)$$

From (47) one can obtain the emitter admittance Y_e shown in Fig. 7, which at low frequencies is approximately equal to the conductance G_{eo}

$$\begin{aligned} Y_e &\doteq G_{eo} = \frac{\partial I_e}{\partial V_e} \\ &\doteq \frac{q}{kT} (I_e + \Delta I_e) \end{aligned} \quad (48)$$

Inserting (48) into (37) we get

$$\begin{aligned} \langle i_{se}^2 \rangle &= 4q\Delta f (I_e + \Delta I_e) - 2q I_e \Delta f \\ &= \left(\frac{4}{kT} G_{eo} \Delta f - 2q I_e \Delta f\right) \end{aligned} \quad (49)$$

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Since for the reverse biased collector junction $G_e \doteq 0$ then $\langle i_{sc}^2 \rangle$ remains unchanged. Furthermore, for this case

$$\begin{aligned} Y_{ce} &\doteq G_{eo} = \alpha_o G_{eo} \\ &\doteq \alpha_c \frac{q}{kT} (I_e + \Delta I_e) \end{aligned}$$

Hence, the cross-correlated noise current is given by

$$\langle i_{se} * i_{se} \rangle = 2kTY_{ce} \Delta f \quad (50)$$

3.3: Flicker Noise

According to Fonger [13], there are two types of flicker noise both so called because of their low frequency spectrum. These two types are denoted surface noise and leakage noise. Several authors have shown the dependence of the former type on environment. Maple, Bess and Gebbie [14] have shown this by changing the ambient temperature while Montgomery [15] showed changes in this surface noise by concentrating carriers on the surface by means of a magnetic field.

Although it is still uncertain what the actual mechanism of this noise is, it is generally accepted that it may be approximated by a current

$$\langle i_f^2 \rangle = \frac{\Gamma I^a}{f^b} \Delta f \quad (51)$$

where I is the d.c. current flowing through the material

Γ is a constant

$a \doteq 1$ for transistors

b may range from 1 to 1.6 for transistors

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It is also believed that $1/f$ noise may be caused by spontaneous fluctuations in the capture and release of carriers by "slow states" on the surface of the material. Fluctuations in the surface charge produced by these majority carriers influence the generation and recombination of electrons and holes at other states (fast states). Changes in both of these types modulate the conductivity of the bulk material, thus producing "surface noise".

Fluctuations caused by this random generation-recombination rate at the surface will modulate the series resistance of the junctions which are strongly current dependent and thus the flow of a direct current will cause this noise at both junctions. Van der Ziel [12] has given an equivalent circuit for flicker noise - this is given by

Fig. 8.

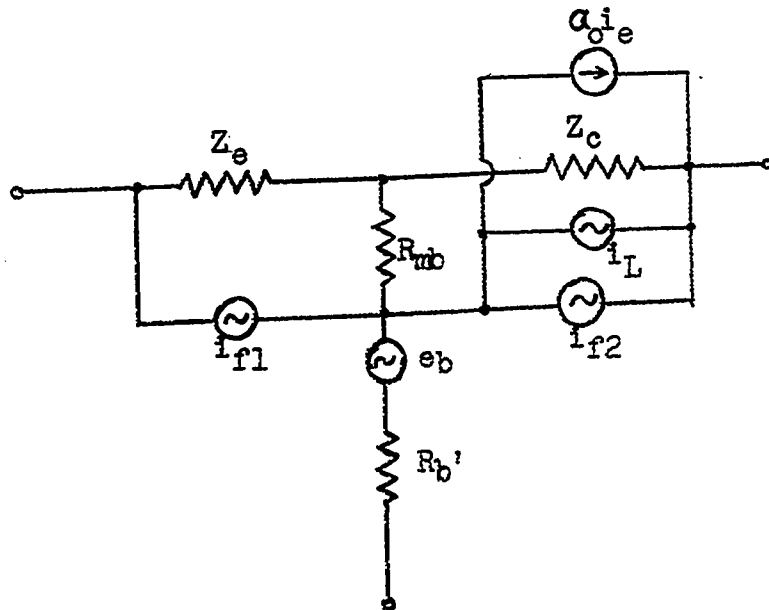


Fig. 8: Flicker noise transistor equivalent circuit.

Fonger [13] also found that the effect of the noise e.m.f. e_b was quite small and may usually be neglected. The reason for this e.m.f. was to account for the fact that the d.c. base resistance R_b' is also modulated by flicker noise.

Leakage noise has been found to be strongly dependent, as mentioned, on the surface condition of the material and, since it increases with increasing bias, it is important only in the reversed bias collector junction. However, proper surface treatment reduces this noise to such an extent that it becomes negligible for $|V_c| < 10$ volts.

For ease of computations, Van der Ziel [12] has reduced the circuit of Fig. 8 to that of Fig. 9.

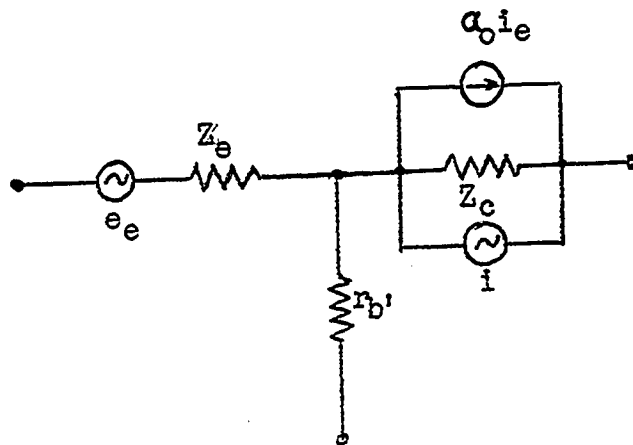


Fig. 9: Modified flicker noise equivalent circuit.

Where the generators in Fig. 8 have been replaced by

$$i = (i_{f2} + \alpha_0 i_{f1} + i_L) \quad (52)$$

$$e_e = -i_{f1} (R_{e0} + R_{mb}) - e_b \quad (53)$$

Chenette [16] has shown that these two quantities are fully correlated as predicted by Fonger's theory, thus showing that i_L can be neglected. Since it has also been stated that e_b is negligible, then equations (52) and (53) become

$$i = (i_{f2} + \alpha_0 i_{f1}) \quad (54)$$

$$e_e = -i_{f1} (R_{e0} + R_{mb}) \quad (55)$$

Equation (54) merely states the fact that flicker noise generated at the surface flows from the base surface towards both junctions and so the current generator 'i' is the sum shown.

In equations (53) and (55) the low frequency value of Z_{mb} has been taken as R_{mb}

$$R_{mb} = I_b \frac{\partial R_{b'}}{\partial I_b} \quad (56)$$

and also

$$R_{e0} = \frac{kT}{qI_e} \quad (57)$$

3.4: Transistor Noise Figure

As it is more convenient to work with the noise figure F rather than with the noise voltages and currents, we will obtain the total noise figure of the transistor and use this to obtain the minimum signal power that may be required.

The latter is given by

$$P_s(\min) = FkT\Delta f \quad (58)$$

where Δf is the bandwidth of the transistor and where F is

$$F \triangleq \frac{\text{Total Mean Square noise voltage at output of transistor}}{\text{Mean square noise voltage at output due to source resistance}}$$

To obtain the total noise figure, however, we may use the fact that it is the sum of the noise figures due to the different types of noise

$$\text{Thus } F = F_{SH} + F_{FL}$$

Where F_{FL} is the noise figure due to flicker noise and where F_{SH} is the noise figure due to shot noise including the base thermal noise.

Furthermore, since we must include a source in the transistor circuit for the method to be used, we must decide on the transistor circuit configuration. However, it is known that the common base and the common emitter circuits both give identical noise figures [12], thus either one of these is suitable.

A common method of obtaining the noise figure is to refer all noise sources to the input, so that the noise figure F is then

$$F = \frac{\langle e_n^2 \rangle}{\langle e_{ns}^2 \rangle}$$

(59)

where $\langle e_n^2 \rangle$ is the total mean square noise voltage of all noise sources referred to the input and where $\langle e_{ns}^2 \rangle$ is the noise voltage due to the source resistance

$$\langle e_{ns}^2 \rangle = 4kT R_s \Delta f$$

Guggenbuehl and Strutt [17] have calculated the noise figure for thermal and shot noise in a junction transistor as

$$F_{SH} = \frac{2qI_c}{|\alpha|^2 4kTR_s} \left[(r_{b'} + Z_e + Z_s)^2 \right] - \frac{2qI_e}{4kTR_s} \left[(r_{b'} + Z_s)^2 \right]$$

$$= \frac{q}{2kTR_s} \left[\frac{I_c}{|\alpha|^2} (R_s + r_{b'} + R_{e0})^2 - I_e (R_s + r_{b'})^2 \right] \quad (60)$$

for the low frequency case.

This expression is similar to that given by Van der Ziel [12] and it is of importance because it expresses shot noise figure in terms of macroscopic parameters. Hanson and Van der Ziel [18] have obtained somewhat similar results; however, they have used the noise current and voltage expressions. Since these two sources are correlated, see Section 3.2, the noise voltage e is separated into a fully correlated noise voltage e'' and a fully uncorrelated part e' . In so doing they have obtained the following expression:

$$F_{SH} = 1 + \frac{r_{b'} + R_{s1}}{R_s} + \frac{g_{s1}}{R_s} \left[Z_s + Z_e + Z_{b'} + Z_{sc} \right]^2 \quad (61)$$

where the terms have been defined as follows:

$$g_{s1} = \frac{\langle i_{s1}^2 \rangle}{|\alpha|^2 4kT\Delta f} \quad \text{the noise conductance.}$$

$$R_{s1} = \frac{\langle e''^2 \rangle}{4kT\Delta f} \quad \text{the noise resistance.}$$

$$Z_{sc} = -|\alpha| \frac{e'}{i_{sl}} \quad \text{the correlation impedance.}$$

Nielsen [19] has neglected the correlation between e and i_{sl} (i.e. $Z_{sc} = 0$) and assumes $R_{sl} = \frac{1}{2} R_{e0}$ at all frequencies. Thus, he obtains

$$F_{SH} = 1 + \frac{r_{b'} + \frac{1}{2} R_{e0}}{R_s} + \frac{g_{sl}}{R_s} \left| Z_s + Z_e + r_{b'} \right|^2 \quad (62)$$

Using (62) he found reasonable agreement between theory and experiment. Taking the value given by Van der Ziel for the noise current, g_{sl} may be written as

$$g_{sl} = \frac{q}{2kT} \left[\frac{(\alpha_0 - |\alpha|^2) I_e + I_{c0}}{|\alpha|^2} \right] \quad (63)$$

where $\alpha = \frac{\alpha_0}{(1 + jf/f_0)}$ f_0 being the α cut-off frequency.

Now obtaining the noise figure for flicker noise the same procedure of referring all noise to the input is used and so the noise figure is given by

$$F_{FL} = \frac{\langle e_{nf}^2 \rangle}{4kTR_s \Delta f} = \frac{R_{nf}}{R_s}$$

where R_{nf} is the equivalent flicker noise resistance to account for the flicker noise. The noise voltage e_{nf} can be shown to be [12]

$$e_{nf} = e_e + \frac{i}{\alpha_0} (R_s + R_{e0} + r_{b'}) \quad (64)$$

where all terms have already been defined in Section 3.3.

Using the usual Nyquist relation we find that

$$R_{nf} = \frac{\langle i^2 \rangle}{4kT\alpha_o^2 \Delta f} \left[(R_s + R_{eo} + r_{b'}) + \frac{\alpha_o e_e}{i} \right]^2 \quad (65)$$

$$\text{Thus } F_{FL} = \frac{\langle i^2 \rangle}{4kTR_s \alpha_o^2 \Delta f} \left[R_s + R_{eo} + r_{b'} + R_{fc} \right]^2 \quad (66)$$

where $R_{fc} = \frac{\alpha_o e_e}{i}$ is the correlation term

$$g_{fl} = \frac{\langle i^2 \rangle}{4kT\alpha_o^2 \Delta f}$$

Thus the total noise figure for the transistor is, combining equations (62) and (66), for the low frequency case

$$\begin{aligned} F &= 1 + \frac{r_{b'} + \frac{1}{2} R_{eo}}{R_s} + \frac{g_{sl}}{R_s} \left[R_s + R_{eo} + r_{b'} \right]^2 + \\ &\quad + \frac{g_{fl}}{R_s} \left[R_s + R_{eo} + r_{b'} + R_{fc} \right]^2 \\ &= \frac{1}{R_s} \left[R_s + r_{b'} + \frac{1}{2} R_{eo} + g_{sl} (R_s + R_{eo} + r_{b'})^2 + \right. \\ &\quad \left. + g_{fl} (R_s + R_{eo} + r_{b'} + R_{fc})^2 \right] \quad (67) \end{aligned}$$

Equation (67) can be also written as

$$\begin{aligned} F &= \left[1 + 2(g_{sl} + g_{fl})(r_{b'} + R_{eo}) + 2g_{fl}R_{fc} \right] + R_s(g_{sl} + g_{fl}) + \\ &\quad + \frac{1}{R_s} \left[r_{b'} + \frac{1}{2} R_{eo} + g_{fl}(r_{b'} + R_{eo})^2 + g_{fl}(r_{b'} + R_{eo} + R_{fc})^2 \right] \\ &= A + B R_s + \frac{C}{R_s} \quad (67a) \end{aligned}$$

If one were to plot this noise figure as a function of R_s one should obtain a curve as shown in Fig. 9:

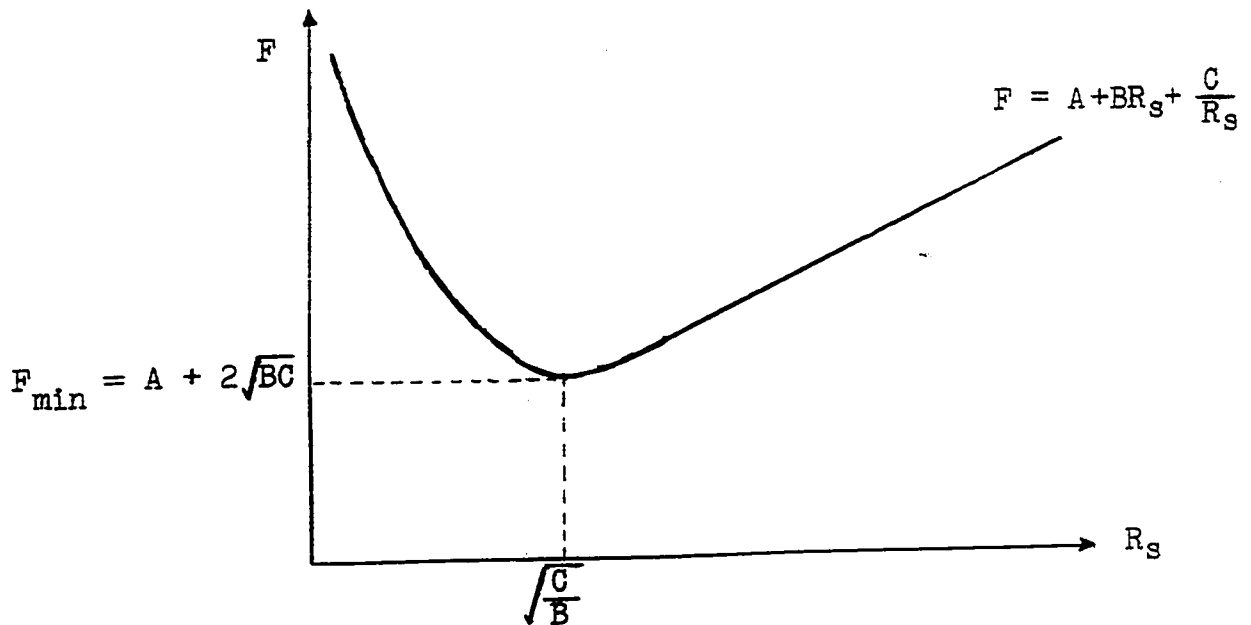


Fig. 9: Curve showing variation of total noise figure with source resistance at low frequency.

Differentiating (67) with respect to R_s and equating the results to zero, we can get a value of R_s for which the noise figure will be a minimum. This value can easily be shown to be:

$$R_s(\text{opt.}) = \sqrt{\frac{r_{b'} + \frac{1}{2} R_{e0} + g_{f1} (r_{b'} + R_{e0} + R_{fc})^2}{(g_{f1} + g_{s1})} + (r_{b'} + R_{e0})^2} \quad (68)$$

Thus the minimum value of the noise figure F at optimum source resistance is

$$F_{\min} = \left[1 + 2 (g_{s1} + g_{f1}) (r_{b1} + R_{e0}) + 2 g_{f1} R_{fc} \right] + \frac{+ 2 \sqrt{(g_{s1} + g_{f1}) \left[r_{b1} + \frac{1}{2} R_{e0} + g_{s1} (r_{b1} + R_{e0})^2 \right] + g_{f1} (r_{b1} + R_{e0} + R_{fc})^2}}{+ g_{f1} (r_{b1} + R_{e0} + R_{fc})^2} \quad (69)$$

where we already have the following relations:

$$1) \quad g_{s1} = \frac{q}{2kT} \frac{(\alpha_0 - |\alpha|^2) I_e + I_{c0}}{|\alpha|^2} \quad (63)$$

$$2) \quad g_{f1} \doteq \frac{\langle i^2 \rangle}{4kT \alpha_0^2 \Delta f} \doteq \frac{\Gamma}{4kT \alpha_0^2 f} I_e \quad (70)$$

$$3) \quad R_{e0} \doteq \frac{kT}{qI_e} \quad (71)$$

From measurements done by Chenette [16] as suggested by Van der Ziel [12] we note that

$$R_{s0} = - (R_{e0} + r_{b1} + R_{fc})$$

where R_{s0} is the point at which the flicker noise resistance is zero. In Chenette's paper one further notes that this resistance decreases in absolute value as the current decreases. Thus for the purpose of this discussion assume $R_{s0} = 0$ for the currents at which we are working.

$$\text{Thus } R_{fc} \doteq (R_{eo} + r_{b'}) \quad (72)$$

Introducing equations (63), (70), (71) and (72) into (69) we get the following:

$$\begin{aligned} F_{\min} &\doteq 1 + 2g_{sl}(r_{b'} + R_{eo}) + 2\sqrt{(g_{sl} + g_{fl}) \left[r_{b'} + \frac{1}{2}R_{eo} + g_{sl}(r_{b'} + R_{eo})^2 \right]} \\ &\doteq 1 + q \frac{r_{b'}}{kT} \left[\frac{(\alpha_0 - |\alpha|^2)I_e + I_{co}}{|\alpha|^2} \right] + \frac{\alpha_0 - |\alpha|^2}{|\alpha|^2} + \frac{I_{co}}{|\alpha|^2 I_e} + \\ &\quad + 2\sqrt{\frac{qI_e}{kT} \left[\frac{\alpha_0 - |\alpha|^2}{|\alpha|^2} + \frac{I_{co}}{|\alpha|^2 I_e} + \frac{\Gamma}{2q\alpha_0^2 f} \right] \left[r_{b'} + \frac{kT}{qI_e} + \right.} \\ &\quad \left. + \frac{qI_e}{2kT} \left(\frac{\alpha_0 - |\alpha|^2}{|\alpha|^2} + \frac{I_{co}}{|\alpha|^2 I_e} \right) \left(r_{b'} + \frac{kT}{qI_e} \right)^2 \right]} \quad (73) \end{aligned}$$

$$\text{However, } |\alpha|^2 = \frac{\alpha_0^2}{1 + (f/f_0)^2} \doteq \alpha_0^2 \quad \text{if } f \ll f_0$$

This approximation holds since we have already assumed the low frequency case and since f_0 , the α cut-off frequency may be usually as high as 100 MHz.

Hence we have that:

$$\begin{aligned} F_{\min} &\doteq 1 + \frac{qI_e r_{b'}}{kT} \left[\frac{1 - \alpha_0}{\alpha_0} + \frac{I_{co}}{\alpha_0^2 I_e} \right] + \left[\frac{1 - \alpha_0}{\alpha_0} + \frac{I_{co}}{\alpha_0^2 I_e} + 2\sqrt{\frac{qI_e}{2kT} \left(\frac{1 - \alpha_0}{\alpha_0} + \right.} \right. \\ &\quad \left. \left. + \frac{I_{co}}{\alpha_0^2 I_e} + \frac{\Gamma}{2q\alpha_0^2 f} \right) \left[r_{b'} + \frac{kT}{qI_e} + \frac{qI_e}{2kT} \left(\frac{1 - \alpha_0}{\alpha_0} + \frac{I_{co}}{\alpha_0^2 I_e} \right) \left(r_{b'} + \frac{kT}{qI_e} \right)^2 \right]} \end{aligned}$$

$$\begin{aligned} \cong 1 + \left[\frac{1-\alpha_0}{\alpha_0} + \frac{I_{co}}{\alpha_0^2 I_e} \right] \left[1 + \frac{q r_{b'} I_e}{kT} \right] + 2 \sqrt{\left(\frac{1-\alpha_0}{\alpha_0} + \frac{I_{co}}{\alpha_0^2 I_e} + \frac{\Gamma}{2q f \alpha_0^2} \right)} \left[\frac{1}{2} + \right. \\ \left. + \frac{q I_e r_{b'}}{kT} + \frac{1}{2} \left(\frac{1-\alpha_0}{\alpha_0} + \frac{I_{co}}{\alpha_0^2 I_e} \right) \left(1 + \frac{q I_e r_{b'}}{kT} \right)^2 \right] \end{aligned} \quad (74)$$

From equation (74) we can see the following:

1) The minimum noise figure is dependent on the emitter current (if one does not take into consideration the fact that the d.c. amplification factor α_0 decreases with decreasing current for silicon).

2) The d.c. amplification factor of the transistor α_0 must be made as close to unity as possible for any emitter current range chosen.

3) The leakage current I_{co} must be made negligible compared to the emitter current ($I_e \gg I_{co}$).

If these three conditions are satisfied, then the noise figure will be minimum as well as the signal power required.

A further factor which has been pointed out by both Nielsen [19] and Van der Ziel [12] and which is also pointed out by equation (74) is that, as the emitter current is decreased, the noise factor also decreases (assuming α_0 to be independent of current). However, this is true only provided the leakage to emitter currents ratio is constant which is usually the case.

Since we have considered the low frequency case we note also from (74) that as the frequency decreases the noise factor increases. This has been found also experimentally by several authors some of whom have concluded that the frequency at which the $(1/f)$ term is negligible is 10KHz while others have taken this frequency at 1KHz.

Since the whole purpose of this noise discussion was to obtain some actual typical noise figure value for use in obtaining a minimum signal power level, we can therefore, assume some typical values for the constants involved.

$$\text{Assume } \alpha_o \doteq 0.98, \frac{I_{co}}{\alpha_o^2 I_e} \doteq .001, r_{b'} \doteq 100 \text{ ohms.}$$

also assume the flicker factor to be negligible at $f = 10\text{KHz}$.

$$\text{say } \frac{\Gamma}{2qf\alpha_o^2} \doteq 0.001 \text{ at } f = 10\text{KHz}$$

$$\begin{aligned} \text{from which } \Gamma &\doteq (10^{-3})(10^4)(.96 \times 2 \times 1.6 \times 10^{-19}) \\ &\doteq (20q\alpha_o^2) \end{aligned}$$

Substituting these values into (74) we get

$$F_{\min.} \doteq 1 + .0214(1 + 3.86 \times 10^3 I_e) + 2 \sqrt{(.0214 + \frac{10}{f}) \left[.50 + 3.86 \times 10^3 I_e + .0107(1 + 3.86 \times 10^3 I_e)^2 \right]}$$

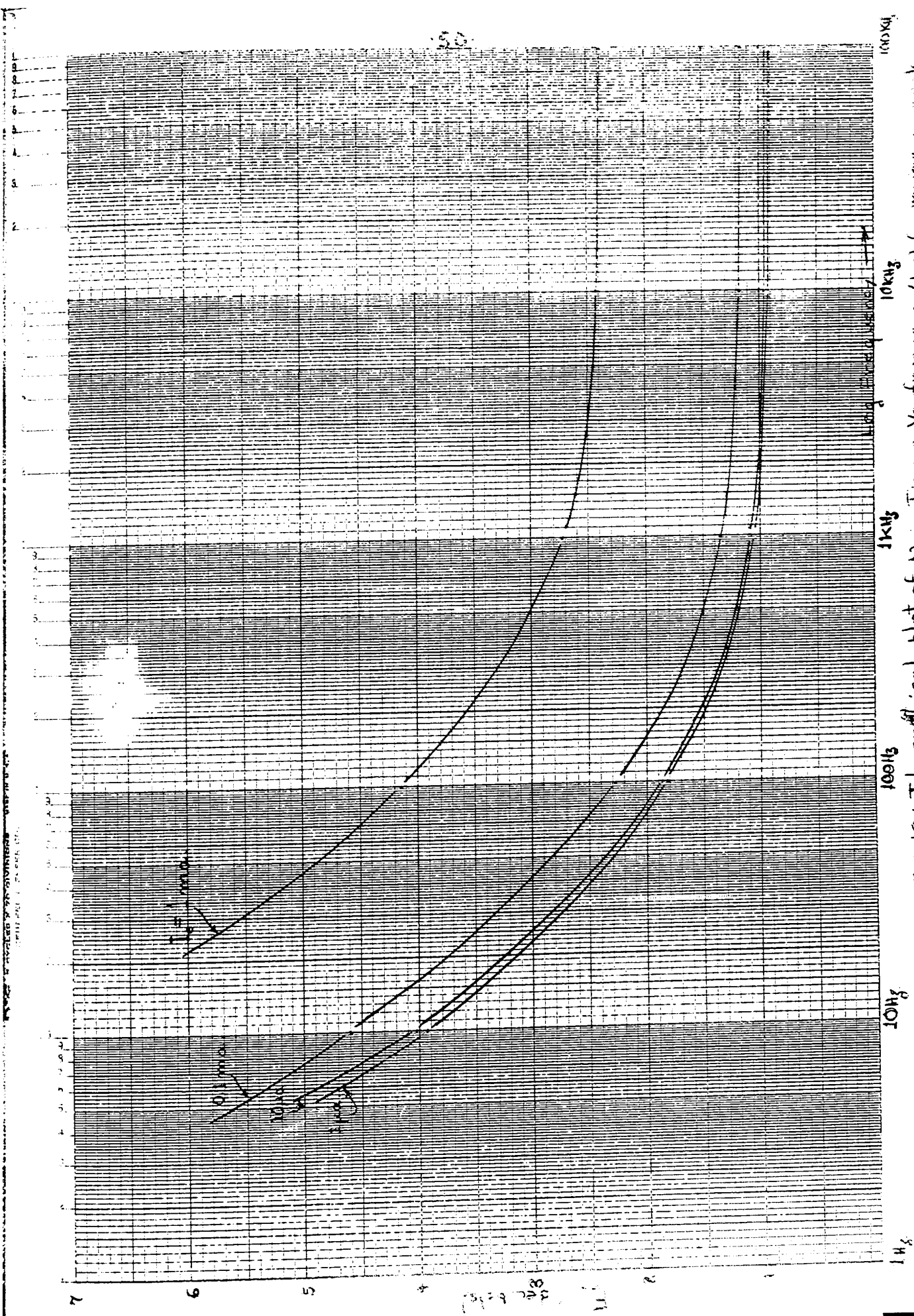


FIG. 10. Theoretical plot of Noise Figure Vs. frequency (log) for various noise powers.

From this equation, one can see more clearly the current dependence of the noise figure. Fig. 10 shows clearly both the current and frequency dependence of this theoretical minimum noise figure value.

For comparison purposes, we include an experimental curve [20] of noise figure plotted against log frequency for a silicon planar transistor amplifier (Fig. 11). Although no data is available as to the emitter current and source resistance used, comparison of these two curves shows quite reasonable agreement.

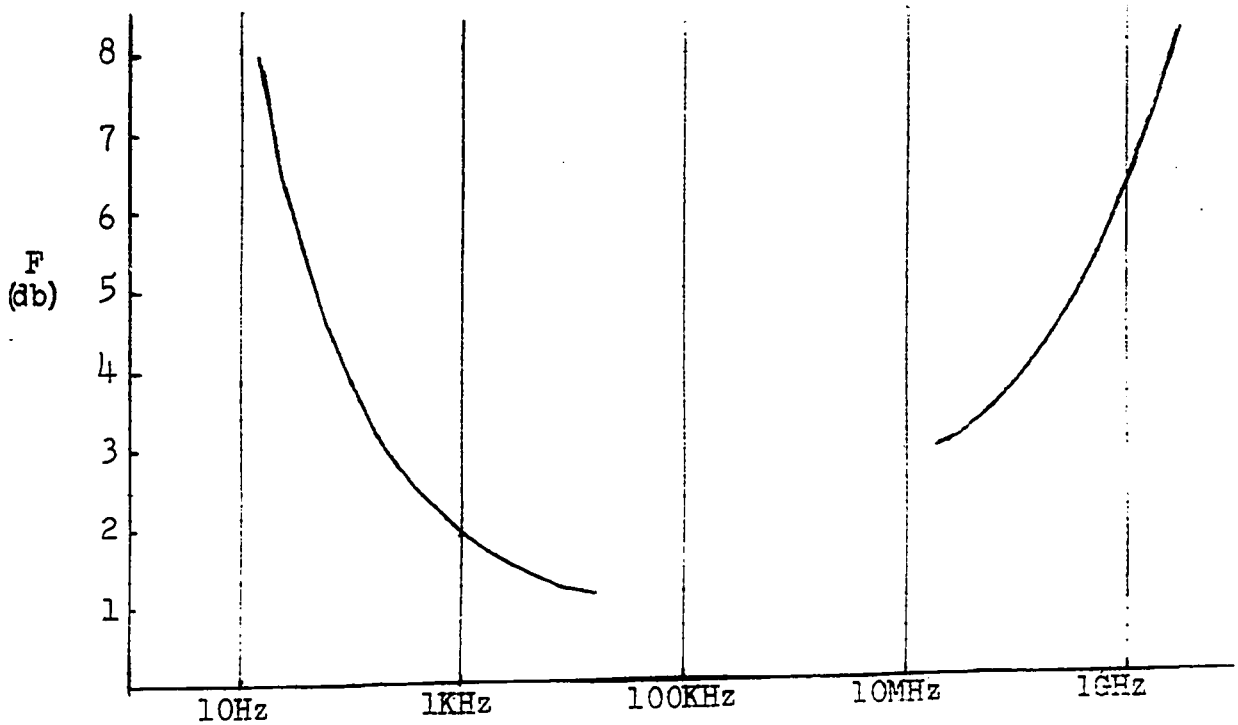


Fig. 11: Semiconductor noise figure for a silicon planar transistor amplifier.

The discrepancy between the theory and experiment would seem to come from the type of function assumed for flicker noise. It should be recalled that this function was of the form $\phi(\frac{1}{fb})$ where the constant 'b' varied in value from 1 to 1.6 and so it could be shown that if a value of $b > 1$ had been used in our theory, the curve obtained would have been quite similar to the experimental curve of Fig. 11.

A further factor shown by the curves in Fig. 10 is that the effect of the emitter current on the noise figure decreases with decreasing current. Thus it appears that in the microampere range, the noise figure remains reasonably constant even though the emitter current might change. Nielsen [19] has experimentally obtained similar results; however, his results were obtained for currents in the milliampere range where the minimum noise figure became somewhat constant at about 0.5 ma. He further stated that the noise figure was experimentally found to increase with further decrease in current but this was probably caused by a decreasing of the alpha of the transistor (whereas in our theory we have assumed this factor to be constant even in the microampere range).

Thus considering the theoretical noise figure curves in the microampere range shown in Fig. 10, we can take a reasonable noise figure value of $F_{min.} \doteq 4\text{db}$ for a 100 MHz bandwidth.

Then, using equation (58), we find that the minimum signal power required is

$$\begin{aligned} P_s(\text{min.}) &\approx 2.5 (kT) \Delta f \\ &\approx (1.04 \times 10^{-19}) \Delta f \text{ at room temperature} \\ &\approx 10.4 \text{ picowatts} \end{aligned}$$

Assuming a power gain for the common emitter configuration of approximately 10^4 , then the minimum output signal power possible is

$$P_{s0}(\text{min.}) \approx 104 \text{ nanowatts}$$

We have thus obtained a minimum power limit necessary to overcome the noise power introduced by both the source and transistor itself. This numerical limit shows that one cannot reduce power indefinitely in order to reduce circuit size, rather, the inherent noise of the elements constitutes the lower limit.

In general, if we were to plot the signal power variation as a function of the transistor bandwidth at constant temperature we would obviously obtain a straight line.

$$P_s(\text{min.}) \approx (1.04 \times 10^{-19}) \Delta f \quad (76)$$

This result is to be expected, since as the transistor bandwidth is improved, the noise power increases and hence to overcome this increase, the signal power must also increase.

CONCLUSIONS

In this discussion, a power range, over which a transistor of silicon monolithic integrated type may function, has been found. The lower limit is given by the minimum signal power required to overcome the noise which is characteristic of any transistor while the upper limit is given by the maximum power which a unit can withstand.

The lower limit is directly proportional to the transistor bandwidth, thus, for example, the least signal power output necessary, for a 100 MHz bandwidth, to overcome the total noise power introduced by both the source and the transistor is approximately 100 nanowatts. Of course, it can be seen from equation (76) that if a smaller bandwidth is used, say 1 MHz, then the output signal power decreases to 1 nanowatt. This lower limit shows that if we could decrease element size indefinitely (ideal technology) we would not be able to decrease the size of the unit beyond such point that it cannot handle this minimum signal power over some given bandwidth.

From a technological point of view, working in this very low power range is impractical, since the size decrease would require resistances in the Megohm range and these are known to occupy extremely large areas, as compared to the transistors or diodes. Thus, by decreasing the power level we would be increasing the area required to place the components.

As an example for obtaining a minimum practical dimension let us consider a transistor in a common emitter configuration (See Fig. 12).

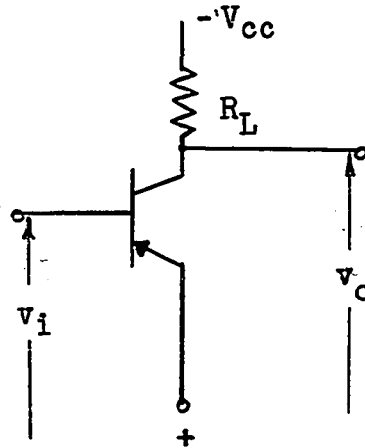


Fig. 12: Transistor in C.E. Configuration

Assuming a one volt supply voltage and one nanowatt output power, it can be shown that the minimum current flowing is one nanoampere and the load resistor must be 500 Mohms. Thus, the minimum current that the transistor emitter must be capable of handling and still give reasonably good transistor action is 1 na. Using this fact, we could find the transistor dimension required.

From the power dissipation viewpoint, interpolating the Graph 1, the point of minimum size for a 1 nanowatt power level will be extremely small, in the angstrom range. Thus, obviously, other factors would need to be considered since dissipation of this minimum power could be easily accomplished with transistor units of any practical dimensions.

Going to the upper power limit obtained, we have found that very small units can dissipate quite large powers, provided the restrictions imposed by the previous discussion on power are obeyed. For instance, we have found that, theoretically, a 50μ square unit having a 20μ square emitter can dissipate a maximum of approximately 30 milliwatts. Such a unit would also be needed to have a maximum emitter current rating of approximately 10 ma. at which point the transistor β begins to fall off rapidly. (This current rating is dictated by the emitter dimensions for a practical semiconductor device. See Appendix "B")

As can be seen, therefore, the power capable of being dissipated by a single transistor unit is quite large with the result that the upper limit is set by the maximum dissipation of the outside case. However, if we have several amplifying stages on a single substrate, then most of the power will be dissipated by a few elements on the output side of the circuit, and so these units will be limited in size by this maximum power figure obtained.

As has been mentioned, the upper limit seems to be set more by the outside package, since it is the latter which is incapable of handling more than a finite amount without special cooling. Present technology has set this limit at 680 milliwatts for a TO-5 package and 500 milliwatts for a flat package. Having assumed this limiting power level, it has been found that a density of approximately 2×10^5 components/cm.³ could be achieved provided the average power dissipation

per component does not exceed some fixed value dependent on the dissipation capability of the outside casing (in this case 2.5 microwatts per element).

This density is obviously not too far from reality, since the Motorola commercial monolithic operational amplifier, the MCL433, has already a volume density of approximately 10^4 . As the technology approaches closer to the dimensions assumed, then there will be no reason why the above density of 2×10^5 components/cm.³ could not be approached. To go a step further, if technology improves beyond that assumed in this study, then densities of the order of 10^6 comp./cm.³ should be possible, provided the maximum power dissipated by any one component does not exceed that obtained from the given curves and provided the minimum signal power is above the noise power introduced by both the circuit and the source for any given bandwidth.

A further factor which would have to be considered when using the minimum power concept is that of speed. Even reducing parasitic capacitances, the speed at which circuit function is directly proportional to the power. Thus, if the signal power is decreased, the speed of computation also decreases. So if speed is important in some circumstances, then the minimum power range will be dictated by this rather than by the noise, as given above.

Some factors which have not been included in this discussion are the increase in surface noise with decrease in size of the unit and the variation in the transistor " α " with decreasing emitter currents for silicon. The latter could perhaps suggest using some other material (gallium arsenide seems to hold some promise). These could be problems for further study.

To summarize, then, it has been shown that noise power and power dissipation are limiting factors to component size in so far as they give a power range over which a transistor unit of given dimensions can probably function. However, there are so many technological factors that must be overcome at present that technology seems to be the major limiting factor to component size.

APPENDIX "A"

To obtain the single summation expression of (32) one must find the limit of the expression first as $n \rightarrow 1$ and then as $m \rightarrow 1$:

$$\begin{aligned}
 & \lim_{n \rightarrow 1} \sum_{m=2}^{\infty} \frac{4 \sin \frac{\alpha L}{2} \sin \frac{\beta \omega}{2} \sinh q_{mn} t}{\pi^2 q_{mn} (n-1)(m-1) \cosh q_{mn} t_s} = \\
 & = \sum_{m=2}^{\infty} \lim_{n \rightarrow 1} \frac{4 \sin \frac{\beta \omega}{2} \left[\frac{\pi L}{H} \sinh q_{mn} t \cos \frac{\alpha L}{2} + \sin \frac{\alpha L}{2} \frac{d}{dn} \sinh q_{mn} t \right]}{\pi^2 (m-1) q_{mn} \cosh q_{mn} t_s + (n-1) \cosh q_{mn} t_s \frac{d}{dn} q_{mn} + (n-1) q_{mn} \frac{d}{dn} \cosh q_{mn} t_s} \\
 & = \sum_{m=2}^{\infty} \left(\frac{4 \sin \frac{\beta \omega}{2}}{\pi^2 (m-1)} \right) \frac{\frac{L}{H} \sinh \frac{2\pi(m-1)}{W} t_s}{2\pi \frac{(m-1)}{W} \cosh 2\pi \frac{(m-1)}{W} t_s} \\
 & = \frac{2LW}{\pi^2 H} \sum_{m=2}^{\infty} \frac{\sin \frac{\beta \omega}{2} \sinh \beta_m t_s}{(m-1)^2 \cosh \beta_m t_s} \tag{A.1.1}
 \end{aligned}$$

Similarly, as $m \rightarrow 1$ the limit of the expression is

$$\frac{2HW}{\pi^2 W} \sum_{n=2}^{\infty} \frac{\sin \frac{\alpha L}{2} \sinh \alpha_n t_s}{(n-1)^2 \cosh \alpha_n t_s} \tag{A.1.2}$$

APPENDIX "B"

Some typical properties which the 50 μ square transistor unit considered might have are as follows:

Assume a 0.5 ohm-cm. gold-doped transistor

Physical Properties:

Emitter area - 20 μ square

Substrate area per unit - 50 μ square

Base Thickness - 0.7 μ

Emitter Thickness - 2 μ

Electrical Properties:

Assume transistor $\beta \approx 50$

We also have that [21]

$$\frac{1}{\beta} = \frac{\rho_e t_b}{\rho_b L_{pe}} \left(1 + \frac{I_e t_b}{2qD_{nb} A_e N_{b'}} \right) + \frac{t_b^2}{4L_{nb}^2} + \frac{SA_s t_b}{2A_e D_{nb}} + \frac{\Delta I_e}{I_e}$$

Where each term of this equation has the following meaning:

The second term is related to base transport and is close to zero for most designs. The third term accounts for surface recombination effects. The last term is the factor which accounts for emitter leakage current. We can thus neglect the second and last term but the third term must be accounted for at lower currents. Its value can at best be only approximated since the surface recombination velocity "S" cannot be measured exactly.

From the above expression we can obtain the current rating or capability of the device which, by definition, has been taken as the point at which

$$\frac{I_{e b} t}{2qD_{nb} A N_{b'}} = 0.1$$

Using typical values

$D_{nb} \doteq 12 \text{ cm}^2/\text{sec}$ is the base diffusion constant which has been calculated for a carrier mobility of $450 \text{ cm}^2/\text{volt-sec}$.

$A_e \doteq 4 \times 10^{-6} \text{ cm}^2$ is the emitter area

$N_{b'} \doteq 5 \times 10^{17} \text{ atoms/cm}^3$ is the impurity concentration at the emitter-base interface.

$$\text{Thus } I_e \doteq \frac{0.2(1.6 \times 10^{-19})(12)(4 \times 10^{-6})(5 \times 10^{17})}{(p.7 \times 10^{-4})}$$

$$\doteq 11 \text{ ma.}$$

From Fig. 2.20 in reference [21], the breakdown collector base voltage $BV_{cbo} \doteq 14$ volts.

Thus the breakdown collector to emitter voltage BV_{ceo} is

$$BV_{ceo} = BV_{cbo} (1 - \alpha)^{1/n}$$

Where n varies from 2 to 4 for silicon transistors. ($n = 3$)

$$BV_{ceo} \doteq \frac{BV_{cbo}}{\sqrt[3]{\beta}} = \frac{14}{\sqrt[3]{50}} = 3.8 \text{ volts}$$

APPENDIX "C"

A.2.1: List of Factors Used in the Program

$$C = \frac{0.44(FN-1)}{7RW} \quad (A.2.1)$$

$$U1 = U1 + \frac{\sin \frac{22P(FN-1)}{7}}{(FN-1)^2} \tanh C \quad (A.2.2)$$

$$U1 = U1 + \frac{\sin \frac{22P(FN-1)}{7}}{(FN-1)^2} \quad (A.2.3)$$

$$U = \frac{49U1}{242PW} \quad (A.2.4)$$

$$B = \frac{0.44(FM-1)}{7W} \quad (A.2.5)$$

$$T1 = T1 + \frac{\sin \frac{0.44(FM-1)}{7W}}{(FM-1)^2} \tanh B \quad (A.2.6)$$

$$T1 = T1 + \frac{\sin \frac{0.44(FM-1)}{7W}}{(FM-1)^2} \quad (A.2.7)$$

$$T = T1 \frac{12250}{121R} \quad (A.2.8)$$

$$A = \frac{.44}{7W} \left[\left(\frac{FN-1}{R} \right)^2 + (FM-1)^2 \right]^{\frac{1}{2}} \quad (A.2.9)$$

$$QN = \sin \frac{22P}{7} (FN-1) \sin \frac{0.44}{7W} (FM-1) \sinh A \quad (A.2.10)$$

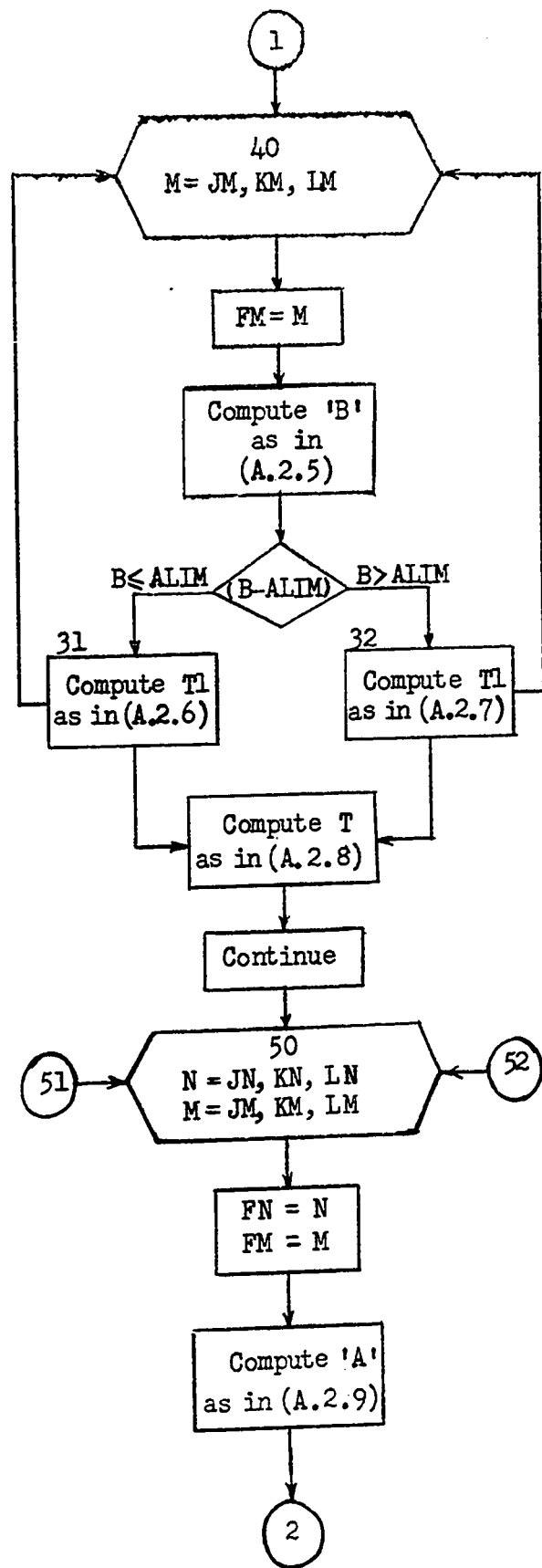
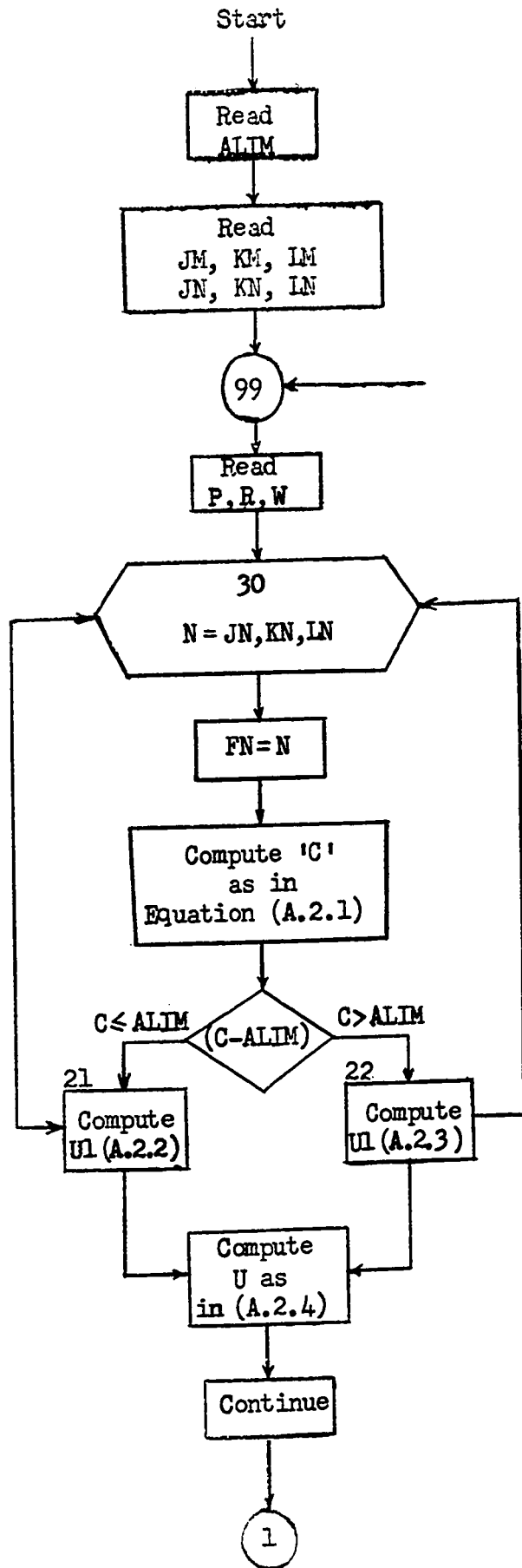
$$QD = (FN-1)(FM-1) \left[\left(\frac{FN-1}{R} \right)^2 + (FM-1)^2 \right]^{\frac{1}{2}} \cosh A \quad (A.2.11)$$

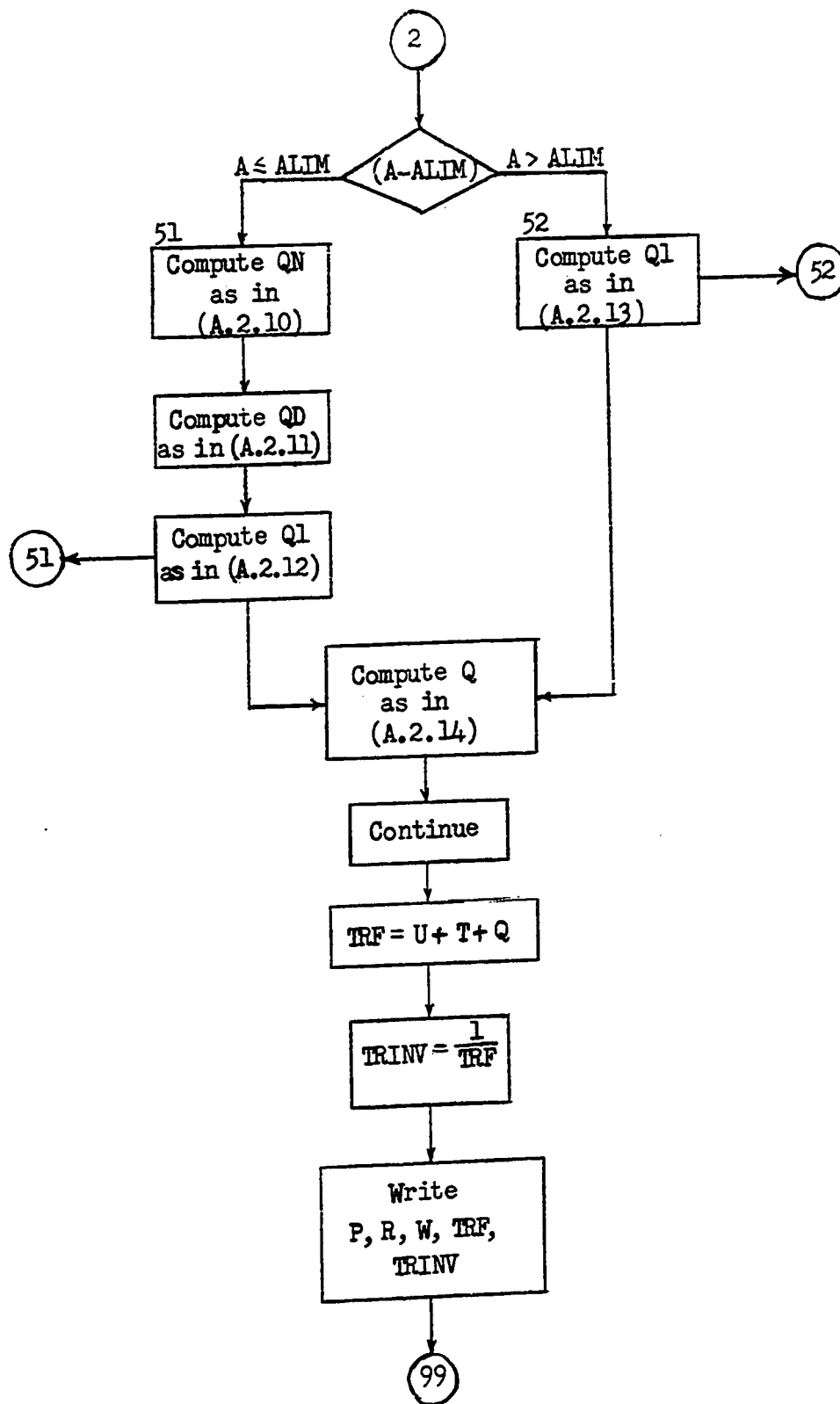
$$Q1 = Q1 + \frac{QN}{QD} \quad (A.2.12)$$

$$Q1 = Q1 + \frac{\sin \frac{22P}{7} (FN-1) \sin \frac{0.44}{7W} (FM-1)}{(FN-1)(FM-1) \left[\left(\frac{FN-1}{R} \right)^2 + (FM-1)^2 \right]^{\frac{1}{2}}} \quad (A.2.13)$$

$$Q = Q1 \frac{42875}{1331PR} \quad (A.2.14)$$

APPENDIX "D"





LEVELO 1JUL66
 C
 THIN FILM HEAT FLOW PROBLEM
 OMEGA=0.002 CM L=PH H=RW W=W
 VINCENT CALOIA

IBM OS/360 BASIC FORTRAN IV (E) COMPILATION

```

S:0001 READ(1,100)ALIM
S:0002 READ(1,101)JM,KM,LM,JN,KN,LN
S:0003 WRITE(3,104)
S:0004 FORMAT(10X,F10.6)
S:0005 100
S:0006 101 FORMAT(10X,6I6)
S:0007 199 READ(1,102)P,R,W
S:0008 102 FORMAT(10X,3F10.6)
S:0009 Q1=0.
S:0010 Y1=0.
S:0011 UI=0.
S:0012 DO 30 N=JN,KN,LN
S:0013 FN=N
S:0014 C=.44*(FN-1.)/(7.*R*W)
S:0015 IF(C-ALIM)21,22,22
21 2XP(-C))
S:0016 GO TO 23
S:0017 UI=UI*SIN((FN-1.)*22.*P/7.)/((FN-1.)*2)
S:0018 23 CONTINUE
S:0019 30 CONTINUE
S:0020 U=49.*UI/(242.*P*W)
S:0021 DO 40 M=JM,KM,LM
S:0022 FM=M
S:0023 B=.44*(FM-1)/(7.*W)
S:0024 IF(B-ALIM)31,32,32
S:0025 31 3) *EXP(-B))
S:0026 GO TO 33
S:0027 Y1=Y1*SIN((FM-1.)*.044/(7.*W))/((FM-1.)*2)
S:0028 33 CONTINUE
S:0029 40 CONTINUE
S:0030 T=T1*12250./((121.*R)
S:0031 DO 50 M=JM,KM,LM
S:0032 DO 50 N=JN,KN,LN
S:0033 FM=M
S:0034 FN=N
S:0035 A=.44*SQR((FN-1.)/R)**2*(FM-1.)*2)/(7.*W)
S:0036 IF(A-ALIM)51,52,52
S:0037 QN=SIN((FN-1.)*22.*P/7.)*SIN((FM-1.)*.044/(7.*W))*(EXP(A)-EXP(-A))
S:0038 QD=((FN-1.)*(FM-1.)*SQR((FN-1.)/R)**2*(FM-1.)*2)*(EXP(A)+EXP(-A)
67))
S:0039 Q1=Q1+QN/QD
S:0040 GO TO 53
S:0041 52 Q1=Q1+SIN((FN-1.)*22.*P/7.)*SIN((FM-1.)*.044/(7.*W))/((FN-1.)*2)*(FM-
S:0042 53 CONTINUE
S:0043 50 CONTINUE
S:0044 Q=Q1*42875./((1331.*P*R)
S:0045 TRF=U*Y1*Q
S:0046 TRINV=1./TRF
S:0047 WRITE(3,105)P,R,W,TRF,TRINV

```

LENGTH RATIO	SL TO WIDTH RATIO (R)	WIDTH	THERMAL FACTOR,	INVERSE TF
0.40	1.00	0.002500	266.865967	0.003747
0.40	1.00	0.003000	272.600586	0.003668
0.40	1.00	0.003500	272.630371	0.003668
0.40	1.00	0.004000	269.625488	0.003709
0.40	1.00	0.005000	258.998779	0.003861
0.40	1.00	0.006000	246.585983	0.004055
0.40	2.00	0.002500	238.206161	0.004198
0.40	2.00	0.003000	226.275101	0.004419
0.40	2.00	0.003500	215.240952	0.004646
0.40	2.00	0.004000	205.110092	0.004875
0.40	2.00	0.005000	187.134415	0.005344
0.40	2.00	0.006000	172.066971	0.005812
0.40	3.00	0.002500	226.710144	0.004411
0.40	3.00	0.003000	207.843430	0.004811
0.40	3.00	0.003500	192.600861	0.005192
0.40	3.00	0.004000	179.869370	0.005560
0.40	3.00	0.005000	159.395203	0.006274
0.40	3.00	0.006000	143.553314	0.006966
0.40	5.00	0.002500	216.869415	0.004611

0.40	5.00	0.003000	192.087173	0.005206
0.40	5.00	0.003500	173.215057	0.005773
0.40	5.00	0.004000	158.134857	0.006324
0.40	5.00	0.005000	134.962234	0.007409
0.40	5.00	0.006000	117.628510	0.008501
0.40	7.00	0.002500	212.306793	0.004710
0.40	7.00	0.003000	184.521454	0.005419
0.40	7.00	0.003500	163.458817	0.006118
0.40	7.00	0.004000	146.649048	0.006819
0.40	7.00	0.005000	120.953003	0.008268
0.40	7.00	0.006000	102.045486	0.009800
0.40	9.00	0.002500	208.775482	0.004790
0.40	9.00	0.003000	178.497696	0.005602
0.40	9.00	0.003500	155.425537	0.006434
0.40	9.00	0.004000	137.030884	0.007298
0.40	9.00	0.005000	109.319107	0.009148
0.40	9.00	0.006000	89.582886	0.011163
0.50	1.00	0.002500	207.223648	0.004826
0.50	1.00	0.003000	217.935104	0.004589
0.50	1.00	0.003500	221.727097	0.004510
0.50	1.00	0.004000	221.706238	0.004510
0.50	1.00	0.005000	215.700439	0.004636
0.50	1.00	0.006000	206.783295	0.004836

0.50	2.00	0.002500	180.093491	0.005553
0.50	2.00	0.003000	174.264954	0.005738
0.50	2.00	0.003500	167.866028	0.005957
0.50	2.00	0.004000	161.423035	0.006195
0.50	2.00	0.005000	149.067078	0.006708
0.50	2.00	0.006000	138.132263	0.007239
0.50	3.00	0.002500	169.787964	0.005890
0.50	3.00	0.003000	157.789917	0.006338
0.50	3.00	0.003500	147.688141	0.006771
0.50	3.00	0.004000	138.987061	0.007195
0.50	3.00	0.005000	124.517319	0.008031
0.50	3.00	0.006000	112.982758	0.008851
0.50	5.00	0.002500	161.242035	0.006202
0.50	5.00	0.003000	144.121262	0.006939
0.50	5.00	0.003500	130.889297	0.007640
0.50	5.00	0.004000	120.173386	0.008321
0.50	5.00	0.005000	103.412689	0.009670
0.50	5.00	0.006000	90.635468	0.011033
0.50	7.00	0.002500	157.330246	0.006356
0.50	7.00	0.003000	137.640305	0.007265
0.50	7.00	0.003500	122.541565	0.008160
0.50	7.00	0.004000	110.358780	0.009061
0.50	7.00	0.005000	91.477203	0.010932

0.50	7.00	0.006000	77.404236	0.012919
0.50	9.00	0.002500	154.322052	0.006480
0.50	9.00	0.003000	132.515793	0.007546
0.50	9.00	0.003500	115.720993	0.008641
0.50	9.00	0.004000	102.211243	0.009784
0.50	9.00	0.005000	81.677505	0.012243
0.50	9.00	0.006000	66.978104	0.014930
0.60	1.00	0.002500	159.989471	0.006250
0.60	1.00	0.003000	174.785675	0.005721
0.60	1.00	0.003500	181.691589	0.005504
0.60	1.00	0.004000	184.160126	0.005430
0.60	1.00	0.005000	182.029907	0.005494
0.60	1.00	0.006000	176.049179	0.005680
0.60	2.00	0.002500	134.295242	0.007446
0.60	2.00	0.003000	133.558487	0.007487
0.60	2.00	0.003500	131.010742	0.007633
0.60	2.00	0.004000	127.616104	0.007836
0.60	2.00	0.005000	119.865158	0.008343
0.60	2.00	0.006000	112.278259	0.008906
0.60	3.00	0.002500	124.936905	0.008004
0.60	3.00	0.003000	118.619965	0.008430
0.60	3.00	0.003500	112.741364	0.008870

NGTH RATIO	SL TO WIDTH RATIO	WIDTH	THERMAL FACTOR,	INVERSE TF
0.60	3.00	0.004000	107.329361	0.009317
0.60	3.00	0.005000	97.716461	0.010234
0.60	3.00	0.006000	89.632782	0.011157
0.60	5.00	0.002500	117.308243	0.008525
0.60	5.00	0.003000	106.426376	0.009396
0.60	5.00	0.003500	97.769913	0.010228
0.60	5.00	0.004000	90.584549	0.011039
0.60	5.00	0.005000	79.001022	0.012658
0.60	5.00	0.006000	69.904556	0.014305
0.60	7.00	0.002500	113.852585	0.008783
0.60	7.00	0.003000	100.723785	0.009928
0.60	7.00	0.003500	90.463394	0.011054
0.60	7.00	0.004000	82.042496	0.012189
0.60	7.00	0.005000	68.721649	0.014551
0.60	7.00	0.006000	58.606583	0.017063
0.60	9.00	0.002500	111.272171	0.008987
0.60	9.00	0.003000	96.351303	0.010379
0.60	9.00	0.003500	84.683304	0.011809
0.60	9.00	0.004000	75.180145	0.013301

0.60	9.00	0.005000	60.550552	0.016515
0.60	9.00	0.006000	49.983154	0.020007
0.70	1.00	0.002500	121.800964	0.008210
0.70	1.00	0.003000	140.006577	0.007143
0.70	1.00	0.003500	149.525177	0.006688
0.70	1.00	0.004000	154.093460	0.006490
0.70	1.00	0.005000	155.235458	0.006442
0.70	1.00	0.006000	151.731293	0.006591
0.70	2.00	0.002500	97.400497	0.010267
0.70	2.00	0.003000	100.947708	0.009906
0.70	2.00	0.003500	101.625366	0.009840
0.70	2.00	0.004000	100.772919	0.009923
0.70	2.00	0.005000	96.834229	0.010327
0.70	2.00	0.006000	91.996399	0.010870
0.70	3.00	0.002500	88.789536	0.011263
0.70	3.00	0.003000	87.212265	0.011466
0.70	3.00	0.003500	84.839661	0.011787
0.70	3.00	0.004000	82.146271	0.012173
0.70	3.00	0.005000	76.523148	0.013068
0.70	3.00	0.006000	71.257523	0.014034
0.70	5.00	0.002500	81.833420	0.012220
0.70	5.00	0.003000	76.100769	0.013140
0.70	5.00	0.003500	71.212524	0.014042

0.70	5.00	0.004000	66.931992	0.014941
0.70	5.00	0.005000	59.608475	0.016776
0.70	5.00	0.006000	53.549026	0.018674
0.70	7.00	0.002500	78.719528	0.012703
0.70	7.00	0.003000	70.995728	0.014085
0.70	7.00	0.003500	64.729126	0.015449
0.70	7.00	0.004000	59.423218	0.016828
0.70	7.00	0.005000	50.727005	0.019713
0.70	7.00	0.006000	43.914627	0.022771
0.70	9.00	0.002500	76.508514	0.013070
0.70	9.00	0.003000	67.283646	0.014862
0.70	9.00	0.003500	59.878342	0.016701
0.70	9.00	0.004000	53.720642	0.018615
0.70	9.00	0.005000	44.031342	0.022711
0.70	9.00	0.006000	36.906921	0.027095
0.80	1.00	0.002500	90.349625	0.011068
0.80	1.00	0.003000	111.433228	0.008974
0.80	1.00	0.003500	123.164658	0.008119
0.80	1.00	0.004000	129.514816	0.007721
0.80	1.00	0.005000	133.433060	0.007494
0.80	1.00	0.006000	132.023453	0.007574
0.80	2.00	0.002500	67.082086	0.014907
0.80	2.00	0.003000	74.254990	0.013467

0.80	2.00	0.003500	77.651733	0.012878
0.80	2.00	0.004000	78.934357	0.012669
0.80	2.00	0.005000	78.180481	0.012791
0.80	2.00	0.006000	75.624771	0.013223
0.80	3.00	0.002500	59.064484	0.016931
0.80	3.00	0.003000	61.469528	0.016268
0.80	3.00	0.003500	62.032837	0.016120
0.80	3.00	0.004000	61.608627	0.016231
0.80	3.00	0.005000	59.302597	0.016863
0.80	3.00	0.006000	56.370697	0.017740
0.80	5.00	0.002500	52.618744	0.019005
0.80	5.00	0.003000	51.180405	0.019539
0.80	5.00	0.003500	49.431198	0.020230
0.80	5.00	0.004000	47.569565	0.021022
0.80	5.00	0.005000	43.796967	0.022833
0.80	5.00	0.006000	40.276428	0.024828
0.80	7.00	0.002500	49.772690	0.020091
0.80	7.00	0.003000	46.554031	0.021480
0.80	7.00	0.003500	43.623474	0.022923
0.80	7.00	0.004000	40.927170	0.024434
0.80	7.00	0.005000	36.120346	0.027685
0.80	7.00	0.006000	32.091995	0.031160

0.80	9.00	0.002500	47.886185	0.020883
0.80	9.00	0.003000	43.428223	0.023026
0.80	9.00	0.003500	39.606216	0.025249
0.80	9.00	0.004000	36.270111	0.027571
0.80	9.00	0.005000	30.751953	0.032518
0.80	9.00	0.006000	26.519928	0.037707

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