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PERFORMANCE IMPROVEMENT OF A BINARY ALL-DIGITAL PHASE-LOCKED LOOP WITH A NEW AIDED-ACQUISITION TECHNIQUE

by

JEAN-PAUL SANDOZ

A thesis
presented to the School of Graduate Studies
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in
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UNIVERSITÉ D'OTTAWA
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ABSTRACT

A non-uniform sampling digital phase-locked loop is proposed with a sequential loop filter, in which two additional phase comparators are added conjointly with an estimation-decision circuit controlling the two distinct modes : ACQUISITION and TRACKING , in which the loop is to operate.These additions provide more freedom to deal with the conflicting requirements of minimum acquisition time and maximum noise rejection in the presence or absence of frequency drift.

Using the state transition model of the modified DPLL, the steady-state phase error variance and the mean acquisition time have been evaluated. The comparision between the theoretical analysis and the experiments has proven to be very satisfactory. Substantial reduction of the acquisition time, without severely degrading the noise reduction performance has been achieved. The improved ability of this modified loop to track frequency drift was also demonstrated.

A digital loop ''quasi-bandwidth'' measure was used in the evaluation of the loop performance, thus allowing for a comparison with other digital loops and to a limited extend with a first order analog loop. The usual difference in

performance favoring the analog loop for high signal-to-noise ratio is shown to be substantially reduced and can be lowered by an appropriate choice of parameters. Moreover, the hardware needed for the implementation is shown to be very simple.

ACKNOWLEDGEMENTS

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CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

Symbols

A	Value of the input signal at sample time T_A
A'	Sgn A
B	Value of the input signal at sample time T_B
B'	Sgn B
B_o	overall frequency locking-range (in the absence of noise)
C	Value of the input signal at sample time T_C
C'	Sgn C
D	Difference of the signed values of B and C (D=B'-C')
E	Sum of D's between consecutive corrections
f_o	Frequency of s(t)
i	Stage index
k	number of complete cycles of s(t) between the sets of samples
ℓ	Integer number of unit phase steps
$\ell\Delta$	Phase between consecutive samples of a same set
m	number of phase states per half cycle
n	ratio between the large ($n\Delta$) and the small (Δ) corrections (integer number)
n(t)	Narrow-band noise process
N	Random-walk filter length (total length=2N+1)
s(t)	Sinusoid of frequency f_o ($s(t)=A \sin(2\pi f_o+\theta_i(t))$)
S_m	Mean number of sets of samples before the completion of the acquisition
T	Period of the input signal
T_A	Sample time of A
T_B	Sample time of B
T_C	Sample time of C
Th	Threshold used to choose the 3PDPLL mode

Symbols cont'd

T_m	Mean acquisition time ($T_m=kTS_m$)
T_s	Time between 2 samples in a same set ($T_s=T\ell\Delta/2\Pi$)
$\theta_i(t)$	Phase of s(t)
$\theta_o(t)$	Output phase of the DPLL
φ	Corresponding angle of T_A
φ'	Corresponding angle of T_B ($\varphi'=\varphi+\ell\Delta$)
φ''	Corresponding angle of T_C ($\varphi''=\varphi-\ell\Delta$)
φ'''	$\varphi+\ell\Delta-\Pi$
Δ	Size of the unit phase step ($\Delta=\Pi/m$)
$\Delta f/f_o$	Proportion of frequency deviation of s(t)
$\phi(t)$	Phase error between s(t) and the DPLL reference clock ($\theta_i(t)-\theta_o(t)$)
ϕ_{RMS}	RMS phase error (steady state)

Chapter I

INTRODUCTION

1.1 STATE OF THE ART

Phase-locked loops play an important role in transmission systems, more particularly for the recovery of the carrier phase and symbol timing in synchronous detection, in order to reduce the probability of error of the received symbols to a minimum. With the development of ''Large Scale Integration'' in digital communication systems and subsystems, the trend is to use digital phase-locked loops because of the decreased size and cost as well as increased reliability, inherent insensitivity to environmental changes (mainly temperature) and long time averaging or filtering capabilities. The digital phase-locked loop is defined as having at least the two following properties :

(1) The output phase is generated in discrete increments, not as a continuous function.

(2) The phase error is generated as a digital number, not as a multilevel voltage nor a continuously varying voltage.

Some of the problems associated with analog PLL's, namely, voltage controlled oscillator non-linearities, limited

capabilities for long time averaging of the loop filter, sensitivity to dc drifts, and the need for initial calibration and periodical adjustments are alleviated by a digital version of the PLL (DPLL).

A recent survey of DPLL's [1] has demonstrated that even with a rather large variety of implementations available, the performance can still be improved upon. With DPLL systems, the designer is usally faced with several different requirements such as minimum phase error variance, small acquisition time and maximum locking-range and he must also produce an inexpensive, flexible and reliable design. In order to keep the DPLL hardware realization simple, the lead/lag DPLL is usually used since it does not required any analog-to-digital conversion. Instead, a hard-limiter determines the sign of the sampled input signal indicating whether it is leading or lagging the loop reference clock.

Some solutions to these basic but yet conflicting requirements are reported by Yamamoto and Mori [2] and Andrea and Russo [3] in the form of a binary quantized all digital phase-locked loop with a variable reset random-walk filter and with a Costas loop configuration respectively. Recently, Heiman and Bar-Ness [4] have demonstrated in their study of the achievable improvements of the tracking and acquisition mode of analog PLL's, ''that by adding another phase detector, the system can be provided with enough additional

freedom to be able to better deal with these conflicting requirements and yield smaller errors''.

1.2 PROBLEM STATEMENT

The purpose of this work is to improve the tracking and acquisition behavior of the solutions [2] and [3] while avoiding any significant increase of the hardware complexity. It is more specifically based on the Costas like DPLL described by Andrea and Russo [3] complemented by the addition of a third phase comparator and a random-walk filter [5], in order to obtain a statistical estimate of the relative amplitude of the phase error (which is unknown if a single sample per cycle of the input signal is taken). These additions will allow the modified DPLL (3PDPLL) to decide whether it is either in acquisition or tracking mode resulting in large or small phase steps, respectively, in the process of phase correction; since fast acquisition is achieved with large phase step corrections and small steady-state phase error with small ones.

1.2.1 Outline of the thesis

Chapter II : The four basic components of a DPLL are described. The phase locking operation of the lead/lag DPLL is analysed and examples of simulations in the presence of noise presented so as to illustrate the effect of the step

size on both the acquisition time and the steady-state phase error.

Chapter III : The block diagram of the proposed DPLL is presented and its operation described. The graphical analysis carried out gives physical insight into the acquisition and tracking behavior in the absence of noise. The acquisition time reduction is derived for the noisefree case . Computer simulation plots are shown which verify the effectiveness of the proposed system changes in the presence of noise.

Chapter IV : Following the description of the input signal, the 3PDPLL is modeled using the Markov chain approach since the number of possible phase error conditions and their respective transition probabilities are defined. The mathematical model so derived follows [2] and [5] and the random-walk technique of [5],[6] and [7] is applied to evaluate the RMS phase error and the mean acquisition time . All the calculation steps are presented along with a numerical example.

Chapter V : A series of plots of numerical results is depicted to show the effect of the variation of some of the 3PDPLL parameters.These results

can then be better compared by using a loop ''performance criterion'' defined in terms of the RMS phase error and the acquisition time (which is closely related to the bandwidth of the loop) for a given signal-to-noise ratio.While providing a common basis for comparison of different digital loops, it also serves, to a limited extend, for the comparison with first order linear loops.

Chapter VI : An experimental system based on a SDK 85 microprocessor and a hardware realization of the 3PDPLL are presented along with the obtained experimental results. The behavior of the 3PDPLL under frequency deviation in the presence of noise is tested experimentally and by computer simulation. Potential applications are discussed.

Chapter II

DESCRIPTION AND OPERATION OF THE DIGITAL PHASE-LOCKED LOOP

2.1 INTRODUCTION

The four essential elements of a DPLL are the digital clock, the sampler, the quantizer and the digital loop filter. Following the presentation of the basic block diagram of the DPLL, each separate element is defined and the phase locking loop operation of the digital loop presented. The lead/lag DPLL [1] with a structure that leads itself well to simple hardware implementation is described. It will serve as a building block for the proposed modified DPLL . Finally, computer simulations of the lead/lag DPLL with a sequential filter in the absence or presence of noise are carried out.

2.2 DESCRIPTION OF THE DPLL COMPONENTS

A DPLL contains four basic components (Fig. 1) :

1. Digital clock
2. Sampler
3. Quantizer
4. Digital loop filter

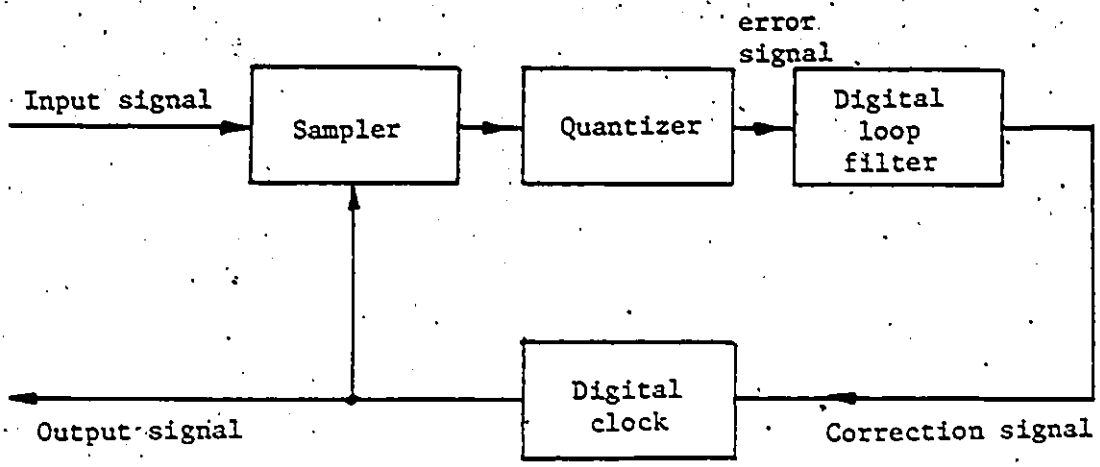


Figure 1: Basic digital phase-locked loop

2.2.1 Digital clock

The digital clock of the loop takes over the function of the voltage controlled oscillator (VCO) of an analog phase-locked loop.It is a time reference that is controlled by an external digital signal so as to decrease the phase difference between the input signal and the digital clock. Usually, in the absence of an input signal or in the case of signals buried in high level noise, the digital clock runs at a preset frequency (usually the most probable input signal frequency). It generates a train of pulses that indicates the sampling times of the input signal.

For first order systems, the corrections result in a phase-step of the clock and for second order systems, the corrections result in either a phase-step or a frequency-

step or both. The digital clock stability is defined by the desired short and long term stability of the system under consideration and also by the characteristics of the input signal.

2.2.2 Sampler and quantizer (digital phase detector)

The input signal is sampled in synchronism with the clock signal. Since the input signal is analog, a conversion ''analog to digital'' is required at this stage of the loop. In a hardware design, a so called ''sample and hold'' scheme is used such that once the sample is taken, it is held in an analog memory until the next sample arrives. In the mean time, that analog value is converted by the quantizer (A/D converter) into a digital number representing a measure of the phase difference between the input and output signals of the loop. The combined sampler and quantizer components of a digital PLL are the equivalent of the phase detector of an analog PLL.

2.2.3 Lead/Lag sampling phase detector

The lead/lag sampling phase detector (LL-PD) is a one bit sampler-quantizer. Frequently encountered in practice for its simple hardware implementation (in the form of a threshold detector), it will be used in the design of the 3PDPLL so as to simplify the practical realization and to minimize cost.

The LL-PD is characterized by an output indicating whether the digital local reference (digital clock) leads or lags the input signal (Fig. 2). Because of the rough quantization, a sequential filter is frequently used to smooth the correction controlling the local reference.

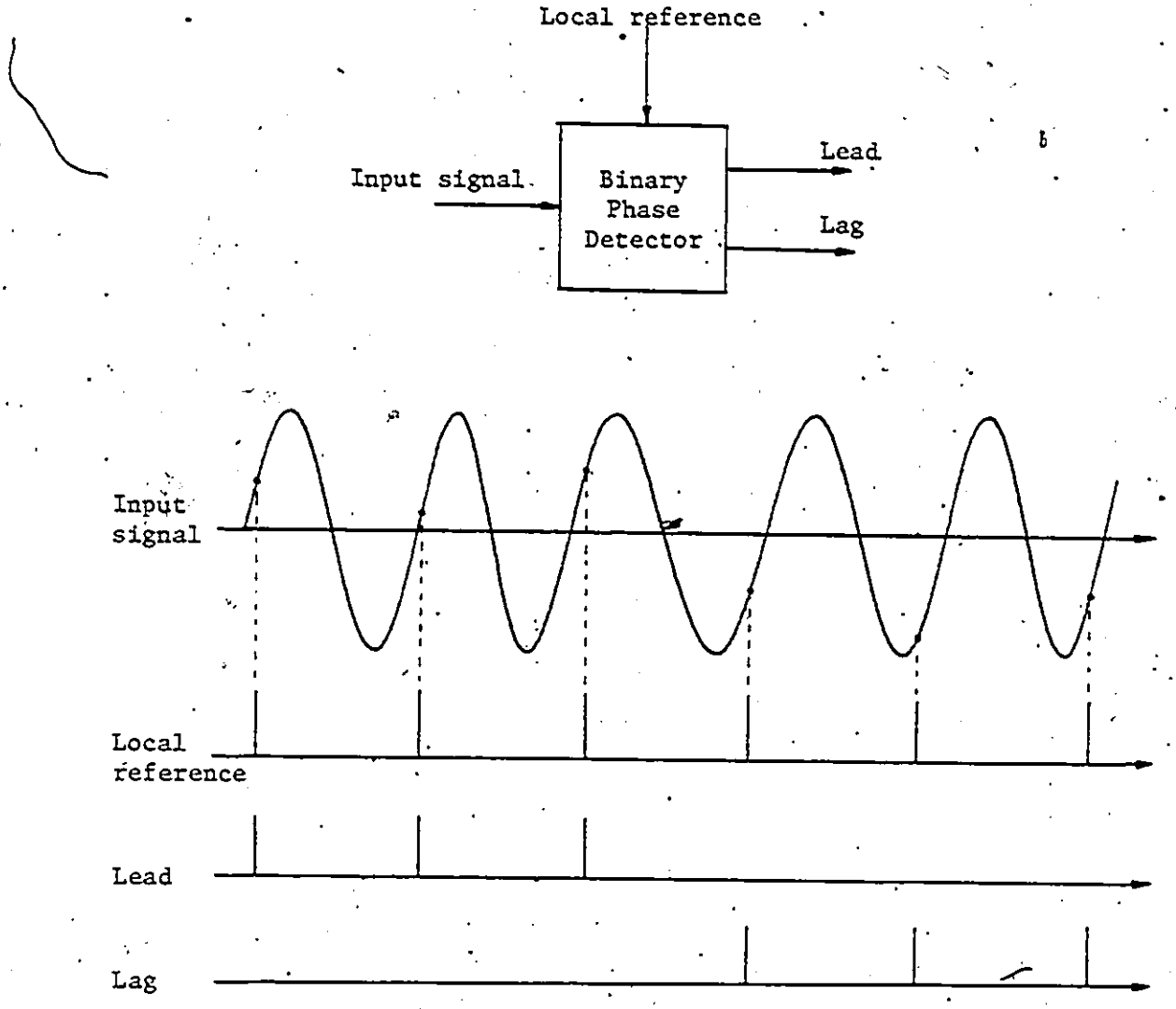


Figure 2: Lead/Lag sampling phase detector

2.2.4 Digital loop filter

The purpose of the digital loop filter (low-pass filter) is to generate a control signal for the digital clock so as to maximize the probability of proper adjustement of the digital clock phase in controlling the rate and amplitude of the phase corrections. This is particularly important when the signal is embedded in noise. It thus provides a limited memory of the phase detector outputs; hence phase adjustements of the digital clock become dependent on an input sequence rather than a single phase detector output.The acquisition time and tracking performances in the presence or the absence of noise are very dependent upon the filter characteristics.

2.3 PHASE LOCK LOOP OPERATION OF THE LEAD/LAG DPLL

This operation is illustrated in Fig. 3 Consider the input signal as a sinusoidal carrier wave form of constant amplitude and without noise. We assume that one sample is taken for every cycle and that we wish to synchronize our digital clock on a positive going zero-crossing of the input signal.

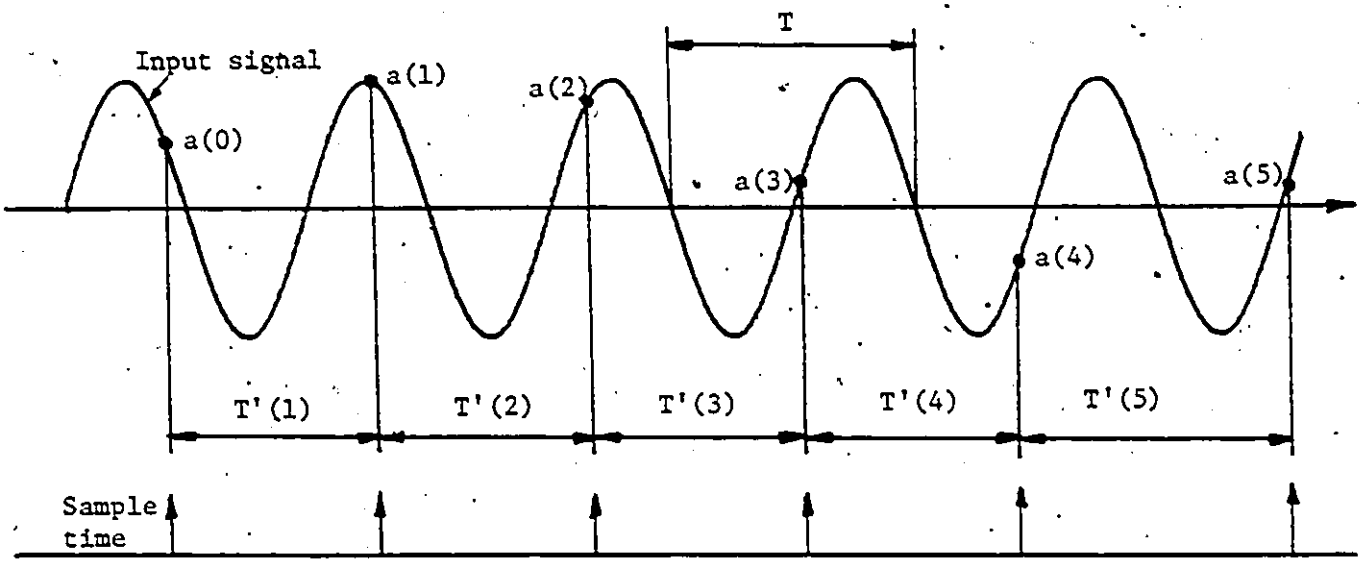


Figure 3: Phase lock loop operation of the LL-DPLL

When it is known whether the digital clock phase leads or lags, it is corrected by , respectively, a negative or a positive phase step. During the correction process, the sampling instant is moved closer to the positive going zero-crossing. Thus, after a few corrections, the digital clock phase will oscillate around the zero-crossing. The amplitude of that oscillation is directly dependent upon the minimum phase step. Assuming that 2m phase corrections are needed to cover a whole cycle (2π), than :

$$T'(j+1) = T - (T/2m)\ \mathrm{sgn}\ a(j) = T\,(\,1 - (1/2m)\ \mathrm{sgn}\ a(j)\,) \quad (1)$$

For the example of Fig. 3 :

a(0) > 0	T'(1) = T (1 - 1/2m)
a(1) > 0	T'(2) = T (1 - 1/2m)
a(2) > 0	T'(3) = T (1 - 1/2m)
a(3) > 0	T'(4) = T (1 - 1/2m)
a(4) < 0	T'(5) = T (1 + 1/2m)
a(5) > 0	T'(6) = T (1 - 1/2m)

2.4 SEQUENTIAL FILTER

In [1], Lindsey and Chie define this type of filter in that ''The name sequential filter implies that the output is not a linear function of a fixed number of inputs since it observes the inputs for a variable duration of time and gives an output when a certain confidence limit on the input is established (similar to the sequential threshold test in estimation theory) ''.

2.4.1 The random-walk filter

As an important part of the proposed DPLL, a class of sequential filter, the ''Random-Walk Filter'' is used. It is made up of a bi-directional counter of length 2N+1. In Fig. 4, the content of the counter is increased or decreased by one for the signal at 'a' or at 'b' respectively (the lead/lag outputs of the binary phase detector). When it

reaches 0 or 2N an output Retard or Advance is produced and the counter is reset to N. So at least N inputs are needed to produce one output and many more if the probabilities of occurances of the inputs are nearly equal. Since a larger N will result in a longer delay before any output is produced, the random-walk filter behaves like a non-linear lowpass filter (whose bandwidth decreases as N increases and varies with the signal-to- noise ratio at its input). The probability relations between input and output of the random-walk filter and the avarage time before termination are analysed as the classical ruin problem [9].

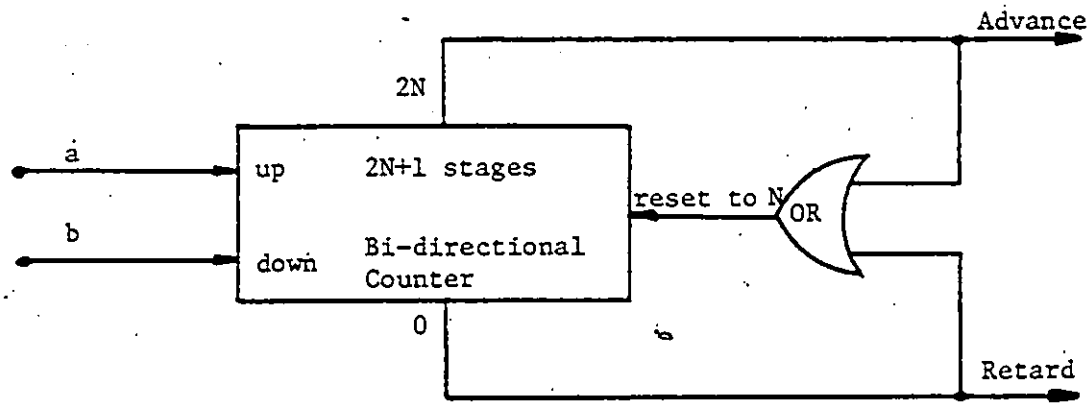


Figure 4: Random-walk filter

2.5 THE LEAD/LAG DPLL WITH RANDOM-WALK FILTER

In Fig. 5, the block diagram of the lead/lag DPLL with random-walk filter (LRDPLL) is presented.The phase corrections are ,in practice, performed by adding or deleting cycles to a stable reference signal . Its frequency is 2m times larger than the frequency of the input signal in order to digitally generate the 2m phase steps desired to quantize a period T in 2m phase states.

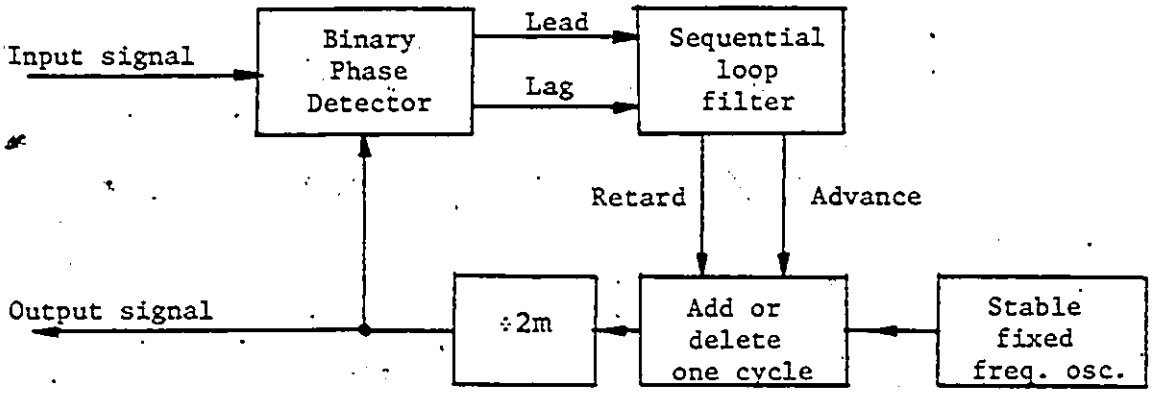


Figure 5: Block diagram of the LRDPLL

2.5.1 Computer simulation of the LRDPLL

Two different cases of simulation of the phase step response are considered :

(1) Simulation in the absence of noise

(2) Simulation in the presence of noise for a narrowband Gaussian noise process.

Samples of results are presented in Fig. 6 and Fig. 7 respectively. These samples of simulations very well illustrate that the transient time (acquisition time) decreases and the variance of the steady state phase error increases when the phase step size increases.

The increasing of the phase step size corresponds to a widening of the loop bandwidth, hence the DPLL time response is reduced but more noise is allowed in the system thus degrading the tracking performance.

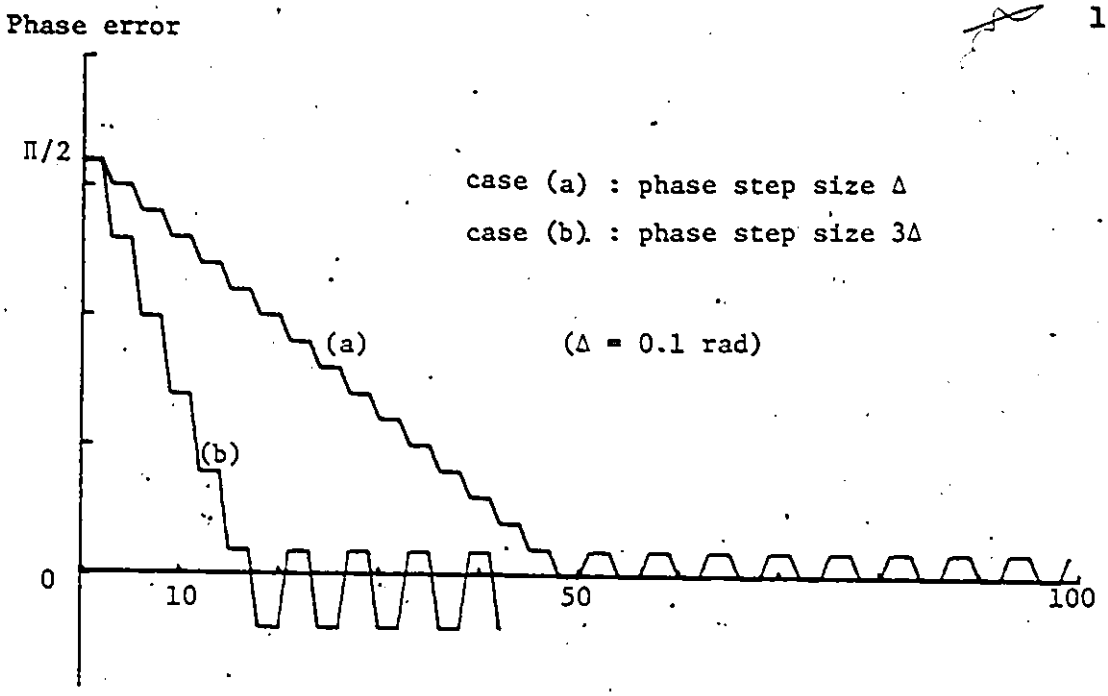


Figure 6: Phase step response of the LRDPLL in the absence of noise

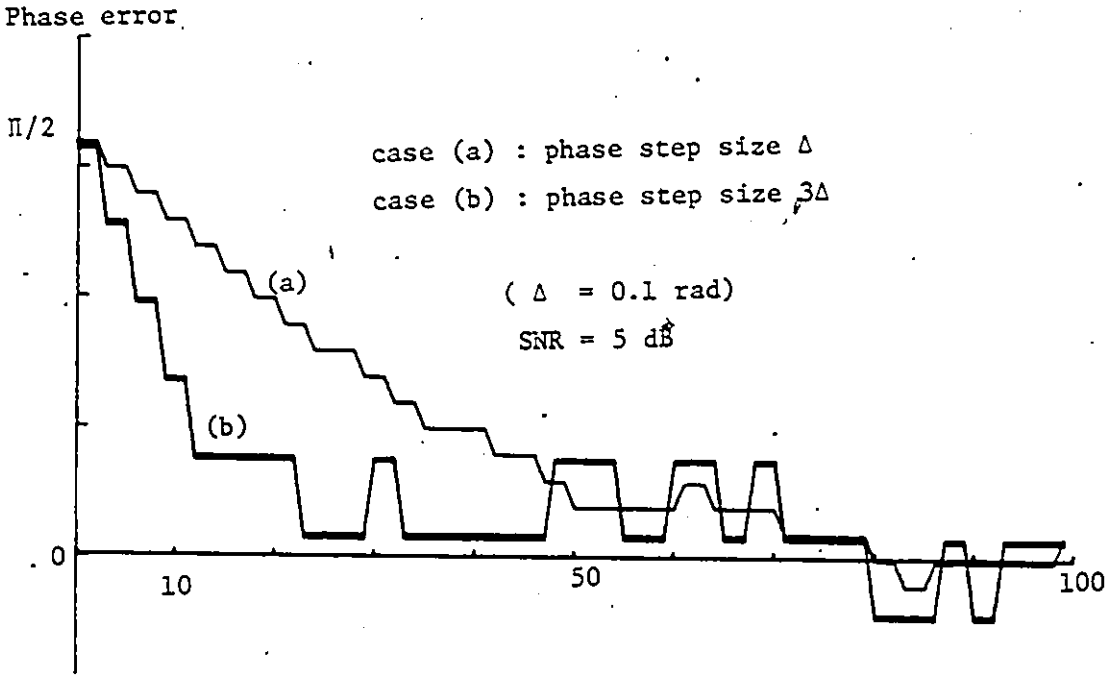


Figure 7: Phase step response of the LRDPLL in the presence of noise

Chapter III

MODIFIED LEAD/LAG DPLL

3.1 INTRODUCTION

When a single sample per cycle of the input signal is taken with a lead/lag phase detector, the sign of the phase error (difference between the input signal phase and the digital clock phase) is the only information obtained (the input signal leading or lagging the local reference).

By taking three samples per cycle of the phase error, some information can be gained pertaining to the relative phase error amplitude. This allows to define two loop operating modes 'Acquisition' and 'Tracking' resulting in a large or small correction phase step respectively.

In the absence of noise, while maintaining the steady state RMS phase error to its level when only small phase steps are used, the modification proves to approximately reduce the acquisition time by a factor equal to the ratio of the two phase steps.

In the presence of noise, the computer simulations carried out demonstrate that some reduction of the mean acquisition time can be achieved without significantly increasing

the steady state RMS phase error . The minimum signal-to-noise ratio below which, in practice, the effectiveness of the 3PDPLL is lost is presented in chapter V.

3.2 PROPOSED DIGITAL PHASE-LOCKED LOOP

The proposed DPLL is shown in Fig. 8 . The input x(t) is defined as :

$$x(t)=s(t)+n(t) \qquad (2)$$

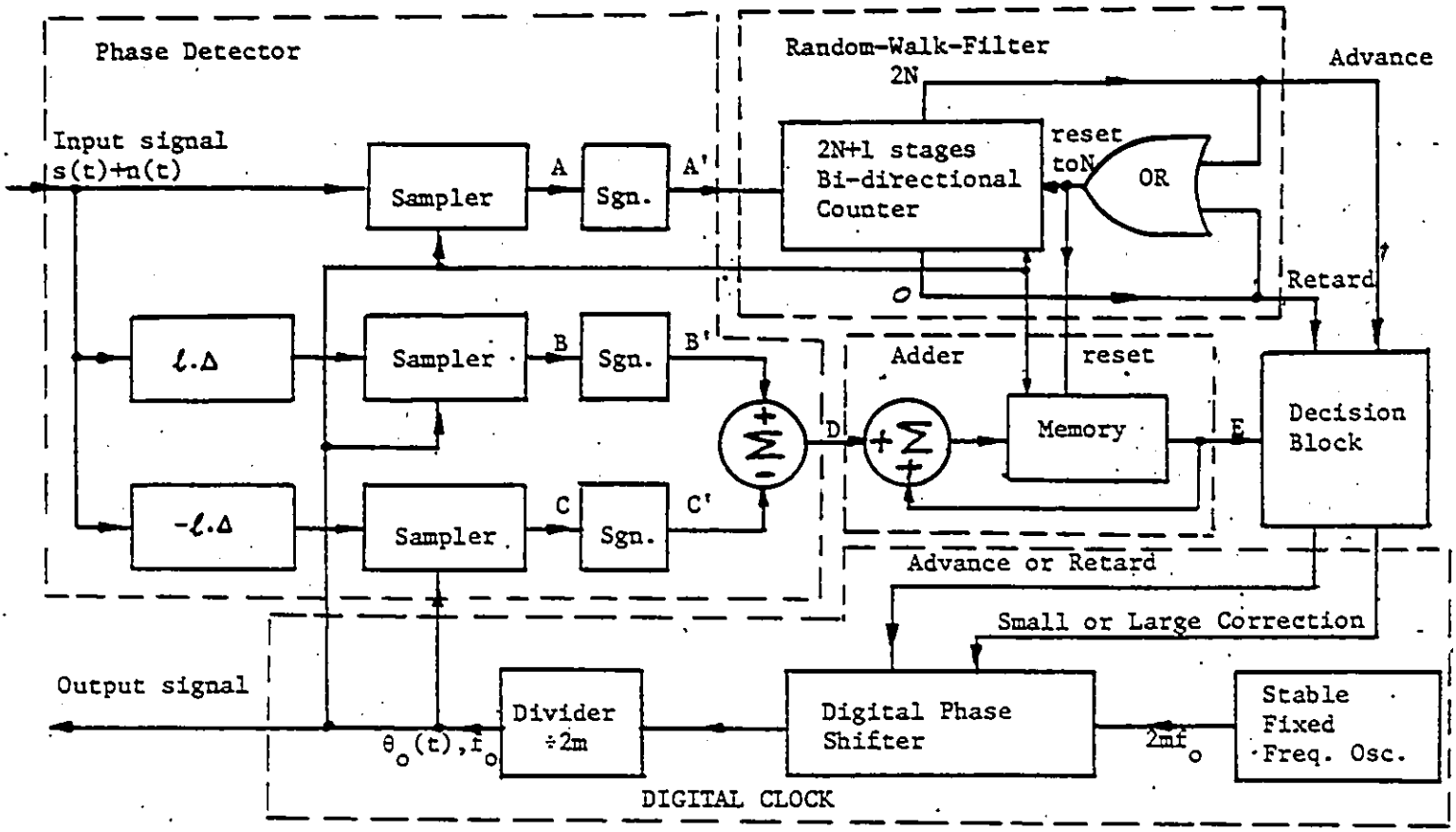
where s(t) is a sinusoid of known frequency f_o (period T) and n(t) is a band limited Gaussian noise. Sets of three samples are taken at every k^{th} (integer) cycle of the signal s(t).

The DPLL itself can be described as a First-Order Transition Sampling DPLL using a Random-Walk-Filter with the addition of an estimation-decision circuit controlling the state in which the loop is to work. We define two possible modes as follows:

(1) Acquisition, using the larger step corrections (wider loop bandwidth)

(2) Tracking , using the smaller step corrections (narrower loop bandwith)

The information at point D (Fig. 8), the difference of the signed values of the shifted input signal x(t), increments or decrements a counter. Its output (E) is used when the random-walk filter gives a command of advance or retard as a criterion for the size of the correction.



$2m$: number of phase states per cycle
$\Delta = \pi/m$: size of the unit phase steps
ℓ : integer number of unit phase steps (define the distance between the three samples)
n : ratio between the large ($n\Delta$) and the small (Δ) corrections (integer number)
$2N+1$: random-walk filter length
$\theta_o(t)$: output phase
$\theta_i(t)$: phase of s(t)
$\Phi(t)$: phase error ($\theta_i(t) - \theta_o(t)$)

Figure 8: Block diagram of the 3PDPLL

3.3 GRAPHICAL ANALYSIS

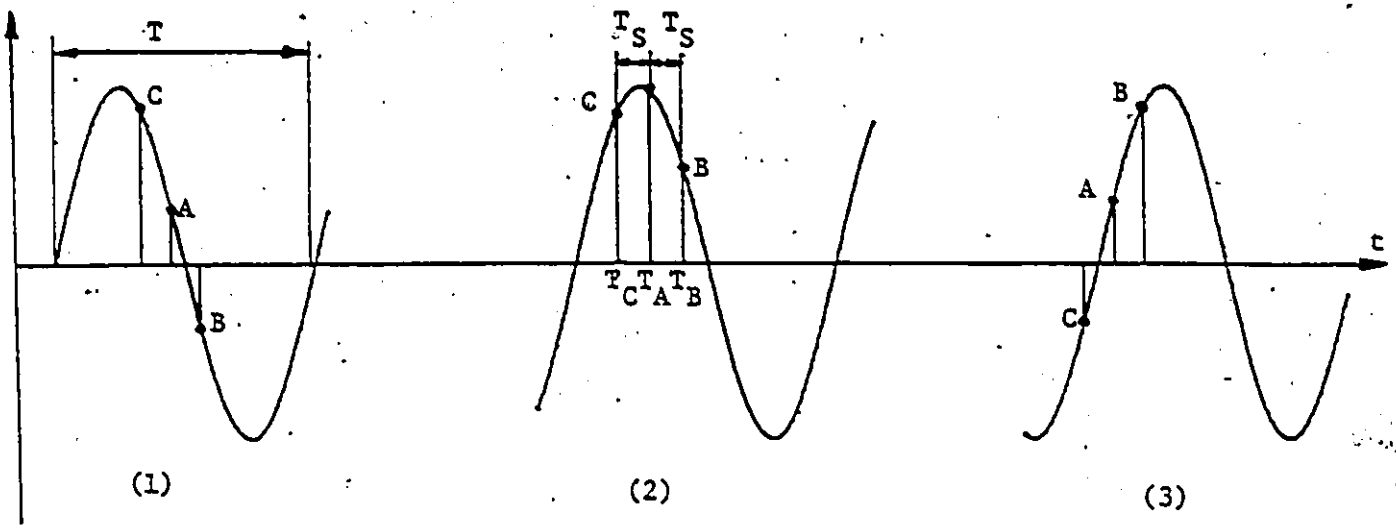
From Fig. 9 , we observe that there are only six possible outcomes for [A' B' C'] and three corresponding outcomes for D (-2,0,+2) as listed in table 1.The plot of D versus the phase error is presented in Fig. 10

If the PLL is assumed to track the positive going zero-crossing of x(t), then we can define the two possible modes as a function of the average value of D (represented by E) at the time of a correction, which can be translated into an appropriate choice of correction step size (i.e. loop gain) as follows :

Mode	Average Value of D	Correction size	Corresponding Phase-Error Φ
Acquisition	-2 , 0	$n\,\Pi/m$	$\ell\cdot\Delta<\lvert\Phi\rvert\leq\Pi$
Tracking	+2	Π/m	$\lvert\Phi\rvert\leq\ell\cdot\Delta$

where n (an integer) is the ratio of the two correction sizes and must satisfy the inequality $n\leq 2\ell$ in order to avoid the danger of an excessively high phase error.

In other words, whenever the phase error falls within $\pm\ell\Delta$, the loop will be in the tracking mode. Conversely, if the absolute value of the phase error is larger than $\ell\cdot\Delta$, the loop will be in acquisition mode. This is illustrated in Fig. 11 .



T_A : Sample time of A, the corresponding angle is φ
T_B : Sample time of B, the corresponding angle is $\varphi' = \varphi + \ell \cdot \Delta$
T_c : Sample time of C, the corresponding angle is $\varphi'' = \varphi - \ell\,\Delta$
T_s : Time between 2 samples in a same set, the corresponding angle is $\ell\Delta$

$$T_s = T\,\ell\Delta/2\pi$$

Figure 9: Example of three different cases of samples [A',B',C']

TABLE 1

Values of D in function of the samples [A'B'C']

	(1)	(2)	(3)	(4)	(5)	(6)
A'	+1	+1	+1	-1	-1	-1
B'	-1	+1	+1	+1	-1	-1
C'	+1	+1	-1	-1	-1	+1
D	-2	0	+2	+2	0	-2

A' = Sgn A, B' = Sgn B, C' = Sgn C, D = B'-C'

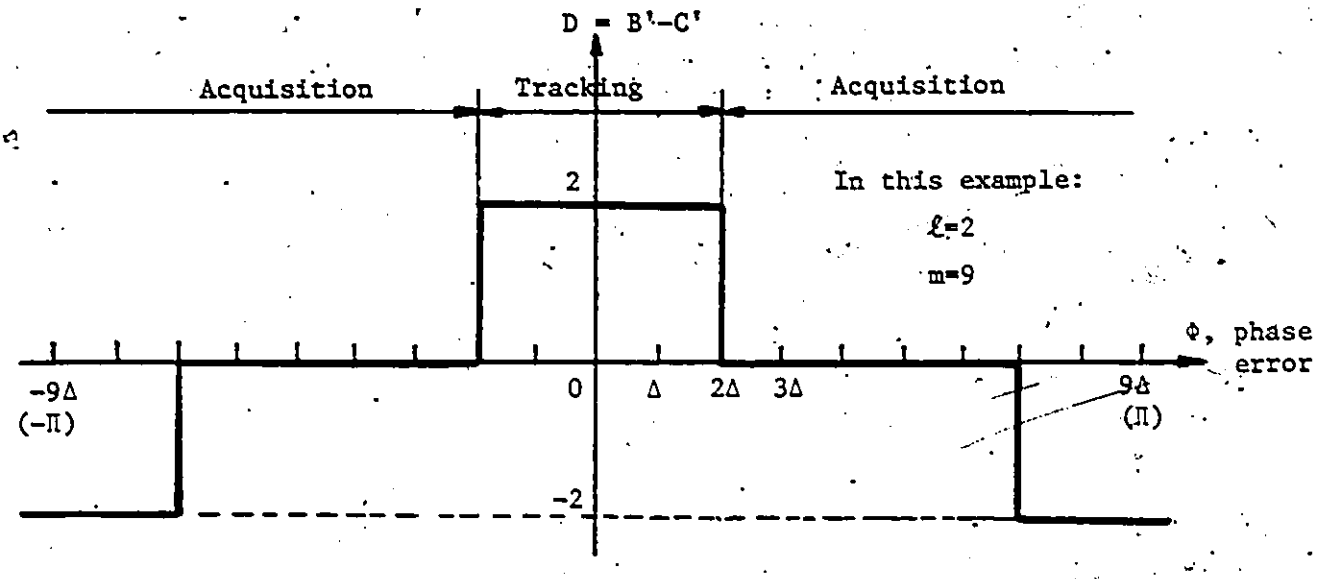


Figure 10: Plot of D versus phase error (noise free case)

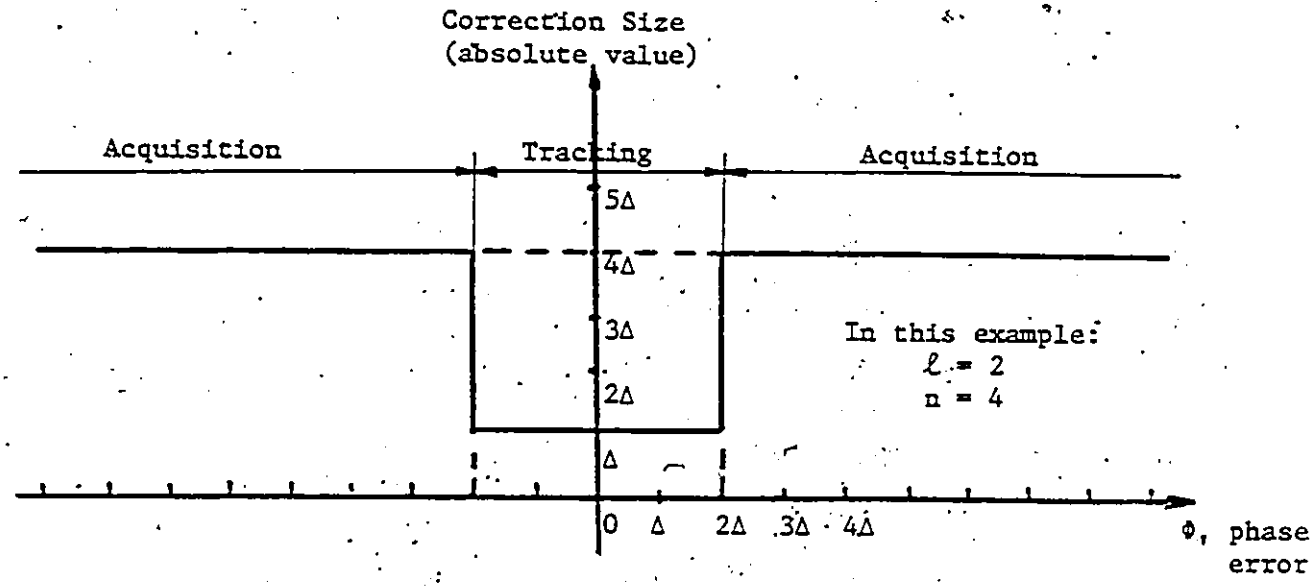


Figure 11: Plot of the correction size versus phase error (noise free case)

In practice (with noise or frequency drift), the average value of the signal at D will fall within the range -2 to +2 and, a threshold (Th), whose value is larger than zero*, is chosen (in the decision block) in order to translate the information from the two additional samplers into the most likely mode in which the loop is to work. It is worth noting that the signal at E (controlling the correction step size) is a measure of the correlation between the samples B and C . It changes when the absolute value of the phase error gets larger than $\ell\Delta$ and the power of s(t) is large compared to the noise variance (high SNR). However, this change becomes less and less noticeable as the SNR gets smaller and smaller. The minimum SNR below which the effectiveness of the 3PDPLL is ,in practice, lost is presented in chapter V.

In Fig. 12, the synchronization process is depicted for an initial phase error of approximately $\pi/2$. As shown, once the acquisition is completed the correction size is reduced and the tracking takes over. The maximum phase error is equal to Δ

---

* From Fig. 18 and 19, Th must be larger than zero in order that when the samples A,B and C (of a same set) have the same signs (+++ or ---), the 3PDPLL would be in acquisition mode. On the other hand, Th must be smaller or equal to N so that when the absolute value of the phase error is smaller than $\ell\Delta$, the 3PDPLL would be in tracking mode.

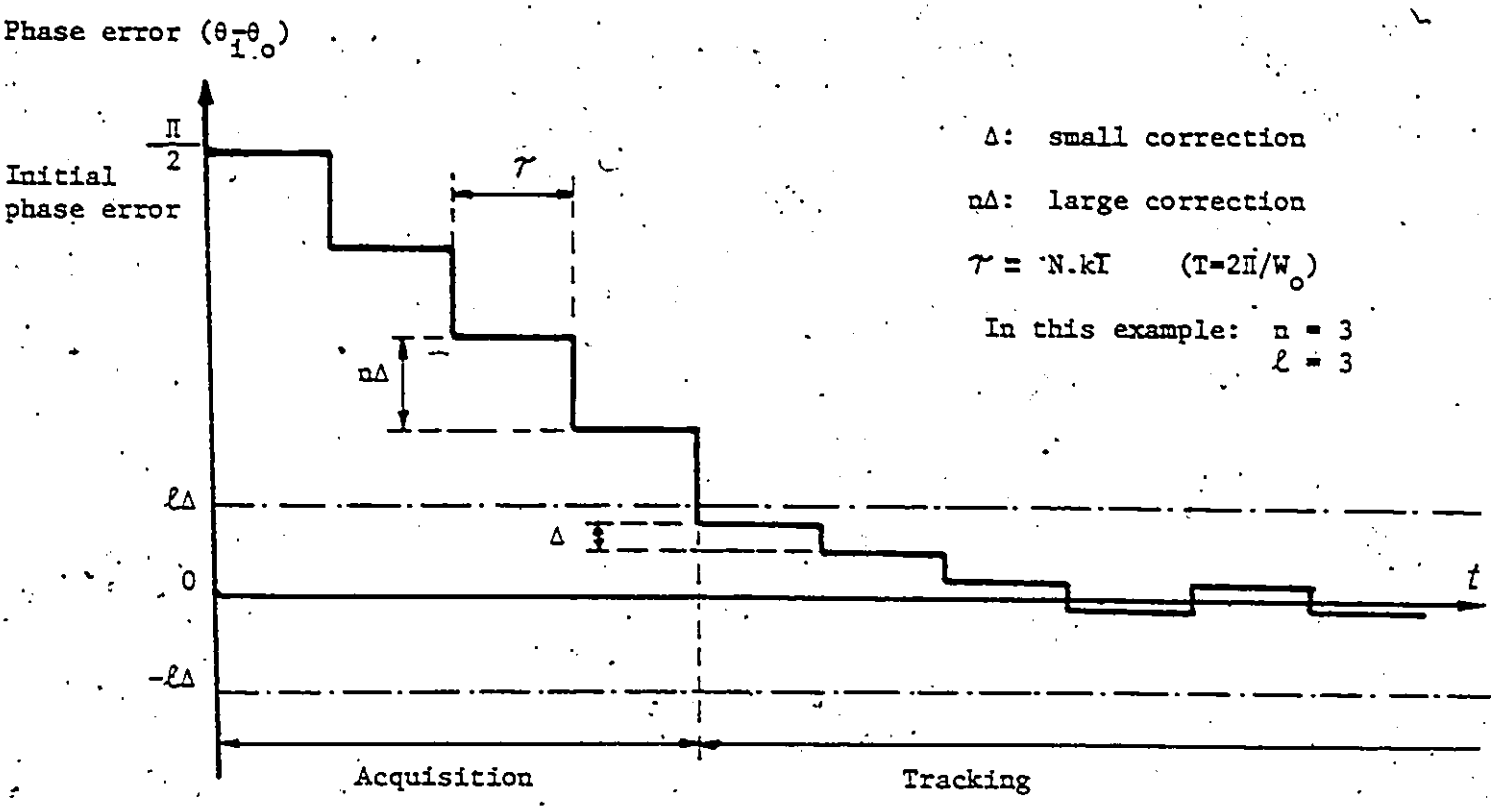


Figure 12: Example of Acquisition and Tracking (noise free case)

3.4 FREQUENCY LOCKING-RANGE AND ACQUISITION TIME

The frequency locking-range of the 3PDPLL is given by :

$$f_{ho} = \frac{1}{T\left(1 - \frac{n/kN}{2m}\right)} = f_o \frac{2mNk}{2mNk-n} \qquad (3)$$

$$f_{lo} = \frac{1}{T\left(1 + \frac{n/kN}{2m}\right)} = f_o \frac{2mNk}{2mNk+n} \qquad (4)$$

$$B_o = f_{ho} - f_{lo} = 2mNf_o k \frac{2n}{4m^2N^2k^2-n^2} \qquad (5)$$

$$B_o \approx f_o \frac{1}{m\,N\,k}$$

where n/kN is the number of unit phase step correction per cycle, f_o is the free-running frequency of the DPLL, f_{ho} and f_{lo} are respectively the high and low limits of the range and B_o the overall range.

The mean number of sets of samples S_m before completion of the acquision (pull-in) can be approximated by the number of sets of samples to cover $\pi/2$ radians .

$$S_m \simeq \frac{N \cdot m}{2 \cdot n} \qquad (6)$$

provided $8\ell < m$ and $n < m/4$

The mean acquisition time T_m is defined by :

$$T_m = k\ T\ S_m \qquad (7)$$

From the equation (5) and (7), the improvement factor on the locking-range and the acquisition time is directely related to n, and the phase error is kept the same since it solely depends upon the smallest phase step Δ during the 'Tracking' phase. These results will be demonstrated in chapter V and VI.

3.5 SIMULATION OF THE 3PDPLL IN THE PRESENCE OF NOISE

In order to estimate the effectiveness of the modified loop in the presence of narrowband Gaussian noise, numerous computer simulations of the transient and steady state responses of both the 3PDPLL and the LRDPLL were carried out. In Fig. 13 and Fig. 14, typical transient response behavior is illustrated (with an initial phase error of $\pi/2$) for a signal-to-noise ratio of 5 dB. The first figure presents one run for the LRDPLL and the 3PDPLL where the second figure presents a superposition of runs (6) for the same SNR but using different noise sequences.

The two cases of the figures 13 to 16 have the following parameters :

(a) LRDPLL : N = 5, m = 32

(b) 3PDPLL : N = 6, m = 32, n = 4, Th = 3, ℓ = 2

Another series of runs was conducted with no initial phase error, to compare the performance in the steady state condition (tracking). Results are presented in Fig. 15 and Fig. 16

These figures confirm that a reduction of the mean acquisition time for very little increase of the RMS phase error can also be achieved in the presence of noise.

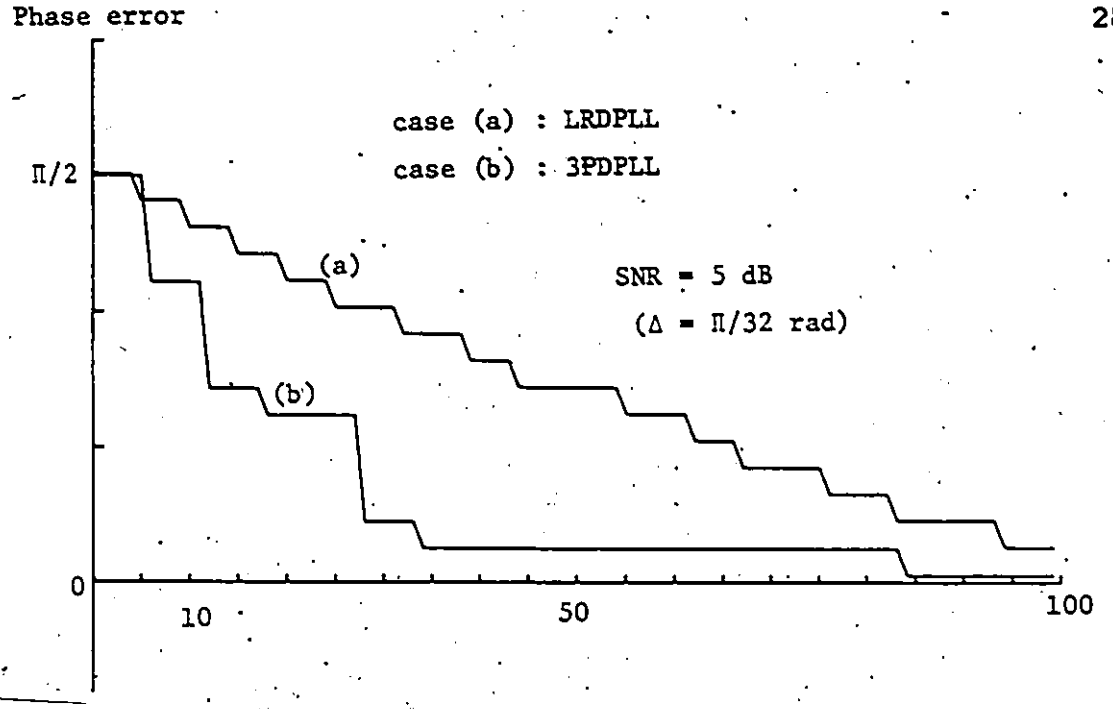


Figure 13: Example of acquisition (one run)

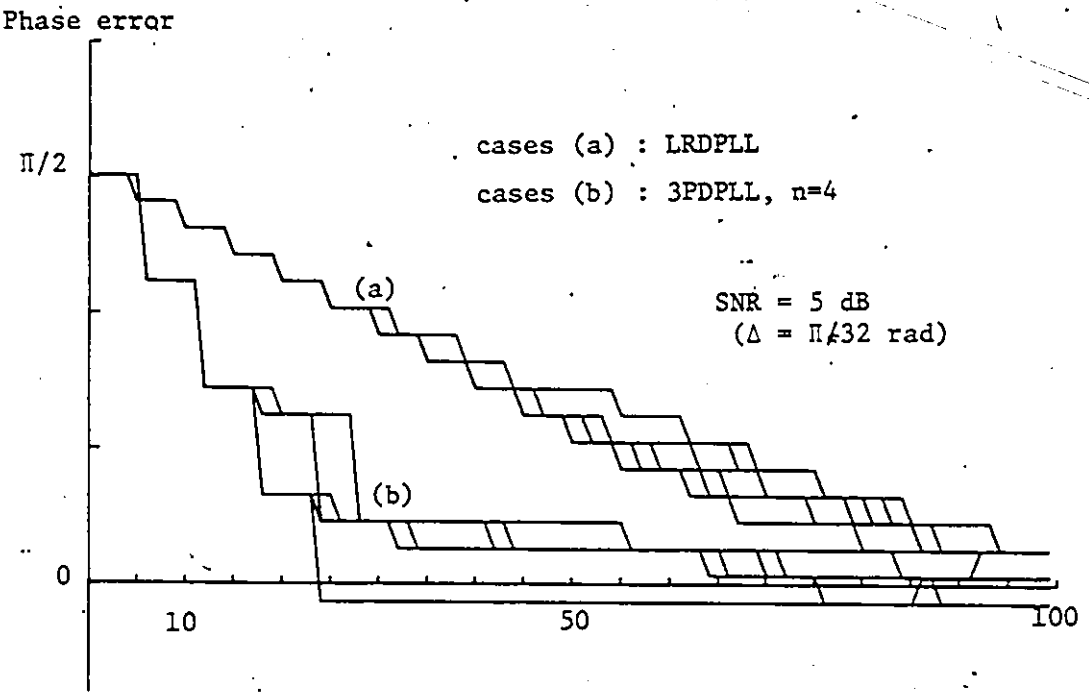


Figure 14: Example of acquisition (6 superposed runs)

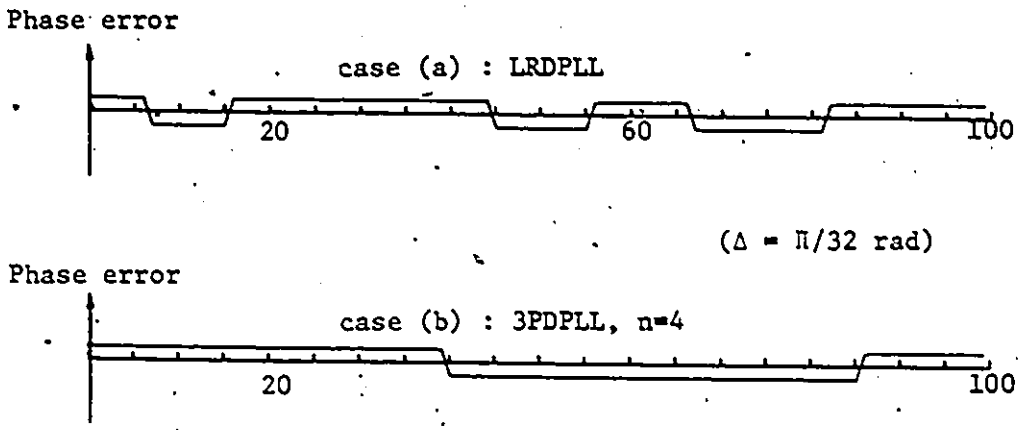


Figure 15: Example of tracking (one run)

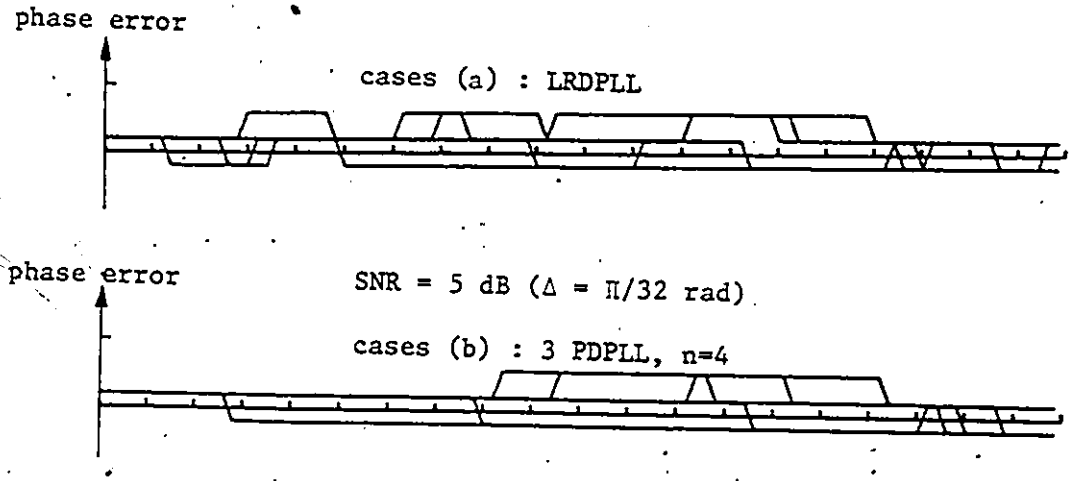


Figure 16: Example of tracking (6 superposed runs)

Chapter IV

THEORETICAL ANALYSIS OF THE 3PDPLL

4.1 INTRODUCTION

In order to numerically compute the RMS phase error and the mean acquisition time needed to choose the parameters of the 3PDPLL, the system has to be appropriately modeled so as to render the numerical computation feasible. Because of the finite number of phase error conditions (2m), a general state transition model made up of m stages (using the symmetry of the system) and a state transition model applicable to all the stages are used.

4.2 CHARACTERIZATION OF THE INPUT SIGNAL

The signal and the noise term of equation (2) can be written as :

$$s(t) = A \sin(W_o t + \theta_i(t)) \quad (8)$$

$$n(t) = n_s(t) \sin W_o t + n_c(t) \cos W_o t \quad (9)$$

The noise n(t) represents a narrowband Gaussian noise process of zero mean and of variance ($\sigma_n^2 = \overline{n_s^2(t)} = \overline{n_c^2(t)}$). $n_s(t)$ and $n_c(t)$ are Gaussian, independent and have identical power spectral density. If a rec-

tangular shaped noise bandpass spectrum of bandwidth B_n is assumed, the spectra of $n_s(t)$ and $n_c(t)$ are rectangular low-pass functions of bandwidth $B_n/2$. From (8) and (9), the signal to noise ratio at the input of the DPLL is:

$$SNR = A^2/2\sigma_n^2 \qquad (10)$$

The autocorrelation of both $n_s(t)$ and $n_c(t)$ thus can be written as :

$$R_{n_s}(\tau) = R_{n_c}(\tau) = \sigma_n^2 \sin(\pi B_n \tau)/\pi B_n \tau \qquad (11)$$

The sets of samples [A B C] are taken every k^{th} cycle of s(t) where k is chosen as the smallest positive integer for which $R_{n_s}(kT)$ approaches zero. This optimizes the overall loop performances (ie. (5) and (7)) and insures non-correlation between the outcomes of the sets.

The time T_s between the samples [A B C] of a given set represented by a phase shift $l \cdot \Delta$ must be small enough so that both $n_s(t)$ and $n_c(t)$ will approximately be constant during $2T_s$ (i.e. $R_{n_s}(T_s) \simeq R_{n_s}(0)$). The above assumptions can be stated as follows :

$$n_s(t_1) \simeq n_s(t_1 + T_s) \simeq n_s(t_1 - T_s) \qquad (12a)$$

$$n_s(t_1 + jkT) \simeq n_s(t_1 + jkT + T_s) \simeq n_s(t_1 + jkT - T_s) \qquad (12b)$$

and

$$n_s(t_1) \neq n_s(t_1 + jkT) \quad \text{(no correlation)} \qquad (13)$$

(similar equations can be defined for $n_c(t)$)

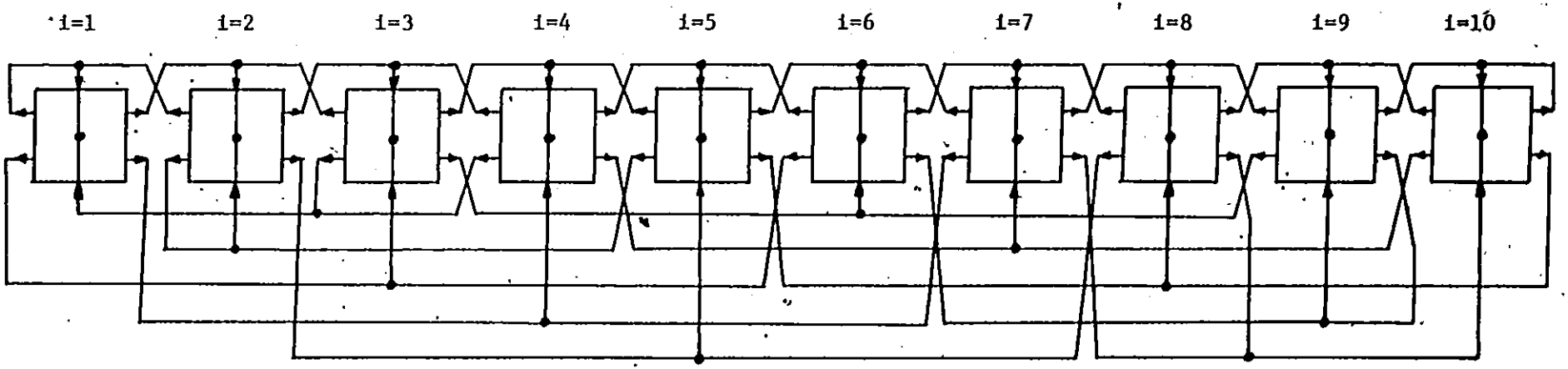
where j is an integer not equal to zero

These hypotheses are necessary to simplify the computation of the probabilities of the outcomes of A',B',C' entering into the calculation of the RMS phase error and the mean acquisition time.

4.3 3PDPLL MODELING

Due to the digital nature of the correction phase steps, there is a finite number of phase error conditions defined as the total number of unit phase step required to cover a complete cycle of the input signal. Therefore , there are 2m possible phase error conditions since phase errors differing by multiples of 2π are indistinguishable. Following [5], let the state of the closed-loop system be defined by the phase error that exists between the DPLL and the input signal and let these states (called stages) be indexed by i. Then the 3PDPLL can be modeled by the general state transition diagram depicted in Fig. 17 Only half of the 2m stages are considered due to the symmetry of the model.

The transitions between stages will either be to the nearest stage or to a farest one if the 3PDPLL is in 'Acquisition' or 'Tracking' mode respectively (as estimated by the decision block).

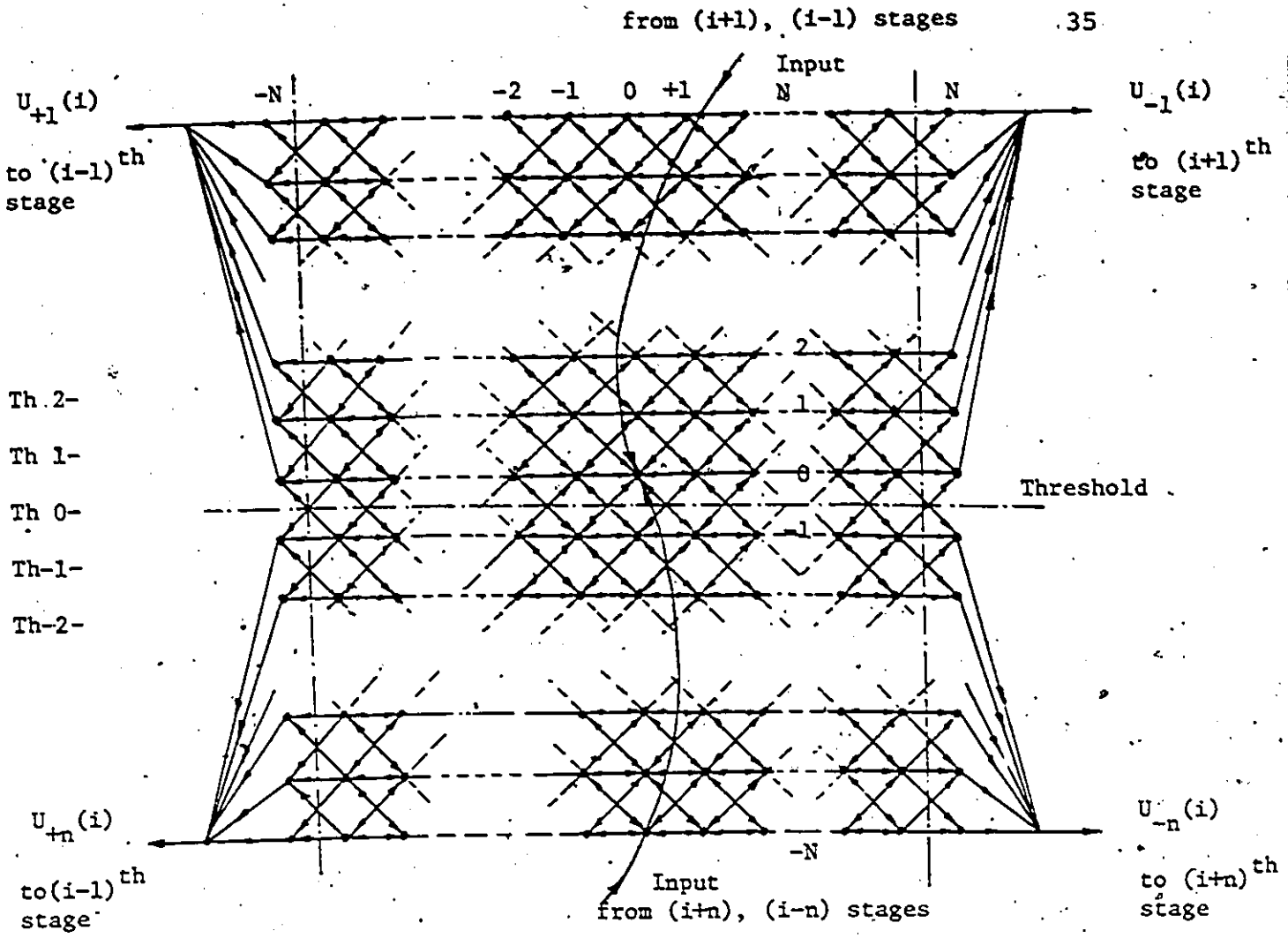


m = 10 , n = 3 $\Delta = \Pi/10$ rad. (18^{o})

Figure 17 : Example of a general state transition model

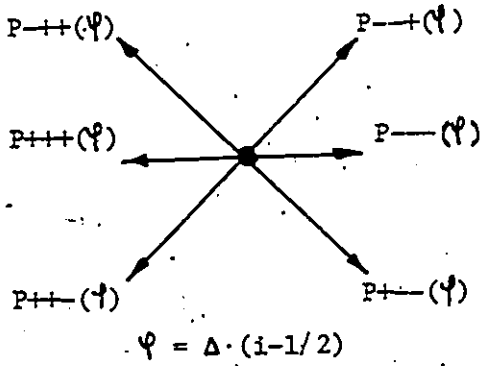
The model of the stages, as shown in Fig. 18, represent the state transition diagram of the combined random-walk filter (A'),adder (B'-C') and decision block (E ≷ Threshold).The propagation within a given stage i occurs according to the probabilities of the six outcomes of A',B',C' for the corresponding phase error. The termination (transition to another stage) happens when either the horizontal nodes '-N' or '+N' (0 and 2N of the random-walk filter) are reached. The threshold (decision block) defines whether a small or a large phase step correction is to be taken. In order to limit the vertical dimension of the state transition model of one stage, the adder is assumed to have its upper and lower limits to +N and -N respectively.

One of the simplest possible case of model of the state transition of one stage of the 3PDLL is presented in Fig. 19 (N=2 , Th=1).

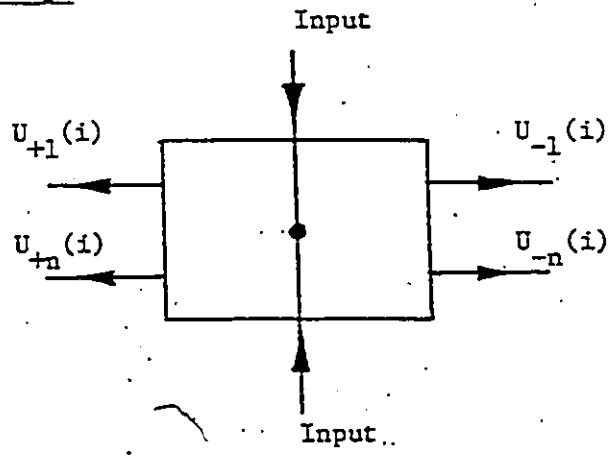


Note: ——● is equivalent to ⟷

i^{th} stage

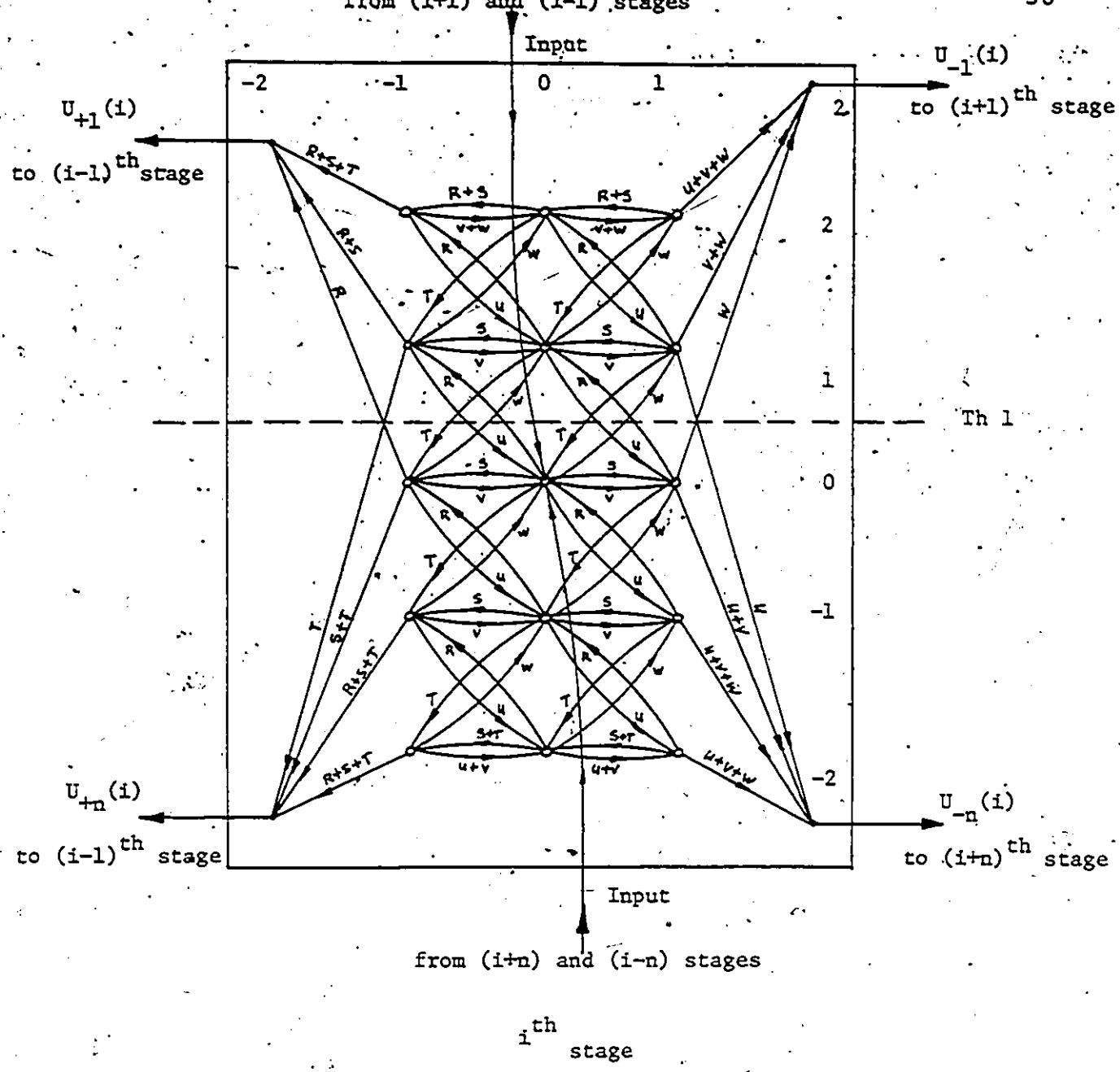


Possible transition for one non-boundary node



Simplified Representation of the i^{th} stage and its corresponding termination probabilities

Fig. 18- State transition model of one stage



$P_{--+}(\varphi) = R$ $\quad P_{---+}(\varphi) = W$

$P_{-++}(\varphi) = S$ $\quad P_{---}(\varphi) = V$

$P_{++-}(\varphi) = T$ $\quad P_{+--}(\varphi) = U$

Figure 19: Example of the state transition model of one stage (N=2, Th=1)

4.4 CALCULATION OF THE RMS PHASE ERROR

Following the procedure of Cessna and Levy [5], the calculation of the RMS phase error (Φ_{RMS}) is performed as follows

1 - Obtain the probabilities of the six possible outcomes of [A',B',C'] for all the different output phase errors.

2 - With 1, obtain the 4 termination probabilities for each stage using the model of Fig. 18

3 - Compute all the stage selection probabilities using the general model of Fig. 17

4 - Compute the average time spent in each stage.

5 - Using 3 and 4, compute the absolute state probabilities of each stage and finally the RMS phase error.

4.4.1 Probabilities of the six outcomes of A',B',C'

From the equations (11) to (13), it appears that for each set of samples, A,B and C are statistically dependent and the joint probabilities of occurrences of A',B'and C' , that are needed to compute the RMS phase error and the mean acquisition time, can be obtained for all possible phase errors by using the probability density function for a positive zero-crossing of a sine wave plus Gaussian noise $p_x(\Phi)$ in function of the phase-error Φ [8].

This probability density function can be written as :

$$p_x(\Phi)=(1/2\pi)\, e^{-S/N}\left[1+\sqrt{4\pi S/N}\cos\Phi\; e^{(S/N)\cos^2\Phi}\,\Omega(\sqrt{2S/N}\cos\Phi)\right] \quad (14)$$

where $\Omega(x)$ is the probability integral defined by :

$$\Omega(x) = (1/\sqrt{2\pi})\int_{-\infty}^{x} e^{-x^2/2}dx \quad (15)$$

and $$S/N = A^2/2\sigma_n^2$$

As illustrated by the cases of Fig.20, the six probabilities are obtained as follows :

Case (a)

$$P_{+++}(\varphi) = P(C'=+1,A'=+1,B'=+1) = \int_{\varphi+\ell\cdot\Delta-\pi}^{\varphi-\ell\Delta} p_x(\alpha)d\alpha \quad (16)$$

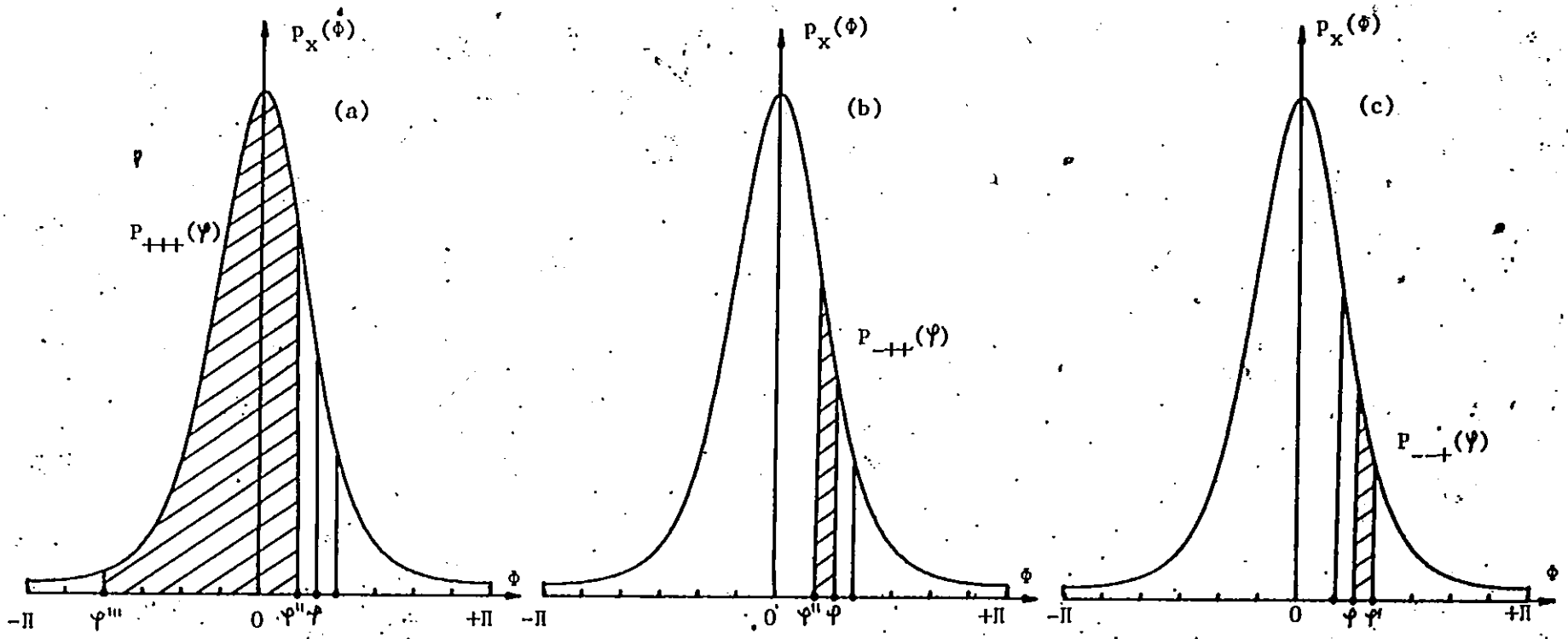
(probability that a positive transition occured in the interval $\varphi'''-\varphi''$)

Case (b)

$$P_{+++}(\varphi) = P(C'=-1,A'=+1,B'=+1) = \int_{\varphi-\ell\cdot\Delta}^{\varphi} p_x(\alpha)d\alpha \quad (17)$$

(probability that a positive transition occured in the interval $\varphi''-\varphi$)

SNR = 0 dB



$$(\varphi''' = \varphi + \ell\Delta - \Pi)$$

Figure 20 : Example of computation of the probabilities of the outcomes A'B'C'

Case (c)

$$P_{--+}(\varphi) = P(C'=-1, A'=-1, B'=+1) = \int_{\varphi}^{\varphi+\ell\Delta} p_x(\alpha)\,d\alpha \quad (18)$$

(probability that a positive transition occured in the interval φ-φ')

By analogy :

$$P_{---}(\varphi) = P(C'=-1, A'=-1, B'=-1) = P_{+++}(\varphi + \pi) \quad (19)$$

$$P_{+--}(\varphi) = P(C'=+1, A'=-1, B'=-1) = P_{-++}(\varphi + \pi) \quad (20)$$

$$P_{++-}(\varphi) = P(C'=+1, A'=+1, B'=-1) = P_{--+}(\varphi + \pi) \quad (21)$$

with $\varphi = \Delta\,(i-1/2)$

The solutions of the equations (16) to (21) can be carried out numerically. The integration of (15) is obtained from a very accurate polynomial* (within 10^{-7}) as follows :

$$\Omega(x) = \int_{-\infty}^{\infty} z(x)\,dx = \begin{cases} 1 - Q\,, & x > 0 \\ Q\,, & x < 0 \end{cases} \qquad z(x) = (1/\sqrt{2\pi})\, e^{-x^2/2}$$

$$Q = z(x)\,T\,((((\,1.330274\,T - 1.821256\,)\,T + 1.781478\,)\,T - .03565638\,)\,T + .3193815\,) \quad (22)$$

where $T = 1/(1 + .2316419\,|x|\,)$

---

* From the Gram-Charlier expansion, the derivation can be found in ''An Introduction to Statistical Communication Theory'' by John B. Thomas, Wiley 1969.

The probability density function $p_x(\Phi)$ is then evaluated for a series of Φ's equally spaced between $-\Pi$ to $+\Pi$ in order to apply Simpson rule to performe the numerical integration of the probabilities of the six outcomes of A'B'C'.

4.4.2 Termination Probabilities (Fig. 18)

A threshold (Th) must be first chosen so as to determine whether a small or a large phase correction is to be taken. The optimum position of this threshold is found not to be critical if set within the bounds used in the next chapter to suit a large variety of signal-to-noise ratio. For the proper operation of the DPLL in the two modes, we can deduce (using Fig.18) that the value of Th must be larger than zero for high SNR and smaller than N-1 for low SNR. Due to the complexity of the model, the termination probabilities $U_{-1}(i)$, $U_{-n}(i)$, $U_{+1}(i)$ and $U_{+n}(i)$ are numerically obtained by setting the input with probability 1 (every other nodes being set to zero), starting the propagation and letting it continue until the model is practically cleared. The outputs accumulated at the four exits points will approximate the termination probabilities. The dimensions of this stage are parameters that can be chosen within the limits imposed by hardware considerations so as to obtain the desired performance.

4.4.3 State Selection Probabilities (Fig. 17)

The probabilities of stage selection L(i) given that a stage transition is occurring are given in terms of the termination probabilities by :

$$L(i) = U_{-1}(i_{-1})\, L(i_{-1}) + U_{-n}(i_{-n})\, L(i_{-n}) + U_{+1}(i_{+1})\, L(i_{+1}) + U_{+n}(i_{+n})\, L(i_{+n}) \qquad (23)$$

Since only half of the 2m possible phase-error values are to be considered due to the symmetry and taken into account the reflections at the two ends of the model, the subscripted i's are defined as follows :

$$i_{-1} = \begin{cases} i-1 & \text{if } i-1 \geqslant 1 \\ 1 & \text{if } i-1 < 1 \end{cases} \qquad (24a)$$

$$i_{-n} = \begin{cases} i-n & \text{if } i-n \geqslant 1 \\ n-i+1 & \text{if } i-n < 1 \end{cases} \qquad (24b)$$

$$i_{+1} = \begin{cases} i+1 & \text{if } i+1 \leqslant m \\ m & \text{if } i+1 > m \end{cases} \qquad (24c)$$

$$i_{+n} = \begin{cases} i+n & \text{if } i+n \leqslant m \\ 2m+1-(i+n) & \text{if } i+n > m \end{cases} \qquad (24d)$$

$$i = 1,2,3.....m$$

The nontrivial solutions to (23) subject to (24) must also satisfy the constraint :

$$\sum_{i=1}^{m} L(i) = 1 \qquad (25)$$

Because of its properties, a numerical solution for the state equations can be found by first assigning an equal state probability of 1/m to all the L(i)'s and by applying the Gauss-Seidel iteration method [10].

The absolute state probalities P(i) can be related to these state selection probalities L(i) through the expected state duration time T(i). The equations describing these expected time are well known [9] and can be readily applied since our model of the stages is equivalent to a random-walk filter as far as T(i) is concerned. Termination will occur at one of the four exit points on the average in a time given by :

$$T(i) = N \quad \text{for} \quad U_a(i) = U_b(i) = 0.5$$

or (26)

$$T(i) = \frac{N}{U_a(i)-U_b(i)} - \frac{2N}{(U_a(i)-U_b(i))[1+(U_a(i)/U_b(i))^N]}$$

for $U_a(i) \neq U_b(i)$; with $U_a(i) = U_{+1}(i) + U_{+n}(i)$

$U_b(i) = U_{-1}(i) + U_{-n}(i)$ and $U_a(i) + U_b(i) = 1$

Then, P(i) is the ratio of the time spent in state i to that spent in all states :

$$P(i) = \frac{L(i)T(i)}{\sum_{j=1}^{m} L(j)T(j)} \qquad (27)$$

Finally, the RMS phase error is obtained as :

$$\phi_{RMS} = \sqrt{\sum_{i=1}^{m} (\pi\, i/m)^2\, P(i)} \qquad (28)$$

4.5 TRANSIENT RESPONSE

The mean acquisition time T_m is defined as the average time taken by the binary digital loop to reach the minimum possible value of phase error assuming equally likely probabilities of initial phase errors. $T_o(i)$ is defined as the mean number of set of samples taken by the binary loop to reach the minimum possible value of phase error with the initial phase error (i) given. It is shown [5] that $T_o(i)$ is given in terms of the state transition probabilities and state duration times by the following difference equation :

$$T_0(i) = T(i) + U_{+1}(i)\, T_0(i_{-1}) + U_{+n}(i)\, T_0(i_{-n}) + U_{-1}(i)\, T_0(i_{+1}) + U_{-n}(i)\, T_0(i_{+n}) \qquad (29)$$

The subscripted i's are defined in equation (24) with the exception of i_{-n} (24c) that is replaced by :

$$i_{-n} = \begin{cases} i-n & \text{for } i-n \geq 1 \\ 1 & \text{for } i-n < 1 \end{cases} \qquad (30)$$

$$i = 1,2,3.....m$$

Finally, the mean acquisition time T_m is obtained as :

$$T_m = (kT/m) \sum_{i=1}^{m} T_0(i) \qquad (31)$$

A numerical solution to (29) subject to (24) and (30) can be found by assigning an initial value to the $T_0(i)$'s as shown in (32) followed by applying the Gauss-Seidel iteration method [10].

$$T_0(1) = 0 \ , \ T_{0_{initial}}(2) = T(2)$$

$$T_{0_{initial}}(i) = T_{0_{initial}}(i-1) + T(i)/n \quad , \ 2 < i < m+1 \qquad (32)$$

4.6 EXAMPLE OF NUMERICAL COMPUTATION

A complete example of a numerical computation is carried out for both the 3PDPLL and the LRDPLL for a SNR of 5dB. All the numerical results of the intermediate steps introduced in the previous sections are successively presented in the form of tables and plots.

The plot of the correction size versus phase error shows the effect of the noise when compared against a noiseless case. For a slight increase (6 %) of the RMS phase error, the 3PDPLL mean acquisition time is reduced by a factor 2 over the LRDPLL's. This is confirmed by the plot of both the absolute state probabilities P(i) and the acquisition time $T_o(i)$ in function of the phase error.

The values of the parameters of the example presented are:

$m = 32$ $\quad \ell = 5$ $\quad Th = 1$ $\quad N = 2$

$n = 3$ (3PDPLL) $\quad n = 1$ (LRDPLL)

SNR = 5 dB

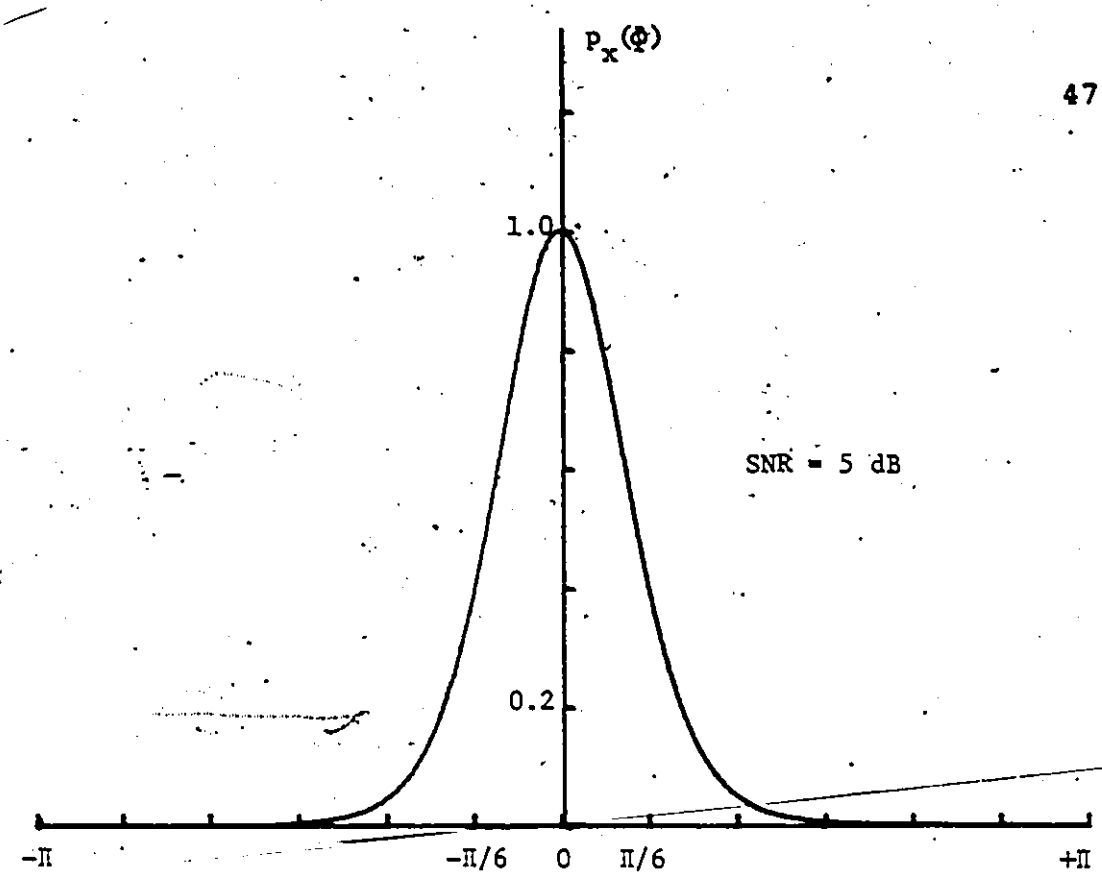


Figure 21: P.d.f. of a positive zero crossing

TABLE 2

Probabilities of the six outcomes of A'B'C'

P_{--+}	P_{-++}	P_{+++}	P_{++-}	P_{+--}	P_{---}	i
0.353	0.408	0.140	0.000	0.000	0.097	1
0.168	0.446	0.355	0.001	0.000	0.030	4
0.056	0.289	0.643	0.001	0.000	0.010	7
0.017	0.120	0.857	0.001	0.001	0.005	10
0.005	0.038	0.951	0.003	0.001	0.003	13
0.002	0.011	0.975	0.008	0.002	0.002	16
0.001	0.004	0.964	0.025	0.004	0.003	19
0.001	0.002	0.900	0.083	0.011	0.004	22
0.000	0.001	0.728	0.225	0.038	0.008	25
0.000	0.001	0.450	0.408	0.120	0.021	28
0.000	0.000	0.198	0.446	0.289	0.066	31

TABLE 3

Termination probabilities, G(i) and T(i)

$U_{+1}(i)$	$U_{+n}(i)$	$U_{-1}(i)$	$U_{-n}(i)$	G (i)	T (i)	i
0.576	0.021	0.392	0.010	1.062	3.96	1
0.803	0.075	0.119	0.002	1.154	3.30	3
0.765	0.208	0.026	0.001	1.418	2.64	5
0.574	0.421	0.005	0.000	1.842	2.29	7
0.350	0.649	0.001	0.000	2.298	2.13	9
0.179	0.820	0.000	0.000	2.640	2.06	11
0.084	0.916	0.000	0.000	2.832	2.04	13
0.038	0.962	0.000	0.000	2.924	2.03	15
0.018	0.982	0.000	0.000	2.964	2.02	17
0.009	0.990	0.000	0.000	2.980	2.03	19
0.005	0.994	0.000	0.000	2.988	2.05	21
0.003	0.996	0.000	0.000	2.992	2.09	23
0.002	0.995	0.000	0.002	2.994	2.19	25
0.001	0.986	0.000	0.012	2.996	2.43	27
0.000	0.942	0.000	0.058	3.000	2.93	29
0.000	0.765	0.000	0.235	3.000	3.70	31

where $G(i) = U_{-1}(i) + U_{+1}(i) + n\,[U_{-n}(i) + U_{+n}(i)]$ is the average number of unit phase step correction

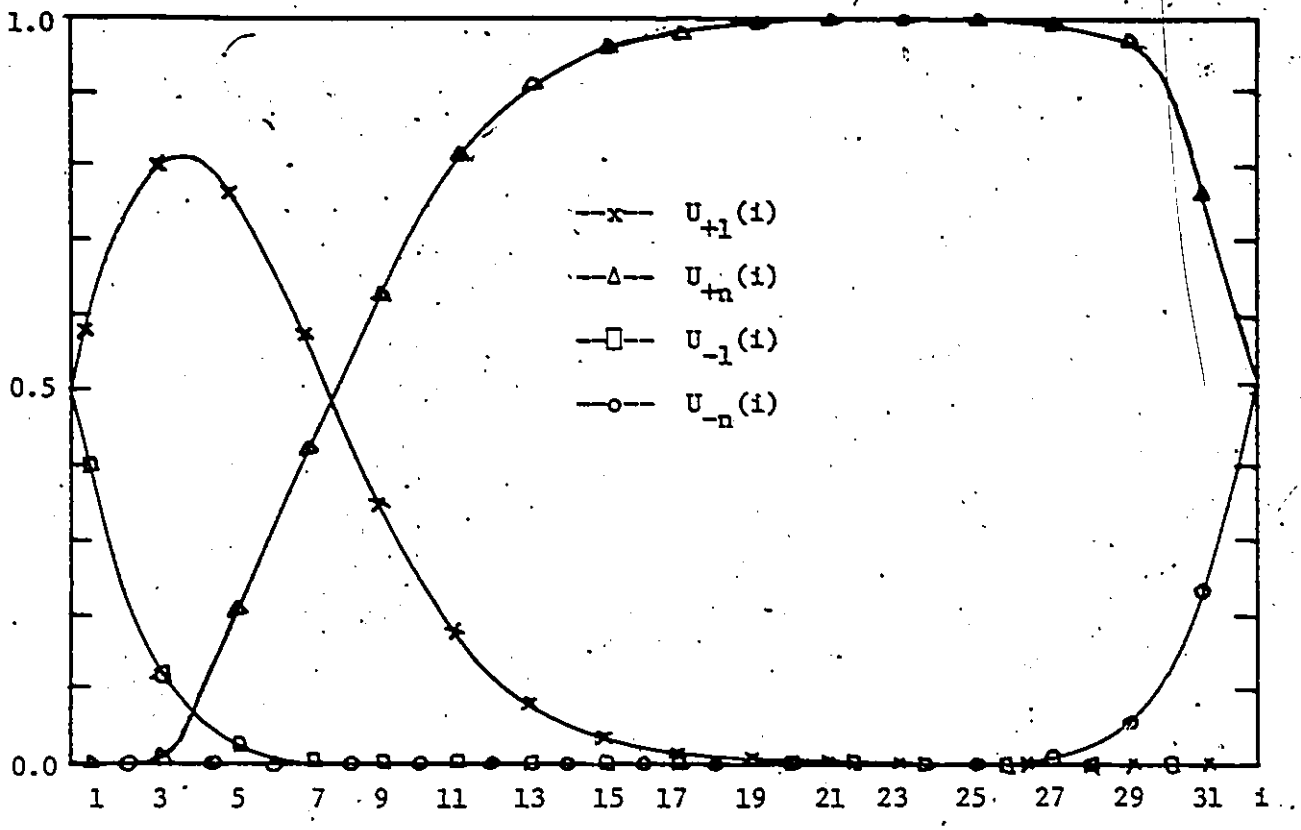


Figure 22: Termination probabilities in function of the phase error

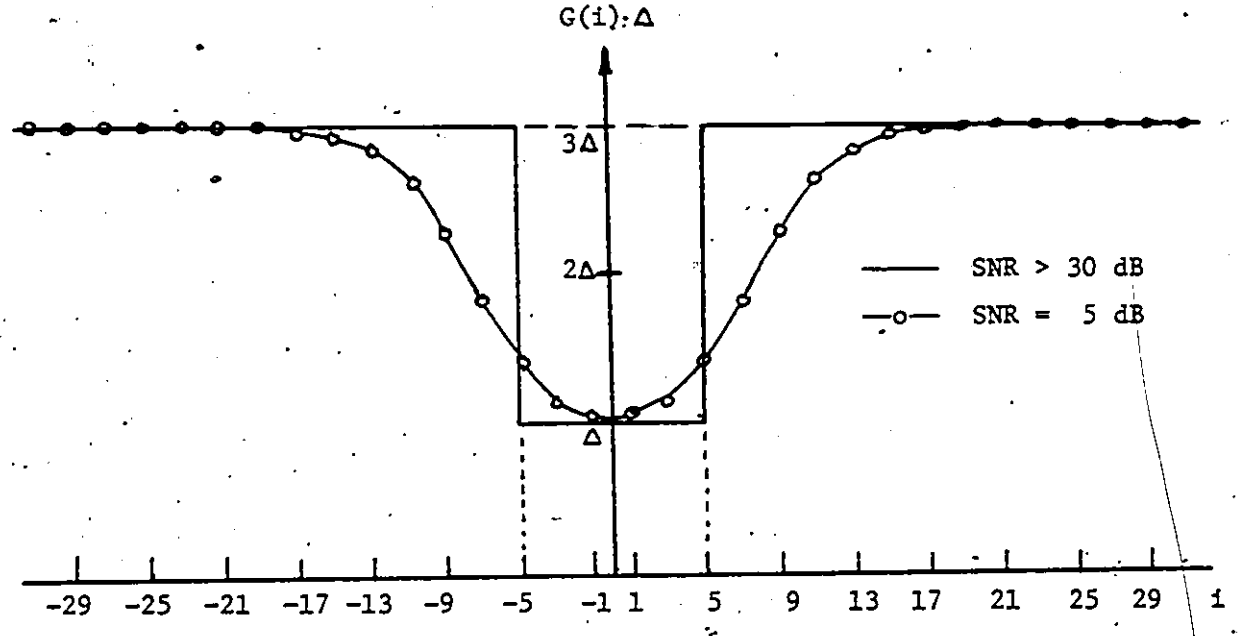


Figure 23: Correction size in function of the phase error

TABLE 4

Selection probabilities L(i) and absolute probabilities P(i)

i		-1,+1	-2,+2	-3,+3	-4,+4	-5,+5
L(i)	3PDPLL	0.281	0.157	0.050	0.010	0.002
L(i)	LRDPLL	0.315	0.142	0.038	0.005	0.000
P(i)	3PDPLL	0.294	0.154	0.044	0.007	0.001
P(i)	LRDPLL	0.308	0.151	0.036	0.004	0.001

RMS phase error

$\Phi_{RMS} = 7.16^{\circ}$ 3PDPLL

$\Phi_{RMS} = 6.71^{\circ}$ LRDPLL

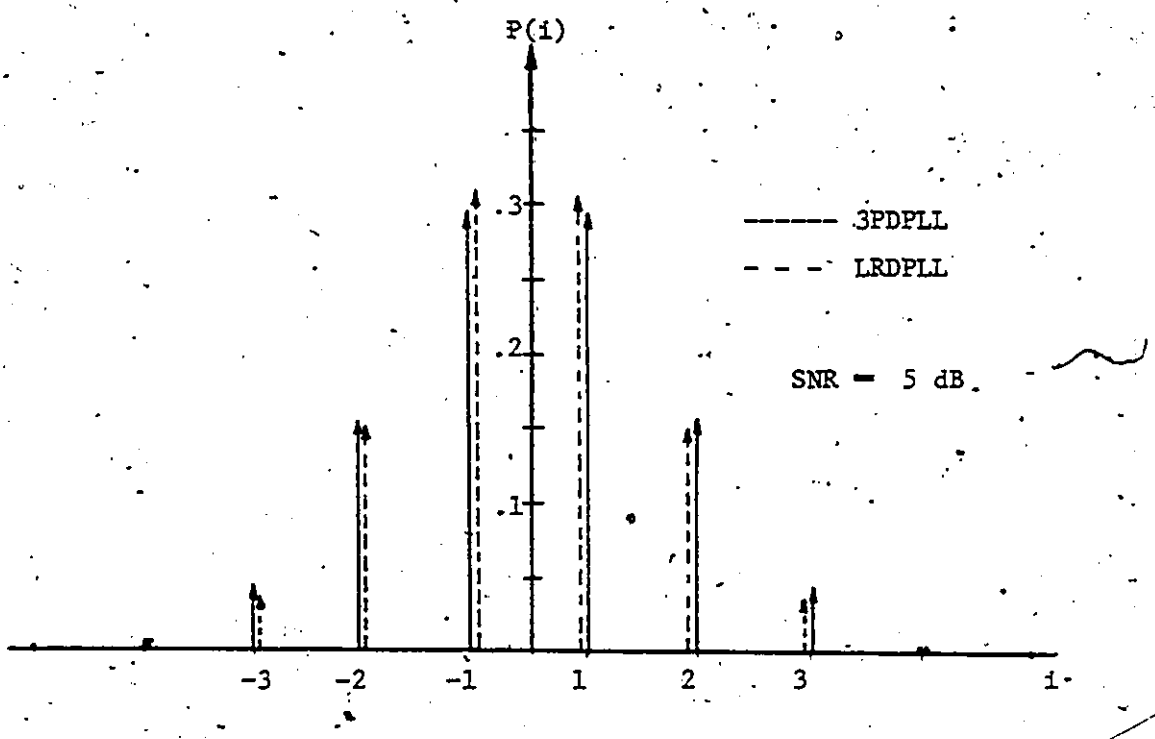


Figure 24: Absolute probabilities in function of the phase error

TABLE 5

Number of set of samples in function of the initial phase error

i	2	5	8	11	14	17	20	23	26	29	32
$T_o(i)$ 3PDPLL	5	12	16	18	20	22	24	26	29	32	37
$T_o(i)$ LRDPLL	6	16	23	29	35	41	47	53	60	69	86

Mean acquisition time

T_m = 21.9 kT 3PDPLL

T_m = 41.2 kT LRDPLL

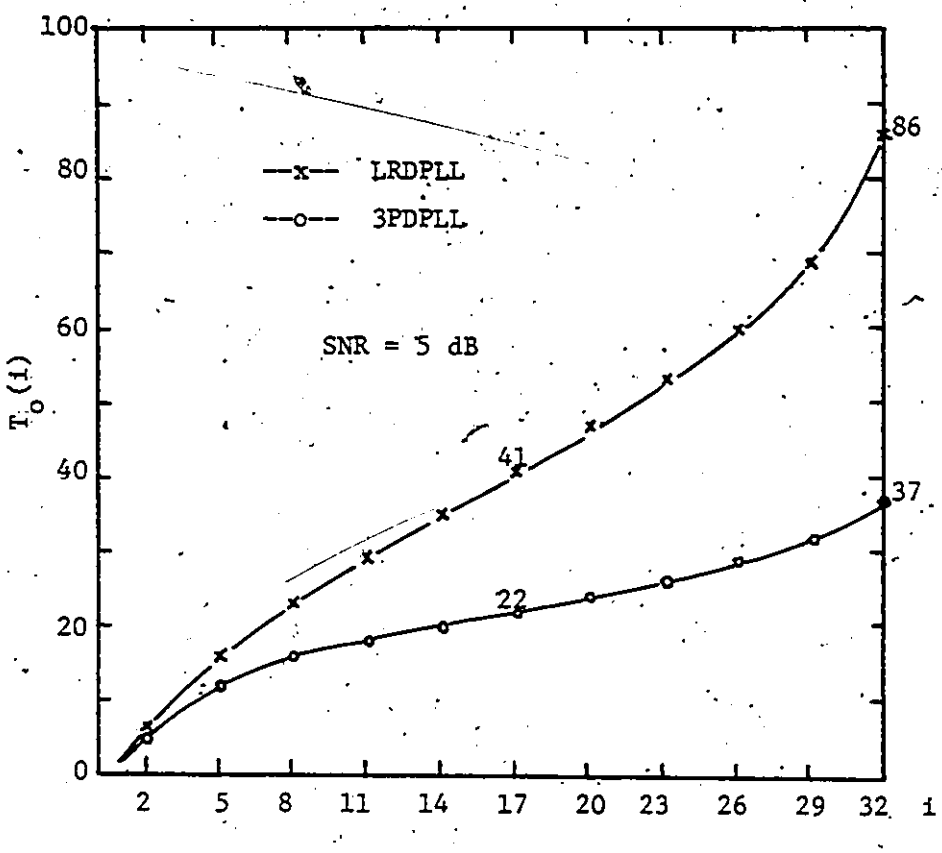


Figure 25: Number of set of samples in function of the phase error

Chapter V

NUMERICAL RESULTS

5.1 INTRODUCTION

Since no closed-form solution can be found for either the RMS phase error or the mean acquisition time, the various parameters of the 3PDPLL are individually tested in order to evaluate their respective effects upon the loop performance.

A series of plots relating the RMS phase error and the mean acquisition time to the signal-to-noise ratio at the input of the loop (10) are presented. The effects of the variations of the ratio 'n' of the step sizes (Fig. 26 and Fig. 27), the random-walk filter length 'N' (Fig. 28 and Fig. 29), the values of the threshold 'Th' (Fig. 30 and Fig. 31) and the distance 'ℓ' between the three samples (Fig. 32 and Fig. 33) are shown consecutively .In order to easily picture the differences between these results, a new digital loop ''Performance Criterion'' measure is introduced.

5.2 RESULTS

Table 6 gives the values of the parameters of the 3PDPLL for the four series of tests carried out.

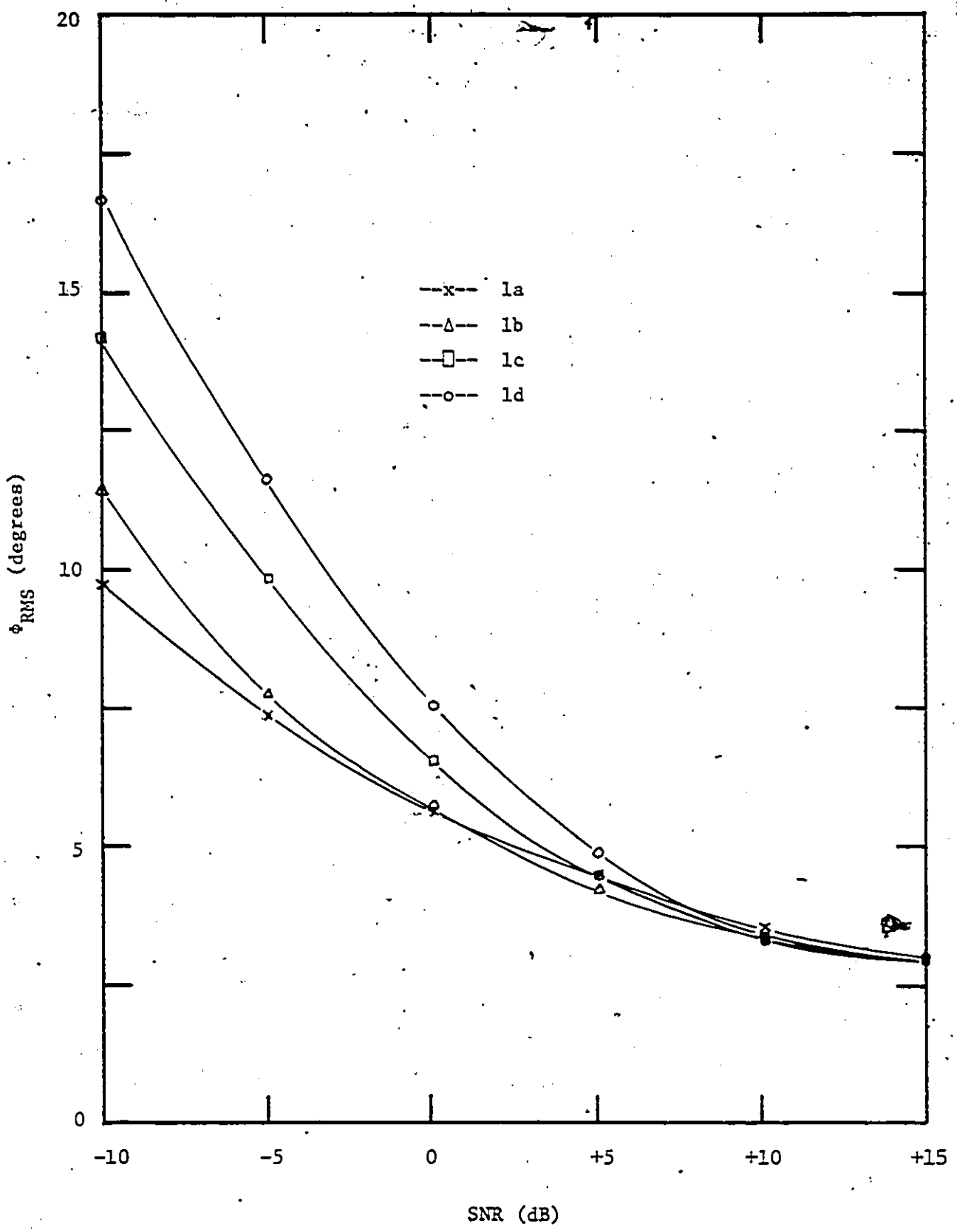
From Fig. 26 and Fig. 27 (test 1), in cases a and b the RMS phase error is approximately the same for a SNR of -5dB and up; but the corresponding acquisition times are decreased by about 20 to 30% for the 3PDPLL. Cases c and d provide up to 60% improvement in acquisition time over the range of SNR's above +5dB for nearly equally good noise rejection performances. The same observations can be made from the three other sets of tests where similar improvements are also achieved. Moreover, for SNR's above 10 dB, reductions of the acquisition time by factors 2 to 3 can easily be achieved for equal RMS phase error.

By varying the adjustable parameters, the user is provided with means of adapting the performance to some desired values (whether locally or over a wide range).

TABLE 6

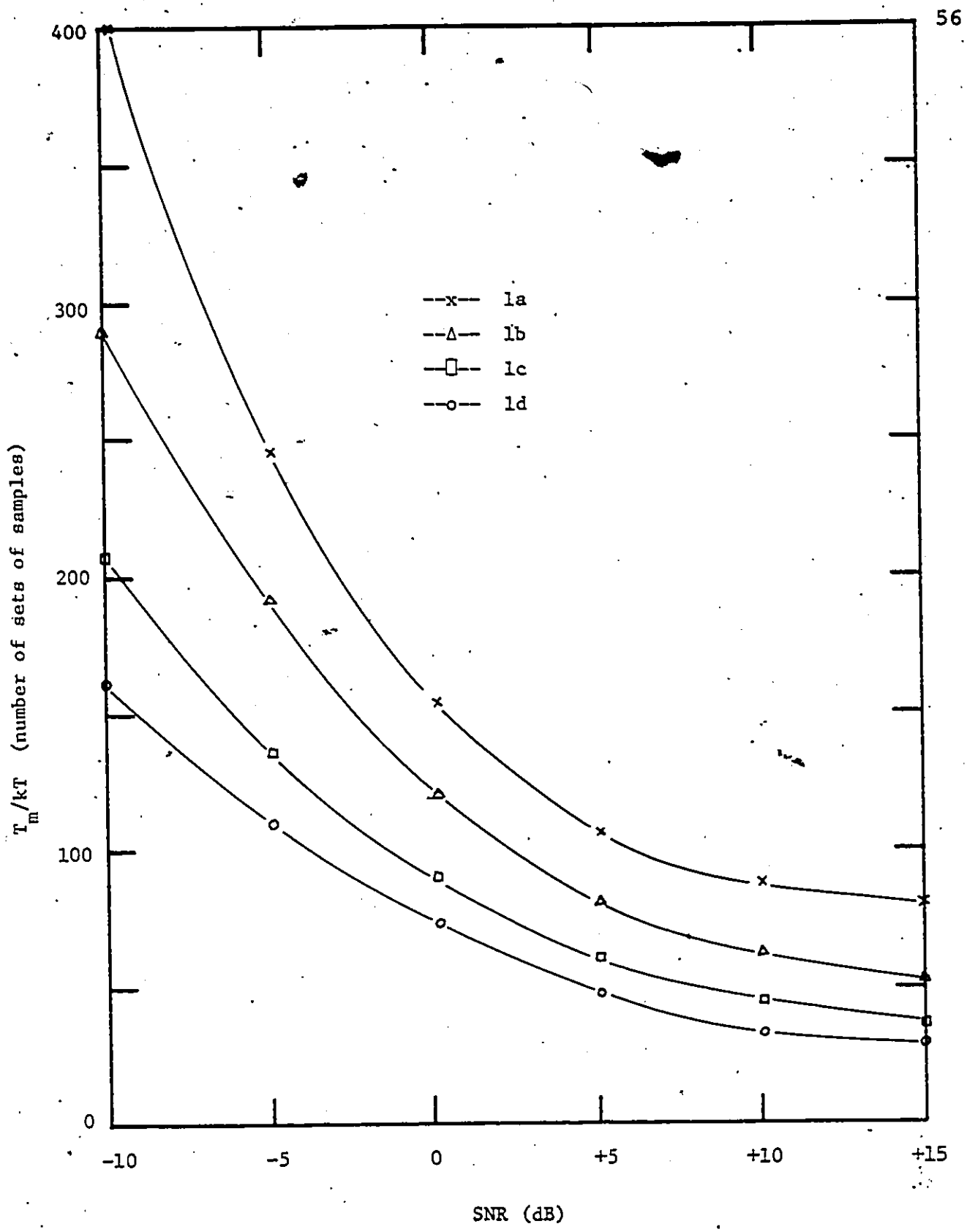
Values of the parameters of the four tests

Test		ℓ	n	N	Th	DPLL	
1	a	/	/	5	/	LRDPLL	Fig.26
1	b	2	2	6	2		and
1	c	2	3	6	2	3PDPLL	Fig.27
1	d	2	4	6	2		
2	a	/	/	5	/	LRDPLL	
2	b	2	3	6	1		Fig.28
2	c	2	3	5	1	3PDPLL	and
2	d	2	3	4	1		Fig.29
2	e	2	3	3	1		
3	a	/	/	3	/	LRDPLL	
3	b	3	3	4	1		Fig.30
3	c	3	3	4	2	3PDPLL	and
3	d	3	3	4	3		Fig.31
3	e	3	3	4	4		
4	a	/	/	2	/	LRDPLL	
4	b	5	3	3	1		Fig.32
4	c	4	3	3	1	3PDPLL	and
4	d	3	3	3	1		Fig.33
4	e	2	3	3	1		



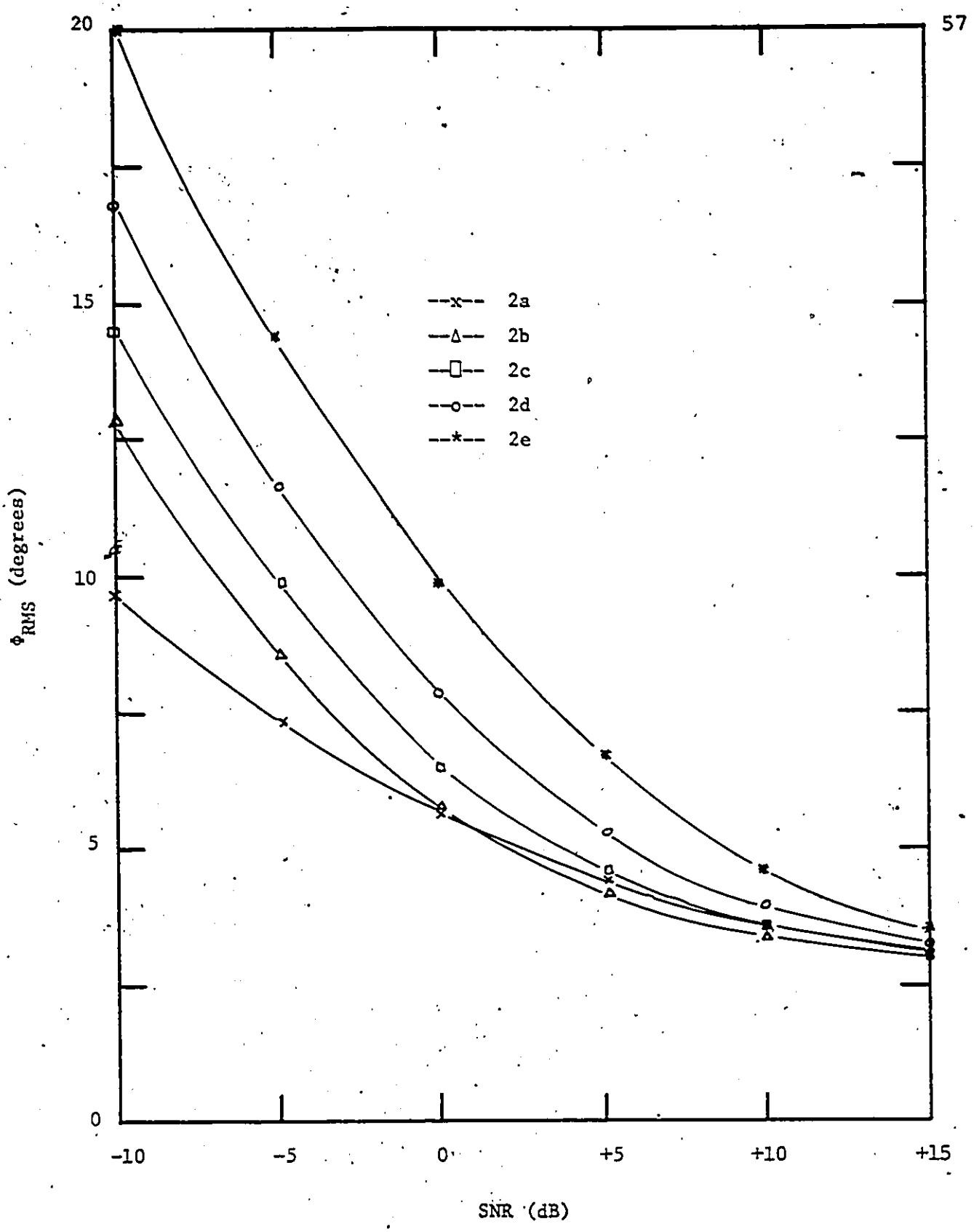
Variable parameter : n

Figure 26: Loop RMS phase error versus SNR



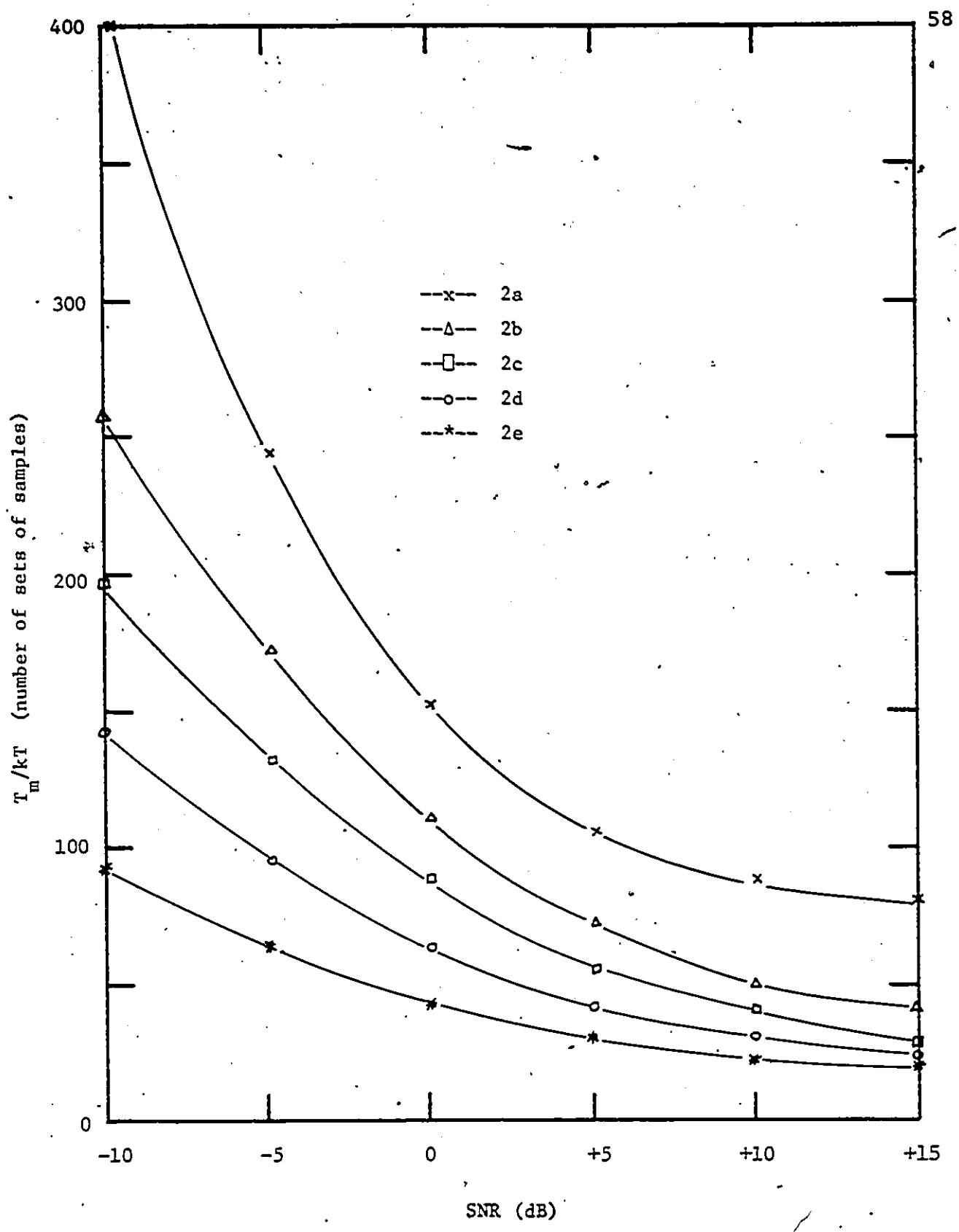
Variable parameter : n

Figure 27: Mean acquisition time versus SNR



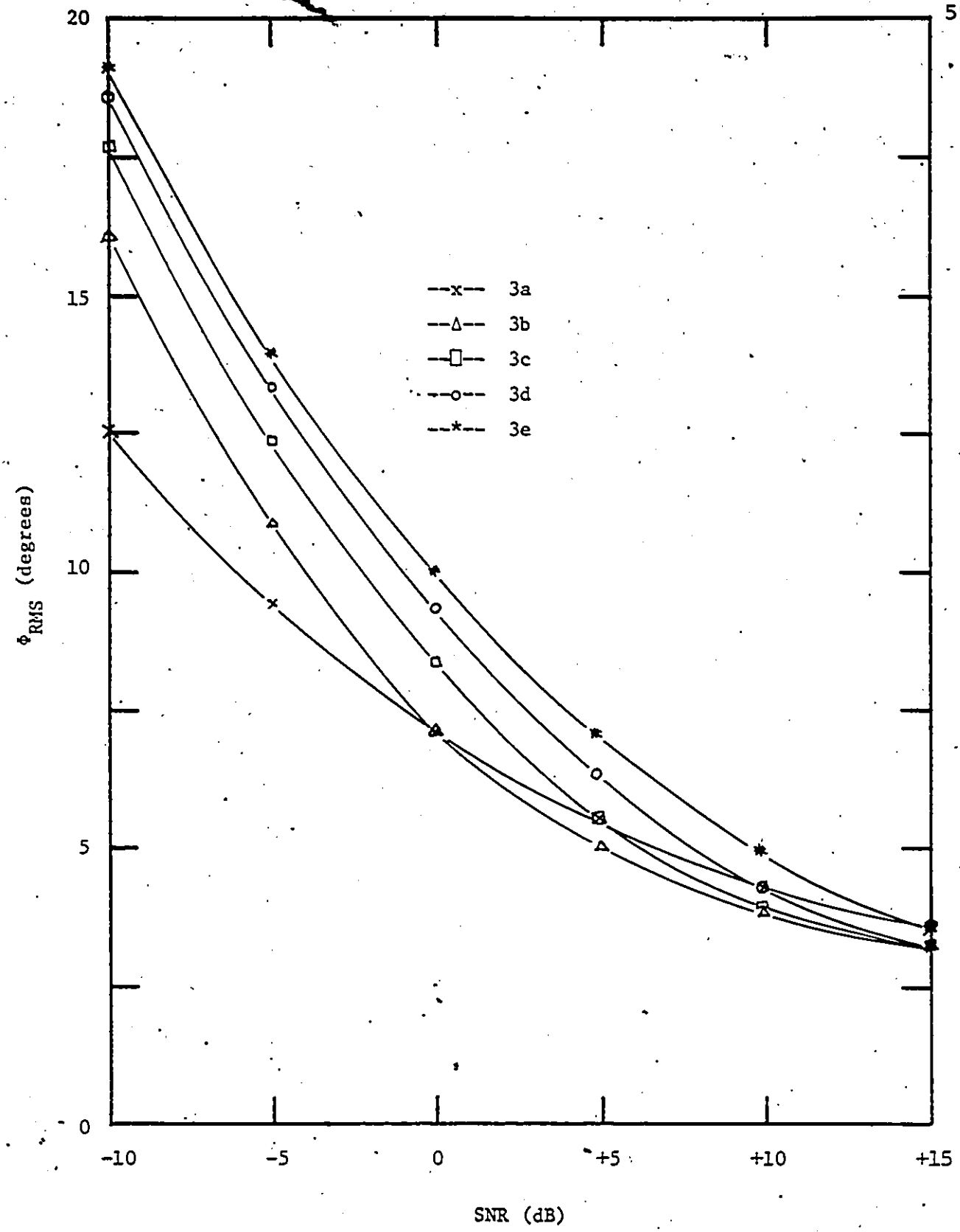
Variable parameter : N

Figure 28: Loop RMS phase error versus SNR



Variable parameter : N

Figure 29: Mean acquisition time versus SNR



Variable parameter : Th

Figure 30: Loop RMS phase error versus SNR

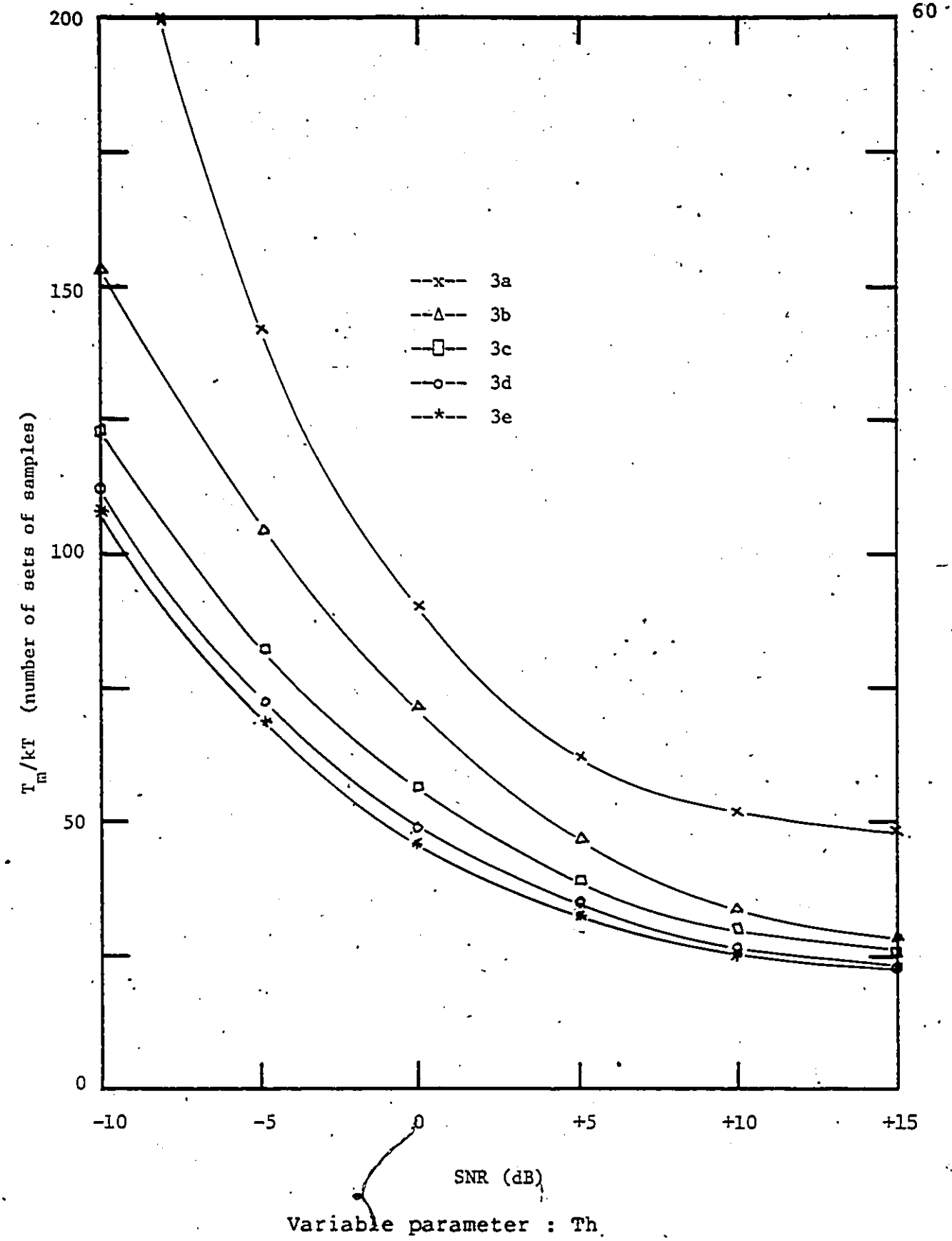
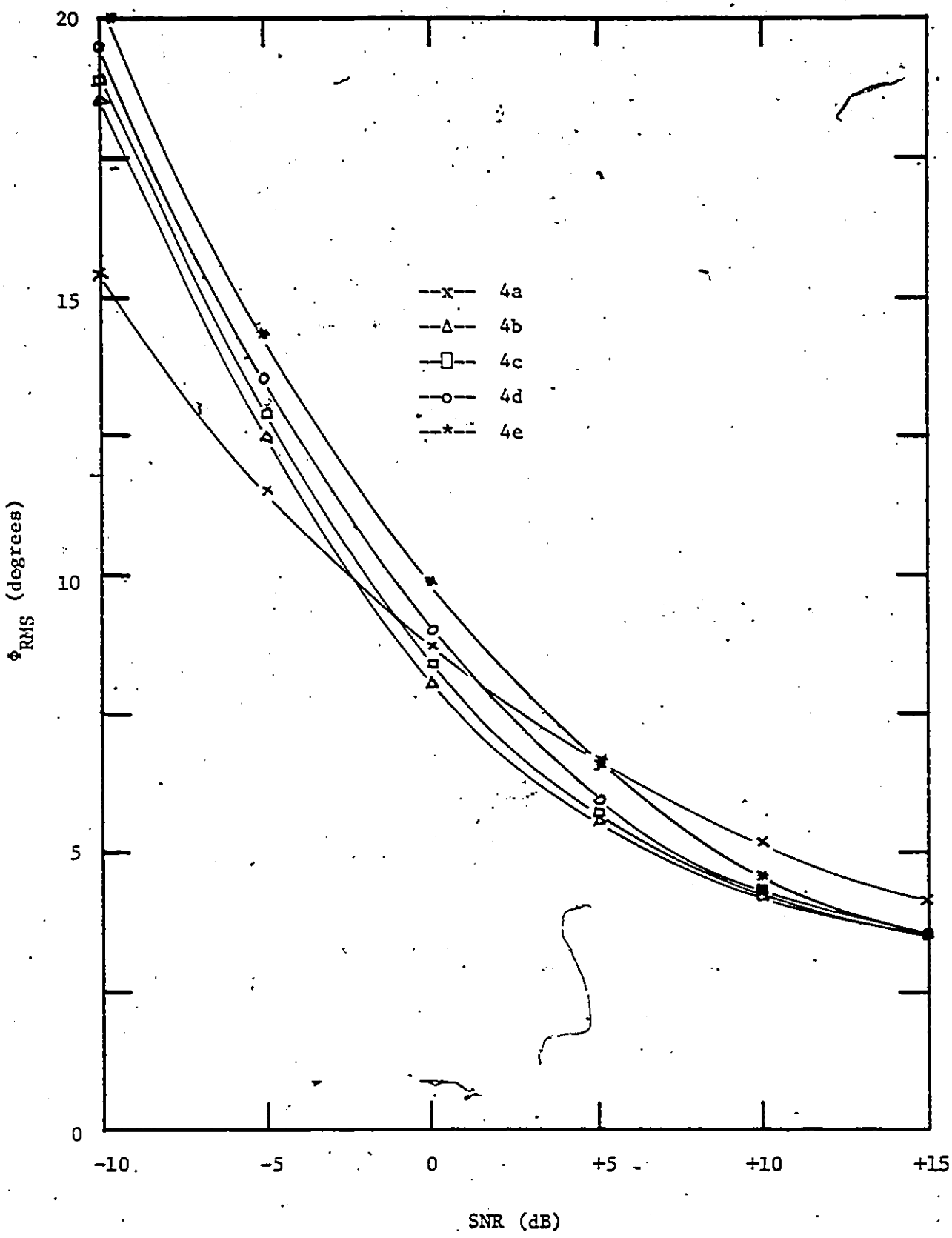
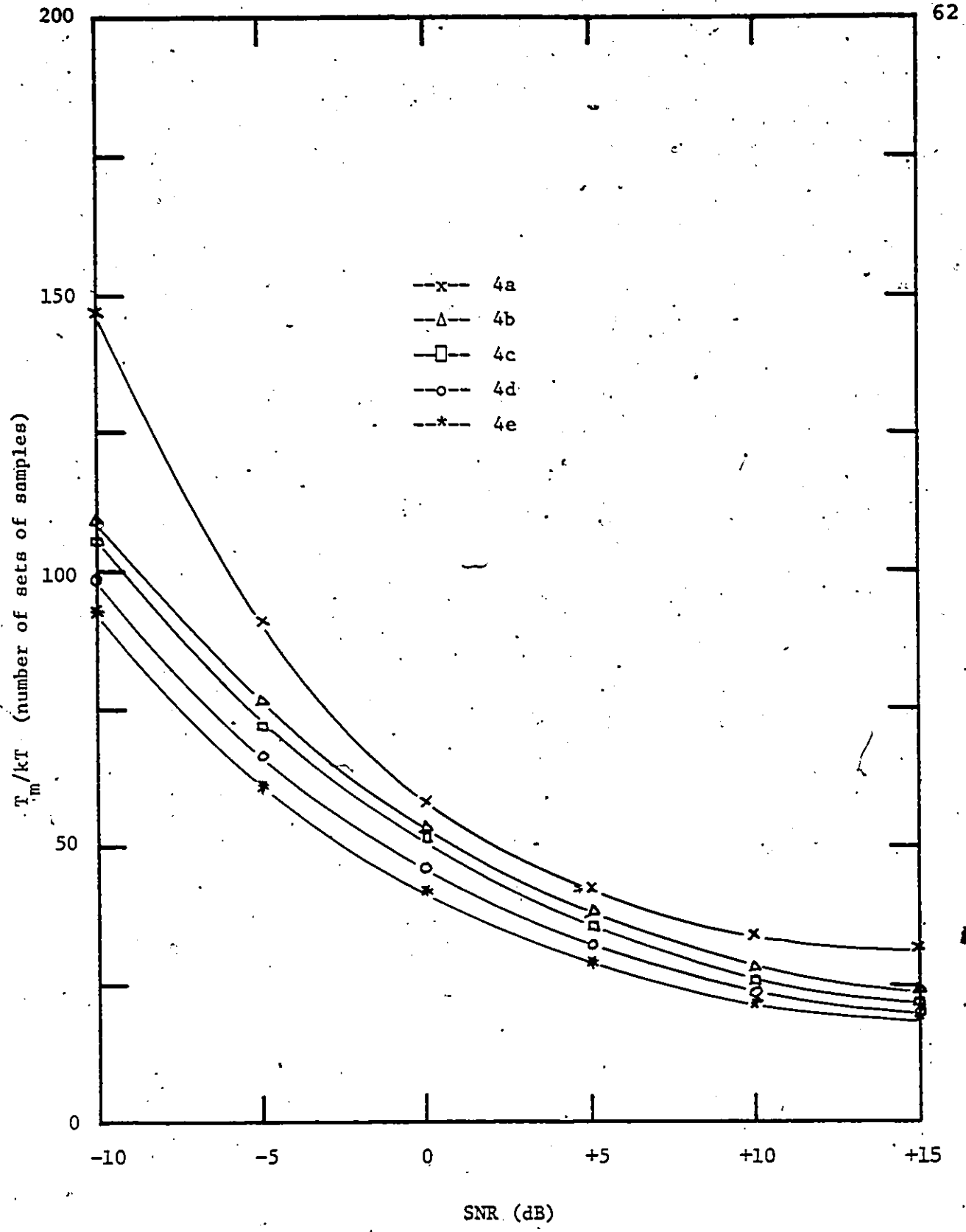


Figure 31: Mean acquisition time versus SNR



Variable parameter : ℓ

Figure 32: Loop RMS phase error versus SNR



Variable parameter : ℓ

Figure 33: Mean acquisition time versus SNR

5.3 . PERFORMANCE COMPARISON

In order to help the designer in his choice of DPLL systems, meaningful criteria need to be used to make comparisons among the digital loops and also compare with an analog loop. One criterion has already been proposed by Cessna and Levy [5] and will be presented here as well as in a modified form. This criterion relates the RMS phase error to the signal-to-noise ratio in a given loop with noise bandwidth B_L. For an analog PLL, linear analysis [11] yields :

$$\Phi_{RMS} = \sqrt{\frac{N_o B_L}{P_s}} \quad \text{(rad)} \tag{33}$$

where

P_S : is the signal power

$N_o = \sigma_n^2 / B_n$: is the one-sided noise power spectral density at the input of the PLL (34)

B_L : is the loop noise bandwidth

The DPLL being inherently non-linear, its loop bandwidth B' is a function of the SNR and thus cannot easily be defined from the loop parameters. The ''Quasi-bandwidth'' measure mentioned in [5] is based on the fact that B' can be approximated by the inverse of the mean time for the loop to traverse a reference angular phase step displacement of $\pi/4$. That is :

$$B' = 1/kT\ T_o\ (m/4) \tag{35}$$

The RMS phase error for the analog PLL and the 3PDPLL and LRDPLL is compared against signal-to-noise ratio in the loop bandwidth B_L or B' in Fig. 34 (for test 1).

As expected, for $P_S / N_o \cdot B'$ ratios higher than 20dB, the 3PDPLL outperforms the non-modified DPLL thus allowing more noise at its input for the same RMS phase error.

From (10),(33) -(35), a ''Performance criterion'' measure $Q(A^2/2\sigma_n^2)$ is defined :

$$Q(A^2/2\sigma_n^2) = \phi_{RMS}\,(A^2/2\sigma_n^2)\,\sqrt{T_m(A^2/2\sigma_n^2) / kT} \qquad (36)$$

The best performance is obtained for the smallest Q value for a given SNR, when the designer tries to minimize both the RMS phase error and the mean acquisition time. Using the numerical results of the four tests of the previous section, the performance criterion for the LRDPLL and the 3PDPLL are compared with that of the linear analog model against signal-to-noise ratio in Fig.35

It is significant to note that for low signal-to-noise ratio (less than -5dB), all the curves have roughly the same slope no matter what the values of the 3PDPLL parameters are. For higher signal-to-noise ratio, the 3PDPLL outperforms the LRDPLL and substantially reduces the difference in performance favoring the analog loop.

An absolute comparison between the digital loops and the linear analog loop can only be made roughly because of the lack of direct correspondence between the respective loop bandwidths B' (as defined by equation (35)) and B_L.

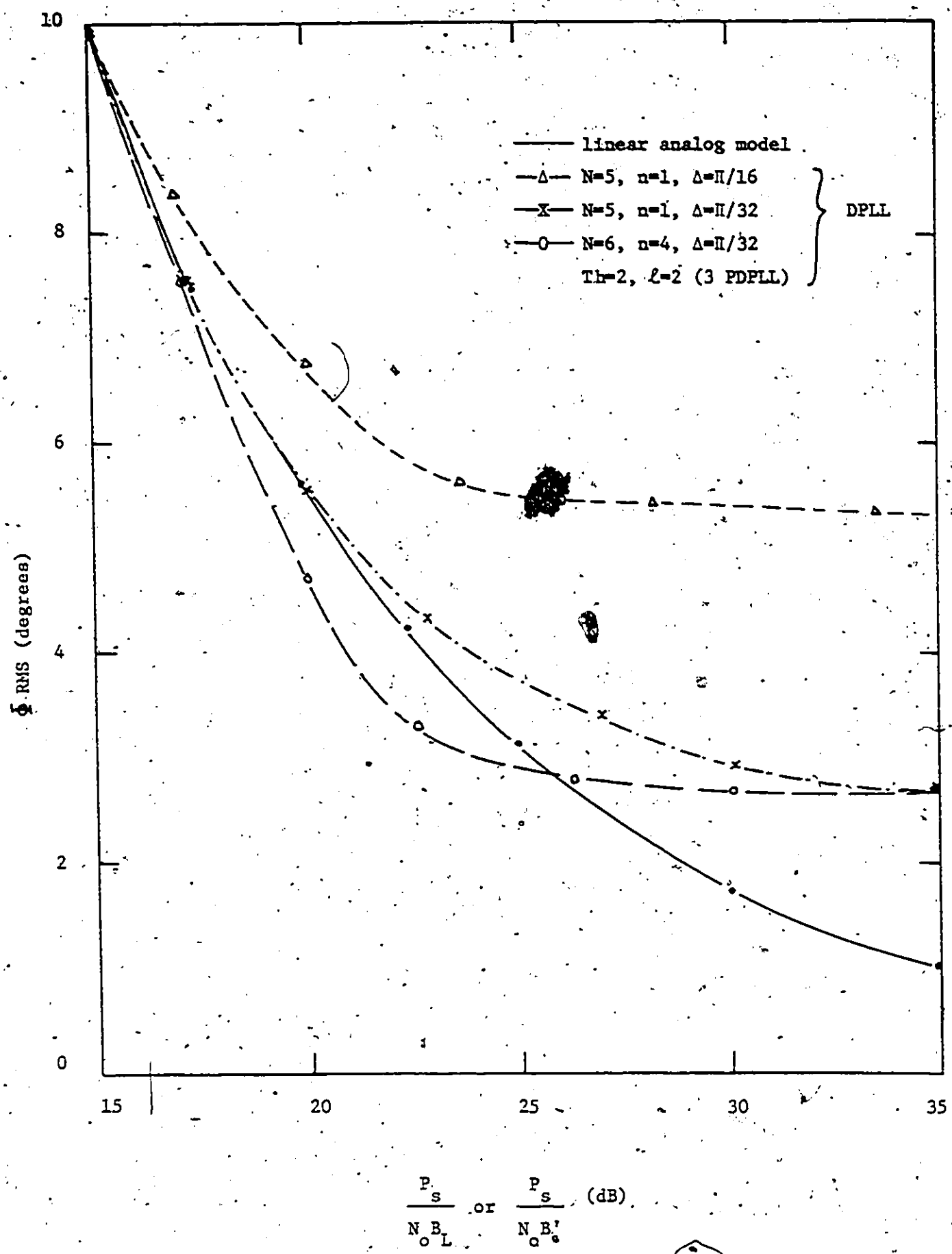


Fig. 34 - Comparison of binary loops with linear analog models.

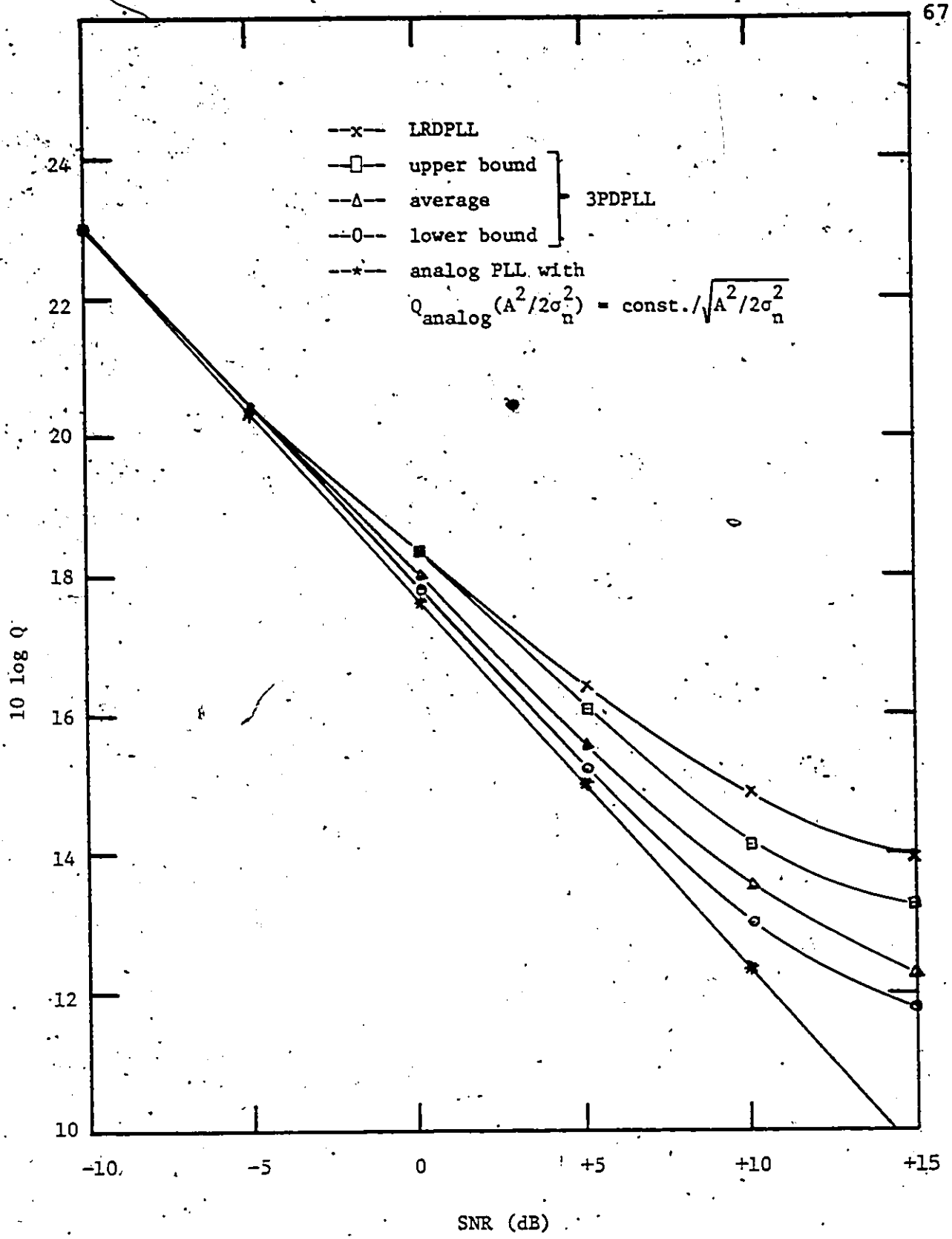


Figure 35: Performance criteria versus SNR

Chapter VI

EXPERIMENTAL RESULTS

6.1 INTRODUCTION

Because of its high flexibility, an experimental system based on the SDK 85 microprocessor was chosen to conduct the experiments needed to measure the RMS phase error with various noise conditions and with input signal frequency deviation. The experimental results are shown to match the numerical results closely.

The pictures of the input signal, the output phase error waveform and probability density function are presented. Finally, a practical hardware realization is suggested and some typical applications are discussed.

6.2 DESCRIPTION OF THE EXPERIMENTAL SYSTEM

The block diagram of the experimental system is shown in Fig. 36 The stable fixed oscillator, the 3PDPLL logic (U/D counter, comparator, digital phase shifter) and the phase comparator functions are all generated by the software controlling the SDK 85. For instance, the timer gives the sampling commands of the input signal and its control register defines the timing of the three samples .It is internally controlled and acts as a digital phase shifter.

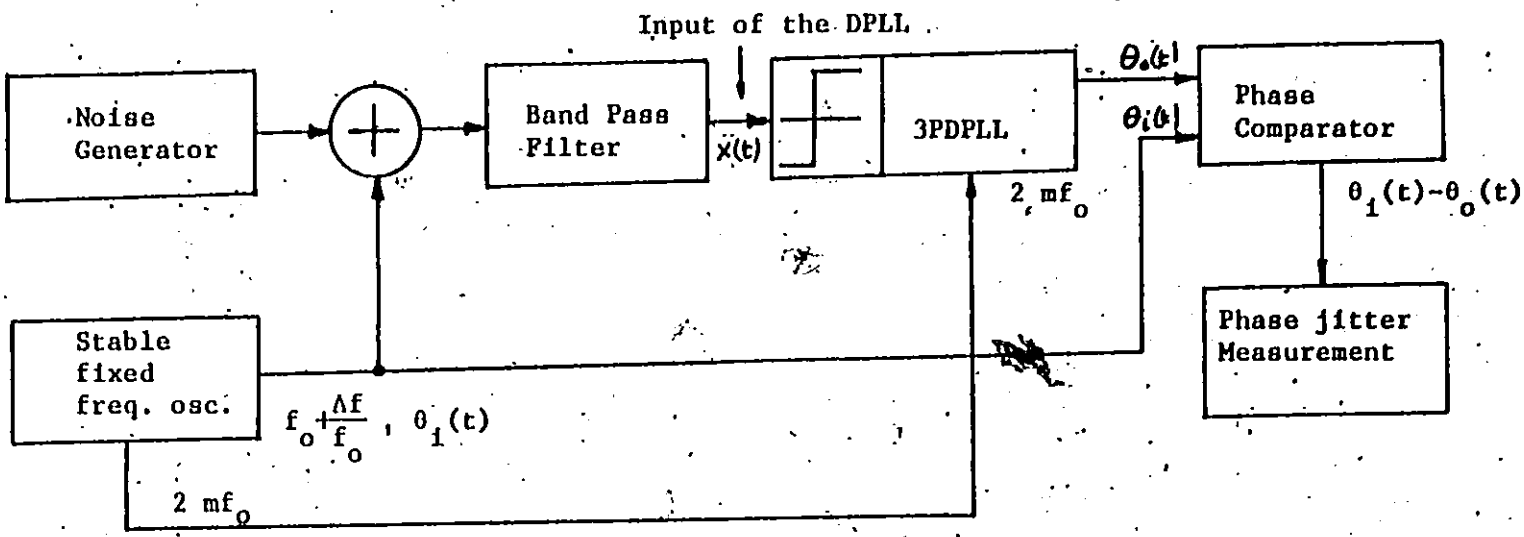


Fig.36 - Block diagram of the experimental system

6.3 RESULTS

The RMS phase errors of test 1 of section 5.2 have been obtained experimentally and are shown in Fig. 37. The corresponding overall locking-range B_o, the mean acquisition time T_m and the RMS phase error Φ_{RMS} in the noise free condition (k=1) are presented in table 7

TABLE 7

	B_o	T_m	Φ_{RMS}
a	0.00625 f_o	80 T	3.25
b	0.0104 f_o	48 T	3.25
c	0.0156 f_o	32 T	3.25
d	0.0208 f_o	24 T	3.25

The results confirm the choice of the simplifying hypothesis and approximations ((12),(13) and (22)) for the numerical analysis. A picture of the input signal waveform (SNR = 0 dB) is shown in Fig. 38. In Fig. 39, the output of the phase detector (phase error) is presented for an SNR of 0 dB while the probability density function of the phase error in the absence and in the presence of noise are shown in Fig. 40

The small and the large phase step correction as well as the variable time between phase corrections (due to the sequential filter) are shown in Fig. 39 The discreetness of the distribution of the phase error is also clear from the two pictures of Fig. 40 The distance between the consecutive peaks is equal to the unit phase step.

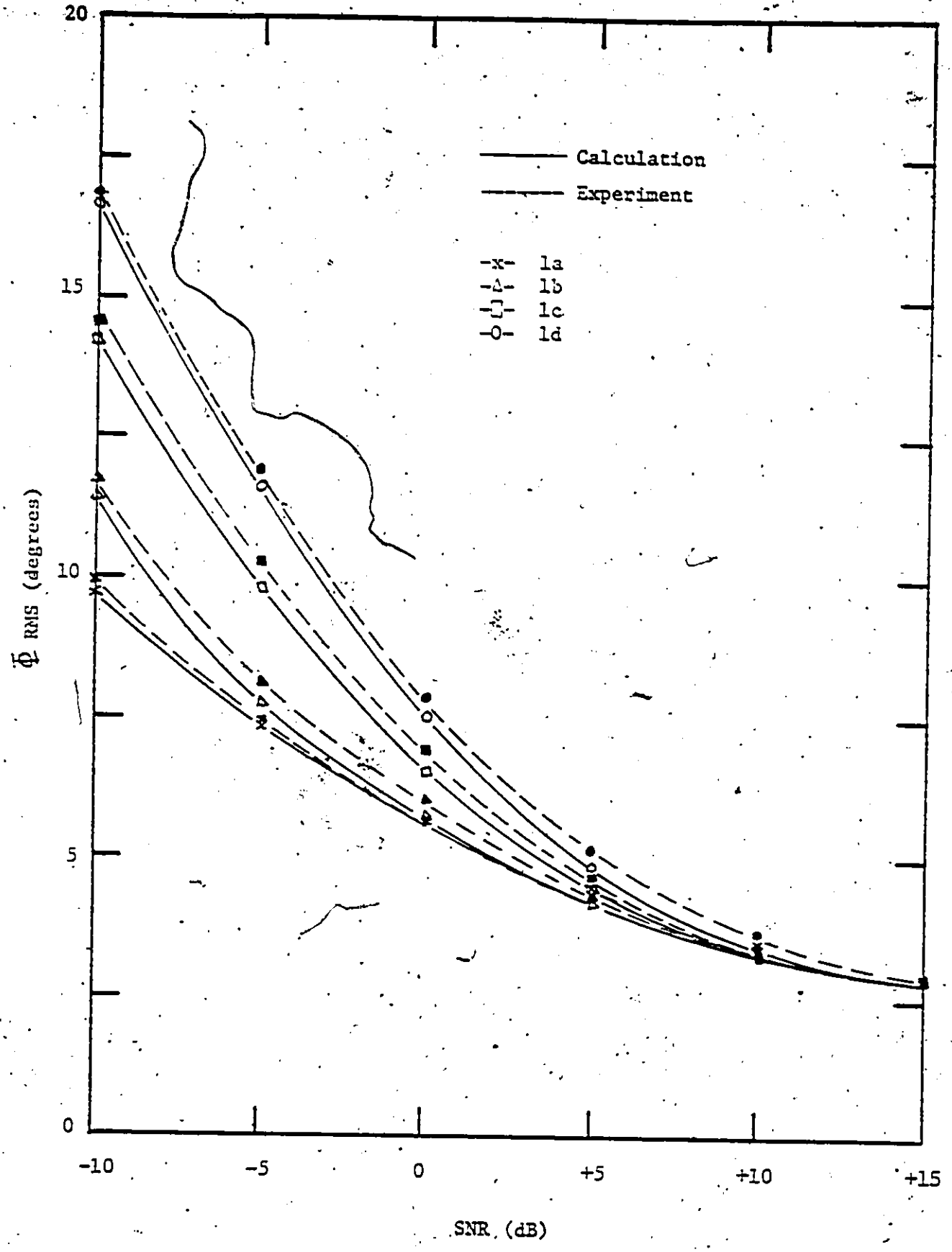
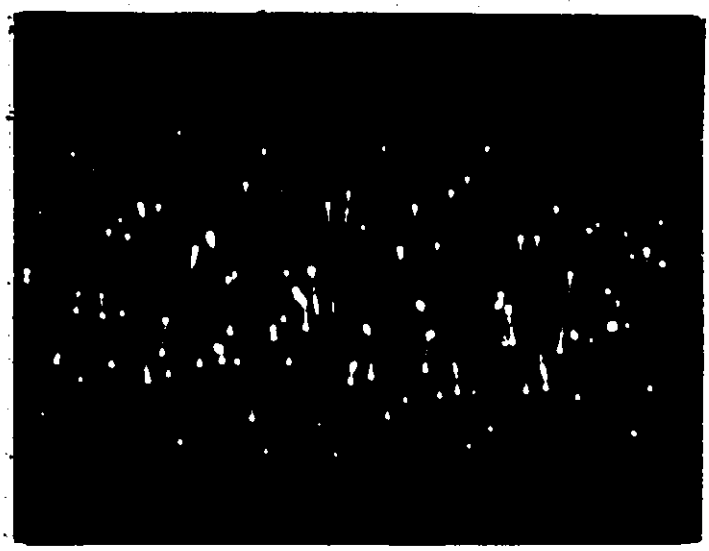
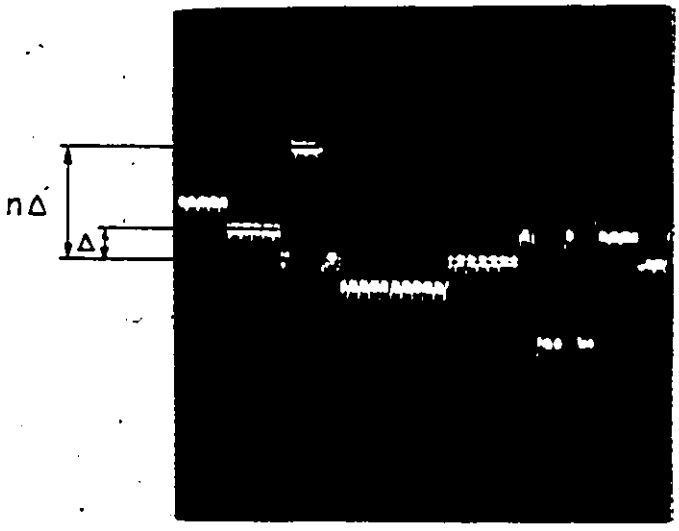


Figure 37: Loop RMS phase error versus SNR (experimental)



$f_o = B_n$

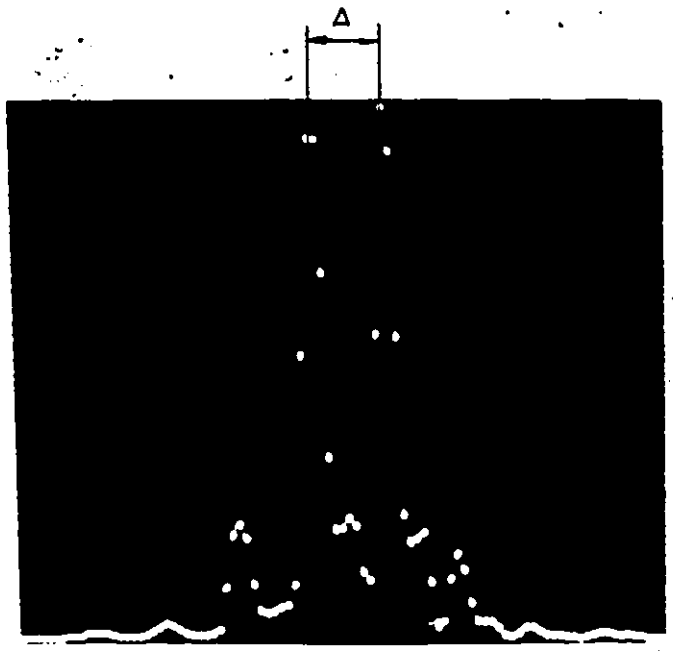
Figure 38: Input signal waveform (SNR = 0 dB)



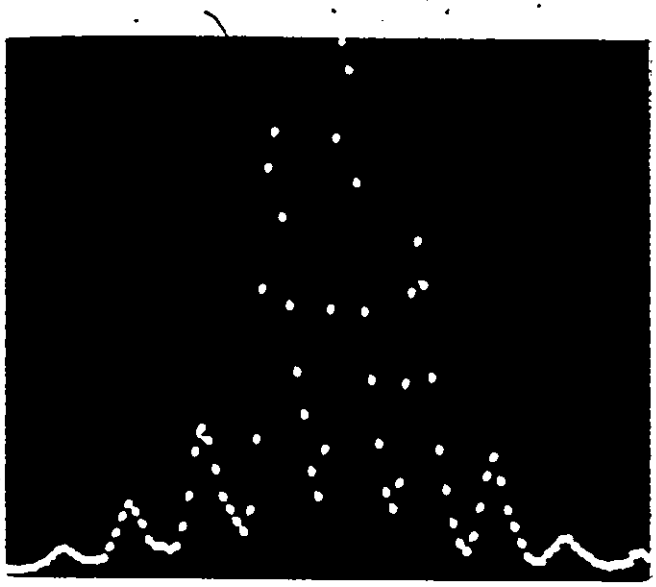
SNR = 0 dB

Test 1d, n=4

Figure 39: Phase detector output waveform



Phase error probability density in the absence of noise



SNR = 0 dB

Test 1d, n=4

Phase error probability density in the presence of noise

Figure 40: 3PDPLL phase error density function

6.4 EXPERIMENTS IN THE PRESENCE OF FREQUENCY DEVIATION

The previous sections have dealt with cases not involving frequency deviation ($\Delta f/f_o = 0$) but this one presents experimental and computer simulation results obtained with frequency deviation introduced, assuming a constant SNR of 10 dB. The results are shown in Fig. 41 The ability of the 3PDPLL to track frequency deviation is a consequence of the widening of the locking-range as pointed out in chapter III equation (5).

In Fig. 42, the phase detector output is presented and the presence of frequency deviation is demonstrated by the slope of the waveform. This is shown, in the picture of Fig. 43, by the continuity of the shape of the phase error probability density function.

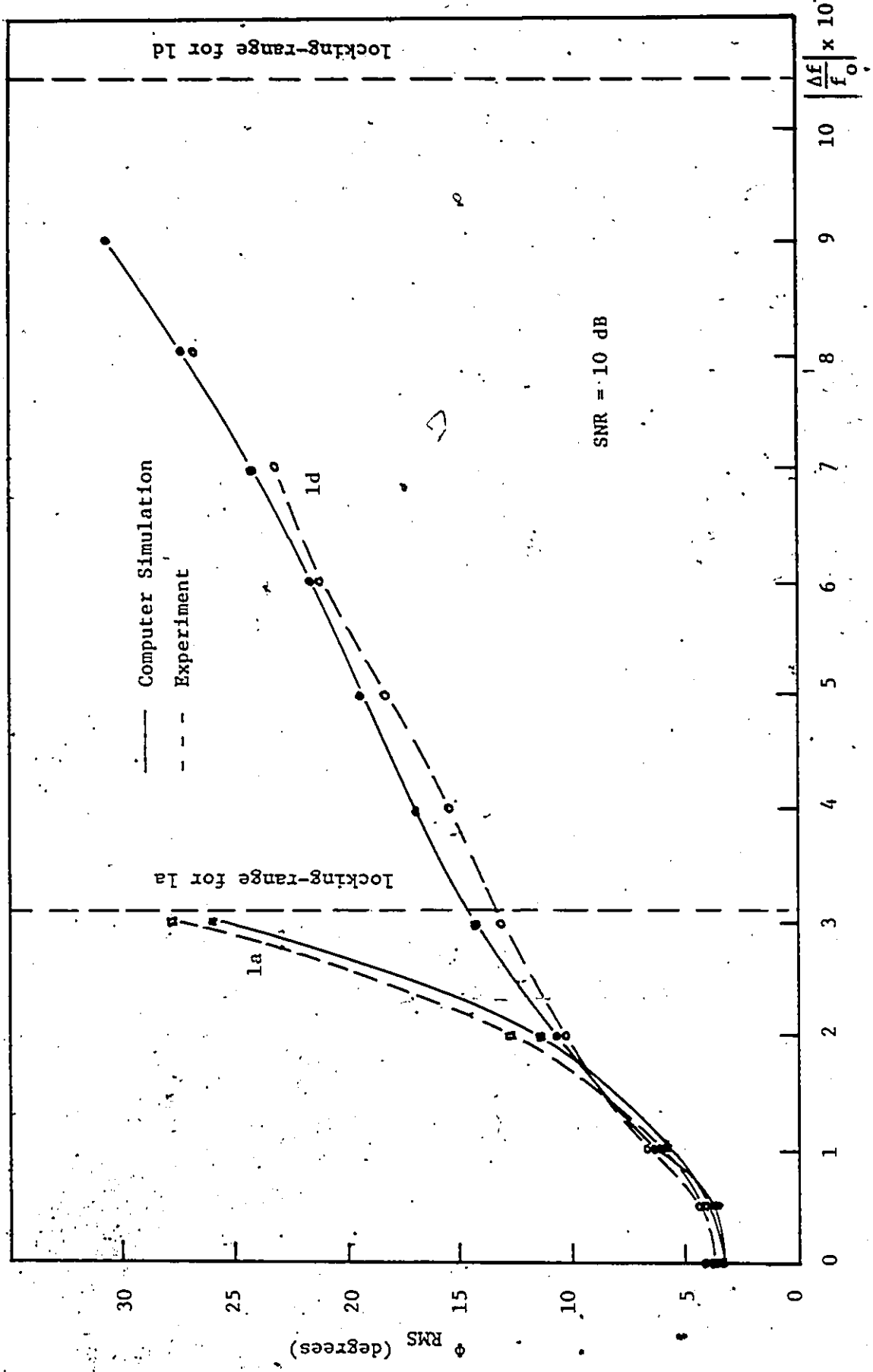
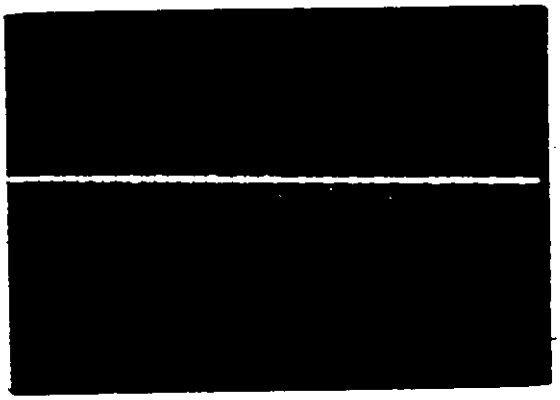
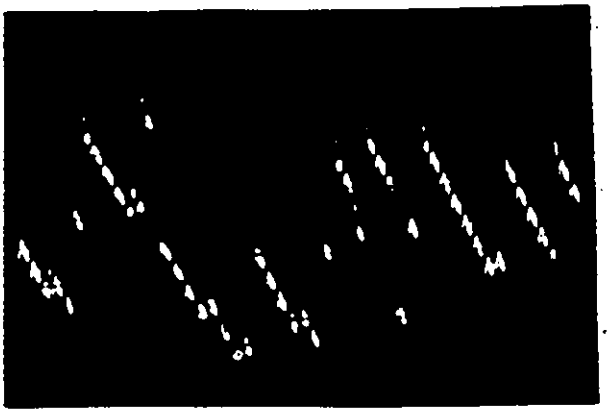


Figure 41 : Output RMS phase error in the presence of frequency deviation.



$\frac{\Delta f}{f_o} = 2\ 10^{-3}$

Phase error output waveform in the absence of noise



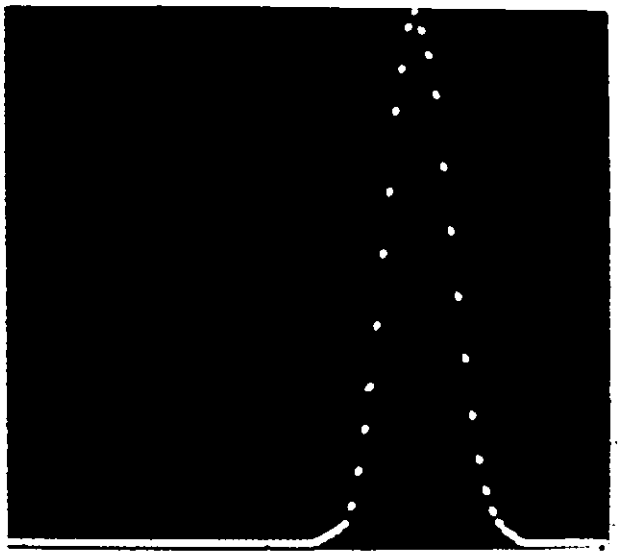
$\frac{\Delta f}{f_o} = 2\ 10^{-3}$

SNR = 0 dB

Test 1d

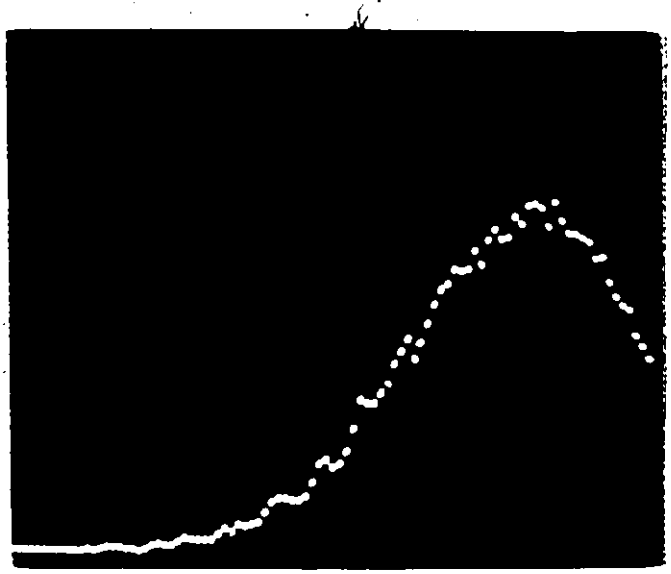
Phase error output waveform in the presence of noise

Figure 42: Phase error output waveform in the presence of frequency deviation



$\frac{\Delta f}{f_o} = 2\ 10^{-3}$

Phase error probability density in the absence of noise



$\frac{\Delta f}{f_o} = 2\ 10^{-3}$

SNR = 0 dB

Test 1d

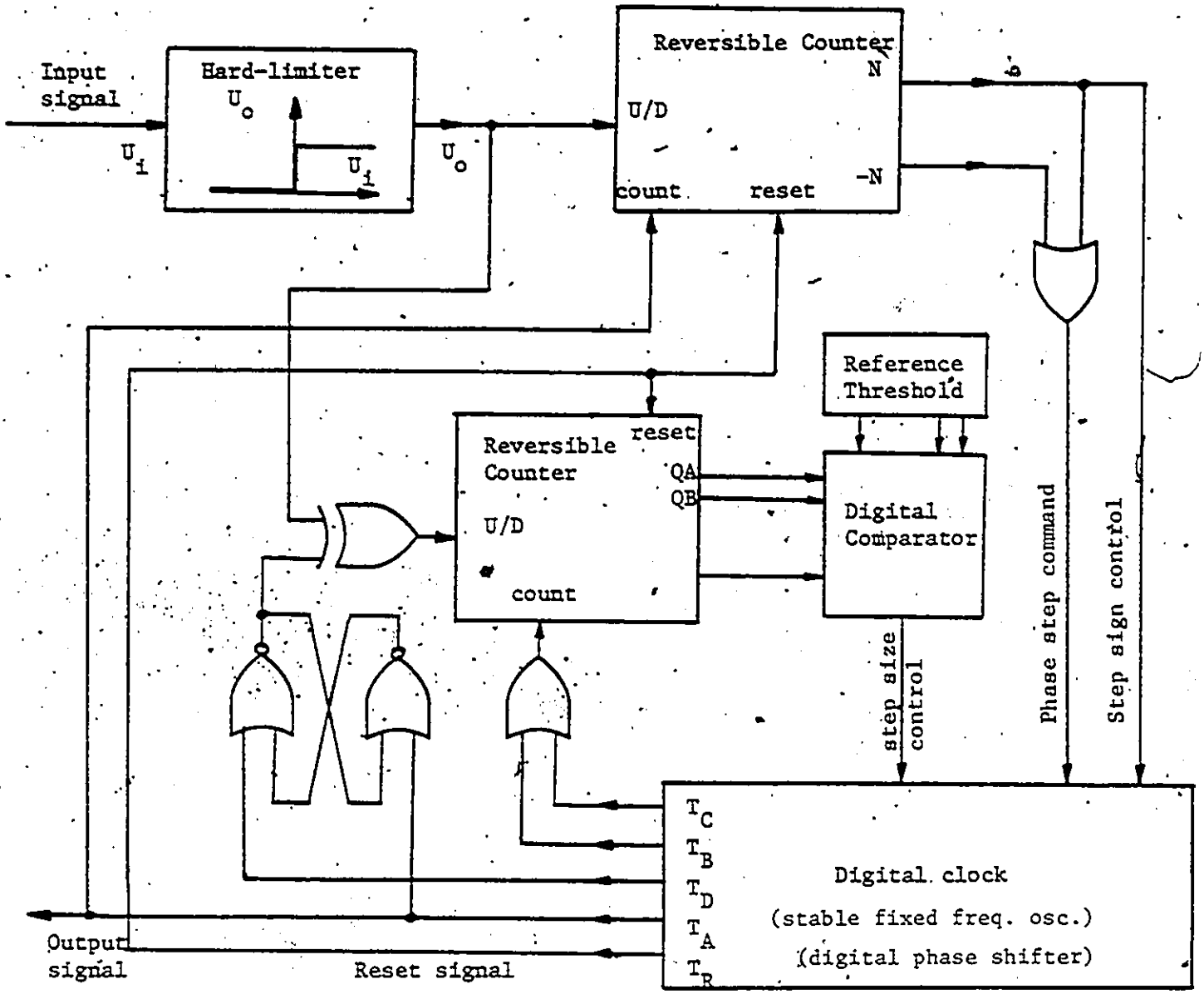
Phase error probability density in the presence of noise

Figure 43: Phase error distribution in the presence of frequency deviation

6.5 HARDWARE REALIZATION

A hardware realization of the 3PDPLL is shown in Fig. 44 It is worth noting that the ''Phase detector'' (Fig. 8) can be practically realized with a single hard-limiter by sequentially clocking the two reversible counters representing both the random-walk filter and the adder. The large and small phase step corrections are derived from a digital phase shifter in the digital clock circuit which realizes the phase shifts by adding or deleting cycles to a signal of frequency 2m times the input signal frequency. This is how the unit phase step $\Delta = \pi/m$ is obtained.

This high clock frequency is a definite limitation to the highest input signal frequency. In their survey of digital phase-locked loops, Lindsey and Chie [1] have demonstrated that with typical (off the shelf) state of the art logic components, one can build a digital controlled oscillator (phase shifter) that operates from a 350 MHz internal clock (stable fixed frequency oscillator). Hence, for a 5.6 degrees (m=32) quantization error, one can work with a maximum input signal frequency of 5.47 MHz. Since all the other components needed for the 3PDPLL work well beyond 10 MHz, the critical component that limits the high-speed application of the DPLL's is clearly the digital controlled oscillator. Note that a microprocessor based design yields a lower speed yet (8 MHz clock, 1-2 μs/instruction).



T_A: Sample time of A

T_B: Sample time of B

T_C: Sample time of C

T_R: Reset time of the counters

T_D: T_C+T_S

T_S: Time between two consecutive samples (of a same set)

Fig. 44 - Hardware realization of the 3 PDPLL

6.6 APPLICATION

The digital phase-locked loop finds its applications in the detection of phase, frequency and amplitude modulation, carrier phase and bit timing recovery to mention only a few possibilities. One of particular interest is the bit and frame synchronization in burst type transmission frequently encountered in integrated digital subscriber terminals handling both digitized voice and data in the same way [12].Because of the relative short duration of the message, a fast acquisition of the bit and frame timing is required while maintaining some good noise rejection performance. This is a typical example where the 3PDPLL (or an extended version) would outperform the frequently used lead/lag DPLL since the signal-to-noise ratio is well above 0 dB. This allows for a valuable mean acquisition time reduction while keeping the output RMS phase error at a low level.

Chapter VII

CONCLUSION

The non-uniform sampling DPLL with sequential loop filter in which the correction sizes are controlled by the accumulated phase differences of two additional phase comparators has been analysed. The numerical and experimental results have confirmed the expected reduction of the acquisition time with the accompanying small degradation of the noise rejection . Furthermore, the hardware needed to implement the 3PDPLL has been shown to be very simple.

Two 'Loop Performance Criteria' were succesfully used to compare DPLL's and illustrate the advantages and limitations of the 3PDPLL. Specifically the improvement of the performance which approaches that of an analog PLL for high signal-to-noise ratio.

Moreover, the improved ability of the 3PDPLL to track frequency drift has been demonstrated and represents an advantage in a system where an unexpected frequency deviation, even of short duration would throw a non-modified loop out of lock thus leading to a temporary loss of information.

These promising results leave the door open for further investigation. Applications in carrier phase and bit timing recovery are to be investigated as these will benefit from the improved performance parameters.

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[14] Jean-Paul Sandoz and Willem Steenaart,''Performance Improvement of a Binary Quantized all-Digital Phase-Locked Loop with a New Aided-Acquisition Technique'', Submitted for publication, IEEE Transac. on Communications.

Appendix A

COMPUTER SIMULATION PROGRAM OF THE LRDPLL AND THE 3PDPLL IN THE PRESENCE OF NOISE

```
C
C       ************************************************************
C       ******  SIMULATION OF THE LRDPLL AND THE 3PDPLL  ******
C       ******          IN THE PRESENCE OF NOISE          ******
C       ************************************************************
C
C
C       THIS PROGRAM PLOTS THE BEHAVIOR OF THE LRDPLL AND
C       THE 3PDPLL IN THE PRESENCE OR ABSENCE OF NARROW-
C       BAND GAUSSIAN NOISE PROCESS FOR FIXED INPUT PHASE,
C       INPUT PHASE STEP, INPUT PHASE RAMP AND COMPUTE THE
C       RMS PHASE ERROR FOR UP TO 999 INPUT DATA.
C
C
C       AM,AX    : VERTICAL SCALES (20% , 80% ON THE SCALE)
C       X(1)     : INPUT PHASE  ( X(1)=0 )
C       Y(1)     : INITIAL OUTPUT PHASE
C       IS       : FOR PLOTTING (1=VERY SLOW,2=SHARP ANGLE
C                                3=NORMAL,4=FAST)
C       D        : INPUT PHASE STEP BETWEEN 2 CONSECUTIVE INPUT DATA
C       NN       : NUMBER OF CONSECUTIVE INPUT PHASE STEPS
C                  NN=1 PHASE STEP
C                  NN=100-1000 FREQUENCY DEVIATION
C       B        : SMALL PHASE STEP SIZE (IN RAD.)
C       C        : LARGE PHASE STEP SIZE (IN RAD.)
C                  (C/B MUST BE AN INTEGER)
C       NW       : RANDOM-WALK FILTER HALF LENGTH
C                  (THE TOTAL LENGTH IS 2*NW+1)
C       DE       : DISTANCE BETWEEN TWO CONSECUTIVE SAMPLES
C                  OF A SAME SET
C       TH       : THRESHOLD (0,1,2... INTEGER)
C       K        : NUMBER OF DATA FOR THE PLOT  (MAX: 100)
C       KT       : TOTAL NUMBER OF DATA USED FOR THE ESTIMATION
C                  OF THE RMS PHASE ERROR  (MAX: 999)
C       S/N(DB)  : SIGNAL POWER TO NOISE POWER RATIO IN DB
C       II       : ANY POSITIVE INTEGER (USED TO GENERATE RANDOM NOISE
C       KPX      : NUMBER OF INTERVALS IN X AXIS
C       KPY      : NUMBER OF INTERVALS IN Y AXIS
C
```

```
C                                  ****
C
      DIMENSION X(999),Y(999),IX(250),IY(250),IXX(250)
      DIMENSION XE(999),NN(3)
500   NN(1)=0
      NN(2)=0
      NN(3)=0
      TYPE*,'AM  AX  Y(1) IS'
      ACCEPT*,AM,AX,Y(1),IS
      TYPE*,'D  NN  B  C  NW  DE  TH  K  KT'
      ACCEPT*,D,N,B,C,NW,DE,CON,K,KT
      NM=0
      XE(1)=0
      X(1)=D
      TYPE*,' S/N (DB)        II
      ACCEPT*,SN,II
      TYPE*,'KPX,KPY,IO(0:SUM,1:1+PRINT,2:1+Y,3:2+X,4:3+AXIS,5:EXIT'
      ACCEPT*,KPX,KPY,IO
      IF (IO.EQ.5) GOTO 600
      L=0
      M=0
      DO 50 I=1,II
      RX=RAN(L,M)
50    CONTINUE
      W=2.0
      A=SQRT(W)*(10.**(.05*SN))
      DO 10 I=1,KT
      XX=0
      YY=0
      DO 70 J=1,12
      XX=XX+RAN(L,M)-0.5
      YY=YY+RAN(L,M)-0.5
70    CONTINUE
      Z=(SIN(X(1)-Y(1))-(XX*SIN(Y(1))-YY*COS(Y(1)))/A)
      NX=1
      IF (Z.LE.0.) NX=-1
      NN(2)=NN(2)+NX
      Z=(SIN(X(I)-Y(I)-DE)-(XX*SIN(Y(I)+DE)-YY*COS(Y(I)+DE))/A)
      NX=1
      IF (Z.LE.0.) NX=-1
      NN(1)=NN(1)+NX
      Z=(SIN(X(1)-Y(I)+DE)-(XX*SIN(Y(I)-DE)-YY*COS(Y(I)-DE))/A)
      NX=1
      IF (Z.LE.0.) NX=-1
      NN(3)=NN(3)+NX
      IF (NN(2).GE.NW) GO TO 111
      IF (NN(2).LE.-NW) GO TO 111
```

```
      XXY=0.0
      GO TO 112
111   XXX=B
      IF ((NN(3)-NN(1)).LT.CON) XXX=C
      XXY=1.0
      IF (NN(2).LT.0) XXY=-1.0
      NN(1)=0
      NN(2)=0
      NN(3)=0
112   IF (N-1.LT.I) D=0
      X(I+1)=X(I)+D
      Y(I+1)=Y(I)+XXY*XXX
      XE(I+1)=XE(I)+(X(I)-Y(I+1))*(X(I)-Y(I+1))
10    CONTINUE
      TYPE*,'RMS PHASE ERROR =',((SQRT(XE(KT)/KT))*57.296)
      IF (IO.EQ.0) GOTO 500
      IF (IO.NE.1) GOTO 400
      TYPE120,(X(I),I=1,20)
      TYPE120,(Y(I),I=1,20)
      TYPE120,(Y(I),I=21,40)
      TYPE120,(Y(I),I=41,60)
      TYPE120,(Y(I),I=61,80)
120   FORMAT (20(1X,F5.2))
      GOTO 500
400   DO 55 I=1,K
      IX(I)=(((X(I)-AM)*300)/(AX-AM))*20+2000
      IY(I)=(((Y(I)-AM)*300)/(AX-AM))*20+2000
      IXX(I)=(((I-1)*100)/K)*100
55    CONTINUE
      CALL DRAW(IS,IXX,IY,K)
      IF (IO.EQ.2) GOTO 500
      CALL DRAW(IS,IXX,IX,K)
      IF (IO.EQ.3) GO TO 500
      II=((-300*AM)/(AX-AM))*20+2000
      CALL AXIS(0,KPX,9999,0,II)
      CALL AXIS(1,KPY,9999,0,0)
      GO TO 500
600   STOP
      END
```

Appendix B

NUMERICAL COMPUTATION OF THE RMS PHASE ERROR AND THE MEAN ACQUISITION TIME OF THE LRDPLL AND THE 3PDPLL

```
C     ************************************************************
C     ******  NUMERICAL COMPUTATION OF THE RMS PHASE  ******
C     ******  ERROR AND THE MEAN ACQUISITION TIME OF  ******
C     ******       THE  LRDPLL  AND THE  3PDPLL       ******
C     ************************************************************
C
C
C                        ***********
C     * THIS PROGRAM COMPUTES THE RMS PHASE ERROR *
C     * AND THE MEAN ACQUISITION  TIME  FOLLOWING *
C     * THE STEP-BY-STEP DESCRIPTION OF CHAPTER 4 *
C                        **********
C
C     SU(I) : PROBABILITY OF A POSITIVE GOING ZERO CROSSING
C                        OCCURRING BETWEEN
C             (I-1)*180/32-90/32 AND (I-1)*180/32+90/32
C                              DEGREES
C     P<(I),-++> = X(1,I)
C     P<(I),--+> = X(2,I)
C     P<(I),+--> = X(3,I)
C     P<(I),++-> = X(4,I)
C     P<(I),+++> = X(5,I)
C     P<(I),---> = X(6,I)
C                              I=1-32
C     U<+1,(I)>  = X(7,I)
C     U<+N,(I)>  = X(8,I)
C     U<-1,(I)>  = X(9,I)
C     U<-N,(I)>  = X(10,I)
C
C     T(I)       = X(11,I)
C     L(I)       = X(12,I)
C     P(I)       = X(13,I)
C     T0(I)      = X(14,I)
C
C
```

```
      DIMENSION Y(331),IY(129),IX(129),SU(33),X(14,32)
      DIMENSION YY(64),Z(19,21),ZZ(19,21)
2     TYPE*,' '
      TYPE*,'S/N (DB) ?'
      TYPE*,' '
      ACCEPT*,SN
C
C     COMPUTATION OF EQUATION (14) WITH THE APPROXIMATION
C     OF EQUATION (22) ..
C
      UU=3.1415926
      A=-UU/64.
      SN=(10.**(.1*SN))
      DO 1 I=1,331
      RR=SQRT(2.*SN)*COS(A)
      T=1./(1.+0.2316419*ABS(RR))
      AQ=T*((((1.330274*T-1.821256)*T+1.7814/8)*T-.3565638)*T+0.3193815)
      AQ=AQ*EXP(-RR*RR/2.)/SQRT(UU*2.)
      IF (RR.GE.0.) AQ=1.-AQ
      AP=AQ*EXP(SN*COS(A)*COS(A))*SQRT(4.*UU*SN)*COS(A)+1.
      Y(I)=(AP*EXP(-SN))/(2.*UU)
      A=A+UU/320.
1     CONTINUE
C
C     PLOT OF THE PROBABILITY DENSITY OF A POSITIVE
C                ZERO CROSSING
C
      TYPE*,' '
      TYPE*,'CENTER=',Y(6),'  SCALE (0:NO PLOT,999:NEW S/N)'
      TYPE*,'AXIS (0:NO AXIS)'
      ACCEPT*,SC,JX
      IF (SC.EQ.0.) GO TO 3
      IF (SC.EQ.999.) GO TO 2
      DO 4 I=1,129
      IX(I)=7.7*(I-1)
4     CONTINUE
      DO 5 I=66,129
      IY(I)=(Y((I-64)*5+1)/SC)*9999
      IY(130-I)=IY(I)
5     CONTINUE
      IY(65)=(Y(6)/SC)*9999
      CALL DRAW(3,IX,IY,129)
      IF (JX.EQ.0) GO TO 2
      CALL AXIS(0,12,9856,0,0)
      CALL AXIS(1,10,9999,4928,0)
      GO TO 2
C     NUMERICAL INTEGRATION USING SIMSON'S RULE
3     K=1
      DO 6 I=1,325,10
      SU(K)=4.*(Y(I+1)+Y(I+3)+Y(I+5)+Y(I+7)+Y(I+9))
      SU(K)=SU(K)+2.*(Y(I+2)+Y(I+4)+Y(I+6)+Y(I+8))
      SU(K)=(SU(K)+Y(I)+Y(I+10))*UU/960.
      IF (SU(K).LE.0.0) SU(K)=0.0
      K=K+1
6     CONTINUE
100   FORMAT (17(1X,F5.3))
      SM=0.
      DO 7 I=2,32
      SM=SM+SU(I)
7     CONTINUE
      SM=(SM+(SU(1)+SU(33))/2.)*2.
```

```
      TYPE*,' '
      TYPE*,'NUMBER OF UNIT STEPS BETWEEN THE SAMPLES (1,2,3,...,15,16)'
      TYPE*,'ONE UNIT PHASE STEP CORRESPOND TO 180/32 DEGREES'
      TYPE*,' '
      ACCEPT*,ID
C
C     THIS PART OF THE PROGRAM COMPUTES THE PROBABILITIES OF
C     OCCURENCE OF THE 6 OUTCOMES (+++ ++- +-- -++ --+ ---)
C     FOR THE 32 POSSIBLE PHASE ERRORS
C
      IF (ID.EQ.0) GO TO 8
      DO 11 J=1,32
      X(1,J)=0.0
      X(2,J)=0.0
      X(3,J)=0.0
      X(4,J)=0.0
      DO 12 K=1,ID
      JJ=J-K+1
      JK=J+K
      KK=J-K+33
      KJ=J+K-32
      IF (JJ.LE.0) JJ=-JJ+2
      IF (JK.GT.33) JK=66-JK
      IF (KK.GT.33) KK=66-KK
      IF (KJ.LE.0)  KJ=-KJ+2
      X(1,J)=X(1,J)+SU(JJ)
      X(2,J)=X(2,J)+SU(JK)
      X(3,J)=X(3,J)+SU(KK)
      X(4,J)=X(4,J)+SU(KJ)
12    CONTINUE
11    CONTINUE
      GO TO 13
8     DO 9 I=1,4
      DO 10 J=1,32
      X(I,J)=0.0
10    CONTINUE
9     CONTINUE
13    SU(1)=SU(1)/2.
      SU(33)=SU(33)/2.
      DO 14 J=1,32
      X(5,J)=-X(1,J)-X(4,J)
      DO 15 K=1,J
      X(5,J)=X(5,J)+SU(K)
15    CONTINUE
      DO 16 K=1,33-J
      X(5,J)=X(5,J)+SU(K)
16    CONTINUE
      X(6,J)=-X(1,J)-X(2,J)-X(3,J)-X(4,J)-X(5,J)+1.0
      IF (X(6,J).GT.1.0) X(6,J)=1.000
      IF (X(6,J).LT.0.0) X(6,J)=0.0
14    CONTINUE
      TYPE*,' '
      TYPE*,'X(1,I) .....  X(6,I), I=1,4,7,10...31'
      TYPE*,' '
      DO 17 J=1,6
      TYPE 100,(X(J,I),I=1,33,3)
17    CONTINUE
      TYPE*,' '
      TYPE*,'N (RANDOM-WALK FILTER), TH (THRESHOLD,IE. 0,1,2..)'
      TYPE*,'ITE (MAXIMUM NUMBER OF ITERATION)'
      ACCEPT*,NW,RT,ITE
      ALI=99.999
```

```
C
C       COMPUTATION OF THE AVERAGE TIME SPENT IN EACH STAGE T(I)
C
        DO 18 K=1,32
        UP=X(1,K)+X(4,K)+X(5,K)
        UD=1.0-UP
        X(11,K)=NW/(UP-UD)-(2.*NW)/((UP-UD)*(1.+(UP/UD)**(NW)))
18      CONTINUE
        TYPE*,' '
        TYPE*,'T(I), I=1,32'
        TYPE*,' '
        TYPE 102,(X(11,K),K=1,16)
        TYPE 102,(X(11,K),K=17,32)
        TYPE*,' '
C
C       COMPUTATION OF THE TERMINATION PROBABILITIES
C               FOR THE 32 POSSIBLE PHASE ERROR
C
        KC=2*NW+3
        KL=KC+2
        K=1
        ITE=0
        DO 19 K=1,32
        DO 20 I=1,19
        DO 21 J=1,21
        Z(I,J)=0.0
        ZZ(I,J)=0.0
21      CONTINUE
20      CONTINUE
        Z((KL+1)/2,(KC+1)/2)=100.00
        X(7,K)=0.0
        X(8,K)=0.0
        X(9,K)=0.0
        X(10,K)=0.0
        T=0.0
30      DO 22 I=2,(KL-1)
        DO 23 J=2,(KC-1)
        ZZ(I,J)=Z(I,J-1)*X(6,K)+Z(I,J+1)*X(5,K)+Z(I-1,J-1)*X(3,K)
        ZZ(I,J)=ZZ(I,J)+Z(I-1,J+1)*X(4,K)+Z(I+1,J+1)*X(1,K)+Z(I+1,J-1)*X(2,K)
23      CONTINUE
22      CONTINUE
        DO 24 I=2,(KL-1)
        DO 25 J=2,(KC-1)
        Z(I,J)=ZZ(I,J)
25      CONTINUE
24      CONTINUE
        DO 27 I=1,KC
        Z(3,I)=Z(3,I)+Z(2,I)
        Z(2,I)=0.0
        Z(KL-2,I)=Z(KL-2,I)+Z(KL-1,I)
        Z(KL-1,I)=0.0
27      CONTINUE
        DO 28 I=1,(KL+1)/2-KT
        X(7,K)=X(7,K)+Z(I,2)
        X(9,K)=X(9,K)+Z(I,KC-1)
        Z(I,2)=0.
        Z(I,KC-1)=0.
28      CONTINUE
        DO 29 I=(KL+1)/2-KT+1,KL
        X(8,K)=X(8,K)+Z(I,2)
        X(10,K)=X(10,K)+Z(I,KC-1)
```

```
      Z(I,2)=0.0
      Z(I,KC-1)=0.0
29    CONTINUE                                                    93
      T=X(7,K)+X(8,K)+X(9,K)+X(10,K)
      ITE=ITE+1
      IF (K.GE.2) GO TO 32
102   FORMAT (17(1X,F6.2))
      IF (ITE.GE.2) GO TO 32
      TYPE*,'U<+1>      U<+N>       U<-1>       U<-N>       ITE     I'
      TYPE*,' '
777   FORMAT (1X,4(6X,F6.2),6X,I3,6X,I3)
32    IF (ITE.GE.IITE) GO TO 800
      IF (T.LE.ALI) GO TO 30
800   X(7,K)=X(7,K)*100.0/T
      X(8,K)=X(8,K)*100.0/T
      X(9,K)=X(9,K)*100.0/T
      X(10,K)=X(10,K)*100.0/T
      TYPE 777,X(7,K),X(8,K),X(9,K),X(10,K),ITE,K
      ITE=0
19    CONTINUE
C
C     COMPUTATION OF THE PROBALITY OF STATE SELECTION GIVEN THAT
C     A STATE TRAMSITION IS OCCURING [ L(I) ]
C
500   TYPE*,' '
      TYPE*,'SMALL PHASE STEP (1,2,4,8 FOR M=32,16,8,4)'
      TYPE*,'K : RATIO LARGE/SMALL PHASE STEP SIZE (INTEGER)'
      TYPE*,' '
      ACCEPT*,KSM,KLA
      AMX=0.0
      KSS=KSM
      IF (KSM.GE.4) KSS=KSM/2
      COR=1.0
      DO 41 K=1,64
      Y(K)=0.0
41    CONTINUE
      DO 45 K=KSS,64,KSM
      Y(K)=(100.0*KSM)/64.0
45    CONTINUE
      KLA=KLA*KSM
      ITE=0
46    DO 43 K=KSS,64,KSM
      IY(1)=K-KSM
      IY(2)=K-KLA
      IY(3)=K+KSM
      IY(4)=K+KLA
      IY(5)=9
      IY(6)=10
      IY(7)=7
      IY(8)=8
      DO 44 I=1,4
      IF (IY(I).LE.0) IY(I)=IY(I)+64
      IF (IY(I).GT.64) IY(I)=-64+IY(I)
      IY(I+8)=IY(I)
      IF (IY(I+8).GT.32) IY(I+8)=65-IY(I+8)
44    CONTINUE
      IF (IY(1).GT.32) IY(5)=7
      IF (IY(2).GT.32) IY(6)=8
      IF (IY(3).GT.32) IY(7)=9
      IF (IY(4).GT.32) IY(8)=10
      YY(K)=Y(IY(1))*X(IY(5),IY(9))+Y(IY(2))*X(IY(6),IY(10))
      YY(K)=Y(IY(3))*X(IY(7),IY(11))+Y(IY(4))*X(IY(8),IY(12))+YY(K)
```

```
      YY(K)=YY(K)*COR/100.0
43    CONTINUE
      DD=0.0
      SM=0.0
      DO 55 K=KSS,64,KSM
      DD=(YY(K)-Y(K))**(2.0)+DD
      Y(K)=YY(K)
      SM=Y(K)+SM
55    CONTINUE
47    COR=100.0/SM
      ITE=ITE+1
      IF (ITE.GE.200) GO TO 522
      IF (DD.GT.AMX) GO TO 46
522   DO 52 I=1,32
      X(12,I)=0.0
52    CONTINUE
      DO 50 I=1,32
      X(12,I)=Y(I)
50    CONTINUE
      DO 51 I=1,32
      X(12,I)=X(12,1)+Y(65-I)
51    CONTINUE
      TYPE*,' '
      TYPE*,'L(I)   I=1,32'
      TYPE*,' '
      TYPE 102,(X(12,J),J=1,16)
      TYPE 102,(X(12,J),J=17,32)
      TYPE*,'NBR OF ITERATION=',ITE
      ASM=0.0
      DO 53 K=1,32
      ASM=X(11,K)*X(12,K)+ASM
53    CONTINUE
      AMQ=0.0
      DO 54 K=1,32
      X(13,K)=X(11,K)*X(12,K)/ASM
      AMQ=AMQ+(((K-0.5)*180.0/32.0)**(2.0))*X(13,K)
      X(13,K)=100.0*X(13,K)
54    CONTINUE
      AMQ=SQRT(AMQ)
      TYPE*,' '
      TYPE*,'P(I) , I=1,32'
      TYPE*,' '
      TYPE 102,(X(13,J),J=1,16)
      TYPE 102,(X(13,J),J=17,32)
      DO 99 K=1,32
      X(7,K)=X(7,K)/100.0
      X(8,K)=X(8,K)/100.0
      X(9,K)=X(9,K)/100.0
      X(10,K)=X(10,K)/100.0
99    CONTINUE
C
C     NUMERICAL COMPUTATION OF THE TIME BEFORE ACQUISITION
C     (IE. BEFORE REACHING THE MINIMUM ERROR FOR THE FIRST TIME)
C     USING THE **GAUSS SEIDEL ** METHOD
C
      X(14,2)=X(11,2)
      DO 60 K=2,31
      X(14,(K+1))=(X(14,K)+X(11,(K+1)))/KSM
60    CONTINUE
      X(14,1)=0.0
      ITE=0
71    DD=0.0
```

```
      SM=0.0
      DO 61 K=2,32
      IY(1)=K-KSM
      IY(2)=K-KLA
      IY(3)=K+KSM
      IY(4)=K+KLA
      YY(K)=0.0
      IF (IY(1).LE.1) GO TO 66
      IF (IY(2).LE.1) GO TO 65
      IF (IY(3).GT.32) IY(3)=65-IY(3)
      IF (IY(4).GT.32) IY(4)=65-IY(4)
      IF (IY(3).EQ.K) GO TO 67
      IF (IY(4).EQ.K) GO TO 68
      YY(K)=X(11,K)+X(7,K)*X(14,IY(1))+X(8,K)*X(14,IY(2))
      YY(K)=YY(K)+X(9,K)*X(14,IY(3))+X(10,K)*X(14,IY(4))
      GO TO 69
67    IF (IY(3).EQ.IY(4)) GO TO 70
      YY(K)=X(11,K)+X(7,K)*X(14,IY(1))+X(8,K)*X(14,IY(2))
      YY(K)=(YY(K)+X(10,K)*X(14,IY(4)))/(1.0-X(9,K))
      GO TO 69
68    IF (IY(3).EQ.IY(4)) GO TO 70
      YY(K)=X(11,K)+X(7,K)*X(14,IY(1))+X(8,K)*X(14,IY(2))
      YY(K)=(YY(K)+X(9,K)*X(14,IY(3)))/(1.0-X(10,K))
      GO TO 69
70    YY(K)=(X(11,K)+X(7,K)*X(14,IY(1))+X(8,K)*X(14,IY(2)))
      YY(K)=YY(K)/(1.0-X(9,K)-X(10,K))
      GO TO 69
65    YY(K)=X(7,K)*X(14,IY(1))
66    YY(K)=YY(K)+X(11,K)+X(9,K)*X(14,IY(3))+X(10,K)*X(14,IY(4))
69    DD=DD+(100.0*(X(14,K)-YY(K))/YY(K))**(2)
      X(14,K)=YY(K)
      SM=SM+X(14,K)
      IY(K+32)=YY(K)
61    CONTINUE
      ITE=ITE+1
      IF (ITE.GT.200) GO TO 206
200   FORMAT(17(1X,I4))
205   IF (DD.GT.AMX) GO TO 71
206   TYPE*,' '
      TYPE*,'TO(I)   I=1,32'
      TYPE*,' '
      TYPE 200,(IY(K+32),K=2,16)
      TYPE 200,(IY(K+32),K=17,32)
      TYPE*,' '
      TYPE*,'MEAN NUMBER OF SETS OF SAMPLES =',SM/32
      TYPE*,'RMS PHASE ERROR (DEGREES)      =',AMQ
      TYPE*,' '
      TYPE*,'NEW SMALL AND LARGE STEP ? (YES=1)'
      ACCEPT*,NEE
      DO 501  K=1,32
      X(7,K)=X(7,K)*100.0
      X(8,K)=X(8,K)*100.0
      X(9,K)=X(9,K)*100.0
      X(10,K)=X(10,K)*100.0
501   CONTINUE
      IF (NEE.EQ.1) GO TO 500
      STOP
      END
```