

# **Microfabrication of Plasmonic Biosensors in CYTOP Integrating a Thin SiO<sub>2</sub> Diffusion and Etch-barrier Layer**

**By**

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## Abstract

A novel process for the fabrication of Long Range Surface Plasmon Polariton (LRSPP) waveguide based biosensors is presented herein. The structure of the biosensor is comprised of *Au* stripe waveguide devices embedded in thick CYTOP claddings with a SiO<sub>2</sub> solvent diffusion barrier and etch-stop layer. The SiO<sub>2</sub> layer is introduced to improve the end quality of *Au* waveguide structures, which previously deformed during the deposit of the upper cladding process and to limit the over-etching of CYTOP to create micro-fluidic channels. The E-beam evaporation method is adapted to deposit a thin SiO<sub>2</sub> on the bottom cladding of CYTOP. A new micro-fluidic design pattern is introduced. Micro-fluidic channels were created on selective *Au* waveguides through O<sub>2</sub> plasma etching. The presented data and figures are refractive index measurements of different materials, thickness measurements, microscope images, and AFM images. Optical power cutback measurements were performed on fully CYTOP-cladded symmetric LRSPP waveguides. The end-fire coupling method was used to excite LRSPP modes with cleaved polarization maintaining (PM) fibre. The measured mode power attenuation (MPA) was 6.7 dB/mm after using index-matched liquid at input and output fibre-waveguide interfaces. The results were compared with the theoretical calculations and simulations. Poor coupling efficiency and scattering due to the SiO<sub>2</sub> are suspected for off-target measurements.

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# 1. Introduction

## 1.1 Optical Biosensors

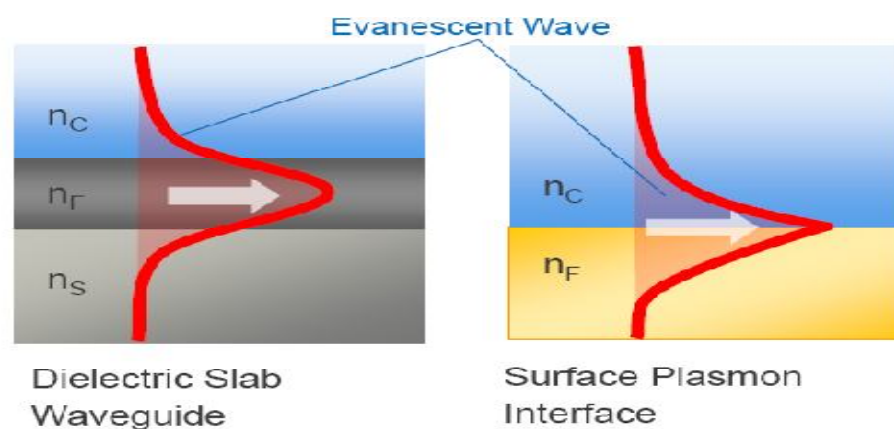
Optical biosensors can be described as analytical devices which can detect biochemical substances and biological entities in different environments using the light-matter interaction analysis technique. In the last decade, there has been an increasing effort devoted to research and development of optical biosensors and biochips worldwide [1]. The optical biosensor typically consists of a detector (transducer) element coated with bio-receptors for the selective capture of the target entity (analyte), micro-fluidic channels, and interrogation optoelectronic components. The bio-receptor, which may consist of a protein target or antibodies, is immobilized on the surface of the optical transducer [2]. The micro-fluidic channels introduce the analyte in the biosensor and separate unbound and bound molecules, which makes the biosensor a powerful biophysical tool for quantitatively characterizing how bio-molecular complexes form and dissociate over time [5].

The detection of analytes is conventionally performed by introducing probes (e.g. fluorescent) and tagging them onto specific targets. These probes are then optically excited and an emission of another wavelength (wavelength-shift) is observed. This technique has the drawbacks of requiring a time-consuming labelling process and photo-bleaching, which occurs because the probes cease to emit light after a certain period of time. Therefore, the principal goal of micro-fabricated biosensors is to improve on this conventional technique by providing label-free, direct sensing, and quantitative monitoring of biological and chemical substances [2].

Label-free optical biosensors represent a useful technology that enables direct observation of molecular interactions in real-time and allows the study of molecular systems

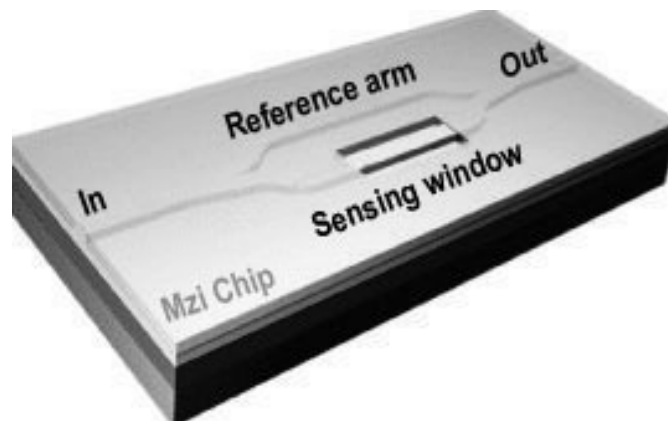
without the use of labels [15]. Optical label-free biosensors measure binding-induced refractive index changes and are typically based on transducers, such as integrated optical S-bends, Y-junctions, couplers, and interferometric structures such as Bragg gratings and Mach–Zehnders [16].

Integrated waveguide sensing has gained much popularity in the development of optical biosensors because of its potential to be practically deployed in various applications. Integrated optical devices for communication applications have become widely available, and these devices are conventionally designed and developed using common fabrication technologies and available dielectric materials. Therefore, there are numerous such device designs available for waveguide structures of optical transducers, some of which have been adapted for biochemical sensing [7]. This type of waveguide-based transducer is commonly referred in the literature as evanescent field sensors (EFS). EFS utilize the decaying or evanescent EM fields, which extends away from the core of a waveguide into the surrounding claddings, as shown in *Figure 1a*. Surface-Plasmon based optical biosensors, as shown in *Figure 1b*, can also be categorized into these types of sensors [6].



**Figure 1:** a) Waveguide concentration of wave energy in core layer. Exponential decay in cover/substrate layers. TE, TM, mono-/ multi-mode surface. b) TM mode propagating at a metal/dielectric interface with exponential decays. Adapted from [6]

The Mach-Zehnder interferometer is one of the most common optical transducers that can be adapted for biochemical sensing. MZI devices are made of two arms of waveguides, where one can be used as a reference arm and the other as a sensing arm, as shown in *Figure 2*. The sensing arm is the branch, which is exposed to the target analyte. This sensing waveguide is often functionalized with biochemical recognition elements, which captures the analyte from the carrier fluid, an aqueous buffer solution, and forms a thin 'adlayer' on top [14]. The MZI's reference and sensing waveguides are joined by a combiner to form the output. Detection is registered in real time through output power variations caused by phase differences between the reference and sensing arm. This phase difference is caused by the adlayer forming on the sensing arm [15].

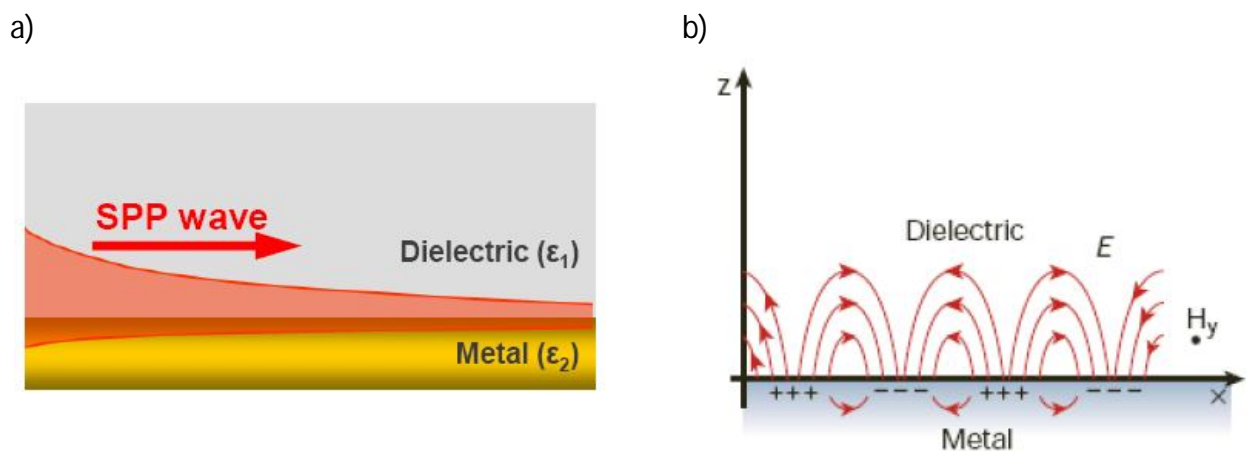


**Figure 2: Schematic diagram of a Mach-Zehnder Interferometer. Adapted from [14]**

## 1.2 Surface Plasmon Resonance for Biosensing applications:

Surface Plasmon Resonance (SPR) has become an extensively used sensing technique in physical, chemical, and biological investigations, due to its many advantageous features such as a high sensitivity to surface effects, real-time detection and analysis, high speed measurements, and label free detection [19].

Surface plasmon waves are polarized transverse magnetic (TM) waves that are confined on the interface between a metal and dielectric layer. Surface plasmons are also termed surface plasmon polaritons (SPP) due their modal wave nature. The TM waves can be described such that the magnetic vector is perpendicular to the direction of propagation of SPP waves and parallel to the plane of interface [20]. The propagation of SPP mode along a metal and dielectric interface is shown in *Figure 3*.

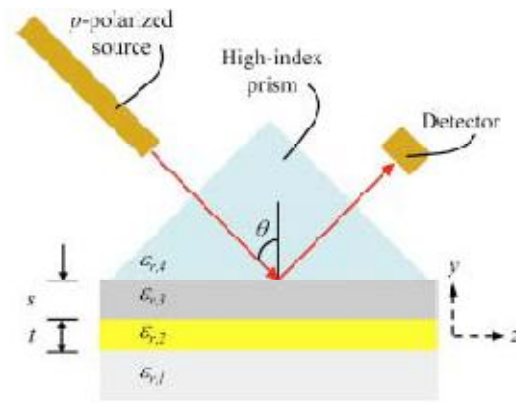


**Figure 3: a) Surface plasmons propagation at metal-dielectric interfaces b) The oscillations in the surface charge density along with the electric field lines [6].**

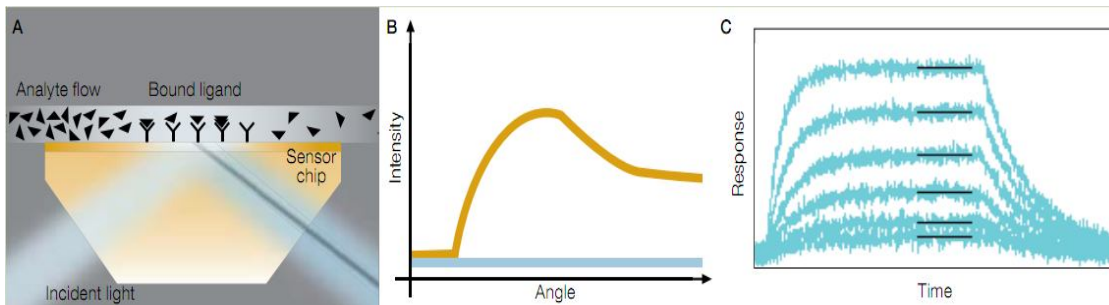
SPPs can be mathematically modeled via Maxwell's equations (including the boundary conditions) and Drude's model for the relative permittivity of a free electron gas [17, 18]. The wave number of the SPP ( $k_{sp}$ ) is readily derived and found to be dependent on the permittivity ( $\epsilon_{r,M}$ ) of the metal and dielectric material ( $\epsilon_{r,D}$ ). This means that for a specific excitation

wavelength, there is only one allowed SPP. The wave number of the SPP is larger than that of photons in the adjacent dielectric; therefore, means to increase the photon wave number are necessary to excite the SPP. One of the ways of exciting a SPP is to use a prism to couple incident light to the interface. Thus, SPPs are excited at a specific angle of incidence which corresponds to the proper longitudinal  $k_{sp}$ . This is shown in *Figure 4a* where the Otto and Kretschmann geometries [21, 22] are used to excite SPP. The Kretschmann configuration ( $s=0$ ) can be adapted to a biosensor by sandwiching the metal layer ( $\epsilon_{r,2}$ ) between the prism and the analyte solution ( $\epsilon_{r,1}$ ).

a)



b)



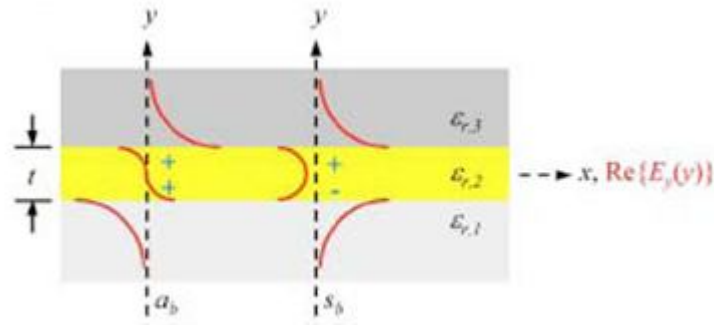
**Figure 4:** a) SPR Sensor – The Otto and Kretschmann configurations utilizing prism coupling to excite SPP.  $\epsilon_{r,1}$ ,  $\epsilon_{r,2}$ ,  $\epsilon_{r,3}$  is the relative permittivity of lower dielectric cladding, metal and upper cladding/analyte, respectively [23]. B) Illustration of the conversion of shift in SPR angle. a) As analyte binds to receptor molecules on the sensor chip surface, the reflected intensity produced by the SPP effect shifts. b) This intensity shift is measured in real time c) The resulting sensogram to quantitatively characterize the interaction. Adapted from [49].

The sensing is accomplished by noticing the change in angle at which there is a sudden drop in intensity of the reflected beam. The SPP coupling angle changes due to the introduction of the target analyte as it is captured at the fluid-metal interface. *Figure 4b* gives an illustration of the sensing mechanism of a SPP biosensor. Surface Plasmon sensing is currently one of the leading optical technologies used for biosensors due to its high sensitivity and low detection limits [24].

The one common function among all different types of label-free optical biosensors that must be implemented for surface sensing is the successful immobilization of receptor molecules. In other words, the receptor molecules have to be attached to the sensing surface [5]. This process involves the formation of covalent bonds between the surface and a bio-recognition element such as a protein (or antibody) [3, 4]. The modification of the sensing surface to introduce coupling functional groups such as -OH, -NH<sub>2</sub>, -COOH, and -SH is required to form these bonds. The sensing surface medium is what dictates the possible functionalization of the biosensor. In the case of metal surfaces, particularly gold, a self-assembled monolayer (SAM) of the -SH (thiol) group can be formed on the surfaces. The other end of the thiol chain can be specified to be -NH<sub>2</sub> or -CxHx for coupling onto enzymes or antibodies [25]. The ad-layer formed of receptor molecules and analyte on the surface affects the output optical properties of the sensing device.

### 1.3 Long-range surface Plasmon polaritons (LRSPPs):

In a planar 1-D geometry, where the metal layer is of finite thickness ( $t$ ), the waveguide has two modes of propagation termed  $s_b$  (symmetric bound) and  $a_b$  (asymmetric bound), as shown in *Figure 5*. If the metal film is relatively thin and bounded by dielectrics of similar refractive index, the  $s_b$  mode propagates with a low attenuation relative to the single-interface SPP; therefore, it is termed the long-range surface plasmon polariton (LRSPP). The modes are named according to their corresponding transverse electric field distribution and their bounded nature to the metal-dielectric interfaces. The corresponding mathematical derivations of mode propagation are found in [26]. All the excited modes on a surface plasmon interface are TM modes. The reason for this is that the TE modes are not allowed because the metal has a negative real relative permittivity.

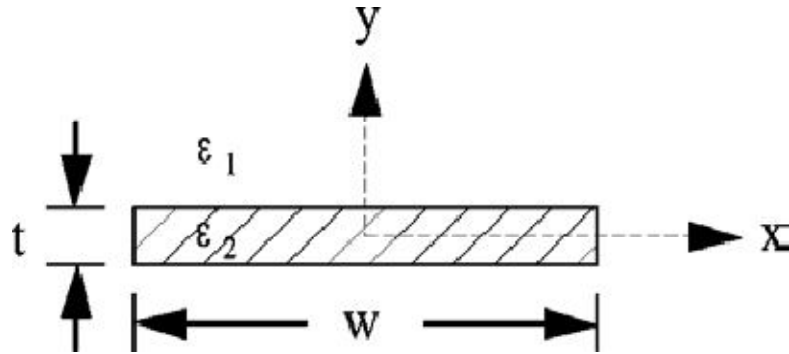


**Figure 5: Symmetrically cladded ( $\epsilon_{r,1} = \epsilon_{r,3}$ )LRSPP modes [23].**

The slab waveguide geometry shown above in *Figure 5* was transformed in [27] by limiting the width dimension of the metal film as illustrated in *Figure 6a*. This structure supports four 1st order modes termed as:  $ss_b^0$  (symmetric-symmetric bound) shown in *Figure 6b*,  $sa_b^0$  (symmetric-asymmetric bound),  $as_b^0$  (asymmetric-symmetric bound), and  $aa_b^0$  (asymmetric-asymmetric bound). The motive to design a finite width waveguide structure in [27] is that by

limiting the metal width, it is possible to provide lateral confinement thereby enabling integrated optical components.

a)



b)

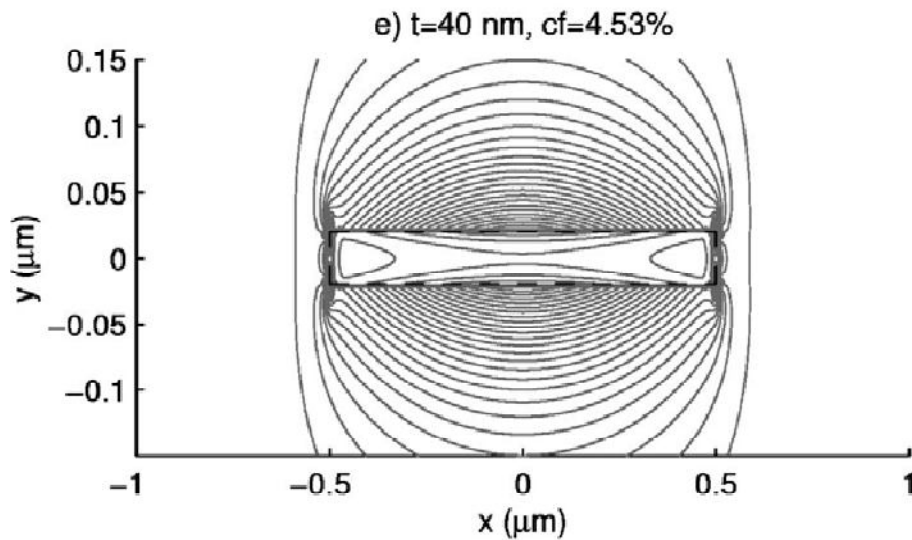
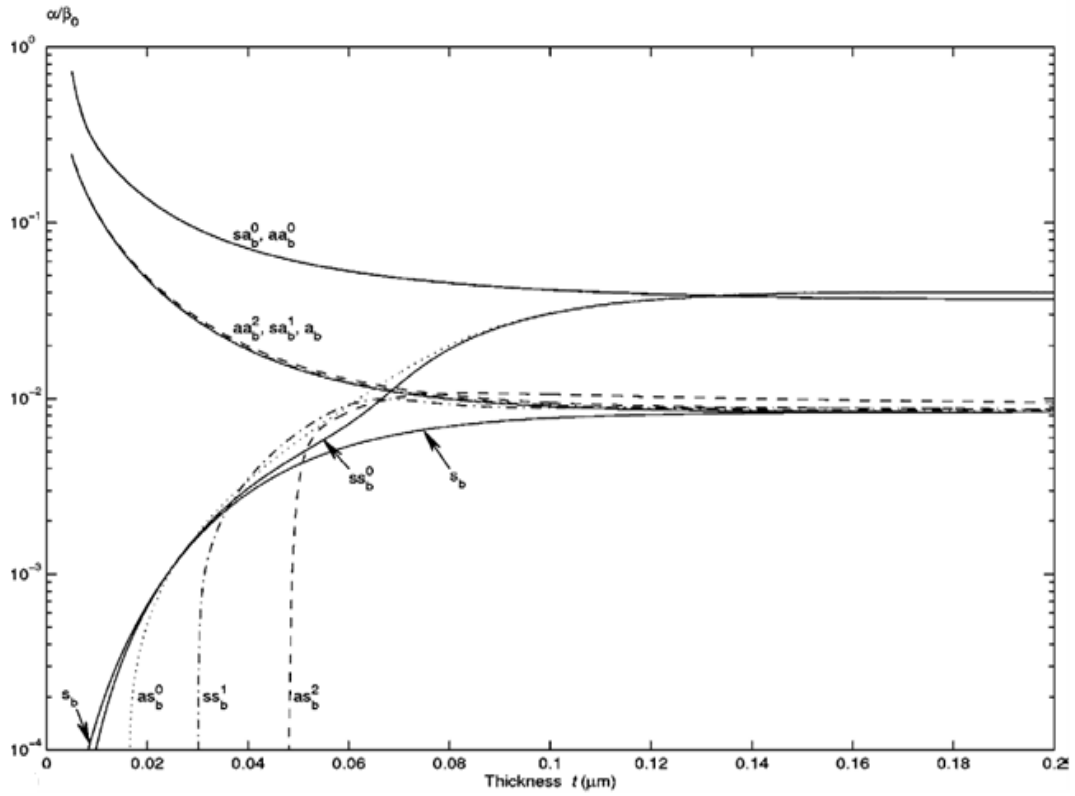


Figure 6: Stripe waveguide structure with finite width to support the fundamental LRSP mode [27].

The  $ss_b^0$  mode has an attenuation constant that is at least 1 to 2 orders of magnitude lower than that of single interface SPP. Hence, the SPP supported on a finite metal waveguide embedded in dielectric claddings is termed long range surface plasmon polariton mode or LRSP. The LRSP field distribution is Gaussian-like, as shown in *Figure 6b*, enabling efficient excitation by end-fire coupling.

a)



b)

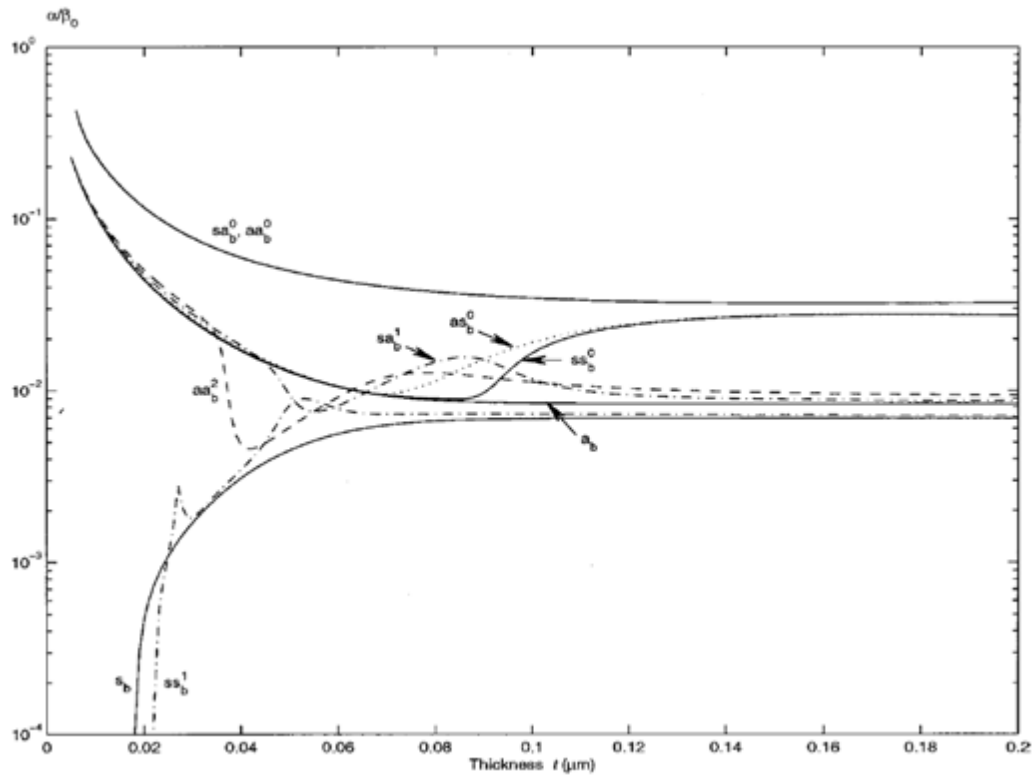


Figure 7: Various mode attenuation constants versus stripe metal thickness. (a) symmetric structure (b) asymmetric structure [27, 28].

#### 1.4 LRSPP sensing structure of interest:

Symmetric LRSPP structures are useful for biosensing applications because of the low attenuation of the LRSPP. Having a low attenuation is important because it increases the sensing length and thus the sensitivity of waveguide-based sensors [24]. As mentioned above, the waveguide-based Mach Zehnder Interferometer (MZI) sensor is useful for biosensing purposes. In [24], it was shown that optimal sensitivity values are limited by the propagation length of the MZI's sensing arm, which was limited by its propagation attenuation constant. In an ideal lossless waveguide scenario, the sensitivity increases along with increasing sensing lengths. Therefore, by lowering the propagating attenuation constant, the sensing length of the waveguide can be increased, which in turn increases the sensitivity of MZI devices. This is the main reason why a symmetric structure based LRSPP waveguide is desirable in order to fabricate practical LRSPP biosensors. In this structure it is important to implement the dielectric sandwich claddings to have equal values of permittivity ( $\epsilon_{r,1} = \epsilon_{r,3}$  in *Figure 5*).

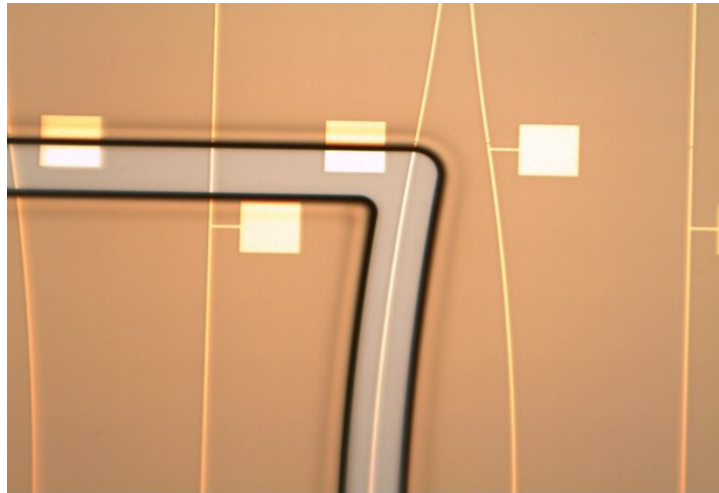
The symmetric metal stripe with the LRSPP propagating as a fundamental mode is of particular interest in the field of plasmonics, and is the main topic of this thesis. This plasmonic structure has been investigated experimentally, using *Au* or *Ag* as the metal for the stripe and various dielectrics as the claddings, including, for example,  $\text{SiO}_2$ , benzocyclobutene (BCB), UV-curable polymer (ZPU – Chemoptics), and perfluorocyclobutane (PFCB) [20]. Many passive optical elements such as S-bends, Y-junctions, couplers, and Mach–Zehnders have been fabricated using the symmetric metal stripe and operated in the LRSPP. Gold and silver are the metals most commonly adapted for surface plasmon sensing [21]. The real part of the dielectric constant of silver is large compared to gold; hence, it exhibits better surface plasmon

characteristics than gold. However, gold is a better choice in biosensors compared to silver because of its compatibility in aqueous environments (water, glycerol, Isopropyl alcohol, etc.), and lower reactivity towards bio-chemical agents [9]. Thus, gold is used as the metal layer for fabricating waveguides embedded in symmetric claddings because of its better features in biosensing environments.

The cladding material must be properly chosen so that it can be used to fabricate symmetric claddings for the biosensing structure and be index-matched to the sensing carrier fluid. The two possible choices for claddings for the metal waveguides are *CYTOP* and Teflon. The optical indexes of both materials are very close to the optical index of de-ionized water, and have been previously studied for slab LRSPS sensors. Teflon has an optical index of  $n_{Teflon} = 1.31$  and was used in [31] to perform sensing with a gold layer interface. *CYTOP* is a fluoro-polymer which has a refractive index of  $1.33$  ( $@ \lambda = 1310 \text{ nm}$ ). After comparing Teflon and *CYTOP* in different configurations and sensing experiments in [33], it was concluded that Teflon was better for bulk sensing, whereas *CYTOP* was better suited for surface sensing (immobilized analyte adlayer). The polymer adapted to fabricate devices in this thesis is *CYTOP*, because of our group's familiarity with the characterization and fabrication process with the material combined with the potential to attain desirable surface sensing results.

It is also desirable to fabricate devices where only selected surfaces are exposed for sensing, and have the rest of the devices embedded in *CYTOP*, which will maintain a perfect symmetric structure while shielding the MZI reference arms from the analyte. The main goal of this thesis is to present a process for fabricating LRSPS *Au* waveguides embedded in *CYTOP* with

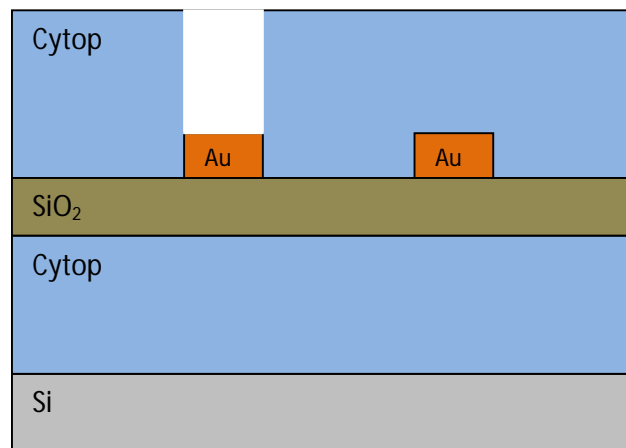
selected surfaces exposed for sensing. A microscope image of a final symmetric LRSSP supporting waveguide structure with biosensing capabilities is shown in *Figure 8*.



**Figure 8: Finished product after the successful implementation of microfluidic flow channels on symmetric embedded LRSSP waveguides for biosensing applications.**

To complete the LRSSP based biosensing structure, an analyte fluid flow system has to be employed on these devices. In order to introduce a target analyte to the biosensing surface, biochemical elements and reagents are usually transported in a liquid medium. Therefore, many biochemical sensors are designed to allow fluid delivery to the transducers. In the case of integrated structures, micro-fluidic channels are a popular choice for fluid delivery on the biosensing surface, and are implemented during the fabrication process. One common method of implementation is to fabricate the channels on a separate wafer and then bond it directly with the finished device. It has the advantage of having a separate fabrication process, hence not effecting the actual waveguide devices, due to different invasive chemicals and plasma reactants used in forming these channels on a substrate. However, it requires a lengthy and difficult process of aligning the channels with the waveguides on a separate wafer, and a costly and complicated bonding process to have a finished product. This is not necessary for the

structure of *Figure 8* because the specifically designed exposed regions formed by etching the CYTOP can act as fluidic channel cavities, and the thick CYTOP upper cladding with an etch-stop  $\text{SiO}_2$  layer makes it relatively immune to aggressive chemical and plasma agents used in fabricating these channels. All that is needed to encapsulate the fluid in the channels is a glass lid. Detailed implementation of this configuration will be presented in *Chapter 6*. The main feature implemented in this thesis is the introduction of thin  $\text{SiO}_2$  layer, which acts as a diffusion and etch-barrier layer (*Chapter 3*). Previous work done in CYTOP embedded LRSP waveguides in [35] and [51] did not have any barrier layer in between the claddings of the embedded metal waveguide. Creating precise micro-fluidic channels in such devices proved difficult due to over-etch into CYTOP bottom cladding from uncontrollable factors of RIE  $\text{O}_2$  plasma. Another issue encountered during the fabrication of those devices was deformation of metal waveguides due to solvent diffusion in bottom claddings during the upper cladding spin-coating process. Therefore, introduction of a  $\text{SiO}_2$  layer (*Figure 9*) is proposed in this thesis in hopes of getting rid of these fabrication problems.



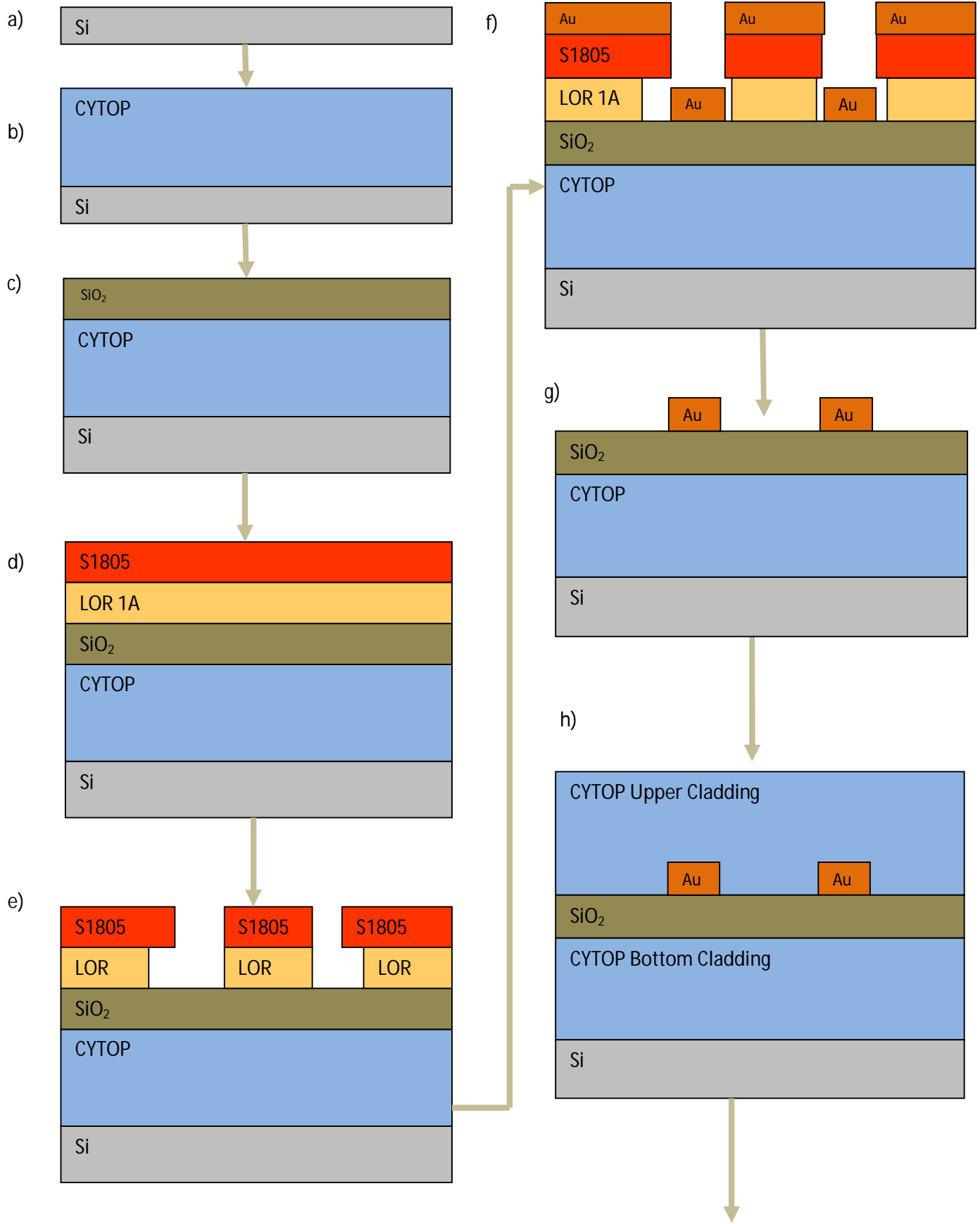
**Figure 9: Cross-sectional schematic of proposed LRSP based biosensor with  $\text{SiO}_2$  barrier layer.**

### 1.5 Process Flow:

The fabrication of LRSPP stripe devices in CYTOP with microfluidic channels is summarized in *Table 1*. The entire fabrication process and the finished products are 2" or 4" wafers ready to be diced for optical testing. More details on this process are provided in the forthcoming thesis. The flowchart following the table as (*Figure 10*) also schematically presents the process flow of the embedded LRSPP devices in CYTOP claddings with SiO<sub>2</sub> as a solvent diffusion barrier and etch-stop layer between the upper and lower claddings.

Step	Process	Detail
1	Removal of native oxide on Si wafer	Hydrofluoric Acid (HF) etch; chemical clean with Acetone, IPA, and DI water
2	Bottom Cladding	Layer-by-layer spin coating of CYTOP.
3	SiO <sub>2</sub> layer deposition	E-beam deposition of glass (SiO <sub>2</sub> ) layer
4	Lithography	Bi-layer lithography for device features.
5	Metal Deposition	E-beam deposition of Chromium and Gold.
6	Metal Liftoff	Strip metal from un-patterned surfaces.
7	Top Cladding	Layer-by-layer spin coating of CYTOP.
8	Lithography of micro-fluidic channels on top of CYTOP upper cladding.	Aligned to certain devices (metal-level) for proper placements of channels.
9	RIE etch of micro-fluidic flow channels	Dry etch using O <sub>2</sub> plasma chemistry.
10	Wafer Dicing	Wafers diced with a dicing saw.
11	Optical Characterization	Power cut-back measurements

**Table 1: Process flow of fabricating symmetric LRSPP waveguide structures**



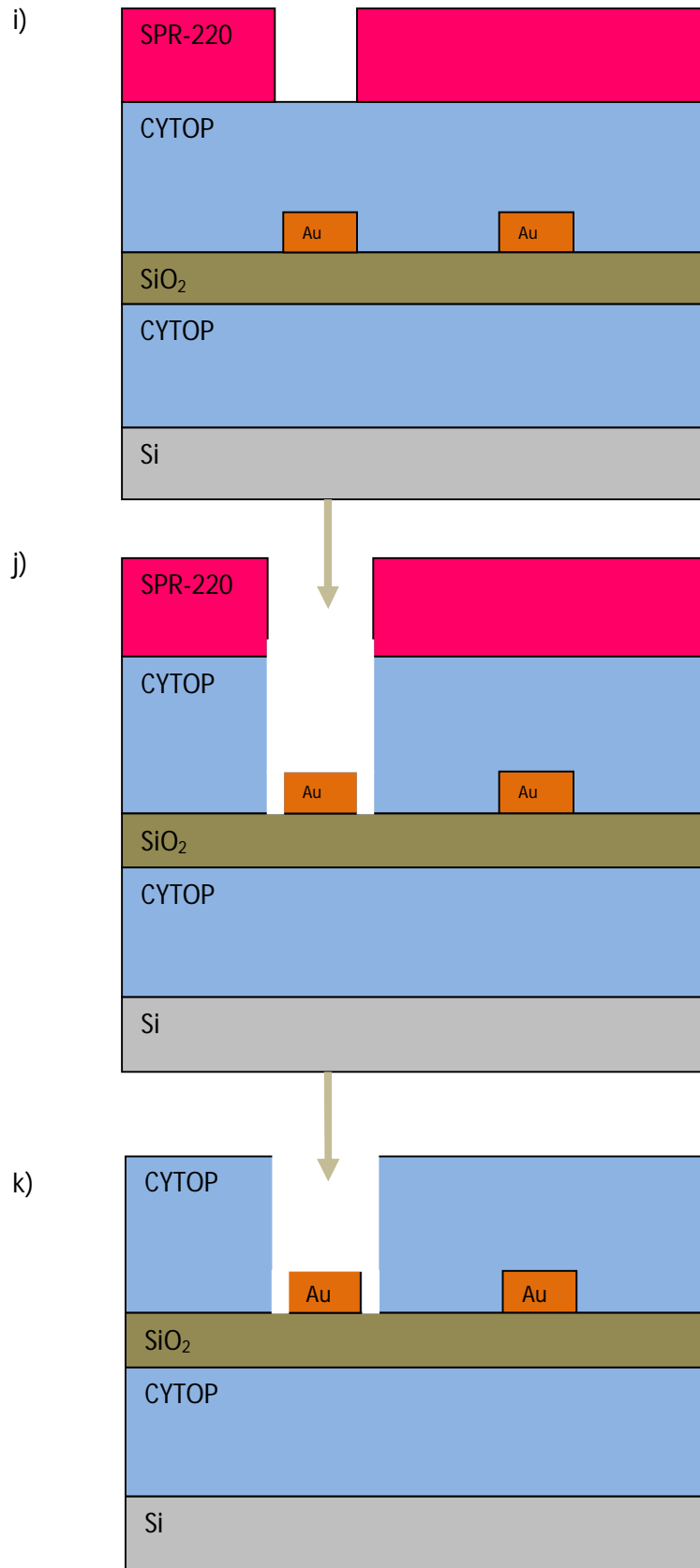


Figure 10 : Process flow of microfabrication of embedded LRSP waveguides with SiO<sub>2</sub> layer and micro-fluidic flow channels.

## 1.6 Thesis Structure

This thesis is structured in sequence with the fabrication steps of the biosensing device. *Table 1 and Figure 10* show the overall process flow of the micro-fabrication cycle of the fully-cladded plasmonic waveguides based optical biosensor devices. This thesis is split into 8 chapters as listed in the Table of Contents. Parts of the process flow chart above (*Figure 10*) will be expanded on for every level of fabrication process. This is done so that the thesis can be reviewed in order of the processes involved in fabricating the full device:

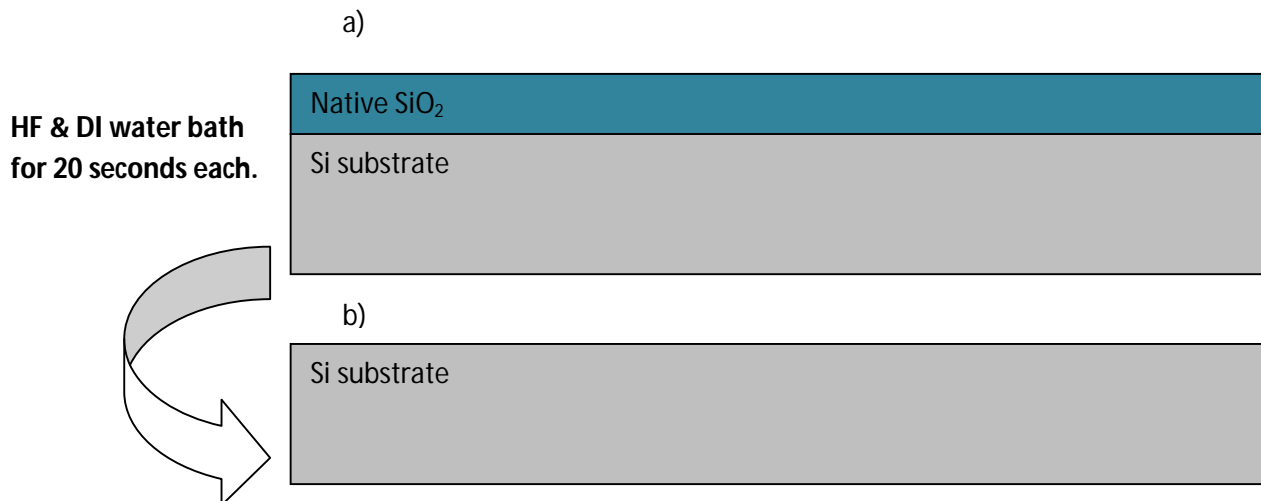
2. Bottom CYTOP cladding
3. Thin-film silicon dioxide layer
4. Device lithography and Metal (Cr + Au) deposition.
5. Upper CYTOP Cladding
6. Microfluidic channels (lithography / etching)
7. Optical characterization

Every chapter describes the detailed, finalized fabrication process for a specific level of the LRSPP device structure. Issues and problems encountered during the development of the fabrication processes are discussed. Solutions and analysis techniques used to address the problems are also presented and discussed for every level of the fabrication process. The last chapter describes the characterization setup used for the optical measurements, followed by measurements of straight waveguide attenuation and end-fire coupling loss to optical fibre, and the analysis of the results with discussion.

## 2 Bottom Cladding

### 2.1 Fabrication Process

The process of depositing *CYTOP* bottom cladding on a silicon wafer is described in *Table 2* and sketched in *Figure 12*. There are two grades of *CYTOP* used in the fabrication of the devices, which are the 5% M-grade (CTL-809M) and 9% S-grade (CTX-809SP2). Before, spin-coating the wafer with *CYTOP* cladding layers, there is an initial step of 'priming' the silicon (*Si*) substrate wafer. This process involves removal of the native thermal oxide ( $SiO_2$ ) through a static bath in 10% concentrated hydrofluoric acid (*HF*) solution for about 20-30 seconds. The wafer is then rinsed with Acetone and IPA separately, and washed in De-ionized (DI) water for 20 seconds. This step is shown in *Figure 11*. The wafer is then subjected to an organic cleaning process using Plasma-Preen cleaner for 5 minutes. The Plasma-Preen Cleaner/Etcher uses microwave energy (2.45 GHz) and  $O_2$ -induced plasma to clean organic and some inorganic contaminants from the *Si* substrate [60].



**Figure 11: (a) *Si* substrate wafer with native thermal  $SiO_2$  (b) bare *Si* substrate ready for spin-coating *CYTOP* layers.**

After priming the *Si* wafer, it is ready for the spin-coating process of CYTOP. CTL-809M (*M-grade*) CYTOP is used for the first layer coating of the bottom cladding of the bio-sensor structure. This particular grade of CYTOP is designed by the manufacturer<sup>1</sup> to adhere onto inorganic materials such as Si, SiO<sub>2</sub>, glass, etc. Therefore, a thin layer (0.4 μm) was first coated to act as an adhesion layer between the *Si* substrate and successive CYTOP layers. The specific spin speed conditions for spin coating the CYTOP are listed in *Table 2*. In order to attain the desired thicknesses, the packaged 9% *M-grade* CYTOP had to be diluted with its solvent (CT-SOLV180), which was also provided by the manufacturer<sup>1</sup>. Previous attempts of spin-coating thick, undiluted layers of *M-grade* CYTOP led to streaking and non-uniformity in thickness [35].

The initial concentration of *M-grade* CYTOP is 9% CYTOP and 91% solvent by weight. To reduce the concentration to 5% CYTOP, a digital scale was used to measure solvent in order to dilute the solution. Spin-coat curves for both concentrations were provided by the manufacturer<sup>1</sup>. After the spin-coating, the wafer was soft-baked at 50°C for 30 minutes. This soft-bake step is done to evaporate the solvent mixed-in with the CYTOP solution, before spin-coating additional CYTOP layers. This step was followed according to the instructions provided by the manufacturer<sup>1</sup>.

After the first adhesion layer (5% *M-grade*) had been coated and soft-baked, additional CYTOP layers were spin-coated sequentially to acquire the desired thickness for the bottom cladding. The CTX-809SP2 (*S-grade*) CYTOP was used to coat thicker layers. The main reason behind the switch from *M-grade* to *S-grade* CYTOP was experimentally determined as each behaves differently in moisture. The *M-grade* CYTOP solutions would spoil in water. The main

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<sup>1</sup> CYTOP was obtained from Asahi Glass Co.[38].

reason for this behaviour is that the *M-grade* CYTOP is designed by the manufacturer to promote *Si* substrate adhesion. This is why silane groups ( $\text{SiH}_4$ ) are included in this composition of CYTOP. The silane groups are known to bind with water. Therefore, *M-grade* CYTOP claddings degrade in water over long periods of time. The *S-grade* CYTOP does not contain silane agents, so it is used as the bulk cladding layer material for this fabrication process, as it is ideal to be used as cladding material in aqueous solutions. Using different CYTOP grades should have no optical consequence as long as the bulk *S-grade* cladding is thicker than  $7\ \mu\text{m}$  [35]. In this micro-fabrication process both of these conditions are satisfied, as shown in the thickness and optical index measurements reported in *sections 2.2 and 5.1*. The 9% *S-grade* CYTOP was repeatedly spun, normally 2 additional layers, and soft-baked until the desired thickness was achieved (*Figure 12b*).

The last CYTOP layer is a thin 5% *M-grade* layer instead of the 9% *S-grade* layer. The main reason for this is to promote the adhesion between the CYTOP bottom cladding and the thin evaporated Silicon dioxide layer (*Chapter 3*), because the Silane groups in *M-grade* are known to bind well with  $\text{SiO}_2$ . Another advantage of using the thin 5% *M-grade* layer is to planarize the top surface to be as smooth as possible. After the last layer was coated and soft-baked, the wafer was subjected to a 'hard-bake' process. The hard-bake was performed at  $200\ ^\circ\text{C}$  for 1 hour and 30 minutes. In order to have smooth thermal transition and proper evaporation of the solvent, the hard-bake is preceded by a temperature ramp from  $50\ ^\circ\text{C}$  to  $200\ ^\circ\text{C}$  for 1 hour. The wafer underwent a total of 2.5 hours of hard-bake. The hard-bake completely evaporates all the solvent [38] and brings the CYTOP claddings above the glass-transition temperature ( $T_g = 107\ ^\circ\text{C}$ ) to improve structural strength for latter parts of the fabrication [51].

Step #	Process Description	Details
1	Strip native SiO <sub>2</sub> layer by dipping the fresh <i>Si</i> wafer in HF.	20 seconds HF dip with light agitation; Rinse the wafer with Acetone and IPA; 20 seconds DI water dip.
2	Dehydration and Plasma-Preen cleaning to prepare the wafer for bottom-cladding CYTOP process.	Plasma-Preen organic clean for 5 minutes.
3	Spin coat 5% CTL-809M CYTOP on <i>Si</i> wafer as an adhesion layer between <i>Si</i> and thicker CYTOP layers.	Spin Speed: 500 RPM for 10 seconds followed by 1000 RPM for 20 seconds. Thickness: ~0.40 μm
4	Soft bake the wafer on hot plate for solvent evaporation.	@ 50°C for 30 minutes.
5	Spin coat 9% CTX-809SP2 (S-grade Cytop)	Spin Speed: 1000 RPM for 10 seconds, followed by 1500 RPM for 20 seconds. Thickness: ~ 2.65 μm
6	Soft bake the wafer on hot plate for solvent evaporation.	@ 50°C for 30 minutes.
7	Repeat Steps 5 and 6 twice to attain the desired thickness.	
8	Spin coat 5% CTL-809M CYTOP on <i>Si</i> wafer as an adhesion layer between <i>Si</i> and thicker CYTOP layers.	The top layer is diluted M-grade Cytop for adhesion purposes.
9	Soft bake the wafer on hot plate for solvent evaporation.	@ 50°C for 30 minutes.
10	Hard-bake for complete solvent evaporation.	Temperature ramp of 150°C / hr, from 50°C to 200°C in 1 hour. Hold @ 200°C for 1.5 hours.

**Table 2: Fabrication process flow for bottom CYTOP claddings.**

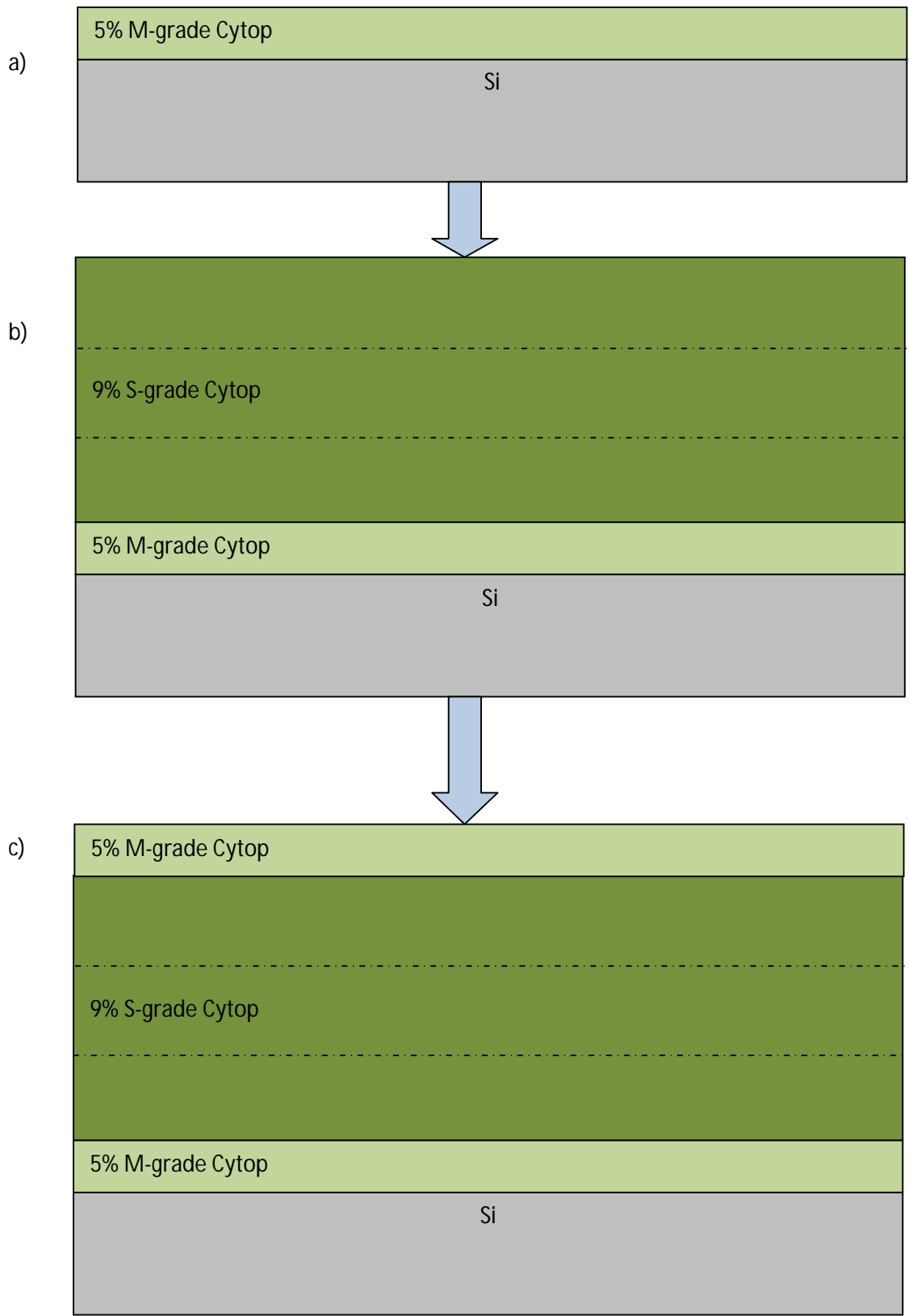


Figure 12: Spin coating process of lower CYTOP cladding.

## 2.2 Thickness, refractive index, and surface roughness check of bottom CYTOP cladding

The values of the coated CYTOP thickness and optical index were measured using a prism coupling tool called the *Metricon 2010/M*. The *Metricon* is an instrument which couples laser light through a prism onto deposited material. There are two wavelength options available for the measurement, which are  $\lambda_1 = 632 \text{ nm}$ , and  $\lambda_2 = 1300 \text{ nm}$ . By varying the coupling incidence angle, different waveguide modes can be excited, which translates into a change in intensity of the reflected light from the material. The changes in intensity of light due to the variation in incidence angle are monitored and recorded with a photo-detector. The software of *Metricon* finds the angle of minimum intensities and calculates the thickness and optical index of the material. The data that needs to be entered in the software for appropriate measurements are the substrates optical index for the wavelength of the laser used for measurements. The index of refraction for Si at  $\lambda = 632 \text{ nm}$  is 3.882. The reason this wavelength was chosen is that it allowed for measurement of CYTOP thicknesses below  $0.5 \mu\text{m}$ . At longer wavelengths it becomes very hard to measure small thicknesses ( $< 0.5 \mu\text{m}$ ), as there are not enough modes generated to do accurate measurements of thickness and optical refractive index.

Various CYTOP claddings were measured for thickness and optical index using the *Metricon*. The measurements were done for each layer of CYTOP cladding because the developed cladding process involved different grades of CYTOP, different concentrations, and different spin speeds. The measured results were compared with the manufacturer's data [38] (thickness only) in *Table 3*. It can be noted that the actual thicknesses are about  $0.05\text{-}0.1 \mu\text{m}$  thinner than the target thicknesses provided by the manufacturer<sup>1</sup>. This discrepancy can be

attributed to subtle factors such as environment temperature, humidity, shelf life, and the accuracy of the spinner [51]. The spin-coating process of CYTOP bottom cladding process yielded about 9.3  $\mu\text{m}$  of CYTOP thickness. This value is much thicker than the theoretical requirement ( $>7\mu\text{m}$ ) for LRSPP modes [35]. Slightly above target thickness in claddings of embedded waveguides will not affect the end-result optical performance of the devices.

# of 5%M-Grade layers	# of 9% S-Grade layers	Measured index	Measured Thickness ( $\mu\text{m}$ )	Manufacturer's Target Thickness ( $\mu\text{m}$ )
1	0	1.3386	0.4073	0.45
1	1	1.3385	3.0573	3.15
1	2	1.3384	5.8651	5.85
1	3	1.3384	8.5005	8.55
2	3	1.3385	8.908	9.0

**Table 3: Thickness and optical index measurement of CYTOP claddings. Measured with *Metricon 2010/M* prism waveguide coupling at  $\lambda = 632.8 \text{ nm}$ .**

The surface roughness of the CYTOP bottom cladding is another important criteria that must be examined, because any roughness will be carried over to the  $\text{SiO}_2$  layer deposition as well as the metal waveguide when it is deposited on top of the cladding. The theoretical studies for the design of plasmonic waveguides have shown that the  $\text{SiO}_2$  thickness and the metal thickness are critical for the waveguide performance. Therefore, it is desirable to fabricate the CYTOP surface to be very flat and smooth, and within acceptable scales of roughness ( $\sim 1 \text{ nm rms}$ ).

Atomic force microscopy (AFM) was performed<sup>2</sup> to measure the surface roughness of the bottom CYTOP cladding in [51]. This is a technique which involves a cantilever probe brought within close proximity of the surface under test. Atomic forces between the cantilever tip and the surface produce the deflection data [12]. Therefore, surface profile images can be

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<sup>2</sup> Atomic Force Microscopy was performed by Surface Science Western at University of Western Ontario, Canada.

constructed by scanning the probe across entire surfaces. Results from AFM of the CYTOP surface roughness were determined to be 0.81 nm RMS, and 0.60 nm average. Surface roughness RMS value less than 1 nm is acceptable for bottom CYTOP cladding according to previous studies [40].

### 3 SiO<sub>2</sub> layer as a solvent diffusion barrier and etch stop layer

#### 3.1 Introduction to SiO<sub>2</sub> layers.

Silicon dioxide films are used in a variety of applications in the electronics and photonics industries, with a corresponding range of desired properties. The requirements for successful implementation of these films include ultra-high purity and uniform deposition over large areas [53].

The application of SiO<sub>2</sub> films is rapidly growing in the field of optical integrated circuits [53]. Silicon dioxide films are used in the photonics applications for the formation of dielectric claddings, wavelength selective optical filters, and mirrors [54]. The relatively low index-of-refraction ( $n_{\text{SiO}_2} \sim 1.46$ ) compared with other transparent oxides is useful as the low index of refraction material in optical structures [55].

SiO<sub>2</sub> films for optics applications must be of high purity and have low surface roughness. Any impurity in the SiO<sub>2</sub> layer causes changes in refractive index, which in turn, causes problems in light guiding applications. Pure fused silica is transparent over a wide spectral range (0.17-8.0  $\mu\text{m}$ ) [52]. Impurities such as OH<sup>-</sup> produce absorption bands ( $\sim \lambda = 1400\text{nm}$ ), and may interfere with the telecommunications wavelength ( $\lambda = 1550\text{ nm}$ ) band [55]. Surface roughness of the silicon dioxide layer embedded in an integrated optical device causes an undesirable scattering of light. The surface scattering coefficient ( $s$ ) scales with the ratio of surface roughness ( $\sigma$ ) to optical wavelength ( $\lambda$ ) (Eq. 1)[53]. Therefore, one of the criteria of deposited SiO<sub>2</sub> films is to have low surface roughness ( $< 1\text{nm RMS}$ ).

$$s \sim R \left[ \frac{4\pi\sigma}{\lambda} \right]^2 \quad \text{—————} \quad \text{Eq. 1: Surface scattering coefficient [53]}$$

### 3.2 Modeling of SiO<sub>2</sub> layer implementation in symmetric LRSPP waveguides:

The effects of a SiO<sub>2</sub> layer on the propagation of the LRSPP mode in fully embedded metal waveguides in CYTOP (as per *Figure 9 in section 1.4*) were modeled by Dr. Chengkun Chen [56]. His results are shown in *Figure 61 in Appendix A*. The indexes of refraction used for the design and simulations of symmetric LRSPP waveguides at wavelength of 1310 nm are:

- $n_{\text{SiO}_2} = 1.4468$
- $n_{\text{CYTOP}} = 1.3348$
- $n_{\text{Au}} = (-86.080000 - 8.322000 j)^{0.5}$

The graphs in *Figure 61 in Appendix A* are used to determine the target SiO<sub>2</sub> and metal (*Au + Cr*) thicknesses for the fabrication process. There is a horizontal red dashed line plotted on each graph of *Figure 61*. These lines highlight the value of the ordinate for the nominal waveguide design that does not have a SiO<sub>2</sub> layer and for which the waveguide layout was produced. It is desirable to use the same waveguide layout so the thicknesses of the SiO<sub>2</sub> and *Au* layers must be selected such that these highlighted values are simultaneously respected (as closely as possible).

There are two separate categories for these graphs. *Figures 61 a and b* are to model straight LRSPP waveguides, and calculate the effective index and Mode Propagation Attenuation (MPA) with different thicknesses of SiO<sub>2</sub> layer. *Figures 61 c and d* are used to model curved LRSPP waveguides, and are used to take into account the bending losses in curved waveguides such as Mach-Zehnder, S-bends, and Y-junctions. The field plots of the LRSPP fundamental mode for different thicknesses of metal and oxide was also simulated. The generated field plots for straight and curved waveguides are shown in *Appendix A, Figures 62 and 63*.

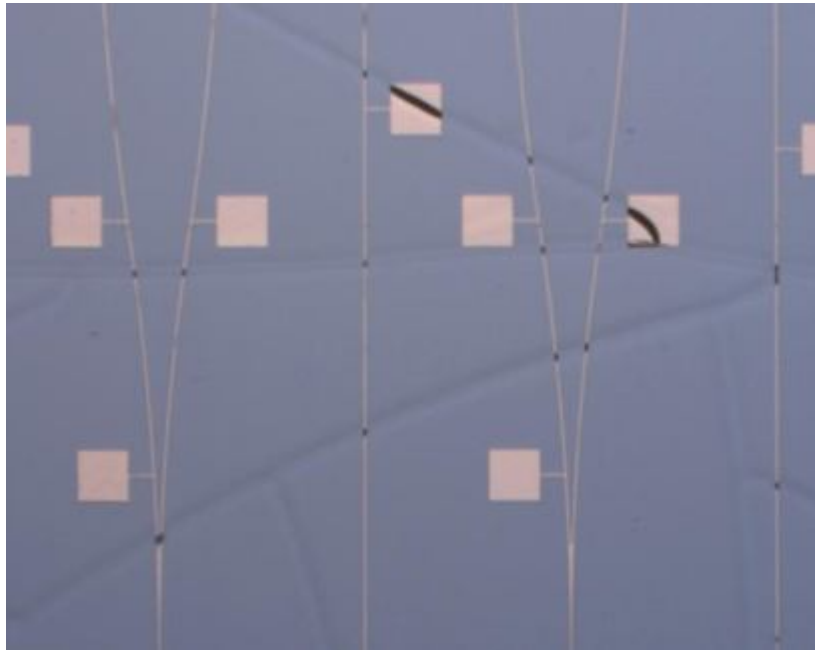
After observing these simulation results, two different sets of thicknesses for metal and SiO<sub>2</sub> layers were selected. The first set that was tested consisted of  $t_{\text{SiO}_2} = 20 \text{ nm}$  and  $t_{\text{metal}} = 30 \text{ nm}$ . The expected MPA with these thicknesses is  $\sim 5 \text{ dB/mm}$  in straight embedded LRSPP waveguides. But, the relatively thin SiO<sub>2</sub> layer ( $t = 20 \text{ nm}$ ) proved to be very fragile during the O<sub>2</sub> plasma etching step used to create the micro-fluidic channels. The effects of the plasma on a very thin oxide layer are evident in *Figure 13*. The thinner oxide film also proved to be very sensitive towards the lithography process, as it failed to provide the desired patterning of waveguides due to potential issues related to surface adhesion and sensitivity to MF 321 developer solution used to etch the lift-off resist and the photoresist. These issues are discussed in detail in Chapter 4 of this thesis.



**Figure 13 : Cracking of oxide layer due to aggressive O<sub>2</sub> plasma.**

Another problem encountered with a thin 20 nm thick layer of SiO<sub>2</sub> was that during some upper cladding spin-coat trials, the SiO<sub>2</sub> layer failed to be stable due to potential problems relating to *CYTOP* solvent diffusion as well as bake temperatures and timings. The

hard-bake process for the upper-cladding is done at 90°C (below the  $T_g = 107^\circ\text{C}$  of CYTOP) and held for a long duration of 4 hours. It is possible that extended thermal excursions (required for reasons described in *section 7.1*) crack and destroy the relatively thin  $\text{SiO}_2$  layer as shown in *Figure 14*. Such cracks are detrimental to the embedded LRSPP waveguides.



**Figure 14: Crack on 20nm thick  $\text{SiO}_2$  layer due to extended thermal exposure.**

The thicknesses of  $t_{\text{SiO}_2} = 30 \text{ nm}$  and  $t_{\text{metal}} = 30 \text{ nm}$  provided more desirable fabrication results as well as proved to be stable under  $\text{O}_2$  plasma etching process as shown in *Figure 54* of completed LRSPP waveguides structure. According to the simulations (shown in *Figure 61* and b of *Appendix A*) for straight waveguides, using the oxide thickness of  $\text{SiO}_2 = 30 \text{ nm}$  (cyan blue line), and metal thickness of 30 nm, the expected MPA (mode propagation attenuation) is 6 dB /mm in embedded LRSPP waveguides.

### **3.3 Techniques of thin SiO<sub>2</sub> layer deposition:**

Deposition of a thin SiO<sub>2</sub> layer can be accomplished by different techniques widely practised in different applications of electronics and photonics. Each one has its advantages and disadvantages over the other, which is summarized below.

#### **3.3.1 Oxidation:**

One of the options available for depositing the SiO<sub>2</sub> layer in the fabrication lab is to use the thermal oxidation technique, which is deposited by the high temperature oxidation of the surface of a substrate. SiO<sub>2</sub> layers with high purity and uniformity can be obtained by this technique. The main drawback to this method of depositing SiO<sub>2</sub> is that production of high quality films requires temperatures of ~800-1200°C [54]. These high temperatures will result in the destruction of the CYTOP used in the bottom cladding layer. Therefore, due to the thermal restrictions required to fabricate the LRSPP waveguide structures using CYTOP as claddings, this method of depositing oxide layer on CYTOP is not practical.

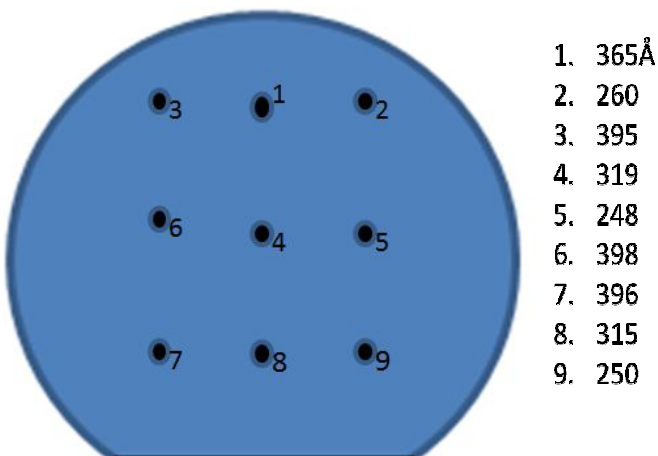
#### **3.3.2 Chemical Vapour Deposition (CVD)**

CVD is a common technique used in the growth of SiO<sub>2</sub> layers for optical applications. The desired material (SiO<sub>2</sub>) is deposited by supplying specific precursor gases (e.g. SiC<sub>12</sub>H<sub>2</sub> and N<sub>2</sub>O for SiO<sub>2</sub> growth) to a heated surface [52]. The temperatures required for deposition of high quality SiO<sub>2</sub> films using CVD reach ~ 700-900 °C [54]. Plasma-enhanced CVD technique allows the deposition of SiO<sub>2</sub> with lower temperatures (~250-400 °C) [54]. However, ion-bombardment during the plasma phase causes defects in the deposited films resulting in non-uniform and

rough surfaces of the deposited SiO<sub>2</sub> film [55]. Due to these issues, this method of depositing SiO<sub>2</sub> was avoided in this fabrication process.

### 3.3.3 Sputtering

Sputtering of quartz glass using a plasma-discharge is also a popular technique to deposit SiO<sub>2</sub> layers in optical devices [52]. Energetic ions bombard the surface of a bulk target, leading to the emission of particles from the target surface. The sputtered particles are deposited on a nearby substrate. The sputtering technique allows for the deposit of SiO<sub>2</sub> at low temperature (~50°C - 90°C) [52], which is sufficiently low enough to be adapted as a deposition technique for the fabrication process of LRSPP waveguides. This method of depositing the SiO<sub>2</sub> layer was tried and tested, but resulted in very non-uniform SiO<sub>2</sub> layers. *Figure15* shows the thicknesses of a SiO<sub>2</sub> layer on a silicon wafer, deposited through sputtering. The sputtering process was performed for 5 minutes under the 25sccm flow of Argon and 10 sccm flow of oxygen.



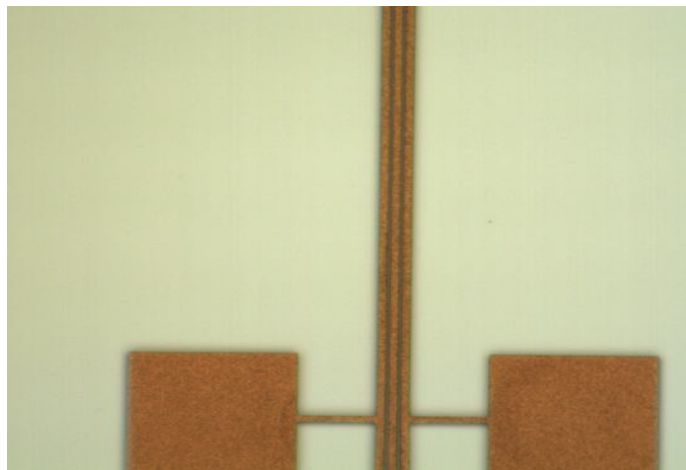
**Figure 15 : Measured thickness of SiO<sub>2</sub> at different parts of the wafer, deposited on silicon using sputtering technique.**

As it can be seen through the above thickness measurements, the sputtered oxide was very non-uniform throughout the 2" wafer. It was also observed that the surface profile of the sputtered oxide is not very smooth. This was observed after the e-beam deposition of gold on the sputtered oxide layer, as the metal waveguides turned out to be very rough even though a chrome adhesion layer was used to have better adhesion between the SiO<sub>2</sub> and gold layer. The following figures (*Figure 16 a, b*) illustrate the roughness incurred due to a non-uniform sputtered oxide layer. Therefore, it was concluded that sputtering of SiO<sub>2</sub> layer was not the best technique for the biosensor fabrication.

a)



b)



**Figure 16 a, b: Poor adhesion between sputtered oxide and (Cr+Au) waveguides.**

### 3.4 Deposition of SiO<sub>2</sub> using e-beam evaporation of Quartz:

Alternatively, e-beam evaporation can be used to deposit the SiO<sub>2</sub> layer. In the evaporation process, a block of the material (Quartz) is deposited by heating it using an electron-beam to the point where it starts to evaporate. This process takes place inside a vacuum chamber, enabling the molecules (SiO<sub>2</sub>) to evaporate in the chamber, where they then condense on all surfaces [61], as shown in *Figure 17*. The e-beam evaporation gave desirable results in terms of the target thickness and uniformity as well as surface roughness, which are shown in thickness and roughness check in *section 3.6*. *Table 4* summarizes the steps employed to deposit a thin layer of SiO<sub>2</sub> on CYTOP. It was not possible to verify the thickness of the SiO<sub>2</sub> layer deposited on top of thick CYTOP bottom cladding due to inconsistent results measured through ellipsometry with wafer composition of (from bottom to top) Si / CYTOP / SiO<sub>2</sub>. Thereafter, a bare silicon wafer was placed inside the e-beam evaporator as a reference to measure the exact thickness of the deposited SiO<sub>2</sub>, which enabled accurate and consistent ellipsometry measurement readings.

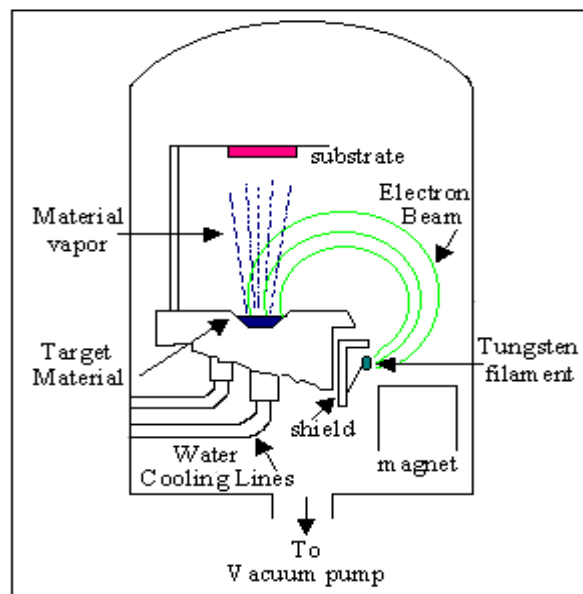


Figure 17: Schematic of commonly employed E-beam evaporator. Adapted from [62].

Step #	Process Description	Details
1	Ash CYTOP wafer in O <sub>2</sub> plasma to roughen the surface	15 seconds under O <sub>2</sub> plasma.
2	Rinse the CYTOP surface with Acetone and Isopropyl alcohol (IPA) followed by immersion in DI water bath.	To clean any impurities on CYTOP surface to promote better adhesion.
3	Load the target material (Quartz) in the crucible of e-beam evaporator.	Make sure, Quartz material is evenly spread.
4	Load the wafers in the evaporator and set the desired thickness and deposition rate. Load one blank 2" wafer with bare silicon to measure the thickness of SiO <sub>2</sub> layer.	Thickness: 30 nm Deposition rate: 10 Å/ second.
5	Perform e-beam evaporation and remove the wafers. Measure the thickness.	Measure the thickness using ellipsometry to ensure that the desired thickness is achieved.

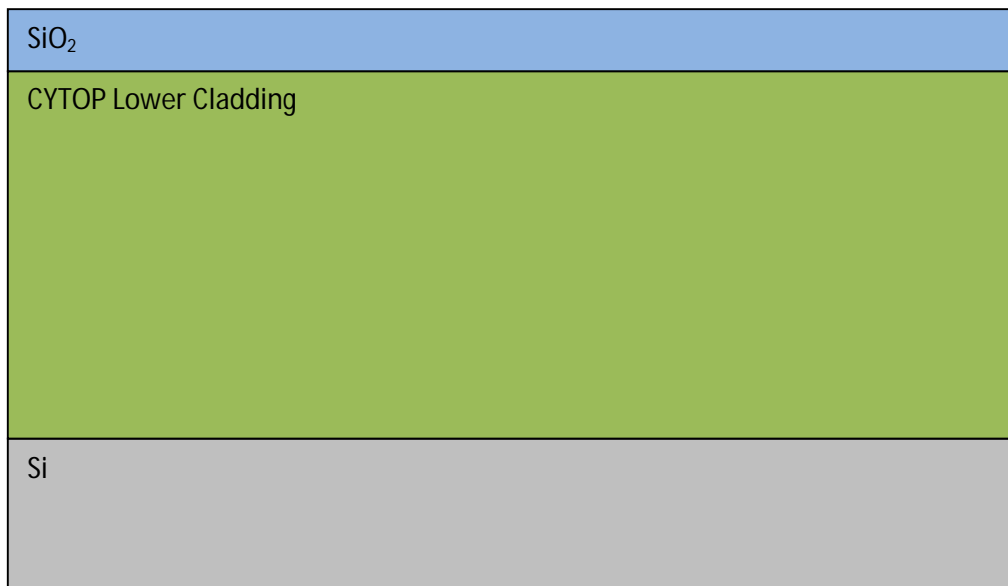
**Table 4: Process of e-beam evaporation of Quartz to deposit a thin SiO<sub>2</sub> layer.**

### 3.5 Purpose of depositing a thin SiO<sub>2</sub> layer

Silicon dioxide (SiO<sub>2</sub>) is used in this microfabrication process for two main reasons, which are:

1. As a solvent diffusion barrier during the deposition of the top CYTOP cladding.
2. Etch-stop layer during the flow channel etch process.

The Oxide layer is deposited after the bottom cladding curing process. *Figure 18* gives an illustration of an oxide layer on top of the CYTOP bottom cladding:



**Figure 18: Schematic of evaporated SiO<sub>2</sub> layer on bottom CYTOP cladding.**

### 3.5.1 SiO<sub>2</sub> as a Solvent Diffusion layer:

In previous micro-fabrication methods, there was no solvent diffusion barrier layer used, so during upper cladding formation the solvent would diffuse into the bottom CYTOP cladding and deform the metal waveguides [51]. This is due to the fact that cured CYTOP remains vulnerable to its solvent (the material does not cross-link during curing); therefore, CYTOP cannot be cured in the conventional sense. The hard-bake process, which will be explained in detail in *section 5.1* related to the upper cladding spin-coating process, introduced some problems with the process explained in [51]. The hard-bake process in [51] simply ensures that the CYTOP cladding is dry and robust as there is no chemical reaction during the bake. As a result, when new layers of CYTOP were coated, the mixed-in solvent diffused to the bottom cladding layers underneath the metal waveguides. This became problematic when the wafer was introduced to the intermediate soft-bake step between layers. When this bake evaporated the solvent, the leaking gas pressure potentially damaged the waveguide from underneath causing ripples as shown in *Figures 20 a and b*. In addition, when the soft-bake temperature is too low, or if there is a lot of trapped solvent, the bottom CYTOP claddings start to form cracks as shown in *Figures 19 a and b*. Therefore, a SiO<sub>2</sub> diffusion barrier layer is introduced in the fabrication process to eliminate this problem, and have uniform and perfectly defined metal waveguide structures with no deformation after spin-coating of upper cladding CYTOP. The introduction of SiO<sub>2</sub> as a barrier layer between the sandwich claddings of CYTOP results in very smooth and damage-free embedded metal waveguides as shown in *Figures 21 a and b*. Additionally, there were no effects found that suggested that there was any solvent trapping in the upper CYTOP cladding.

a)



b)

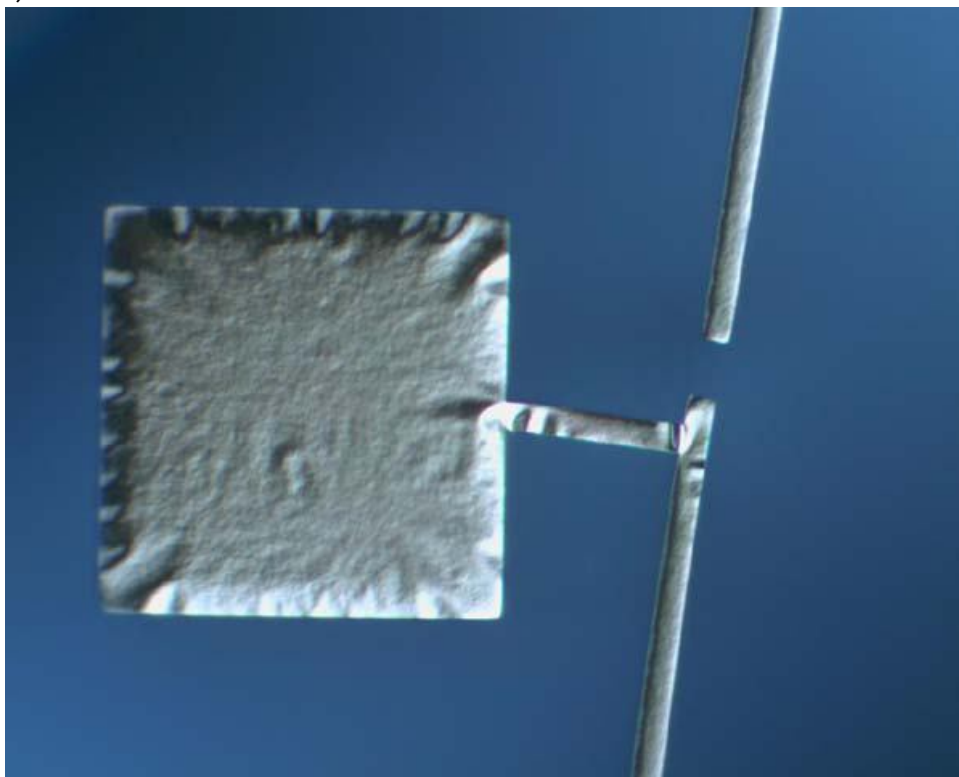


Figure 19 a, b: Waveguide deformation due to thermal expansion of top CYTOP cladding (a) 25x magnification (b) 100x magnification [51].

a)



b)

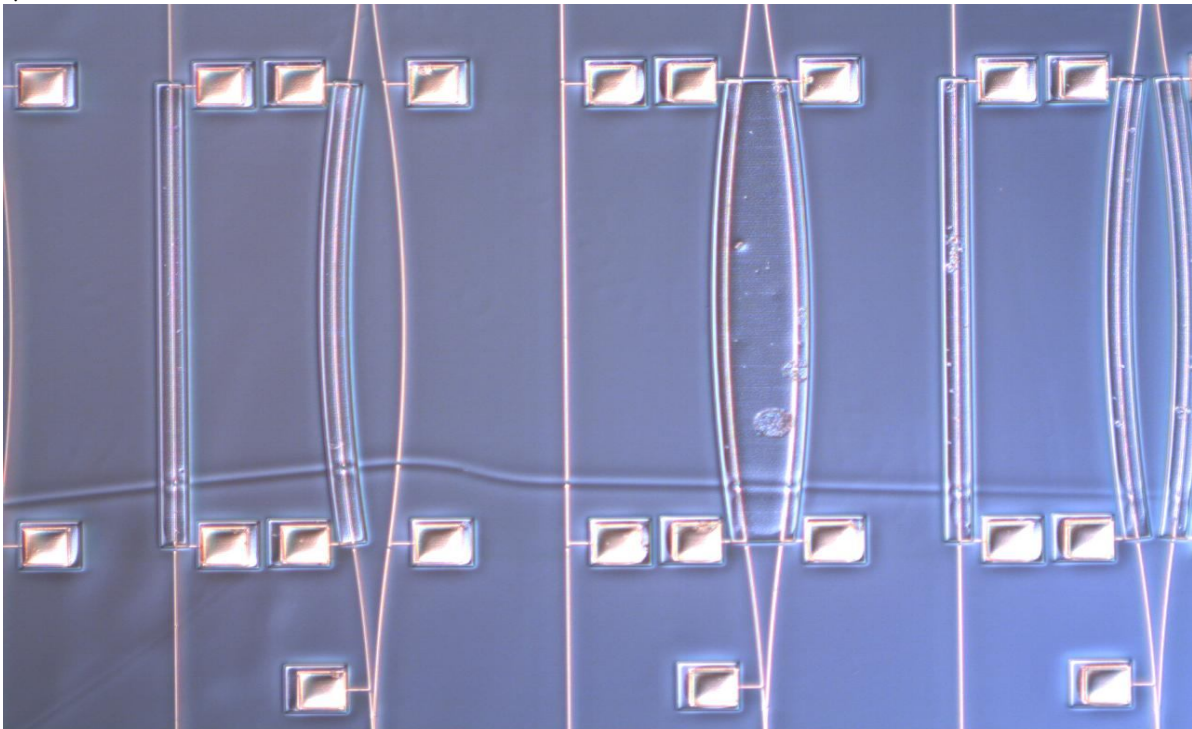
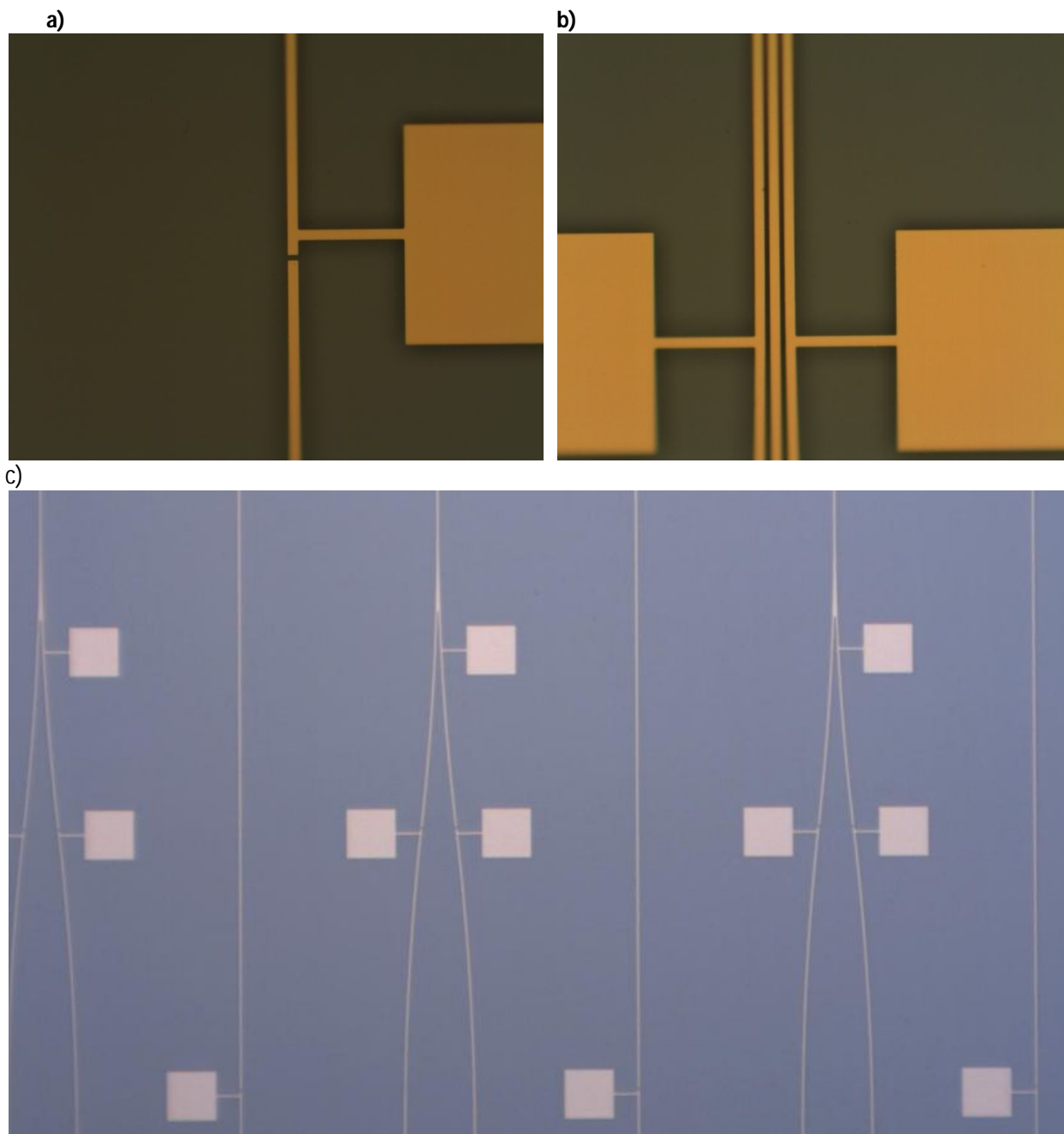


Figure 20 a) Solvent trapping in lower cladding b)'scratch' lines and roughness due to solvent diffusion in lower cladding [51].



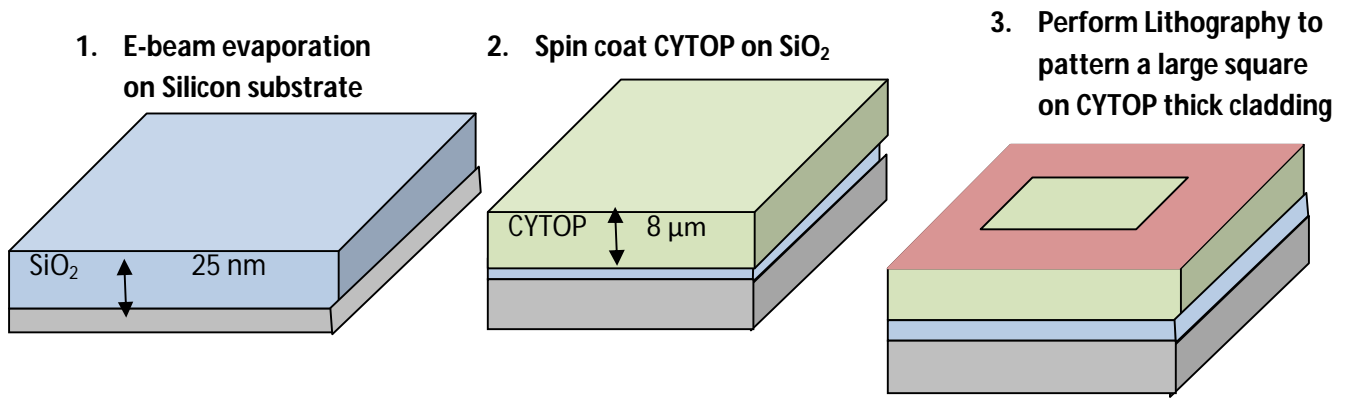
**Figure21: Fully cladded LRSP supporting waveguide structures with no apparent damage to the metal waveguides or solvent trapping in upper cladding layers of CYTOP.**

### 3.5.2 SiO<sub>2</sub> as an etch-stop layer:

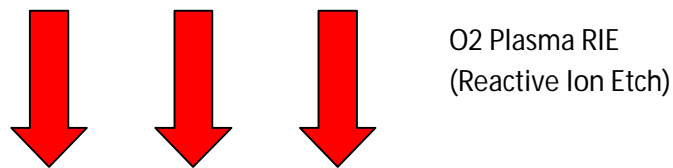
Another important reason for introducing the SiO<sub>2</sub> layer between the upper cladding and lower cladding CYTOP layers, is its use as an etch-stop layer to properly etch the micro-fluidic channels formed in the CYTOP upper cladding through the O<sub>2</sub> plasma RIE etching method previously developed in [51]. It was learned in [51] that the O<sub>2</sub> plasma over-etched the CYTOP repeatedly in different experiments. It is desirable to stop the etching process at the instant the metal waveguides are exposed. This was very difficult to perform because the metal is only 30 nm thick, while the etch rate was measured to be around 920 nm/min [51]. This means that the precision of the timed etch would have to be down to seconds. Though this is not impossible to do, there are two other factors affecting the precision of the etch process, which are cladding thickness and etch uniformity. It was discovered experimentally that the spin-coating of CYTOP to obtain a target thickness is accurate to within 0.05 μm. In addition, the etch uniformity was discovered to vary by 0.5 μm. Considering the two errors, it is difficult to stop the etch process right after the waveguides have been exposed. Therefore, the SiO<sub>2</sub> layer could possibly act as an etch-stop layer. Experiments were conducted to find out if SiO<sub>2</sub> was a feasible solution to act as an etch-stop layer.

A thin layer of SiO<sub>2</sub> (~ 25 nm), very close to the thickness used in the fabrication process was deposited on a bare silicon substrate using e-beam evaporation. After the oxide deposition, the wafer was coated with a thick CYTOP cladding (~ 8 μm), which is very close to the thickness of upper CYTOP cladding. Large square patterns were imprinted and developed on the CYTOP layer using the same process as the micro-fluidic channel lithography explained in *section 6.2, Table 11*. These samples were exposed to RIE (Reactive Ion Etching) O<sub>2</sub> plasma to etch the

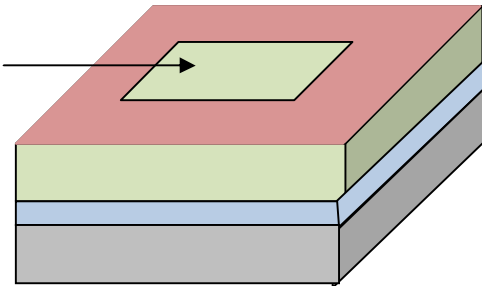
square patterns and, in turn, find the etch rate of CYTOP and SiO<sub>2</sub>. The flowchart in *Figure 22* shows the process used in the experimentation to characterize the etch profile of CYTOP on a thin SiO<sub>2</sub> layer. The experiments were conducted using 2 different plasma powers of 200 W and 100 W. The lower power of 100 W slows down the etch process considerably, but takes a very long time to complete. The wafer was RIE etched for several different time intervals and at different plasma powers, and consequently the square area, which was exposed to RIE etching, was measured for thickness and etch depths.



4. RIE etch the exposed region of CYTOP till the SiO<sub>2</sub> layer is reached



Patterned square to be etched through with O<sub>2</sub> plasma, surrounded by thick photoresist



5. Measure the thickness of SiO<sub>2</sub> layer using Ellipsometer.

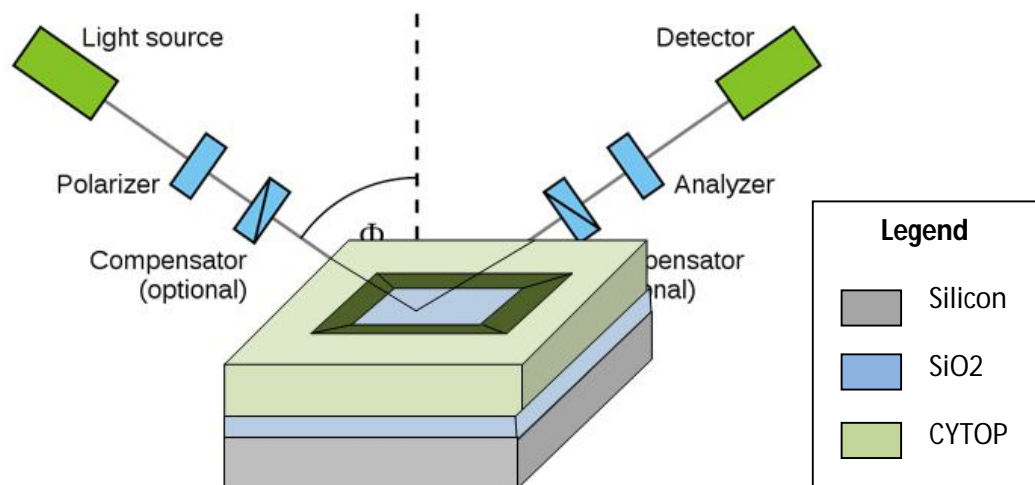
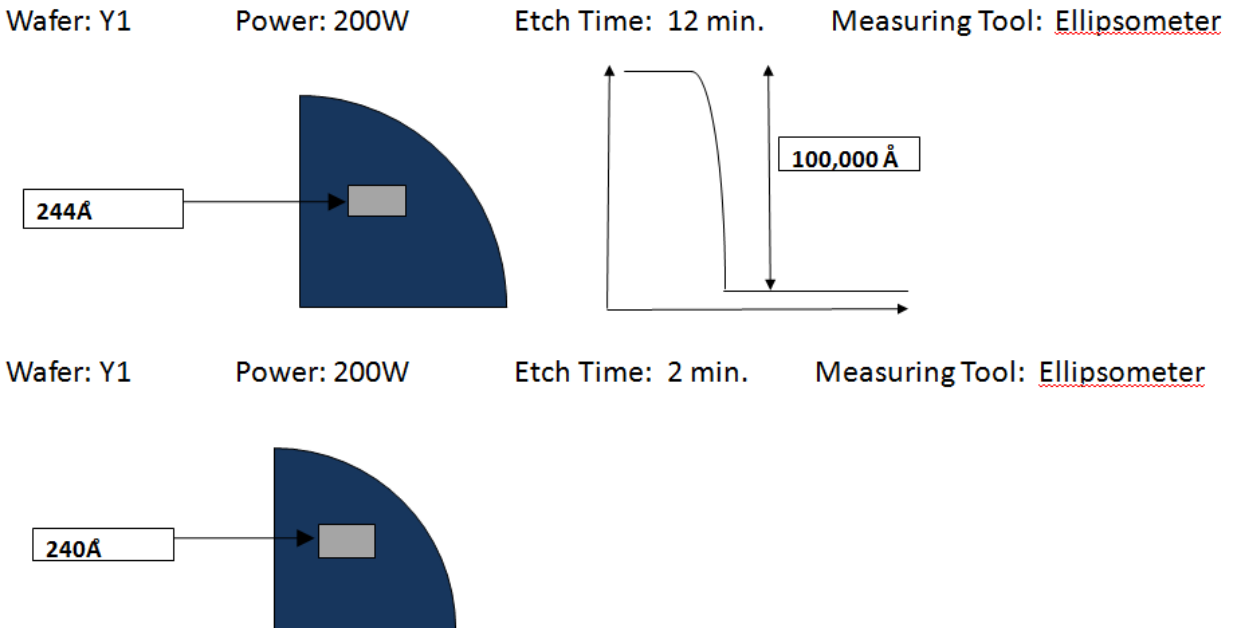


Figure 22: Method of performing etch-test on SiO<sub>2</sub> layer

The results attained from the above experiments are summarized in *Figure 23* below:



**Figure 23: etch profile results of CYTOP/SiO<sub>2</sub>/Silicon under 200 W of O<sub>2</sub> plasma RIE.**

The above results show that the wafer named Y1 was etched for 12 minutes under 200 Watts of O<sub>2</sub> plasma RIE etching. The consequent depth of the etch was 100, 000 Å (10 µm), which was measured using a profilometer. The thickness of the exposed SiO<sub>2</sub> layer was measured and found to be 24.4 nm, which is very close to the originally deposited layer of SiO<sub>2</sub> (~25 nm). The sample was introduced to RIE etching for another 2 minutes. The thickness of SiO<sub>2</sub> layer was measured again using ellipsometry and was found to be 24nm. In the experiment conducted at 100 W of O<sub>2</sub> plasma RIE, it was determined that the etch rate was very slow (~ 0.4 µm / minute). Although this is a very precise and controlled process, it is unfortunately quite time constraining. The etch results shown for 200 W O<sub>2</sub> plasma RIE gave very desirable results for 30 nm thick SiO<sub>2</sub> layer, so it was adopted for the etch process of micro-fluidic channels on embedded LRSP waveguides. Although, one disadvantage that the more powerful, and

aggressive, plasma etch did present was that it was particularly reactive to the relatively thinner SiO<sub>2</sub> layers (~20 nm). Hence, the extended exposure to the plasma caused some damage to the SiO<sub>2</sub> layer.

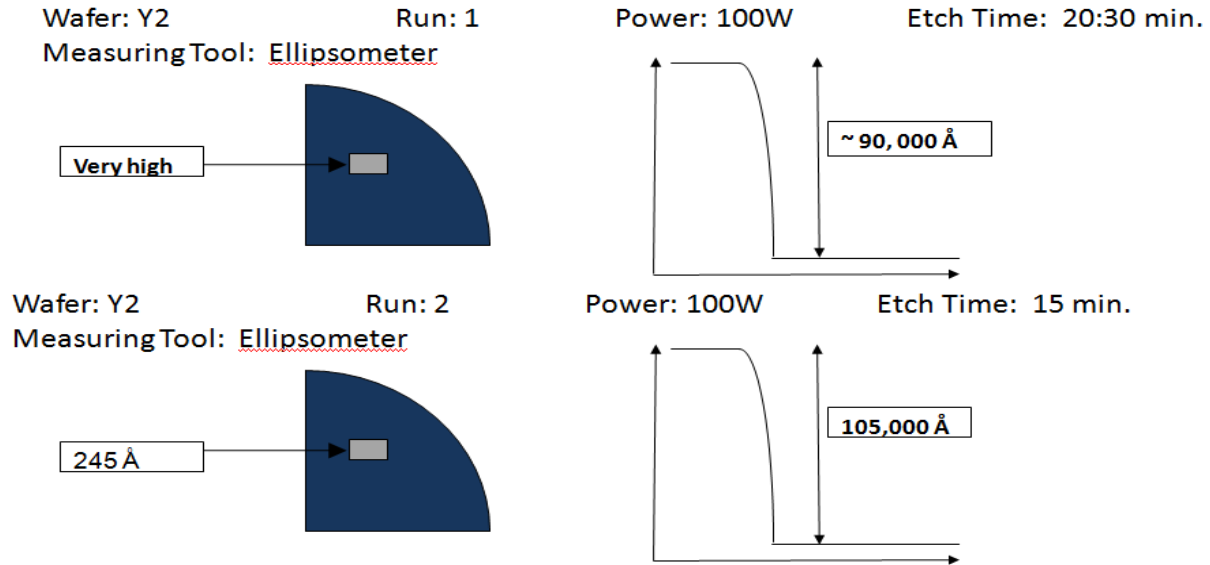
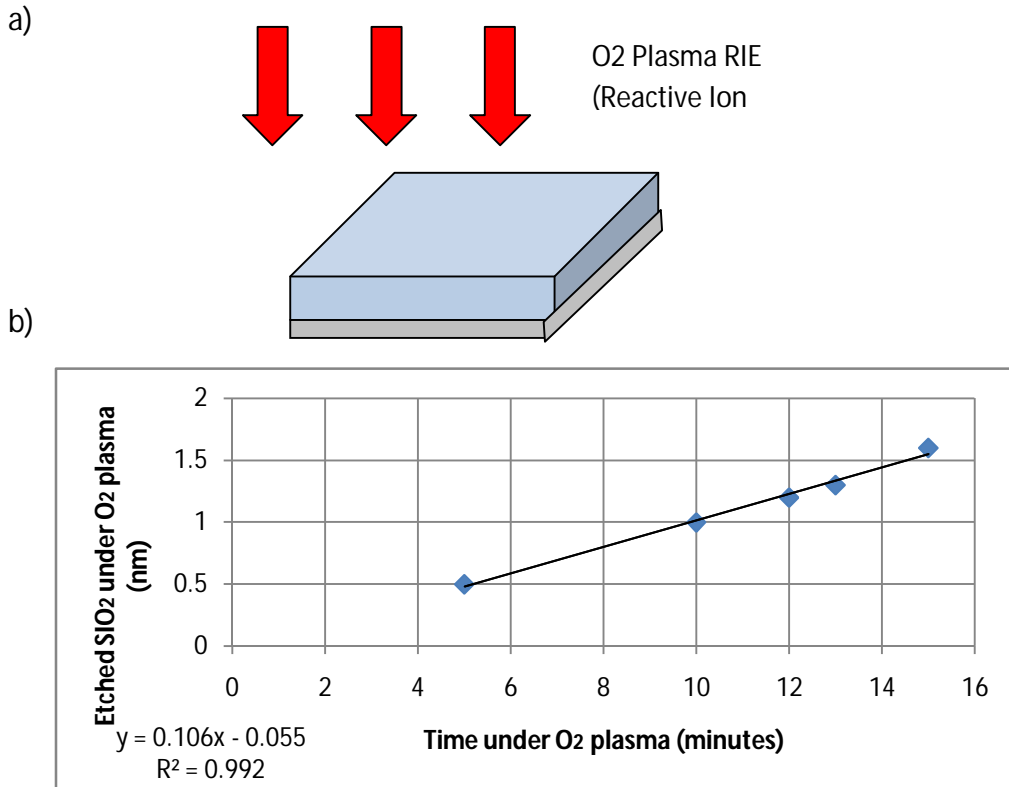


Figure 24: etch profile results of CYTOP/SiO<sub>2</sub>/Silicon under 100 W of O<sub>2</sub> plasma RIE.

Separately, another experiment was conducted to find the etch rate of exclusively the SiO<sub>2</sub> layer under O<sub>2</sub> plasma RIE etching. In this process, only a thin SiO<sub>2</sub> layer was deposited on silicon, and placed in RIE etching tool. *Figure 25* gives an explanation of the experiment conducted to characterize the etch profile of SiO<sub>2</sub> only.



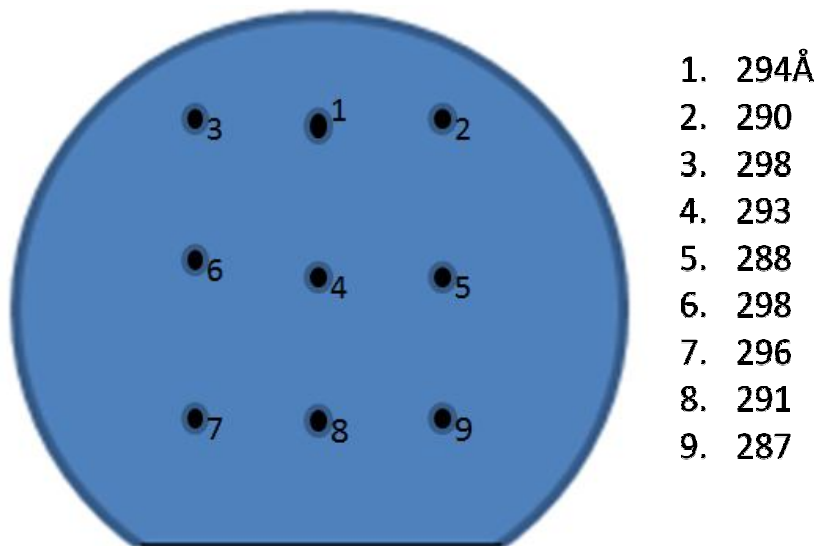
**Figure 25: 25 nm thick SiO<sub>2</sub> layer exposed to O<sub>2</sub> plasma RIE. Consequent graph to calculate etch rate of SiO<sub>2</sub> under O<sub>2</sub> plasma.**

The SiO<sub>2</sub> layer (~25 nm) was exposed to 200W O<sub>2</sub> plasma RIE for 5 minutes. Afterwards the thickness of the SiO<sub>2</sub> layer was measured using ellipsometer, which came out to be 24.5 nm. This proved that the SiO<sub>2</sub> was relatively immune to the aggressive plasma etching, and the etch rate of SiO<sub>2</sub> was very slow (0.1 nm /s). The etch rate of the SiO<sub>2</sub> layer under 100 W of O<sub>2</sub> plasma RIE is even slower. This means that the SiO<sub>2</sub> layer can effectively be characterized as an etch-stop layer.

### 3.6 Thickness, refractive index, and surface uniformity check:

#### 3.6.1 Thickness Check

The surface roughness and uniformity check was an important criterion in order to proceed with the e-beam evaporation method to deposit the SiO<sub>2</sub> layer. First the thickness of the layer deposited on silicon substrate was determined using the ellipsometry technique by measuring SiO<sub>2</sub> thickness in different parts of the wafer to assure thickness uniformity throughout the SiO<sub>2</sub> layer. The target thickness of the deposited SiO<sub>2</sub> layer during e-beam evaporation was 29 nm. *Figure 26* shows the thickness measurements of a SiO<sub>2</sub> layer at different parts of a 2" silicon wafer.

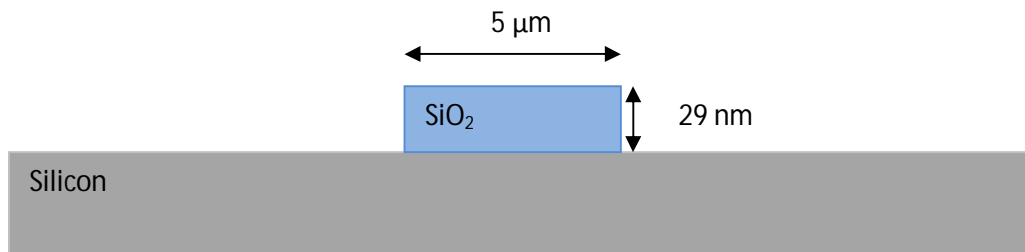


**Figure26: Measured thickness of SiO<sub>2</sub> deposited (1 nm = 10Å) on silicon using e-beam evaporation.**

The above thickness measurements assured that the average thickness was ~ 29 nm. This proves that precise target thickness of the oxide layer could be acquired using the e-beam evaporation method. The variation between the measured thicknesses and the target thickness was at most  $\pm 0.5\text{nm}$ . These results were acceptable, and thickness uniformity was sufficient enough to implement metal waveguides.

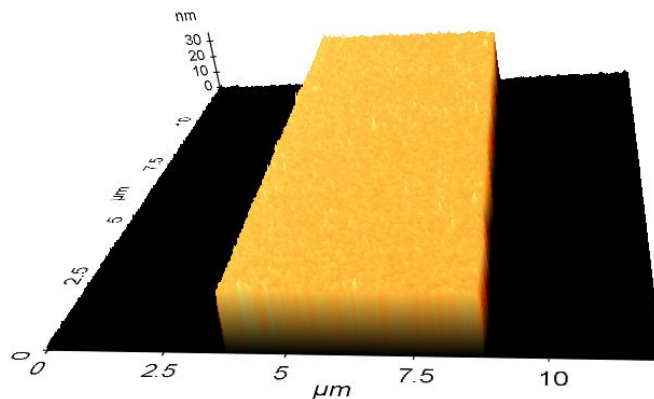
### 3.6.2 Surface roughness check using AFM:

In order to corroborate the thickness measurements, and determine the surface roughness of an evaporated SiO<sub>2</sub> layer on a silicon substrate, the wafer was first patterned using the same mask as the one used for lithography for the actual waveguides, which is described in chapter 4 of this thesis. Steps are described in *Table 7, steps 2-9*. After developing the pattern, SiO<sub>2</sub> was deposited using e-beam evaporation, and then lifted-off from non-patterned parts of the silicon substrate. The target thickness was 29 nm, and the width of the patterned SiO<sub>2</sub> stripe was expected to be 5 μm. *Figure 27* gives an illustration of SiO<sub>2</sub> patterned on silicon, used for this experiment <sup>3</sup>.



**Figure 27: Schematic of patterned SiO<sub>2</sub> on Silicon substrate.**

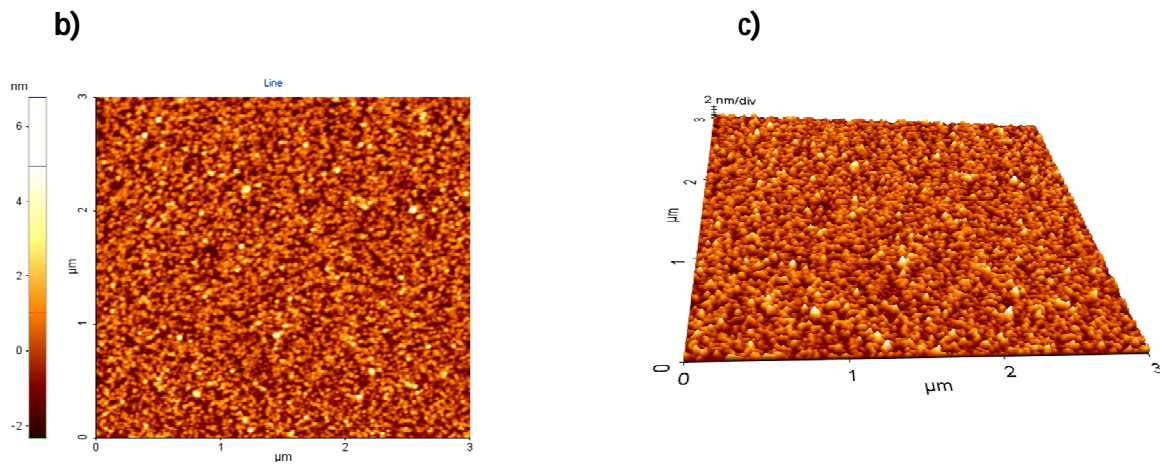
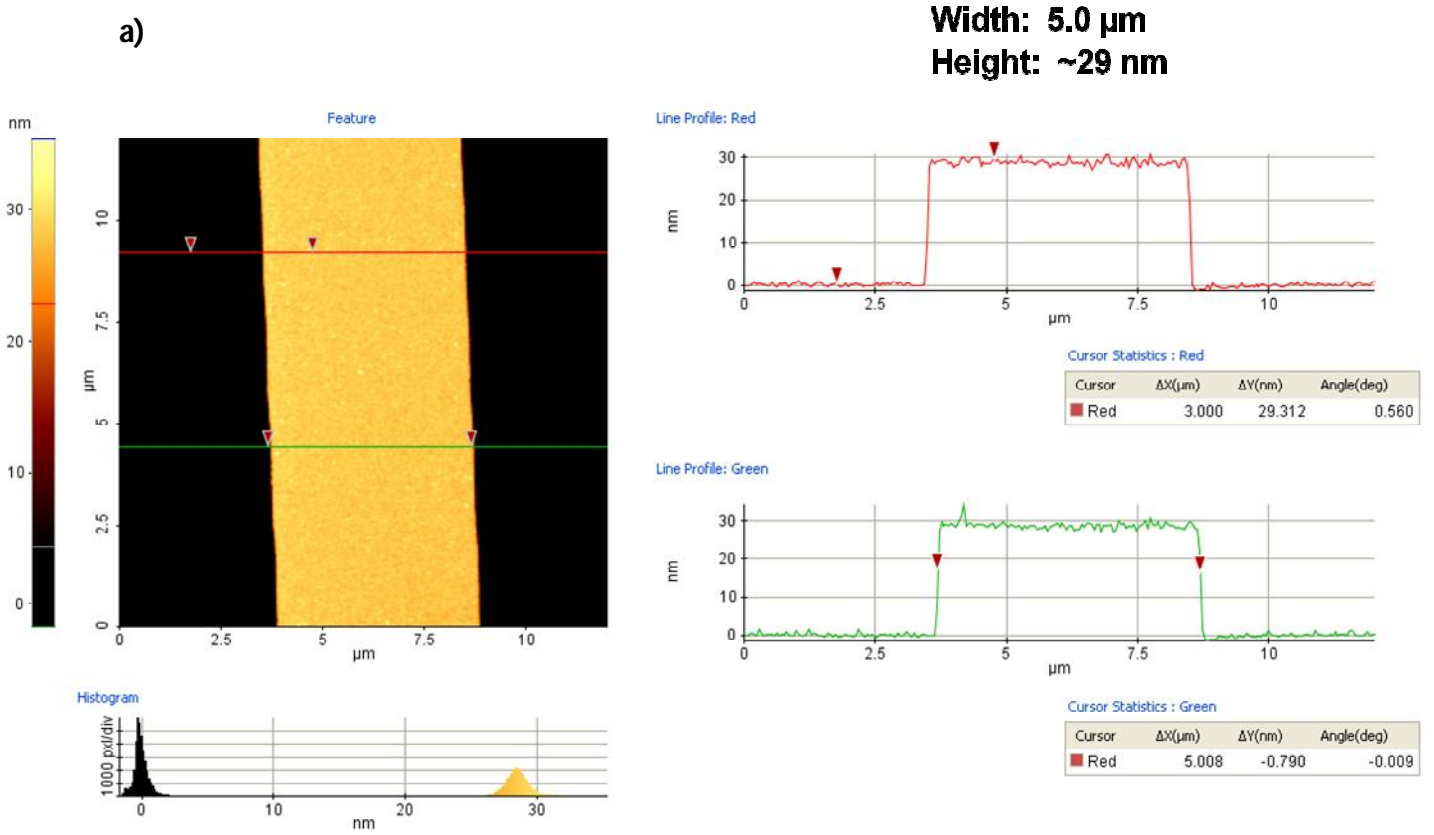
The AFM results<sup>4</sup> are shown in Figures 28 and 29:



**Figure 28: 3-D visualization of SiO<sub>2</sub> stripe on silicon.**

<sup>3</sup> The above experiment was designed and conducted by Hamoudi Asiri, M.A.Sc. student, University of Ottawa.

<sup>4</sup> The AFM microscopy of patterned SiO<sub>2</sub> was obtained by Surface Science Western, University of Western Ontario.



Area roughness

Statistics

Region	Min(nm)	Max(nm)	Mid(nm)	Mean(nm)	Rpv(nm)	Rq(nm)	Ra(nm)	Rz(nm)	Rsk	Rku
Red	-2.330	6.779	2.224	0.000	9.109	0.942	0.754	8.492	-0.541	3.767

Figure 29: a) AFM surface and dimension profiles of  $\text{SiO}_2$  stripe waveguides. b)  $\text{SiO}_2$  surface amplitude measurement.

Roughness = 0.942 nm RMS, 0.754 nm average. (e)  $\text{SiO}_2$  Surface phase shift profile

The AFM results<sup>3</sup> were used to verify the thickness and surface roughness of the e-beam deposited SiO<sub>2</sub> layer. The results shown above confirmed that the target thickness of 29 nm was precisely achieved. The surface roughness of the SiO<sub>2</sub> came out to be about 0.942 nm RMS, which meets the requirement of being less than 1 nm RMS. Another AFM measurement was done on another wafer to verify the surface smoothness of the oxide layer after the deposition of metal waveguides detailed in section 4.4. The AFM results<sup>3</sup> shown in Figure 30 represent the oxide between the metal layer and CYTOP bottom cladding.

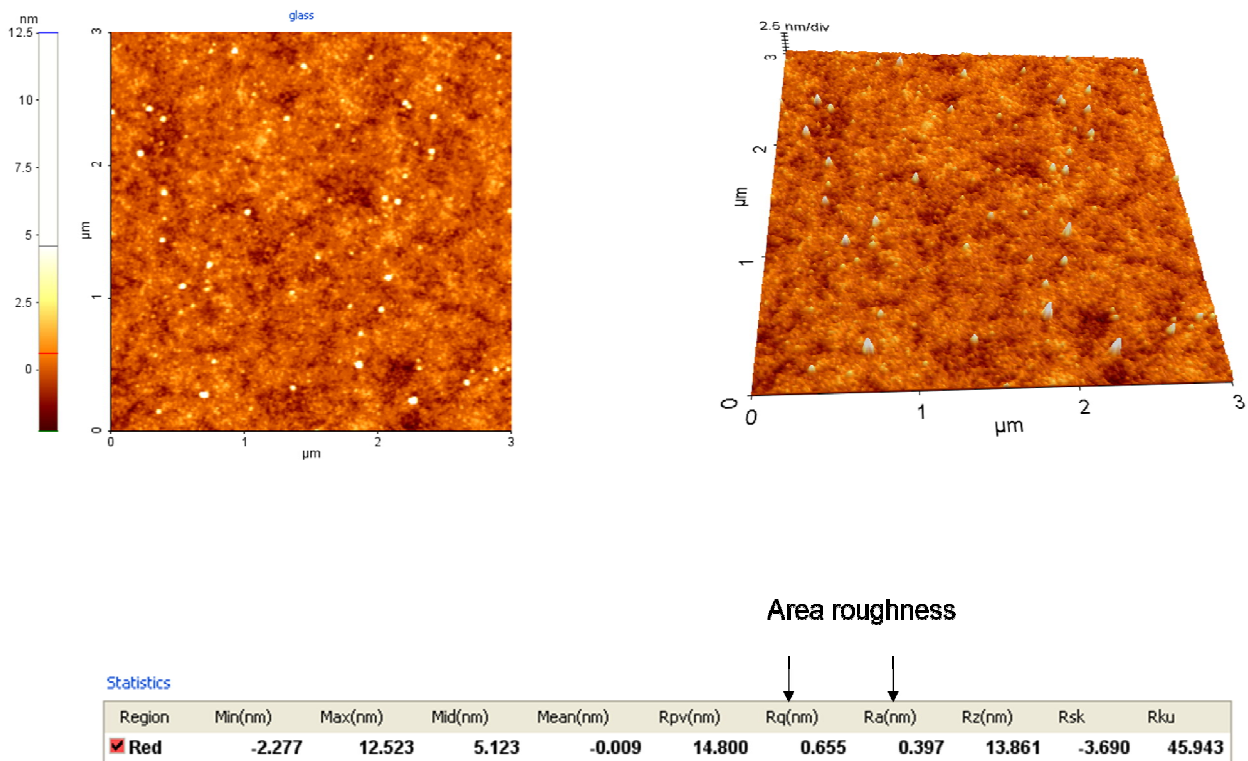


Figure 30: a) SiO<sub>2</sub> surface amplitude measurement after metal deposition step. Roughness = 0.655 nm RMS, 0397 nm average. (e) SiO<sub>2</sub> Surface phase shift profile.

The above results further verify that the oxide layer deposited through e-beam evaporation is a viable option to implement in the fabrication of LRSP waveguides, because

very precise and accurate results in terms of layer thickness and surface roughness can be obtained through this process.

### 3.6.3 Optical Index measurements

The optical index used as a parameter to model the effects of SiO<sub>2</sub> in LRSPP guiding in the waveguides was  $n_{\text{SiO}_2} = 1.4468$ . Therefore, it was critical that the index of the evaporated oxide be very close to the theoretical optical index in order to achieve the expected performance, and minimize the optical attenuation. First, the optical index of a very thick *thermal oxide*<sup>5</sup> was measured using the Metricon at  $\lambda = 1310$  nm for reference, which is shown in *Table 5*.

<b>n</b>	<b>Standard deviation</b>	<b>% Standard Deviation</b>	<b>Thickness (μm)</b>	<b>% Standard Deviation</b>
1.44762	0.0005	0.00	15.2291	0.98

**Table 5:** refractive index measurements of thermal SiO<sub>2</sub>.

The measured optical index of the thermal oxide at  $\lambda = 1310$  nm is very close to the expected value for this type of oxide. Afterwards, a thick layer of *evaporated SiO<sub>2</sub>* was measured using Metricon at  $\lambda = 1310$  nm. The results listed in *Table 6* were achieved:

<b>n</b>	<b>Standard deviation</b>	<b>% Standard Deviation</b>	<b>Thickness (μm)</b>	<b>% Standard Deviation</b>
1.44638	0.00043	0.03	2.7105	0.75

**Table 6:** refractive index measurements of evaporated SiO<sub>2</sub>.

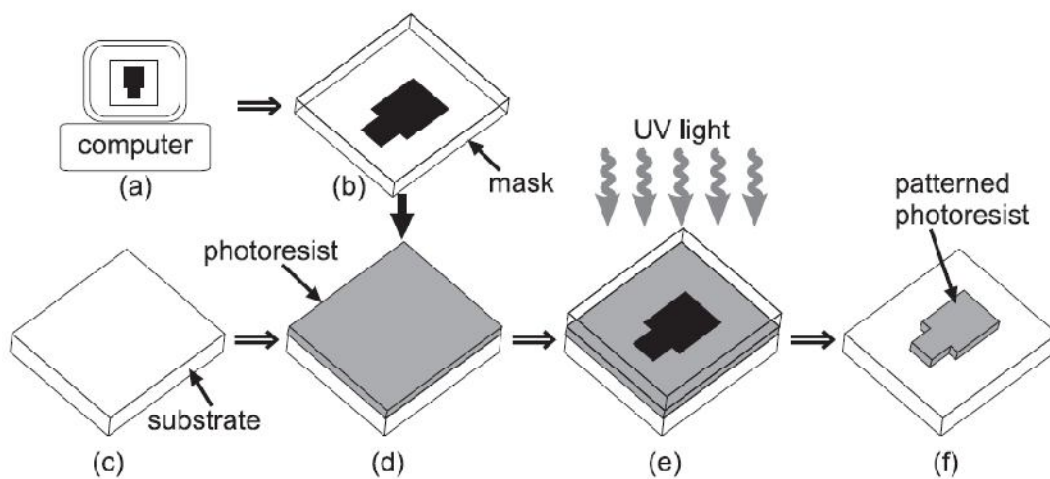
The above measured optical index is very close to the theoretical optical index of 1.4468. Therefore, these measurements further supported the application of evaporated SiO<sub>2</sub> in the fabrication of symmetric LRSPP waveguides.

<sup>5</sup> The deposited thermal oxide was obtained by a supplier (Silicon Quest International).

## 4 Lithography

### 4.1 Device Features Layout

Photolithography is used to transfer the desired patterns into a substrate. The process is represented in *Figure 31*. The specific pattern is designed using a commercial computer aided design (CAD) software (*dw-2000 layout editor*), and transferred onto a mask. The mask is a glass plate that has a defined thick material, usually chrome, covering the un-patterned surface. The substrate is spin coated with photoresist and loaded in an aligning tool that holds the patterned mask. The UV-exposure source is integrated in the same aligner tool. The substrate and mask are brought in near vicinity, and UV light is exposed through the mask on to the photoresist. The photoresist under the transparent portions of the mask is exposed to UV radiation. The wafer is immersed in a developing solution, which etches the UV-exposed patterns on the photoresist. This type of resist is referred as a positive photoresist; whereas, the negative photoresist etches from where it was not exposed to UV light. The remaining photoresist acts as a protective mask to transfer the material in the developed patterns [59].



**Figure 31: Pattern transfer with photo-lithography. Adapted from [59].**

The device-level lithography in our fabrication process consists of imprinting the actual waveguide devices onto the SiO<sub>2</sub> layer sitting on top of the *CYTOP* bottom cladding. The lithography patterns put down in this layer were designed in [34, 35]. Some example devices are shown in *Figures 32- 34*. Most devices in the layout are Mach-Zehnder interferometers and waveguide couplers of varying lengths since the main application of these devices is biosensing. The layout also contains many straight waveguides for use as reference and for optical characterization and cut-back measurements. *Figures 32a and 33b* are simple MZI structures with a single input and output. The function of these devices was explained in *section 1.1*. *Figure 33a* shows a MZI where the sensing arm is curved. The curve creates a different path length with respect to the reference arm. This path difference introduces a constant 90° phase offset, which is the most sensitive region of a MZI sensor. This makes the device more sensitive to temperature and environmental changes because the slightest fluctuation will trigger a detectable power output. *Figure 32b and 34a* show a MZI with dual/triple output. The sensing and reference arms are directed to a four/five port coupler, which allows for differential sensing by observing and comparing the fraction of power transferred from one output to the other. The couplers in *Figure 34a* are the smallest feature size in the layout of the photo-mask. The couplers are shown as three parallel stripe waveguides, which are 5 μm in width and 2 μm apart. In most of the thesis, this area serves as a reference for dimension accuracy, since they require the most precision in different steps of the fabrication to have accurate device features.

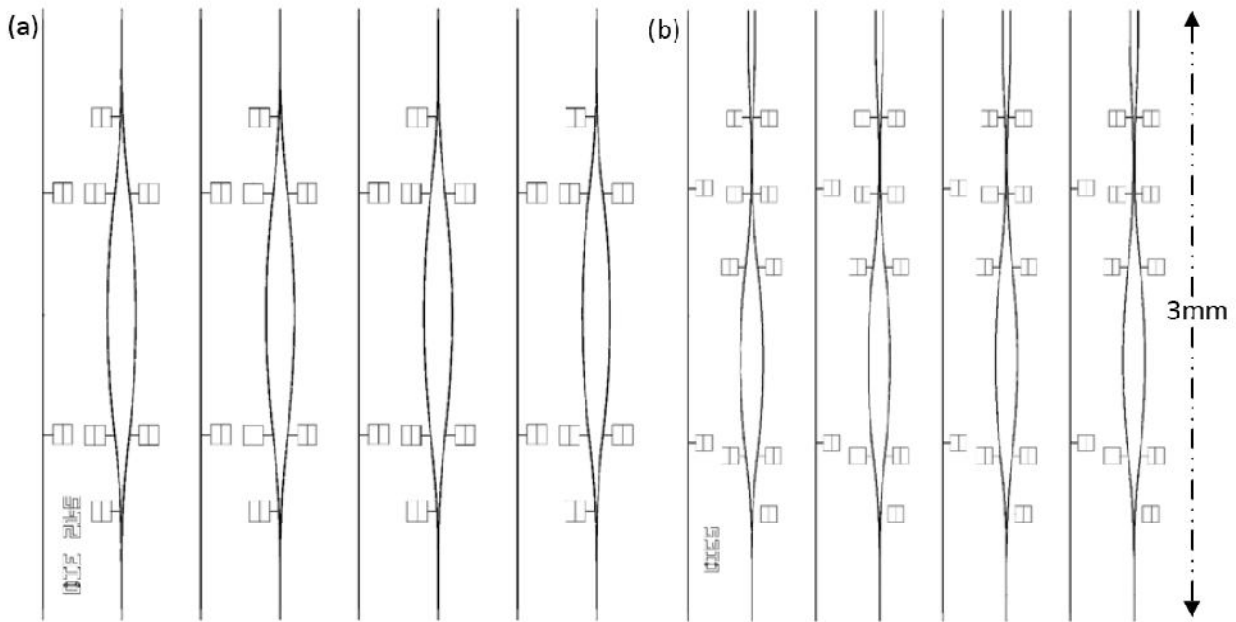


Figure 32: 3 mm long waveguide devices (a) straight waveguides and single-output MZIs (b) Straight waveguides and MZIs with dual outputs [51].

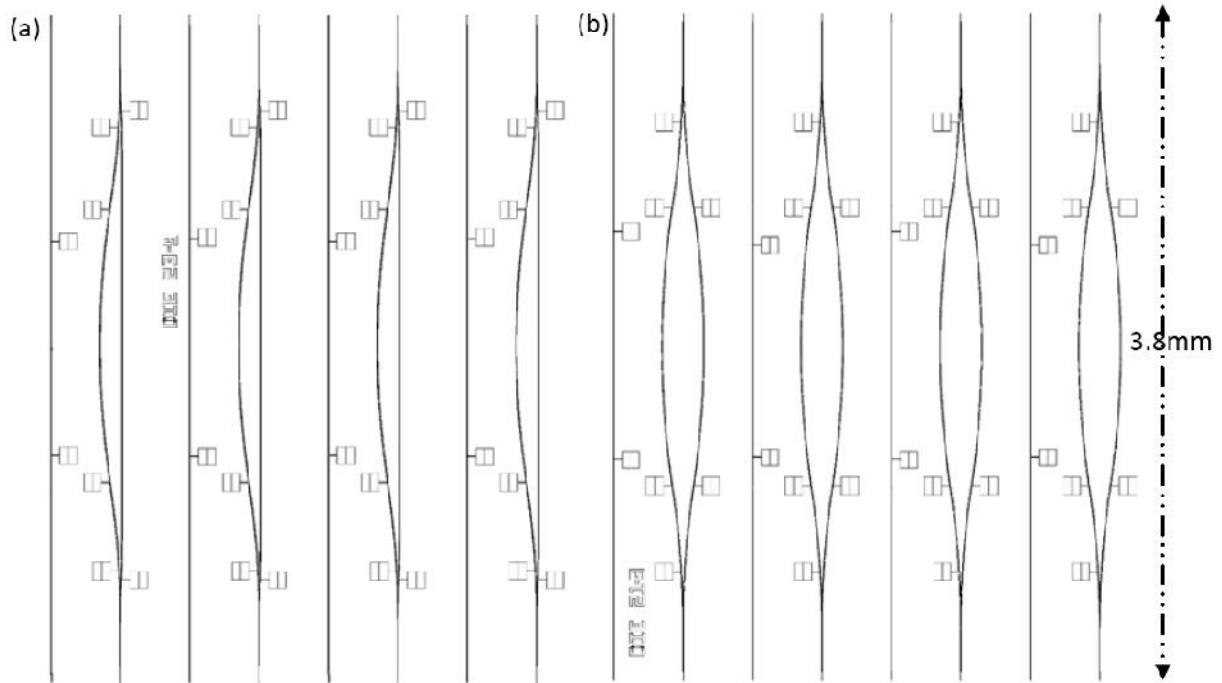


Figure 33: 3.8 mm long waveguide devices (a) straight waveguides and path adjusted MZIs (b) Straight waveguide and MZIs [51].

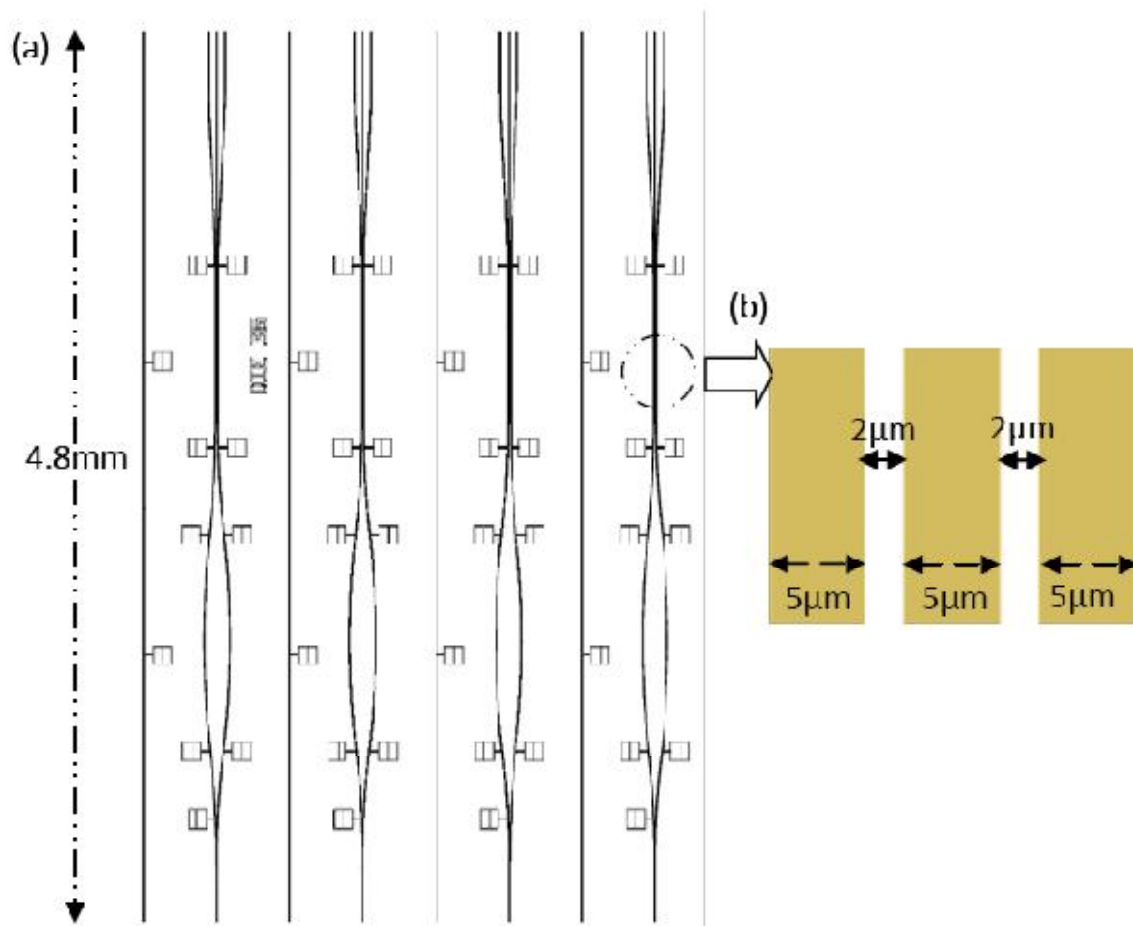


Figure 34: 4.8 mm long waveguide devices (a) straight waveguides and MZIs with triple coupling output (b) feature size of triple waveguides [51].

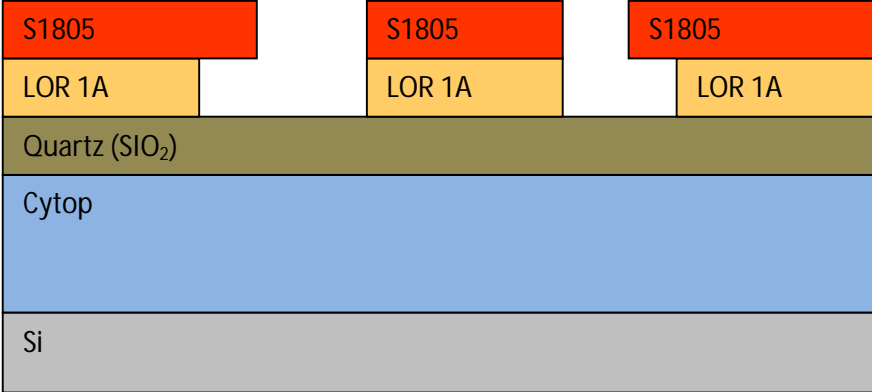
## 4.2 Bi-layer Lithography Process for Metal Waveguide Devices:

A bi-layer lithography process is a common method of patterning metal devices on substrates, which involves spinning two different resists on the wafer. First, the lift-off resist (LOR-1A) is coated on the SiO<sub>2</sub> layer followed by a photoresist (S1805) layer. Both layers have a bake time after the spin-coating process, which is summarized in *Table 7*. After the spin coating of lift-off and photo-resist, the wafer is subjected to UV-exposure to imprint the photo-mask features into the resist.

*CYTOP* is transparent in the ultraviolet (UV) spectrum. This causes any UV radiation incident on the thick *CYTOP* cladding to be transmitted and reflected without significant decay in intensity. Therefore, the resist is exposed twice to the UV radiation, thereby resulting in rough edges due to the over-exposure of the resist to UV light. To solve this issue, the exposure time was very small, and carefully tuned for the specific lamp intensities. The photoresist was exposed for 7 seconds under UV intensities of 6.6m W/cm<sup>2</sup> at 365 nm and 12 mW/cm<sup>2</sup> at 400 nm [51].

Only the photoresist is sensitive to UV radiation exposure not the underlying lift-off resist. But both the lift-off resist and photoresist materials are susceptible to developer etching. The developer solution etches UV-exposed resist first, and then the lift-off resist also starts to etch. Depending on the lift-off resist etch time, an under-etch will occur beneath the patterned edges. The resulting side-wall profile prevents the deposited metal devices from being in contact with the adjacent bi-layer structures. This undercut helps to eliminate metal edge roughness, which occurs due to accumulation of metal at the corners and sidewalls. The bi-layer lithography procedure for fabricating metal-guided LRSP devices is described in *Table 7*

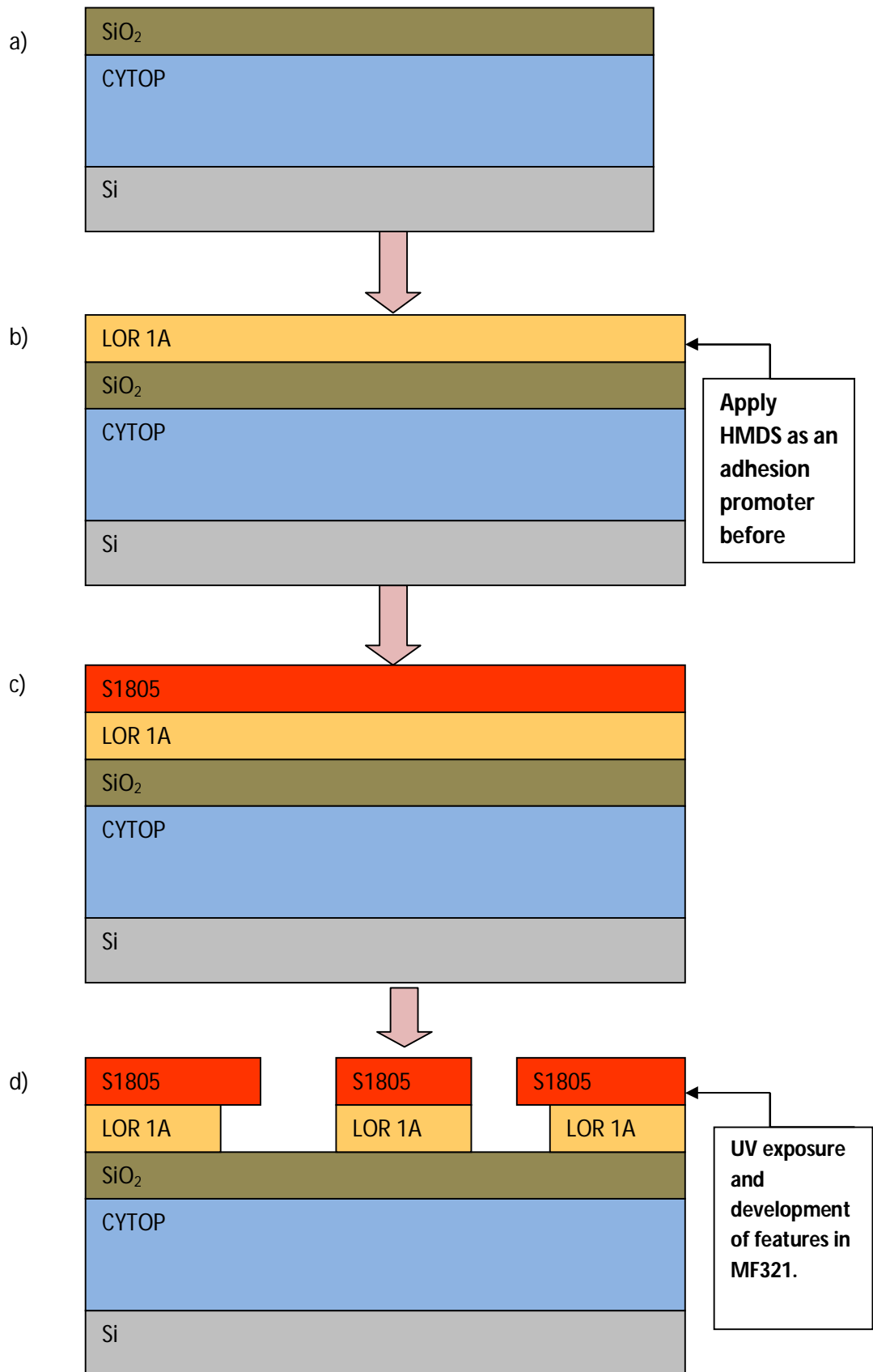
and shown in *Figure 36*. *Figure 35* shows a schematic of the layout pattern imprinted on top of SiO<sub>2</sub> using lift-off and photo resist.



**Figure 35:** Schematic of a wafer with developed features on lift-off and photo resist ready for metal deposition.

Step #	Process Description	Details
1	Clean the SiO <sub>2</sub> surface with Acetone and IPA rinsing, followed by DI water bath for 10 seconds, and Nitrogen air dry.	To have clean and smooth surface for better adhesion and smooth lithography patterns.
2	Spin coat hexamethyl disiloxane (HMDS) for lift-off resist adhesion.	1000 rpm for 10 sec.
3	Soft-bake on hot plate.	@ 105°C for 1 minute.
4	Spin coat lift –off resist (LOR-1A) layer.	Spin Speed: 1000 RPM for 10 seconds, followed by 4000 RPM for 30 seconds.
5	Soft-bake on hotplate	@105°C for 9 minutes.
6	Spin coat photoresist (S1805) layer	Spin Speed: 1000 RPM for 10 seconds, followed by 4000 RPM for 30 seconds.
7	Load biosensor mask in Mask Aligner	Align markers to flat of wafer.
8	UV exposure	7 seconds of UV exposure.
9	Develop the patterns in MF-321	Development time: 40 seconds with very light agitation.
10	Pattern uniformity and sharpness inspection	Check for edge smoothness and deformities. If patterns are rough follow next instructions.
11	Strip Lift-off and photoresist by immersing the wafer in Microstrip 1165 for 20 seconds.	Preheat the Microstrip 1165 to 70°C.
12	Repeat steps 1-10	

**Table 7: Bilayer Lithography process for LRSPP waveguides**

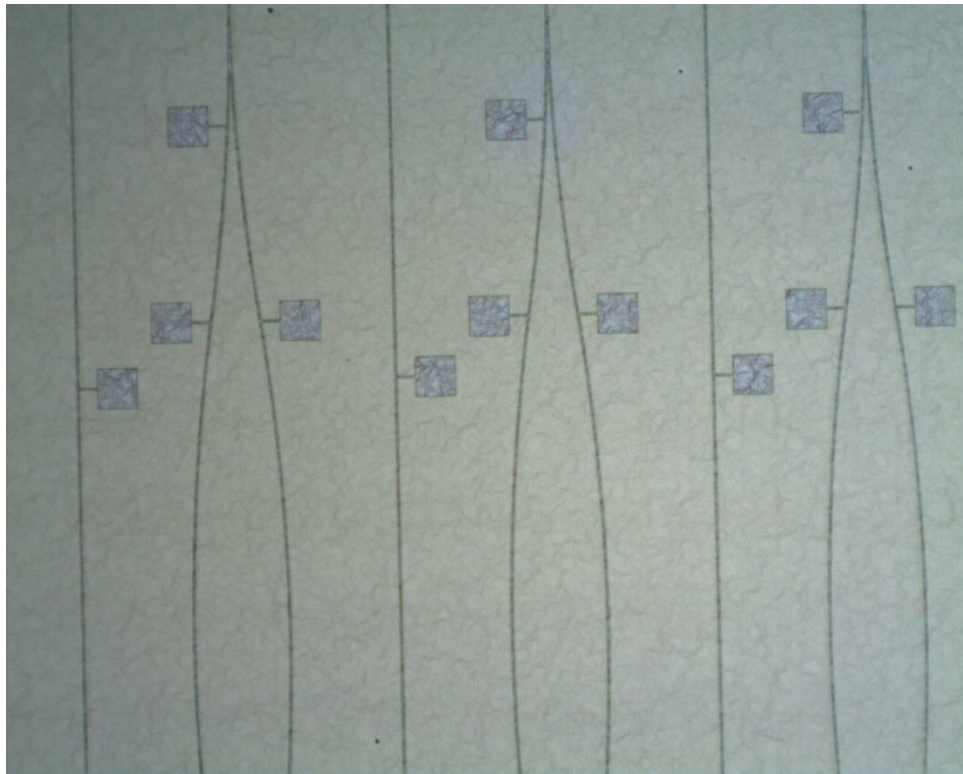


**Figure 36: Schematics of Bilayer Lithography process for LRSP**

### 4.3 Past and current Issues:

#### 4.3.1 Thermal restrictions

One of the main criteria for successful lithography on the thin SiO<sub>2</sub> layer is to be careful about the thermal budget for the baking process of the Lift-off Resist (LOR) and the Photo-resist (PR). The previous lithography process required high temperature LOR bakes for the bi-layer lithography at about 180 °C. The glass transition temperature for CYTOP is T<sub>g</sub> = 107°C. This resulted in CYTOP 'rippling' in the bottom cladding, which in turn destroyed the SiO<sub>2</sub> layer as illustrated in *Figure 37*:



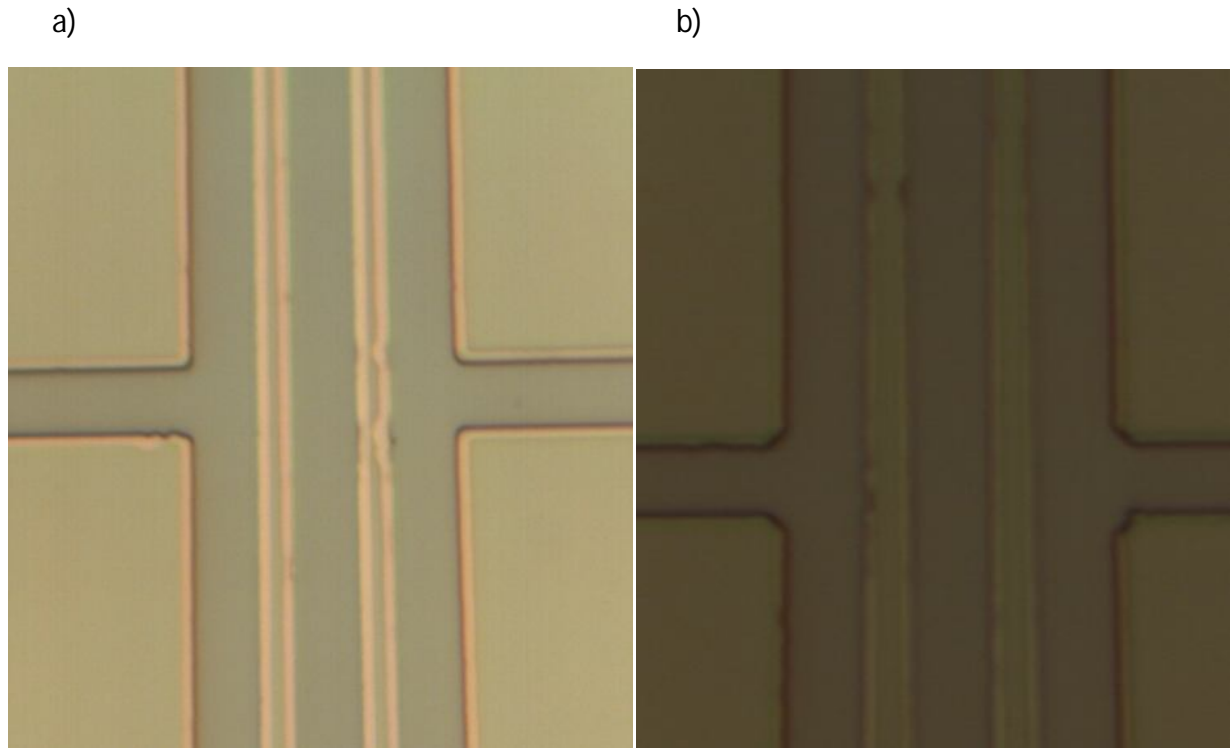
**Figure 37: Rippling effect of CYTOP due to bake temperatures for LOR exceeding the T<sub>g</sub> of CYTOP.**

Therefore, it was very crucial to keep the LOR baking temperatures lower than T<sub>g</sub> = 107° C to acquire desirable lithography results. As a result, the baking temperature for both S1805 photo-resist and the LOR-1A lift-off resist was constrained to 105 °C, to avoid any rippling of

CYTOP in the bottom cladding. In turn, the bake time was increased to achieve proper device features during development. This was done in accordance with manufacturer's specifications in [47].

#### **4.3.2 Lithography**

Another advantage that the evaporated SiO<sub>2</sub> layer provided was better features in the lithography process. In the previous process described in [51] the lithography was done directly on top of the CYTOP cladding. In that procedure, it was critical that the lift-off resist had excellent adhesion to the CYTOP lower cladding, which required plasma 'ashing' to clean the surface of the CYTOP cladding so that the resist could better adhere to the wafer. Although, the process improved the lithography results significantly in terms of dimensions and smoothness compared to procedures before described in [34], the lithography results were not always very consistent, and sometimes provided rough feature profiles as shown in *Figure 38*. After a standard lithography procedure was prescribed, the device features were always very smooth and sharp, with an accurate width of 5µm of waveguide.

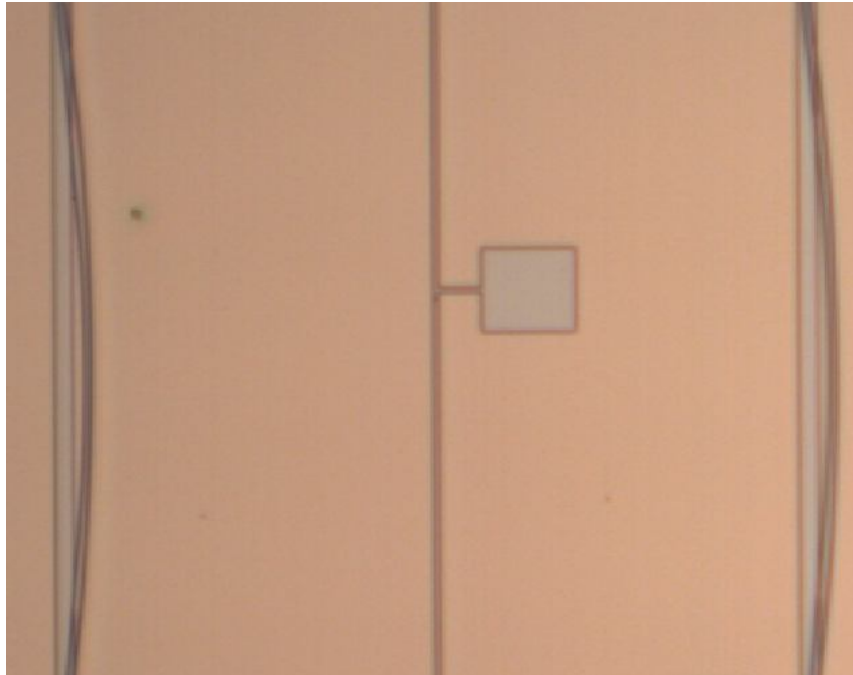


**Figure 38: Roughness in LOR edges indicating poor lithography results.**

In developing a standard procedure for the lithography process on the SiO<sub>2</sub> layer, it was important that the wafer not be developed for too long. The reason for this is that the lift-off resist (LOR) between the triple waveguides will eventually be completely etched away, thus destroying the desired features. This is shown in *Figure 39* where it is obvious that the LOR has been either etched away or completely collapsed leaving behind a dangling strip of photoresist (PR). It was one of the recurring problems with the initial trials to come up with a bi-layer process due to a faster etch rate caused by a lower LOR/PR hard-bake temperature (105°C). *Figure 39* shows a microscope image of a wafer developed for 43 seconds instead of 40 seconds. One can easily observe that the triple waveguides are deformed due to the overexposure to MF321 developer. At lower temperature of 105°C, the etch rate of the lift-off

resist is significantly larger compared to high temperature bakes of 180°C of older procedure of fabricating devices directly on CYTOP bottom claddings.

a)

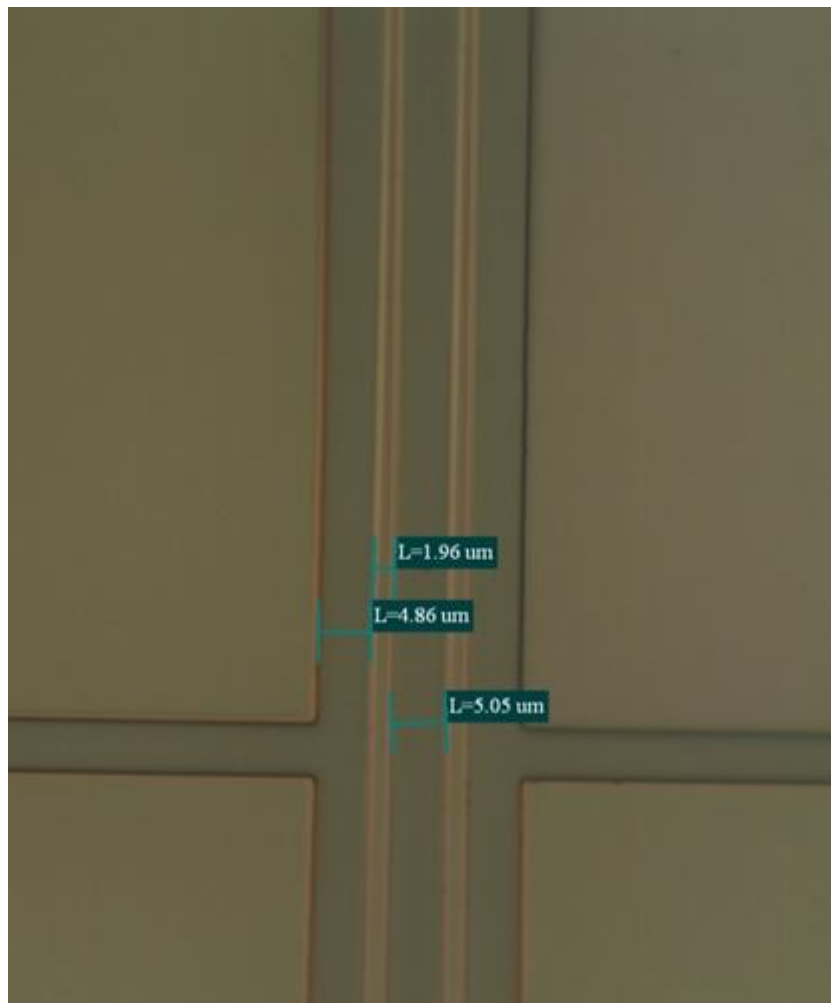


b)



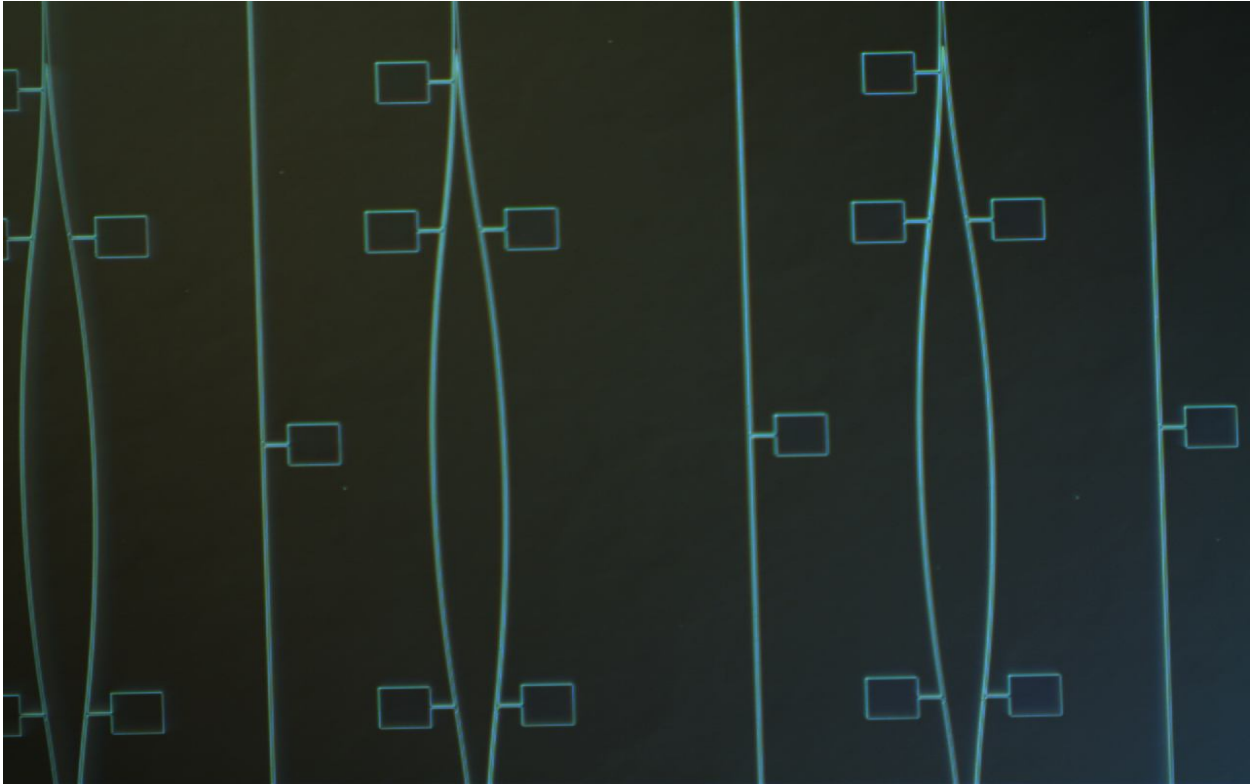
**Figure 39 : Triple waveguides deformed due to overexposure to MF321. A) 10x magnification b) 100x magnification**

The successful lithography procedure for device-level patterning is listed in *Table 7*. The lift-off resist and photoresist in this procedure were targeted to be 105 nm and 500 nm thick respectively. With a hard-bake temperature of 105°C, the lift-off resist etched at a rate of 14.075 nm/s when immersed in the developer solution. This resulted in 0.56  $\mu\text{m}$  of undercut LOR beneath the patterned resists. The undercut translated to 0.88  $\mu\text{m}$  of support width for the 2  $\mu\text{m}$  space between the triple waveguides. The patterned resist surrounded by LOR undercut is shown in *Figure 40*. *Figure 41* also illustrates the smooth waveguide patterns achieved through this lithography process.



**Figure 40: Desired Lithography results with accurate widths for the waveguide.**

a)



b)

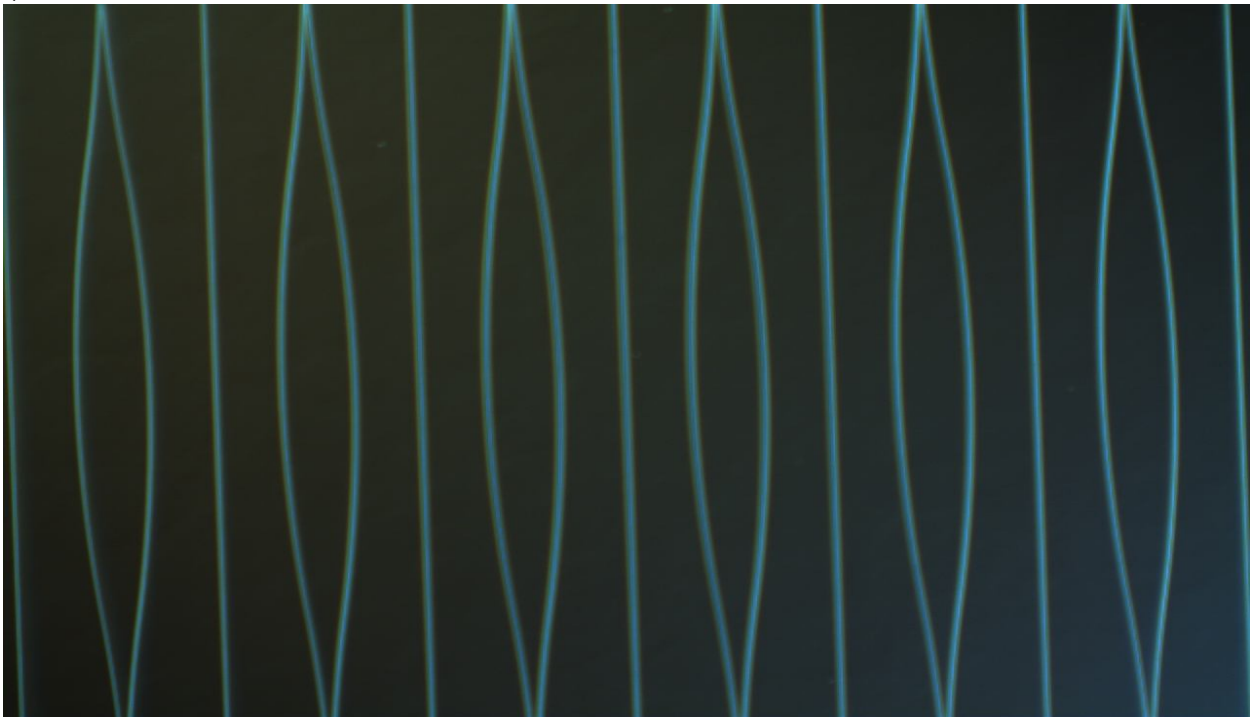


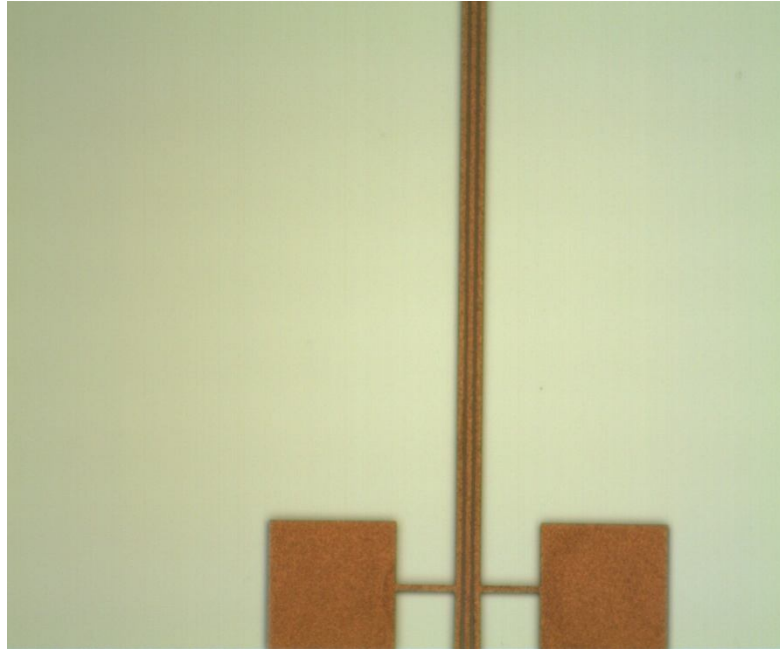
Figure 41: Smooth patterns achieved for MZI waveguides, seen through polarized light under microscope

#### 4.4 Metal Liftoff

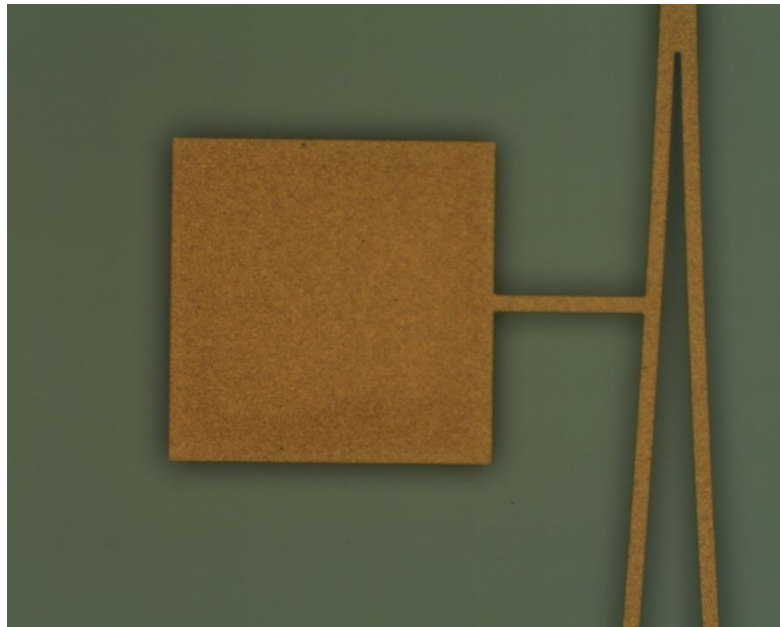
After achieving the desirable lithography results, in terms of edge smoothness of the device features, the wafers were immediately subjected to metal depositing in an e-beam BALZERS evaporator. It was desirable to perform this step as soon as possible in order to keep the wafer clean from any organic or inorganic contamination. The metal deposition was done in two steps. First, a very thin film of Chromium was deposited to promote adhesion of the Gold with the SiO<sub>2</sub>. It was learned from previous studies [38] that Gold does not adhere very well to oxide layers; hence, an adhesion promoting layer is needed for proper realization of gold features on SiO<sub>2</sub> layer. Then, without breaking the vacuum, the Gold layer was deposited. *Figure 42* shows microscope images for the direct depositing of Gold on SiO<sub>2</sub>. It can clearly be seen that although Gold is deposited throughout, some roughness and texture in bigger features such as the contact pad are clearly visible. It was also very crucial to select the right thickness of Chromium adhesion layer since too little (~1nm) would not allow adequate adhesion, and a significantly larger thickness would act as an optically invasive loss medium in plasmonic waveguides. Therefore, after different experimental trials of deposition and microscope inspections, it was determined that 2-3 nm of Chromium was adequate to use as an adhesion layer between the Gold and SiO<sub>2</sub> layers. It was very important to monitor the deposition of Chromium as the target thickness was very thin, and the lowest deposition rate available in the BALZERS evaporator is 0.1nm / s, which is difficult to achieve. Normally, the deposition rate was higher than this set rate, reaching 0.5-1 nm/s. After the required vacuum was achieved ( $1 \times 10^{-6}$  torr), it was essential to open the shutter window very slowly to avoid any spikes of power from the e-beam evaporator. This power spike would result in a

significantly higher thickness of Chromium than desired. Therefore, the deposition shutter was opened very slowly to allow smooth e-beam deposition, and as soon as the target thickness was achieved, the shutter window was closed rapidly to avoid going over the target thickness.

a)



b)



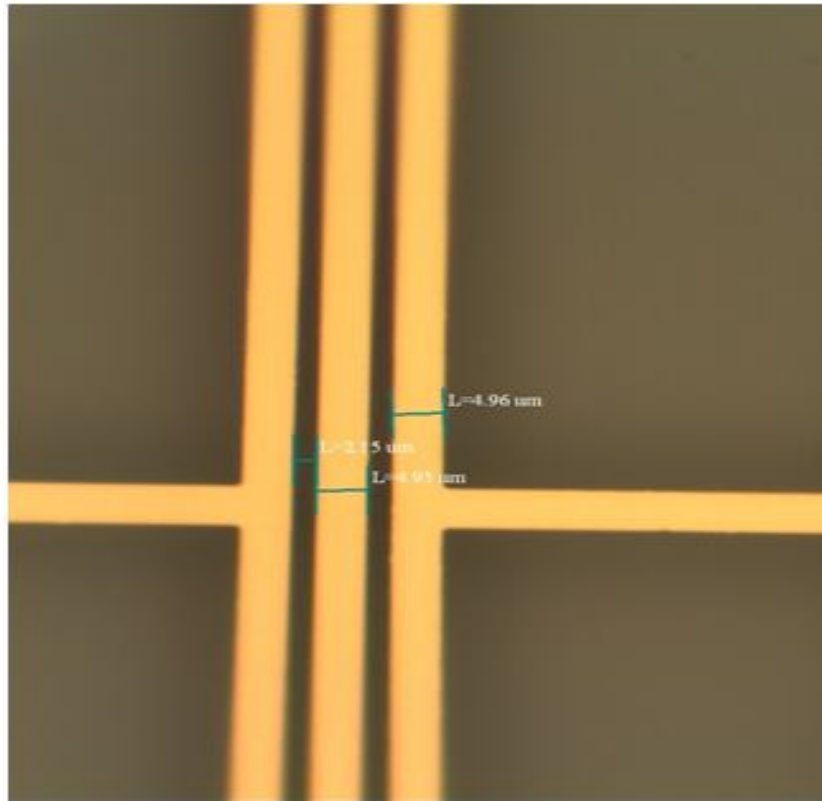
**Figure 42: a) and b) demonstrate the poor adhesion of Au on SiO<sub>2</sub> without the Cr adhesion.**

After the thin adhesion promoting Chromium layer was deposited, the e-beam system was allowed to cool-down for 10 minutes, without pumping out vacuum. After ten minutes, the target metal was moved to Gold by moving the crucible and Gold was deposited. Since the target thickness for Gold is also considerably very thin (28nm), the deposition was set low at a rate of 2 nm/s. The procedure was carefully monitored to make sure that the metal did not “spit” large spots of gold due to sudden changes in power.

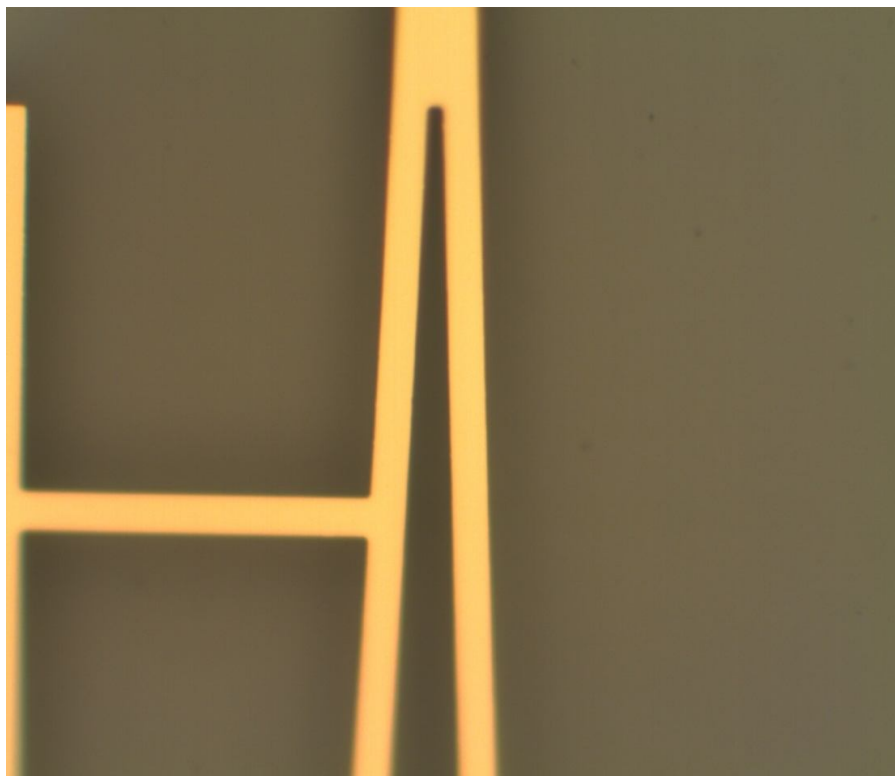
After the metal deposit of gold and chromium, the wafer was immediately immersed in a solution of resist stripper, *Microstrip 1165* [45], and agitated within an ultrasonic basin. The combination of chemical solution and physical agitation easily lifted off the bi-layer resists leaving behind the Au/Cr features on the SiO<sub>2</sub> layer. The details for this lift-off process can be found in *Table 7*. Again, it was very crucial to take note of the temperatures during lift-off in the Microstrip bath. The Microstrip was required to be heated up to 80°C in [51] in order to be effective. In the adapted lift-off process, the Microstrip 1165 baths were only heated up to 70°C to take extra precautions for the SiO<sub>2</sub> layer, as it is very sensitive to thermal effects.

Throughout, the lift-off process, the wafers were thermally monitored carefully so that the temperature does not rise above threshold limits resulting in *CYTOP* deformation due to thermal expansion as discussed in *section 3.5-1*, and shown in *Figure 19*. *Figure 43* shows the desired results after the metal-lift-off process has been completed. A successful metal deposition results in the desired width of 5µm (checked with microscope), thickness of 30 nm for Chromium and Gold combined (checked with Profilometer), and smooth Gold films and edges.

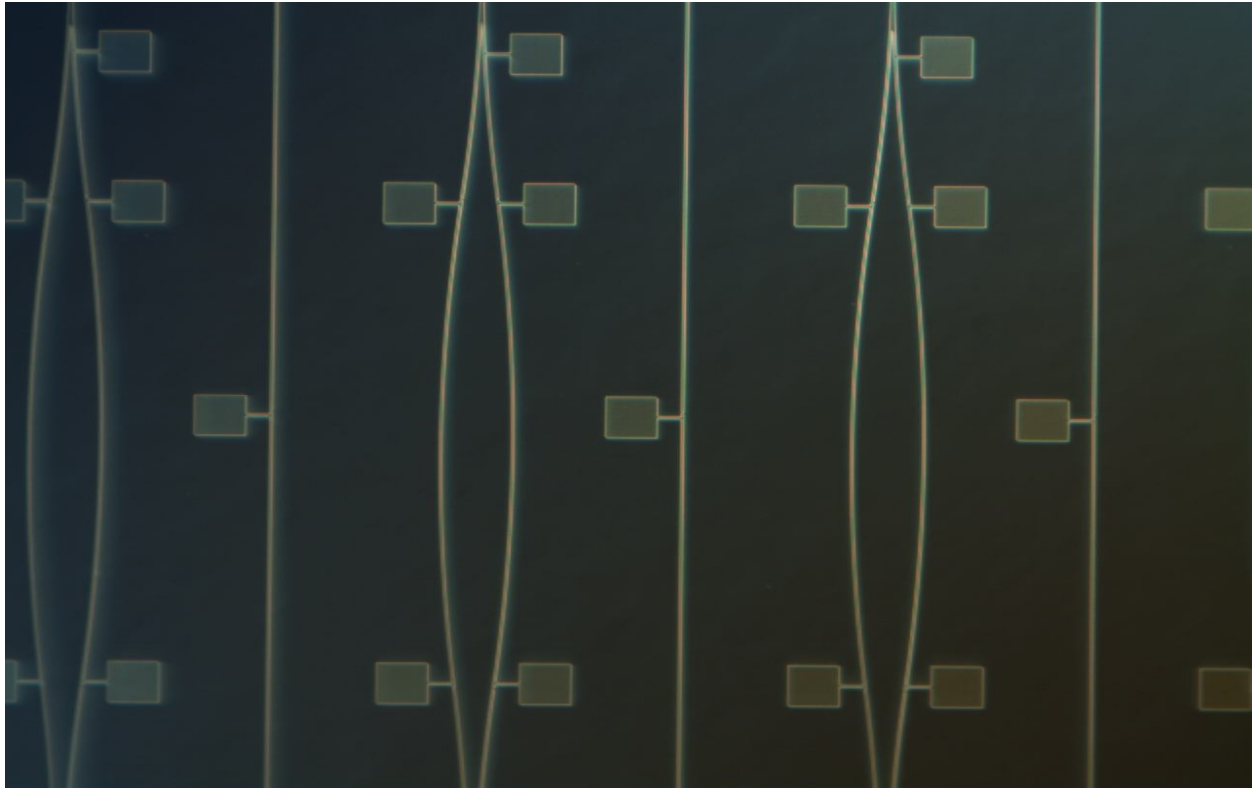
a)



b)



c)



d)

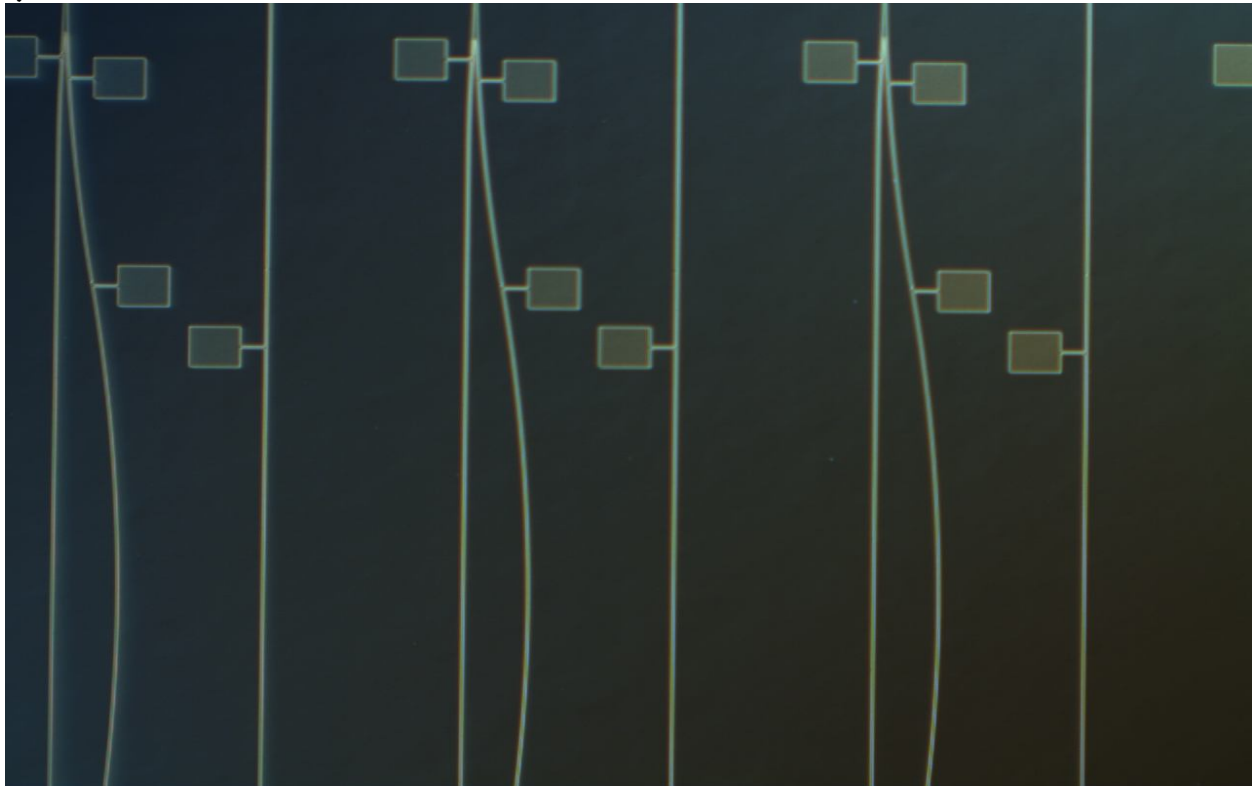


Figure 43: Desired Lithography results with accurate widths for the waveguides. a & b show results in 50x magnification. c & d show results in 20x magnification under polarized light.

Step #	Process Description	Details
1	Load Gold (Au) and Chromium (Cr) in the crucibles of electron beam evaporator (BALZERS).	Set Cr as target metal. Note the position of Au in the crucible, as the target will needed to be switched.
2	Load wafers in electron beam evaporator.	Vacuum chamber to $1 \times 10^{-6}$ .
3	Set Parameters (Deposition rate, Deposition Power, Desired Thickness etc.) for Cr. Deposition.	Target Thickness: 2nm (20 Å)
4	Deposit Cr, by carefully manipulating the shutter window between the evaporated target and wafer.	
5	Cool down the e-gun. Change the target to Au.	Cool for 10 minutes.
6	Set Parameters (Deposition rate, Deposition Power, Desired Thickness etc. ) for Au. Deposition.	Target thickness: 28 nm
7	Remove the wafers from e-beam evaporator.	
8	Immerse the wafer in bath 1 of Microstrip 1165 to lift-off the metal not deposited to lithographic features.	Static dip for 10 minutes.
9	Subject the wafers to ultrasonic agitation	For 10 seconds.
10	Immerse the wafer in bath 2 of Microstrip 1165 to lift-off the metal not deposited to lithographic features.	Static dip for 10 minutes.
11	Subject the wafers to ultrasonic agitation	For 10 seconds.
12	Immerse wafer in isopropyl alcohol (IPA) bath	Static dip for 10 minutes
13	Immerse wafer in de-ionized (DI) water	Static dip for 10 minutes

**Table 8: Process steps for metal (Cr + Au) deposition using e-beam evaporation and metal lift-off.**

#### 4.4.1 Metal Surface roughness Check:

The AFM measurements<sup>6</sup> given in *Figures 44 and 45* were used to check the metal thickness and surface roughness after the metal deposit and lift-off steps. The wafer that was sent out for AFM measurements had targeted thickness of 36 nm for the metal stack of (Cr+Au). The AFM results showed an actual metal thickness of 40 nm with surface roughness of 0.699 nm RMS. The metal thickness was about 10% thicker than the target 36 nm. This can be fixed by adjusting the deposition instrument's controller sensor to compensate for the overshoot. The width of the waveguide came out to be 4.9  $\mu\text{m}$ , which is slightly off from the target width of 5  $\mu\text{m}$ . The discrepancy in widths can be attributed to the lithography errors. The metal's surface roughness is very low ( $\ll 1\text{ nm}$ ), confirming the quality of e-beam evaporation for metal depositing. This suggests that the metal deposition process is a very surface-smooth procedure. The precision of the metal thickness and roughness is limited by the performance of the e-beam evaporator.

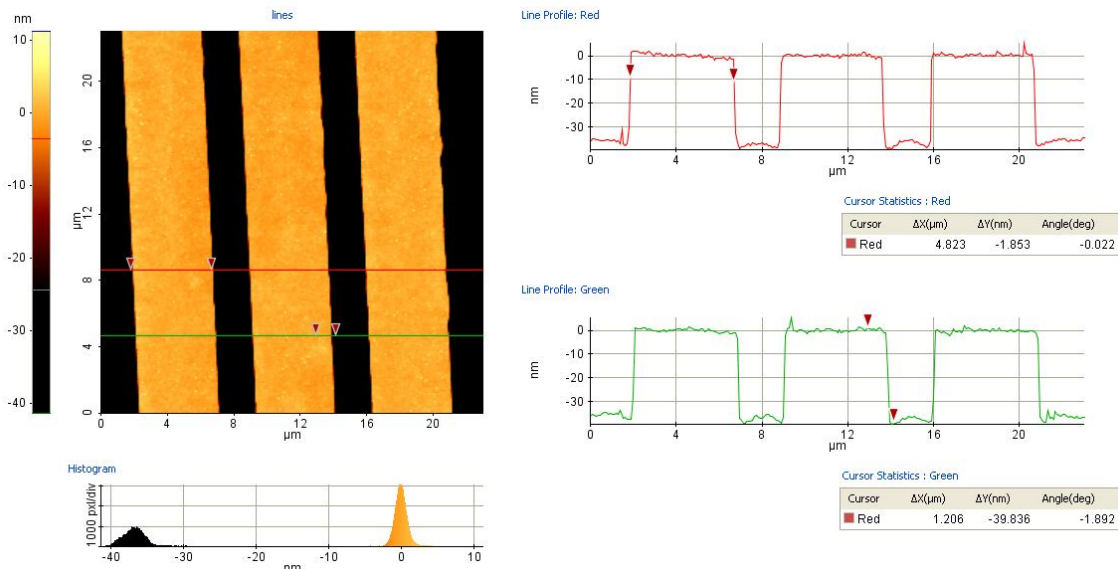


Figure44: AFM surface and dimension profiles of Au stripe waveguides on SiO<sub>2</sub>.

<sup>6</sup> The AFM measurements were obtained by Surface Science Western, University of Western Ontario

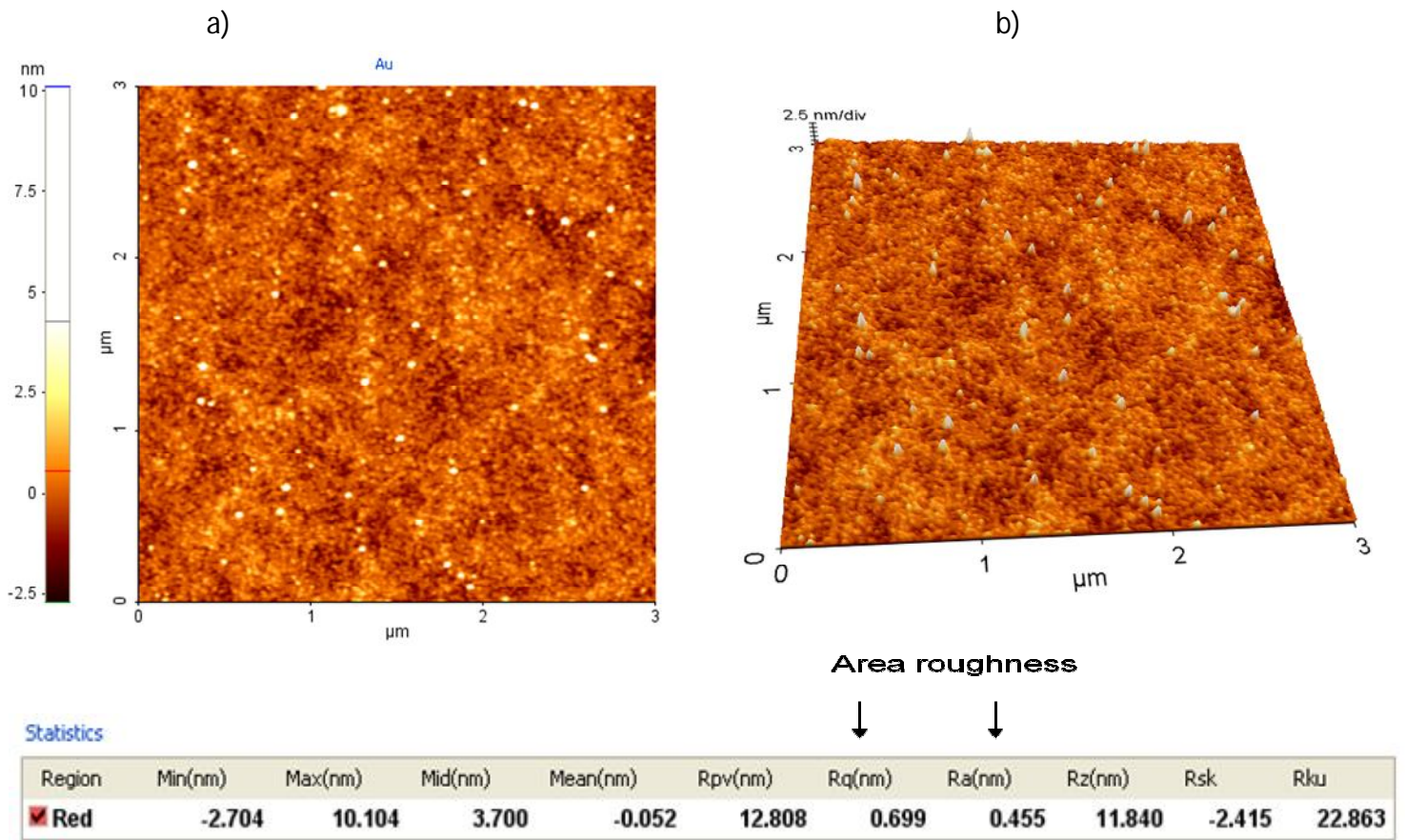


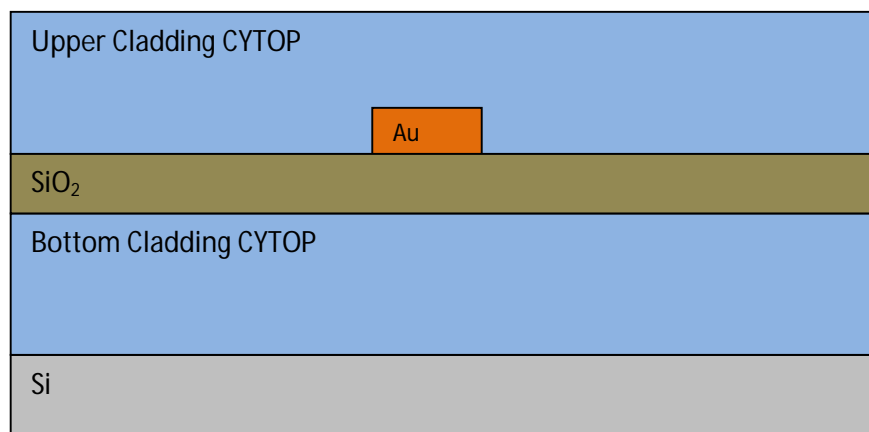
Figure 45 (a) *Au* surface amplitude measurement. Roughness = 0.699 nm RMS, 0.72 nm average. (b) *Au* Surface phase shift measurement

## 5 Top Cladding

### 5.1 Fabrication Process:

The top cladding of CYTOP on metal waveguides to create symmetric LRSPP supporting optical waveguides is described in this chapter. The top claddings are coated only after the metal waveguides have been properly patterned and deposited on the SiO<sub>2</sub> layer. *Figure 46* shows the end point of the top cladding process.

The wafer was first spin coated with 5% *M-grade* CYTOP to create an adhesion layer between the SiO<sub>2</sub> and the upper cladding CYTOP layers. After the adhesion layer it was further spin-coated with multiple bulk-layers of 9% *S-grade* CYTOP. Detailed spin-coat conditions are outlined in *Table 9* and sketched in *Figure 47*. Each layer underwent 30 minutes of soft-bakes at 50 °C before successive layers were spin-coated. A slow and higher temperature bake was applied at the end (*Table9, Step 6*) to evaporate the solvent. The goal is to complete the following structure of the biosensor:



**Figure 46: LRSPP Gold (Au) waveguide embedded in Cytop.**

Step #	Process Description	Details
1	Spin coat 5% CTL-809M CYTOP on Si wafer as an adhesion layer between SiO <sub>2</sub> and thicker <i>CYTOP</i> upper-cladding layers.	Spin Speed: 500 RPM for 10 seconds followed by 1000 RPM for 20 seconds. Thickness: ~0.40 μm
2	Soft bake the wafer on hot plate for solvent evaporation.	@ 50°C for 30 minutes.
3	Spin coat 9% CTX-809SP2 (S-grade Cytop)	Spin Speed: 1000 RPM for 10 seconds, followed by 4000 RPM for 20 seconds. Thickness: ~ 1.35 μm
4	Soft bake the wafer on hot plate for solvent evaporation.	@ 50°C for 30 minutes.
5	Repeat Steps 3 and 4 five times to attain the desired thickness.	Final thickness of 8 μm.
6	Hard-bake for complete solvent evaporation.	Temperature ramp of 20°C / hr, from 50°C to 90°C in 2 hour. Hold @ 90°C for 2 hours.

**Table 9: Fabrication process flow for upper claddings of CYTOP.**

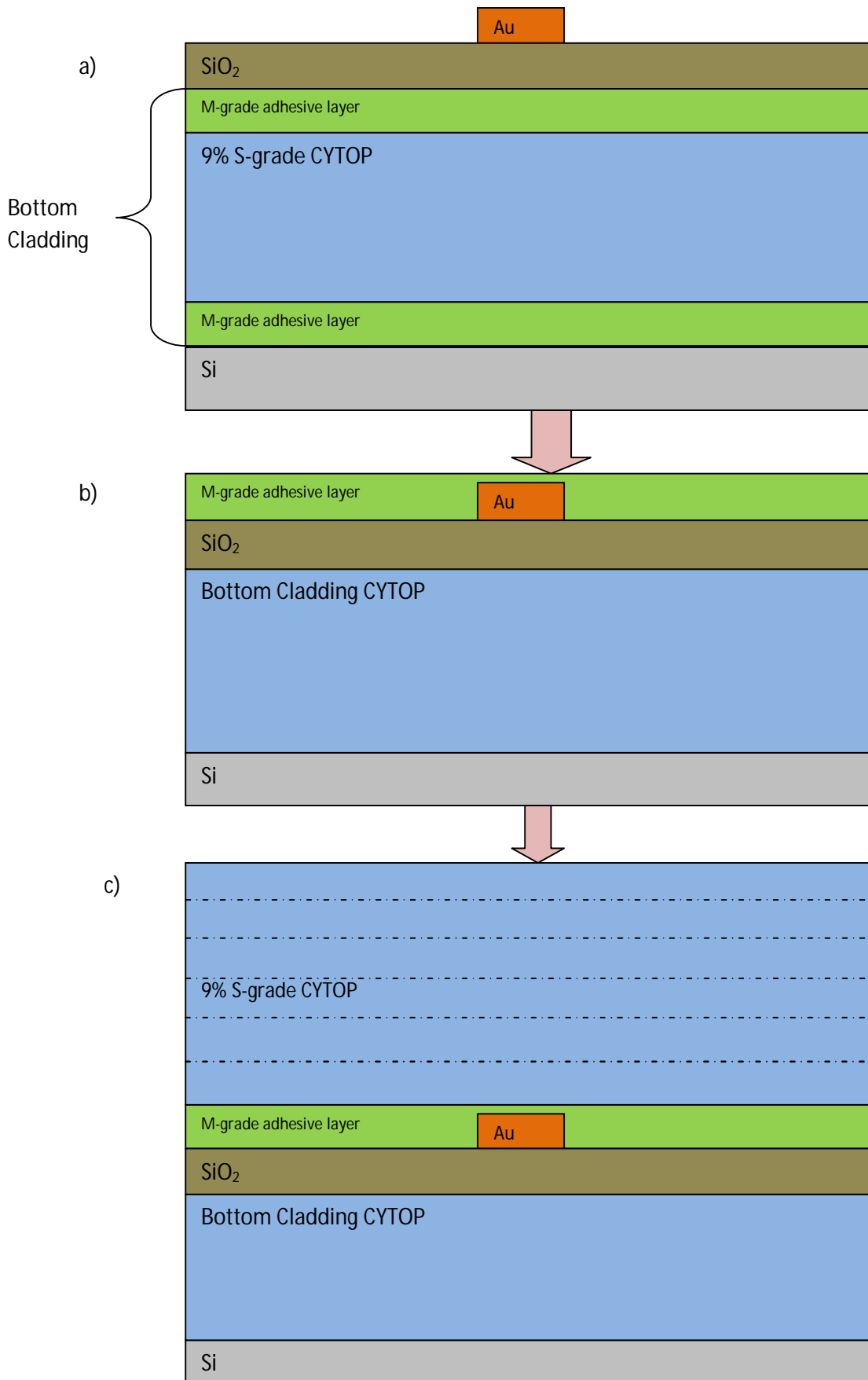


Figure 47: Schematic of implementing top cladding for the embedded waveguide structure

## 5.2 Thermal and Solvent Issues with CYTOP:

The curing process of upper claddings is not as straightforward as it was for the bottom cladding. In previous experiments directly cladding thick CYTOP layers deformed the metal waveguides due to thermal expansion and solvent interactions with the metal as well as the bottom cladding CYTOP. As mentioned earlier, heating CYTOP above its  $T_g = 105\text{ }^\circ\text{C}$  will deform the metal waveguides and the  $\text{SiO}_2$  thin layer. The reason for this behaviour can be attributed to the thermal expansion coefficient (TEC), which shows sudden variations within the range of the glass transition temperature. Thus, the device deformation worsens as the bake temperature increases. The second factor affecting the metal layer is CYTOP's intrinsic weakness to its solvent, which is already been discussed in *section 3.5-1*.

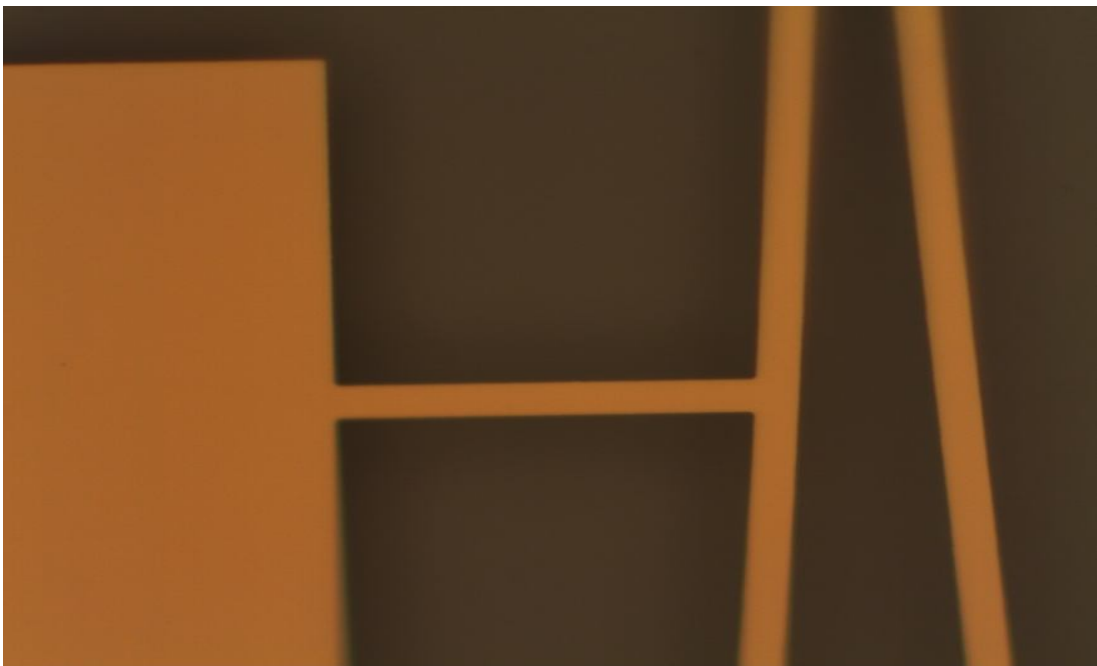
Considering the two problems mentioned above, it was necessary to design a procedure which involved a fast and effective way of evaporating as much solvent as possible, and a hard-bake process below  $T_g = 107\text{ }^\circ\text{C}$ . To minimize the solvent content, all top CYTOP layers were cladded with 9% concentration of *S-grade* CYTOP so that we have a higher concentration of CYTOP relative to solvent, and spun with a very fast spin speed (4000 RPM) to attain a very thin CYTOP layer. To address the thermal issues related to CYTOP curing process, all soft-bakes were done at  $50\text{ }^\circ\text{C}$  and the hard-bake temperature was limited to  $90\text{ }^\circ\text{C}$ . In order to reduce damage caused by gas leakage, a very slow temperature ramp of  $20\text{ }^\circ\text{C}/\text{hour}$  was used to raise the temperature to  $90\text{ }^\circ\text{C}$ . Once the wafer reached  $90\text{ }^\circ\text{C}$ , it was held there for an additional 2.5 hours to make sure all the solvent has evaporated from the CYTOP. The result from these cladding conditions is shown in *Figure 48*. There is no surface bulging at large metal areas (i.e. contact pads) and arm joints compared to the results of previous micro-fabrication process

shown in *Figures 19 and 20* in *section 3.5-1*. Also, there are no obvious observable deformities across the length of the waveguide devices.

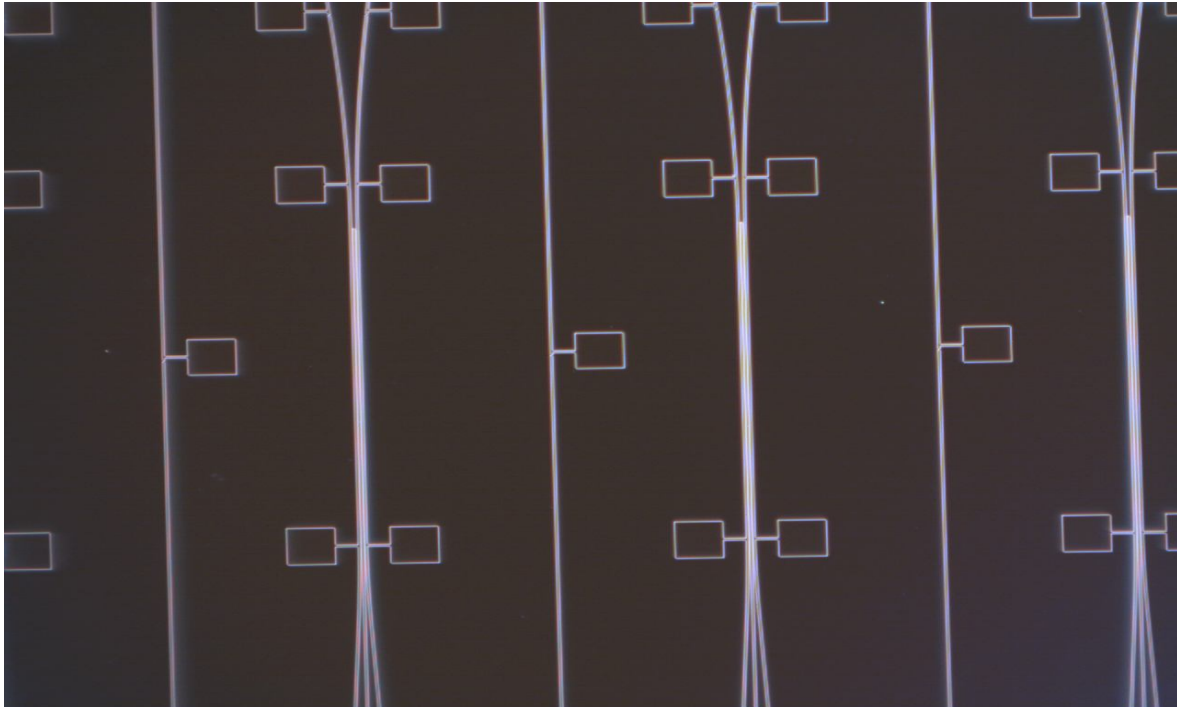
a)



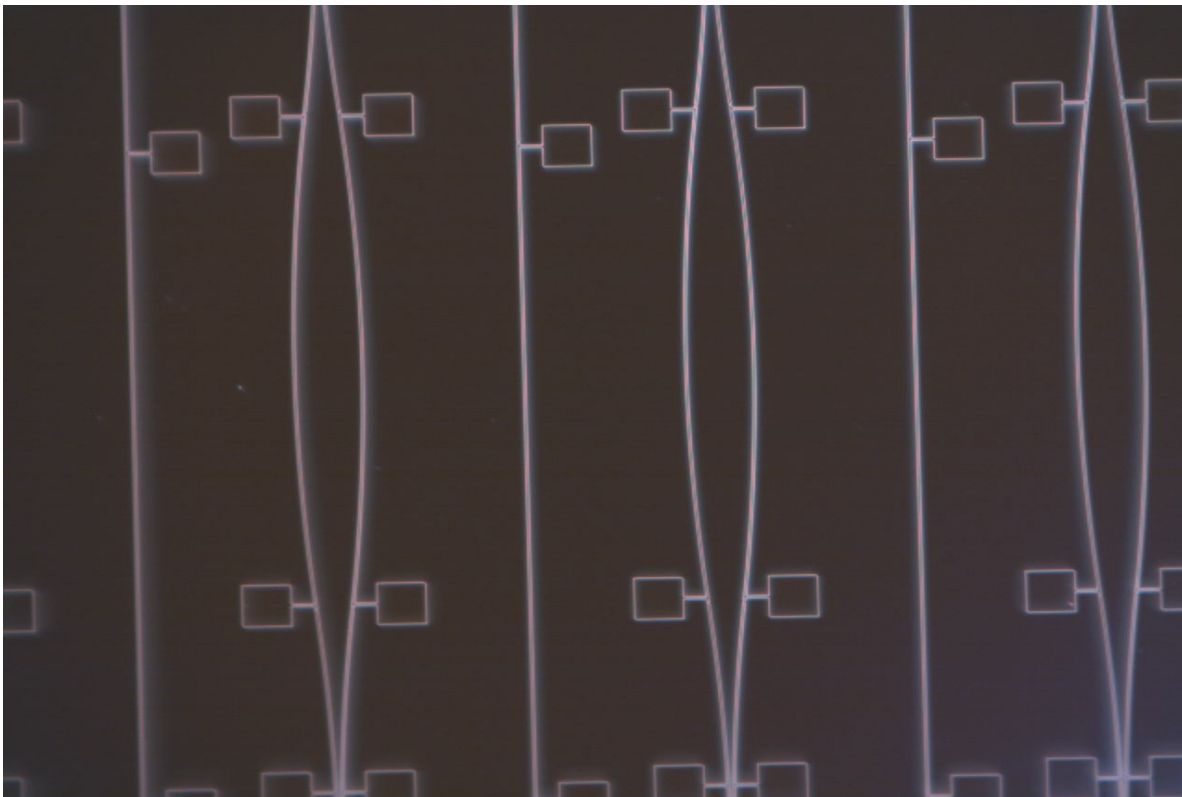
b)



c)



d)



**Figure 48: a,b) Fully cladded waveguides with smooth metal waveguides under 50x magnification. c,d) waveguides under polarized light and 20x magnification with very smooth waveguide features and CYTOP surroundings**

The thickness requirement for the top CYTOP cladding is the same as the bottom cladding to create symmetric LRSPP waveguides. Specifically, it has to be greater than 7  $\mu\text{m}$ . However, in the upper cladding process, it is only possible to spin one thin CYTOP layer at a time, as opposed to fewer thick layers in the lower cladding in order to minimize the amount of solvent we introduce in coating each layer. Therefore, the thickness for different layers spin-coated onto silicon wafers was measured with the *Metricon* as shown in *Table 10*.

<b>9% S-Grade Layers</b>	<b>Index</b>	<b>Thickness (<math>\mu\text{m}</math>)</b>	<b>% Standard Deviation</b>	<b>Target Thickness</b>
6	1.3387	8.02	0.49	6.0
8	1.3386	10.180	0.84	8.0
9	1.3386	11.712	0.71	9.0

**Table 10: Thickness and optical index measurement of top CYTOP claddings using Metricon prism-coupling.**

The refractive index of CYTOP upper cladding layers matches that of the lower claddings (~1.3386). Therefore, symmetric LRSPP waveguide structures can be realized using these CYTOP cladding processes. The thickness measured for each 9% *S-grade* CYTOP layer spun at 4000 RPM is around 1.3  $\mu\text{m}$ . During spin-coating of upper-cladding layers of CYTOP, it was observed that thin threads of CYTOP spun off the wafer. This can be attributed to large amount of polymer concentration spinning at very high speeds compared to the spin-coating process for the lower cladding, which required relatively lower spin-speeds. However, this was the only way of coating CYTOP while delivering the least amount of solvent for every spin-coated layer. Following *Table 10*, we see that 6 layers yielded 8  $\mu\text{m}$ , which satisfies the thickness requirements for CYTOP upper cladding needed to build symmetric LRSPP waveguides. The surface roughness check was not performed because no new layer of devices was to be built on top of the claddings. The Micro-fluidic channels are etched into the CYTOP upper cladding without introducing any new lasting material in the biosensor structure.

## 6 Micro-fluidic Channels

### 6.1 Micro-fluidic Channels Masks:

The implementation of fluidic flow channels within an integrated sensing chip is one of the most desirable features of a biosensing device. Not all structures embedded in CYTOP should be etched away; some are required to be embedded in CYTOP claddings for different reasons. In order to create fluidic channels on specific waveguide devices, it was necessary to design a mask, which would only expose certain areas that are going to be etched away to create the flow channels for biosensing. The lithography step for creating micro-fluidic channels is followed after the top CYTOP claddings have been coated and hard-baked as explained in Chapter 7. The main purpose behind this second level of lithography is to pattern the sensing arms of various MZI devices and then expose to plasma etching. This is a necessary step for biosensing because the exposed waveguides can then be chemically functionalized and immersed in aqueous buffer solutions. This Chapter describes in detail two different masks used for flow channels, their lithographic definition, and finally the CYTOP etch step to create flow channels within the integrated waveguides.

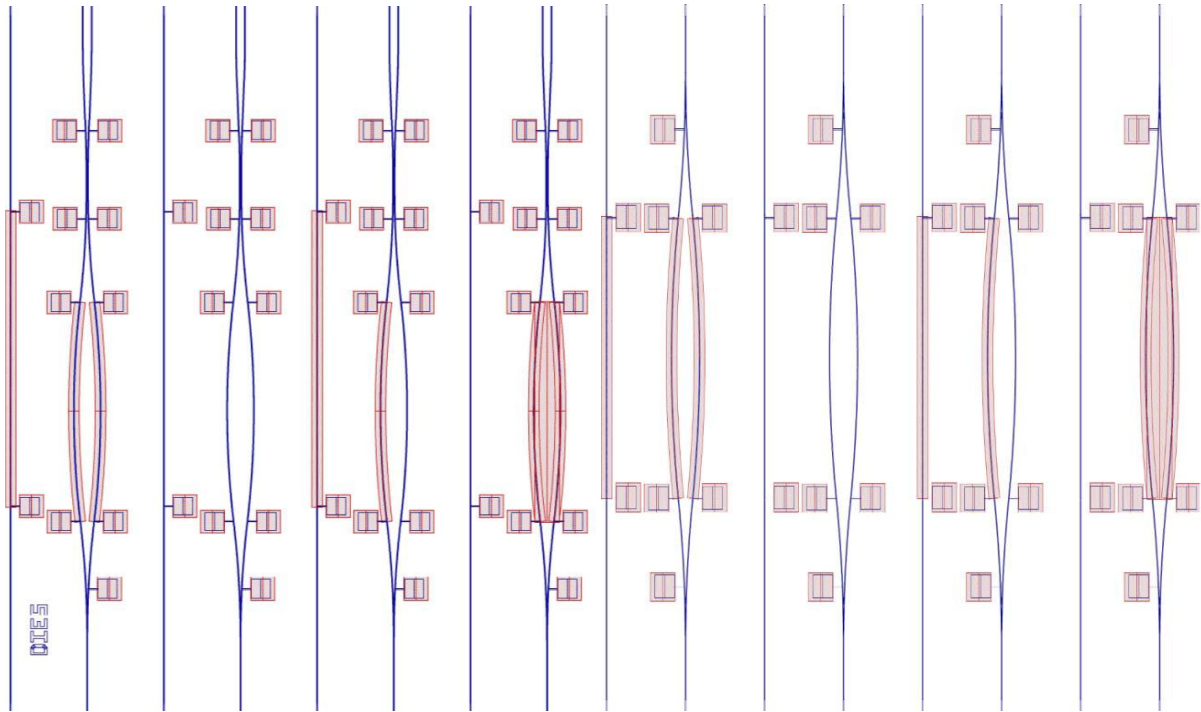
Both micro-fluidic channel masks were designed with the commercial software DW-2000<sup>7</sup>. The schematics of the first mask are shown in *Figure 49*. Mainly, four types of patterns were designed for each die, which consisted of no openings, one arm open, two arms open separately, and two arms open together. The MZI with no openings are completely embedded in CYTOP claddings, because part of the wafer is not intended for bio-sensing. These devices are used for optical characterization of embedded waveguides and structures. The MZI with one

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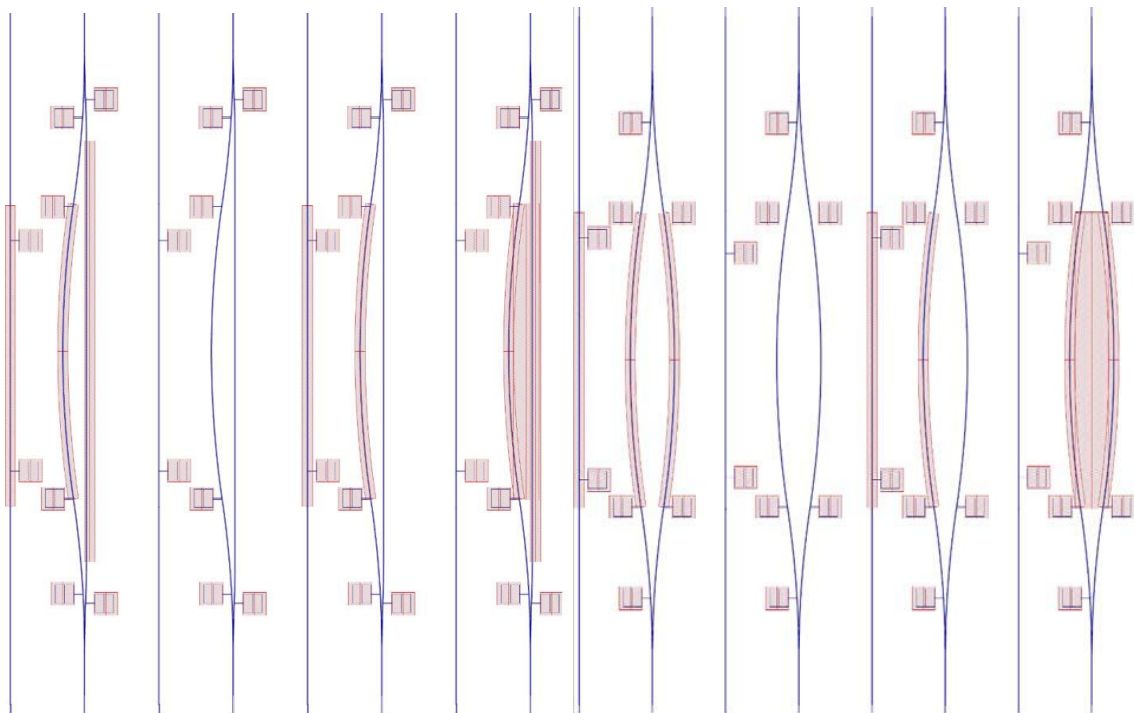
<sup>7</sup> The masks were designed by Charles Chiu and Ewa Lisicka-Skrzek, University of Ottawa.

arm open presents the advantage of having one arm being physically isolated from the sensing fluid, which makes the application of surface chemistry much easier. The reason for incorporating varying designs of MZI bio-sensors with separate and combined openings is for the purpose of studying liquid flow effects in different biosensing configurations. In addition to MZI devices, straight waveguides were also patterned to be exposed for optical characterization tests on waveguide performance in CYTOP and in the sensing fluid. The width of single exposed channels is 55  $\mu\text{m}$  with varying lengths between 1.231~1.631 mm.

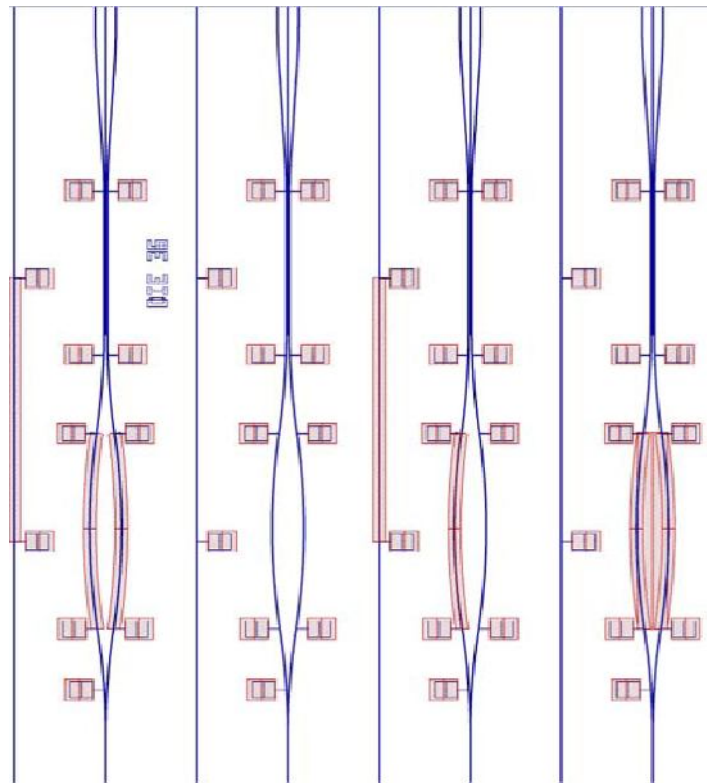
a)



b)



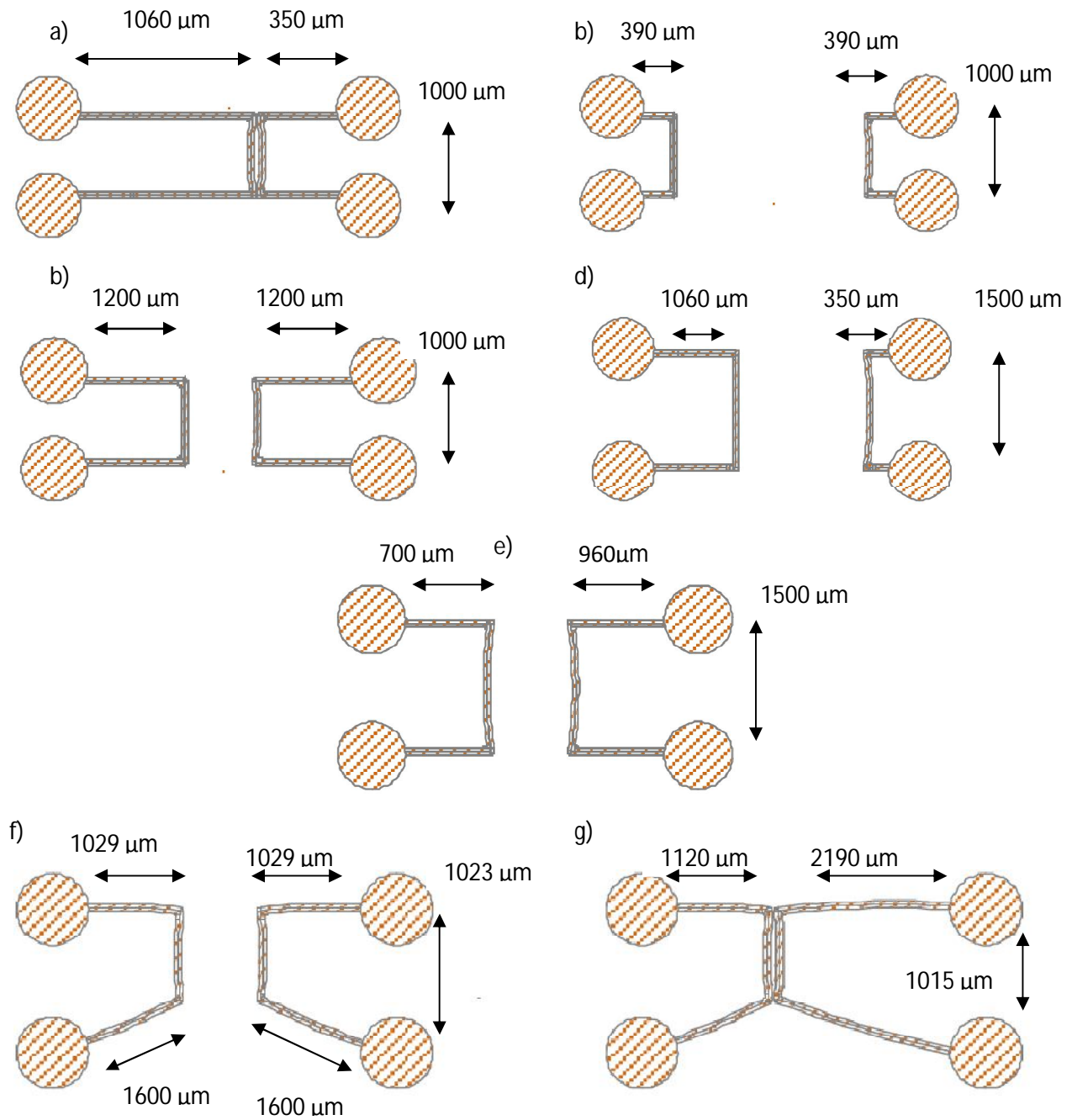
c)



**Figure 49: (a) 3.0 mm devices, 1.236 mm channels (b) 3.8 mm devices, 1.613 mm channels (c) 4.8 mm devices, 1.613 mm channels [51].**

A second mask was designed to enforce a more controlled introduction of bio-chemical agents and fluids through larger etched circular holes with canals towards a few MZI biosensing devices. Another purpose behind the larger features for this mask is that the future work for these biosensing devices includes implementing a glass-lid on top of the embedded biosensor with drilled holes equal to the size of the etched CYTOP holes fabricated in current devices for better packaging of the biosensor. Again, in this design of micro-fluidic mask, four types of patterns were designed for different dies with varying lengths of flow-canals and the fluidic channel on top of sensing MZI devices as well as some straight waveguides. This consisted of devices with no openings, one arm open, two arms open on different MZI, and two arms open

on the same MZI. The diameter of the circular features is  $800\ \mu\text{m}$ . *Figure 50* illustrates different features of this mask. The width of single exposed channels is  $80\ \mu\text{m}$  with varying lengths between  $900\text{--}2230\ \mu\text{m}$ .



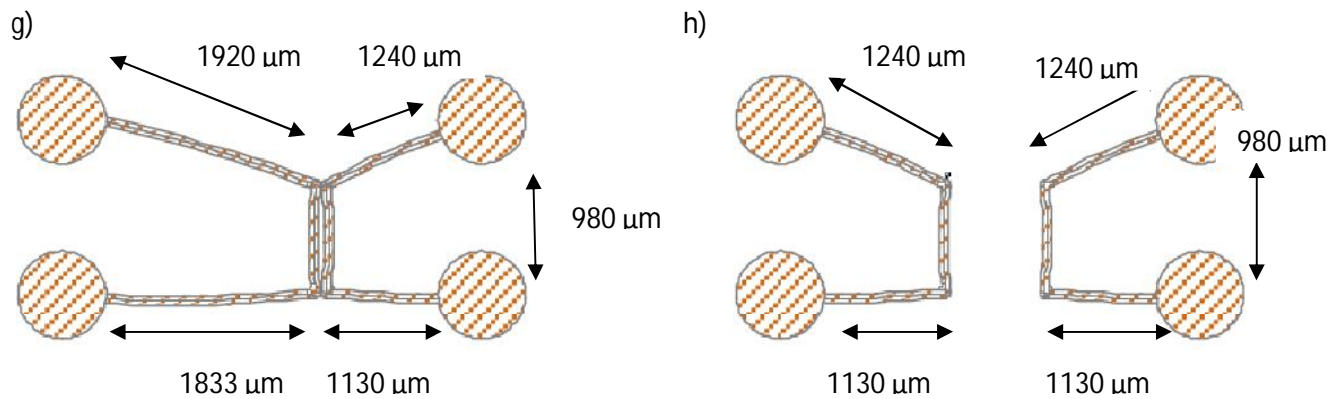


Figure 50 : Patterns of mask used for Micro-fluidic channels design.

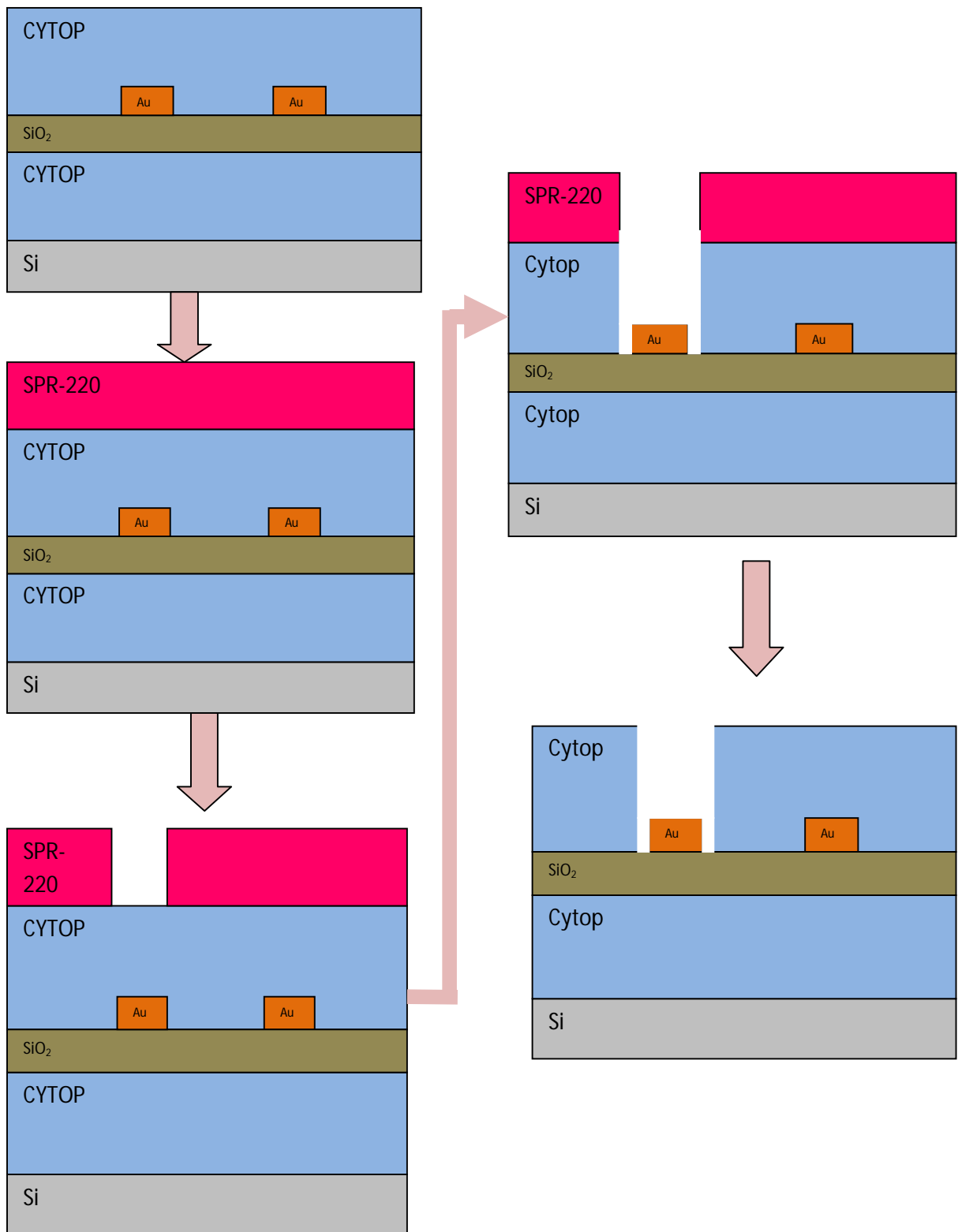
## 6.2 Micro-fluidic flow-channels lithography:

The thickness of the top CYTOP cladding measured in *section 5.3* is approximately 8  $\mu\text{m}$ . In order to acquire the desired profile of micro-fluidic channels on CYTOP, a thick coating ( $\sim 10 \mu\text{m}$ ) of photoresist was required to effectively define and develop the flow-channels features. The reason for a thick layer of photoresist is that during the  $\text{O}_2$  plasma etching of CYTOP process to create flow channels (*section 6.3*), part of the photoresist is also etched away. Thin layers of photoresist would be etched away instantly, and  $\text{O}_2$  plasma would start etching the CYTOP upper cladding not intended to be exposed to  $\text{O}_2$  plasma. The photoresist SPR-220-7 was chosen because it was possible to coat above 15  $\mu\text{m}$  with one spin [44]. The spin coat process (*Table 11, Step 4-5*) yielded a 10  $\mu\text{m}$  thick resist layer. Again, the thermal effects of the soft-bake and hard-bake of the photoresist had to be accounted for in order to sustain uniform thin  $\text{SiO}_2$  layer. The temperature for hard-bake process for the photoresist had to be kept under 107°C, below the glass-transition temperature of  $\text{CYTOPT}_g = 107^\circ\text{C}$ . Therefore, the hard-bake was done at 105°C for 3 minutes, to obtain the desired thickness of the photoresist, as well as

keeping the SiO<sub>2</sub> layer stable. The process is outlined in *Table 11* which was derived from referencing the manufacturer technical sheets, and sketched in *Figure 51*.

Step #	Process Description	Details
1	Mildly Ash CYTOP of Upper Cladding in O <sub>2</sub> plasmas to roughen the surface to promote adhesion.	10 seconds for 4" wafer.
2	Spin coat hexamethyl disiloxane (HMDS) for resist adhesion.	Spin @ 1000 rpm for 10 minutes.
3	Bake on hotplate	105°C for 1 minute
4	Spin coat SPR-220-7 for a thick positive resist layer	1000 rpm for 30 seconds; 2300 for 10 seconds (~ 10 µm thick)
5	Soft-bake on hotplate	35 °C for 30 seconds; 105°C for 3 minutes.
6	Load Microfluidic Channels mask in mask aligner..	Align the features on the mask to the specific embedded waveguide devices.
7	UV exposure	90 – 100 seconds for thick ~8 µm top cladded CYTOP wafers.
8	Photo-reaction hold	Keep the wafer at room temperature for at least 2 hours to allow solvent to diffuse back into photoresist film.
9	Post exposure hard-bake	@ 105°C for 2 minutes.
10	Develop features in MF-24 A	For 2 minutes with strong agitation.
11	Features inspection	Check alignment of fluidic channels with waveguide devices. Also, look for colour fringes for possible incomplete etching of resist.

**Table 11: Process flow of fabricating micro-fluidic channels.**



**Figure 51: Process flow of forming flow-channels by etching top CYTOP cladding.**

The bake procedure for the photoresist before UV exposure required a two-stage step-up in temperature from 35 °C to 105 °C. This was necessary because the direct introduction of spin coated SPR-220-7 to high temperature of 105°C resulted in the resist forming uneven spattering patterns across the surface. The suspected reason for this was mainly uneven thermal distribution along with the high thickness and viscosity of the resist. The soft bake at 35°C helped to slowly distribute heat evenly across the wafer.

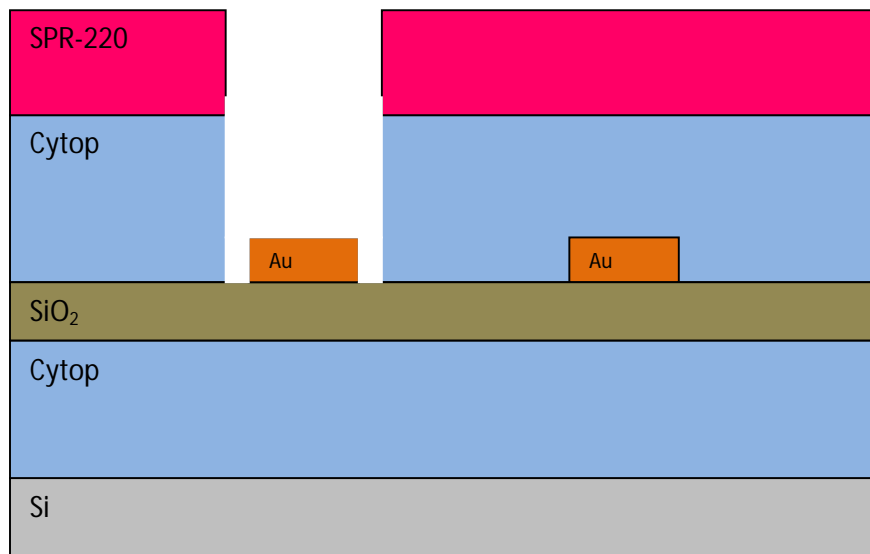
Due to the relatively high thickness of SPR-220-7 (~10 µm), longer UV exposure time is needed to allow UV radiation to define the flow channels patterns throughout the depth of the photoresist. It was determined that an exposure time of at least 90 seconds was needed to have well-defined micro-fluidic channels. One of the difficulties in this experiment was to ensure that all the patterned resist have been etched away after development in MF-41 A. Under-development could possibly leave a residue layer of resist on top of the patterned openings. To check if the channels were fully developed, the patterned openings were tested for roughness using a surface profiler. The difference in surface roughness of CYTOP and the photoresist serves as a good indication of complete development of flow channels. A microscopic check was also performed by carefully checking for the existence of colour variations and fringes on the patterned surface and edges.

The photo-reaction hold time of 2 hours in between exposure and development processes (*Table 11, Step 8*) was a necessary step because the thicker resist required a longer hold time in order for water to diffuse back into the film and complete the photo-reaction process [44]. The post exposure bake (*Table 11, Step 9*) was also recommended by the

manufacturer. It was observed that bypassing the two steps (*Table 11, Step 8-9*) yielded longer or incomplete development of photoresist etches.

### 6.3 O<sub>2</sub> plasma CYTOP etch:

In order to deliver sensing fluids to the waveguide devices, the top cladded CYTOP must be removed methodically to expose the sensing waveguide arms. The resulting channel opening serves as the main structure to introduce fluids for biosensing as shown in *Figure 52*. The popular way of etching a polymer like CYTOP, is to dry etch it with plasma. Reactive Ion etching consists of bombarding the target material with highly energetic chemically reactive ions generated with different reactive gases. Reported work on etching CYTOP using RIE with O<sub>2</sub> and O<sub>2</sub>/CHF<sub>3</sub> chemistry are explored in [43]. Similar experiments were performed on CYTOP wafers to determine the etch rate of CYTOP with anisotropic RIE using O<sub>2</sub> plasma in [51], which resulted in smooth anisotropic micro-fluidic channels in the fully integrated biosensor.



**Figure 52: Schematic representation of etched flow channels using O<sub>2</sub> plasma**

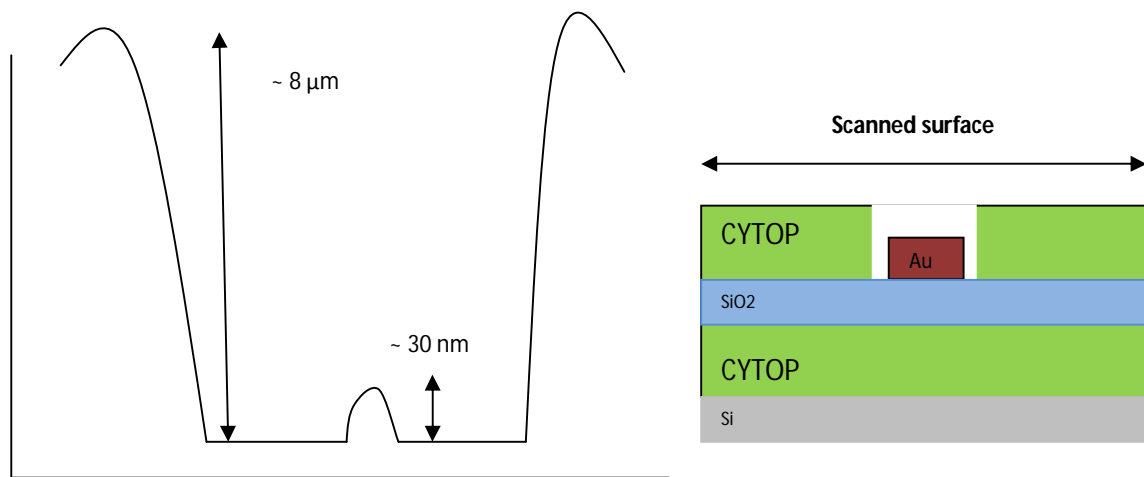
Etching CYTOP using CF<sub>4</sub>/O<sub>2</sub> plasma chemistry was not used for the creation of flow channels within upper cladding of CYTOP because previous experiments conducted in [51]

showed very undesirable results with  $\text{CF}_4/\text{O}_2$  plasma chemistry. The results presented very unusual profile of the CYTOP etch, where the etch chemistry seemed to be cutting into the sidewalls centered at the interface between the *CYTOP* and the resist. It is suspected that the  $\text{CF}_4/\text{O}_2$  etch chemistry may be very aggressive to CYTOP.

Therefore, creation of micro-fluidic channels on embedded waveguides was done using a pure  $\text{O}_2$  etch in order to create more anisotropic etched channels. The plasma etch was carried out using  $\text{O}_2$  flow rate of 100 sccm and power of 200 W. Some experiments were also carried out under 100 W of plasma power, but the etch rate was determined to be very slow, so the final devices were fabricated using 200 W power to etch micro-fluidic flow channels. The average etch rate of CYTOP under  $\text{O}_2$  plasma was measured to be around  $0.9 \mu\text{m}/\text{minute}$  in [51]. The etch profiles using  $\text{O}_2$  are much more ideal, as the CYTOP etch resulted in deep and anisotropic sidewalls.

In previous experiments described in [51], it was noted that without the  $\text{SiO}_2$  etch-stop layer there was an over etch of  $\sim 1\text{-}2 \mu\text{m}$  due to various uncontrollable factors presented during the  $\text{O}_2$  plasma etch process. The  $\text{SiO}_2$  layer acted perfectly as an etch-stop layer, which was concluded after different experiments done in *section 3.5-2*. Considering the etch-rate of CYTOP ( $\sim 0.9 \mu\text{m} / \text{minute}$ ), the wafer was etched for 15 minutes under  $\text{O}_2$  RIE plasma. This should have resulted in etch depth of about  $\sim 13.8 \mu\text{m}$ . The etch depth on average was consistently  $\sim 8 \mu\text{m}$ , which was checked using surface profilometry. The surface profilometry showed a step curve equal to that of exposed waveguides of accurate thickness ( $\sim 30 \text{ nm}$ ). Therefore, the problem of over-etching the CYTOP was avoided using the  $\text{SiO}_2$  etch stop layer, and further enabled us to

fabricate uniform, and accurate micro-fluidic flow channels within the integrated biosensor structure. *Figure 53* is an illustration of a common surface profile when scanning across a single exposed metal waveguide. An actual profilometry figure cannot be shown because the equipment used for surface profilometry did not allow the results to be saved.



**Figure 53: Representation of Surface probe profilometry across an etched micro-fluidic channel with exposed metal waveguide.**

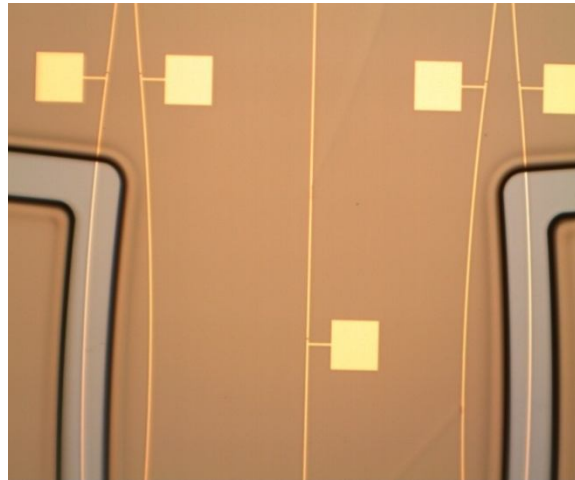
The successful etch of the micro-fluidic channels is the final step in the fabrication process for embedded LRSP *Au* waveguide biosensors. Therefore, microscope inspections of the devices with micro-fluidic channels are presented in *Figures 54*. The final devices used for optical characterization were fully embedded *Au* waveguides in CYTOP with SiO<sub>2</sub> barrier layer, shown in *Figure 46* of *section 7.1*. The reason for this is that the devices that were fabricated with micro-fluidic channels exhibited poor adhesion between the CYTOP claddings and the SiO<sub>2</sub> layer. There is a dicing process performed after the fabrication process is completed in the lab, to dice the wafer into dies of varying lengths, which can then be used for optical measurements. The poor adhesion in the wafers with integrated micro-fluidic channels resulted in lifting of CYTOP cladding and the *Au* waveguides. The adhesion problem was later resolved by

performing an ashing process of upper cladding CYTOP (*Table 4, step1*) and cleaning the CYTOP surface with acetone and isopropyl alcohol (*Table 4, step2*). This improved the adhesion of the SiO<sub>2</sub> layer with the surrounding claddings dramatically. Unfortunately, this was realized very late into the thesis progress. Due to time constraints, the wafer used for optical measurements were kept fully cladded to avoid potential problems relating to reaction of O<sub>2</sub> plasma with the SiO<sub>2</sub> layer. Also, the effects of SiO<sub>2</sub> layer on propagation of LRSPP mode in fully embedded devices needed to be studied first for optical testing and characterization.

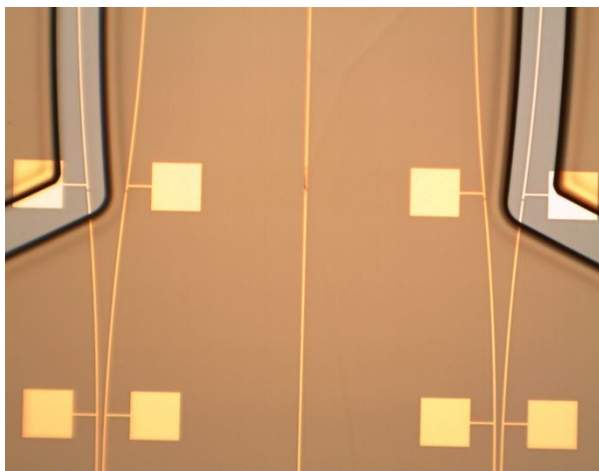
a)



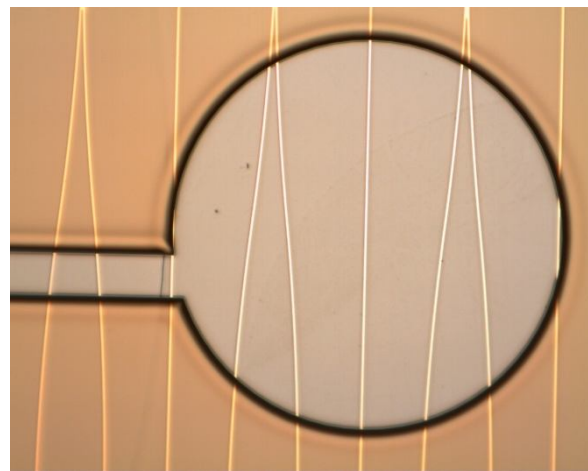
b)



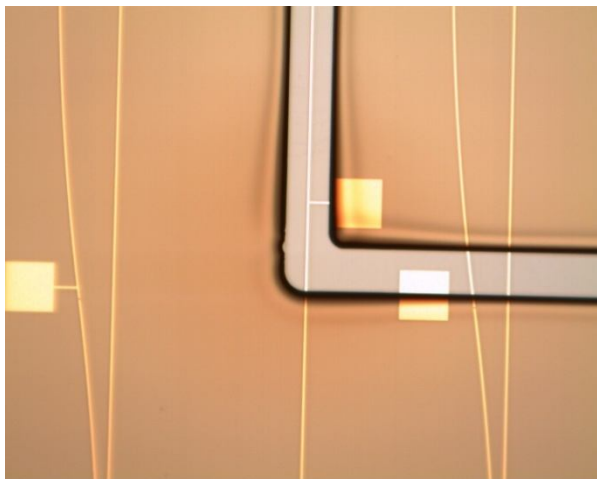
c)



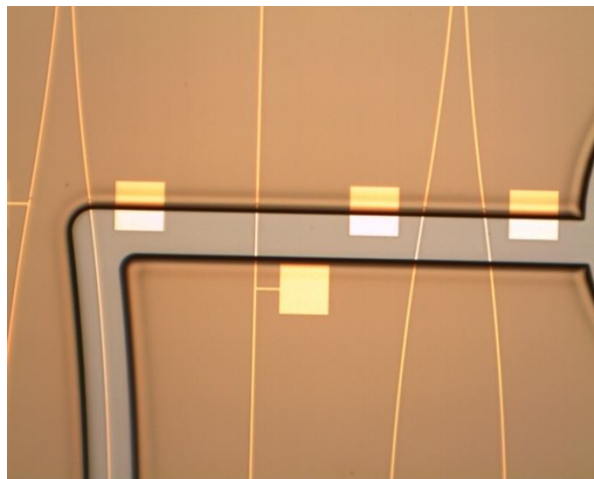
d)



e)



f)



**Figure 54: Microscope images of etched micro-fluidic flow channels**

## 7 Optical Characterization

### 7.1 Setup Description

There are several methods of LRSPP mode excitation along a symmetric waveguide. The prism coupling technique illustrated in Figure 4 can also be used to excite LRSPP mode but requires accurate precision with placement of the base of high-index prism on top of an embedded metal stripe. The angle of incidence of the input light also has to be precisely controlled while making sure that the permittivity of the claddings ( $\epsilon_{r,3}$  and  $\epsilon_{r,1}$ ) covering the metal stripe ( $\epsilon_{r,2}$ ) are index-matched [57]. Another method explored to excite LRSPP modes on metal waveguides is through broadside excitation using tapered fibre in [34]. A difficulty with this method is that it requires accurately cleaving the fibre tip at a set angle. The devices used in LRSPP mode excitation experiments [34] were only bottom cladded with CYTOP. Therefore, in order to have index-matched claddings around the metal stripe, it was necessary to submerge the devices in a liquid that is index-matched to CYTOP. This method of LRSPP mode excitation resulted in large losses in terms of power coupling efficiency. One of the reasons for this is that this setup required using tapered fibres and placing them so that the incident light coupled onto the waveguide at an angle. Tapered fibre were also used for the characterization of fully embedded waveguides with a SiO<sub>2</sub> barrier layer in order to reduce scattering light at the facet due to radiation caused by SiO<sub>2</sub> slab underneath the waveguides. It was hoped that tapered fibre would help focus the input power from the fibre precisely on to the metal waveguide at the facet interface of the die; thus avoiding the SiO<sub>2</sub> layer at the facet causing the input light to radiate in the SiO<sub>2</sub> slab. Although the mode at the output had minimal radiation in

its surrounding, the mode profile was relatively weak. The results are shown in *Figure 64* in *Appendix B*.

The devices that were optically tested for this thesis were completely embedded in CYTOP. End-fire LRSPP excitation method was adapted because it was relatively easy to implement and provided good results in previous experiments [51]. The fabricated wafer was diced using a dicing saw, because cleaving the wafer resulted in metal waveguides and SiO<sub>2</sub> layer lift-off due to uneven and rough cuts around the facets of the embedded waveguides. After the dicing process, dies of different lengths were placed in an optical characterization setup shown in *Figure 56*. The setup consisted of separate micro-positioners for input/output optical fibres, and the die holder. The micro-positioners for the input/output fibres are capable of 5 degrees of freedom for adjustment, which includes movement in the X-Y-Z axis, rotation in X-Y axis, and rotation in X-Z axis illustrated in *Figure 55*. The input fibre is a polarization-maintaining (PM) fibre. The orientation of the fibre is so that the H-field is polarized horizontally (TM). The output fibre (SMF) measures the power output at the end facet of the waveguide. The laser wavelength used for optical measurements of embedded waveguides is 1310 nm. The core of both fibres is 7 µm in diameter. The die was placed in between the fibres on top of a 2-degree micro-positioner, which allowed manipulation of the die placement in Y-Z axis. A microscope was placed on top of the die, which was used for visual alignment between the devices and the fibres. The described setup showed in *Figure 56*, enabled sufficient MPA (mode power attenuation) measurements of CYTOP embedded devices.

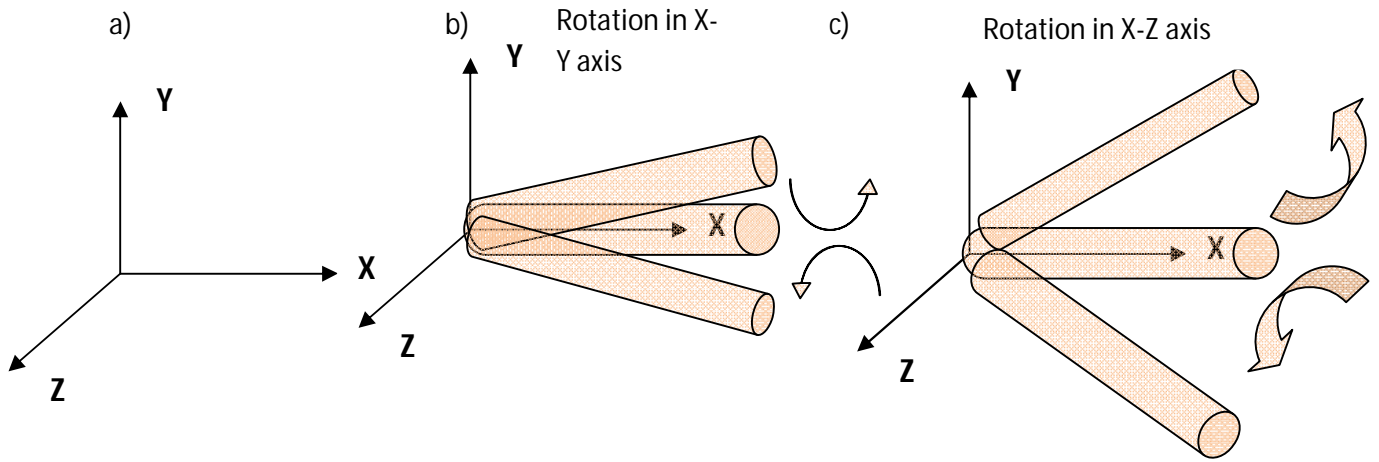


Figure 55: Degrees of freedom for fibre alignment to the embedded waveguide a) along the X-Y-Z axis b) rotation in X-Y axis c) rotation in X-Z axis.

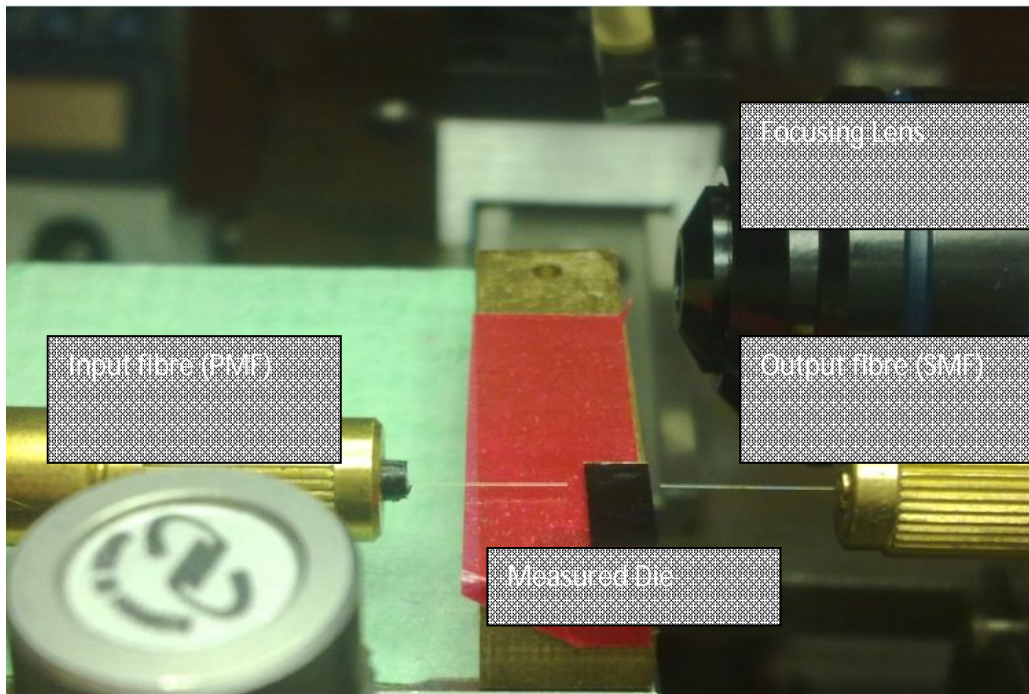


Figure 56: Equipment setup for optical measurements.

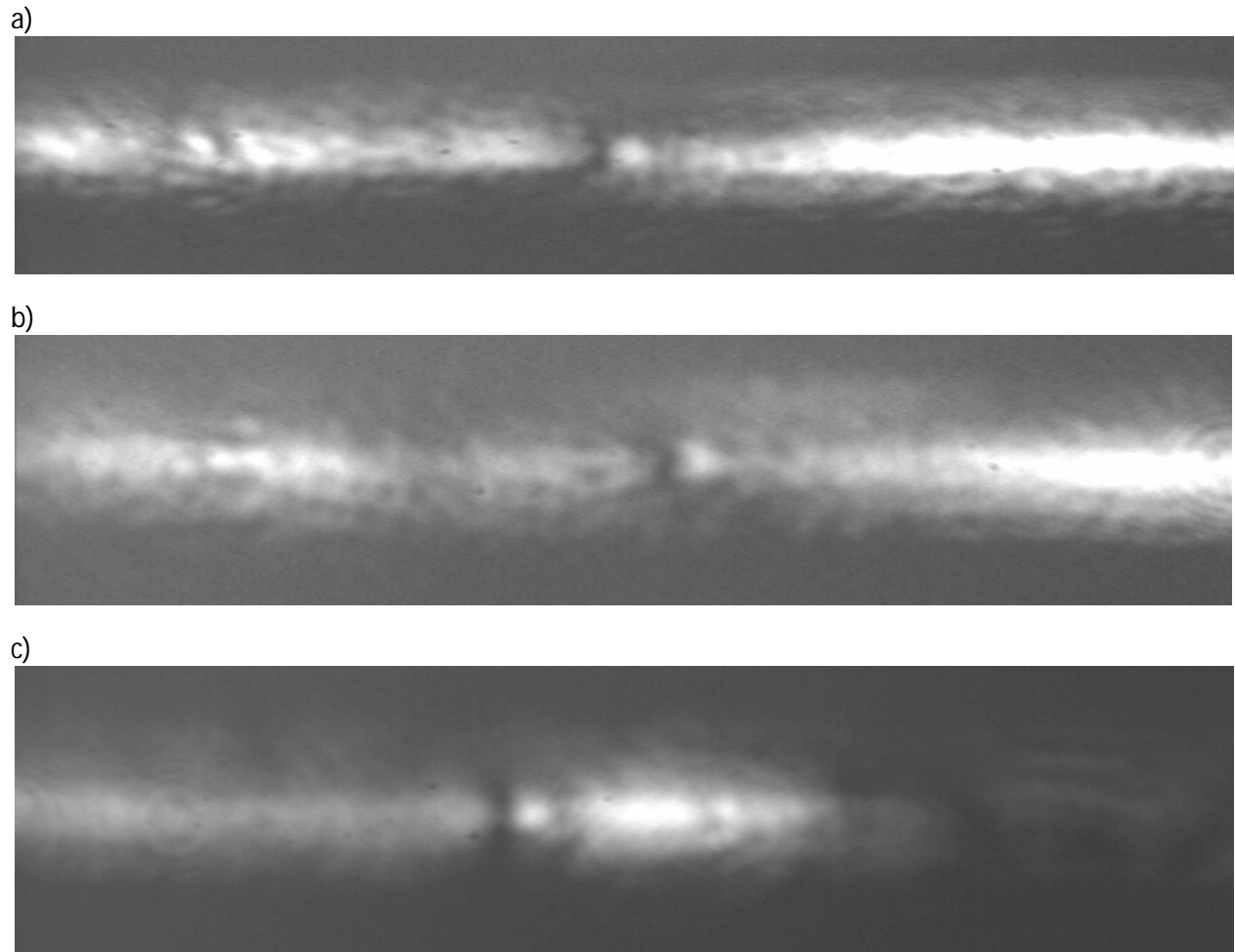
## 7.2 Measurements:

To characterize the fabricated devices, power cutback measurements were performed on varying lengths of straight embedded waveguides. A power cutback curve is a plot which allows us to determine the device MPA as well as the coupling loss for the two end facets. The lengths of dies used for cutback measurements were 3 mm, 3.8 mm, and 4.8 mm. Three different lengths are sufficient to construct cutback curves for MPA and power coupling losses. Although more lengths improve the accuracy of the cutback curve, here the limit is three lengths because of the particular dicing map adopted to produce dies from wafers. Power calibration for power coupling between the input and output fibres was first performed to record accurate mode power attenuation. This calibration was done by aligning the ends of input (PMF) and output fibre (SMF), and measuring the losses incurred during this coupling. This coupling loss between the fibres was then subtracted from the measured MPA, to determine the exact value of attenuation in embedded waveguides.

After the fibre coupling calibration, the die to be measured was placed between the fibres shown in *Figure 56* of optical characterization setup. The input fibre was aligned to a single straight waveguide by visually monitoring the mode output from the waveguide through a camera connected to a monitor. An optical lens was aligned at the output facet of the waveguide to focus the output mode on the camera lens placed some distance away from the main characterization setup. It was important to find the real output mode from the embedded waveguide because of significant guidance from the SiO<sub>2</sub> slab underneath the metal waveguide. It was possible to focus on the wrong area mistaken for a mode, which was actually a high intensity scattering area of light. The desired output mode should be very sharply focused with

very little radiation in surroundings, and easily lost even with slight movement of the input fibre.

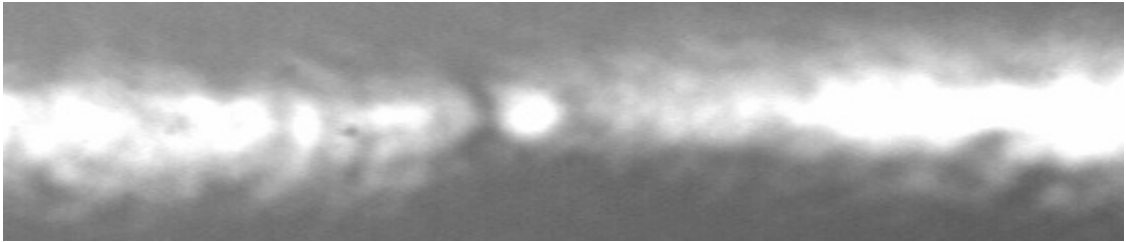
Initial optical characterization of the fabricated waveguides was done with no index-matching fluid at the interface of the fibre and waveguide at both the input and output end. The results showed a weak mode at the output of the waveguides due to a large power coupling loss at the input of the waveguide, with strong radiation. The mode outputs using this setup of optical measurements is shown in *Figure 57*.



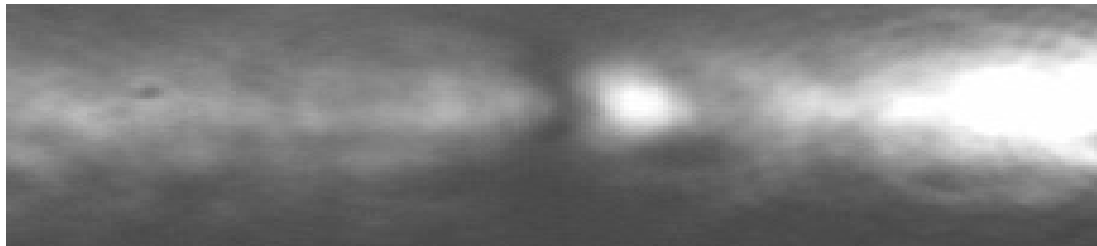
**Figure 57: LRSPP mode outputs from embedded waveguides without index-matched liquid at fibre-waveguide interface. a) 3mm die b) 3.8 mm die c) 4.8 mm die.**

An index-matched liquid with refractive index very close to that of the core of the fibres ( $n_{\text{core}} = 1.455$ ) was applied at input fibre-waveguide interface in the hopes of achieving better results in terms of mode output. This setup significantly enhanced the output results due to better coupling of light at the input of the waveguide, which is shown in *Figure 58*. Although there is still radiation around the mode, the intensity of the mode is much stronger, allowing for much better cut-back measurements. This also concludes that without the index-matching liquid, there is significant power coupling losses at the waveguide end-facets.

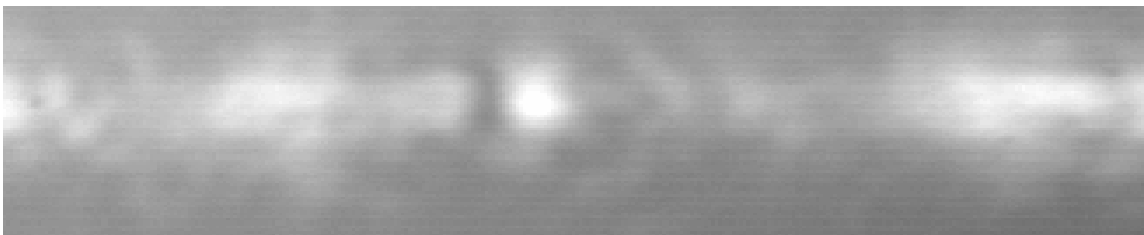
a)



b)



c)



**Figure 58: LRSPP mode output with index-matched liquid at the input fibre-waveguide interface. . a) 3mm die b) 3.8 mm die c) 4.8 mm die.**

Once the desired output mode is found on the display screen indicating the proper alignment of input fibre with the waveguide, the lens was replaced with the output fibre. The output fibre was visually brought close to the output facet through the microscope, and manipulated through micro-positioners with index-matched liquid placed between the output fibre and the waveguide-end facet. The power output from the SMF was observed on a power meter. The position of the output fibre was tuned by observing the corresponding power output. The precise alignment resulted in maximum power output reading on the power meter.

### **7.3 Power Cut-back measurement curves:**

The output power in decibels dBm was recorded and subtracted from the input power (in dBm) to determine the insertion loss of the waveguides. The input power from the PM fibre was measured to be ~ 3dB. The waveguide insertion loss was plotted against the length of the waveguide to construct the power cutback curve. *Figure 59* shows power cut-back curves of insertion losses with no index-matched liquid at fibre-waveguide interface, and *Figure 60* shows measurements with index-matched liquid at the fibre-waveguide interface. The slope of the curve represents the MPA and the y-intercept shows power loss at the facets (coupling loss). The curves were constructed from different sets of dies from the same wafers. The results are summarized in *Table 11* and compared to theoretical simulated values presented in *Appendix A*, calculated by Dr. Chengkun Chen.

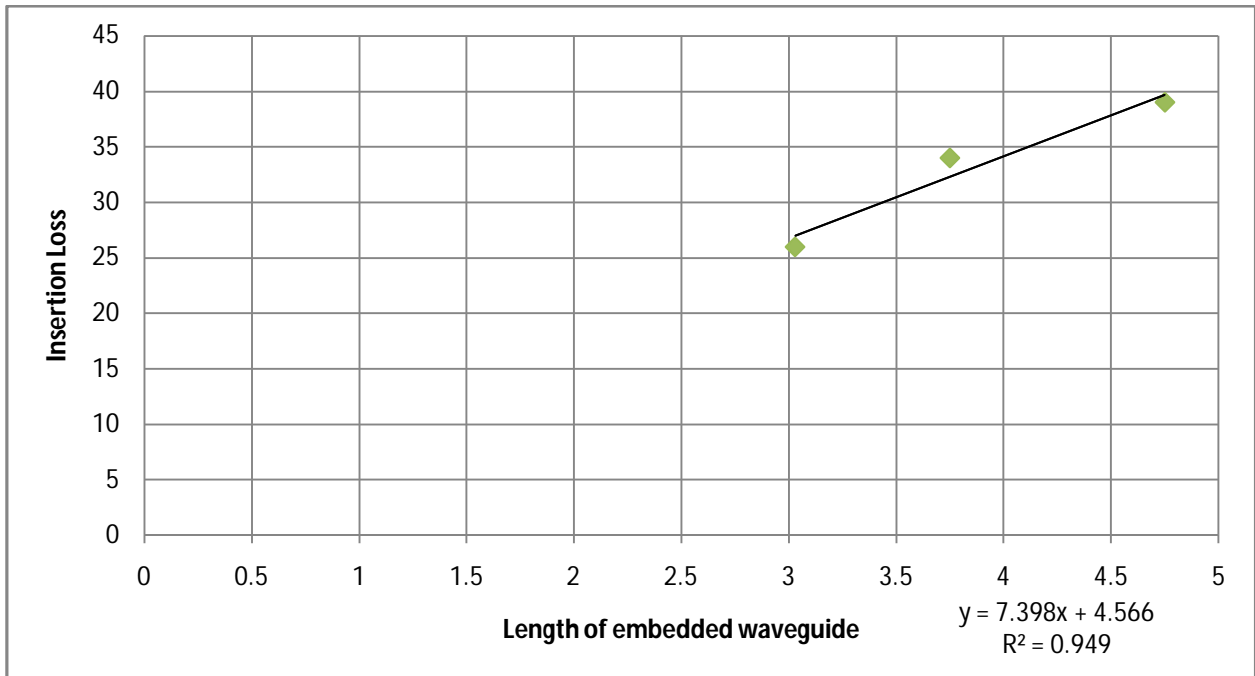


Figure 59: Power cut back curves without index-matched liquid at fibre-waveguide interface

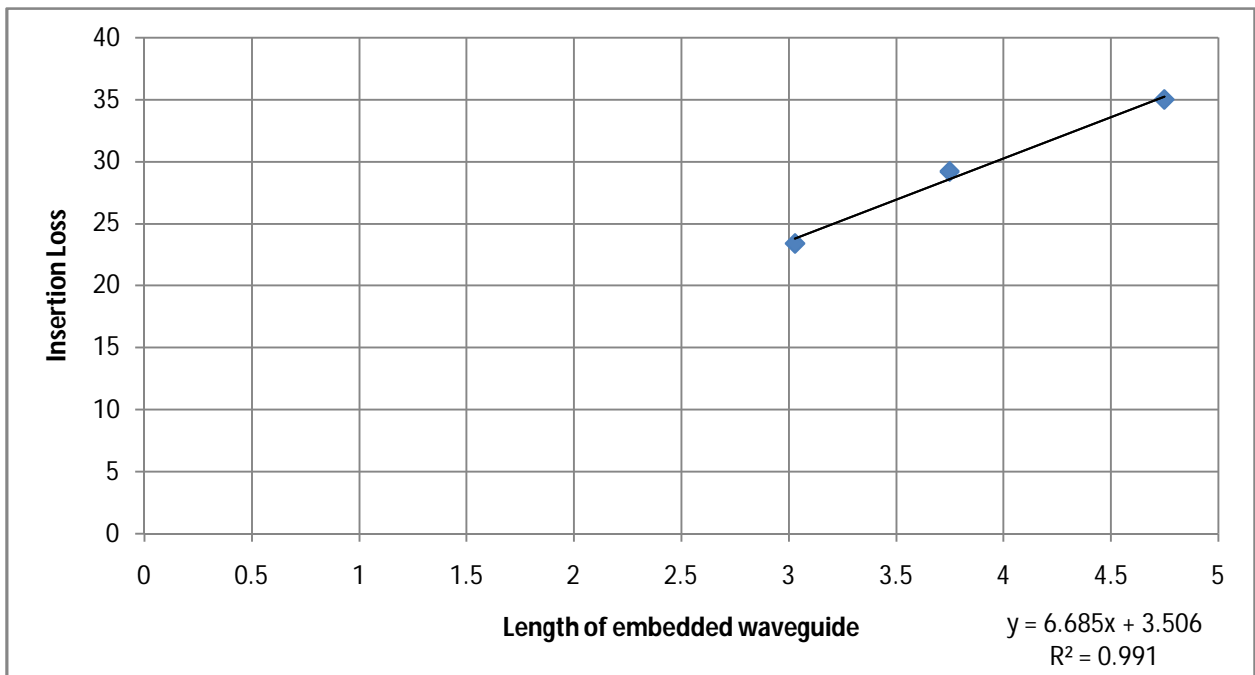


Figure 60: Power cut back curves with index-matched liquid at fibre-waveguide interface

	MPA (dB/mm)	Coupling loss per facet (dB)
<b>Embedded waveguide without index-matched liquid at fibre-waveguide interfaces</b>	7.4	2.3
<b>Embedded waveguide with index-matched liquid at fibre-waveguide interface</b>	6.7	1.75
<b>Theoretical values</b>	6	0.9

**Table 11: MPA and coupling losses of embedded waveguide.**

The value of MPA is relatively large for the embedded waveguide where index-matched liquid was not used at the input and output fibre-waveguide interface (*Figure 59*). This was expected as there was a significance amount of background radiation observed during visual alignment of the mode using a camera. The coupling loss per facet is also significantly high, possibly due to index mismatch at the interface. This results in significant power radiating within the slab, and scattered along the waveguide. The reliability of the results in this case is not very high.

The values achieved through applying index matching fluid at the fibre-waveguide interfaces at both input and output of the waveguide, show that the power coupling efficiency is greatly enhanced with this method (*Figure 60*). Therefore, coupling loss per facet through power cut-back measurements were achieved and a more reliable fit to a linear model is observed. The MPA measured (~ 6.7 dB/mm) with this method is still higher than the theoretical MPA (~ 6 dB/mm), but is slightly higher. Causes for this discrepancy are under investigation. Perhaps the metal or SiO<sub>2</sub> thicknesses are slightly off or the SiO<sub>2</sub> layer causes light scattering.

## 8 Conclusion and Future Work

The main purpose of this thesis was to successfully fabricate fully integrated LRSPP biosensors with excellent metal waveguide features in terms of dimensions and surface smoothness as well as implementing well-defined micro-fluidic flow channels. This thesis outlined each and every step in detail for realizing this goal. Gold stripe waveguide devices were fabricated in CYTOP claddings with a SiO<sub>2</sub> layer which acted as a solvent diffusion barrier and etch stop layer

The claddings were fabricated through spin-coating layers of CYTOP below and above the waveguide structures. Optical measurements were performed using Metricon to determine the optical index and thickness of the CYTOP claddings. The optical index of CYTOP was measured to be 1.3386 (@  $\lambda=1310$  nm). The thickness of bottom cladding was  $\sim 9$   $\mu\text{m}$ , and the thickness of top cladding was measured to be  $\sim 8$   $\mu\text{m}$ .

The SiO<sub>2</sub> layer was deposited through the e-beam evaporation method. The thicknesses of the SiO<sub>2</sub> layer and the metal (Cr+Au) stripes were selected according to simulation results obtained by a co-worker. After analyzing simulation results, it was determined that  $t_{\text{SiO}_2} = 30\text{nm}$  and  $t_{\text{metal}} = 30$  nm were very good choices in terms of MPA as well as fabrication feasibility. Deposition accuracy and thickness were measured using ellipsometry and AFM. The thickness of a SiO<sub>2</sub> layer deposited on top of the bottom cladding was measured to be  $\sim 30\text{nm}$ , which matched the target thickness.

The waveguide devices were realized through a bi-layer lithography process. Thermal restrictions were considered due to SiO<sub>2</sub> and CYTOP sensitivity towards higher temperatures.

The bi-layer procedure was developed and adjusted to achieve accurate dimensions. Gold was deposited using electron-beam evaporation. An adhesive chromium layer (~ 2nm) was deposited using e-beam evaporation to promote better adhesion between SiO<sub>2</sub> and gold. The target thickness of the waveguides was 30 nm, and the desired width was 5 µm. The metal waveguides were studied under AFM and microscope. The results showed that the target thicknesses and widths of the waveguides were achieved through successful lithography and e-beam evaporation.

After spin coating of the CYTOP upper cladding, the wafers were thoroughly inspected under the microscope for any waveguide damage or cracks in the structure due to solvent diffusion. It was determined that the SiO<sub>2</sub> successfully worked as a diffusion barrier avoiding any damage to the metal waveguides or 'rippling' in bottom CYTOP cladding. Once the waveguide devices have been embedded in CYTOP, a second level lithography was performed to pattern micro-fluidic channels. The channel structures were etched through O<sub>2</sub> plasma etching of top CYTOP claddings. The SiO<sub>2</sub> layer also acted as an etch-stop layer, and successfully stopped any over etching into the lower CYTOP claddings.

The fabricated wafers were diced into small dies for optical testing purposes. The characterization setup involved fibre optic excitation and detection through end-fire coupling. A power cutback curve was constructed for separate straight waveguides embedded in CYTOP with and without index-matching fluids at the fibre-waveguide interfaces. The mode power attenuation (MPA) was extracted from power cut-back curve fitting and was determined to be 7.4 dB/mm for samples where index-matching was not used between the fibre-waveguide

interfaces. Applying index-matched fluid between the fibre-waveguide interfaces provided better results in terms of both MPA ( $6.7\text{dB/mm}$ ) and coupling loss per facet ( $1.75\text{dB}$ ). This MPA agrees reasonably well with the theoretical value of  $\sim 6\text{ dB/mm}$ . The main reason attributed to higher attenuation could be discrepancies in the layer thicknesses as well as scattering of light in the  $\text{SiO}_2$  layer.

In conclusion, fully embedded LRSPP waveguide based biosensor devices were successfully fabricated, which improved upon several aspects of previous fabrication methods. The inclusion of a  $\text{SiO}_2$  layer on top of bottom CYTOP cladding enabled the fabricating metal waveguides of smooth surface and edges with accurate target thicknesses, which is the most important aspect of the LRSPP waveguide sensors. It also enabled us to create accurate micro-fluidic channels in the integrated biosensor by effectively stopping the  $\text{O}_2$  plasma etch to reach the bottom CYTOP cladding. On the other hand, the  $\text{SiO}_2$  layer had a significant impact on optical measurements. Radiation around the output LRSPP mode was observed possibly due to  $\text{SiO}_2$  layer acting as a slab waveguide and scattering input power into the claddings of the embedded waveguide. As a result the measured MPA was  $6.7\text{ dB / mm}$  compared to the theoretical value of  $6\text{ dB / mm}$ . The large coupling losses at the facets of the waveguides showed that there is a requirement for a better procedure to couple light into the waveguide. Perhaps, PMF fibres with smaller core, close to the width of the metal waveguide ( $\sim 5\text{ }\mu\text{m}$ ) could be utilized to couple light into the waveguide.

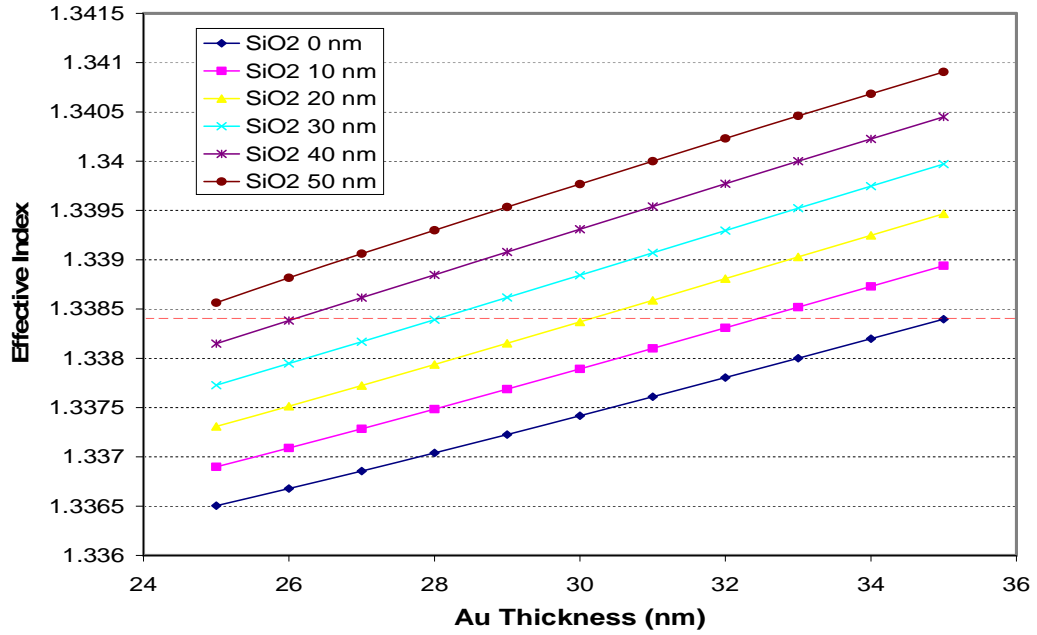
Future improvements may attempt using a lift-off resist (LOR) that allows for bakes at a lower temperature ( $< 105^\circ\text{C}$ ), and low etch-rate in MF321 to achieve better lithography results.

Furthermore, the implementation of a better source for SiO<sub>2</sub>, which does not scatter a lot of light in the waveguide, could also be possible. Work under way right now to improve the overall packaging of the biosensor includes implementing a glass wafer with drilled holes (~diameter equal to the etched holes in micro-fluidic-channels) to transport fluids into the sensor more efficiently. Adhesion is also a key in improving the performance of the biosensor. Better adhesion at every new layer is critical in order to achieve stable structures. Chemical agents or plasma techniques could be explored for this goal.

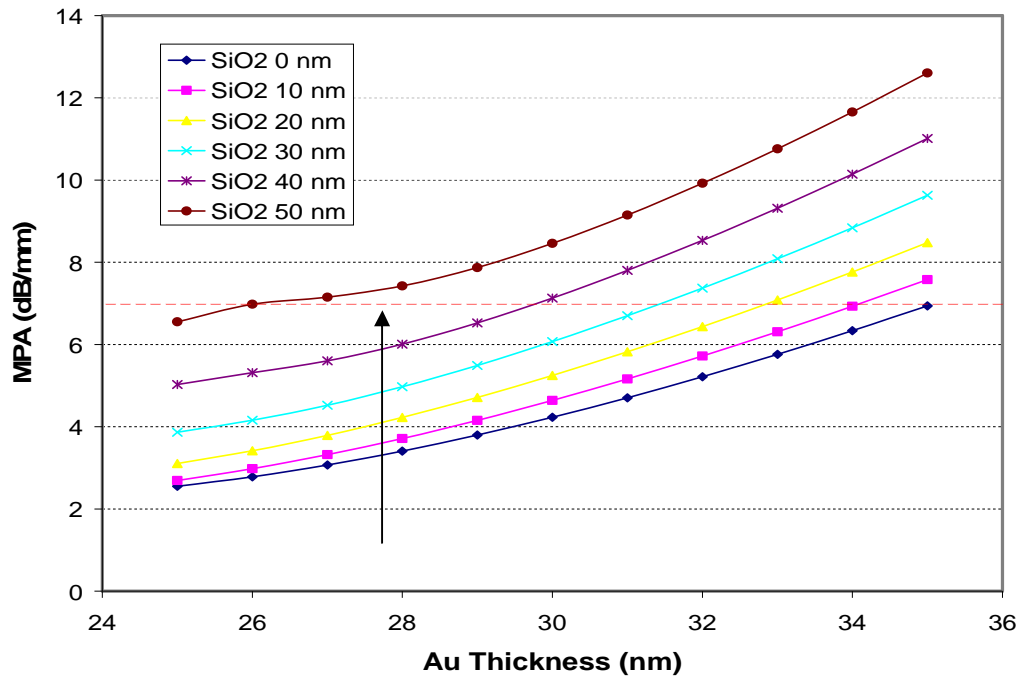
# 9 Appendix A: Modeling of straight and curved LRSP waveguides by Chengkun

Chen.

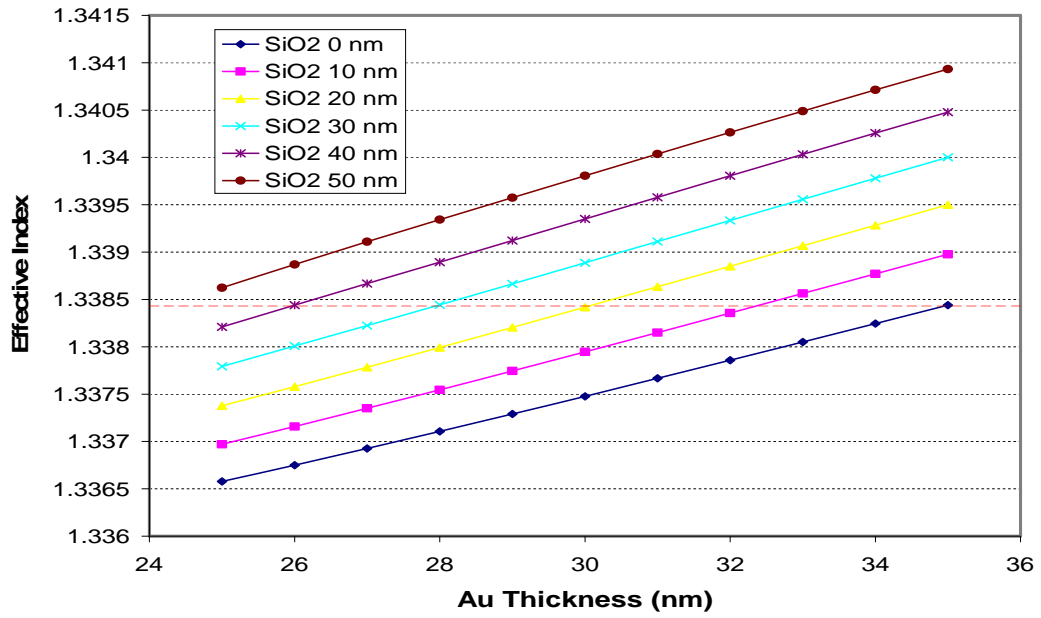
a)



b)



c)



d)

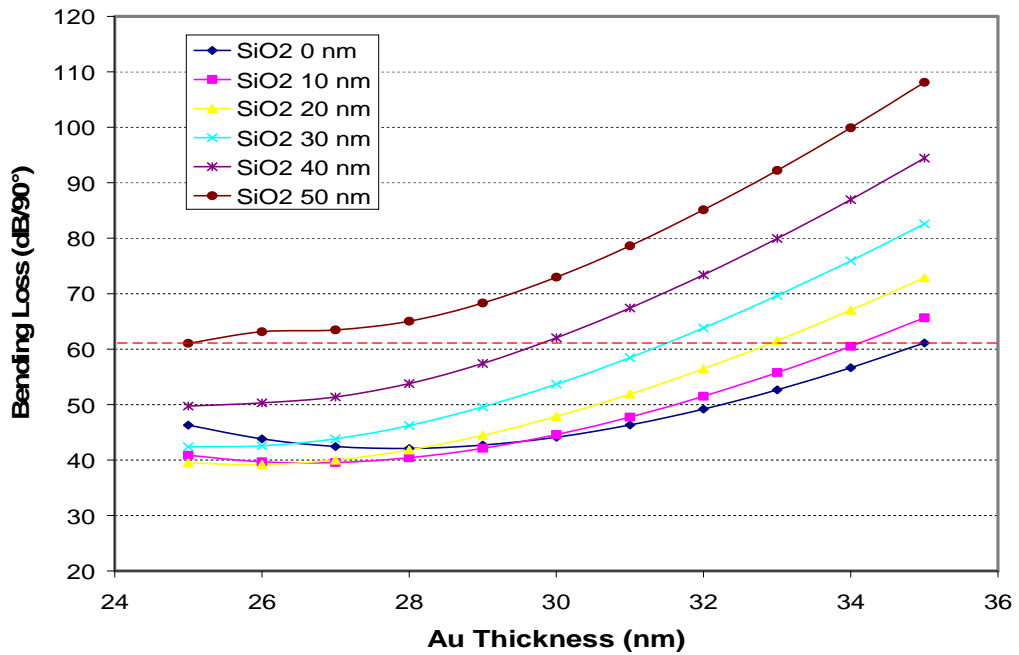
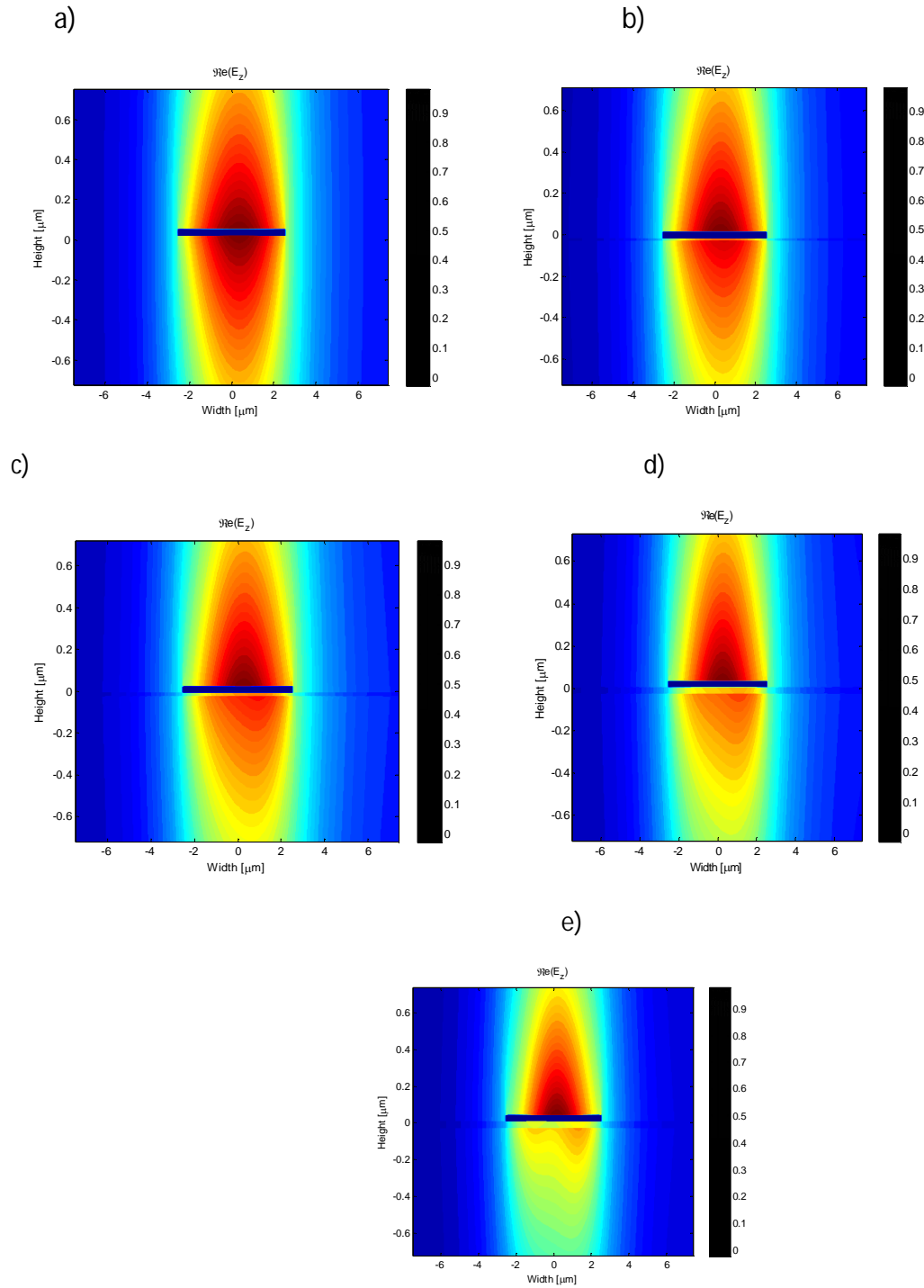
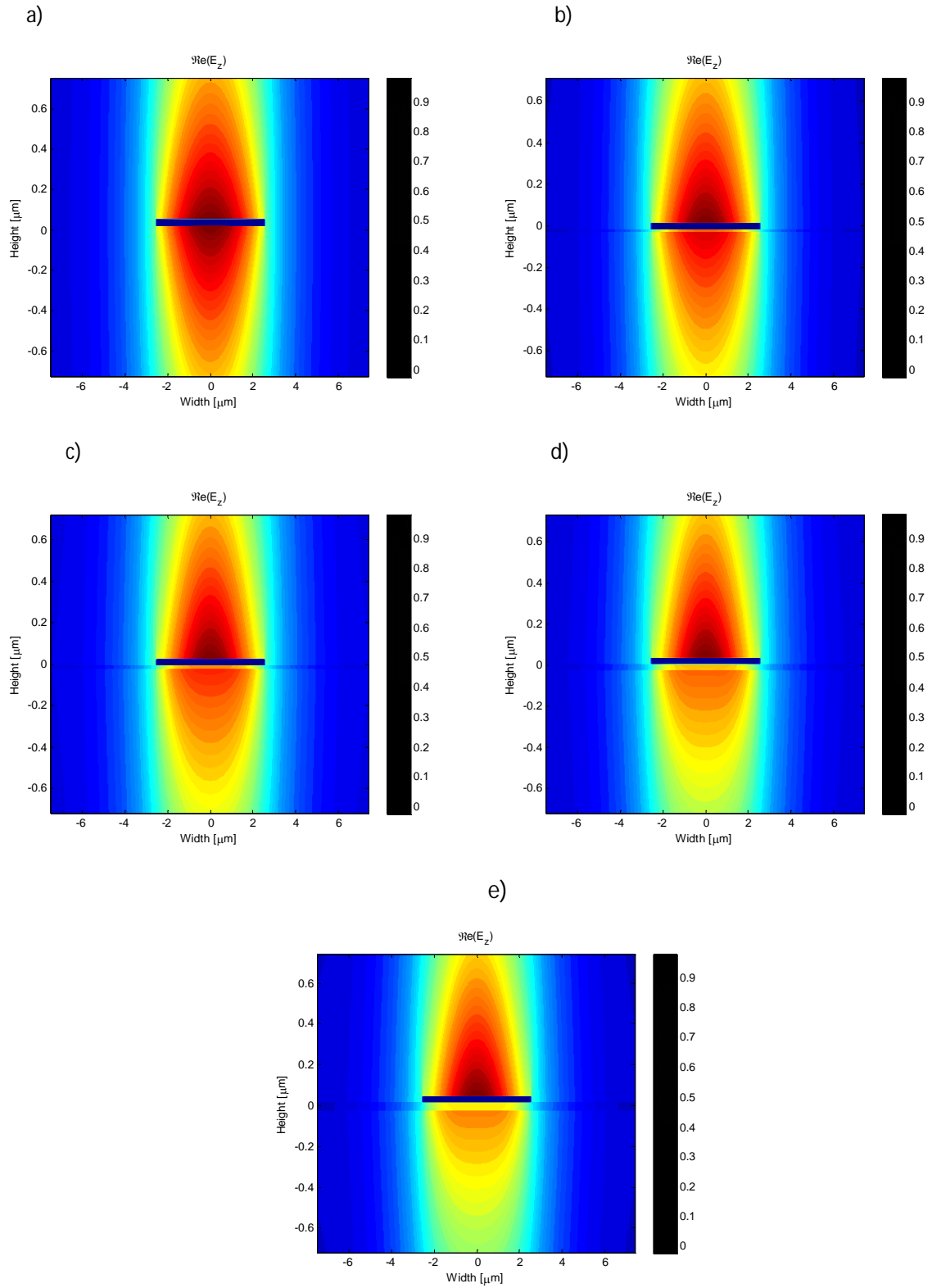


Figure 61: (a) and (b) straight waveguide, and (c) and (d) bended waveguide with  $r_0=5.5$  mm.



**Figure 62: Field plots of bent waveguides with different oxide and metal thicknesses a)  $t_{\text{SiO}_2} = 0 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$  b)  $t_{\text{SiO}_2} = 10 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$  c)  $t_{\text{SiO}_2} = 20 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$  d)  $t_{\text{SiO}_2} = 30 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$  e)  $t_{\text{SiO}_2} = 40 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$**



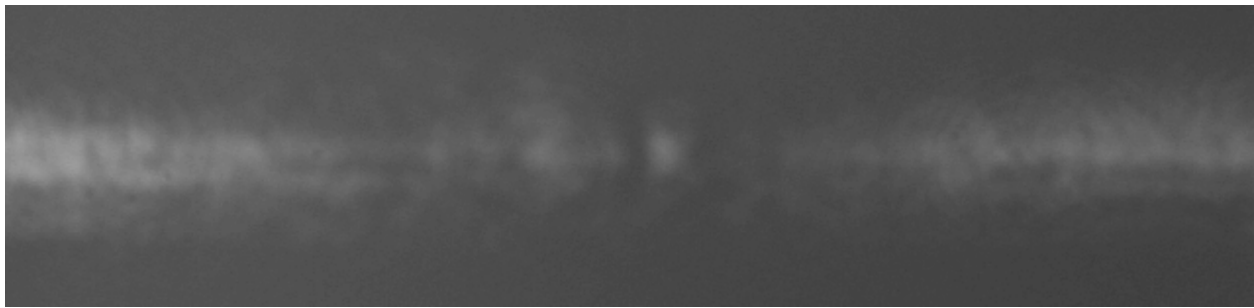
**Fig. 63 : Field plots of straight waveguides with different oxide and metal thicknesses a)  $t_{\text{SiO}_2} = 0 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$  b)  $t_{\text{SiO}_2} = 10 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$  c)  $t_{\text{SiO}_2} = 20 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$  d)  $t_{\text{SiO}_2} = 30 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$  e)  $t_{\text{SiO}_2} = 40 \text{ nm}$ ,  $t_{\text{metal}} = 30 \text{ nm}$**

## 10 Appendix B: LRSPP modes using Tapered Fibre

a)



b)



c)

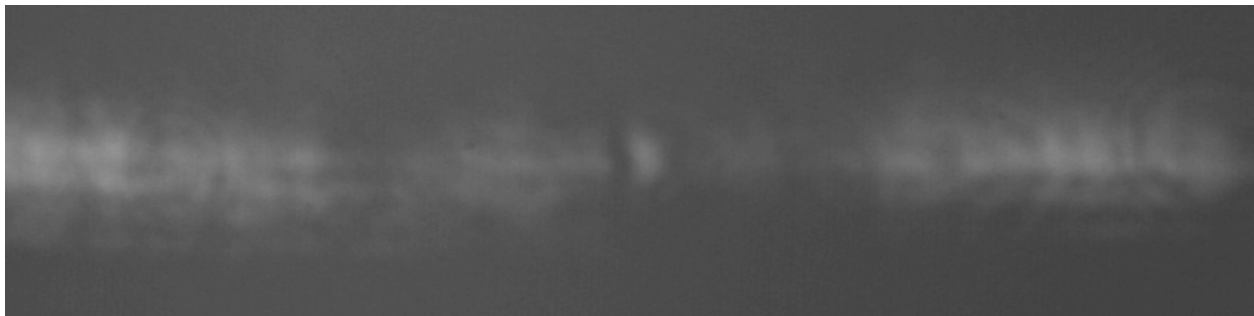


Figure 64: LRSPP mode profiles at output end of straight single waveguides for a)3 mm die b)3.8 mm die c)4.8 mm die.

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