Design of Broadband GaN 0.15μm RF Switches and X-band Reconfigurable Impedance Tuner

by

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Abstract

Radio-frequency (RF) switches are widely used in electrical systems, telecommunications, and wireless applications. In RF systems, it is often desirable to change the signal path effectively, by using couplers, duplexers, and RF switches for signal division and combining. Typically, in modern RF systems, the RF switch is mostly capitalized in order to reduce the RF footprint but with efficient switch characteristics. A simple method to reduce transceiver space requirement is to integrate RF switches with the frontend module on a single chip.

Recent advances in Gallium Nitride (GaN) technology allows RF designers to design faster, smaller, and efficient components using this technology. With high data rates in demand for wireless communication systems, wideband characteristics are needed in modern systems [1]. Therefore, it is desirable to design wideband circuits; such as, mixers, amplifiers, and switches. In this work, a comprehensive study of NRC GaN150 HEMT is conducted to design broadband RF switches. Single pole and double pole switch topologies operating at 1-12 GHz are designed to evaluate GaN 0.15μm RF switches. The main objectives were to design compact sized switches, while having high power handling, low insertion loss, high isolation and high return loss. Additionally, a transmit-receive switch is designed for integration into a frontend module and further fabricated to operate at 10 GHz.

There are many applications of RF switches in an RF transceiver, one of which is an impedance tuner. Impedance tuner are attractive for many applications where mobile devices are used for wireless communications. As mobile technology continues to evolve, they are designed to be compact, leaving minimal space for the antenna. Consequently, the radiating element is often electrically small and sensitive to near-field coupling requiring tuning. Matching networks aim to tune matching conditions; for example, loading effects due to human hand [2]. For such situations, specialized matching networks can be designed to account for specific loading environmental effects. However, for mobile systems, the environment is unknown; thereby, yielding unpredictable antenna loading, especially for electrically small antennas that have rapidly changing real and imaginary impedance. As a result, it is necessary to design a reconfigurable impedance-matching network to account for possible load impedances. In this work, a 16-bit reconfigurable impedance tuner design comprising of passive microwave components and NRC GaN 0.15μm FET operating at X-band is presented to evaluate its performance for integration with the frontend module on a single chip to reduce cost and increase efficiency of the system.

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Acronyms and Abbreviations

CRC	Communications Research Center Canada
CMOS	Complementary Metal-Oxide-Semiconductor
DP4T	Double-Pole Four Throw
DPDT	Double-Pole Double-Throw
DPST	Double-Pole Single-Throw
EVM	Error Vector Magnitude
ESR	Equivalent Series Resistance
FEM	Frontend Module
GaAs	GaAs
GSG	Ground-Signal-Ground
IM3	Third order intermodulation
LNA	Low Noise Amplifier
MEMS	Microelectromechanical systems
MESFET	Metal Semiconductor Field Effect Transistor
MIC	Microwave Integrated Circuits
MIM	Metal-insulator-metal
MIMO	Multiple Input Multiple Output
mmWave	Millimeter Wave
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
OTOI	Output Third Order Intercept Point
PA	Power Amplifier
PAE	Power Added Efficiency
Q Factor	Quality Factor
SNR	Signal-to-Noise Ratio
SP4T	Single Pole Four Throw
SPDT	Single-Pole Double-Throw
SPST	Single-Pole Single-Throw
T/R	Transmit-Receive
TDD	Time Division Duplexing

List of Variables

C	Channel Capacity
C_{ds}	Drain to Source Capacitance
C_G	Gate Capacitance
C_{load}	Load Capacitance
C_{OFF}	OFF State Capacitance
E_c	Critical Electric Field
ESR	Equivalent Series Resistance
ε_r	Dielectric Constant
f_0	Resonant Frequency
F_{min}	Minimum Noise Factor
I_D	Drain Current
I_F	Intermediate Frequency
IIP_3	Input Third Order Intercept Point
L_{ON}	ON Inductance
NF	Noise figure
OIP_3	Output Third Order Intercept Point
P_{in}	Power received by the load
$P_{incident}$	Incident Power
P_L	Power delivered to the load line in OFF State
P_0	Power delivered to the load line in ON state
P_{out}	Power Transmitted to the load
$P_{reflected}$	Reflected Power
Q_C	Quality Factor of Capacitor
Q_L	Quality Factor of Inductor
Q_U	Unloaded-Q
$R_{circuit}$	Circuit Resistance
r_{ds}	Drain to Source Resistance
R_{in}	Input Resistance
R_L	Load Resistance
R_{ON}	ON State Resistance
R_P	Equivalent Parallel Resistance
R_S	Source Resistance
SNR_i	SNR In
SNR_o	SNR out
T_f	Fall Time
T_r	Rise Time
V_{BR}	Breakdown Voltage
V_D	Drain Voltage
$V_{incident}$	Voltage Wave, Incident

V_{PO}	Pinch-Off Voltage
VSWR	Voltage Standing Wave Ratio
$V_{transmitted}$	Voltage Wave, Transmitted
X	Reactance
Z_0	Characteristic Impedance
Γ_{opt}	Optimum Reflection Coefficient
Γ_s	Source Reflection Coefficient
ϵ_s	Dielectric Constant
μ_n	Mobility
ω_0	Angular Frequency

1

Introduction

For applications, such as, defense, radar, and communications, existing technologies such as GaAs and Laterally Diffused MOSFET (LDMOS) simply cannot keep pace with the evolving demands for size, reliability, linearity, power density and energy efficiency. GaN-based discrete transistors, amplifiers, and switches are rising to the challenge, providing RF system designers with the flexibility to achieve significantly higher power and efficiency, with lower part count, allocated space, and cost [3] [4]. A wide bandgap technology, such as, GaN have sufficiently matured in the last few years that is being used extensively in switching, control, and low noise applications [5]. As the technology develops, it is transitioning from government-funded technology to a high volume commercial mainstay [3].

In the next decade, a mobile traffic increase of 1000x has been projected compared to its current volume. To meet this estimated traffic growth, next-generation mobile networks are expected to achieve a 1,000-fold capacity increase to the current generation of wireless network deployments [6]. As a result, the next generation of wireless communication is being discussed, evaluated, and experimentally implemented to meet such demands [6].

This chapter presents the economic and technological motivations behind the drive for integrated GaN switches and reconfigurable impedance tuners for applications in current and future wireless communication systems. The chapter begins with an overview of the trends in wireless communications and technology. The role of RF switch is discussed with examples where the impact of on-chip switch designs is discussed. Finally, the last section outlines the organization of this thesis.

1.1 Background

Radiofrequency spectrum is part of the electromagnetic spectrum over which radio communication takes place. Different parts of the radio spectrum are allocated for various strictly regulated radio technologies and applications. The demand for these telecommunication spectrums is increasing at an unprecedented rate to meet the requirement of growing wireless applications. A number of major Canadian research labs such as Communications Research Center Canada (CRC) stated that their Research and Development (R&D) program would focus on methods, techniques and technologies that can maximize the use of the RF spectrum. This enables development of various wireless services (e.g.: 4G, 5G, and other radios) as well as advanced applications (e.g.: intelligent transportation, energy management and public safety) that require spectrum [7]. Figure 1-1 displays an overall growth in the number of mobile devices and connection projection [8].

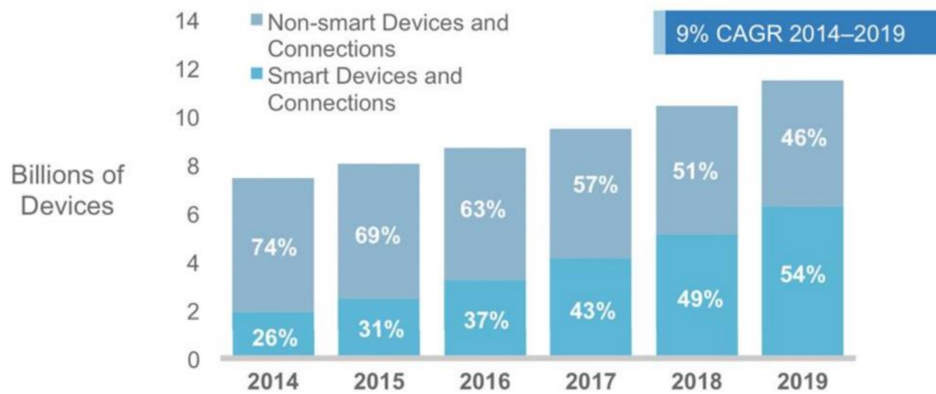


Figure 1-1: Global Growth of Smart Mobile Devices and Connections

To accommodate such staggering number of always-on data-centric wireless devices, there is a need to investigate the next generation of wireless technology in a newly available spectrum. As most of the current frequency bands below 3GHz are occupied, the attention towards acquiring a new spectrum for the next generation of wireless communications has shifted to frequency bands above 3GHz and up to the millimeter wave (mmWave) [6]. Table 1-1, summarizes the frequency bands expected to be assigned for wireless communications systems.

Due to the governance of spectrum allocation by regional wireless regulatory bodies, the potential new licensed spectrum in each region is estimated to lie within the range of 3 to 10 GHz [6]. As a result, S-band (2 to 4 GHz), C-band (4 to 8 GHz), and X-band (8 to 12 GHz) frequencies are possible spectrum landing spots for the next generation of wireless communication systems.

Table 1-1: Potential allocation of spectrum and associated bandwidth for future wireless technologies [6].

Frequency	Bandwidth	Notes
Below 6 GHz	0.6-2.5 GHz	Mainly at 3.5 GHz
28 GHz	1 GHz	
39 GHz	1.5 GHz	
45 GHz	9 GHz	Both licensed and unlicensed; under planning in China
60 GHz	Up to ~7 GHz	
Total new spectrum	3-10 GHz	Considers the regional availability of new spectrum

1.2 RF Switches

The architecture of a heterodyne RF transceiver front-end (FEM), in Figure 1-2 illustrates how the received RF signals are passed through a band-pass filter, and switched to a low-noise-amplifier (LNA) [9]. The gain of the LNA essentially sets the signal-to-noise (SNR) ratio for the entire receiver [10]. This amplified signal is first filtered for improved image-rejection and down-converted to an intermediate frequency (IF) with a mixer. This is subsequently filtered for channel selection and shifted to a baseband frequency by a second mixer.

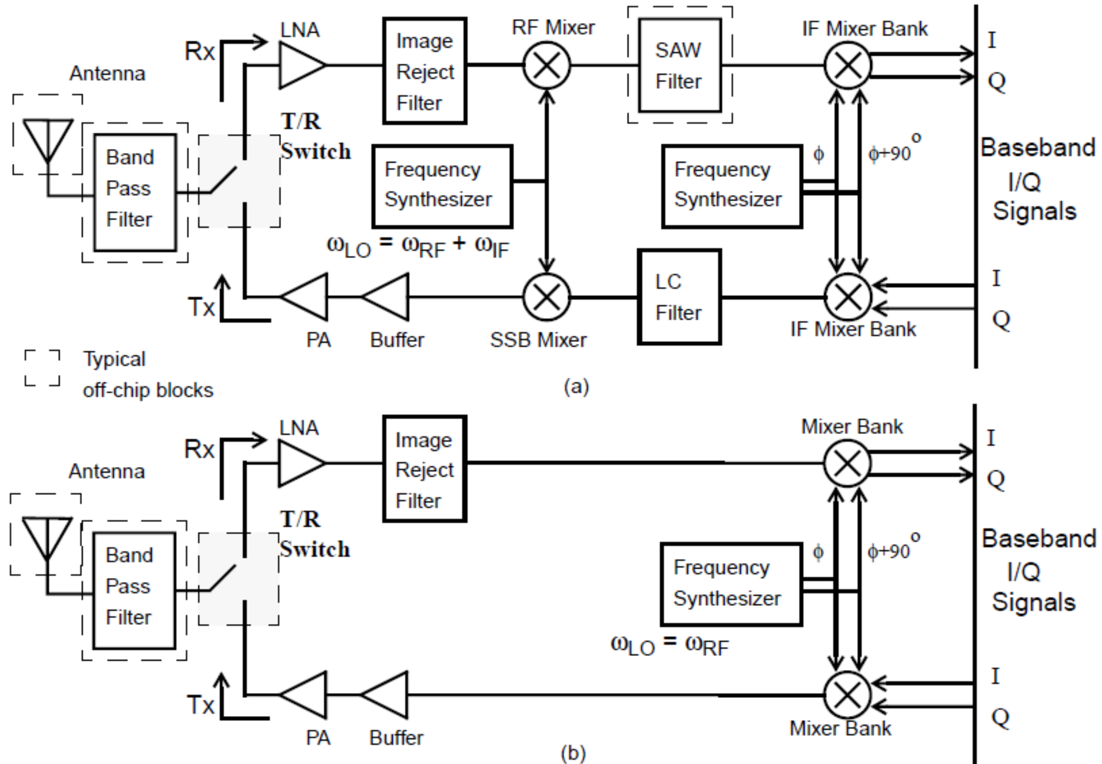


Figure 1-2: RF transceiver architectures (a) Heterodyne and (b) Direct down-conversion.

A transmitter is complementary of the receiver chain where the signal at baseband are up-converted to the RF carrier using an IF stage, where a power amplifier (PA) is used to drive the antenna. A transmit-receiver (T/R) switch is used to alternate between the receiver and transmitter chain, which is then connected to the antenna.

The direct down-conversion architecture mixes the incoming RF signals with carrier frequency directly to the baseband. Similarly, on the transmitter side, the signals are directly up converted to the RF carrier using one mixing stage during transmission. Three aspects of direct conversion with respect to heterodyne architecture validates the utilization of the direct down-conversion architecture. Namely, these aspects are (1) the absence of an image that greatly simplifies the IC design, (2) channel selection performed by a low-pass filter, which can be, realized on-chip with active circuit topologies having stringent cutoff characteristics, and (3) mixing spurs that are considerably reduced enabling simpler handling capabilities. Due to the low cost and simplicity of the design, the industry is increasingly looking at direct down-conversion architecture to facilitate further integration by reducing the component requirements [9]. However, there are some disadvantages to using direct-down conversion architecture; such as, signal leakage paths that can occur in the receiver, local-oscillator energy that can leak through the mixer state to the antenna input and reflect back into the mixer. There is also some design modification that needs to be incorporated into the architecture while designing a direct-down conversion transceiver.

To date, there are many transceiver designs, which include LNA and PA on the same die, yet not many include an integrated switch. In cases where the switch is on-chip, a number of them are designed in such a way where a switch matrix cannot be formed for a larger system to accommodate multiple frequency bands in a compact module as expected from today's mobile communication systems [9]. The RF FEM switches are found in several places in the radio architecture. In a T/R switch, a signal-pole double throw (SPDT) arrangement of switch multiplexes the access to the antenna between the PA and LNA. SPDT used as T/R switches must have a high linearity to ensure that high power signals at the output of the PA are transmitted to the antenna with minimal distortion. The specific criteria of such linearity requirements presents a serious challenge in integrating T/R switches into on-chip, which can be improved and simplified using GaN technology [11]. This is because GaN as a technology is known to have a highly linear substrate that incorporates T/R switches on-chip while maintaining the high linearity requirements [12].

1.3 Impedance Tuner

As mentioned in the previous section, there are many applications of RF switches. It can be used to create the building blocks of many RF components either as control or as a reconfiguring mechanism. As shown in Figure 1-2, components; such as, PA, LNA, switches, filters, mixers, and the RF processing chain of the radio are also included in the FEM. When testing in isolation or in simulations, these components display the desired results. However, when testing is conducted in the real world, where the FEM modules are closely linked with the device and environmental effects are constantly changing, the specifications of these components can be inaccurate.

RF devices are typically designed to have an impedance of 50 Ω to match many common transmitter antenna types. The use of 50 Ω is due to a traditionally coax cable with an arithmetic mean between 30 Ω that gives the best power handling capability, and 77 Ω which has the lowest loss that gives 53.5 of arithmetic mean with a geometric mean of 48 Ω. Hence, the choice of 50 Ω is a compromise between power handling capability and signal loss per unit length for air dielectric [13].

The impedance of the transceiver and transmission lines should be matched to that of antenna across all frequency bands. However, this rarely occurs because of the antenna design, bandwidth limitations, and environmental factors. One solution to reduce reflections is to incorporate matching between the load and source. By tuning this matching network, it is possible to make the load impedance close to that of source impedance. When used in the context of antennas, impedance tuners are capable of dynamically adjusting the impedance, which is referred to antenna tuning. By integrating matching condition between the antenna and transceiver, it is possible to have an efficient system where PA is able to provide maximum power to drive the antenna and reduce noise in the receiver chain, thus greatly improving the overall signal to noise ratio of the receiver.

1.4 Literature Review

GaN Switches achieve high power handling in a small form factor, particularly versus insertion loss. When designing RF switches, all parameters must be considered simultaneously as they set the topology and circuit architecture of the switch.

Jim [14] argues that figure of merit comparisons are useful within a technology that consists of 0.25μm and 0.15μm GaAs pHEMT to demonstrate which process variant has the lowest on resistance and off capacitance. He further states that GaAs and GaN displays very similar figure of merit values

indicating the ability of GaN switches to achieve small signal performance levels similar to GaAs solutions. Jim states that series switch power handling can be approximated by a simple power relationship between the series FET cell's maximum current value and system impedance. Typically GaAs FET have maximum current handing capabilities of 500-600 mA/mm while GaN FET technology has the capability to be above 1 A/mm giving it a significant advantage when it comes to power handling for a series switch configuration [14]. Extensive review of GaN substrate is carried in section 2.3.6.

Mark et al. [15] designed single pole four throw (SP4T) using series-shunt switch topology using Nitronex NRF1 power HFET process. On average, they have measured -0.95 dB and -1.5 dB insertion loss at 1 GHz and 2 GHz, respectively, while realizing an isolation higher than 28 dB up to 2.5 GHz. For 1 GHz, the measured 1 dB compression point of 45 dBm was achieved at the control voltage of 28 V. GaN HFET had a length of 0.7μm and a width of 1 mm. Various switch configuration is discussed and compared in section 3.3.

Hidetoshi et al. [16] designed a high power RF switch IC using GaN HFETs. They have used series-shunt configuration for both arms to design a single stage single-pole double throw switch. He indicates, as gate width of the FET increases the insertion loss improves but isolation degrades for series switch. Subsequently in the shunt FET, as gate width is increased, insertion loss degrades and isolation improves slightly [16].

1.5 GaN Technologies

A typical power device used in RF and microwave systems can be classified into two categories: power rectifiers and power switches. Silicon has long been the dominant semiconductor of choice for high voltage power switching devices; however, silicon power devices are approaching the theoretical limits of performance.

There has been a concerted effort to reduce the ON-resistance by increasing the device die area in order to minimize the power losses in a silicon Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET). However, in high-frequency applications, as the die size increases, the increase in the input capacitance produces a corresponding increase in the switching losses. As a result, it becomes necessary to reduce the specific ON-resistance per millimeter in order to keep the die size small for small input capacitance.

Wide bandgap semiconductors; such as, Silicon Carbide (SiC) and GaN, are becoming attractive because they offer several potential advantages over silicon devices in the areas of switching (faster with lower losses), operating temperature and blocking voltage. Their unique material properties; such as, wide bandgap, high electric breakdown field, and high saturated electron velocity enables their tremendous potential [12].

There has been a significant progress in growth and process technology for SiC and GaN. GaN High-electron-mobility transistors (HEMTs) are close to high volume commercialization, which can be incorporated in various applications, especially RF switches. This is because GaN HEMTs have high power handling capabilities, higher breakdown voltages, high linearity, and low ON-resistance and OFF-capacitances.

1.6 Thesis Contributions

This work contributes to the field of RF switch theory, design, and implementation. The key objective of this work is to investigate techniques to design RF switches using a novel GaN 0.15μm HEMT technology and evaluate its application. To the author's best knowledge, this work would be the first to evaluate GaN 0.15μm HEMT technology for the design of RF switches and tuners. For this purpose, the RF components designed are as follows:

- Broadband Single-Pole Single-Throw Switch (SPST),
- Single-Pole Double-Throw Switch (SPDT),
- Double pole switch topology to operate as Double-Pole Single-Throw (DPST) and Double-Pole Double Throw Switch (DPDT),
- π-network reconfigurable X Band impedance tuner and,
- Integrated T/R switch for 10 GHz FEM

The complete FEM module using the NRC GaN 0.15μm process was fabricated by CMC Microsystems.

1.7 Thesis Overview

Chapter 2 describes general properties of RF switches. In this chapter, various switch topologies are discussed and general performance and integration characteristics are presented. A comparative study will be discussed between different types of technologies.

Chapter 3 discusses RF switch design using NRC GaN 0.15μm. FET and component modelling of capacitors and inductors will be carried out to establish optimal operating points and topologies for different applications. The parameters most relevant for RF switch design are subsequently demonstrated. The design and results of different switch designs will then be reported.

Chapter 4 discusses the relevant parameters required for tuner designs. Studies of different types of matching network are presented. Design and simulation results of the impedance tuner are also discussed.

Chapter 5 discusses the FEM module and integrated 10 GHz T/R switch designs. Design details and simulations are presented and summarized. Finally, Chapter 6 summarizes the contributions of this dissertation and outlines the scope of future work.

2

RF Switch

RF switches are an integral component of modern communication systems. There are various switch topologies, design techniques, and parameters to consider while designing an RF switch. This chapter presents fundamental RF switch topologies and then discusses design considerations for RF switches. Lastly, a comparative analysis is carried out for various RF switch technologies.

2.1 Switch Topologies

For switches, the term 'poles' is used to describe the number of nodes where a signal will converge while 'throws' are the possible connection of nodes. An RF switch can be classified into four main topologies: Single-Pole Single-Throw (SPST), Single-Pole Double-Throw (SPDT), Double-Pole Single-Throw (DPST), and Double-Pole Double-Throw (DPDT). This section will present these fundamental switch topologies.

2.1.1 Single-Pole Single-Throw Switch

The SPST switch plays an important role in the number of advance communication and radar systems [17]. SPST can be used as an individual component or as an integral element in subsystems or system. Figure 2-1 displays a basic structure of an SPST switch.

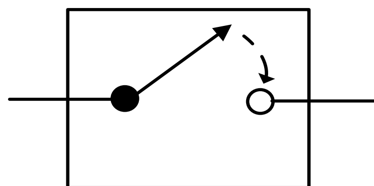


Figure 2-1: SPST RF Switch

It can be used for high data rate short-range communication as well as in high-resolution radar systems. The SPST switches can be used for the transmitter with a fast switching time and high isolation with low insertion loss. SPST can be designed to have high isolation, which is crucial in order to reduce or prevent RF leakage since it not only degrades other coexisting systems but also reduces the dynamic range [18] [19] [20].

2.1.2 Single-Pole Double-Throw Switch

The single-pole double-throw (SPDT) switch is the fundamental switch where there is one input or output node switching between two chains. In wireless communication systems; such as, time division duplexing (TDD), T/R switch plays an important role to direct the RF signal flow either to a transmitter or a receiver [21] [22]. Figure 2-2 displays a basic structure of an SPDT switch.

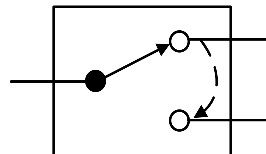


Figure 2-2: SPDT RF Switch

An SPDT can be designed to integrate within a transceiver to eliminate the need for external switches, thus reducing the component count.

2.1.3 Double-Pole Single-Throw Switch

A double-pole single-throw (DPST) switch has four terminals as shown in Figure 2-3. Two for input and two for output signals. The switch operates to create a single RF path out of two possible chains. In DPST, only one pole can be connected to the output terminal at a given point.

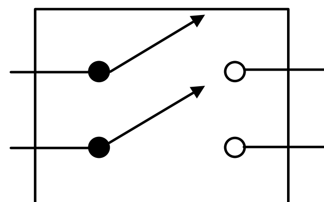


Figure 2-3: Double-Pole Single-Throw RF Switch

2.1.4 Double-Pole Double-Throw Switch

For a single transceiver, the SPDT is the fundamental switch that links between the antenna port and the analog FEM component at operating frequency. In the most advanced wireless communica-

tion systems, the demand for $n \times m$ switch matrices is increasing rapidly, and can be used with diversity antennas [23]. The basic structure of a DPDT switch is illustrated in Figure 2-4.

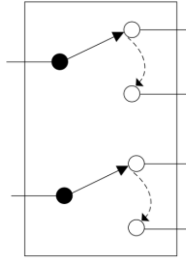


Figure 2-4: Double-Pole Double-Throw RF Switch

In a large system, a switching matrix has the disadvantage related to the need for a greater number of switching devices and complicated control logic to operate them. Typically, DPDT switches are developed for dual antenna and dual ports, one for each chain in the transceiver. However, if a system is required to operate as a Multiple Input Multiple Output (MIMO) system, a double-pole four-throw (DP4T) switch is required.

The fundamental switches presented in this section can be used in a larger switch matrix to form multi-pole and multi-throw switches. The following section will discuss the design considerations of RF switches.

2.2 Design Considerations

Many parameters are considered simultaneously when designing an RF switch. This section will present key design considerations; such as, insertion loss, return loss, isolation, power handling, linearity, switching speed, and noise. This section will introduce the mentioned parameters and provide ways to quantify them.

2.2.1 Insertion Loss

Insertion loss plays a key role in a transceiver, particularly in receiver applications, where the effective sensitivity and dynamic range of the system is lowered by insertion loss [23]. Insertion loss can be expressed in many different ways; it is common to use S-parameters to describe the properties of a two-port schema as shown in Figure 2-5.

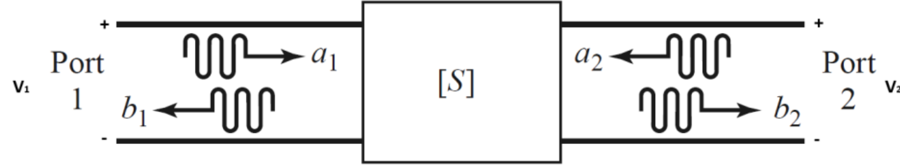


Figure 2-5: S-parameters representation of a 2-port network [24]

The S-parameters are defined by

$$b_1 = s_{11}a_1 + s_{12}a_2 \quad (2.1)$$

$$b_2 = s_{21}a_1 + s_{22}a_2 \quad (2.2)$$

From (2.1) s_{21} can be written as

$$s_{21} = \frac{b_2}{a_1} \quad , \quad a_2 = 0 \quad (2.3)$$

Insertion loss is expressed as the reciprocal of the ratio of the signal power delivered to the part of the line following the device to the signal power delivered to that same part prior to insertion assuming a load of $Z_L = 50\ \Omega$ at port 1 and port 2. Therefore, insertion loss is expressed as:

$$Insertion\ Loss = -20log_{10}|s_{21}| \quad (2.4)$$

This is utilized to determine the loss measurement and is measured in both ON and OFF mode.

2.2.2 Return Loss

Return loss of an RF switch refers to the RF loss that is reflected back by the device, typically characterized by S_{11} at the input and S_{22} at the output of the switch in the ON state. The main contributing factors include the mismatch of the total switch characteristic impedance.

2.2.3 Isolation

Isolation of RF switch is characterized by S_{21} of the switch in the OFF state. The main contributing factors include capacitive coupling and surface leakage.

2.2.4 1dB Compression Point

The 1dB compression point is a measure of the amount of power a device can handle prior to saturation. At low signal power level, a typical device tends to be linear; however, as the input signal is increased, the output power begins to trail off to gain compression as the output signal (voltage, current, power) eventually reaches the limits. When this trailing difference of output power from the linear response reaches 1 dB, the input or output power of this point is measured and referred to as

the input 1dB or output 1dB compression point respectively. Figure 2-6 is depicting an output power versus input power plot showing the 1 dB compression point [25].

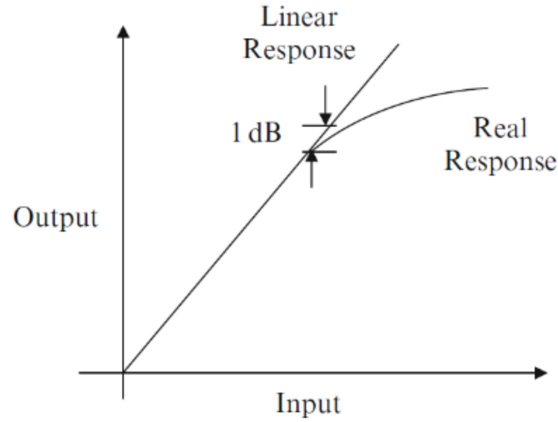


Figure 2-6: 1 dB compression point [25]

A large signal curve can be described by a polynomial, $S_o = a_1 + a_2 {s_i}^1 + a_3 {s_i}^2 + \cdots a_n {s_i}^{n-1}$. For an input signal of $s_i = S_1 \cos(\omega_1 t)$, the cubic terms generate $S_1^3\left(\frac{3}{4}\cos(\omega_1 t) + \frac{1}{4}\cos(3\omega_1 t)\right)$. Therefore, the apparent gain of a system is described by equation (2.5) [26].

$$G = \frac{S_{o,\omega_1}}{S_{i,\omega_1}} = \frac{a_1 S_1 + \frac{3}{4} a_3 S_1^3}{S_1} = a_1 + \frac{3}{4} a_3 S_1^2 = a_1\left(1 + \frac{3}{4}\frac{a_3}{a_1} S_1^2\right) = G(S_1) \tag{2.5}$$

Using equation (2.6), the input level where the gain has dropped by 1 dB is obtained where the term S_1 refers to the fundamental signal.

$$20log\left(1 + \frac{3}{4}\frac{a_3}{a_1} S_1^2\right) = -1dB;\ \frac{3}{4}\frac{a_3}{a_1} S_1^2 = -0.11 \tag{2.6}$$

2.2.5 Linearity

The output signal of a network consisting active devices; such as, transistors, is a non-linear function of the input signal. If the input signal is $s_i = S_1 \cos(\omega_1 t)$ with $\omega_1 = 2\pi f_1$, the output of the system can be modeled by equation (2.7) [27].

$$S_o = a_1 + a_2 {s_i}^2 + a_3 {s_i}^3 + \cdots a_n {s_i}^n = \sum_n a_n S^{n-1}\,; n = 1, 2, 3, \ldots \tag{2.7}$$

In equation (2.7), terms $n > 1$ are referred to as the harmonics of the fundamental signals. If the input signal comprises of multi-tone signals, intermodulation products are also generated. These intermodulation products is the additive and subtractive combinations of the fundamental signal and

the harmonics as shown in Figure 2-7 [27].

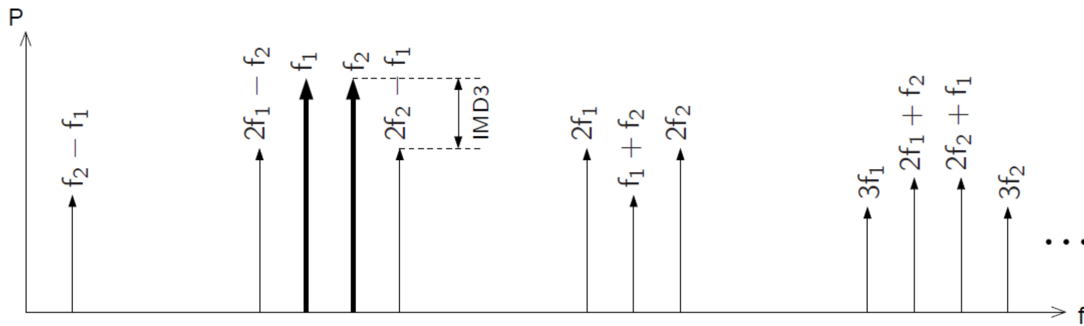


Figure 2-7: Spectrum of two tone signals at frequencies f_1 and f_2 with their harmonics and intermodulation products [27]

It can be observed from Figure 2-7, that the third order intermodulation products at the frequencies $2f_1 - f_2$ and $2f_2 - f_1$ are the closest to the operating frequency. Therefore, as an indicator of non-linearity of a system, the difference between the amplitudes of the fundamental signals and third order intermodulation product is used and is defined as third order intermodulation distortion (IMD_3). The power of 3rd order intermodulation products is cube of the input power; whereas, the output power of the fundamental signals is linearly proportional to the input power as shown in Figure 2-8 [28].

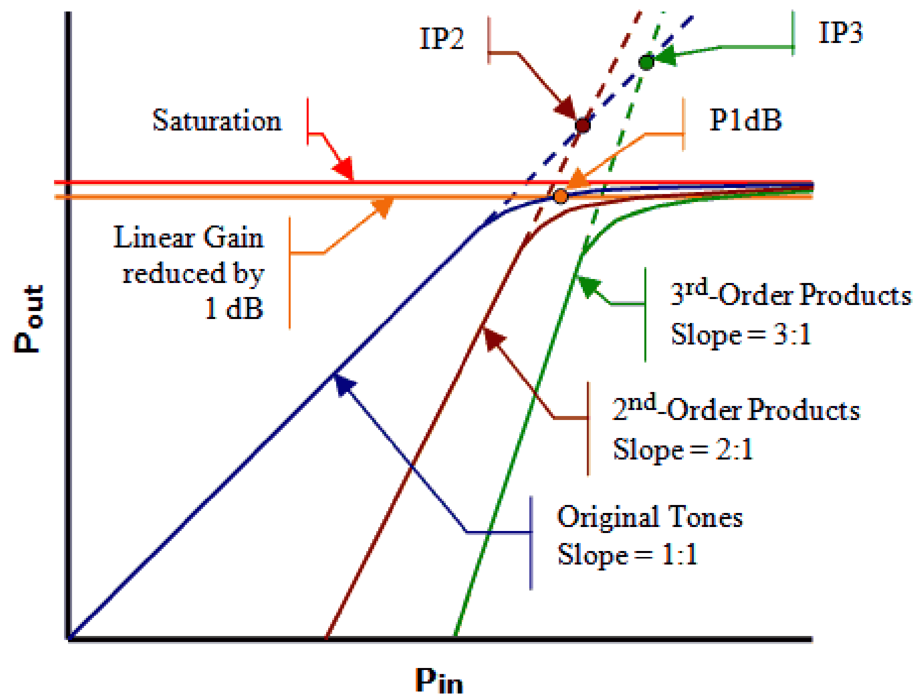


Figure 2-8: Input and output of two-tone and intermodulation distortion [28]

Figure 2-8 depicts the intercept point of the extrapolated fundamental and the third order response, which is called the third order intercept point (IP_3). Signal response from fundamental and third order indicates the tendency of the network to be nonlinear as the input power increases. At the IP_3 point, the input power level is known as IIP_3 and the point where the output power occurs is known as the OIP_3 point.

2.2.6 Switching Speed

"Rise Time" and "Fall Time" are fundamental to many designs and are composed of several subsets; each one defining the time required for switching to take place between two states in the switch response. Rise time is defined as the period between the OFF state to ON state, typically from 10% of this condition to 90% of the square-law-detected RF power and can be expressed in terms of circuitry resistance ($R_{circuit}$) and load capacitance (C_{load}) as shown in (2.8) [23].

$$T_r = 2.2 R_{circuit} C_{load} \tag{2.8}$$

Conversely, fall time is the period between 90% ON state to 10% OFF state and can be calculated using (2.9) [23].

$$T_f = 2.2 R_{circuit} C_{load} \tag{2.9}$$

It should be noted that rise and fall time do not include driver or other propagation delays. Figure 2-9 displays the rise time during the associated ON time period and fall time during the OFF time period. "ON Time" and "OFF Time" are time lapse between 50% of full input control signal from the previous stage to 90% of the square-law-detected RF power. When the device is switched from OFF to ON, it is called the ON time. Subsequently, the OFF time begins when 50% point of control signal occurs, to the point where 10% of its square-law detected RF power is achieved and the unit is switched from full ON to OFF.

The port-to-port switching time shown in Figure 2-10 is sometimes referred to as "Commutation Time", when RF power level at the OFF port falls to 10% of its original level to the time the RF power in the ON port rises to 90% of its final value. Typically, in high-speed reflective switches, commutation time is slightly longer than ON or OFF time.

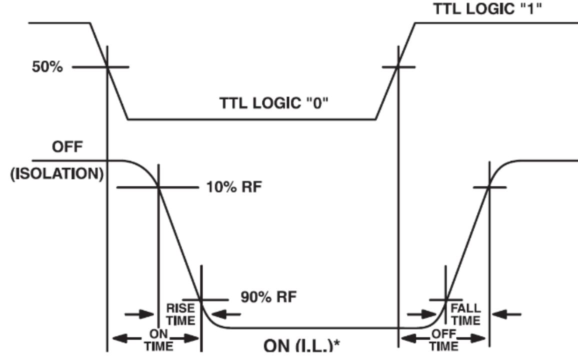


Figure 2-9: Detected RF Power depicting rise time and fall time [29]

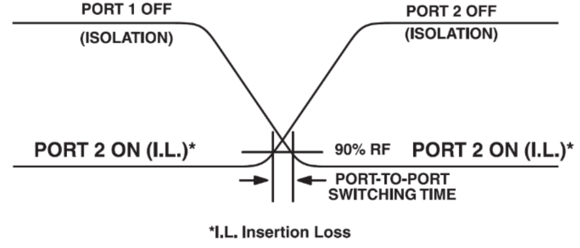


Figure 2-10: Switching Speed Characteristics [29]

2.2.7 Noise

Noise factor is the measure of signal-to-noise ratio (SNR) degradation by noisy circuit after signal passes through it. Noise factor, F, can be described as (2.10) [10]:

$$F = \frac{SNR_i}{SNR_o} \tag{2.10}$$

An expression for noise factor of a two-port network, which is related to the reflection coefficient of a two-port network is shown in (2.11) [10].

$$F = F_{min} + 4\frac{R_N}{Z_o}\frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{(1 - |\Gamma_S|^2)\left|1 + \Gamma_{opt}\right|^2} \tag{2.11}$$

where F_{min} is the minimum noise factor, R_N is the equivalent noise resistance, Γ_S and Γ_{opt} are the optimal reflection coefficient corresponding to the optimal source admittance that provides the minimum noise factor. These parameters are the device characteristics. The SNR at the FEM output is reduced by factor F and is obtained using (2.12), where NF is the noise figure of the RF FEM system [10].

$$SNR_o = SNR_I - NF \tag{2.12}$$

NF of a system is the noise factor expressed in dB and can be described as (2.13) [10].

$$NF = 10\,log\frac{SNR_i}{SNR_o} = 10\,log\left(1 + \frac{P_{N_system}}{P_{N_i}}\right)\text{ dB} \tag{2.13}$$

The physical meaning of the noise figure is a measure of the SNR degradation as the signal passes through a system [30]. Now spectral efficiency of a digital modulator can be defined as the number of bits per second that can be transmitted in 1 Hz of bandwidth. Channel capacity can be calculated using Shannon-Hartley theorem, which is suitable to describe spectral efficiency and can be stated as

(2.14) [10].

$$C = W log_2 \left(1 + \frac{S}{N}\right) \tag{2.14}$$

where $\frac{S}{N}$ is the ratio of average signal power received to noise power and W is the channel bandwidth. It can be seen that capacity is related to the signal to noise ratio based on (2.14). As the noise of the system increases, the $\frac{S}{N}$ would decrease, which in turn reduces the capacity. Thus, noise at FEM reduces the system capacity.

2.3 Comparison of Various Switches

There are a variety of switches available for advance communication systems; however, the most important and basic types of switches are designed with PIN Diode, GaAs FET, MESFET, MOSFET, MEMS and GaN technologies, which are all discussed and compared in this section.

2.3.1 PIN Diode Switch

A PIN diode is a semiconductor diode in which a high resistivity intrinsic (I) region is sandwiched between p-type and n-type region and named as P-I-N. Without proper biasing of a PIN device, the diode behaves like a capacitance and with biasing it behaves like an inductor. As PIN diodes have high linearity characteristics, it can be used for high frequency and high power applications. A higher DC power is required to have a substantially low insertion loss.

PIN diode is a current-controlled resistance that operates as a variable resistor at the RF regime of the electromagnetic spectrum. The resistance value of a PIN diode is determined only by the forward-biased DC current. PIN diode has the ability to control large RF signals while using much smaller levels of DC excitation. Typically, an ON-state PIN diode is biased using a large current of about 10 mA to ensure that AC resistance is low [31]. Subsequently, in the OFF state, the PIN structure has a low junction capacitance, which ensures large isolation.

PIN diode switches can be fabricated using silicon and gallium arsenide, which displays a low insertion loss($< 1\ dB$) and high power handling($> 5\ W$) up to very high frequencies. However, due to their static power consumption, the bias current requirement severely limits its applications [32]. Since a large bias current is required to control the PIN diode switch, it is supplied through a choke, which simply pass DC signal and block everything else. Due to the power consumption requirement, PIN diode switches are not ideal for mobile radio systems.

2.3.2 GaAs FET Switch

A Gallium Arsenide (GaAs) FET integrated switch circuit can be used to achieve switching between multiple RF chains [33]. It behaves as a voltage controlled resistor and typically used in broadband communication systems from 0.5 to 4 GHz [23]. GaAs switches can provide lower insertion loss with good isolation performances, low power consumption and better switching speeds compared to Complementary Metal-Oxide-Semiconductor (CMOS). However, there is a drawback of maximum control voltage that can be applied, which is typically up to 6V, which limits the power handling capabilities.

2.3.3 MESFET Switch

Metal Semiconductor Field Effect Transistor (MESFETs) are carrier devices that are applicable for high-speed operations. This can be fabricated using silicon, gallium arsenide, and indium phosphide [34]. However, silicon based MESFETs cannot handle large powers and are typically slower than other materials. For high power ($> 1\ W$) and high frequency ($> 1\ GHz$) applications, MESFETS are implemented using GaAs due to its band gap properties, which results in high breakdown voltage. However, GaN provides larger band gap than GaAs, hence resulting in higher breakdown voltage. There is a tradeoff between its ON-state resistance and OFF-state capacitance. In order to achieve a low insertion loss, a large device with low ON-resistance can be used, but this degrades the isolation performance since the OFF-state capacitance will be larger. The major limitation of GaAs MESFET switches is that they cannot be integrated with silicon-based transceiver.

2.3.4 MOSFET Switch

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is one of the simplest switch options available for RF applications. It is also available in a CMOS process. Only silicon-based MOSFETs are suitable for RF switches due to the absence of a gate insulator for other materials [35]. The ON-state resistance of silicon MOSFET is significantly inferior to a GaAs MESFET due to poor electron mobility in the channel at low electric fields. Development in technology offers very small channel length MOSFETs with a better R_{ON} x C_{OFF} product [36]. Thin gate dielectric and small channel length enables low voltage operation. The channel and substrate resistances are the main sources of power loss in the MOSFET. Substrate resistance may be reduced by grounding the substrate in close proximity to the device. The low quality factor of the source and drain parasitic junction capacitors leads to significant losses and further degradation as frequency of operation increases. The linearity of the MOSFET switch is limited for large signal swings due to conductivity modulation caused

by a changing gate-source (V_{GS}) and drain-source (V_{DS}) voltage for a large input signal.

2.3.5 MEMS Switch

The Micro-Electro-Mechanical Systems (MEMS) switches are micro machine devices that utilize mechanical movement to achieve ON (short) or OFF (open) circuit in a RF path.

The mechanical movement of MEMS switch controls the impedance of a transmission line. Typically, RF MEMS switches are designed to operate between frequencies 0.1 – 100 GHz of the spectrum. As a result, they have significant advantages over traditional RF switches with their broadband operating frequency range.

Furthermore, they have high isolation, low insertion loss, low power consumption, simple biasing network, and low intermodulation products [37]. However, they have several disadvantages; such as, slow switching speed that can be in orders of microseconds, high actuation voltage requirement, and hot switching effects in high-power applications.

2.3.6 GaN HEMT Switch

The wide bandgap of SiC and GaN results in very low intrinsic carrier concentration that gives negligible junction leakage current up to 500°C. As a result, these devices can operate at a very high temperature without excessive leakage or thermal runaway, which significantly reduces cooling requirements. Table 2-1 compares key electronic properties of major semiconductors.

Table 2-1: Physical properties of different semiconductors for high-voltage devices [39].

Material	Si	4H-SiC	GaAs	GaN
Bandgap (eV)	1.11	3.2	1.43	3.4
Dielectric constant	11.8	9.7	12.8	9
Breakdown field (x10^5 V/cm)	2	30	4	30
Electron mobility (cm^2/Vs	1350	800	6000	1000
Hole mobility (cm^2/Vs)	450	120	330	300
Saturated velocity (x10^7 cm/s)	1	2	1	1.5
Thermal conductivity (W/cmK)	1.5	4.9	0.5	1.3

The high breakdown strength requires thinner drift layers for a given blocking voltage as compared to silicon, thus reducing the specific ON-resistance and storage of minority carriers [39]. Therefore, the associated switching loss is reduced, which allows higher switching frequency of the devices that significantly reduces the size in switches.

A key parameter to consider for RF switches is its active component's breakdown voltage V_{BR}, ON state resistance R_{ON}, and voltage control ratio $VBR/\Delta Vcontrol$. Typically, if low R_{ON} is desired, the device doping-level should be increased, since V_{BR} is twice the integration of the doping level along the depletion region. Therefore, it drops at a square rate with the decrease of the ON-resistance.

A figure of merit can be used to compare devices with different rating of V_{BR} and R_{ON} as shown in (2.15) [40].

$$\text{Figure of merit to compare semiconductors} = \frac{{V_{BR}}^2}{R_{ON}} \qquad (2.15)$$

Table 2-2 shows the figure of merit of different wide bandgap semiconductors, the advantages of AlGaN/GaN over SiC [39] [41]. The low thermal conductivity of GaN can be largely mitigated by the SiC substrate that the GaN can be grown on.

HEMTs can be fabricated on AlGaN/GaN material system to take advantage of the 2-DEG (two-dimensional Electron Gas) at the heterojunction which provides high mobility that further reduces the ON-resistance. Furthermore, it enables high channel density due to large band discontinuity and the polarization field. A HEMT structure also leads to low input capacitance, since the 2-DEG can be generated without doping the AlGaN layer of a device.

Table 2-2: Normalized figure of merit of wide bandgap semiconductors [43]

	Si	4H-SiC	GaAs	GaN
JFM	1.0	215.1	1.8	215.1
BFM	1.0	223.1	14.8	186.7
FSFM	1.0	61.2	11.4	65.0
FPFM	1.0	56.0	3.6	30.4
FTFM	1.0	3424.8	40.7	1973.6

JFM: Johnson's figure of merit is a measure of the ultimate high frequency capability of the material.
BFM: Baliga's figure of merit is a measure of the specific ON resistance of the drift region of a FET
FSFM: Figure of merit of FET switching speed
FPFM: Figure of merit of FET power handling capacity
FTFM: Figure of merit of FET power switching product

Recently, high μ·ns product (μ=1500 cm2/V·s and ns=2. 15x1013 cm-2) has been achieved, which has the potential to offer very low ON-resistance and high switching speed for GaN HEMTs [43]. ON-resistance of a vertical device structure with uniform doping can be represented by (2.16) [44].

$$R_{ON} = \frac{4{V_{BR}}^2}{\varepsilon_r \mu_n {E_c}^3} \tag{2.16}$$

where ε_r is the dielectric constant, μ_n is the mobility and E_c is the critical electric field. ON-resistance of SiC can be lowered by two orders of magnitude than that of Si for same breakdown voltage.

The industry uses a simplified version of Figure of Merit (FOM) to rate the switching characteristics of different switching elements which is based on capacitance realization when FET is in OFF state (C_{OFF}) and R_{ON} values. The Figure of Merit to rate switches can be represented by (2.17) [45].

$$Figure\ of\ Merit = \frac{1}{2\pi\ x\ C_{OFF}\ x\ R_{ON}} \tag{2.17}$$

Figure of Merit could be characterized in terms of frequency where the higher the value, the easier it is to achieve larger bandwidth. As a rule of thumb, the switching $\frac{1}{10} \times FOM$ gives the highest frequency that the device can be made to perform as a switch. Table 2-3 shows the comparison of different technologies that can be used to design RF switches and its parameters.

Table 2-3: Comparison of Different Technologies to Design RF Switches [46]

	1 micron MESFET	Silicon PIN diode	GaAs PIN diode	0.25 micron PHEMT	0.15 micron NRC GaN150 HEMT [47]
Number of terminals	3	2	2	3	3
Typical ON-resistance	1.5 Ω-mm	1.7 Ω	1.7 Ω	1.2 Ω-mm	3.56 Ω-mm
Typical OFF-capacitance	0.40 pF/mm	0.05 pF	0.05pF	0.32 pF/mm	0.07 pF/mm
Figure of merit	265 GHz	1872 GHz	1872 GHz	414 GHz	638 GHz
Breakdown voltage	15 volts	50 volts	30 volts	8 volts	80 V
Lower frequency limit	DC	10 MHz	10 MHz	DC	DC
Highest operational switch frequency	26.5 GHz	187.2 GHz	187.2 GHz	41.4 GHz	63.8 GHz
Driver circuit complexity	low	high	high	low	Low
Driver requirements	0 volts on -5 volts off	5 to 10 mA on 0 to -30 V off	5 to 10 mA on 0 to -30 V off	+0.5 volts on -5 volts off	2 volts on -8 to -3.6 V off

2.4 Conclusion

In this chapter, various switch topologies were investigated. A comparative analysis with MESFET, Si PIN, GaAs PIN, and 0.25μm pHEMT was conducted to identify benefits of GaN RF switches. The NRC GaN150 technology has a large breakdown voltage, high FOM, and high operational frequency. NRC GaN150 FET have slightly higher ON resistance compared to other technology but have smaller OFF capacitance than 1 micron MESFET and 0.25μm pHEMT.

The following chapter will use the presented concepts to characterize FET and other passive components to design fundamental switch topologies, SPST, SPDT, and double pole switch configurations.

3

GaN RF Switch Design

The technology being offered by the National Research Council of Canada is a GaN-based HFET technology using 3-inch silicon carbide wafers of 75μm thickness. It features a 0.15μm long metal gate, two metal layers for interconnect, 50 Ω/sq nichrome resistors and MIM capacitors with densities of 0.19 fF/μm^2 [47]. All transistors included in this version, do not employ field plate designs; however, the shape of the gate results in better frequency performance and is suitable for 30V maximum drain voltage bias, and yield power levels of ~7 W/mm (measured at 8 GHz). The design kit used here includes a provisional root model for the GaN HFETs and the through-wafer vias on thinned SiC substrates that are supported to improve the thermal performance, as well as add additional design flexibility.

The goal of this Chapter is to characterize circuit components in order to develop an understanding of fundamental building blocks of RF switch topology, using series, shunt, and series-shunt topologies. This will form the basis on which more complex switch topologies will be designed and analyzed. Thereafter, a section will outline a broadband SPDT design to operate at L, S, C, and X bands. Then, a double-pole diamond structure switch is presented, which can operate as DPST, with two poles and one active throw and DPDT, with two poles and two active throw [48]. Lastly, the section will conclude by analyzing different switch parameters and potential target applications.

3.1 Switch Design Procedures

This section presents a systematic procedure to design a generic RF switch.

1. FET AC Analysis
   - **Drain current density:** Drain current density versus gate voltage will determine the gate plateau voltage governed by the transconductance of the device [49]. Typically, when

the gate voltage reaches the threshold voltage, the drain current begins to increase very rapidly until it reaches the ON state current density [49]. This helps determining the optimum gate width for desired specific ON resistance based on current density.

- **Drain-Source Bias Voltage:** Maximum drain-source voltage will provide guidelines of the signal voltage level the transistor can handle.
- **Gate-Source Voltage:** Provides the range for the control voltages for the switch.
- **DC Power per Millimeter Gate Width:** Provides the power handling capabilities of a transistor based on gate width.

2. FET DC Analysis
   - **Plot C_{OFF} versus V_{GS}:** Obtain V_{GS} where C_{OFF} is lowest. This provides optimum OFF state bias voltage for single FET switch operation.
   - **Plot Resistance versus V_{GS}:** This will evaluate the parallel resistor value when in OFF state, and series resistor value when in ON state.
   - **Plot R_{ON} vs V_{GS}:** Obtain V_{GS} where R_{ON} is lowest. This helps find optimum ON-State bias point for single FET

3. Calculate Figure of Merit
   - **Assess the device:** Carry out figure of merit simulations based on R_{ON} and C_{OFF} to estimate the expected performance.

4. Characterize components
   - **Capacitor and Inductor:** Simulate design kit component to obtain its quality factor. This plot will suggest the component sizes that can be used to design switch topologies.

5. Topology

   The requirement from the switch will vary if it is configured for transmit port (large signal operation), receive port (small signal operation) or as a T/R switch.

6. Small signal analysis
   - **Insertion Loss, $S_{21_ON\ State}$:** Plot of insertion loss to evaluate the loss of the switch over frequency when in ON state.
   - **Isolation ($S_{21_OFF\ State}$):** Plot of insertion loss to evaluate the loss of the switch over frequency when in OFF state.
   - **Return Loss, (S_{11} and S_{22}):** For input return loss and output return loss of the switch, S_{11}

and S_{22} simulations are carried out, respectively.

7. Large signal analysis
   - **Input versus Output RF power:** Input versus output power plot in large signal simulation can present the switch behavior based on the input RF power. This simulation can also be executed by keeping the switch in OFF state to identify which large signal isolation should the switch use to only switch between large signal paths.
   - **Loss Compression versus Input Power:** This plot of loss compression versus input power will assist in identifying the 1 dB compression point of the switch. The switch compression point is influenced by many factors, such as wafer process, design topology, magnitude of the DC bias control voltage, frequency of operation, and thermal properties [50]. Power range should begin from small signal to large signal to establish the drop in gain in the plot.
   - **Output Third Order Intercept (OTOI) versus Input Power:** OTOI versus Input power plot will evaluate the third order intercept point of the switch for a given input power.
   - **Linearity:** Parameters to specify switch linearity are IIP_3, or error vector magnitude (EVM). Typically, plotting the fundamental and IMD_3 to identify the IIP_3 of the switch will describe the linearity performance of the switch. Parameters for linearity give a better indication whether the switch will meet the system linearity and spurious emission requirements at the input signal levels, which will be incident upon the switch in a system. The specific linearity requirement, the frequency of operation, wafer process, and topology must match up to meet such a requirement.

8. Layout Rules:
   - Plan access to RF ports and DC pads.
   - Minimize discontinuities.
   - Ensure adequate dimensions are used for traces to be connected to drain and source.
   - Ensure gate has access to DC Feeds.
   - Minimize transmission length to reduce losses (if not $\lambda/4$ shunt switch).

3.2 Component Modelling

3.2.1 FET

The device used in this work is based on NRC GaN 0.15μm process. The FET available in this PDK has a larger T-gate overlap of 0.25μm [47]. As a result, they have a high breakdown voltage; however, it is a trade off with frequency performance. Transistor characteristics of GaN150 are outlined in Table 3-1.

Table 3-1: NRC GaN 150 Parameters [47]

Parameter	Abbreviation	Value
Breakdown Voltage	V_{DS_BD}	>80 V
Maximum drain current Density	J_{DSmax}	1000 mA/mm
Drain current density at V_{GS}=0	J_{DSS}	800 mA/mm
Maximum long-term operating drain current Density	J_{DS}	350 mA/mm
Drain-Source Bias Voltage	V_{DS}	30 V
Gate-Source Voltage	V_{GS}	-8 to +2 V
Gate Leakage Current Density	J_{GS}	1 mA/mm
DC Power per Millimeter Gate Width	P_{DC}	10 W

3.2.1.1 Power Handling

Power handling for switches correspond to the onset of gain compression. Once it exceeds the calculated power handling, the insertion loss of switch starts to increase. Ideally, a switch should operate without any compression. Power handling for FETs in the ON state can be expressed using the maximum current of the device that it can pass and is defined by (3.1) [51].

$$ON\ state\ power\ handling = \frac{{I_{max}}^2 Z_0}{2} \tag{3.1}$$

Maximum current handling capability of the devices is proportional to the periphery of the device. The minimum gate width of the FET is 2x20 μm and maximum of 2x250 μm is available; however, 2x200 μm is the maximum recommended size by the foundry. Since the device has a rating of P_{DC} = 10W/mm, which gives a range of 1.025 to 20 W power handling capabilities from 2x20 and 2x200μm FET respectively. The maximum power handling for FETs in the OFF state is a function of breakdown voltage and is stated in (3.2) [51].

$$OFF\ state\ power\ handling = \frac{(V_{BR} - V_{PO})^2}{2 \cdot Z_0} \tag{3.2}$$

The greater the difference between a pinch off voltage (V_{PO}) and breakdown voltage (V_{BR}), the higher the power handling in the OFF state. Therefore, optimum voltage for power handling is merely the arithmetic average, which is represented by (3.3) [51].

$$Optimum\ OFF\ voltage = \frac{V_{BR} + V_{PO}}{2} \tag{3.3}$$

3.2.1.2 On-State

As discussed previously, figure of merit for comparing switches is a function of the ON resistance, R_{ON}, and the OFF capacitance, C_{OFF} of the FET channel. Figure 3-1 shows a pHEMT small signal equivalent circuit model [52].

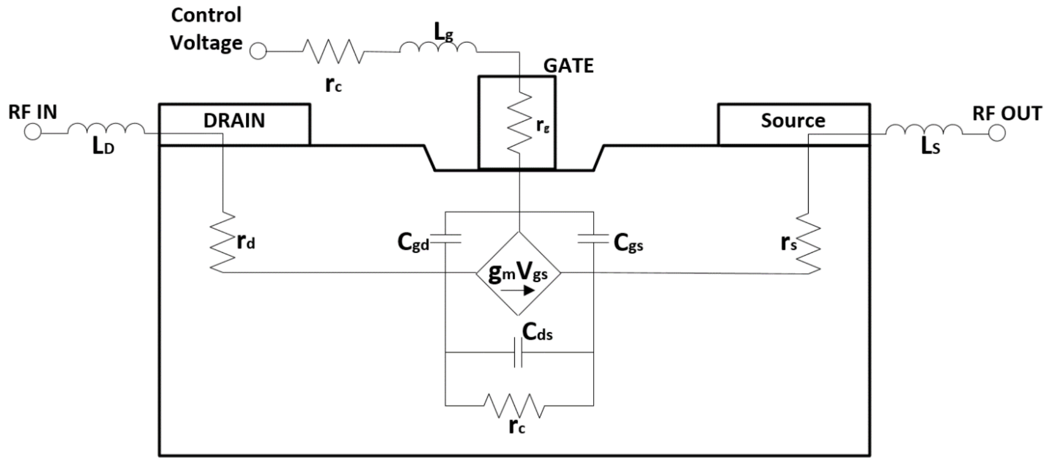


Figure 3-1: Small signal model of pHEMT

Parameters of interest that affect R_{ON} and C_{OFF} are r_{ds} and C_G respectively. The resistance, r_{ds} can be calculated using an assumption that r_d and r_s are insignificant compared to r_{ds}. Hence, by measuring V_D and I_D of a given device, r_{ds} can be determined in terms of the ratio given by (3.4) [52]. The plot of I-V characteristic of a 2x200 µm FET with biasing from V_{GS} -8V to 2V in steps of 1 V is shown in Figure 3-2.

$$r_{ds} \cong \frac{V_D}{I_D} \tag{3.4}$$

Figure 3-2 and Figure 3-3, shows the ON state FET impedance and inductance versus gate bias voltage varying FET size of 2x20, 2x40, 2x60, 2x80, 2x100, 2x120, 2x140, 2x160, 2x180, and 2x200µm for center frequencies of L-Band, S-band, C-band, and X-Band, respectively. This will determine the ON state bias voltage of different FET sizes.

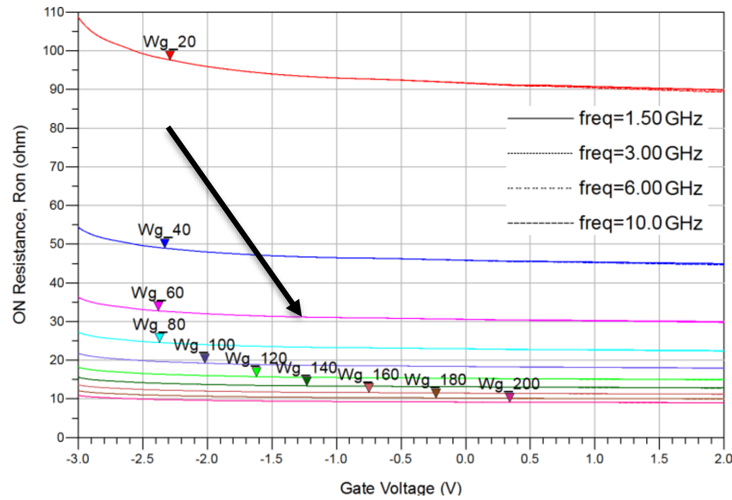


Figure 3-2: R_{ON} Vs Gate Votage of an ON State FET varying gate width

For all frequency bands of interest, the impedance and inductance is lower for bigger FET sizes. The lowest impedance of 8.9 Ω is determined for a device with dimensions of 2x200μm; whereas, the largest impedance of 89.27 Ω is obtained when the FET size is 2x20μm.

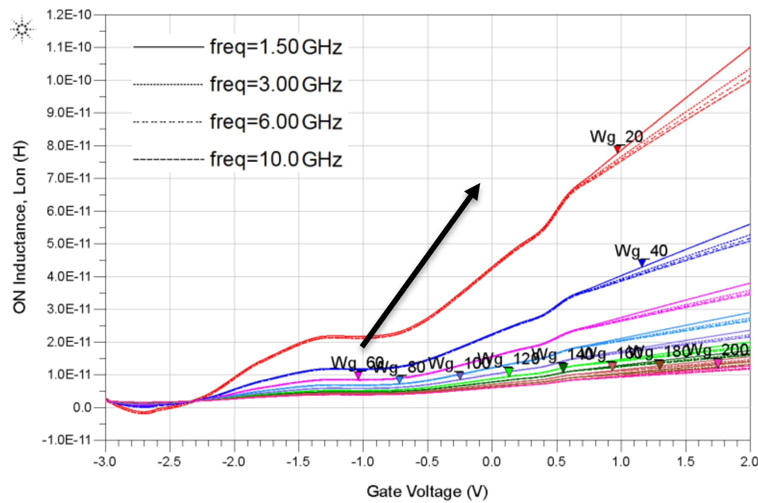


Figure 3-3: Inductance Vs gate voltage of an ON State FET varying gate width

3.2.1.3 Off-state

Drain to source capacitance, denoted by C_{DS} is dominated by the drain to gate and from gate to source capacitance, C_G. The minimum C_G is controlled by the physical dimensions of the device as well as the dielectric constants of the substrate, C_{Gmin} and can be defined by (3.5) [53].

$$C_{Gmin} = \frac{\epsilon_s \cdot W \cdot L}{a} \tag{3.5}$$

where ϵ_s, is the dielectric constant, W is the width of the device, L is the length of the devices, and a

is the maximum space charge width. Figure 3-4 and Figure 3-5 are simulations for OFF state FET. They display plots of resistance and capacitance versus gate bias voltage varying FET size of 2x20, 2x40, 2x60, 2x80, 2x100, 2x120, 2x140, 2x160, 2x180, and 2x200μm for L Band, S band, C band, and X Band frequencies, respectively.

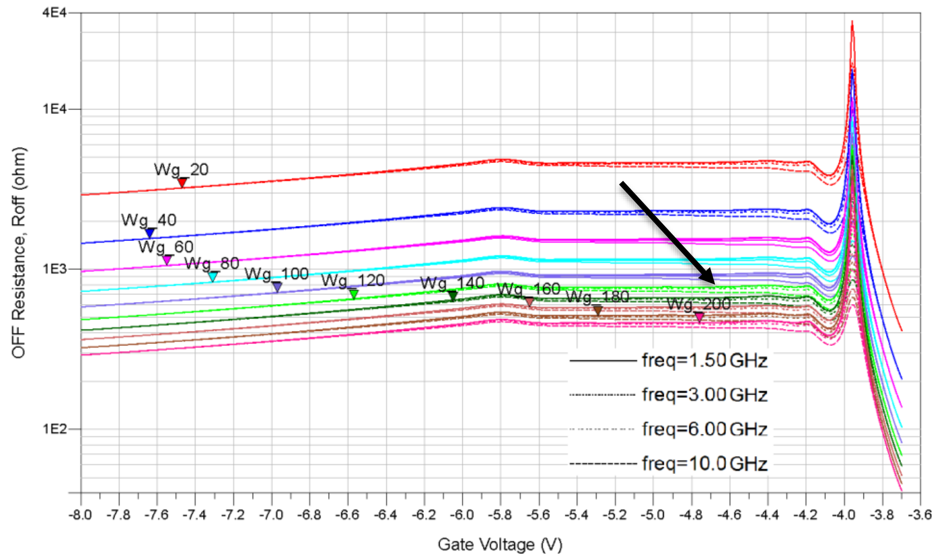


Figure 3-4: FET R_{OFF} Vs Gate Votlage of an OFF State FET varying gate width

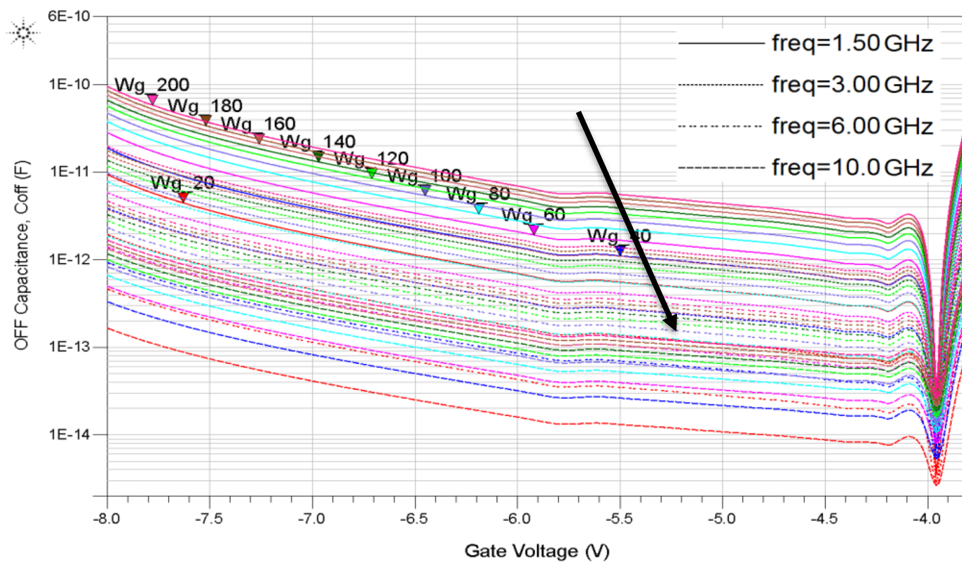


Figure 3-5: FET capacitance Vs gate bias of an OFF State FET varying gate width

3.2.1.4 Summary

As shown in Figure 3-4 and Figure 3-5, for all frequency bands of interest, the impedance is highest and capacitance is lowest for smaller FET sizes when the device is biased around -4V. By characterizing ON and OFF state FET, the FET biasing voltage and optimum FET size is obtained.

As previously discussed, for ON state, the R_{ON} must be at its lowest, which is obtained when the gate voltage is at the highest tolerable voltage of the FET (2V) and C_{OFF} is lowest when the gate voltage is around -4V. As a result, bias voltages of 2V and -4V for ON and OFF state, respectively, provide higher FOM expressed by (2.17). Table 3-2 shows the parameters for a single FET switch. It indicates the C_{OFF} and R_{OFF} for OFF state and R_{ON}, and L_{ON} for ON state varying different gate widths.

Table 3-2: Summary of RF Switch parameters of GaN150 FET

	R_{ON} @ 2V (Ω)		L_{ON} @ 2V (pH)		R_{OFF} @ -3.96 (Ω)		C_{OFF} @ -3.96V (fF)	
Widthµm	1.5 GHz	10 GHz	1.5 GHz	10 GHz	1.5 GHz	10 GHz	1.5 GHz	10 GHz
2x20	89.90	89.28	110.00	99.77	4683.00	4234.00	3.34	2.65
2x40	44.95	44.64	56.04	50.88	2317.00	2098.00	6.63	5.30
2x60	29.96	29.77	38.03	34.59	1528.00	1383.00	9.87	7.96
2x80	22.47	22.33	29.02	26.44	1130.00	1027.00	13.06	10.61
2x100	17.98	17.86	23.62	21.55	857.30	812.30	16.20	13.26
2x120	14.98	14.89	20.01	18.29	673.50	661.70	19.30	15.91
2x140	12.84	12.76	15.96	15.96	638.00	583.20	22.36	18.56
2x160	11.24	11.17	15.50	15.50	544.10	490.90	25.38	21.20
2x180	9.92	9.92	14.00	12.85	466.70	432.00	28.37	23.85
2x200	8.98	8.93	12.79	11.76	418.70	394.80	31.32	26.50

3.2.2 Capacitor

The quality factor of a capacitor quantifies its ability to store energy and can be defined by [24]:

$$Q_C = \frac{X_C}{R_C} = \frac{1}{\omega_0 C R_C} \tag{3.6}$$

where Q_C is the quality factor, X_C the reactance of the capacitor, C the capacitance, R_C the equivalent series resistance (ESR) of the capacitor, and ω_0 the angular frequency, as displayed in Figure 3-6.

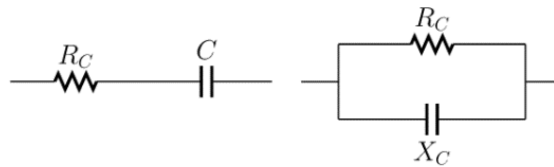


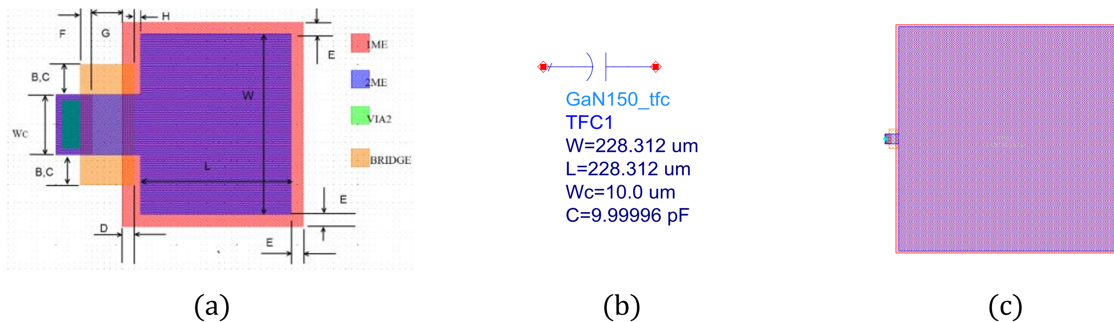
Figure 3-6: Equivalent series resistance of capacitor (ESR)

Metal-Insulator-Metal (MIM) capacitors are formed by an interconnect layer using 3µm of gold (2ME) on top of the interconnect layer formed using 1µm of gold (1ME) without a connecting layer between 1ME and 2ME (VIA2) being present [47].

A layer of silicon nitride is used as a dielectric layer and provides insulation. The statistical yield of fabricated capacitors is affected by defects in the dielectric. An excellent yield can be obtained with a maximum size of 800 x 800μm containing an allowed tolerance of the less than ±10%. As a result, maximum capacitance from this model is 122 pF. Electrical parameters of the capacitors are shown in Table 3-3 [47]. Figure 3-7 shows an NRC GaN150 capacitance model that depicts high level capacitor diagram with layers, schematic, and ADS momentum layout view of the component respectively.

Table 3-3: NRC GaN150 Capacitor Parameters

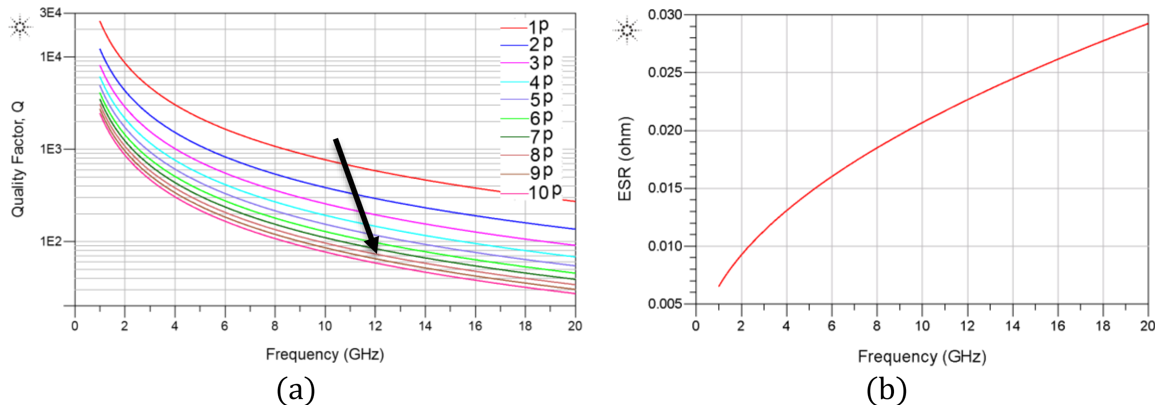
Parameters	Value
Dielectric Thickness	0.3μm
Dielectric Constant	6.5
Capacitance Density	0.19 fF/μm²
Maximum Capacitance	122 pF
Maximum Operating Voltage	40 V
Minimum Breakdown Voltage	180



(a) (b) (c)

Figure 3-7: (a) Sizing; (b) Schematic model; and (c) layout model of GaN150 MIM capacitor

Figure 3-8 uses equation (3.6) to calculate the quality factor of the NRC GaN150 capacitor model for 1 to 10 pF capacitors. The quality factor is observed to be higher for smaller size capacitor and decreases over frequency.



(a) (b)

Figure 3-8: (a) Quality factor of different capacitor value over frequency; (b) ESR vs Frequency using GaN150

The ESR is not a constant value with regards to frequency, it varies with frequency due to the skin effect, as well as other effects related to the dielectric characteristics. This is illustrated in Figure 3-8, where a GaN150 kit model was simulated over frequency to plot the ESR over frequency.

3.2.3 Inductor

Resistance as a quality factor is important because it will add loss to the signal path. Any resistance will reduce the overall inductor Q factor. A simple inductor AC model can be expressed as a perfect inductor with a series resistor as shown in Figure 3-9.

$$Q = \frac{X_L}{R} = \frac{2\pi f L}{R} \tag{3.7}$$

Figure 3-9: Equivalent circuit of an Inductor

where L is a perfect inductor and R is the associated resistance of the inductor. Equation (3.7) can be used to calculate the quality factor for an inductor [24]. Equation (3.7) demonstrates that the inductive reactance X is frequency dependent, hence Q will also vary for different frequency of operation. The resistance losses, R, are due to the skin effect, radiation losses, eddy current, and hysteresis, which also varies with frequency but are not captured by the equation (3.7).

The GaN150 kit has a spiral inductor model. It is a wound around a central empty area with a recommended minimum size of 50 x 50µm. The inductor turns are reinforced on 2ME on 1ME which results in a higher Q-factor. Figure 3-10 shows NRC GaN150 spiral inductor model, it depicts a high level capacitor diagram with specific layers identified as an ADS schematic component and an ADS momentum layout component respectively.

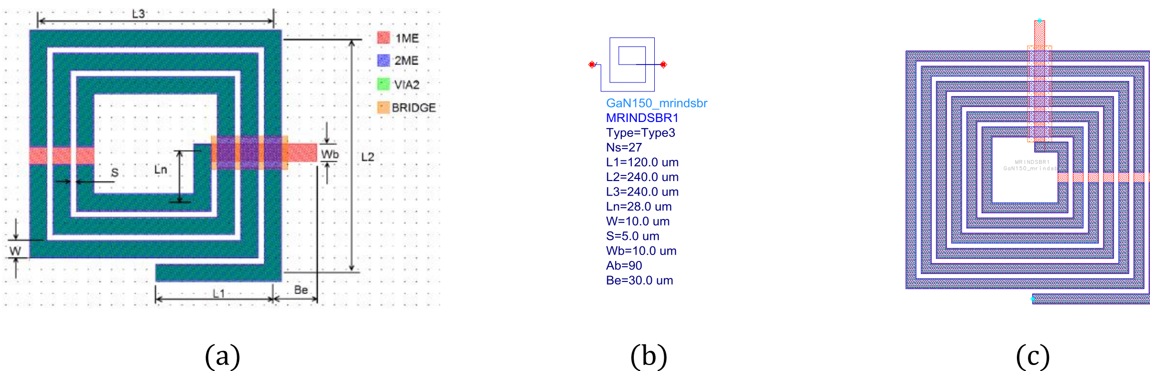


Figure 3-10: (a) Sizing; (b) Schematic model; and (c) layout model of GaN150 spiral inductor

Inductance for different inductor sizes and the real impedance of a spiral GaN150 inductor varying in the number of turns over frequency is presented in Figure 3-11. As the number of turns increases, the inductance peaks at a lower frequency with higher inductance value. Figure 3-12 shows a plot of quality factor using Equation 3.7 and shows that Q is narrow for higher number of turns.

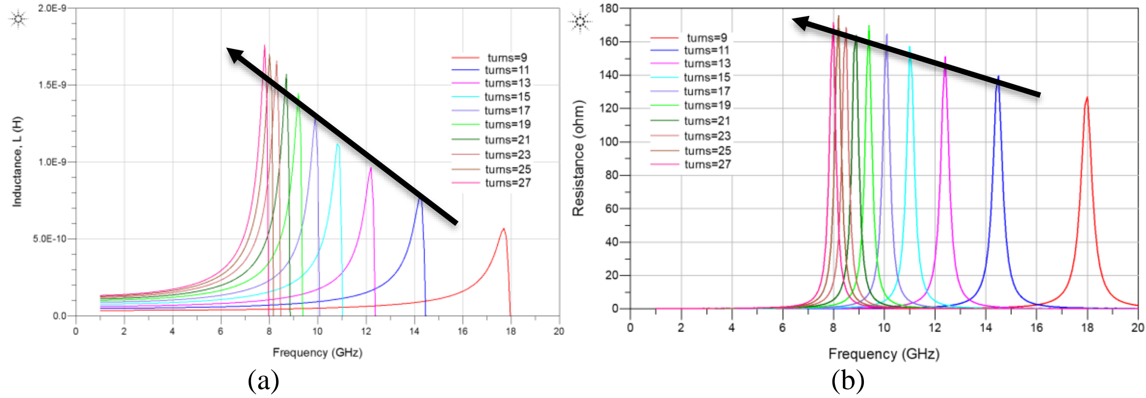


Figure 3-11: (a) Inductance vs. Frequency; (b) Resistance vs. Frequency for different turn values

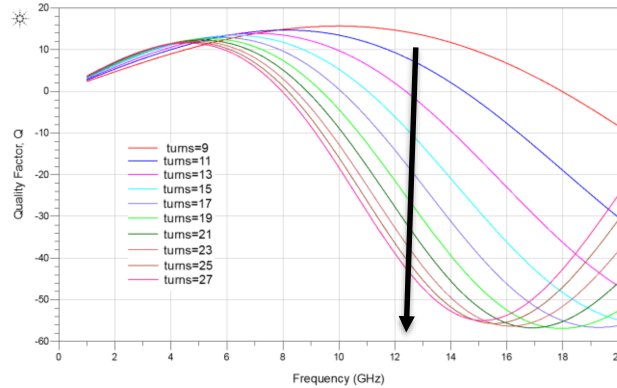


Figure 3-12: Quality Factor vs. frequency for different turn values

3.3 SPST RF Switch

In the following sections, a SPST switch configuration using GaN150 from NRC is described. The objective of this section is to simulate a single FET switch and identify insertion loss, isolation, return loss, 1 dB compression point, OTOI points and IIP_3. The frequency bands of interest are L, S, C, and X.

3.3.1 Single FET Series Switch

The SPST is a basic configuration of RF switches. In this work, a SPST is designed using GaN FET. Its schematic is displayed in Figure 3-13.

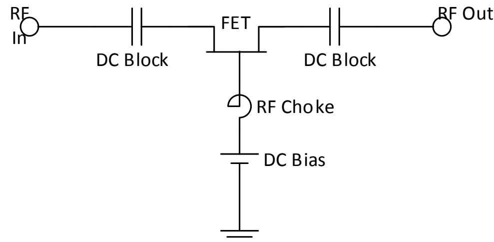


Figure 3-13: Topology of single FET switch

Single series GaN FET as a switch gives relatively low insertion loss and high isolation. It works such that FET between two ports are intended to have low insertion loss between them. This is because only the FET drain to source distance is recognized for RF transmission and only R_{ON} is the effective loss. A limitation of this design is that the isolation may not be adequate when implemented in part of a larger topology, which may lead to poor SNR or increased RF leakage because of the equivalent FET models. Isolation degradation is due to the frequency dependency of C_{OFF} of the FET. As seen in Figure 3-14, in the OFF state case, the FET can be modeled by R_{OFF} in parallel with C_{OFF}, where R_{OFF} can degrade the isolation of the switch.

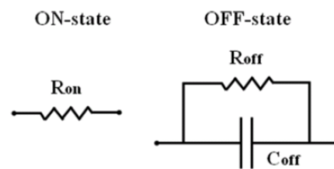


Figure 3-14: Simple model of FET in switch configuration

To obtain a better idea about how the above configuration works with GaN FET, GaN150 2 fingers FET models were used to perform simulations. Figure 3-15 illustrates the schematic diagram for a series GaN switch.

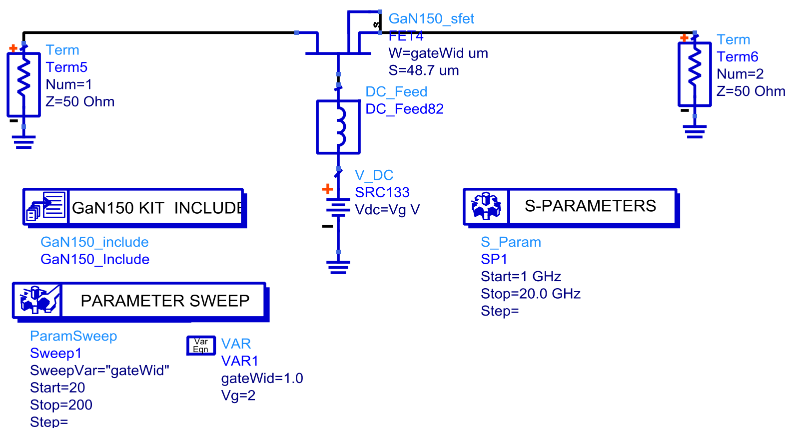


Figure 3-15: Simulation Setup for Series GaN SPST Switch

Ideal DC feed was used to supply the control voltage of -4 V for OFF state and 2 V for ON state. Simulations were conducted for different gate width for the FET to understand the performance parameters for different sized FET.

The simulations shown in Figure 3-16 display the Insertion Loss versus Frequency and Return Loss versus Frequency respectively. As mentioned in previous sections, when the gate width is increased, the R_{ON} decreases. As a result, the insertion loss decreases as well. In the simulation, the lowest insertion loss of -0.72 dB was obtained for 2x200 µm and the highest insertion loss of -5.43 dB is obtained for the device sized 2x20 µm. The response for insertion loss for all simulated frequencies of 1.5, 3, 6, and 10 GHz provides similar results.

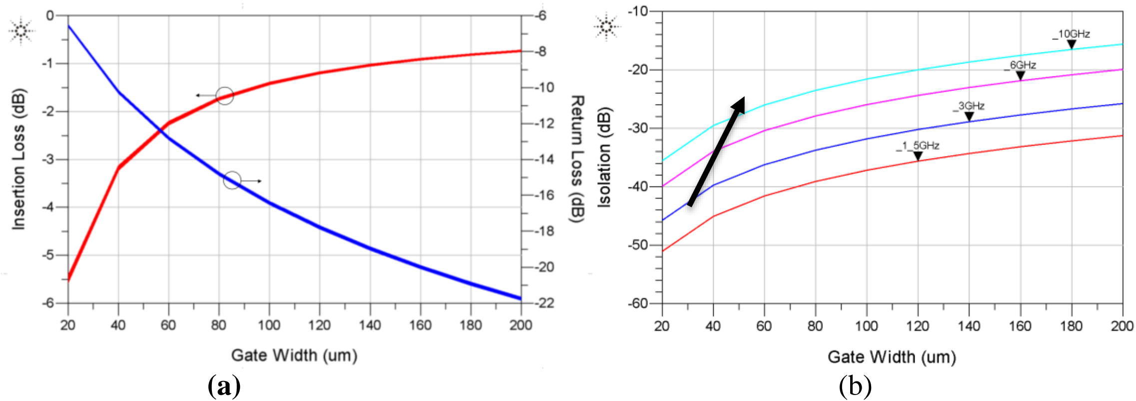


Figure 3-16: (a) Simulation of Insertion and Return Loss; (b) Isolation versus Gate Width for Single GaN FET RF Switch versus FET Gate Width

For the return loss plot in Figure 3-16, the response appears to be improving independent of the frequency when gate width is decreased. Isolation degrades as the gate width of the FET is increased and when it operates in higher frequencies. This is an expected result as increasing the FET gate width would increase C_{OFF} which; thereby, resulting in poorer isolation.

In Figure 3-17 (a), it can be seen that as the FET size increases, its 1 dB compression point increases as expected due to larger power handling capabilities from larger FETs. The 1 dB compression point of a 2x20 µm FET is 21 dBm, 2x110 µm is 36 dBm and 2x200 µm is 42 dBm. Although, series FET switch configuration has been shown to generate good results, in order to achieve higher levels of isolation, a shunt FET needs to be analyzed which typically provides a higher level of isolation to RF switches. Figure 3-17 (b) shows the OTOI point versus input power.

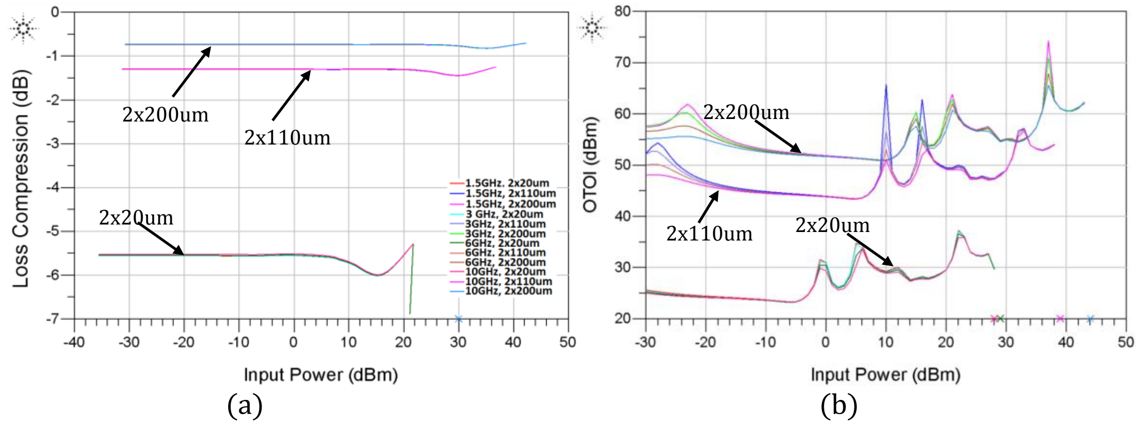


Figure 3-17: (a) Series SPST Gain/Loss vs Input Power; (b) Output Third Order Intercept Point versus Input Power over L, S, C, and X band

Depending on the mode of switch operation, ON or OFF, the non-linearity for different mechanisms effects a FET. For ON state switch, the non-linearity is mainly contributed by R_{ON} and is parasitic. For OFF state switch, the linearity is influenced by C_{OFF} and is also parasitic [54].

In this section, a series only single FET RF switch was examined. From the analysis, it can be concluded that, larger FET sizes have better insertion loss, and power handling capabilities; however, degrades the isolation and return loss of the switch. The performance of the switch was independent of the frequency of operation except isolation, where lower frequencies have better results compared to higher frequencies.

The following section will discuss a shunt switch topologies composed of a single transistor and transmission line in order to evaluate its switch performance.

3.3.2 Single FET Shunt Switch

The switch architecture of a shunt FET SPST switch is displayed in Figure 3-18. It is composed of a shunt mounted FET with a series λ/4 transmission line in its design.

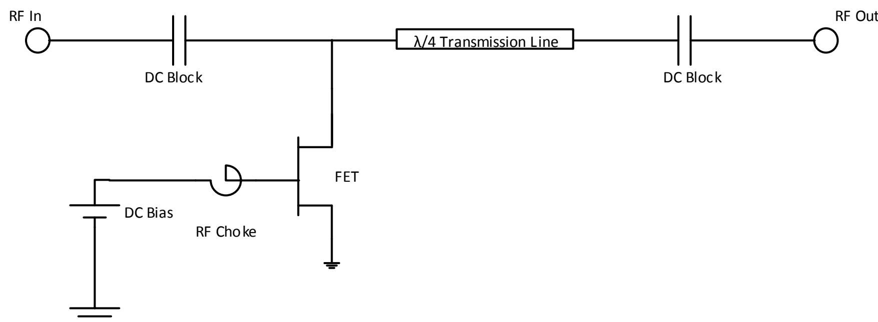


Figure 3-18: Shunt GaN SPST Switch Design

This configuration intends to provide improved isolation. However, shunt configured FET switches may have a narrow bandwidth because of the use of quarter wave transmission lines. The quarter wave line will transform the short circuit to an open circuit (90° transform). Therefore, when the FET is OFF, RF signal delivers an open circuit. Similarly, when the FET is ON, the RF signal sees short to ground with λ/4 transmission line to short the RF signal to load. Despite its high isolation properties, this design has a drawback in that, when the frequency is changed from its center frequency, the λ/4 lines change in electrical length thereby, creating a mismatch.

Shunt switch configuration was simulated using NRC GaN150 kit. The schematic used for this task is displayed in Figure 3-19. Table 3-4 shows GaN150 substrate parameters which are used to calculate the transmission line dimensions [47].

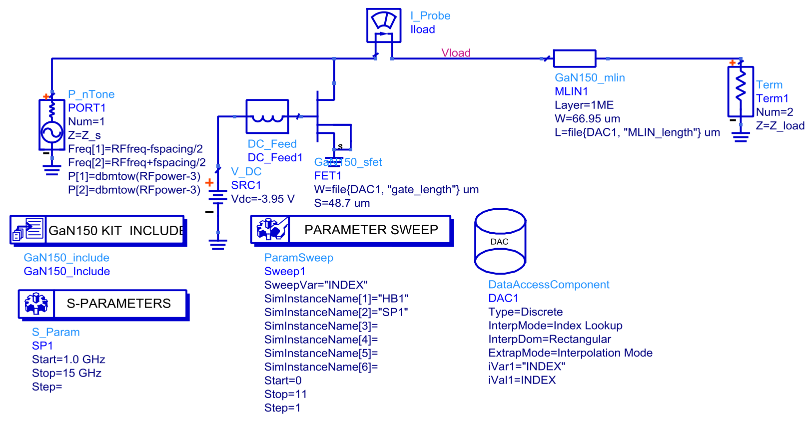


Figure 3-19: Simulation setup for Shunt GaN SPST Switch suing NRC GaN150 model

The quarter wave line was calculated using the LineCalc tool in ADS with the specific properties are outlined in Table 3-4, while the associated dimensions of λ/4 lines are presented in Table 3-5.

Table 3-4: MSUB parameters for NRC GaN 150

Parameters	Value
Substrate Relative dielectric constant (ε_r)	10
Relative permeability	1
Substrate Thickness (H)	75 μm
Metal thickness (T)	5 μm
Conductor conductivity (Cond)	4.1e7
Electrical impedance (Z_0)	50 Ω
Degree	90°

Table 3-5: Dimensions of λ/4 M1 MLIN for shunt configured switch

Frequency	Dimensions (width x length)
L Band (1.5 GHz)	66.97 x 19764.90 μm
S Band (3 GHz)	66.97 x 9880.97 μm
C Band (6 GHz)	66.95 x 4938.36 μm
X Band (10 GHz)	66.91 x 2960 μm
X Band (10 GHz)	66.91 x 2960 μm

As previously mentioned, shunt configuration has a significant drawback due to the dimension of λ/4 line. The electrical length of RF bands L, S, C, and X are calculated and shown as a dimension for transmission lines for 50 Ω with 90° shift. As the lengths for lower frequencies are very large, they may not be a cost effective way to recognize a switch in shunt configurations. Figure 3-20 displays the results obtained for isolation varying gate width for L, S, C, and X band. FET in ON state is supplied with a gate voltage of 2 V, while the FET OFF state is created with V_{GS} of -4 V.

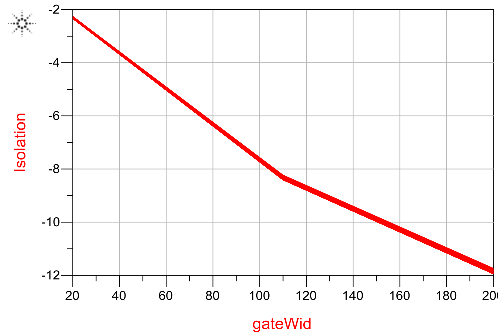


Figure 3-20: Isolation vs Gate Width of NRC GaN150 varying frequency in Shunt RF Switch Configuration

Gate width of the FET appears to impact the isolation of the switch. Larger devices provide higher isolation since R_{ON} is lower which provides an easy path for signal to ground. For all RF bands of interest in this work, isolation is within -11.8 to -12.8 dB as shown in Figure 3-20. Although, the shunt FET switch was supposed to give higher isolation levels than series FET configuration, the GaN150 FET model proved not to be as impressive when it was used in shunt configuration. This behavior is frequency independent.

In Figure 3-21, Figure 3-22, and Figure 3-23, simulations are conducted from 1 to 15 GHz for different gate widths with individual shunt switch based on frequency of operation.

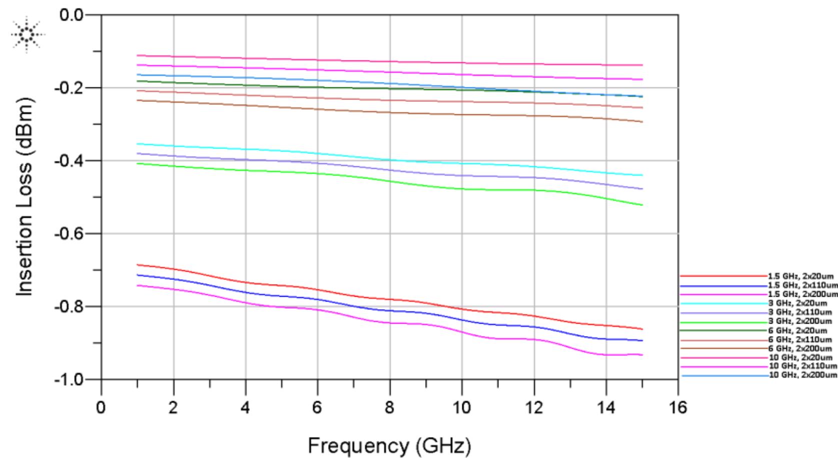


Figure 3-21: Insertion loss versus frequency for shunt switches with varying FET sizes and λ/4 MLIN

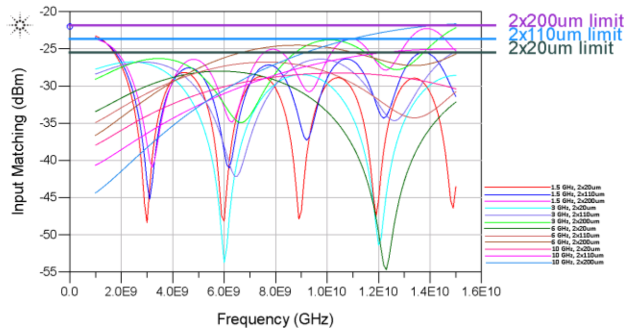


Figure 3-22: Input Return Loss versus frequency for shunt Switch

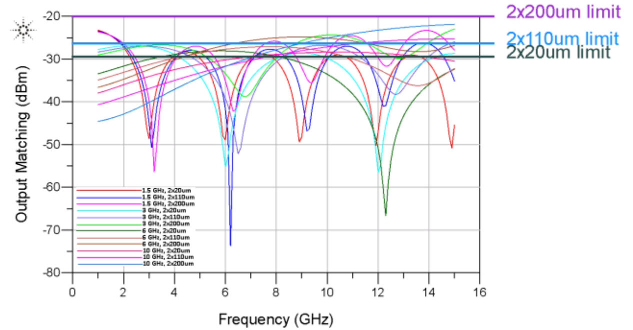


Figure 3-23: Output Return Loss versus frequency for shunt Switch

As displayed in Figure 3-21, insertion loss is preferred for switches configured at higher frequencies with smaller gate width. The effect of the quarter wave transmission line is apparent in the input and output return loss versus frequency plots above. Since the switch configurations are optimized for a single frequency operation due to λ/4 line, the return loss plot ripples are based on the electrical length of the quarter wavelength. The input and output return loss is below -20 dB as can be seen from Figure 3-22 and Figure 3-23. However, the same periodical behavior is observed due to the quarter wave transmission line. Figure 3-24 shows the Loss compression and OTIOI versus Input power varying FET sizes of 2x20, 2x110 and 2x200µm.

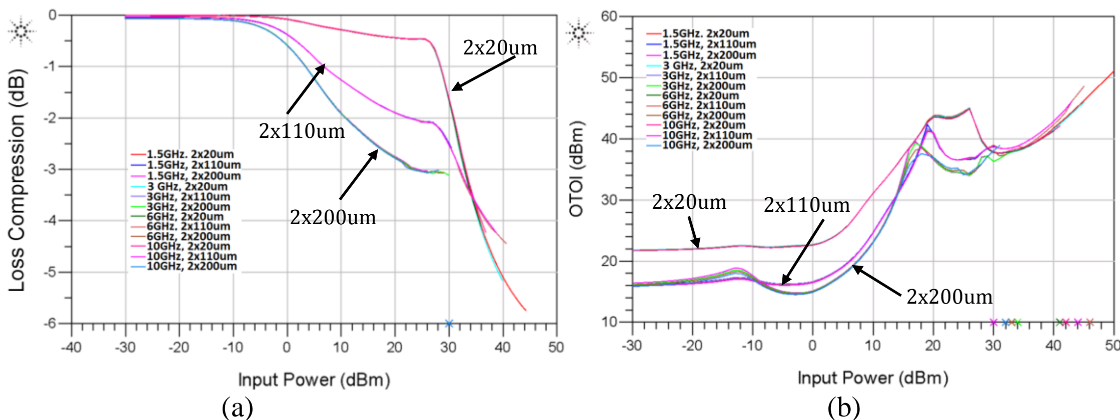


Figure 3-24: (a) Gain vs Input Power of GaN Shunt Switch; (b) OTOI vs Input Power of GaN Shunt Switch

These switches are found to have high power handling capabilities. As seen in Figure 3-24, smaller FET sizes in shunt configuration for improved power handling capabilities are preferred.

In this section, a single FET shunt switch has been evaluated. The power handling, insertion loss, and return losses were better for smaller sized FET. The distinction between isolation and insertion loss for series and shunt switch can be improved by using a combination of series FET and a shunt FET in a switch configuration. This is known as series-shunt FET switch configuration, which will be discussed in the following section.

3.3.3 Series-Shunt SPST Switch

Series-shunt GaN SPST topology is aiming to have insertion loss characteristics of the series GaN FET switch and isolation of shunt GaN FET configuration. The circuit diagram is given in Figure 3-25.

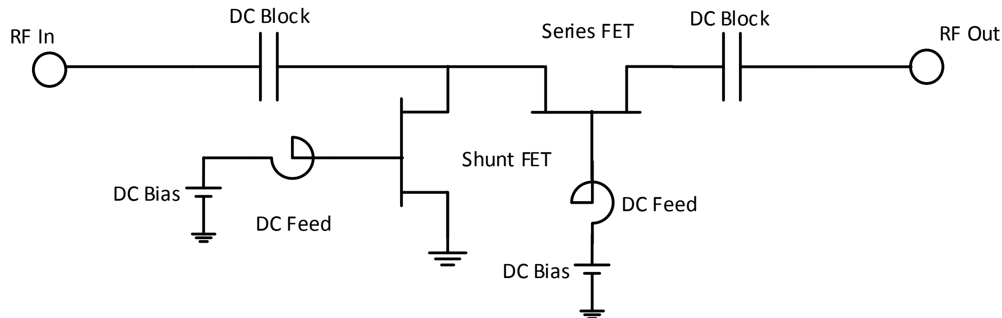


Figure 3-25: Series-Shunt GaN FET Switch Design

When a switch is in the ON state, series FET is supplied with 2 V at the gate for it to be in the ON state, while the shunt FET is choked with -5 V at the gate so that power is not lost. On the other hand, for the series-shunt switch to be in the OFF state high isolation is required; the series FET attenuates the signal with a bias voltage of -5 V and shunt FET is shorted with 2 V gate bias. Figure 3-26 shows the schematic diagram of an SPST switch in series-shunt configuration where FET1 is in series and FET2 is in shunt.

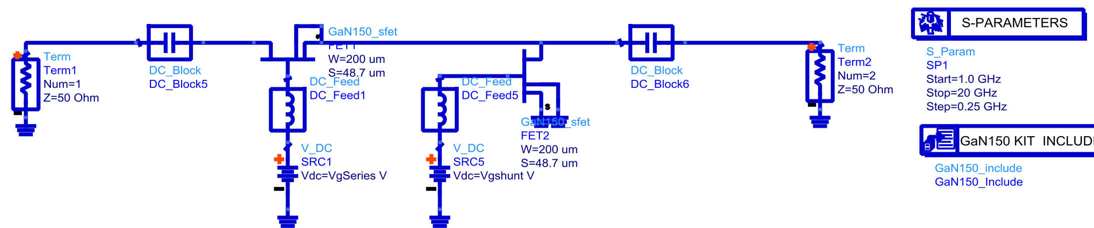
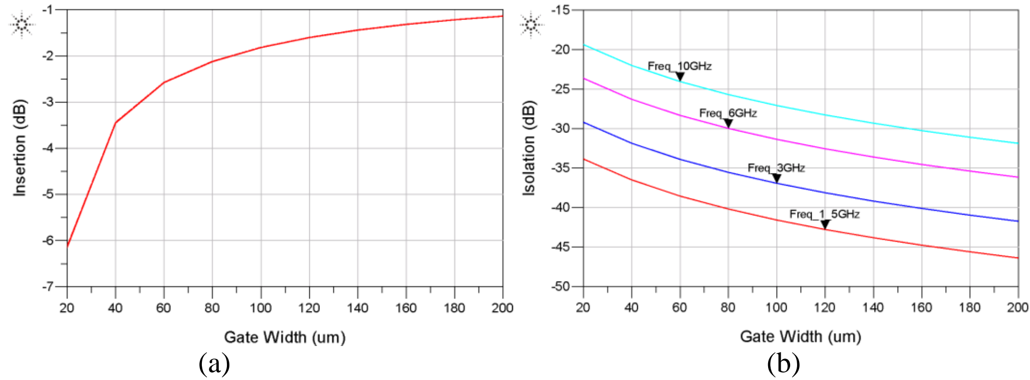


Figure 3-26: Schematic model of Series-Shunt SPST switch using NRC GaN150 model

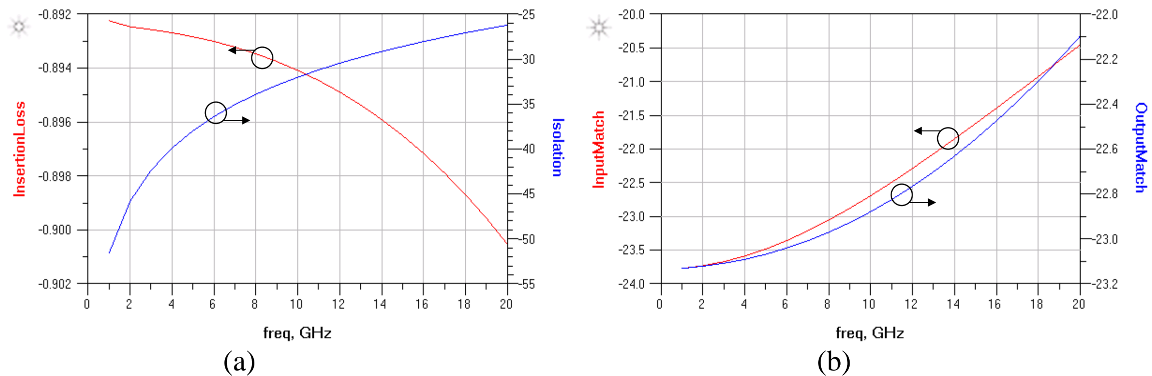
Simulation results of series-shunt SPST switch is displayed in Figure 3-27. The FET gate width is swept from 2x20 to 2x200µm and for isolation simulation, the series FET is kept at a constant width of 2x200µm while shunt FET was varied from 2x20 to 2x200µm.



(a) (b)

Figure 3-27: (a) Insertion loss versus GaN FET gate width; (b) Isolation versus GaN FET gate width

From Figure 3-27, the insertion loss simulation shows frequency independent behavior. Insertion loss fairs much better when series and shunt FET are of 2x200 μm. Isolation is better for lower frequencies and when gate widths are at their largest of 2x200 μm. As a result, in series-shunt configuration, isolation is optimum using higher FET sizes. The tradeoff between the two parameters must be considered for different applications. For the following simulation of series-shunt topology shown in Figure 3-28, 2x200 μm FETs are used.



(a) (b)

Figure 3-28: (a) Insertion Loss and Isolation versus Frequency; (b) Input and Output Matching versus Frequency of GaN Series-Shunt SPST using 2x200 μm NRC GaN150 FET model

By having a series-shunt configuration, a good combination is achieved in terms of insertion loss and isolation. Input and output return loss is also well below -20 dB. Figure 3-29 (a) shows the 1dB compression point and Figure 3-29 (b) shows OTOI point of a series-shunt switch varying shunt FET of 20, 110 and 200μm.

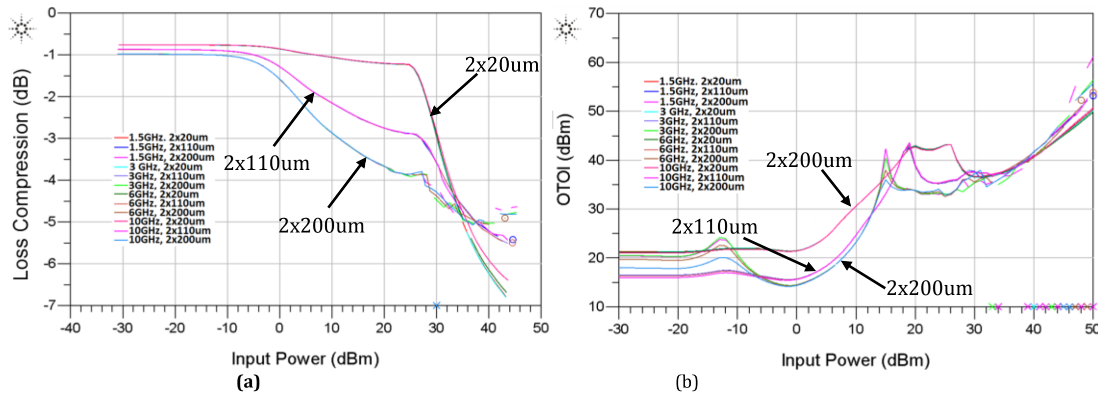


Figure 3-29: (a) Series-Shunt Switch Gain vs Input power; (b) Series-Shunt Switch OTOI vs Input power

A series-shunt configuration for large signal simulation of shunt FET provides an input referred 1dB compression point of 28 dBm, 8 dBm, and 4 dBm for 2x20, 2x110 and 2x200µm gate width respectively. From Figure 3-29 (a), it can be seen that the larger shunt FETs significantly degrade power handling capabilities of the switch compared to series only switch. This is because for ON state switch operation, larger shunt FET (in OFF state) has larger capacitance, which in turn allows more signal to be grounded.

3.3.4 Conclusion

In this section, NRC GaN150 FET was used to form a basic structure of RF switch. Series FET, Shunt FET, Series-Shunt FET were presented and simulation results were analyzed. These basic forms can be used in complex switch configurations based on the target application. Table 3-6 compares different topologies for GaN SPST RF switches all using 2x200 µm FETs.

Table 3-6: GaN SPST 2x200 µm Comparison of different topologies

	L - Band			S - Band			C - Band			X - Band		
	Series	Shunt	Series-Shunt	Series	Shunt	Series-Shunt	Series	Shunt	Series-Shunt	Series	Shunt	Series-Shunt
Insertion Loss (dB)	0.74	0.66	0.89	0.89	0.33	0.89	0.89	0.17	0.89	0.89	0.11	0.89
Isolation (dB)	31.27	12.74	48.23	25.78	12.14	42.35	19.95	11.88	36.39	15.62	11.94	32.01
IRL (dB)	-21.67	-35.31	-23.75	-23.67	-33.08	-23.67	-23.36	-28.24	-23.36	-22.7	-23.68	-22.69
ORL (dB)	-21.67	-37.21	-23.13	-23.11	-39.76	-23.11	-23.04	-35.85	-23.04	-22.88	-26.24	-22.88
1dB Compression (dBm)	45.2	5.6	42.5	45.2	5.6	42.5	45.2	5.6	42.5	45.2	5.6	42.5

In summary, the best insertion loss was found for a series switch FET with 2x200 µm and improved isolation was observed for shunt FET with 2x200 µm. Further tradeoffs need to be considered for a given application.

3.4 Single-Pole Double-Throw RF Switch

Single-pole double-throw (SPDT) switching elements are the key components of T/R modules in the performance of various communication link schemes. SPDT switches are used to selectively couple signals between two RF ports, where it provides a simultaneous high isolation to the inactive path and low insertion-loss for the active path. A typical application of an SPDT is T/R RF switch is shown in Figure 3-30. In Figure 3-30, the switch is selecting between the transmit path which is connected to a PA, and a receiver path through an LNA. Fundamentally, an SPDT switch is constructed by configuring two SPST switches, as shown in Figure 3-31.

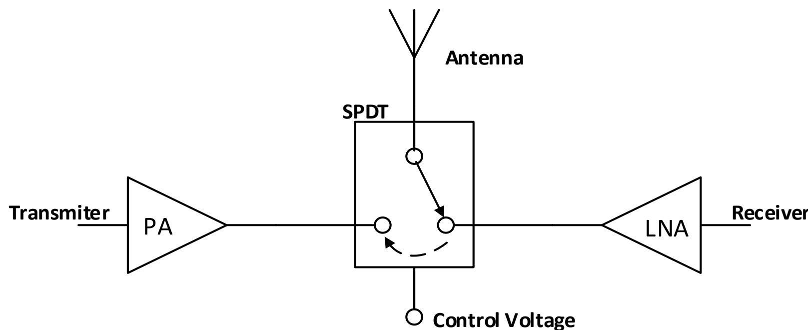


Figure 3-30: SPDT application as a T/R switch in a transceiver

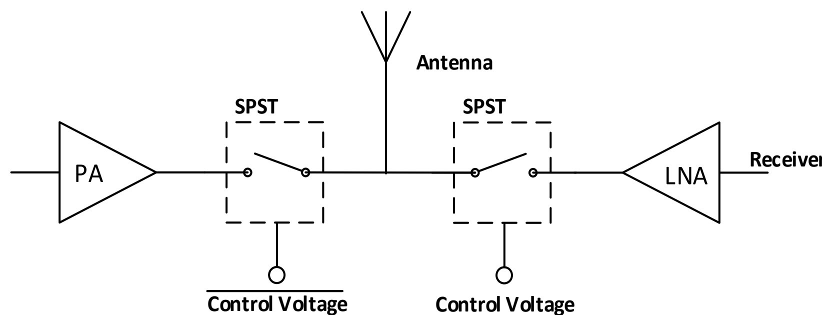


Figure 3-31: SPDT switch composed of two configured SPST switches

The activated SPST switch provides a low insertion loss and good return loss usually matched with 50 Ω. The inactive switch should provide high isolation and high input impedance, ideally providing a perfect open circuit.

In this section, a SPDT RF Switch is presented. Firstly, an SPDT will be configured based on SPST analysis carried out in the previous section. A full SPDT layout will be presented and full EM-simulation will be analyzed for L, S, C, and X band operations. Lastly, the SPDT design in this work will also be compared with other commercially available switches. The target specifications of the switch are extracted from TriQuint TGS2352 SPDT switch. Table 3-7 shows the key features of TriQuint's SPDT switch, which will be the target performance parameters of this work for SPDT switch.

Table 3-7: TriQuint TGS2352-2 SPDT Switch Specifications [55]

Device	TriQuint 0.25µm SiC production process
Input power	Up to 20 W
Insertion Loss	< 1 dB
Isolation	-35 dB typical
Return Loss @ 10 GHz	< -15

3.4.1 Design

A high wideband isolation and low insertion loss for SPDT switch is required for suitable operation at different frequency bands. Considering this factor, a wideband T/R switch has been designed and is currently in fabrication. The target requirement for GaN SPDT switch involves an insertion loss less than 1 dB, isolation better than 35 dB, and an input and output return loss better than -15 dB and up to 20W of power handling. From previous sections, a good balance of power handling, wideband, and small signal values were obtained from a series-shunt topology biased at -5 V for OFF state and 2 V for ON state. A series-shunt symmetrical SPDT topology was implemented to achieve the broadband performance.

Figure 3-32, is a single stage series-shunt configured SPDT. In this case, the SPDT is being used as a T/R switch. FET1 and FET2 forms the series-shunt configuration for the transmitter chain and FET3 and FET4 forms the series-shunt configuration for the receiver chain. The supply voltage for FET1 and FET3, and FET2 and FET4 are complementary and can be designed to operate using only one control voltage (either V_{ON} or V_{OFF}).

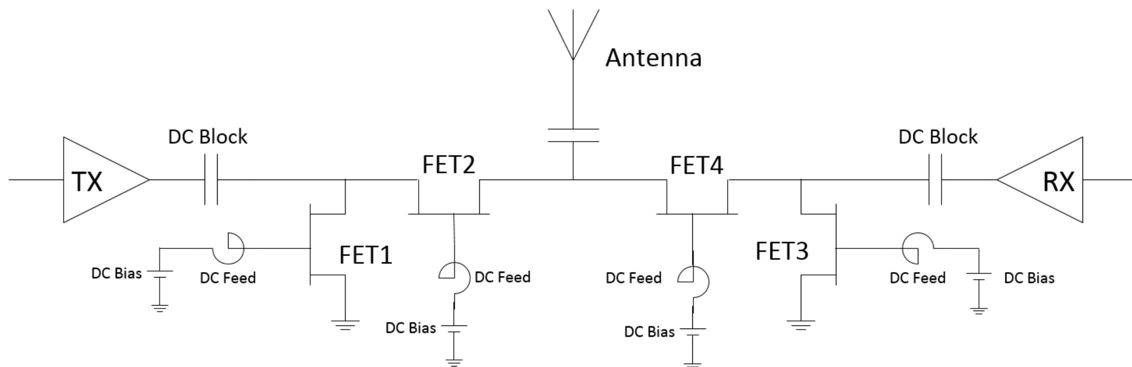


Figure 3-32: GaN150 Series-Shunt Configuration for SPDT Switch

From the previous section, the SPST series only switch does not meet the isolation criteria, while the shunt only switch is frequency dependent. As a result, the series only or shunt only switches are

not ideal for a broadband RF switch. Figure 3-33 illustrates the schematic circuit of a series-shunt broadband SPDT.

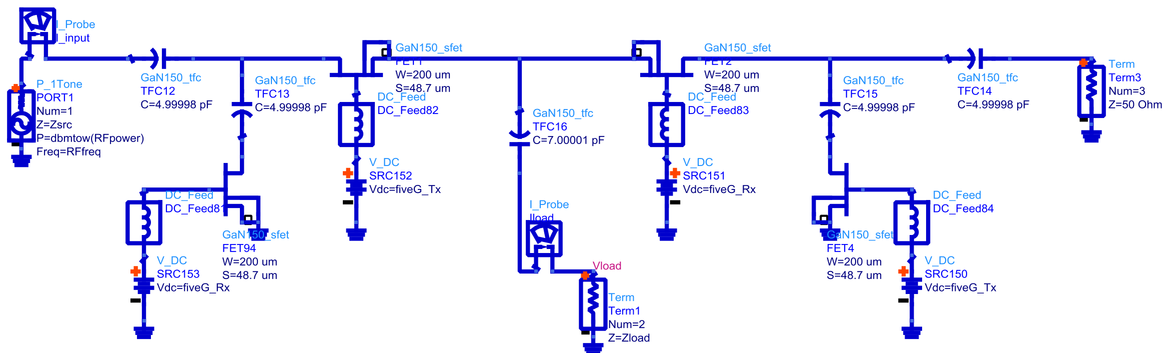


Figure 3-33: Schematic design of broadband SPDT

DC coupling capacitor for transmit and receive chain is 5 pF and 7 pF for output. As previously mentioned, FETs in Figure 3-33 can be implemented using single ON/OFF control voltage in a larger system. A complete layout of the SPDT is shown in Figure 3-34.

In Figure 3-34, the upper portion of the layout is connected to the receiver chain and the lower portion to the transmitter chain. The output to antenna port is on the right of the layout design. This allows for easy access to DC feed resistors, which were designed using a 3x100 µm nichrome resistors of approximately 1500 Ω. GaN MIM capacitors for coupling and matching. The signal path is designed using M1 layer and the width was kept constant at 38 µm consistent with the FET drain width to reduce any width change discontinuity. As for 90° bends, a curve trace is used to reduce any discontinuity due to bend. Transmitter and receiver ports are kept 380 µm apart to reduce RF leakage. The complete design size is 776x610 µm.

For the shunt FET, two Through Hole VIAs were used to short signal to ground. The VIAs are only on one side of the FET to reduce die space. Sources of the FET are connected via 20x80µm air bridges across the entire length of the FET to ensure a good connection as shown in Figure 3-36. Figure 3-35 shows the layout diagram of GaN150 air-bridge. The resistivity of the air-bridge is the same as that of the 2ME layer (9 mΩ/sq). To accurately model the impact of stray capacitance from the air-bridges, where 1ME crosses other metal layers, EM simulations were performed to account for both the parasitic edge and parallel plate capacitances. The current carrying capacity of an air-bridge is less than the landed 2ME, as the lack of thermal extraction to the substrate increases heat. This causes the current capacity to decrease as the length of the span increases; however, a nominal value of 6 mA/µm width is used for the air-bridges.

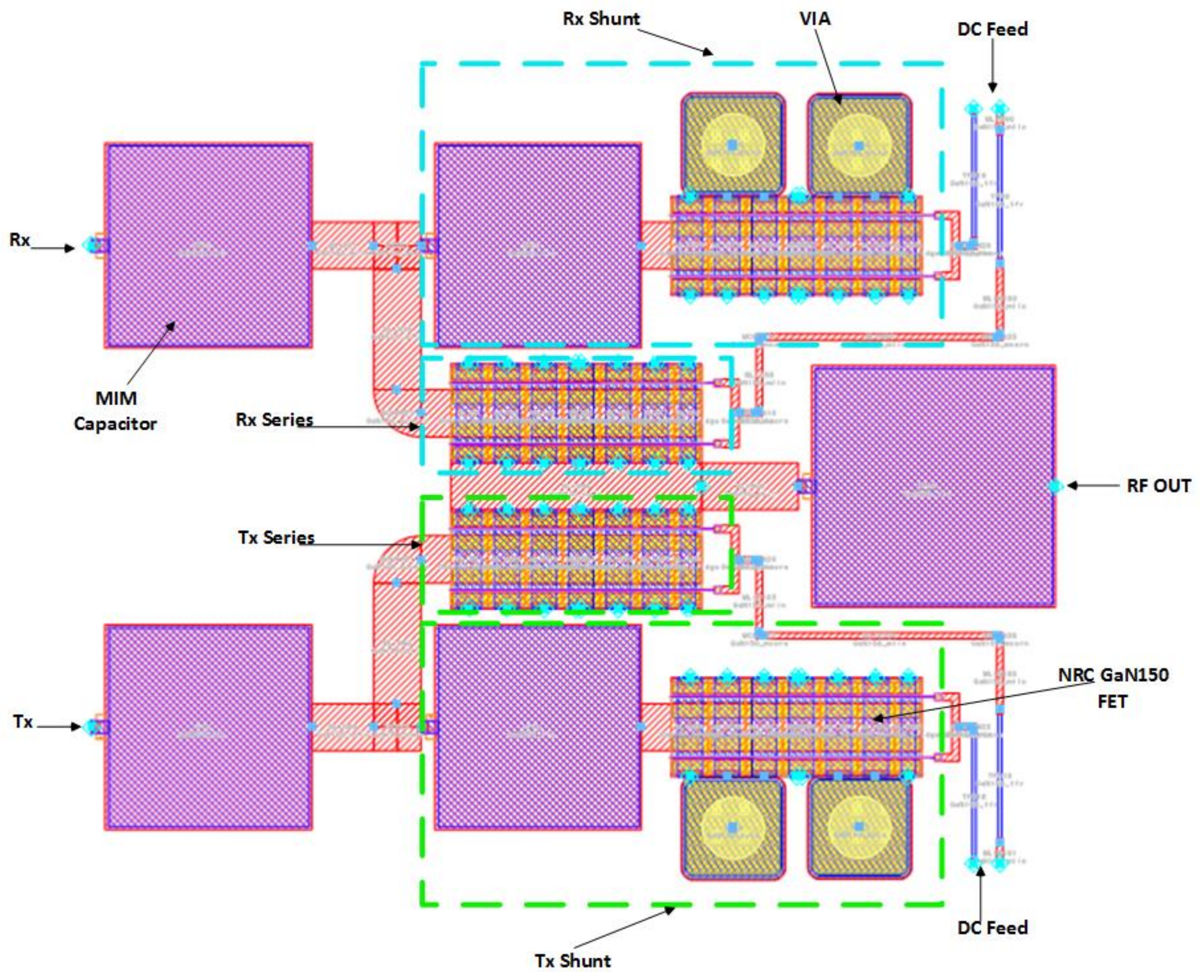


Figure 3-34: Complete layout of NRC GaN150 SPDT RF Switch

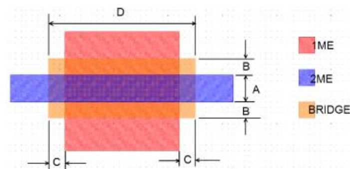


Figure 3-35: Layout of GaN150 air bridge

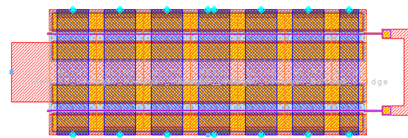


Figure 3-36: GaN150 FET source connections using air bridges

The layout driven schematic of SPDT is displayed in Figure 3-37. The NRC GaN150 kit is used to model the SPDT. As depicted in the SPDT layout, all signal traces are M1 layer.

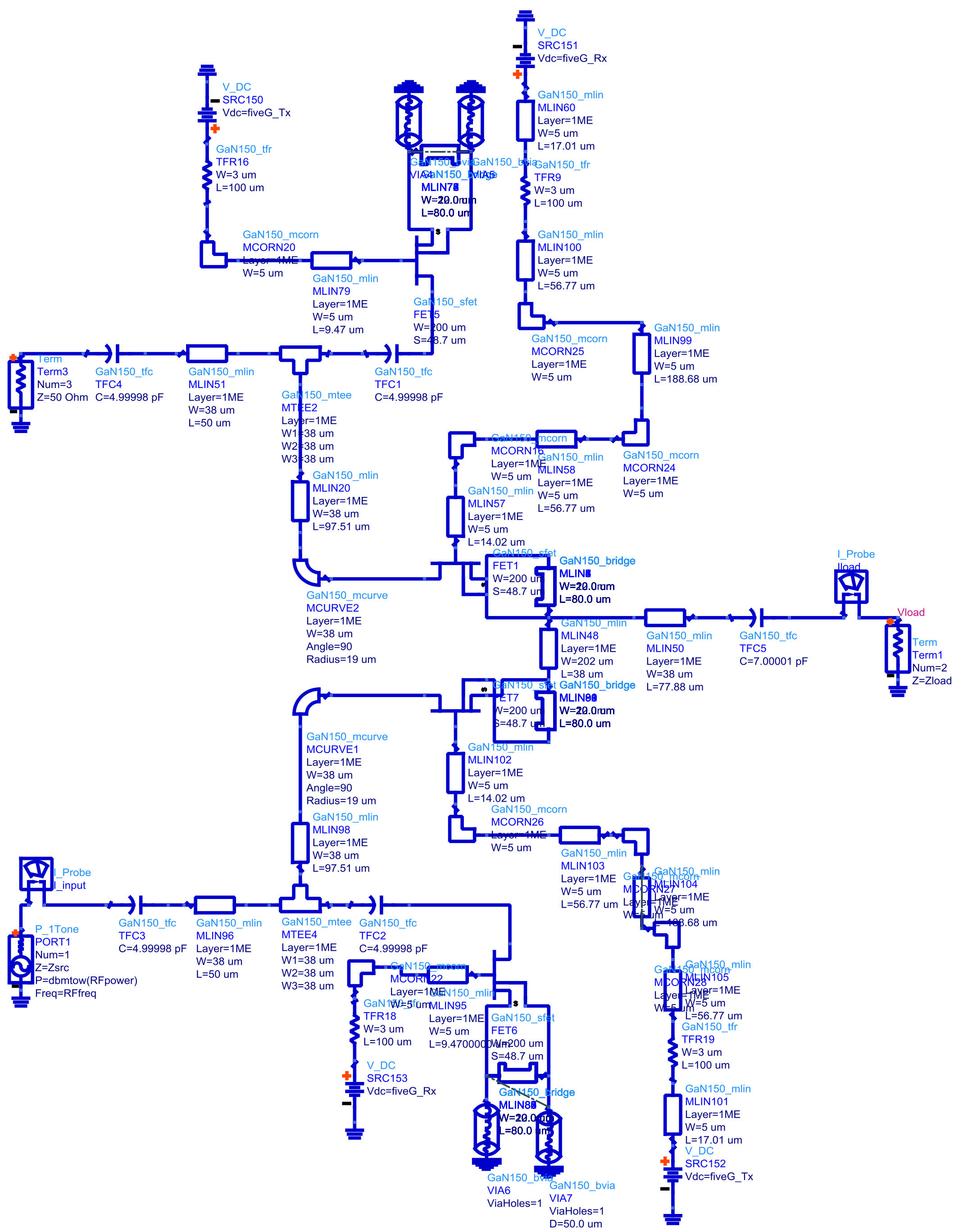


Figure 3-37: Layout driven Schematic of SPDT Switch

3.4.2 Results

Figure 3-38 shows EM-simulation results of the SPDT switch using series-shunt configuration. For ON-state the FET was biased at 2 V and for OFF state, -5 V is used.

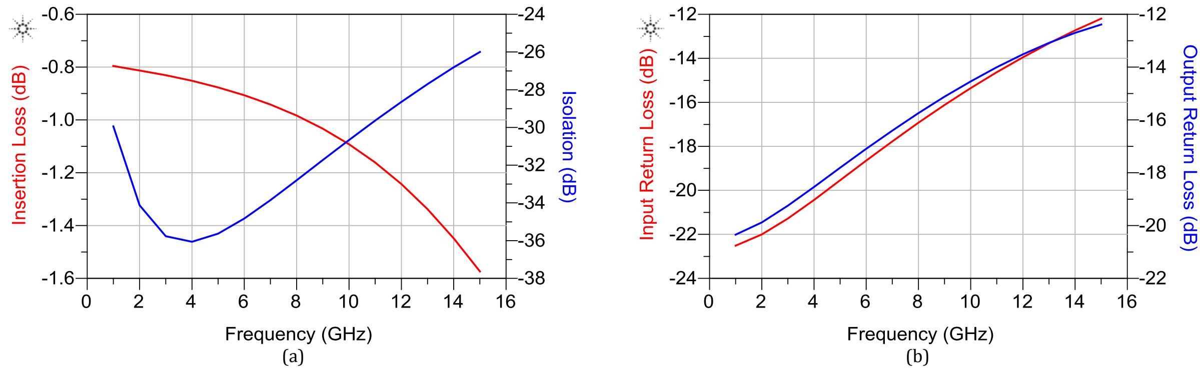


Figure 3-38: (a) Insertion and Isolation vs Frequency; (b) Return loss vs Frequency

The insertion loss for SPDT is better than 1.2dB from 1 GHz to 12GHz. The isolation of the SPDT is controlled over the frequency of interest with results better than 28 dB from 1 to 12GHz. The input and output matching is below -13.5 dB for frequencies lower than 15 GHz, but it increases with frequency. Figure 3-39 shows the Loss Compression and OTOI vs Input Power of SPDT when the switch is in the ON state.

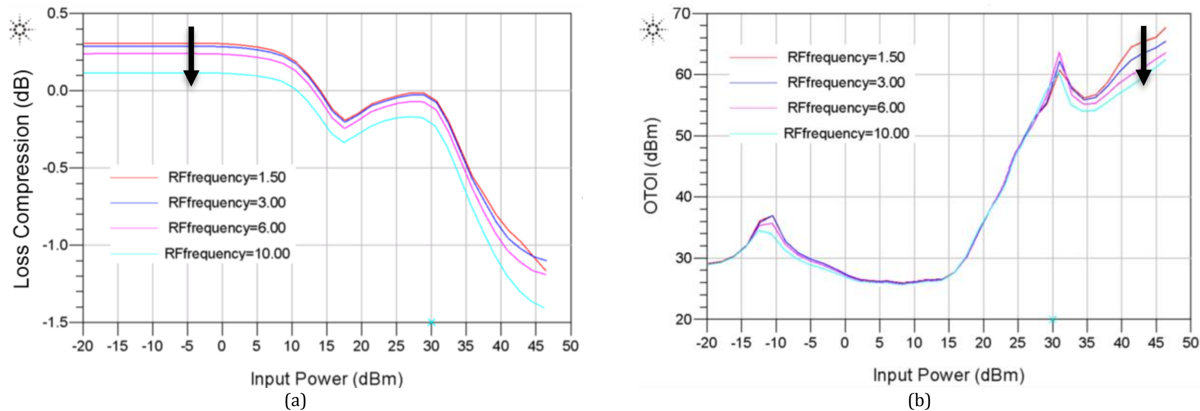


Figure 3-39: (a) Loss compression vs. Input Power; (b) OTOI vs. Input Power of SPDT Switch

According to Figure 3-39, the input referred 1dB compression point is greater than 36 dBm. Simulations for all four bands of interest were carried out; Figure 3-39 shows the OTOI points for all four bands of interest and can be seen that the switch have linearity for input power range from -20 to 45 dBm. Next, to determine IIP_3 of the switch, the first and third-order power lines are extrapolated as shown in Figure 3-40.

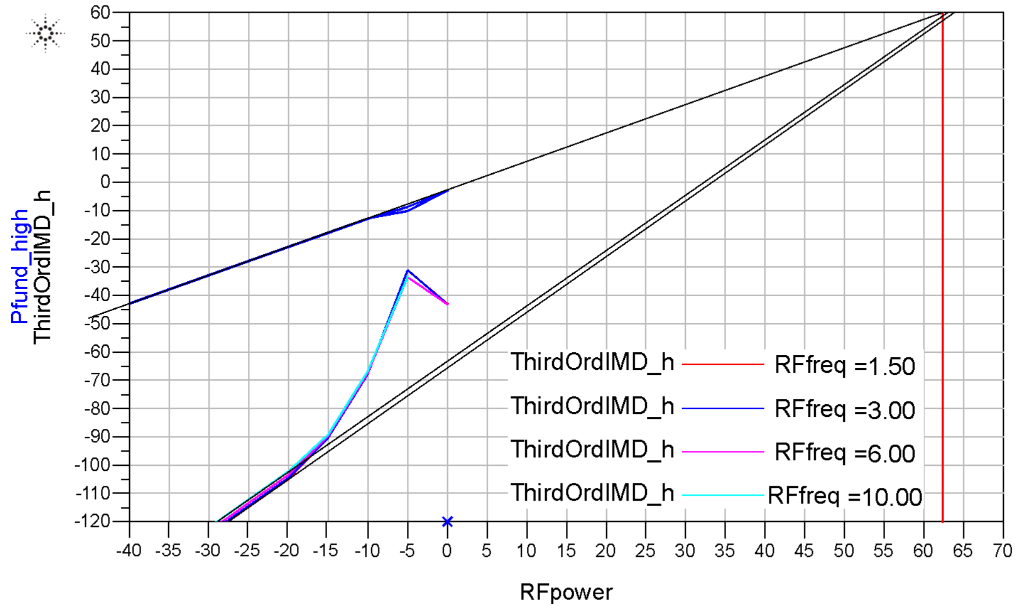


Figure 3-40: Determining IIP3 of SPDT switch

The IIP_3 for SPDT switch was found to be 62-63 dBm for all frequency bands of interest. Table 3-8 provides a summary of design SPDT switch parameters.

Table 3-8: EM Simulation results of design SPDT

Performance	L Band	S Band	C Band	X Band
Insertion Loss (dB)	0.82	0.83	0.90	1.09
Isolation (dB)	31.94	35.76	34.83	30.67
Input Return Loss (dB)	-22.11	-21.28	-18.65	-15.36
Output Return Loss (dB)	-20.62	-19.23	-17.10	-14.55
1-dB Compression	38.63 dBm	37.76 dBm	37.76 dBm	37.76 dBm
IIP_3	62 dBm	62 dBm	63 dBm	63 dBm

A comparative analysis between in market GaN SPDT is outlined in Table 3-9. In market devices are all based on 0.25µm GaN technology. This is the first broadband SPDT design implemented in a GaN 0.15µm technology to the author's knowledge.

Table 3-9: Comparison of SPDT (this work) for X band with in market switches

X Band Comparison	RF Lambda	Plextek 0.25µm GaN [56]	TriQuint's 0.25um GaN [55]	This work @ X-band
Insertion Loss (dB)	2.04	1.0	0.9	1.09
Isolation (dB)	21.69	40	33	30.00
Input Return Loss (dB)	-17.95	-18	-17	-15.36
Output Return Loss (dB)	-15.50	-	-17	-14.55
1-dB Compression	43 dBm	63 dBm	40 dBm	37.76 dBm
Area (mm2)	-	-	1.15 x 1.65	0.98 x 0.85

In the GaN150 SPDT in X-band operation, the insertion loss is slightly better than other commercially available devices being discussed. The isolation of the SPDT developed here was comparable to that of a TriQuint switch [54], but has a slightly higher output return loss; whereas, the 1-dB compression point is comparable to RF Lambda and TriQuint's SPDT. The occupied area of the SPDT in this work is comparable to that of the TriQuint.

3.5 Double Pole RF Switch

Most digital cellular systems have adopted a multi antenna design incorporating a T/R switch that connects to an antenna for transmitting or receiving circuit. For mobile devices, low insertion loss and high power double pole switches are indispensable as FET switches are advantaged with low power consumption, high speed switching, and simplified bias network [23]. In this section, a double pole switch is designed to exhibit a low insertion loss and high isolation. Extensive parametric analysis will be carried out for double pole single throw (DPST) and double pole double throw (DPDT) switches. The target double pole switch specific for this work is obtained from a MACOM GaAs MMIC Switch, MASWGM0001-DIE. The switch has operational frequency of 2.0 to 14.0 GHz, having an insertion loss of 3 dB, isolation of 40 dB, and 1 dB compression point of 25 dBm [57].

3.5.1 Design

In the conventional DPDT configuration, two SPDTs are used to connect any one antenna port to either transmitter or receiver. Such circuit arrangement increases the size of the switch and adds additional circuit requirements, which decreases the quality of the switch. This is outlined in Figure 3-41.

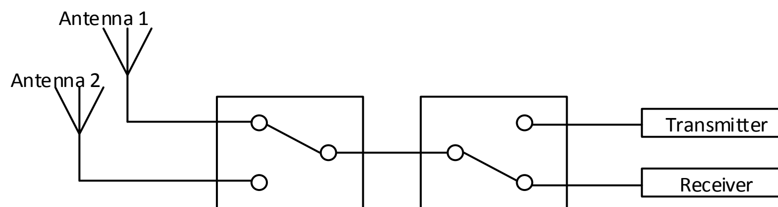


Figure 3-41: Conventional Configuration

The designed SPDT in this work enables an RF signal to pass only through one switch block causing a much lower insertion loss. The proposed DPDT topology has a diamond shaped structure with four separate paths as illustrated in Figure 3-42 [58].

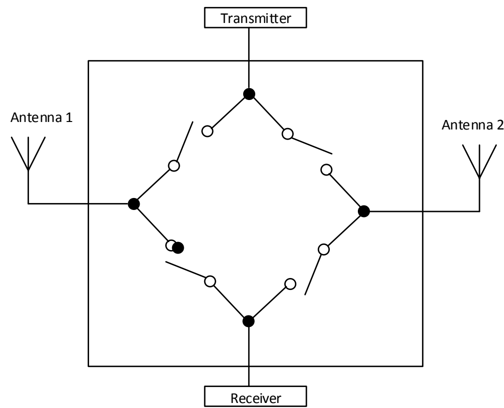


Figure 3-42: DPDT topology for this work

Using this structure allows the transmitter and receiver to access both antennas. This is beneficial as the diamond structure of the DPDT RF switch enables simultaneous use of both antennas by both transmitter and receiver. This topology serves as a 2x2 MIMO switch given enough isolation when simultaneously in operation. In the designed topology shown in Figure 3-43, a series 2x200 µm FET is used by having two shunt 2x100 µm FETs for each RF ports and antenna.

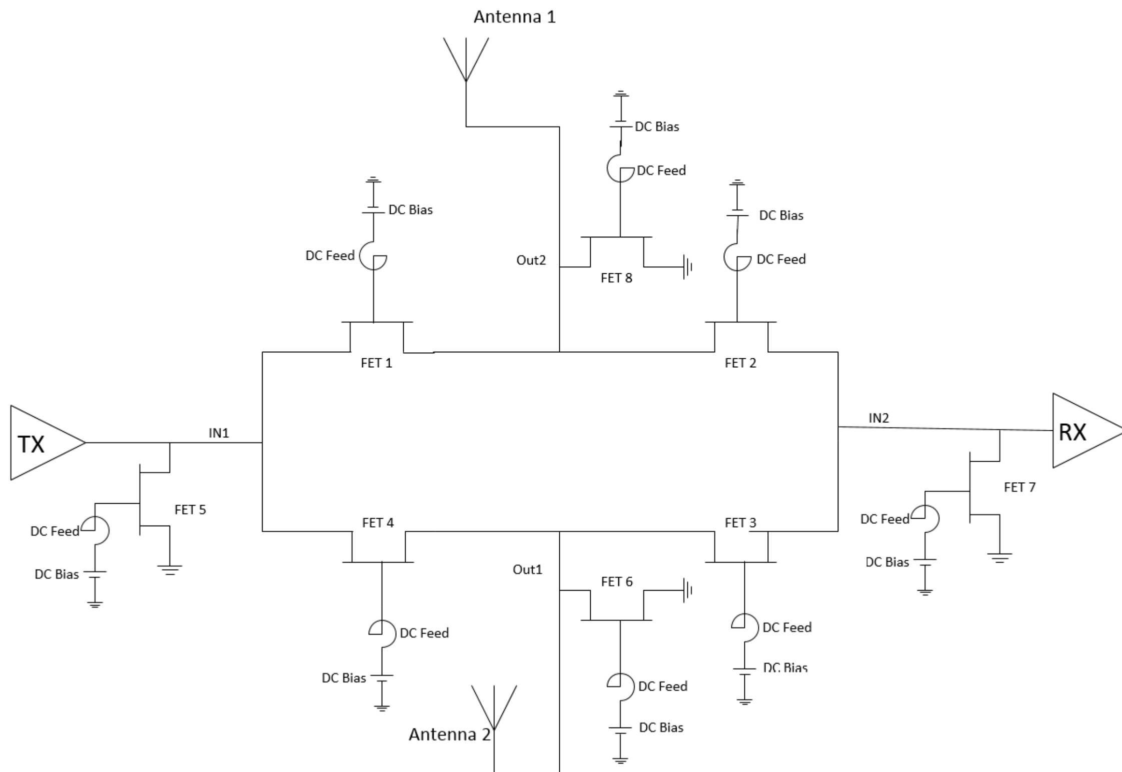


Figure 3-43: Schematic circuit of DPDT Topology

This gives a series-shunt configuration for each RF path which can be characterized to provide enough isolation for both chains. For TX to be directed to Antenna1, only FET1 is turned ON amongst

the series FETs; while FET5 and FET8 is turned OFF amongst the shunt FETs with the rest stagnant in the ON state. Since there are more pathways for RF leakage in this topology, FETs are biased to provide the best ON and OFF state for each FETs. Figure 3-44 shows the schematic diagram derived from the proposed broadband double pole switch layout.

Figure 3-44: Layout driven schematic of double pole

The bias of FETs is different for the various use of the double pole switches based on the number of throws. When only one RF path is operating, the switch is in DPST mode. When both paths are active, the switch is in DPDT mode.

Figure 3-45 shows the layout of the series shunt double pole switch. The design was made as compact as possible in order to minimize losses. It consists of two coupling capacitors at the RF I/O ports. Also, 3x100 μm nichrome resistors are used to provide the DC feed to gate the FET with a value of 1500 Ω. To maintain the proportionality of the design, each shunt FETs is divided into two 2x100 μm to provide a total of 2x200 μm. The total area of the series-shunt double pole switch design is 1.2 x 1.1mm.

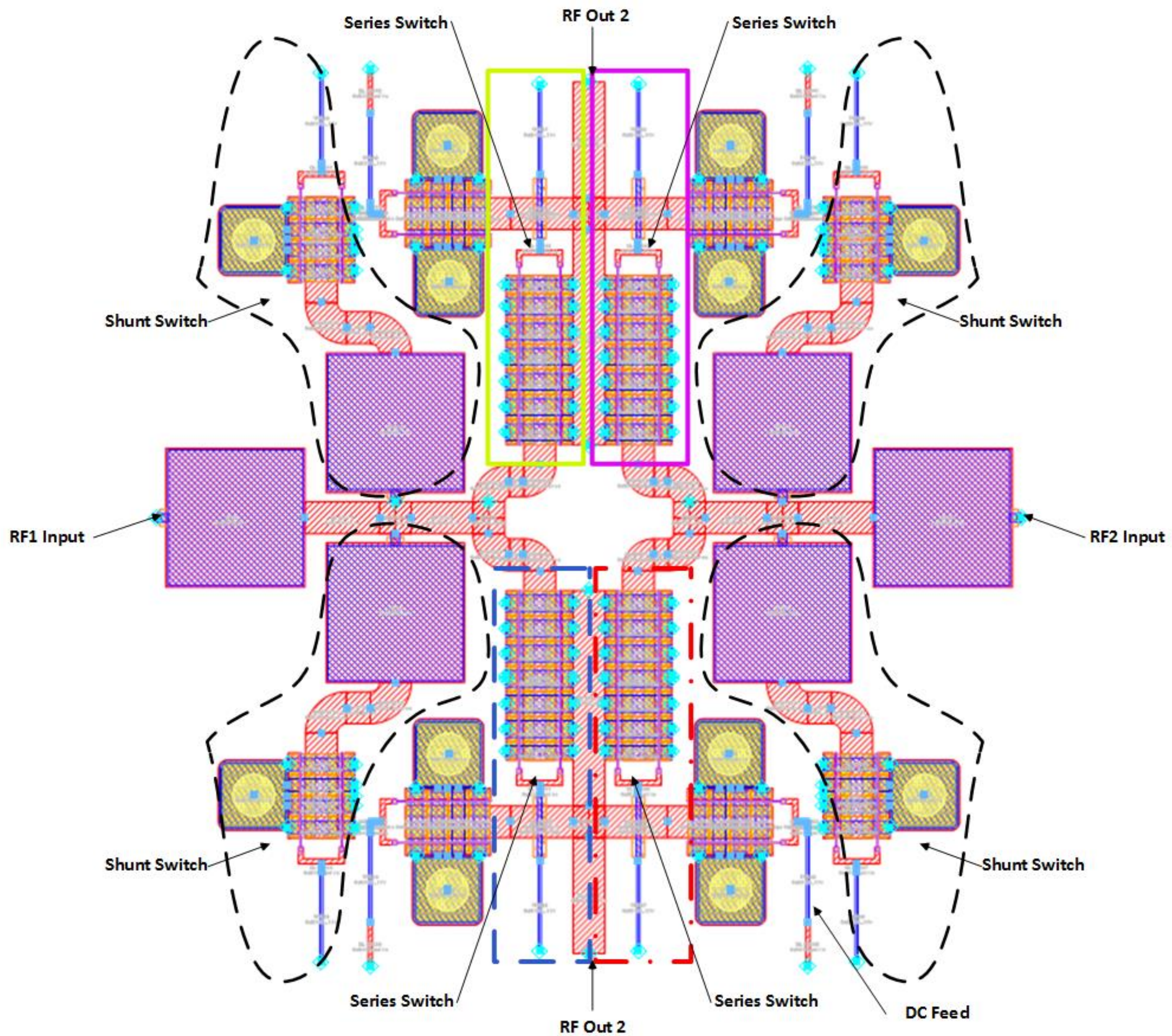


Figure 3-45: Layout of broadband double pole RF Switch using GaN150

3.5.2 Results

For DPST switch operation, only one RF path is active. Bias points of -5 V/2 V are used to obtain measurements. All analysis is conducted by performing EM-simulation using ADS. Figure 3-46 shows the insertion loss, isolation and return loss versus frequency of DPST.

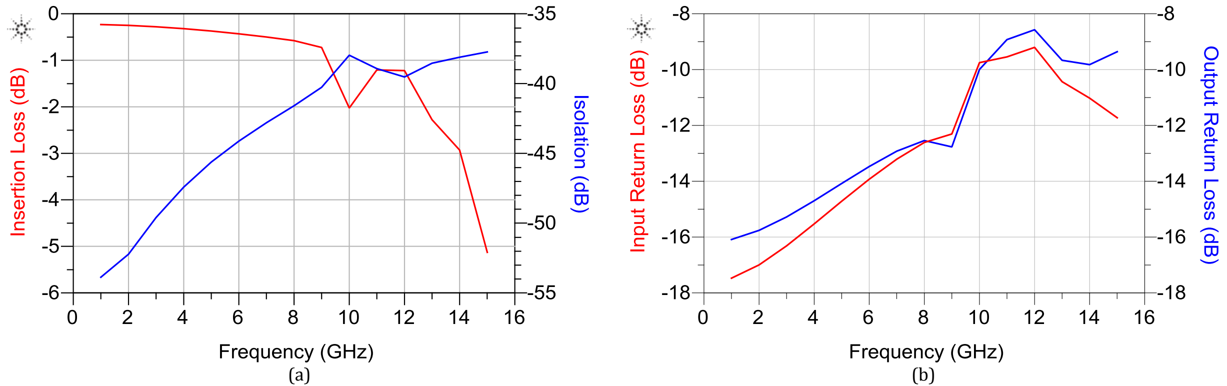


Figure 3-46: (a) Insertion loss versus Frequency; (b) Isolation versus Frequency of series-shunt DPST switch

For one active path, the insertion loss is less than 1 dB up to 9 GHz; whereas, the isolation for one active path is more than 38 dB for all frequency bands of interest to ensure good separation to reduce unwanted effects of crosstalk and leakage. The input and output return loss is better than 9 dB.

Figure 3-47 shows the Loss Compression versus Input Power of DPST and plot of OTOI versus Input power when the switch is in the ON state for all frequency bands of interest. The fundamental and IMD_3 plot to obtain IIP_3 is illustrated in Figure 3-48. Subsequently, Table 3-10 present a summary of switch parameters for a single active patch DPST switch.

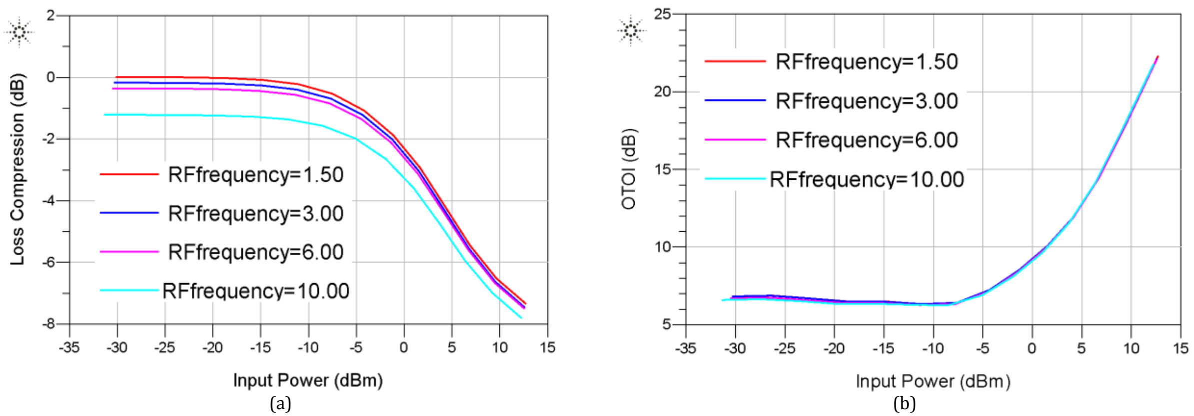


Figure 3-47: (a) Loss compression versus Input Power; (b) OTOI versus Input Power for DPST series-shunt switch.

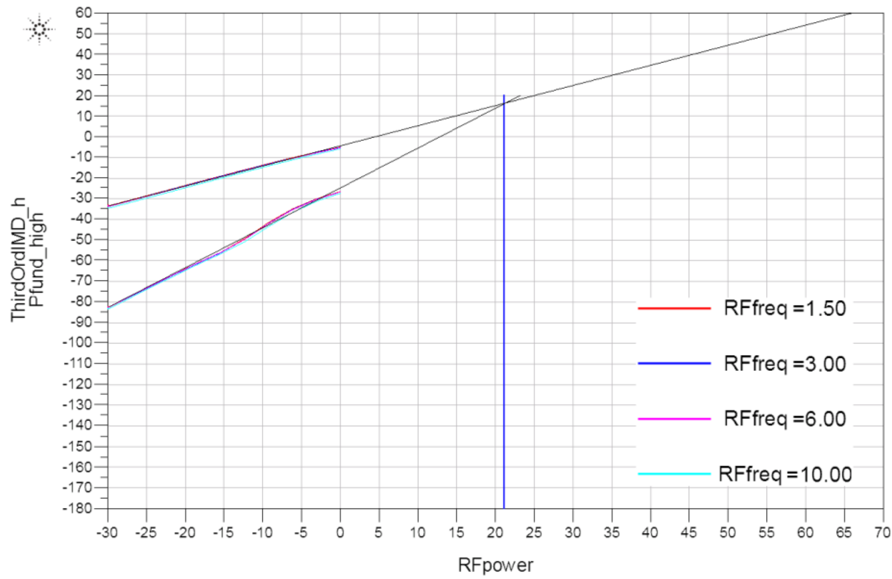


Figure 3-48: Determining IIP3 of series-shunt series-shunt DPST

Table 3-10: Simulation results of DPST design of this work

DPST	L Band	S Band	C Band	X Band
Insertion Loss (dB)	0.23	0.39	0.52	2.03
Isolation (dB)	53.83	50.21	43.23	37.87
Input Return Loss (dB)	-17.72	-16.73	-14.35	-9.84
Output Return Loss (dB)	-15.93	-15.32	-13.87	-10.03
1-db Compression	-4.2 dBm	-4.3 dBm	-4.4 dBm	-2 dBm
IIP_3	25 dBm	25 dBm	66 dBm	70 dBm

Switch bias was then set to operate the double pole switch as DPDT, where the same structure was used to simulate DPDT switches with two active paths. FET biased at a voltage of -5 V for OFF state and 2 V for ON state was also integrated. Figure 3-49 shows a plot of insertion loss and isolation from port to port for DPDT switch.

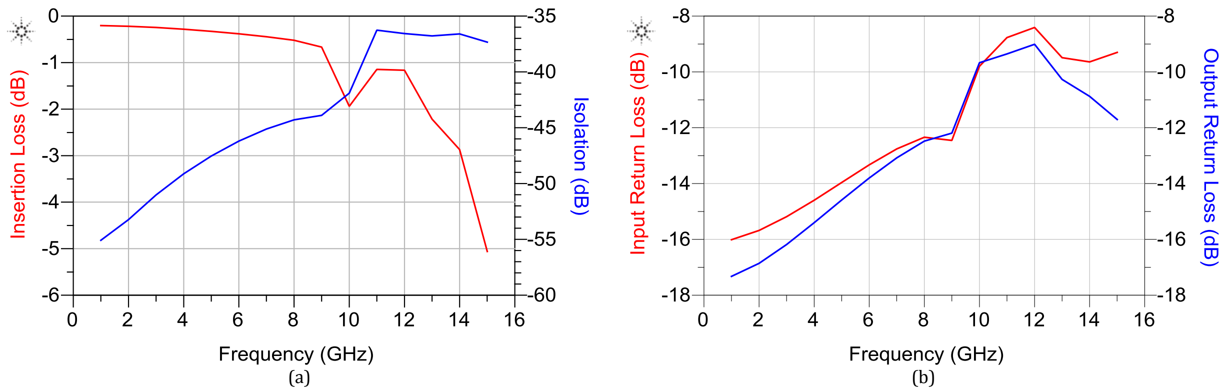


Figure 3-49: (a) Insertion loss and Isolation versus Frequency; (b) Input and Output Return Loss versus Frequency of series-shunt DPDT switch

The insertion loss of DPDT is comparable to that of DPST. The insertion loss is lowest for 1.5 GHz at 0.35 dB; whereas, the insertion loss is highest at a higher frequency, such as, 12 GHz, where the loss is -1.27 dB. Port isolation is observed to be better than 54.72 dB, which can be obtained at 1.5 GHz. As frequency increased to 10 GHz, isolation is approximately 43.28 dB. Loss compression versus RF input power and OTOI points versus Input power is presented in Figure 3-50.

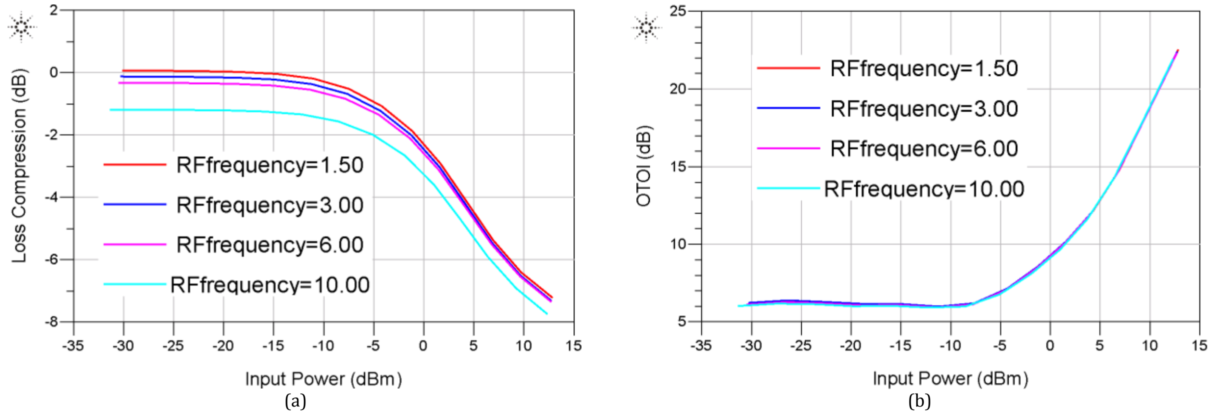


Figure 3-50: (a) Loss Compression versus Input Power; (b) OTOI versus Input Power of series-shunt DPDT switch.

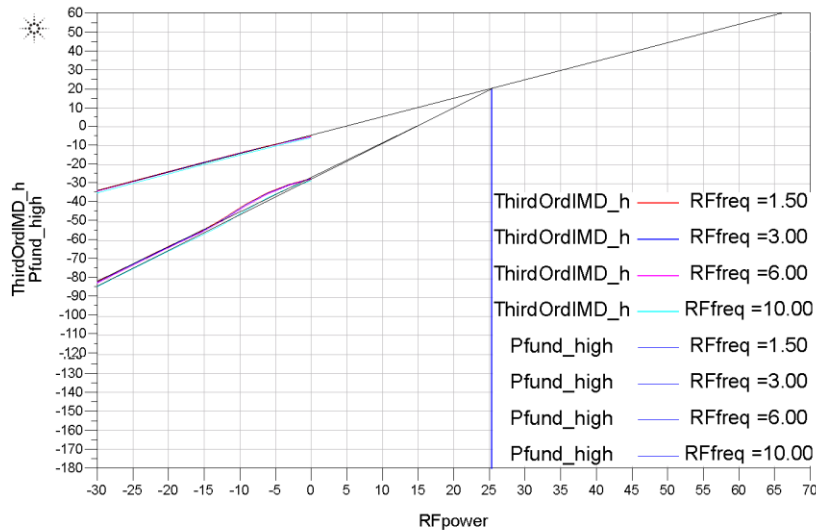


Figure 3-51: Determining IIP3 of series-shunt DPDT switch

Input and output return loss for both active RF paths are below 8 dB as shown in Figure 3-49. Figure 3-50 and Figure 3-51 display the large signal analysis of the DPDT, where the 1dB compression point is between -4.2 dBm and -4.4 dBm for L, S, C, and X band of input power for DPDT switch.

The following section will present a modification of the double pole switch using only series configured FETs to assess if the power handling performance can be improved.

Table 3-11: Simulation results of series-shunt DPDT switch design

DPDT	L Band	S Band	C Band	X Band
Insertion Loss (dB)	0.35	0.37	0.47	1.97
Isolation (dB)	54.72	50.23	46.66	43.28
Input Return Loss (dB)	-15.77	-15.47	-13.43	-9.82
Output Return Loss (dB)	-15.33	-16.29	-13.92	-9.82
1 dB Compression	-4.2 dBm	-4.3 dBm	-4.4 dBm	-4.4 dBm
IIP_3	26 dBm	26 dBm	26 dBm	26 dBm

3.5.3 Modifications

The layout in Figure 3-52 uses four 2x200μm FETs configured in series. The design uses the main structure designed in Figure 3-45 as a foundation with the exception of the shunt FETs, which makes the design considerably smaller compared to the previous design.

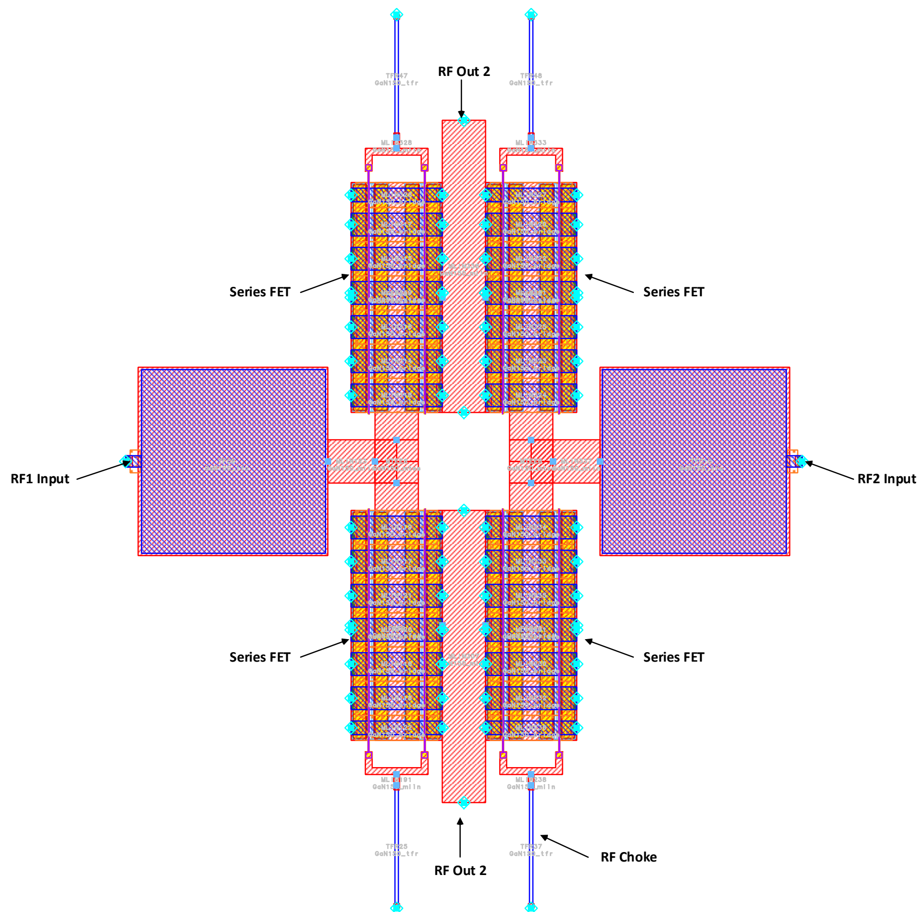


Figure 3-52: Modified Series only Double Pole RF Switch Layout

The series only double pole switch was first analyzed for small signal. Optimum bias conditions for small signal analysis was 2 V for ON state and -5 V for OFF state. Large signal peak performances are obtained with a bias condition of 2V/-5 V. Figure 3-53 shows the insertion loss, isolation and return losses for DPST using modified layout design.

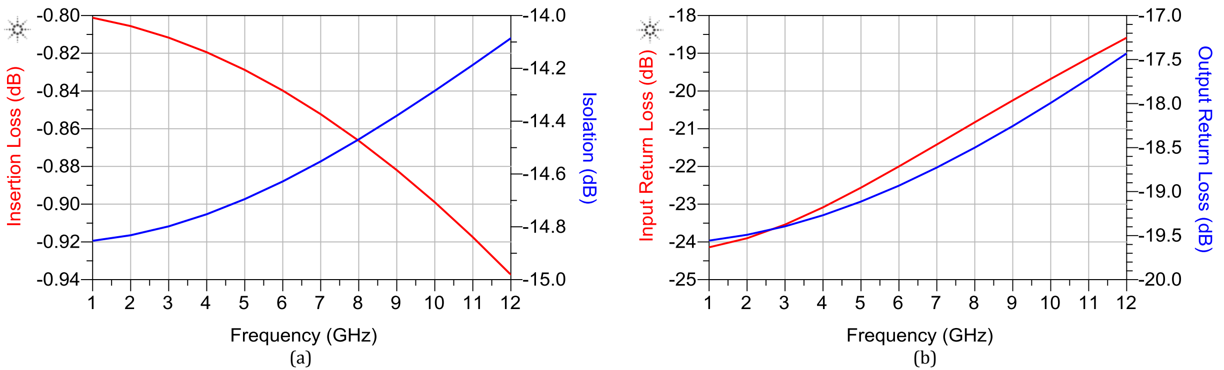


Figure 3-53: (a) Insertion and Vs Isolation Loss vs Frequency; (b) Isolation vs Frequency (right) for DPST Switch operation

Figure 3-53, displays the Insertion loss of less than 1 dB and isolation as greater than 14.1 dB. Additionally, the input return loss was found to be greater than -18 dB and greater than -17 dB for output return loss. Figure 3-54 shows plot of Loss Compression versus Input power for L, S, C, and X band. This figure shows how the 1dB compression point for all frequency bands of interest can be approximated to 18 dBm, which is a significant improvement from the series-shunt configured DPST. Table 3-12 summarizes the performance parameters of the modified DPST.

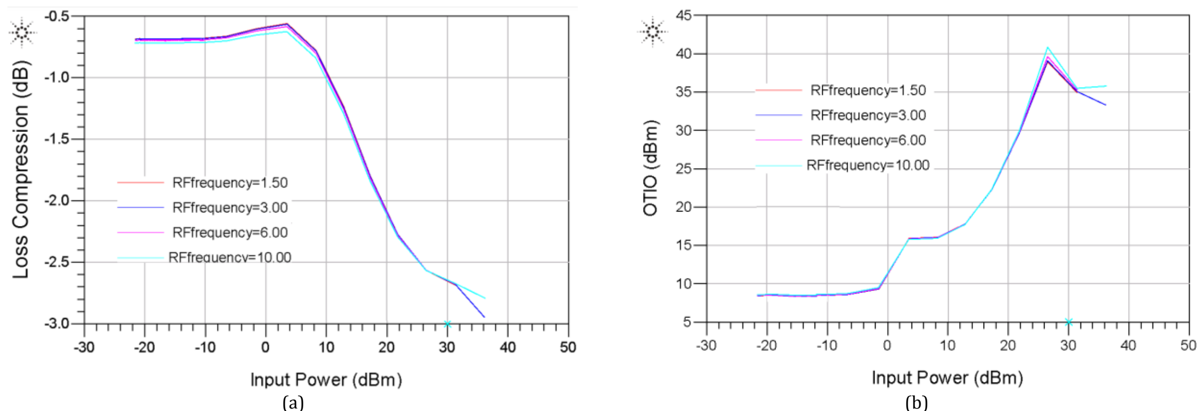


Figure 3-54: (a) Gain versus Input Power; (b) OTOI versus Input Power of series only DPST switch.

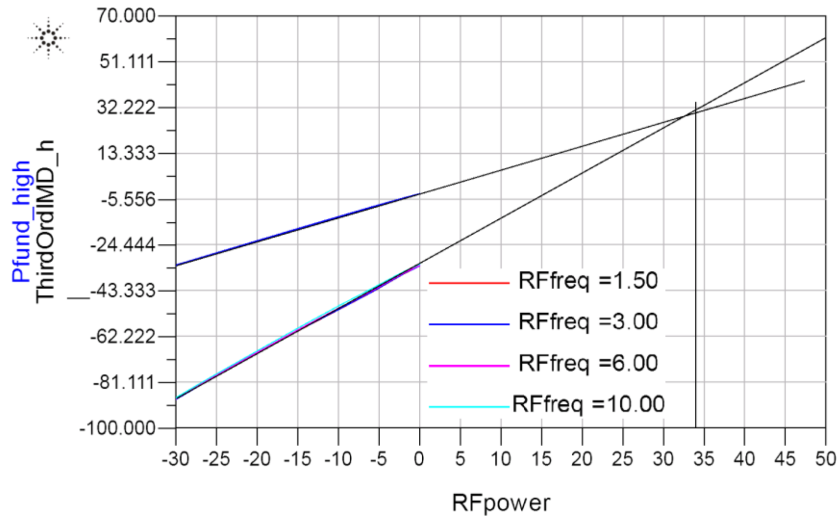


Figure 3-55: Determining IIP3 of series only DPST

Table 3-12: Simulation results of series only DPST design of this work

Modified DPST	L Band	S Band	C Band	X Band
Insertion Loss (dB)	0.81	0.81	0.84	0.89
Isolation (dB)	14.85	14.80	14.63	14.28
Input Return Loss (dB)	-24.14	-23.54	-22.00	-19.68
Output Return Loss (dB)	-19.56	-19.40	-18.93	-17.99
1dB Compression	17 dBm	17 dBm	17 dBm	17 dBm
IIP_3	33 dBm	33 dBm	33 dBm	33 dBm

Figure 3-56 shows the insertion loss, isolation, and return losses for the modified switch in DPDT operation. The difference in isolation between series-shunt DPST and series only DPST is approximately 10 dB. There were slight improvements to the insertion loss and return loss of the. Significant improvements were implemented to the 1dB compression point. Figure 3-47 shows the Loss Compression versus Input Power and OTOI versus Input power. The series only DPST has 1dB compression point of 17 dBm from 1 to 12 GHz as compared to -4.2 to -2 dBm for series-shunt DPST.

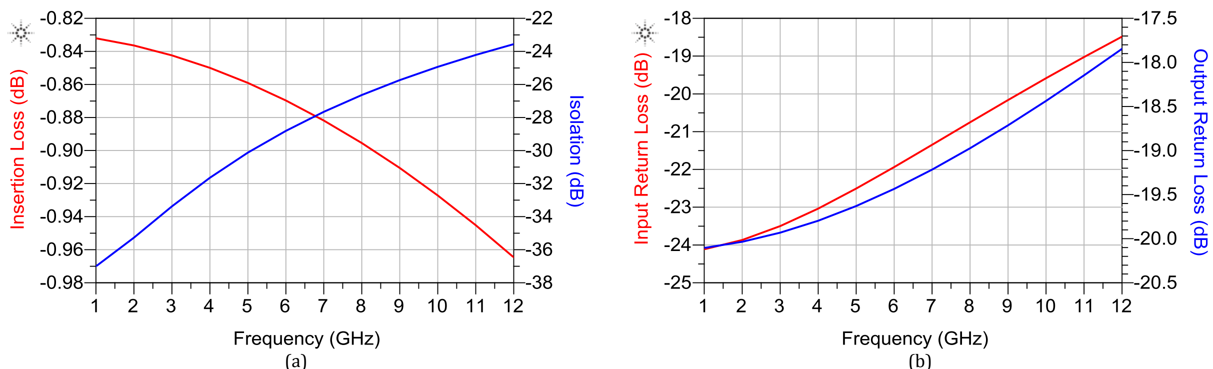


Figure 3-56: (a) Insertion loss and Isolation of different ports versus frequency; (b) Input and Output Return Loss versus frequency of sereis only DPDTswitch

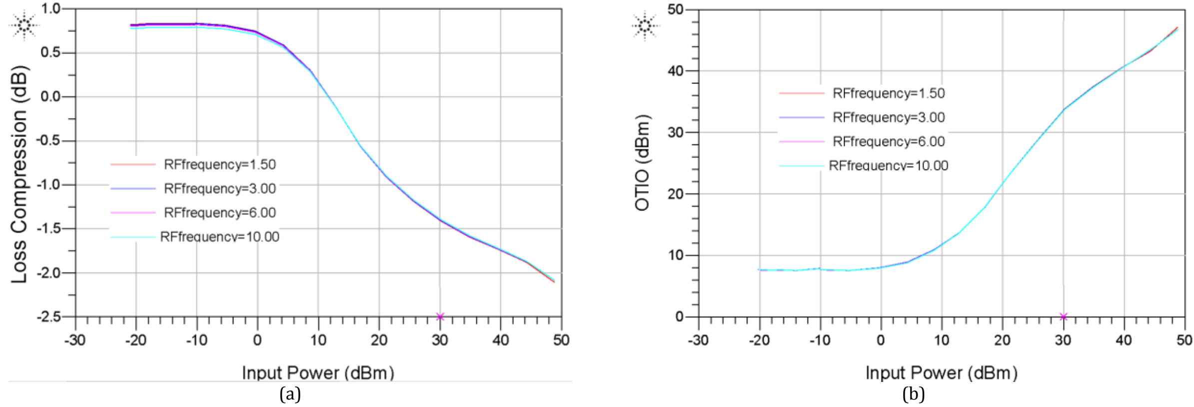


Figure 3-57: (a) Gain versus Input Power; (b) OTOI versus Input Power of series only DPDT switch.

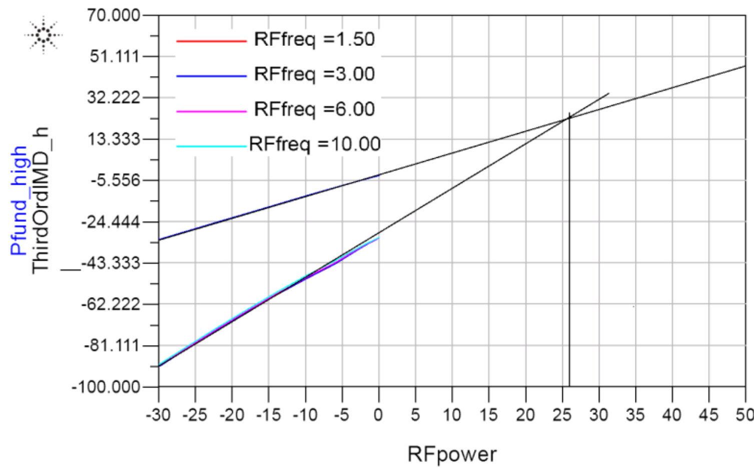


Figure 3-58: Determining IIP3 of series only DPDT

Table 3-13 shows DPDT switch performance parameters using series only configuration for L, S, C, and X band.

Table 3-13: Simulation results of series only DPDT design of this work

Modified DPDT	L Band	S Band	C Band	X Band
Insertion Loss (dB)	0.84	0.84	0.87	0.92
Isolation (dB)	36.5	33.38	28.81	24.94
Input Return Loss (dB)	-23.91	-23.5	-21.94	-19.59
Output Return Loss (dB)	-19.97	-19.93	-19.45	-18.48
1 dB Compression	14 dBm	14 dBm	14 dBm	14 dBm
IIP_3	26.5 dBm	26.5 dBm	26.5 dBm	26.5 dBm

To conclude this section, Table 3-10 can be compared with Table 3-12, to find significant improvements from the series only DPST in terms of 1dB compression point and linearity, while having lower isolation as tradeoff. For DPDT switch configuration, comparing Table 3-11 and Table 3-13 demonstrates improvements from series only switch for increased 1dB compression point. However,

both of the DPDT configuration presented in this work does not meet the target 1dB compression of 25 dBm. Future work will include further studies to improve the design of the DPDT switch to meet this power handling requirement.

3.6 Conclusion

In this chapter, GaN FET characterizations are shown to form the building blocks of RF switches. This work presented single FET switches that evaluated series, shunt, and series-shunt switch configurations. These single FET switches are of key building blocks in order to implement larger and more complex switches.

From the analysis, it was found that series only switch configurations are ideal for low insertion loss and power handling capabilities. Shunt only switch components are good for applications that are of single frequency since the λ/4 transmission line needs to be configured. A good balance of both insertion loss and isolation is found when series-shunt configuration is used.

The single switch block formed SPDT, DPST and DPDT designs presented in this chapter. The SPDT switch design displayed efficient results that can easily be integrated into a large switch matrix. Chapter 5, a design of integrated GaN 0.15μm SPDT sent to CMC for fabrication will be presented.

DPDT switch design using GaN 0.15μm shows promising results for low power applications. In this Chapter, both series-shunt and series only topology of the switch was investigated. However, for small signal it shows promising results. This Chapter also examines GaN DPST switches. DPST operation of double pole switch is configured in series-shunt configuration as it has a lower 1dB compression point. The trade-off was the isolation, as expected from a series only switch topology.

This Chapter also presents an RF switch design procedure using FETs. It provides the characterization of FET design parameters for the design of RF switches. It suggests techniques for good layout designs. Single FET switches described in this Chapter can subsequently be used to form more complex structures for different applications. Typically, in RF chains, reconfigurable matching networks are used to either improve transmit power for the PA or to match a variable antenna to FEM modules. The following Chapter presents an application of GaN switches in the form of impedance tuner operating in X-band.

4

Reconfigurable Impedance Tuner

4.1 Introduction

The input impedance of an antenna is sensitive to its surroundings [59] [60]. In mobile devices, the antenna input impedance varies depending on environmental factors. These variations, caused by the antenna orientation, thermal, etc., can imply impedance mismatch, which results in power reflection back into the transceiver or antenna and, subsequently, reduces the transmit power and the link quality. This reflected power is detrimental to components that are directly connected to the antenna; such as, PA [61]. Therefore, tuning is a key component for RF FEM to avoid the aforementioned drawbacks with robust and high performing devices. Hence, an antenna tuning unit must be able to detect the antenna impedance variation and adjust itself to compensate for the deviation in real time. For this prospect, a block diagram of adaptive matching system technique is shown in Figure 4-1.

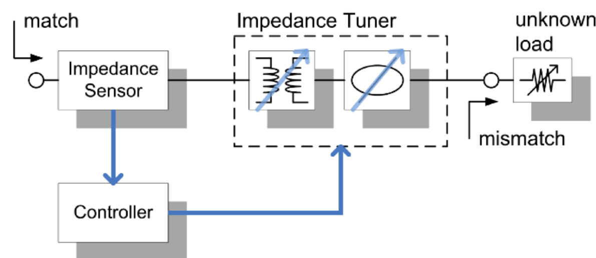


Figure 4-1: Block diagram of a closed loop adaptive matching system [61].

Figure 4-1 shows a block diagram of a closed-loop system consisting of an impedance tuner, an impedance sensor, and a controller. Among them, the impedance tuner is the component responsible for transforming any unknown load impedance to the system impedance while introducing low insertion.

An impedance tuner is an indispensable component in applications; such as, source-pull and load-pull measurements for noise [62] [63]and large-signal characterizations [64] [65]of transistors. Furthermore, they can also be specifically designed as tunable matching networks that may be either connected to antennas to compensate for antenna impedance variations [66], or placed right after power amplifiers to provide optimal load conditions at different frequency bands [67] [68] or power levels [69] [70].

Theoretically, as long as the load impedance, Z_L, has a positive real part, a matching network can be designed as its counterpart. Factors that are important in the selection of a particular matching network include:

- **Complexity**: A simple matching network that is cheaper for smaller die space, which contributes less loss to the system due to a low component count.
- **Bandwidth**: A matching network can ideally give a perfect match at a single frequency; however, it is usually desirable to match a load over a band of frequencies; this adds to complexity.
- **Implementation**: Depending on the type of transmission lines or waveguides being used, one type of matching network may be more preferable than another.

In this work, a π-network impedance tuner is proposed which consists of a variable transformer based on band-pass networks. It provides uniform coverage in the four quadrants of the Smith chart and exhibits a low circuit complexity. The proposed tuner also has the advantage that the mapping between the load impedance and the control signals is more straightforward when compared with stub-based or loaded-line tuners. As a result, when used in an adaptive matching system, the proposed tuner can be controlled using less complicated control schemes.

4.2 Design Considerations

In this section, basic design concepts of impedance tuner will be discussed. This will form the basis of the tuner design parameters.

4.2.1 Reactance and LC Resonance

Reactance takes two forms: inductive, X_L, and capacitive X_C. They can be defined by (4.1) and (4.2) respectively [24].

$$X_L = \omega L = 2\pi f L \tag{4.1}$$

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C} \tag{4.2}$$

where ω is the angular frequency, f is frequency, L is inductance, and C is capacitance. When the magnitudes of L reactance and C reactance are equal, the L -C pair resonates;the resonant frequency is given by (4.3) [24]

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.3}$$

4.2.2 Quality-Factor

The quality factor, Q, serves as a measure of how ideal the reactance is. It is characterized as the ratio of the energy stored versus the energy dissipated that can be expressed by (4.4) [71].

$$Q = \frac{2\pi \cdot (\max instantaneous\ energy\ stored)}{energy\ dissipative\ per\ cycle} \tag{4.4}$$

In this expression, Q is a dimensionless unit that is expressed as a function of reactance X and resistance R, in (4.5) [71].

$$Q = \frac{X}{R} \tag{4.5}$$

The quality factor of the L -C circuit is defined at circuit resonance. If the circuit reactance is plotted as a function of frequency, the slope of the reactance of the resonance frequency is a measure of Q, where Q of a reactive component is the ratio of its reactance magnitude of its resistance and is defined as by (4.6) and (4.7) [24].

$$Q_{inductor} = \frac{X_L}{R_L} = \frac{\omega L}{R_L} \tag{4.6}$$

$$Q_{capacitor} = \frac{X_C}{R_C} = \frac{1}{\omega C R_C} \tag{4.7}$$

4.2.3 Unloaded-Q

The loaded quality factor, Q_L is the ratio of the magnitude of the reactance of L or C at the resonance frequency to the total circuit resistance. Physical reactive elements always have some resistive losses in terms of its Q. The unloaded-Q (Q_U) is the Q associated with the reactive elements only as represented by (4.8) [72].

$$\frac{1}{Q_U} = \frac{1}{Q_{ind}} + \frac{1}{Q_{cap}} \tag{4.8}$$

4.2.4 Loaded-Q

A loaded-Q of a resonant circuit depends on three main factors:

- The source resistance, R_S.
- The load resistance, R_L.
- The component Q-factors.

As shown in Figure 4-2, the resonant circuit sees an equivalent $R_P$resistance, R_S in parallel with R_L, as stated by (4.9) [73].

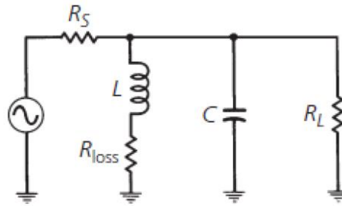


Figure 4-2: Circuit diagram for loaded-Q

$$R_P = \frac{R_S \times R_L}{R_S + R_L} \tag{4.9}$$

The $R_P$resistance is larger in value than either R_S or R_L assuming lossless components, for Q which can be defined by (4.10) [73].

$$Q = \frac{R_P}{X_P} \tag{4.10}$$

where R_P is the equivalent parallel resistance of R_S and R_L where $X_P$is inductive or capacitive reactance.

4.3 Types of Matching Network

The technique of impedance matching forces a load impedance to be perceived as the complex conjugate of the source impedance, enabling maximum power to be transferred to the load [24]. Figure 4-3 illustrates Impedance matching of a resistance source and complex load for maximum power transfer . The matching process becomes substantially difficult when the tangible parts of the terminations are unequal; this work aims to address these factors for X-Band operation.

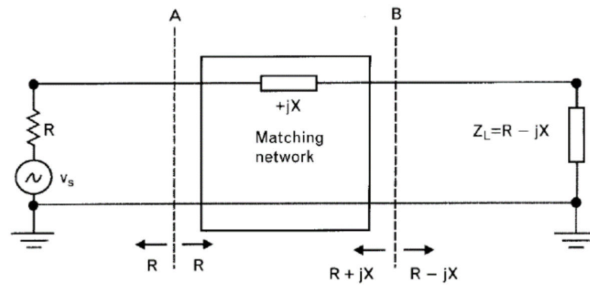


Figure 4-3: Impedance matching of a resistance source and complex load for maximum power transfer [19]

Impedance tuning is important for the following reasons:

a) The delivery of maximum power to the load when it is matched to the line, where the power loss in the feed is minimized.
b) Sensitive receiver components; such as, antenna, LNA, etc. may improve the signal-to-noise ratio of the system.
c) Power distribution network; such as, the antenna array feed network may reduce the amplitude and phase error.

4.3.1 Transformers

Impedance matching using transformers is another possible option to match resistive source and resistive loads. Power entering into a transformer is equal to the output power (discounting negligible losses). Transformers only match real impedances; if there is a large load reactance, a transformer will not eliminate these reactive components, and additionally contribute to the exaggeration of the reactive portion of the load impedance. Transformer based matching works poorly at microwave frequencies but provides a larger bandwidth than L-C matching circuits which have excellent amplitude, phase balance, and lower input VSWR.

4.3.2 Quarter-Wave (λ/4) Transformer

An impedance transformer can be established by inserting a transmission line of one quarter of the wavelength (λ/4) long with appropriate characteristic impedance. In theory, quarter-wave transformer is utilized to match complex impedances but common practice is to match real impedances; however, a complex load impedance can always be transformed to a real impedance by adding appropriate series or shunt reactive component. The characteristic impedance of a λ/4 line is the geometric average of Z_{in} and Z_L. Several techniques used for quarter-wave transmission line matching are outlined as follows:

a) The quarter-wave transformer, depicted in Figure 4-4, provides perfect matching at one operating frequency and thus, has a limited bandwidth.

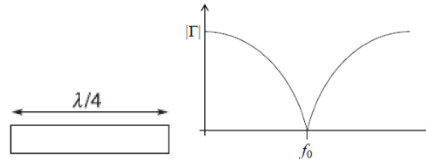


Figure 4-4: Quarter-wave transformer [74]

b) A broadband transformer, shown in Figure 4-5, can be designed by using a cascade of λ/4 transmission line sections, while gradually varying their characteristic impedance.

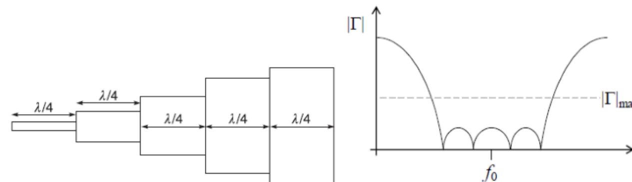


Figure 4-5: Broadband transformer [74]

It is not possible to obtain a near zero reflection for the entire desired band. Therefore, available design approaches specify a maximum reflection coefficient within tolerance in the frequency band of operation.

c) Tapered line transformer, presented in Figure 4-6, with a continuous varying characteristic impedance along its length, can be applied to obtain broadband matching. Typically, the required length of the tapered section should be about 0.5 to 1.5 times the wavelength. A different narrow-band approach involves the stub matching; for example, the insertion of a shunt imaginary admittance on the transmission line where the admittance is realized with a section (or stub) of transmission line.

Figure 4-6: Tapered line transformer [74]

Similarly, insertion of series impedance stub along the line can also achieve narrow-band matching.

4.3.3 Lumped Elements

4.3.3.1 L-Network

L-section matching network uses two reactive elements to match an arbitrary load impedance to a transmission line. It displays two possible configurations for L-network. If the normalized load impedance $z_L = \frac{Z_L}{Z_O}$, is within the $1 + jX$ circle on the Smith chart, then Figure 4-7 (a) should be used; if outside, Figure 4-7 (b) should be used.

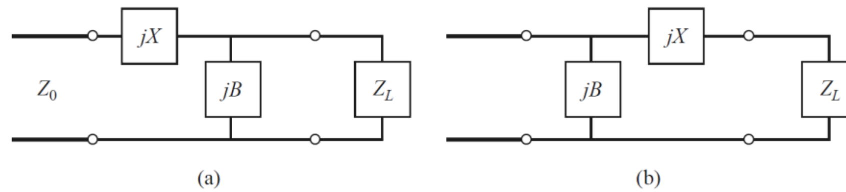


Figure 4-7: L-section matching network [24]

Depending on the load impedances, the reactive matching elements may either be inductors or capacitors which results in eight distinct possibilities. The analytical value of such reactive components can be estimated by (4.11) and (4.12) [73].

$$B = \frac{X_L \pm \sqrt{\frac{R_L}{Z_0}}\sqrt{R_L^2 + Z_L^2 + Z_0 R_L}}{R_L^2 + Z_L^2} \qquad X = \frac{1}{B} + \frac{X_L Z_0}{R_L} - \frac{Z_0}{B R_L} \qquad Q = \frac{X_L}{B} \qquad \text{when } R_L > Z_0 \tag{4.11}$$

$$B = \pm \frac{\sqrt{\frac{Z_0 - R_L}{R_L}}}{Z_0} \qquad X = \pm\sqrt{R_L(Z_0 - R_L} - X_L \qquad Q = \frac{X}{X_L} \qquad \text{when } R_L < Z_0 \tag{4.12}$$

To match an arbitrary complex load to a characteristic line impedance Z_0, the real part of source impedance of the matching network must equal to Z_0, while the imaginary part must equal to zero, thereby, giving the L-section matching circuit two degrees of freedom that are provided by the values of the two reactive components. L-network impedance matching is simple, low cost and easy to design; however, it has a narrowband operation.

4.3.3.2 π-Network

One can analyze the π-matching circuit by delineating it into two L circuit sections. Figure 4-8, shows two back-to-back connected L-match circuits to form a π-network. The additional element in the π-network compared to L-match, allows independent setting impedance transformation ratio $\left({}^{R_L}/_{R_{in}}\right)$ and the quality factor for the circuit.

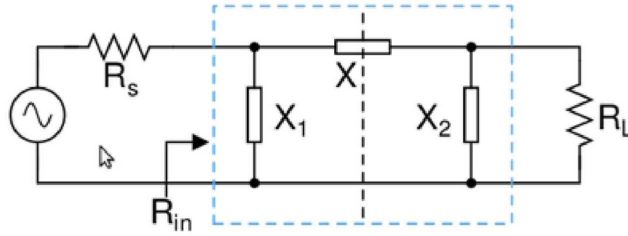


Figure 4-8: Two L-match circuit forming a π-network [76]

The analysis of π-match circuit in Figure 4-8, can be simplified by redrawing the circuit into two L-match sections as shown in Figure 4-9.

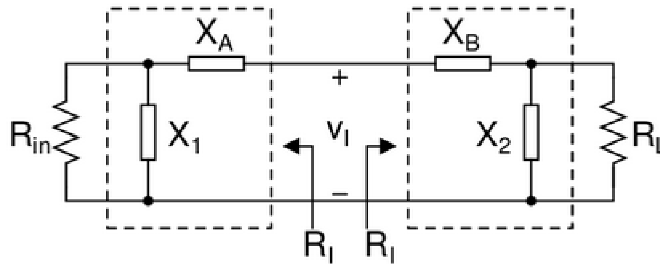


Figure 4-9: Simplified π-match circuit redrawn into two L-match sections [75]

If V_I is the input voltage of the L-match circuit and R_I is the impedance seen looking into each L-match circuit, then the current flowing through the inductor of each L-match circuit is $I_L = \frac{V_L}{R_I}$. The Q-factor looking into each parallel R-X branch is then given by (4.13) [73].

$$Q_1 = \frac{R_{in}}{X_I} \qquad\qquad Q_2 = \frac{R_L}{X_2} \tag{4.13}$$

By doing a series-to-parallel transformation, the quality factor can be described by (4.14) and the total Q of the circuit then can be expressed as (4.15) [73].

$$Q_1 = \sqrt{\frac{R_{in}}{R_I} - 1} \qquad\qquad Q_2 = \sqrt{\frac{R_L}{R_I} - 1} \tag{4.14}$$

$$Q = Q_1 + Q_2 = \sqrt{\frac{R_{in}}{R_I} - 1} + \sqrt{\frac{R_L}{R_I} - 1} \tag{4.15}$$

At the resonant frequency, $|X_A| = |X_{1,s}|$ and$|X_B| = |X_{2,s}|$. This can be equated by (4.16) [73].

$$X_A = \frac{X_1}{(1+Q_1^2)} \qquad X_B = \frac{X}{(1+Q_1^2)} \tag{4.16}$$

For a low-pass π-match, equation (4.17) and (4.18) can be used to calculate the component values of the matching circuit [73].

$$X_1 = \frac{1}{\omega_0 C_1} \qquad X_2 = \frac{1}{\omega_0 C_2} \tag{4.17}$$

$$X_A = \omega_0 L_A \qquad X_A = \omega_0 L_B \tag{4.18}$$

For high-pass π-match, equations (4.19) and (4.20) can be used to calculate the component values of the matching circuit [73].

$$X_1 = \omega_0 L_1 \qquad X_2 = \omega_0 L_2 \tag{4.19}$$

$$X_A = \frac{1}{\omega_0 C_A} \qquad X_A = \frac{1}{\omega_0 C_B} \tag{4.20}$$

4.4 Tuner Metrics

Design of an impedance tuner depends on the application specifications; such as, loss, linearity, power handling, impedance coverage, and speed of adaptation. Typically, an ideal tuner would be lossless and with 100% tuning range [76]. However, this is rarely achievable due to trade-offs between loss and tuning range, along with power handling and linearity. A lossy tuner with wide tuning range might be suited for antenna tuning where minimization of reflected power is of the highest priority; whereas, for the PA, a relatively small tuning range with a very low loss might be best suited since the PA load impedance is not expected to change drastically. This section explains the parameters relevant to designing an impedance tuner: tuning range, loss, and tuner control.

4.4.1 Tuning Range

The tuning range of an impedance tuner is quantified by the area covered on the Smith chart, where an impedance tuner with 100% coverage would have a tuning area of π (total area of Smith chart). Figure 4-10 shows a uniform 0.1 gamma grid where each dot is representative of a load impedance at a single frequency that can be matched by a tuner.

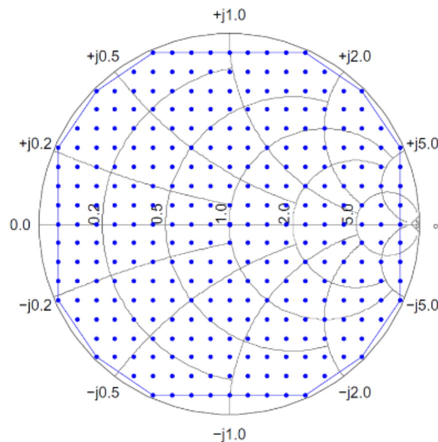


Figure 4-10: Illustration of impedance tuner coverage. Each dot on the Smith chart represent load impedances that can be matched [61].

Apart from the coverage specification, the density of the points within the covered area is also importance as it is related to the allowable VSWR. Tuner coverage contains the worst-case quality of match that can be achieved inside the area.

4.4.2 Tuner Loss

For the impedance tuner to match a highly reflective load impedance, it needs to be configured to provide the complex conjugate in order to maximize the power transfer. To achieve such impedance, a low-loss matching network is necessary. In practice, an impedance tuner than can produce impedance up to VSWR of 40 is considered to be a low loss tuner. However, this loss will increase in frequency with the decrease in Smith chart coverage. The general equation to calculate loss is known as Loss Factor, which is defined as by (4.21) [61]. .

$$Loss\ Factor = 1 - |S_{11}|^2 - |S_{21}|^2 \tag{4.21}$$

However, (4.21) is only valid when the source and load are matched. A more appropriate measure of tuner insertion loss is where it accounts for unmatched 2-port network as stated in (4.22) [26].

$$Insertion\ Loss = \frac{P_{DL}}{P_{DS}} = \frac{|S_{21}|^2}{1 - |S_{11}|^2} \tag{4.22}$$

As per the definition, port 1 is connected to a source and port 2 is connected to a dynamic load. Equation (4.22) eliminates the mismatch at port 1 where it negatively impacts the insertion loss. For tuner, the mismatch at port 2 should be factored out when calculating insertion loss rather than mismatch at port 1. Since source sees a matched load, the tuner loss should only be considered when the impedance is not matched. This leads to a special insertion loss of tuners given by (4.23) [26].

$$Insertion\ Loss\ for\ Tuner = \frac{|S_{21}|^2}{1 - |S_{22}|^2} \tag{4.23}$$

4.4.3 Tuner Control

There are two types of tuner controls; continuous tuner and discrete tuner. Continuous tuner consists of a circuitry where reactance is a function of DC voltage [61]. For continuous tuner, a variable reactance device is used to change the characteristic impedance. Such tuners are typically implemented using digital to analog (DAC) converters, where only a discrete number of states exist in practice.

Discrete tuners are built using switches that can be implemented using transistors, PIN diodes, or MEMS device. Digital tuners consist of various capacitors where each capacitor increases the number of states by 2^n, where n is the number of capacitors [61]. Single-pole multi throw switches can also be used to design phase shifters where each throw can be configured to use as 0°, 45°, 90°, and 135° of relative phase between them.

4.5 Architecture and Analysis

The proposed impedance matching is based on π-matching network. This network has better control compared to the L-matching network. The π-network fairs better for tuning compared to the lumped tuning method due to its low loss as it only passes through a single inductor. This work presents a 16-bit π-structure matching network with the ability to match at-least 30 to 80 Ω and covers a region approximately within ±j35. The impedance tuner presented in this work is directed towards X-band applications.

In this section, a simplified design will be discussed, where a 16-bit π-matching network for X-band will be discussed to a wide range of complex impedances. A complete layout of the design will then be presented and lastly, EM-simulation results will be analyzed.

4.5.1 Design

A 16-bit π-network structure is shown in Figure 4-11. The FETs are in two operation modes, ON or OFF. Each FET and capacitor arm creates C_S and C_L where C_S on the source side and C_L is the load side capacitances that are part of one matching condition.

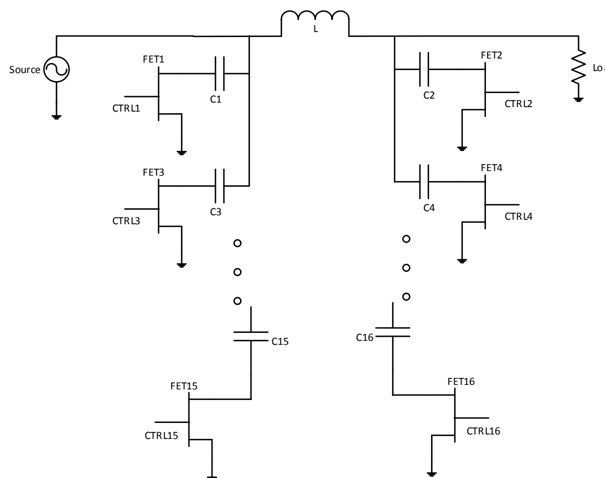


Figure 4-11: 16-bit Π-Matching Network

This topology has low loss since the signal path is much shorter and gives more flexibility in terms of controlling shunt capacitors. Each FET is 2x200 μm biased at -4 V in OFF state and 2 V for ON state to ensure proper choke and signal path to ground, respectively. The series spiral inductor produces 1 nH. The insertion loss and isolation was simulated over series device widths for different shunt device dimensions to find out the best match to be incorporated as one of the bit strands in this design. The full structure of the impedance tuner is shown in Figure 4-12.

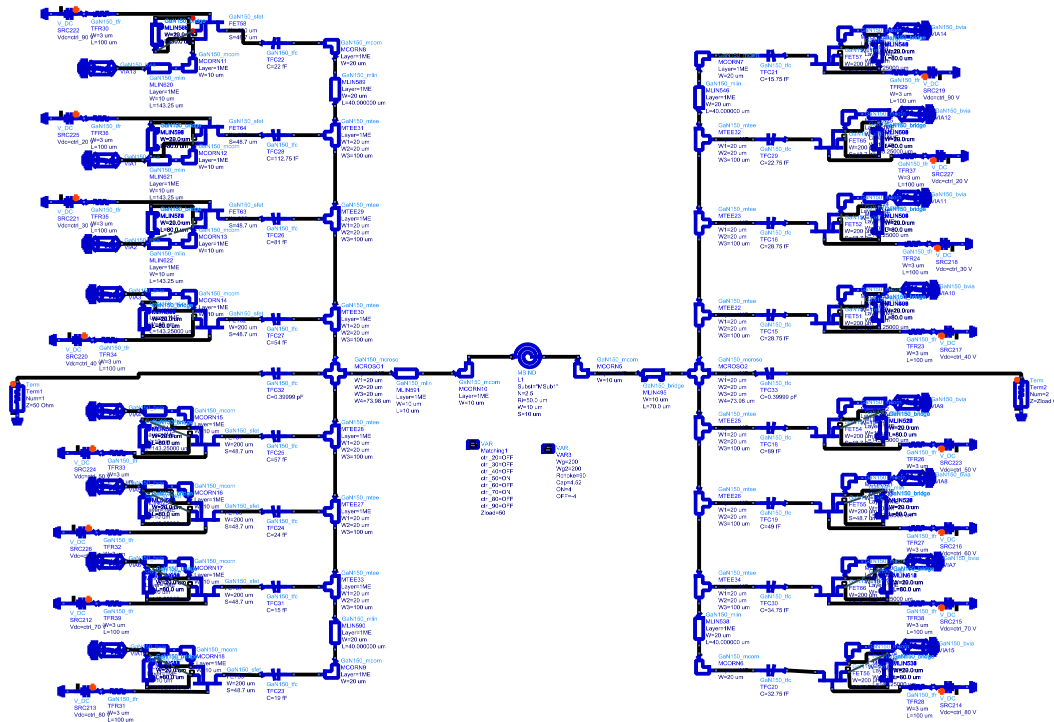


Figure 4-12: 10 GHz 16-bit Impedance Tuner

A 20x70μm air-bridge is used to access the inside node of the inductor. Each strand for the matching network shown in Figure 4-13 consists of a 2x200μm FET. Additionally, a 1 nH series inductor, 20x80μm air-bridges, tuned MIM capacitor, 3x100μm nichrome resistor (equivalent to 1500 Ω as DC feed for the FET) are used. Figure 4-13 shows a single shunt matching network strand.

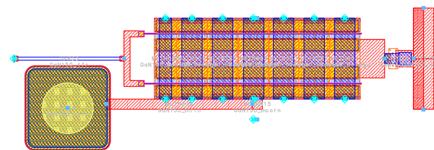


Figure 4-13: Single matching network strand

Air-bridges are used to ensure good connectivity between two sources. A transmission line is stretched out to connect to a VIA, and a 1500 Ω nichrome resistor is placed at the gate of the FET to act as a DC feed and supply V_G. Each shunt capacitances is tuned to ensure proper matching for X

band, with a total 16 capacitor-shunt combinations, creating 16-bit tuner. Figure 4-14 shows complete the layout of the tuner. It occupies 1x1.2mm of total die space.

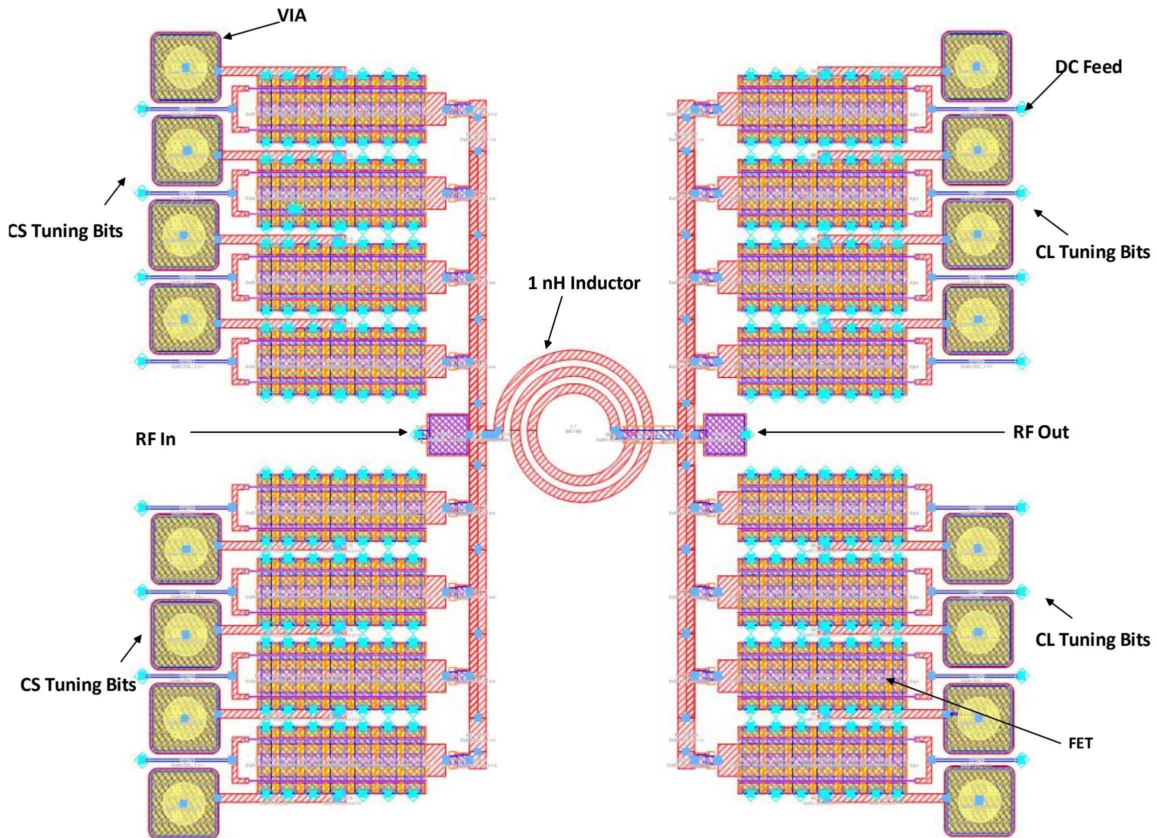


Figure 4-14: Layout of 16-bit programmable impedance tuner

4.5.2 Results

Stability of the tuner is confirmed by verifying the stability factor and the stability measure which as displayed in Figure 4-15 where it has been found to meet the criteria for the desired operating frequency range.

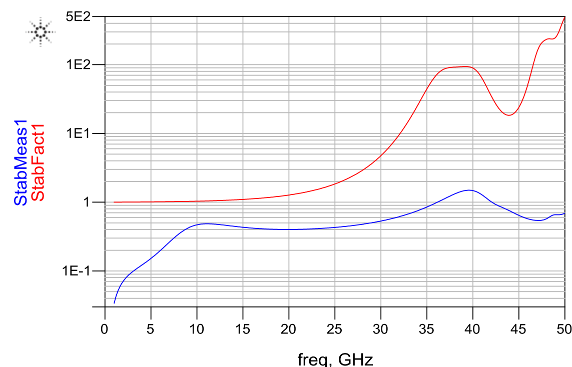


Figure 4-15: Stability of Impedance Tuner

The impedance tuner is designed to have low loss from port to port. Small or no loss should be observed. Simulations were performed using 2 V for ON and -4 V for OFF control voltage.

Figure 4-16 displays the plots of S_{11} while Figure 4-17 illustrates insertion loss of the impedance tuner based on equation (4.23) and VSWR of the 16-bit impedance tuner for 2^{16} combination (represented by variable INDEX). The target bandwidth of 8 to 12 GHz to cover X Band entirely was not possible due to low tuning range of the series inductor. Hence, the tuner was only able to operate from 9 to 10 GHz. Simulations were performed using Data Access Component in ADS, setting the control bits for each of the tuner strands. Table 4-1 presents a summary of the tuner parameters.

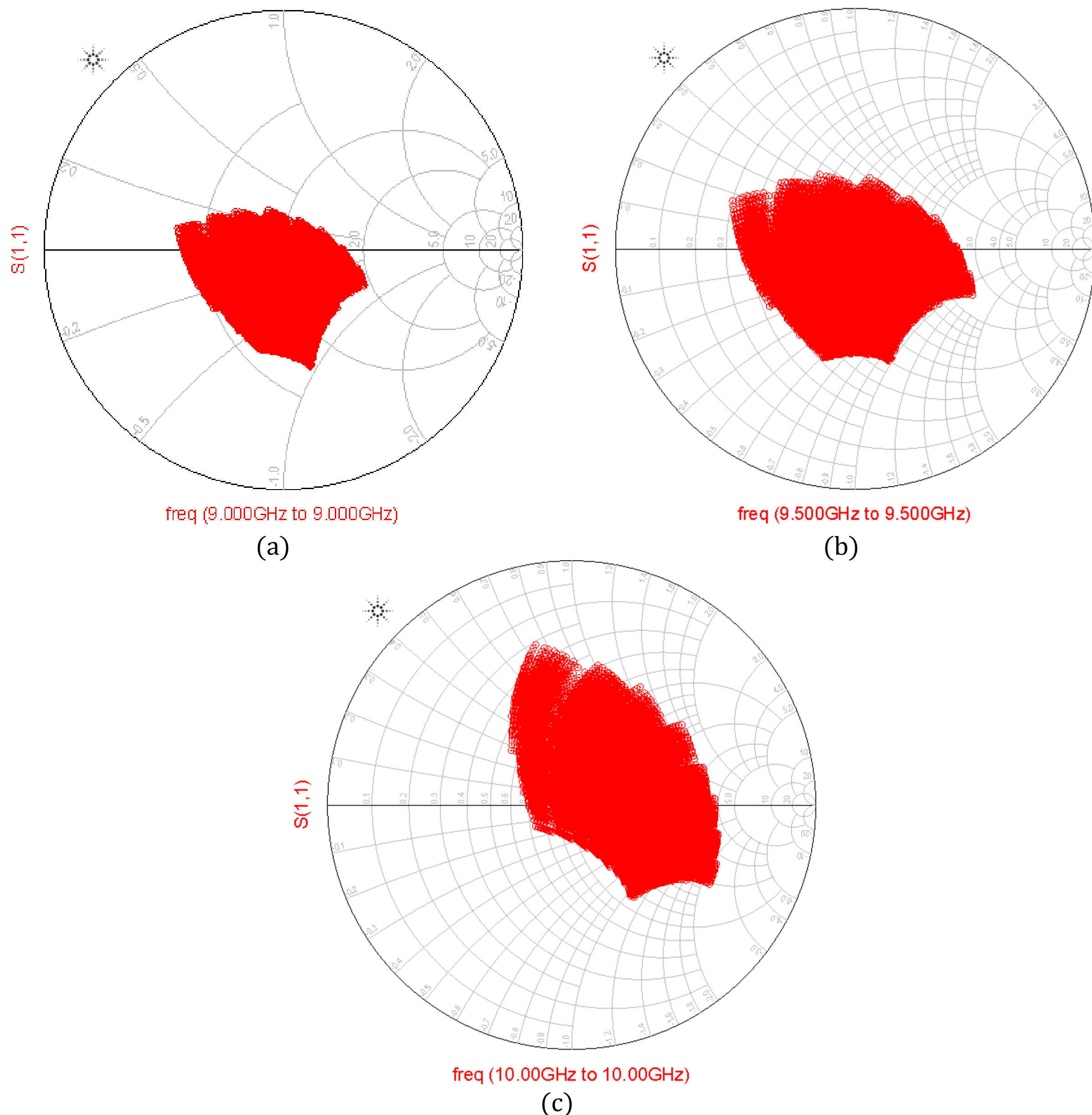


Figure 4-16: (a) S_{11} of Impedance Tuner at 9 GHz; (b) S_{11} of Impedance Tuner at 9.5 GHz ; (c) S_{11} of Impedance Tuner at 10 GHz with signal series inductor

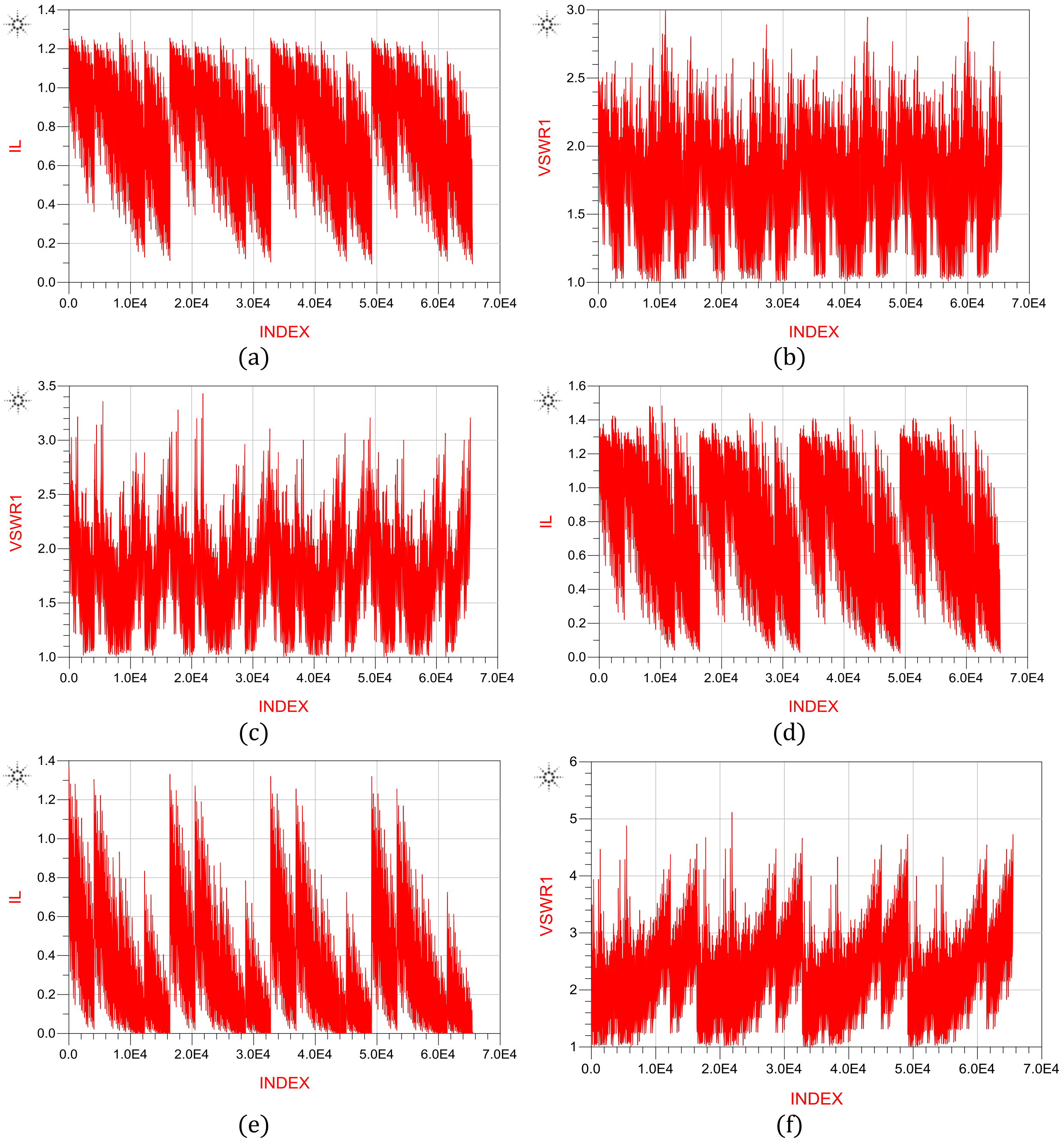


Figure 4-17: (a) Insertion loss at 9 GHz; (b) VSWR at 9 GHz; (c) Insertion loss at 9.5 GHz; (d) VSWR at 9.5 GHz; (e) Insertion loss at 10 GHz; (f) VSWR at 10 GHz with signal series inductor

Table 4-1: 16-Bit Impedance Tuner Parameters with single series inductor

Frequency	Real Imped-ance Range	Imaginary Impedance Range	VSWR	Maximum Insertion loss of Tuner	Approximate Smith Chart Coverage
9 GHz	15-80 Ω	-j40 to j30	2.5:1	1 dB	20 %
9.5 GHz	20-200 Ω	-j30 to j80	3:1	1.2 dB	32 %
10 GHz	20-200 Ω	-j30 to j80	3.5:1	1 dB	30 %

The impedance tuner having one series inductor is only able to cover 9 to 10 GHz. However if the entire X-band coverage is required, the series inductor needs to be tunable to cover all operating frequencies of the band. The following section presents a tunable series inductor which is added to the tuner to increase the bandwidth.

4.5.3 Modifications

The modification of topology presented in section 4.5.1 is examined in this section. There is a 3-bit inductor tuner added as the series inductor shown in Figure 4-11. The 3-bit inductance generator, shown in Figure 4-18.

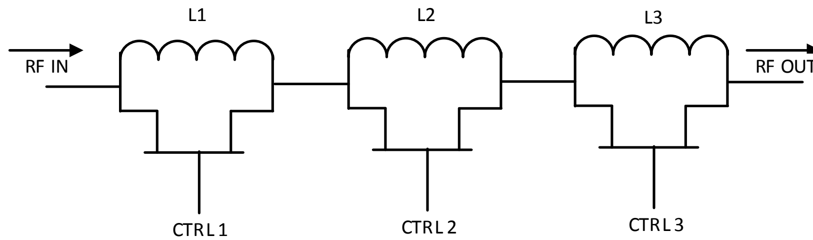


Figure 4-18: 3-bit inductance generator

Three inductors are utilized where each is in parallel with a 2x200 µm FET. To recognize L1, CRTL1 is turned OFF and CTRL2 and CTRL3 both turned ON. When the FET is turned OFF, the full inductance is realized; whereas, when turned ON, the signal sees a small loss for each FET in the chain. The spiral inductors 1, 0.50, and 0.25 nH are used as L1, L2, and L3 respectively, where the H shaped structure contributes the additional 0.2 nH of inductance. The target frequency range for this design is 8 to 12 GHz to cover the X-band in its entirety. The particular combination of gate voltages for the 3-bit inductor structure were optimized by ADS tuning as shown in Figure 4-19 and plot of inductance and insertion loss versus frequency is illustrated in Figure 4-20.

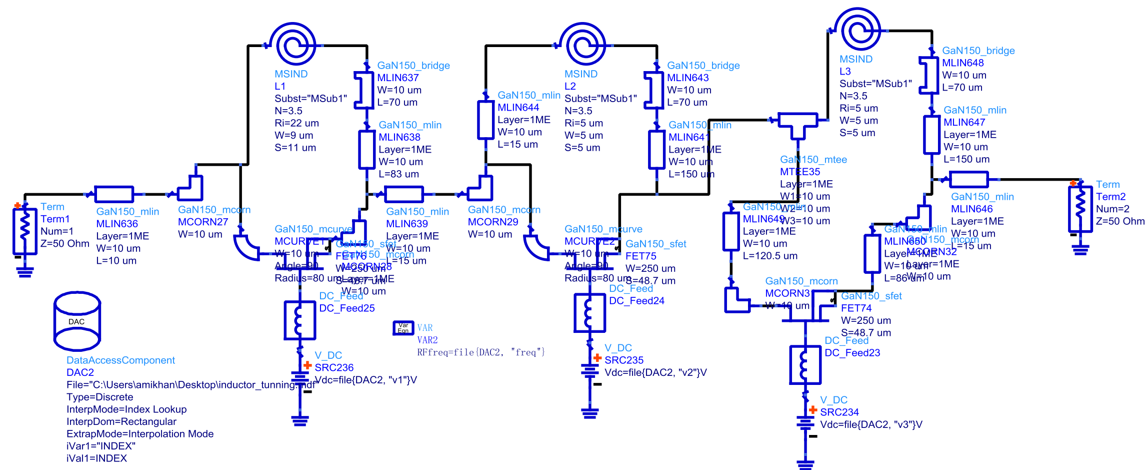


Figure 4-19: ADS schematic of 3-bit inductance tuner

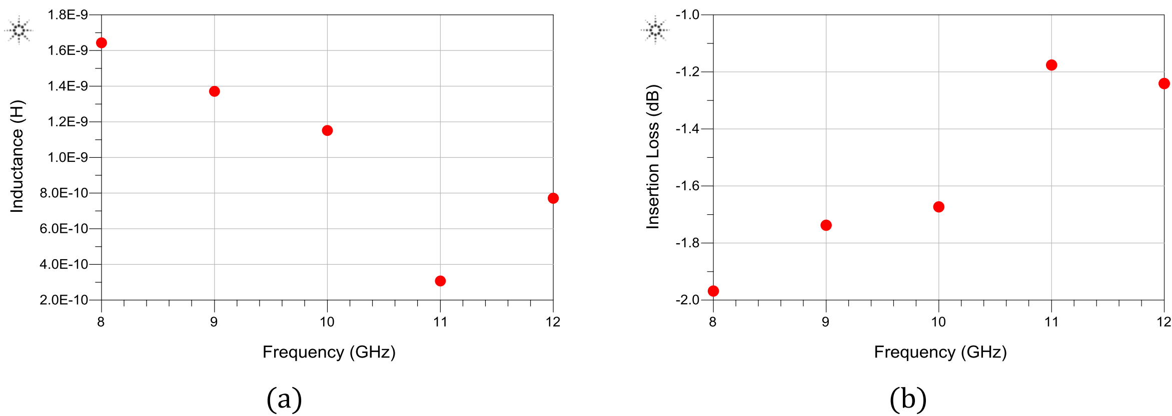


Figure 4-20: Layout driven schematic simulation of (a) inductance and (b) insertion loss versus frequency

A full layout of the impedance tuner with 3-bit inductor tuner is displayed in Figure 4-21, which requires an allocated space of a 1.1x1.2 mm of die space. Subsequently the schematic is presented in Figure 4-22.

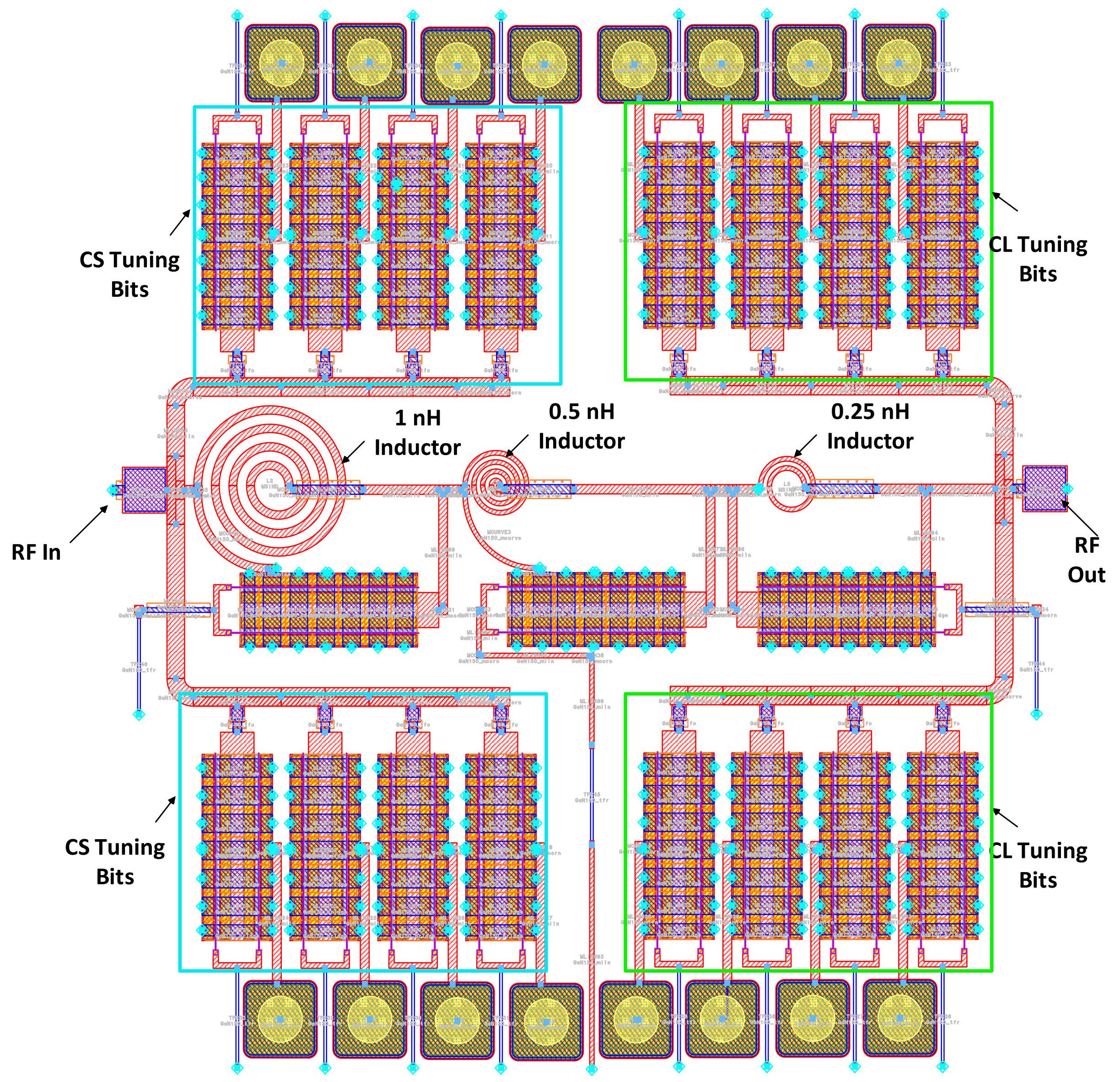


Figure 4-21: Layout of 16-bit reconfigurable impedance tuner with 3-bit inductor tuner

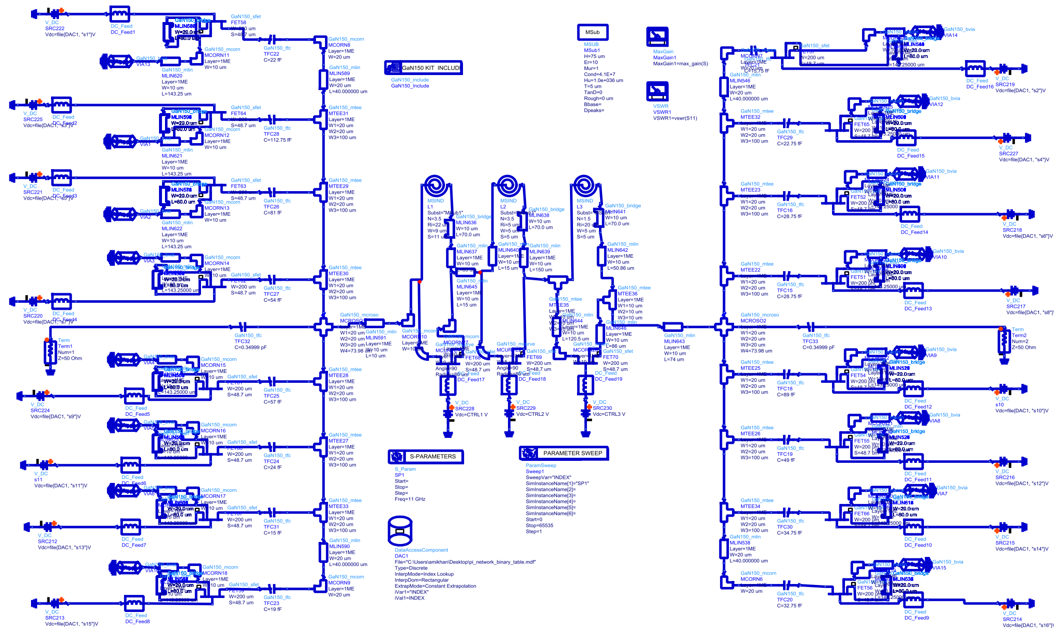
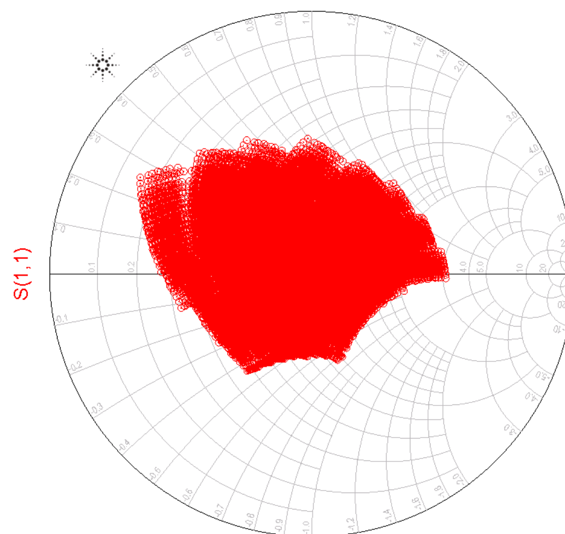
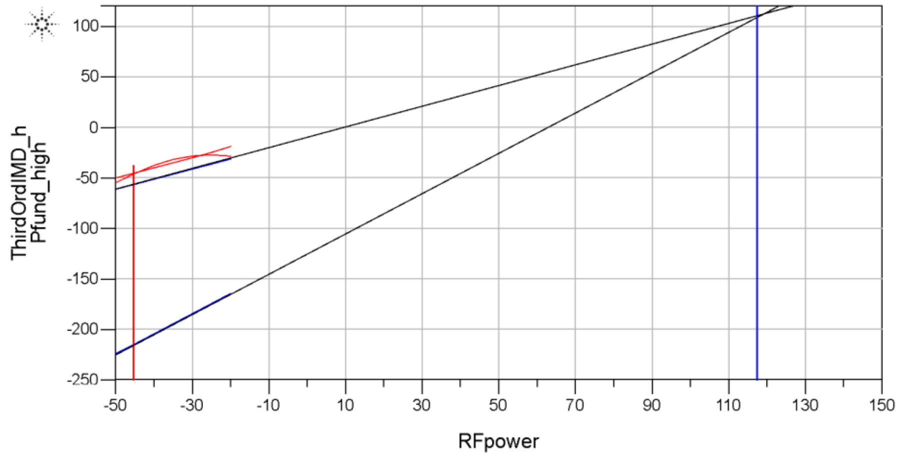


Figure 4-22: X-Band 16-bit Impedance Tuner with 3-bit inductance tuner

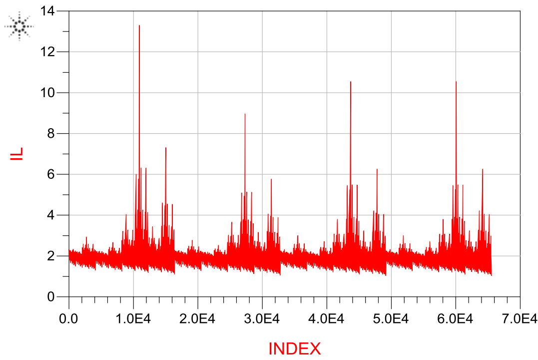
Figure 4-23, Figure 4-24, Figure 4-25, Figure 4-26, and Figure 4-27 display plots of S_{11}, insertion loss, and VSWR for 8, 9, 10, 11, and 12 GHz respectively where the variable INDEX represents 2^{16} combinations. Subsequently Table 4-2 presents a summary of the tuner parameters of the modified design. The red vertical line for linearity plots represents all capacitors in the OFF state and the blue vertical line represents all capacitors in the ON state.



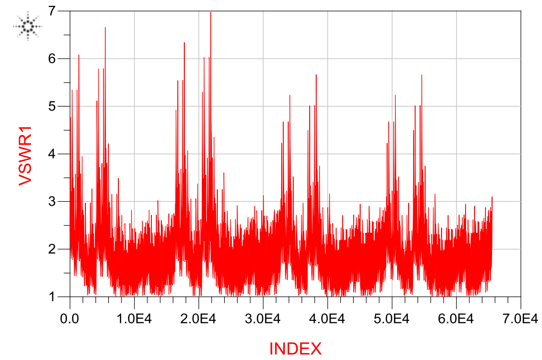
(a)



(b)

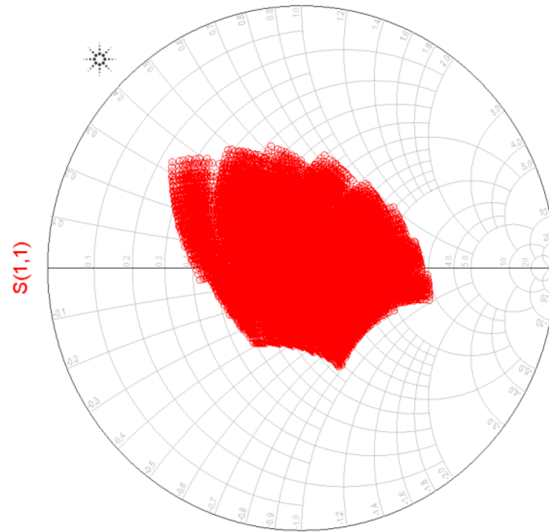


(c)

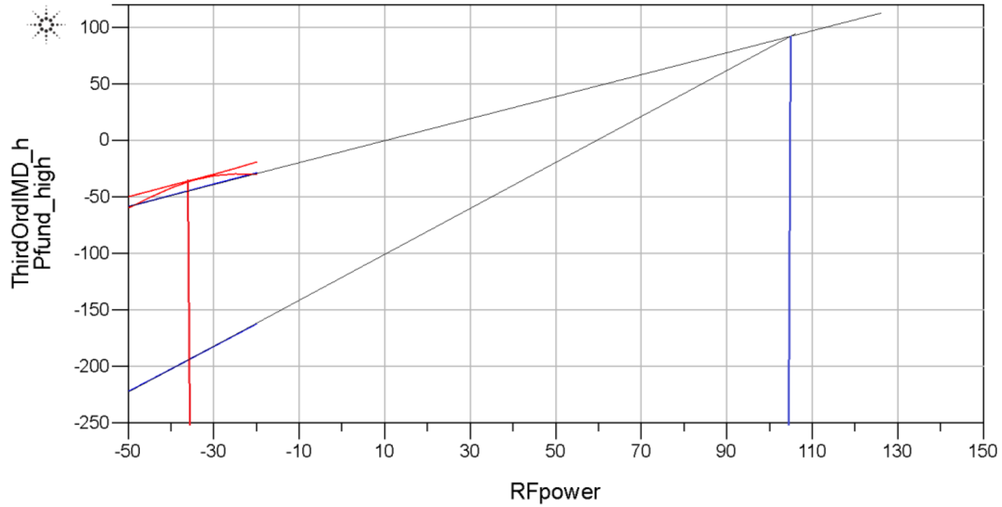


(d)

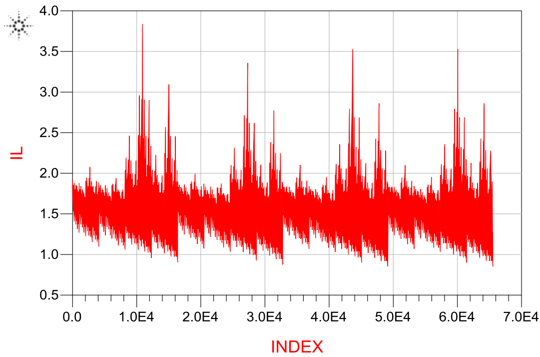
Figure 4-23: (a) S_{11} of Impedance Tuner; (b) Linearity; (c) Insertion Loss of Tuner; (d) VSWR of Tuner at 8 GHz with series 3-bit inductor tuner

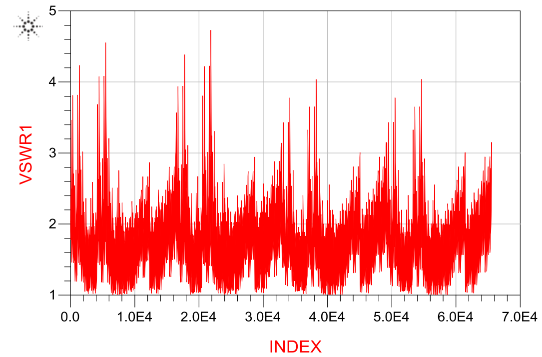


(a)



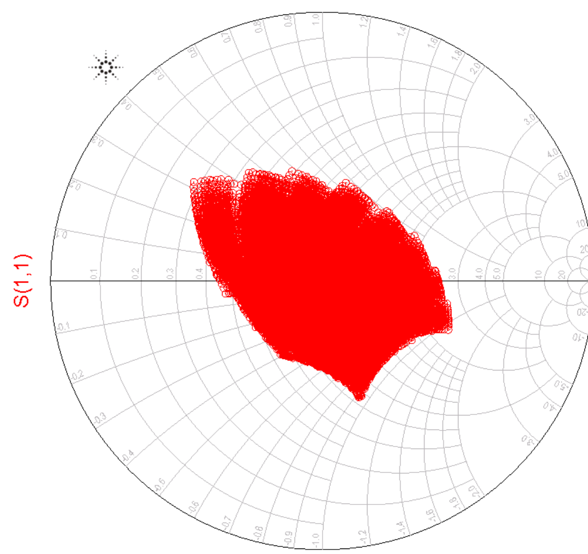
(b)



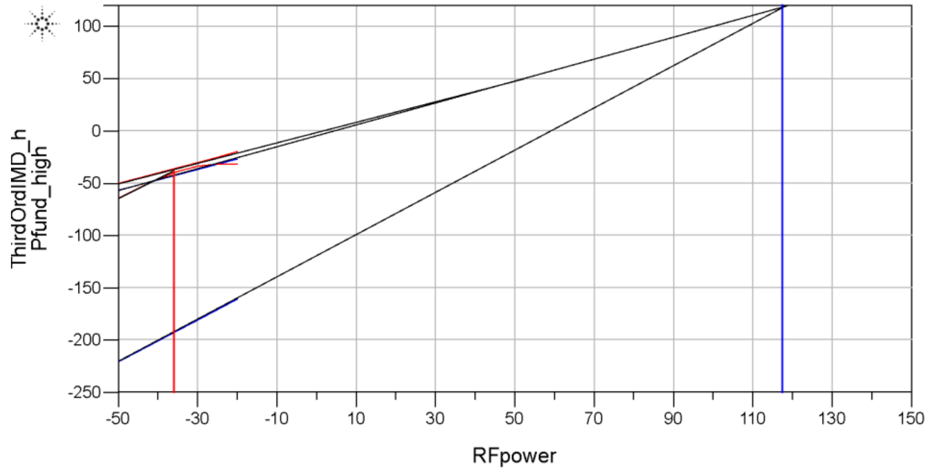


(c) (d)

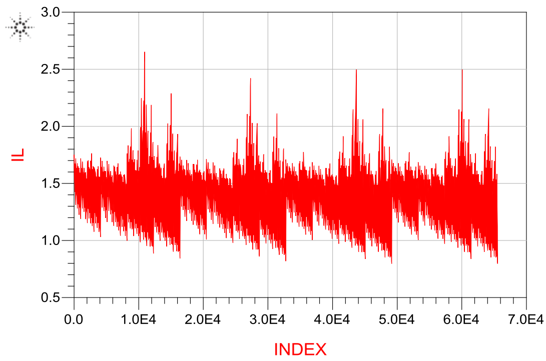
Figure 4-24: (a) S11 of Impedance Tuner; (b) Linearity; (c) Insertion Loss of Tuner; (d) VSWR of Tuner at 9 GHz with series 3-bit inductor tuner



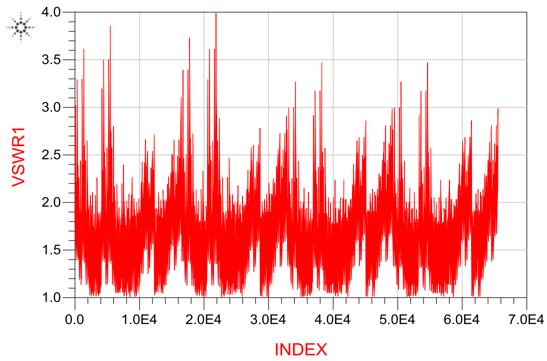
(a)



(b)

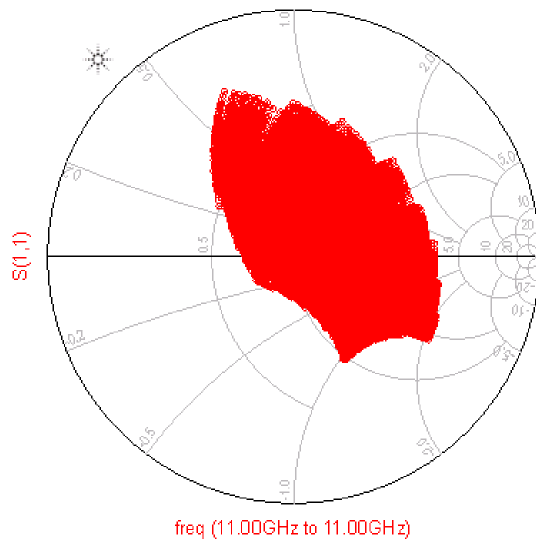


(c)

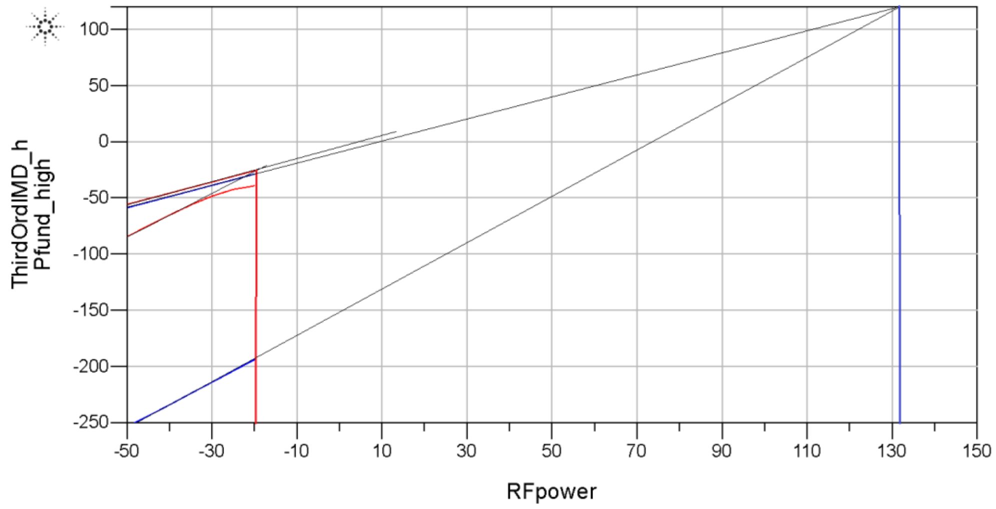


(d)

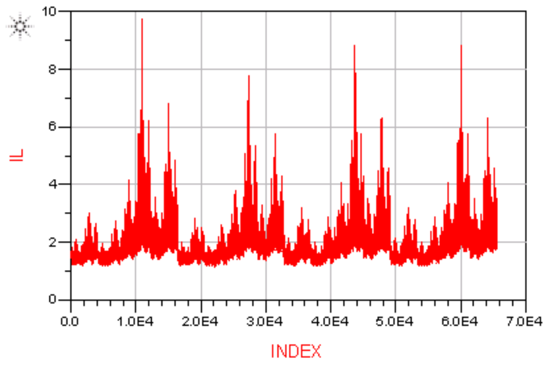
Figure 4-25: (a) S11 of Impedance Tuner; (b) Linearity (c) Insertion Loss of Tuner; (d) VSWR of Tuner at 10 GHz with series 3-bit inductor tuner

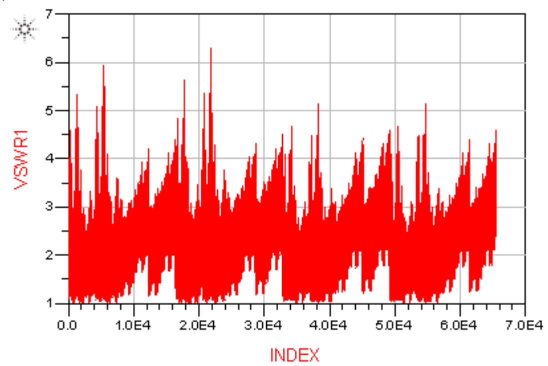


(a)



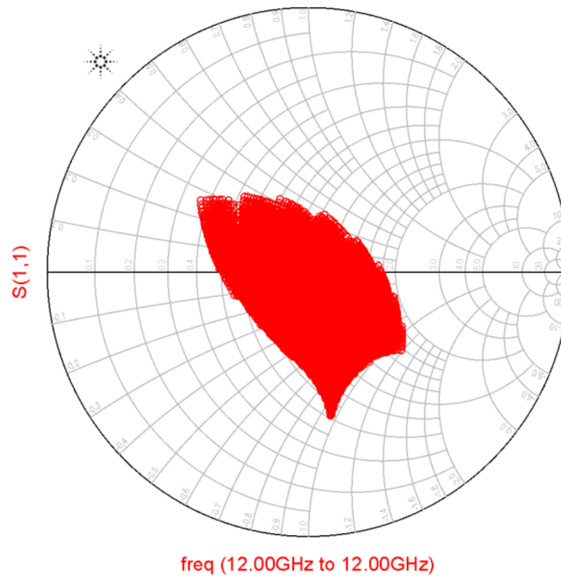
(b)





(c) (d)

Figure 4-26: (a) S11 of Impedance Tuner; (b) Linearity; (c) Insertion Loss of Tuner; (d) VSWR of Tuner at 11 GHz with series 3-bit inductor tuner



(a)

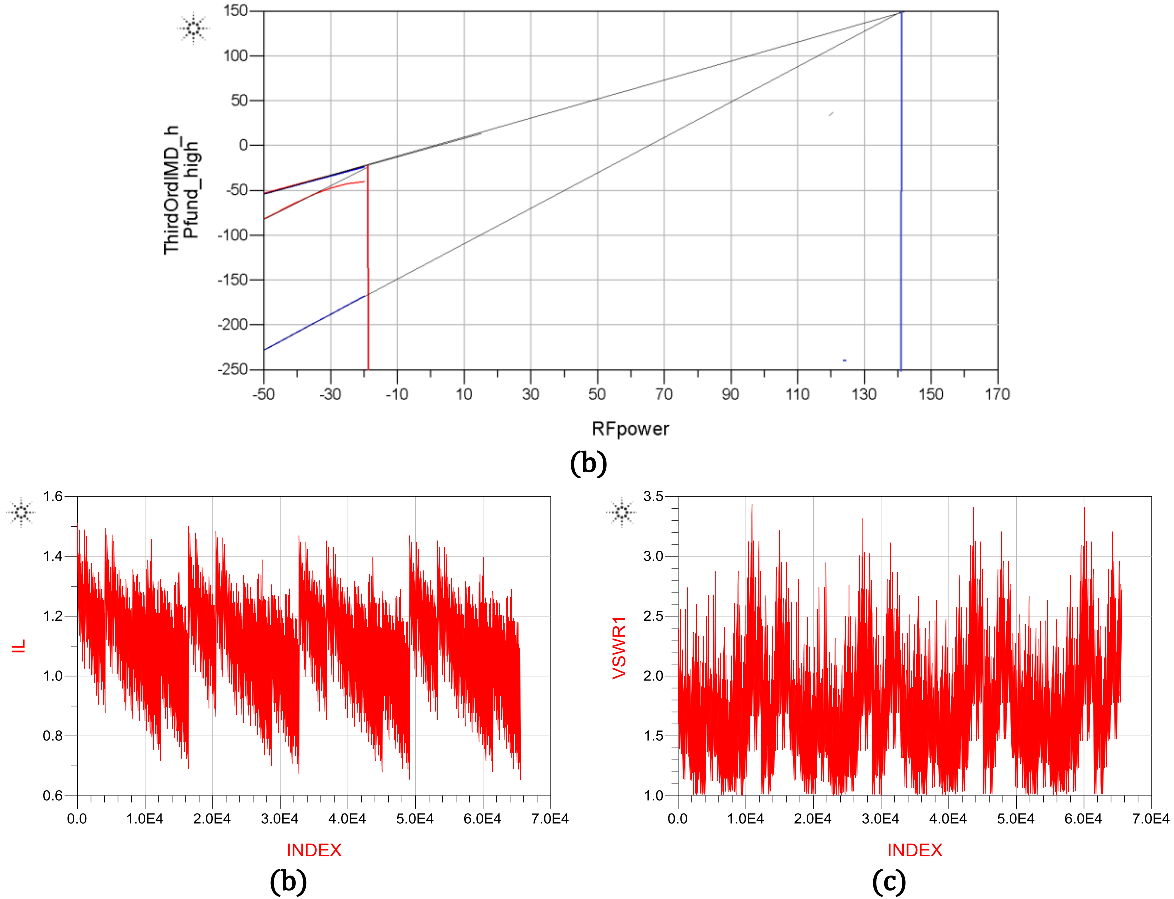


Figure 4-27: (a) S_{11} of Impedance Tuner; (b) Linearity; (c) Insertion Loss of Tuner; (d) VSWR of Tuner at 12 GHz with series 3-bit inductor tuner

Table 4-2: 16-Bit Impedance Tuner Parameters with 3-bit inductor tuner

Frequency	Real Impedance Range	Imaginary Impedance Range	VSWR	Maximum Insertion loss of Tuner	Approximate Smith Chart Coverage
8 GHz	10-80 Ω	-j40 to j80	3:1	3 dB	25 %
9 GHz	10-100 Ω	-j40 to j70	3:1	2 dB	21 %
10 GHz	20-100 Ω	-j40 to j60	3:1	1.8 dB	18 %
11 GHz	30-150 Ω	-j30 to j80	3.5:1	3 dB	22 %
12 GHz	20-100 Ω	-j40 to j50	3.5:1	2.5 dB	15 %

4.5.4 Conclusion

The 16-bit impedance tuner presented in this work shows good Smith chart coverage while having low maximum insertion loss for 9 to 10 GHz. With the antenna port matched to 50 Ω, the tuner generates approximately 15 to 80 Ω tuning range for 9 GHz, 20 to 200 Ω for 9.5 GHz, and 20 to 200

Ω for 10 GHz with a single series inductor. The maximum insertion loss of the tuner as 1.2 dB was obtained at 9.5 GHz. Majority of the tuner indices for VSWR simulation falls at a ratio of 2:1; however, for the given number of indices, the VSWR is high. The drawback of the single inductor tuner is its bandwidth of operation, which is optimized at 1 GHz with the frequency of operation from 9 to 10 GHz.

The modification design presented with added 3-bit series inductance tuner increased the frequency of the operation from 8 to 12 GHz. However, with increased bandwidth, an increase in insertion loss of the tuner with slightly higher VSWR and lower percentage of Smith chart coverage was realized.

In this Chapter, a brief description of tuner design parameters was discussed. A single series inductor π-network matching network was designed to operate at 9 to 10 GHz. A modification of the circuit was also presented to increase the frequency of operation from 8 to 12 GHz.

5

Frontend Module

This section will discuss the FEM and integrated SPDT that has been submitted for fabrication to CMC. The PA consists of 2 W of output power and upwards of 12 dB of gain from the LNA at 10 GHz with a total of 4x2 mm allocated space for fabrication. It was of key importance not to degrade the receiver and transmitter performance while designing the SPDT. In this Chapter, the design will be discussed and a layout of the complete FEM will be presented. Thereafter, EM-simulation results of the PA, LNA, and SPDT will be shown to demonstrate the performance of the FEM.

5.1 Design

The switch was integrated to make a FEM at 10 GHz. The PA and LNA (designed by fellow group researcher) was incorporated in the module. The requirement for the PA was to provide 2 W matched with 50 Ω and LNA to provide a gain greater than 12 dB. A one state series-shunt configured SPDT was designed to be utilized as T/R switch operating at 10 GHz. For each throw, one 2x200μm series FET and one 2x200μm shunt FET was used to bias at -4.5 V and 0 V. The complete layout of the FEM sent for fabrication is shown in Figure 5-1.

The LNA has two stages with a 160μm gate width GaN HEMT. Feedback topology was used to ensure adequate stability of the circuit. The DC bias of the LNA was set at V_{GS} of -3.76 V and V_{DS} of 20 V. The two stage, class AB PA was simulated at a drain voltage of 20 V and gate voltage of -2.3 V at 10 GHz.

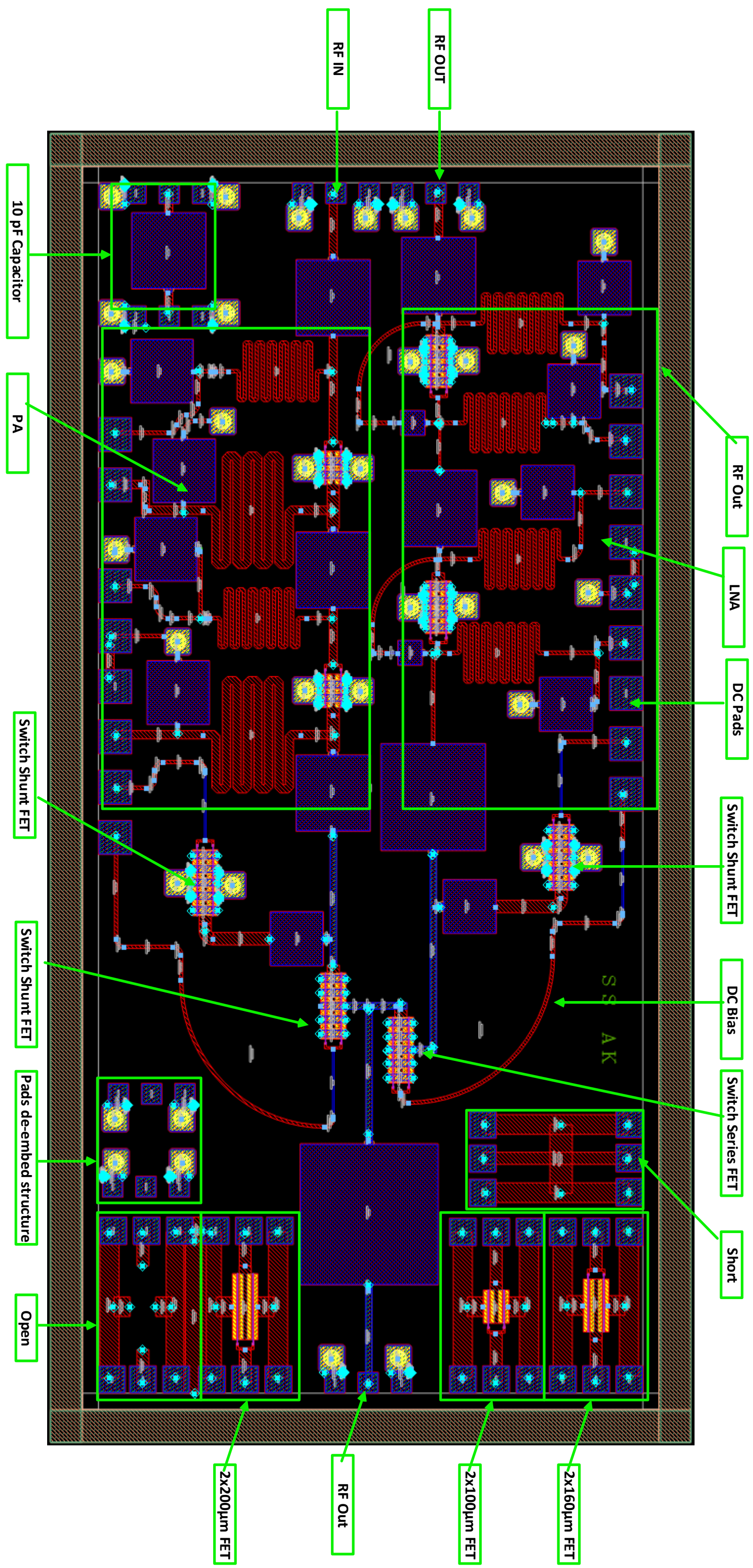


Figure 5-1: Layout of Complete FEM

There are two signal probes and two DC probes that were used (details of probes discussed in section 5.2). The design was made to ensure all probes are lined up accordingly. For DC probes, the spacing is 150µm while the signal probe spacing is 100µm pad to pad. There are several de-embedding and component characterization structures within the 2x4 mm die space. Three different HFET sizes were used; namely, 100, 160, and 200µm. All of the HFET's have a separate test structure to be able to characterize them. They are designed to be probed by ground-signal-ground (GSG) probes.

Seven DC probes were allocated for PA and LNA and two DC probe on each side were allocated for the switch. Additionally, there is a MIM capacitor with GSG pads to measure the capacitance of this device. The SPDT traces were modified to fit the LNA and PA structures. The DC feed using 1500 Ω nichrome resistors were connected to the gate of the FETs. An additional ME1 of 5x1µm was added to each end of the resistors to ensure minimum 5µm to ME1 length meets the design rule check (DRC). There are no sharp edges in the layout and all bends are designed using curve traces. The complete FEM is DRC error free and has been sent to NRC for fabrication.

5.2 Simulation Results

As mentioned, the SPDT was modified to integrate a T/R switch for FEM. As a result, bias points are slightly different then discussed in section 3.3.2. For the switch, ON state: 0 V and OFF State: -4.5 V biasing is used. The probes were modelled using 3 nH and 0.4 Ω. Each probe was connected from the pad to simulate the most accurate results. Figure 5-2 shows the insertion loss, isolation and return losses for the modified SPDT to fit within FEM.

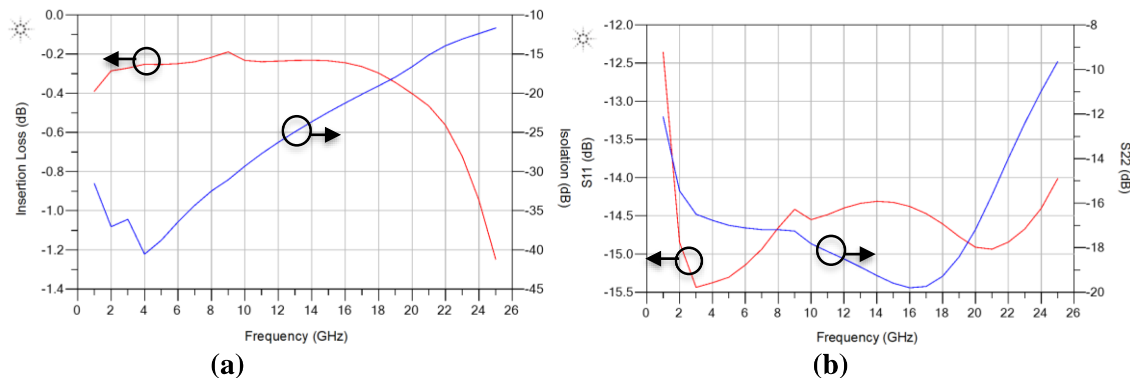
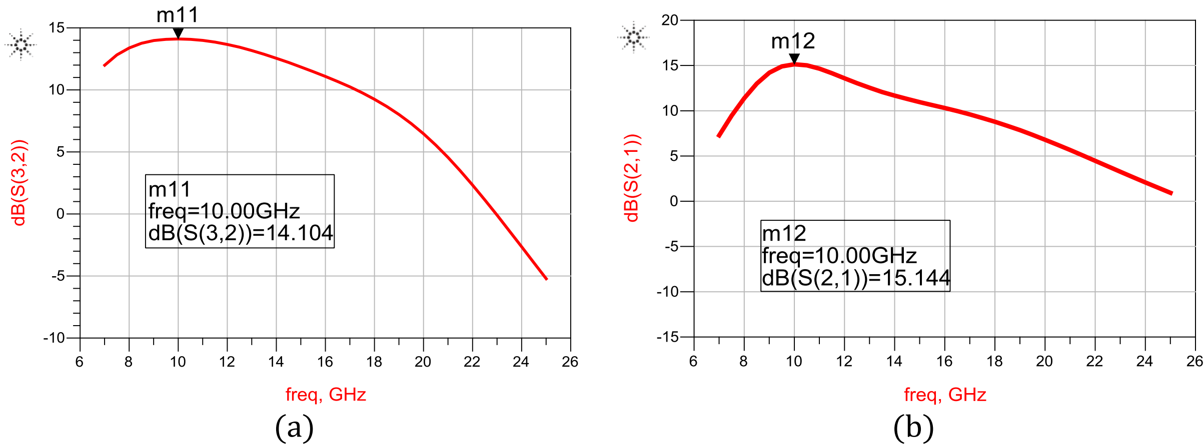


Figure 5-2: (a) Insertion Loss and Isolation versus Frequency; (b) Input and Output Return Loss versus Frequency for modified SPDT to integrate in FEM

Insertion loss of the modified SPDT is 0.22 dB while having isolation of -30 dB at 10 GHz. S_{11} and S_{22} of the switch indicates a good broadband response as it was found to be -14.5 dB and -18.3 dB

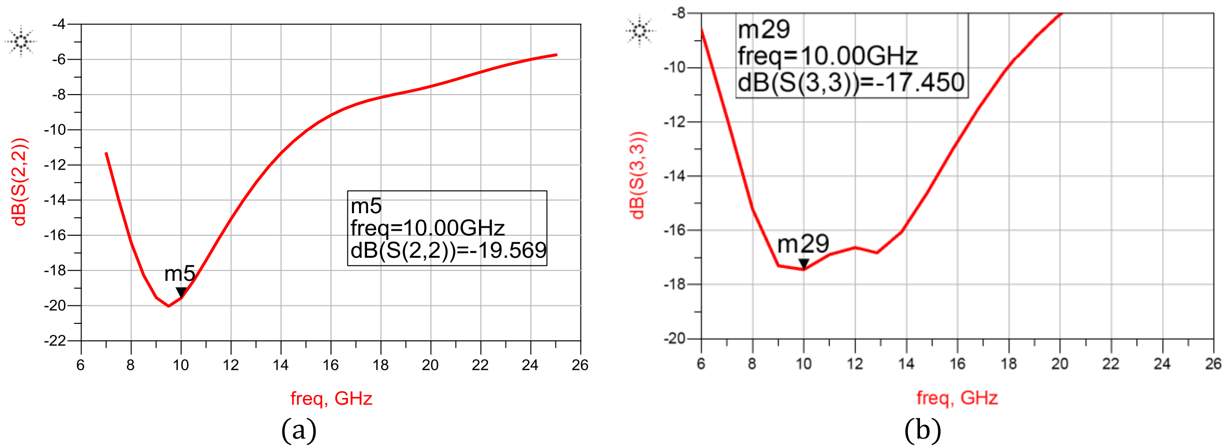
respectively at 10GHz. Figure 5-3 shows a plot of the total receiver and transmitter forward gain versus frequency. The receiver S_{21} was found to be 14.1 dB and 15.1 dB for transmitter.



(a) (b)

Figure 5-3: (a) FEM Receiver Forward Gain versus Frequency; (b) Transmitter Forward Gain versus Frequency

Figure 5-4 presents the S_{11} and S_{22} of the receiver chain and was found to be below -19.6 dB and -17.4 dB respectively.



(a) (b)

Figure 5-4: (a) FEM Receiver Input Return Loss; (b) FEM Output Return Loss

Transmit chain (PA and SPDT) was biased to display improved performance for large signaling. Figure 5-5 displays the transducer power gain and Power Added Efficiency(PAE) versus output power, where the output power of the FEM is 32.67 dBm.

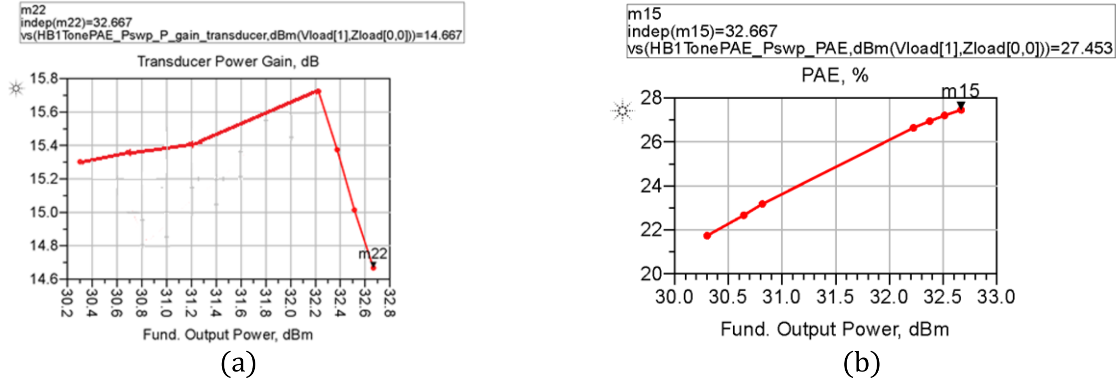


Figure 5-5: Power Gain versus Output Power of the FEM

Table 5-1, Table 5-2, and Table 5-3 represent the summary of the FEM parameters. It can be seen that the PA outputs 33.6 dBm power with 27.45% efficiency while consuming 180 mA of Supply Quiescent Drain Current. For the receiver chain, the forward gain was found to be greater than 12 dB for a frequency between 7 to 14 GHz, while having good input and output return losses.

Table 5-1: Receiver Performance Summary

Parameters	LNA	Switch	Receiver Chain
Forward Gain, S_{21}	$\geq$ 12 dB (7-15 GHz)	IL $\leq$ 1 dB (2-18 GHz)	$\geq$ 12 dB (7-14 GHz)
S_{11}	$\leq$ 10 dB (6-14 GHz)	$\leq$ 10 dB (2-18 GHz)	$\leq$ 10 dB (7-15 GHz)
S_{22}	$\leq$ 10 dB (3.8-15.5 GHz)	$\leq$ 10 dB (2-18 GHz)	$\leq$ 10 dB (7-18 GHz)

Table 5-2: Transmitter Performance Summary (Input at 18 dBm)

Parameters	PA	Transmitter Chain
Output Power	33.60 dBm	32.67 dBm
S_{21}	15.60 dB	14.67 dB
PAE	29.90 %	27.45 %

Table 5-3: FEM Power Consumption

Single DC Supply Voltage	Supply Quiescent Drain Current - Receiver	Supply Quiescent Drain Current - Transmitter
20V	80 mA	180 mA

The switch in the receiver chain was found to not significantly impact the forward gain, return losses and bandwidth coverage of the LNA. For the transmitter, the switch resulted in a 0.93 dBm of output power loss and a reduction of 2.45% in PAE.

5.3 Conclusion

In this Chapter, an SPDT was configured to be integrated in a 10 GHz FEM as T/R switch. The single stage series-shunt SPDT was modified to form a compact design presented in section 3.4 in order to connect to the LNA and PA. DC probe pads and GSG pads were planned with LNA and PA designer to ensure proper allocation of pads. Overall, the SPDT did not have significant negative impact for the receiver and transmitter. The FEM was submitted for fabrication with several test structures included, which will be used to characterize the models of the kit. A measurement of the FEM will be carried out as future work. This shows the application of RF switch as T/R operation mode in a 10 GHz FEM.

6

Conclusion and Future Work

6.1 Summary

Wireless devices have experienced an explosive growth in the last few years; a trend that is expected to progress even further. The drive for low power, low cost, and smaller form factor continues to inspire innovations in wireless products. GaN RF systems are beginning to achieve satisfactory levels of performance and expected to provide a much needed boost for the consumer wireless market. With the continuous consideration and implementation of GaN technology, new techniques and architectures are actively being studied. RF switches and impedance tuners are examples of such architectures. In this research, that the design of GaN based RF switches were examined for integration into RF transceivers with simple architecture while decreasing the number of components without sacrificing performance. This was demonstrated with the application design of impedance tuner and integration of SPDT in a FEM.

The efficient performance of GaN devices as RF switches was demonstrated through their high power handling capabilities, higher breakdown voltages, high linearity, and low ON resistance and OFF capacitances. In this work, the GaN 0.15µm kit provided by NRC was used to characterize the components (FET, capacitor, and inductor) to be used in switch topologies.

Subsequently, a Series only, Shunt only, and Series-Shunt SPST were designed in order to examine the characteristics of switch building blocks. The simulated performance of SPST created the fundamental building blocks of broadband SPDT, DPST and DPDT, which were also designed in this thesis.

A diamond structure double pole switch was designed to operate as DPST as well as DPDT. A Series-Shunt double pole switch design was also evaluated; however, due to low power handling capabilities, the switch can be integrated only for small signal power applications. A modification of

Series only switch to the double pole switch topology was presented. Improvement was observed in power handling capabilities with Series-only double pole switch design, with isolation degradation trade-off.

Impedance tuners were also investigated as application of RF switches. Various tuner design considerations and matching networks were presented, along with, a 16-bit reconfigurable π-matching network tuner designed for X-band operation. The tuner indicated good Smith chart coverage with low tuning complexity. The complete tuner is designed to be compact and easily reconfigurable.

Finally, the SPDT T/R switch was integrated in an X-band FEM. The integrated SPDT switch has low insertion loss and high isolation and it was shown to have minimal impact to the overall performance of the FEM.

6.2 Future Works

The switches presented generated promising results at X-band frequencies using the NRC 0.15 μm GaN process. As a result, the following recommendations are suggested for future work:

- The ON resistance of the device can be reduced to improve the switch performance. Improving the R_{ON} can benefit the figure of merit of the switch. The PDK should provide shifted-gate FET models or the ability to shift the gate placement between source and drain. This will enable a measurement and understanding of its impact on the RF performance of the device. By shifting the position of the gate asymmetrically towards source, linearity, and RF performance vary [77]. Therefore, the ability to control gate position between source and drain can help to improve performance of individual devices. The pad width of through hole VIAs is large (80μm); thus minimizing the size of the VIA will enable more compact designs.
- In this work, a 16-bit reconfigurable matching network was demonstrated. The π-matching network circuit presented needs to be improved for lower VSWR. Future direction would be to replace instruments with control circuits that are integrated with the tuner within the transceivers. One of the challenges for the control circuitries is to dynamically generate bias or control voltages to generate accurate matching. Furthermore, in order to actively correct the mismatch, the speed of the control voltages must also be analyzed.
- The list of design consideration for impedance tuners includes insertion loss, impedance coverage as seen in the Smith chart, complexity of the control tuning scheme, die size, and linearity. In this work, emphasis was given to impedance coverage in the four quadrants of the

Smith chart, compact circuit die space and simple control scheme. In future works, more efforts should be made towards lower insertion loss and higher linearity implementations. To reduce insertion loss, the capacitors must exhibit high quality factors while providing reasonable tuning.

- Although DPDT design presented in this work shows promising results, improvements need to be made in terms of the 1dB compression point. Further studies into DPDT specific switch topologies should be conducted to improve power handling capabilities and increased linearity, while having high isolation.

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