RFID Tag Design and Range Improvement

By

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Abstract

Radio Frequency Identification (RFID) is a short range radio technology for communication between two objects namely, a reader and a tag. Design of an RFID tag with the best range is always the motive of an RFID designer.

In this thesis two RFID tags were simulated, designed and manufactured. The first one is a semi-passive RFID tag, which also serves as a discrete prototype tag for the research group to master RFID tag designs. The user can program and further extend the use of this tag according to the requirements. This RFID tag is provided with JTAG interface to program and debug. The read range of this prototype tag is found to be 1m with reader EIRP of 30dBm. The second design is a passive tag which can be commercialized. It achieves a competitive read range of 2.9m for reader EIRP of 21dBm. The read range when measured in a practical implementation inside a building corridor was 15m.

Dedicated to my Parents

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Chapter 1: Introduction

Radio Frequency Identification (RFID) is a short range radio technology used to communicate between two objects namely, a reader and a tag. The primary feature of this technology is its use in automatic tracking, identification, and localization of objects, but more generally in all walks of life from applications ranging from supply chain management to livestock management. Some of the common applications of RFID are toll collection without stopping, managing traffic, gaining access to buildings, preventing shoplifting and automobiles, accessing corporate campus and airports, dispensing goods, providing ski lift access, tracking library books, etc.

RFID and its applications seem uncomplicated and undemanding. But in reality, this technology has its elements in so various areas like system design, software development, RF and microwave theory, antenna theory, circuit theory, receiver design, integrated circuit design, materials technology, mechanical design, encryption and network engineering, to name a few. Hence, the constant increase in the number of engineers involved directly or indirectly in the development of RFID systems.

An RFID system consists of a small inexpensive device called a tag or a transponder and a more complex device called reader or interrogator. Generally, RFID tags are attached to objects, which need to be tracked and the reader is standalone and usually connected to a data processing unit. RFID systems use operating frequencies from 100 kHz to 10GHz as reported in Table I-1.

Table I-1: RFID Frequencies and applications [1]

Classification	Frequency Band	Application
LF	125/134 kHz	Access control, Animal ID
HF	13.56 MHz	Access control
UHF	303/433MHz	Transport
	866-928 MHz	Transport, Inventory Supply chain management
SHF	2.45 GHz	Transport
	5.6 GHz	Under development

1.1 Motivation

RFID tags have received a lot of attention in the recent past because of the multitude of applications they serve. Associated to the recent advancement in RFIC/ASIC chip technology that made it possible to have very low cost RFID transponder chips, RFID tags are increasingly becoming an integral part in our day to day lives. Therefore, it is really important to explore the steps for design and construction of the tag to efficiently use this technology in different applications.

The objective of this thesis is to design two different kinds of RFID tags (a semi-passive tag and a passive tag) and to outline the steps involved. A block level design was performed for the semi-passive tag, whereas the passive RFID tag design essentially involves choosing the transponder IC and designing the corresponding antenna. Both these tags use backscatter modulation to communicate back to the reader.

The purpose of the first prototype is to serve as a discrete prototype tag for the research group to master RFID tag designs. Any potential user can program and extend the use of this tag according to his/her requirements. This RFID tag is provided with JTAG interface to program and debug. The design of each block of the tag is discussed in detail.

The other objective of the thesis is to design a marketable passive RFID tag with a range of more than 5m with the EIRP of 30dBm, which can be used for personal identification. Nowadays passive tags are used for personal identification in a plethora of applications. For example, access card for students or staff in universities, in companies, or for toll collection. The designed passive tag can be used in any of the personal identification applications. To make it easy to carry, it is in the size of bank card. This card can also be deployed commercially.

1.2 Contribution overview

In this work, the first goal was to enhance the performance of a semi-passive RFID tag afforded by the collaborating company. However, because the RF section of the company's tag was not working, almost all the RF blocks representing the RF section were redesigned while the existing digital section was used as provided.

This work also includes the design of a passive tag for commercial deployment. This tag uses a transponder IC from the market and the work involves selecting the IC for the desired application and designing the related antenna within the size of a bank ATM card.

To summarize, the contributions of this thesis are the following,

- All the individual RF blocks of a semi-passive tag were designed, analyzed and optimized for the desired operation. In fact, modulator, demodulator and backscatter circuits were designed under the basic EPCglobal Gen 2 Class-1 standard. A coplanar inverted-F antenna (CIFA) was also designed and optimized to match the tag circuit impedance, leading to a reading distance of 1m.
- A passive tag using a commercial chip was designed and implemented for commercial deployment. It uses a modified dipole with a T-match and tip loading at its ends. The read range of the tag is 2.89m for a reader Effective

Isotropically Radiated Power (EIRP = P_rG_r) of 21dBm. When measured in a real scenario, the results showed a range of 15m in a building corridor. This range can be considered as commercially competitive.

1.3 Thesis outline

This thesis outlines the overall design of the two RFID tags and is organized as follows. Chapter 2 discusses the background of RFID tags related to the thesis. Starting with the history of RFID tags, the chapter proceeds to describe the different types and then to overview the RFID technology with its building blocks.

Chapter 3 starts with an overview of power harvesting in RFID tags. Several charge pump designs are discussed briefly before proposing the final design.

Chapter 4 outlines the three stages of an RFID tag namely, modulator, demodulator and digital section. Design of a demodulator is detailed.

Chapter 5 deals with the antenna design of the RFID tag. It first introduces the fundamentals of antenna and its design considerations and then the necessary background for the design of an antenna.

Chapter 6 explains the design of the second RFID tag aimed for commercial deployment.

Chapter 7 covers the fabrication, testing results of the tag and its building blocks, and presents the overall performance of the RFID tag.

Chapter 8 summarizes the work presented in this thesis and main contributions. Possible future works are also suggested in this chapter.

Chapter 2: Background and related work

2.1 History of RFID

The development of the RFID technology can be attributed to the convergence of radio broadcast technology and radar. An early work, which can be thought as one of the first in the field of RFID technology is "Communication by means of reflected power," published in 1948 [2]. Since then, the RFID technology has evolved over the years to reach what it is today. With the technical development in radio and radar in the 1930s and 1940s, the 1950s saw the exploration of RFID techniques. Some of the landmark inventions and papers published after this laid the foundations for the explosion of RFID technology. Some of those were "Theory of Loaded Scatters" in 1964 [3], "Remotely Activated Radio Frequency Powered Devices", and "Passive Data Transmission Techniques Utilizing Radar Echoes" [4] [5]. The 1960s also saw the beginning of commercial activities in the field of RFID. This was followed by increased interest among government laboratories, academic institutions, companies, developers and inventors in the 1970s [5]. And hence began the development of practical tags with a operational range of tens of meters. The 1980s saw full fledge implementation of RFID technology in transportation, personnel access, and animal tracking [5].

The 1990s witnessed widespread deployment of RFID tags in electronic toll collection, access control and a wide variety of other commercial applications all over the world. This time, a lot of companies joined the RFID race, such as, Texas instruments, Microdesign, CGA, Alcatel, Bosch, and Philips. New technological advancements also accompanied this growth. One example is the fabrication of microwave Schottky diodes on CMOS Integrated Circuits (IC). Low forward voltage drop and fast switching action

of a Schottky diode makes a voltage multiplier to operate at low input power levels. Several books were published in the field of RFID technology. One of the first was written by Klaus Finkenzeller in 1999 [5]. The later part of this decade saw tremendous growth of RFID technology with a lot of companies entering the industry.

The 21st century saw the implementation of smallest RFID tags with significant advancements in the IC technology. Number of components was scaled down to two namely, single CMOS IC and antenna, and RFID tags in different shapes started to emerge. Technical breakthroughs in the late 1990s made tremendous growth in the use of RFID tags in supply chain management and article tracking. The development of RFID still continues and its full potential is now limited only by the advancements in the areas of application software; development of privacy policy; development of supporting infrastructure to design, installation and maintenance, and others. Table II-1 shows the major milestones in the RFID technology over the years [5].

Table II-1: The decade of RFID [5]

Decade	Event
1940-1950	Further advancement in Radar; RFID invented in 1948
1950-1960	Early exploration of RFID technology; laboratory experiments
1960-1970	Development of the theory of RFID; start of applications field trial
1970-1980	Explosion of RFID development; tests of RFID accelerates; very early adopter implementation of RFID
1980-1990	Commercial applications of RFID enter mainstream
1990-2000	Emergence of standards. RFID widely deployed; RFID becomes part of everyday life
2000-	RFID explosion continues

2.2 Types of RFID tags

RFID as a prospective automatic identification technology is being applied to a wide variety of fields [6] [7]. In an RFID system, the tags storing data and communicating with a base station or reader can be attached to or incorporated into products, as animal implants or persons. A typical RFID system consists of a reader and a transponder; the latter, in general, has an antenna, an analog RF-front end and a digital IC core. The transponder itself can be completely passive [8], semi-passive [9], or active. Sometimes sensors are also included. The passive RFID tag obtains its power from the interrogating electromagnetic signal generated by the reader and thus requires no battery. Based on its functionality, EPCglobal standard classifies RFID tags into four different classes [10]:

1. **Class 0 and 1:**
   - Passive identity tags (usable range of 3 meters)
   - Backscatter (interrogator speaks first)
   - Lowest cost
2. **Class 2:**
   - Passive identity and memory tags (usable range of 3 meters)
   - Programmable
   - Backscatter (interrogator speaks first)
   - Security
   - Lowest cost
3. **Class 3:**
   - Battery assisted passive tags
   - More functionality on chip – memory, sensors, etc
   - Backscatter (interrogator speaks first)
   - 100 meter range
   - Moderate cost

4. **Class 4:**
    - Active battery tags (tags transmit carrier)
    - Active transmission (permits tag-talks-first operating modes)
    - 100 meter range
    - High cost

2.2.1 Passive Tags (Classes 0, 1 and 2)

These types of tags have no battery and should extract power from the RF energy transmitted by the reader. The received RF signal is rectified and the RF component is filtered to get DC voltage. The power control circuit in turn regulates and powers the circuits. Data from the reader is also extracted in the process using a demodulator and decoder. These tags use backscatter modulation to talk back to the reader. Fig. 2.1 shows the RFID system with passive RFID tag.

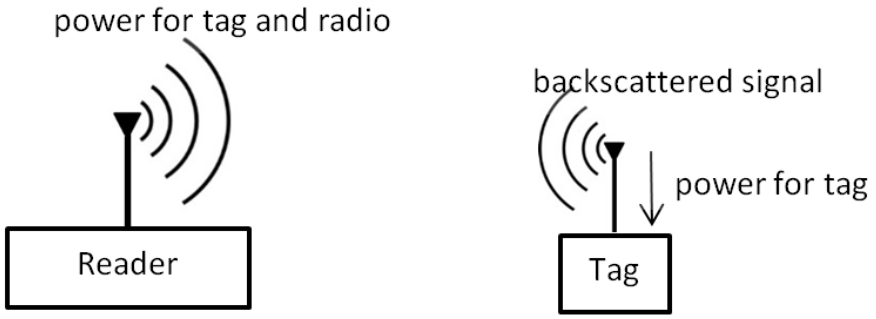


Fig. 2.1: Passive RFID system [11]

2.2.2 Semi-passive Tags (Class 3)

This type uses battery to power the tag circuitry, and hence the name battery-assisted passive. But, it still uses the backscatter communication for talking back to the reader.

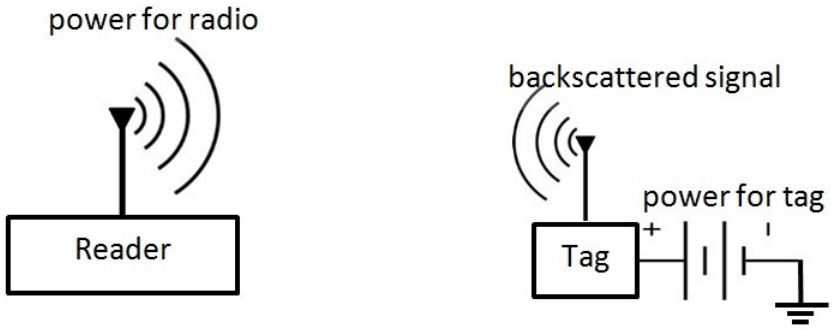


Fig. 2.2: Semi-passive RFID system [11]

2.2.3 Active Tags (Class 4)

Active tag works as in the conventional bidirectional radio communication system. It has a local power source, which also powers a transmitter.

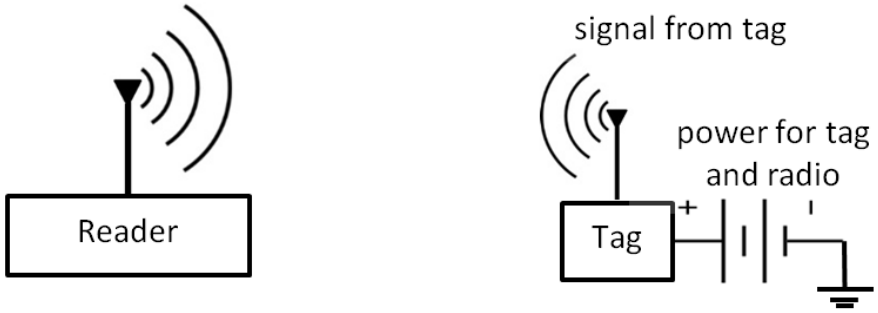


Fig. 2.3: Active RFID system [11]

2.3 RFID tag communication

The communication between the RFID tag and reader is either by electromagnetic radiation or by coupling. The most widely used standardized frequency bands allocated for this technology are low-frequency (LF, 125-134 kHz), high-frequency (HF, 13.56MHz), ultra-high-frequency (UHF, 860-960 MHz) and microwave (2.4 GHz and

5.8 GHz). Among these, LF and HF are based on quasi static magnetic flux coupling among the readers and tag coils. UHF and microwave systems involve electromagnetic interaction among true antennas and permit longer communication links [12].

The antenna along with the power sensitivity of the microchip are the important factors in deciding the overall RFID tag performance in terms of overall size, reading range, and compatibility with tagged objects. UHF RFID tag antennas are generally implemented as modified printed dipoles to get the desired inductive input reactance required for microchip conjugate impedance matching and to reduce antenna size.

2.3.1 Field regions

The space surrounding an antenna can be divided into three regions based on the behavior of the electromagnetic fields. These regions are the reactive near-field, the radiating near-field (or Fresnel), and the far-field (or Franhofer) as shown in Fig. 2.4 [13]. The far-field is the normal electromagnetic radiation region and extends till infinity. The radiated power density decreases as the square of the distance from the antenna. In the case of the far-field antenna, absorption of the radiated power by the receiving antenna has no effect on the power transmitted by the transmitter. On the other hand, the near-field region has reactive field due to the currents and charges in the antenna. These effects decrease more rapidly with distance than far-field region. As the coupling/absorption of the radiated power changes, it is fed back to the transmitter as change in the impedance.

2.3.2 Near-field and far-field antennas

A small loop antenna can be inductively coupled to a tag, even at UHF frequencies. When tag and reader are both small loops, only inductive coupling is present; and the reader is operating as a near-field device. Inductive coupling has the disadvantage to work for only small distances. Near-field tag antennas are used in applications where the size of the tag antenna is highly constrained. In this case, a simple loop antenna can be used. These loops do not radiate and also do not receive radiation. An example of near-

field antenna is shown in Fig. 2.5. Simple loop antenna has a parallel resonance at a circumference of about 0.45 λ. For diameter smaller than this, the loop looks like a simple inductive load [1] [11].

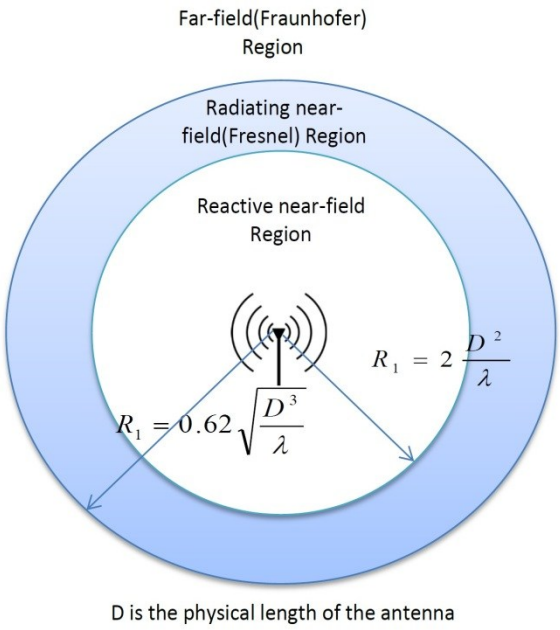


Fig. 2.4: Antenna field regions

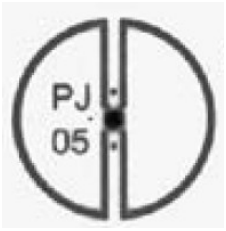


Fig. 2.5: Near-field antenna [11]

Most of the far-field UHF RFID tag antennas are modified printed dipoles. A printed half wave dipole acting as an RFID tag antenna is shown in Fig. 2.6. An unmodified half-wave dipole is not a good antenna for typical tag ICs. The antenna reactance is quite small to be matched to the tag IC and as such the half wave dipole is physically too big for most of the RFID tag applications.

So, some modifications need to be done for a decent performance without losing the simplicity of the dipole [1] [11].

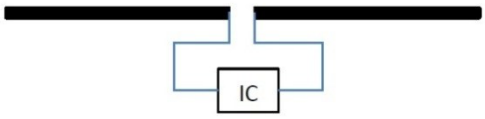


Fig. 2.6: Far-field antenna

2.4 Link-budget – Friis equation

In the case of an RFID tag, the Friis equation can be used for link budget calculations [14]. Link margin is the difference between the received signal power, P_R, and the sensitivity of the receiver. There will be additional losses to include in the Friis equation for making the link budget realistic. The range of an RFID system is the maximum distance at which the link operates with a signal level equals to the receiver sensitivity level.

When an EM wave propagates through the wireless medium, it experiences reduction in signal strength due to path loss. There are several path loss models proposed in different environments. One of the most prominent ones is the HATA model, which predicts path loss in urban, suburban and rural areas [15]. One of the usable models in the indoor environment is the ITU (International Telecommunication Union) Indoor Location Model [16] that estimates the path loss inside buildings or rooms, which is delimited by walls of any form. The link budget calculations can be modified to include these path loss models to get an accurate estimate of the range.

The available power received by the tag is governed by the Range Equation [17]. The fundamental power relationship between the transmitter and the receiver of any communication system begins with consideration of an isotropic radiation source, which emits power equally in all directions.

The power density on a hypothetical sphere of radius r can be calculated by dividing the transmitted power by the area of that sphere [13].

$$p(r) = \frac{P_t}{4\pi r^2} \qquad Watts/m^2 \tag{2.1}$$

Equation (2.1) is the power density that will be seen by the tag antenna, when the reader and tag are separated by a distance *r*. The tag antenna intercepts only a portion of the transmitted power depending upon the effective area A_e of that antenna. The received power, therefore, is given by,

$$P_r = p(r)A_e = \frac{P_t A_e}{4\pi r^2} \qquad Watts \tag{2.2}$$

Equation (2.2) gives the maximum power available at the tag, given an isotropic radiator and an effective area of the tag antenna. The FCC almost always specifies limits on radiation based on an EIRP. In North America, for example, the EIRP limit for UHF RFID is 4 Watts. The transmitted power P_t in equation (2.1) can be replaced by the EIRP:

$$P_r = EIRP\frac{A_e}{4\pi r^2} \qquad Watts \tag{2.3}$$

The relationship between the tag antenna gain G_r and the tag antenna effective area is

$$G_r = \frac{4\pi A_e}{\lambda^2} \tag{2.4}$$

where $\lambda = c / f$ is the free space wavelength, c is the speed of light, and f is the operating frequency. Replacing A_e in (2.3) using (2.4) allows us to come to a final expression for the available power at the tag due to a given transmit EIRP.

$$P_r = \frac{EIRP.G_r.\lambda^2}{(4\pi r)^2} \qquad Watts \tag{2.5}$$

As will be discussed later, a tag antenna is often a variation of a dipole. A classic half-wave (length = λ/2) dipole has a gain G = 1.64. Using EIRP = 4W, G_r =1.64, r = 10 m, and f = 950 MHz in equation (3.5) results in a receive power P_r = 41.4 μWatts. Clearly, the tag design must have extremely low threshold.

2.5 Factors limiting range

Equation (2.5) only indicates the power available to the tag antenna. The actual power accepted by the tag circuit could be significantly less, depending upon several loss mechanisms, including antenna mismatch, polarization mismatch, antenna misalignment, and environmental scattering. Any number of loss mechanisms can be added to (2.5) by multiplying by loss factors ranging from 0 to 1. For example, we can include a polarization loss factor p, where $0 \le p \le 1$ and an antenna mismatch factor τ, where $0 \le \tau \le 1$.

In equation (3.5) taking into account these loss mechanisms [18], we get,

$$P_{r(effective)} = \frac{ERIP.G_r.\lambda^2.p.\tau}{(4\pi r)^2} \qquad Watts \tag{2.6}$$

As was shown in [18], the mismatch factor τ is given by

$$\tau = \frac{R_c R_a}{|Z_c + Z_a|^2} \tag{2.7}$$

where $Z_c = R_c + jX_c$ is the tag chip input impedance and $Z_a = R_a + jX_a$ is the tag antenna impedance.

These equations can be used to compute the power available at the antenna terminals, given the transmit EIRP and the range. As mentioned earlier, the tag can only begin operation once the input power has exceeded a certain threshold P_{th}. Rearranging (2.6) allows us to compute the range r in terms of the other parameters including the threshold power and the signal wavelength λ:

$$r = \frac{\lambda}{4\pi}\sqrt{\frac{EIRP.G_r.\tau.p}{P_{th}}} \qquad meters. \tag{2.8}$$

For example, using the previous values plus a chip threshold power P_{th} = 10μW, a mismatch factor of 0.5, and polarization loss factor of 0.5, yields to a range r = 10 m.

2.6 RFID System Overview

In a Class-1, Generation-2 protocol system, a reader transmits information to a tag by modulating an RF signal in the 860 – 960 MHz frequency range. The passive tag receives both information and operating energy from this RF signal. If the transponder lies within the range of the reader, an alternating RF voltage is induced on the transponder antenna and is rectified in order to provide a DC supply voltage for tag operation.

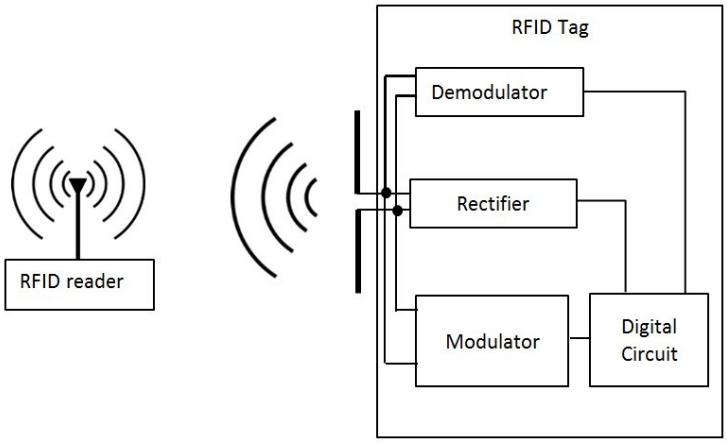


Fig. 2.7: UHF RFID System Diagram [1]

The reader receives information from a tag by transmitting a continuous-wave (CW) RF signal to the tag. The tag responds by modulating the impedance placed on the antenna terminals, thereby backscattering an information signal to the reader. Fig. 2.7 shows the RFID system diagram illustrating the RFID reader, tag and backscattering mechanism. The reader sends information to one or more tags by modulating an RF carrier using double-sideband amplitude shift keying (DSB-ASK), single-sideband amplitude shift keying (SSB-ASK) or phase-reversal amplitude shift keying (PR-ASK) at a bit rate ranging between 26.7 to 128 kbits/s. [11].

Before modulation with the carrier, the data is encoded in pulse-interval encoding (PIE) format, wherein data is passed to the tag by sampling the carrier wave at differing time intervals to indicate a 0 or 1 bit. Tags only respond after they receive commands from the reader, and there is a rigorous protocol for allowing a single reader to manage many tags during an inventory session.

The EPC global specification provides all details of the protocol for tag selection, identification and anti-collision. Once a command has been sent, the reader emits a CW signal to continuously provide power to the tags. The selected tag then backscatters energy by commutating the impedance applied at the input of the tag antenna. The modulation mechanism selectively places one of the two impedances across the antenna

terminals as commanded by the digital logic block (a low-power digital state machine). The tag can use either ASK or phase shift keying (PSK) modulation at a bit rate ranging between 40 to 640 kbits/s for FM0 baseband encoding or 5 to 320 kbits/s for Miller sub-carrier encoding [11].

2.7 Building blocks of an RFID tag

The architecture of a passive transponder is shown in Fig. 2.8. The system is divided into two main sections: the analog front-end and the digital section. The analog front-end performs all analog processing for DC power, receive signal detection/demodulation, and transmit modulation. The digital section decodes incoming data, responds to commands from the transmitter (reader), reads and writes to internal EEPROM memory, and encodes and transmits data to the modulator.

The coupling element is an antenna, typically is a dipole or a patch antenna. A voltage multiplier converts the input alternating voltage into a DC voltage, which is used by a series voltage regulator to provide the regulated voltage required for the correct operation of the transponder. The voltage multiplier is matched with the antenna in order to ensure a maximum power transfer from the transponder's antenna to the input of the voltage multiplier. A backscatter modulator is used to modulate the impedance seen by the transponder's antenna, when transmitting. The RF section is then connected to the digital section, which is typically a very simple microprocessor or a finite-state machine able to manage the communication protocol.

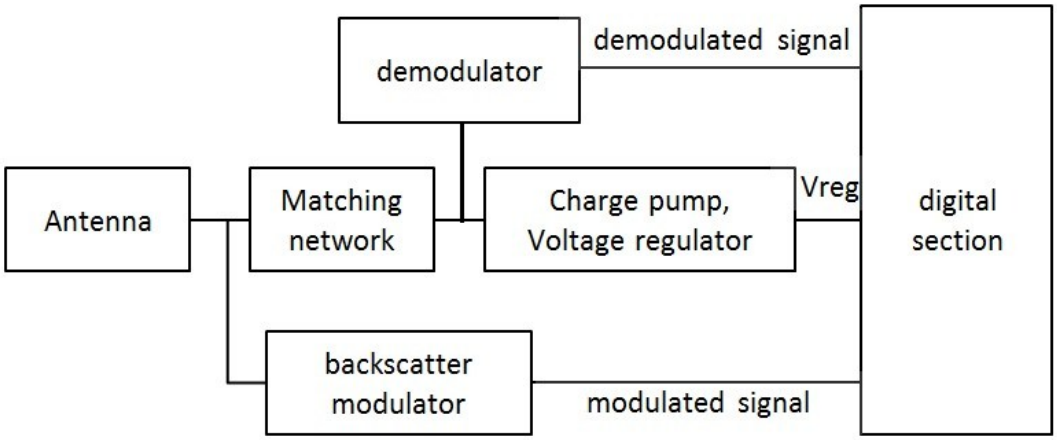


Fig. 2.8: Block diagram of passive RFID tag [8]

2.8 Conclusion

In this chapter, basic theory and background of RFID tags have been reviewed, highlighting the fact that the analog front-end is the key block of a passive RFID transponder. It rectifies the incoming RF signal, providing a regulated voltage supply for the digital core and other circuits. Furthermore, in receiving mode, it detects and demodulates the ASK modulated RF signal and provides a digital bit stream for the digital core. In transmitting mode, it changes the input impedance of the transponder between two states, in order to realize the backscatter modulation. In addition, it generates the power-on-reset signal that resets the digital core during power-up. For correct tag operation at the longest possible readout distance, the RF to DC conversion efficiency must be optimized in first place. Schottky diodes, which have low forward voltage and quick transition time, are frequently employed in the RFID front end [19]. The following chapters discuss the design of each building element of the analog front-end of a semi-passive RFID tag.

Chapter 3: Radio Frequency Power Harvest

3.1 Introduction

The operating power of passive RFID devices are harvested from the radio-frequency waves transmitted from the RFID reader. Based on a wireless link coupling mechanism, the wireless link between an RFID tag and a reader can be classified into two groups: near-field coupling and far-field coupling. Near-field coupling is basically an inductive coupling with frequencies up to few tens of MHz. Because of the close proximity with the reader, the coupling coils of near-field coupled RFIDs will have a large voltage at its terminals and is not that severely affected by nearby devices. However, this is not the case with UHF RFID tags, which work on far-field coupling.

Power harvesting is an important aspect while designing RFID tags since the efficiency of the power harvest is one of the key factors determining the range of the tag. The efficiency of power harvesting in UHF RFID tags is determined by different factors like, efficiency of the antenna, accuracy of the matching between antenna and circuitry, and efficiency of the voltage multiplier [8].

In the case of near-field passive wireless systems, the link established between the reader and the tag is like a transformer with the reader connected to the primary winding and the tag connected to the secondary winding of the transformer. A large voltage of the reader will be induced in the coil of the near-field tag. In this case, a diode bridge rectifier can be used to convert the carrier signal to DC.

Far-field RFID tags, on the other hand, require an efficient way to convert RF to DC, since the voltage at the antenna will be typically a few hundred mV.

In this case, voltage multipliers that increase the voltage levels and at the same time perform the RF-to-DC conversion are used. The following sections briefly discuss different types of voltage multipliers.

This chapter deals with the theory and design of a radio frequency power harvesting block. Different configurations of voltage multipliers, such as Cockcroft-Walton voltage multiplier, Dickson voltage multiplier, and modified-Dickson voltage multiplier are discussed. The target of the voltage multiplier design is to build a design which can detect power levels as low as -15dBm and to achieve voltage multiplication levels of about four times the input.

3.2 Voltage Doubler

The simplest voltage multiplier is a voltage doubler as shown in Fig. 3.1. It consists of a voltage clamper, formed by diode D1 and capacitor C1, and a voltage peak detector formed by D2 and C2. The operation of a voltage doubler is explained as follows. During the negative half cycle of the ac input V_{in}, the diode D1 conducts and the capacitor C1 charges to the peak voltage V_m. During the following positive half cycle, diode D1 will be reverse biased and the voltage across C1 will add on to the input voltage. Hence, voltage at point 1 is given by $V1=V_{in}+V_m$. The forward biased D2 will make the capacitor C2 charged to $2V_m$ [20].

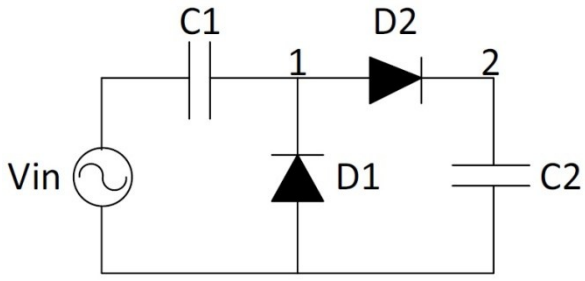


Fig. 3.1: Voltage doubler

To improve the RF-to-DC conversion ratio of the rectifier, Schottky diodes can be used because of their very low forward conduction voltage compared to p-n diodes. This feature enables the Schottky diode to be a more sensitive detector than a p-n diode. The main advantage of a Schottky junction compared to p-n rectifying junction is that Schottky junction operates with majority carriers only. The presence of minority carriers in a p-n junction diode slows down the recovery time when the forward biasing driving signal changes its polarity to opposite polarity. The instantaneous change of impedance of a Schottky diode with the polarity makes it to have very high rectification efficiency over a wide frequency range.

3.3 Cockcroft-Walton Voltage Multiplier

Multi-stage voltage multipliers are needed for obtaining a DC voltage of more than $2V_m$. One of the most famous voltage multiplier implementation is the Cockcroft-Walton Voltage Multiplier as shown in Fig. 3.2 [21][22]. In this circuit, two clock signals are fed with the input signal. The clock signals are supplied to turn the respective diodes on and off. Since the clocking signals ϕ and ϕ_1 are fed only to the first two coupling capacitors, one requirement for efficient multiplication of the Cockcroft-Walton Voltage Multiplier is that the coupling capacitance C should be much larger compared to the stray capacitance C_S at the coupling nodes [20]. This type of voltage multiplier is used for high voltage applications such as in high energy physics.

3.4 Dickson Voltage Multipliers

The modified version of Cockcroft-Walton Voltage Multiplier, with clock signals ϕ and ϕ_1 fed to all coupling nodes as shown in Fig. 3.3, was proposed by Dickson [20].

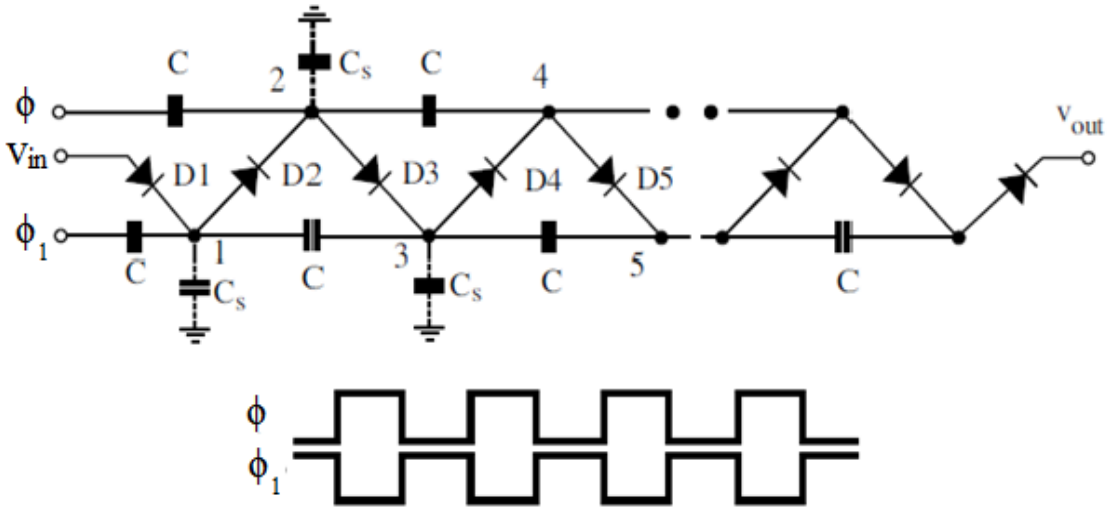


Fig. 3.2: Cockcroft-Walton Voltage Multiplier [21]

In this case both the coupling and the stray capacitance are driven by the clock signals, thereby eliminating the drawback of Cockcroft-Walton Voltage Multiplier. The output DC voltage of the N-stage Dickson voltage multiplier is given by,

$$V_{DC} = N.(V_m - V_T) \tag{3.1}$$

where V_T is the forward conduction voltage of the diodes and N is the number of stages. Schottky diodes are generally used in voltage multipliers due to their low conduction voltage, large saturation current, low junction capacitance, and small series resistance [22]. Dickson voltage multipliers can also be constructed in CMOS, MOSFET or pMOS diodes. The main drawback of a Dickson voltage multiplier with MOSFET diodes is that it will have a voltage loss of at least one threshold voltage across MOSFETs.

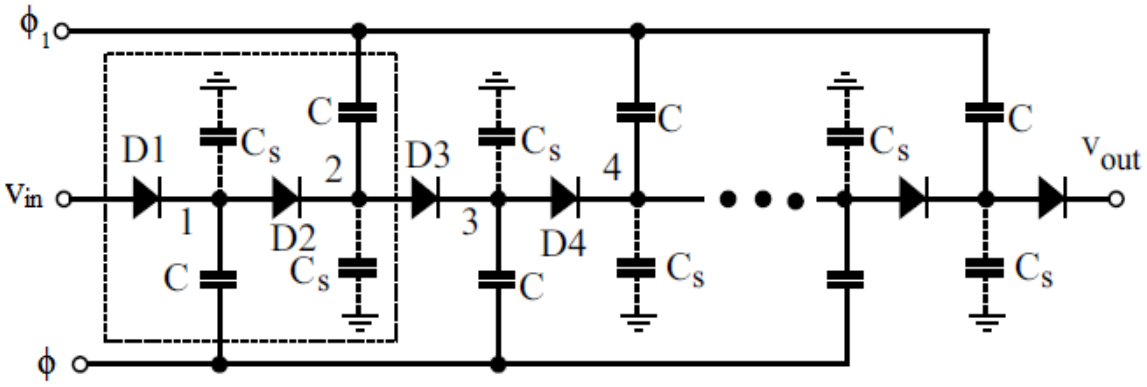


Fig. 3.3: Dickson Voltage Multiplier [20]

3.5 Modified Dickson Voltage Multipliers

The Dickson voltage multiplier can be modified for circuits having RF signals as given in Fig. 3.4. It can be noticed that, when the ϕ_1 and V_{in} terminals are grounded and the RF input connected to the ϕ terminal, each section behaves as a voltage doubler. This configuration is called Modified Dickson voltage multiplier. The performance can be improved further if a differential input is available and fed as V_{in+} and V_{in-} coupled to $C_{1,3,5,...}$ and $C_{2,4,6,...}$respectively. The output DC voltage of the N-stage modified Dickson voltage multiplier is given by (3.1).

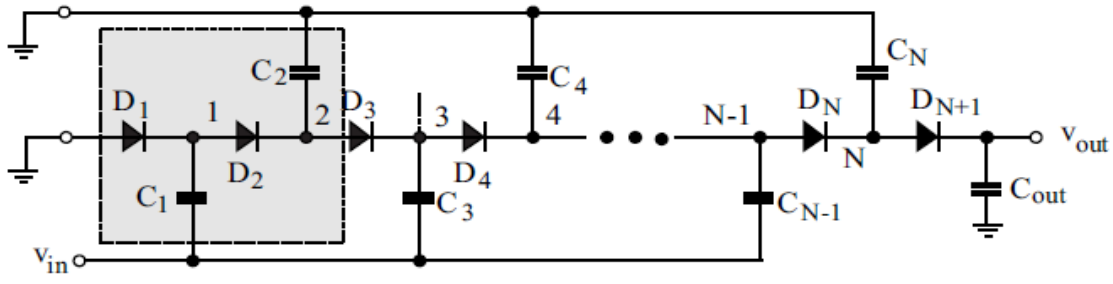


Fig. 3.4: Modified Dickson Voltage Multiplier [20]

Other types of voltage multipliers are also used in wireless micro-systems [22], like the Mandal-Sarpeshkar voltage multiplier, which overcomes the drawback of modified Dickson voltage multiplier with MOSFET-diodes or the Bergeret Voltage multiplier shown in Fig. 3.5. This latter was designed based on the conclusion that the reason of low power efficiency of Dickson voltage multipliers including modified Dickson is propagation of high-frequency signals throughout the circuits. Bergeret et al. [20] modified the conventional voltage multiplier to one with only one stage rectifier to generate DC voltage.

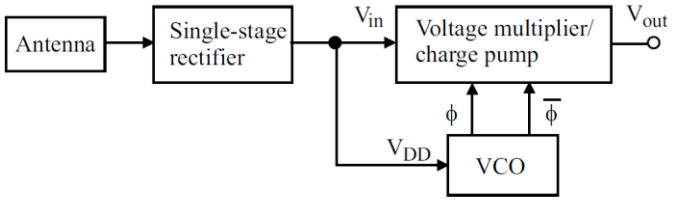


Fig. 3.5: Voltage Multiplier proposed by Bergeret et al. [20]

Among the various voltage multiplier configurations discussed above, the frequently used voltage multiplier configuration in UHF RFID is the modified Dickson voltage multiplier, because of the presence of RF signal in the system. All other types require a clock to turn the diodes on or off. Generally, it is used with a cascaded voltage regulator.

The general configuration of an N-stage voltage multiplier with cascaded regulator block is shown in Fig. 3.6. The voltage multiplier converts the incoming RF voltage into DC voltage and feeds the voltage regulator, thus providing the regulated voltage for the operation of the transponder. In this manner, the incident RF signal is converted to a DC supply voltage for the whole transponder chip.

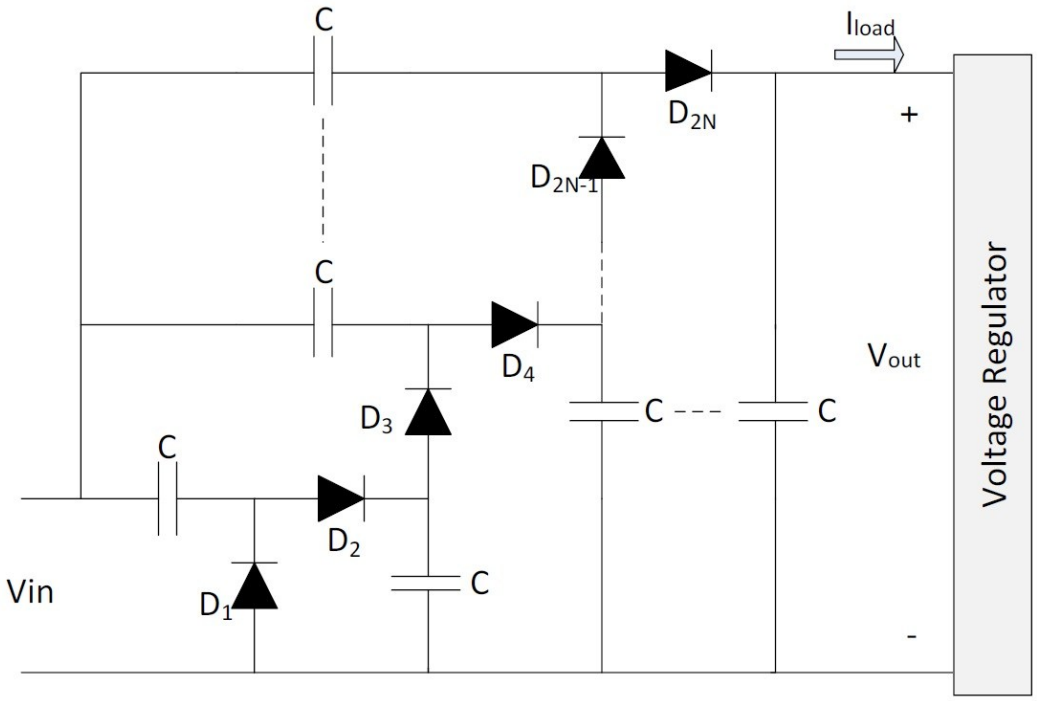


Fig. 3.6: N-stage voltage multiplier and cascaded voltage regulator [8]

As we add more stages, the output voltage will increase but at the expense of reduced power efficiency. The power efficiency of an N-stage charge pump is given by

$$\eta_{cp} = \frac{P_{load}}{P_{total}} = \frac{V_{out} I_{load}}{V_{out} I_{load} + 2NV_T I_{load}} = \frac{V_{out}}{V_{out} + 2NV_T} \tag{3.2}$$

where P_{load} is the total output power, V_{out} is the output voltage, I_{load} is the load current of charge pump. $2N*V_T*I_{load}$ is the power dissipated in $2N$ diodes used in the N-stage charge pump.

It can be seen that the power efficiency of the charge pump decreases as the number of stages increases for a given diode turn-on voltage and output voltages. This result is plotted in Fig. 3.7. The choice of the number of stages is a compromise between the desired multiplication level and the efficiency.

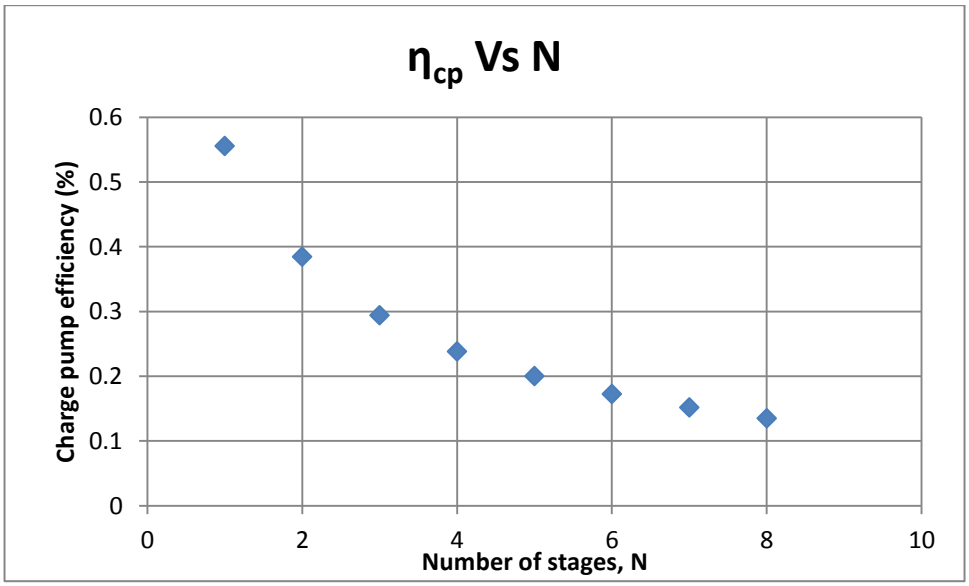


Fig. 3.7: Charge pump efficiency

3.6 Design – Simulation and Measurements

3.6.1 Design#1 – Using BAT62 diodes

A design based on the Dickson charge pump was performed for N= 4. After choosing the type of rectifier, the next step in the design will be to choose the component values and the diodes. The rectifier should fulfill two tasks: 1) it is the first stage of the RF-DC converter, and 2) it provides the envelope of the RF signal to the demodulator. In AC analysis, all capacitors will appear as short circuit and all diodes are connected in parallel (or anti parallel) to the RF input signal by the capacitors. In DC analysis, all capacitors are open circuit, and all diodes are connected in series to allow flow of a DC current. Thus, the generated voltage is approximately equal to [11]

$$V_{DC} = N.(V_{RF,in} - V_d) \tag{3.3}$$

where N is the number of stages, $V_{RF,in}$ is the amplitude of the RF input signal and V_d is the forward voltage of each Schottky diode. A 4-stage rectifier is designed to generate sufficient voltage for feeding the demodulating circuits. The Schottky diodes (BAT62) with low series resistance and low junction capacitance are used. The design and optimization is done in Agilent ADS and the simulation schematic and results are shown in Fig. 3.8-Fig. 3.11.

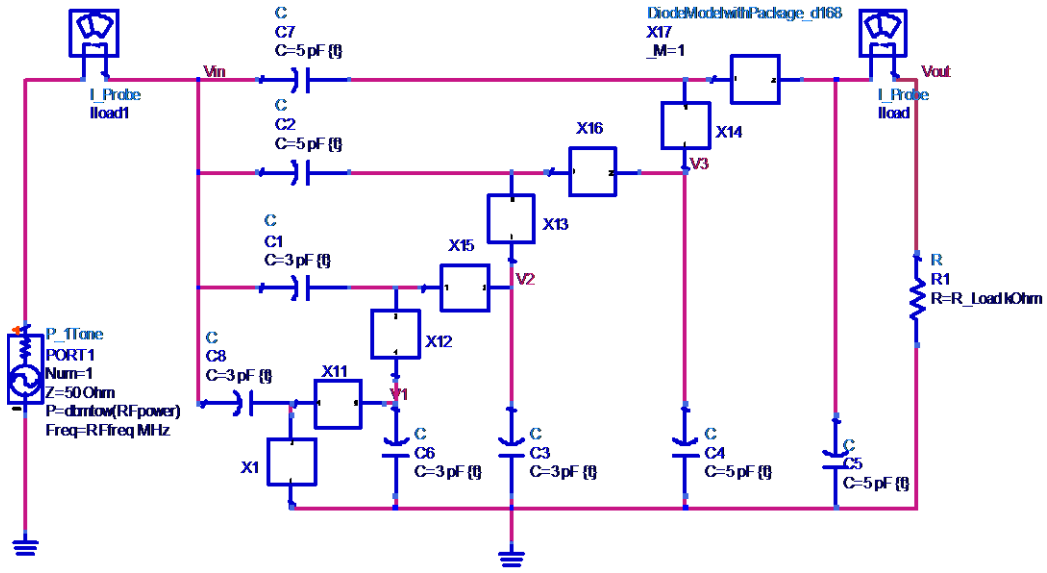


Fig. 3.8: Simulation schematic

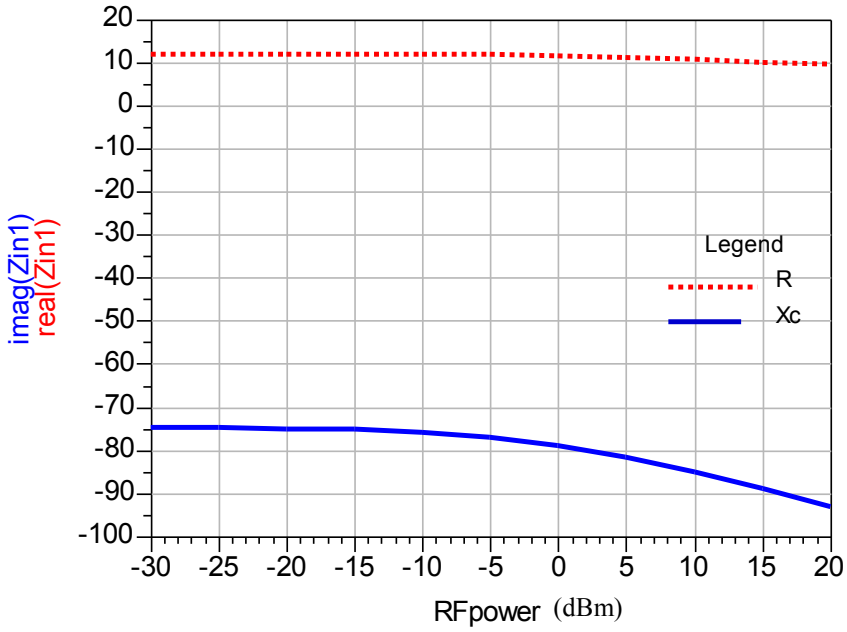
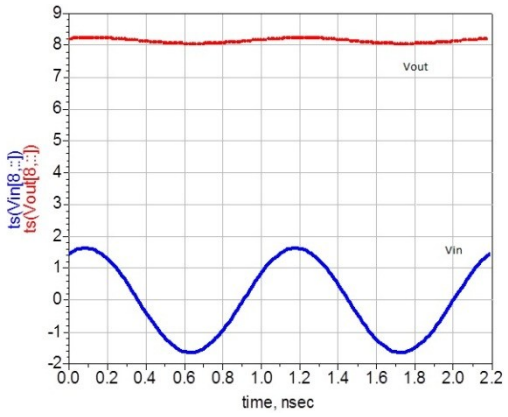


Fig. 3.9: Change in Input impedance (in Ω) with power

RFpower	C	R
-30.000	2.324E-12	11.948
-25.000	2.323E-12	11.942
-20.000	2.320E-12	11.925
-15.000	2.312E-12	11.883
-10.000	2.295E-12	11.796
-5.000	2.260E-12	11.635
0.000	2.204E-12	11.365
5.000	2.130E-12	10.972
10.000	2.046E-12	10.487
15.000	1.958E-12	9.948
20.000	1.872E-12	9.384
25.000	1.789E-12	8.818
30.000	1.711E-12	8.262

Fig. 3.10: C (in F) and R (in Ω) values of tag circuitry vs. Power (dBm)



RFpower	max(mag(Vin))	max(mag(Vout))
-30.000	0.016	0.005
-25.000	0.028	0.014
-20.000	0.049	0.044
-15.000	0.088	0.129
-10.000	0.157	0.346
-5.000	0.281	0.850
0.000	0.504	1.921
5.000	0.909	4.053
10.000	1.641	8.147
15.000	2.965	15.845
20.000	5.355	30.086

Fig. 3.11: Voltage maximum values (V).

3.6.2 Design#2 – Using ZBD diodes

For diode rectifiers, the minimum power required to turn ON one p-n diode is usually around 0.7V. In our case, the voltage multiplier circuit starts to operate as a multiplier when the diode forward voltage is around 0.3V. Table III-1 shows the input voltage, output voltage and their ratio for the designed voltage multiplier. The slight increase in voltage level at the output below this power level is mainly due to the charging of the capacitor in the output stage. One solution to this problem is to modify the design with diodes having lower threshold voltage. So, another type of diodes called zero bias detector (ZBD) Schottky diodes was used. ZBD diodes are specially made to have the lowest voltage for a given forward bias current, when compared to p-n junction diodes and low barrier height diodes. Figure 3.12 shows the forward I-V curves of a Si p-n junction diode, a low barrier height Schottky diode, and a ZBD Schottky diode.

There are several suppliers for this ZBD Schottky diode. Avago's HSMS-285x family of zero bias Schottky detector diodes is best suited for applications in small signal levels (P_{in} < -20dBm) at frequencies below 1.5GHz. These diodes are ideal for applications where a DC bias power supply is not available. The diode has a typical tangential sensitivity of -57dBm at 915MHz.

Table III-1: Output and input voltage (V) for various input power levels (dBm)

RFpower	max(mag(Vin))	max(mag(Vout))	Vol_Ratio
-30.000	0.016	0.001	0.085
-25.000	0.028	0.003	0.121
-20.000	0.049	0.010	0.204
-15.000	0.088	0.034	0.393
-10.000	0.156	0.133	0.852
-5.000	0.278	0.485	1.743
0.000	0.497	1.385	2.785
5.000	0.894	3.259	3.646
10.000	1.610	6.863	4.263
15.000	2.848	12.221	4.290
20.000	4.895	18.954	3.872

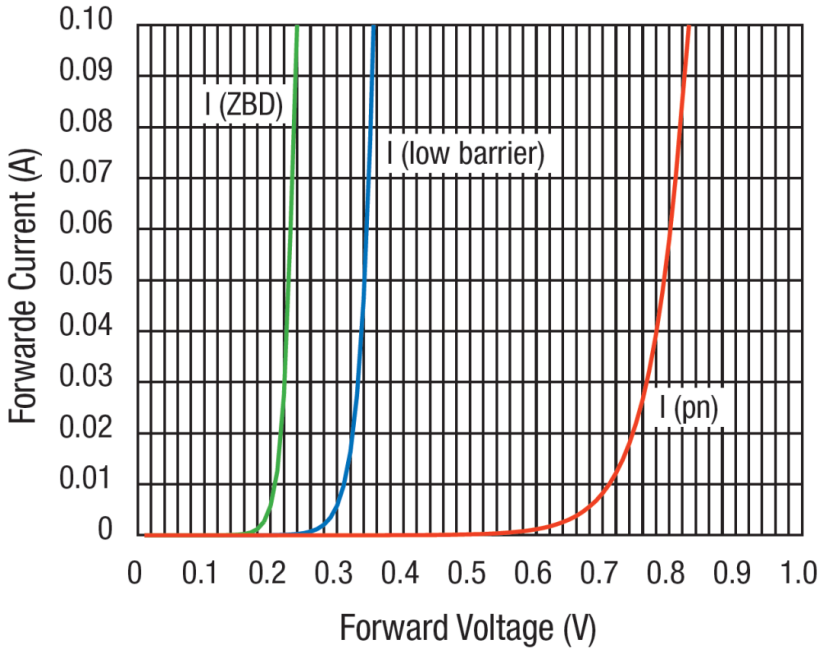


Fig. 3.12: Typical Forward current vs. Forward voltage for different diodes [23]

The simulation was done in Agilent ADS (Fig. 3.13) using the diode SPICE model. The results are shown in Fig. 3.14 and Fig. 3.15. It can be seen that the threshold power required for the diode to operate has come down and the voltage multiplication has been achieved at very low power levels. Estimating the range for minimum input power level required for a reasonable operation of the multiplier circuit gives the expected maximum range. The minimum power required for the operation of the tag is -15dBm at the input.

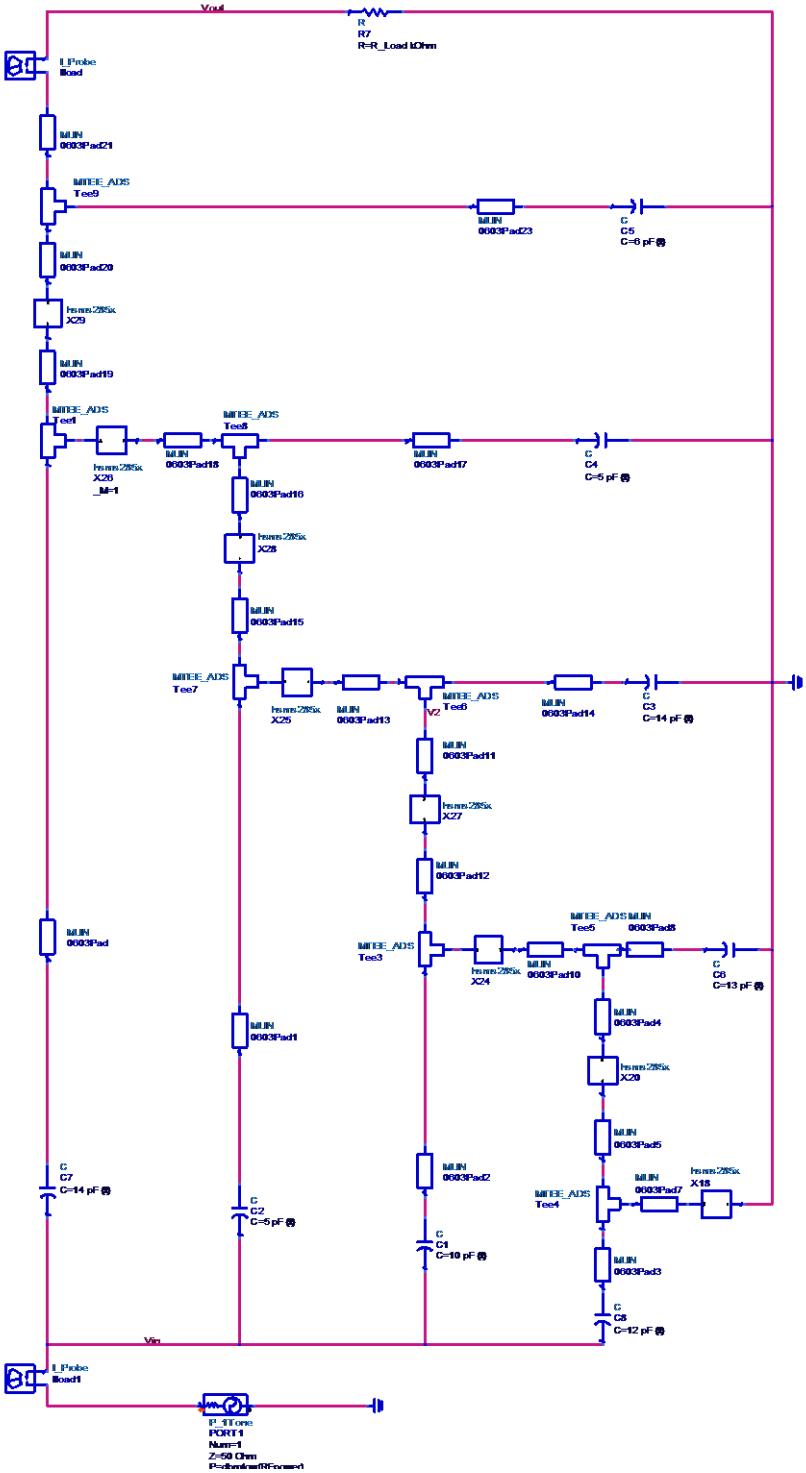


Fig. 3.13: Simulation schematic

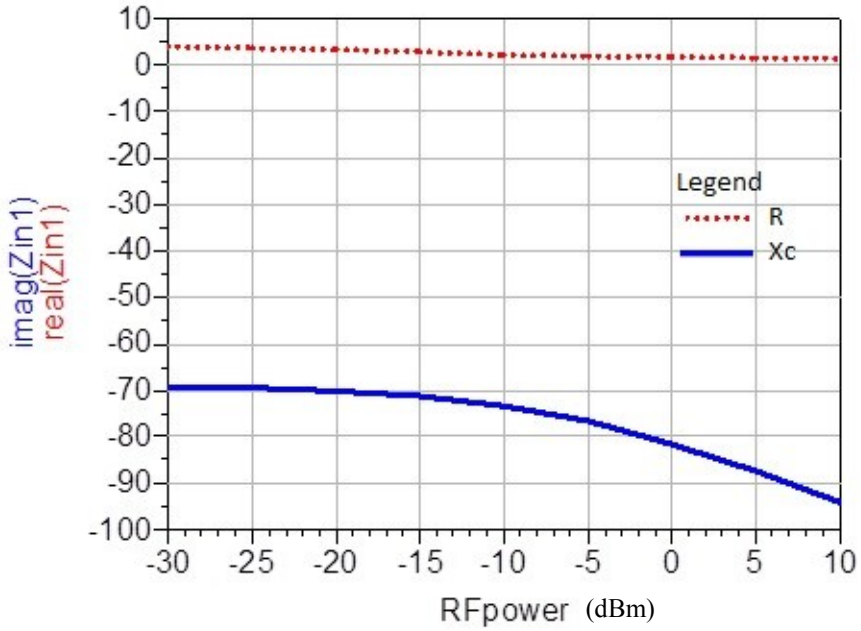
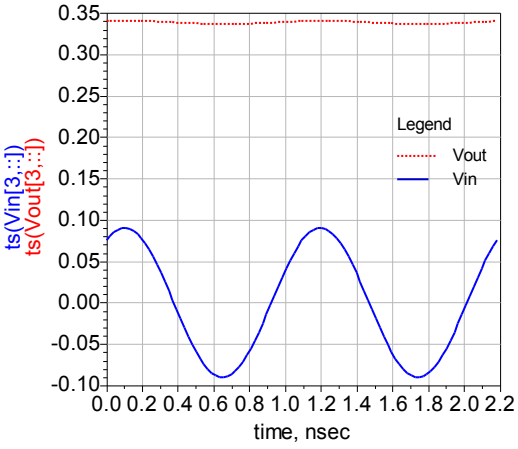


Fig. 3.14: Impedance (Ω) of tag circuitry Vs Power



RFpower	max(mag(Vin))	max(mag(Vout))
-30.000	0.016	0.015
-25.000	0.028	0.045
-20.000	0.050	0.130
-15.000	0.090	0.339
-10.000	0.163	0.784
-5.000	0.295	1.661
0.000	0.534	3.326
5.000	0.969	6.409
10.000	1.755	12.032

Eqn Vol_Ratio=mag(max(Vout)/max(Vin))

Fig. 3.15: Simulation Results - Output and input maximum voltage (V)

3.7 Conclusion

Various types of voltage multipliers have been studied. The target was to design a charge pump which can detect a low power of -15 dBm and have a multiplication ratio of about 4 times. The modified Dickson charge pump with 4 stages was retained for the voltage multiplier. A comparison between different diodes was performed and the ZBD diode was selected. The simulation results show that, using a low barrier Schottky diode, voltage multiplication of 3 times is achieved at input power of -5dBm, whereas it is achieved at -15dBm when using ZBD diodes.

Once the received signal level is increased, the next stage will be to extract data from the signal. The demodulator circuit does this and is explained in the next chapter. On the other hand, modulation of the data from the tag is achieved by backscatter, which is also explained in the next chapter.

Chapter 4: Data modulator, demodulator and digital section

4.1 Introduction

Generally RFID signals are digitally modulated. A simple example is on-off keying (OOK), in which a binary '1' is indicated by a large signal power and binary '0' is represented by a small or zero signal power (Fig. 4.1). Any circuit, which can change the output power, can be used to make an OOK signal (For example, a switch).

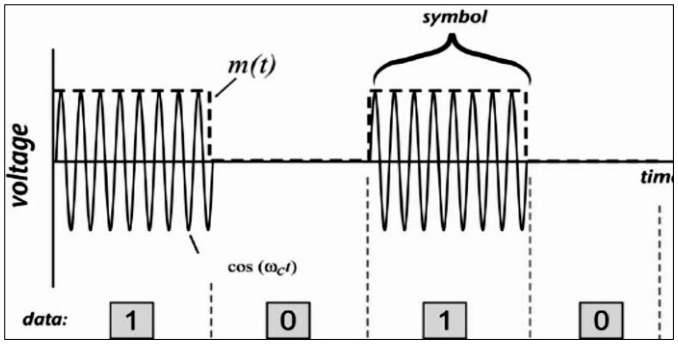


Fig. 4.1: OOK signal [11]

The passive RFID tag extracts the power transmitted from reader. Hence, once the power is interrupted, as in the case of OOK, the tag stops working. Therefore, OOK signal is not desirable for a passive RFID tag. If the data from the reader contains bits of zeroes for long time, the tag will get turned off. This problem can be avoided by coding the binary data before modulation. An example of a coding is pulse-interval encoding (PIE) (Fig. 4.2). The coded signal is used to modulate the carrier.

In this case, even for binary 0 there exists a short full-power interval, which will be adequate for the operation of the circuit. This scheme is used in EPC Global Class 1 Generation 2 reader. Fig. 4.3 shows a pulse-interval encoded OOK modulation of carrier wave.

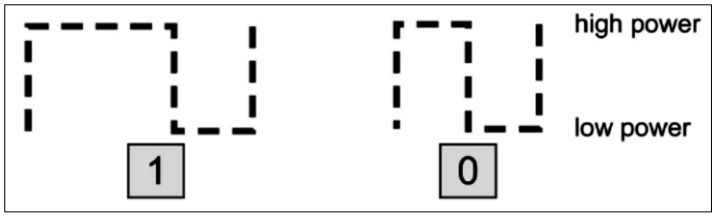


Fig. 4.2: PIE [11]

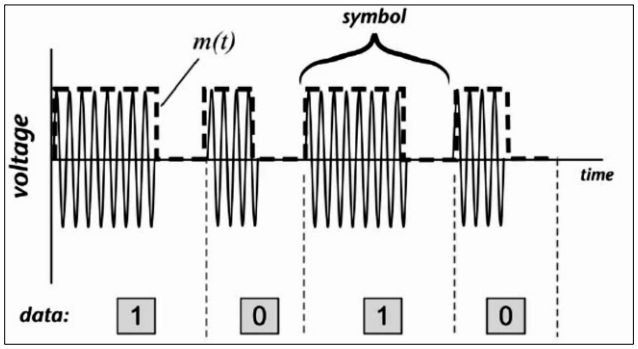


Fig. 4.3: Final modulated carrier wave [11]

Once the modulated RF signal from the reader is received at the RFID tag, the next step will be to extract the information. The demodulator can be a simple circuit which extracts amplitude variations of the RF signal (as in the case of the ASK demodulator shown in Fig. 4.4) or a much complicated circuit used for Pulse-interval-encoded data (as shown in Fig. 4.5). The ASK demodulator circuit simply involves extracting the RF envelope and then comparing that to an average voltage of received RF power. A capacitance *C* with a storage time longer than the RF cycle but short compared to the length of data-carrying modulation pulses will do the envelope detection with a resistive discharge path as shown in Fig. 4.4.

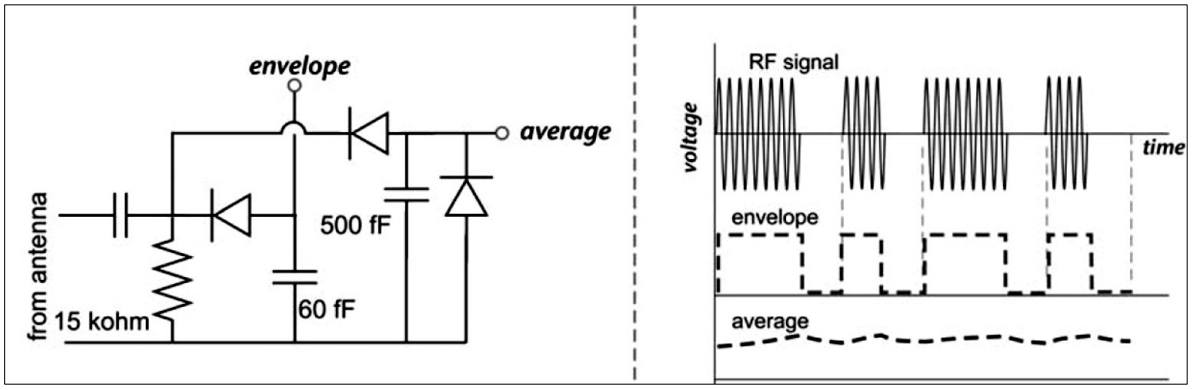


Fig. 4.4: ASK demodulator circuit [24]

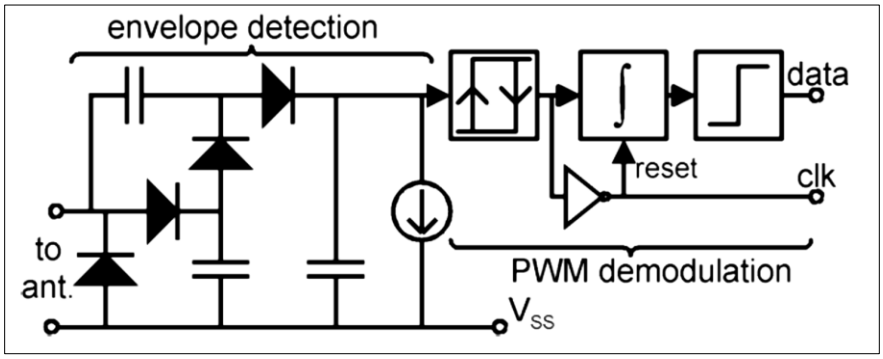


Fig. 4.5: Functional block diagram of Demodulator for PWM [19]

A similar circuit with a longer time constant, over many symbols, can be built to obtain the average voltage of the RF power. Generally, to obtain larger voltage levels for a given RF signal peak, a multi-stage charge pump can be used (as in Fig. 4.5).

The objective in the design of the data modulator is to build a simple ASK demodulator which can process the modulated data in the EPCglobal™ Class 1 Gen 2 UHF RFID standard. In the case of the modulator, it was desirable to design an uncomplicated backscatter modulator circuit, without the use of any amplifier circuit.

4.2 Design – Simulation and results

A four-stage Dickson charge pump is used as envelope detector and also to boost up the input signal. The fast charge pump detects the ASK modulated RF signal envelope, which is further processed by the peak detector (e.g., a 1N4148 diode). The envelope signal and its slowing moving part are then compared to produce the demodulated signal in digital format. The following two low-pass filters are used to average the boosted input signal with large time constant circuit, which eliminates the carrier noise and power ripple. The output voltages of these two low-pass filters are then fed to a comparator (MAX942CPA) to generate the output data bit-stream, which is the demodulated data. Schematic and voltage levels are shown in Fig. 4.6 and Fig. 4.7, respectively.

Time domain simulation of the demodulator circuit without the comparator was done in LTSpice. A modulated data for a stream of random bits were fed into the input of the circuit and the voltage at the output is viewed.

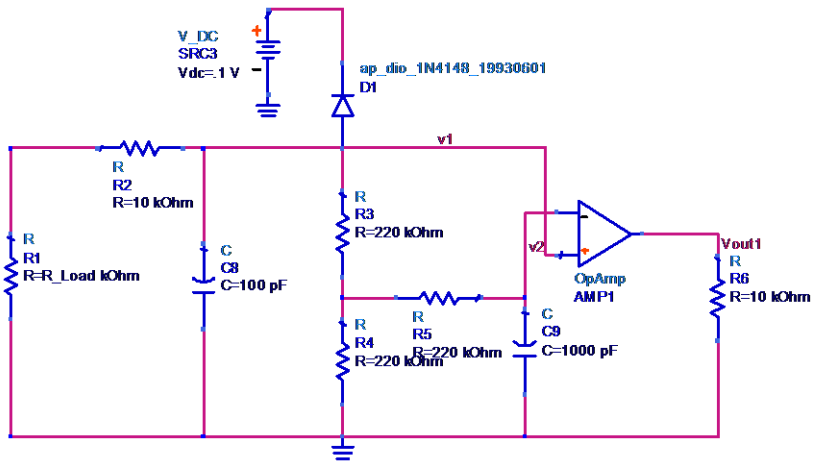


Fig. 4.6: Schematic of the AM demodulator

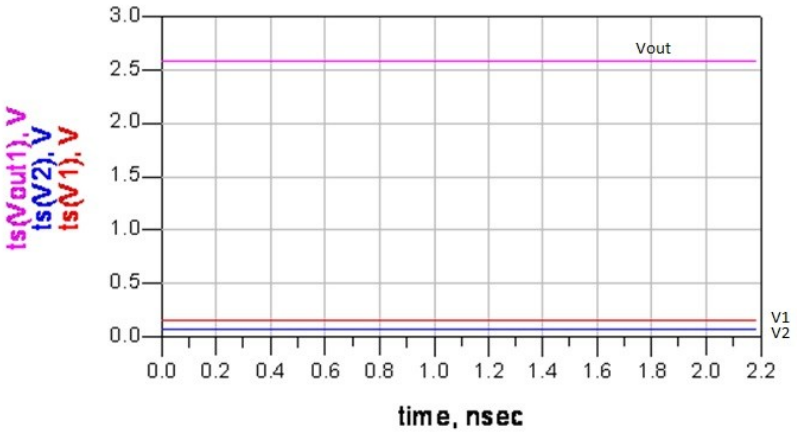


Fig. 4.7: Demodulator's output voltage versus input voltage

Fig. 4.8 shows the schematic and the simulation results are shown in Fig. 4.9. V(syn) is the input modulated carrier signal fed into the circuit, V(p2) is the output of the circuit, which will be fed into the Pin-2 of the comparator and V(p3) will be fed to the Pin-3 of the comparator IC. Pin-3 is the non-inverting input terminal of the comparator and Pin-2 is the inverting input terminal of the comparator. Based on the difference signal felt at both these pins, comparator switches the output between Vcc and 0V. It can be seen that the circuit does envelope detection and then feeds the envelope and a reference voltage levels to the input of the comparator, which in turn outputs the signal. This output will be the demodulated data from the signal received. In this simulation the differential impedance of the comparator is replaced with its equivalent impedance as given in the MAX 942 data sheet which is 8.2kΩ [Appendix A].

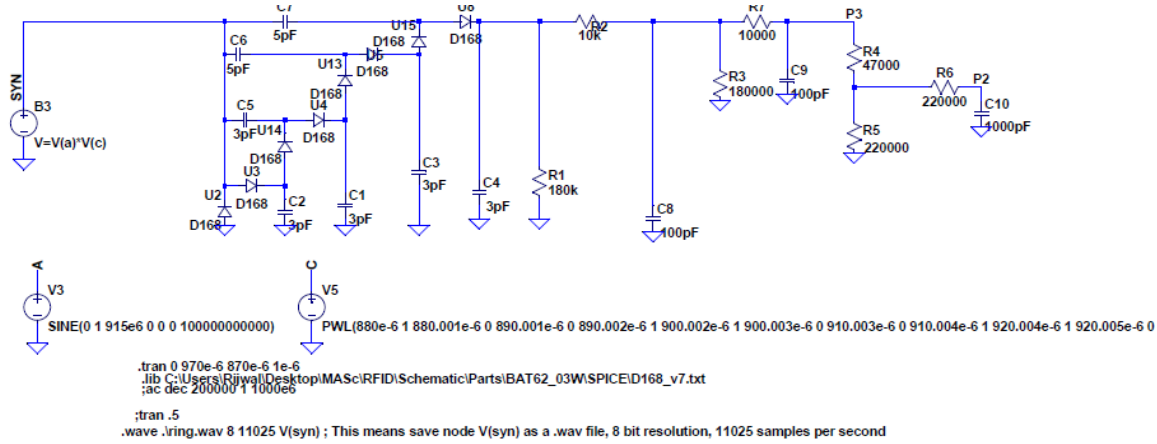


Fig. 4.8: LTSpice simulation schematic

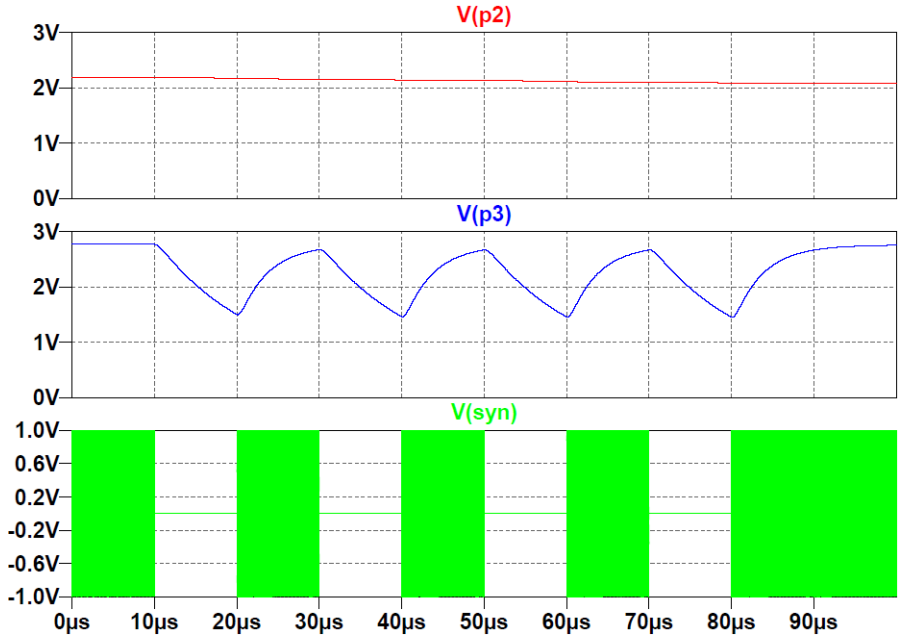


Fig. 4.9: Simulation results showing voltage levels at different nodes

The entire circuit with the multiplier and the demodulator was simulated in ADS to find its input impedance. Fig. 4.10 shows the schematic.

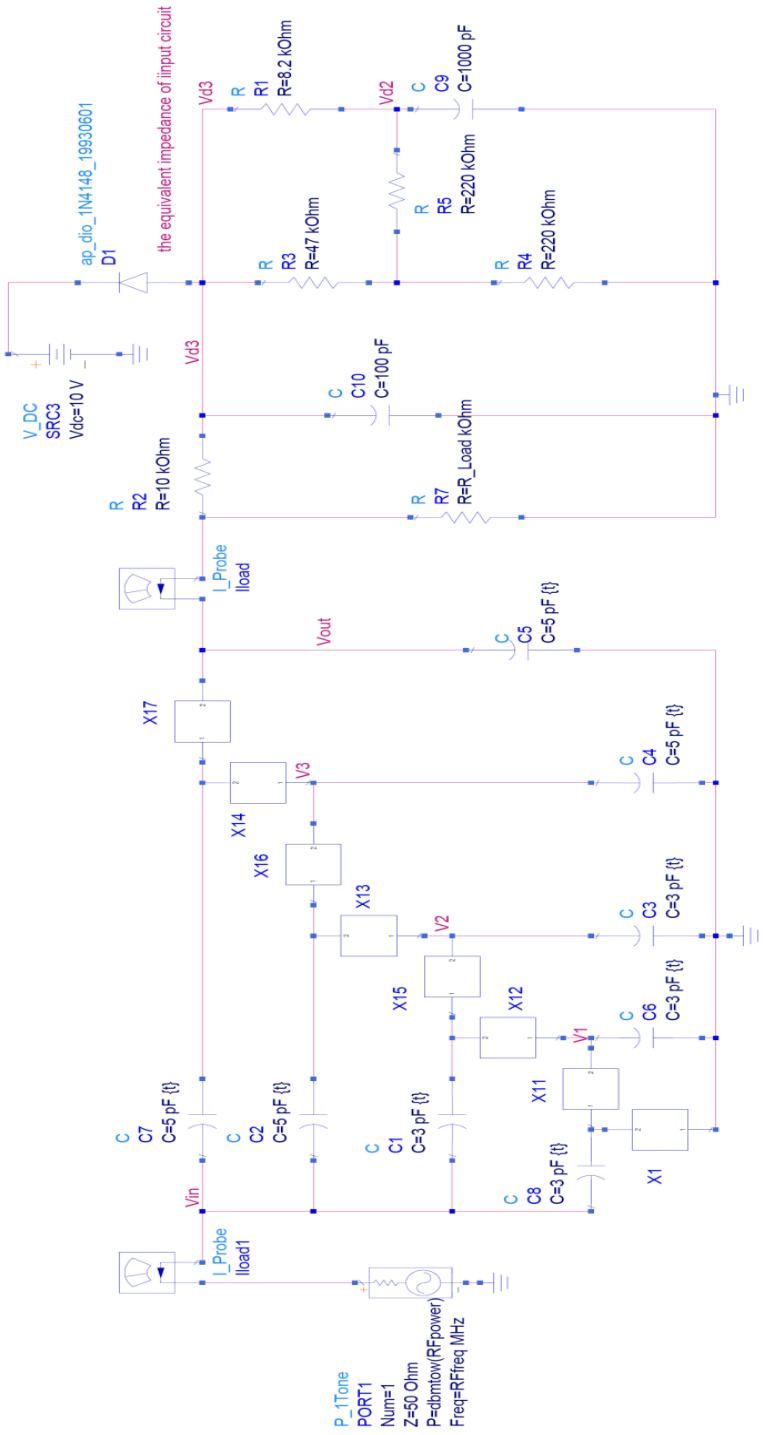
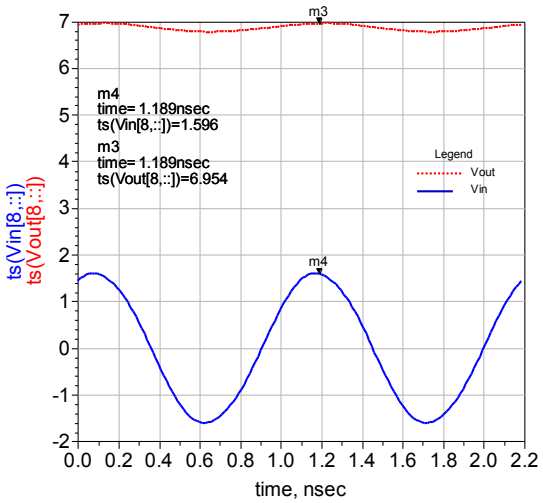


Fig. 4.10: Simulation schematic of voltage multiplier with demodulator

The simulation results show that there is not much change in input impedance and voltage multiplication levels due to the addition of the comparator circuit.



RFpower	max(mag(Vin))	max(mag(Vout))
-30.000	0.016	0.001
-25.000	0.028	0.003
-20.000	0.049	0.010
-15.000	0.088	0.034
-10.000	0.156	0.133
-5.000	0.278	0.485
0.000	0.497	1.385
5.000	0.894	3.259
10.000	1.610	6.863
15.000	2.848	12.221
20.000	4.895	18.954

Fig. 4.11: Output voltage Vout (V) and input voltage Vin (V) waveforms and values.

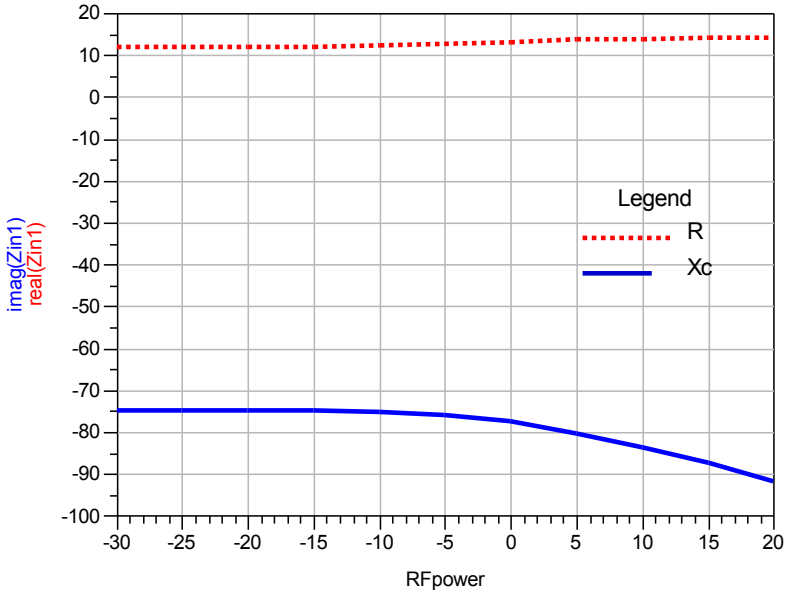


Fig. 4.12: Input impedance (Ω) vs RF power input (dBm)

4.3 Backscatter modulator

Passive and semi-passive RFID tags do not use a radio transmitter for transmitting back the signal; instead they use modulation of the reflected power from the tag antenna. The reflected power is decided by the scatter aperture σ (A_s) of the antenna. In this way a small part of the reader power transmitted is returned by the transponder. Data exchange between the reader and the tag is shown in Fig. 4.13.

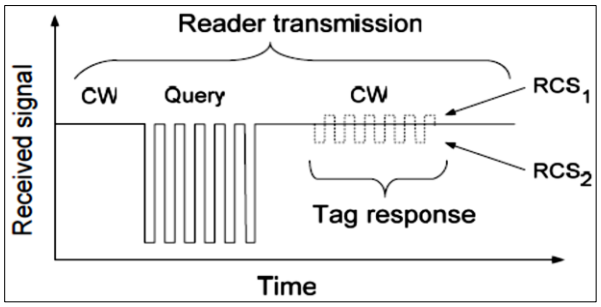


Fig. 4.13: Data exchange between an RFID reader and a tag [25]

The theory can be explained for a backscattered communication to achieve an AKS modulation. The modulator can be visualized as a switch which will turn on and off based on the modulating signal. The effect of turning on and off the impedance across the antenna terminals makes the scatter aperture to vary and thus the power P_s reflected by the tag. This will in turn change the impedance across the antenna terminals, making the effective radar cross section (RCS) of the antenna to switch between RCS_1 and RCS_2. This modulation backscatter operation is shown in Fig. 4.14.

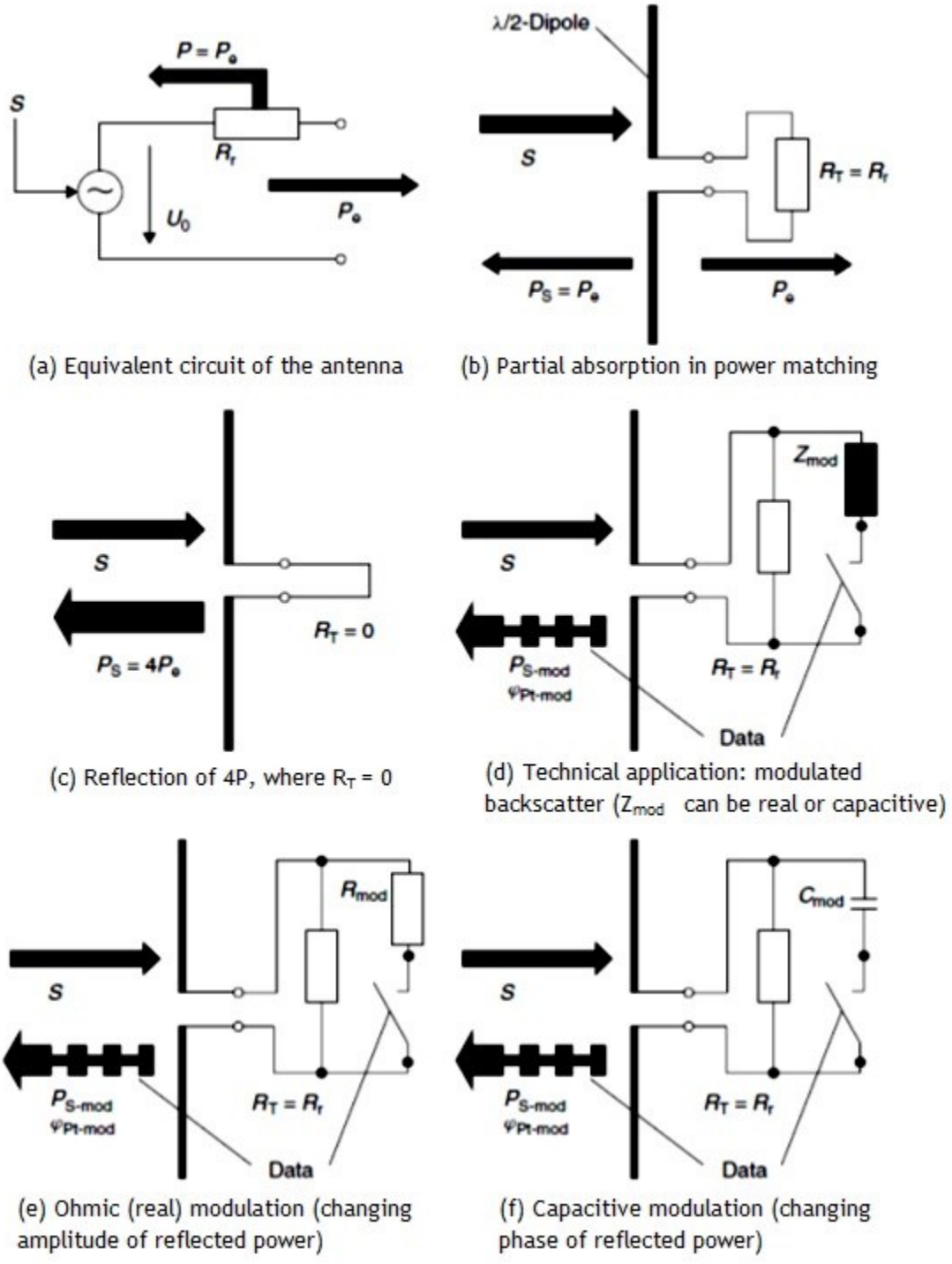


Fig. 4.14: Generation of modulated backscatter [1]

This impedance switching can be achieved in several ways. One simple implementation is shown in Fig. 4.15. In this circuit, a high frequency diode is connected at the terminals of the antenna. Since the diode current-voltage characteristic has an AC resistance that depends on the biasing point, the DC bias can be changed to present different impedance values across the antenna terminals. This can be achieved in similar manner using other nonlinear semiconductor devices – Schottky diodes, Varactor diodes, PIN diodes, and MOSFETs.

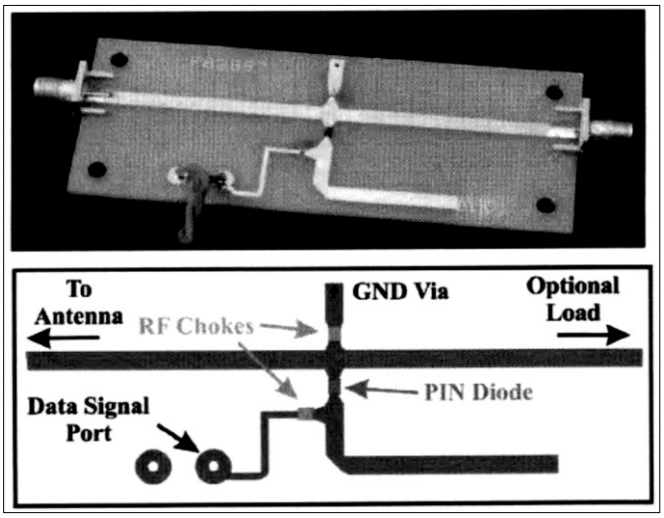


Fig. 4.15: Practical implementation of backscatter modulator using PIN diode [26]

Another practical implementation is with a transistor as antenna load as shown in Fig. 4.16. In this circuit, when the transistor base is held at the appropriate potential to turn the transistor ON, current travels through the channel making it similar to a short circuit. When the transistor is turned off, the channel becomes nonconductive. Since the current induced on the antenna, and thus, the backscattered wave received at the reader, depends on the load presented to the antenna, this scheme creates a modulated backscattered wave at the reader.

The modulator modifies the capacitance of a varactor connected to the antenna according to the digital signal input.

Varying the capacitance will vary the radar cross section (RCS) of the antenna. The reader detects these variations so that the back-scattered information can be recovered on the reader side. The varactor is connected to the antenna terminals through a blocking capacitor. The voltage across the varactor is controlled by the amplifier stage located before the switch transistor, which can slow down the speed of capacitance change such that the back-scattered modulated signal can meet the requirement of FCC emission regulations.

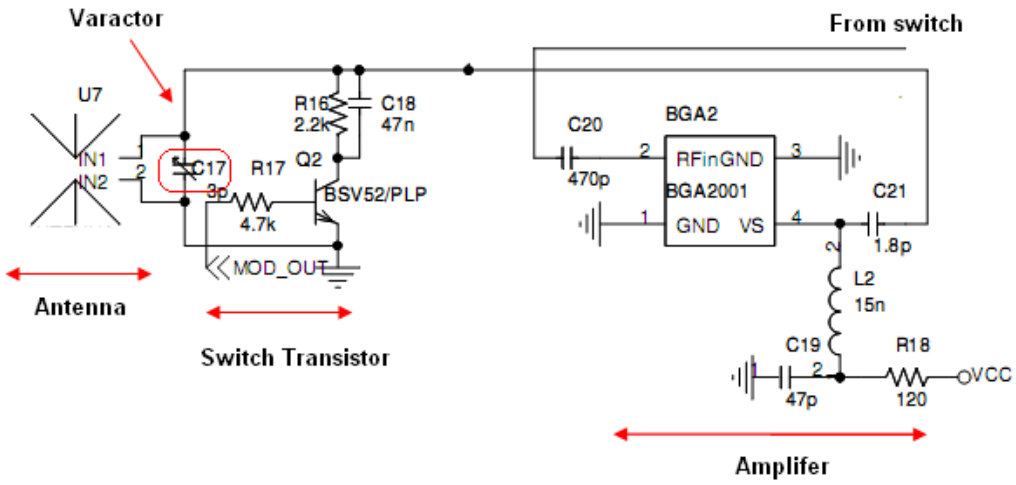


Fig. 4.16: Schematic of the backscatter circuit [27]

4.4 Design – simulation results

The design of the backscatter modulator was achieved using the transistor BSV52 in an SOT-23 package. The transistor is intended to switch the impedance across the antenna by acting as a switch based on the voltage level at the base of the transistor. The simulation basically involves finding the total input impedance into the RF circuit, when the transistor is turned ON and OFF as shown in Fig. 4.17 and Fig. 4.18.

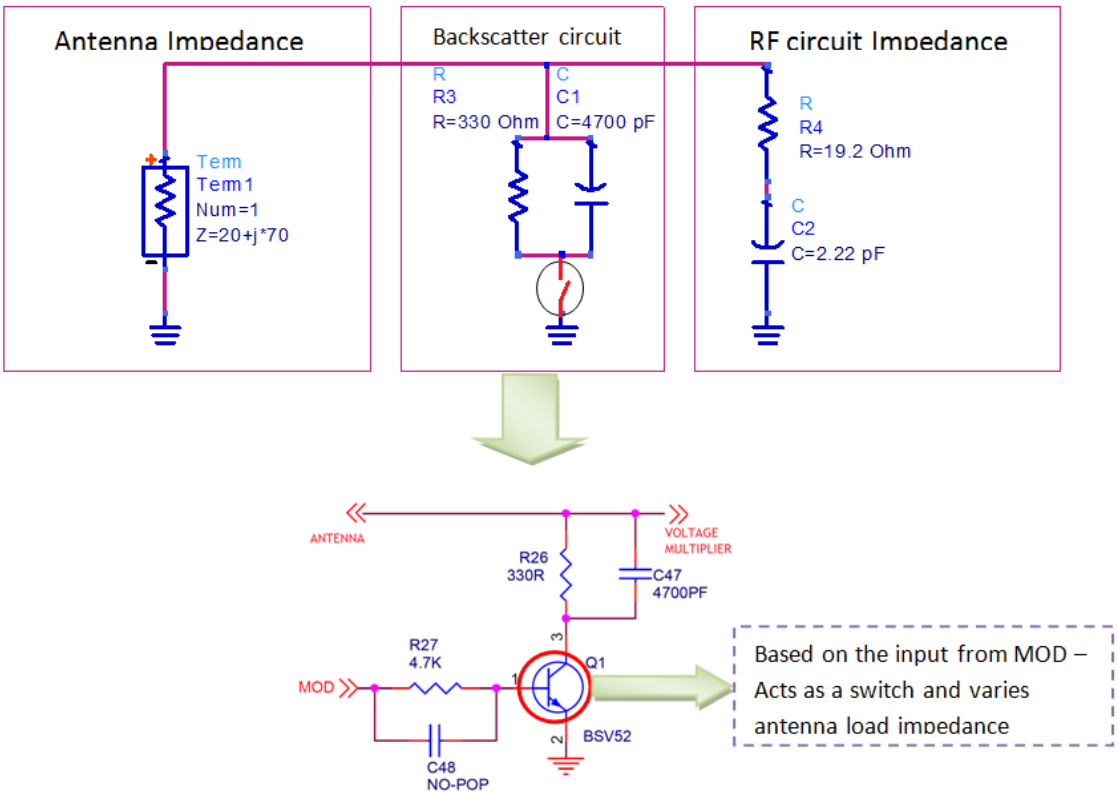


Fig. 4.17: Backscatter load modulator with Transistor Q1

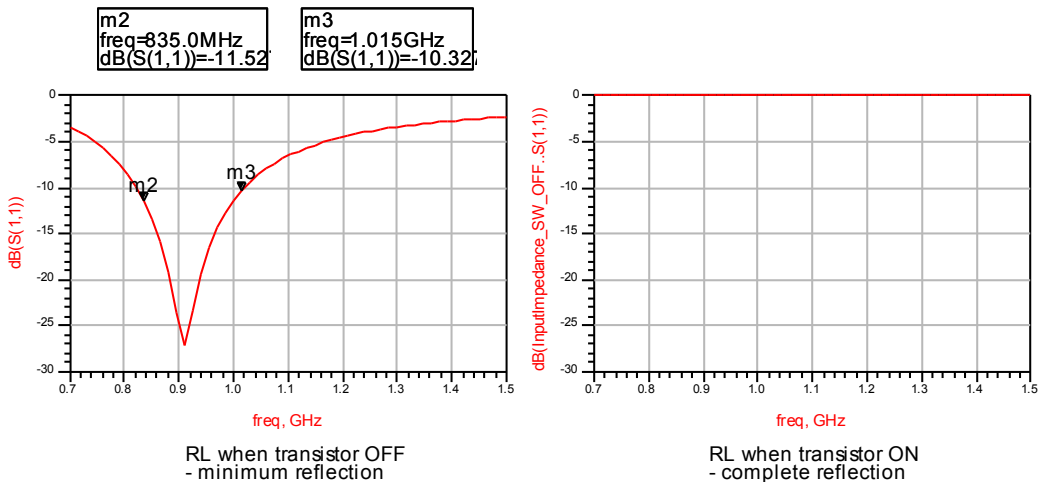


Fig. 4.18: Simulation results showing return loss when Q1 is ON or OFF

Further system level simulation was done with a "scroll command" sequence to illuminate the tag with CW energy. This provides a sync pulse, so the tag can reply using modulated backscatter. The modulation is driven by random data and may be viewed via a test point on the antenna. These are shown in Fig. 4.19 and Fig. 4.20.

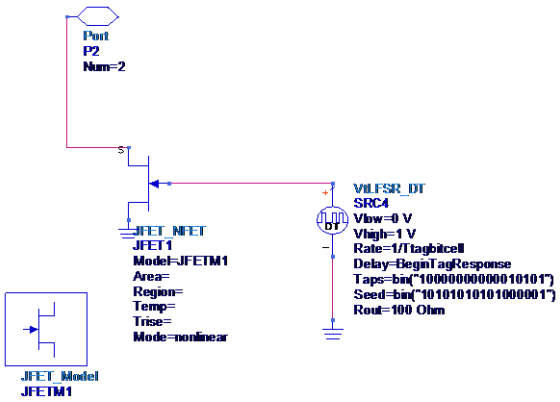


Fig. 4.19: Transistor base fed with the scroll command

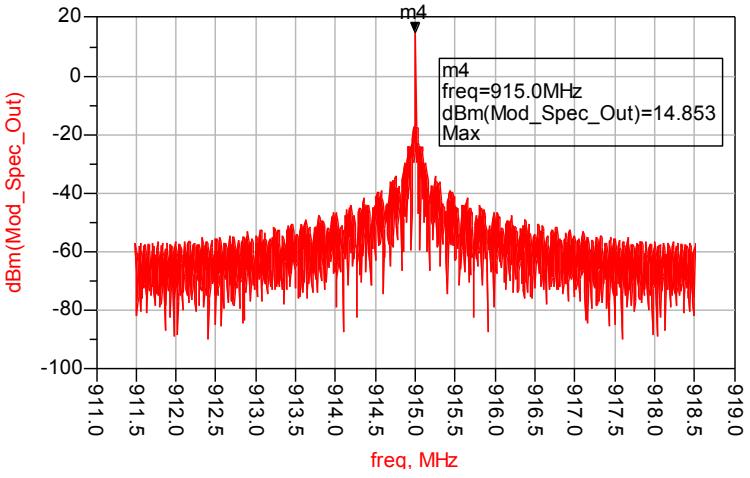


Fig. 4.20: Backscatter modulator - Power spectrum

4.5 Digital section

The control logic unit is used to utilize the communication protocols. The "Demodulator" converts the analog RF signal to a digital form and passes it to the "Shift Register & Logic". The "Shift Register & Logic" process the data by comparing the address from the reader to its own internally stored address. If the address from the RFID reader matches the internal address of the RFID, the "Shift Register & Logic" output its own address through backscattering for the RFID reader to verify; if it does not match with its internal address, the RFID tag does not backscatter.

In this work, we used the ATmega128 digital section [Appendix B], as provided by the collaborative company, which is as shown in Fig. 4.21 [27].

4.6 Conclusion

The four-stage charge pump designed in the previous chapter was used as an envelope detector and acts as the first stage of the demodulator block. Hence simple but efficient ASK demodulator and backscatter modulator circuits were designed for the RF section of the semi-passive RFID tag. The simulation results show that the designs work as expected.

The other critical part in an RFID tag design is the antenna. The challenge will be to come up with a structure which will be less affected by the RFID tag circuitry, the presence of which will deteriorate its properties as an antenna. The next chapter takes all these factors into consideration to design an antenna which is also conjugate matched with the input impedance of the tag circuitry.

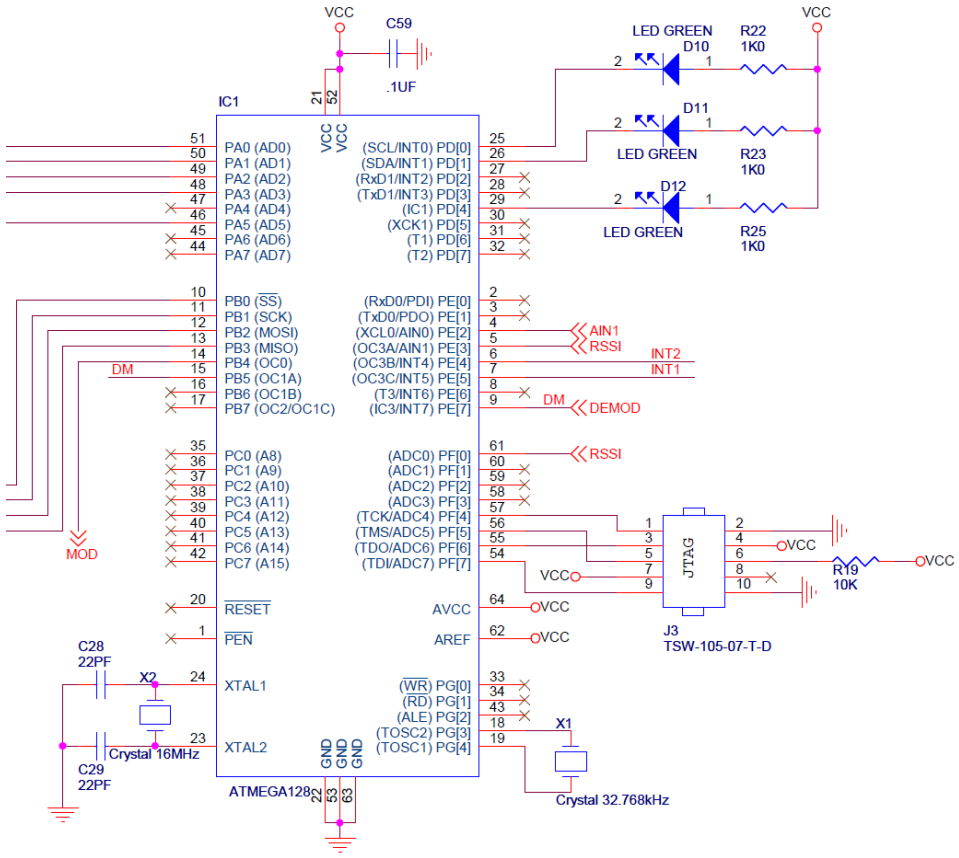


Fig. 4.21: Digital circuit using ATmega128

Chapter 5: Antenna Design and Matching Techniques

5.1 Introduction

The other most important part of an RFID tag is the antenna for radiating or receiving radio waves. Antennas can be of different kinds like wire antennas, aperture antennas, planar antennas, array antennas, reflector antennas, lens antennas, to name a few. Among these, dipole antennas (a type of wire antennas) and micro-strip patch antennas are extensively used in RFID tags. Most of the UHF RFID tags use variants of dipole. Figure 5.1 shows the dipole and patch antenna configurations with their electrical equivalent circuit. The dipole antenna looks as a series RLC circuit while a patch antenna looks like a parallel RLC circuit. Among these antennas, the dipole antenna is the simplest and the most versatile. Planar antennas are low profile, conformable to planar and non-planar circuits, simple and inexpensive to manufacture. The dipole antenna exhibits an omni-directional radiation pattern whereas the patch antenna has a directional radiation pattern (maximum amplitude in only one direction). The patch antenna is very popular for RFID readers and the dipole antenna for RFID tag. By changing the shape of the antenna, its characteristic properties, such as radiation resistance and bandwidth can be changed. Figure 5.2 shows some possible implementations of dipole antennas used in RFID tags.

The first goal in the antenna design is to build an antenna which will be less affected by the presence of RF circuitry. Secondly, to accommodate both the antenna and the RF/digital sections in the space requirement of 3inches x 2.5inches.

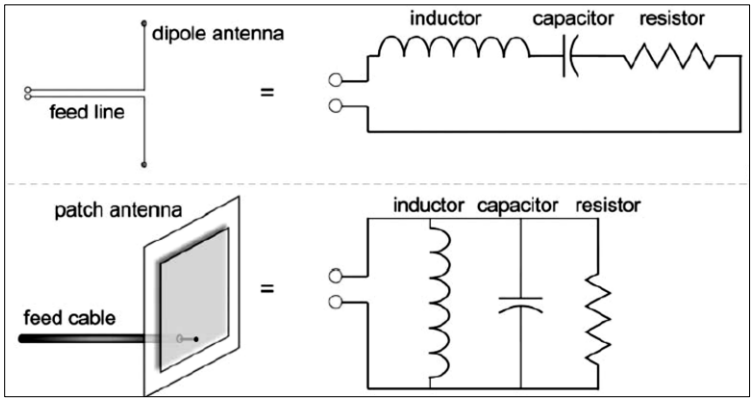


Fig. 5.1: Dipole vs. Patch equivalent electrical circuit [11]

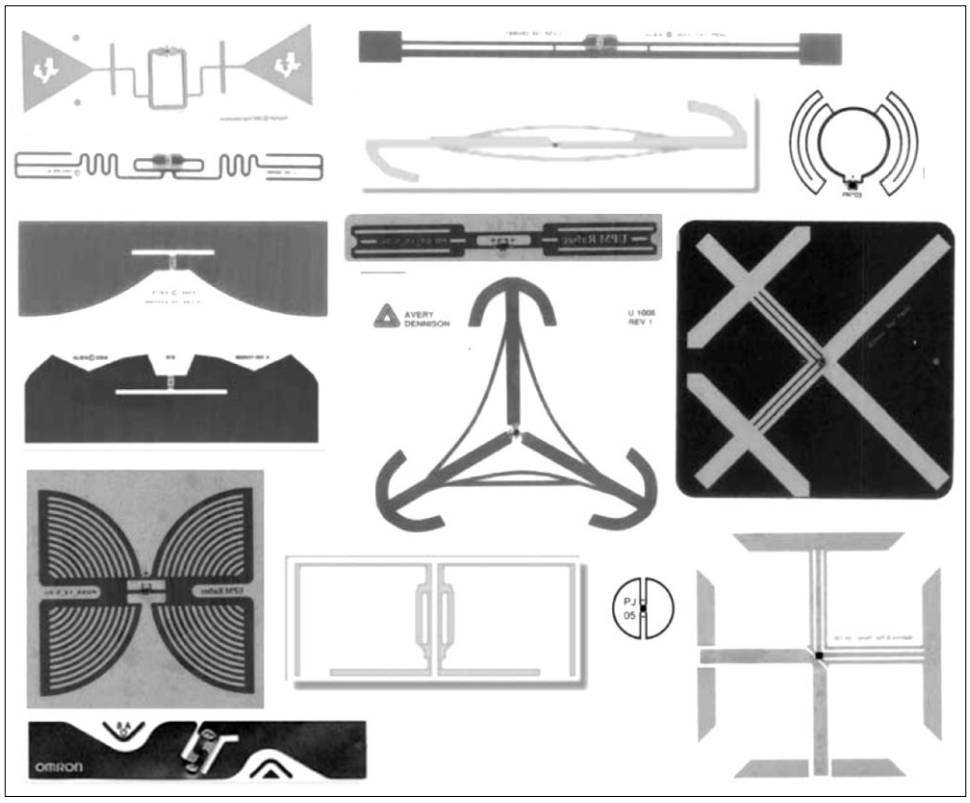


Fig. 5.2: Some dipole configurations used in RFID tags [11]

5.2 Fundamental parameters of an antenna

The performance of an antenna can be described by a number of parameters like,

- *Gain and radiation pattern*: These two quantities give an idea about the extent to which the power radiated from an antenna is concentrated in a specific direction.
- *Effective aperture*: This parameter describes the power capturing characteristic of the antenna, when the wave impinges on it. In the case of an incoming plane wave with power density S, the effective aperture relates S to the maximum received power that can be drawn from an antenna, given alignment and correct polarization.

$$P_e = A_e.S \tag{5.1}$$

- *Polarization*: The polarization describes the time varying direction and relative magnitude of the electric-field vector. In general, the polarization of the receiving antenna will not be same as the polarization of incoming (incident) wave, referred to as polarization mismatch. Because of the polarization loss due to this mismatch, the power extracted by the antenna from the incoming signal will be lower.
- *Impedance*: The impedance presented by an antenna at its terminals or the ratio of voltage to current at a pair of terminals. From the electrical point of view, an antenna can be modeled by an RLC circuit, as shown above. This parameter is closely related with frequency.
- *Bandwidth*: defined as “the range of frequencies within which the performance of the antenna, with respect to some characteristic, conforms to a specified standard” [11]. Several definitions of bandwidths exist: impedance bandwidth, directivity bandwidth, polarization bandwidth, and efficiency bandwidth. Pattern bandwidth

is associated with gain, side lobe level, beam width, polarization, and beam direction.

There are two working modes for the RFID tag. In receiving mode, the RFID antenna is receiving a signal from a reader antenna and it powers the rest of the transponder circuit. The second is transmitting mode. The chip sends data to the backscattering circuit for switching the antenna load to achieve load modulation. The equivalent circuit of the RFID tag at these two modes of operation is shown in Fig. 5.3.

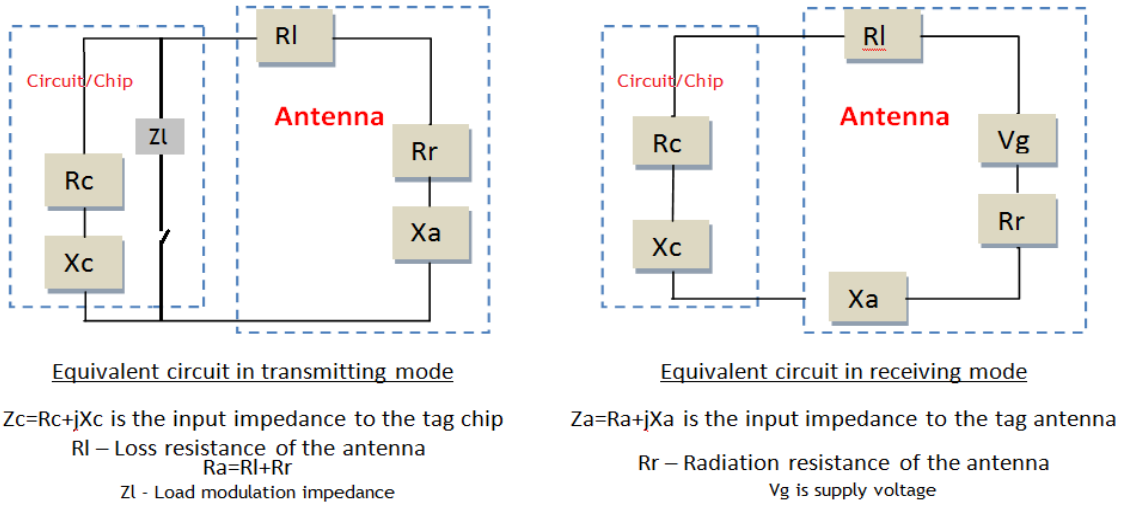


Fig. 5.3: Block diagram of the backscattering RFID tag [18] [13]

In receiving mode, the tag antenna receives the radiated energy from the reader and delivers the signal to the next stage of the tag. This is shown by a voltage source V_g in receiving mode equivalent circuit. In transmit mode, the chip and the associated circuitry will switch the load to reflect the signal. In the case of a passive RFID tag, the received energy will also serve to power the rest of the circuit. The condition for perfect matching between antenna and load is given by (based on the notations shown on Fig. 5.3),

$R_a = R_c$ and $X_a = -X_c$ (complex conjugate)

In this case, the power captured by the antenna is given by

$$P_r = \frac{|Vg|^2}{4}\left[\frac{1}{Rr + Rl}\right] \qquad Watts \tag{5.2}$$

and the power delivered to the rest of the circuit is given by (for $Rc = Ra = Rr + Rl$)

$$P_l = \frac{|Vg|^2}{8}\left[\frac{1}{Rr + Rl}\right] \qquad Watts \tag{5.3}$$

Since perfect matching does not exist, the power delivered to the rest of the circuit is less than that predicted by the ideal Friis transmission equation. For reflection and polarization matched antennas aligned for maximum directional radiation and reception, the Friis transmission equation is given by,

$$P_r = \frac{Pt.G_t.G_r.\lambda^2}{(4\pi r)^2} \qquad Watts \tag{5.4}$$

The power delivered to *Rr* is called scattered or reradiated power. Under conjugate matching, the power delivered to the chip circuit is only half of the total power captured. Tags communicate with reader by varying the amount of power they scatter back to the reader antenna. Radar scattering cross section is used to describe the amount of power backscattered. This is the ratio of power radiated by the tag to the power incident on it

$$A_{sc} = \frac{\lambda^2}{4\pi} G^2 \left|\frac{2Rr}{Zc + Za}\right|^2 \tag{5.5}$$

5.3 Design consideration for RFID antenna

5.3.1 Frequency of operation and impedance matching

The design goal of paramount importance in RFID is the impedance match between the antenna and the chip. In the case of a passive RFID tag, adding an external matching network with lumped elements is usually not preferred to minimize the tag cost and space; instead the antenna can be directly matched to the impedance of the circuitry/chip to which it is connected. Note that the power efficiency of the transponder is strongly influenced by the antenna losses and the package losses.

5.3.2 Available real estate

The other consideration while designing an antenna is its size in order to accommodate the antenna in the space provided. This can be done by bending the wires, so that we can reduce the linear extent taken up by the wire to something lesser. Among others, a bent dipole or a meandered dipole can realize this purpose, but with electrical consequences like increased radiation losses and hence reduced radiation.

5.3.3 Other considerations

In addition, the capacitance and the inductance of the meandered structure are not the same as that of the straight structure. For instance, they can get reduced by shortening the dipole, making the resonant frequency higher. As shown in Fig. 5.4, there are different approaches to tackle this, such as making the antenna wire longer than resonance to shift the resonance to a lower frequency, adding a matching structure to the antenna, or flaring the end of the antenna to a larger structure (capacitive tip loading).

Some of the other aspects that need to be considered while designing an RFID tag are the local environment, interference and collocation, in which case the power from a distant interferer can be much larger than a reflected tag signal. The next section is devoted to explain the techniques to modify the half-wave dipole, to make it shorter and to achieve complex conjugate impedance matching.

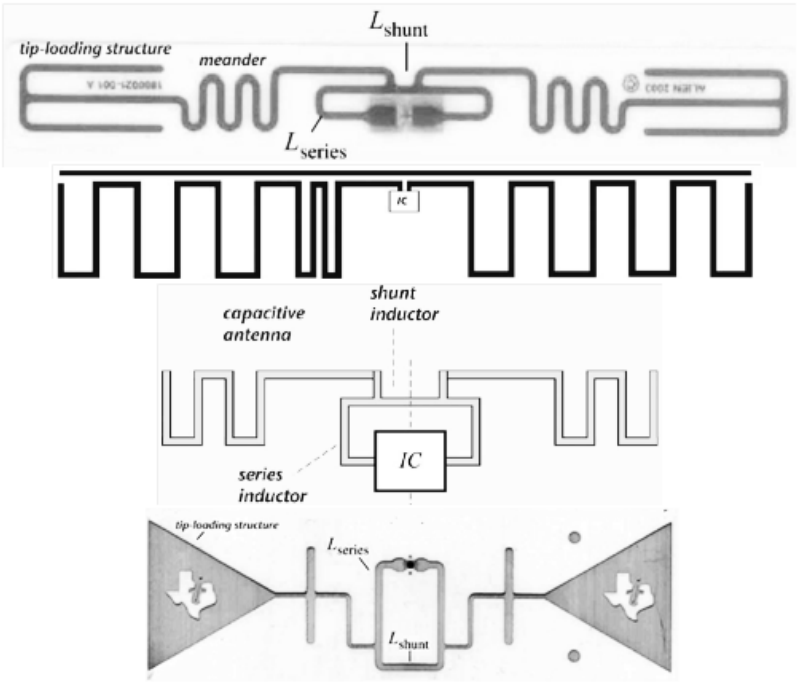


Fig. 5.4: Different realizations of dipole antenna [11]

5.4 Modifying the half wave dipole – size and impedance matching

Most of the far-field UHF RFID tag antennas are modified printed dipoles as in Fig. 5.5. An unmodified half-wave dipole is not a good antenna for typical tag IC since its reactance is too small to be matched to the tag IC and as such the half-wave dipole is physically too large for most UHF RFID tag applications. So some modifications need to be done for a decent performance without losing the simplicity of the dipole.

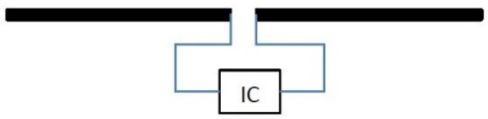


Fig. 5.5: Half-wave dipole

5.4.1 Methods for conjugate impedance matching

With a voltage multiplier circuit consisting of energy-storage components as first stage, the tag input reactance is strongly capacitive and usually varies from -100 Ω to -400Ω, whereas the real part in the order of 10 Ω. Hence, the antenna impedance should be inductive for complex conjugate matching. There are several ways to achieve matching, such as T-match, proximity coupling to small loop and inclusion of shaped slots [12].

5.4.2 T – Match

One of the methods to change the impedance of the dipole is to add a short-circuited stub to the antenna element, as shown in Fig. 5.6. This element of length $a \leq l$, is kept at a distance b from the main radiating element. The current will be distributed between both elements. The impedance at the point where the source is connected is given by [12].

$$Z_{in} = \frac{2Z_t(1+\alpha)^2 Z_A}{2Z_t + (1+\alpha)^2 Z_A} \tag{5.6}$$

with

- Z_t, the impedance of the short-circuit stub formed by the T-match conductors and given by $jZ_o \tan(ka/2)$; with $Z_o \approx 276 \log_{10}(b/\sqrt{(r_e r_e)})$ the characteristic impedance of the two-conductor transmission line with spacing b.
- Z_A , the dipole impedance without the T-match section.
- r_e = 0.25w and r_e' = 8.25 w', the respective equivalent radii of the dipole and the matching stub, and
- $\alpha = \ln(b/r_{e'})/\ln(b/r_e)$, the current division factor between the two conductors.

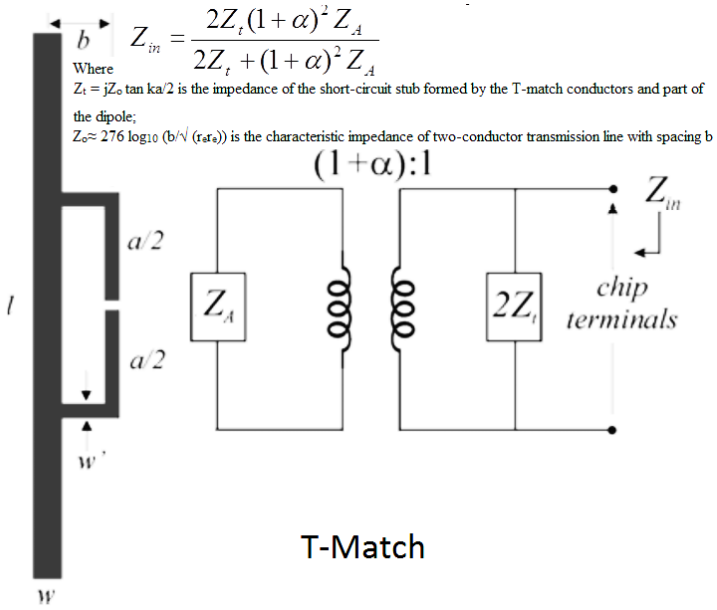


Fig. 5.6: T-match configuration and its equivalent circuit [12]

By adjusting the values of *a*, *b* and *w'*, one can match the antenna impedance to the complex chip impedance, Z_{chip}. Several papers have been published on the use of T-match in impedance matching and it is understood that even with small values of *a* and *b*, high values of input resistance can be obtained. Hence, a single T-match is not enough to match the RF transponder circuit. Further modifications like multiple T-matches can be used. Another implementation of T-match embedded into a main radiator is shown in Fig. 5.7.

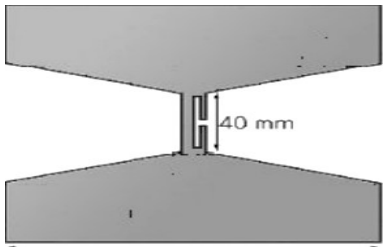


Fig. 5.7: Embedded T-match feed [12]

5.4.3 Inductively coupled loop

The radiating dipole can be fed with an inductive coupling by a small loop kept near by the radiating part. The microchip is directly connected to the loop terminals. This adds an inductance to the antenna. The strength of coupling and the reactance is controlled by the distance between the loop and the radiating body. The inductive coupling can be modeled by a transformer. An inductively coupled loop and its transformer model are shown in Fig. 5.8 [12]. The input impedance of the inductively coupled loop is given by

$$Z_{in} = Z_{loop} + \frac{(2\pi fM)^2}{Z_A} \tag{5.7}$$

where

$$Z_{loop} = j\,2\pi f L_{loop} \tag{5.8}$$

is the loop's input impedance.

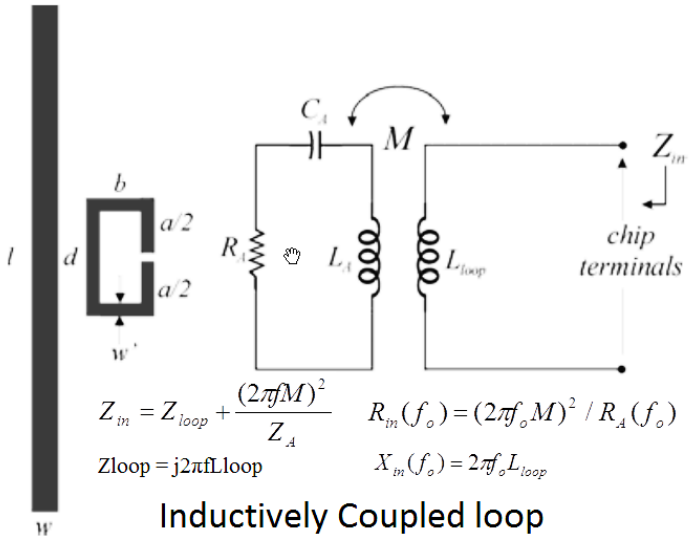


Fig. 5.8: Inductively coupled loop and its equivalent circuit [12]

The total input reactance depends only on the loop inductance, L_{loop}, whereas the resistance is related to the transformer mutual inductance, M, irrespective of whether or not the dipole is at resonance [12].

$$R_{in}(f_o) = (2\pi f_o M)^2 / R_A(f_o) \tag{5.9}$$

$$X_{in}(f_o) = 2\pi f_o L_{loop} \tag{5.10}$$

The mutual coupling and therefore the total input resistance are dependent on both the loop shape and the dipole-loop distance, while the reactance, L_{loop}, is mainly affected only by the loop aspect ratio. The design step involves choosing the loop shape and size for cancelling the chip capacitive reactance and then properly choosing the loop-dipole distance, d, to match the chip's resistance.

5.4.4 Nested Slot

This type of matching strategy employs a nested shaped slot and is useful for tags fabricated with large planar dipoles or suspended patches. This has the capability to provide impedance matching even when the tag is attached onto a high permittivity substrate. This structure can be seen as a slot-line impedance transformer, where each discontinuity provides energy storage and radiation. More degrees of freedom can be further added by increasing the number of teeth with the possibility of miniaturization and achieving multi-band operations. The geometry of the nested slot suspended-patch is shown in Fig. 5.9. The maximum gain is determined by the length of the patch side, l, while changing the slot dimensions, a and b, tunes the impedance. By varying the shape and the size of the internal slot, the antenna can work as a broadband dipole, as a doubly folded dipole or as a H slot. For an RLC behavior with strong resonance, the slot width, b needs to be made much smaller than the side, l. Increasing the size of b moves the resonance towards DC [12].

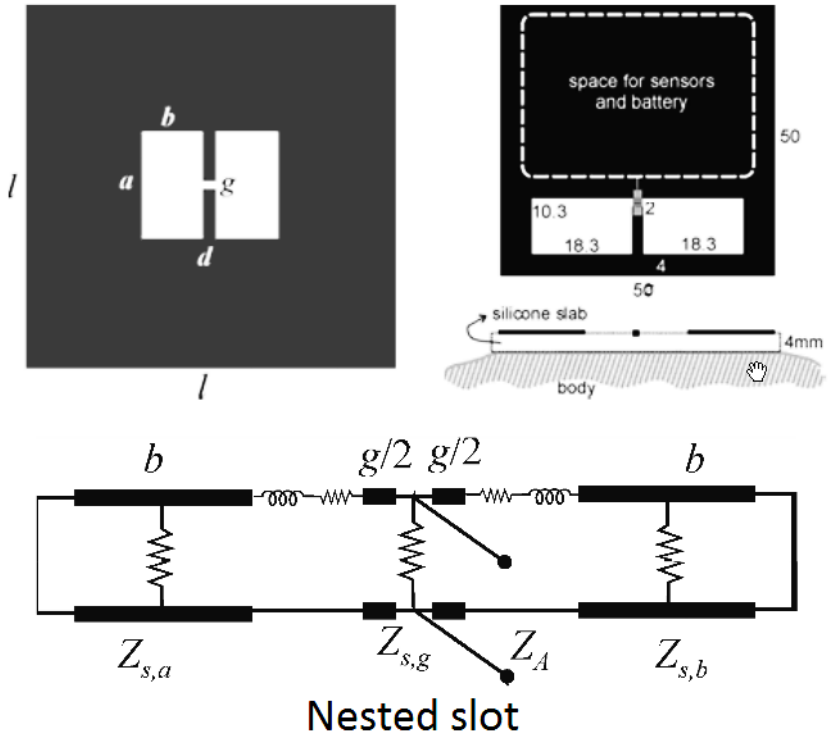


Fig. 5.9: The geometry of the nested-slot suspended-patch [12]

5.5 Antenna design

Antenna design simulations were performed to obtain the desired antenna impedance. The impedance of the RF front-end of the tag was first determined through simulations and measurements. From these, we can have an estimate of the input impedance for different input power levels. Generally, for obtaining maximum range, the value of the circuit impedance at minimum power level is used in the design of the antenna. Figure 5.10 shows plots of impedance and range as function of frequency, highlighting three different resonances namely,

- Tag resonance – the frequency at which the peak range is obtained;
- Antenna self-resonance – the frequency at which the reactance part of the antenna impedance is zero; and
- Antenna resonance with 50 Ω load.

In RFID, the most important factor is achieving the maximum range is determined by the tag resonance. It can be seen that the tag resonance happens when the tag antenna impedance (Z_A) and the chip/RF front end impedance (Z_C) of the RFID tag are complex conjugate matched.

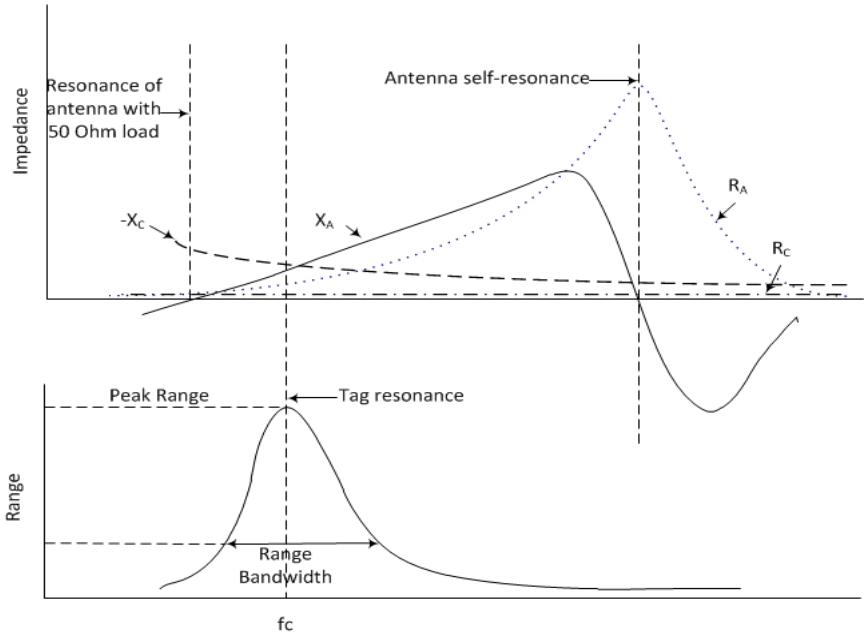


Fig. 5.10: Impedance vs. freq and Range vs. Freq for RFID tag [18]

In [18], Rao *et al*. described the antenna design process for RFID tag antenna (flow-chart shown in Fig. 5.11). The first step is to identify the tag requirements from its application. Once the required antenna parameters are known, the next step involves a parametric study and optimization with one of the EM simulation tool. The tag antenna is then simulated and optimized for the best read range performance, gain and impedance. Then, prototypes are built and performance measured. This process could be repeated to reach the desired performance.

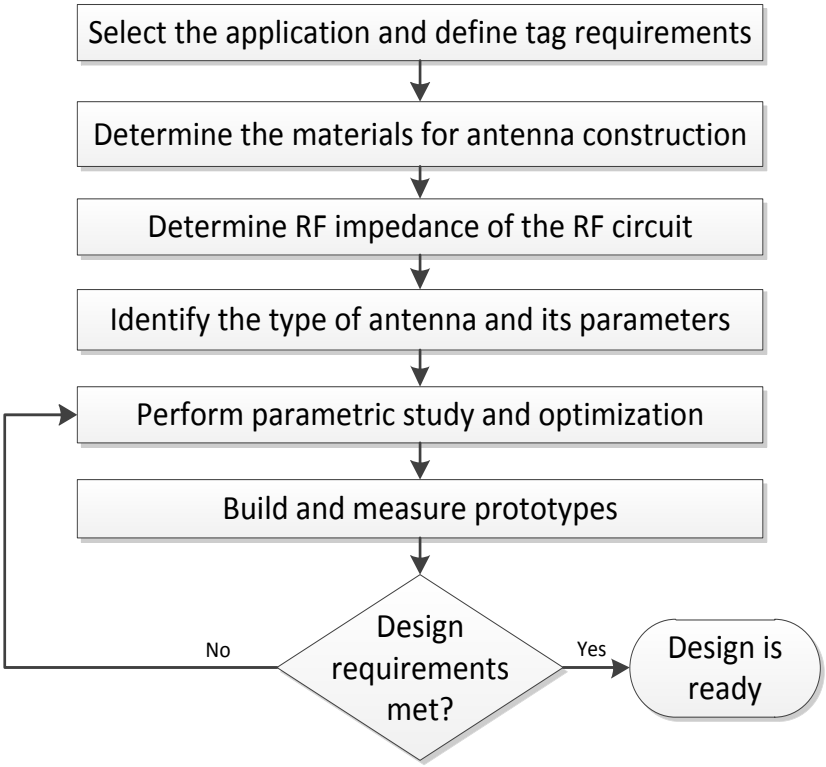


Fig. 5.11: RFID tag antenna design process [18]

5.6 Antenna for the RFID prototype tag#1

This section describes the implementation and results of the final antenna for the semi-passive tag. Various antenna types were considered and simulations were performed to design the best antenna for the RFID tag, which uses discrete components. Because of the need to mount a circuitry for RF and digital sections, the antenna designs and simulations were done with a nearby ground plane. The main effect of having a ground plane near the radiating element, was the change in the antenna input impedance and an increased gain. A modified version of a Planar Inverted F Antenna (PIFA) called Coplanar Inverted F Antenna (CIFA) was chosen for the design because of the following reasons-

- CIFA length is λ/4, with the other half provided by the ground plane.

- Inverted-F antenna is flexible in impedance matching and for the generation of horizontally and vertically polarized electric fields [28].
- The circuitry can be embedded into the ground plane of the inverted F structure, without altering the performance of the antenna severely.
- No additional cost, ease of manufacture, acceptable bandwidth, compact size, omni-directional radiation pattern.

5.6.1 Antenna design

CIFA is derived from the Inverted F antenna (IFA) configuration, which is a variant of monopole antenna. The vertical radiating element of monopole antenna has been folded down to make it parallel with the ground plane. This is done to reduce the height of the antenna, keeping the resonant length the same. Folding of the radiating element of the antenna introduces additional capacitance to the input impedance of the antenna. This is compensated by adding a short-circuited stub to the ground plane. The proposed CIFA structure is shown in Fig. 5.12.

CIFA design parameters can be determined easily. The total length $L+H$ of the inverted-F strip can be determined to be approximately one-quarter wavelength of the center frequency in free space (relative permittivity of the substrate has very minimal effect on the resonant length of the inverted F element). The length of the IFA is $\lambda/4$ and the image of the antenna element due to the ground plane acts as the other $\lambda/4$. Effectively, the length of the antenna is $\lambda/2$. The ground plane plays an important role in the operation of the antenna. When the antenna terminals are excited with current, it also causes excitation of currents in the ground plane. So, at a far-field distance, the electromagnetic field is formed by the interaction of the IFA and its image in the ground plane. Here the ground plane acts as an energy reflector and indeed, is a perfect energy reflector when the ground plane is infinite or very much larger than the dimensions of the monopole. The length L of the folded portion of inverted-F strip and the distance D between the center strip and the shorting strip can be tuned to achieve good impedance matching.

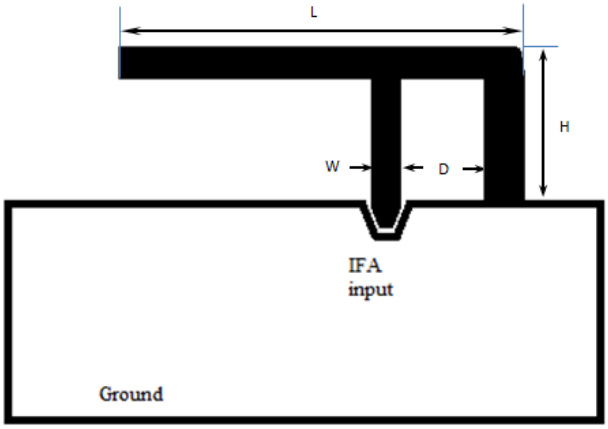


Fig. 5.12: CIFA Structure

At the operating frequency, the required length of the antenna element is 8 cm. This is too long for the desired tag dimensions. So, it is required to reduce the size of the antenna by one of the size reduction techniques discussed earlier. In this case, meandering is used.

The limit on antenna geometry is fixed by the RFID tag dimension requirement. From the tag size specification, it needs to fit within an overall size of 3000mils x 2500mils (7.62cm x 6.35cm). In which, the portion allocated to the circuit is 2000mils x 2500mils (5.08cm x 6.35cm). This means that the space left for the antenna is about 1000mils x 2500mils (2.54cm x 6.35cm). Also, from the wavelength calculation, the dimensions of the inverted-F strip can be determined as,

$L+H = \lambda/4 = 8.2$ cm

A strip width of 1mm was chosen based on the bandwidth and space available. In order to accommodate the antenna in the available space, the antenna structure was modified by meandering the structure.

The possible PCBs to be used for the prototype RFID tag are commercially available FR4 and RT/Duroid 5880 PCBs which specifications are given in Table V-1. These values are used for substrate definition in EM simulation.

Table V-1: Details of the PCB used – FR4 and RT/Duroid 5880

a) FR4	
Dielectric constant	4.5
Thickness	61 mils
tanδ	0.035
Conductor thickness	1.2 mils

b) RT/Duroid 5880	
Dielectric constant	2.2
Thickness	61 mils
tanδ	0.0009
Conductor thickness	1.2 mils

In the design, the ground plane accommodates the tag circuitry. This is of comparable dimensions to the monopole, hence acting as the other half of the monopole as well as good energy reflector. But, because of the presence of other circuit elements in the ground plane, there will be differences in current distribution in both dipole arms. This creates some distortion in radiation pattern. A rough estimate of ground plane dimension for a multi-lobed radiation pattern is that it should be longer than λ/4. Also a smaller ground plane than λ/4 will make the tuning extremely difficult and degrade the overall performance [28]. In the proposed design, the ground plane dimensions are 2000mils x 2500mils (5.08cm x 6.35cm), which is less than the required λ/4 of 8cm. This will further deteriorate the radiation performance of the antenna.

5.6.2 Simulation Results

The simulation started from the initial estimate of the CIFA and final dimensions were obtained from parametric analysis using Ansoft-HFSS. The final antenna configuration is given in Fig. 5.13 and Table V-3. From the original dimensions, the antenna has been modified to fit into the space requirement. The monopole tail has been meandered to reduce the space taken by the antenna. Additionally, a loading bar was introduced to have an optional tuning for the resistance of the antenna input impedance.

The simulation results are shown in Fig. 5.14 to Fig. 5.16, with the radiation pattern summarized in Table V-2.

Table V-2: Pattern cuts used for plotting radiation pattern

For XY plane	Φ=-180^o to 180^o, θ=90^o
XZ plane	Φ=0, θ=-180^o to 180^o
YZ plane	Φ=90, θ=-180^o to 180^o

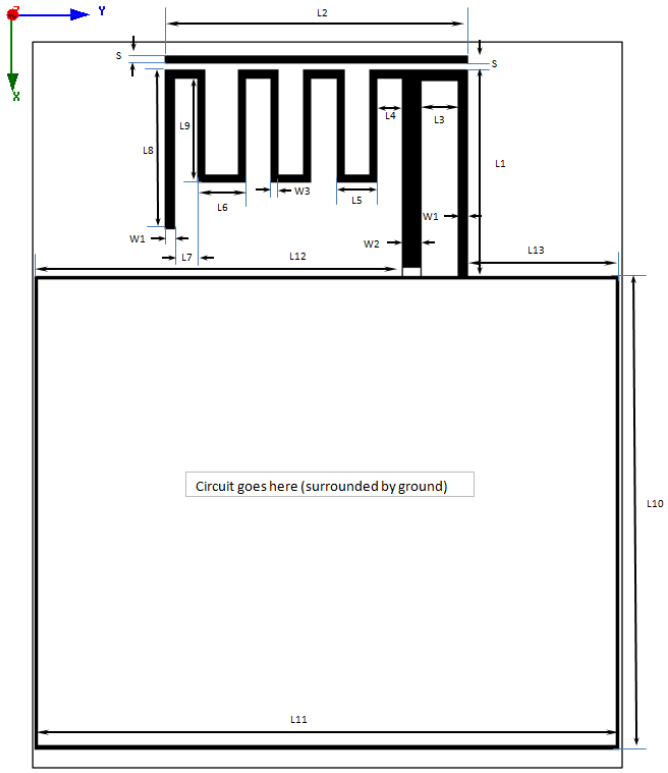


Fig. 5.13: Antenna configuration showing dimensions

Table V-3: Dimensions (in mils)

L1	872	L10	2000
L2	1286	L11	2500
L3	160	L12	1566
L4	106	L13	654
L5	170	W1	40
L6	200	W2	80
L7	100	W3	30
L8	670	S	30
L9	440	All dimensions in mils	

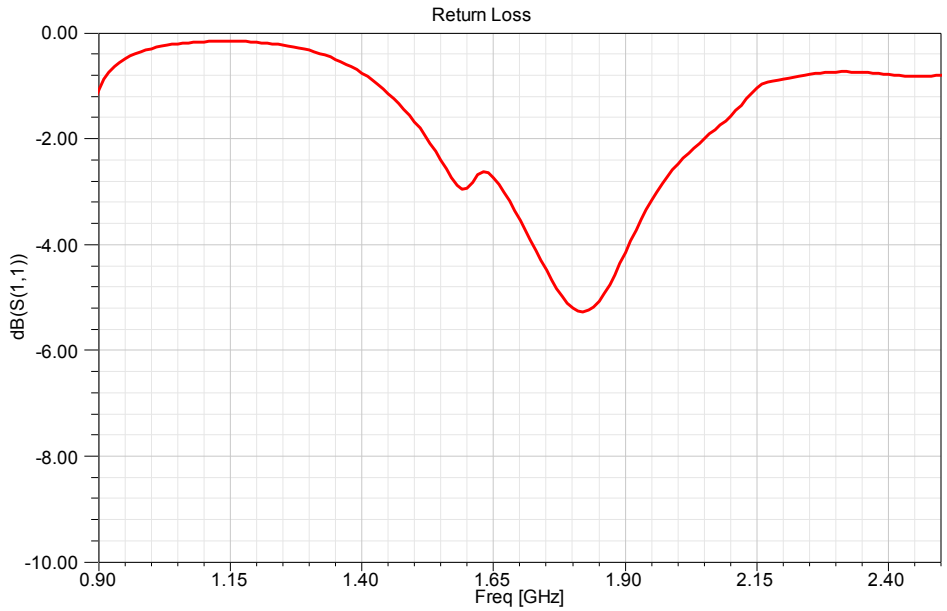


Fig. 5.14: CIFA: Return loss plot of the designed antenna

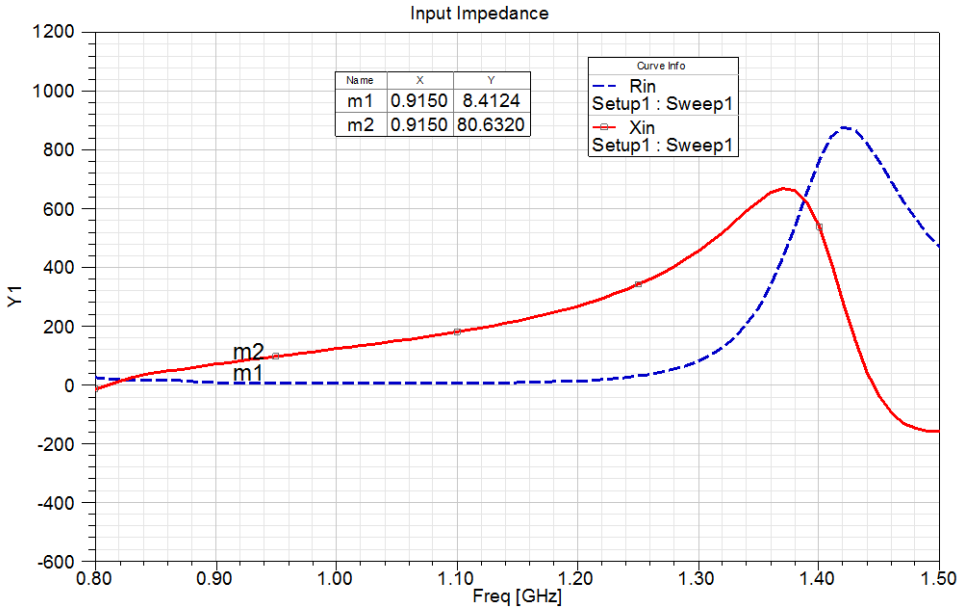


Fig. 5.15: CIFA: Impedance vs. Frequency

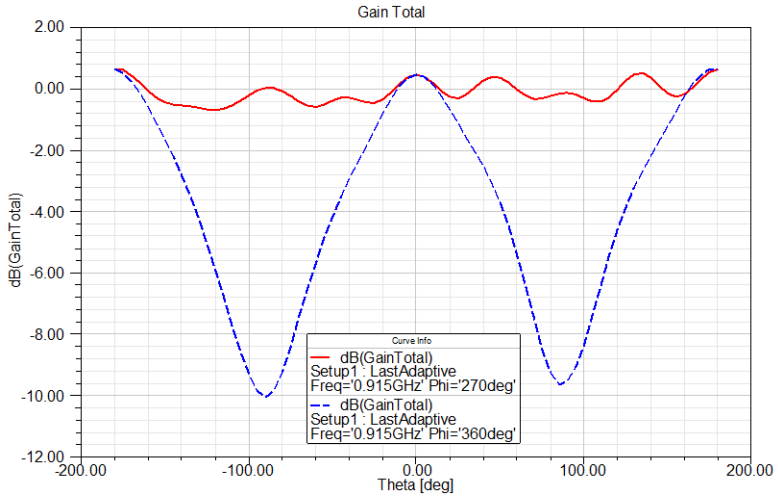
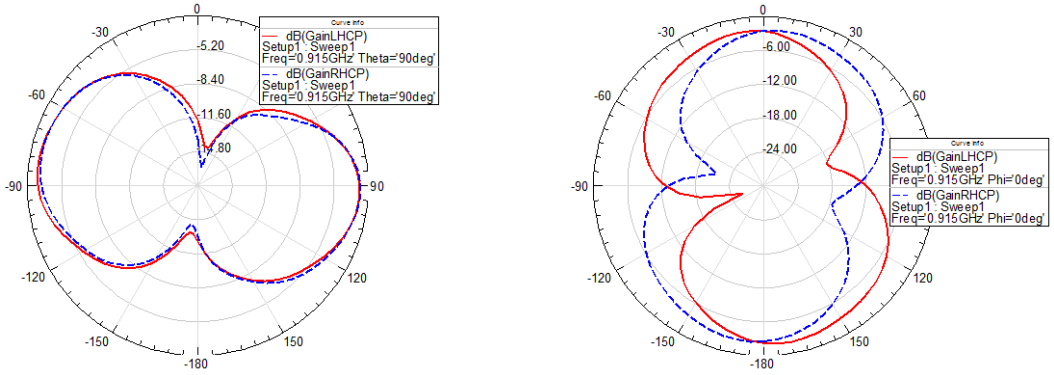
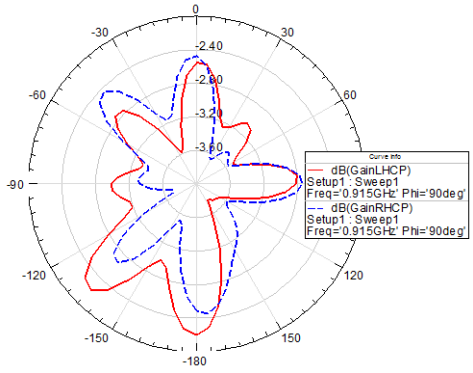


Fig. 5.16: CIFA: 2D Gain



a) Radiation pattern - XY Plane

b) Radiation pattern - XZ Plane



c) Radiation pattern - YZ Plane

Fig. 5.17: CIFA: Radiation pattern plots

5.7 Conclusion

In this chapter, the antenna design procedure for the semi-passive tag was discussed in detail. The same procedure will be used to design the second antenna in this work. The designed antenna is a modified version of PIFA, called coplanar inverted F or CIFA.

Essentially, this type of antenna is best suited for designs which require a circuit nearby. The need of nearby ground can be used to the system designer's advantage, to embed additional analog or digital circuits required for the system. The general reason of building this tag was also for research interest and to have a block-level design insight. On the other hand, there is a need for the design of a commercial RFID tag, which will use an RFID transponder chip available in the market. The next chapter will discuss the design of an RFID tag for commercial/industrial use.

Chapter 6: Design – 2: smart card size RFID tag

An RFID tag with discrete components can only be considered as a prototype tag. Commercializing of this prototype tag, unless being used as a demo-board or a development kit, is not possible because of the following reasons.

1. **Size of the board:** The overall size of the board is huge because of discrete components used in the design. The integrated circuit (IC) technology has matured to an extent that the entire circuitry required for an RFID tag is available in a chip/die form.
2. **Power supply:** the board requires a great deal of power to operate. The prototype tag requires 7V DC supply for its operation. This means that it always needs a power supply/battery pack to be carried with it.
3. **Cost:** the manufacturing cost for 5 pcs. of the RFID tag was around 500$ including the PCB (printed circuit board) and the BOM (bill of materials). However, if a significantly large order is placed then 10-20% discount may be possible. Even then, this will remain too high considering the products available in the market.
4. **Targeted application**: the size of the hardware itself will impose a restriction on the application. Since the tag has a big ground plane enclosing a circuitry there is always a chance that the tag circuitry can be easily affected by the presence of a strong electric or magnetic field. It was even noticed that the use of a DC power supply alters the received signal. So it may even be required to have a shield around the circuit to reduce any interference.

All these factors lead to a tag which must be small, low power consuming and cheap. This is possible only when the tag circuitry is replaced with a small IC. Currently, the IC technology is so mature that all the required blocks, be it RF front end or the digital section, are available in a single IC. Recent advancements in IC technology have made it possible to deliver ICs even for $0.02 each. Considering these facts and because of the presence of RFID tag ICs in the market, the next effort was to build an RFID tag using existing transponder ICs. This chapter explains the design of a prototype RFID tag making use of an RFID ICs available in the market. In this case, the tag design mainly involves the design of an antenna matched to the chip impedance of the IC.

6.1 RFID Transponder chip

There are several high performance RFID transponder chips available in the market. Transponder chips are available in different packages such as Wafer (bumped die on sawn wafer), TSSOP (plastic thin shrink small outline package), XSON3 (plastic extremely thin small outline package), FCS2 and FCS3 (plastic flip chip strap package). For this design, a transponder chip from NXP semiconductor's UCODE product family is used.

The UCODE G2X is a chip for passive tags supporting EPCglobal Class 1 Generation 2 UHF RFID standard. The TSSOP8 chip package is used for the design [30]. This package is a plastic, thin shrink, with 8 leads and a body width of 3mm. The package outline and pin-description are shown in Fig. 6.1 and summarized in Table VI-1.

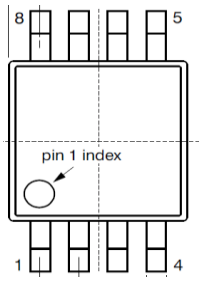


Fig. 6.1: Package outline

Table VI-1 Pin description

Symbol	Pin	Description
RFN	1	Grounded antenna connector
-	2 to 7	Not used
RFP	8	Ungrouded antenna connector

The TSSOP8 package has an impedance of 16-j148Ω and the input parallel capacitance is 1.16pF. Some of the key features of this IC are,

1. 512-bit user memory
2. 240-bit EPC memory
3. 64-bit tag identifier (TID) including 32-bit unique serial number
4. Memory read protection
5. Long read/write ranges due to extremely low power design
6. Advanced anti-collision

The key benefits of this transponder are high sensitivity providing long read range, low Q-factor for consistent performance on different material, large input capacitance for ease of assembly and high assembly yield, reliable and robust RFID technology suitable for dense reader and noisy environments etc. The block diagram of the IC mainly consists of an analog RF interface, digital controller and EEPROM. The analog part absorbs the signal from the antenna and demodulates the data to be processed by the digital part. It also provides stable supply voltage for the IC to operate. Digital section handles the

protocol, communication and other required tasks. The EEPROM contains the EPC and the user data.

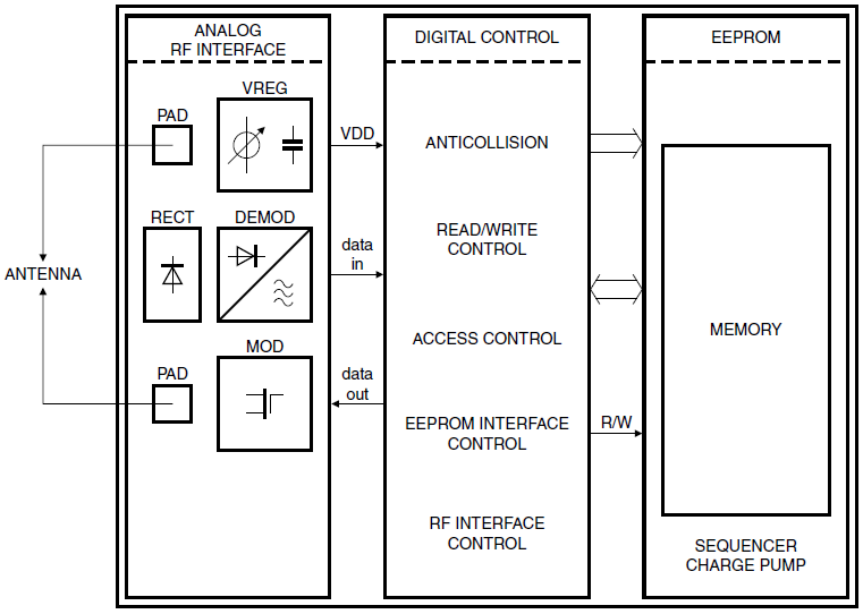


Fig. 6.2: Block diagram of the IC [30]

6.2 Antenna design and Simulation results

The application aimed in developing the passive RFID card (ISO/IEC 7810 ID-1, 85.60X53.98mm) was for its use in personal identification. Within this small size, λ/2 length of about 16cm cannot be accommodated. Hence, it was required to use one of the size reduction techniques discussed earlier. This tag design will be made in an RT/Duroid 5880 PCB (Table VI-2). The proposed antenna is a dipole with capacitive loading at the ends and a T-match section to match with the transponder IC. As given above, the IC has an impedance of 16-j148Ω and the antenna should be conjugate matched to this impedance value. The final antenna configuration is shown in Fig. 6.3 and dimensions summarized in Table VI-3. Simulation results are shown in Fig. 6.4 to Fig. 6.7.

Table VI-2: Details of the PCB used RT/Duroid 5880

Substrate details – RT/Duroid 5880	
Dielectric constant	2.2
Thickness	31 mils
tanδ	0.0009
Conductor thickness	1.2 mils

Table VI-3: Smart card tag: Dimensions (in cm)

L1	3.94	L7	5.5
L2	2.7	S1	0.32
L3	1.8	S2	0.1
L4	2.26	W1	0.32
L5	5.1	W2	0.2
L6	8.5	R	0.3

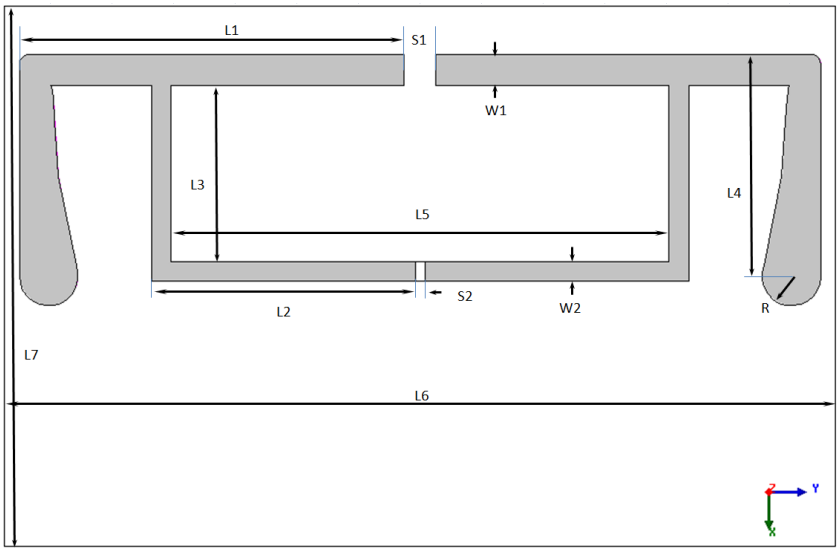


Fig. 6.3: Smart card tag: Antenna configuration showing dimensions

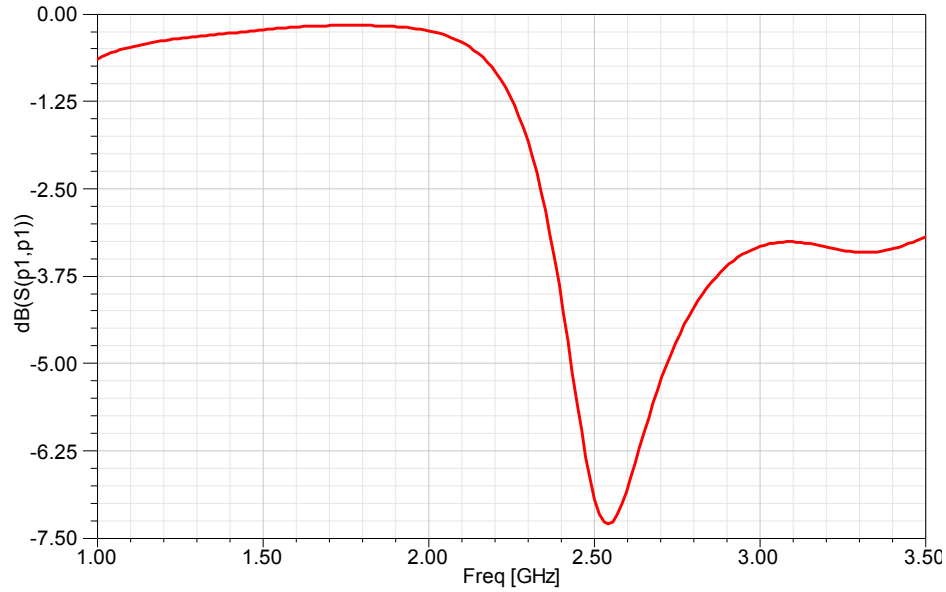


Fig. 6.4: Return loss plot of the designed antenna

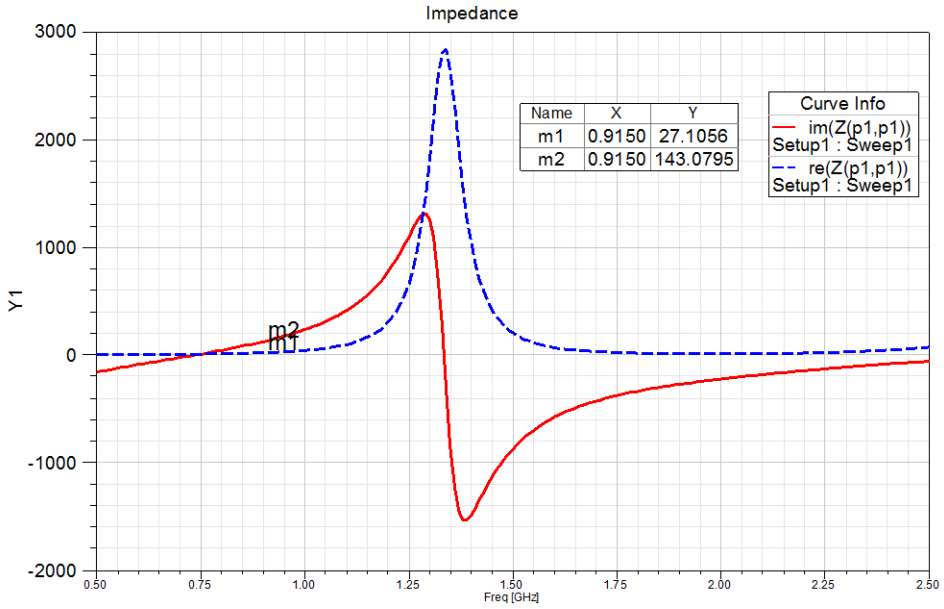


Fig. 6.5: Impedance vs. Frequency

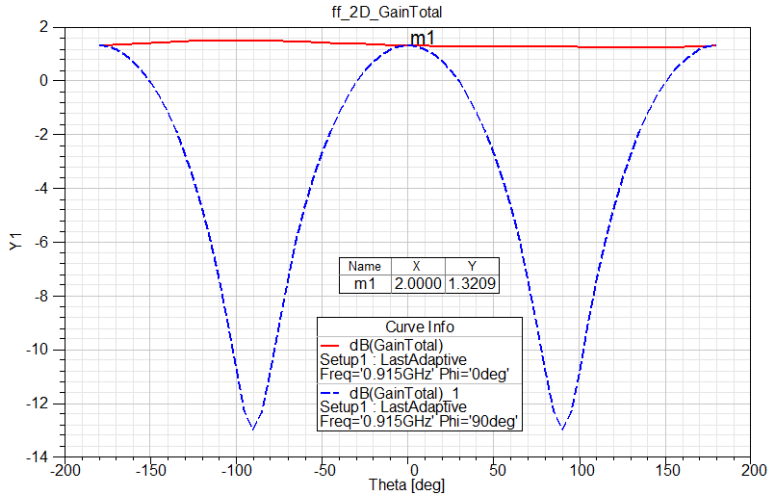
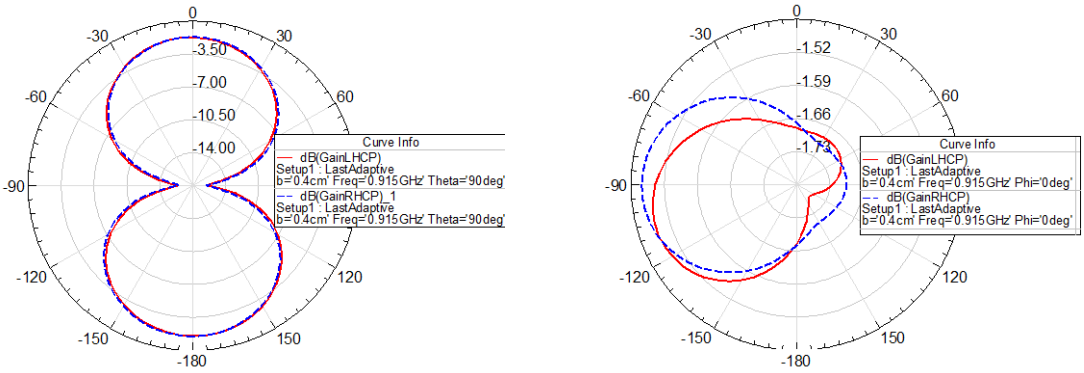
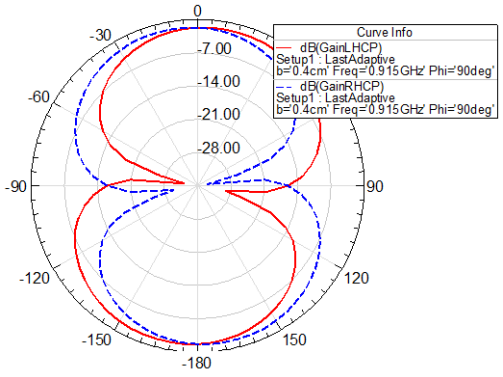


Fig. 6.6: Total gain_2D



a) Radiation pattern - XY Plane

b) Radiation pattern - XZ Plane



c) Radiation pattern - YZ Plane

Fig. 6.7: Modified dipole design - Radiation pattern plots

6.3 Conclusion

This chapter discusses the design of a marketable passive RFID tag. First, the choice of the chip has been done based on the industry requirements. The other deciding factors are the RFID tag specifications, such as size, range, environment, etc. Considering all these, an antenna was designed. The designed antenna is a modified dipole with a T-match and tip loading which is within the size of a bank ATM card.

With the different blocks of the RF front-end designed, the next stage was to manufacture these tags and test them. This involved testing the blocks for its desired functionality by measuring the parameters and comparing with the simulations. This also involved making necessary changes, if any of the specification was not met. Once this was done, all the blocks were be combined together to perform the whole system testing. These aspects of the thesis will be explained in the next chapter.

Chapter 7: Circuit Fabrication and Test results

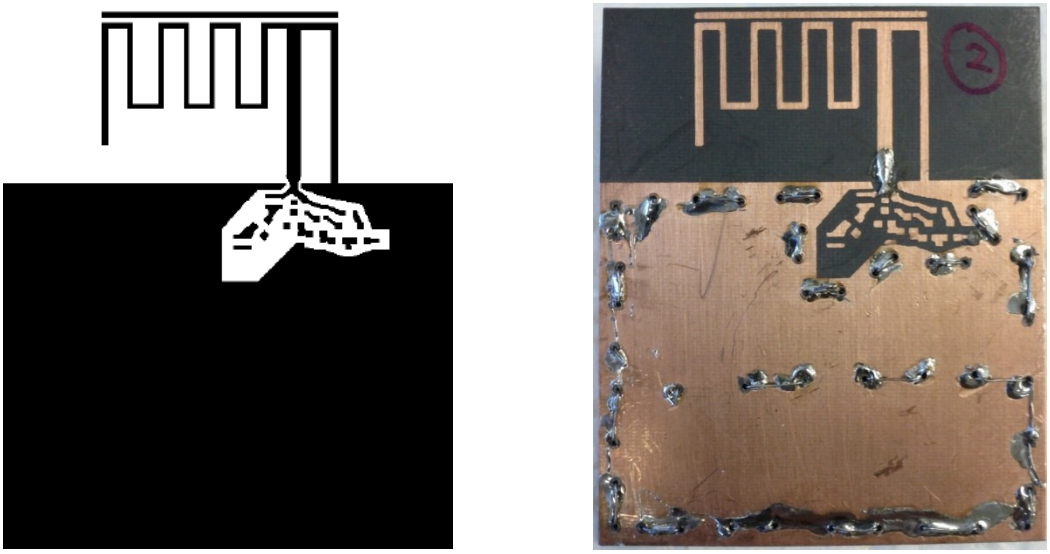
7.1 Introduction

This chapter discusses the test and measurement of each of the designed building blocks. In the case of backscatter modulator, the testing was not performed separately but with all blocks combined together. Finally, the full RFID tag circuit was constructed and the range measured.

7.2 Antenna

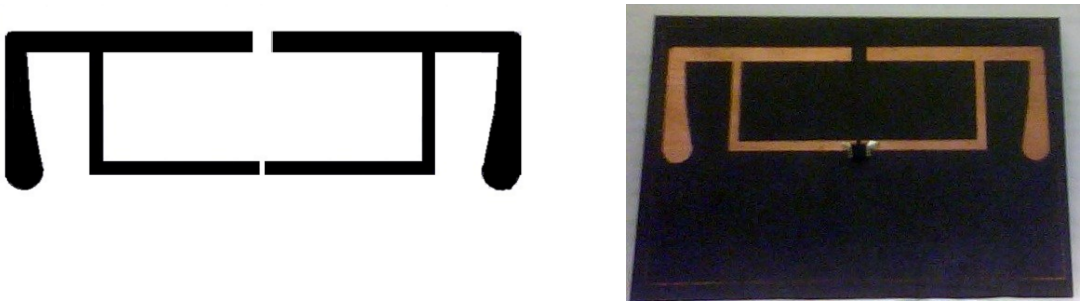
7.2.1 Prototype

The final designs were fabricated and measured. Final prototype tag dimensions were found after two prototype iterations, since the measured results were slightly different from simulations. The final semi-passive tag PCB was fabricated in 61 mils RT/Duroid 5880 board and the passive tag PCB in 31 mils RT/Duroid 5880. Layout mask and fabricated prototype board of the semi-passive tag is shown in Fig. 7.1. Passive tag layout mask and prototype PCB is shown in Fig. 7.2.



a) layout mask **b) Fabricated PCB**

Fig. 7.1: Semi-passive tag PCB showing the antenna with the loading bar and the foot print for charge pump circuit



a) layout mask **b) Fabricated PCB**

Fig. 7.2: Passive tag PCB

7.2.2 Testing

Antenna testing involves measuring the antenna radiation pattern, gain, impedance etc. In the case of passive RFID tags, the most important factor which decides the range is the power transfer from the antenna to the circuitry, which is achieved through complex conjugate matching between the antenna impedance and the circuit impedance. So, the most important measurement in RFID tags is impedance measurement.

1 Impedance measurement:

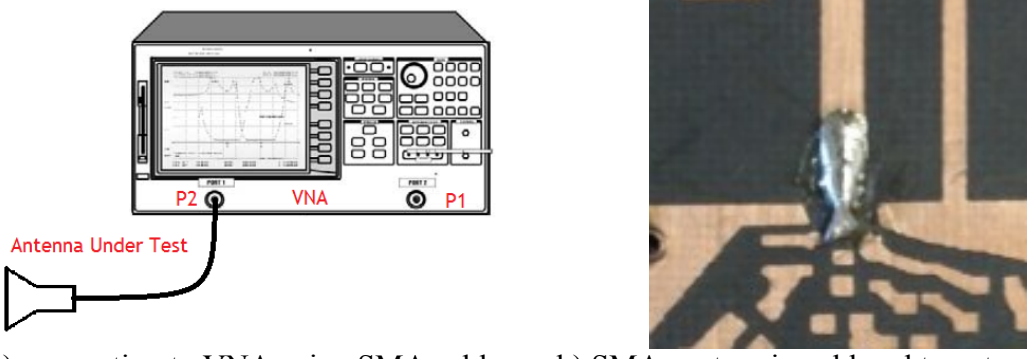
The impedance of the antenna over a wide range of frequencies is measured using a vector network analyzer (VNA) and the setup varies based on the type of antenna, whether balanced or unbalanced. In the case of a CIFA antenna, which is an unbalanced antenna, impedance can be measured directly using the test setup shown in Fig. 7.3. Unlike the CIFA, which is a variant of monopole, the dipole antenna feed is balanced. So, unbalanced coaxial lines cannot be used directly to measure the antenna impedance. There are several papers published on different techniques for measuring the input impedance of a dipole antenna [30] [31] [32].

A well known technique for measuring the impedance of a balanced antenna is to measure the impedance of half of the antenna. In this technique, the impedance of half of the antenna is measured instead of the full antenna, with E-symmetry plane replaced by a metal plate of considerable size. The test setup is shown in Fig. 7.4 and the metal plate is made of stainless steel (46.5 inch x 27.5 inch). The cable from the VNA connects to the SMA connector below the metal plate. The pin of the SMA connector passes through the circular hole in the plate thereby forming a small 50-Ohm section of coaxial line. The antenna feeding point is soldered to the center pin of the SMA connector. In this case, the total antenna impedance is twice the half antenna impedance. It is to be noted that the VNA is calibrated without the SMA connector of the test fixture and hence the reference plane is below the metal plate surface. It is expected to have additional reactance and shift of reference plane, as in the HFSS antenna simulation. This can be corrected by de-embedding the parasitic reactance of the SMA connector [31].

The measurements have been performed with the Anritsu 37347A VNA (40MHz-20GHz). The impedance measurement results of the CIFA antenna are plotted in Fig. 7.5. Figure 7.6 shows the impedance of the dipole antenna. It can be seen that there is a slight difference in the measured impedance values from the simulated ones; this is due to the effect of the SMA connector, which was not taken into account during calibration.

2 Radiation pattern measurement:

There are several methods to measure the radiation patterns of antennas and the commonly used one is the far-field test range. Furthermore, the methods generally used for gain calculation are the gain transfer method and the absolute gain method. Since dipole antennas are omni-directional, this poses problem while measuring the radiation pattern. This is due to the fact that while testing, the radiation pattern will be modified by the structures on which the antenna is mounted. Since it is difficult to measure the radiation pattern of the omni-directional antenna and also due to the unavailability of the resources for accurate measurements, it was decided not to do the radiation pattern measurement. Estimate of the radiation pattern and the gain was based on simulation results.

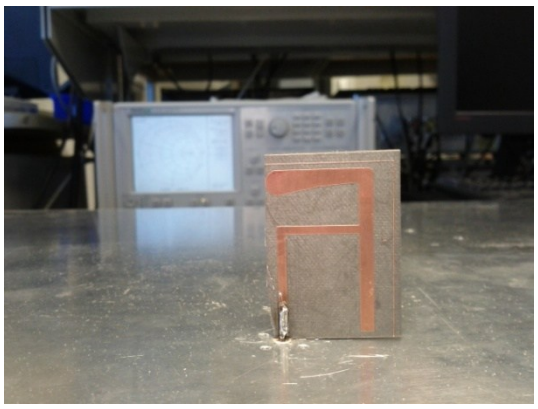


a) connection to VNA using SMA cable b) SMA center pin soldered to antenna feed

Fig. 7.3: Setup 1 – for unbalanced antenna

a) antenna soldered to center pin of SMA connector and is mounted on a metal plate

b) VNA connection to SMA connector



c) half antenna soldered to cc-pin of SMA

Fig. 7.4: Setup 2 – for balanced antenna

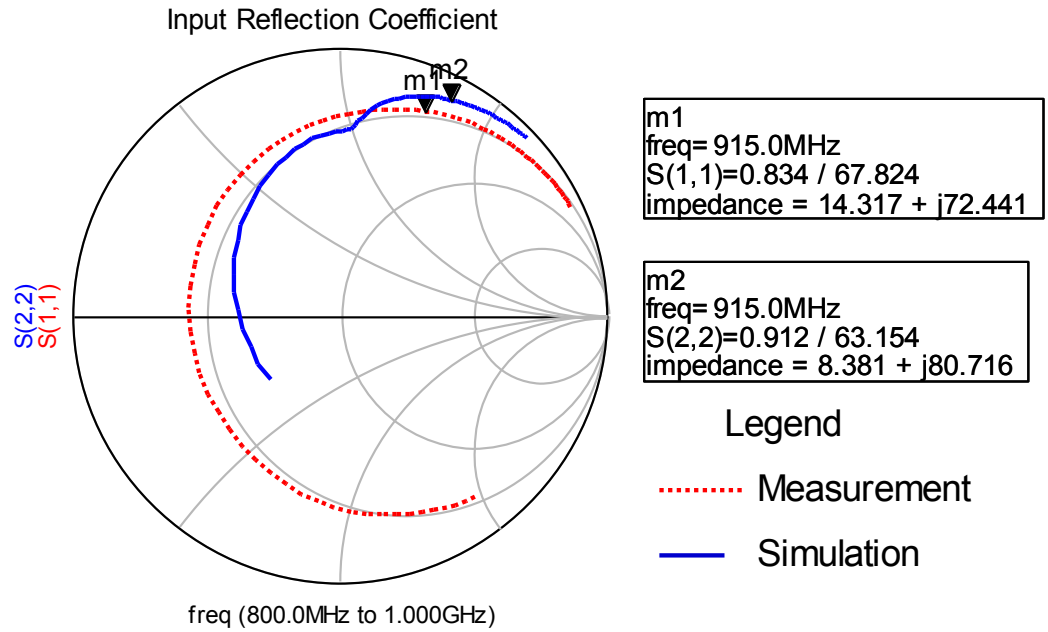


Fig. 7.5: Comparison simulated and measured Impedance - CIFA

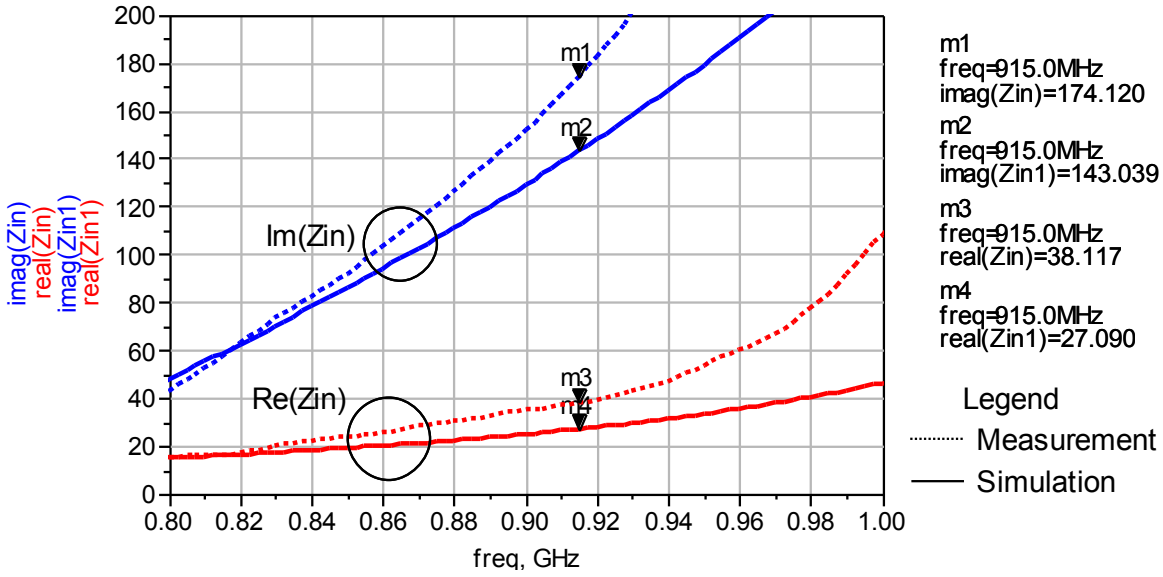
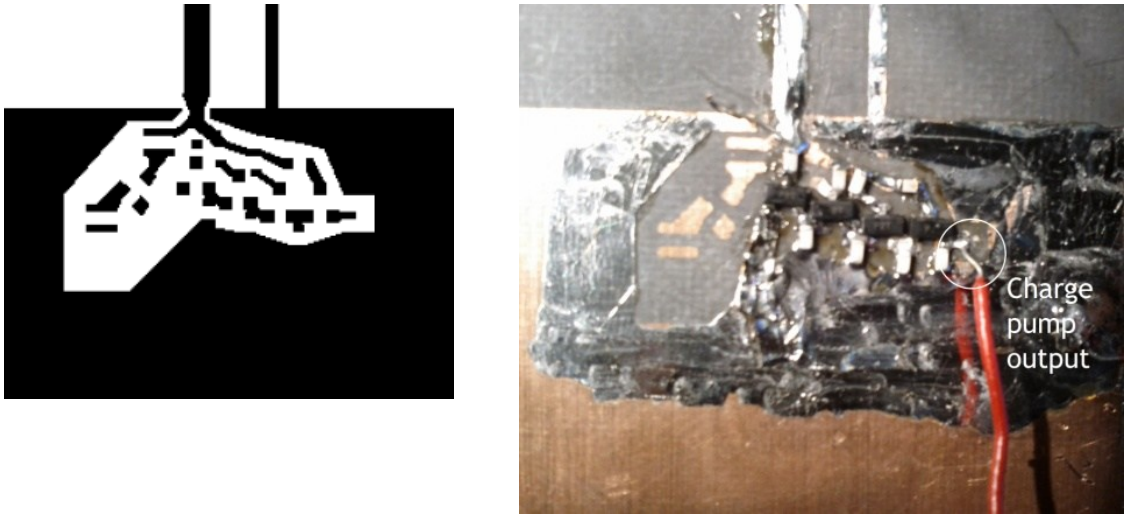


Fig. 7.6: Comparison simulated and measured Impedance - Dipole

7.3 Charge pump and demodulator circuit

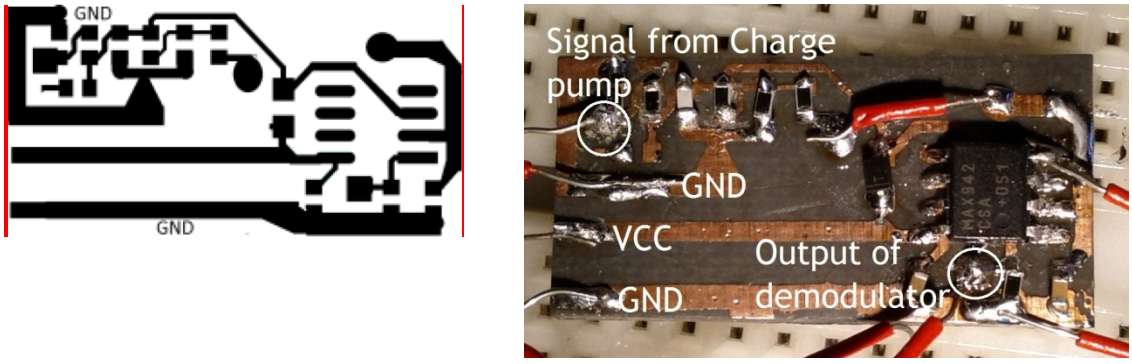
7.3.1 Assembly

The layout design is crucial from an RF perspective since this stage receives the RF signal and thus the layout should ensure that it adds minimum PCB parasitic to the circuit. All the lumped elements used in the circuit were of size (0.6 x 0.3mm) and the diodes are HSMS-2852 ZBD diodes from Avago technologies. The prototype of the antenna with the rectifier circuit was assembled (the layout mask and the assembled unit is shown in Fig. 7.7). Similarly the demodulator circuit was also fabricated (the layout mask and the PCB are shown in Fig. 7.8).



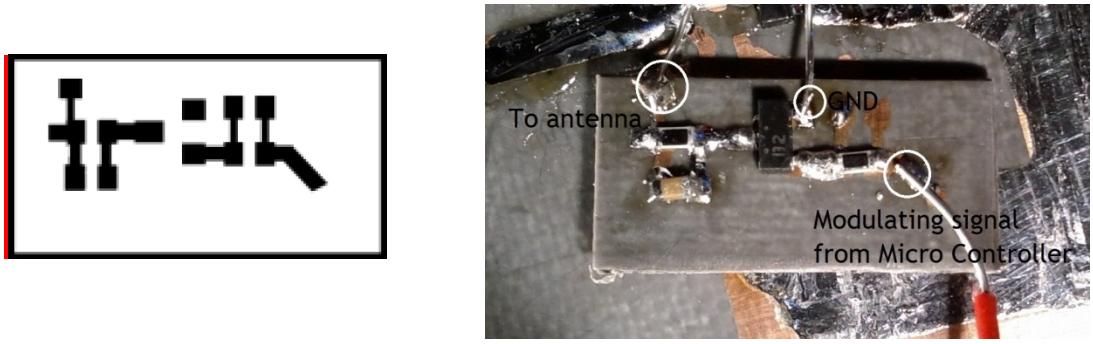
a) layout mask **b) assembled PCB**

Fig. 7.7: Charge pump – Layout mask and assembled unit



a) layout mask **b) assembled PCB**

Fig. 7.8: Demodulator – Layout mask and assembled unit



a) layout mask **b) assembled PCB**

Fig. 7.9: Backscatter modulator – Layout mask and assembled unit

7.3.2 Testing

These blocks were tested using an RFID reader. The RFID reader is made to send the signals and the rectifier and demodulator outputs are displayed in an oscilloscope as shown in Fig. 7.10. The resulting waveforms as seen in the oscilloscope are shown in Fig. 7.11 and Fig. 7.12, respectively. It can be seen that the RF front end and the demodulator circuit function very well as desired.

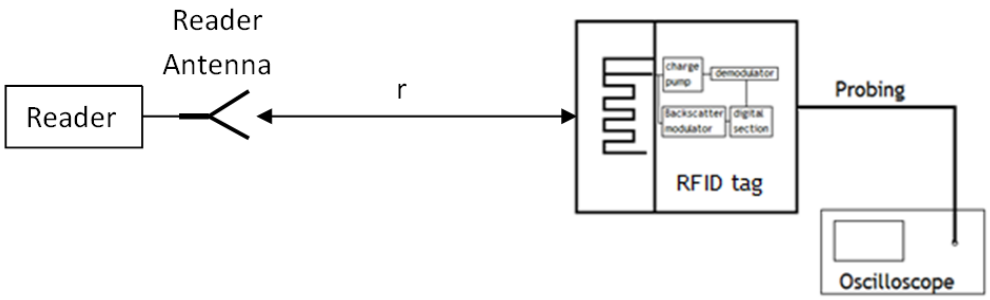


Fig. 7.10: Test setup – Oscilloscope probing

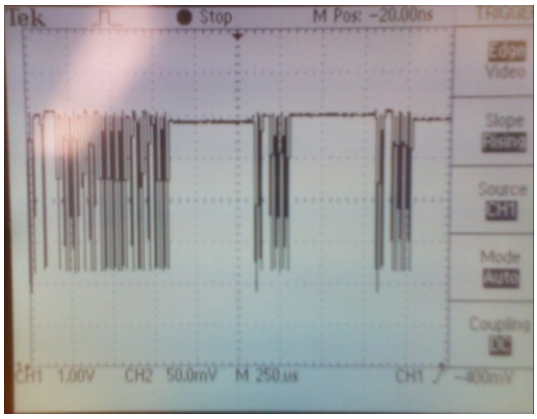


Fig. 7.11: Rectifier output as seen in oscilloscope

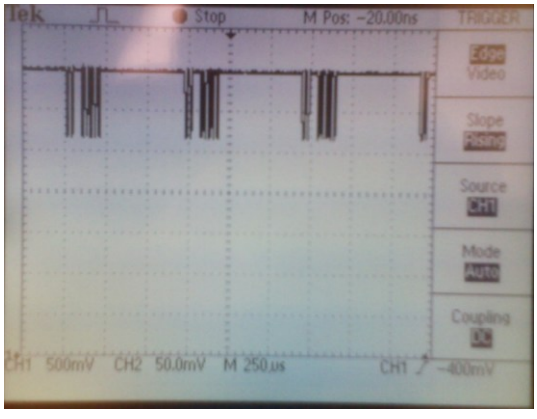


Fig. 7.12: Demodulator output as seen in oscilloscope

The testing of the backscatter and digital circuits was not done as individual blocks. This was done after connecting all the blocks together to form the tag. Thus, the operating range of the tag was measured. A properly functioning tag implies a correct operation of individual blocks.

7.4 Performance measure: Range -Simulation vs. Measurement

The next stage was to combine all the blocks and perform the complete RFID tag testing. Figure 7.13 shows the semi-passive tag with all the sections combined together and Fig. 7.14 shows the assembled passive tag.

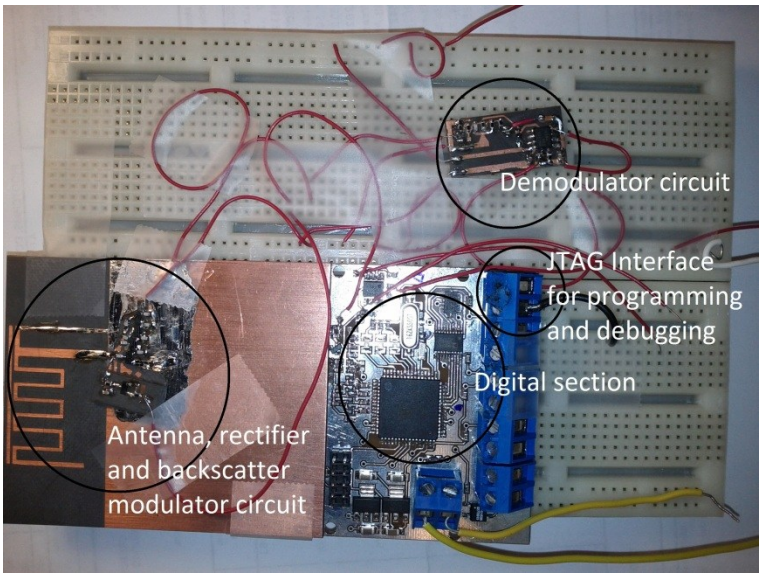


Fig. 7.13: Prototype tag#1 – Semi-passive tag

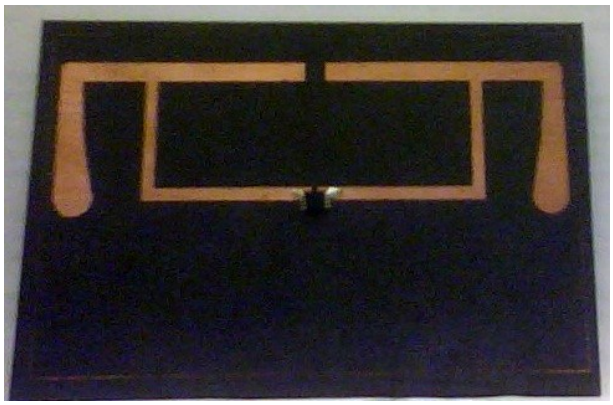


Fig. 7.14: Final RFID tag#2 – Passive tag

The most important performance characteristic of an RFID tag is its read range. Read range is the maximum distance at which the RFID tag can be detected by the reader. Various factors will affect the read range, such as propagation environment, tag orientation, etc. As explained earlier, the read range can be obtained from the Friis free-space formula,

$$r = \frac{\lambda}{4\pi}\sqrt{\frac{P_t G_t G_r \tau}{P_{th}}} \tag{7.1}$$

where λ is the wavelength, P_t is the power transmitted by the reader, G_t is the gain of the transmitting antenna, G_r is the gain of the receiving tag antenna, P_{th} is the minimum threshold power necessary to provide enough power to operate the RFID chip, and τ is the power transmission coefficient given by,

$$\tau = \frac{4R_c R_a}{\left|Z_c + Z_a\right|^2}, 0 \le \tau \le 1 \tag{7.2}$$

where chip impedance, $Z_c = R_c + jX_c$ and antenna impedance $Z_a = R_a + jX_a$.

The range of an RFID tag can be used as a measure of its performance and an estimate can be predicted based on simulation results. Practical range evaluation was done in an anechoic chamber, and the maximum distance at which the reader and the tag can communicate with each other was measured. Substituting values obtained from simulation in (7.1), range estimation can be found for a range of frequencies. This performance curve is plotted for the following values of parameters:

- Gain of antenna#1 (G_r) at maxima is 0.46dB;
- Gain of antenna#2(G_t) at maxima is 1.32dB;
- EIRP ($G_r P_r$) of the reader is 30dBm;
- Frequency of operation is 915 MHz;
- Sensitivity of the RF front end is -5 dBm (based on minimum power level required for the charge pump circuit to function);
- Chip sensitivity is -15.23 dBm (Or 30μW, minimum operating power of the tag).

7.4.1 RFID tag#1 – Semi-passive tag

The chip and antenna impedances are plotted vs. frequency in Fig. 7.15. It can be seen that R_a and R_c are matched in the desired frequency range. Also, X_c and X_a are complex conjugate matched to give maximum read range of 1.39m at 915 MHz as shown in Fig. 7.15. This estimate gives the maximum possible range, since damping due to object materials and environmental conditions are not taken into account.

The read range is measured inside a far-field chamber. The maximum range is measured by moving the tag farthest away from the reader with successful communication. The setup is shown in Fig. 7.16, for the dipole tag designed. The range for the semi-passive RFID tag is found out to be 1m at 915 MHz.

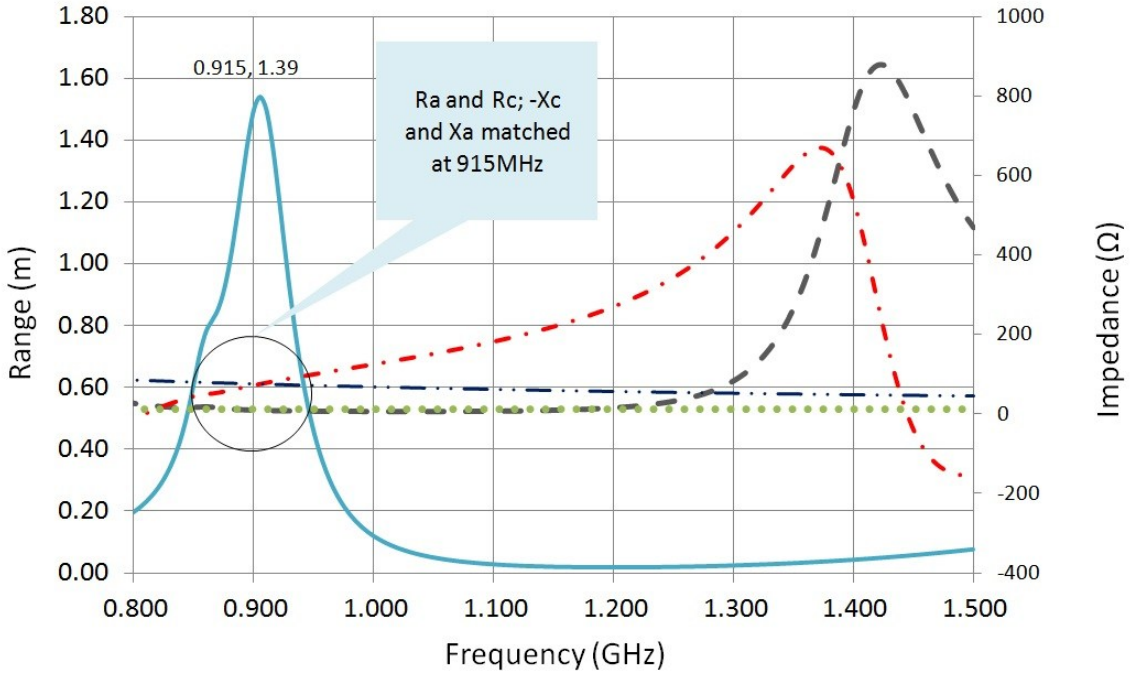


Fig. 7.15: CIFA - Impedance and Range vs. Frequency

7.4.2 RFID tag# 2 – Passive tag

Similarly, the second tag impedance and range are plotted vs. frequency and shown in Fig. 7.17. The maximum range obtained based on simulations is 5.34m. Range of RFID tag#2 is also measured in anechoic chamber and is found to be more than 4.8m. This was the maximum range, which can be measured inside the chamber because of its size limitation. Since the tag is expected to have higher range, it was measured at lower power level of 21dBm EIRP. At this power, the maximum range at which the tag can communicate is 2.84m, which is quite good. When measured in a real scenario of using the tag inside a building corridor, passive tag showed very promising read ranges of about 15m. The reason for improved range can be attributed to better signal strength due to reflection from the walls of the corridors.

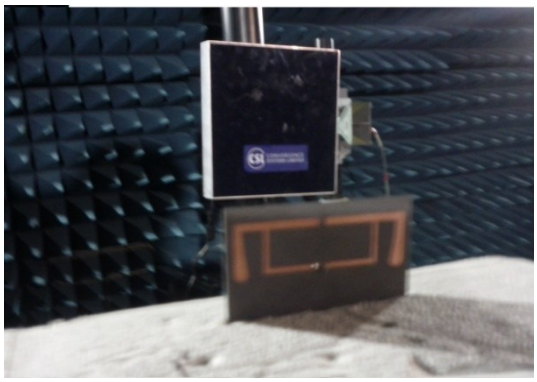


Fig. 7.16: RFID tag test inside far-field chamber

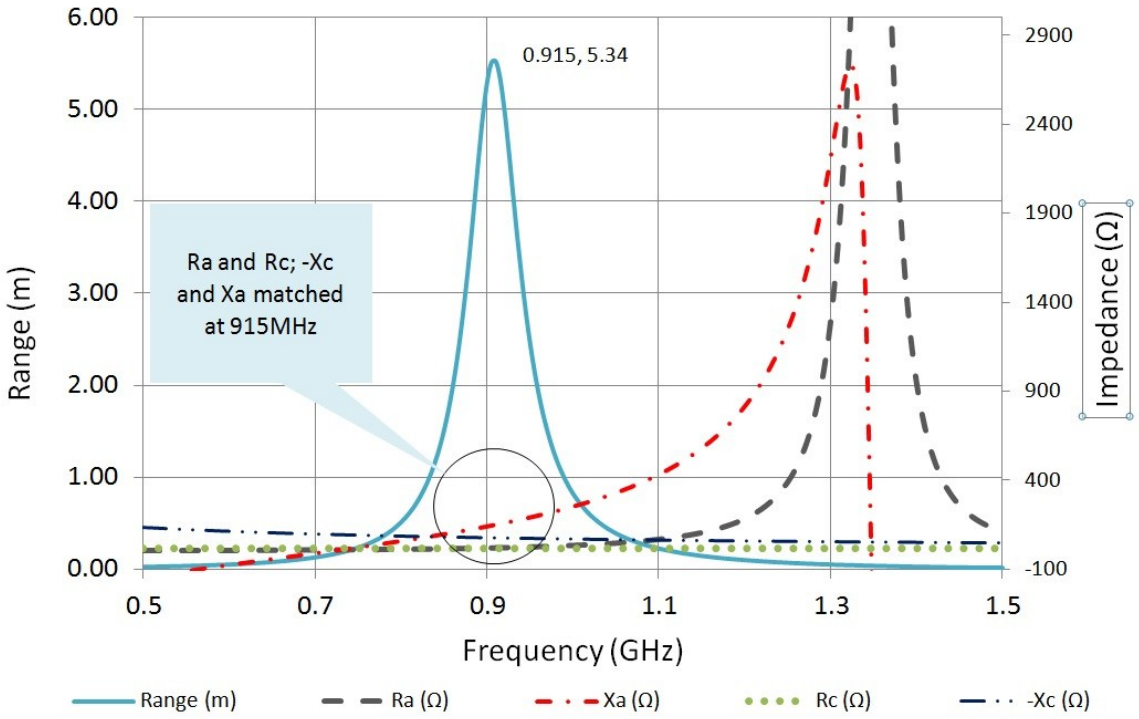


Fig. 7.17: Dipole - Impedance and Range vs. Frequency

7.5 Conclusion

Two RFID tags were designed and tested. RFID tag#1 is a semi-passive made from discrete components while RFID tag#2 is a passive RFID tag using a transponder chip.

Note that the individual blocks of the semi-passive RFID tag were first tested and optimized individually. Then, all the blocks were combined together to build the complete tag. The test results were in complete agreement with the simulation results. Range measurements were done in far-field chamber and for the semi-passive tag, the range obtained is 1m for a reader EIRP of 30dBm. In the case of the passive RFID tag, the range obtained is 2.84m for an EIRP of 21dBm.

Chapter 8: Conclusion

8.1 Summary

This work outlines the design of two RFID tags with a commercially competitive range. The first objective was to enhance the performance of a semi-passive RFID tag afforded by the collaborating company. Based on discrete components, the design of this tag was achieved through a thorough analysis of each block and final design was proposed after considering different configurations. The design of the antenna, charge pump and modulator and demodulator circuits were also discussed. The digital section of the tag was taken from the collaborating company. A promising measured range of 1m is achieved.

The second requirement was to design a passive tag with a range of more than 10m in its actual implementation. The passive tag done in this design achieves a range of 15m when tested inside the building corridor. The passive RFID tag design involves choosing the transponder IC and matching antenna. The antenna is designed to have the maximum range. All these designs were fabricated and tested and an acceptable agreement was reached.

8.2 Contribution

The main contributions of this thesis are the following,

- A semi-passive RFID tag which supports the basic EPCglobal Gen 2 Class 1 has been designed and tested. The read range of the tag is found to be 1m.

- All the individual blocks in the Semi-passive tag have been designed, analyzed and optimized for the desired operation. Antenna, modulator, demodulator and backscatter circuits were designed for the tag. The antenna used is a CIFA and was designed and optimized to match the tag circuit impedance.
- A modified dipole with a T match and tip loading at ends was designed and implemented for passive RFID tag aimed for commercial deployment. The read range of the tag is 2.89m for reader EIRP of 21dBm. When measured in a real scenario of its use inside a building, the range is measured at a building corridor and the results showed a range of 15m. This range can be considered as commercially competitive.

8.3 Future work

The thesis work can be expanded in several other directions.

- The individual blocks can be designed in a single chip to have all in one RFID transponder IC.
- The main objective of the thesis was to design an RFID tag with a competitive read range. The next extension can be to design tags that are orientation insensitive or can operate in metal-water scenarios etc.
- The other direction for future work will be to measure the sensitivity of various transponder ICs to find the transponder IC with the best sensitivity. Measurement of transponder input impedance can also be done and results used in the design of the antenna. The results in this thesis are based on the information provided by the chip supplier and simulation.

APPENDIX A

MAX 942 DATA SHEET [34]

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

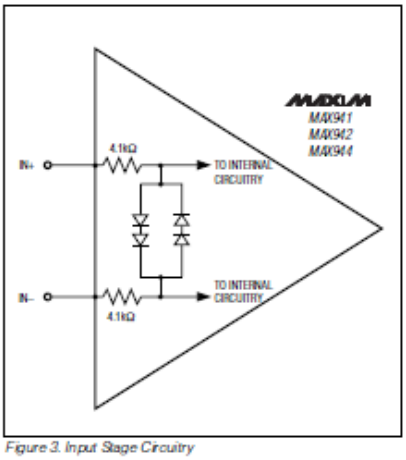


Figure 3. Input Stage Circuitry

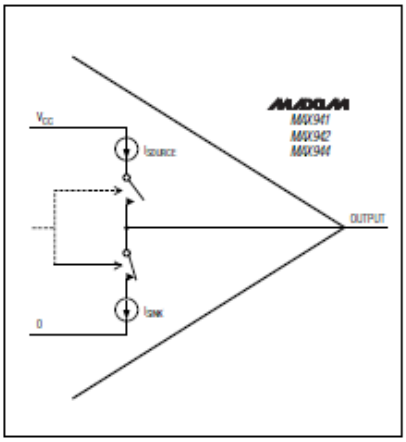


Figure 4. Output Stage Circuitry

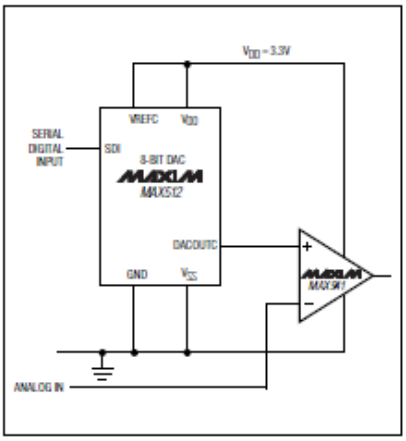


Figure 5. 3.3V Digitally Controlled Threshold Detector

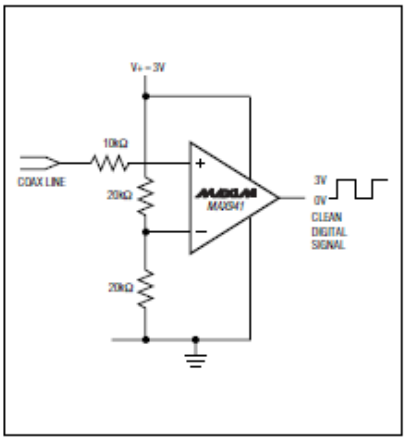


Figure 6. Line Transceiver Application

APPENDIX B

ATmega128 DATA SHEET [65]

Features

- High-performance, Low-power Atmel®AVR®8-bit Microcontroller
- Advanced RISC Architecture
  - 133 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers + Peripheral Control Registers
  - Fully Static Operation
  - Up to 16MIPS Throughput at 16MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 128Kbytes of In-System Self-programmable Flash program memory
  - 4Kbytes EEPROM
  - 4Kbytes Internal SRAM
  - Write/Erase cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Up to 64Kbytes Optional External Memory Space
  - Programming Lock for Software Security
  - SPI Interface for In-System Programming
- QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix acquisition
  - Up to 64 sense channels
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - Two Expanded 16-bit Timer/Counters with Separate Prescaler, Compare Mode and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Two 8-bit PWM Channels
  - 6 PWM Channels with Programmable Resolution from 2 to 16 Bits
  - Output Compare Modulator
  - 8-channel, 10-bit ADC
    - 8 Single-ended Channels
    - 7 Differential Channels
    - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Dual Programmable Serial USARTs
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - Software Selectable Clock Frequency
  - ATmega103 Compatibility Mode Selected by a Fuse
  - Global Pull-up Disable
- I/O and Packages
  - 53 Programmable I/O Lines
  - 64-lead TQFP and 64-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V ATmega128L
  - 4.5 - 5.5V ATmega128
- Speed Grades
  - 0 - 8MHz ATmega128L
  - 0 - 16MHz ATmega128

ATMEL

8-bit Atmel Microcontroller with 128KBytes In-System Programmable Flash

ATmega128
ATmega128L

Rev. 2467X–AVR–06/11

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