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FACULTY OF GRADUATE AND
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GRADE / DEGREE

Systems Science

FACULTÉ, ÉCOLE, DÉPARTEMENT / FACULTY, SCHOOL, DEPARTMENT

Built-in Self-test Techniques for Analog and Mixed Signal Circuits

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**BUILT-IN SELF-TEST TECHNIQUES
FOR ANALOG AND MIXED SIGNAL CIRCUITS**

By

Jila Zakizadeh

**A THESIS SUBMITTED TO THE FACULTY OF GRADUATE AND
POSTDOCTORAL STUDIES IN PARTIAL FULFILMENT OF THE
REQUIREMENTS FOR THE
DEGREE OF MASTER OF SCIENCE (SYSTEMS SCIENCE)**

**SYSTEMS SCIENCE
FACULTY OF GRADUATE AND POSTDOCTORAL STUDIES**

UNIVERSITY OF OTTAWA



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395 Wellington Street
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Ottawa ON K1A 0N4
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Your file *Votre référence*

ISBN: 0-494-11469-X

Our file *Notre référence*

ISBN: 0-494-11469-X

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Acknowledgement

First and foremost, I would like to express my sincerest appreciation and gratitude to my supervisor, Dr Sunil R. Das, Professor Emeritus, School of Information Technology and Engineering, University of Ottawa, Ottawa, Ontario, Canada, for his patient guidance, constant support, both moral and technical, and active cooperation during the entire period of this research was carried out. Without him this work would never have materialized in its current form.

Thanks are also due to Dr. Mansour H. Assaf of the School of Information Technology and Engineering, University of Ottawa, for his constant help and unforgettable support during the entire period of this research.

I want to thank specially Ms. Monique Walker of the Department of Systems Science for her administrative help that is truly appreciated.

I would also like to express my gratitude to all my friends and colleagues at the University of Ottawa, who helped me immensely in successful completion of this work.

Finally, I owe very special thanks and gratitude to my family members for their love and never-ending support.

Abstract

The present thesis attempts to develop new techniques for testing analog parts of embedded cores-based mixed signal integrated circuits and systems. In particular, the oscillation based test methodologies have been investigated in the thesis. In the oscillation based test methods, the circuit under test (CUT) is first converted to an oscillator in the test mode and the oscillation parameters, viz. frequency, amplitude, etc. are then measured. Any deviation of these parameters causes either the oscillation frequency of the converted CUT to differ from its nominal value, or the converted CUT stops oscillation altogether. For evaluation purpose, a program has been written in C to help us in simulating our test methodologies. The program is used to inject faults to the circuit under test. The detailed experimental results provided give frequency and amplitude measurements data performed on the individual circuit blocks together with fault coverage. In this work, however, only catastrophic faults were considered. The simulation experiments carried out on different circuits not only demonstrate that the developed approaches are quite feasible but show in addition that the fault coverage is quite satisfactory (100%) in all cases.

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List of Abbreviations

AMS	Analog and Mixed Signal
ASIC	Application Specific Integrated Circuit
ATE	Automatic Test Equipment
BILBO	Build-In Logic Block Observer
BIST	Built-In Self-Test
BJT	Bipolar Junction Transistor
CAD	Computer-Aided Design
CALBO	Cellular Automata Logic Block Observer
CMOS	Complementary MOS
CUT	Circuit Under Test
DfT	Design for Test
DOT	Defect-Oriented Testing
DUT	Device Under Test
DTMF	Dual Tone Multi-Frequency Detector
FET	Field Effect Transistor
HBIST	Hybrid Built-In Self-Test
IC	Integrated Circuit
LCD	Level Cross Detector
MOS	Metal Oxide Semiconductor
OBIST	Oscillation-Based Built-In Self-Test
OBT	Oscillation-Based Test
VLSI	Very Large Scale Integrated
SPICE	Simulation Program with Integrated Circuit Emphasis
SPOT	Specification-Oriented Testing
SoC	System-on-a-Chip
TDM	Time Division Multiplexer
TPG	Test Pattern Generator
TRE	Test Response Evaluator

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Chapter 1

Introduction

Electronic circuits have become more complex with high integration densities and increasing demand in high performance applications. On the other hand, the design and manufacturing of high volume products never guarantee 100% yield in semiconductor processing and they usually need rigorous design effort, detailed testing, with an evaluation of prototypes before production. Thus, testing becomes an essential part of the whole design process. The major aim of detailed testing is to ensure if the manufacturing products are defect free and meet specifications. Moreover, the information that can be obtained would help us in increasing the product yield and consequently reducing the product cost. When we take a close look at the IC fabrication process that consists of photolithography, printing, etching and doping steps, we will find that these steps are not done perfectly in real world and these errors may introduce some failures in the operation of each individual IC. Specially, the performance of mixed signal IC will fail since Mixed-Signal circuits are very sensitive to very small errors in any step. In the digital circuits, some errors are unimportant; however, in the mixed signal circuits, minor errors such as small capacitance between the traces can present a significant circuit component, which can change the circuit performance dramatically. By shrinking the circuit geometry, the circuit performance sensitivity is exaggerated such that IC may malfunction with very small error in its production process. That is why each IC must be tested prior to shipping to a customer. The testing improves quality of product by preventing shipping of the defected IC, although the testing has no effect on IC quality as an individual entity. The testing assures quality of a product when implemented during key phases of product development. It can be a method for validating design and checking process. High sensitivity of mixed signal circuits to very small fault during design process and their broad specifications require very detailed and long performance tests. These requirements result in the high cost test that necessitates the need for research in the field of mixed signal testability. In order to reduce the test cost in mixed signal ICs, researchers are seeking to combine both analog and digital testing techniques either applying digital signal such as serial bit stream to drive analog circuits, or analog signals to drive digital circuits.

As ICs become larger and more complex, the testing of IC during the design phase and design for test (DFT) becomes more essential; otherwise, testing will be very costly. A DFT method reduces test application time, improves fault coverage, or reduces test generation. In DFT, some features are added to the circuit during design phase to make the circuit testable. These features include: adding I/O pins on an IC for injecting or monitoring signals,

disconnecting certain internal interconnections during the test time, or partitioning the complete circuit into blocks that are individually testable. Reconfiguring circuit such that it would have different modes of operation can make a circuit testable as well. Nevertheless, the reconfiguring of the circuit would add to the complexity of the circuit design. It is worthy to have a review of the test history before we reveal the motivation behind this research.

History

Historically, all electronic circuits were made with analog components that were mounted discretely on a board. The first efforts to develop the alternative test methods for analog circuits were made in 1960s and the efforts concentrated on discrete analog circuits. During the test, every node was accessible and the challenge in testing was to reduce test time. Purpose of the discrete circuit test was not only to detect the faults but also to diagnose the fault, which identifies the faulty component, where repair of the circuit was important. All branch currents and node voltages of the circuit were computed by measuring few branch current and node voltage; then the computed values were compared with their expected values thereby identifying the faulty circuit. Through advent of the integrated circuits, the analog and digital functions have been developed on the separate ICs and they had interconnections only at the board level. However, in the last decade, both analog and digital circuits are implemented on the same IC. This chip is called mixed signal IC. Advances in integrated circuits made changes in the testing process; for instance, the diagnosis and location of faults are unnecessary since circuit cannot be repaired easily. But the fault diagnosis will be important if the manufacturing process has poor performance with high rate of faulty parts.

Although the advances in integrated circuits made possible the designing of very large circuits on a very small silicon area, accessibility of the nodes gets limited such that only the inputs and output pins are accessible from outside the board. This is not a problem for testing entirely digital circuits, since many efficient digital test techniques have been developed. Nevertheless, it is problem in analog circuits. We cannot eliminate the analog parts from any system because in real world where the circuit must interface with outside the board, we would need analog and mixed signal circuits such as ADC, DAC, etc. more often in a system-on-a-chip (SoC). However, mixed signal test is given more attention since they can be integrated with digital circuits.

Current Research

Test is system dependent and fall into three categories: digital, analog and mixed signal test. Recent research has concentrated on analog and mixed signal IC test. Integration increases test difficulties due to limitation in the pin counts such that access to internal signals is very hard and sometimes is impossible. Even input and output of an analog part of a system may not be directly accessible and as such measuring such signals is a very difficult task. Nowadays, researchers emphasize on the testability techniques that will reduce manufacturing test cost.

Digital test methodologies are very well developed. These include D-algorithm [2], Built-In Logic Observer (BILBO)[3], Level Sensitive Scan Design (LSSD) [4] and IEEE Standard 1149.1 [5][6]. In contrast, analog test methodologies are underdeveloped such that analog test is bottleneck in mixed signal test, especially when industry attempts to shrink analog circuits on a very small area. Although mixed signal test takes benefit of the digital test development and experience, analog and mixed signal test development is still far beyond the digital test. The reason is the lack of accepted test principle such as a standard fault model for analog components. Almost all the digital test techniques are based on stuck-at fault model and the algorithms are evaluated by their fault coverage. Although the stuck-at fault model for functional test is accepted, a model for performance test is not accepted easily. Furthermore, source of test difficulties in digital and analog circuits is different; for example, the circuit's size and complexity of digital circuits add difficulty to test whereas the behavior of circuit signals is more important than the circuit size in analog and mixed signal circuits. One problem in analog testing is the defining of the line between fault-free and faulty analog circuits that affects the quantifying of the product yield. However, fault coverage in analog circuit is defined as the number of detected faults to the total number of possible faults.

1.1 Motivation

As complexity of analog and mixed signal IC increases, the necessity for proper test solution is highly noticeable. Recent test techniques that are applied in the industry are not proper enough such that they may affect the manufacturer in terms of time, cost, and product throughput. For instance, the redundancy in a functional test makes it a time-consuming test method. Furthermore, Automatic Test Equipment (ATE) is getting very complicated and costly as complexity of IC arises. The importance of research and development for the efficient test methodologies become

apparent especially when the technology is pacing fast to implement high speed and high performance systems on a very small area. Test problem is almost feasible for the entirely digital circuits since the research is on going smoothly in digital area as the technology is getting toward the nanometer range. Systems have to interact with outside world; this will not be possible without analog and digital interaction. In other word, analog and mixed signal circuits help system to interface with the outside world. Test problems arise when analog and mixed signal circuits are implemented on a chip since analog testing still is on its way to improve and it has many difficulties. Some of the difficulties in analog testing include the lack of proper fault models, sensitivity to distortion, measurement errors, and node inaccessibility. Analog testing has become the bottleneck of mixed signal testing.

Along these difficulties, broad specifications, high sensitivity to tolerance of mixed signal circuits, lack of accuracy for CMOS technology smaller than $0.18\mu\text{m}$ [7] and unavoidable process tolerance lead to an alternative test solution. Design for test (DFT) and built-in self-test (BIST) are the test solutions that enhance test process performance and reduce the test cost.

Many DFT methods are proposed for the controllability and observability of the nodes, but the test pins coming out the chip are limited by condensing the integrated circuits on a chip. On the other hand, analog signals are likely to be corrupted due to parasitic loading and coupling of the transmitted test signal to the ATE. Hence another test technique is required. A BIST technique is an extreme outcome of DFT, where the whole or partial test process is done on the chip.

BIST has some advantages over other DFT methods. BIST method reduces the test time and the test equipment cost, and the test result is only a pass or fail bit or a multibit signature. Also BIST method allows an IC to be operated on its normal operating speed and consequently the timing faults can be detected. And the other advantage is that on-chip test circuitry is not accessible from the outside world so that the test performance will not be degraded by external noise, especially when there is an analog block with low-level input signal on the chip. Despite these advantages, sometimes, area and performance overhead and increasing design time keep industry away of using this technique. Nevertheless, the interest in BIST is rapidly increasing since operating speed, pin count and complexity of ICs are increasing fast.

Ease of implementation is extremely important in accepting a new methodology. Every new test technique must be proven in simulation, hardware and production. Although many BIST methods are proposed for analog and mixed signal ICs, most of these methods use the conversion of analog test problem to digital test problem. Thus a powerful Digital Signal Processor (DSP) is required on the chip for processing the obtained data. Otherwise, processing the obtained data is very time consuming in order to determine if a CUT will pass or fail. This will affect the product

throughput since the large volume of data is transferred to ATE in order to be processed off-line. For this purpose, the data should be stored somehow in the memories and this will definitely add complexity to the test problem. On the other hand, BIST requires an effective signal generator. Multitone digital oscillator is a good option but it usually needs huge hardware resources [8]. In contrast, there is a method that alters the circuit structure in order to generate a signal that will reflect the CUT performance. This method is called Oscillation-Based Test (OBT) method which is promising since conceptually it is simple and in addition there is no need for any complex test circuitry. The OBT method is a fault-based method [9]. It can be applied as either an off-line or an on-line testing method. On-line testing that is so called Oscillation-based Built-In Self-Test (OBIST) has a test circuitry that is embedded on the same chip as the circuit itself. The idea is simple such that the circuit under test (CUT) is converted into an oscillator by additional circuitry. Then oscillation parameters are measured and compared with the oscillation parameters of fault-free case. Then the faulty circuit is detected. In this work, OBIST method is investigated for testing analog part of the mixed signal circuits because it is a promising method which neither requires a stimulus generator nor a complex result analyzer.

1.2 Thesis Overview

This thesis is dedicated to the following objectives:

- Investigating Oscillation-Based Built-In Self-Test method by applying it for an inverter, CMOS Operational Amplifier, state-variable filter, and voltage controlled voltage source filter.

Chapter 2 provides some background in order to understand the test problem. The background consists of overview of BIST for digital ICs, mixed signal ICs architectures, analog and mixed signal test, and previous works on BIST for mixed signal ICs.

Chapter 3 describes oscillation-based test strategy, OBIST architecture, and techniques for modifying the circuit under test to make it testable in the OBIST method. Also fault model and test procedure considered for this work are explained. An example is demonstrated at the end of this chapter.

Chapter 4 presents the experimental results of applying OBIST method for CMOS operational amplifier, continuous-time state-variable filter and VCVS filter.

Chapter 5 concludes the thesis and discusses future work.

Chapter 2 Background

Referring to Moore's first law about the microelectronics revolution that the number of transistors in a chip has been doubling in every 10 months is leading to more functionality for integrated circuits (IC). With the current trends in IC fabrication and advances in the electronic packaging, we are experiencing tremendous development in the area of mixed signal technology. Interfacing system with outside world demands the necessity of mixed signal circuits. For instance, the requirement of analog circuits inside a chip will be apparent when a speech signal has to be converted to digital signal, a digital bit streams has to be converted to radio frequency (RF) modulation pattern, and a microprocessor has to receive signal from sensors. Applications of mixed signal circuits could be seen in smart sensors, automotive ASIC, portable devices (laptop, cellular phones, etc) and on-chip functionality (on-chip TV). The analog circuits sit very close to the digital circuits in mixed signal devices, which create design challenge and may create difficulty in their test. The demand on mixed signal test is increasing as the demand on mixed signal ICs is growing.

One of the important aspects in designing and evaluating of the ICs lies in their ability to be tested under analog test or digital test or mixed signal test environments. Analog test and digital test procedures had been a research topic for many years in industry and academia. But currently there is a huge need for the development of mixed signal test methods. Generally, testing is a verification process and determines whether design specification has been met. Test of mixed signal circuits is always complex and challenging and hence semiconductor industry attempts to find the proper ways of testing and to lower the cost of test particularly for analog portion of mixed signal devices. Table 2.1 shows the importance of this endeavor [11].

Table 2.1. Comparisons between analog and digital circuits that embedded in a mixed signal circuit.

Mixed signal IC	Analog part	Digital part
Area	10-20%	80-90%
Design effort	80%	20%
Test cost	85%	15%

As Table 2.1 shows, up to 85% of the test cost is dedicated to the analog functions that typically occupy only around 10% of the chip area. Therefore reducing the test cost is a very important issue for analog parts since its cost largely exceeds the test cost of digital parts.

Many parts of the systems-on-a-chip (SoC) are not accessible due to complexity of SoC, and SoC has limited test pins. However, accessibility of a node that is either controllable or observable in a circuit can be increased using design for test (DFT) strategy [10],[62]. DFT is well established in digital domain like DFT in full or partial scan circuits that successfully implemented in most complex systems (vide the IEEE standard 1149.1 test access port and boundary scan architecture and BIST). Although this strategy reduces the test cost, some noise will be introduced by transferring the signals between the tester and circuit under test (CUT). Since analog signal has very high sensitivity to crosstalk and noise, false detection will occur very frequently.

Therefore, built-in self-test (BIST) can be a solution for this problem. This idea was first proposed around 1980 and has grown to become one of the most important testing techniques at the current time, as well as for the future. BIST technique allows the circuits to test themselves. Nevertheless, BIST technique has advantages such as reduction of automatic test equipment (ATE) cost as well as test time, testability of untestable functions, which are faster than ATE, elimination of off-chip interfacing, ability to be tested many times during manufacturing cycle of the product and consequently optimization of test.

2.1 BIST for Digital ICs

Before elaborating the digital BIST, it is better to explain about fault model and digital test methodology. Generally, four principal fault models are considered important for digital circuits: stuck-at faults, bridging faults, stuck-opens faults, and pattern sensitive faults. Major contributor to the success of digital testing is its well-defined fault model, stuck-at fault model. Stuck-at fault model is the most common model used in digital testing. This model assumes that every physical defect in a digital circuit makes a pin fixed either at logic zero or logic one. These faults concentrate on the gate level at the circuit design, and we do not directly consider the overall primary input and output functionality of the circuit. But as complexity of a circuit is arising, testing at gate level becomes a very difficult task. Thus recent testing methodologies concentrate on testing at functional or behavioral level.

Generally, in digital testing only the functional test is applied and unlike the analog testing, there will no need for parametric test. In digital testing input test pattern are applied to the CUT and output signals are observed which determines the circuit characteristics, and then a decision is made. Normally, testing of all ICs has to be performed through the input and output pins of the ICs. To test a digital circuit, generation of appropriate test vectors is required. Automatic test pattern generator (ATPG) generates proper test vectors for the CUT. ATPG program runs until the fault coverage is in accepted level or runs for a given time. ATPG program is inadequate for very complex VLSI circuits and is replaced by self-test or other test strategies. By allocating very small silicon area for an IC, access to every node is highly restricted. Moreover, by condensing the integrated circuits on a chip, access to every integrated circuit from outside the chip will be impossible due to pin count limitation. The pin limitation causes problems in testing. BIST circuit allows the CUT to test itself and returns a pass/fail bit or a multibit signature. Then a simple and low cost ATE will be able to determine the quality of the CUT.

In BIST circuitry, the CUT becomes its own test vector generator and test response analyzer and there is no need to any ATPG data based on stuck-at fault model. In fact, test generation is fault model independent [12]. Generally on-chip circuitry is used to apply a predetermined set of test vectors to internal sections of the circuit. And another on-chip circuitry is used to monitor the results of the test and to compare them with stored correct responses.

A generalized BIST architecture is illustrated in Figure 2.1. It consists of test pattern generator (TPG), CUT, test response evaluator (TRE), BIST controller for controlling the CUT and BIST circuitry in test mode and interconnections (data). The test pattern generator produces the digital input to be applied to the CUT and the test response evaluator may be a signature analyzer that verifies whether the CUT produced the correct sequence of outputs.

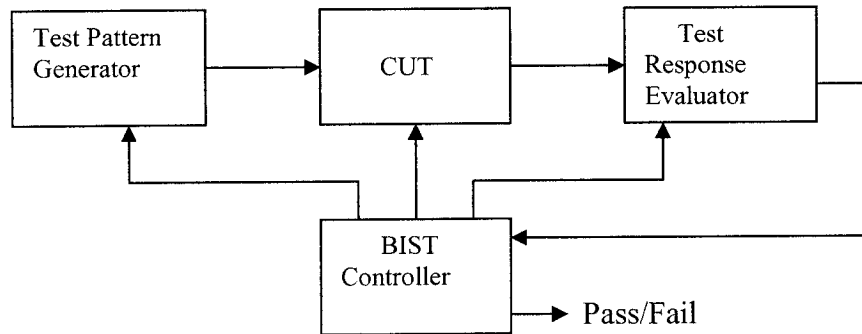


Figure 2.1. Typical digital BIST architecture.

For BIST of a chip, additional components like buses, multiplexers, scan paths and distribution system for data between TPG and CUT, TRE and CUT are required. Test sets can be generated for exhaustive, pseudoexhaustive, or pseudorandom testing.

Some of the common BIST approaches are the built-in logic block observer (BILBO), cellular automata logic block observation (CALBO), pseudoexhaustive BIST techniques, circular BIST, memory BIST, scan-based BIST, BIST for regular structures, microcode BIST, BIST for FPGAs and CPLDs, and the integration of BIST with concurrent fault detection techniques for on-line testing [13]-[15].

Many BIST approaches are proposed for increasing reliability and fault coverage. Das et al. [16]-[18] proposed efficient space and time compression support hardware for BIST that minimizes the storage requirement for the CUT with high fault coverage. Furthermore, several methods are used for generating the test patterns in BIST such as pseudorandom, pseudoexhaustive and weighted random test patterns. Finite automata and cellular automata are often used to generate and decompress test patterns, and create and store the output response signatures. Although weighted random testing is most effective, there are some faults that are

hard to test and they are not detected by above testing method. The solution can be mixed-mode test approaches. In this approach, deterministic testing is mixed with pseudorandom or weighted random testing. Deterministic test patterns are usually used for the design with restricted dissipated energy and test time.

2.2 Analog and Mixed Signal SoC

Combination of analog and digital elements in a circuit forms a mixed signal circuit. Some experts argue that mixed signal circuits are those that have significant interaction between analog and digital signals but there are some mixed signal circuits that include analog and digital signals separately and they never interact with each other. For instance, a CMOS comparator, which compares two analog voltages and determines if the first voltage is greater or smaller than the second voltage, is a mixed signal circuit since its inputs are analog signals and its output is digital. A CMOS inverter is also considered a mixed signal circuit since digital input controls its analog output between two levels of voltage. A CMOS analog switch can be considered as a mixed signal circuit since the resistor of transistor varies with digital signal. The most common mixed signal devices are analog to digital converters (ADCs) and digital to analog converters (DACs).

Process technology has allowed analog and mixed signal designers to integrate notable amount of functionality of a system onto a single chip. This movement, integrating a system onto a chip, is critical unlike ASIC design where SoC is optional. The cost and performance are objectives in today's electronics design world so that the designers are driven toward SoC technology [19]. In general, there are two types of SoCs: one type has grown from the ASIC world and the other has grown from the custom IC world. At the first type, the design is digital integration and it is interfaced with analog devices by embedded software. Analog and mixed signal blocks are integrated only when the time and cost spent on the integrating are reasonable. The latter type of design, which is called analog and mixed signal design, has high performance and complex signal paths through both analog and digital components. An example of the latter type of SoC is illustrated in Figure 2.2, where the main mixed signal components tend to be ADC, DACs, OpAmps, PLL, and filters.

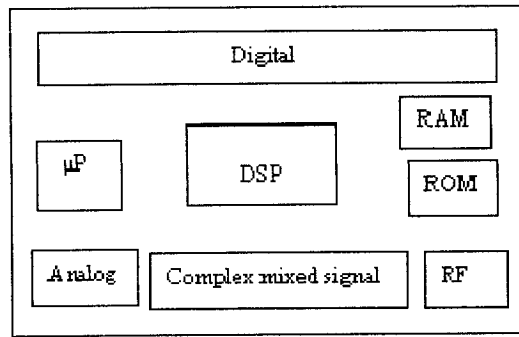


Figure 2.2. A typical analog and mixed signal SoC.

In general, there are two kinds of design methodologies: top-down design and down-top design methodologies.

Design flow for designing an analog and mixed signal SoC (as shown in Figure 2.3) consists of set of design stages as follows:

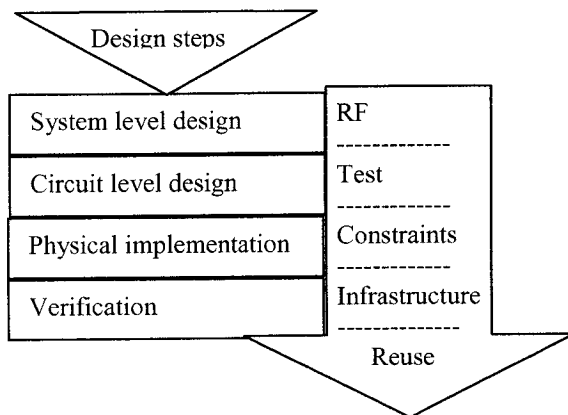


Figure 2.3 Design flow of analog and mixed signal SoC.

This is a typical design flow and all the details are not specified. As we know, a design starts with an idea; this is not an exception with designing the analog and mixed signal design. Thus, the design flow for analog and mixed signal circuits begins with an idea and ends up with a layout. Some steps that refine the design process are in between. These steps are based on specification and verification. At first, an idea is converted to a set of specifications that is verified by customers. Then the specifications are converted to the functional descriptions or an

algorithm that is verified by system simulator. The functional description is converted to architecture that is verified by simulator. In electrical design process, the blocks are converted to transistor level that is verified by simulator such as SPICE. On the other hand, the architecture is converted to a floorplan in physical design process; then all the blocks are laid out and routed. Then the layout and routes are verified by extracting the circuit from the layout. The layout verification assures all schematic matches and whether it satisfies all rules to be fabricated. Once the layout is completed, the entire design process is presented in detail. Since simulation of every fine detail is very expensive, the design process itself must assure the functionality of the design in all circumstances and if the design meets all specifications and requirements. Generally, the last thing before sending to manufacturing is to develop the test program that is verified by running it on the working model of the chip. The testing will be costly since the developing test program at the end of the design process will affect time to market and moreover, mixed signal testers are occupied for a long time to develop test program. Thus developing test program in the final step is not very efficient.

In the top-down design methodology, system level model of the chip is available early in the design process that can be used during developing the test program. This involves test engineers with project in early steps of design process. Therefore, test engineers can communicate with design engineers efficiently. The improved communication causes reducing the test development cost. Further, involving test engineers in design stages allows faults to be simulated and the design for test to be applied for chip. We will discuss about testing the analog and mixed signal chips in detail in the next section.

2.3 Analog and Mixed Signal Test

Purely analog integrated circuits unlike the digital integrated circuits usually consist of relatively few circuit primitives such as amplifiers, comparators and etc, but many parameters must be considered for test. Test parameters are specified by designers and can be gain, offset voltage, slew rate, signal to noise ratio, bandwidth and etc. Traditionally, analog circuits have been tested functionally for specification such as offset voltage, signal to noise ratio, etc. Functional test is still used in wafer level and packaged tests. This is due to lack of standard fault model for analog circuit. The goal of functional testing is to verify an IC if it meets the

specification. Figure 2.4 shows the testing that is applied in different stages during manufacturing process.

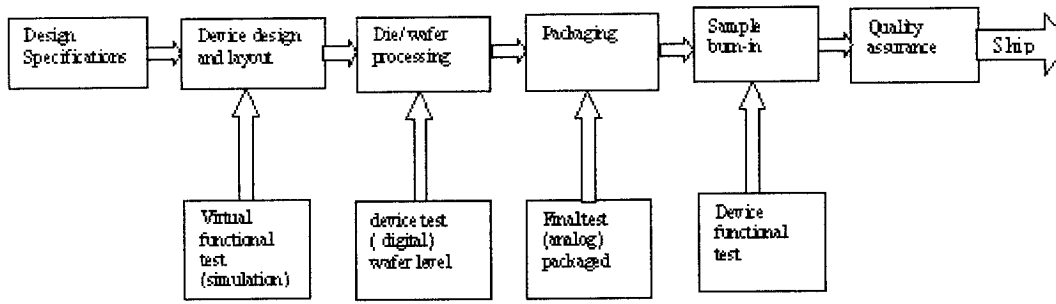


Figure 2.4 Simplified IC manufacturing flow.

Functional test is very time consuming because of redundant testing, and it requires engineering resources that is very expensive. Also, it is not effective in terms of fault coverage and yield cannot be estimated. In analog circuits not only catastrophic faults but also parametric faults must be considered. Therefore, in testing not only non-functional operation but also circuit performance must be checked.

It is known that an analog component is more difficult to be tested than a digital part. Lack of standard fault model, nonlinearity, continuous characteristics, ease of signal distortion and component tolerance of analog circuits make testing of them very difficult. In addition, analog circuit has smaller design margin; therefore high precision test equipment is required for testing such circuits. Many mixed signal circuits consist of amplifiers, filters, ADC, DAC and etc. The applications such as laptops, cellular telephones and modems are the complex mixed signal circuits.

Although the testing the individual circuits is important, testing the whole system will be necessary in order to guarantee the fault-free circuits. Condensing the integrated circuits into a single chip causes the testing of the mixed signal circuit a very challenging task. While developing a test method, test engineer faces challenges such as time to market, accuracy, repeatability, correlation, production test economic, electromechanical fixture, and so on[20]-[24]. Historical electronic circuits were once completely analog such that all the analog parts were mounted discretely on a board and every node was accessible during test. Research in test was to find the methods that would decrease test time.

Advancement in integrated circuits allows designing large electronic circuit on a very small area, but accessibility of the nodes is limited. Sometimes only the inputs and outputs are accessible during test. Pin count limitation is not the problem in testing of entirely digital circuits since very efficient test methods and techniques are available. Although reliability of digital design techniques allows engineers designing a big system entirely in digital, systems will need mixed signal circuits, such as ADC, DAC and etc, in order to be interfaced with the real world. Therefore, we cannot eliminate the analog parts from systems. Condensing the digital and analog circuits on a single chip that reduces the board size makes the testing very costly and complicated. Interaction between the digital and analog circuits is complex and unique for every application. Test engineer must understand the individual application prior to applying a test method; often test engineer and design engineer will spend lots of time to realize testable design that satisfies the specifications. That is why the testing of the mixed signal circuits is very time consuming. In contrast, digital circuits test problem are solved such that a structured testing approach is applied for very complex digital circuits. CAD tools are used to generate the necessary DFT structures automatically. Also these software tools are used to generate test patterns which are tested on prototypes of circuits including register transfer level (RTL) software descriptions, gate level software descriptions, and field-programmable gate array (FPGA) prototypes prior to the availability of silicon. However, simpler digital circuits such as those in many low-complexity mixed signal ICs can be tested without structured DFT techniques that need area overhead. Most digital circuit testing techniques are based on circuit partitioning to reduce test time and increase observability. Generally, a complex digital circuit can be partitioned into pieces that can be tested separately. Testing pieces individually can determine the functionality of the whole circuit. Other requirement of digital DFT is ability of reset and preset the registers and flip-flops to a known state before applying a test vector. Since failure mechanism and test requirements are not well defined for analog circuits in a mixed signal IC, mixed signal DFT cannot be standardized. Aim of every DFT technique is to increase

controllability and observability of internal nodes. Different DFT methods are applied according to the characteristic and specification of a circuit [25]-[27]. Figure 2.5 shows various DFT techniques that can be applied at various hierarchical levels of a mixed signal IC.

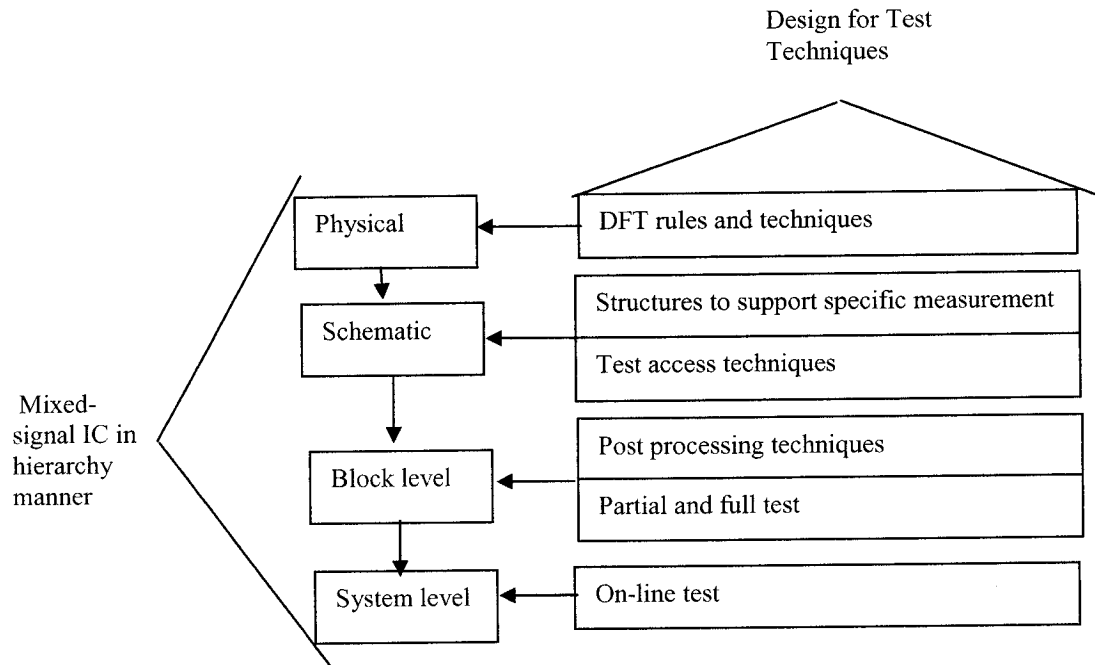


Figure 2.5 DFT techniques for hierarchical levels of a mixed signal IC.

At every level, specific DFT method can be applied to improve test coverage of an IC. Test techniques such as scan methods, analog test buses and BIST are the techniques that improve the testability of an IC. In general, analog and digital blocks in a mixed signal chip are tested separately such that each block is isolated by scan path. A scan chain is added to the interface between converters and DSP core. Scan chain allows digital test data to be loaded simultaneously to the shift registers and shifted out sequentially. Analog shift registers can be made by sample and hold circuit, but the error caused by sample and hold circuit motivated development of structure using analog multiplexers that reduce the error. This concept and success of the 1149.1 scan bus have developed IEEE Mixed Signal Testability Bus Standard P1149.4 [28], which improves test access at the chip level. Consequently, scan chain improves fault coverage and links failure to specific block.

2.3.1 IEEE Standard P1149.4

The great success of IEEE standard 1149.1 digital boundary scans standard has urged extending the idea of the 1149.1 to mixed signal testing and developing the analog bus standard, IEEE1149.4 that is the analog complement to IEEE1149.1. The 1149.4 standard allows analog test and verification of a chip to chip interconnection similar to traditional digital boundary scan. Also, it includes optional extension for internal analog signal testing. The major difference between 1149.1 and 1149.4 scan bus is that the 1149.4 standard has new test pins and analog switches. The 1149.4 structure is based on IEEE standard 1149.1 and an implementation is shown in Figure 2.6.

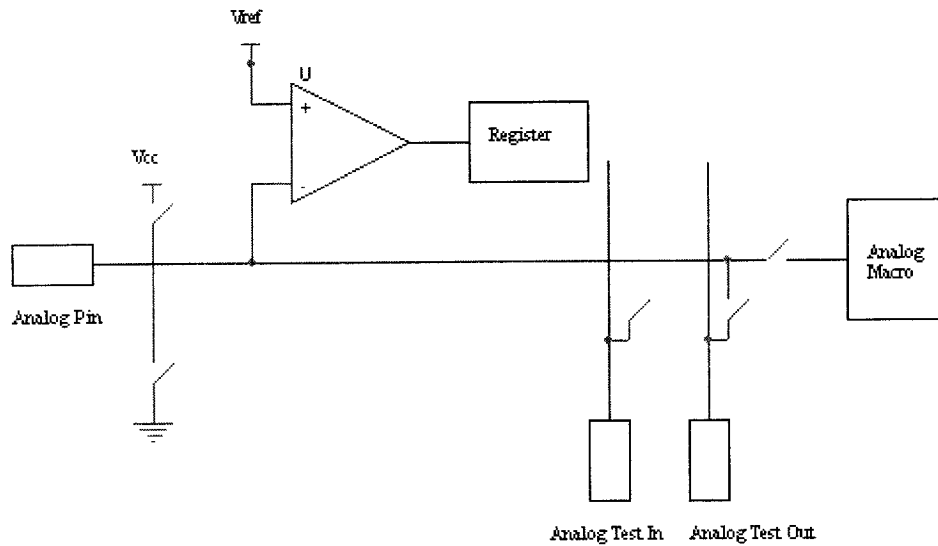


Figure 2.6. Simplified schematic of a P1149.4 test bus [67].

The structure requires two analog pins in addition to four mandated digital pins of the TAP controller (TCK, TMS, TDI, and TDO). The structure allows access to the internal analog nodes to test the interconnect failures such as shorts and opens, discrete analog components and network between ICs. The structure allows testing the analog functions within the ICs themselves as well.

Nevertheless, before applying this standard to the internal signal testing, some considerations such as the effect of the 1149.4 standard on analog circuit must be considered. The effect can be crosstalk between all the observed nodes. However, a solution can be the choosing of proper switches such as CMOS T-switch configuration which reduces the crosstalk effect. Figure 2.8 shows CMOS T-switch implementation that is used in analog test bus. CMOS transistor M1 provides ground to the midpoint of the switches in series. When two switches in series are opened, M1 turns on and shunts any potential crosstalk signal to the ground.

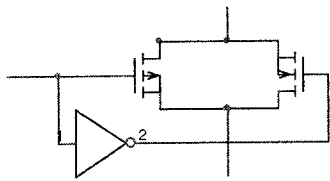


Figure 2.7 CMOS switch implementation.

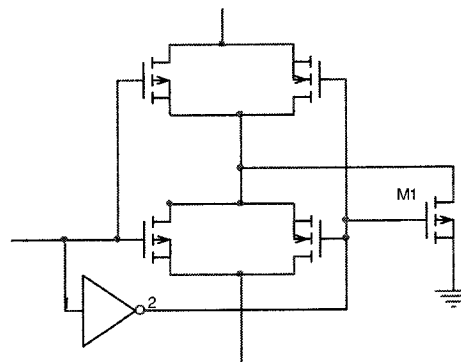


Figure 2.8 CMOS T-switch implementation.

Applying DFT reduces the test cost, improves quality of product, and makes easy the design characterization and test program development. To increase testability and controllability of internal nodes, test buses and scan circuitry are used. Nevertheless, output signal has to be transmitted through long wires in order to be measured and processed. Analog signals will be degraded easily through this transmission. Therefore, the test result will be falsified and hence production yield will be decreased. The solution to this problem can be a built-in self-test circuitry. In a BIST method, signal generator and response analyzer are implemented on a chip instead. However, CUT signal is less corrupted before being measured.

2.4 BIST for Mixed Signal ICs

BIST for digital circuits have been active area of research and development for about 25 years, and very good approaches for digital test of mixed signal ICs have been proposed and are being applied for testing circuits in industry. But analog testing is still on its way to be improved, and recently it is the interest of research community. Lack of standard fault model for components of analog circuits, broadness of analog specifications and incomplete test set may decrease test quality for analog portion. However, mixed signal BIST is more application specific solution rather than a general purpose solution. BIST requires some ATE functionalities inside the chip that include test stimuli generator, response analyzer and control circuitry. Figure 2.9 represents the typical mixed signal BIST.

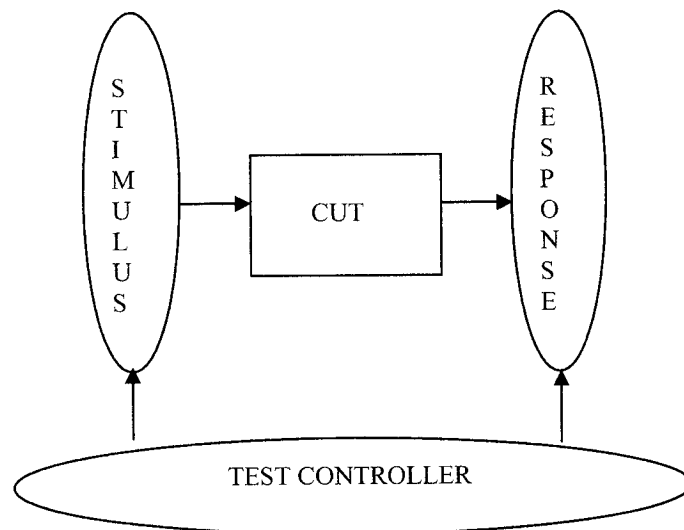


Figure 2.9 Block diagram of typical BIST.

There are two test techniques, functional that is specification based, known as specification-oriented testing (SPOT), and the other is structural that is fault based, known as defect-oriented testing (DOT). Functional test or SPOT technique is strongly depends on analog components of the IC, and generalizing functional test method will be unfeasible. Fault based or DOT technique is a cost saving approach that shows great promise [29X]. DOT is based on the assumption that major faults are predictable and known, and can be detected by measuring a set of parameters. Furthermore, quality of test can be measured by its fault coverage in DOT technique.

Different built-in self-test approaches for analog and mixed signal ICs have been proposed with respect to applicability, area overhead and test pattern generation [29]-[33]. BIST methods for mixed signal circuits are either fault-based or functional test. The fault-based test diagnoses the hard and soft faults as well as DC and AC faults, while in functional test the specifications are tested. Although the fault-based test techniques provide high fault coverage but the fault model is not general enough to get satisfaction out of testing. A promising test technique for analog BIST is fault-based testing technique; however, the fault-based approach can be taken to mixed signal testing if the design margin is not tight so that we do not need extreme accuracy in parameter measurement.

Ohletz [34] proposed a hybrid BIST method for mixed signal circuits. Figure 2.10 illustrates the implementation of HBIST.

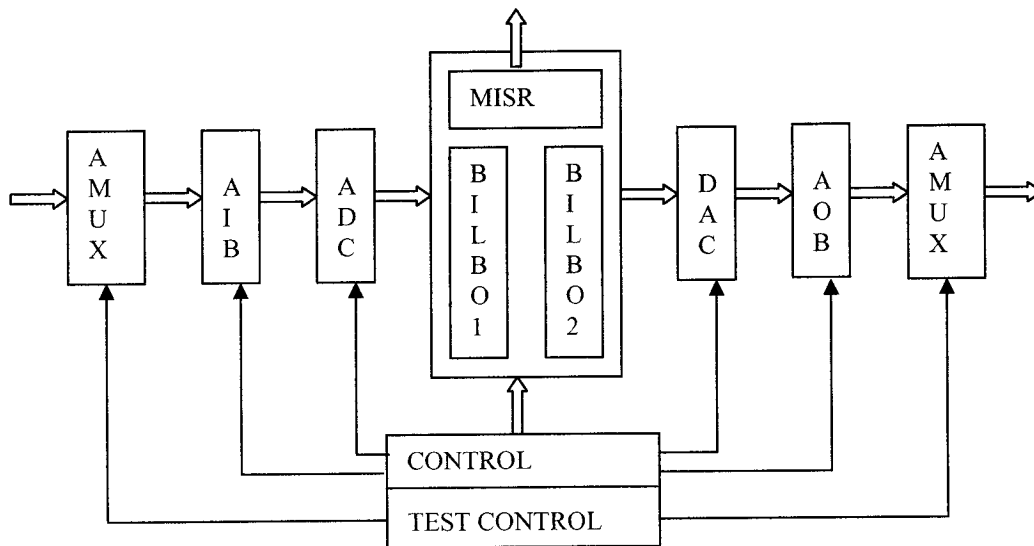


Figure 2.10 Implementation of Ohletz BIST.

In this method, a linear feedback shift register (LFSR), a DAC and an amplifier generate a pseudorandom input signal with different amplitude. During test mode, the inputs and outputs of the CUT are isolated from the system environment. An analog multiplexer (AMUX) disconnects the inputs and feeds the test stimulus. Test signals are generated by a hybrid test signal generator built by built-in logic block observer (BILBO2) and DAC. The output of analog input block (AIB) is converted to digital signal by ADC. Then the output is captured by BILBO1. Then the stored signal in the BILBO1 is fed to a multiple input signature register (MISR) which compacts

the data using signature analysis [34]. Therefore test response measurement takes place in digital domain.

Salmani et al. [35] proposed a BIST method called translation BIST (TBIST) measurement takes place in analog domain. A detection and translation circuit, which captures the parameter and converts it to a DC voltage, is used for every test parameter. Then the DC voltage is compared with two reference voltages. Then the result of test is stored in a digital shift register.

Chatterjee et al. [36] presents analog checksum BIST. The voltages at the selected internal nodes are summed. A cascade of integrators implements the checking circuit. If the circuit is faulty, the checking circuit generates a non-zero signal. The experiments are done only for linear circuits.

Negreiros et al. [37] presents the spectral analysis method for analog BIST. In this method, on-chip random signal generator is used and the power spectrum density is used as a system signature.

Frisch et al. [38] proposed Histogram-based analysis such that the shape of the fault-free (ideal) analog signal is created by software or taken from simulation result and the correspondent histogram is created. When an actual signal is sampled, its histogram is compared with the fault-free histogram. This technique is known as "at speed" test technique. Histogram-based BIST can be used for measuring the characteristics such as clipping, crossover distortion, and integral and differential linearity of analog circuits [39].

Velasco-Medina et al. [40] present the current-based analog checker to analyze the output test response. It is used in such a way that first, voltage is converted to current, then AC current is converted to DC current which is proportional to the amplitude of the AC current signal, and at last the DC current is compared with two reference currents.

Brosa et al. [41] introduce a BIST method that uses the relation between the input and output in the XY plane. The obtained XY shape (Lissajous curves) contains the information about the circuit. Digital signature is created based on the information in XY mode. A fault in a CUT causes the XY shape of the circuit under test to deform, and hence its signature will differ from the fault-free one. So a faulty circuit is detected by comparison of the signatures. In this method a control line is automatically generated in XY plane, and a counter is used to determine the number of times the Lissajous curve crosses the control line during a certain period of time. The number, which the counter shows, determines the BIST signature.

Mir et al. [42] presented a unified BIST approach (AUBIST) which is a system level BIST approach. The output response of cascade biquads is compared in this method.

Wang et al. [43] propose a BIST structure in which a virtual instrument that based on ADC and DAC converter technology is used for generating the test inputs, measuring the outputs and comparing the measured response with fault-free response. It is shown that most circuits can be tested only with a single test frequency and sample point with proper circuit synthesis. In general, digital signal processing (DSP) based BIST consist of two converters, ADC and DAC. The DAC generates the test stimuli for the analog part of the CUT whereas the ADC converts the analog test response to the digital signal to be analyzed by DSP. This setup allows the DSP to test the analog part of the CUT without any additional analog component or mixed signal ATE.

Toner et al. [44] propose MADBIST concept for sigma-delta converters. This method is a functional test technique and it is suitable for a mixed-signal circuit where the digital kernel is surrounded by analog circuits in the input and output.

Sunter et al. [45] present an algorithm that calculates the analog parameters of DAC and ADC.

Huang et al. [46] present a delta-sigma modulation-based BIST. Figure 2.11 illustrates the delta-sigma modulation-based BIST architecture. To generate the desired stimulus, a software $\Delta\Sigma$ modulator converts test signal to 1 bit digital stream then this 1 bit digital signals, digital 1's and 0's, are converted to two analog levels by one bit DAC then pass through the low pass filter to remove modulation noise. The generated stimulus signal is applied to the CUT. To analyze the test response, a 1 bit $\Delta\Sigma$ modulator converts the analog CUT output signal to the 1 bit digital stream which is then analyzed by DSP or microprocessor of the core.

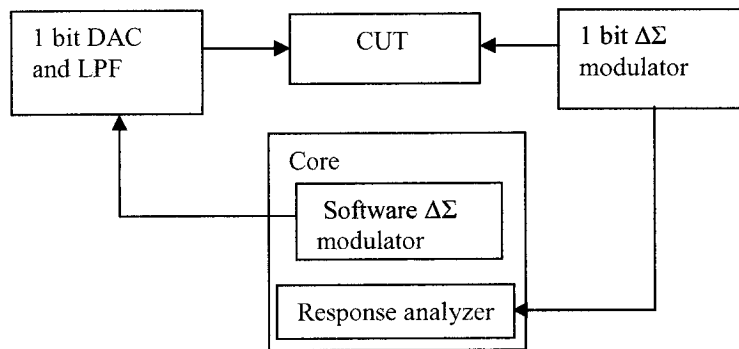


Fig 2.11 Delta-sigma modulation-based BIST architecture.

Among all the fault-based test strategies, Oscillation-based BIST deserves special attention because it is conceptually simple and extensive modification for testing purpose is not required [47]. In OBIST methodology, the CUT first is converted to an oscillator and oscillation parameters are extracted and compared with fault-free condition parameters. Arabi et al. [47] uses an LCD (Level Cross Detector) and a counter to measure frequency of oscillator output. A control unit compares the measured frequency with frequency of fault-free oscillator and then determines if the CUT fails or passes. Many researches show that high fault coverage for catastrophic faults can be achieved by oscillation-based test methodology. But obtaining high fault coverage for parameter faults is conditioned by considering other oscillation parameters along with oscillation frequency, such as amplitude, distortion, etc.

Chapter 3

Oscillation-based BIST of Mixed-Signal Integrated-Circuits

Increasing use of the mixed signal in applications in technology motivated intensive research in the mixed signal test area. Condensing a system on a very small area makes the design for testing a very challenging task, specially when the pin count, speed and testing time are very restricted. BIST is a very promising technique that IC industry applies in mixed signal IC testing recently. As we discussed in previous chapters, many BIST methods are proposed by now. One of the most recent DFT concepts is the application of the oscillation-based test strategy to the CUT in order to measure the performance of the circuits. Using oscillation BIST (OBIST), partitioned blocks of the circuit to be tested are configured as oscillator in the test mode. Oscillation parameters are measured to determine whether the blocks of the circuit are performing as expected.

We will discuss OBIST in this chapter by elaborating the oscillation-based test strategy, OBIST architecture and oscillation theory. Then we will explain the faults models used in the simulation and test procedure as well.

3.1 Oscillation-Based Test Strategy

Oscillation-based test strategy (OBT) has been proposed by Arabi et al. [48] which is defect-oriented technique and can be applied as either on-line or off-line testing. In oscillation test method, there is need to neither test stimuli generator nor test specification that is very costly. In applying OBT for a system, certain aspects must be considered such as: system partitioning, feedback type, necessary measurements, fault coverage, and etc. Procedure is such that a complex analog circuit is partitioned into functional building blocks such as: operational amplifier, comparator, filter, phase lock loop and etc. or combination of these blocks. Then each building block is converted to an oscillator by adding proper circuitry in order to achieve sustained

oscillation; then the oscillation parameters are evaluated. Faulty circuit is detected by deviation of its oscillation parameters with respect to the oscillation parameters under fault-free condition. In view of the fact that oscillation parameters are regardless of the type of the CUT, analog testing can hence be standardized. Figure 3.1 demonstrates the oscillation test strategy. Oscillation parameters can be frequency, amplitude, and distortion and DC level of output signal. Although this method provides high fault coverage by considering only the oscillation frequency, but there may be some faults that are not correlated with frequency and in such cases other test parameters are to be taken into account. For example, it is indicated in [49] that the fault coverage is improved by monitoring the supply current in addition to the oscillation frequency and the output voltage.

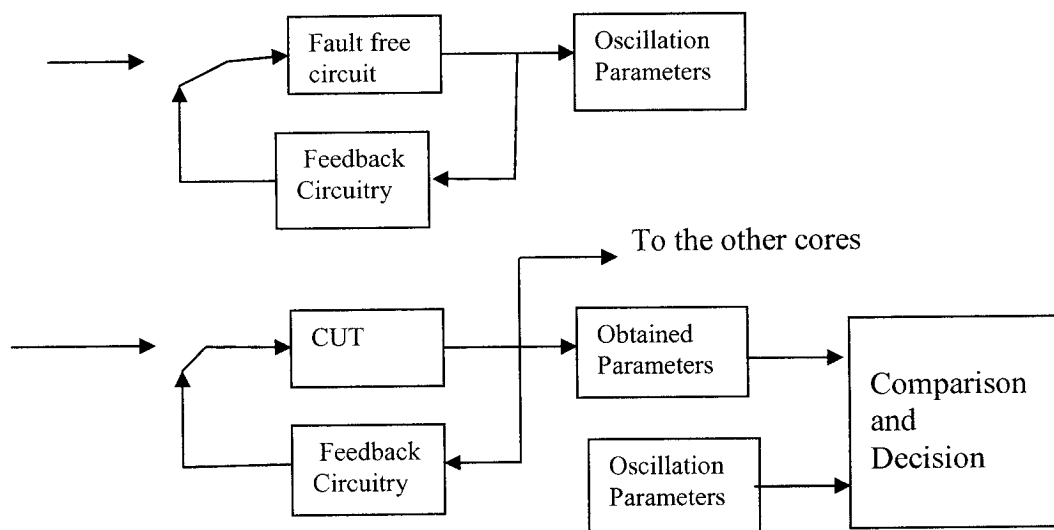


Figure 3.1. Oscillation test strategy.

Some methods are proposed in the literature to extract the oscillation parameters from the output test signals. Vazquez et al. [50] proposed a simple method to evaluate the output signal coming off the OBT technique application. In this method, $\Sigma\Delta$ modulator is connected to the output of the CUT to provide a train of modulated pulses that contain all the information about the output of the CUT. In order to extract oscillation parameters, the train of pulses is processed using ATE or on-chip DSP.

Oscillation-based test methodology has been applied for many circuits such as A/D converters, filters, etc. Furthermore, applicability of OBT methodology to a dual tone multi-frequency detector (DTMF) [51], analog microcell, switched capacitor circuits and CMOS micro-electro-mechanical systems has also been studied [50],[52]-[56].

3.2 OBIST Architecture

As complexity of a mixed signal ICs arises, the accessibility to the internal nodes decreases. Thus controllability and observability of the nodes are restricted from outside the ICs. To overcome these problems, many DFT methods were developed. Among them, BIST methods are very promising because it is a solution to the pin count problem that arises with shrinking a system on a chip as well as a complex mixed signal IC on a very small area. BIST technique will be an efficient method when the input stimuli and response analyzer are very accurate and BIST circuitry occupies very small area of the chip. As we studied different BIST methodologies in previous chapter, most of the BIST circuitry requires area overhead as well as accurate signal generator or algorithm for input stimulus. Since variety of parameters must be measured in order to analyze the response of the CUT, sometimes the response analysis is done off the chip. Nevertheless, oscillation-based BIST is introduced [47] to decrease the problems in relation to test input stimuli, response analyzer and finally area overhead.

In this method, the CUT is partitioned to some functional building blocks such as operational amplifier, filters, PLL, etc. The block diagram of OBIST is illustrated in Figure 3.2. The switches that isolate each block from the others are controlled by BIST control circuitry. An analog multiplexer is used to select the test point. A parameter extractor is used to extract the oscillation parameters of the block that is selected by analog multiplexer and then the extracted oscillation parameters are compared with the fault-free oscillation parameters, and eventually a pass or fail decision is made. Implementation of the OBIST may vary by trade-offs between the test time and area overhead. G. Huertas et al. [51] have studied three different approaches of OBIST implementation on biquad filters. The sw- OpAmp (switchable OpAmp) concept [57] is

used in their study. In the first approach, all the building blocks are transformed to oscillators simultaneously and every stage has a comparator. Although this approach reduces the test time, extra hardware is required for this approach. In the second approach, only one comparator is used such that each block is converted to an oscillator sequentially by using sw-OpAmp and analog multiplexer. In the third approach, sw-OpAmp is used to bypass signals from their inputs. Only one block is converted to an oscillator at a time. And the evaluation is done sequentially. The continuity of the blocks can be tested by the second and third approaches although more testing time is needed.

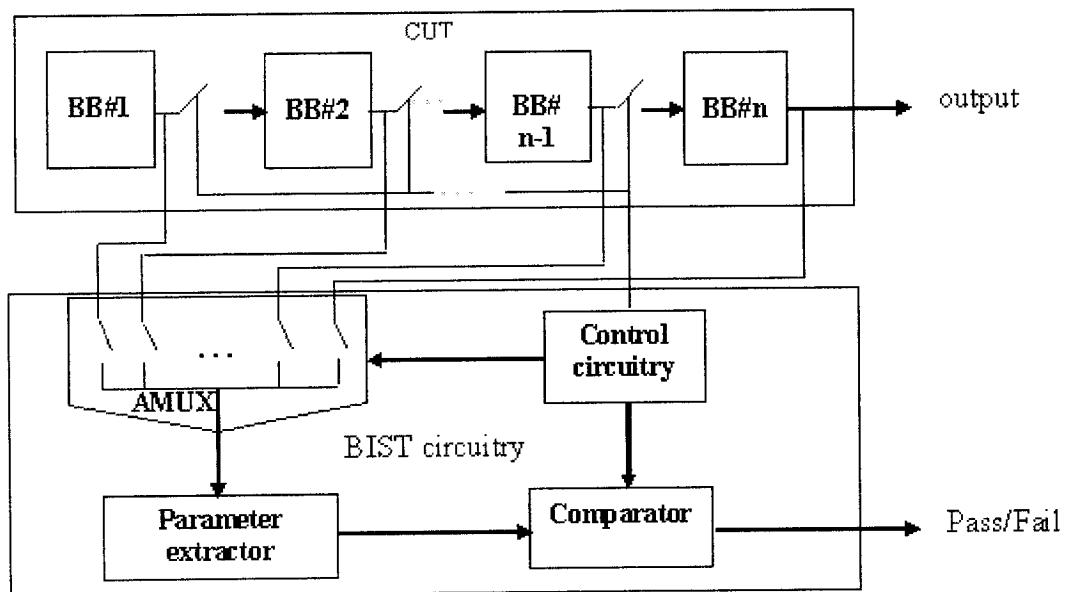


Figure 3.2 Oscillation-based BIST structure.

In the test mode, the CUT is partitioned into proper building blocks such that each of them is converted to an oscillator and then an analog multiplexer selects the test point. Oscillation parameters of the test point are extracted by an extractor, and then a comparator is used to compare the extracted parameters of the block with the oscillation parameters of the fault-free CUT. Arabi [47] discusses explicitly about the implementation of the parameter extractor that replaced the frequency to number converter, analog multiplexer and embedded switches and control logic circuitry. One of the crucial issues to be considered is how the output of the block is extracted and evaluated if we want to evaluate the oscillation parameters other than frequency. Measuring accurate oscillation frequency can be time consuming. Roh et al. [58] propose a BIST method using TDM (time division multiplexer) comparator. In this method, the CUT is converted to an oscillator and oscillation waveform is compared with two reference voltages; then results are stored in the counters by TDM. Accumulating the comparison result into the counters generates signature.

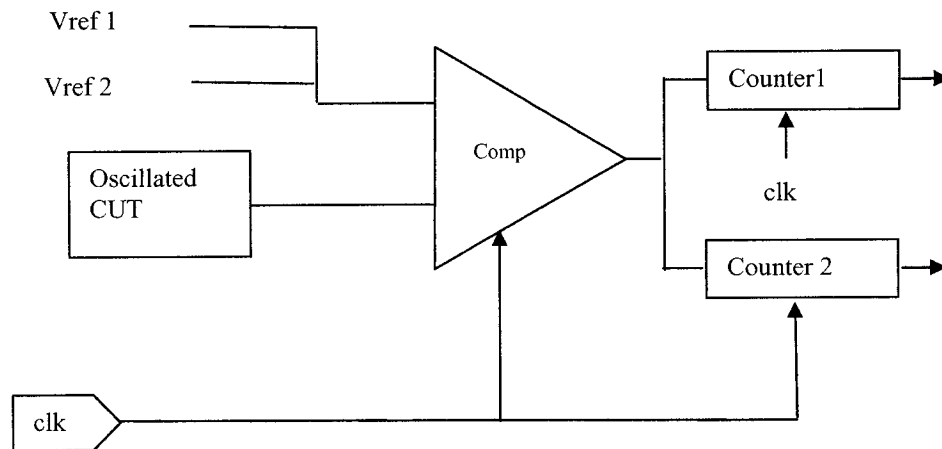


Figure 3.3 BIST scheme using TDM comparator.

Vazquez et al. [59] propose an on-chip parameter evaluation unit. The unit consists of a $\Sigma\Delta$ modulator that is used to obtain a digital encoding of the oscillation signal and a set of digital counters (frequency, amplitude, and DC counter) as shown in Figure 3.4. The counters extract the oscillation parameters by processing the train of modulated pulses.

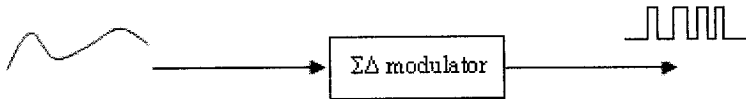


Figure 3.4 Functionality of $\Sigma\Delta$ modulator.

3.3 Oscillator Theory

An oscillator is an electronic device that generates an output without requiring any input signal. It is initiated by factors such as noise pickup or DC power supply. The output signal must be repetitious, usually of a fixed frequency and of a particular wave shape. The output wave shape may be sinusoidal, pulse, square wave, sawtooth, triangle, etc. The basic requirements for any oscillator are to encourage an amplified signal that produces self-sustaining oscillations. An oscillator operates based on feedback control system. The standard discussion of feed back theory is the one used in the study of fundamentals of an amplifier [74]. Figure 3.5 shows a block diagram of the feed back amplifier. The control loop consists of an input voltage differencing section whose output is amplified by a positive gain section. A fractional part of the signal output is then returned to the negative terminal of the differencing section though the feedback network. Then the difference in the signals at the (+) and (-) inputs amplified by the open-loop voltage gain of the amplifier: The equation that describes this feedback loop is given by:

$$A_{cl} = \frac{A}{1 - \beta A}$$

A_{cl} = voltage gain with feedback;

A = voltage gain without feedback (open-loop gain);

β = feed back factor.

This is the key equation in feedback system that indicates the close loop gain is dependent upon the open-loop gain, A , and the feedback factor, β . The product, βA , in the denominator is called the loop gain.

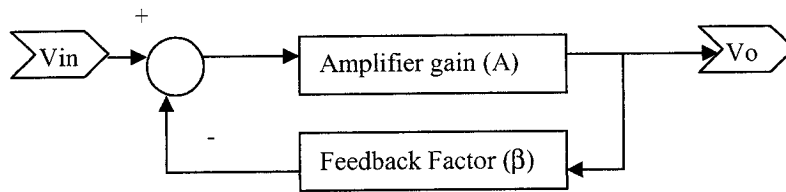


Figure 3.5 Block diagram of feed back amplifier.

When the β factor is positive, this amplifier may be able to function as an oscillator.

Barkhausen criterion for oscillation is the condition for feedback loop in order to provide frequency of oscillation ω_0 .

It specifies a feedback product of $A\beta$ equal to unity:

$$A(\omega_0) \beta(\omega_0) = 1,$$

where the phase of the loop gain should be zero and the magnitude of the loop gain should be unity.

$$|A(\omega_0) \beta(\omega_0)| = 1;$$

$$\arg (A(\omega_0) \beta(\omega_0)) = 0.$$

3.3.1 Building the Oscillator

The basic requirements for oscillation are a signal feedback from output to input of proper phase and sufficient amplitude. Some oscillators use RC elements for phasing. Some oscillators operate on the principle of presenting a negative resistance as the feedback element. The design equations of an oscillator are determined by analyzing the denominator of the transfer equation $T(s)$, of the circuit. The poles of the denominator of $T(s)$, or equivalently, the zeros of the characteristic equation s , determine the time domain behavior and stability of the system. An oscillator is on the borderline between a stable and an unstable system and is formed when a pair of poles is on the imaginary axis. The magnitude and phase equations of an oscillator also must be analyzed. If the magnitude of the loop-gain is greater than one and the phase is zero, the amplitude of oscillation will increase exponentially until a factor in the system, such as the supply

voltage, restricts the growth. In contrast, if the magnitude of the loop-gain is less than one, the amplitude of oscillation will exponentially decrease to zero.

Building general oscillators are different from building oscillator for testing purpose. In designing general oscillators, well-defined and stable oscillation frequency and amplitude are desired. In contrary, the oscillator that is built from the conversion of the CUT is designed such that the variation of the components is detected by measuring the oscillation frequency and amplitude. That means, there is no need of another circuitry (automatic gain controller) to stabilize the oscillation [58].

3.3.2 Filter to Oscillator Conversion

Converting a filter into an oscillator requires a mechanism to force a placement of a pair of poles on the $j\omega$ -axis. The general biquadratic transfer function is given by:

$$H(s) = \frac{Vo(s)}{Vi(s)} = \frac{a_2s^2 + a_1s + a_0}{s^2 + b_1s + b_0}$$

$$b_1 = \omega_0/Q, \quad b_0 = \omega_0^2$$

The relation between the pole and pole frequency and pole quality factor is given by:

$$p_1, p_2 = \sigma \pm j\omega = -\frac{\omega_0}{2Q} \pm j\omega_0\sqrt{1 - (1/4Q^2)}$$

where ω_0 is the pole frequency and Q is the pole quality factor that determines the distance of the poles from $j\omega$ axis; an infinite Q locates the poles on the $j\omega$ axis and this can cause the circuit to oscillate. Therefore in order for a filter to oscillate, the quality factor must be increased. Zarnik et al. [60] have presented the transformation of the active filters to oscillation mode.

A way to obtain a sinusoidal oscillator from the transfer function is to connect the output terminal of the filter to the input terminal [61]. By doing this we will have:

$$(s^2 + (\frac{b_1 - a_1}{1 - a_2})s + (\frac{b_0 - a_0}{1 - a_2}))Vo(s) = 0$$

Equating coefficient of s to zero satisfies oscillation condition.

In this work, we converted state-variable filter to the oscillator by connecting the band pass stage output to the input of the filter, and sustained oscillation is achieved.

3.4 Fault model

Fault models for analog circuits can be categorized in two groups: hard fault and soft fault [12]. Hard faults or catastrophic faults are the faults that cause the circuit performance to differ catastrophically from normal conditions. Local defect mechanism such as particles on surface of the wafer that are generated by equipment during processing causes the catastrophic faults in integrated circuits. Other examples for the local defect producer are misalignment of layers, oxide defects which cause short on transistors, particles which block exposure of a local area during masking which cause open on the circuit and so on. Catastrophic faults on the printed circuit boards are caused by excess solder, bridging, insufficient solder, misalign or tilted components, wrong components or missing components [62]. Catastrophic fault model is the same as stuck-at fault model in digital domain where every component can be stuck-open or stuck-short. Stuck-open is occurred when a terminal of a component is not connected to the rest of the circuit while stuck-short is occurred when a short is created between terminals of a component. On the other hand, soft faults or parametric faults refer to changes in a circuit that do not affect its connectivity and cause circuit functions out of specifications. Parametric fault can be modeled as variation of component parameter that is out of its tolerance limit.

In this work only catastrophic faults are considered. The catastrophic fault models include the short and open faults for a resistor or a capacitor, collector-base short, base-emitter short, base open, and emitter open faults for a BJT, and drain-gate short, gate-source short, and drain open faults for a MOSFET. These faults have been identified to be the most common defect mechanism for BiCMOS process. Each short fault is modeled as a 10Ω resistor in parallel with the two faulty nodes and each open fault is modeled as a $100M\Omega$ resistor in series with the faulty

node. Figure 3.6 depicts the fault model for resistor, capacitor and MOSFET where value for parallel resistor R_p is 10Ω , that emulates stuck-short and series resistor R_s has a value of $100M\Omega$ that emulates stuck-open.

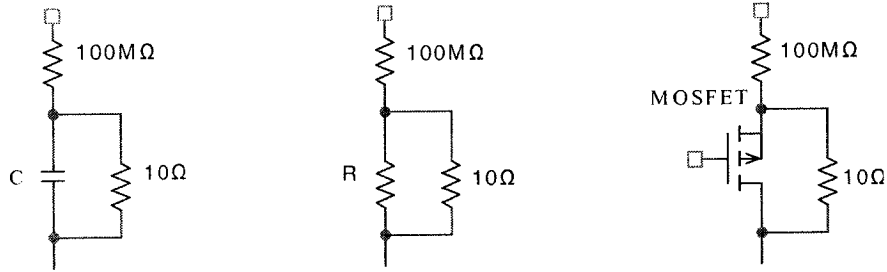


Figure 3.6 Stuck-open and stuck-short model for resistor, capacitor and MOSFET.

Above faults models are simulated in HSPICE for this work.

3.5 Test Procedure

For our purpose of analyzing OBIST method we consider an inverter circuit. In most integrated circuits, inverter is the basis for building other logic gates. It is important to have a decent analysis of an inverter in order to be able to do a proper synthesis of integrated circuits. We will investigate an inverter circuit in the following sections. For the purpose of our analysis we choose Hspice that has a complete set of built-in functions used for simulating a broad range of electrical circuits. Circuits are simulated, analyzed, and optimized in steady state, transient state and frequency domain from DC to frequencies greater than 100 GHz.

We consider catastrophic faults (short and open faults) here. We inject the opens and shorts faults at the circuit level. These faults are described in HSpice format that are injected into nominal circuit description. By using HSpice simulator, transient response is evaluated and thus frequency and output voltage are measured. Figures 3.7, Figure 3.8, and Figure 3.9 illustrate the test procedure proposed for OBIST method. In the following we briefly review the different steps of the procedure.

- Fault-free circuit that is converted to an oscillator is simulated and test parameters (oscillation frequency and amplitude of the output signal) are derived.
- Fault list is derived from the CUT (circuit netlist).
- Faulty netlist is generated (fault injection).
- Simulation is done for the faulty circuit.
- Oscillation parameters are obtained.
- Fault detection is completed by comparison of faulty output measurements with fault-free test parameters.
- Procedure continues until all faults are injected.
- Fault coverage is calculated.

This whole process is accomplished by the program written in C. For the sake of simplicity, we did not consider the tolerance of the components.

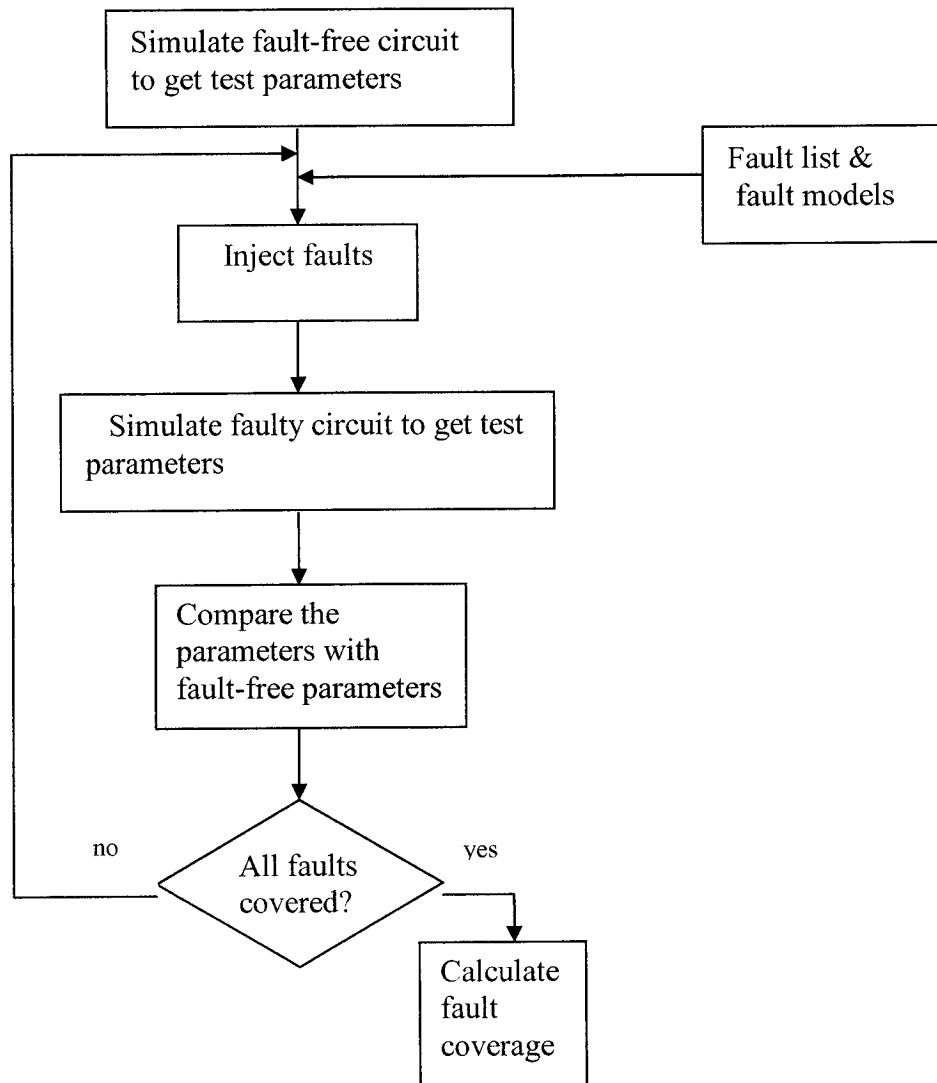


Figure 3.7 Test procedures for OBIST method.

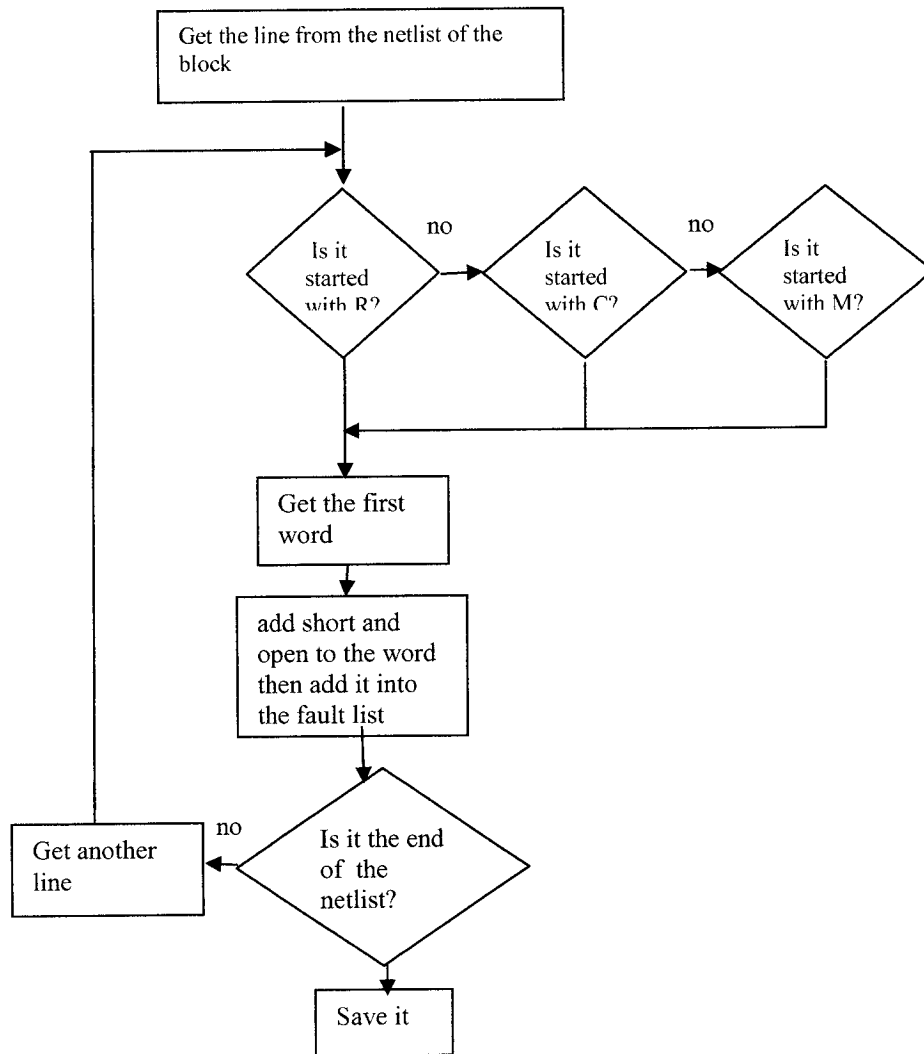


Figure 3.8 Catastrophic faults list maker flow chart diagram.

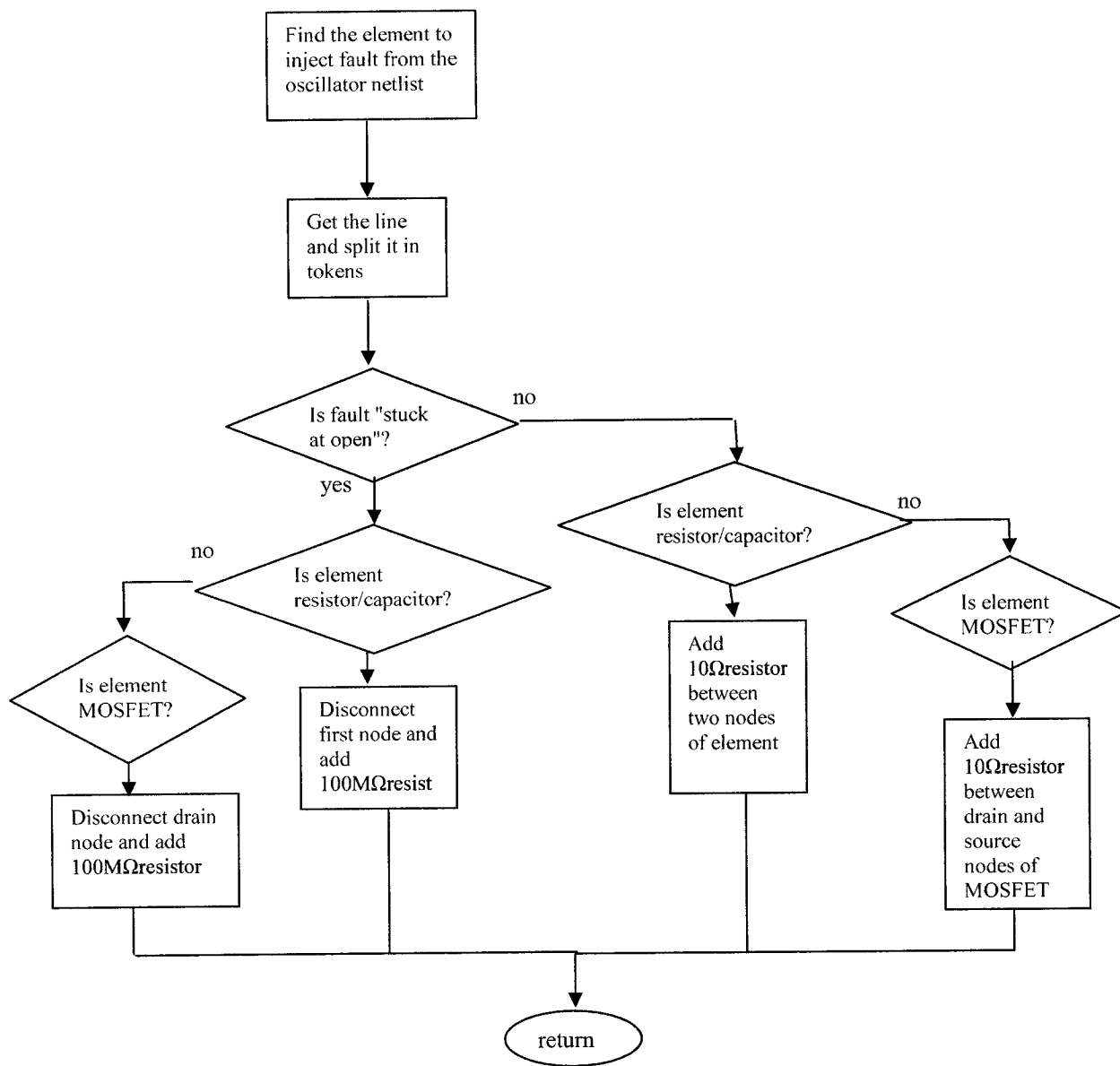


Figure 3.9 Fault injection flow chart diagram.

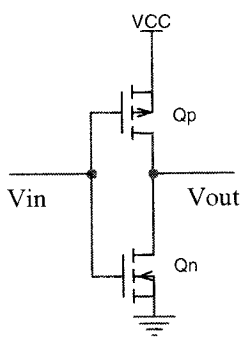
3.6 Example Inverter

This example is concerned with the test of a CMOS inverter by applying the oscillation-based test methodology. Before applying the test method, we wish to explain the CMOS inverter in detail. Complementary MOS is the most useful technologies of the integrated circuits among the MOS technologies, which comprises NMOS and PMOS. CMOS uses MOS transistors of both polarities. That is why designing many powerful analog and digital circuits become possible.

3.6.1 CMOS Inverter

Complementary transistors PMOS and NMOS form the CMOS inverter, with their gates connected together as input and their drains connected together as an output. To obtain the symmetric characteristic, it is necessary to make the PMOS device wider than NMOS device such that the threshold voltage becomes $V_{cc}/2$. To achieve the threshold voltage of $V_{cc}/2$, we choose the width of PMOS 2.5 times wider than that of the NMOS. The considered CMOS inverter and its characteristics in this example are illustrated in Figure 3.10.

a) Circuit.



b) Transfer characteristic.

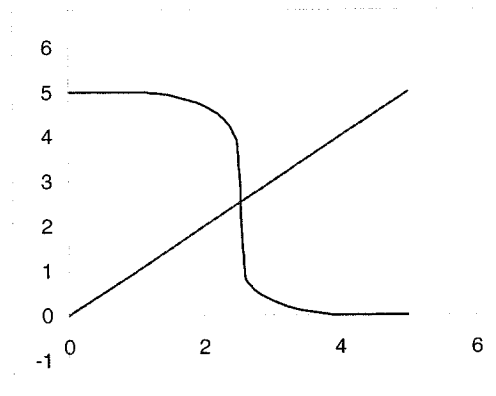


Figure 3.10 CMOS inverter.

As it can be seen from the transfer characteristic, the point of symmetry is when $V_{in} = V_{out} = V_{cc}/2$; that means, the changeover between logic levels is symmetrically done at this point. Therefore threshold voltage for transistors is $V_{th}=V_{cc}/2$.

3.6.2 Inverter Oscillator

We begin to test the inverter by applying oscillation-based test methodology. For this purpose, the circuit must be oscillating. In order to make the CMOS inverter oscillate, we employ classical CMOS Astable oscillator concept, as shown in Figure 3.11.

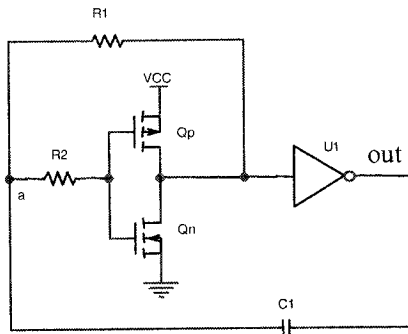


Figure 3.11 CMOS Astable oscillator

R_1 connects output of the CUT (CMOS inverter) to its input and thus acts as DC negative feedback. The output of the CUT is connected to the input of the inverter U_1 directly. The output of the U_1 is connected with a capacitor to the input of the CUT. This is the positive AC feedback.

3.6.3 Oscillation Frequency Calculation for Inverter

Let us assume that the input of the CUT is zero, then output of the U_1 is low and then there is no charge across the capacitor. Capacitor begins to charge through the resistor R_1 since

the input impedance of the CMOS chips is quite large. As soon as the capacitor voltage exceeds the threshold voltage of the CUT, V_{th} ($V_{th} = V_{cc}/2$), the output of the CUT will transit to zero. Thus the output of U1 becomes high. It is known that the voltage across the capacitor is continuous; therefore voltage difference between the two sides of the capacitor must remain $V_{cc}/2$. That means when one side of the capacitor jumps to V_{cc} from zero, the other side must jump to $3V_{cc}/2$. $3V_{cc}/2$ appears on common node of R1 and C1 where the other node of R1 is zero so that capacitor starts to discharge through R1. As soon as the voltage across R1 reaches the value V_{th} , the output of the CUT will transit to V_{cc} and therefore the output of U1 becomes zero. The voltage of common node of R1 and C1 is pulled to $-V_{cc}/2$. Thus the capacitor C1 starts to charge towards V_{cc} . This cycle continues to give us our square wave output. Frequency of oscillation can be determined as the follows:

During the time interval t_1 when the output is low, v_c (voltage across the capacitor C1) rises from $-V_{cc}/2$ to V_{th} . The exponential rise of v_c can be described by:

$$v_c = V_{cc} - (V_{cc} - (-V_{cc}/2))e^{-t_1/R_1C_1} \quad (3.1)$$

Substituting $v_c = V_{th} = V_{cc}/2$ at $t = t_1$ results in

$$t_1 = R_1C_1 \ln 3 \quad (3.2)$$

Also during the time interval t_2 when the output is high, v_c falls from $3V_{cc}/2$ to V_{th} . The exponential fall of v_c can be described by :

$$v_c = 3V_{cc}/2 e^{-t_2/R_1C_1} \quad (3.3)$$

Substituting $v_c = V_{th} = V_{cc}/2$ at $t = t_2$ results in

$$t_2 = R_1C_1 \ln 3 \quad (3.4)$$

Period of the output T can be achieved by summing t_1 and t_2 as

$$T = t_1 + t_2 \quad (3.5)$$

$$T = 2 R_1C_1 \ln 3 = 2.2 R_1C_1 \quad (3.6)$$

Frequency of oscillation will be:

$$f_{osc} = 1/2.2 R_1C_1 \quad (3.7)$$

By substituting the following value of parameters in Eq.(3.7):

$R1=500k$,

$C1=10n$,

$R2=5M$,

Results in:

$f_{osc}= 90.9Hz$.

We obtained the oscillation frequency of the simulated circuit in HSPICE as follows:

$f_{osc}= 86.95Hz$.

The output signals are illustrated in Figure.3.16.

In this example, only catastrophic faults are considered. Figure 3.12 depicts the fault model for MOS transistors where value for the parallel resistor R_p is 10Ω that emulates stuck-short and the series resistor R_s has a value of $100M\Omega$ that emulates stuck-open.

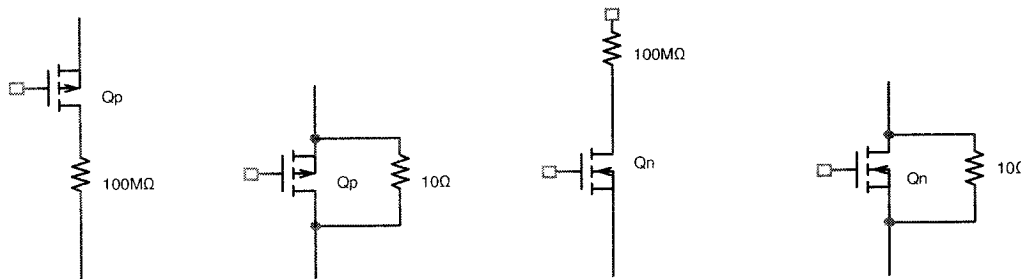


Figure 3.12 The considered fault models for NMOS and PMOS transistors of inverter.

Let us we consider that the Q_p is stuck open, as shown in Figure 3.13. Assume that the input of UI is +5v so its output will be zero. The capacitor $C1$ will start to charge through $R1$ until the gate voltage of Q_n becomes more than the V_t (the threshold voltage of Q_n) or $V_{gs} \geq V_t$. Therefore Q_n will operate and V_{ds} of Q_n will be zero from $V_{ds} = V_{gs} - V_t$. The

output of U1 will turn to high (+5V) and stay high since the drain of Qp which is disconnected has no influence on the output of Qn .

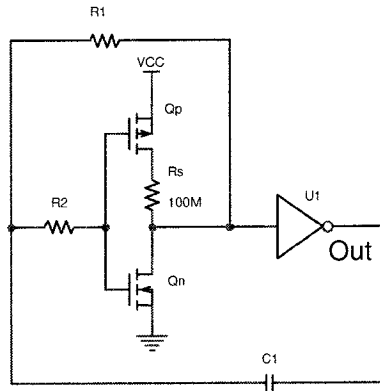


Figure 3.13 The Oscillator with the stuck-open Qp.

The same result is obtained with the HSpice simulation as shown in Figure 3.16(b).

Now let us we consider that the Qp is stuck short, as shown at Figure 3.14. Since the input of U1 is shorted to Vcc, the output always will be zero.

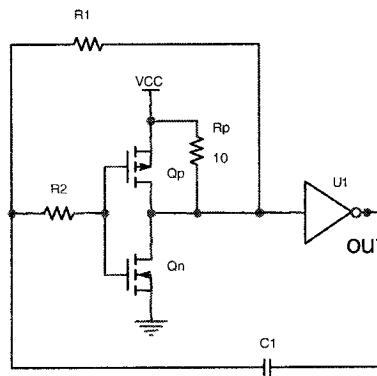


Figure 3.14 The Oscillator with the stuck-short Qp.

The same result is obtained with the HSpice simulation as shown in Figure 3.16 (d).

To inject every fault, first we find the Qp or Qn through the netlist file of the oscillator; then connect Rp or Rs as required for the faults.

General syntax for a MOSFET element in an HSPICE netlist is:

```
Mxxx nd ng ns <nb> mname <<L =>length> <<W =>width> ...
```

and for a Resistor is:

```
Rxxx n1 n2 <mname> <R =>resistance ...
```

For instance, to inject a stuck-open fault to Qp that is defined in the netlist as:

```
m1 inm in vccm vccm p w=45u l=5u,
```

first the netlist file of the oscillator is read and "m1" is found from the file and then Rs is added as follows:

```
m1 ccm in vccm vccm p w=45u l=5u.
```

```
Rs inm ccm 100e+6.
```

After these changes are done, the faulty circuit is simulated and the output signal is observed and the frequency of oscillation is measured. All the faults are injected and the output signal of each fault is illustrated in Figure 3.16.

In conclusion, the inverter of astable stops oscillating by injecting any of four considered faults to the circuit in Figure 3.11. If one of the transistors in the inverter circuitry becomes short or open, the output will remain either high or low according to the injected fault. Consequently, the simulation results agree with the theory.

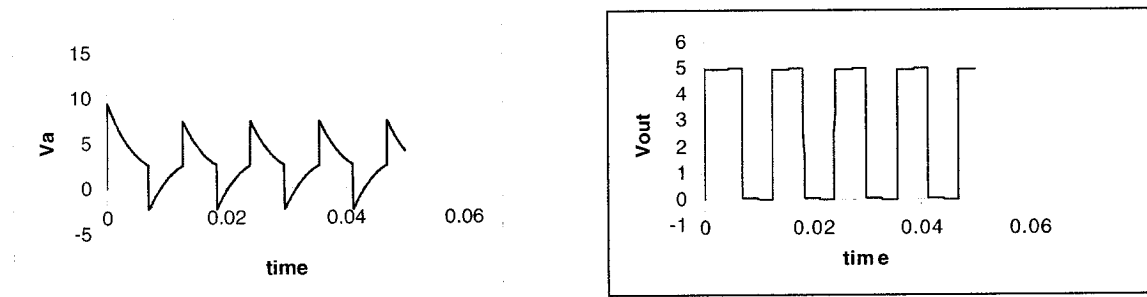
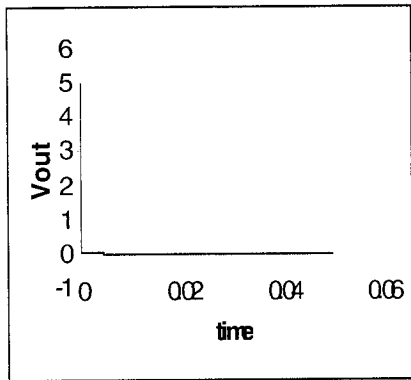
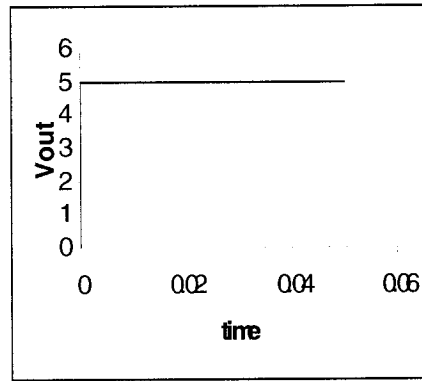


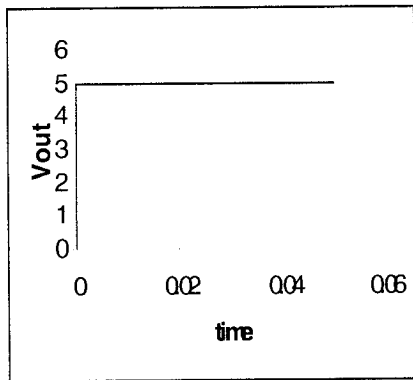
Figure 3.15 Outputs of CMOS Astable.



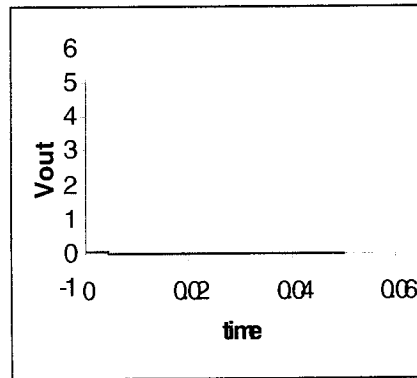
a) The output of Astable when Q_n is stuck open.



b) Output of Astable when Q_p is stuck open.



c) The output of astable when Q_n is stuck short.



d) The output of astable when Q_p is stuck short.

Figure 3.16 The output of astable when fault is injected.

Chapter 4

Simulation Experiments

4.1 Selections of the CUT

Filters and operational amplifiers are widely used in analog and mixed signal circuits. Efficient way to test the OpAmps and filters are desired because of their importance in analog systems. In this section, simulation results are shown for the single OpAmps, the continuous time state-variable filter, and voltage control voltage source circuits. In order to test any circuit with oscillation-based method, first the circuit under test must be converted to an oscillator by adding extra circuitry as a feedback. If the circuit is faulty, the converted circuit either will not oscillate or the oscillation frequency and voltage will differ from fault-free conditions.

4.1.1 CMOS OpAmp

Figure 4.1 shows the operational amplifier from Analog and Mixed Signal Benchmark Circuits- First Release [1]. The OpAmp is a two-stage compensated CMOS operational amplifier that has been designed using Mitel semiconductor 1.2 μm CMOS technology parameters.

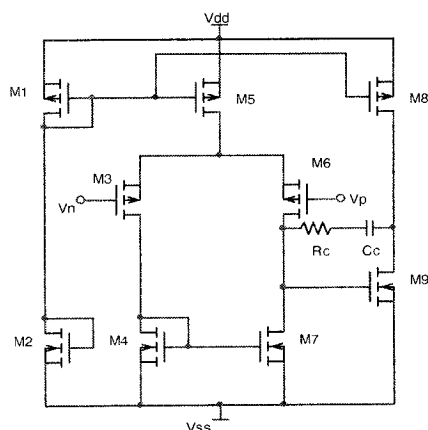


Figure 4.1 Compensated operational amplifier.

As shown in Figure 4.2, the OpAmp is converted to an oscillator by adding both negative and positive feedbacks in the test mode. However, OpAmp is changed to a second order system that has potential for oscillation.

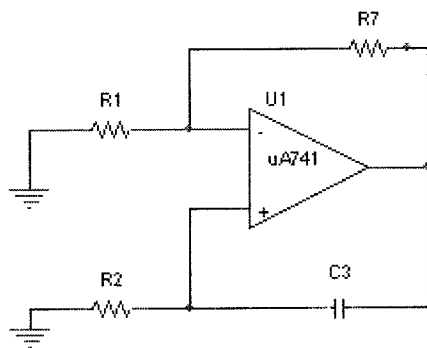


Figure 4.2 Single OpAmp oscillator.

The transfer function of Figure 4.1 is characterized by a single pole for an OpAmp:

$$K(s) = \frac{K_0}{1 + \frac{s}{\omega_p}} \quad ; \quad (4.1)$$

Where ω_p is the pole frequency.

$$\text{Since } \frac{s}{\omega_p} \gg 1 \text{ , } K(s) = \frac{K_0 \omega_p}{s} = \frac{GB}{s} \text{ ,} \quad (4.2)$$

where GB being the unity-gain bandwidth.

The open loop transfer function of the above circuit (Fig. 4.2) is:

$$A(s) = \frac{R1 + R7}{R1 + \frac{R1 + R7}{K(s)}} = \frac{R1 + R7}{R1 + \frac{R1 + R7}{\frac{GB}{s}}} = \frac{R1 + R7}{R1 + \frac{s(R1 + R7)}{GB}} \quad (4.3)$$

In the above, $K(s)$ is the amplifier gain. $K(s) \rightarrow \infty$ if amplifier is ideal so that $A = \frac{R7}{R1} + 1$.

The feedback factor β of the RC feedback network is given by:

$$\beta(s) = \frac{R2}{R2 + \frac{1}{sC3}} = \frac{sR2C3}{sR2C3 + 1} \quad (4.4)$$

The loop gain is:

$$A\beta = \left(\frac{R1 + R7}{R1 + \frac{s(R1 + R7)}{GB}} \right) \left(\frac{sR2C3}{sR2C3 + 1} \right) \quad (4.5)$$

This can be written as:

$$A\beta = \left(\frac{GB(R1 + R7)R2C3s}{[GBR1 + s(R1 + R7)](sR2C3 + 1)} \right) = \frac{GBR2C3(R1 + R7)s}{s^2(R1 + R7)R2C3 + s(R1 + R7 + R2C3R1GB) + GBR1}$$

The characteristic equation of the circuit is:

$$1 - L(s) = 0,$$

or

$$1 - A(s)\beta(s) = 0 \quad (4.6)$$

According to Barkhausen's criterion, the circuit will produce sinusoidal oscillations at frequency

$$\omega_0 \text{ if } A(j\omega_0)\beta(j\omega_0) = 1 \quad (4.7)$$

In order to make $A(j\omega_0)\beta(j\omega_0) = 1$ at $\omega = \omega_0$, the characteristic Equation (4.6) must have a

factor of the form $s^2 + \omega_0^2$.

Thus two limit cycle equations will be:

$$1) R_2 C_3 R_1 G_B + R_1 + R_7 - G_B (R_1 + R_7) R_2 C_3 = 0$$

$$\Rightarrow R_1 R_2 C_3 G_B + R_1 - G_B R_1 R_2 C_3 = R_7 (G_B R_2 C_3 - 1)$$

$$\Rightarrow \frac{R_1}{R_7} + 1 = G_B R_2 C_3 \quad (4.8)$$

and

$$2) \omega_0^2 = \frac{G_B R_1}{(R_1 + R_7) R_2 C_3} \quad (4.9)$$

By considering the following values, we simulate the circuit in Figure (4.2).

$$R_1 = R_2 = 10 \text{ k}\Omega,$$

$$R_7 = 20 \text{ k}\Omega,$$

$$C_3 = 10 \text{ pF}.$$

4.1.2 State-Variable Filter

The second circuit considered for the study is a continuous state-variable filter from Analog and Mixed-Signal Benchmark Circuits. Figure 4.3 shows state-variable filter circuit that is also known as KHN biquad used in this experiment. This filter is popular because of its improved stability and ease of implementation. The availability of the filtering functions like high pass, low pass and band pass from the same circuit is a good property of this filter. To make the circuit oscillate, we consider its band pass functionality.

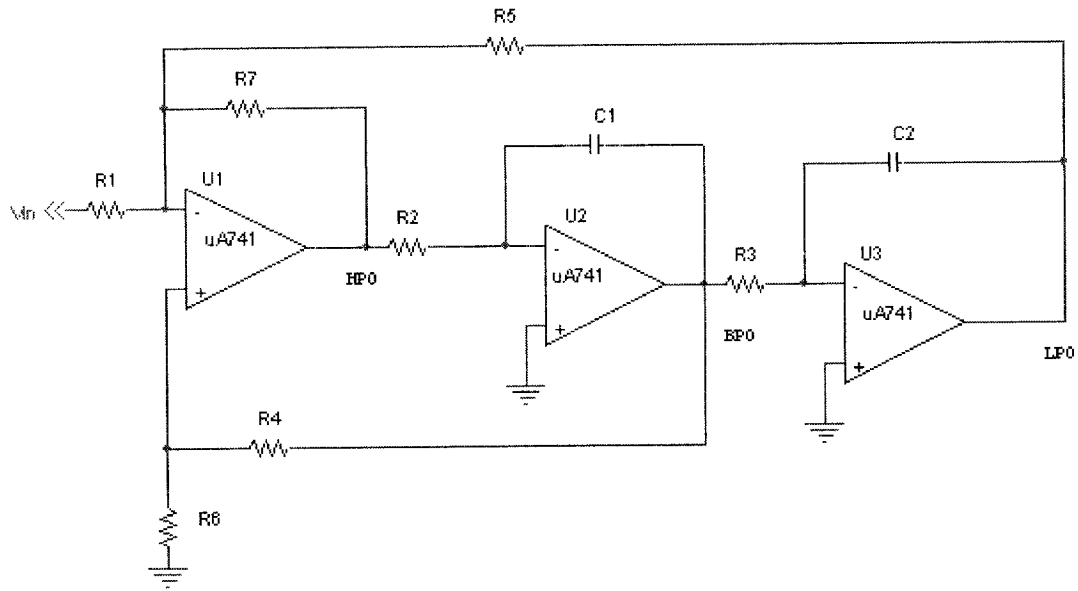


Figure 4.3 State-Variable filter.

Transfer function of the above circuit when it functions as a band pass filter is:

$$\frac{V_{BPO}}{V_{in}} = \frac{\frac{R7}{R1R2C1} s}{s^2 + \frac{(R1 + R5)R6R7}{R5R1R2(R4 + R6)C1} s + \frac{R7}{R2R3R5C1C2}}$$

with

$$\omega_0^2 = \frac{R7}{R2R3R5C1C2}$$

By considering the following component values, the frequency of pole will be $\omega_0 = 795\text{Hz}$.

$$R1=R2=R3=R5=R7=10\text{k}\Omega,$$

$$R4=7\text{k}, R6=3\text{k}\Omega,$$

$$C1=C2=20\text{nF}.$$

We convert the circuit in Figure 4.3 to an oscillator and simulate it. The nominal oscillation waveform is illustrated in the simulation result sub-chapter 4.2. We obtain the oscillation frequency and voltage level in fault-free condition as follows:

$$f_{osc} = 7.8966E+02\text{Hz}, V_{out} = \langle -4.5476E+00, 4.2384E+00 \rangle.$$

4.1.3 Voltage Controlled Voltage Source Filter

Now, we apply oscillation-based method to the voltage controlled voltage source (VCVS) filter. VCVS filters are a variation of the Sallen and Key circuits. The unity gain follower of the Sallen and Key filter is replaced with a non-inverting amplifier of gain greater than one. The VCVS exists in various circuit realizations such as high pass, low pass, band pass filters. In this experiment, we consider band pass VCVS filter as shown in Figure 4.4.

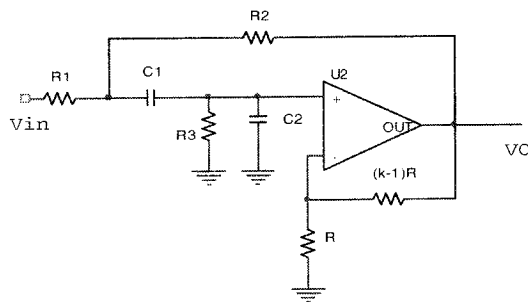


Figure 4.4 Voltage controlled voltage source filter- band pass filter.

The center frequency for the VCVS band pass filter is expressed by :

$$\omega_0 = \sqrt{\frac{R_1 + R_2}{R_1 R_2 R_3 C_1 C_2}}$$

For the parameters with the following values, the center frequency will be $f_0 = 562.69\text{Hz}$.

$$R_1 = R_2 = R_3 = 20\text{K}\Omega,$$

$$C_1 = C_2 = 20\text{nF},$$

$$K \leq 2.5.$$

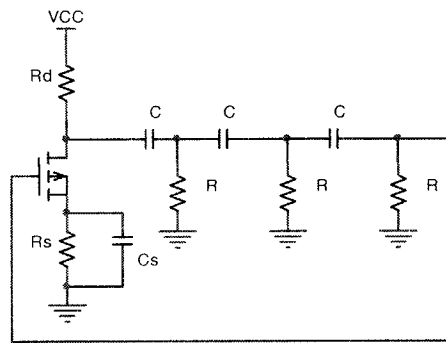
For the filter to oscillate, we have to increase K , the gain, after connecting the output of the filter to its input. Thus, we increase K slightly such that the poles are pushed to $j\omega$ axis. The above circuit will oscillate with $k=2.500855$. Waveforms are illustrated in the simulation result subchapter 4.2.

4.1.4 FET

In the following, we will demonstrate how to test a transistor based on oscillation test methodology. In order to test a transistor, we make an oscillator circuit with the transistor under test. In this experiment we made a phase shift oscillator circuit. By a number of phase shift circuits we will gain enough phase shift in order to force the circuit into oscillation. The FET provides the negative gain amplifier with 180 degrees phase shift and each RC pair results in 60 degrees phase shift. Each RC section loses one third of the signal level and therefore the minimum gain required for the active element in order to compensate for this loss will be 27. Figure 4.5 shows the phase shift oscillator. The frequency of oscillation is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{6}RC}$$

here



$R=10\text{k}\Omega$,
 $C=6.5\text{ nf}$,
 $R_d=10\text{k}\Omega$,
 $R_s=3\text{k}\Omega$.

Figure 4.5 Phase shift oscillator.

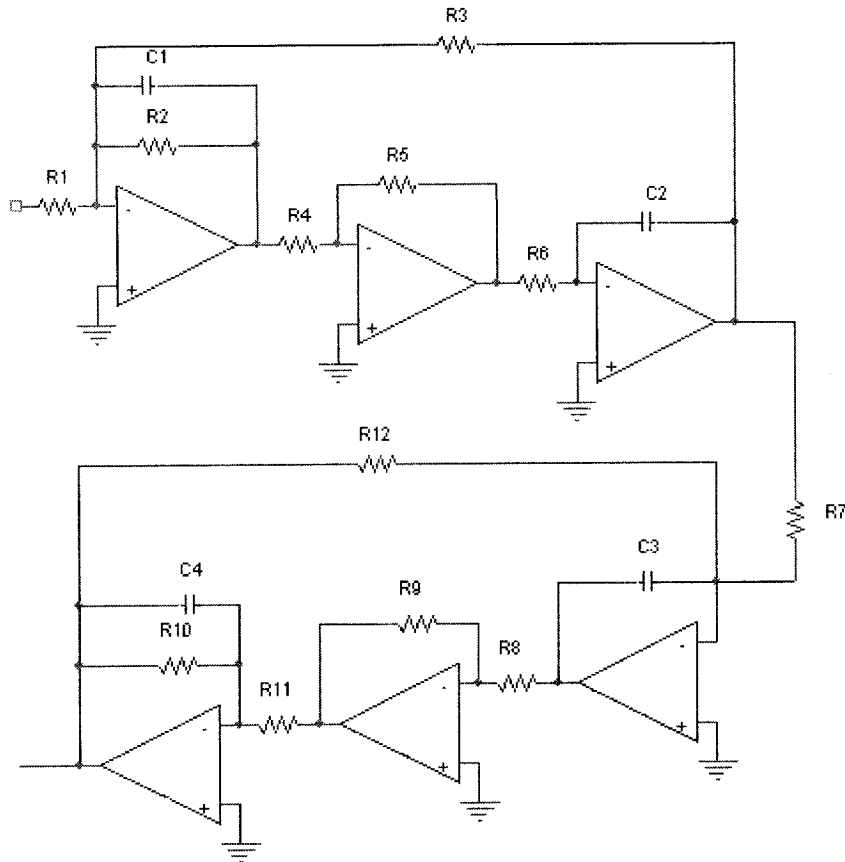
Using the above formula we will find the oscillation frequency which is:

$$F_{\text{osc}} = 999.6\text{Hz}.$$

The circuit stops oscillation by injecting the faults into the FET. The output of the circuit during oscillation and injected faults for FET are illustrated in the simulation result sub-chapter 4.2.

4.1.5 Leapfrog Filter:

Another circuit used for testing is a leapfrog filter from Analog and Mixed Signal Benchmark Circuits. In order to generate oscillations for this circuit, we connect the output to the input through an inverter amplifier.



Here $R_i = 10\text{k}\Omega$ for $i=1-12$, $C_1=C_4= .01\mu\text{f}$, $C_2=C_3= .02\mu\text{f}$

Figure 4.6 Leapfrog filter.

The circuit will oscillate at the blow frequency:

$$f_{osc} = \frac{1}{2\pi R \sqrt{C_1 C_2}}$$

The frequency of oscillation in the fault-free oscillator that is obtained by HSPICE is:

$$F_{osc} = 1.174 \text{ kHz.}$$

4.1.6 Notch Filter:

The last circuit we used for testing is a Notch filter. Figure 4.7 shows the Notch filter.

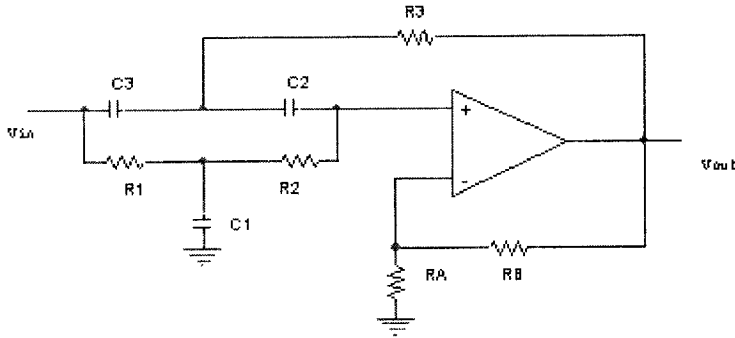


Figure 4.7 Notch filter.

Its transfer function is given by:

$$\frac{V_{out}}{V_{in}} = K \frac{s^2 + \frac{C_1 + C_3}{R_1 R_2 C_1 C_2 C_3}}{s^2 + \left[\frac{1}{R_3 C_3} (1 - K) + \frac{C_2 + C_3}{R_2 C_2 C_3} \right] s + \frac{C_2 + C_3}{R_1 R_2 C_1 C_2 C_3}}$$

By choosing appropriate value of K, the poles are pulled to $j\omega$ axis of s-plane. Therefore, the circuit will oscillate at the frequency:

$$f_{osc} = \frac{1}{2\pi} \sqrt{\frac{C_2 + C_3}{R_2 C_2 C_3}}$$

4.2 Simulation Results

Figure 4.8 illustrates the nominal case oscillation waveform of the OpAmp as a CUT .

In fault-free situation the oscillation frequency and output voltage levels are:

$$f_{osc} = 1.9598 \text{ MHz}; V_{out} = \langle -4.6676, 4.8642 \rangle.$$

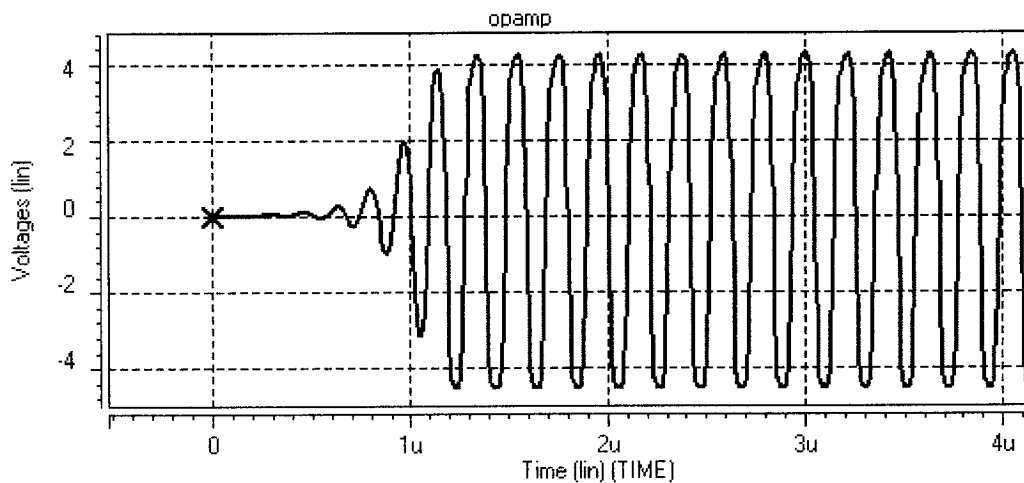


Figure 4.8 Output voltage in single OpAmp oscillator.

For these simulations, we use catastrophic faults. The fault is injected and the frequency and amplitude for every fault were measured and then the fault coverage calculated.

The simulation results in table 4.1 show the oscillation frequency and amplitude measurement for every individual fault. As we can see from these results, the output frequency significantly deviates with any injected fault. Only the short at compensator resistor (R_c) causes the oscillation frequency and amplitude to be very close to nominal ones. The other faults cause significant variation in both output frequency and amplitude of the CUT.

Table 4.1 Opamp faults.

Fault	Output Voltage Level (V)	Output Oscillation Frequency
Rc ,Cc open	< -4.6631E+00 , 4.8537E+00 >	2.3407E+06
Rc short	< -4.6675E+00 , 4.8649E+00 >	1.9609E+06
M2 open	< -2.2027E-04 , 8.4368E-02 >	5.0216E+06
M2 short	< -2.0471E+00 , 4.9197E+00 >	2.4402E+06
M1 open	< -1.9502E+00 , 4.9159E+00 >	2.2839E+06
M1 short	< -3.0465E-02 , 3.0439E-02 >	4.9732E+06
M5 short	< -4.7005E+00 , 4.8290E+00 >	2.3264E+06
Other Faults	No Oscillation	

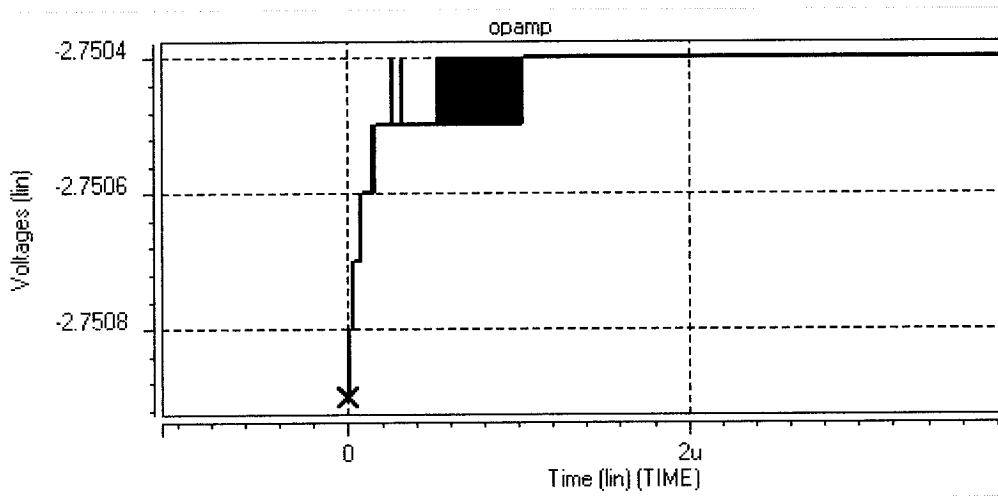
Table 4.1-a. Fault detectability of any element in the operational amplifier.

	open	short
Rc	1	1
Cc	1	1
M1	1	1
M2	1	1
M3	1	1
M4	1	1
M5	1	1
M6	1	1
M7	1	1
M8	1	1
M9	1	1

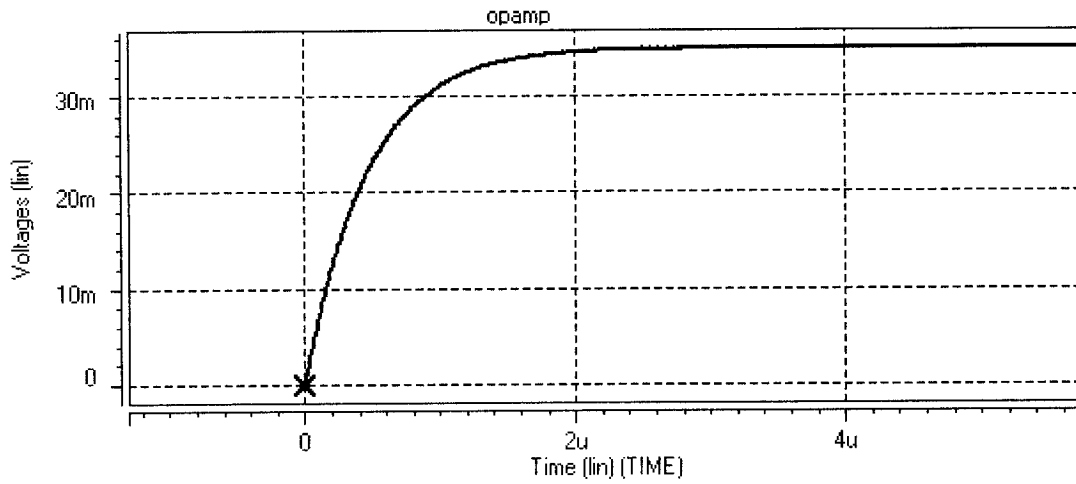
1: detected

Therefore by considering both frequency and voltage measurements, high fault coverage is obtained. The obtained fault coverage for this experiment is 100%.

Figure 4.9 illustrates the outputs of the faulty OpAmp oscillator.



a)



b)

Figure 4.9 Single OpAmp oscillator output for the typical injected faults.

The nominal oscillation waveform for state variable filter oscillator is illustrated in Figure 4.10.

We obtain the oscillation frequency and voltage level in fault-free condition as follows:

$$f_{osc} = 7.8966E+02 \text{ Hz}, V_{out} = \langle -4.5476E+00, 4.2384E+00 \rangle$$

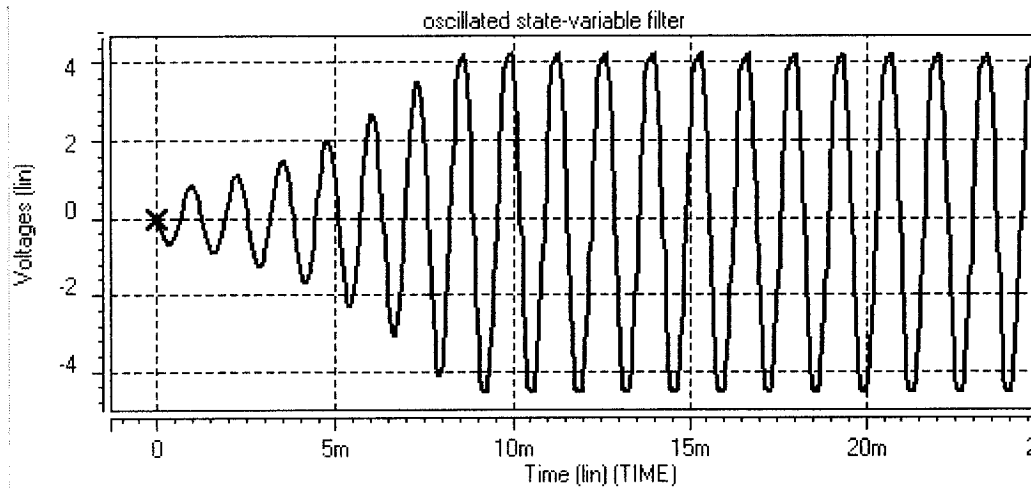


Figure 4.10 Output signal in state variable filter oscillator.

Table 4.2 gives the injected faults along with output frequency and voltage. Just as we observe from the results, the oscillation frequency deviates significantly for every fault. Even by measuring only the frequency, we can detect all the catastrophic faults in this filter.

Table 4.2 State variable filter faults

Fault	Output Voltage	Output Oscillation
	Level (V)	Frequency
R1 open	< -7.7595E-02 , 3.8166E-02 >	7.4398E+02
R2 open	< -4.6736E+00 , 4.6182E+00 >	6.8491E+02
R3 short	< -4.6109E+00 , 4.3127E+00 >	3.1290E+03
R4 short	< -1.8609E-02 , 1.7040E-02 >	8.0958E+03
R5 short	< -5.8972E-01 , 3.2922E-01 >	9.9331E+03
R6 open	< -3.3209E-01 , 5.8148E-02 >	9.8912E+03
R6 short	< -4.5420E+00 , 4.1179E+00 >	3.1457E+02
R7 open	< -4.6559E+00 , 4.6587E+00 >	2.0602E+02
C1 open	< -4.5865E+00 , 4.1690E+00 >	1.5217E+04
C1 short	< -4.1846E-04 , 1.0502E-06 >	9.9968E+03
C2 open	< -5.2414E-04 , 4.2881E-04 >	9.9792E+03
Other faults	No Oscillation	

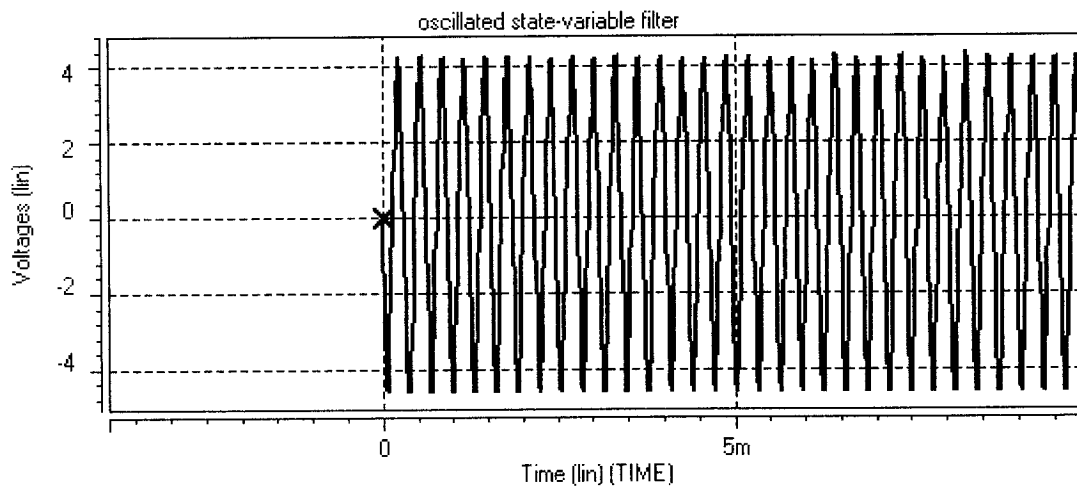
Table 4.2 -a. Fault detectability of any element in the state-variable filter

	open	short
R1	1	1
R2	1	1
R3	1	1
R4	1	1
R5	1	1
R6	1	1
R7	1	1
C1	1	1
C2	1	1

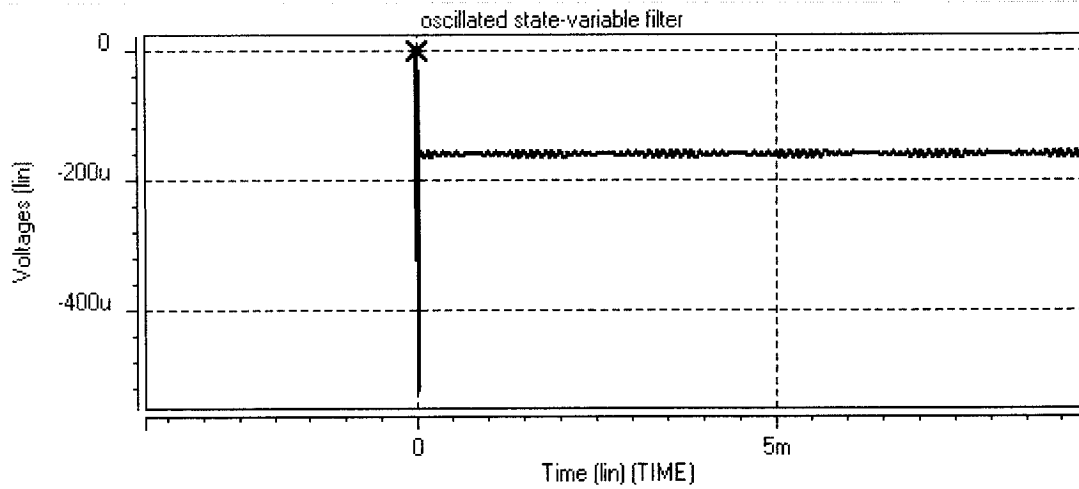
1: detected

The obtained fault coverage is 100 %

Figure 4.11 shows the oscillator while the typical faults are injected.



a)



b)

Figure 4.11 Output signals of state variable filter for a typical injected faults.

The oscillation frequency obtained by simulation for VCVS filter as a CUT is : 560.99 Hz and range of amplitude is :

$\langle -1.1843E-03, 2.1159E-03 \rangle$

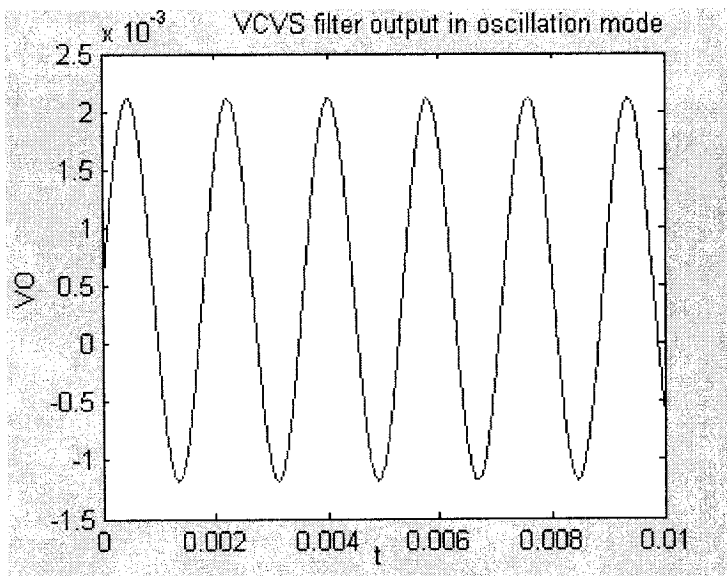


Figure 4.14 Output of VCVS band pass filter in the oscillation mode.

Figure 4.13 illustrates the output of VCVS filter in the test mode with injected "R2 open" fault.

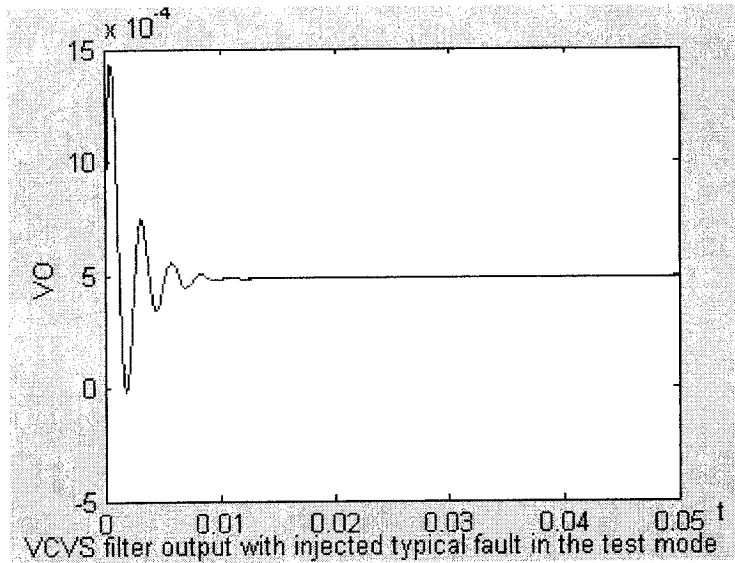


Figure 4.13 Output of VCVS bandpass filter with injected typical fault in the test mode.

Table 4.3 shows the injected faults to the VCVS filter along with output frequency and voltage.

Table 4.3 VCVS filter faults

Fault	Output Voltage	Output Oscillation
	Level (V)	Frequency
R1 short	< -5.2753E+00 , 4.9536E+00 >	1.4476E+03
R2 short	< -5.2753E+00 , 4.9536E+00 >	1.4476E+03
C2 open	< -4.6429E+00 , 4.8767E+00 >	9.8437E+02
Other faults	No oscillation	

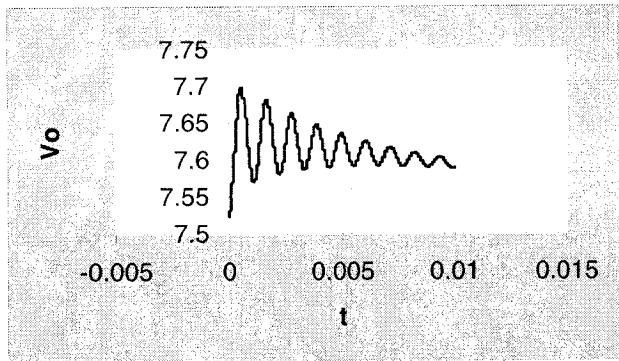
Table 4.3-a. Fault detectability of any element of the VCVS filter

	open	short
R1	1	1
R2	1	1
R3	1	1
R	1	1
C1	1	1
C2	1	1

1: detected

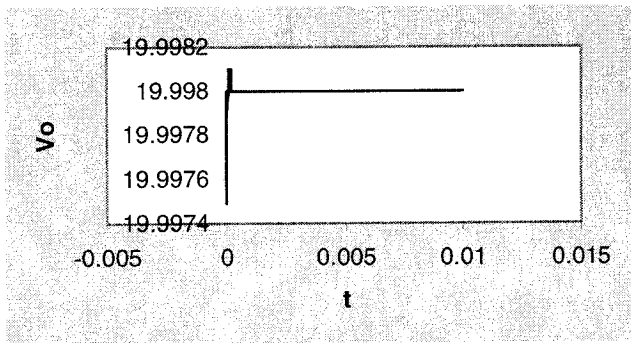
The obtained fault coverage is 100 %.

The waveforms obtained by simulation of FET as a CUT are shown:



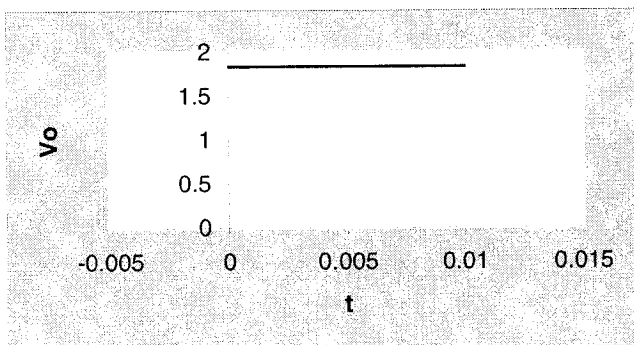
a)

When FET is open means it is disconnected from the circuit. The circuit does not oscillate.



b)

By injecting short faults in the circuit, the FET operates in cutoff region, as can be seen from the following graph.



(c)

Figure 4.14 Output signals of the FET as a CUT in test mode.

Figure 4.15 illustrates the output of leapfrog filter in oscillation mode.

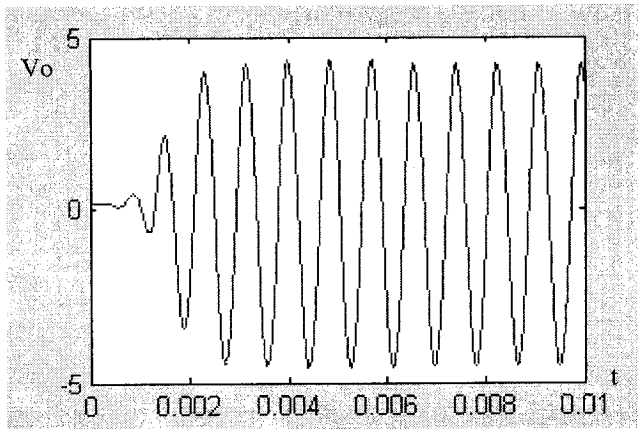


Figure 4.15 Output of the leapfrog filter during oscillation mode.

Table 4.4 depicts the simulation result for testing leapfrog filter.

Table 4.4 Simulation result for testing leap frog filter

Inserted Fault	Output Voltage	Output Oscillation
	Level (V)	Frequency
R2 open	< -6.8844E+00 , 6.6512E+00 >	9.5640E+02
R3 open	< -6.5409E+00 , 6.1659E+00 >	9.9136E+02
R4 short	< -7.1448E+00 , 5.8759E+00 >	9.7568E+02
R5 open	< -5.9213E+00 , 5.3756E+00 >	1.1669E+03
R7 short	< -4.3850E+00 , 4.4082E+00 >	3.1651E+03
R8 short	< -1.4850E+00 , 1.5946E+00 >	4.1432E+03
R9 open	< -5.2000E-01 , 7.9886E-01 >	6.0393E+03
R10 open	< -1.2983E+01 , 1.1136E+01 >	1.1062E+03
R11 short	< -1.2033E+00 , 1.1957E+00 >	3.8369E+03
R12 open	< -8.4403E+00 , 7.9554E+00 >	7.8056E+02
R13 open	< -5.4342E+00 , 5.5190E+00 >	1.0045E+03
C1 open	< -2.3735E+00 , 2.3349E+00 >	1.5133E+03
C4 open	< -1.8255E+00 , 1.9589E+00 >	1.6537E+03
Other faults	No oscillation	

Table 4.4-a. Fault detectability of any element in the leapfrog filter

	open	short
R1	1	1
R2	1	1
R3	1	1
R4	1	1
R5	1	1
R6	1	1
R7	1	1
R8	1	1
R9	1	1
R10	1	1
R11	1	1
R12	1	1
C1	1	1
C2	1	1
C3	1	1
C4	1	1

1: detected

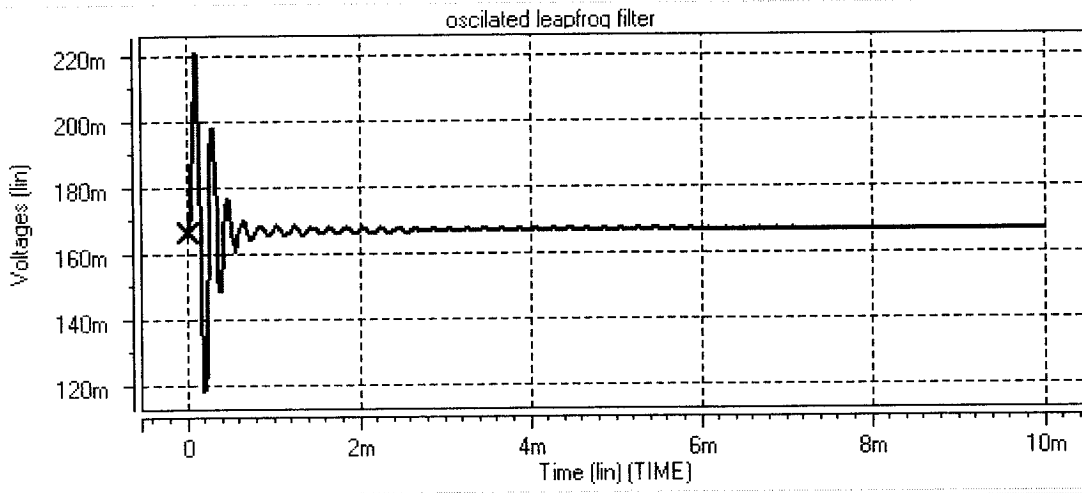


Figure 4.16 Output of a faulty leapfrog filter.

By considering the OpAmps to be ideal in many cases of testing the filters, we will be able to obtain 100% fault coverage. However, in real life they are not 100% ideal, and this will provide an acceptable range for testing with a very good testing margin.

The oscillation frequency of a Notch filter as a CUT obtained by simulation is $4.1160E+03$ Hz and range of amplitude is $\langle -3.1117E-03, 1.9397E-03 \rangle$ Volts.

Table 4.5 Simulation result for testing a notch filter

Inserted Fault	Output Voltage	Output Oscillation
	Level (V)	Frequency
R1 open	$\langle -4.5310E+00, 4.6894E+00 \rangle$	$1.4805E+04$
C1 short	$\langle -4.5234E+00, 4.2553E+00 \rangle$	$1.6779E+04$
R3 open	$\langle -4.4884E+00, 4.8268E+00 \rangle$	$4.2787E+03$
R3 short	$\langle -1.7175E-03, 1.2047E-04 \rangle$	$1.0084E+05$
Other faults	No oscillation	

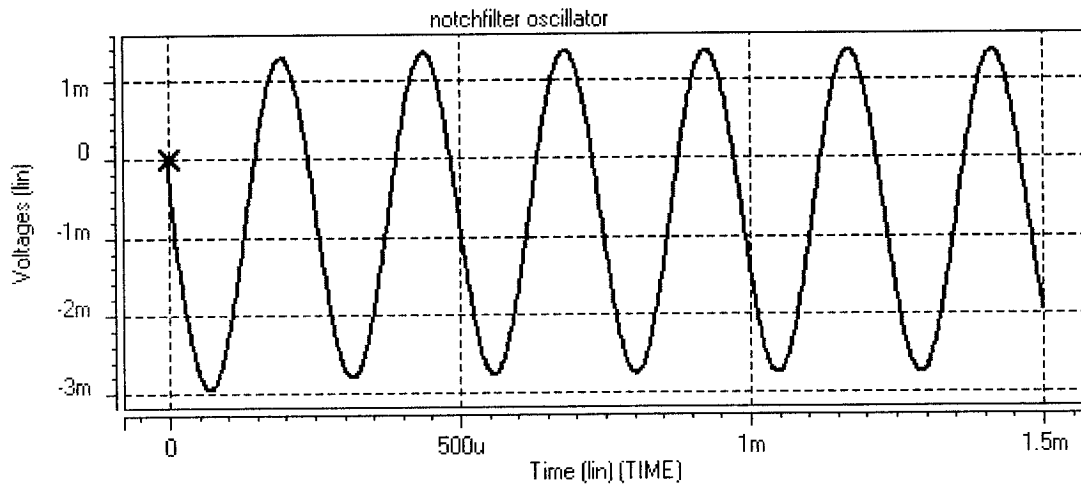


Figure 4.17 Output of Notch filter in the oscillation mode.

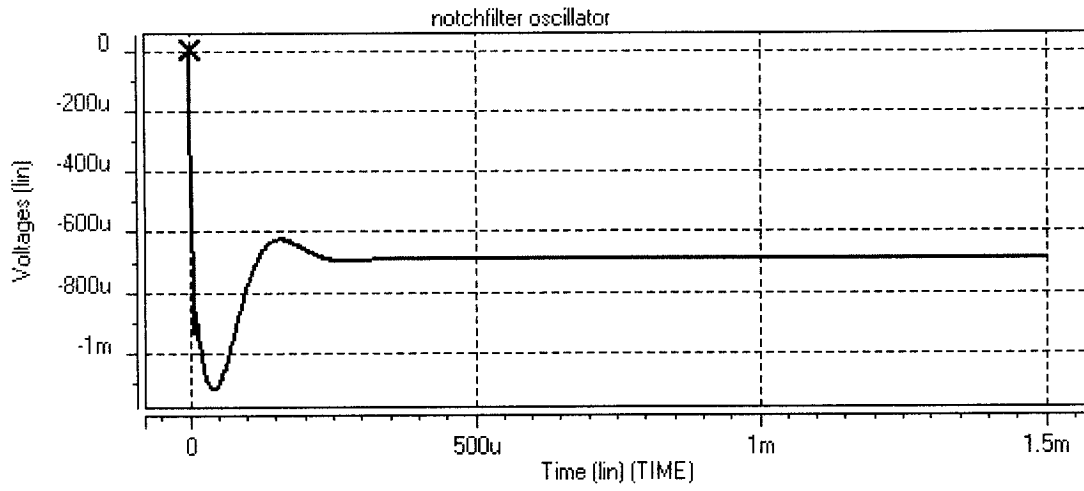


Figure 4.18 Output of a faulty notch filter.

All the injected faults are detected, and 100% fault coverage is obtained.

Chapter 5

Conclusions and Future

5.1 Conclusion

This thesis concentrates on testing analog and mixed signal embedded cores-based circuit chips using BIST methodologies. We focused on oscillation BIST so that a simulator is prepared and analog circuits of various types could be simulated to verify the effectiveness of the approaches in terms of fault coverage. We applied our techniques to inverter, CMOS OpAmp, state variable filter, VCVS filter, FET, leapfrog filter, and Notch filter. Only catastrophic faults are considered for the fault coverage evaluation. By injecting the faults (according to the defined fault model) into the CUT, we measured the frequency and amplitude of the output signal. Then by comparing the results with the test parameters in fault-free condition, CUT is determined to be either faulty or fault-free. Extensive simulation results show that OBIST allows high fault coverage whenever both frequency and amplitude are measured. The emphasis of this method is based on the sensitivity of the oscillation frequency of the CUT to the its other parameters.

5.2 Future Work

Based on the efforts we made and the results we presented in this thesis, there is absolutely no doubt that there remains enormous scope of advancing the objectives of the current research in this evolving field of analog and mixed signal SoCs. Analog BIST is still in its infancy. In future, we intend to extend our research efforts to cover parametric faults in particular and to explore means of increasing the fault coverage yield under such fault conditions in testing mixed signal SoCs.

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**LIST OF PAPERS BY THE AUTHOR ON SOME OF WHICH PORTIONS OF THE
CURRENT THESIS IS BASED**

1. J. Zakizadeh, S. R. Das, M. H. Assaf, E. M. Petriu, and M. Sahinoglu: *Built-in self-test techniques for analog and mixed-signal circuits*, Presented at the **IASTED International Conference on Modeling, Identification and Control**, Innsbruck, Austria, February 16-18, 2005 (Conference Proceedings, pp. ♦-♦).
2. S. R. Das, J. Zakizadeh, M. H. Assaf, E. M. Petriu, and M. Sahinoglu: *Testing analog and mixed-signal circuits with built-in hardware – new approach*, **22nd IEEE Instrumentation and Measurement Technology Conference**, Ottawa, Ontario, Canada, May 17-19, 2005 (accepted for presentation).
3. S. R. Das, J. Zakizadeh, M. H. Assaf, E. M. Petriu, and M. Sahinoglu: *Test Methodology for embedded system-on-chip (SOC) with mixed-signal and analog cores*, **International Symposium on Integrated Design and Process Technology**, Beijing, China, June 13-17, 2005 (accepted for presentation).

Appendix

Definitions:

E exponential

n nano

u micro

m mili

k Kilo