# Class E GaN Power Amplifier Design for WiMAX Base Stations

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A thesis presented to Ottawa-Carleton Institute
for Electrical and Computer Engineering
in partial fulfillment to the thesis requirement for the degree of

**MASTER OF APPLIED SCIENCE**

**in**

**ELECTRICAL AND COMPUTER ENGINEERING**

uOttawa

University of Ottawa
Ottawa, ON, Canada

January 2016

# Abstract

Modern wireless communication systems transmit complex modulated signals with high peak to average ratio in order to deliver high data rates. It demands wide bandwidth and rigorous efficiency performance for power amplifiers. Today's conventional RF power amplifiers have relatively poor operating efficiency and require more power and area for operation. Therefore, more research on high efficiency power amplifier is crucial to the growth of the wireless industry. Until recent days, WiMAX systems are using technology processes such as Gallium Arsenide (GaAs) and Si LDMOSFET to obtain the performance. Although they are providing the required functional performance, they do not optimize cost and/or size.

The primary focus of this thesis is to enhance the efficiency and output power of a compact microwave Power Amplifier suitable for a WiMAX base station. To achieve this goal, this thesis explores the highly efficient switched mode Class E microwave power amplifier using the Gallium Nitride on Silicon Carbide HFET (GaN-on-SiC) technology. The smallest gate length (0.15 μm) device recently released by NRC is used in this design. It provides higher performance at lower cost and area than the alternative Gallium Arsenide (GaAs) technology. Importance is given in designing the bias network of the device. The biasing network has a great impact on efficiency of power amplifiers. Many new techniques of Class E design have been presented to date, but there is not significant improvement related to the biasing network. A highly efficient Class E power amplifier for WiMAX base station transmitter was developed in this thesis for 2.5 GHz application. An improved bias network was introduced for biasing the active device. This successful design shows acceptable simulated performance with a gain of 10.12 dB, an output power of 34.12 dB, and a power added efficiency of 41.7 % at the peak output power.

# Acknowledgements

I was enjoying the whole period of working with this thesis. Yes, there was frustration when I was not getting the expected results but it gave me a lot of joy and happiness when I could figure out the problems. I want to take the opportunity to thank some awesome and great people who were always there when I needed them most during the last couple of years.

First of all, I want to thank National Research Council Canada (NRC) for providing me the latest released GaN design kit that is the backbone of this thesis. I would like to express my sincere gratitude and appreciation to everyone who made this thesis possible. Most of all, I would like to thank my supervisor, Dr. Mustapha C.E. Yagoub for his guidance and his patience during my research. With his knowledge and experience, he has guided me to successfully achieve my thesis objective.

Second, I would like to specially thank to my best friend Faria Safina Zaman and her family for their support and encouragements. She was always there to give me hope when I became disappointed to my work. I thank them for helping me pursue my academic goals.

Third, I would like to thank my brother Mehedi Hasan for his valuable suggestions and motivational comments. He was always pushing me up toward my goal. Without his help, it would be difficult for me to complete this work on time.

Fourth, I would like to thank Abdullah Mohammed, a PhD student at the University of Ottawa, for his last moment help regarding the layout design.

Last, but most importantly, I would like to thank my parent. Without their support and sacrifice, it would not be possible to successfully complete this research.

I will always be indebted to all of these extraordinary people.

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# List of Acronyms and Abbreviations

| | |
|---|---|
| 2DEG | Two Dimensional Electron Gas |
| ACPR | Adjacent Channel Power Rejection |
| AM | Amplitude Modulation |
| BJT | Bipolar Junction Transistor |
| CAD | Computer Aided Design |
| CDMA | Code Division Multiple Access |
| CMOS | Complementary Metal Oxide Semiconductor |
| DSP | Digital Signal Processing |
| EER | Envelope Elimination and Restoration |
| EM | Electromagnetic |
| EMC | Electromagnetic Compatibility |
| ET | Envelope Tracking |
| FM | Frequency Modulation |
| GSM | Global System for Mobile communications |
| HBT | Heterojunction Bipolar Transistor |
| HEMT | High Electron Mobility Transistor |
| HFET | Heterojunction Field Effect Transistor |
| IMD | Intermodulation Distortion |
| LDMOSFET | Laterally Diffused MOSFET |
| LTE | Long-Term Evolution |
| MESFET | Metal-semiconductor Field Effect Transistor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| NRC | National Research Council Canada |
| PAE | Power Added Efficiency |
| PEP | Peak Envelope Power |
| PAPR | Peak to Average Power Ratio |
| PM | Phase Modulation |
| PTP | Point-to-Point |
| PMP | Point-to-Multipoint |
| Q-factor | Quality factor |
| RF | Radio Frequency |
| RFC | Radio Frequency Choke |
| RFIC | Radio Frequency Integrated Circuit |
| SOFDMA | Scalable Orthogonal Frequency Division Multiple Access |
| SOC | System-on-Chip |
| SPST | Single Pole Single Throw |
| SMT | Surface Mount Technology |
| VLF | Very Low Frequency |
| WCDMA | Wideband Code Division Multiple Access |
| WiMAX | Worldwide Interoperability for Microwave Access |

# List of Variables

| | |
|---|---|
| $\eta$ | Efficiency of the device |
| $f_{max}$ | Maximum frequency |
| $I_C$ | Current through capacitor |
| $I_{max}$ | Maximum current |
| $I_{SC}$ | Short circuit current |
| $I_{out}$ | Output current |
| $I_{load}$ | Load current |
| PAE | Power added efficiency |
| $P_{out}$ | Output power |
| $P_{in}$ | Input power |
| $P_{DC}$ | DC power |
| $P_{SW}$ | Switching power |
| $V_{CC}$ | DC suply voltage |
| $V_{SC}$ | Voltage across the switch |
| $V_{out}$ | Output voltage |
| $V_{DD}$ | Drain voltage |
| $V_{BAT}$ | Battery voltage |

# Chapter 1

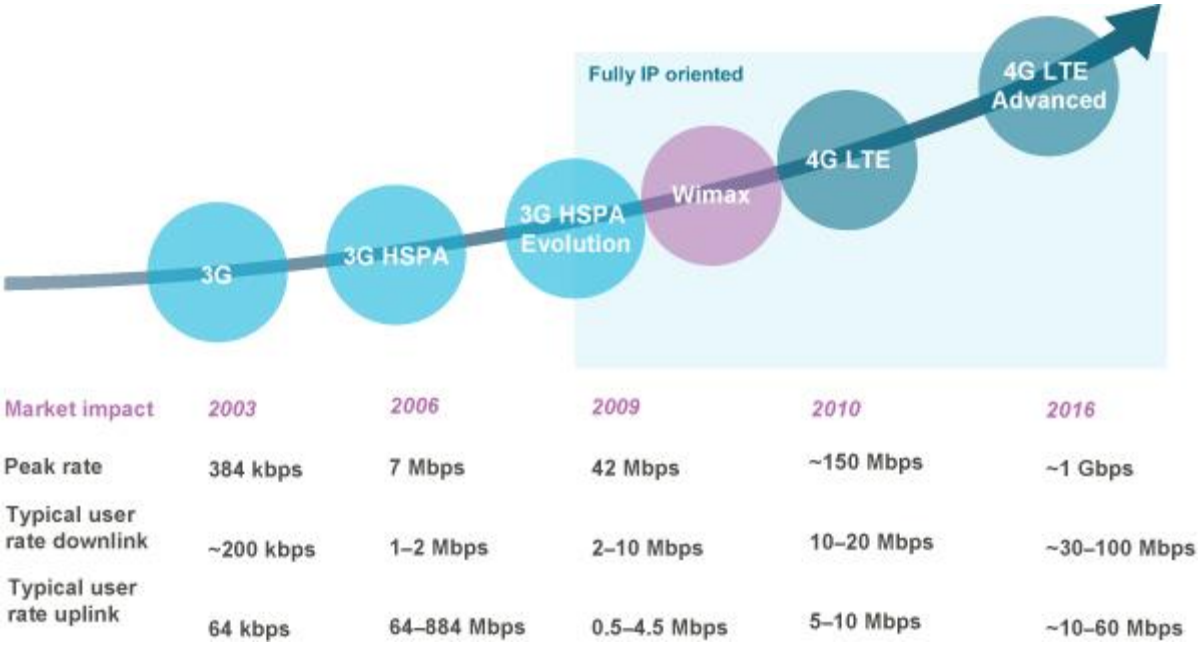
# Introduction

## 1.1 Motivation

The number of subscribers and digital content is growing rapidly. Many new services like music download and internet access over wireless cellphones and tablets have meant more and more data transmission over the wireless infrastructures. However, at the same time, the frequency allocation for wireless communications has been almost constant leading to overcrowded wireless network. Meeting these demands increased the base station procurement costs and operating expenses. These extra expenses are driven by high-energy consumption. The base station power amplifiers (PAs), which are responsible to drive the wireless signal outward from the base station, require approximately 30% of the base station costs [1].

The rapid growth is stressing the wireless infrastructures in more and more data demand on a limited wireless spectrum. This can be related to very crowded traffic at a rush hour in a highway. Imagine the wireless spectrum as highway and the data (voice call, internet content etc.) as cars. The size of the highway or the number of lanes represents the fixed amount of wireless spectrum. Adding more spectrum in the wireless system is like adding more lanes in the highway, which needs much undertaking. In the highway, all the cars want to arrive their destination on time. However, when too much cars start gathering at the same highway, the speed slows down. The same thing happens in the wireless network.

Now the wireless providers have switched to wireless standards that can use the spectrum more efficiently [2]. This can be related to stacking multiple cars in a big truck and then sending it down the highway. The truck will take all the cars in it to the desired destination. In this way, more data can be transferred using the same network without slowing down the system. The wireless standards CDMA2000, W-CDMA, TD-SCDMA, MC-GSM, WiMAX and LTE have been mainly defined in purpose of improving the spectral efficiency [2, 3]. Figure 1 shows the wireless standards defined in recent years to improve the spectral efficiency. These standards can move greater amount of data in the fixed wireless spectrum but they also have downsize. They are very sensitive to the distortion of base station power amplifiers (PA).




| Market impact | 2003 | 2006 | 2009 | 2010 | 2016 |
|---|---|---|---|---|---|
| Peak rate | 384 kbps | 7 Mbps | 42 Mbps | ~150 Mbps | ~1 Gbps |
| Typical user rate downlink | ~200 kbps | 1–2 Mbps | 2–10 Mbps | 10–20 Mbps | ~30–100 Mbps |
| Typical user rate uplink | 64 kbps | 64–884 Mbps | 0.5–4.5 Mbps | 5–10 Mbps | ~10–60 Mbps |

Figure 1: Evolution of wireless standards [4]

This distortion can degrade signal quality and have impact on data traffic. Wireless providers must think of this and they need to reduce the transmit power of the base station power amplifier or they have to purchase a large PA to cover the whole area.

### 1.1.1 Worldwide Interoperability for Microwave Access (WiMAX)

In recent years, one of the wireless communication standards, known as WiMAX, has been gradually popular in the market [5-8]. This technology is gaining popularity for its point-to-point (PTP) and point to multipoint (PMP) message services as well as for providing high data rate and long transmission distance [8].

WiMAX standard is hitting its popularity due to the lack of wireline broadband services in many areas. Broadband services are mainly available in large developed metropolitan areas and in some small cities, but the rural areas and developing countries are deprived of wireline backbone due to high cost in building optical fiber or cable-based infrastructure. In most cases, the service providers do not see significant return-on-investment for wireline implementation. So, they leave many communities without broadband access.

The name WiMAX was created by the WiMAX forum established in June 2001 [8]. The WiMAX forum describes this standard as "a standard-based technology enabling the delivery of last mile wireless broadband access as an alternative to cable and DSL". The WiMAX broadband standard is based on IEEE 802.16 family of wireless network standards [9]. IEEE announced 802.16a in 2003 [8]. It transmitted data through non-line of sight radio channels to and from omnidirectional antennas. Later on, the 802.16-2004 standard was released in 2004. This standard combined the updates from the IEEE 802.16a, 802.16b and 802.16c regulations [8, 9]. This new standard expanded the WiMAX service to a 30-mile range. In 2005, IEEE came up with the first mobile WiMAX system. It was IEEE 802.16e. This version of the standard used a SOFDMA engine, which supported over 2000 subcarriers and increased network security. IEEE is still working on the update and modification of the WiMAX system to further improvements. They are looking forward to deploy 802.20 standard in near future, which got the nickname "Mobile-Fi" [9].

WiMAX can provide a variety of applications, including that of providing broadband coverage across whole cities or countries with its range of up to fifty kilometers [8]. In North America, one or more copper line connections are used for backhaul operation in urban regions [8, 10]. The remote cellular operations are sometimes backhauled via satellite. WiMAX is offering more substantial backhaul bandwidth. In recent days, the use of wireless microwave backhaul is rising in North America and existing links are being upgraded in all regions [10].

WiMAX technology promises to offer the best broadband services to the end-users. This technological advancement has been possible by stretching the limits of existing solid-state power amplifiers. However, the improvement of existing power amplifiers has been done without the significant change in size or in transmitter efficiency and complexity. This makes the power amplifier the most expensive in any radio front-end. In many high frequency power amplifiers, up to ninety percent (90%) of applied DC power is lost as heat leading to low DC-RF conversion efficiency [4, 6]. In reality, designers are forced to design inefficient and bigger sized power amplifiers in terms of extra circuitry for heat removal, in order to minimize adjacent channel spillover to save valuable spectrum.

### 1.1.2 Power Amplifier

Power amplifier is a type of electronic amplifier used to convert a low-power signal into a larger signal of significant power, typically for driving the antenna of a transmitter. To understand how a power amplifier works, consider Figure 2. An ideal power amplifier has one to one or linear response shown by the straight line (upper line in figure 2). That means if the input power is increased by 20 percent, the output power increases by the same amount of 20 percent. The bottom curve of figure 2 depicts the performance of a real world power amplifier.

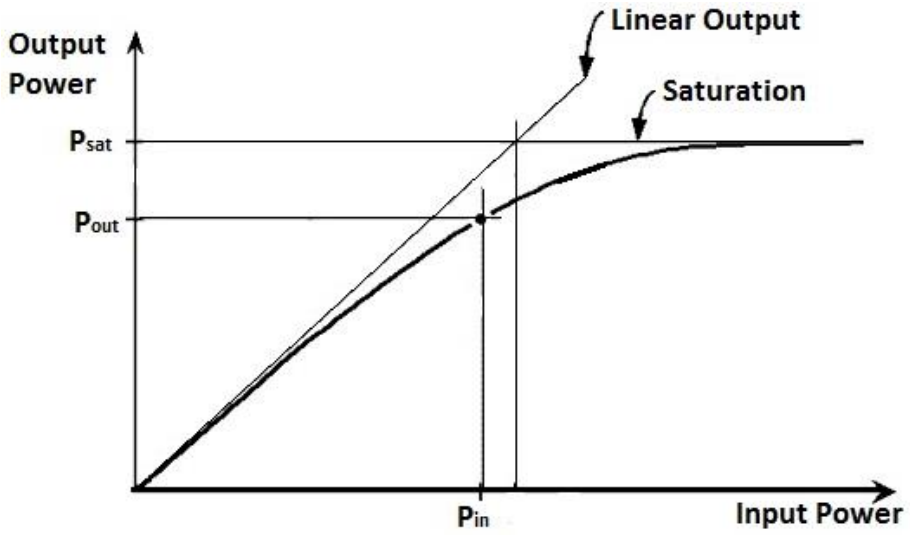



Figure 2: Input-output characteristic of Power Amplifier

Power amplifiers are categorized in two groups, linear power amplifiers and switched mode power amplifiers [11]. Switched mode amplifiers are highly efficient having compromise with linearity. The power amplifier's efficiency (Ƞ) is a measure of its ability to convert the DC power of the supply into the signal power delivered to the load. On the other hand, power added efficiency (PAE) is defined as the ratio of the difference of the output and input signal power to the DC power consumed.

High efficiency for a single power level can be achieved through some ways such as harmonic tuning [12], single stage Class B or AB design [11, 12], Chireix outphasing [13], Envelop elimination and restoration (EER) [14], Doherty [15] and Envelop tracking (ET) [16]. However, these techniques face problems like poor output power or average efficiency when a non-constant

envelop signal is being amplified. Switched mode power amplifiers such as Class D, Class E and Class F can be considered in this case due to their ability to deliver high efficiency with a high output power level [11, 13]. Class D amplifiers are mainly suitable for audio frequencies. Class F amplifier design is difficult mainly due to the complex design of the output matching network. This complex design intentionally squares the voltage waveform through controlling the harmonic contents of the output waveform. Class F and $F^{-1}$ power amplifiers have been implemented mainly in the 1-5 GHz band [17]. In recent days, Class E switched-mode power amplifier is demonstrating its nobility in high efficiency applications [18-25]. In early 70's, Artym, Gruzdev, Popov, Kozyrev and N. Sokal introduced the Class E amplifier operation [26, 27]. N. Sokal's contribution is more important in this case [26]. He introduced the first practical design formulas for output matching network components calculation. However, Class E operation in the microwave range got the serious attention of the wireless industry due to the work done by Mader and others [27]. Class E uses a significant amount of second-harmonic voltage to reduce the overlap between voltage and current edges with finite sharpness. The most important advantage of the Class E structure is that it includes a shunt capacitor at the drain of the transistor, which allows the device parasitic capacitance at the drain to be incorporated into the design. It helps avoiding the performance degradation or the need to resonate out this capacitor. In a simple way, Class E architecture of a power amplifier can provide the needed higher efficiency without compromising the gain or output power with a simplified load network than other switched mode amplifiers. However, the conventional Class E PA does not have an efficient bias network like other classes of amplifiers [17]. There is much less research conducted in the bias network area of Class E amplifiers, while the transistor biasing network is an important part of the design. The DC input signal enters into the device through the input biasing network and the RF output signal comes out of the device through the output biasing network, hence the biasing network has to be lossless and much more efficient to achieve the actual usefulness of using Class E type amplifier.

### 1.1.3 Gallium Nitride (GaN) technology

In near past, LDMOSFET was the most attracted device for power amplifier design due to good voice and data transmission [28]. LDMOS behaviour is more linear than other technologies. However, its lower frequency range makes LDMOS less attractive in high frequency and high power operation. Although, designers are using Gallium Arsenide (GaAs), Indium Phosphide (InP)

or Silicon Germanium (SiGe) amplifiers for high frequency applications, their performance are limited to low power and/or low voltage states and more importantly, these solutions are costly and only a limited range of applications can be addressed [28]. In recent days, microwave designers are showing their interest toward Gallium Nitride (GaN) technology as a potential replacement for heavily taxed Silicon (Si) based microwave base station systems [29, 30]. GaN is gaining attention of the designers around the world and thus, this work introduces high efficiency and low sized microwave GaN power amplifier to support the cost effective and high frequency base station applications.

GaN is the technology that allows designers to implement essential clean-tech innovation where efficiency is a key requirement. It belongs to the family of wide bandgap semiconductors. It has the ability to support high supply voltages, high DC-RF conversion efficiency and high power generation. Until now, bulk GaN substrates are not available, that is why Silicon Carbide (SiC) or Sapphire are used as substrates [31]. Sapphire costs lower than SiC, but its thermal impedance makes it less attractive than SiC for power applications. SiC and Diamond are the only wide bandgap semiconductors in this family, which can be found in bulk format. They can offer superior properties of high frequency greater than 1 GHz and high power operation [31, 32].

The excitement about GaN comes from its unique material and electronic properties. The key characteristics provided by GaN devices include high dielectric strength, high operating temperature, high current density, high-speed switching and low on-resistance. GaN devices offer ten times higher electrical breakdown, three times the bandgap and exceptional carrier mobility compared to Silicon (Si) devices [30]. All these provided the inspiration to study more about switched-mode Class E GaN based microwave power amplifier in this thesis.

## 1.2 Thesis Contributions

This thesis focuses on the design of switched mode Class E power amplifier for WiMAX base station application. Class E amplifier can be included to a GaN-on-SiC based circuit with some modifications for possible application in the WiMAX (IEEE 802.16-2005) band at 2.5 GHz. Linearity is a critical design issue in many applications. The power amplifier design always considers the trade-offs between linearity and efficiency. Switched mode power amplifiers are considered as highly nonlinear while maintaining high efficiency. Linearity of the power amplifier

alone is worthy of a thesis topic. As Class E topology is applied here and the main purpose of this work is to enhance the efficiency of the PA unit, linearity is outside the scope of this work. The specific contributions of this work include:

- The use of the smallest gate length GaN based HFET recently released by the NRC for Class E amplification [32]
- The design of a high efficiency wide band GaN based Class E PA with improved bias network. Many researches have been conducted regarding efficiency and output power of the amplifier while quite few ones were related to the improvement on the bias network. This thesis introduces an improved bias network for Class E amplifier.
- Discussion related to various circuit design issues and efforts to propose solutions to PA designers.

## 1.3 Thesis outline

The rest of the thesis is developed upon the motivation and objectives discussed in the last sections, leading to the full design of a Class E microwave power amplifier. Chapter 2 discusses the basics of power amplifier design and the different microwave power amplifier classes. Then, Class E amplifier is introduced in this chapter followed by a discussion about the configuration and operation of Class E power amplifier. Chapter 3 presents a brief literature review about previous researches in the area. This chapter also discusses about the conventional MOSFETs and HFETs. There is comparison of the wide bandgap semiconductors with others. Chapter 4 presents the improved bias network designed in this work and the different biasing techniques to bias a power amplifier.

Chapter 5 introduces the high efficiency Class E microwave power amplifier designed in this work, for the possible application in WiMAX transmitters. Simulation results are presented and compared to prior works. Chapter 6 describes the layout design and co-simulation results. Chapter 7 abbreviates the whole work and discusses about future possible contributions in the area.

# Chapter 2

# Microwave Power Amplifiers

## 2.1 Basics of Microwave power amplifiers

The RF/microwave power amplifier is a critical element in the base station communication unit. It is expected to provide suitable output power at a very good gain with a high linearity and efficiency. The function of a power amplifier is to take the RF/microwave signal and transfer it to the output with significantly larger amplitude by converting the DC power to the microwave signal. The output power from the power amplifier must be sufficient for reliable transmission. Power amplifier performance is usually evaluated by two main parameters: efficiency (Ƞ) and power added efficiency (PAE).

Efficiency (Ƞ) is a measure of how well a device converts one energy source to another. In different processes that occur in everyday life, different levels of efficiency can be expected, usually based on the physics of the device involved. In microwaves, the conversion of DC power to RF power is the matter of great concern. For example, the longer life of a cell phone's battery is dependent on the higher efficiency of a power amplifier. This is because the transit amplifier chain is primarily responsible for the draining of the battery. The power added efficiency (PAE) is similar to drain efficiency, but it takes into account the RF power that is added to the device at its input. In theoretical sense, a power amplifier with infinite gain will have PAE equal to drain efficiency. For a real amplifier, PAE will always be less than drain efficiency. The maximum possible PAE of a device always decreases with frequency. This is because the natural tendency for maximum gain of an active device to decrease with frequency. That is why it becomes a challenge for designers to maintain high PAE at the higher frequency level. The definition of the efficiency can be represented in an equation form as [33]:

$$\eta = \frac{Signal\ power\ delivered\ to\ load}{DC\ power\ supplied\ to\ output\ circuit} \qquad (1)$$

While the Power added efficiency (PAE) can be expressed as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (2)$$

where $P_{out}$ is the output power, $P_{in}$ is the input power, and $P_{DC}$ is the DC power of the amplifier.

The behavior of power amplifier can be categorized in two modes [33]. One of them is the current source mode, where the transistor acts as a high impedance current source. Other one is the switched mode, where the transistor acts like a typical ON/OFF switch. Choosing the bias points of an RF power amplifier can determine the level of performance ultimately possible with that PA. The trade-offs for output power, efficiency, linearity or other parameters for different applications can be evaluated by comparing PA bias approaches. The power class of the amplification determines the type of bias applied to an RF power transistor

A power amplifier has three fundamental characteristics [33, 34]. First, the output power determines the range of the wireless signal. Greater output power determines the larger coverage area for the base station. Second, the power efficiency of the PA increases with the increment of output power and it is highest near the saturation region. These two characteristics show that it is best to operate the base station at its highest power to have the larger coverage area and most efficient power consumption. The third one is that the distortion increases with the increase of output power and it becomes significant when the PA begins to deviate from its ideal curve. This third characteristic is important because modern wireless standards are much more susceptible to distortion. That means that base station power amplifiers must be operated at levels well below the saturation level to provide acceptable signal quality. On the other hand, at levels below saturation, a handsome percentage of input power is dissipated as heat rather than transmitted to the output.

Figure 3 illustrates the block diagram of a typical WiMAX base station system. There are different power amplifier classes based on different applications such as class A, class B, class AB, class C, class E, class F, etc. These amplifier classes are designed with the trade-offs between linearity and efficiency. In recent days, due to the development of high data rate wireless systems, power amplifiers are required to have different operation modes and operating frequencies. High gain reduces the amplifier's number of stages and therefore, the size and production cost.

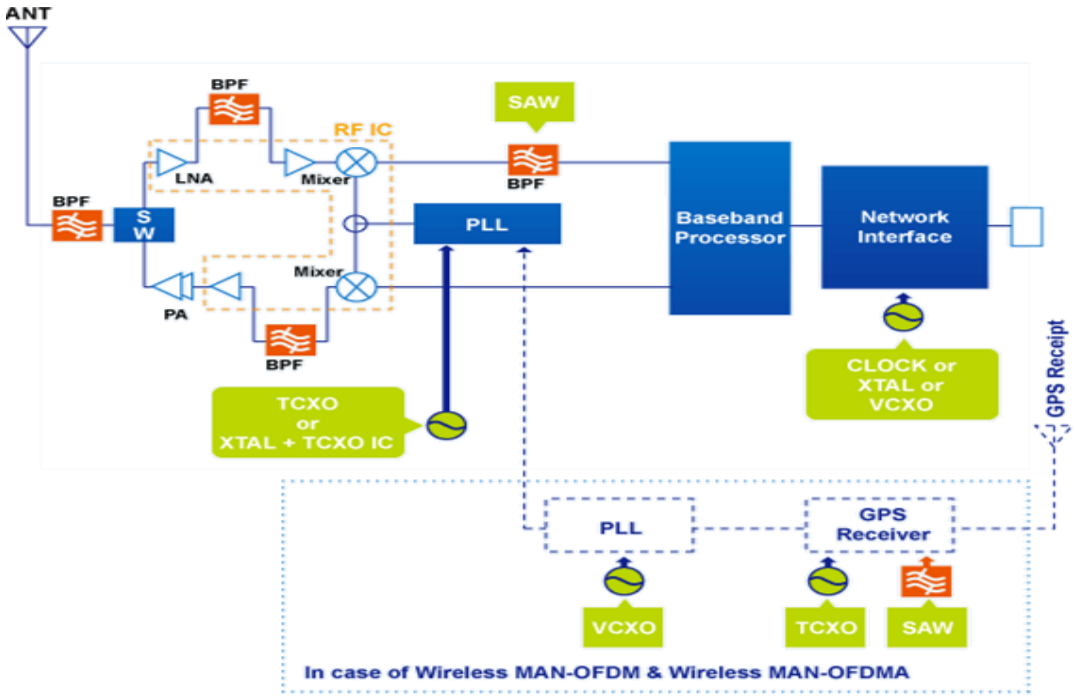



Figure 3: Typical WiMAX Base Station block diagram [35]

High efficiency improves the thermal management and increases the battery lifetime. It also reduces the operational costs. Good linearity is needed to have bandwidth efficiency modulation. However, these requirements require certain level of trade-offs among the performance parameters. The different classes of power amplifier mentioned above differ from each other in terms of output power, gain, linearity, and efficiency.

## 2.2 Conventional power amplifier classes

Microwave power amplifiers are used in a large variety of applications including wireless communication, TV transmission, and Radar, to name a few. The basic techniques for microwave power amplification can use classes for frequencies ranging from VLF (very low frequency) through millimeterwave frequencies and beyond. Output power can range from mW to MW depends on application.

Most important parameters that define an RF power amplifier are output power, gain, linearity, stability, DC supply voltage, efficiency, ruggedness, weight, and cost.

## 2.2.1 Class A power amplifier

This type of power amplifier is defined as an amplifier that is biased in a way so that the output current flows at all the time and the input signal drive level is kept small enough to avoid driving the transistor in cut-off. Another way of stating this is to say that the conduction angle of the transistor is 360°, meaning that the transistor conducts during the full cycle of the input signal. That makes Class A the most linear of all amplifier types, where linearity means simply how closely the output signal of the amplifier resembles the input signal. Figure 4 depicts the input-output waveforms of a typical class A PA.

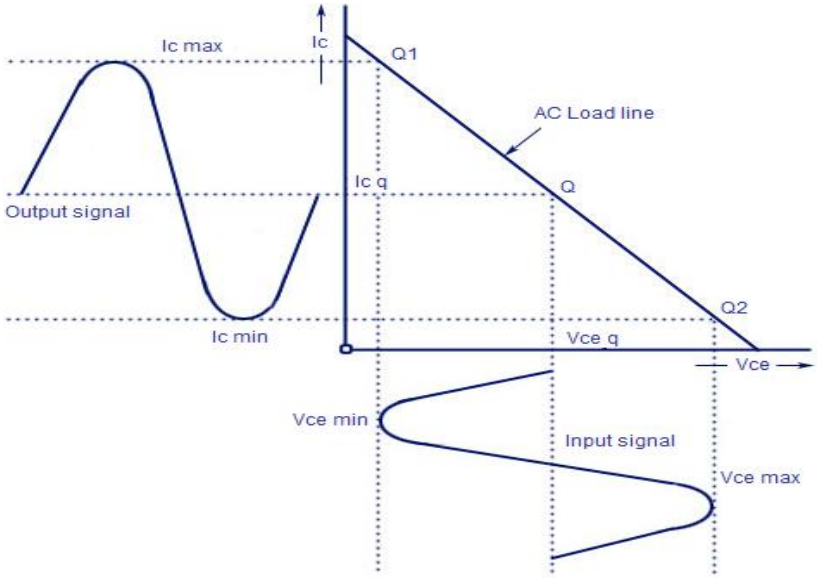



Figure 4: Class A PA regions and waveforms [36]

The main disadvantage of this class of amplifiers is that the transistor never turns OFF because of having biasing Q-point in the middle of its load line. Therefore, the device is constantly carrying current, which represents a continuous loss of power in the amplifier. The efficiency of real class A PAs is degraded by the ON state resistance or saturation voltage of the transistor. It is also degraded by the presence of load reactance, which in essence requires the PA to generate more output voltage or current to deliver the same power to the load [33].

$$\text{Ƞ (Efficiency of class A)} = \frac{Max\ Load\ Voltage}{2*V_{cc}^2} \qquad (3)$$

where $V_{cc}$ the bias voltage supply.

## 2.2.2 Class B power amplifier

This is an amplifier in which the conduction angle for the transistor is approximately 180°. Thus, the transistor conducts only half of the time, either on positive or negative half cycle of the input signal. The same as in class A, the DC bias applied to the transistor determines the class B operation. Figure 5 shows the input-output waveforms of an ideal class B power amplifier.

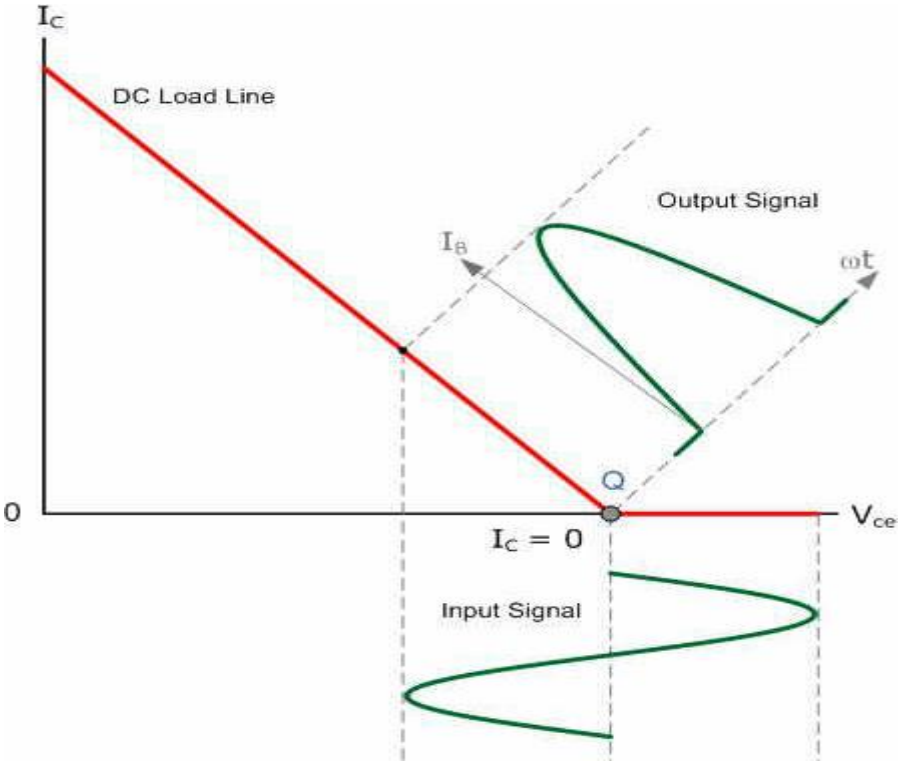



Figure 5: Class B PA waveforms [37]

Class B amplifiers are more efficient than class A amplifiers. The instantaneous efficiency of a class B PA varies with the output voltage and, for an ideal PA, reaches π/4 (78.5%) at PEP. On the other hand, they are much less linear than class A amplifiers. Therefore, a typical class B amplifier will produce quite a bit harmonic distortion that must be filtered from the amplified signal. There is no DC base bias current in this amplifier as its quiescent current is zero, so that the dc power is small, leading to a much higher efficiency compared to class A amplifiers. The efficiency of class B power amplifiers can be determined as [11]

$$\text{Ŋ (Efficiency of class B)} = \frac{(\pi * V)}{(4 * V_{cc})} \qquad (4)$$

However, the class B amplifier design can create distortion at the zero-crossing point of the waveform due to the transistors dead band of input base voltages from -0.7 V to +0.7 V.

### 2.2.3 Class AB power amplifier

This amplifier is a compromise between class A and class B in terms of efficiency and linearity. The transistor is biased typically to a quiescent point which is somewhere in the region between the cut-off point and the class A bias point, at ten to fifteen percent of $I_{Cmax}$. In this case, the transistor will be ON for more than half a cycle but less than a full cycle of the input signal. Conduction angle in class AB is between 180° and 360° and efficiency is between 50% and 78.5%. Figure 6 illustrates the input-output waveform of typical class AB power amplifier.

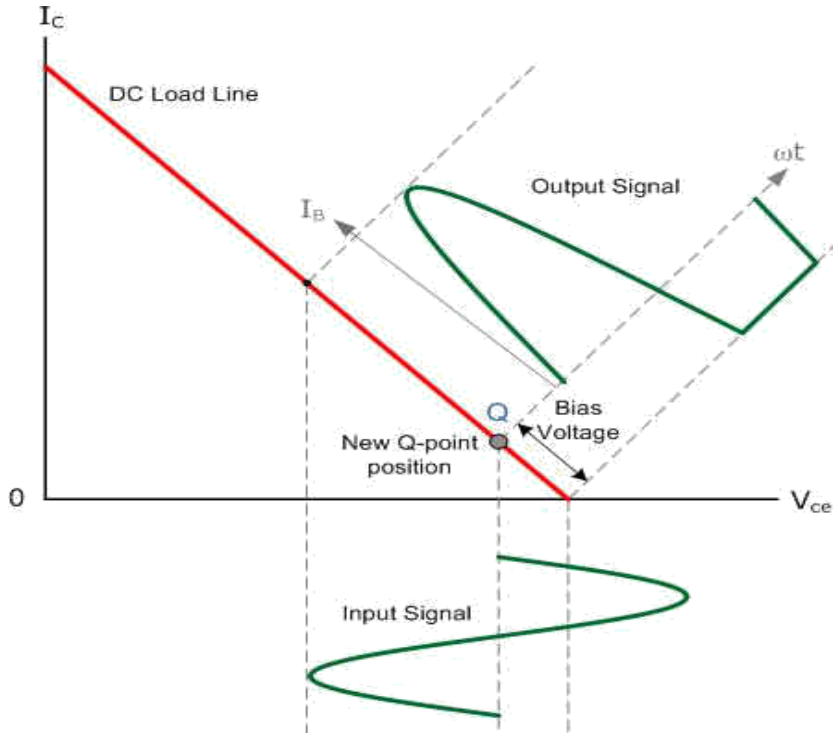



Figure 6: Class AB PA waveforms [38]

Experimentally, it was found that class AB often offers a wider dynamic range than either class A or class B operation. This is because gain compression in class AB comes from a different and additional source than class A. Saturation effects are primarily caused by the clipping of the RF voltage on the supply rails. Conventional class AB operation incurs odd degree nonlinearities in the process of improving efficiency. Theoretically, increasing efficiency all the way up to 78.5%, the device shall generate only even order nonlinearities. Such a device will not generate

undesirable signals close to carrier intermodulation distortion. Amongst the many requirements of a base station power amplifier, linearity and efficiency are the most crucial. Power amplifier can be operated at a backed off power level from the peak output power in a linear and efficient class of operation to meet the linearity requirements. Class AB amplifier would be a better choice in this case. However, due to the high PAPR of the signal, it will lead to a very low efficiency at the average output power of the signal [11].

### 2.2.4 Class C power amplifier

In this type of amplifier, the conduction angle for the transistor is significantly less than 180°. Figure 7 represents the input-out output waveform of Class C amplifier. The transistor is biased such that under steady state conditions no collector current flows and thus, idles at cut-off [11].

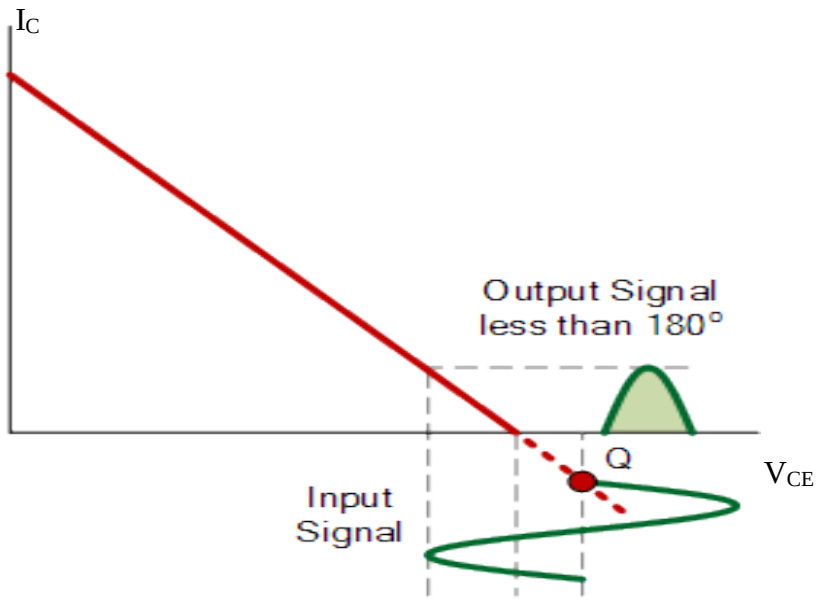



Figure 7: Class C PA waveforms [39]

The efficiency of this class of amplifier can approach 85%, which is much better than either class A or class B. In order to bias a transistor for class C operation, it is necessary to reverse bias of base-emitter junction. External biasing is usually not needed because it is possible to force the transistor to provide its own bias using an RF choke from base to ground. However, one of the major problems with utilizing Class C in solid-state applications is the large negative swing of the input voltage, which coincides with the collector/drain output voltage peaks. This is the worst condition for reverse breakdown in any kind of transistor, and even small amount of leakage

current flowing at this point of the cycle have an important effect on the efficiency. For this reason, true Class C operation is not often use in solid-state at higher RF and microwave frequencies.

Table 1 presents the conduction angles and the theoretical maximum drain efficiencies for the conventional amplifiers discussed so far.

Table 1: Conduction angles and maximum drain efficiencies of conventional PAs [11, 33]

| **PA class** | **Conduction angle (°)** | **Drain efficiency, $DE_{max}$ (%)** |
|---|---|---|
| Class A | 360 | 50 |
| Class B | 180 | 78.5 |
| Class AB | 360-180 | 50-78.5 |
| Class C | < 180 | 85 |

## 2.3 Switch-mode Power Amplifiers

The operating principle of a switch-mode PA is based on the idea that the active device operates in saturation, thus it can be represented as a switch and either voltage or current waveforms across the active device are alternatively minimized to reduce overlap, so minimizing power dissipation in the device itself. If the transistor is an ideal switch, a 100% of efficiency can be achieved by the proper design of the output matching network [17]. In actual cases, several losses mechanisms, such as capacitive and ohmic discharge or leakage, cause an unavoidable overlapping between the voltage and current waveforms, together with power dissipation at higher harmonics, thus limiting the maximum achievable efficiency levels. Following is the discussion about some well-established switched-mode PAs reported to date.

### 2.3.1 Class D power amplifier

The voltage mode Class D amplifier is defined as a switching circuit that results in the generation of a half-sinusoidal current waveform and a square voltage waveform. Figure 8 shows the voltage-current waveform of Class D amplifier. Class D PAs use two or more transistors as switches to generate a square drain voltage waveform. Figure 8 depicts the output voltage and current waveforms of an ideal Class D power amplifier. A series tuned output filter passes only the fundamental frequency component to the load. Class D amplifiers can theoretically reach 100%

efficiency, as there is no period during a cycle where the voltage and current waveforms overlap. However, no real amplifier can be a true Class D as non-zero switch resistances and capacitive as well as inductive parasitic restrict the shape of the drain voltage waveform.

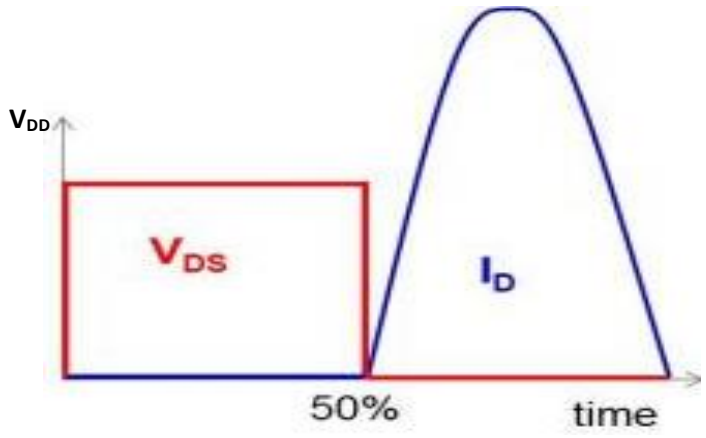



Figure 8: Class D voltage and current waveforms [40]

### 2.3.2 Class F power amplifier

Class F boosts both efficiency and output by using harmonic resonators in the output network to shape the drain waveforms. The voltage waveform includes one or more odd harmonics and approximates a square wave while the current includes even harmonics and approximates a half sine wave. Alternatively, in inverse Class F, the voltage can approximate a half sine wave and the current a square wave. Class F amplifier designs intentionally squaring the voltage waveform through controlling the harmonic content of the output waveform. This is accomplished by implementing an output matching network that provides high impedance 'open circuit' to the odd harmonics and low impedance 'short circuit' to the even harmonics. This results in a squared off voltage waveform. Only the third harmonic is peaked. Figure 9 depicts the voltage and current waveforms of Class F amplifier. Class F amplifiers are capable of high efficiency (88.4% for traditionally defined Class F or 100% if infinite harmonic tuning is used). However, the design of this type of amplifier is difficult mainly due to the complex design of the output matching network.

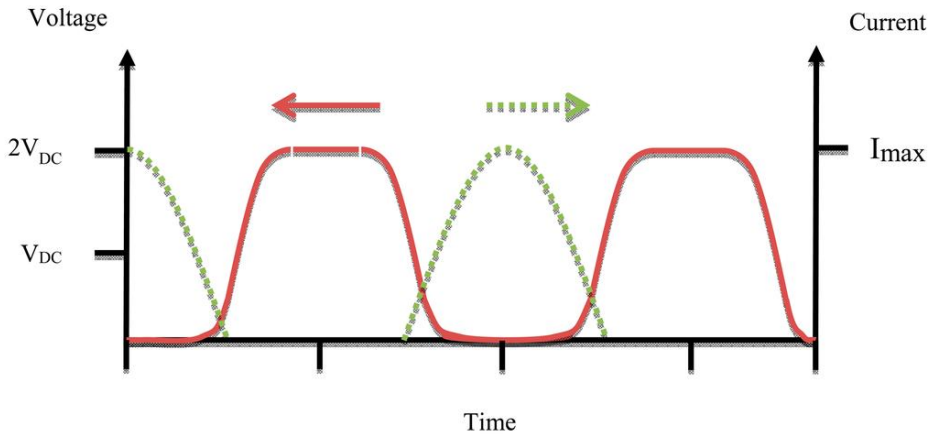



Figure 9: Class F voltage and current waveforms [41]

### 2.3.3 Class E power amplifier

Class E employs a single transistor operated as a switch. The collector/drain voltage waveform is the result of the sum of the DC and RF currents charging the drain shunt capacitance, which is parallel with the transistor internal capacitance. In optimum Class E, the drain voltage drops to zero and has zero slope just as the transistor turns on. The result is an ideal efficiency of 100%, elimination of the losses associated with charging the drain capacitance in Class D, reduction of switching losses and good tolerance of component variation. The transistor behaves as a perfect switch. Figure 10 shows the transistor switching behavior. When it is ON, the collector/drain voltage is zero and when it is OFF the collector/drain current is zero.

Class E power amplifiers are primarily variant from other classes of amplifiers discussed in previous sections. In case of conventional classes of power amplifiers, it was noticed that the operational differences were obtained by the selection of the bias point. However, in case of Class E amplifier, only circuit independent signal guidelines are provided. Moreover, the circuit topology is not restricted to any particular design. This section provides an insight of switched mode Class E power amplifier.

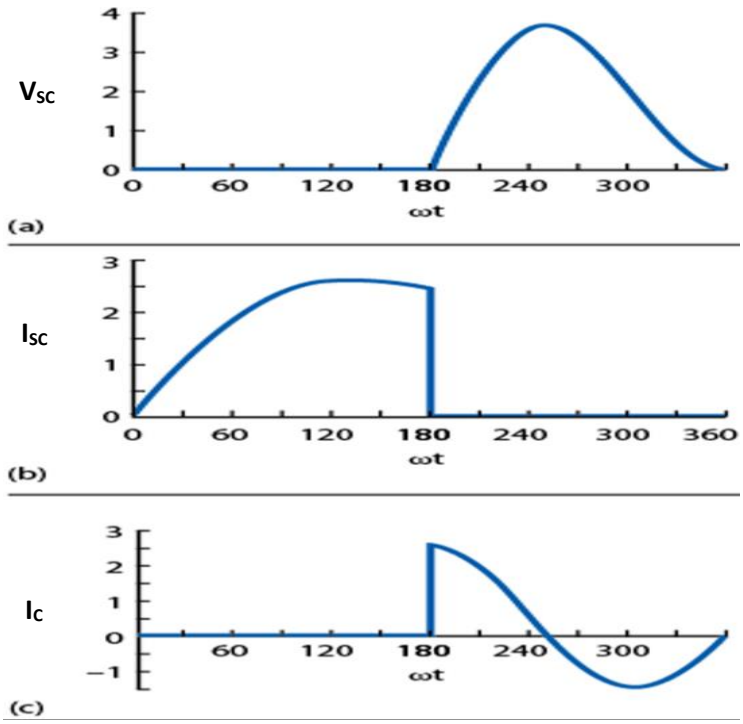



Figure 10: Class E voltage and current waveforms [42]

### 2.3.3.1 Class E Configuration analysis

The original form of the Class E circuit is to use a shunt capacitor with the active device. Figure 11 illustrates an ideal class E circuit with a shunt capacitor, $C_P$, parallel with a single-pole, single-throw (SPST) switch. The value of $C_P$ is considered as a linear design parameter. Basically, this shunt capacitor $C_P$ is entirely or at least partially composed of the output capacitance of the active device. The series resonator consists of $L_S$ and $C_S$ and is also important in the design. The resonator is tuned to the fundamental frequency.

Several assumptions about the ideal circuit can be made to simplify the analysis [17]:

- The switch that models the transistor is lossless. It has instantaneous switching action.
- The inductor, $L_{rfc}$, through which the DC bias is provided, is lossless. It has a high enough reactance to restrict any variation in DC current and prohibit loading the circuit.
- The series resonator circuit has a high Q-factor to force a sinusoidal output current at the fundamental frequency.

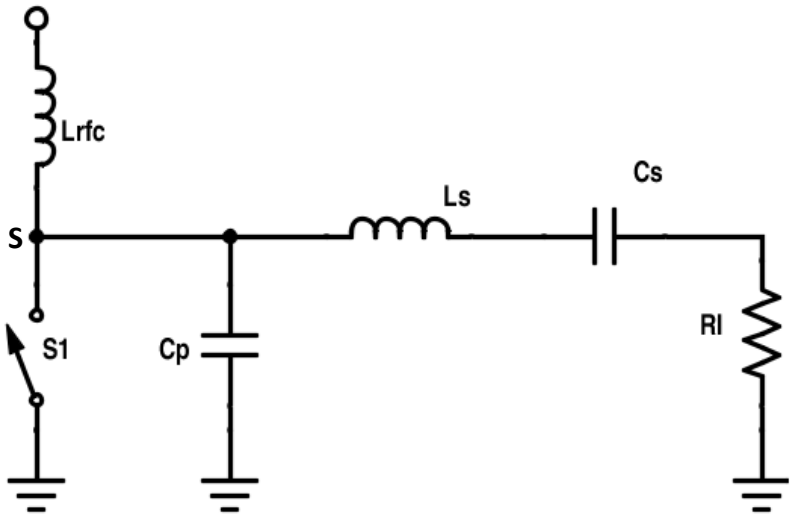



Figure 11: Ideal Class E amplifier

Consider the voltage and current waveform illustrated in figure 10. It is clear from the figure that the non-zero voltage and current never coexist. It is the direct effect of using an ideal switch as active component. This concept is defined by three principle objectives:

- When the switch opens, the drain voltage should not rise until the transistor is completely OFF.
- When the switch closes, the drain voltage should be zero before the drain current starts to rise.
- When the switch closes, the slope of the drain voltage should be zero.

As for the circuit analysis, it continues with the idea that the output current waveform is nominally phase shifted. Then the current through the switch-capacitor combination is [17],

$$I_{sc} = I_{dq} - I_{out}\sin(\omega t + \varphi) \qquad (5)$$

where $I_{sc}$ is the current flows through the switch when it is closed and through $C_p$ when it is opened. $I_{dq}$ is the actual drain current drawn from the power supply. $I_{out}$ is the output current through the load. **φ** is the phase shift of the output current waveform.

The voltage at node 's' is determined by the charging of capacitor $C_p$, when the switch is OFF.

$$V_{sc} = \frac{1}{\omega C_p}\int_0^{\omega t} I_c d(\omega t) \qquad (6)$$

Here, $I_c$ is the current through the capacitor $C_p$, when the switch is closed. Since, each element in the circuit is lossless except for $R_l$, there is no DC power dissipated as heat. All is converted to RF energy that makes the way to the load. The DC input power and RF output power are given by [17],

$$P_{out} = \frac{V_{dq}^2}{R_{dc}} \tag{7}$$

$$P_{in} = \frac{1}{2}\frac{V_{out}^2}{R_l} \tag{8}$$

where $R_{dc} = \frac{(1+\frac{\pi^2}{4})R_l}{2}$. Substituting $R_{dc}$ into equations (7) and (8) leads to

$$P_{out} = P_{in} = \frac{2V_{dq}^2}{(1+\frac{\pi^2}{4})R_l} \tag{9}$$

Taking the ratio of $P_{in}$ to $P_{out}$ gives a drain efficiency, $DE$ = 100%.

It is important to choose the right device technology in this case. If the goal is to maximize output power, then peak drain voltage and current outing must be known during device selection. The physical nature of AlGaN/GaN heterostructure consents high sheet charge density in the conducting 2DEG. It also authorizes the device to dispute a high critical electric field. The AlGaN/GaN can undergo high voltages whilst generating high RF current. This makes it as an ideal choice for this work.

### 2.3.3.2 Class E operation

The output matching network in a Class E power amplifier performs three important tasks:

- In order to minimize the switching loss in the circuit, the output matching network shapes the voltage and current pulses in the required format.
- To increase the switching speed, it allows the transistor's zero voltage turn ON condition, while reducing the equivalent input capacitance.
- To act as a harmonic filter to eliminate harmonic loss in the load.

The unique property of Class E operation is the switch closes when the voltage across $C_p$ (Figure 11) has a zero value. This means that the capacitor is empty at the moment when it is shorted. It allows avoiding the instantaneous discharge through the switch and eliminating the switching loss. At the same time, the current through $C_p$ also has zero crossing. This characteristic of the amplifier contributes to a relatively insensitive Class E amplifier efficiency to the output impedance variation. The closed form time domain expressions for the voltage and current of the transistor can be found by putting the following initial conditions [17]:

$$V_{sc}(t)|_{t=\frac{T_s}{2}} = 0; \qquad \frac{dv_{sw}}{dt}|_{t=\frac{T_s}{2}} = 0 \qquad (10)$$

The optimal Class E output impedance can be found by performing Fourier transformation of these two waveforms and taking the ratio between their fundamental components.

The input RF signal controls the switching state of the amplifier, which is the only information transferred between input and output of this kind of amplifier. This characteristic makes Class E power amplifiers suitable for amplification of constant envelope signal such as FM. Different other techniques such as EER, Chirex outphasing etc. are available to further extend their applicability to signals with variable envelope.

### 2.3.3.3 Class E at Microwave Frequencies

In ideal situation or in low frequency case where parasitic effect can be ignored, specific design equations can be used to design a successful and fully operational class E amplifier. In case of microwave frequencies, device parasitics have to be included in the design. The range of allowable voltages that exist across the drain and source terminals of the device is the fundamental difference between conventional power amplifiers and class E amplifier. The effect of knee voltage of the transistor is particularly important on acquiring high efficiency operation. When operated as a high impedance current source, the device never enters the triode region during conduction, but operating as a switch, the drain-source voltage must be as low as possible requiring traversal into the triode region during part of the RF cycle. In practice, the actual efficiency reduction occurs with the combined power dissipation in this finite ON-resistance as well as in the drain and source resistances. The microwave power amplifier in this thesis was implemented with transmission lines in order to reduce insertion loss.

The Class E power amplifier has been discussed so far under the consideration that the transistor only switches between two discrete states, ON and OFF. It is considered that the gate of the transistor is driven with an ideal square wave. Sokal covered gate driving circuit and method in his paper [26]. Using a large amplitude sinusoidal voltage in the absence of a driving circuit or the unavailability of a high frequency square wave generator is a common practice to overdrive the input of a switching power amplifier. The sinusoidal driving power ($P_{sw}$) required to completely switch the device is a function of the gate-source voltage ($V_{gsw}$) needed to switch the gate, the input capacitance ($C_{gs}$), and the switching frequency ($f_{sw}$). Equation (11) combines all of these parameters [26].

$$P_{sw} = C_{gs} V_{gsw}^2 f \qquad (11)$$

When selecting the right device technology, it is important to consider that parasitic capacitances irreversibly hang up an upper limit on the frequency permissible for Class E operation. The maximum frequency ($f_{max}$) is derived in this case [26] as

$$f_{max} = \frac{I_{max}}{56.5 C_{dso} V_{dq}} \qquad (12)$$

$I_{max}$ represents the maximum current handling capability of the active device. $C_{dso}$ is the output capacitance of the transistor.

## 2.4 Conclusion

Class A power amplifier is the most linear of all amplifier types. It can be used where linearity is the major issue. Class AB is a compromise between Class A and Class B. Switched-mode Classes of amplifiers are the more efficient, while behaving as highly nonlinear. Class E Power amplifier was chosen for this work because of its simple design and scope to improve the biasing network.

# Chapter 3

# Literature and Technology review

## 3.1 Literature Review

Power amplifiers are the most power consuming blocks in wireless communication system. Wireless spectrum are expensive and newer technologies demand maximum amount of data transmission with minimum spectrum usage. It is therefore critical to maximize the power added efficiency while minimizing the number of off-chip components for any radio frequency transmission system, especially for portable and space-borne wireless applications where the battery and the overall system sizes must be small [30-33]. A significant amount of researches have been conducted to date regarding the enhancement of power amplifier performances for WiMAX standard. Following is a brief overview of some of the best reported researches.

### 3.1.1 Doherty PA for mobile WiMAX

Most of the modern wireless applications such as WiMAX use non-constant envelope modulation with high peak to average ratio. Power amplifiers implemented in such applications are forced to operate at backed off region from saturation. Linearity is also a critical issue here.

A technique for wider range of output was proposed in 1936 by W.H Doherty to improve the drain efficiency of power amplifiers like class A or class AB [36-38]. The Doherty amplifier consists of two amplifiers, the main amplifier and the peaking amplifier. Their parallel combination enhances the power added efficiency of the main amplifier at 6dB back off from the maximum output power. A power amplifier for mobile WiMAX application in 2.5~2.7 GHz has been presented in [36]. The power amplifier used a 2 μm InGaP/GaAs HBT process. Broadband input and output matching techniques were used for broadband Doherty operation. A 1.5 times larger peaking amplifier than the carrier amplifier was used to get high efficiency for mobile WiMAX signal. The signal has 9.6 dB crest factor and 8.75 MHz bandwidth. Crest factor indicates how extreme the peaks are in a waveform. The power amplifier with a supply voltage of 3.4V achieved an EVM of 2.3%, PAE of 31.5% and output power of 24.75 dBm at an operating frequency of 2.6 GHz. A PAE of over 30.3% and an output power of over 24.6 dBm with an EVM lower than 3.15% and a gain variation

of 0.2 dB were achieved across 2.5~2.7 GHz without any assistant technique for linearization [36]. Figure 12 shows the performance of the designed amplifier. Table 2 summarizes the achievements of this work.

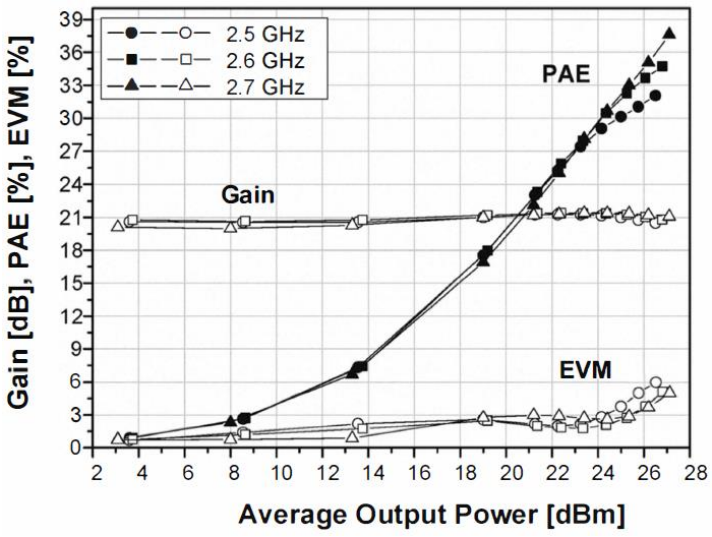



Figure 12: Measured performance of the power amplifier designed in [36]

Table 2: Achievement of Doherty PA for mobile WiMAX application [36]

| **Operating frequency** | **Device Technology** | **Output power (Measured)** | **Efficiency (Measured)** |
|---|---|---|---|
| 2.5~2.7 GHz | InGaP/GaAs | 24.6 dBm | 30.3% |

## Limitations:

The primary concern in the Doherty technique is the RF bandwidth limitation caused by the λ/4 transformer. This makes the technique limited to a single frequency or single band operation. In addition, the required area of the Doherty amplifier is greater than the other amplifier types due to the use of two transistors. These two transistors need two different types of biasing circuitry [37]. As a result, the area requirement increases in this technique.

### 3.1.2 Class E PA with Envelope tracking

A class E power amplifier is easier for monolithic integration compared with class F power amplifier. It is arguably the most efficient class of power amplifier if the optimal switching conditions can be met to minimize power dissipation in the device and theoretically achieve 100% PAE [17]. Unfortunately switched mode power amplifiers are highly nonlinear. Therefore, linearization techniques using envelope elimination and restoration (EER) or envelope tracking (ET) architectures are often needed to accompany class E power amplifiers to meet this tight linearity requirement.

A monolithic SiGe class E power amplifier with an open loop envelope tracking technique for mobile WiMAX application was developed in [39]. One-stage and two-stage class E power amplifiers were designed in 0.18 µm BiCMOS SiGe technology [39].

The one-stage class E power amplifier achieved peak power added efficiency of 62% at output power of 21 dBm in single-tone measurement. The design of linear-assisted switching envelope amplifier involved balancing and trade-offs between efficiency and signal fidelity. Detailed co-design system simulations including RF circuits and digital DSP blocks showed that the designed class E power amplifier can be linearized by the open-loop envelope tracking based transmission system meeting the stringent 802.16e TX mask with ~33% overall average efficiency at output power of 18.5 dBm. However, this work did not show any improvement in the class E configuration, rather it uses one extra efficiency improvement technique. Figure 13 shows the simplified circuit schematic while Table 3 summarizes the achievements of this work.

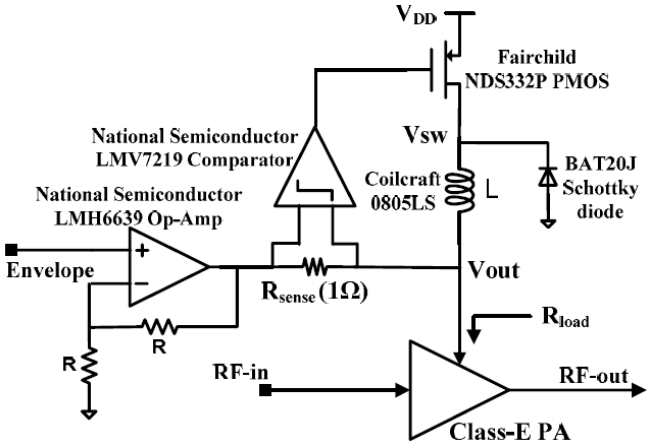



Figure 13: Simplified circuit schematic of the amplifier [39]

Table 3: Achievement of Class E power amplifier with Envelope tracking [39]

| **Operating frequency** | **Device Technology** | **Output power (Measured)** | **Efficiency (Measured)** |
|---|---|---|---|
| 2.3~2.4 GHz | SiGe | 18.5 dBm | 33% |

## Limitations:

Additional linearization technique requires more area by means of extra circuitry. Envelope tracking technique has been applied mainly to current-mode power amplifiers. In case of switched mode amplifiers, it faces some compatibility issues. In case of using SiGe monolithic at ~2.3 GHz, the effect of parasitic bondwire inductance at the emitter node to ground is significant [39].

### 3.1.3 CMOS PA for WiMAX application

With the rapid growth of wireless technology, the demand is never-ending for the higher integrations of wireless transceivers to achieve low-cost, low power, and enhanced functionality [40]. Thus, a single-chip radio transceiver system is increasingly required for having System-on-Chip (SOC) using CMOS technologies. With the advancements of CMOS technologies, more low-cost MOS power amplifiers of SOC have been introduced and demonstrated in some wireless applications, such as wireless LAN and Bluetooth [41]. With the help of the CMOS scaling, the performance of a CMOS single-chip radio transceiver system has potential possibility to compete with those of RF circuits using BiCMOS, GaAs, and SiGe technologies. However, it is still a great challenge to integrate a high-performance power amplifier for the use in future RF WiMAX applications.

In [40], a radio frequency class A power amplifier for WiMAX application using TSMC 0.18 μm CMOS technology was described. A novel two-stage cascode common-source amplifier and a load-pull output matched power amplifier were designed for the WiMAX application of 2.5 GHz transmitting frequency. Figure 14 shows the schematic of the designed CMOS power amplifier. The designed power amplifier exhibited 19.8 dBm of 1-dB compression point, 24.1 dBm of output power, 35% power added efficiency and 23.3 dB of power gain under 3.3 V and 1.8 V supply

voltages. The power consumption was about 827.34 mW. A small sized chip of 0.81x0.65 $mm^2$ was achieved with all matching networks. Table 4 summarizes the achievements of this work.

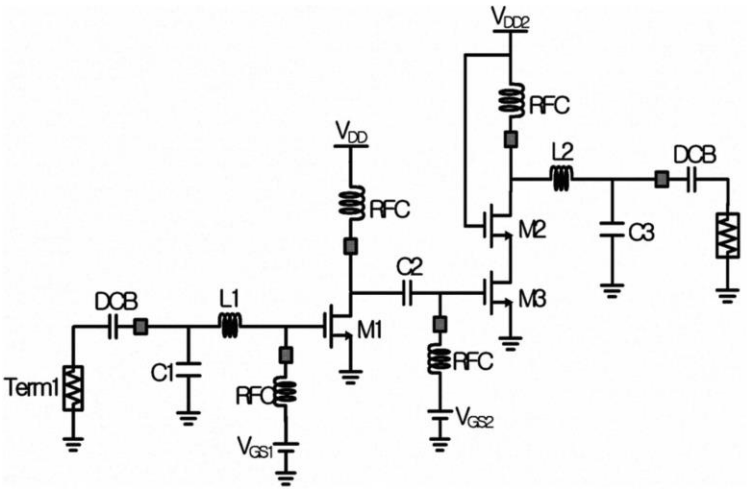



Figure 14: Schematic of the CMOS power amplifier [40]

Table 4: Achievement of CMOS power amplifier for WiMAX application [40]

| **Operating frequency** | **Device Technology** | **Output power (Simulated)** | **Efficiency (Simulated)** |
|---|---|---|---|
| 2.5 GHz | CMOS | 24.1 dBm | 35% |

## Limitations:

Class A topology was applied in designing the power amplifier module. Class A is the least efficient of all classes of amplifiers but most linear one. In case of designing highly efficient power amplifier for WiMAX station, class A is not a good choice.

### 3.1.4 Dual band Class E PA for WCDMA/WiMAX

As the ongoing development of wireless systems tends to diverge in many different directions, mobile devices are more and more required to operate in multi-modes to allow roaming across different systems. Therefore, multi-band and multimode designs of RF components and subsystems have become rather popular because they can reduce component counts and system complexity. So far, power amplifiers still encounter serious technical problems in this design

aspect. The prior designs used switched or dual-band output matching networks for linear PAs to operate in two different bands [42, 43]. However, those dual-band designs are usually at the expense of adding circuit complexity and potential instability to the linear PAs. Besides, there is an inherent trade-off between linearity and efficiency in linear PA design. Generally, power back-off is the most common approach used to prevent the nonlinear effects of linear PAs. For a high PAPR system, the power back-off value must be increased accordingly to avoid signal distortion. Unfortunately, the linear PA's efficiency peaks only when it operates near saturation and drops rapidly as the output power decreases.

A highly efficient but nonlinear class E power amplifier applied to a dual-mode RF transmitter for WCDMA/WiMAX systems was designed in [42]. At first, a class E power amplifier design was carried out for dual band operation based on the proposed modified class E condition. Then, the Envelope tracking and digital pre-distortion techniques were applied to linearize the class E power amplifier by improving the PA AM/AM and AM/PM distortions. The designed class E power amplifier, although classified as a switching-mode PA, can act as a linear power amplifier for diverse high PAPR wireless systems. The experimental results showed that a quadrature modulation transmitter incorporating the presented envelope-tracking dual band class E power amplifier could simultaneously achieve high average efficiency and adjacent channel power rejection for 1.95 GHz WCDMA and 2.6 GHz WiMAX applications [42]. However, the bias was applied in the conventional way. This work did not show any improvement on the biasing network. Figure 15 depicts the power added efficiency of the dual-mode power amplifier for WCDMA/WiMAX. Table 5 summarizes the achievements of this work.

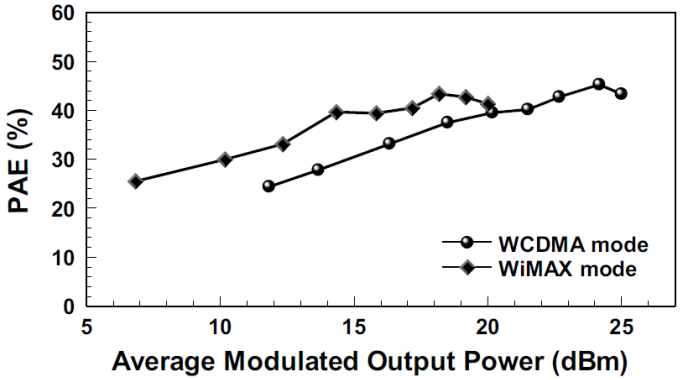


Figure 15: Measured PAE of the implemented dual-mode power amplifier [42]

Table 5: Achievement of Dual band Class E power amplifier for WCDMA/WiMAX [42]

| **Operating frequency** | **Device Technology** | **Output power (Measured)** | **Efficiency (Measured)** |
|---|---|---|---|
| 1.9/2.5 GHz | GaAs | 6.4-21.6 dBm | 25-43% |

## Limitations:

The dc feed chokes were replaced with finite valued inductor. The finite dc feed inductance is, in effect, approximately in parallel with output capacitance, and can be reduced as reducing the amount of output capacitance, hence reducing the output power.

### 3.1.5 SiGe BiCMOS PA for WiMAX

Recently, worldwide interoperability for microwave access (WiMAX) wireless communication system has been gradually popular in wireless communication market. This technology provides not only point-to-point (PTP) and point-to-multipoint (PMP) message services; it can also offer a high data rate and long transmission distance. Power amplifier is one of the key components in mobile communications. It needs some characteristics, such as high output power, high linearity and high power added efficiency (PAE). In the past, such implementations were predominantly made in more expensive compound semiconductor technology like Gallium Arsenide (GaAs) and Indium Phosphide (InP). The SiGe-heterojunction bipolar transistor (SiGe-HBT) technology became popular in microwave applications due to its characteristics of low power consumption, high integration level, and low cost than GaAs and InP [45]. Many papers on SiGe technologies of power amplifiers have been published. A power amplifier operating at 3.5 GHz for WiMAX application was designed in [44]. The TSMC 0.35 μm SiGe BiCMOS technology was used in this design. The choice of using SiGe BiCMOS technology for this design was based on its better breakdown robustness than CMOS and Si BJT, its technology availability and maturity, and its single chip integration potential with multi-million gate digital CMOS. The power amplifier was designed with two stages as shown in Figure 16.

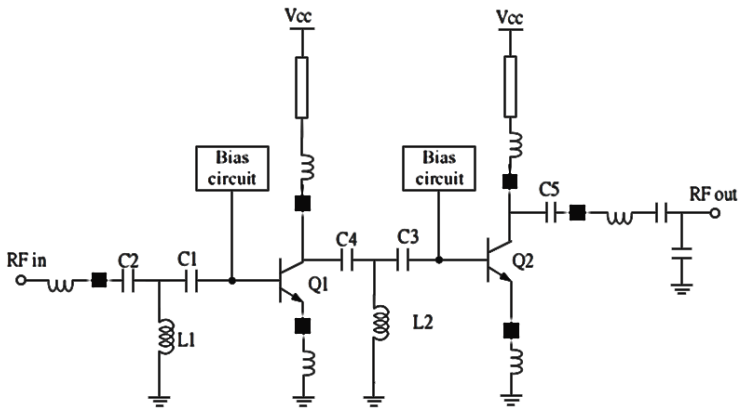



Figure 16: Schematic of the two-stage power amplifier [44]

The results demonstrated that it could provide a reasonable efficiency, linearity and good output power. The output 1-dB compression point $P_{1dB}$ was 22.1 dBm at operating frequency of 3.5 GHz. A reasonable PAE of 44.5% was obtained. The supply voltage of the power amplifier is 3V and the quiescent power consumption is 220 mW. The power amplifier achieved 24.1 dBm of power gain and 23.7 dBm of maximum output power. Table 6 summarizes the achievements of this work.

Table 6: Achievement of SiGe BiCMOS power amplifier for WiMAX [44]

| **Operating frequency** | **Device Technology** | **Output power (Simulated)** | **Efficiency (Simulated)** |
|---|---|---|---|
| 3.5 GHz | SiGe | 23.7 dBm | 44.5% |

### Limitations:

It is a two-stage power amplifier. Additional stage needs extra area in terms of extra circuitry.

## 3.2 Technology review

Transistor technology for microwave operation has evolved over the ages from the basic metal-semiconductor field effect transistor (MESFET) to modern high performance III-V and wide bandgap high electron mobility transistors (HEMTs). This section tries to go through the transistor technology to understand the usefulness in high performance microwave operation.

### 3.2.1 MOSFETs and HEMTs

Today's emerging wide bandgap semiconductor includes AlN, SiC, AlGaN etc. [46]. They are well known and well established for their high frequency performance. III-V HEMTs such as GaAs and InP also offer high frequency performance, but they pay for low power densities compared to the wide bandgap technology. The Si LDMOSFET technology is used in most modern base station microwave power amplifiers [47]. It supports higher breakdown voltages, but upper limit of parasitic capacitance at more than 3 GHz risks the usefulness of this technology [22].

Typical HEMT consisted of AlGaAs/GaAs heterostructure [48]. That is why it also known as Heterostructure FET (HFET). The two-dimensional electron gas (2DEG) is the defining feature of HEMT structures. This feature provides high carrier mobility for the transistor, but to qualify a device with superior microwave performance this feature alone is not enough. Good electron confinement with 2DEG sheet charge density ($\eta_s$) is another necessary requirement for high frequency operation. The HEMT heterostructure does not have a large enough conduction band offset to fulfill this requirement [48, 49].

Advancements in material systems such as lattice-matched heterostructures on InP with InGaAs channel layers can provide larger conduction band offsets, which can simplify the higher frequency operation. This advanced heterosructure with InGaAs offers conduction band offset as high as 0.66 eV compared to 0.22 eV for GaAs [49]. As a result, InP devices can support $\eta_s$ and low-field carrier mobility two to three times higher than that of GaAs devices [50]. This allows the InP HEMTs to attain record cut off frequencies ($f_T$) of 340 GHz and maximum frequency of oscillation ($f_{max}$) of 600 GHz [51, 52].

Power capability is another important matter of concerns besides the frequency of operation for microwave devices. InP devices show a reduced output power level of at least two comparable frequencies. Currently the largest market share in commercial base station power amplifiers is held by Si LDMOSFETs. This technology offers high output power and breakdown voltages in the range of 20 V to 40 V up to 3 GHz at much lower cost [53]. It offers $f_T$ and $f_{max}$ anywhere between 5 GHz and 15 GHz. Until now, single Si LDMOSFETs with up to 220 W of output power at 2 GHz have been reported in [54]. The trade-off is ascertain between speed and breakdown voltage. In case of modern small sized devices, the gate length becomes shorter to achieve higher $f_T$, which

results from the reduced physical space between gate and drain. It helps the device to support a larger gate-drain electric field.

### 3.2.2 Comparison: Conventional and Wide bandgap HEMTs

Wide bandgap transistors, especially AlGaN/GaN HEMTs are the rising technology for both high frequency and high power operation at larger power densities than existing III-V semiconductors. Figure 17 shows the typical AlGaN/GaN physical structure. A high purity 2DEG caused by the Al content in the AlGaN is formed at the hetero-interface towards the GaN layer. The sheet charge density in the AlGaN/GaN is $10^{13}$ $cm^{-2}$ which is five times higher than AlGaAs/GaAs system with 2DEG electron densities at around $2*10^{12}$ $cm^{-2}$ [55]. All these characteristics, such as high electron mobility, high electron saturation velocity and the ability to support high breakdown electric field, allow AlGaN/GaN HEMTs to deliver high RF power levels at high frequencies.

Table 7 presents some of the key material properties of Gallium Nitride (GaN) compared to Silicon (Si), Gallium Arsenide (GaAs) and the most common Silicon Carbide (SiC) crystal structure. The thermal conductivity of the wide bandgap materials is higher than the others. This makes them most attractive for base station application. The reliability of these materials at higher temperatures can reduce a huge cost associated with the cooling equipment in the base stations.

Table 7: Material properties of Si, GaAs, SiC and GaN [55]-[57]

| **Parameter** | **Si** | **GaAs** | **SiC** | **GaN** |
|---|---|---|---|---|
| Energy gap (eV) | 1.11 | 1.43 | 3.2 | 3.4 |
| Breakdown field (V/cm) | $5.7*10^5$ | $6.4*10^5$ | $3.3*10^6$ | $3.8*10^6$ |
| Electron mobility ($cm^2$/Vs) | 1350 | 6000 | 800 | 1600 |
| Electron peak velocity ($10^7$ cm/s) | 1 | 1.8 | 2 | 2.5 |
| Thermal conductivity (W/K cm) | 1.5 | 0.46 | 3.5 | 1.7 |

Scientific communities have experienced advancements on the theory and techniques of reliably processing GaN on various substrates within the last twenty years. SiC, Sapphire and Si are among

the substrates. Currently GaN grown on SiC substrate is the most common among the GaN based microwave circuits [57, 58]. The fundamental reason behind using SiC is the property of thermal conductivity. It is more thermally conductive than Si and GaAs. Moreover, the superior 2DEG electron confinement is achieved by the energy gap at the hetero-interface. As a result, AlGaN/GaN-on-SiC HEMTs have shown excellency in providing high frequency performance and record power densities.

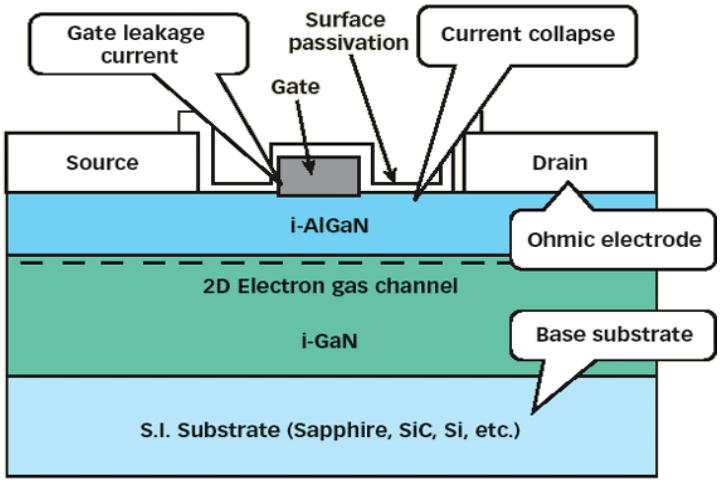



Figure 17: Cross section of a typical GaN HEMT [59]

Table 8 presents a comparison of some of the best cut-off frequencies reported for AlGaN/GaN, AlGaAs/GaAs, and InP HEMT devices. Study showed an InGaN intermediate layer grown on top of the GaN buffer layer on SiC to enhance electron confinement in the 2DEG. It effectively increases the $f_T$ to a record of 153 GHz and the $f_{max}$ to 230 GHz [60].

Table 8: Best reported $f_T$ and $f_{max}$ [55]-[61]

| **Transistor** | $L_g$ **(μm)** | $f_T$ **(GHz)** | $f_{max}$ **(GHz)** |
|---|---|---|---|
| AlGaAs/GaAs p-HEMT | 0.1 | 113 | 110 |
| InP p-HEMT | 0.05 | 343 | 740 |
| AlGaN/GaN-on-Si p-HEMT | 0.5 | 32 | 27 |
| AlGaN/GaN-on-SiC | 0.1 | 153 | 230 |

Table 9 shows a comparison of some of the best reported power densities for AlGaAs/GaAs, InP, and AlGaN/GaN devices. InP devices are most effective at high frequencies (V-band and W-band) operation. InP HEMTs are well known for their superior channel transport properties and low breakdown voltage. The low breakdown voltage is the direct impact of the Indium (In) content in the channel. As mobile services rushing towards high frequencies, the breakdown levels in both GaAs and InP devices are the major concerns [61, 62].

Table 9: Power performances of transistor technologies [55]-[60]

| **Transistor** | ***f* (GHz)** | $P_{out}$ **(W)** | **PAE (%)** | $P_{density}$ **(W/mm)** |
|---|---|---|---|---|
| AlGaAs/GaAs HEMT | 2.2 | 40 | 35 | 0.37 |
| InP HEMT | 60 | 0.186 | 36 | 0.37 |
| AlGaN/GaN-on-Si HEMT | 2.14 | 1.2 | 52.7 | 12 |
| AlGaN/GaN-on-SiC HEMT | 4 | 8 | 54.8 | 32.2 |

Silicon Carbide (SiC) is the most highly refined bulk substrate nowadays compared to other substrates [57]. It is more thermally conductive than any other substrate. With a power density above 30 W/mm, GaN-on-SiC HEMT is an attractive solution in terms of power, performance and efficiency for the next generation microwave base station systems.

## 3.3 Conclusion

Class E type of power amplifiers have been used for WiMAX application in various researches, most of them focusing on improving the efficiency and output power using different technologies and various efficiency improvement techniques. However, a very few focused on most promising GaN technology and improving the actual Class E circuit. This thesis is not going to use another efficiency technique, since the switched mode itself is an efficiency improvement technique. As detailed in the next chapter, this work presents an improved bias network for class E amplifier circuit while using the most promising GaN technology. This is a rare combination of using GaN technology in Class E power amplifier for the possible application in WiMAX transmitters.

# Chapter 4

# Bias network design

## 4.1 Design requirements

The effect of the bias insertion circuit and the manner in which bias is inserted into the power amplifier is an important design consideration. The DC biasing circuitry has to be properly designed to isolate the DC signal from the RF signal. Proper bias network design is essential for any nonlinear circuit design to ensure that right amount of bias reaches the device and it does not load/leak the desired RF energy [63]. The choice of bias network topology is pretty much dependant on the frequency of operation. For lower frequencies, designers can use inductors/chokes in the DC bias path and for higher frequencies, high impedance quarter wavelength transmission line is the preferred choice.

In [64], the input and output bias networks are considered integral parts of the Class E microwave power amplifier. These are included in every part of the design process. These biasing circuits are designed to interface with a 50Ω system and not to interface with the input and output matching network of the power amplifier.

The bias network can sometimes load the matching network; hence, it is important to consider this impact seriously while designing the network. A power amplifier may not operate at the peak power level all the time. The power amplifier is more likely to be operated in back-off region in case of wireless standards that use non-constant envelope modulation schemes or PA power control. Since the RF output power is reduced, it is desirable to reduce the DC power consumption to increase efficiency under back-off.

### 4.1.1 PA biasing for improved efficiency

The main concerns in selecting the bias scheme for a power amplifier include cost, efficiency, bandwidth, and distortion. The four biasing schemes [65] reported to date are:

- Fixed biasing.
- Dynamic biasing of gate.

- Dynamic biasing of drain using linear regulators.
- Dynamic biasing of drain using switching regulators.

#### 4.1.1.1 Fixed biasing

Biasing a power amplifier with fixed biasing is the most common way of biasing. In this scheme, both the gate and drain voltages are constant. Figure 18 shows the fixed biasing of the device.

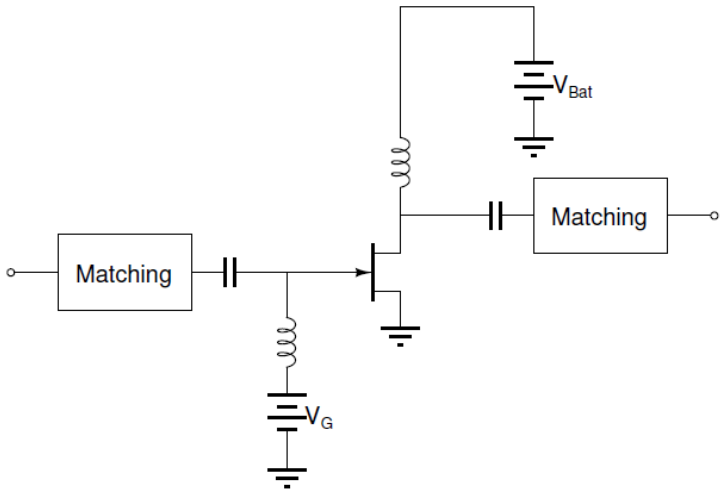



Figure 18: Fixed biasing

The gate is connected to a fixed voltage that defines the quiescent current and the drain is connected to the battery through an RF choke.

#### 4.1.1.2 Dynamic biasing of gate

The quiescent current of the power amplifier is defined by the gate voltage. The quiescent current and the conduction angle are reduced by reducing the gate voltage closer to the threshold voltage. Under power back-off conditions, reducing the gate voltage can increase the efficiency. Figure 19 depicts the configuration of a power amplifier utilizing dynamic biasing of the gate. Any change in gate voltage can considerably change the behavior of the power amplifier. The change becomes significant as the gate voltage approaches the threshold voltage. Another issue is that any change at the gate will be amplified, which makes the noise an important issue when modulating the gate voltage. The major benefit of this configuration is its relatively small size. Since the dynamic biasing circuit does not need to pass through all of the output power, the size of the circuit can be small and can be integrated into the power amplifier MMIC [65].

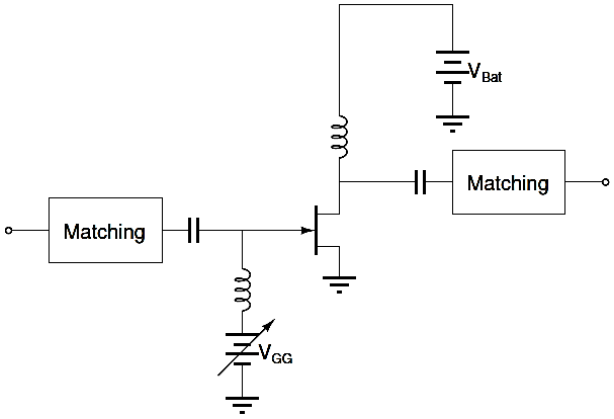



Figure 19: Dynamic biasing of gate

### 4.1.1.3 Dynamic biasing of drain using linear regulators

The load line of the power amplifier is changed by varying the drain voltage. The reduction of the drain voltage causes the RF signal disputing a larger portion of the load line, which leads to higher efficiency. The amplitude distortion and the phase distortion are lower when the drain is dynamically biased instead of the gate. For power amplifiers using dynamic bias of the drain, almost all of the current that flows through the power amplifier must flow through the dynamic biasing circuit. This directs to a bigger sized pass transistor in the linear regulator, which needs to be capable of handling current as in GSM applications with negligible drop-out voltage [65]. Any dropout voltage will directly reduce the maximum output power of the power amplifier at the peak output power level. Figure 20 shows the dynamic biasing of drain using linear regulators.

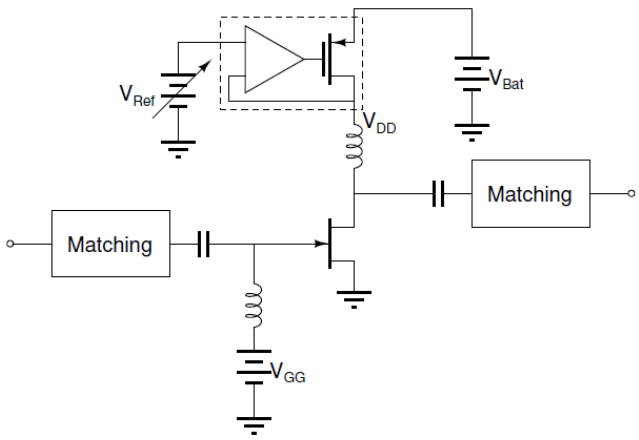



Figure 20: Dynamic biasing of drain using linear regulators

The efficiency of the linear regulator can be approximated as [65]

$$\eta_{LR} = \frac{V_{DD}}{V_{BAT}} \qquad (13)$$

Figure 21 shows that the power amplifier can be modeled as a load to the linear regulator (with a resistor in parallel to a DC current source). The power amplifier resembles a DC current source when it is biased closer to the Class A region. However, the power amplifier load is closer to a resistor when it is operating near saturation. When the power amplifier is closer to a DC current source, reduction of drain voltage with a linear regulator does not increase the efficiency since the DC power consumption remains fairly constant. The overall efficiency can be written as [66]

$$\eta = \eta_{LR}\eta_{PA} \qquad (14)$$

with

$$\eta_{PA} = \frac{P_{out}}{V_{DD}I_{load}} \qquad (15)$$

Now with the help of equations (13) and (15), the overall efficiency is given by

$$\eta \approx \frac{P_{out}}{V_{BAT}I_{DC}} \qquad (16)$$

which is the same as the efficiency of a power amplifier with fixed biasing.

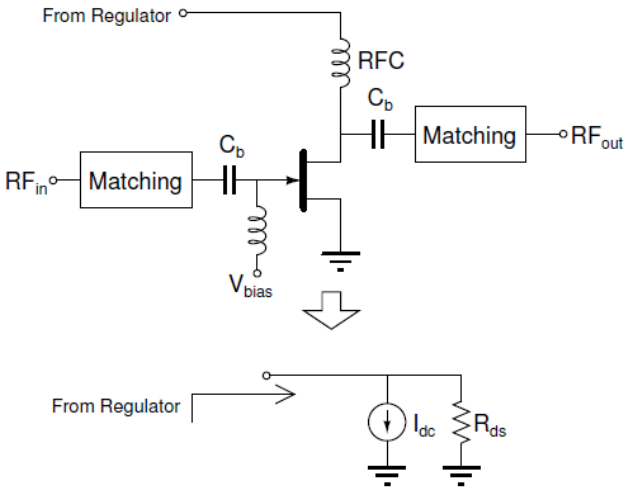



Figure 21: Power amplifier as a load to the regulator

### 4.1.1.4 Dynamic biasing of drain using switching regulators

Linear regulators become lossy when the power amplifier is backed-off from the peak output power. Efficiency can be greatly increased by using a buck-switching regulator instead of a linear regulator. Figure 22 shows the use of switching regulator. The switching regulator suffers from the same problem as in the linear regulator at peak output power level, since the regulator itself has DC loss.

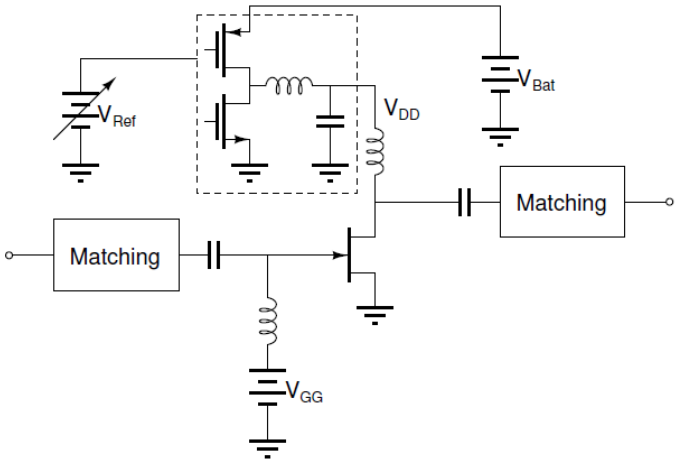



Figure 22: Dynamic biasing of drain using switching regulator

The maximum output voltage of the switching regulator is

$$V_{out,max} = V_{BAT} - I_{load}\left(R_{DS,ON} + DCR\right) \qquad (17)$$

where $I_{load}$ is the load current, $R_{DS,ON}$ is the ON resistance of the transistor and $DCR$ is the DC resistance of the inductor. To achieve the same voltage drop as in a linear regulator, the transistor size has to be larger to reduce $R_{DS,ON}$ and an inductor with lower DC resistance has to be used. Such an inductor is usually larger in size. The large power transistor size usually directs to a larger die size and higher cost, while the large-sized inductor takes up too much board space. Dynamic biasing of the drain using a switching regulator has the best performance among the four biasing schemes discussed here, but its use has been limited because of cost issues.

## 4.2 Previous approaches of biasing circuits

Figure 23 [67] and figure 24 [68] show existing designed biasing circuits of Class E PA. In case of figure 23, the circuit can efficiently cancel the noise. It has an efficient power supply decoupling section. It uses an extra protection resistor to protect the circuit from unwanted electrical fail. However, the network used too many lumped elements as the capacitors and resistors. Using of lumped elements in higher frequencies is not recommended because, at higher frequencies, the size of lumped element components become an appreciable portion of a wavelength. This means that the distribution effects begin to become significant. That is why, using of transmission line in case of designing high frequency circuits is the preferred choice. The circuit of figure 23 also used ferrite bead to suppress the noise. There is resistive loss in ferrite bead. It may cause heat generation, though it is little in portion. This type of beads require much area in the circuit board.

The circuit of figure 24 represents a simple bias network. Much lower area is needed to design this network. However, the circuit design did not consider of using any stability resistor to keep the amplifier stable all the time.

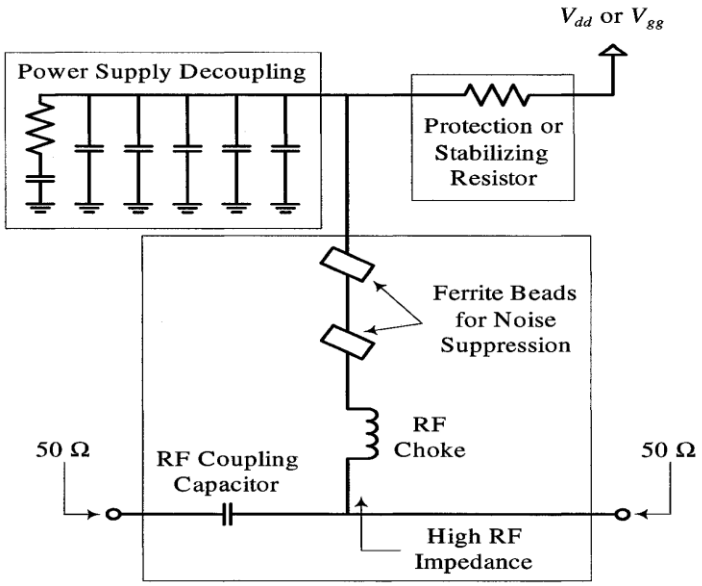



Figure 23: Bias network from [67]

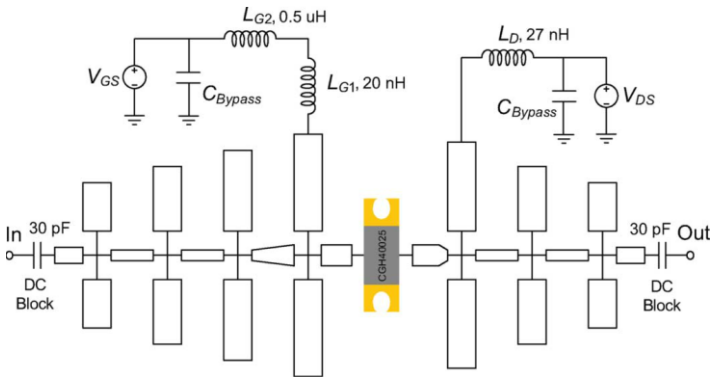



Figure 24: Bias network from [68]

## 4.3 Bias network design using fixed biasing

Power amplification with high efficiency is highly desirable for today's wireless application. Highly efficient switched mode Class E power amplifier design needs accurate voltages for gate and drain to provoke transistor to operate in class E mode. A specific gate voltage is required to obtain drain current and voltage specification of the transistor. Thus, fixed biasing scheme is applied in designing the transistor biasing network. The proper bias point can be found from the transistor polarization curve. Figure 25 shows the I-V curves of the GaN HFET used in this work. The point B is selected as the quiescent point of Class E amplifier. Following steps are followed to select the quiescent point:

- Select $V_{GS}$ curve that provides expected drain current in saturation mode,
- Select a $V_{DS}$ voltage according to the $V_{GS}$ and $I_{DS}$ values obtained in previous step, which is supported for the respective transistor.

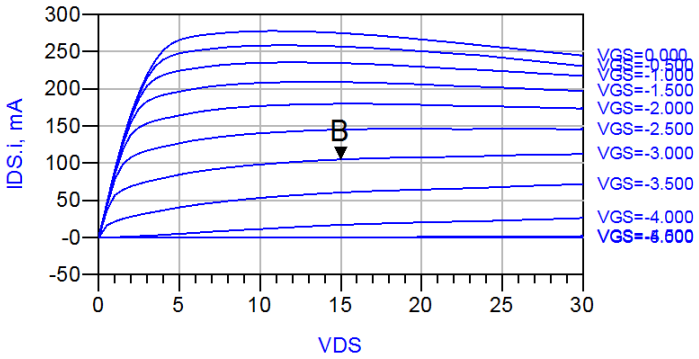



Figure 25: GaN HFET I-V characteristic

The bias insertion networks at the input and output side of the transistor are basically similar. The only differences are in the stabilizing elements and in the tolerances of the components used. The complete realization of the biasing unit includes:

- Input bias section.
- Output bias section.
- Gate bias section.
- Drain bias section.

The RF signal will enter the transistor gate through the input bias section of the network. This section will ensure the entrance of the input RF signal without any disturbance and/or noise. The gate voltage is provided through the gate bias section. This section protects the gate voltage from any unwanted noise signal. The drain bias section helps the supply voltage to reach the drain of the transistor with a high quality factor inductor as RF choke. Output bias section assists the output signal from the transistor. This section designed with LC filter makes sure that only the fundamental component of current and voltage goes out of the transistor.

### 4.3.1 Input bias section

This section is for the input side of the bias network. As shown in figure 26, this section includes a capacitor $C_1$, a resistor $R_1$, a taper $Taper_1$ and transmission lines.

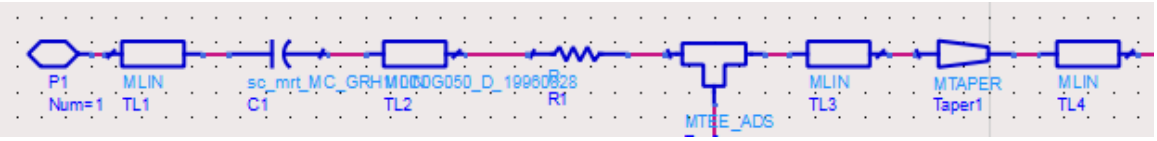



Figure 26: Input bias section

The series capacitor $C_1$ acts as a DC blocking component. It prevents the flow of audio and DC components, while offering minimum interference to RF signals. This kind of capacitor has the advantage that it is nearly invisible to higher frequencies. The capacitance has to be increased to pass frequencies down to 1 MHz, which makes them the perfect DC blocking component. Surface-mount technology (SMT) capacitor is used in this case. This type of technology has much higher component density and many more connections per component. It has lower initial cost and time of setting up for production. SMT components are simpler and faster in automated assembly than the regular ones.

The resistor $R_1$ is used as the stability resistor. It prevents the device from being unstable in the desired frequency range. The value of the resistor has to be tuned to achieve the device stability.

Microstrip taper is used for providing gradual transition to 50Ω impedance line. In the microwave frequency range and for a substrate with a permittivity comprised between 2 and 10, the both widths of the taper are usually close and a quarter wavelength taper is sufficient to obtain a good return loss. In any case, the taper length must be chosen as a multiple of a quarter of a wavelength in order to minimize the return loss.

### 4.3.2 Output bias section

This section is designed for the output side of the bias network; it is basically the load network for Class E amplifier. In this unique design, this section serves both the purposes of Class E lumped element load network and the output bias insertion unit. This section includes a shunt capacitor $C_2$, a series inductor $L_1$, a series capacitor $C_3$ and transmission lines, as shown in figure 27.

The output bias circuit includes the components similar to the typical Class E load network. Capacitor $C_1$ is parallel to the drain of the active device. It makes the way of the current to the ground when the switch is OFF. The drain voltage waveform is the result of the sum of the DC and RF currents charging the drain-shunt capacitance $C_2$, which is parallel with the transistor internal capacitance $C_o$. In case of optimum Class E, the drain voltage drops to zero and has zero slope just as the transistor turns ON. The transistor output capacitance $C_o$, and hence $C_2$, is independent of voltage. It results a high efficiency operation, eliminating the losses associated with charging the drain capacitance. It also helps reducing the switching losses and provides good tolerance to component variations.

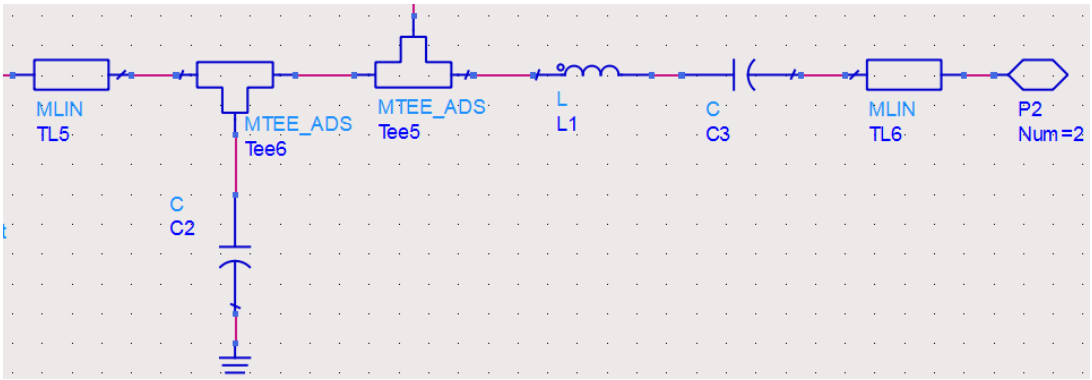



Figure 27: Output bias section

The capacitor $C_3$ and inductor $L_1$ makes a filter at the output of the device. The $Q$ of the output circuit consisting $L_1$ and $C_3$ is high enough so that the output current and output voltage consist of only the fundamental component. The class E amplifier exhibits an upper limit on its frequency of operation based on the output capacitance required for the output matching circuit that produces the class E waveforms. In order to achieve this, the class E amplifier requires an upper limit on capacitance $C_3$ for optimum efficiency. This $C_3$ requirement implies that for high power at high frequencies, higher current densities are required, as the cross-sectional area of the switch corresponds directly to the device's intrinsic capacitance.

Fourier analysis of Class E load network gives an expression for the fundamental component of the voltage ($V_{SC}$) across the switch $S_1$ in figure 11. This voltage, divided by the RF current in the load network, gives the RF phasor impedance as a function of switching angular frequency ($\boldsymbol{\omega}_s$) and shunt capacitance ($C_p$),

$$Z_E \approx \frac{0.28015}{\omega_s C_p} e^{j49.0524^\circ} \qquad (18)$$

keeping in mind that $C_p$ is intended to be solely composed of the HFET's output capacitance. The Class E load network consists of lumped elements and the output bias insertion circuit is assumed not to affect the RF performance of the whole unit. The output bias circuit is effectively indiscernible to the transistor. The transistor actually experiences the circuit in figure 28.

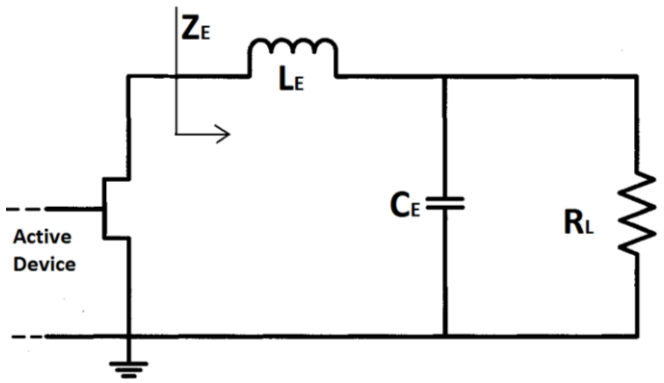



Figure 28: Transistor view to the output without facing issues due to output bias circuitry.

The input impedance of the load network is given by,

$$Z_E = j\omega_s L_E + \frac{R_L}{1 + j\omega_s C_E R_L} \tag{19}$$

Equating (18) and (19) gives the expressions for $L_E$ and $C_E$:

$$L_E = \frac{k_0}{\omega_s^2 C_p}\left(\sin\theta_0 + \cos\theta_0 \sqrt{\frac{\omega_s C_p R_L}{k_0 \cos\theta_0} - 1}\right) \tag{20}$$

$$C_E = \frac{1}{\omega_s R_L}\sqrt{\frac{\omega_s C_p R_L}{k_0 \cos\theta_0} - 1} \tag{21}$$

where $k_0$ = 0.28015, $\theta_0$ = 49.0524°, $R_L$ is the load resistance and $C_p$ is the required shunt capacitance with the output of the active device. Independent variables such as $\boldsymbol{\omega_s}$, $R_L$, $C_P$ from equations (20) and (21) can be chosen independently.

### 4.3.3 Gate bias section

This section is designed to assist the gate biasing signal. The supplied gate voltage reaches the gate through this section. According to figure 29, this section includes capacitor $C_4$, inductor $L_2$, resistor $R_2$ and transmission lines.

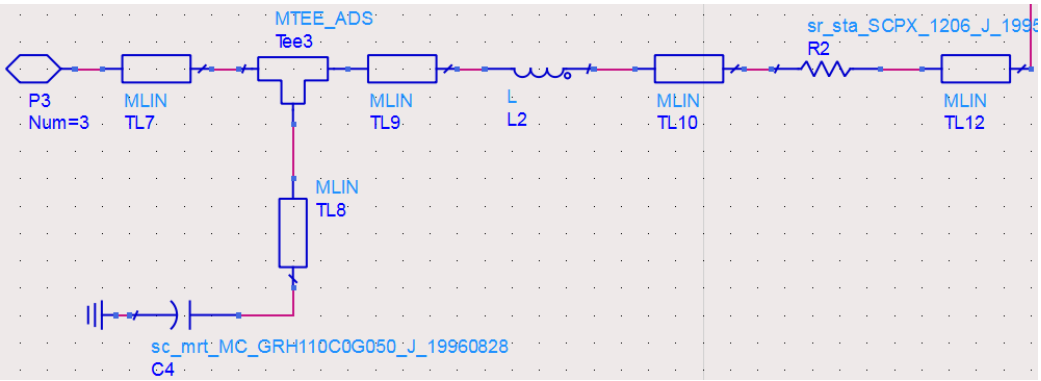



Figure 29: Gate bias section

Capacitor $C_4$ is used here as a bypass capacitor. Its goal is to short AC signal to ground, so that any AC noise that may be present on a DC signal is removed. This capacitor blocks the DC from entering it by the high resistance it offers to the signal but accepts the AC noise that may be on the DC line and shunts or bypasses it to ground.

Inductor $L_2$ acts as a DC bias choke in this section. It is used to block higher frequency alternating current (AC) in the circuit, while passing lower frequency or direct current (DC). The chokes impedance increases with frequency. Its low electrical resistance passes both AC and DC with little power loss, but it can limit the amount of AC due to its reactance. Series resistor $R_2$ is used as a stability resistor in this section. SMT component is used in this case for better performance. The stability of the device can be control by controlling this resistance.

### 4.3.4 Drain bias section

This section is designed for the drain biasing purpose. Device's supply voltage $V_{DD}$, enters through this section. This section ensures a clean signal from the power supply. As shown in figure 30, the drain bias section includes a parallel capacitor $C_5$ and an inductor $L_3$.

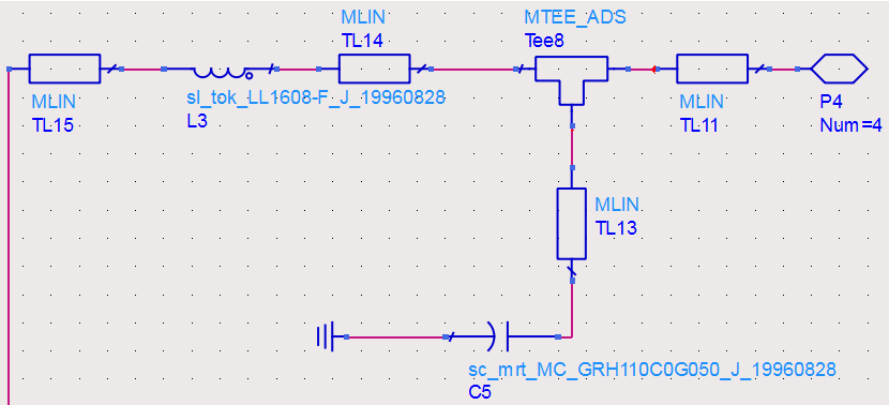



Figure 30: Drain bias section

Capacitor $C_5$ is used here as a bypass capacitor. It shorts the AC signal to ground, so that any AC noise that may be present on a DC signal is removed, producing a much cleaner and pure DC signal.

Inductor $L_3$ is used as the RF choke for class E amplifier. This radio frequency choke (RFC) is large, with the result that only DC current flows through it. The induction of this choke is very high to protect the device's drain terminal from the unwanted AC noise and provide an easy way to the DC signal. SMT inductor is used here as the RFC. It provides better EMC performance (lower radiated emission) due to the smaller radiation loop area (because of the smaller package) and the smaller lead inductance. The layout design of the bias network will be presented in Chapter 6.

## 4.4 PA Stability

Power amplifier stability is a common matter of concerns throughout the design. In the bias network design, small signal stability is clearly enforced with a series resistance in the input bias feed. Extra caution regarding the stability of the design is taken by inserting another fixed valued resistor in the gate bias feed. The same technique is used to restrain transistor burn-out.

Small and large signal stability is checked with the bias insertion circuits integrated into the power amplifier module. The variable stability resistance, *Stab_R*, is placed in series with the input bias feed. Two conditions should be met for the circuit to be stable.

- Stability factor, *k*, must be greater than unity to meet the circuit stability condition. Here,

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \qquad (22)$$

  where $\Delta = S_{11}S_{22} - S_{12}S_{21}$

- Stability measure must be greater than zero.

Figure 31 and 32 show the small and large signal stability curves of the analysis, respectively. In the graphs, stability factor is plotted on the left Y-axis with log scale and the stability measure is plotted on the right Y-axis. It can be noticed that stability factor is more than 1 and stability measure is greater than 0 over the entire frequency range, hence the device is unconditionally stable with the help of stability resistors.

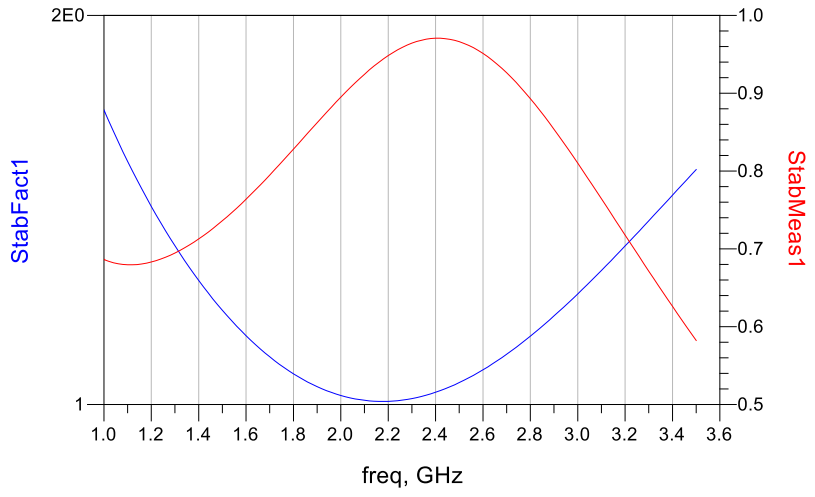



Figure 31: Small signal stability analysis of the device

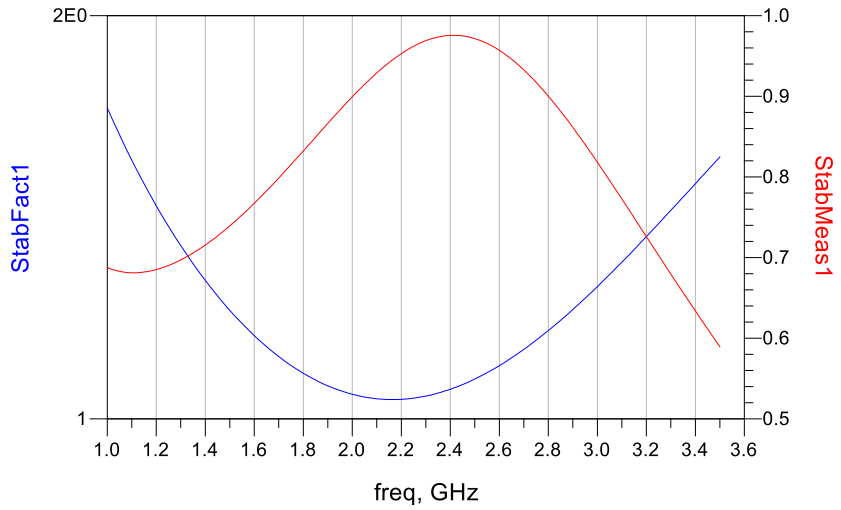


Figure 32: Large signal stability analysis of the device

## 4.5 Conclusion

An improved bias network is introduced for class E amplifier. Two stability resistors are used in the biasing circuit, one of them in series with the gate terminal and the other one in parallel with the gate. High Q-factor DC bias choke is used in the drain terminal and the output network maintains the conventional L-C filter configuration. The power amplifier is unconditionally stable with the newly designed bias network. The complete circuit design proceeds with the improved bias network. Chapter 5 presents the designed highly efficient GaN based Class E microwave power amplifier.

# Chapter 5

# GaN Based Class E Microwave Power Amplifier

## 5.1 Design requirements

High breakdown voltage and high current density of GaN HFETs encourage the design of a Class E microwave power amplifier in this work presented so far. The class E switched-mode concept is not novel. Others have published working class E power amplifiers, but most of them based on GaAs or SiGe technology and a very little on GaN [13, 18, 39, 41, 42]. To the best of the author's knowledge, none of them considered the effect of biasing network and thought deeply in this regard. Perhaps the single most distinguishing feature of the power amplifier in this work is that the active device has the most suitable and efficient biasing network. Another important feature includes the active device has a silicon carbide substrate; a technology that combines the superior performance of GaN with a mass-producible inexpensive substrate.

This chapter evolves a basic lumped element design into a planar transmission line circuit. The degree of 'idealness' is removed as the chapter goes forward, from the circuit simulation until a practical design of each component in the power amplifier is developed. The power amplifier design specifications are established in table 10, along with substrate properties [69, 70].

Table 10: Class E PA specification and material properties

| | |
|---|---|
| Design frequency ($f_1$) | 2.5 GHz |
| Output power ($P_1$) | 2 W |
| Gain | $\geq$ 9.5 dB |
| Power added efficiency ($PAE$) | $\geq$ 40% |
| Drain bias supply voltage ($V_{DD}$) | 15 V |
| Breakdown voltage ($V_{DS\_BD}$) | > 80 V |
| Substrate thickness | 75 µm |
| Dielectric constant | 10 |

## 5.2 Ideal class E power amplifier

The basic Class E power amplifier and its theoretical performance, discussed in chapter 2, is shown again in figure 33.

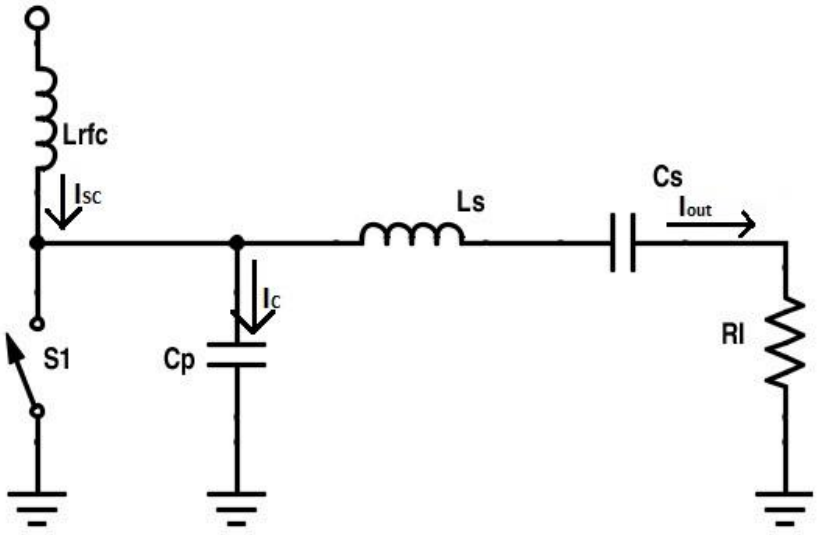



Figure 33: Ideal class E PA used to verify class E operation in simulation

The design is fairly straightforward; requirements include fundamental frequency, device breakdown voltage and loaded Q-factor ($Q_L$). These values help to solve the design equations introduced by N. Sokal [17, 19]. The idealized output power level and circuit elements are computed using equations (23)-(27) for $V_{dq}$ = 15 V, $Q_L$ = 5, and $R_L$ = 50 Ω. The calculation results in $P_{out} = 2.32\ W$, $C_p = 0.27\ pF$, $C_s = 0.34\ pF$, $L_s = 0.15\ nH$, $L_{rfc} = 450\ nH$.

$$\frac{P_{out}R_L}{V_{dq}^2} = 0.51659 \qquad (23)$$

$$C_p\omega_s R_L = 0.20907 \qquad (24)$$

$$C_s\omega_s R_L = 0.26924 \qquad (25)$$

$$L_s = \frac{Q_L R_L}{\omega_s} \qquad (26)$$

$$L_{rfc} = \frac{30}{\omega_s^2 C_p} \qquad (27)$$

Figure 34 shows the simulation spectrum for ideal model. There are instantaneous spikes in current across the switch, at the exact moment when the switch turns ON, which would normally appear as losses across any inductance present between the switch and $C_p$. It has been indicated that, for non-zero output power, at least one such discontinuity per cycle is necessary.

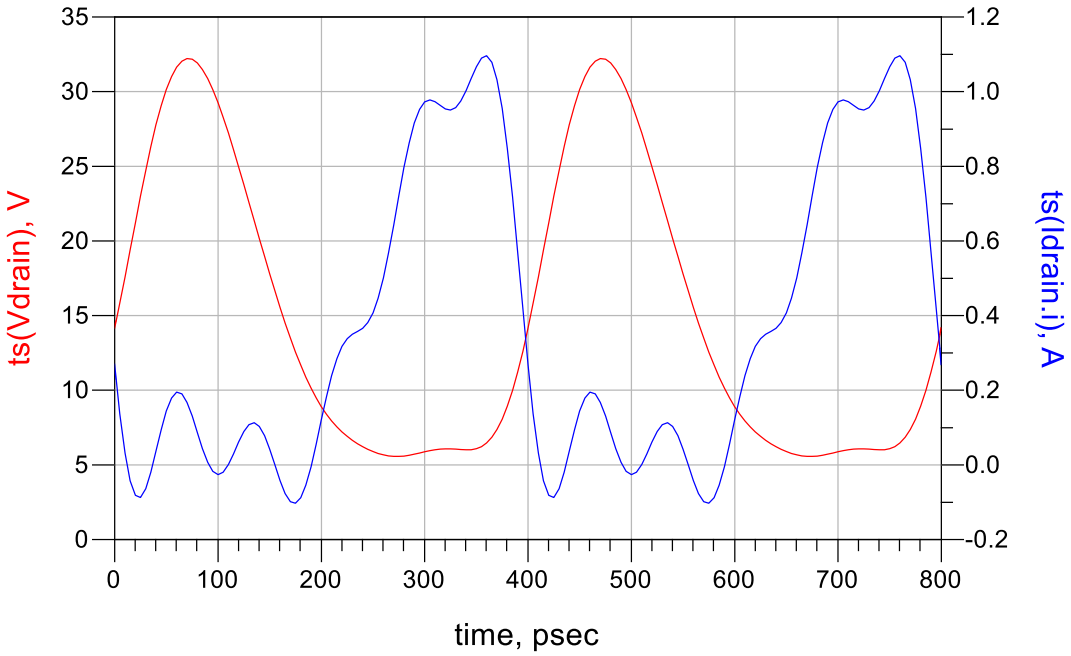



Figure 34: Drain voltage and current waveform of the active device

The ideal class E power amplifier presents a valid design strategy. However, the required class E shunt capacitance is calculated and cannot be chosen independently. The driving waveform is an additional concern. A 2.5 GHz square wave input drive with a 50 % duty cycle is difficult to implement. A simple impedance analysis can solve this problem of implementation and allow the load network to be realized with microstrip transmission lines.

## 5.3 Load pull analysis

Load pull technique is used to vary the load impedance seen by the device and the performance of the device is determined at the same time. It is a very commonly used and preferred analysis for PA design applications. Load pull is the technique during which the source impedance and source power are kept constant at certain level and then, a sweep impedance or reflection coefficient of load over certain section in smith chart is performed to characterize some essential PA parameters such as output power, power added efficiency, IMD (with two-tone load pull); the purpose being

to find out the optimum impedance to be presented to the device and then, accordingly, to perform the impedance matching network design. Some critical points should be determined while performing load pull simulation:

- The section of the smith chart to use for load impedance
- The source impedance to keep constant while performing load pull simulation
- The amount of source power for load pull simulation

There are not any straight way to determine these issues. Following the simple guidelines of load pull analysis and working through them in an iterative manner before final load pull analysis can be a good solution. Following are some guidelines followed in this work:

i. The required section of smith chart can be obtained from device datasheets, which sometimes provide such information. Another way is to define a section and then go around to finalize the optimum location. Usually power devices work at lower impedances, so sections near periphery are the best guess to start with.

ii. Usually power devices have lower impedances, so keeping the source impedance as 5 or 10 Ω offers good starting point for a design. Later on, this can be pinched to achieve a good value. After successful load pull simulation, the circuit simulator (here ADS) provides quite good estimation of optimum source impedance. For example, in this design, at first 5 Ω resistor in series with gate was used, hence 10 Ω was used as a starting point for source impedance during load pull simulation.

iii. The good amount of source power estimation can be found in device datasheet, which provides gain of the device at a given frequency. A good way to estimate the required input power is to use the simple formula: "output power required – gain (as mentioned in datasheets) + 3 dB" [43]. Then it can be increased or reduced in couple of iterations and the final value of source power can be determined.

In this design of a Class E power amplifier, it has been noticed that the impedance seen by the device for maximum efficiency, power or gain can be quite different. The impedances are chosen as per the design requirements in such cases. It has been also noticed that the impedance values vary with bias. In this design, load pull was performed to obtain maximum efficiency. The results obtained from this simulation show that the transistor needs to see an impedance of (23.034 –

j16.854) Ω at the output and (64.959 – j106.904) Ω at the input as shown in figures 35 and 36, respectively. The design proceeds with these numbers. The load network and the input matching network design are the next steps of designing the Class E PA.

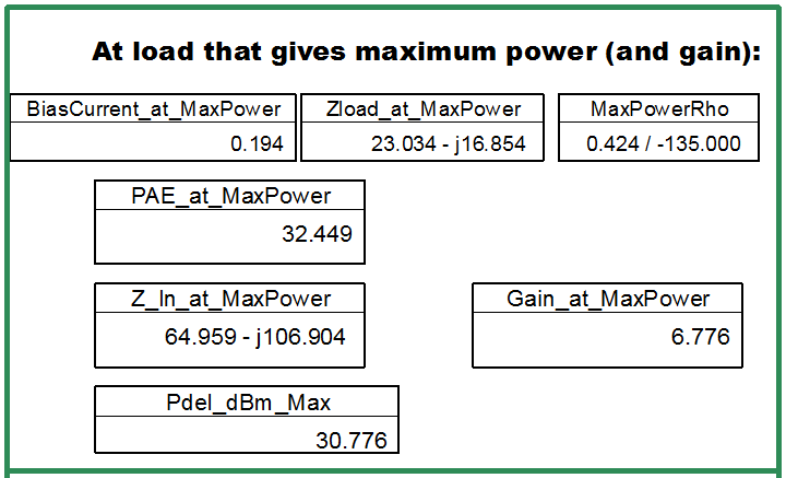



Figure 35: Load pull analysis to determine load and source impedance for maximum efficiency

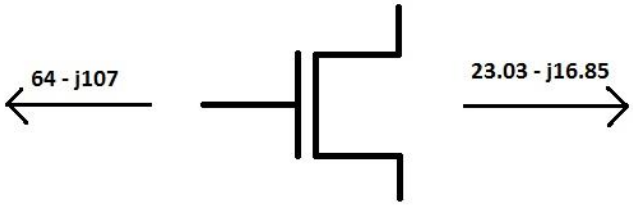



Figure 36: Load and source impedances for maximum efficiency

## 5.4 Class E output network

The output network of class E power amplifier serves three purposes. First, it provides the right amount of impedance magnitude and load angle to the output of the active device at the fundamental frequency. Second, it ensures high impedance terminations for all higher-order harmonics. Third, it helps to match the output impedance of the active device with the load of the power amplifier. The first purpose is understandable, but due to the narrowband nature of the transmission line circuits, the second one is complicated. This work assumes that the higher order harmonics are entirely removed.

The input and output biasing circuits are designed to not affect circuit performance. They should appear invisible to the drain of the active device. This level of individuality can be maintained by the biasing network discussed and presented in chapter 4. The important issue regarding the bias network to be considered is that, the bias supply is properly decoupled and the bias circuitry does not load the power amplifier over the RF band of interest. Microstrip transmission line implementation is presented next along with the discussion regarding harmonic terminations.

### 5.4.1 Transmission line implementation

According to the ideal Class E amplifier, all higher order harmonics meet a high impedance load. It has been shown in practice that only two harmonics are sufficient at the drain of the device for constructive class E operation. None of the load network or the input driving waveform saddles ideal condition to the transistor. So, all that can be attained is a closer approximation. The microstrip class E power amplifier uses a three-stage load network whose assignments include:

- presenting adjusted impedance to the drain of the active device at the fundamental frequency (2.5 GHz),
- offering open circuit condition to the second harmonic (5 GHz) and,
- matching the output impedance of the active device with the load.

Figure 37 depicts the output network for class E power amplifier. By adjusting the lengths of transmission lines closest to the drain of the active device to 45° at the fundamental frequency, the high impedance second harmonic termination was achieved. The electrical length of the transmission line is 90° at the second harmonic. It makes them quarter wave impedance transformer. The open circuit at ‘A’ transformed into short circuit at ‘B’ and turns back to open circuit at ‘C’ where the transmission line interfaces to the drain of the active device. First two stages of the load network take intensive care of the termination of second harmonic. The third stage transform the 50 Ω load impedance to adjusted impedance at the fundamental frequency as seen at the output of the active device at ‘C’.

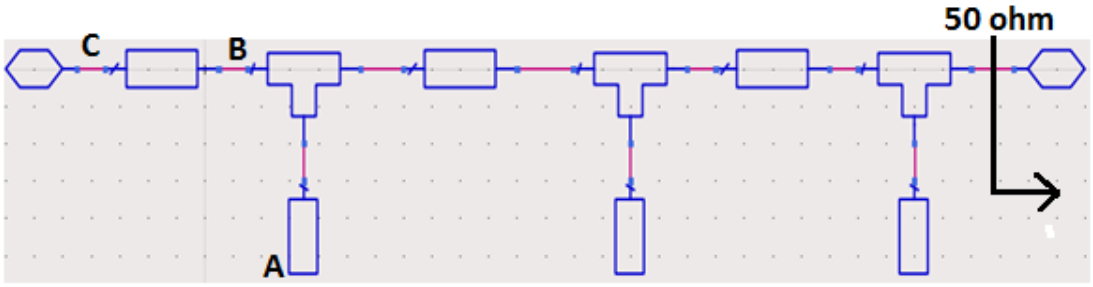



Figure 37: 3-stage output network to provide high impedance termination to second harmonic and adjusted impedance to fundamental frequency

Transmission line lengths and characteristic impedances have to be adjusted in the practical implementation, so that the impedance requirements at 2.5 GHz and 5 GHz are met at the same time. The final test of the load network design will be presented later in the report where high efficiency class E power amplifier operation is verified in terms of simulations.

The simulated $S_{11}$ response in figure 38, shows a return loss of 31.5 dB. Figure 39 shows the layout of the output network. The width of all the transmission lines has been set 65 µm. The length of the series and parallel lines are 250 µm and 150 µm, respectively.

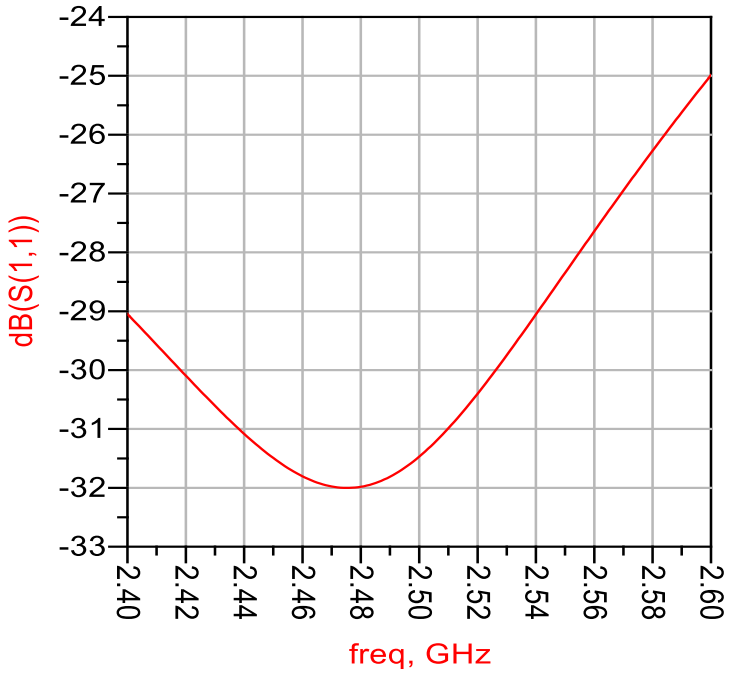



Figure 38: Simulated $S_{11}$ response of the output network

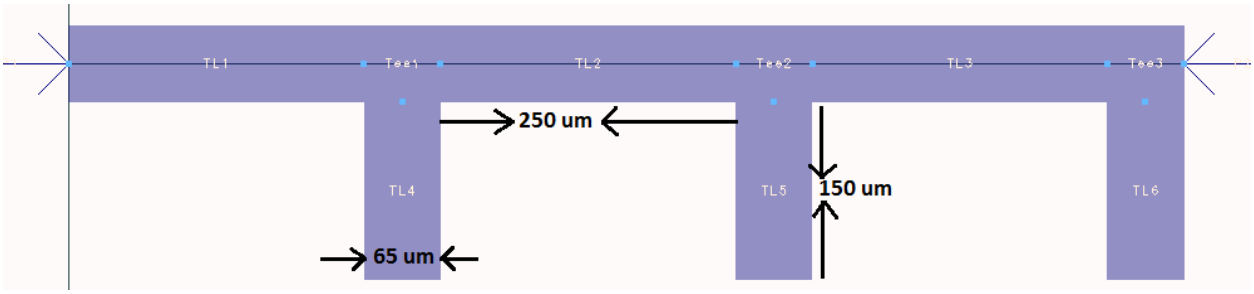



Figure 39: Layout of the output network

## 5.5 Input matching network

An RF signal source is used as the input driver of the power amplifier. Maximum amount of power from the RF signal source has to be delivered to the gate of the active device. An input matching network ensures this. The initial design strategy is to provide a conjugate or small signal input match to facilitate the characterization of the load network. The transmission line implementation of the input matching network is shown in figure 40. The simulated $S_{11}$ response in figure 41 shows a return loss (*RL*) of 22.7 dB.

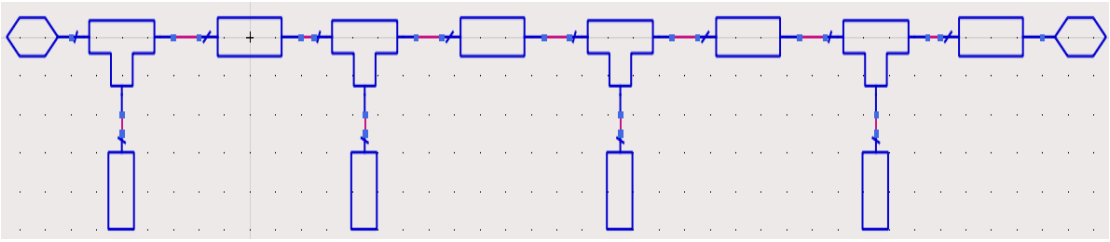


Figure 40: Input matching network

The switching of the active device requires effectively high drive level. A drive level of 24 dBm is applied to the GaN device. Applying this level of RF power to a matched 50 Ω input, results in 33.7 V peak-to-peak voltage swing at the gate terminal. This takes the transistor outside of the small signal regime.

Two points have been considered while designing input matching circuit. First, the gate of the active device must be driven by the required RF power level: $P_{avs} = P_{SW} = 24$ dBm. Second, the input matching circuit must be tuned until drain efficiency and output power are maximized for the applied input power level.

Figure 42 shows the layout of the input matching network. The difference in the small signal and large signal impedances can be noticed when the performance of the power amplifier is assessed.

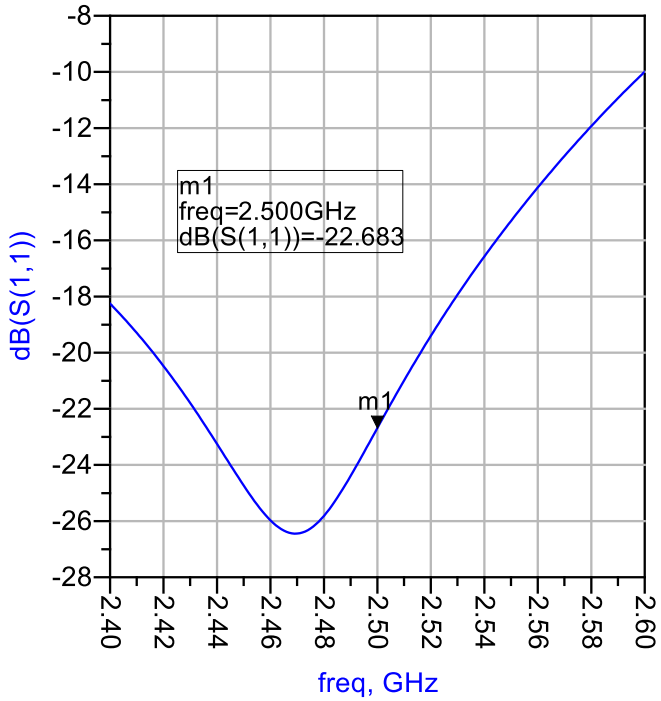



Figure 41: Simulated $S_{11}$ response of the input matching network

Table 11 provides a brief analogy of how the circuit behaves with a conjugate matching circuit versus a power match at a source power of 24 dBm. It is noticeable that all the parameters are slightly higher with the power match at the input.

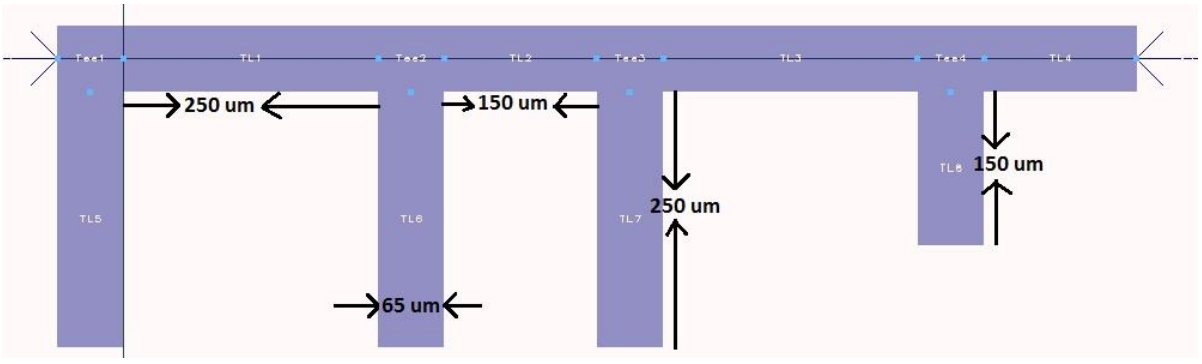



Figure 42: Layout of the input matching network

Table 11: Class E PA performance for small and large signal input matching

| Parameter | Small signal | Large signal |
|---|---|---|
| $P_{out}$ | 30.529 dBm | 30.776 dBm |
| Power Gain | 6.529 dB | 6.776 dB |
| PAE | 30.873% | 32.449% |

Two conclusions can therefore be made from these considerations. First, the class E power amplifier operates more efficiently and with higher output power when the gate of the active device is loaded with a large signal than when loaded with a small signal. Second, the improvement with a power input match is effective, but not stringent. The design strategy of using a conjugate input match to assess the accomplishment of the load network and to predict the overall performance of the power amplifier is therefore valid.

## 5.6 Simulation results

The bias network and the complete circuit simulation setup for 2.5 GHz class E GaN-on-SiC power amplifier is shown in figures 43 and 44, respectively. The power amplifier performance was tested by using Keysight's Advanced Design System. The simulations were done by means of single-tone and two-tone harmonic balance simulations. The two-tone test results are compared with the design specifications for WiMAX transmitter.

### 5.6.1 Single-tone simulation

A single tone harmonic balance simulation was performed to plot the voltage and current waveforms at the drain of the active device. The resultant waveforms are presented in figures 45 and 46, respectively.

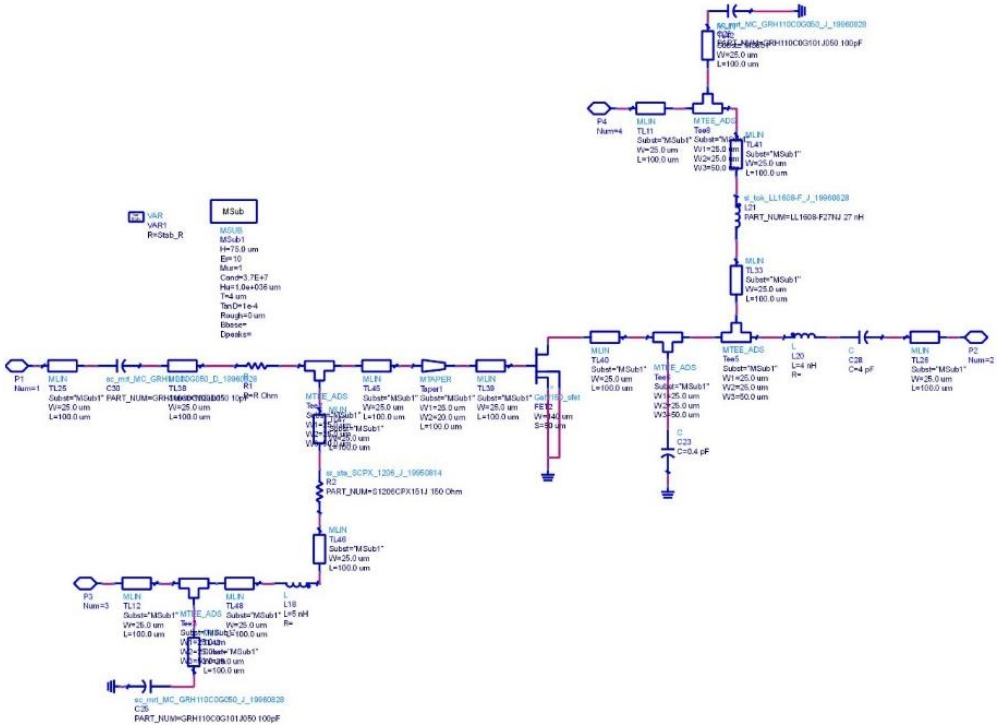


Figure 43: Complete Bias network with the active device

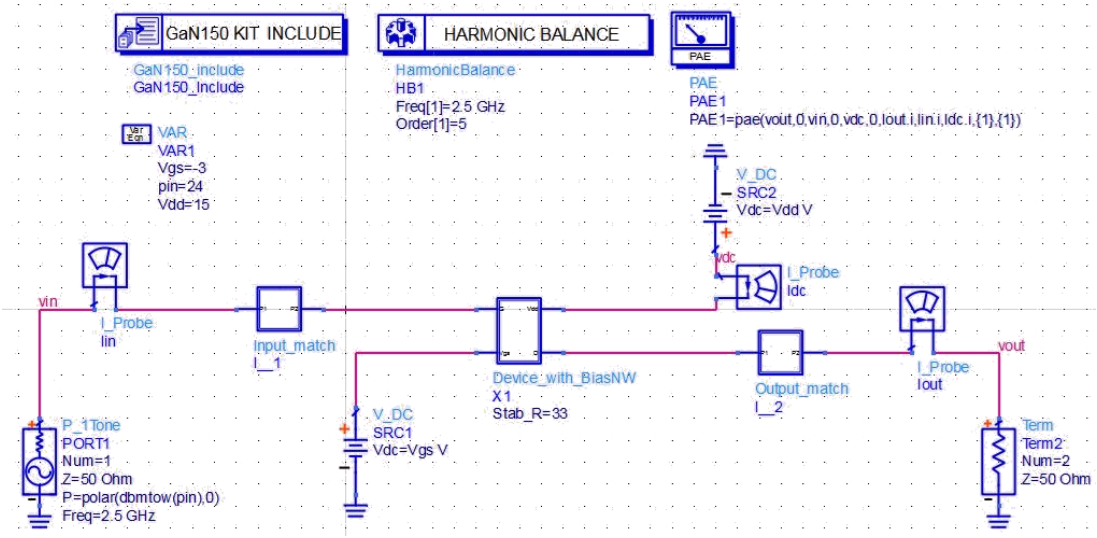



Figure 44: Complete circuit simulation setup

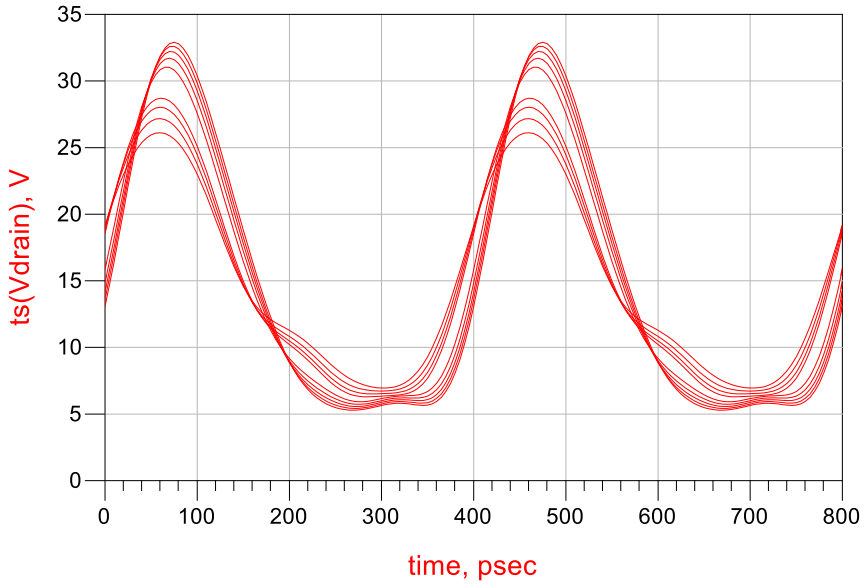



Figure 45: Class E drain voltage waveform

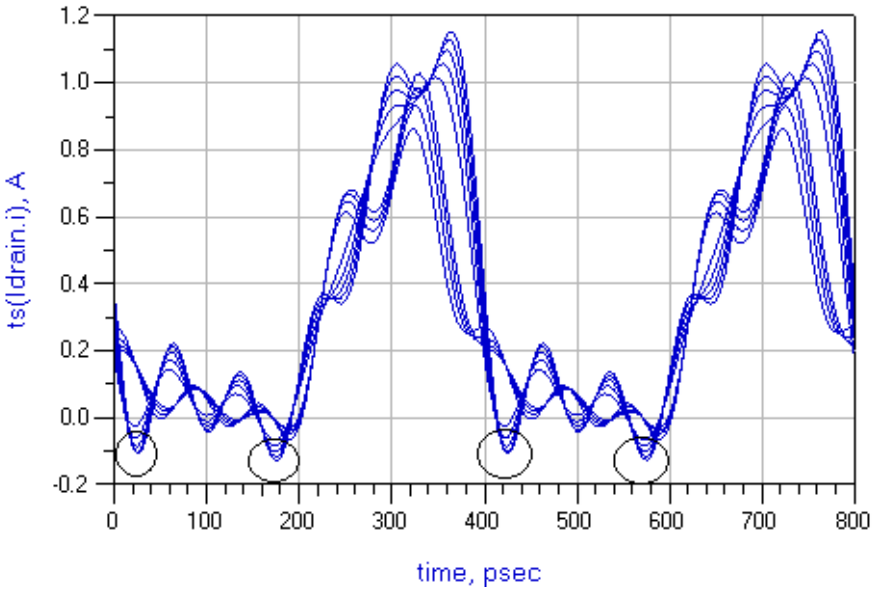



Figure 46: Class E drain current waveform

Harmonic balance is a frequency domain analysis technique for simulating distortion by providing the spectral content of voltages and currents in the circuit. It is very useful to compare intercept point and intermodulation distortion. This is also used to determine the power added efficiency of the amplifier in the presence of interferers. Figure 45 corresponds to the drain voltage of Class E. The voltage waveform is not a perfect sinusoid because of the presence of higher order harmonics.

Figure 46 corresponds to the drain current of Class E. Drain current waveform is a peaked half sinusoidal waveform. It can be noticed that the current peaks occur for the period of time when voltage is at its minimum and that the current minimum coincides for maximum voltage values. Hence the power loss is greatly reduced thereby increasing efficiency. The negative transitions of the drain current waveform are due to the imperfect cancellation of the reactive part at the output of the transistor. This is shown as the circled regions in figure 46.

Table 12 presents the second, third, fourth and fifth harmonic levels at the output. The harmonic contents at the load must be as low as possible in order to avoid unnecessary power loss and matching issues. The class E power amplifier presents harmonic contents at an extremely low level at the output due to the harmonic trapping filter.

Table 12: Harmonic levels at the output

| **$2^{nd}$ harmonic (dBc)** | **$3^{rd}$ harmonic (dBc)** | **$4^{th}$ harmonic (dBc)** | **$5^{th}$ harmonic (dBc)** |
|---|---|---|---|
| -98.19 | -79.63 | -119.23 | -57.41 |

### 5.6.2 Two-tone simulation

Two-tone harmonic balance simulations were performed on the Class E design. Two-tone simulations of amplifier is recommended analysis to find out the IMD performance of the designed amplifier, which also provides clear indication of Adjacent Channel Power Rejection (ACPR) in case of modulated signals. The two-tone frequencies of this design were chosen to be 2.45 GHz and 2.55 GHz. Fifth order harmonic balance simulation was performed to account for all harmonics up to the fifth harmonic. Figure 47 is a plot of the output spectrum of Class E PA.

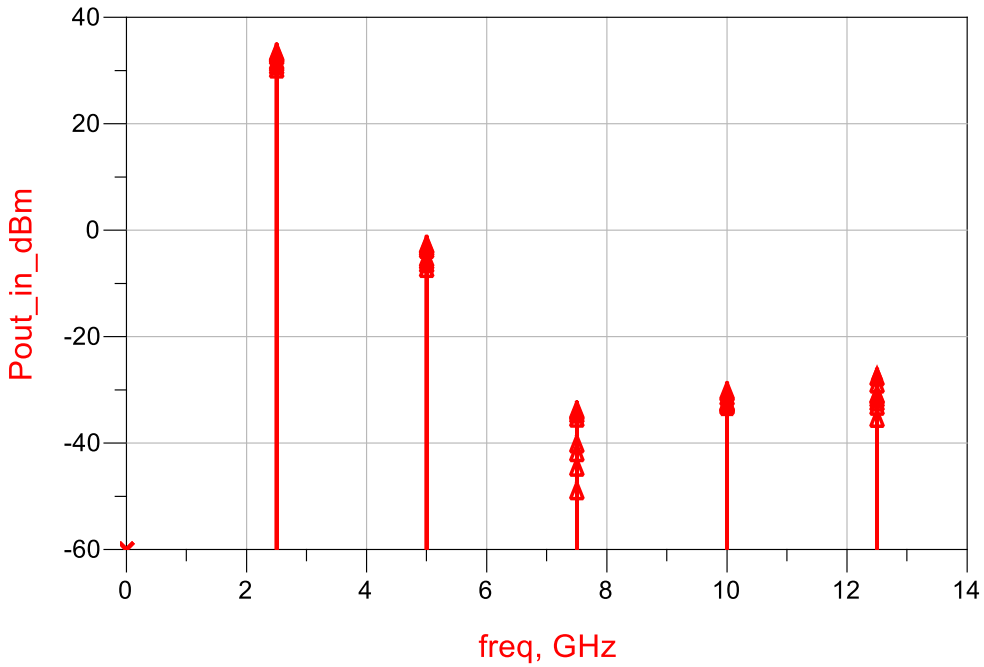



Figure 47: Output spectrum of Class E PA

Figure 48 is the plot of the output spectrum of the PA zoomed around the fundamental frequency. In this plot, the third and fifth intermodulation products are shown. This plot can also be used to determine the corresponding intercept points.

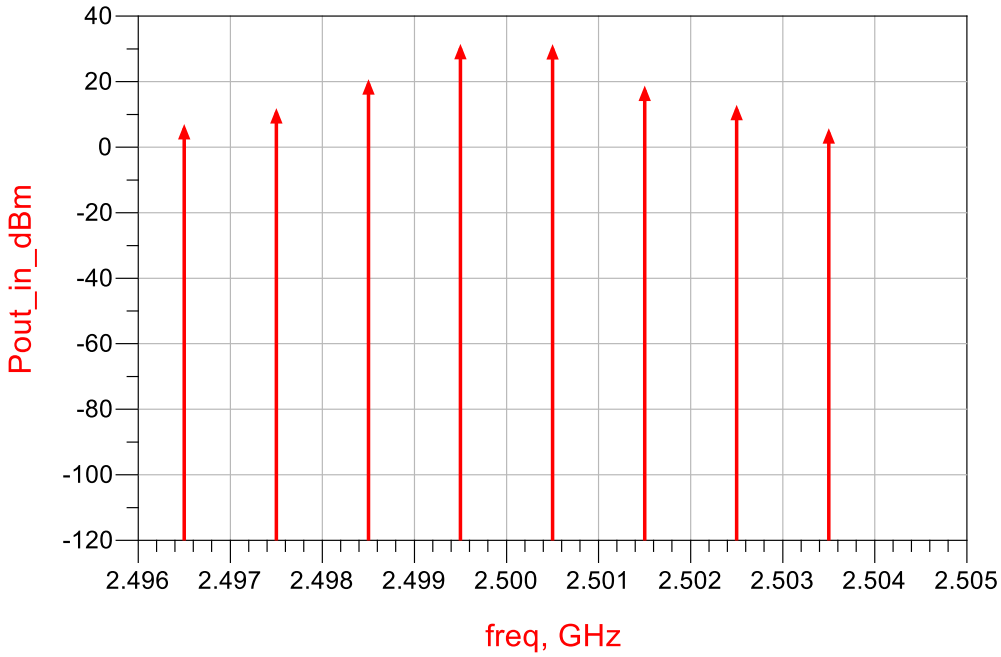



Figure 48: Output spectrum showing 3rd and 5th order IMD products

Figure 49 shows the input-output relationship of the RF power. It can be seen from the plot that the output power is 34.1 dBm at the input power level of 24 dBm, which satisfies the design specifications of the amplifier.

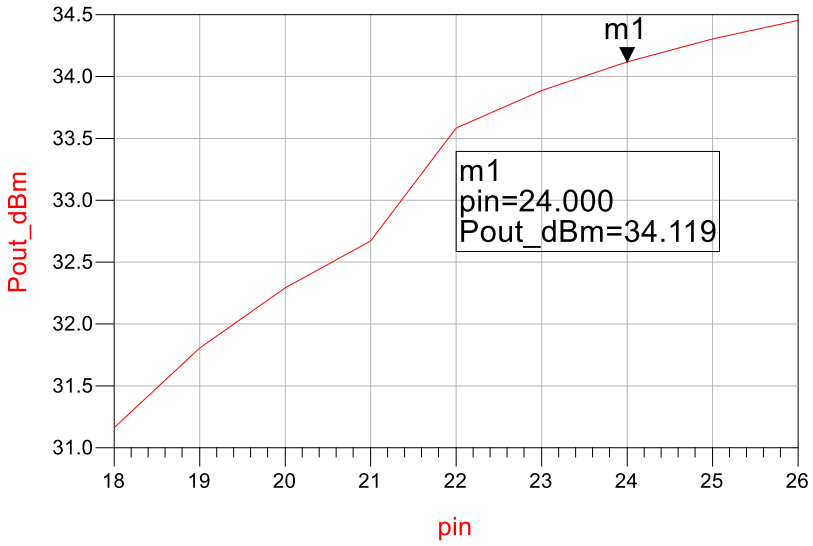



Figure 49: Output vs Input RF power plot

Having met the output power specifications, we determined the power added efficiency of Class E PA. Figure 50 depicts the PAE plot of Class E PA.

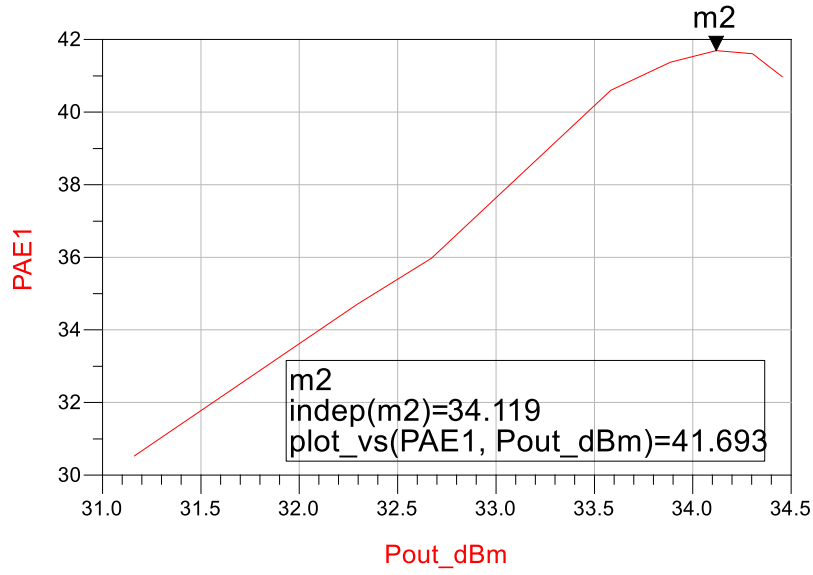



Figure 50: PAE plot of Class E PA

The newly designed Class E power amplifier shows an improvement in efficiency over most previously designed amplifiers of this type. The simulated efficiency of Class E PA at peak power level is 41.7%. This is a significant improvement knowing that this is mainly due to the proposed bias network.

The power gain of the amplifier is shown in figure 51. A gain of 10.12 dB has been achieved at the maximum output power level. The gain plot shows the improvement in gain that is achieved by using Class E type of amplifiers.

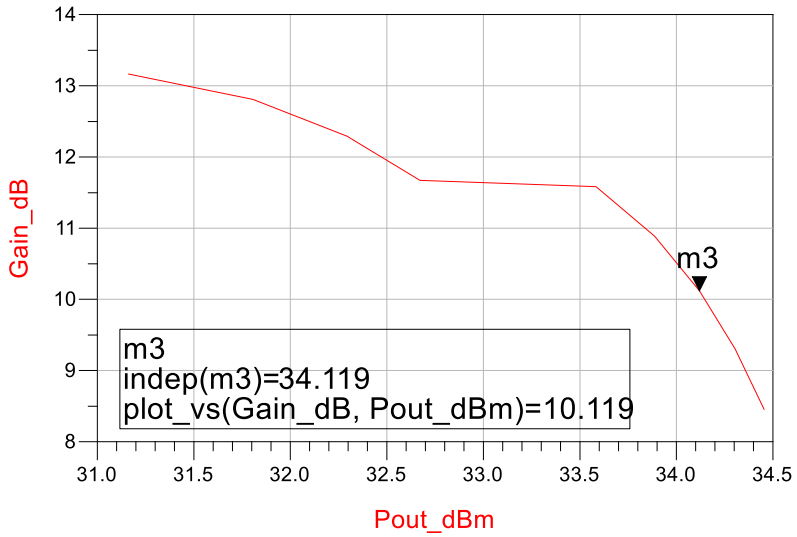



Figure 51: Gain of Class E PA

Peak envelope power (PEP) has been calculated as 10.3 W at the operating frequency of 2.5 GHz. The layout of the complete Class E power amplifier will be discussed in Chapter 6.

### 5.6.3 Modulated signal analysis of the PA

The PTolemy simulator was used to perform the modulated signal analysis. Complete simulation setup is shown in figure 52. Figure 53 illustrates the original signal and the modulated signal. Signal bandwidth is 100 MHz. With a calculated input signal power of 31.7 dBm, the obtained output signal power is 42 dBm. Table 13 presents the calculated ACPRs along with the input and output powers.

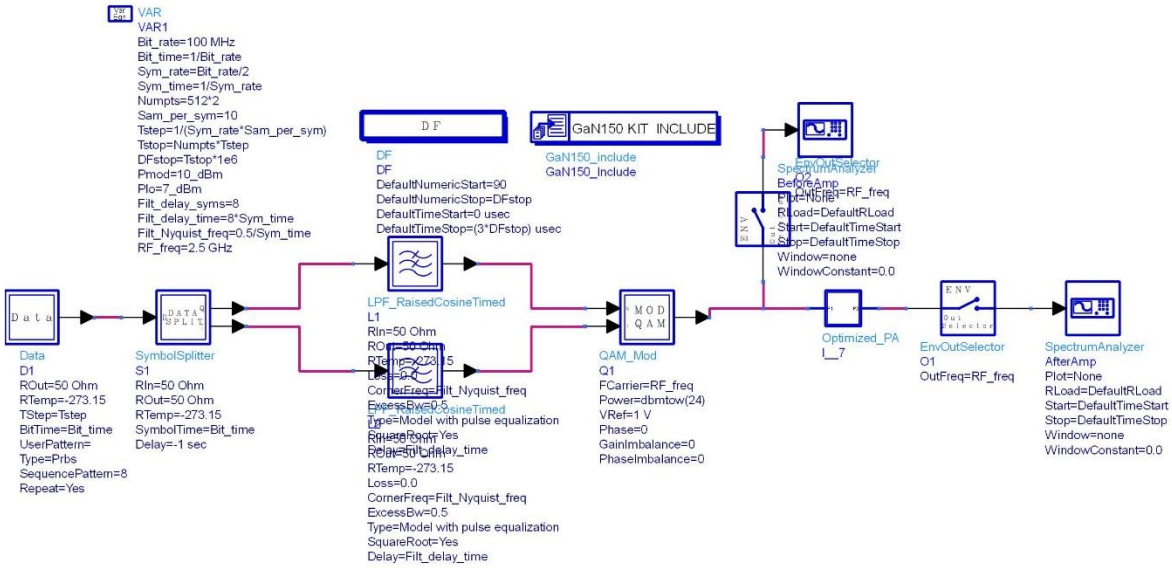



Figure 52: Simulation setup for QPSK modulator

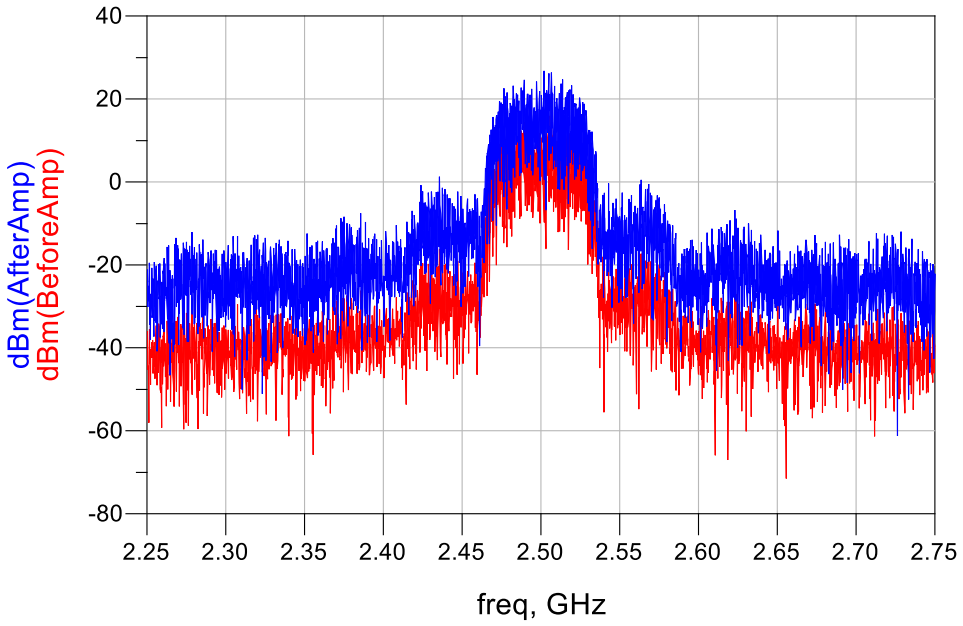



Figure 53: Modulated signal spectrum of the PA

Table 13: Modulated signal performances

| PA_IP_Power | PA_OP_Power | ACPR_Lower | ACPR_Upper |
|---|---|---|---|
| 31.686 | 42.009 | 27.426 | 27.645 |

### 5.6.4 Improved bias network: Performance and Comparison

As reported in Table 14, the improved bias network, designed in this thesis, shows appreciable performance compared to the prior approaches.

Table 14: Performance and Comparison of the improved bias network

| **No. of components used** | **No. of lumped components** | **Total size $mm^2$** | **Power consumption (W)** | **Reference** |
|---|---|---|---|---|
| 21 | 15 | 5.1 | 1.5 | [36] |
| 19 | 12 | 4.9 | 1.3 | [39] |
| 17 | 11 | 4.6 | 1.2 | [40] |
| 17 | 12 | 3.9 | 1.0 | [42] |
| 12 | 8 | 3.6 | 1.1 | [44] |
| 12 | 12 | 6.8 | 1.7 | [67] |
| 30 | 7 | 4.6 | 1.5 | [68] |
| **22** | **10** | **2.6** | **0.9** | **This work** |

It is clear from the above table that the improved bias network designed in this work achieved the lowest power consumption compared to others. Also it is the smallest in size, though it has used a little bit more components. Next section will present the improvements achieved in terms of gain, output power and power added efficiency, using this bias network.

### 5.6.5 Class E PA performance and comparison

All of the simulation results discussed above shows that the designed Class E power amplifier performs well. Table 15 presents the simulated overall performance of the PA at 2.5 GHz.

Table 15: Simulated results of Class E PA

| **Parameters** | **Class E PA performance** |
|---|---|
| Input Power ($P_{in}$) | 24 dBm |
| Output Power ($P_{out}$) | 34.12 dBm |
| Gain | 10.12 dB |
| PAE at maximum output power | 41.7% |
| Drain bias voltage ($V_{dd}$) | 15 V |
| Gate bias voltage ($V_{gg}$) | -3 V |
| DC power consumption ($P_{dc}$) | 1.6 W |
| Peak Envelope Power ($PEP$) | 10.3 W |

Demonstrating peak quantities is a common practice when evaluating power amplifier performance. That is why, published works on this topic quote gain and output power at the input power level that gives maximum power added efficiency. Table 16 compares this work with other reported works for similar application. Figure 54 shows the graphical representation of the comparison of performance parameters. The comparison of performance parameters at the operating frequency of 2.5 GHz is illustrated in figure 55. GaN HFETs operating as a switching elements in Class E PAs is relatively new to the wireless applications. So, most of the reported literatures center around demonstrating device capabilities in other device technologies and/or using other efficiency improvement techniques. In fact, Class E microwave PA design using GaN HFET for the possible application in WiMAX transmitter, is a rare combination.

For application in WiMAX transmitter, the new Class E PA demonstrates comparable power added efficiency to that reported in [44], but has an over 10.42 dBm of output power and over 0.32 dB of gain. In addition to that, the newly designed Class E PA exhibits a higher performance than other reported amplifiers at the operating frequency of 2.5 GHz.

Table 16: Comparison of this work with the prior approaches

| Operating frequency (GHz) | Device Technology | $P_{out}$ (dBm) | Gain (dB) | PAE (%) | Reference |
|---|---|---|---|---|---|
| 2.5~2.7 | InGaP/GaAs | 24.6 | 9.6 | 30.3 | [36] |
| 2.3~2.4 | SiGe | 18.5 | 13.1 | 33 | [39] |
| 2.5 | CMOS | 24.1 | 23.3 | 35 | [40] |
| 1.9/2.5 | GaAs | 6.4-21.6 | 8.2 | 25-43 | [42] |
| 3.5 | SiGe | 23.7 | 9.8 | 42.5 | [44] |
| **2.5** | **GaN** | **34.12** | **10.12** | **41.7** | **This work** |

Figure 54 presents the graphical representation of the performance comparison of this work with the prior approaches. Figure 55 represents the comparison of this work with the prior approaches at the similar frequency band of 2.5 GHz.

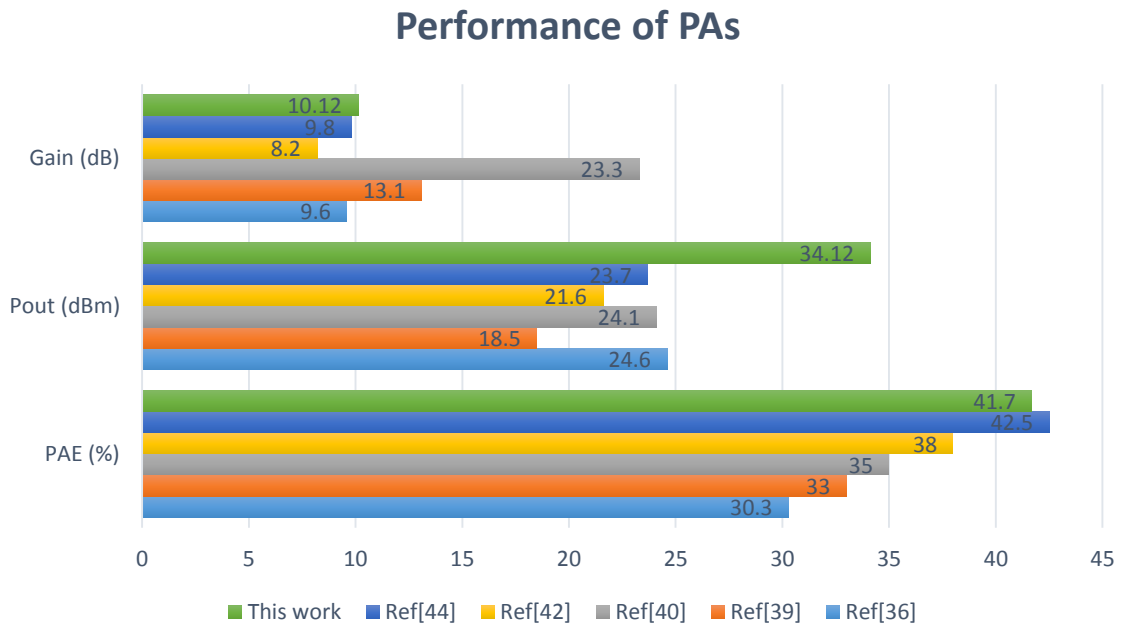



Figure 54: Comparison of performance parameters of the PAs

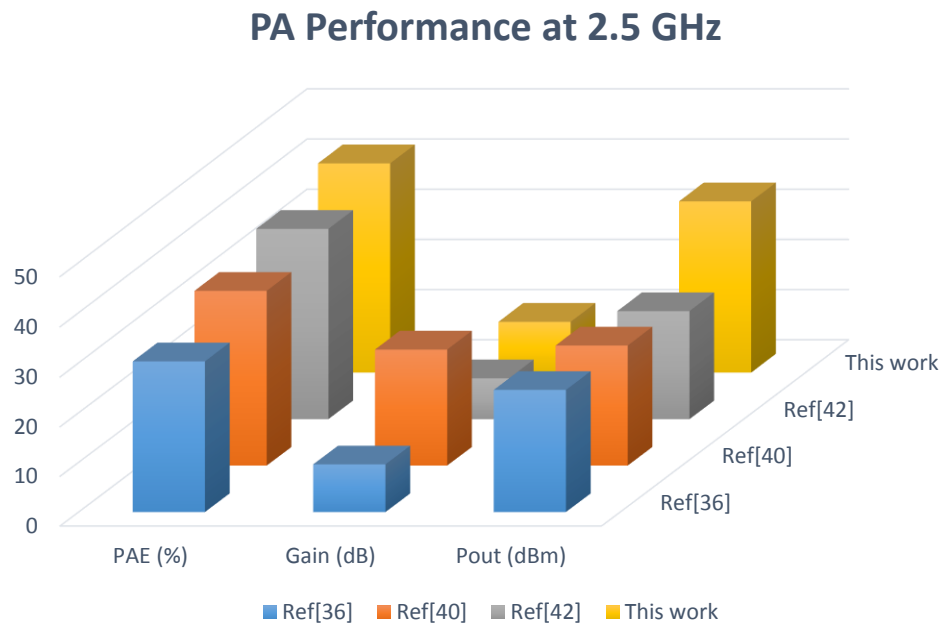



Figure 55: Performance comparison of PAs at 2.5 GHz

## 5.7 Conclusion

The work presented in this chapter took the familiar lumped element configuration and transformed it into a planar Class E PA operating in the WiMAX band at 2.5 GHz. Different simulations were conducted on the designed Class E power amplifier. The amplifier designed with the improved bias network, provides an efficiency of 41.7% at 34.12 dBm of maximum output power with a gain of 10.12 dB. The Class E power amplifier was compared with recently published works for the similar application. Hence, it is found to be a good choice for a WiMAX base station transmitter operating at 2.5 GHz. Next chapter will present the layout design of the power amplifier and perform co-simulation to validate the layout.

# Chapter 6

# Layout Design and Co-simulation

## 6.1 Transmission line

To achieve the 50 Ω characteristic impedance, different transmission line widths were considered. The most suitable transmission line width that can provide 50 Ω characteristic impedance was found to be around 65 µm. Figure 56 shows the impedance curve for 65 µm transmission line width.

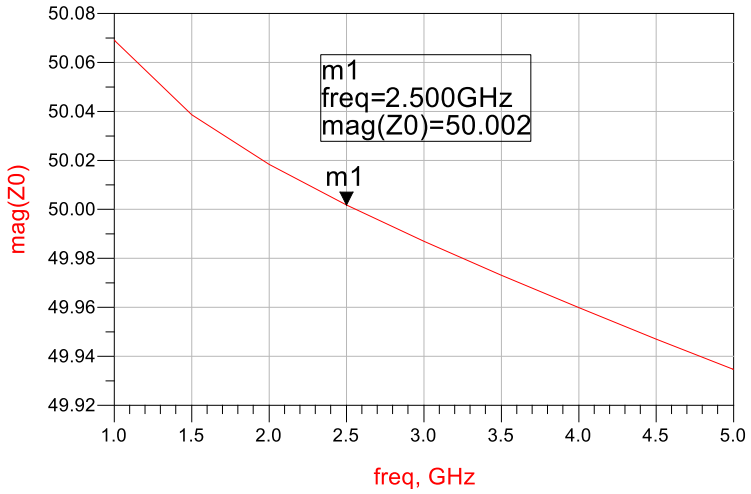



Figure 56: Characteristic impedance for 65 µm width of the transmission line

## 6.2 Layout design

It is to be noted that in the process of designing layout, the passive components used in this design are already built-in and taken from the design kit provided by NRC.

The layout of the output and input matching networks have been shown in figures 39 and 42, respectively. Figure 57 shows the layout design of the bias network. Combining the input-output matching networks and the bias network, figure 58 illustrates the complete power amplifier layout (total area of 3580 x 1623 $\mu m^2$). The layout ground is considered to be ideal. Figure 59 shows the

co-simulation set up for the power amplifier. Next sub section will present the co-simulation results.

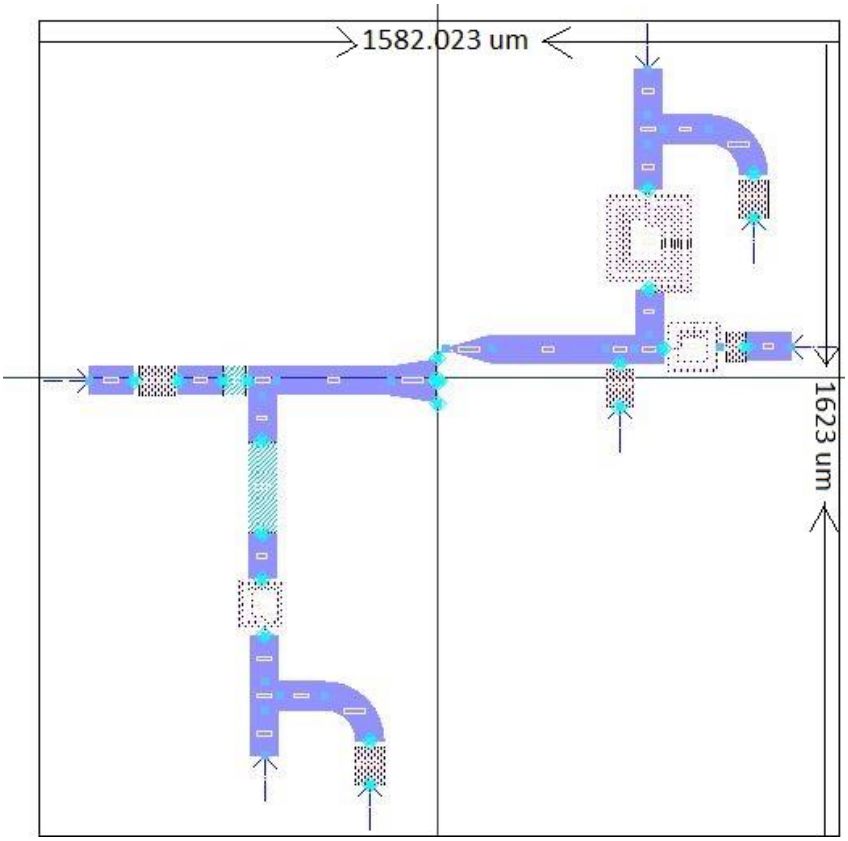



Figure 57: Layout of the bias network

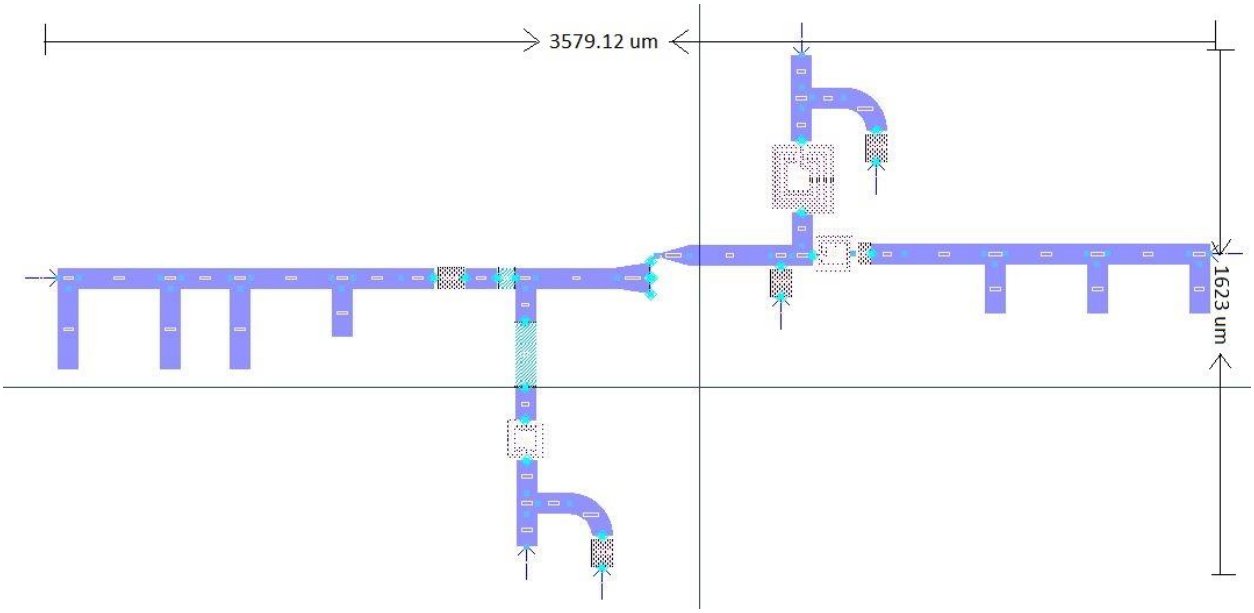



Figure 58: Full PA layout

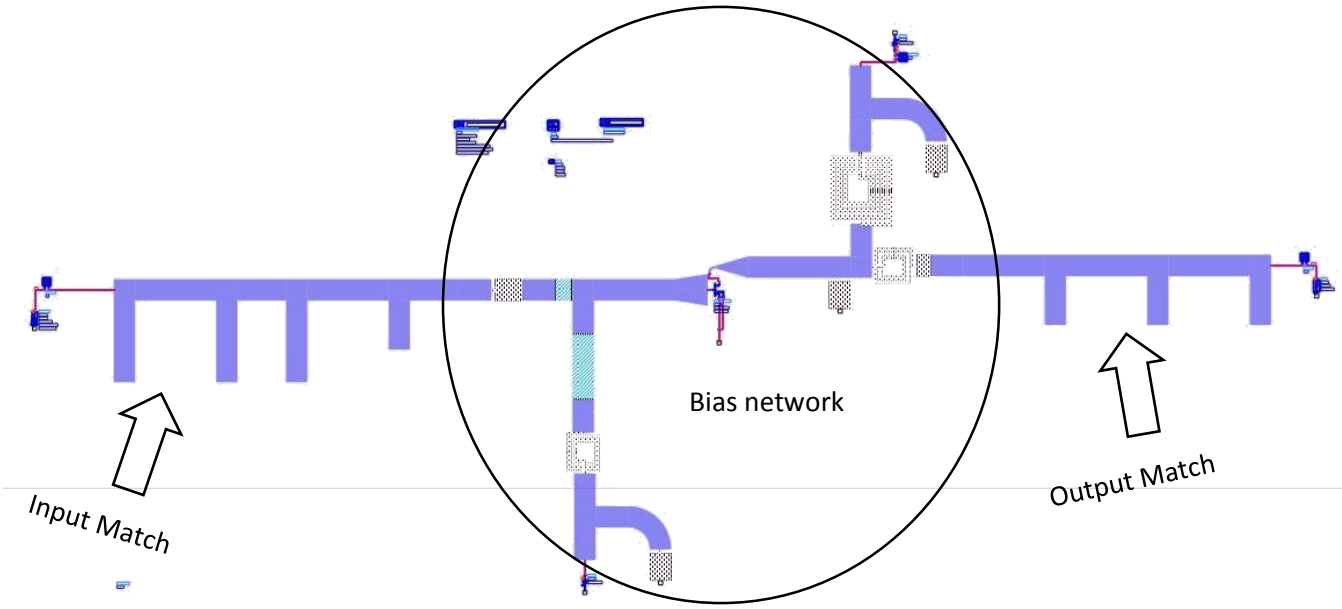



Figure 59: Co-simulation set up for the Class E PA

## 6.3 Co-simulation results

This section presents the co-simulation results for the PA stability, output power, gain and power added efficiency. Figure 60 shows the comparison of stability curves of the PA. It shows a little bit improvement in the stability factor compared to the schematic simulation.

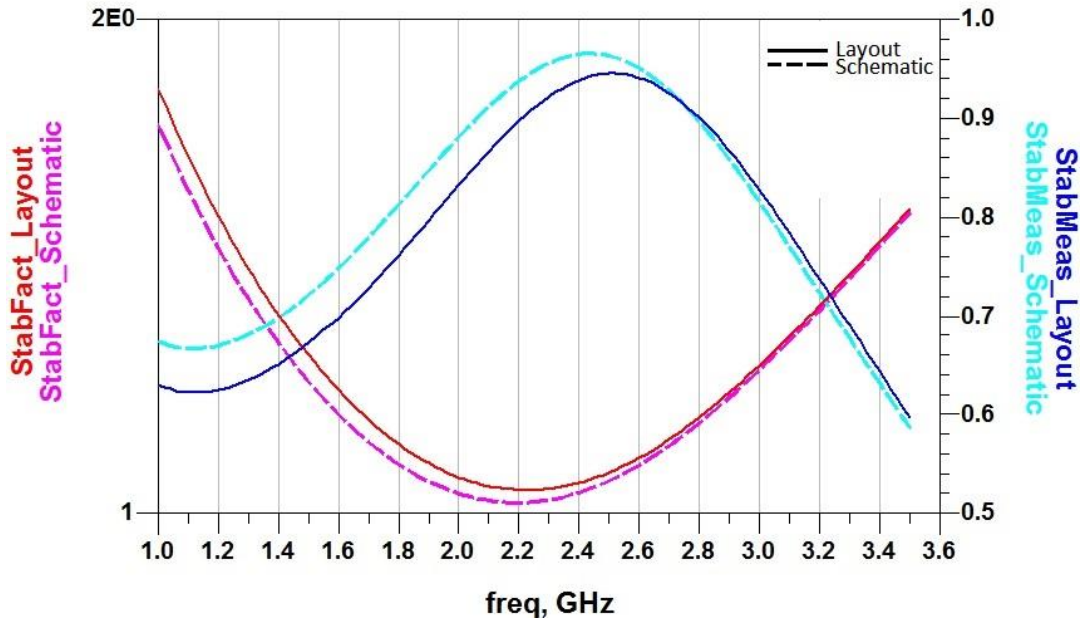



Figure 60: Comparison of the stability analysis of the PA

Figure 61 shows the comparison of output power curves of the power amplifier. The output power found in co-simulation is 0.5 dBm lower than the result of the schematic simulation. Figure 62 depicts the comparison of gains of the PA. It is also 0.5 dB lower than that of schematic simulation.

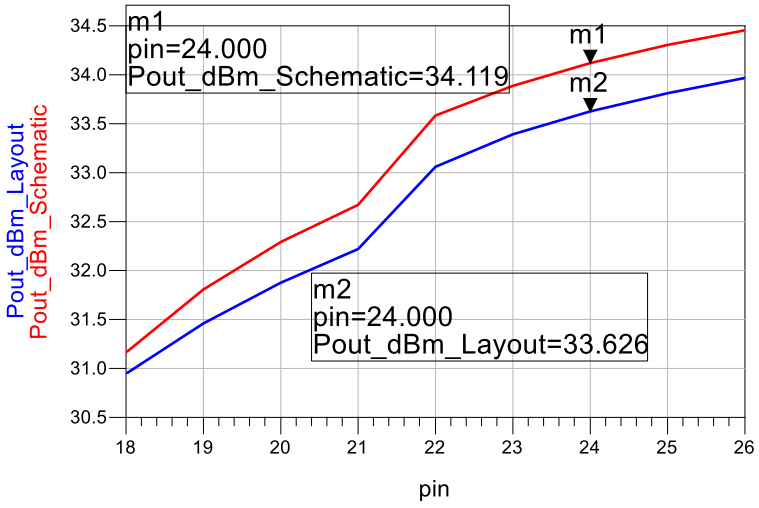



Figure 61: Comparison of the output power of the PA

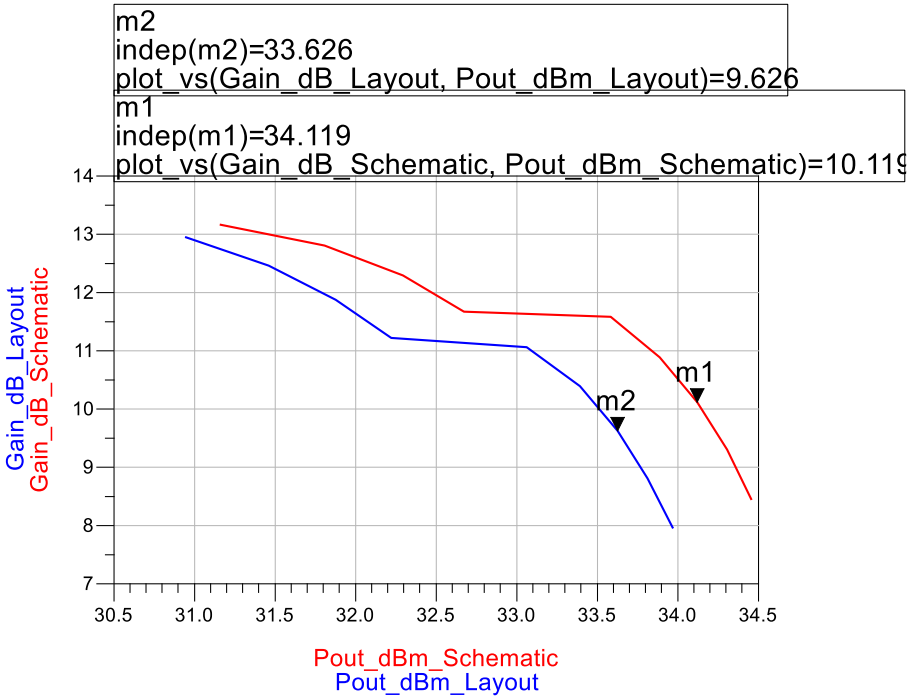



Figure 62: Comparison of gains of the PA

Figure 63 shows the comparison of PAE of the power amplifier after co-simulation. Here, the efficiency is slightly decreased than that of the result found in the schematic simulation.

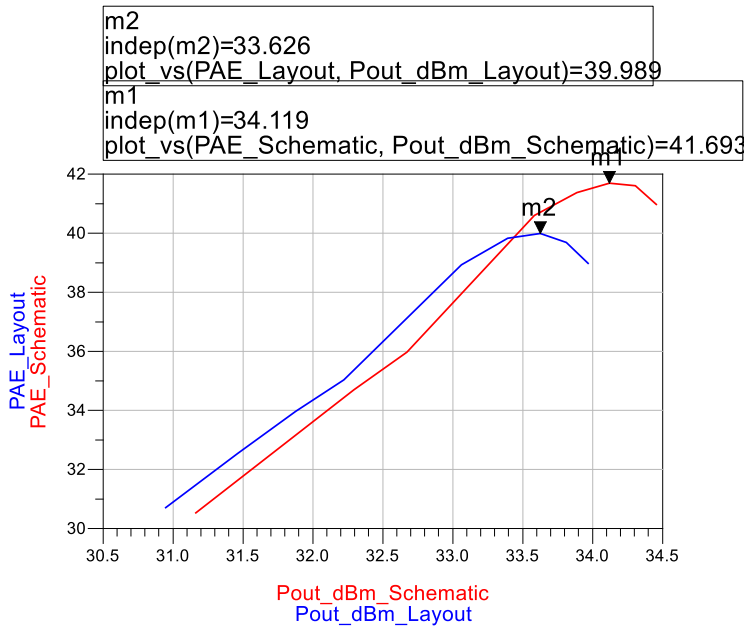



Figure 63: Comparison of PAEs of the PA

Table 17 presents the performance summary of layout and schematic simulation. The differences in the results may be occurred due to the discontinuity issue in the layout. However, both schematic and layout simulation results meet the minimum specification of the design.

Table 17: Class E PA performance in layout and schematic

| **Performance Parameter** | **Minimum Specification** | **Schematic performance** | **Layout performance** |
|---|---|---|---|
| Input Power ($P_{in}$) | 24 dBm | 24 dBm | 24 dBm |
| Output Power ($P_{out}$) | 2 W | 2.6 W | 2.3 W |
| Gain | ≥ 9.5 dB | 10.12 dB | 9.626 dB |
| PAE at maximum output power | ≥ 40% | 41.7% | 40% |

## 6.4 Conclusion

Layout design and simulation of the Class E power amplifier have been performed in this chapter. A very little mismatch is noticed in the results but those are not that significant. The overall layout design meets the minimum requirements of the power amplifier design. Next chapter will conclude the report and suggest the possibilities of future research in the area.

# Chapter 7

# Conclusion

## 7.1 Summary

The Class E power amplifier has seen applications in low power, low frequency, but has not been efficient in high power applications primarily due to the inadequate device technology. This thesis has shown the successful demonstration of GaN transistor technology for switched-mode Class E microwave power amplifier. GaN technology promises to be superior in performance than the alternative GaAs, InP, SiGe technologies. GaN devices are better suited to high frequency, high power and switched-mode PA applications than established technologies due to high 2DEG sheet charge densities and higher breakdown electric field level.

An improved bias network is introduced in this work. The improved network shows an efficient transition of signals from the input to the output of the PA without any significant power loss. The stabilization technique used in the bias network provides the required stability of the PA in the entire frequency range. The gate voltage and supply voltage of the PA are getting purified before entering into the circuit. It was considered that the bias insertion unit should not load the matching circuitry while designing the network. A stable operating point is presented to the transistor in spite of the large signal variations at the input and output port of the transistor. The desired RF signal at 2.5 GHz is properly AC-coupled in to and out of the PA.

The design and optimization of a 2.5 GHz Class E power amplifier have been carried out with the help of the improved bias network. The PA has been designed using Kesight's ADS design software with the latest released GaN design kit. The power amplifier has been successfully demonstrated in hybrid microstrip technology. The designed amplifier delivered 34.12 dBm of maximum output power at a gain of 10.12 dB. The power added efficiency is as 41.7% at the maximum output power. The simulated performance of the PA is in good agreement with the specifications. However, because all obtained values are based on CAD simulations, actual performance of the designed amplifier may vary significantly. Overall, this work shows the suitability of GaN transistor technology for switched-mode microwave power amplifiers with possible application in WiMAX base station transmitter.

## 7.2 Future works

This thesis has been successful in achieving the objectives initially set out, yet it presents a lot of scope for further research and development. Improving the efficiency of power amplifiers while maintaining the linearity will remain an essential aspect of future work. It would be worthwhile to explore the following to build on this work.

- Investigation on other switched-mode topologies.
- The bias network designed in this work can be applied to other switch mode amplifiers.
- More research can be conducted to reduce the components of the biasing network
- Study of multi-band power amplifiers. In this case, designing of efficient switching circuitry is necessary to be able to switch between the frequencies.
- Research on narrowing down the trade-offs between linearity and efficiency of the PA.
- Use of GaN devices in other part of the communication systems such as low-noise receiver, phase shifter, mixer etc.

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