A BIPOLAR TRANSISTOR MODEL FOR COMPUTER AIDED CIRCUIT DESIGN

by

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ABSTRACT

Computer circuit analysis programs require models of the active devices used and the accuracy of the solution usually hinges on the accuracy of the model. The circuit designer has a number of models to choose from, but for circuits where the operation of the device is non-linear, the accuracy improves with the complexity of the model. However this improved accuracy is achieved at the expense of increased computing time. For some of the more complex models, the determination of their parameters is sometimes difficult. In this thesis, a bipolar transistor model based on the Ebers-Moll transport model, modified by a simplified charged control relation, is developed. The base width modulation, the low current fall-off of 'β' and the avalanche multiplication effects are incorporated in the model in such a manner that the terminal current equations are convenient for computation. The intrinsic model requires 26 parameters but these are easily obtained from fewer measurements. The model is used in conjunction with the NANSIM program via a separate subroutine. Several examples are given to illustrate the application of the model to analyse the d.c., a.c. and the transient operation of circuits. The results are compared with experimental values, and in some cases with the values obtained using the Ebers-Moll model.

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LIST OF SYMBOLS

b_n	Critical field for avalanche
C_E	Total emitter capacitor
C_C	Total collector capacitor
C_{JE}	Emitter junction capacitance
C_{JC}	Collector junction capacitance
C_{DE}	Emitter diffusion capacitance
C_{DC}	Collector diffusion capacitance
D_n	Electron diffusion coefficient
D_p	Hole diffusion coefficient
$\mathcal{E}$	Electric field
$\{e_k\}$	k^{th} iteration of the voltage
e	n x 1 vector of node voltages
f_T	Unity current gain cut-off frequency
G	Admittance matrix
g_m	Transconductance of the small-signal model
g_{mF}	Transconductance in the forward mode
g_{mR}	Transconductance in the reverse mode
I_{ES}	Reverse saturation current of emitter diode when the collector terminal is shorted to the base
I_{CS}	Reverse saturation current of collector diode when the emitter terminal is shorted to the base
I_{eo}	Reverse saturation current of the emitter diode when the collector in open circuited ($I_C = 0$)

I_{co}	Reverse saturation current of the collector diode when the emitter is open circuited ($I_E = 0$)
I_s	Saturation current (function of base doping)
I_N	Transported current component in normal mode
I_I	Transported current component in inverse mode
I_{CC}	Dominant collector current component
I_A	Avalanche multiplication current component
I_f	Forward current component of I_{CC}
I_r	Reverse current component of I_{CC}
I_{be1}	Ideal base current component
I_{be2}	Non-ideal base current component
I_{bc}	Recombination current in collector region
I_{kN}	Knee current in the forward mode
I_{kI}	Knee current in the inverse mode
I_1	Low current parameter for ' β_N '
I_2	Corner current in forward mode
I_3	Low current parameter for ' β_I '
I_4	Corner current in inverse mode
I_E	Emitter terminal current
I_B	Base terminal current
I_C	Collector terminal current
$\bar{I}$	n x 1 vector representing the d.c. current sources

J_n	Electron current density
J_p	Hole current density
k	Boltzman's constant
m	Slope of log β_N vs log I_C at low current
n	Slope of log β_I vs log I_E at low current
$\bar{N}(\bar{e})$	n x 1 vector of non-linear functions
$n'_p(o)$	Excess electron charge density at the edge of emitter junction
n_{po}	Equilibrium minority carrier density in the base
$n'_p(w)$	Excess hole charge density at the edge of collector junction
n_E	Gradient coefficient of emitter junction
n_C	Gradient coefficient of collector junction
p	Hole density
q	Electron charge
Q_b	Total stored charge in the base
Q_{bo}	Total equilibrium stored charge in the base
Q_e	Emitter junction stored charge
Q_c	Collector junction stored charge
r_o	Output resistance in the small signal model
r_E	Ratio of max. capacitance to zero bias capacitance of the emitter junction
r_C	Ratio of max. capacitance to zero bias capacitance of the collector junction
r_{be}	Base to emitter resistance in the small signal model

R_B	Extrinsic base resistance
R_E	Extrinsic emitter resistance
R_C	Extrinsic collector resistance
V_{EB}	Emitter to base voltage
V_{CB}	Collector to base voltage
V_{CE}	Collector to emitter voltage
V_{EC}	Emitter to collector voltage
V_1	Base node voltage
V_2	Collector node voltage
V_3	Emitter node voltage
v_k	Voltage across diode
V_M	Breakdown voltage
V_{AN}	Early voltage in the normal mode
V_{AI}	Early voltage in the inverse mode
V_{OE}	Voltage across base-emitter junction at the previous time step
V_{OC}	Voltage across collector base junction at the previous time step
v_s	Saturation velocity
w	Base width
α_F	Common base current gain in the forward direction
α_R	Common base current gain in the reverse direction
β_N	Common emitter current gain in normal mode
β_I	Common emitter current gain in the inverse mode
β_{NO}	Maximum current gain in normal mode

β_{IO}	Maximum current gain in inverse mode
ϵ	Dielectric constant
ϕ_E	Built in potential of emitter junction
ϕ_C	Built in potential of collector junction
τ_F	Base transit time in normal mode
τ_R	Base transit time in inverse mode
λ	Parameter representing high current effects
ΔT	Time step for transient analysis
ω	Frequenoy in radians / sec.

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CHAPTER 1

INTRODUCTION

Computer Aided Design (CAD) covers a broad spectrum of activities in which the computer is used as a design tool to help in designing circuits , preparing masks , testing etc., Computer Aided Circuit Design (CACD) can be considered as a subset of computer aided design. There are a number of circuit analysis programs available. Their use allows the designer to vary some of the parameters at will , in search of the appropriate performance desired of the circuit. This is most important with integrated circuits , and may lead to an appreciable economy of time and money in the design stage.

The simulation procedure requires models of the components of the circuit , and especially of the active devices. The success of the simulation depends critically on the model chosen to represent the behaviour of the devices. A model of insufficient accuracy can lead to inaccurate or meaningless results. On the other hand the use of accurate or more complex models increases the CPU time , increases the chances of numerical errors and limit the size of the circuits that the simulation program can accomodate. Moreover the more complex the model the more time and effort must be spent in determining the model parameters. Thus simplicity and accuracy are the important factors and for a practical model a compromise has to be reached.

In computer aided design , the most important requirements of a practical model are:

1. The model should predict the behaviour of the device over a wide range of operating conditions.
2. The model parameters should be easily obtainable.
3. The model equations or components should be compatible with the numerical techniques used in the circuit analysis program and should be efficient.

There are a number of models of bipolar transitors available. For different applications different models may be needed. There are two main applications of modeling of active devices:

1. Modeling for the purpose of understanding the physical phenomena taking place within the device.
2. Modeling for the purpose of circuit analysis and design.

It is the second application which is considered here. In this thesis a model of the bipolar transistor suitable for CAD is developed. The model takes into account a number of non-linear effects e.g. low current fall-off of 'β', base conductivity modulation, the Early effect and avalanche multiplication.

The model equations are simple enough so that the computation time is not excessive and the process of determining the parameters is not overly involved. This is obviously a compromise situation ; the usefulness of the model has been verified by its inclusion in a circuit analysis program, and the results obtained indicate that the model gives satisfactory results.

The model is used with NANSIM (Non-Linear Active Network Simulation) developed at Bell Northern Research Lab., via a separate subroutine.

In chapter 2 , a brief review of the Ebers-Moll and the Gummel-Poon model is given. In Chapter 3 , the model is developed and its parameter determination is described. Chapter 4 describes the use of the model with NANSIM, and a few examples are given, and Chapter 5 gives the conclusions drawn from this work.

CHAPTER 2

LARGE SIGNAL BIPOLAR TRANSISTOR MODELS

This Chapter presents a brief historical background of transistor models. The Ebers-Moll and Gummel-Poon model are described as these models form the necessary background for the model developed in the next chapter.

2.1 Historical Background

One of the earliest large signal model of bipolar transistor was formulated by Ebers and Moll in 1954 [1]. It is based directly on device physics and covers all operating regimes, that, is, active, saturation and cut-off operation. A number of approximations limit the accuracy of the model.

In 1957 Beaufoy and Sparkes [2] analyzed the bipolar transistor from a charge control point of view. The basis of the charge control model for bipolar transistors is that the collector current is proportional to the charge stored in the base and in order to change the collector current the charge stored in the base must also be changed. This model characterizes the dynamic behaviour of the transistor in terms of internally stored charges.

The Linvill model [3], developed in 1958, is obtained by solving the continuity equations for current carriers at finite intervals in the base. The form of the solution leads to a set of lumped elements which can be treated as parts of a network. The accuracy of the model depends on the number of sections into which the base is divided.

Hamilton et al [4] have developed a comparison of the above three models and have found them to be basically equivalent. Murphy [5] and Ohtsuki and Kani [6] have proposed transistor models which are very complex and are not found advantageous in circuit analysis programs. Steele [7] has proposed a computer model for n-p-n transistors in an

integrated circuit utilizing p-n junction isolations. Various workers [8] - [11] have used the Ebers-Moll model with some modifications to characterize the transistor.

Gummel and Poon [12] have developed an Integral Charge control Model (ICM) which is based on a charge control relation developed by Gummel [13]. The relation describes the operational characteristics of the bipolar transistor and is obtained from the basic one-dimensional carrier transport equations. In its simplest form, the Gummel-Poon model reduces to Ebers-Moll model under low level injection conditions. The model includes many effects in the transistor not included in the previous models.

Recently, Fossum [14] has described modeling techniques which are applicable to computer aided analysis and design. The modeling approach is to separate the terminal currents into various significant components. These components take into account different effects and depending upon the complexity and the users requirement they may be added or deleted.

In the following sections the Ebers-Moll model in its transport form [15] and the Gummel-Poon model will be developed as these form the basis of the model developed in the next chapter.

2.2 Ebers-Moll Model

In this section, the Ebers-Moll model is developed so as to be useful for the circuit design purposes. The Ebers-Moll model is based upon the concept of superimposing normal and inverse transistors in which the collector base and emitter base junctions are represented by diodes shunted with capacitors. Following is a brief description of the model.

Consider a N-P-N transistor shown in Fig. 2.1 with its cross-section, in which the base is so thin that the diffusion length of the electrons is much greater than the base of the transistor. In the transistor operation the excess minority carriers are injected or extracted by applying a voltage to either junction. The excess carrier concentration at the edge of each space charge layer is given by Boltzman's relation. Thus the excess concentration at the edge of the emitter space charge layer is given by

$$n'_p(o) = n_{po}\left(e^{\frac{-qV_{EB}}{kT}} - 1\right) \qquad (2.1)$$

where n_{po} is the equilibrium minority carrier density in the base, k is Boltzmann's constant, q is electron charge and V_{EB} is the instantaneous emitter to base voltage. In a similar manner, the excess minority carrier concentration at the edge of base-collector junction is

$$n'_p(w) = n_{po}\left(e^{\frac{-qV_{CB}}{kT}} - 1\right) \qquad (2.2)$$

where V_{CB} is the instantaneous collector to base voltage and w is the base width. As shown in Fig. 2.2, the positive concentration of excess electrons indicates that each junction is forward biased. The slope is linear, as the assumptions of low-level injection, uniform base doping and no recombination have been made. This excess charge may be resolved into two components, forward and reverse. Since the current flow in the transistor is due to the excess minority carriers, we can represent the currents as the sum of forward and reverse currents. The forward current component I_F if given by

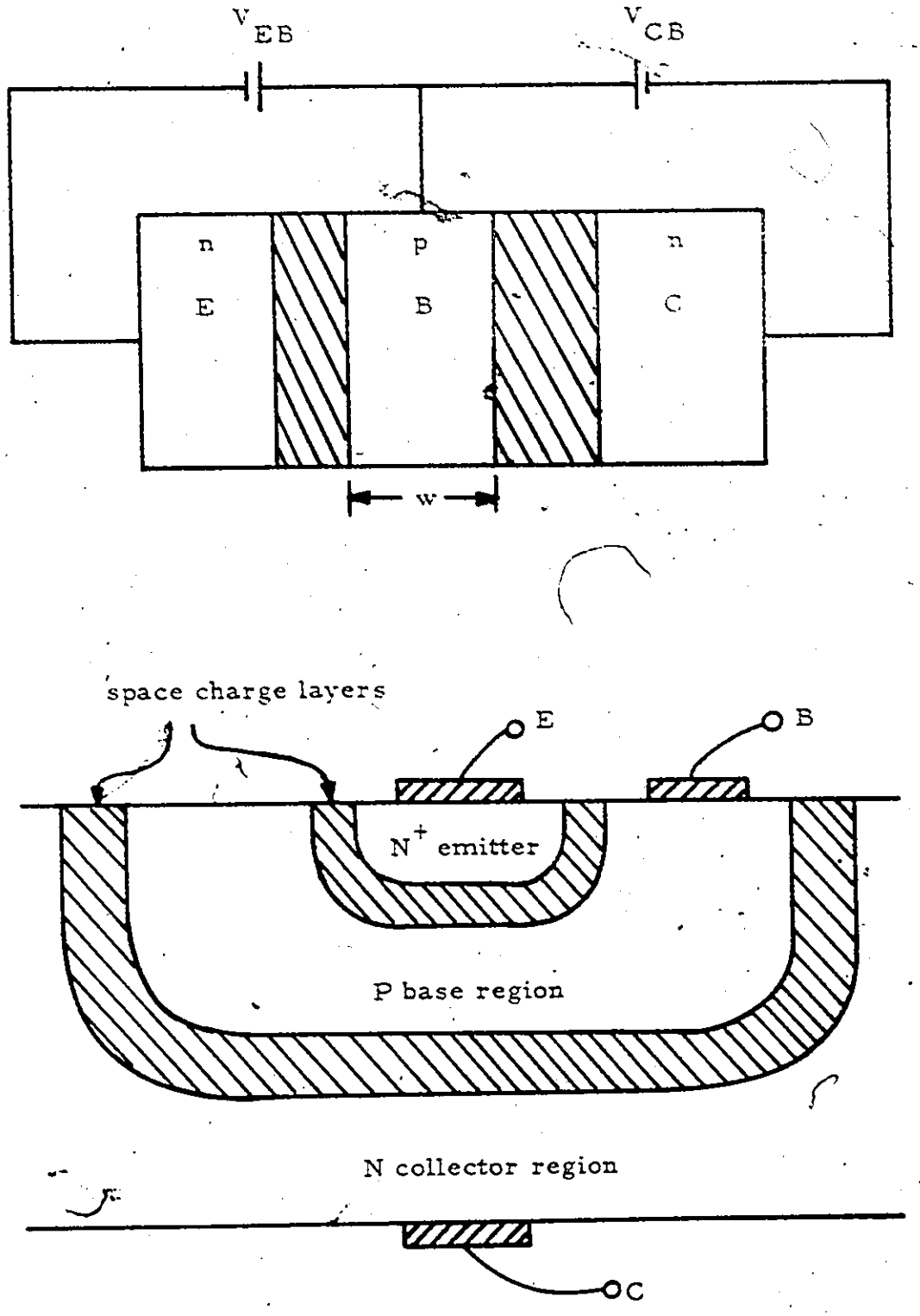


Fig. 2.1 N-P-N transistor with its cross-sectional view.

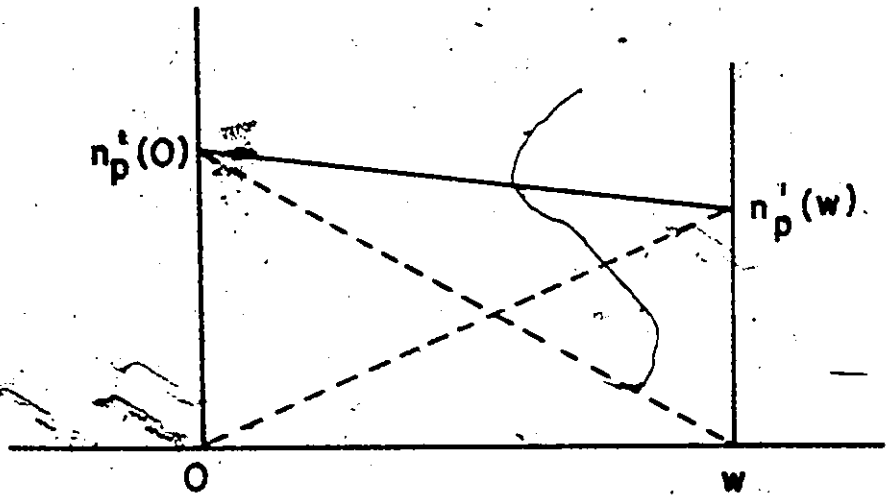


Fig. 2.2 Carrier concentration in the base region

$$I_F = -I_{ES}\left(e^{\frac{-qV_{EB}}{kT}} - 1\right) \qquad (2.3)$$

and the reverse current component

$$I_R = -I_{CS}\left(e^{\frac{-qV_{CB}}{kT}} - 1\right) \qquad (2.4)$$

Now the total emitter current is given by the sum of the forward current component and the reverse current component transported across the base to the emitter. Thus

$$I_E = -I_{ES}\left(e^{\frac{-qV_{EB}}{kT}} - 1\right) + \alpha_R I_{CS}\left(e^{\frac{-qV_{CB}}{kT}} - 1\right) \qquad (2.5)$$

In a similar manner, the collector current consists of the reverse current component and the part of the forward component transported to the collector.

$$I_C = \alpha_F I_{ES}\left(e^{\frac{-qV_{EB}}{kT}} - 1\right) - I_{CS}\left(e^{\frac{-qV_{CB}}{kT}} - 1\right) \qquad (2.6)$$

The above relations are derived by assuming that there is negligible voltage drop across emitter and collector regions due to flow of majority carriers and also that low level injection conditions prevail.

We can relate the saturation current of diodes I_{ES} and I_{CS} to the leakage currents of the transistor, by

$$I_{eo} = (1 - \alpha_F \alpha_R) I_{ES} \qquad (2.7)$$

$$I_{co} = (1 - \alpha_F \alpha_R) I_{CS} \qquad (2.8)$$

Thus rewriting (2.5) and (2.6) in the matrix form, using (2.7) and (2.8)

$$\begin{bmatrix} I_E \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{-I_{eo}}{1-\alpha_F\alpha_R} & \frac{\alpha_F I_{co}}{1-\alpha_F\alpha_R} \\ \frac{\alpha_F I_{eo}}{1-\alpha_F\alpha_R} & \frac{-I_{co}}{1-\alpha_F\alpha_R} \end{bmatrix} \begin{bmatrix} e^{\frac{-qV_{EB}}{kT}} - 1 \\ e^{\frac{-qV_{CB}}{kT}} - 1 \end{bmatrix} \tag{2.9}$$

The parameters I_{eo}, I_{co}, α_F, α_R etc. are not independent and are related as,

$$I_{ES}\ \alpha_F = \alpha_R\ I_{CS} = I_s$$

thus,

$$\frac{I_{eo}}{1-\alpha_F\alpha_R} = \frac{I_s}{\alpha_F} = I_s\left(1 + \frac{1}{\beta_N}\right) \tag{2.10}$$

$$\frac{I_{co}}{1-\alpha_F\alpha_R} = \frac{I_s}{\alpha_R} = I_s\left(1 + \frac{1}{\beta_I}\right) \tag{2.11}$$

where $$\beta_N = \frac{\alpha_F}{1-\alpha_F} \tag{2.12}$$

$$\beta_I = \frac{\alpha_R}{1-\alpha_R} \tag{2.13}$$

and I_s is the saturation current which depends on the base doping.

We now define I_N as the component of the current in the normal mode transported across the base from emitter to collector [15] and I_I as the component of the current in the inverse mode transported across the base

from collector to emitter. Thus we can write

$$I_N = I_s \cdot \left(e^{\frac{-qV_{EB}}{kT}} - 1 \right) \tag{2.14}$$

$$I_I = I_s \left(e^{\frac{-qV_{CB}}{kT}} - 1 \right) \tag{2.15}$$

from (2.9), using (2.10) to (2.15) then we get

$$\begin{bmatrix} I_E \\ I_C \end{bmatrix} = \begin{bmatrix} -\left(1 + \frac{1}{\beta_N}\right) & 1 \\ 1 & -\left(1 + \frac{1}{\beta_I}\right) \end{bmatrix} \begin{bmatrix} I_N \\ I_I \end{bmatrix} \tag{2.16}$$

which may be written as,

$$I_E = -\left(1 + \frac{1}{\beta_N}\right) I_N + I_I \tag{2.17}$$

$$I_C = I_N - \left(1 + \frac{1}{\beta_I}\right) I_I \tag{2.18}$$

We also have :

$$I_B = \frac{I_N}{\beta_N} + \frac{I_I}{\beta_I} \tag{2.19}$$

Thus equations (2.17) to (2.19) represent the non-linear equations for the transistor model. The equivalent circuit is given in Fig. 2.3. β_N, β_I, I_s and $\frac{q}{kT}$ are the parameters of the above model.

The model developed above describes the behavior of a transistor at its electrical terminals for arbitrary bias voltages. That is, either junction can be forward or reverse biased. In the following section,

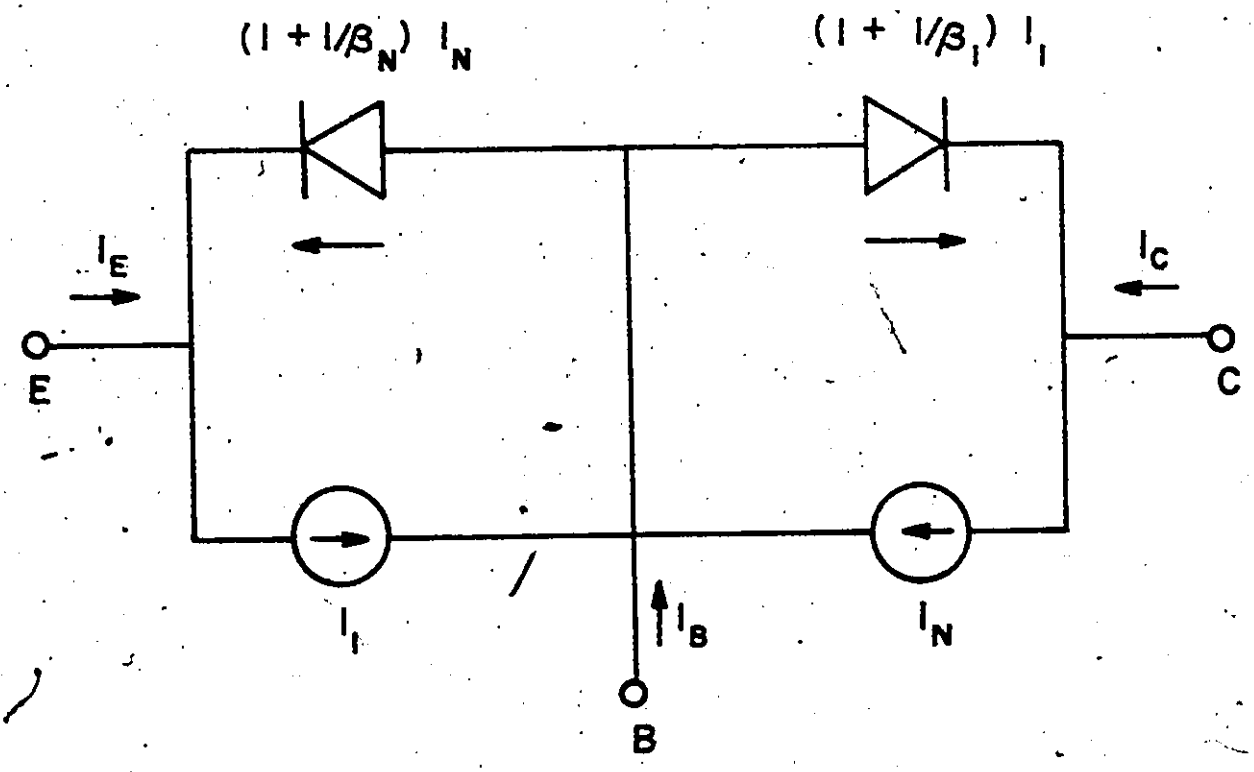


Fig. 2.3 Circuit representation of the Ebers-Moll model

the dynamic behaviour of the model is described.

2.2.1 Dynamic Behavior

For the dynamic behavior of the transistor, various charge storage effects have to be taken into account. There are two types of charge storage in the transistor .

1. Fixed charge in the depletion region. This charge is voltage dependent
2. Mobile charges in the base region which are current dependent.

In order to include the charging currents which flow under dynamic conditions because of above stored charges, two capacitances have to be included across each junction. This is shown in Fig. 2.4. C_{JE} and C_{JC} are voltage dependent junction capacitances representing the emitter and collector depletion regions. They are given by [16] ,

$$C_{JE} = \frac{C_{OE}}{(V_{EB} - \phi_E)^{n_E}} \qquad (2.20)$$

$$C_{JC} = \frac{C_{OC}}{(V_{CB} - \phi_C)^{n_C}} \qquad (2.21)$$

where C_{OE} and C_{OC} are the zero bias capacitances, ϕ_E and ϕ_C are built-in potentials and n_E and n_C are the grading coefficients.

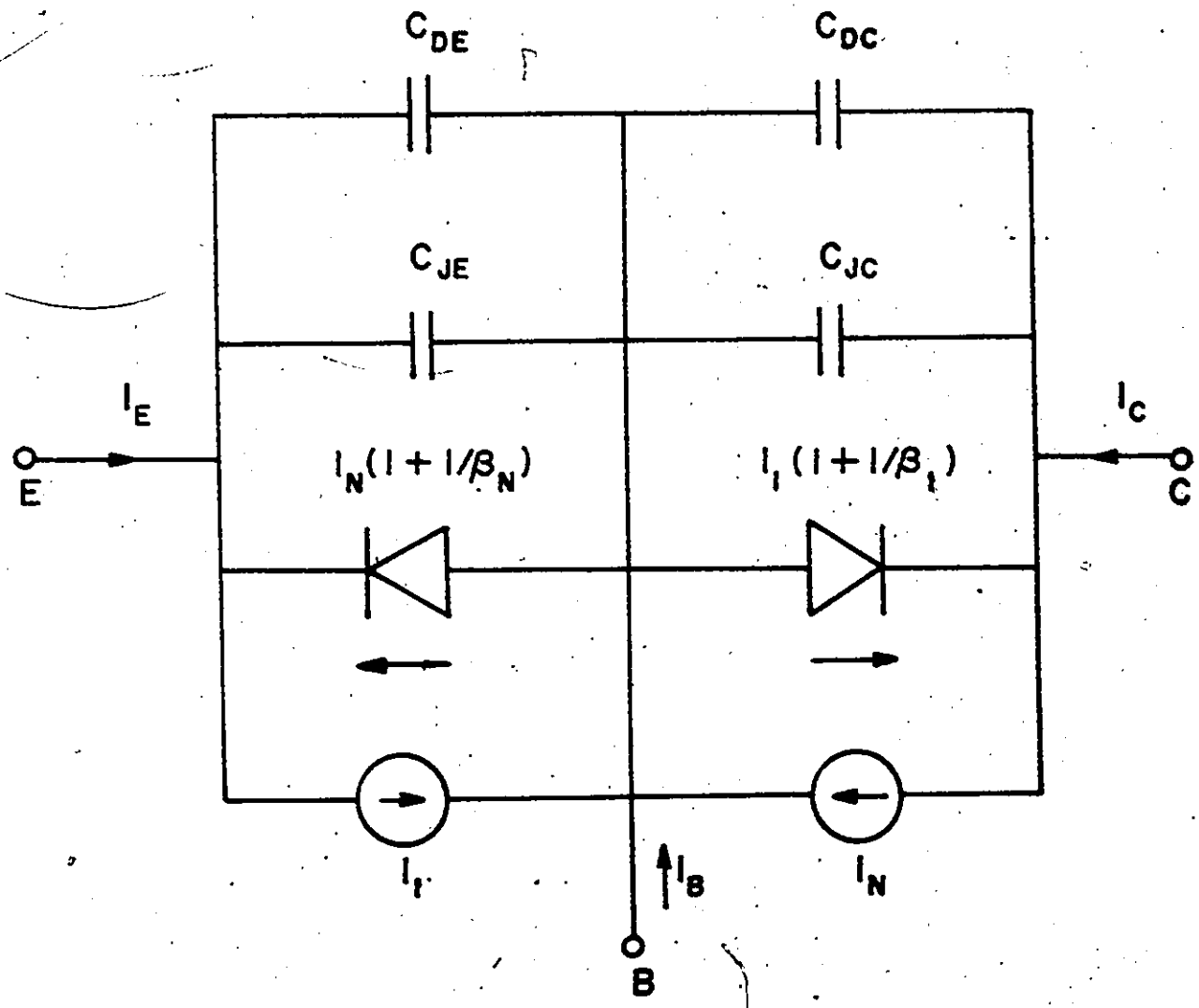


Fig. 2.4 Circuit representation of Ebers-Moll model for dynamic operation.

C_{DE} and C_{DC} are the current dependent capacitances and represent the minority carrier charge stored due to current flow. According to charge control theory [2], the charges are directly proportional to the reference currents such that the capacitances, which are the incremental change of charge with junction voltage, then become

$$C_{DE} = \frac{q}{kT} \tau_F (I_N + I_s)$$

$$C_{DC} = \frac{q}{kT} \tau_R (I_I + I_s)$$

where τ_F and τ_R are the transit times in the forward and reverse direction respectively.

The model described above does not include many non-linear effects in the transistor because of the several assumptions made in the derivation. These effects are, for example, collector current dependent output conductance due to base width modulation (Early effect) [17], space charge layer generation and recombination (Sah-Noyce-Shockley effect) [18], conductivity modulation in the base (Webster effect) [19], base push-out (Kirk effect) [20], and emitter crowding [21,22]. Many of these effects were not identified at the time the Ebers-Moll model was formulated.

Some of these effects have been included into the Ebers-Moll model in various ways. The common approach has been to specify some parameters of the model as function of bias and to describe this bias dependence in tabular form or through parametric expressions. For example, in the NET-1 program [23], the common-emitter current gain is given by a series expansion in the emitter-base voltage. In the CIRCUS program [24], forward and reverse current gains and forward

and reverse transit times are specified as functions of collector current in tabular form. Such "curve-fitting" modeling tends to require a large number of parameters or table entries for an accurate description.

A more complete model which takes into account some of the effects mentioned above, developed by Gummel and Poon, is described in the next section.

2.3 Gummel Poon Model

In this section, a more elaborate model developed by Gummel and Poon and known as the Integral Charge-control Model (ICM) [12], is described. First the description of the static non-linear model is given. Then the small signal model derived from the non-linear model is given.

The ICM takes into account many effects in the bipolar transistor not included in the previously described Ebers-Moll model. The model includes conductivity modulation in the base and collector regions, space charge layer recombination, base push out and avalanche multiplication.

The ICM is based on a charge control relation derived by Gummel [13]. This relation is the result of integrating the current transport equation from the emitter contact to the collector contact under the assumption that the recombination in the transistor is negligible. The result shows that the dominant component I_{CC} of the collector current (i.e., electron current for an n-p-n transistor) is given by [Appendix I]

$$I_{CC} = \text{Const.} \times \frac{\exp(qV'_{EB}/kT) - \exp(qV'_{CB}/kT)}{Q_b} \qquad (2.26)$$

where V'_{EB} is the emitter base junction voltage, V'_{CB} is the collector base junction voltage and Q_b is the total majority carrier charge stored in the base.

(2.26) reduces to the basic Ebers-Moll relation when Q_b is set to Q_{bo} i.e., the total amount of charge stored at equilibrium. [28]

2.3.1. ICM Model Equations

The intrinsic part of the transistor is described by three basic equations that express: (i) collector current, (ii) total stored charge in the base and (iii) the base current.

These three equations are,

$$I_c = I_{cc} - I_{bc} + I_A \tag{2.27a}$$

$$Q_b = Q_{bo} + Q_e + Q_c + B\,\tau_f\,I_f + \tau_r\,I_r \tag{2.27b}$$

$$I_b = I_{be_1} + I_{be_2} - I_A + I_{bc} \tag{2.27c}$$

Following is the explanation of each equation.

(A) The meaning of the terms in the first equation (2.27a) is explained with reference to Fig. 2.5, which shows a schematic side view of an n-p-n transistor and the flow of hole and electron particle currents. The solid lines represent the flow of electrons and the dashed lines the flow of holes. I_{cc} is the dominant current through the transistor and its bias dependence is given by

$$I_{cc} = \frac{I_k^2\,\tau_f}{Q_b}\,\exp(-v_k)\left[\exp\left(\frac{qV'_{EB}}{kT}\right) - \exp\left(\frac{qV'_{CB}}{kT}\right)\right] \tag{2.28}$$

where I_k, τ_f and v_k are the model parameters and Q_b is the total majority carrier charge.

I_{bc} is a small current component that is due to recombination in the collector region and is given by

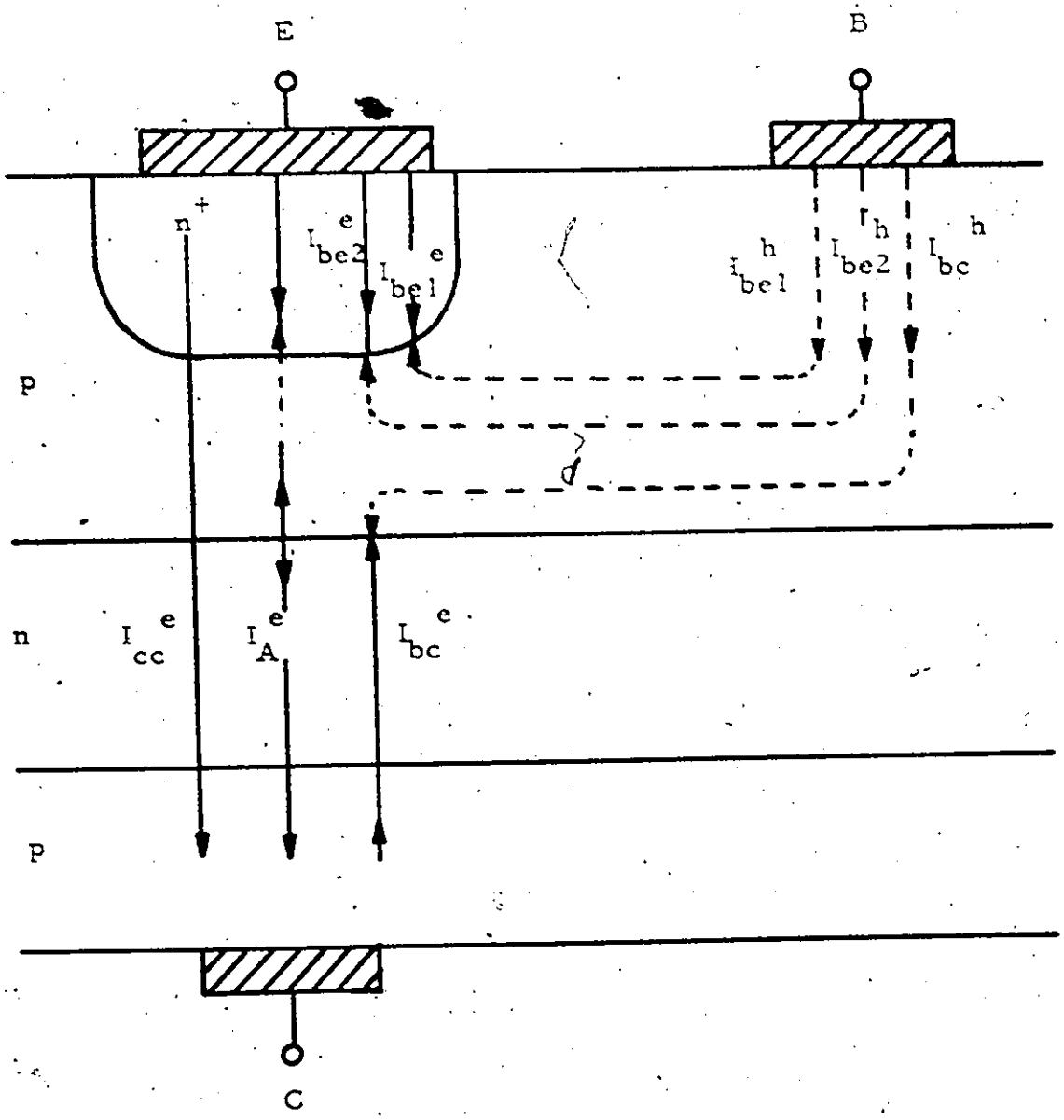


Fig. 2.5 Cross-section of a transistor showing the direction of flow of electron and hole current in the ICM.

$$I_{bc} = -I_k\, i_3 \exp(-v_k/n_c)\,[\exp(qV_{CB}'/n_c kT) - 1] \qquad (2.29)$$

where i_3 and n_c are model parameters.

I_A is the current component generated by impact ionization. Electrons generated by impact ionization flow into the collector and cause an additional current component to the collector current. I_A is given by [25],

$$I_A = \left(\frac{2a_n}{b_n}\right) I_C \left|\frac{kT\, v_{oc}}{q} + V_{CB}'\right| \cdot \left(1 + \frac{\eta E_o}{\sqrt{\left|\frac{kT\, v_{oc}}{q} + V_{CB}'\right|}}\right) \cdot \exp\left(-b_n/E_m\right) \qquad (2.30)$$

where

$$E_m = \sqrt{\left|\frac{2kT\, N_o\, v_{oc}}{\epsilon}\right| \left[1 - V_{CB}'\, q/kT\, v_{oc}\right]^{1/2} \cdot \left[1 - \frac{I_C}{q v_s A_e N_o}\right]^{1/2}}$$

$$- E_o \left[1 - \left(\frac{V_{CB}'\, q}{kT\, v_{oc}}\right)\right]^{1/4} \left[1 - \frac{I_c}{q\, v_s\, A_e\, N_o}\right]^{n_A}$$

and

$$\eta = \frac{3}{4}(\pi\, b_n)^{1/2} \left|\frac{\epsilon}{2\, kT\, N_o\, v_{oc}}\right|^{3/4}$$

where ϵ is the dielectric constant, a_n is the avalanche coefficient, b_n is the critical field for avalanche, and v_s is the saturation velocity for electrons (n-p-n transistor). N_D, E_o, n_A A_e and v_{oc} are model parameters.

(B) The second equation (2.27b) describes the stored charge in the base. The base charge Q_b is modelled according to the charge control concept [2] and is given by

$$Q_b = Q_{bo} + Q_e + Q_c + B\,\tau_f\,I_f + \tau_r\,I_r \qquad (2.31)$$

where Q_{bo} is the equilibrium total stored charge in the base, Q_e the capacitively stored charge of the emitter junction, and Q_c that of the collector junction. $B\,\tau_f\,I_f$ and $\tau_r\,I_r$ represent forward and reverse diffusion capacitance stored charge respectively. τ_f and τ_r are the forward and inverse transit times. B is a factor describing the base push-out effect, which is a monotonically increasing function of $|I_C|$ and a decreasing fucntion of $|V_{CB}|$. The current I_f and I_r are components of the dominant collector current I_{cc}. All the above quantities are expressed as follows.

$$Q_{bo} = -I_k\,\tau_f$$

$$Q_e = -(I_k\,\tau_f)\,R\,(qV_{EB}/kT,\ P_e)$$

$$Q_c = -(I_k\,\tau_f).R\,(qV_{CB}/kT,\ P_c)$$

where:

$$R(v,P)_{\substack{c\\e}} = P_3\left\{\frac{1}{(1+P_4)^{P_2}} + \frac{(v/P_1 - 1)}{\left[\left(\frac{v}{P_1} - 1\right)^2 + P_4\right]^{P_2}}\right\} \qquad (2.32)$$

P_e and P_c are defined in terms of four parameters describing the emitt and collector junction capacitances [26],

$$B = \left\{1 + r_\omega \frac{\left[\sqrt{i_4^2 + r_{p1}} - i_4\right]^{n_p}}{4\left(I_c^2/I_k^2 + r_{p2}\right)}\right\}^2 \qquad (2.33)$$

$$i_4 = \frac{I_c}{I_k} + \frac{(V_{oc} - qV_{CB'}|_{kT})}{V_{rp}} \qquad (2.34)$$

V_{rp}, r_ω, r_{p1}, r_{p2} and n_p are model parameters describing base push out effects.

$$I_r = \frac{I_k^2 \tau_r}{Q_b} \exp(-v_k) \exp(q V_{EB'}|_{kT}) \qquad (2.35)$$

$$I_r = \frac{I_k^2 \tau_r}{Q_b} \exp(-v_k) \exp(q V_{CB'}|_{kT}) \qquad (2.36)$$

(C) The third equation (2.27c) describes the base current and is given by

$$I_b = I_{be_1} + I_{be_2} + I_{bc} - I_A \qquad (2.37)$$

I_{bc} and I_A are given by (2.29) and (2.30)

$$I_{be_1} = I_k i_1 \exp(-v_k) [\exp(q \frac{V_{EB'}}{kT}) - 1] \qquad (2.38)$$

$$I_{be_2} = -I_k i_2 \exp(-v_{k/n_e}) [\exp(q \frac{V_{EB'}}{kT}) - 1] \qquad (2.39)$$

i_1, i_2 and n_e are model parameters.

Thus the ICM is described by three main equations (2.27a), (2.27b) and (2.27c).

The defination of the parameters can be found in the references quoted in the preceding text, and have not been repeated here.

2.3.2 Iterative Scheme for the ICM :

In order to use the above model in the circuit analysis program , one has to solve non-linear equations. It has been found that a simple iterative scheme tends to be very slow or may lead to an oscillatory solution [Appendix II]. Thus better iterative schemes are required to solve the equations. A fast algorithm has been developed and is described in detail in Appendix II.

2.4. Small Signal Gummel-Poon Model

In this section, a small signal model derived from the ICM is given. In the following derivation, the avalanche effects are not included in order to simplify the calculations.

In order to derive the small signal model, the collector junction is assumed to be reverse biased. The ICM equations in the active mode (assuming $I_I = 0$) may be obtained from [27] as ,

$$I_c = \lambda I_N \tag{2.40}$$

$$I_E = -\lambda \left[1 + \frac{1}{\beta_N} \right] I_N \tag{2.41}$$

$$I_B = \frac{\lambda I_N}{\beta_N} \tag{2.42}$$

where

$$I_N = I_s \left[e^{\frac{V_{EB}}{V_T}} - 1 \right] \tag{2.43}$$

$$\frac{\lambda}{\beta_N} = \frac{I_1}{I_s} + \frac{I_2}{I_N} \left[\left(1 + \frac{I_N}{I_s} \right)^{\frac{1}{n_e}} - 1 \right] \tag{2.44}$$

$$\lambda = \frac{2}{k + \sqrt{k^2 + 4B \frac{I_N}{I_k}}} \tag{2.45}$$

$$k = 1 + q_e + q_c \tag{2.46}$$

$$\left.\begin{matrix} q_e \\ q_c \end{matrix}\right\} = p_3 \left[\frac{1}{(1+p_4)^{p_2}} + \frac{\frac{v}{p_1} - 1}{\left[\left(\frac{v}{p_1} - 1\right)^2 + p_4\right]^{p_2}} \right] \tag{2.47}$$

$$B = \left\{ 1 + \frac{R_\omega}{4} \frac{\left[\left\{ (I_c + I_1)^2 + I_2^2 \right\}^{1/2} - (I_c + I_1) \right]^2}{(I_c^2 + I_2^2)} \right\} \tag{2.48}$$

$$I_1 = A_e \frac{(V_{oc} - V_{CB})}{\rho w_c} \tag{2.49}$$

The circuit representation of equations (2.40) to (2.42) is shown in Fig. 2.6. The incremental behavior of the two current sources in Fig. 2.6 has to be evaluated to give the small signal model. The linear equivalents of the current sources are derived from the following equations.

$$\delta I_B \cong \delta V_{BE} \frac{\partial I_B}{\partial V_{BE}} + \delta V_{CE} \frac{\partial I_B}{\partial V_{CE}} \tag{2.50}$$

$$\delta I_c = \delta V_{BE} \frac{\partial I_c}{\partial V_{BE}} + \delta V_{CE} \frac{\partial I_e}{\partial V_{CE}} \tag{2.51}$$

The above equations may be expressed as

$$\delta I_B = \delta V_{BE} / r_{be} \tag{2.52}$$

$$\delta I_c = \delta V_{BE} \cdot g_m + \delta V_{CE} / r_o \tag{2.53}$$

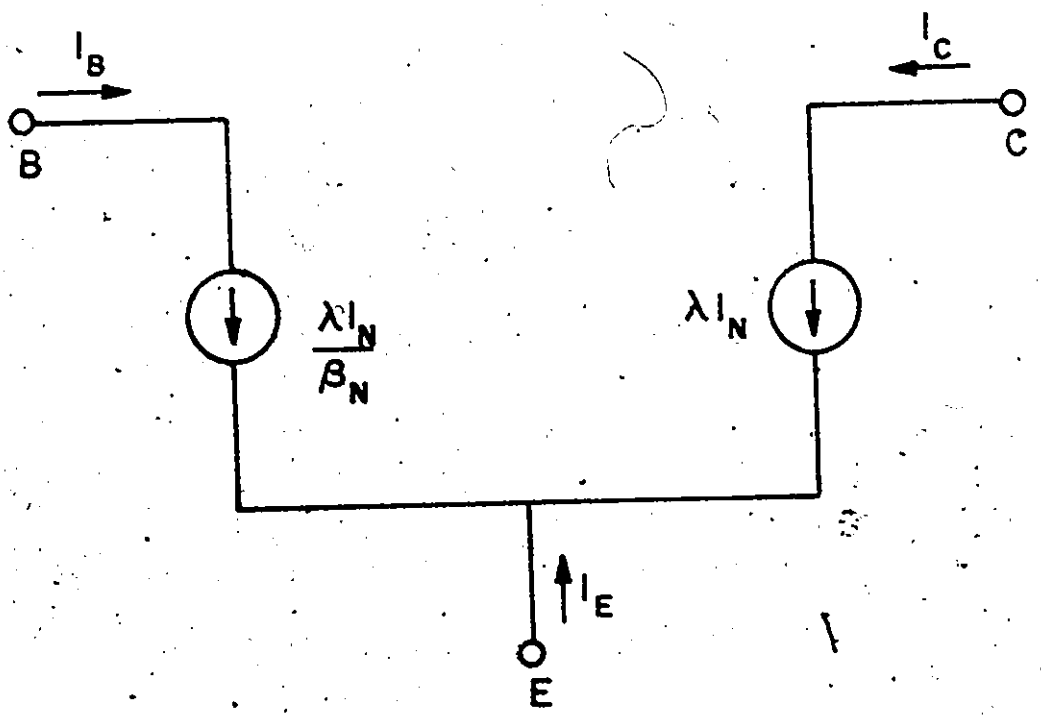


Fig. 2.6 Equivalent d.c. representation of ICM in active region.

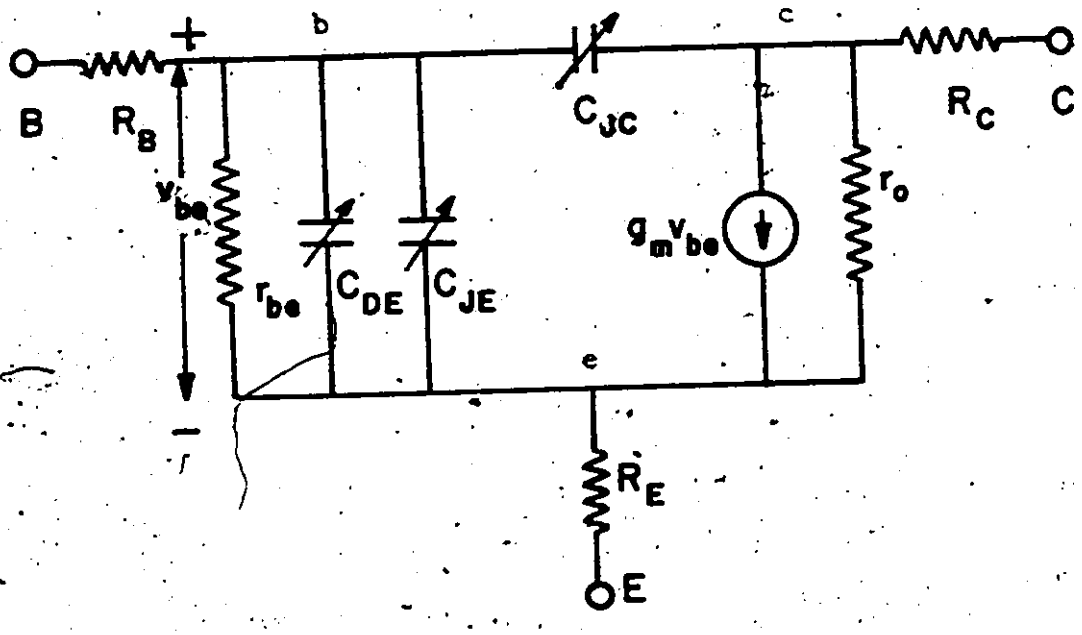


Fig. 2.7 Hybrid-π ICM small signal model.

where

$$r_{be} = \frac{\partial V_{BE}}{\partial I_B}$$

$$g_m = \frac{\partial I_c}{\partial V_{BE}}$$

and $$r_o = \frac{\partial V_{CE}}{\partial I_c}$$

'δ' signifies an incremental change. The second term on right hand side of equation (2.50) is nil when $I_I = 0$.

The small signal model defined by (2.52) and (2.53) is shown in Fig. 2.7.

The figure also shows the depletion layer capacitances C_{JE}, C_{JC}, the diffusion capacitance C_{DE} and the extrinsic resistances R_B, R_E and R_C.

2.4.1 Calculation of r_{be}

In the following the expressions for r_{be}, g_m and r_o will be derived.

$$r_{be} = \frac{\partial V_{BE}}{\partial I_B} \Big| \delta v_{ce} = o \qquad (2.54)$$

From (2.42) and (2.44)

$$\frac{\partial I_B}{\partial I_N} = \frac{I_1}{I_s} + \frac{I_2}{n_e} \left(1 + \frac{I_N}{I_s}\right)^{\frac{1}{n_e}} \cdot \frac{1}{I_s} \qquad (2.55)$$

From (2.43)

$$\frac{\partial I_N}{\partial V_{BE}} = \frac{I_N}{V_T} \qquad (2.56)$$

From (2.54) we get

$$\frac{1}{r_{be}} = \frac{1}{V_T} \cdot \frac{I_N}{I_s} \left\{ I_1 + \frac{I_2}{n_e} \left(1 + \frac{I_N}{I_s}\right)^{\frac{1}{n_e}} \cdot \frac{1}{I_s} \right\} \quad (2.57)$$

2.4.2 Calculation of g_m (2.58)

$$g_m = \frac{\partial I_C}{\partial V_{BE}} \Big| \delta v_{ce} = 0$$

From (2.40)

$$g_m = \lambda \frac{\partial I_N}{\partial V_{BE}} + I_N \frac{\partial \lambda}{\partial V_{BE}} \quad (2.59)$$

we may write also

$$g_m = \frac{\partial I_N}{\partial V_{BE}} \left[\lambda + I_N \frac{\partial \lambda}{\partial I_N} \right] \quad (2.60)$$

Since λ is function of B and B is function of I_C, therefore,

$$\frac{\partial \lambda}{\partial I_N} = \frac{\partial \lambda}{\partial I_N} + \frac{\partial \lambda}{\partial B} \cdot \frac{\partial B}{\partial I_N} \quad (2.61)$$

and $$\frac{\partial B}{\partial I_N} = \frac{\partial B}{\partial I_c} \cdot \frac{\partial I_c}{\partial I_N} \quad (2.62)$$

From (2.45) $$\frac{\partial \lambda}{\partial I_N} = - \frac{\lambda^3}{2-k\lambda} \cdot \frac{B}{I_k} \quad (2.63)$$

$$\frac{\partial \lambda}{\partial B} = - \frac{\lambda^3}{2-k\lambda} \cdot \frac{I_N}{I_k} \quad (2.64)$$

from (2.40) $$\frac{\partial I_c}{\partial I_N} = \lambda + I_N \frac{\partial \lambda}{\partial I_N} \quad (2.65)$$

From (2.48) $$\frac{\partial B}{\partial I_c} = -4\sqrt{B}\left(\sqrt{B}-1\right)\left\{\frac{1}{\left[(I_c+I_1)^2+I_2^2\right]^{1/2}}+\frac{I_c}{I_c^2+I_2^2}\right\} \quad (2.66)$$

Using (2.61) to (2.65) we obtain,

$$\frac{\partial \lambda}{\partial I_N} = -\frac{\lambda^3}{2-k\lambda}\cdot\frac{B}{I_k} - \frac{\lambda^3}{2-k\lambda}\cdot\frac{I_N}{I_k}\left(\lambda + I_N\frac{\partial \lambda}{\partial I_N}\right)\frac{\partial B}{\partial I_c}$$

From which

$$\frac{\partial \lambda}{\partial I_N} = \frac{\lambda - \frac{\lambda^3}{2-k\lambda}\cdot\frac{I_N}{I_k}\cdot B}{1+\frac{\lambda^3}{2-k\lambda}\frac{I_N^2}{I_k}\frac{\partial B}{\partial I_c}} \quad (2.67)$$

Thus using (2.67) and (2.56) in (2.60), we get

$$g_m = \frac{I_N}{V_T}\left[\frac{\lambda - \frac{\lambda^3}{2-k\lambda}\cdot\frac{I_N}{I_k}\cdot B}{1+\frac{\lambda^3}{2-k\lambda}\frac{I_N^2}{I_k}\frac{\partial B}{\partial I_c}}\right] \quad (2.68)$$

where $\frac{\partial B}{\partial I_c}$ is given by (2.66)

2.4.3 Calculation of 'r_o'

$$\frac{1}{r_o} = \frac{\partial I_c}{\partial V_{CE}} \simeq \frac{\partial I_c}{\partial V_{CB}} \quad \text{for } V_{EB} << V_{CB}$$

From (2.40)

$$\frac{\partial I_c}{\partial V_{CB}} = I_N\cdot\frac{\partial \lambda}{\partial V_{CB}} \quad (2.69)$$

$$\frac{\partial \lambda}{\partial V_{CB}} = \frac{\partial \lambda}{\partial B}\cdot\frac{\partial B}{\partial V_{CB}} + \frac{\partial \lambda}{\partial k}\cdot\frac{\partial k}{\partial V_{CB}} \quad (2.70)$$

$$\frac{\partial B}{\partial V_{CB}} = \frac{\partial B}{\partial I_1} \cdot \frac{\partial I_1}{\partial V_{CB}} \qquad (2.71)$$

From (2.45) to (2.49) we have,

$$\frac{\partial \lambda}{\partial k} = \frac{\lambda^2}{2 - k\lambda} \qquad (2.72)$$

$$\frac{\partial B}{\partial I_1} = -4\sqrt{B}\,(\sqrt{B}-1) \cdot \frac{1}{\left[(I_c + I_1)^2 + I_2^2\right]^{1/2}} \qquad (2.73)$$

$$\frac{\partial I_1}{\partial V_{CB}} = -\frac{A_e}{\rho w_c} \qquad (2.74)$$

$$\frac{\partial k}{\partial V_{CB}} = \frac{p_{c3}}{p_{c1}\left[\left(\frac{v_c}{p_{c1}} - 1\right)^2 + p_{c4}\right]^{p_{c2}}} \left\{1 - \frac{\left(\frac{v_c}{p_{c1}} - 1\right)^2 p_{c2}}{\left(\frac{v_c}{p_1} - 1\right)^2 + p_{c2}}\right\} \qquad (2.75)$$

From (2.69) to (2.74) we obtain,

$$\frac{1}{r_o} = I_N \left\{\frac{\lambda^3}{2-k\lambda} \frac{I_N}{I_k} \frac{A_e}{\rho w_c}\left[\frac{-4\sqrt{B}\,(\sqrt{B}-1)}{\{(I_c+I_1)^2 + I_2^2\}^{1/2}}\right] - \frac{\lambda^2}{2-k\lambda} \frac{\partial k}{\partial V_{CB}}\right\} \qquad (2.76)$$

2.4.4 Depletion Layer and Diffusion Capacitances

The depletion layer capacitances C_{JE} and C_{JC} are obtained as [26].

$$C_{JE} = \frac{dq_e}{dV_{BE}} \tag{2.77}$$

$$C_{JC} = \frac{dq_c}{dV_{CB}} \tag{2.78}$$

where q_e and q_c are the stored charges associated with emitter-base and collector-base junction capacitances respectively and are given by (2.47).

The diffusion capacitance C_{DE} is obtained from the base charge ($\tau_f BI_f$) associated with the component I_f of the dominant current [27].

All the elements of the small signal model are obtained from the non-linear static equations and thus no additional parameters are required for the small signal analysis using the Gummel-Poon Model.

CHAPTER 3

PROPOSED BIPOLAR TRANSISTOR MODEL AND ITS PARAMETER DETERMINATION

In this Chapter, a bipolar transistor model based on the Ebers-Moll transport model modified by a simplified charge control relation is developed. The base width modulation, the low current fall-off of β and the avalanche multiplication effects are incorporated in the model in such a manner that the terminal current equations are convenient for computation [29].

The model is then modified for transient analysis. A small signal hybrid-π model is also derived from the non-linear model. Techniques for determining the model parameters are given. A number of transistor characteristics have been calculated using the model and the results obtained in the case of a 2N3118 transistor are compared with experimental values. Following is the development of the model.

3.1 Development of the Model

In order to derive the model equations the Ebers-Moll transport model described in Chapter 2 will be used. The transport model for n-p-n transistors is represented by the following equations

$$I_C = I_N - \left(1 + \frac{1}{\beta_I}\right) I_I \tag{3.1}$$

$$I_E = -\left(1 + \frac{1}{\beta_N}\right) I_N + I_I \tag{3.2}$$

$$I_B = -I_C - I_E \tag{3.3}$$

where

$$I_N = I_s \exp (\theta V_{EB} - 1) \qquad (3.4)$$

$$I_I = I_s \exp (\theta V_{CB} - 1) . \qquad (3.5)$$

β_N and β_I are the current gains in the forward and reverse direction respectively and θ is equal to $\frac{q}{kT}$. In Fig. 3.1 the circuit representation of the above model is shown. Fig. 3.2, shows the components of the currents in the transistor.

The above model does not include high injection effects, ' β ' fall-off at low current, the Early effect etc. Means of incorporating these effects in the above equations will be developed in the following sections.

3.1.1 High Current Effects : Base conductivity modulation, which is in part responsible for the fall-off of ' β ' at high current, is incorporated by using the Gummel charge control relation [13]. The Gummel expression relates the dominant current in the transistor with the base charge, which is dependent on injected carriers into the base and the junction voltages. Since no assumptions of low level injection is made, the high level effects are taken into account automatically. The charge control relation is given by

$$I_{CC} = I_s \frac{Q_{bo}}{Q_b} [e^{\theta V_{EB}} - e^{\theta V_{CB}}] , \qquad (3.7)$$

using (3.4) and (3.5) we can write

$$I_{CC} = \lambda [I_N - I_I] \qquad (3.8)$$

where $\lambda = \frac{Q_{bo}}{Q_b}$, ' Q_{bo} ' being the fixed charge in the base

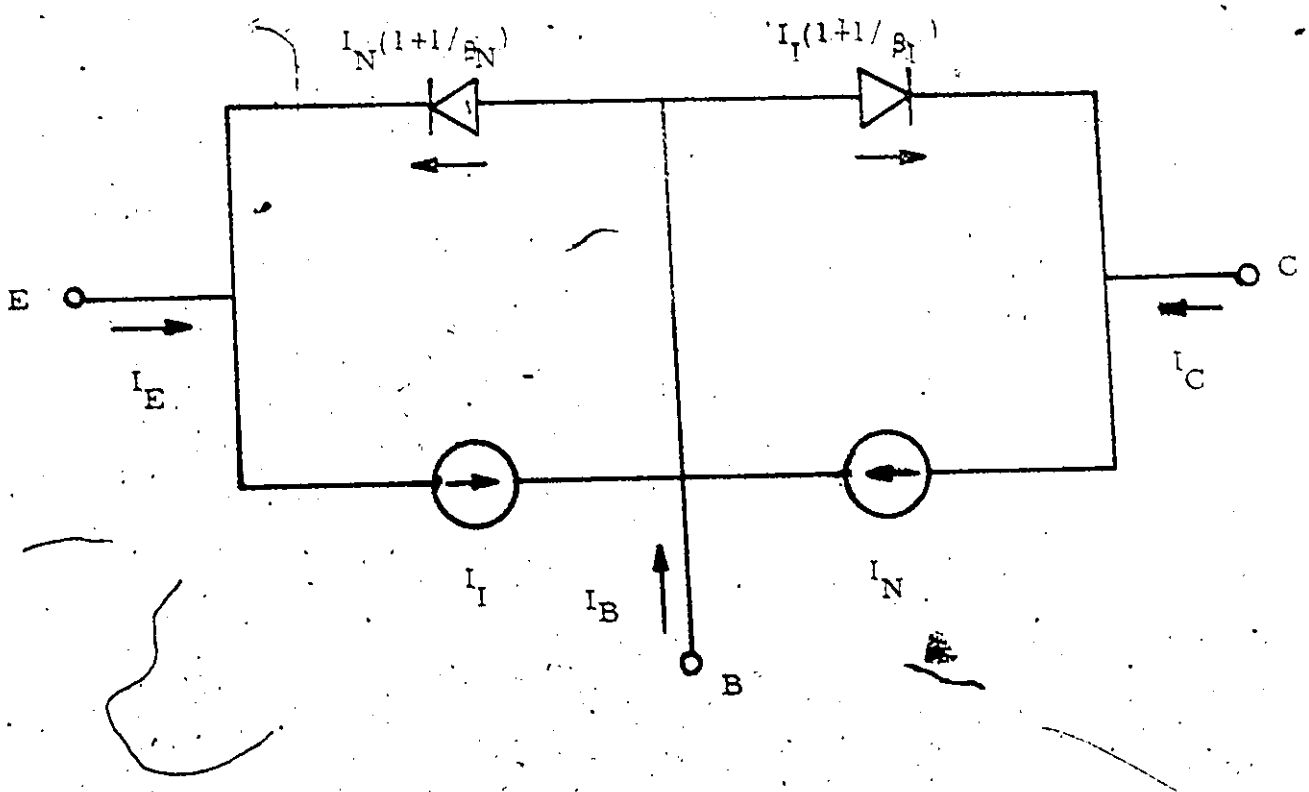


Fig. 3.1 Circuit representation of the transport model.

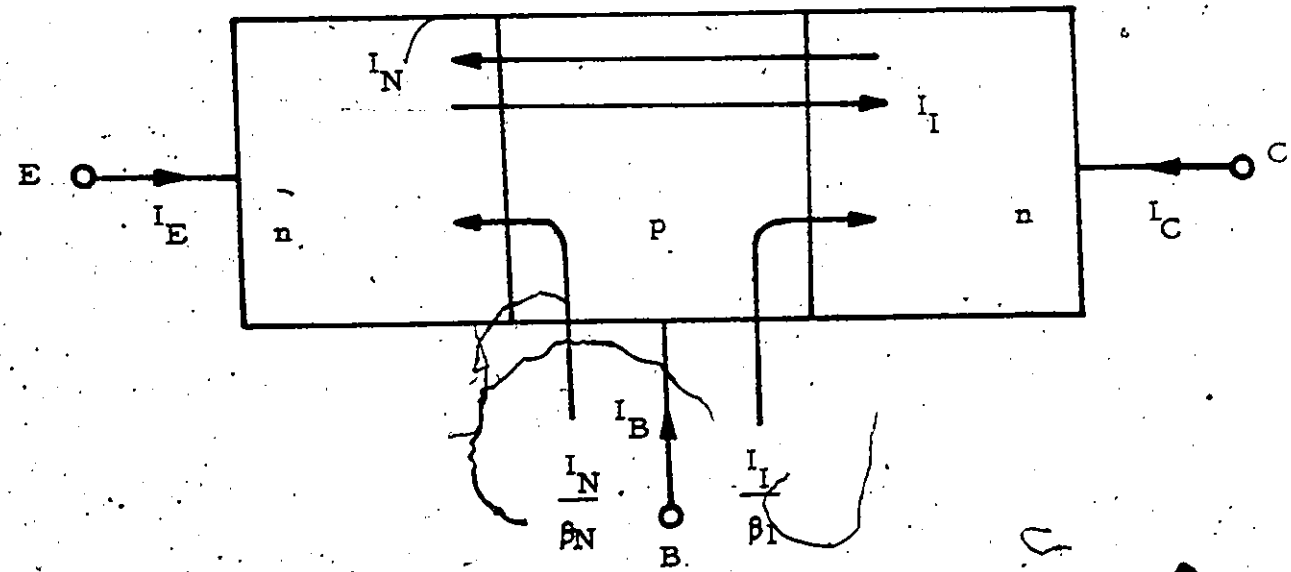


Fig. 3.2 Current components in the transistor.

region and Q_b is the base charge under bias condition.

Rewriting (3.1) and (3.2)

$$I_C = (I_N - I_I) - \frac{I_I}{\beta_I} \tag{3.9}$$

$$I_E = -\frac{I_N}{\beta_N} - (I_N - I_I) \tag{3.10}$$

In (3.9) and (3.10), the dominant component is $(I_N - I_I)$. Comparing with (3.8), the high current effects are incorporated by changing $(I_N - I_I)$ in (3.9) and (3.10) to $\lambda (I_N - I_I)$.

Thus the model equations become

$$I_C = \lambda(I_N - I_I) - \frac{I_I}{\beta_I} \tag{3.11}$$

$$I_E = -\frac{I_N}{\beta_N} - \lambda (I_N - I_I) \tag{3.12}$$

$$I_B = -I_E - I_C \tag{3.13}$$

Now the expression for λ will be derived. According to the charge control theory [30], the total charge Q_b in the base may be expressed

$$Q_b = Q_{bo} + \tau_f (\lambda I_N) + \tau_r (\lambda I_I) \tag{3.14}$$

where τ_f and τ_r are the transit times in the forward and reverse direction respectively.

Defining,

$$I_{kN} = \frac{Q_{bo}}{\tau_f} \qquad (3.14a)$$

$$I_{kI} = \frac{Q_{bo}}{\tau_r} \qquad (3.14b)$$

(3.14) may be expressed as

$$\frac{1}{\lambda} = 1 + \lambda \frac{I_N}{I_{kN}} + \lambda \frac{I_I}{I_{kI}}$$

from which,

$$\lambda = \frac{2}{1 + \sqrt{1 + 4\left(\frac{I_N}{I_{kN}} + \frac{I_I}{I_{kI}}\right)}} \qquad (3.15)$$

It may be seen that under low injection condition i.e. $I_N << I_{kI}$ and $I_I << I_{kI}$, λ is equal to unity. I_{kN} and I_{kI} are the parameters indicating the start of high injection condition.

3.1.2 Base Width Modulation

The slight increase in collector current with the increase of collector to emitter voltage can be incorporated in equations (3.11) and (3.12) by using Lindholm and Hamilton's [31] approach. Since the dominant component of the collector current $\lambda (I_N - I_I)$ can be assumed to be larger than the other components, the variation of I_C with V_{CE} in the normal and inverted mode may be taken into account by two more parameters V_{AN} and V_{AI}, which are the Early voltages in the normal and inverted

mode respectively. Modifying λI_N by $\lambda I_N (1 + \frac{V_{CE}}{V_{AN}})$ and λI_I by $\lambda I_I(1 + \frac{V_{EC}}{V_{AI}})$ in (3.11) and (3.12), we get

$$I_C = \lambda \left[1 + \frac{V_{CE}}{V_{AN}}\right] I_N - \lambda \left[1 + \frac{1}{\lambda \beta_I} + \frac{V_{EC}}{V_{AI}}\right] I_I \quad (3.16)$$

$$I_E = -\lambda \left[1 + \frac{V_{CE}}{V_{AN}} + \frac{1}{\lambda \beta_N}\right] I_N + \lambda \left[1 + \frac{V_{EC}}{V_{AI}}\right] I_I \quad (3.17)$$

$$I_B = \frac{I_N}{\beta_N} + \frac{I_I}{\beta_I} \quad (3.18)$$

3.1.3 Low Current Effects

At low current, recombination in the depletion layers may not be neglected since it causes the ' β ' of the transistor to decrease. As shown in Fig. 3.3, log β_N varies approximately linearly with log I_C at low currents. Using Bode's plot analogy [32], β_N can be modeled to take into account the variation of ' β_N ' with I_C by the following expression

$$\beta_N = \frac{\beta_{N0} \left[1 + \left(\frac{I_1}{I_N}\right)^2\right]^{m/2}}{\left[1 + \left(\frac{I_2}{I_N}\right)^2\right]^{m/2}} \quad (3.19)$$

where, as shown in Fig. 3.3, β_{N0} is the maximum current gain, I_2 is the corner current value and m is the slope. I_1 is taken to be any value less than I_2 in the linear region. In a similar manner,

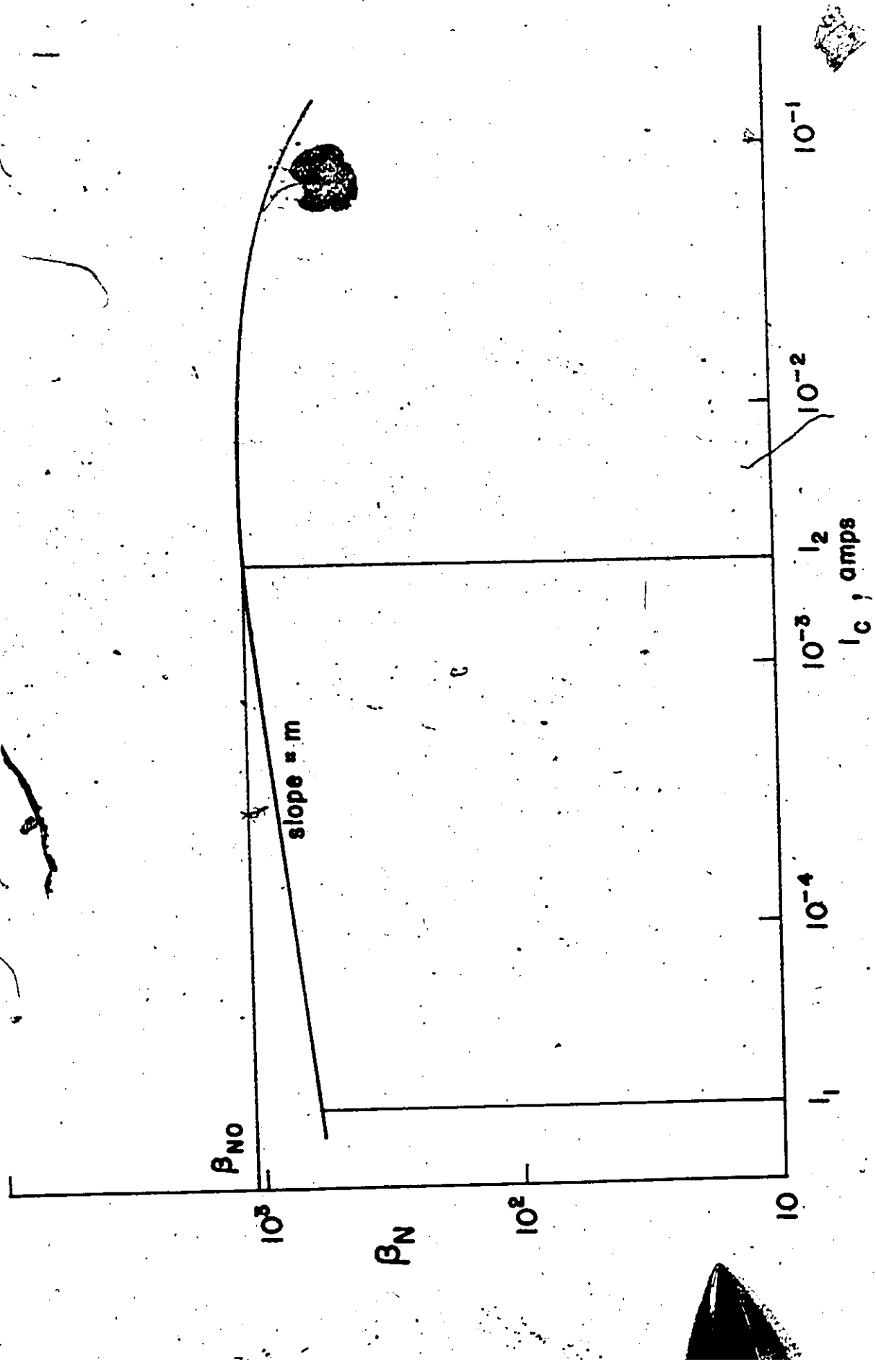


Fig. 3.3 Log β_N vs $\log_{10} I_C$ plot.

$$\beta_I = \frac{\beta_{I0}\left[1 + \left(\frac{I_3}{I_I}\right)^2\right]^{n/2}}{\left[1 + \left(\frac{I_4}{I_I}\right)^2\right]^{n/2}} \qquad (3.20)$$

with I_3, I_4, β_{I0} and n defined as above but with the transistor operated in the inverse mode.

3.1.4 Avalanche Multiplication

If the reverse-bias voltage of the collector base junction is made sufficiently large, significant avalanche multiplication of the collector current carriers may take place as they travel through the space-charge layer.

Avalanche multiplication of current carriers in the collector base junction is incorporated by using a factor M as given by Fossum [14]:

$$M = 1 + \exp\left[A_C (V_{CB} - V_M)\right] \qquad (3.21)$$

for $V_{CB} << V_M$, $M = 1$

where A_C and V_M are parameters and are positive constants. The model is then represented by the following terminal current equations,

$$I_C = \lambda\left[1 + \frac{V_{CE}}{V_{AN}}\right] M \cdot I_N - \lambda\left[1 + \frac{1}{\lambda\beta_I} + \frac{V_{EC}}{V_{AI}}\right] I_I \qquad (3.22)$$

$$I_E = -\lambda\left[1 + \frac{V_{CE}}{V_{AN}} + \frac{1}{\lambda\beta_N}\right] I_N + \lambda\left[1 + \frac{V_{EC}}{V_{AI}}\right] I_I \qquad (3.23)$$

$$I_B = -I_E - I_C \qquad (3.24)$$

where,

$$I_N = I_s \exp\left(\theta V_{EB}^{-1}\right) \qquad (3.25)$$

$$I_I = I_s \exp(\theta V_{CB} - 1) \tag{3.26}$$

$$\beta_N = \frac{\beta_{N0}\left[1 + \left(\frac{I_1}{I_N}\right)^2\right]^{m/2}}{\left[1 + \left(\frac{I_2}{I_N}\right)^2\right]^{m/2}} \tag{3.27}$$

$$\beta_I = \frac{\beta_{I0}\left[1 + \left(\frac{I_3}{I_I}\right)^2\right]^{n/2}}{\left[1 + \left(\frac{I_4}{I_I}\right)^2\right]^{n/2}} \tag{3.28}$$

$$\lambda = \frac{2}{1 + \sqrt{1 + 4\left(\frac{I_N}{I_{kN}} + \frac{I_I}{I_{kI}}\right)}} \tag{3.29}$$

and

$$M = 1 + \exp\left[A_C (V_{CB} - V_M)\right] \tag{3.30}$$

The intrinsic model parameters are I_s, θ, I_{kN}, I_{kI}, V_{AN}, V_{AI}, I_1, I_2, I_3, I_4, m, n, V_M and A_C. The circuit representation of the model is shown in Fig. 3.4.

The effects of the resistivity of the bulk material in the base, emitter and collector regions are taken into account by adding the resistances R_B, R_E and R_C to the intrinsic model of Fig. 3.4 as shown in Fig. 3.4a.

3.2 Transient Operation

As discussed in section 2.1.2, two types of charge storage in the transistor need to be taken into account for transient analysis. These are

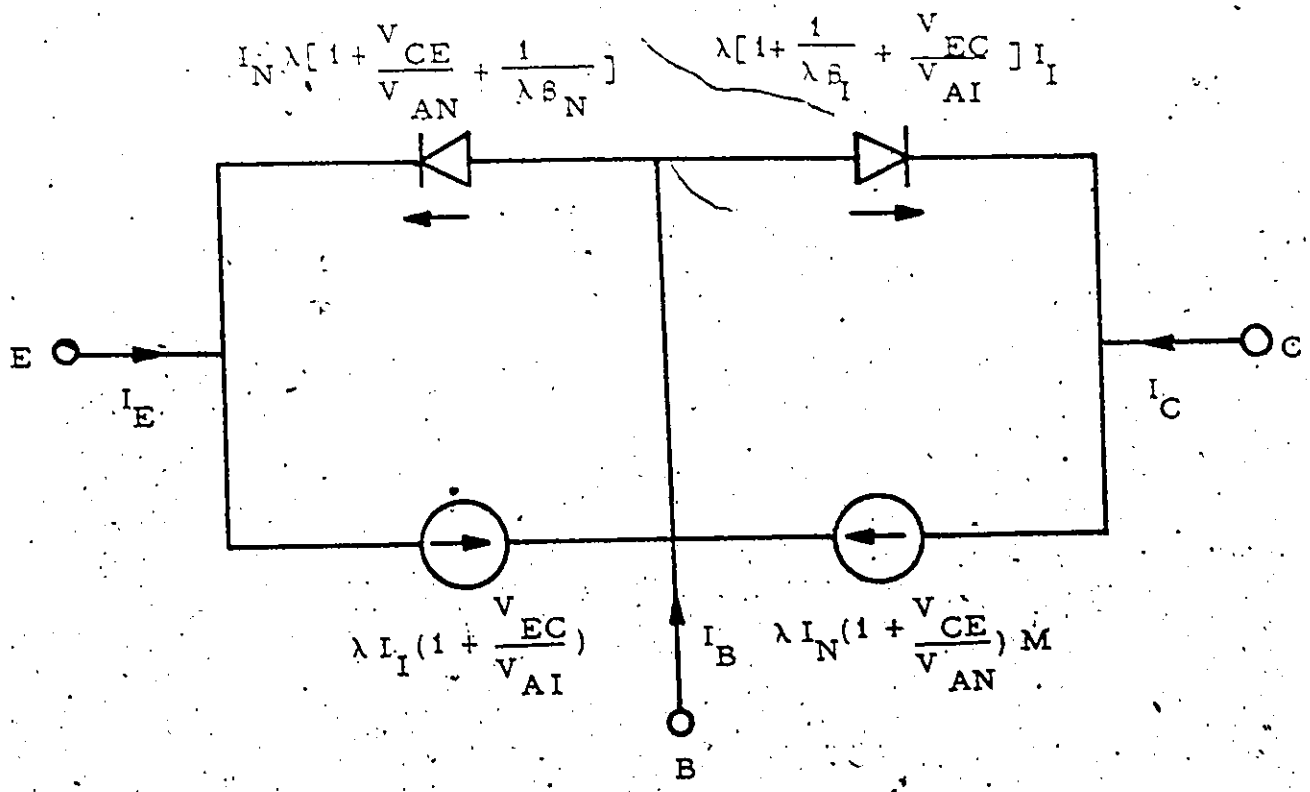


Fig. 3.4 Circuit representation of the intrinsic model.

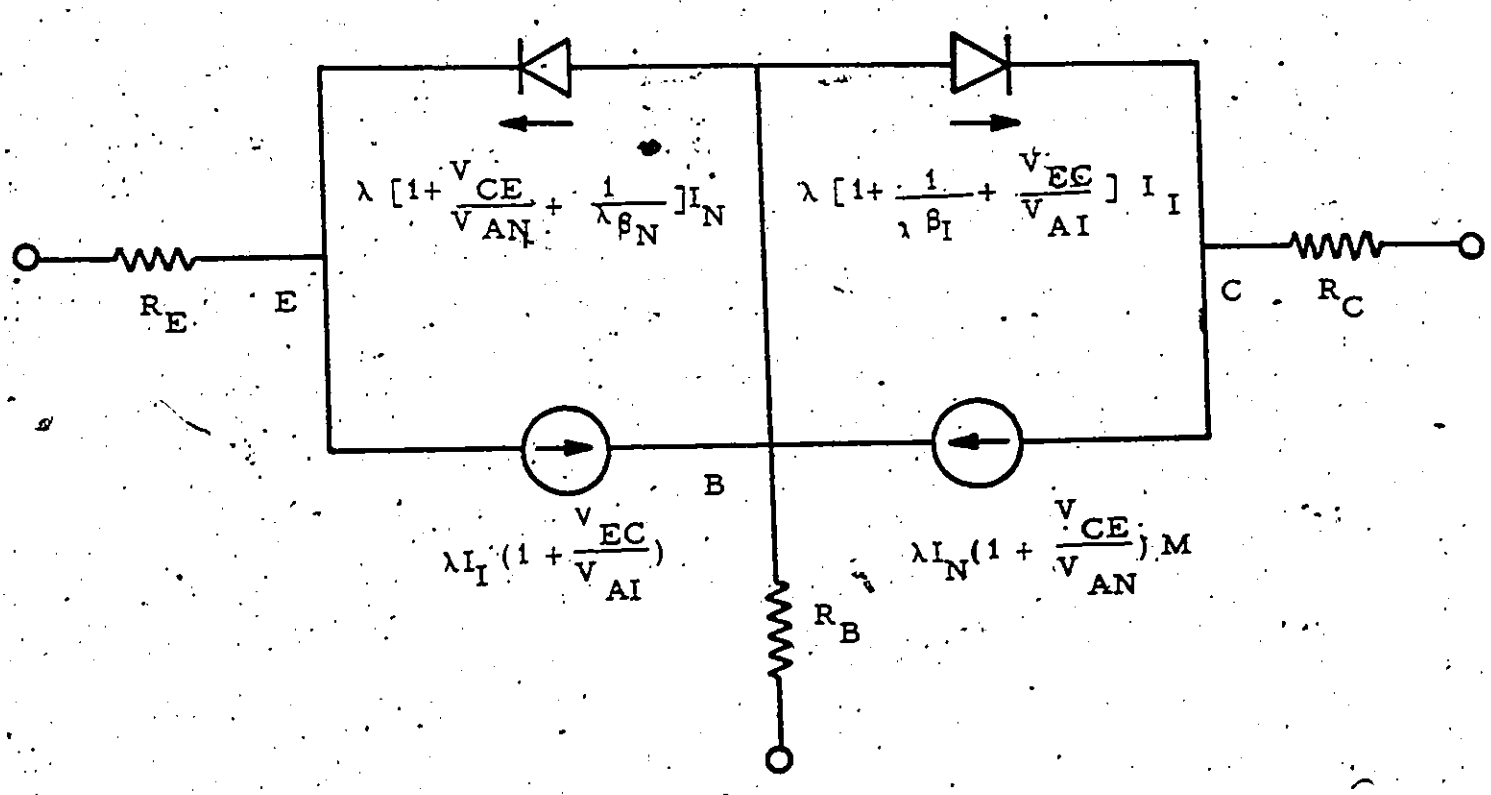


Fig. 3.4a Circuit representation of the model including parasitic resistances.

1. Fixed charges in the depletion region

2. Mobile charges in the base region.

Fixed charges in the depletion region are represented by C_{JE} and C_{JC} as shown in Fig. 3.5. C_{JE} is the emitter-base depletion layer capacitance. These capacitances are given by the following expression [26],

$$C_J = \frac{C_O}{(a+b)^{n/2}} \left[1 + \frac{n}{1-n} \frac{b}{a+b}\right] \quad (3.31)$$

where $a = \left[\frac{V}{\phi} - 1\right]^2$ (3.32)

$$b = \frac{1}{[(1-n) r]^{2/n}} \quad (3.33)$$

C_O = zero bias capacitance

n = grading coefficient

ϕ = built in potential

$r = \frac{\text{max. junction capacitances in forward bias}}{C_O}$

V = Voltage across junction

The advantage of using (3.31) over (2.20) is that at the built in potential, the capacitance does not approach infinity as in (2.20).

The mobile charges in the base region are represented by two capacitances C_{DE} and C_{DC} as shown in Fig. 3.5.

These capacitances are given by [33] :

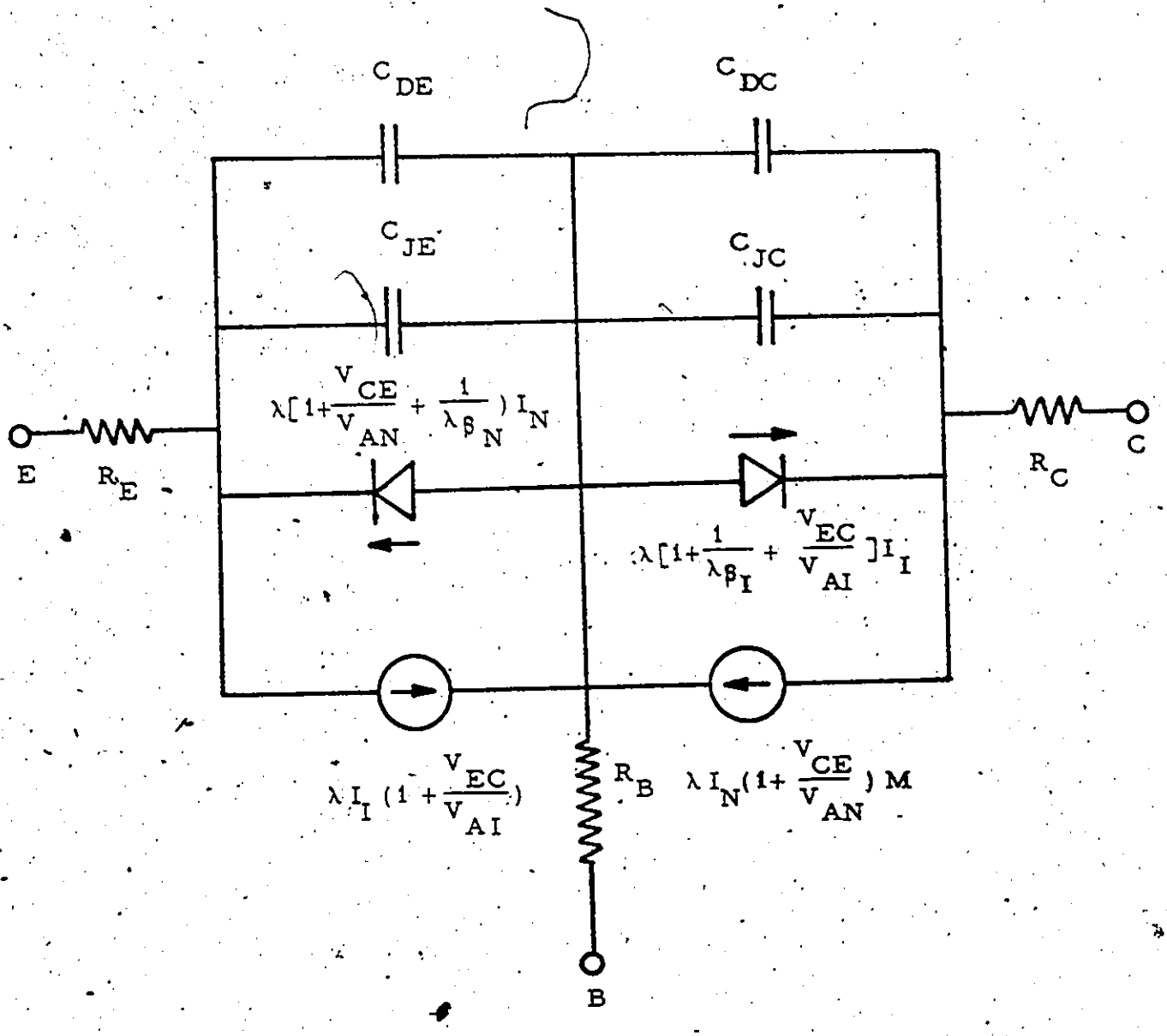


Fig. 3.5 Transistor model under dynamic operation.

$$C_{DE} = \frac{dQ_B}{dV_{EB}} = \tau_F \frac{dI_C}{dV_{EB}} = \tau_F g_{mF} \qquad (3.34)$$

$$C_{DC} = \frac{dQ_B}{dV_{CB}} = \tau_r \frac{dI_C}{dV_{CB}} = \tau_r g_{mr} \qquad (3.35)$$

Where τ_F and τ_r are the transit times in the forward and in the reverse mode respectively. Similarly, g_{mF} and g_{mr} are the transconductances in the forward and inverse mode.

The expressions for g_{mF} and g_{mr} are derived as g_3 and g_4 respectively in the next chapter in section 4.3.

A total of ten additional parameters ϕ_E, ϕ_C, n_E, n_C, r_E, r_C, C_{0E}, C_{0C}, τ_F and τ_r are required for transient operation analysis.

3.3 Small Signal Model

In this section, a small signal hybrid model will be derived. The hybrid -π type of model is particularly chosen here because it can readily be derived from the non-linear model given in Fig. 3.5. The model is the incremental version of the non-linear model and so once the characterization of the non-linear static model is achieved, the complete information for small signal analysis is also available.

In the active region, the collector junction is assumed to be reverse biased and from (3.26) and (3.34) we have

$$I_I = 0$$

$$C_{DC} = 0$$

At low frequency, the currents are,

$$I_C = \lambda \left[1 + \frac{V_{CE}}{V_{AN}} \right] I_N M \qquad (3.35)$$

$$I_E = -\lambda \left[1 + \frac{V_{CE}}{V_{AN}} + \frac{1}{\lambda \delta_N} \right] I_N \qquad (3.36)$$

$$I_B = \frac{I_N}{\delta_N} + (1 - M) \left[1 + \frac{V_{CE}}{V_{AN}} \right] \lambda I_N \qquad (3.37)$$

Fig. 3.5 can be simplified and redrawn to satisfy (3.35) to (3.37). The result is given in Fig. 3.6.

As discussed in section 2.4, the incremental behaviour of the two current sources of Fig. 3.6 has to be evaluated in order to obtain the small signal model parameters. The linear equivalents of the current sources are obtained from (2.50) and (2.51) as

$$\delta I_B = \delta V_{BE} / r_{be} \qquad (3.38)$$

$$\delta I_C = \delta V_{BE} \cdot g_m + \delta V_{CE} / r_o \qquad (3.39)$$

where $r_{be} = \dfrac{\partial V_{BE}}{\partial I_B}$

$g_m = \dfrac{\partial I_C}{\partial V_{BE}}$

and $r_o = \dfrac{\partial V_{CE}}{\partial I_C}$

' δ ' signifies an incremental change.

Fig. 3.7 shows the small signal model represented by eqns. (3.38) and (3.39). It may be noted that the extrinsic base spreading resistance R_b is also added in the circuit. Now the expressions for the linear elements r_{be}, g_m and r_o will be derived.

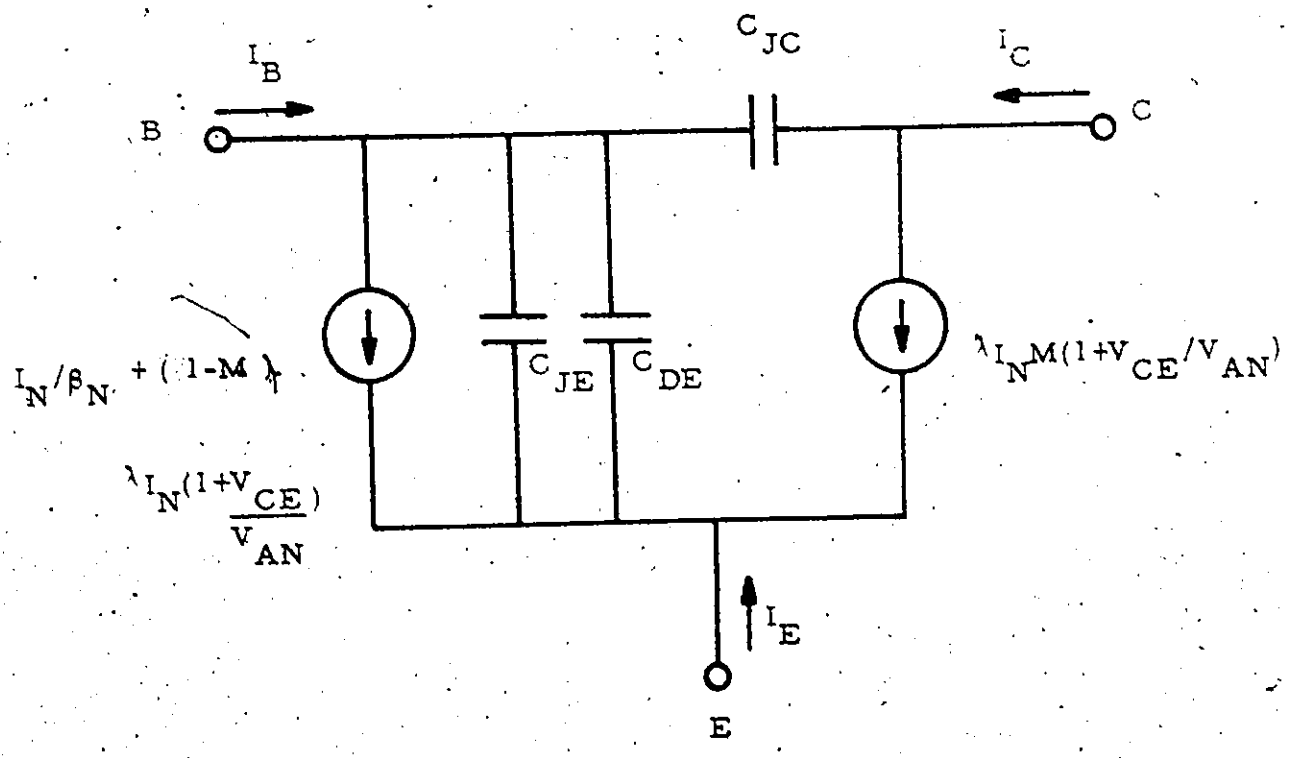


Fig. 3.6 Non-linear transistor model in the active mode.

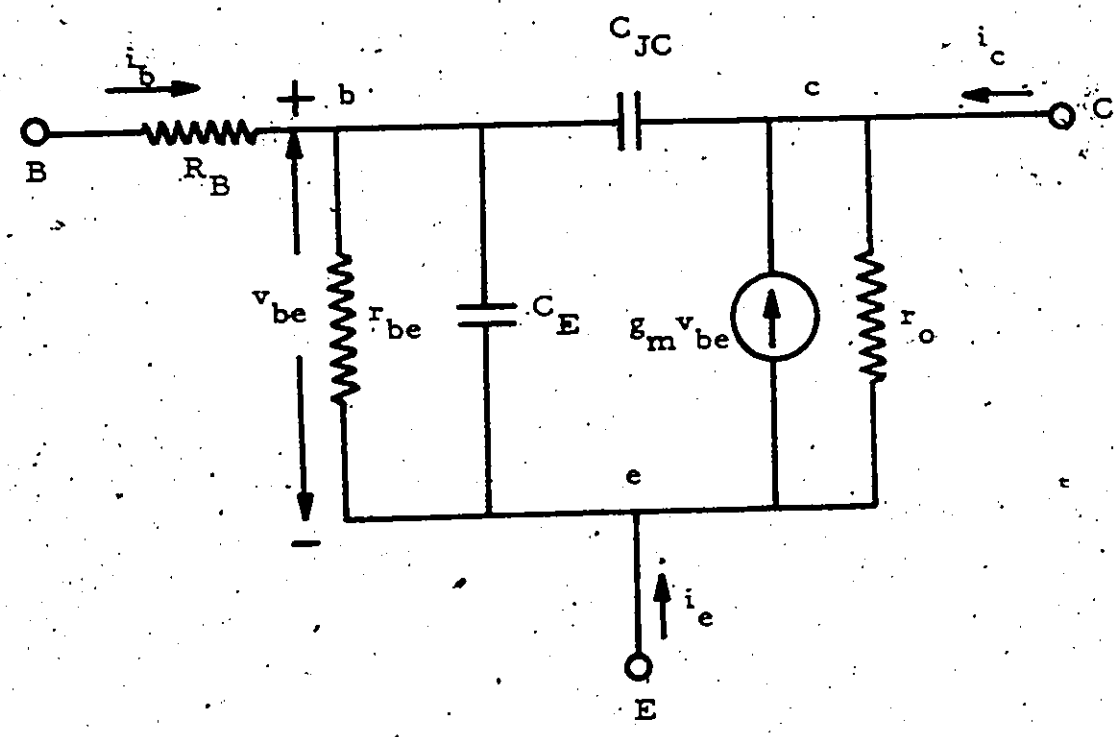


Fig. 3.7 Small signal hybrid-π model.

3.3.1 Derivation of r_{be}

$$r_{be} = \frac{\partial V_{EB}}{\partial I_B} \tag{3.40}$$

$$\frac{1}{r_{be}} = \frac{\partial I_B}{\partial V_{EB}} = \frac{\partial I_B}{\partial I_N} \cdot \frac{\partial I_N}{\partial V_{EB}} \tag{3.41}$$

from (3.25)

$$\frac{\partial I_N}{\partial V_{EB}} = a I_N$$

from (3.37)

$$I_B = \frac{I_N}{\beta_N} + (1 - M)\, I_N \lambda \left(1 + \frac{V_{CE}}{V_{AN}}\right)$$

$$\frac{\partial I_B}{\partial I_N} = \frac{1}{\beta_N} - \frac{I_N}{\beta_N^2} \frac{\partial \beta_N}{\partial I_N} + (1-M)\,\lambda \left(1 + \frac{V_{CE}}{V_{AN}}\right)$$

$$+ (1-M)\, I_N \left(1 + \frac{V_{CE}}{V_{AN}}\right) \left[\frac{-\lambda^3}{(2-\lambda)\, I_{kN}}\right]$$

$$= \frac{1}{\beta_N} - \frac{I_N}{\beta_N^2} \cdot \frac{\partial \beta_N}{\partial I_N} + (1-M)\left(1 + \frac{V_{CE}}{V_{AN}}\right) \left[\lambda - \frac{I_N \lambda^3}{(2-\lambda)\, I_{kN}}\right] \tag{3.42}$$

from (3.27)

$$\frac{\partial \beta_N}{\partial I_N} = \frac{m \beta_N I_N (I_2^2 - I_1^2)}{(I_N^2 + I_1^2)(I_N^2 + I_2^2)} \tag{3.43}$$

$$\frac{1}{r_{be}} = \theta I_N \left\{ \frac{1}{\beta_N} - \frac{m I_N^2 (I_2^2 - I_1^2)}{\beta_N (I_N^2 + I_1^2)(I_N^2 + I_2^2)} + (1-M)\left(1 + \frac{V_{CE}}{V_{AN}}\right) \left[\lambda - \frac{\lambda^3 I_N}{(2-\lambda) I_{kN}}\right] \right\} \quad (3.44)$$

3.3.2 Calculation of 'g_m'

from (3.35)

$$I_C = M\lambda \left[1 + \frac{V_{CE}}{V_{AN}}\right] I_N \quad (3.45)$$

$$g_m = \frac{\partial I_C}{\partial V_{EB}} = M\lambda \left[1 + \frac{V_{CE}}{V_{AN}}\right] \frac{\partial I_N}{\partial V_{EB}} + M I_N \left(1 + \frac{V_{CE}}{V_{AN}}\right) \frac{\partial \lambda}{\partial V_{EB}} \quad (3.46)$$

From (3.29)

$$\frac{\partial \lambda}{\partial V_{EB}} = \frac{\partial \lambda}{\partial I_N} \cdot \frac{\partial I_N}{\partial V_{EB}} = \theta I_N \left[\frac{-\lambda^3}{(2-\lambda) I_{kN}}\right] \quad (3.47)$$

$$\therefore \quad g_m = M\left(1 + \frac{V_{CE}}{V_{AN}}\right) \left[\theta I_N \lambda - \frac{-\theta \lambda^3 I_N^2}{(2-\lambda) I_{kN}}\right]$$

$$g_m = I_C \theta \left[1 - \frac{\lambda^2}{(2-\lambda)} \frac{I_N}{I_{kN}}\right] \quad (3.48)$$

3.3.3. Calculation of r_o

$$\frac{1}{r_o} = \frac{\partial I_C}{\partial V_{CE}} \quad (3.49)$$

from (3.45) and (3.30)

$$I_C = \left\{1 + e^{A_C (V_{CB} - V_M)}\right\} \lambda I_N \left\{1 + \frac{V_{CE}}{V_{AN}}\right\}. \quad (3.50)$$

If It is assumed that for $V_{CB} >> V_{EB}$

$$V_{CB} \approx V_{CE}$$

$$\therefore \quad \frac{\partial I_C}{\partial V_{CE}} \approx e^{A_C(V_{CB} - V_M)} \cdot A_C \cdot \lambda I_N \left(1 + \frac{V_{CE}}{V_{AN}}\right) + \frac{M\lambda I_N}{V_{AN}}$$

$$\text{or} \quad \frac{1}{r_o} = \frac{M-1}{M} A_C I_C + \frac{M\lambda I_N}{V_{AN}} \qquad (3.51)$$

Thus all the elements of the small signal low frequency equivalent circuit may be obtained from the non-linear large signal model.

3.4 Parameter Determination

It is important that the model parameters be easily obtained from measurements. There are many ways of obtaining the model parameters. Rohrer et al. [34] have described an automated parameter determination approach in which the parameters are obtained by least square fit of experimental data utilizing adjoint network techniques. Zaniolo et al. [35] have described a simple on-line interactive computing methodology for determining static parameters of large signal models using optimization techniques. Poon [36] has given a method of extraction of parameters for the Gummel-Poon Model [12], where the parameters are obtained by least square-fit in the region where those parameters are of importance. Agarwal [37] has also described some techniques for determination of the Gummel-Poon model parameters. For the present model, however much simpler techniques are used and the model parameters are easily obtained from a number of characteristics of the devices as described below.

I_s, θ, I_{kN}

The transfer characteristic of the transistor in the forward active region, i.e. I_C vs V_{BE} for a constant value of V_{CB} is plotted. The circuit configuration used is shown in Fig. 3.8. θ is the slope of the curve, and I_{kN} the knee point as shown in Fig. 3.10. I_s is obtained from the linear portion of the curve, e.g.,

$$I_s = \frac{I_1}{e^{\theta \cdot V_1}}$$

where V_1 and I_1 are shown in Fig. 3.10

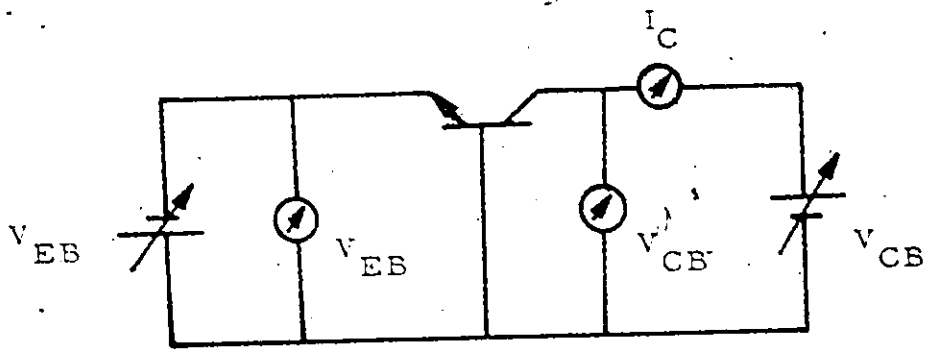


Fig. 3.8 Circuit diagram used for the measurements.

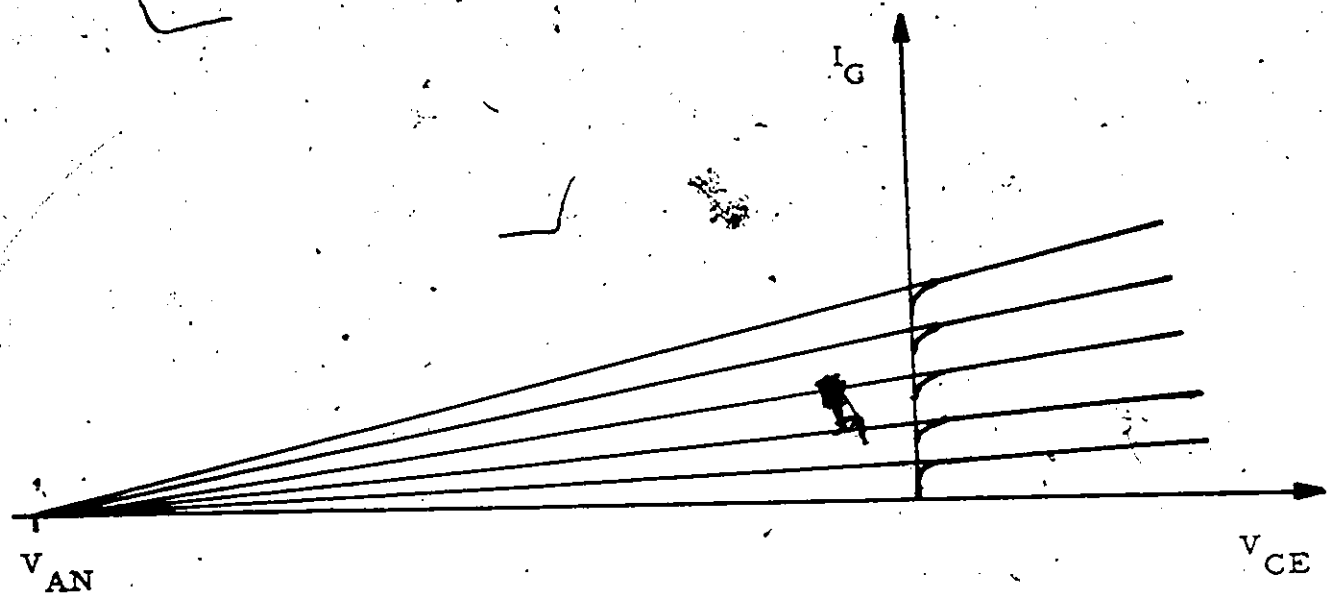


Fig. 3.9 Output characteristic of the transistor.

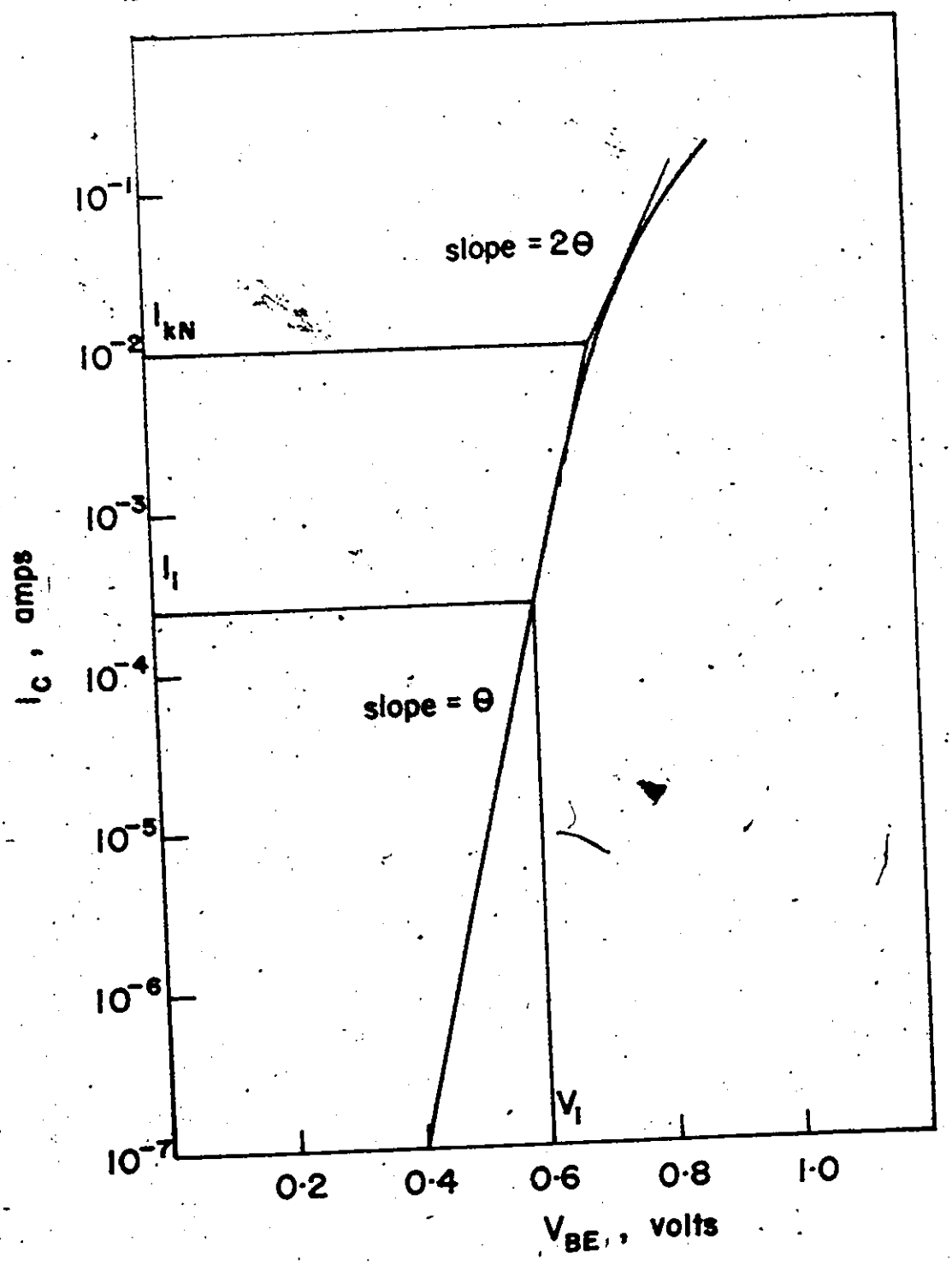


Fig. 3.10 Transfer characteristic of a transistor

I_{kI}

Exactly the same measurements as above are made but in this case the transistor is operated in the inverted mode. I_E vs. V_{BC} is plotted and the knee point of the curve gives I_{kI}.

V_{AN}, A_C, V_M

To obtain these parameters the output characteristics of the transistor are plotted. As shown in Fig. 3.9, the Early voltage V_{AN} is obtained by extrapolating the characteristics. This measurement can be made on a curve tracer. A_C and V_M are calculated so as to fit the curve in the avalanche multiplication region with equation (3.22).

V_{AI}

The output characteristics of the transistor in the inverted mode are plotted and the Early voltage, V_{AI} is extrapolated from the characteristics.

I_1, I_2, m, β_{N0}

The d.c. 'β' of the transistor in the forward active region for different values of I_C is measured. The circuit shown in Fig. 7, may be used here also. From the plot of log β_N vs log I_C, the four parameters are easily obtained as shown in Fig. 3.3.

I_3, I_4, n, B_{I0}

The same procedure as above is used but with the transistor operated in the inverted mode.

R_B

R_B is calculated from the transfer characteristic in the forward mode, as described by Bowers and Sedore [38].

R_E, R_C

R_E and R_C are obtained by plotting I_B vs V_{CE} (sat) in the forward mode and I_B vs V_{EC} (sat) in the inverted mode. The slope of these curves gives R_E and R_C respectively [39].

C_{0E}, ϕ_E, n_E, r_E

These parameters are obtained from the measurement of the emitter base junction capacitance under reverse bias on a capacitance bridge. The parameters are chosen to fit the measured values [38].

C_{0C}, ϕ_C, n_C, r_C

The same procedure as above is followed for the collector-base junction. The parameters are chosen to fit the measured values.

τ_f, τ_r

τ_f may be obtained from the calculation of f_T using 's' parameters measurements [40]. τ_f is given by

$$\tau_f = \frac{1}{2\cdot\pi f_T}$$

Also τ_f may also be obtained from pulse measurements and calculated from the rise time. τ_r is obtained from the measurement of the saturation time [38]. Also τ_r may be calculated as,

$$\tau_r = \tau_f \times \frac{I_{kI}}{I_{kN}}$$

from eqns. (3.14a) and (3.14b).

3.5 Results

The parameters of the model described in the previous section were determined for the 2N3118 transistor and are given in Table 3.1. The model was then used to evaluate analytically the characteristics of the device, and compare them to those obtained by measurements.

Fig. 3.11 shows the transfer characteristics of the transistor and Fig. 3.12 the current gain 'β' in the normal and inverted mode. Fig. 3.13 and 3.14 show the output characteristics and Fig. 3.15 and 3.16 the emitter and collector junction capacitance respectively. In Fig. 3.17 the data used to measure R_E and R_C are shown.

It may be seen in Fig. 3.11 that the transfer characteristics give a very close match. In Fig. 3.12 the current gain 'β' give a good match at low and medium current levels but the model does not seem to fit the high current level as well, and needs improvement in this direction. The output characteristics also match relatively well. The curves for the junction capacitances are also well matched.

The model developed takes into account a number of effects in the transistor and gives a reasonably accurate representation of the transistor characteristics. The model equations are simple enough that the computation time is not excessive, and the parameter determination are not overly involved. This is obviously a compromise situation ; the usefulness of the model has been verified by its inclusion in a circuit analysis program. This is discussed in the next Chapter.

TABLE 3.1

Device Parameters for a 2N3118

I_s	=	2.3×10^{-14}	amps
θ	=	39.0625	$volt^{-1}$
I_{kN}	=	0.15	amps
I_k	=	0.015	amps
V_{AN}	=	278	volts
V_{AI}	=	15	volts
I_1	=	10^{-7}	amps
I_2	=	3.4×10^{-3}	amps
I_3	=	10^{-7}	amps
I_4	=	2×10^{-3}	amps.
m	=	0.132	
n	=	0.1079	
β_{NO}	=	110	
β_{IO}	=	2.7	
A_C	=	7.0	
V_M	=	70.0	volts
R_B	=	5	ohms
R_C	=	1.9	ohms
R_E	=	0.8	ohms
C_{0E}	=	30.9×10^{-12}	Farads
C_{0C}	=	11.35×10^{-12}	Farads
n_E	=	0.3894	
n_C	=	0.3545	
ϕ_E	=	0.65	volts
ϕ_C	=	0.6	volts
τ_f	=	4.19×10^{-10}	secs.
τ_r	=	4.19×10^{-9}	secs.
r_E	=	2.0	
r_C	=	2.5	

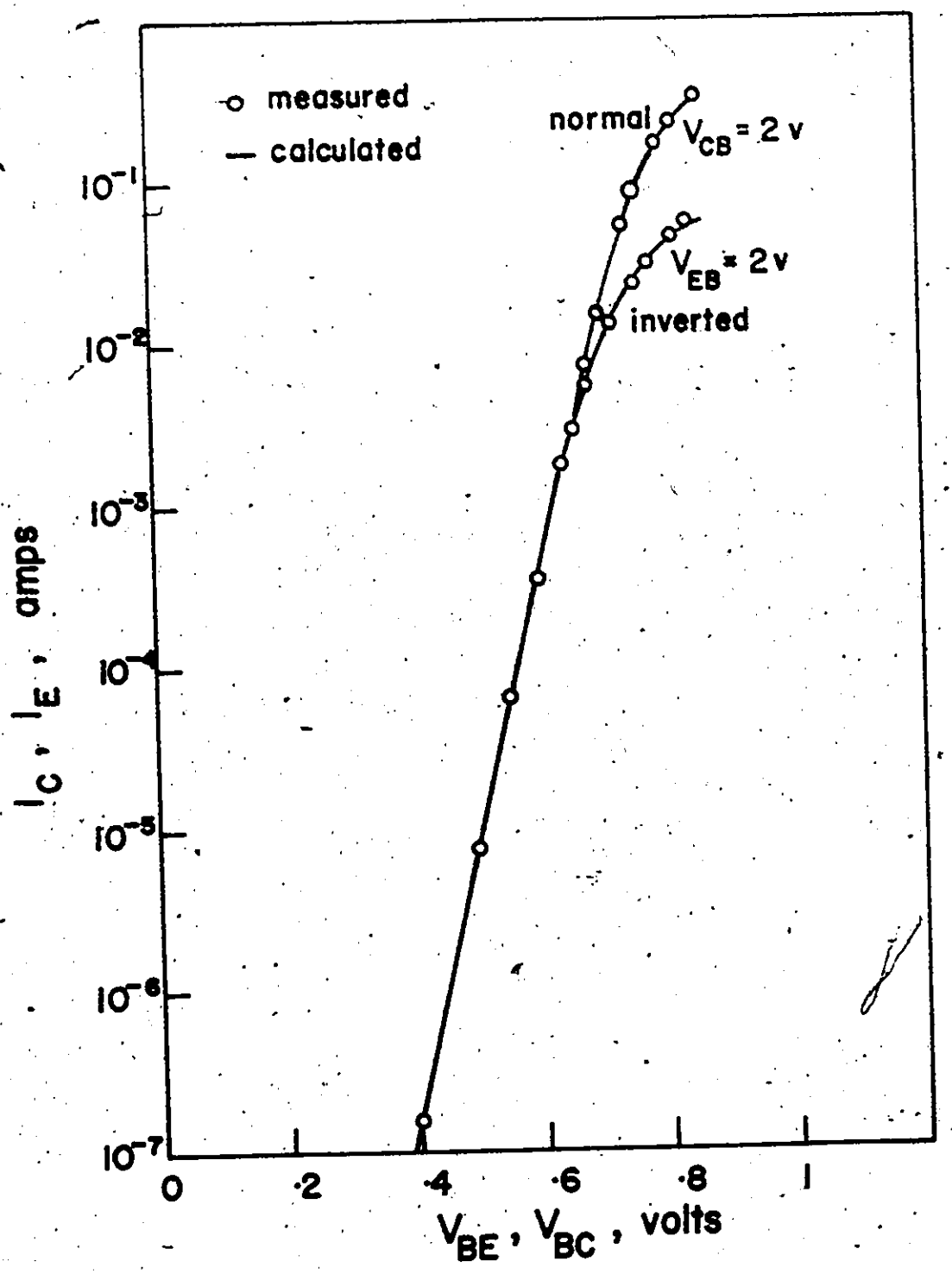


Fig. 3.11 : Transfer characteristics of the transistor in the normal and inverted mode.

transistor in the normal and

inverted mode.

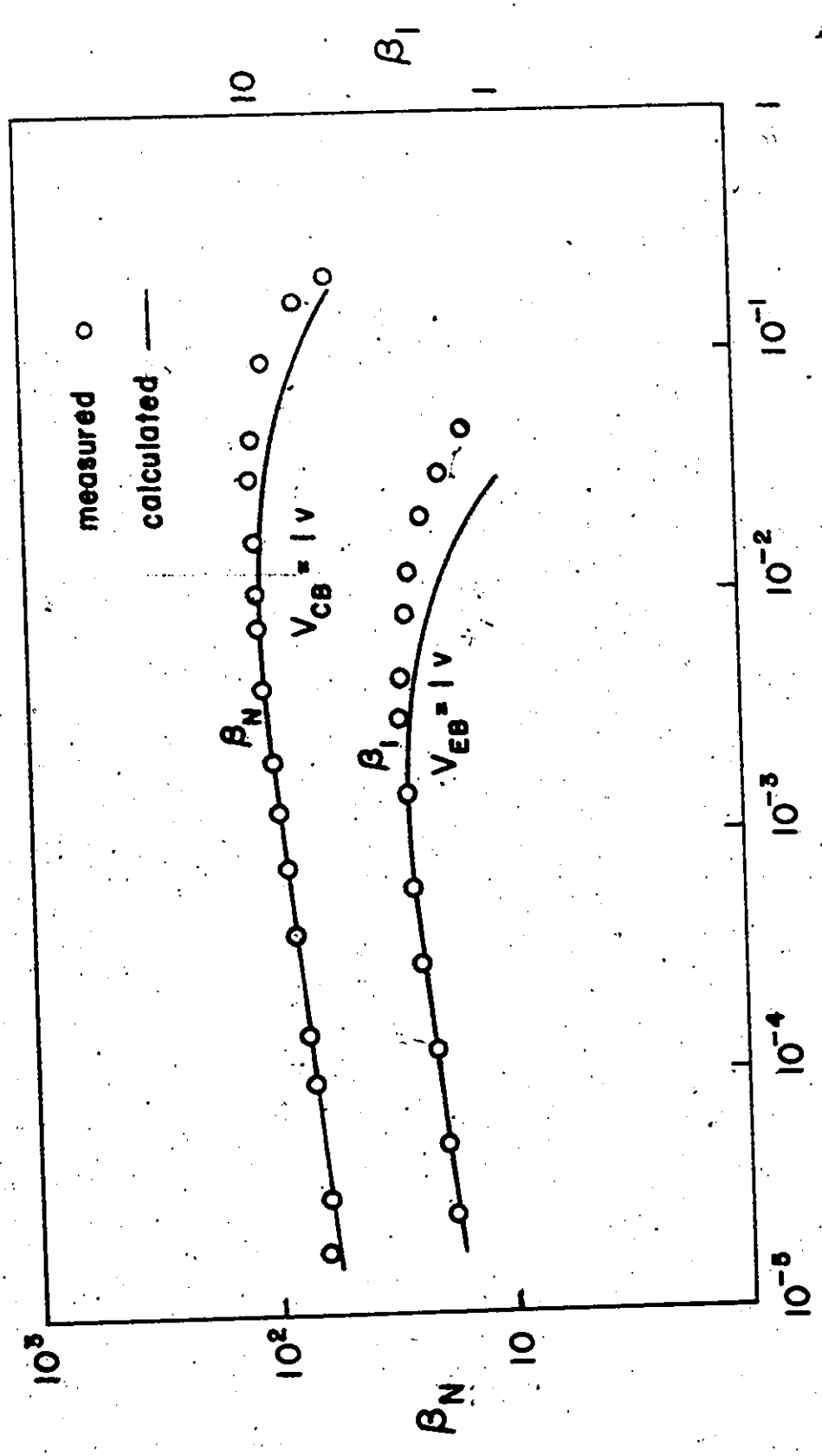


Fig. 3.12 Current gain of the transistor in the normal and inverted mode.

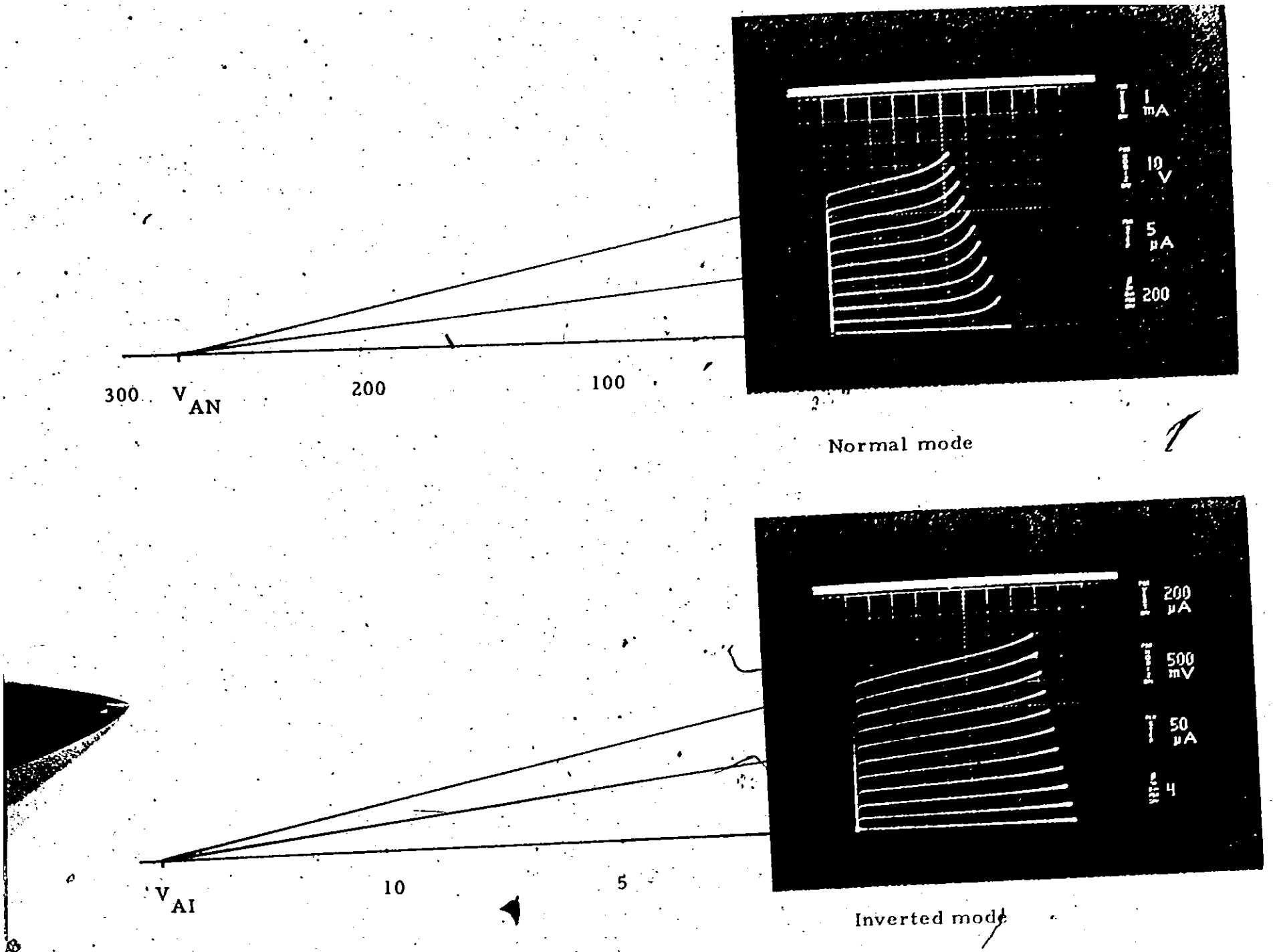


Fig. 3.13 Output characteristics in the normal and inverted mode.

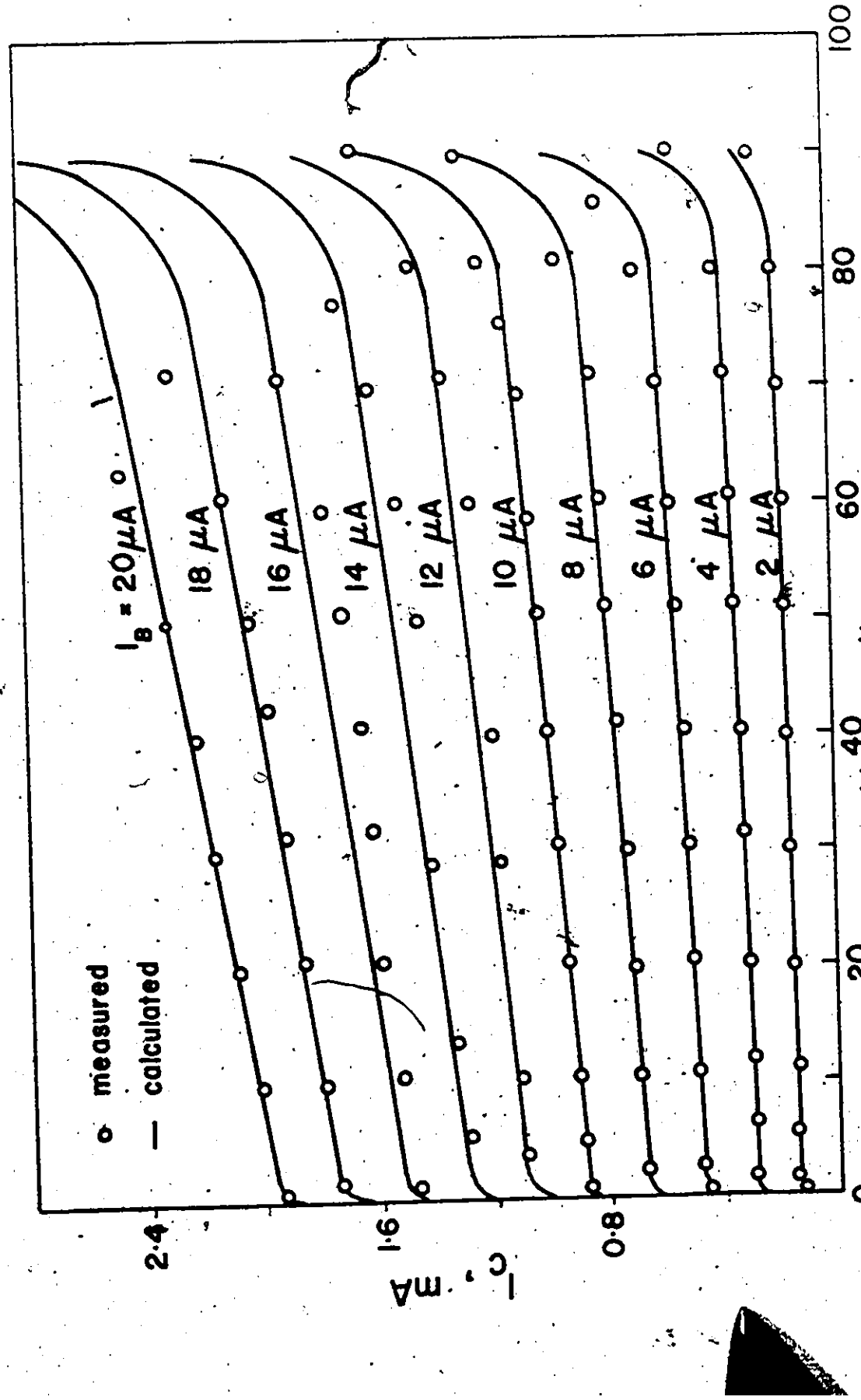


Fig. 3.14 Output characteristics of the transistor in the normal mode.

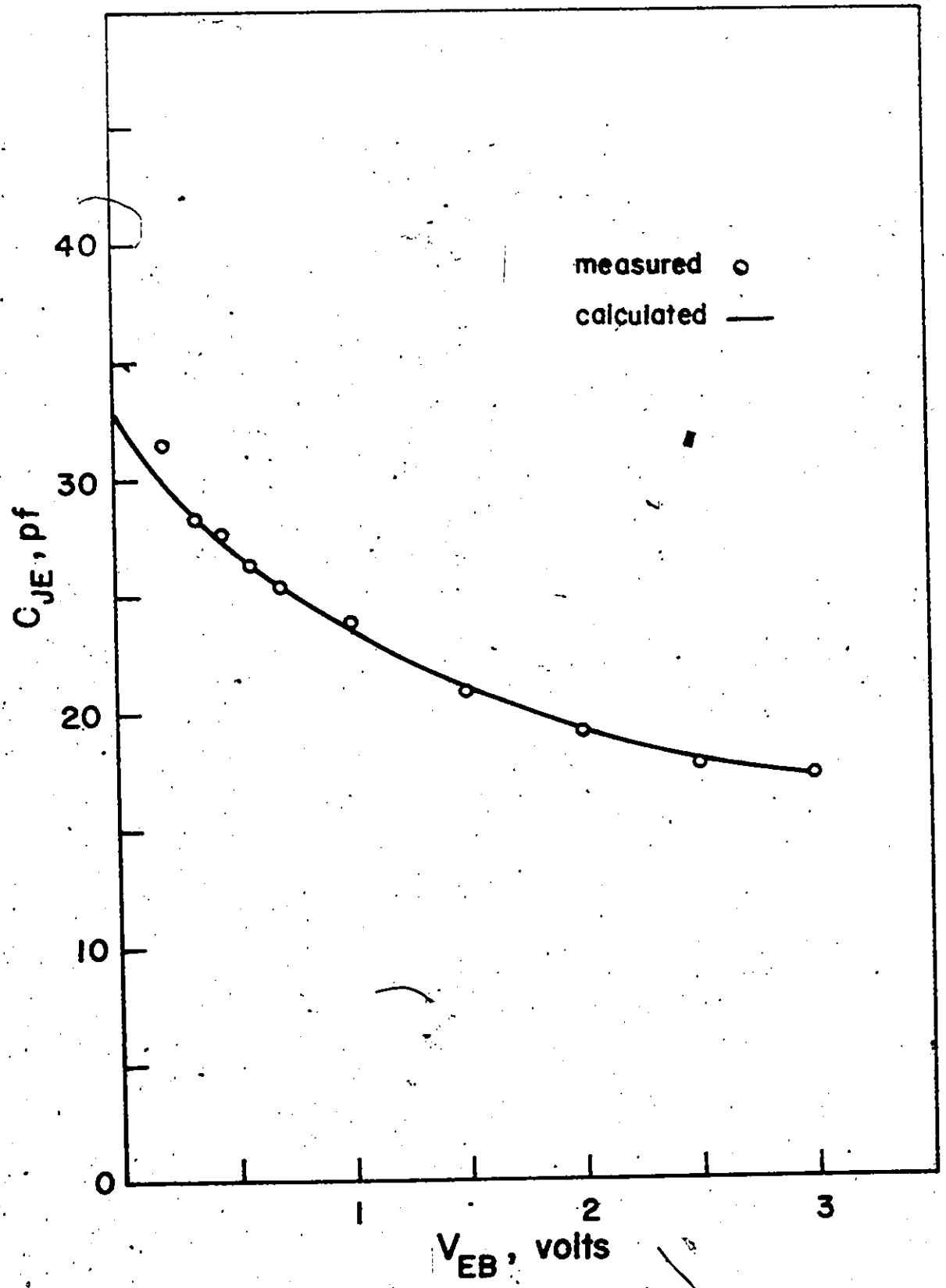


Fig. 3.15 Emitter base junction capacitance.

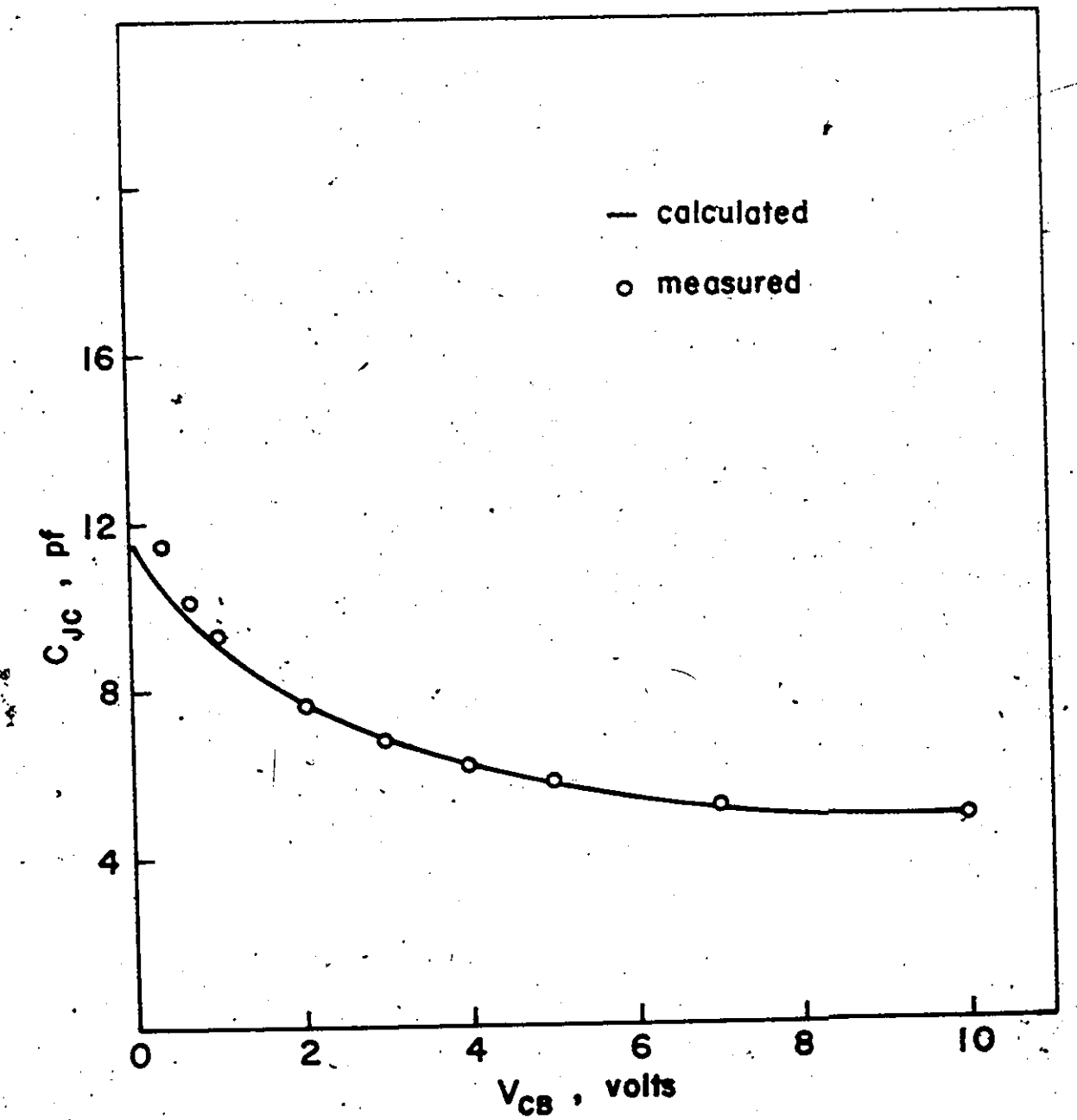


Fig. 3.16 Collector base junction capacitor.

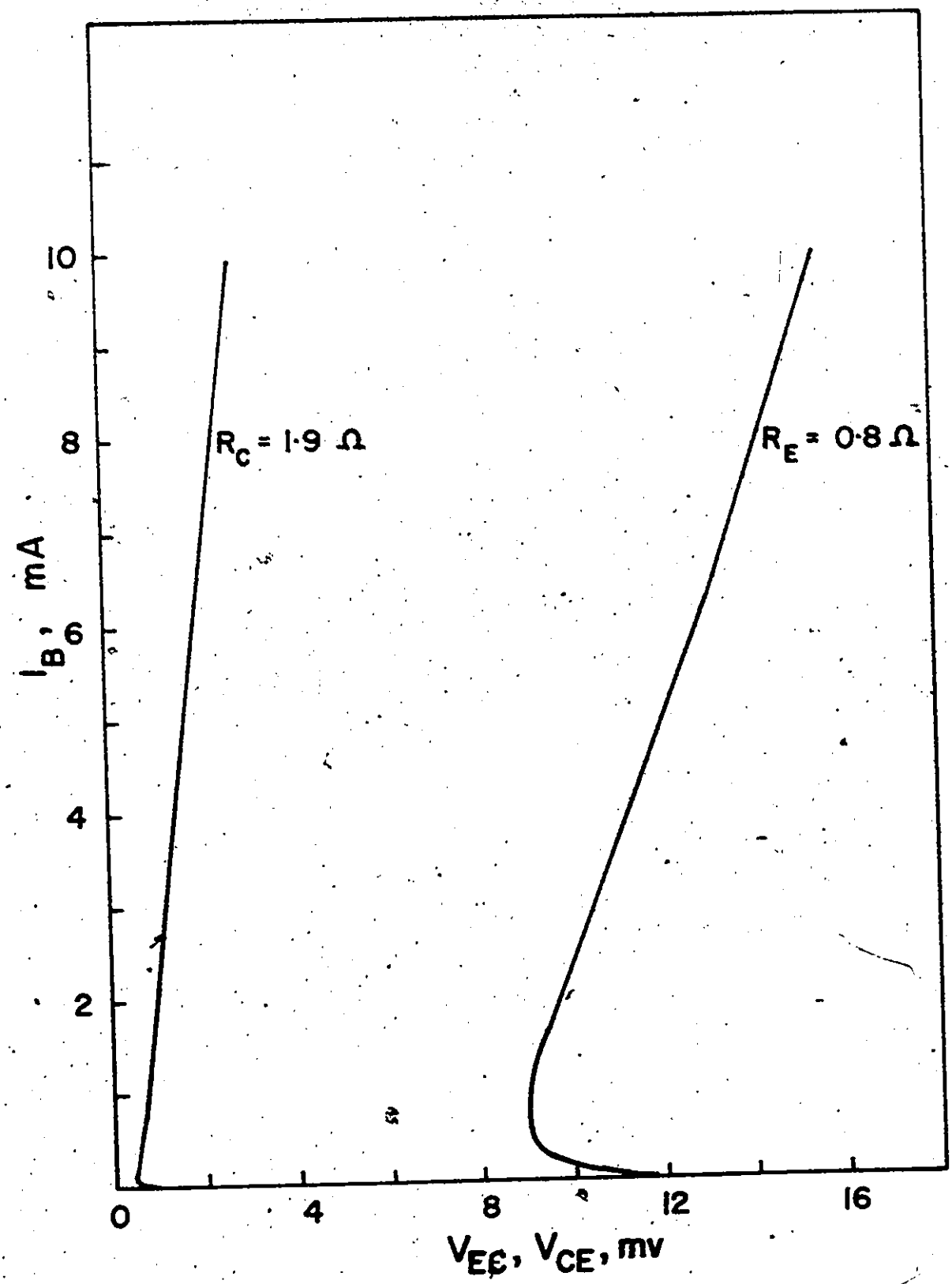


Fig. 3.17 Measurement of R_C and R_E.

CHAPTER 4

SIMULATION OF CIRCUITS USING THE PROPOSED MODEL

In this chapter, the model developed in chapter 3 is used in a circuit analysis program. First, the use of a nodal analysis technique for non-linear circuits, using the Newton-Raphson iteration scheme is discussed. Then the use of the model in a network analysis program is described [41]. Finally several examples are given to illustrate the application of the model to analyse the d.c., a.c. and transient operation of selected circuits.

4.1 Circuit Analysis Programs

From the time the first general purpose computer circuit analysis program ECAP [42] was released, there have been a large number of circuit programs developed. Recently an article published by Greenbaum [43] summerizes briefly the state of the art of the circuit programs. Different programs have different features. Table 4.1 gives a comparison of the capabilities of the programs. The table gives the general data of the program size, the different types of computers on which each program is operational, its core requirements, network size limits, the availability and a few words about unique features. This listing does not cover many programs which have been developed to solve specific problems e.g., see special issue of IEEE on computer-aided circuit design [44]. One such program is NANSIM (Non-linear Active Network Simulation) [45], developed at Bell Northern Research Lab., Ottawa.

NANSIM is interactive, with terminal modifying facility so that the designer can modify the circuit parameters without interrupting the operation of the program and get the desired results in seconds. Another advantage of NANSIM is the input language which is in a simple free format and is very easy to use. The most spectacular feature

Table 4.1 General Information

Program Name	Type Of Analysis: Linear	Type Of Analysis: Nonlinear	Approx No. Of Statements	Core Requirements (Bytes)	Computers On Which Operating (7)	Time In Use (Years)	Debug Status	Topological Limits	Documentation	Program Availability	Unique Program Features
ANP3	X		4 K	80 K to 135 K	1,2,3,4,5,7,8 (1)	2	Complete	100 Branches 40 Nodes	Good	No Restrictions	Excellent Teaching Program Written in FORTRAN and ALGOL
BELAC	X		10 K	120 K	4	5	Complete	None (5)	Good	No Restrictions (2)	Available on Time Share, Batch, and Remote Batch
COMPACT	X		2 K	64 K	2,6,7	2	Complete	1 and 2 Port Topologies	Good	No Restrictions (3)	Microwave Design and Optimization
CORNAP	X		3 K	80 K to to 110 K	2,5,6,7	6	Complete	30 Elements to 70 Elements	Good	No Restrictions	State Equation Oriented Completely ANSI and FORTRAN 4
LISA	X		-	140 K	7	6	Complete	125 Elements 50 Nodes	Good	No Restrictions	Provides Poles and Zeros and Block Diagram
MARTHA	X		-	32 K	7	3	Complete	2 Port Topologies	Good	No Restrictions	Simple, Open Ended Library of Elements, Responses, Fast, Builtin Functions and Frequency Transformations
PTNA	X		1.5 K	115 K	7	2	Complete	30 Elements (4)	Good	No Restrictions	Primarily Suited to Instruction of Undergraduates
SCAP	X		1.4 K	126 K	7	0.5	Complete	200 Nodes 500 Branches 100 Coupled Elements	Good	No Restrictions	Response Evaluated by Loopless Code
SNAP	X		1.5 K	26 K	2	3	Complete	35 Nodes 100 Branches	Good	No Restrictions	Symbolic Transistor Function

Table 4.1 General Information (continued)

Program Name	Type of Analysis: Linear	Type of Analysis: Nonlinear	Approx No. Of Statements	Core Requirements (Bytes)	Computer On Which Operating (7)	Time In-Use (Years)	Debug Status	Topological Limits	Documentation	Program Availability	Unique Program Features
ADA-74	X	X	4 K	64 K	4	8	Complete	None (5)	Good	No Restrictions (3)	Optimized for Most Efficient Use of CPU Time and Memory
ASTAP	X	X	60 K	200 K	7	4	Complete	None (5)	Good	No Restrictions (3)	Statistical Transient Analysis
DACSEP	X	X	—	1200 K	2	0.5	Complete	300 Nodes	None	Restricted	Models Large Microwave Transistor
CURE2000	X	X	9 K	600 K	2	0.5	Complete	200 Elements	Good	Restricted	Convergence Features, Large Signal Sensitivities
IMAG2	X	X	10 K	100 K	4,5,7,10	3	Complete	None (5)	Good	No Restrictions (3)	3rd Generation Features
R-CAP	X	X	3 K	200 K	9	2.5	Complete	-	Good	Restricted	3rd Generation Features
CIRCUS-2	X	X	18 K	180 K, 600 K, 400 K	4 (3), 7, 2	3	Complete	None (5)	Good	No Restrictions	Convolution Integral Modeling of Linear Systems 3rd Generation Features
NAP2		X	6.5 K	104 K or 250 K	7	1	80%	200 Branches-50 Nodes or 1500 Branches 500 Nodes	Preliminary Users Manual	No Restrictions	3rd Generation Features Well Suited for Stiff Systems
SCEPTRE	X	X	16 K	180 K	7, 4 (3)	5	Complete	300 Nodes	Good	No Restrictions	FFT and Monte Carlo Added to GE Version
SYSCAP	X	X	12 K (6)	240 K (4)	2	4	Complete	255 Nodes	Good	No Restrictions (3)	

(1) ALGOL version of program

(2) GE system has time share and remote batch

(3) Available commercially

(4) Adjustable

(5) None implies computer memory limited

(6) SYSCAP consists of three separate analysis programs; each requires indicated quantities

(7) LEGEND: 1 = Burroughs, 2 = CDC, 3 = ICL, 4 = GE/Honeywell, 5 = UNIVAC, 6 = PDP, 7 = IBM, 8 = RC4000, 9 = SPECTRA, 10 = C.I.I.

of NANSIM is that the models of the devices can be replaced without disrupting the rest of the program. Because of this feature NANSIM has been used here to test the model developed in the previous chapter by analyzing a number of circuits.

4.1.1 Simulation Procedure

The simulation in NANSIM is performed using the nodal admittance formulation for circuit analysis. The d.c. and transient simulation of non-linear circuits is carried out using the Newton-Raphson method of successive approximations. In this method the solution is recalculated a number of times, starting from an initial guess, until the accuracy of the solution is within specified limits. In the small signal analysis, the non-linear devices are treated as linear devices and the small signal admittances needed are calculated automatically by the program for each of the non-linear device using the particular bias condition already determined in the d.c. analysis. Following is a brief description of the analysis.

4.2 D.C. Node Equations

The d.c. solution is obtained by the nodal equation approach [45,47]. The node equations for determining the d.c. solution are obtained by opening all capacitors, shorting all inductors, nulling all time varying sources and writing the equations for the remaining resistive network. The node equation for a network with n nodes is of the form

$$G\,\bar{e} + \bar{N}(\bar{e}) = \bar{I} \qquad (4.1)$$

where $\bar{e}$ is the n x 1 vector of node voltages, G is an n x n conductance matrix due to the linear resistors in the network, $\bar{N}(\bar{e})$ is an n x 1 vector of non-linear functions of $\bar{e}$ representing the diode junctions and $\bar{I}$ is an n x 1 vector representing the d.c. current sources.

Equation (4.1) is obtained by applying Kirchhoff's current law at each node. This gives a set of non-linear simultaneous algebraic equations in $\bar{e}$ which can be solved by using the Newton-Raphson iteration scheme given as

$$\bar{e}_{k+1} = \bar{e}_k - \frac{G\bar{e}_k + \bar{N}(\bar{e}_k) - \bar{I}}{\left[G + \frac{\partial \bar{N}(\bar{e}_k)}{\partial \bar{e}}\right]} \qquad (4.2)$$

where $\bar{e}_k$ is the k^{th} iteration of $\bar{e}$. Equation (4.2) can be re-written as

$$\left[G + \frac{\partial \bar{N}(\bar{e}_k)}{\partial \bar{e}}\right] \bar{e}_{k+1} = \frac{\partial \bar{N}(\bar{e}_k)}{\partial \bar{e}} \cdot \bar{e}_k - \bar{N}(\bar{e}_k) + \bar{I} \qquad (4.3)$$

It can be shown that (4.3) is equivalent to the node equation obtained by replacing all non-linearities by linear equivalents. For example, as shown in Fig. 4.1 a for a diode, its linear equivalent can be represented by a resistor and a d.c. source given by the tangent line drawn at the value of the voltage across the diode, v_k . This simple circuit representation is shown in Fig. 4.1b. By replacing all of the non-linearities by such linear equivalents, it is then possible to arrive at (4.3) directly. The G's which represent diode conductances will be entered into one large admittance matrix Y along with and in the same manner as for linear resistors. These are of course the same terms represented by $\frac{\partial \bar{N}(e)}{\partial \bar{e}}$ that are added to G in (4.3). The $\bar{J}$ sources of the diodes will be added to the $\bar{I}$ vector. These terms can be identified in (4.3) as

$$-\bar{J} = \frac{\partial \bar{N}(\bar{e}_k)}{\partial \bar{e}} \cdot \bar{e}_k - \bar{N}(\bar{e}_k) \qquad (4.4)$$

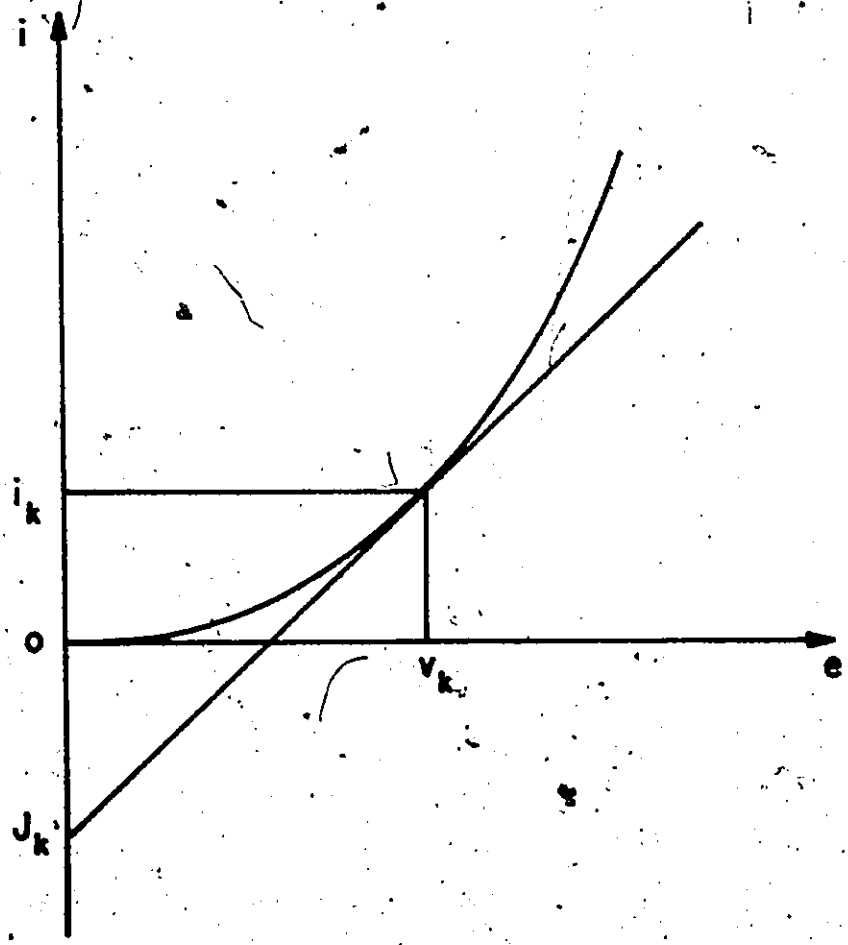


Fig. 4. 1a Diode curve and tangent line at v_k.

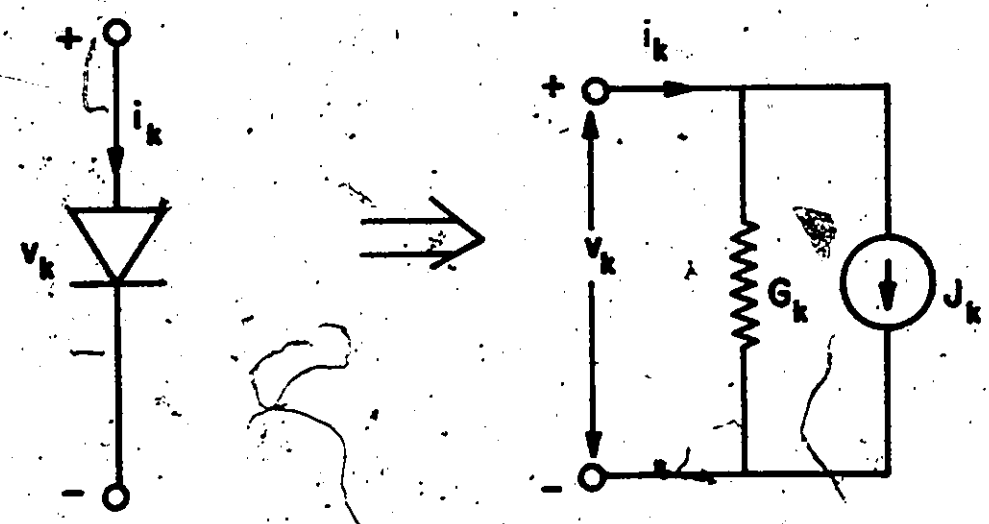


Fig. 4. 1b Equivalent linear model.

Therefore, at each iteration, the node equation for the Newton-Raphson iteration is easy to obtain. From (4.3) and (4.4),

$$Y(\bar{e}_k)\,\bar{e}_{k+1} = \bar{i}(\bar{e}_k, \bar{I}) \tag{4.5}$$

where

$$Y(\bar{e}_k) = G + \frac{\partial \bar{N}(\bar{e}_k)}{\partial \bar{e}} \tag{4.6}$$

and

$$\bar{i}(\bar{e}_k, \bar{I}) = \bar{I} - \bar{J} \tag{4.7}$$

Equation (4.5) is the node equation of the linearized circuit for the k^{th} iteration. The solution of (4.5) is $\bar{e}_{k+1}$. A new linear model for the circuit is obtained at this point and the new circuits is solved for $\bar{e}_{k+2}$. This procedure is continued until convergence is obtained. Note that this procedure does not require one to write the full node equation of (4.1). However, it is necessary to know the error associated with (4.1) defined as

$$\bar{F}(\bar{e}) = G\bar{e} + \bar{N}(\bar{e}) - \bar{I} \tag{4.8}$$

$\bar{F}(\bar{e})$ is the function of $\bar{e}$ that must be set to zero to find the d.c. solution. $\bar{F}(\bar{e})$ can be used to determine a convergence criterion for the Newton iteration. $\bar{F}(\bar{e}_k)$ can be calculated as follows. From (4.2), (4.6) and (4.7)

$$\bar{e}_{k+1} = \bar{e}_k - [Y(\bar{e}_k)]^{-1}\,[\bar{F}(\bar{e}_k)] \tag{4.9}$$

$$\bar{F}(\bar{e}_k) = Y(\bar{e}_k)\,[\bar{e}_{k+1} - \bar{e}_k] \tag{4.10}$$

4.2.1 Damping Scheme

There is a severe problem associated with the Newton method as applied to transistor circuits and that is the problem of overflow [48]. Since we are dealing with exponential functions, it does not take a very large forward junction voltage to cause the junction current to exceed the overflow limits of the computer. Even if overflow does not occur, the iteration may diverge away from the solution. In order to avoid this problem a damped converging scheme is used. It is described in Appendix III.

4.3 D.C. Analysis

As discussed in section 4.2, in order to use the Newton-Raphson iteration technique, one has to define a linear model of the transistor and the nodal admittance matrix Y of the circuit. Following is the description of how this is done.

The non-linear nodal equations for the bipolar transistor model are given by (eqns. 3.22-3.26)

$$I_C = M\lambda \left[1 + \frac{V_{CE}}{V_{AN}}\right] I_N - \lambda \left[1 + \frac{1}{\lambda \beta_I} + \frac{V_{EC}}{V_{AI}}\right] I_I \quad (4.11)$$

$$I_B = \frac{I_N}{\beta_N} + \frac{I_I}{\beta_I} + (1 - M) \left[1 + \frac{V_{CE}}{V_{AN}}\right] \lambda I_N \quad (4.12)$$

$$I_E = -\lambda \left[1 + \frac{V_{CE}}{V_{AN}} + \frac{1}{\lambda \beta_N}\right] I_N + \lambda \left[1 + \frac{V_{EC}}{V_{AI}}\right] I_I \quad (4.13)$$

The non-linear model representing the above equations is shown in Fig. 4.2. V_1, V_2 and V_3 are the base, collector and emitter node voltages respectively. The linearized model of the transistor of Fig. 4.2 is shown in Fig. 4.3. By inspection, the nodal admittance matrix formulation is given by

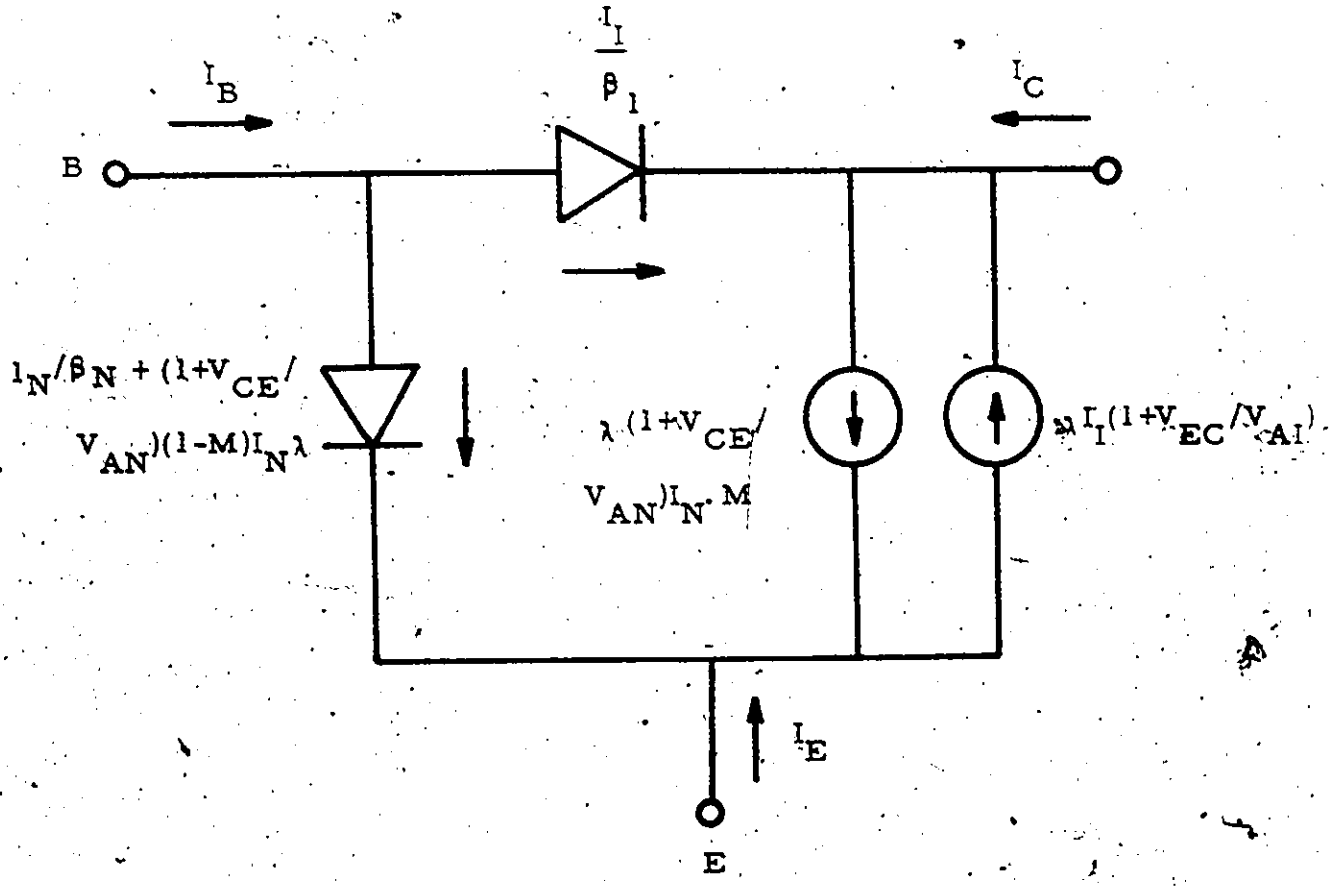


Fig. 4.2 Non-linear model of the transistor.

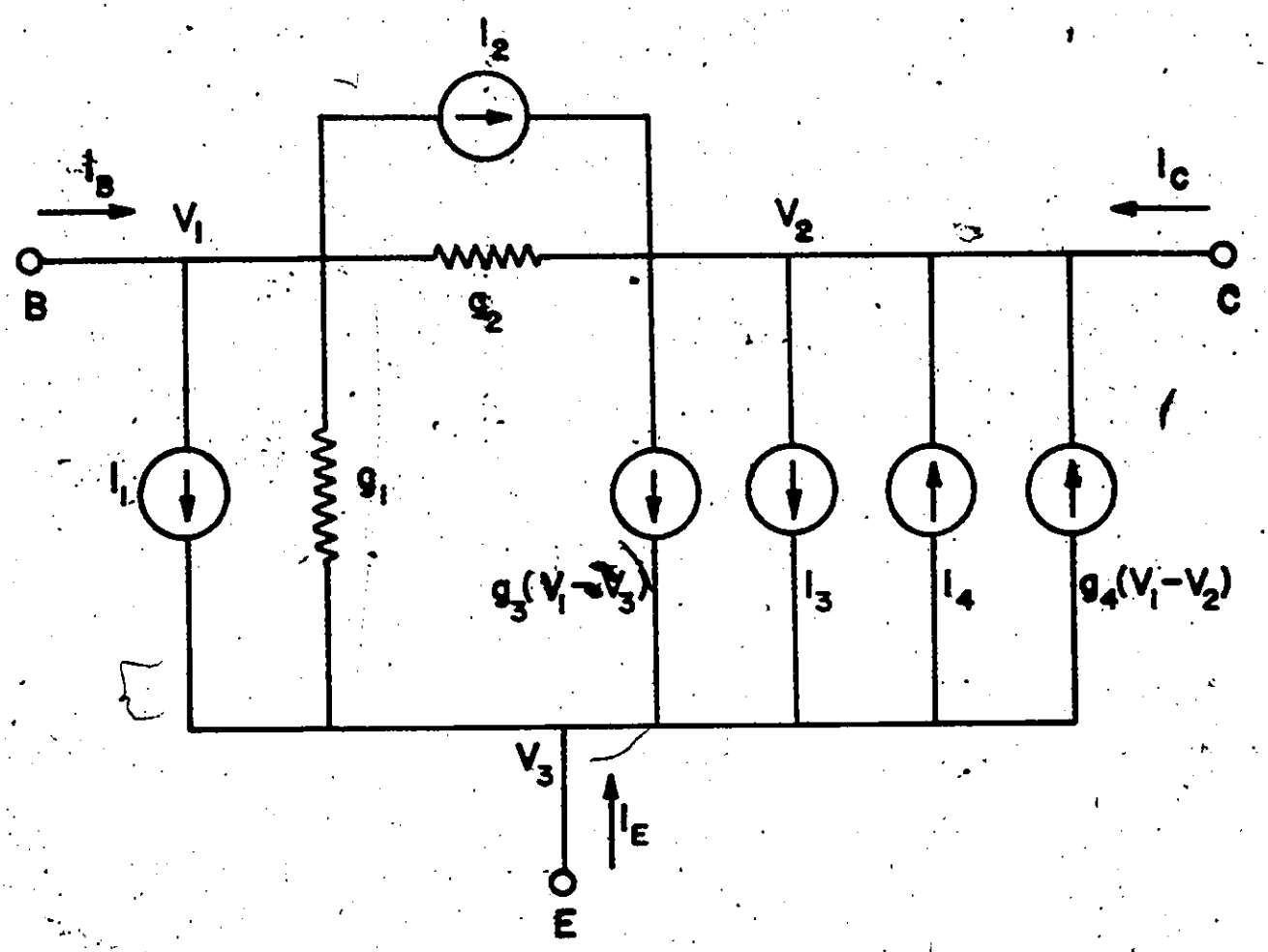


Fig. 4.3 Linear model of the transistor of Fig. 4.2.

$$\begin{bmatrix} g_1 + g_2 & -g_2 & -g_1 \\ g_3 - (g_1 + g_2) & g_2 + g_4 & -g_2 \\ g_4 - (g_1 + g_3) & -g_4 & g_1 + g_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} -I_1 & -I_2 \\ -I_3 + I_2 + I_4 \\ -I_4 + I_1 + I_3 \end{bmatrix} \tag{4.14}$$

where

$$I_1 = \frac{I_N}{\beta_N} + (1-M)\left[1 + \frac{V_{CE}}{V_{AN}}\right] \lambda I_N \tag{4.15}$$

$$I_2 = \frac{I_I}{\beta_I}$$

$$I_3 = M\lambda \left[1 + \frac{V_{CE}}{V_{AN}}\right] I_N \tag{4.17}$$

$$I_4 = \lambda \left[1 + \frac{V_{EC}}{V_{AI}} I_I\right] \tag{4.18}$$

The conductances are calculated as,

$$g_1 = \frac{\partial I_1}{\partial V_{BE}} = \theta . I_N \left\{ \frac{1}{\beta_N} - \frac{n I_N^2 (I_2^2 - I_1^2)}{\beta_N (I_N^2 + I_1^2)(I_N^2 + I_2^2)} + (1 - M)\left(1 + \frac{V_{CE}}{V_{AN}}\right) \lambda - \frac{\lambda^3 I_N}{(2-\lambda) I_{kN}} \right\} \tag{4.19}$$

$$g_2 = \frac{\partial I_2}{\partial V_{BC}} = \theta \frac{I_I}{\beta_I} \left[1 - \frac{n I_I^2 (I_4^2 - I_3^2)}{(I_I^2 + I_3^2)(I_I^2 + I_4^2)}\right] \tag{4.20}$$

$$g_3 = \frac{\partial I_3}{\partial V_{BE}} = M\theta \lambda \left[1 + \frac{V_{CE}}{V_{AN}}\right] I_N \left[1 - \frac{\lambda^2 I_N}{(2-\lambda) I_{kN}}\right] \tag{4.21}$$

$$g_4 = \frac{\partial I_3}{\partial V_{BE}} = \theta \lambda \left[1 + \frac{V_{EC}}{V_{AI}}\right] I_I \left[1 - \frac{\lambda^2 I_I}{(2-\lambda) I_{KI}}\right] \quad (4.22)$$

Where all the parameters have been previously defined in Chapter 3.

4.4 Small Signal Analysis

For the small signal analysis, the junction and diffusion capacitances have to be added to the linearized model. The equivalent small signal model is shown in Fig. 4.4. The equivalent 'g' matrix required for the small signal analysis is then given by,

$$\begin{bmatrix} g_1 + g_2 + j\omega(C_E + C_C) & -(g_2 + j\omega C_C) & -g_1 - j\omega C_E \\ g_3 - (g_2 + j\omega C_C + g_4) & g_2 + j\omega + g_4 & -g_3 \\ g_4 - g_3 - g_1 - j\omega C_E & -g_4 & g_1 + j\omega C_E + g_3 \end{bmatrix}$$

4.5 Transient Analysis

In the transient analysis the currents are calculated after each specified time interval (ΔT). The currents due to the capacitances in the transistor during the transient modes are calculated as follows,

$$i_C = G_{CC} \cdot (V_{BE} - V_{OC}) \quad (4.24)$$

$$i_B = G_{CC} (V_{BC} - V_{OC}) + G_{CE} (V_{BE} - V_{OE}) \quad (4.25)$$

$$i_E = G_{CE} (V_{BE} - V_{OE}) \quad (4.26)$$

where

$$G_{CE} = \frac{C_E}{\Delta T} \quad (4.27)$$

$$G_{CC} = \frac{C_C}{\Delta T} \quad (4.28)$$

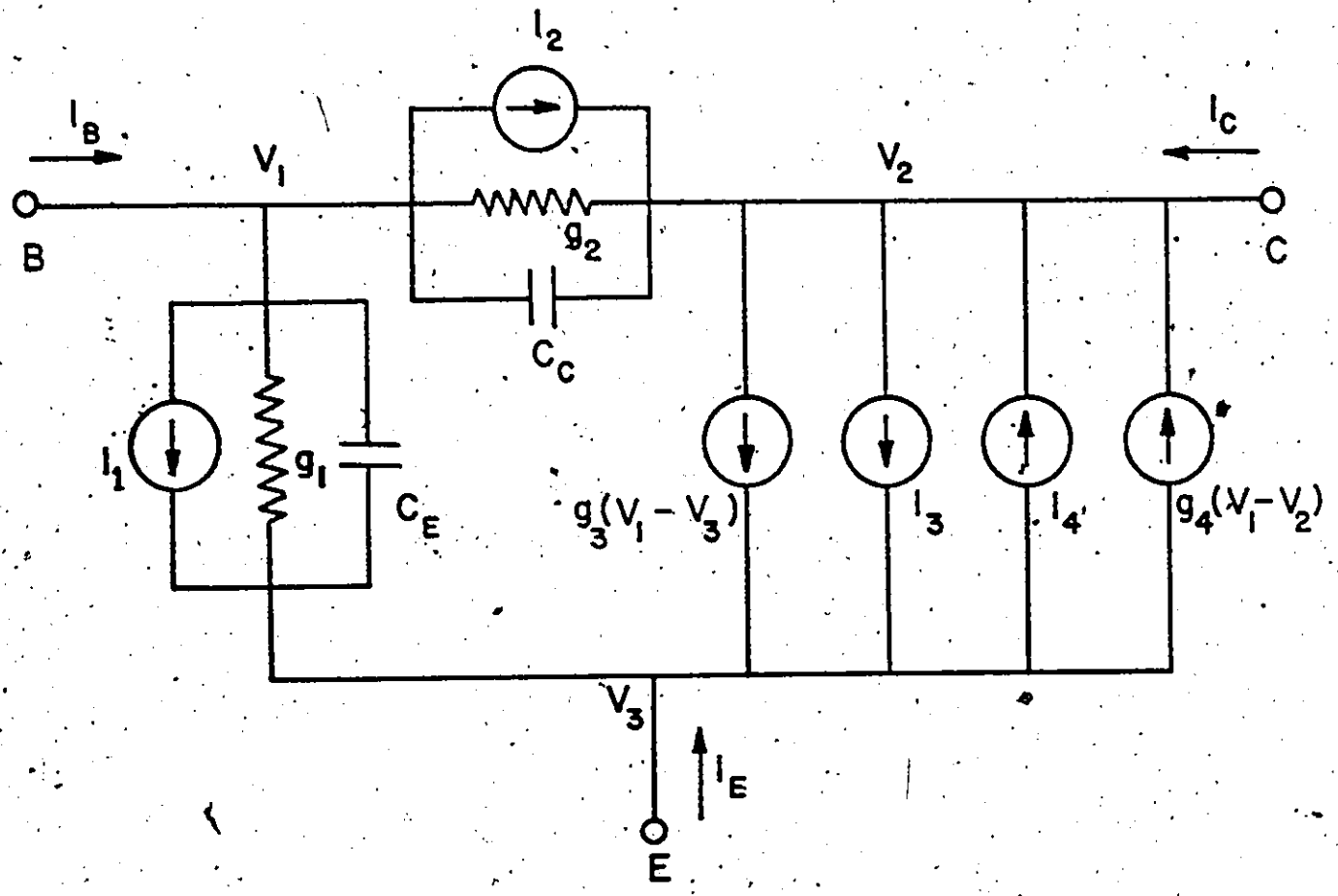


Fig. 4.4 Linear model of the transistor for small signal analysis.

V_{OE} = Voltage across base-emitter at the previous time step

V_{OC} = Voltage across base-collector at the previous time step.

The terminal currents are then given by,

$$I_C = I_C' + i_C \quad (4.29)$$

$$I_B = I_B' + i_B \quad (4.30)$$

$$I_E = I_E' + i_E \quad (4.31)$$

where I_C', I_B' and I_E' are the collector, base and emitter current respectively obtained from the d.c. analysis.

4.6 Use of the Model with NANSIM

The implementation of the model in the NANSIM circuit analysis program for d.c., small signal and transient analysis is achieved by the subroutine given in Appendix IV. The model is used in NANSIM with the following command [49].

DONANSIM f_n BJTT

where f_n is the data file name.

4.6.1 Model Parameter Entries

The input parameters to the transistor are given in three lines as follows,

I line &TNPNn

or

&TPNPn N_B, N_C, N_E, β_N, β_I, I_s, θ, V_{AN}, I_{kN}, I_2, m

II line C_{OE}, n_E, ϕ_E, r_E, C_{OC}, n_C, ϕ_C, r_C, τ_f, τ_r.

III line V_{AI}, I_{kI}, I_1, I_3, I_4, n, A_C, V_M

where n is the element number (Transitor) and N_B, N_C and N_E are base, collector and emitter node numbers respectively.

4.6.2 Default Values

It is important that all the parameters be specified. If any one of the parameters is not known, a default value must be given. The default value for some of the parameters has been chosen as follows when needed:

V_{AN}	=	1E10
V_{AI}	=	1E10
I_{IN}	=	1E10
I_{kI}	=	1E10
I_1	=	0
I_2	=	0
I_3	=	0
I_4	=	0
m	=	1
n	=	1
A_C	=	1
V_M	=	1E10

These values are chosen such that they do not affect the numerical computation of the model in the analysis.

4.7 Simulation Examples

For the purpose of demonstrating the use of the model a few examples are described below.

4.7.1 Example 1 (d.c. analysis)

The darlington amplifier circuit shown in Fig. 4.5. has been analysed with NANSIM. The data files for the circuit , using the Ebers-Moll model and the model developed in Chapter 3 , as well as the output node voltages are given in Lists 4.1 and 4.2 respectively. Table 4.2 gives the model parameters for the 2N3118 transistor used in the simulation. In table 4.3 , the results obtained with the two models are compared with the experimental results. It can be seen that the node voltages obtained with the proposed model match closely the experimental results. The computation time using the Ebers-Moll model is 1.85 secs. , while with the proposed model is 3.53 secs.

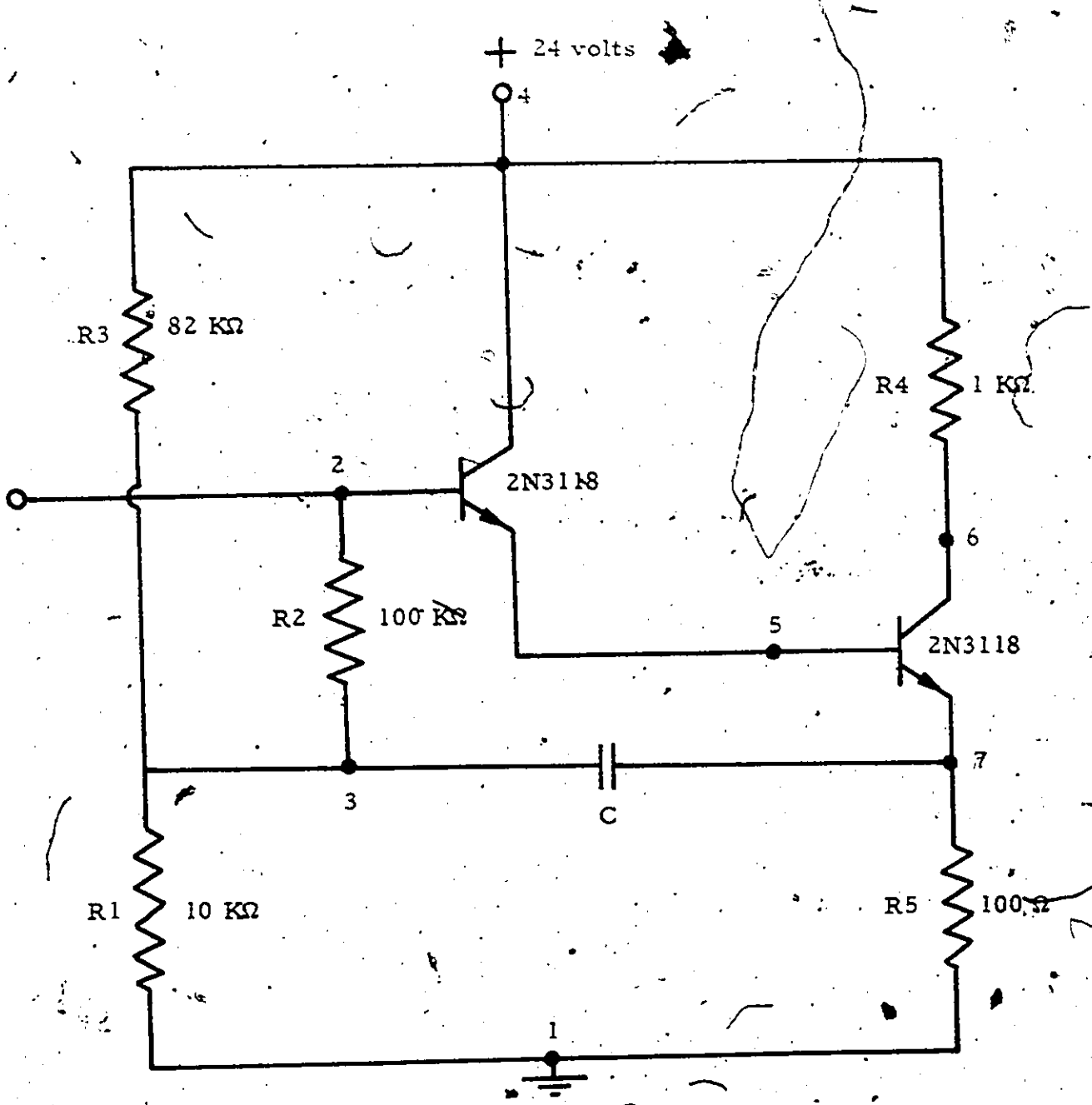


Fig. 4.5 Circuit diagram of a Darlington amplifier.

List 4.1 Data file of the circuit of Fig. 4.5 using the Ebers-Moll model.

```
$'DARLINGTON AMPLIFIER CIRCUIT
$DC

        DC  ANALYSIS

$DATUM
1
$ELEMENTS
&R1 3 1 1E4
&R2 3 2 1E5
&R3 3 4 8.2E4
&R4 6 4 1E3
&R5 7 1 1E2
&TNPN6 22 44 55 110 2.7 2.3E-14 39.0625
&TNPN7 5 66 77 110 2.7 2.3E-14 39.0625
&C8 3 7 1E-6
&C9 2 22 1E-6
&C10 6 9 1E-6
&R11 2 22 5
&R12 4 44 1.9
&R13 5 55 5.8
&R14 6 66 1.9
&R15 7 77 .8
$FIXED
NODE 4 AT 24
$INITIAL
2 2.5
5 1.9
6 12
7 1.2
22 2.5
55 1.9
66 12
77 1.2
44 24
$ANALYSIS
&STEP
&RUN
$OUTPUT
&NV 2 5 6 7
&EC 1 2 4
$EXECUTE
 TIME=    0.0                    4
NV    2  5  6  7  0      2.500171D 00    1.928805D 00    1.183361D 01    1.227
EC    1  2  4  0  0      2.599815D-04    9.964288D-07   -1.216640D-02
END OF ANALYSIS. RUN TIME REACHED
$MODIFY
```

List 4.2 Data file of the circuit of Fig. 4.5 using the proposed model.

```
$EXECUTION BEGINS...
'DARLINGTON AMPLIFIER CIRCUIT
$DC

        DC  ANALYSIS

$DATUM
1
$ELEMENTS
&R1 3 1 1E4
&R2 3 2 1E5
&R3 3 4 8.2E4
&R4 6 4 1E3
&R5 7 1 1E2
&TNPN6 22 44 55 110 2.7 2.3E-14 39.0625 278 .15 3.4E-3 .132
30.8E-12 .65 .3894 2 11.3E-12 .6 .3545 2.5 4.19E-10 4.19E-9
15 .015 1E-7 1E-7 2E-3 .1079 .5 90
&TNPN7 5 66 77 110 2.7 2.3E-14 39.0625 278 .15 3.4E-3 .132
30.8E-12 .65 .3894 2 11.3E-12 .6 .3545 2.5 4.19E-10 4.19E-9
15 .015 1E-7 1E-7 2E-3 .1079 .5 90
&C8 3 7 1E-6
&C9 2 22 1E-6
&C10 6 9 1E-6
&R11 2 22 5
&R12 4 44 1.9
&R13 5 55 5.8
&R14 6 66 1.9
&R15 7 77 .8
$FIXED
NODE 4 AT 24
$INITIAL
2 2.5
5 1.9
6 12
7 1.2
22 2.5
55 1.9
66 12
77 1.2
44 24
$ANALYSIS
&STEP
&RUN
$OUTPUT
&NV 2 5 6 7
&EC 1 2 4
$EXECUTE
TIME=    0.0                    5
NV    2  5  6  7  0      2.449611D 00    1.880568D 00    1.230800D 01    1.18
EC    1  2  4  0  0      2.595675D-04    1.460658D-06   -1.169199D-02
END OF ANALYSIS. RUN TIME REACHED
$MODIFY
```

TABLE 4.2

Device Parameters for 2N3118

I_S	$= 2.3 \times 10^{-14}$	amps
θ	$= 39.0625$	$volt^{-1}$
I_{KN}	$= 0.15$	amps
I_{KI}	$= 0.015$	amps
V_{AN}	$= 278$	volts
V_{AI}	$= 15$	volts
I_1	$= 10^{-7}$	amps
I_2	$= 3.4 \times 10^{-3}$	amps
I_3	$= 10^{-7}$	amps
I_4	$= 2 \times 10^{-3}$	amps
m	$= 0.132$	
n	$= 0.1079$	
β_{NO}	$= 110$	
β_{IO}	$= 2.7$	
A_C	$= 7.0$	
V_M	$= 70.0$	volts
R_B	$= 5$	ohms
R_C	$= 1.9$	ohms
R_E	$= 0.8$	ohms

TABLE 4.3

Comparison of Node Voltages in Fig. 4.5

Node No.	Ebers-Moll model (volts)	Proposed Model (volts)	Experimental Node voltages (volts)
2	2.5001	2.4496	2.43
5	1.9288	1.8805	1.88
6	11.833	12.308	12.2
7	1.2277	1.1802	1.21

4.7.2 Example 2 (Transient analysis)

In this example, a simple gate shown in Fig. 4.6 is simulated to demonstrate transient analysis. The transistor is a 2N4124 and its parameters are given in Table 4.4. The data files for the circuit using the Ebers-Moll model and the proposed model are given in Lists 4.3 and 4.4 respectively. The calculated input and output voltage waveforms using the Ebers-Moll model and the proposed model are shown in Fig. 4.7 and 4.8 respectively. Fig. 4.9 shows the waveforms of the input and output pulses.

Table 4.5 gives a comparison of the delay time, rise time, fall time and saturation time obtained by using the Ebers-Moll model and the proposed model with the experimental results. It may be noted that the results obtained from the proposed model match closely with the experimental results except for the saturation time. This is not surprising , since the model is based on the charge stored in the active region of the base only. An extension of the model to include the effect of charge stored in the outer regions of the base in saturation , or of the charge stored in the collector region has not been attempted. The computation time is 11.01 secs. in the case of the proposed model and 7.05 secs. when the Ebers-Moll model is used.

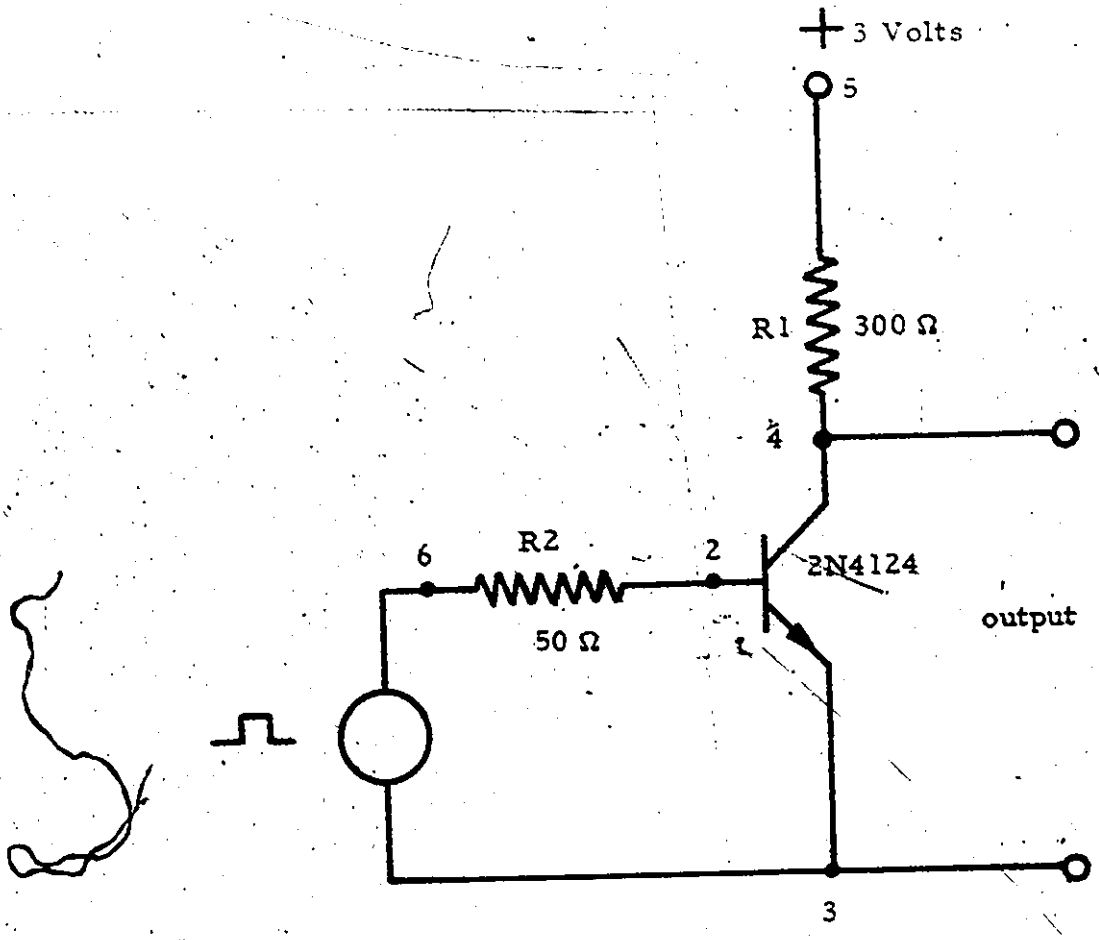


Fig. 4.6 Transistor gate for transient analysis.

TABLE 4.4

Model parameters for a 2N4124 transistor

β_{NO}	= 330	
β_{IO}	= 10	
I_s	= 1.6E-14	amps.
θ	= 38.911	volts^{-1}
V_{AN}	= 17.6	volts
V_{AI}	= 4.5	volts
I_{kN}	= 2E-2	amps
I_{kI}	= 2.2E-3	amps
I_1	= 1E-9	amps
I_2	= 8E-3	amps
m	= 0.16749	
I_3	= 1E-6	amps
I_4	= 1.5E-3	amps
n	= 0.2606	
A_C	= 5.4	
V_M	= 25	volts
C_{OE}	= 7.79E-12	farads
C_{OC}	= 5.1E-12	farads
n_E	= 0.3319	
n_C	= 0.3	
ϕ_E	= 0.65	volts
ϕ_C	= 0.6	volts
r_E	= 2.0	
r_C	= 2.5	
τ_f	= 6.4E-10	secs.
τ_r	= 5.7E-9	secs.

List 4.3 Data file of the circuit of Fig. 4.6 using the Ebers-Moll model.

```
$FILE
$TRANSIENT ANALYSIS
$DATUM
3
$ELEMENT
&R1 4 5 300
&R2 2 6 50
&QNPN3 2 4 3 330 10 1.6E-14 38.91
&CT4 2 3 7.79E-12 .65 .3319 2
&CT5 2 4 5E-12 .6 .3 2.5
&CD6 2 3 1.6E-14 6.4E-9 38.91
&CD7 2 4 1.6E-14 5.8E-10 38.91
$FIXED
NODE 5 AT 3
$INITIAL
4 3
2 0
$OUT
&NV 4 6 2
&EC 1 2
$ANALYSIS
&RUN 3E-8
&STEP .5E-10
$DRIVEN
6 5E-9 1E-8 4E-8 1.5E-8 0 .85 3E-8
$OUT
&OUT 50
&TIME
&PLOT
NV 4 6
&CHAR F K
&RANGE 0 4 0 2
$EXECUTE
$END
```

List 4.4 Data file of the circuit of Fig. 4.6 using the proposed model.

```
$FILE
$TRANSIENT ANALYSIS
$DATUM
3
$ELEMENT
&R1 4 5 300
&R2 2 6 50
&TRPN3 2 4 3 330 10 1.6E-14 38.91 17.6 2E-2 8E-3 .16749
7.79E-12 .65 .3319 2 5E-12 .6 .3 2.5 6.4E-10 5.7E-9
4.5 2.2E-3 1E-9 1E-6 1.5E-3 .2606 5.4 25
$FIXED
NODE 5 AT 3
$INITIAL
4 3
2 0
$OUT
&IV 4 6 2
&EC 1 2
$ANALYSIS
&RUN 8E-8
&STEP .5E-10
$DRIVEN
6 5E-9 1E-8 4E-8 1.5E-3 0 .05 8E-8
$OUT
&OUT 50
&TIME
&PLOT
IV 4 6
&CHAR F K
&RANGE 0 4 0 2
$EXECUTE
$END
```

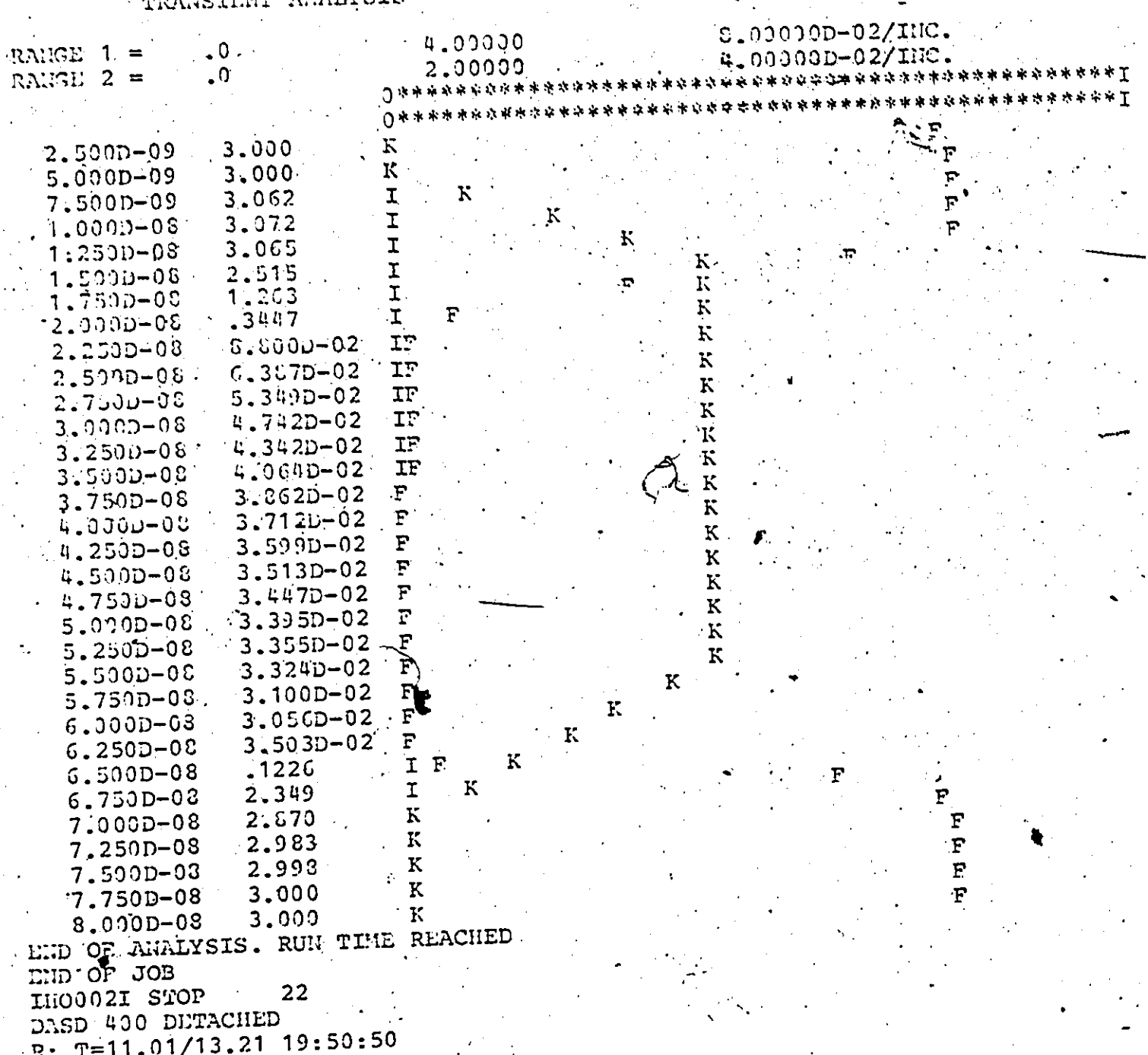
Fig. 4.7 Simulated transient response with the Ebers-Moll model.

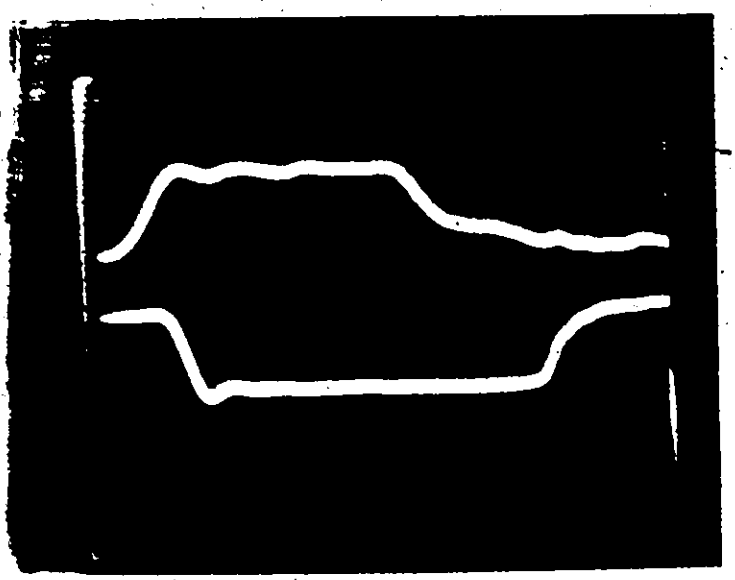
```
TRANSIENT ANALYSIS

RANGE 1 =     .0                4.00000          8.00000D-02/INC.
RANGE 2 =     .0                2.00000          4.00000D-02/INC.
                                0**********************************************I
                                0**********************************************I

  2.500D-09   3.000             K                                             F
  5.000D-09   3.000             K                                              F
  7.500D-09   3.062             I    K                                         F
  1.000D-08   3.072             I      K                                       F
  1.250D-08   3.067             I        K                                     F
  1.500D-08   2.140             I          K                    F
  1.750D-08   .4290             I    F     K
  2.000D-08   1.110D-02         F          K
  2.250D-08   1.103D-02         F          K
  2.500D-08   1.103D-02         F          K
  2.750D-08   1.103D-02         F          K
  3.000D-08   1.103D-02         F          K
  3.250D-08   1.103D-02         F          K
  3.500D-08   1.103D-02         F          K
  3.750D-08   1.103D-02         F          K
  4.000D-08   1.103D-02         F          K
  4.250D-08   1.103D-02         F          K
  4.500D-08   1.103D-02         F          K
  4.750D-08   1.103D-02         F          K
  5.000D-08   1.103D-02         F          K
  5.250D-08   1.103D-02         F          K                    F
  5.500D-08   1.103D-02         F            K
  5.750D-08   2.963D-02         F              K
  6.000D-08   .3140             I    F           K
  6.250D-08   1.964             I                K                   F
  6.500D-08   2.823             I      K                                  F
  6.750D-08   2.931             I    K                                     F
  7.000D-08   2.947             K                                          F
  7.250D-08   2.992             K                                          F
  7.500D-08   2.999             K                                          F
  7.750D-08   3.000             K                                          F
  8.000D-08   3.000             K
END OF ANALYSIS. RUN TIME REACHED
END OF JOB
IHO002I STOP     22
DASD 400 DETACHED
R; T=7.05/7.84 19:56:20
```

Fig. 4.8 Simulated transient response with the proposed model.





Input
. 5V/div.

Output
2 V/div.

- 10 nsecs./div.

Fig. 4.9 Input and output waveforms for the gate of Fig. 4.6.

Table 4.5 Comparison of the switching times.

switching times	Ebers-Moll model	Proposed model	Experimental results
delay time t_d	7.5 nsecs.	7.5 nsecs.	6 nsecs.
rise time t_r	7.5 nsecs.	10 nsecs.	10 nsecs.
fall time t_f	10 nsecs.	7.5 nsecs.	8 nsecs.
saturation time, t_s	2.5 nsecs.	10 nsecs.	23 nsecs.

4.7.3 Example 3 (Small signal analysis)

This example gives the small signal analysis of an amplifier. The amplifier circuit is shown in Fig. 4.10. The transistor used is 2N3118 whose parameters are given in Table 3.1. Here also the Ebers-Moll and the proposed model have been used to obtain the frequency response of the amplifier.

Fig. 4.11 shows the frequency response obtained with the Ebers-Moll model and Fig. 4.12 shows the frequency response with the proposed model. Fig. 4.13 gives the measured frequency response of the amplifier. In Table 4.6, comparison of the band width and the gain of the amplifier is made. It is noted that the results obtained from the proposed model match more closely with the experimental results as compared to that obtained from the Ebers-Moll model. The computation time is 2.1 secs. in the case of Ebers-Moll model and 3.35 secs. in the case of the proposed model.

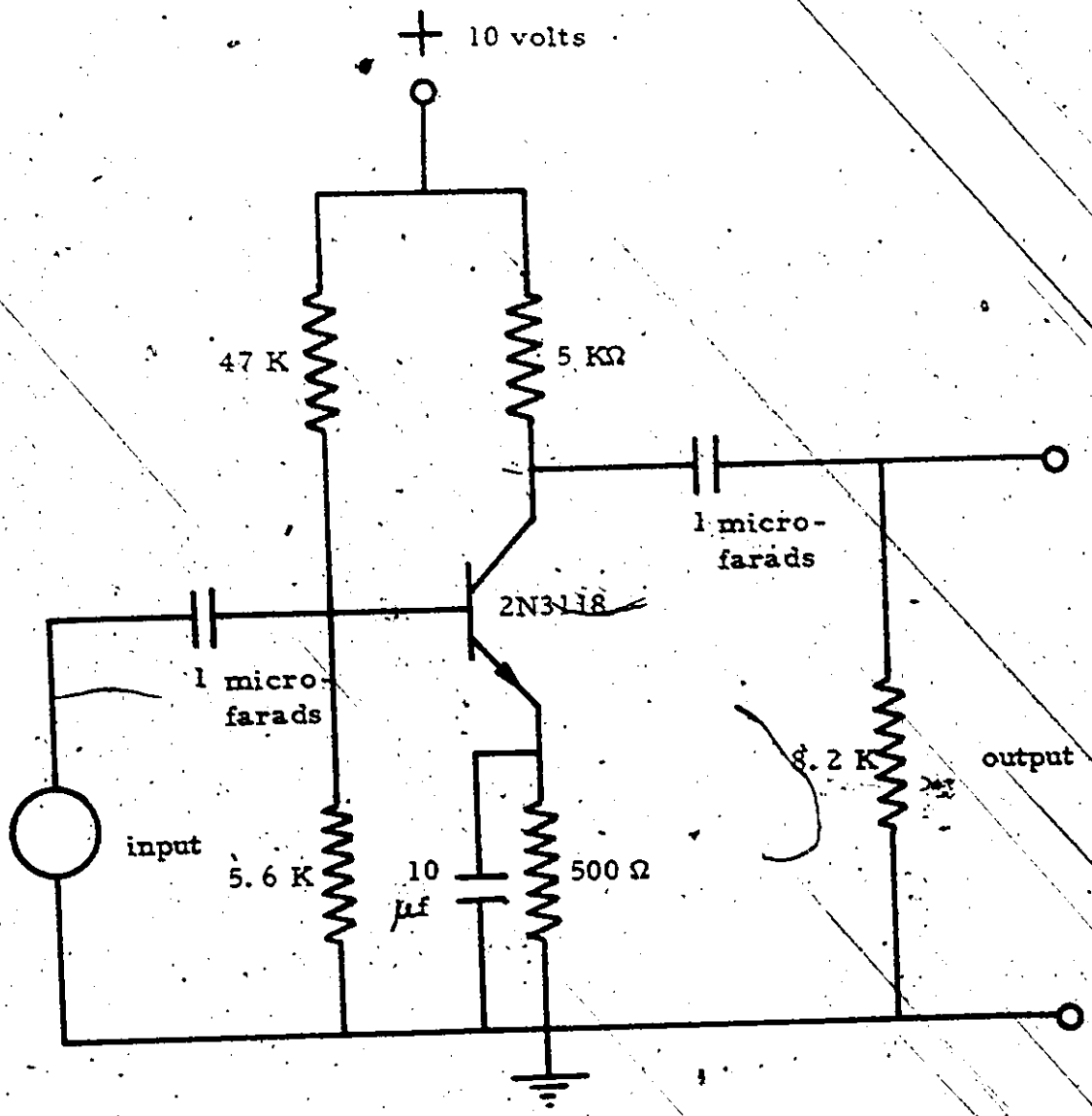


Fig. 4.10 Amplifier circuit for small signal analysis.

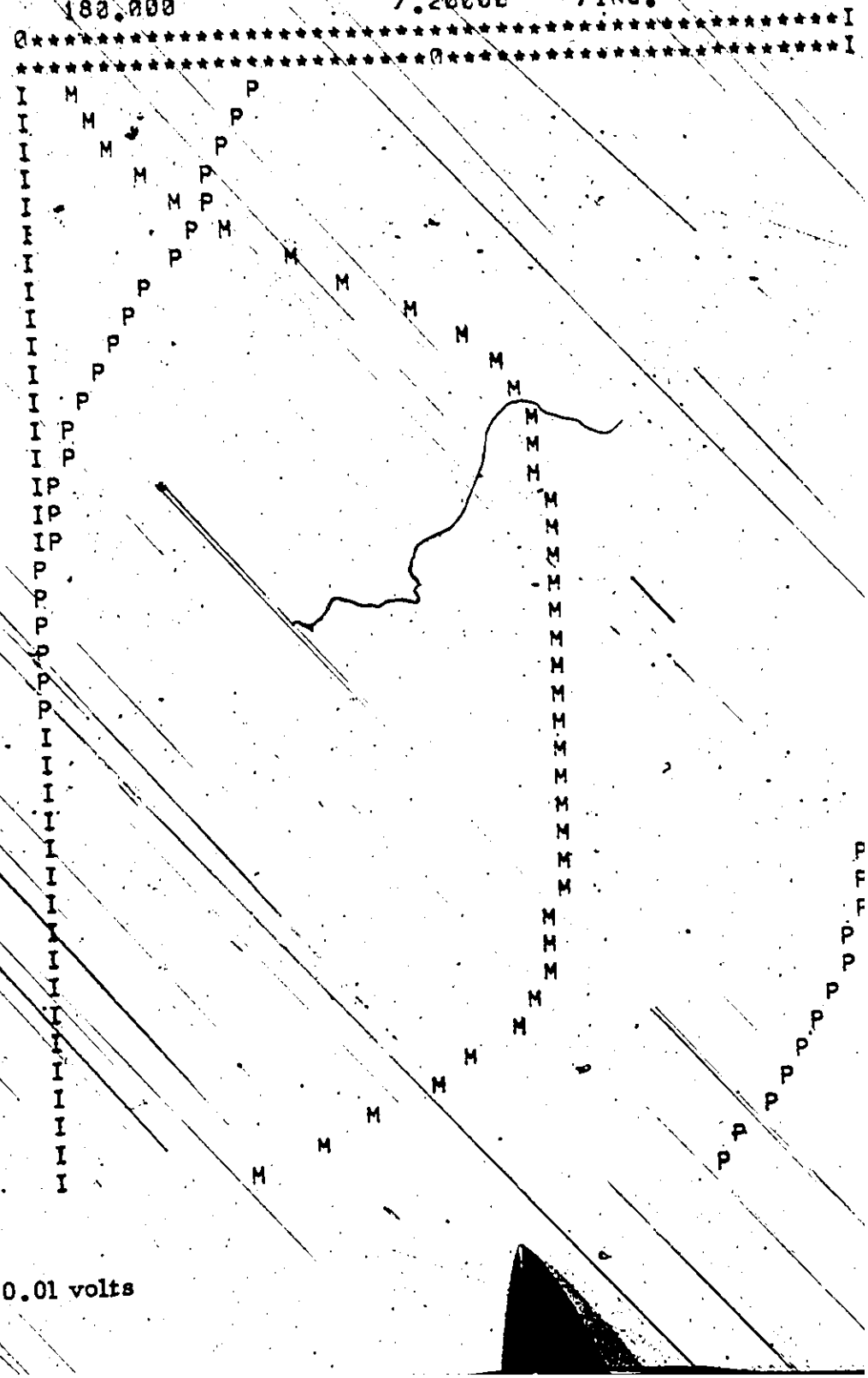
Fig. 4.11 Frequency response of the amplifier of Fig. 4.10 with the Ebers-Moll model.

BNR REMOTE TERMINAL SUPPORT SYSTEM

RANGE 1 = 0.0 1.50000 2.999998D-02/INC.

RANGE 2 = -180.000 180.000 7.20000 /INC.

Freq. (Hz)	Volts
50.00	8.0823D-02
68.37	0.1118
93.50	0.1532
127.9	0.2080
174.8	0.2791
239.1	0.3677
327.0	0.4716
447.1	0.5822
611.4	0.6861
836.1	0.7709
1143.	0.8314
1564.	0.8702
2138.	0.8933
2924.	0.9065
3999.	0.9138
5468.	0.9177
7477.	0.9199
1.0225D 04	0.9210
1.3983D 04	0.9216
1.9121D 04	0.9220
2.6148D 04	0.9221
3.5758D 04	0.9222
4.8898D 04	0.9222
6.6868D 04	0.9222
9.1441D 04	0.9221
1.2504D 05	0.9220
1.7100D 05	0.9217
2.3384D 05	0.9210
3.1977D 05	0.9200
4.3728D 05	0.9177
5.9797D 05	0.9137
8.1772D 05	0.9065
1.1182D 06	0.8933
1.5292D 06	0.8703
2.091ND 06	0.8317
2.8596D 06	0.7561
3.9104D 06	0.6843
5.3475D 06	0.5744
7.3126D 06	0.4738
9.9999D 06	0.3623

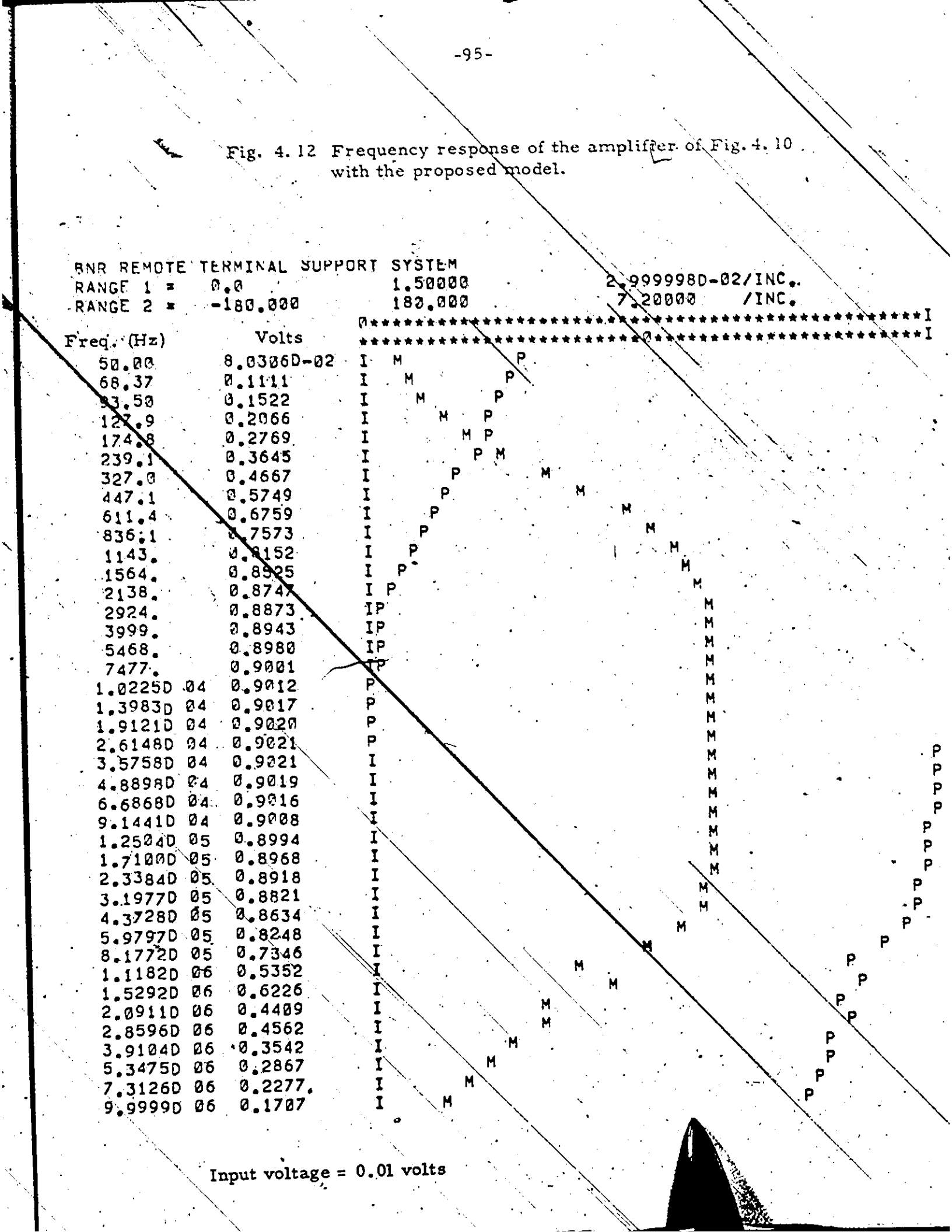


Input voltage = 0.01 volts

Fig. 4.12 Frequency response of the amplifier of Fig. 4.10 with the proposed model.

```
BNR REMOTE TERMINAL SUPPORT SYSTEM
RANGE 1 =    0.0              1.50000          2.999998D-02/INC.
RANGE 2 =   -180.000          180.000          7.20000    /INC.
```

Freq. (Hz)	Volts
50.00	8.0306D-02
68.37	0.1111
93.50	0.1522
127.9	0.2066
174.8	0.2769
239.1	0.3645
327.0	0.4667
447.1	0.5749
611.4	0.6759
836.1	0.7573
1143.	0.8152
1564.	0.8525
2138.	0.8747
2924.	0.8873
3999.	0.8943
5468.	0.8980
7477.	0.9001
1.0225D 04	0.9012
1.3983D 04	0.9017
1.9121D 04	0.9020
2.6148D 04	0.9021
3.5758D 04	0.9021
4.8898D 04	0.9019
6.6868D 04	0.9016
9.1441D 04	0.9008
1.2504D 05	0.8994
1.7100D 05	0.8968
2.3384D 05	0.8918
3.1977D 05	0.8821
4.3728D 05	0.8634
5.9797D 05	0.8248
8.1772D 05	0.7346
1.1182D 06	0.5352
1.5292D 06	0.6226
2.0911D 06	0.4409
2.8596D 06	0.4562
3.9104D 06	0.3542
5.3475D 06	0.2867
7.3126D 06	0.2277
9.9999D 06	0.1707



Input voltage = 0.01 volts

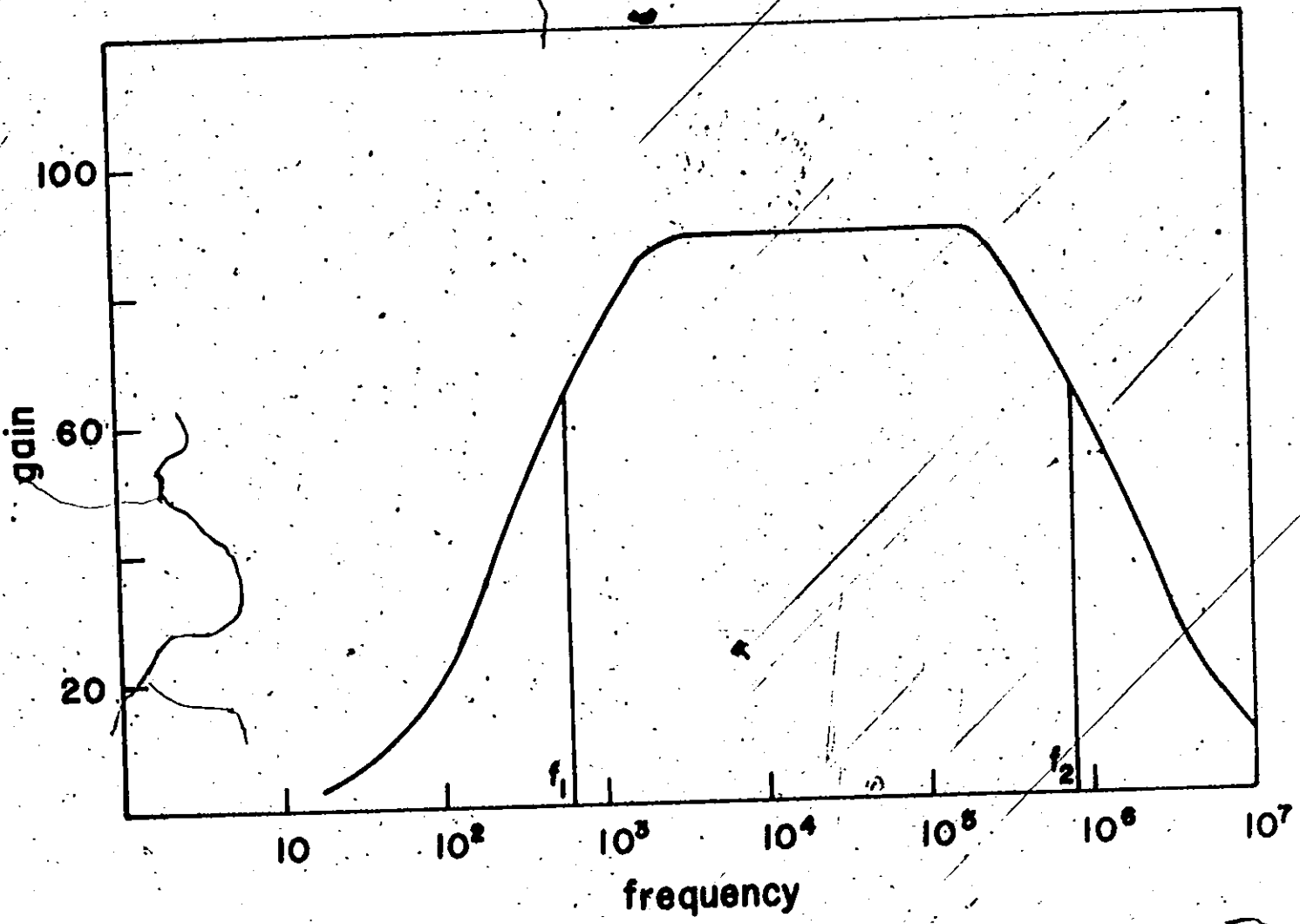


Fig. 4.13 Measured frequency response of the amplifier of Fig. 4.10.

Table 4.6 Comparison of Gain and cut-off frequencies of the amplifier of Fig. 4.10.

	Ebers-Moll model	Proposed model	Measured results
Gain	92.22	90.21	88.0
f_1	600 Hz	600 Hz	600 Hz
f_2	4.0×10^6 Hz	1.2×10^6 Hz	0.8×10^6 Hz

4.7.4 Example 4

In the previous examples, the use of the model is illustrated with simple circuits. In this example the model has been used to analyse the amplifier shown in Fig. 4.14. This amplifier is the main amplifier of the 274 Mb/s digital repeater [50] used to provide amplification to compensate cable, equaliser and ALBO losses in the LD 4 digital transmission system. The amplifier is a thick film hybrid circuit, shown in Fig. 4.15. It provides 22.5 ± 1.5 db of gain in the frequency range 100 KHz to 300 MHz.

The circuit is basically a series-series triple (Q1-Q3) with dual output. A diode at the input stabilizes the operating point of the first transistor with temperature. A split voltage feedback bias scheme stabilizes the current through Q1 against changes in supply voltage. Following is the simulation procedure.

A) Simulation Procedure

The first step is to obtain the parameters of the transistors. The amplifier consists of two types of transistors, low power (Q1 and Q2) on one chip, and medium power (Q3 and Q4) The parameters were obtained by the measuring procedure outlined in Chapter 3. Table 4.7 summarizes all the parameters for the four transistors. Table 4.8 gives the stray components.

The next step is to build the data file for the circuit. As indicated before, the file is written in the manner required for NANSIM. The data file is printed out in List 4.5.

Finally the circuit is analysed to give the d.c. node voltages and the frequency response of the amplifier. Voltage

variation and temperature effects have also been predicted. The temperature dependence of currents can be evaluated by calculating the dependence of I_s, as given by Logan [15].

B) Results

Table 4.9 compares the simulated collector node voltages with the measured voltages. It may be noted that the maximum error is 3%. Table 4.10 provides the collector node voltage change with the change of supply voltage. Table 4.11 gives the change in collector node voltage with the temperature increased to 80°C from room temperature. Also in Table 4.10 and 4.11 the percentage change is compared with the measured change.

The frequency response with the normal supply voltage of 14.5 volts is given in Fig. 4.16. Fig. 4.17 and 4.18 give the frequency response with supply voltages of 13.7 and 15.3 volts respectively. It is noted that there is negligible change in the frequency response. The calculated power gain vs frequency is shown in Fig. 4.19. The calculated power gain is 23.8 db and the band width is 350 MHz. These results are very close to the amplifier specification of 22.5 ± 1.5 db gain in the frequency range of 100 KHz to 300 MHz.

The simulation of a practical circuit in this example shows that the results obtained with the proposed model match closely with the measured results. The computer time for obtaining the frequency response is of the order of 6 secs.

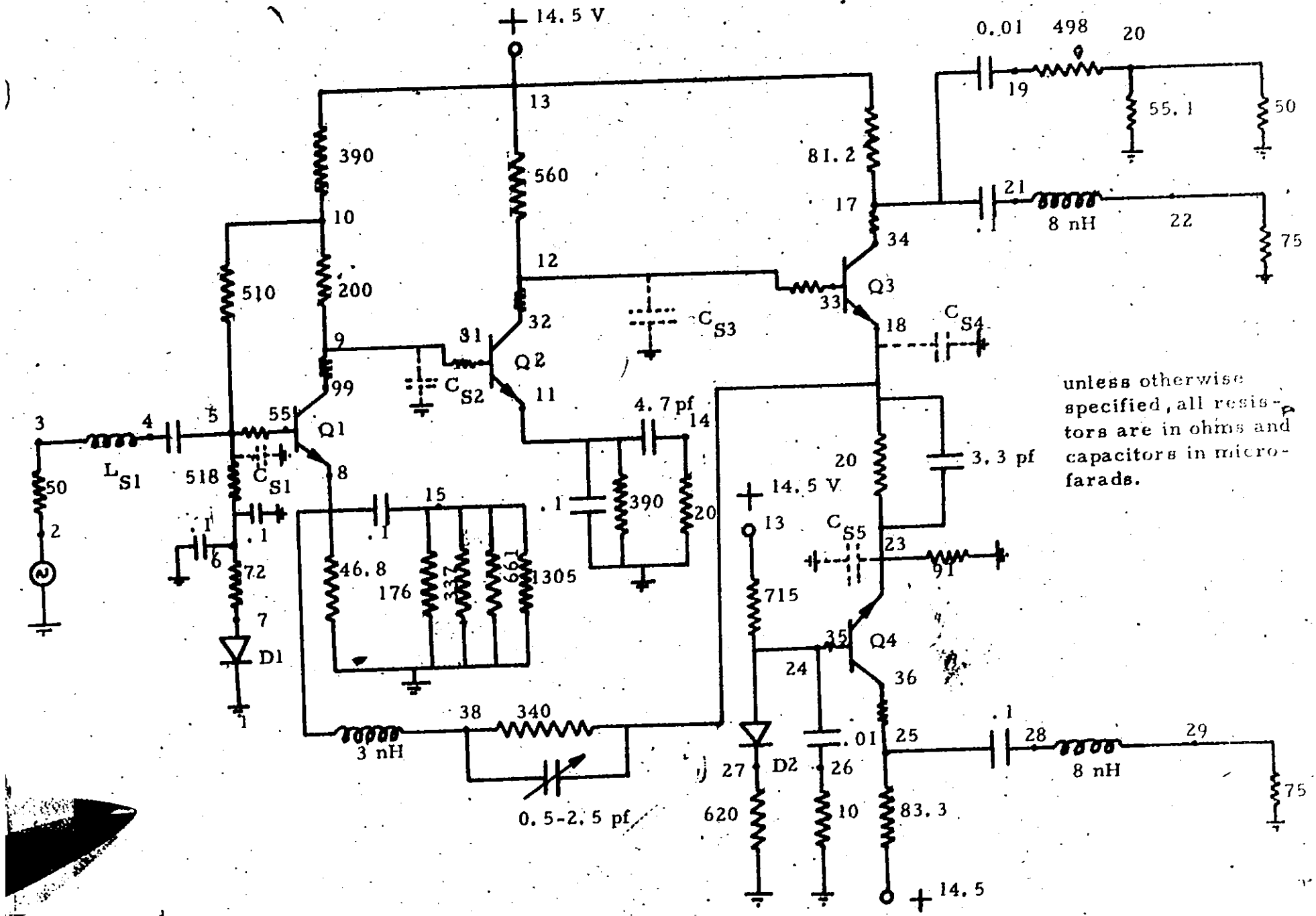


Fig. 4.14 Circuit diagram of the main amplifier.

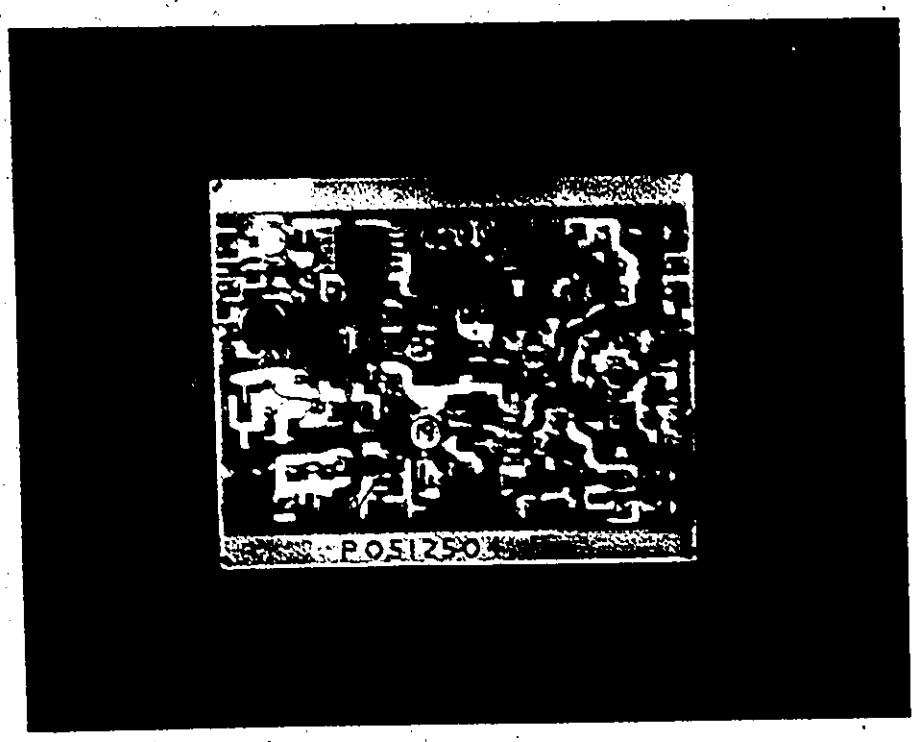


Fig. 4.15 Photograph of the hybrid circuit of the amplifier

Table 4.7 Transistors Parameters.

Parameter	Q1	Q2	Q3	Q4
θ	38.376	38.376	38.376	38.376
I_s	5.3E-16	4.5E-16	2E-15	2E-15
β_{NO}	110.0	108.	96	96
β_{IO}	3.8	4.2	6.8	6.8
I_{kN}	9E-3	8.5E-3	3.5E-2	3.5E-2
I_{kI}	7E-4	7E-4	7E-4	7E-4
V_{AN}	47	49	68	68
V_{AI}	2.1	2.38	4	4
I_1	2E-6	2E-6	2E-6	2E-6
I_2	2E-4	1E-4	4E-5	4E-5
m	0.1337	0.06214	0.1409	0.1409
I_3	2E-6	1.5E-6	3E-6	3E-6
I_4	6E-4	9E-4	5E-3	5E-3
n	0.1153	0.1132	0.1473	0.1473
C_{0E}	.995E-12	1.145E-12	3E-12	3E-12
C_{0C}	1E-12	1E-12	2E-12	2E-12
n_E	0.26	0.224	0.28	0.28
n_C	0.33	0.33	0.35	0.35
ϕ_E	0.65	0.65	0.65	0.65
ϕ_C	0.65	0.65	0.65	0.65
r_E	3.5	3	4	4
r_C	4	4	5	5
τ_f	3.42E-11	3.42E-11	4.582E-11	4.582E-11
τ_r	5.51E-10	5.51E-10	3.5E-10	3.5E-10
R_B	15	15	12	12
R_C	3	3	1	1

Table 4.8 List of strays

stray	value
C_{S1}	1.5 pf
C_{S2}	1.3 pf
C_{S3}	1.3 pf
C_{S4}	1.4 pf
C_{S5}	1.4 pf
L_{S1}	3 nH
L_{S2}	3 nH

List 4.5 Data file of the circuit of Fig. 4.14

```
$FILE
$DC
$DATUM
1
$ELEMENTS
&R1 5 6 51.8
&R2 7 6 72
&R3 5 10 510
&R4 10 13 390
&R5 9 10 200
&R6 8 1 46.8
&R7 15 1 176.2
&R8 18 38 340
&R9 15 1 337
&R10 15 1 661
&R11 12 13 560
&R12 11 1 390
&R13 15 1 .1305
&R14 14 1 20
&R15 13 24 715
&R16 27 1 620
&R17 26 1 10
&R19 17 13 81.2
&R20 18 23 20
&R21 25 13 33.3
&R24 19 20 498
&R25 23 1 91
&R27 20 1 55.1
&R28 2 3 50
&R29 20 1 50
&R30 22 1 75
&R22 29 1 75
&R35 5 55 15
&R36 9 99 3
&R37 9 31 15
&R38 12 32 3
&R39 12 33 12
&R40 17 34 1
&R65 24 35 12
&R67 25 36 1
&L31 3 4 1.5E-9
&L32 21 22 8E-9
&L33 28 29 8E-9
&L34 8 38 3E-9
&C41 4 5 1E-7
&C42 6 1 1E-7
&C43 8 15 1E-7
```

Data file of Fig. 4.14 (contd.)

```
&C44 38 16 5E-13
&C45 11 1 1E-7
&C46 11 14 4.7E-12
&C47 24 26 1E-8
&C49 17 19 1E-8
&C50 17 21 1E-7
&C51 16 23 3.3E-12
&C52 25 28 1E-7
&C53 9 1 1.3E-12
&C54 12 1 1.3E-12
&C55 10 1 1.4E-12
&C56 23 1 1.4E-12
&C57 5 1 1.5E-12
&TNPN61 35 99 8 100 4.2 4.5E-16 38.2764 49 6.5E-3 1E-4 0.06215 3.42E-11 5.5E-10
'1.145E-12 .65 .224 2 1E-12 .65 .33 4 3.42E-11 5.51E-10
'2.3 7E-4 2E-6 1.5E-6 9E-4 0.113231977
&CT86 55 99 1E-12 .65 .33 4
&CT87 55 8.1.145E-12 .65 .224 3.5
&TNPN62 31 32 11 110 3.8 5.2E-16 38.2764 47 9E-3 2E-4 .13375 3.42E-11 5.51E-10
'.995E-12 .65 .26 2 1E-12 .65 .33 4 3.42E-11 5.8435E-10
'2.1 7E-4 2E-6 2E-6 6E-4 0.1153934
&CT90 31 32 1E-12 .65 .33 4
&CT91 31 11 .995E-12 .65 .26 3
&TNPN63 33 34 18 96 6.8 2E-15 38.2764 68 3.5E-2 4E-5 0.1409 4.582E-11 3.56E-10
'3E-12 .65 .28 4 2E-12 .65 .35 5 4.582E-11 3.458E-10
'4 7E-4 2E-6 3E-6 5E-3 0.1473195
&CT94 35 36 2E-12 .65 .35 5
&CT95 33 34 2E-12 .65 .35 5
&CT96 33 16 3E-12 .65 .28 4
&CT97 35 23 3E-12 .65 .28 4
&TNPN64 35 36 23 96 6.8 2E-15 38.2764 68 3.5E-2 4E-5 0.1409 4.582E-11 3.5E-10
'3E-12 .65 .28 4 2E-12 .65 .35 5 4.582E-11 3.458E-10
'4 7E-4 2E-6 3E-6 5E-3 0.1473195
&D71 7 1 2E-15 38.2764
&D72 24 27 2E-15 38.2764
&CT81 7 1 5E-12 .65 .28 2
&CT82 24 27 5E-12 .65 .28 2
&CD83 7 1 2E-15 6.91E-11 38.2764
&CD84 24 27 2E-15 6.91E-11 38.2761
$FIXED
NODE 13 AT 14.5
$INITIAL
5 1.375
6 .94
7 .76
8 .456
```

Data file of Fig. 4.14 (contd.)

```
9 4.66
10 6.6
11 3.84
12 7.12
17 11.65
18 6.3
23 5.55
24 6.42
25 12.77
27 5.66
55 1.374
99 4.66
31 4.66
32 7.12
33 7.12
34 11.65
35 6.42
36 12.77
$ANALYSIS
$OUTPUT
&NV 5 6 7 8 9 10 11 12 17 18 24 23 25 27
&LC 1 2 3 5 6  11 12 19 20 25 15 16 21 36 38 40 67
$EXECUTE
$MODIFY
$SSIG
$SSDRIVE
&POLAR 2 1E-2 0
$SSOUTPUT
&NV 29 28 22 12 17 9
&PLOT
NV 29.
&POLAR
&LENGTH 50
&RANGE 0 .2 -180 180
&FRLQ
&CHAR M P
$ANALYSIS
&LOGFREQUENCY 1000 3E9 40
$EXECUTE
$MODIFY
$END
```

Table 4.9 Simulated and measured collector node voltages.

Transistor	Simulated collector voltage (volts)	Measured collector voltage (volts)	% Error
Q1	5.34750	5.35	-0.046
Q2	7.55423	7.36	2.57
Q3	10.75454	10.60	1.436
Q4	11.53906	11.19	3.025

Table 4.10 Collector node voltage change with change of supply voltage.

Transistor	13.7 (volts)	14.5 (volts)	15.3 (volts)	% change (computed)	% change (measured)
Q1	5.0892	5.3475	5.6053	-4.83, 4.82	-7.4, 5.9
Q2	7.1608	7.5542	7.9469	-5.207, 5.1	-5.5, 4.9
Q3	10.1745	10.7545	11.3355	-5.39, 5.4	-7.6, 7.8
Q4	10.9035	11.5390	12.1743	-5.5, 5.49	-5.5, 4.1

Table 4.11 Collector node voltage change with change of temperature.

Transistor	Collector voltage at room temp. (28.7 C)	Collector voltage at 80°C	% change (computed)	% change (measured)
Q1	5.3475	5.2262	-2.268	-1.5
Q2	7.5542	7.4621	-1.219	-2.3
Q3	10.7545	10.7066	-4.453	-5.0
Q4	11.539	11.5025	-3.163	-4.0

Fig. 4.16 Frequence response of the amplifier of Fig. 4.14 with supply voltage of 14.5 volts.

SMALL SIGNAL ANALYSIS

RANGE 1 = .0 .200000 4.00000D-03/INC.
RANGE 2 = -180.000 180.000 7.20000 /INC.

Freq. (Hz)	Volts	
1000.	1.852D-04	P
1466.	4.138D-04	MP
2149.	9.119D-04	M
3149.	2.103D-03	IM
4617.	4.996D-03	IM
6767.	1.079D-02	I M
9919.	2.201D-02	I M
1.454D+04	3.604D-02	I M
2.131D+04	5.053D-02	I M
3.124D+04	6.344D-02	I M
4.579D+04	7.229D-02	I M
6.712D+04	7.932D-02	I M
9.838D+04	8.474D-02	I M
1.442D+05	8.851D-02	I M
2.114D+05	9.070D-02	I M
3.099D+05	9.191D-02	I M
4.542D+05	9.251D-02	I M
6.658D+05	9.279D-02	I M
9.760D+05	9.291D-02	I M
1.431D+06	9.297D-02	I M
2.097D+06	9.301D-02	I M
3.074D+06	9.302D-02	I M
4.506D+06	9.303D-02	I M
6.604D+06	9.304D-02	I M
9.681D+06	9.299D-02	I M
1.419D+07	9.305D-02	I M
2.080D+07	9.307D-02	I M
3.049D+07	9.311D-02	I M
4.469D+07	9.322D-02	I M
6.551D+07	9.341D-02	I M
9.603D+07	9.376D-02	I M
1.408D+08	9.419D-02	I M
2.063D+08	9.352D-02	I M
3.024D+08	8.550D-02	I M
4.433D+08	5.906D-02	I M
6.498D+08	2.847D-02	I M
9.525D+08	1.099D-02	I M
1.396D+09	3.320D-03	IM
2.047D+09	7.024D-04	M
3.000D+09	1.181D-04	M

MODIFY

Send

Input voltage = 0.01 volts.

END OF JOB

Fig. 4.17 Frequency response of the amplifier of Fig. 4.14 with supply voltage of 13.7 volts.

SMALL SIGNAL ANALYSIS

RANGE 1 = .0 .200000 4.000000-03/INC.
RANGE 2 = -100.000 100.000 2.000000 /INC.

Freq. (Hz)	Volts
1030.	3.9150-04
1466.	4.2120-04
2140.	4.2770-04
3140.	2.3440-03
4617.	5.0780-03
6767.	1.0870-02
9910.	2.2510-02
1.4540+04	3.6450-02
2.1310+04	5.1340-02
3.1240+04	6.3990-02
4.5790+04	7.2600-02
6.7120+04	7.8730-02
9.8390+04	8.5020-02
1.4420+05	8.8670-02
2.1140+05	9.0790-02
3.0970+05	9.1940-02
4.5420+05	9.2520-02
6.6550+05	9.2790-02
9.7660+05	9.2910-02
1.4310+06	9.2970-02
2.0970+06	9.3000-02
3.0740+06	9.3010-02
4.5060+06	9.3020-02
6.6040+06	9.3040-02
9.6810+06	9.3060-02
1.4190+07	9.3090-02
2.0800+07	9.3160-02
3.0490+07	9.3320-02
4.4690+07	9.3650-02
6.5510+07	9.4350-02
9.6030+07	9.5720-02
1.4080+08	9.7980-02
2.0630+08	9.8800-02
3.0240+08	8.3130-02
4.4330+08	4.5050-02
6.4980+08	1.8390-02
9.5250+08	6.4430-03
1.3960+09	1.7730-03
2.0470+09	3.5460-04
3.0000+09	6.6000-05

MODIFY

Input voltage= 0.01 volts

$end
END OF JOB

Fig. 4.18 Frequency response of the amplifier of Fig. 4.14 with supply voltage of 15.3 volts.

SMALL SIGNAL ANALYSIS

RANGE 1 = .0 .200000 5.000000-07/INC.
RANGE 2 = -100.000 100.000 7.00000 /INC.

Freq. (Hz)	Volts
1000.	1.0500-04
1466.	4.0070-04
2149.	8.9640-04
3149.	2.0730-03
4617.	4.9150-03
6767.	1.0547-02
9919.	2.1720-02
1.4540+04	3.5020-02
2.1310+04	5.0020-02
3.1240+04	6.2980-02
4.5790+04	7.1760-02
6.7120+04	7.9800-02
9.8390+04	8.4430-02
1.4420+05	8.8310-02
2.1140+05	9.0570-02
3.0990+05	9.1020-02
4.5420+05	9.2450-02
6.6550+05	9.2740-02
9.7600+05	9.2870-02
1.4310+06	9.2930-02
2.0970+06	9.2960-02
3.0740+06	9.2980-02
4.5060+06	9.2990-02
6.6040+06	9.3000-02
9.6810+06	9.3060-02
1.4190+07	9.3050-02
2.0800+07	9.3120-02
3.0490+07	9.3270-02
4.4690+07	9.3590-02
6.5510+07	9.4260-02
9.6030+07	9.5500-02
1.4080+08	9.7810-02
2.0630+08	9.8980-02
3.0240+08	8.4060-02
4.4330+08	4.7120-02
6.4960+08	1.9340-02
9.5250+08	6.8120-03
1.3960+09	1.8830-03
2.0470+09	3.7040-04
3.0000+09	7.0630-05

MODIFY

Input voltage = 0.01 volts

END OF JOB

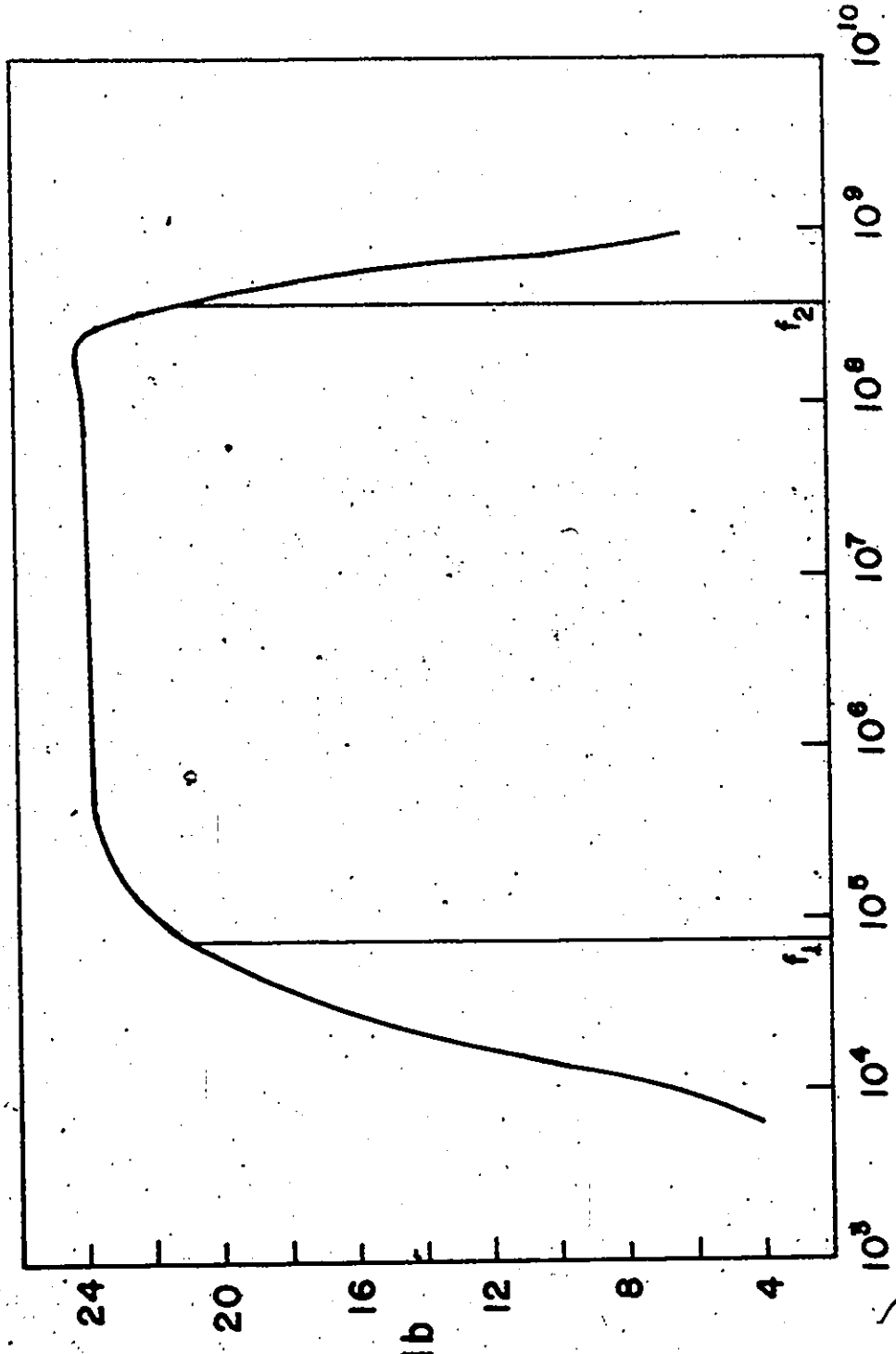


Fig. 4.19 Power gain of the amplifier (calculated).

CHAPTER 5

CONCLUSIONS

In this thesis , a model of the bipolar transistor has been developed for the analysis and design of transistorized circuits with the use of a computer. Whilst it was recognised at the beginning of this work that the Gummel-Poon model gave a fairly accurate representation of the bipolar transistor , its complexity is such that it is a deterrent for general usage. Both the determination of its parameters , and its inclusion in a computer program , require an appreciable amount of work , not to mention the computer time required for the analysis. The model developed includes some non-linear effects in the transistor: base width modulation , low current fall-off of ' β ' , base conductivity modulation and the avalanche multiplication. The model is more complex than the Ebers-Moll model , but much less involved than the Gummel-Poon model. In particular , most of its parameters can be determined by simple measurements.

After a brief description of the Ebers-Moll model and the Gummel-Poon model , the latter is extended for the small signal analysis. A fast algorithm has been developed for solving the non-linear equations in this model. Then the proposed model is developed. It is based on the Ebers-Moll transport model, modified by a simplified charge control relation. The model equations are in a form that is convenient for the NANSIM program. This program , developed and made available by Bell Northern Research Lab. of Ottawa , allows the inclusion of a variety of models into

the program. This is the main feature , besides its ready availability , that led to its selection over a number of other programs which could have been used.

The intrinsic model requires 26 parameters and these are obtained from a few sets of measurements. Details of how each parameter is obtained is given. Several characteristics of the transistors using the measured parameters are obtained using the model, and the results are compared with the experimental characteristics to verify the accuracy of the model.

The use of the model with NANSIM is described , and four examples are given to illustrate the application of the model in d. c. , a. c. and transient analysis. In each case , the results are compared with the experimental results , and found to match closely. A comparison is also made with with the results obtained with the Ebers-Moll model in the first three examples. Although the answers are very similar , for such simple examples , those obtained with the proposed model show a degree of improvement.

5. 1 Suggestion for Further Work

Although the model includes a number of non-linear effects in the bipolar transistor , some have not been included in order to limit the complexity of the model. Not all the known non-linear effects appear in a given mode of operation , and the model may be modified to suit the application at hand. What is needed , though , is a means to add some of the effects not considered in this thesis. For instant, the base push-out effect at high current can be included by making the forward transit time and the base charge a function of current and voltage. It is less

evident how the excess charges stored in the remote region of the base under saturation can be included. If the model is to be used in switching circuit design, this storage effect should be modeled.

The base resistance R_B and the collector resistance R_C have been assumed to be constant, but they are known to be current dependent. The intent of this work was to obtain a model that lends itself to computer aided design techniques without being of such complexity as to deter possible uses. A number of assumptions had to be made, and this has lead to a compromise situation. Some of the work mentioned above could have been done, but this would have increased the complexity of the model. It is felt that further development of the model should be made with specific application in mind.

APPENDIX I

Derivation of Charge Control Relation

The electron and hole current density equations for a one-dimensional analysis are given by [30],

$$J_n = q D_n \frac{dn}{dx} + \mu_n q n \mathcal{E} \qquad \text{(A1-1)}$$

$$J_p = - q D_p \frac{dp}{dx} + q \mu_p p \mathcal{E} \qquad \text{(A1-2)}$$

where the symbols have their usual meaning

For a n-p-n transistor, if it is assumed that there is no recombination in the base region,

$$J_p = 0$$

and from (A1-2), the electric field is given by

$$\mathcal{E} = \frac{1}{p} \frac{D_p}{\mu_p} \frac{dp}{dx}$$

Using the Einstein relationship,

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{q} \qquad \text{(A1-3)}$$

we get

$$\mathcal{E} = \frac{1}{p} \cdot \frac{kT}{q} \frac{dp}{dx} \qquad \text{(A1-4)}$$

Substituting (A1-4) in (A1-1) and using (A1-3) we get

$$J_n = q D_n \left[\frac{dn}{dx} + \frac{1}{p} \frac{dp}{dx} n \right] \qquad \text{(A1-5)}$$

or

$$p \frac{dn}{dx} + n \frac{dp}{dx} = \frac{J_n p}{q D_n} \qquad \text{(A1-6)}$$

Integrating the above from 0 to w, where w is the base width, we get

$$\left[n\,p \right]_0^w = \frac{J_n}{q} \int_0^w \left(\frac{p}{D_n} \right) dx \qquad \text{(A1-7)}$$

from this,

$$J_n = \frac{-q \left[n(o)\, p(o) - n(w)\, p(w) \right]}{\int_0^w \left(\frac{p}{D_n} \right) dx} \qquad \text{(A1-8)}$$

Assuming constant or average value for D_n

$$J_n = \frac{-D_n q^2 \left[n(o)\, p(o) - n(w)\, p(w) \right]}{Q_B} \qquad \text{(A1-9)}$$

where $Q_B = \int_o^w q\, p(x)\, dx$ (A1-10)

i.e. total majority charge in the base of n-p-n transistor

Now from the Shockley boundary condition we have,

$$n(o)\, p(o) = n_i^2 \, e^{\frac{qV_{EB}}{kT}} \qquad \text{(A1-11)}$$

$$n(w)\, p(w) = n_i^2 \, e^{\frac{qV_{CB}}{kT}} \qquad \text{(A1-12)}$$

where V_{EB} is Emitter-base junction bias and V_{CB} is collector base junction bias.

Substituting (A1-11) and(A1-12) in (A1-9), we get

$$J_n = \frac{-D_n q^2 n_i^2 \left[e^{\frac{qV_{EB}}{kT}} - e^{\frac{qV_{CB}}{kT}} \right]}{Q_B} \qquad \text{(A1-13)}$$

Thus $I_{CC} = -A * J_n$

where A is the area of the junction,

$$\text{or} \quad I_{CC} = \frac{A D_n q^2 n_i^2 \left[e^{\frac{qV_{EB}}{kT}} - e^{\frac{qV_{CB}}{kT}} \right]}{Q_B} \qquad \text{(A1-14)}$$

This is the dominant component of the collector current (electron). The expression (A1-14) is known as charge control relation.

APPENDIX II

A Fast Algorithm for Solving ICM Equations

This appendix describes an algorithm which is applicable to solve the ICM equations [51]. As pointed out in section 2.3.2, the collector current 'I_C' is a function of the base push out factor 'B' (equations 2.27a and 2.31) and 'B' is a function of 'I_C' (equation 2.33). This relationship may be expressed as

$$B = f(I_C) \qquad \text{(A2-1)}$$

$$I_C = f(B) \qquad \text{(A2-2)}$$

Equations (A2-1) and (A2-2) are non-linear equations and these are to be solved for 'I_C' and 'B'. The curves for $I_C(B)$ and $B(I_C)$ are plotted for a typical high injection condition in Fig. A2-1. As shown by the dotted lines, the simple iterative scheme tends to diverge or may lead to oscillatory solutions. This is because the magnitude of the slope of $B(I_C)$ at the intersecting point is greater than that of $I_C(B)$. In cases where the slope of $B(I_C)$ is not greater than that of $I_C(B)$ and the iteration process converges, a large number of iterations may be required. In order to avoid these shortcomings, a new iterative scheme has been developed. It is described below

The key feature of this new scheme is that in order to obtain the value of $I_C(B)$, the 'B' used is not the previous value, as was the case in the previous iterative scheme, but rather a new predicted 'B' is used. Similarly for $B(I_C)$, 'I_C' is a new predicted value. These new predicted values of 'B' and 'I_C' are obtained by linear interpolation.

Prediction of new 'B'

In order to describe the prediction of new 'B', let us assume that we have already predicted a new I_C (i.e. we are in the iteration process). This is denoted as I_{C1} (point 1) in Fig. A2-1. In this prediction assume that the values B1, I_{CC} and B2 are used.

Now using this I_{C1}, BB is calculated and from this I_{C2} is calculated, as shown in Fig. A2-1, A New value of 'B' is then obtained by joining B2 to BB and I_{CC} to I_{C2}. Intersection of these two lines gives new 'B' and is denoted as 'B1' (point 2). The value of new 'B' is obtained from the following relations.

$$\frac{I_C - I_{C1}}{B - BB} = \frac{I_{CC} - I_{C1}}{B2 - BB} = m \qquad \text{(A2-3)}$$

$$\frac{I_C - I_{C2}}{B - BB} = \frac{I_{CC} - I_{C2}}{B1 - BB} = n \qquad \text{(A2-4)}$$

from (A2-3) and (A2-4)

$$B = BB + \frac{I_{C2} - I_{C1}}{(m - n)} \qquad \text{(A2-5)}$$

This gives new 'B'

Prediction of new 'I_C'

From the above predicted new 'B' denoted as B1, I_{CC} is calculated and from I_{CC}, B2' is calculated as shown in Fig. A2-1. The new 'I_C' is obtained by joining I_{CC}' to I_{C2} and B2' to BB. The intersection of these two lines gives new 'I_C' and is denoted as 'I_{C1}'. This is obtained from the following relations.

$$\frac{B - B1}{I_C - I_{CC}'} = \frac{BB - B1}{I_{C2} - I_{CC}} = m' \qquad (A2\text{-}6)$$

$$\frac{B - B2'}{I_C - I_{CC}'} = \frac{BB - B2}{I_{C1} - I_C} = n' \qquad (A2\text{-}7)$$

from (A2-6) and (A2-7)

$$I_C = I_{CC}' + \frac{B2' - B1}{m' - n'} \qquad (A2\text{-}8)$$

This gives the new I_C

This converging scheme is described by solid lines in Fig. A2-1. Point '1' is the predicted new I_C, point '2' is the predicted new 'B' and again point '3' is the predicted new I_C.

The algorithm used in the computer for the above converging scheme is as follows,

Step 1	Start with B = 5 (say)	denote as B1
Step 2	Calculate I_C (B)	denote as I_{CC}
Step 3	Calculate B (I_C)	denote as B2
Step 4	Predict new I_C	denote as I_{C1}
Step 5	Calculate B (I_C)	denote as BB
Step 6	Calculate I_C(B)	denote as I_{C2}
Step 7	Predict new B	denote as B1

Step 4 and step 7 are obtained from equations (A2-8) and (A2-5) respectively. Repeat the cycle from step 2 to step 6 if the difference between the previous I_C and the new I_C does not converge within the

prescribed error. It may be noted that in the first run the prediction of new 'I_C' cannot be done for step 4 because BB; and I_{C2} are not known, so it is calculated as $I_C(B)$. For subsequent runs the above scheme follows automatically.

The above algorithm is used to describe the characteristics of the BFY 90 transistor. The estimated 21 Gummel-Poon parameters of a BFY 90 transistor are given in table A2-1. Fig. A2-2 shows the semilog plot of I_C vs V_{BE} (transfer characteristics) for V_{CB} = 0 1, 2, 3 volts. The number of iterations required is only 3 to 4 in high level conditions ($V_{BE} > 0.85$).

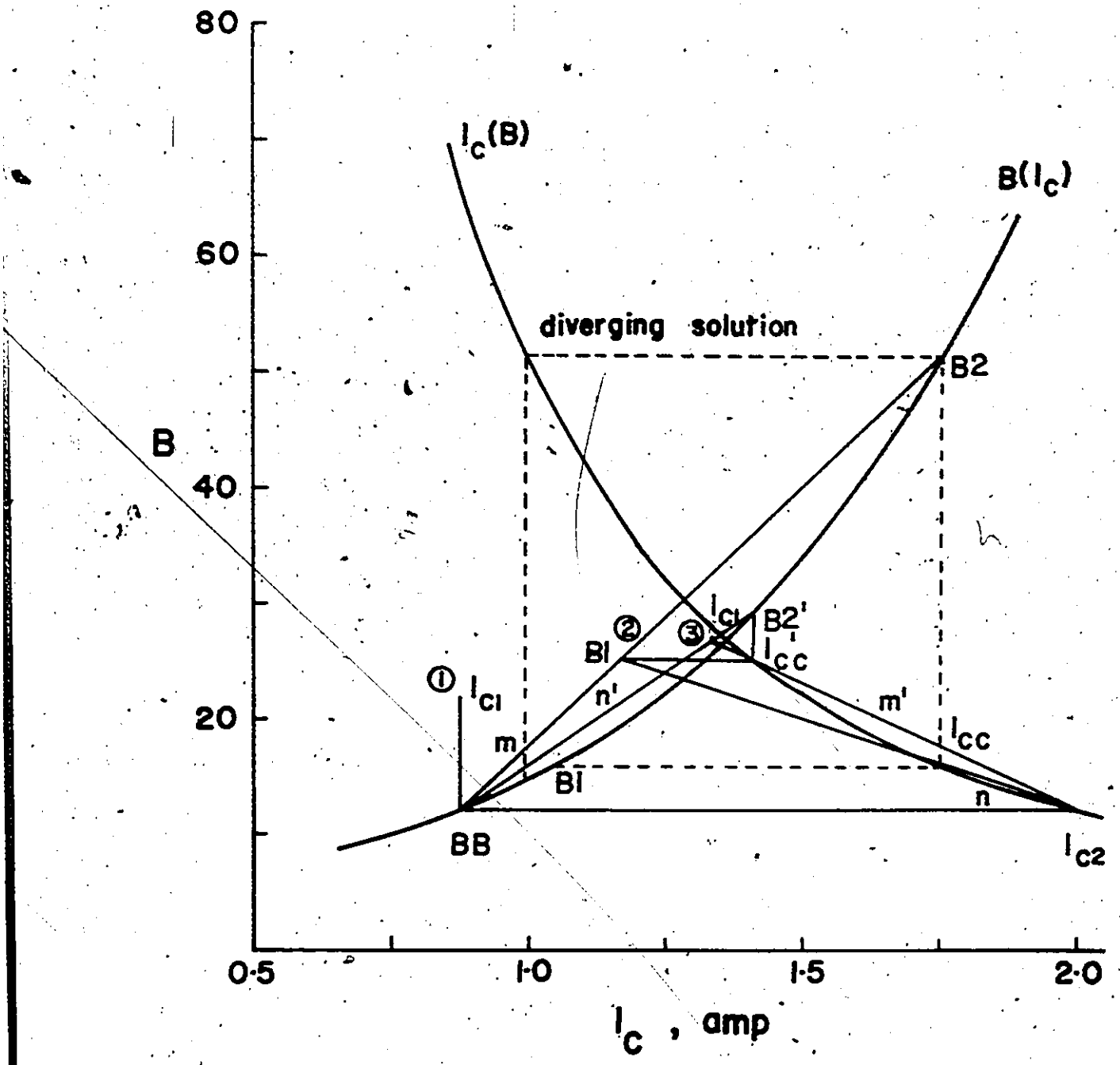


Fig. A2-1 Converging scheme for ICM equations.

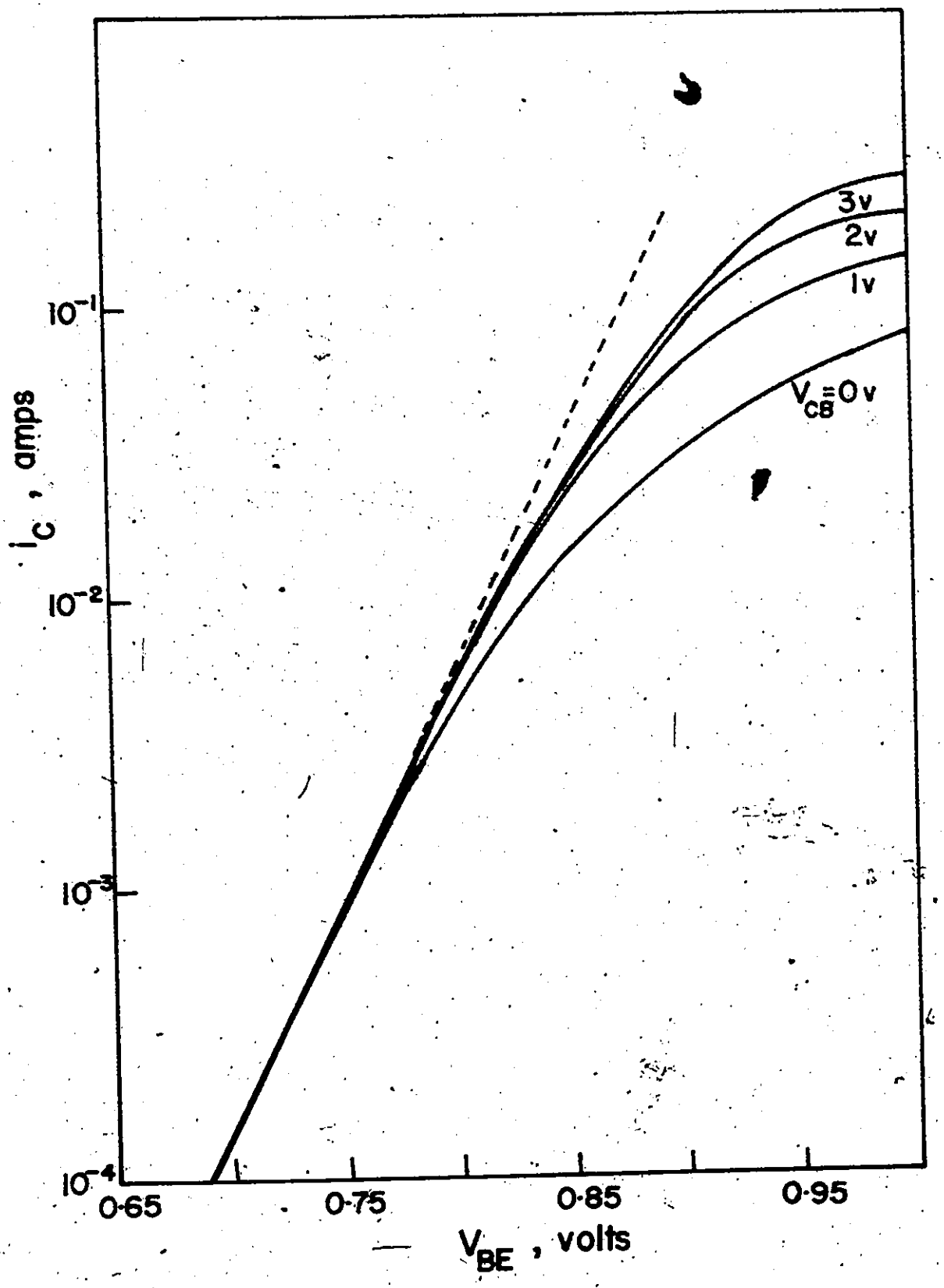


Fig. A2. 2 Transfer characteristics of the BFY90 transistor using the converging scheme of Fig. A2. 1.

Table A2-1 Estimated ICM parameters for a BFY90 transistor

L_k	-2.8E-2
v_k	31.53
τ_f	1.58E-10
r_T	10.0
i_1	2.1E-4
i_2	9.0E-3
i_3	1.E-4
n_E	1.7
n_C	1.5
r_p	4.0
v_{rp}	17.0
r_w	8.2
n_p	3.0
$\frac{kT}{q}$	-0.026
P_{e1}	27.0
P_{e2}	0.2
P_{e3}	0.419
P_{e4}	3.0E-3
P_{c1}	27.0
P_{c2}	0.15
P_{c3}	2.84E-2
P_{c4}	1.0E-3

APPENDIX III

Damped Converging Scheme for Exponential Functions

In this appendix a damped scheme to achieve convergence of the solution in the case of exponential functions [48] is described. In the NANSIM subroutine for bipolar transistors [Appendix IV], the input quantities are the voltage of each node and the outputs are the terminal currents calculated for the model. As shown in Fig. A3-1 if the initial voltage is V_1, then the current is given by

$$I_1 = I_s \left[e^{\frac{q V_1}{k T}} - 1 \right] \qquad (A3-1)$$

In the second iteration, assume that the voltage is V_2. As can be seen from Fig.A3-1,if the current is calculated using equation (A3-1) for V_2, it will give an unrealistically large value for I and may lead to overflow. So, as shown in Fig.A3-1, instead of V_2, I_2 is predicted from the current solution, i.e.

$$I_2 = I_1 + g (V_2 - V_1) \qquad (A3-2)$$

where g is the slope of the characteristic at $V = V_1$

Using (1), we obtain,

$$V_N = \frac{kT}{q} \log \left(\frac{I_2}{I_s} + 1 \right) \qquad (A3-3)$$

This value of V_N is used instead of V_2 for the next iteration.

This scheme may not be required every time but only when the voltage of the next iterate is greater than the previous one. If the voltage is less than the previous value then the iteration is done on the voltage using eqn. (A3-1) .

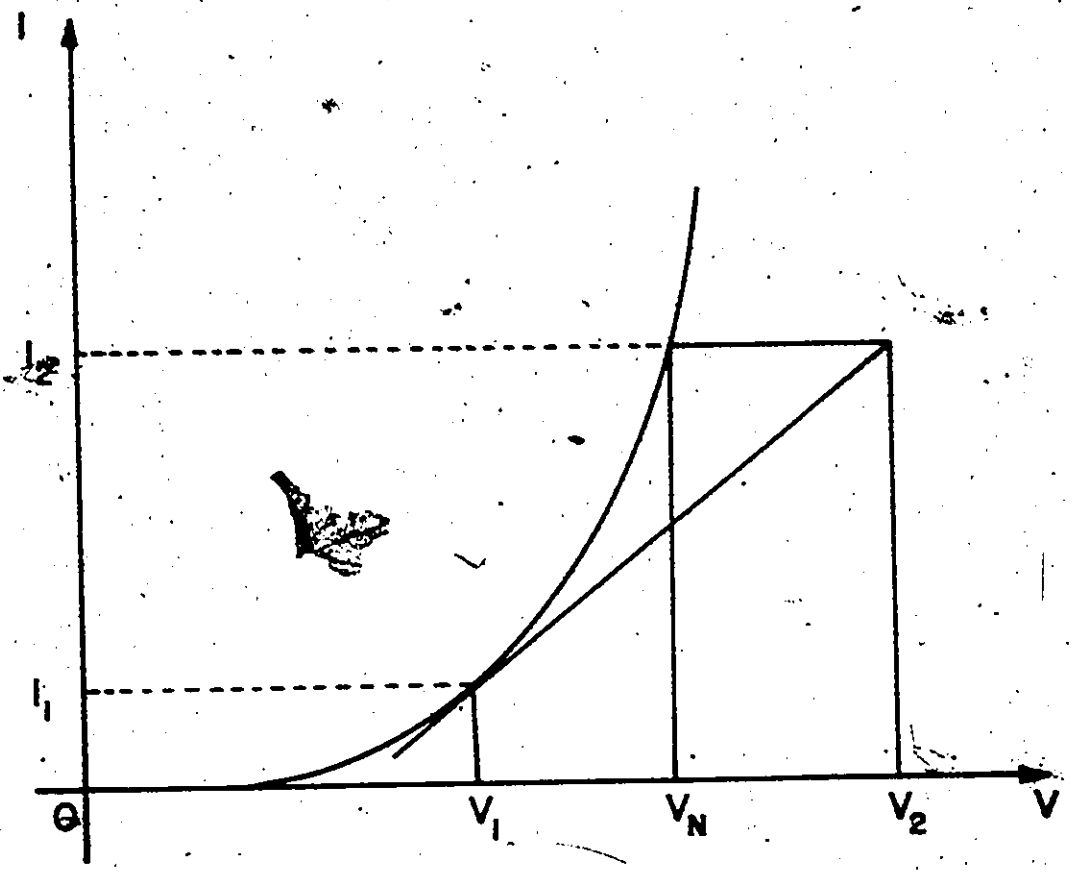


Fig. A3-1 Damped converging scheme for exponential functions.

APPENDIX IV

Subroutine For The Proposed Bipolar Transistor Model

```
      SUBROUTINE BJT
C     MODIFIED TRANSISTOR MODEL
C     TRIPLE LINE INPUT PARAMETERS
      IMPLICIT REAL*8(A-H,O-Z)
      COMMON /ELEM/VALUE(10),VOLT(4),PNV(4),PCUR(4),FREQ,DEFVAL,DELTAT
     3,TYPE,LREAD,LSSIG,LDC,LX,XVAL(10),EVOL(4)
      COMPLEX*8 CY(4,4)
      LOGICAL LREAD,LSSIG,LDC,LX
      DIMENSION Y(4,4),V(4),CUR(4),X(10)
C'FRE'
C     COMMON BLOCK 'FRE' CONTAINS THE ARRAYS USED BY THE FREE
C        INPUT SUBPROGRAM 'FREENAM'
      COMMON /FRE/ XIN(40),LET(80),DSI,KONTRL(80),ELTID
      INTEGER*2 LET,KONTRL
      INTEGER DSI,ELTID
C'ENDFRE'
      REAL*8 IN ,II,LEN,IC,IB,IE
      DATA TNPN/'T N P N '/
      DATA X/1E10,1E10,3*0.,1.,1.,1E10,2*0./
      DATA COE/30.9E-12/,PHIE/.65/,ENE/.3894/,CRE/2.7/,COC/11.3E-12/
      DATA PHIC/.6/,ENC/.3545/,CRC/2.5/,TAUF/4.1E-10/,TAUR/4.2E-9/
C
      IF(.NOT.LREAD)GO TO 99
      IF(IR.EQ.1)GOTO 98
      COE=XIN(1)
      PHIE=XIN(2)
      ENE=XIN(3)
      CRE=XIN(4)
      COC=XIN(5)
      PHIC=XIN(6)
      ENC=XIN(7)
      CRC=XIN(8)
      TAUF=XIN(9)
      TAUR=XIN(10)
      IR=1
      RETURN
98    DO 91 K=1,8
91     X(K)=XIN(K)
      IR=2
      RETURN
99     IR=3
      CONTINUE
      IF (LSSIG) GO TO 1
      VEB=VOLT(3)-VOLT(1)
      VCB=VOLT(2)-VOLT(1)
      VCE=VCB-VEB
      VEC=VEB-VCB
      VEB2=PNV(3)-PNV(1)
      VCB2=PNV(2)-PNV(1)
      VEB1=EVOL(2)
      VCB1=-EVOL(1)
C     IF PNP VOLTAGES ARE NEGETIVE
      IF (TYPE.EQ.TNPN)GO TO 122
```

```
      VCB=-VCB
      VEB=-VEB
      VCE=-VCE
      VEC=-VEC
      VEB2=-VEB2
      VCB2=-VCB2
      VEB1=-VEB1
      VCB1=-VCB1
C     INITIALISATION OF BIASING POINT
122     IF(VEB.EQ.VEB2)GO TO 2
      DV=VEB-VEB1
       IF(DV.GE.0.)GO TO 2
      IF(VEB.GE.0.)GO TO 2
      IN=XVAL(7)-XVAL(3)*DV/XVAL(10)+VALUE(3)
      VEB=-DLOG(IN/VALUE(3)+1.)/VALUE(4)
C     CALCULATION OF IN AND II
2     STORE=(-VALUE(4)*VEB)
      IF (STORE.GT.174.) PRINT 100,VEB
100   FORMAT(' HIGH VEB (',G15.6,')ON TRAN')
      IF (STORE.GT.174.)STORE=174.
      IN=VALUE(3)*(DEXP(STORE)-1.)
        IF(VCB.EQ.VCB2)GO TO 20
      DV=VCB-VCB1
       IF(DV.GE.0.)GO TO 20
      IF(VCB.GE.0.)GO TO 20
      II=XVAL(9)-XVAL(5)*DV/XVAL(6)+VALUE(3)
      VCB=-DLOG(II/VALUE(3)+1.)/VALUE(4)
20    STORE=(-VALUE(4)*VCB)
      IF (STORE.GT.174.) PRINT 101,VCB
101   FORMAT(' HIGH VCB(',G15.6,')ON TRAN')
      IF (STORE.GT.174.)STORE=174.
      II=VALUE(3)*(DEXP(STORE)-1.)
C
      A=IN/VALUE(6)+II/X(2)
      AA=1.+4.*A
      LEM=2./(1.+DSQRT(AA))
C
      IF (VEB.GE.0.)GO TO 10
      BN=VALUE(1)*((IN*IN+X(3)*X(3))/(IN*IN+VALUE(7)*VALUE(7)))
     1**(VALUE(8)/2.))
      GO TO 11
10    BN=VALUE(1)
11    IF (VCB.GT.0.)GO TO 12
      IF(II.EQ.0.0)GOTO 12
      BI=VALUE(2)*((II*II+X(4)*X(4))/(II*II+X(5)*X(5)))**(X(6)/2.)
      GO TO 13
12    BI=VALUE(2)
C
13    IF(VCE.LT.0)VCE=0.
      IF(VCE.GT.0)VEC=0.
      XM=1.+DEXP(X(7)*(VCB-X(8)))
      XM1=1.
      A1=LEM*(1.+VCE/VALUE(5))*XM
```

```
      A2=LEM*(1.+1./(LEM*BI)+VEC/X(1))
      IC=A1*IN-A2*II
      IL=-LEM*(1.+VCE/VALUE(5)+1./(LEM*BN))*IN+LEM*(1.+VEC/X(1))*II
      IB=-IC-IL
C     CALCULATIONS OF ADMITTANCES
      AA=(IN*IN+X(3)*X(3))*(IN*IN+VALUE(7)*VALUE(7))
      IF(AA.EQ.0.)GO TO 64
      A=VALUE(8)*IN*IN*(VALUE(7)*VALUE(7)-X(3)*X(3))/AA
      GO TO 65
64    A=0.
65    G1=VALUE(4)*(II+VALUE(3))*(1.-A)/BN+(1.-XM)*(1+VCE/VALUE(5))*IN
     3*VALUE(4)*(LEM-LEM*LEM*LEM*IN/(2.-LEM)*VALUE(6))
      AA=(II*II+X(4)*X(4))*(II*II+X(5)*X(5))
      IF(AA.EQ.0.)GO TO 61
      A=X(6)*II*II*(X(5)*X(5)-X(4)*X(4))/AA
      GO TO 63
61    A=0.
63    G2=VALUE(4)*(II+VALUE(3))*(1.-A)/BI
      G3=VALUE(4)*LEM*(1.+VCE/VALUE(5))*(IN+VALUE(3))*(1.-(LEM*LEM*IN)/(
     4(2.-LEM)*VALUE(6)))*XM
      G4=VALUE(4)*LEM*(1.+VEC/X(1))*(II+VALUE(3))*(1.-(LEM*LEM*II)/((2.-
     1LEM)*X(2)))
C     CALCULATIONS OF CAPACITANCES
      VE=VOLT(1)-VOLT(3)
      VC=VOLT(1)-VOLT(2)
      VOE=PNV(1)-PNV(3)
      VOC=PNV(1)-PNV(2)
      IF(TYPE.EQ.TNPN)GO TO 82
      VE=-VE
      VC=-VC
      VOE=-VOE
      VOC=-VOC
82    B=1./((1.-ENE)*CRE)**(2./ENE)
      A=(VE/PHIE-1.)*(VE/PHIE-1.)
      CTE=COE*(1.+(ENE/(1.-ENE))*B/(A+B))/(A+B)**(ENE/2.)
      BB=1./((1.-ENC)*CRC)**(2./ENC)
      AA=(VC/PHIC-1.)*(VC/PHIC-1.)
      CTC=COC*(1.+(ENC/(1.-ENC))*BB/(AA+BB))/(AA+BB)**(ENC/2.)
C     CALCULATION OF DIFFUSION CAPACITANCES
      CDE=TAUF*G3
      CDC=TAUR*G4
C
      CE=CTE+CDE
      CC=CTC+CDC
      IF(LDC)GO TO 15
      GCE=CE/DELTAT
      GCC=CC/DELTAT
      XIB=GCC*(VC-VOC)+GCE*(VE-VOE)
      XIE=GCE*(VE-VOE)
      XIC=GCC*(VC-VOC)
      IB=IB+XIB
      IC=IC-XIC
      IE=IE-XIE
```

```
      GO TO 36
15    GCE=0.
      GCC=0.
36    CUR(1)=IB
      CUR(2)=IC
      CUR(3)=IE
      V(1)=-VCB
      V(2)=VEB
      V(3)=VOLT(2)-VOLT(1)
      IF (TYPE.EQ.TRUE)GO TO 3
C     FOR PNP CURRENTS ARE NEGETIVES
      DO 4 I=1,3
      CUR(I)=-CUR(I)
4     V(I)=-V(I)
3     VALUE(1)=G1
      VALUE(2)=G2
      VALUE(3)=G3
      VALUE(4)=CE
      VALUE(5)=G4
      VALUE(6)=A2
      VALUE(7)=IN
      VALUE(8)=CC
      VALUE(9)=II
      VALUE(10)=A1
C ADMITTANCE MATRIX PARAMETERS
      Y(1,1)=+G1+G2+GCE+GCC
      Y(1,2)=-G2-GCC
      Y(1,3)=-G1-GCE
      Y(2,1)=-G2-G4+G3-GCC
      Y(2,2)=+G2+G4+GCC
      Y(2,3)=-G3
      Y(3,1)=-G3+G4-G1-GCE
      Y(3,2)=-G4
      Y(3,3)=G3+G1+GCE
      CALL MATFIL(V,CUR,VALUE,Y,CY)
      RETURN
C
1     G1=VALUE(1)
      G2=VALUE(2)
      G3=VALUE(3)
      G4=VALUE(5)
      CE=VALUE(4)
      CC=VALUE(8)
CC    CALCULATION OF DISTORTION
C     IN=VALUE(7)
C     LEM=VALUE(8)
C     CUR(2)=IN*VALUE(10)
C     A2=G3*G3/CUR(2)+G3*VALUE(4)-CUR(2)*VALUE(4)*VALUE(4)
C     A=2.-LEM
C     B=LEM*LEM*LEM
C     AA=LEM*B*(4.-LEM)/(A*A*A)
C     A1=AA*CUR(2)*IN*VALUE(4)*VALUE(4)*IN/(VALUE(6)*VALUE(6))
C     D2=(A2+A1)/(4.*G3)
```

```
C       A3=2.*G3*(A2+A1)/CUR(2)-G3*G3*G3/CUR(2)*CUR(2)
C       AA3=(A2+A1)*VALUE(4)-G3*VALUE(4)*VALUE(4)
C       A4=G3*A4/CUR(2)+2.*A1*VALUE(4)
C       A5=B*[illegible]4.*LEN+2.*LEN*LEN)/A
CC       A6=-B[illegible]LUE(6))
C       A7=CUR(2)*IN*IN*VALUE(4)*A6*A5*VALUE(4)/(VALUE(6)*VALUE(6))
C       D3=(A3+AA3+A4+A7)/(24.*G3)
C       PRINT 202,D2,D3
C202    FORMAT(' D2=',E15.4,3X,'D3=',E15.4)
CC
C     CNTRX(COL,ROW)
      CY(1,1)=DCMPLX(+G1+G2,+FREQ*(CL+CC))
      CY(1,2)=DCMPLX(-G2,-FREQ*CC)
      CY(1,3)=DCMPLX(-G1,-FREQ*CL)
      CY(2,1)=DCMPLX(-G2+G3-G4,-FREQ*CC)
      CY(2,2)=DCMPLX(+G2+G4,FREQ*CC)
      CY(2,3)=DCMPLX(-G3,0.0D0)
      CY(3,1)=DCMPLX(-G3+G4-G1,-FREQ*CL)
      CY(3,2)=DCMPLX(-G4,0.0D0)
      CY(3,3)=DCMPLX(+G1+G3,FREQ*CL)
      CALL MATFIL (V,CUR,VALUE,Y,CY)
      RETURN
      END
```

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