Fabrication of Gold Hyperdoped Silicon Photodetectors

Derrick Wu

Thesis submitted to the

University of Ottawa

In partial fulfilment of the requirements for

The MASc degree in Electrical and Computer Engineering

School of Electrical Engineering and Computer Science

Faculty of Engineering

University of Ottawa

Abstract

Short wave infrared light has multiple applications across the fields of imaging, telecommunications, and defense. Photodetectors for use in this spectrum usually require expensive and rare materials such as InGaAs, Ge, or HgCdTe. By hyperdoping silicon with gold, the optical absorption cutoff wavelength can be extended from 1100 to 2500 nm, allowing silicon to replace these materials, leveraging the robustness, maturity, and know-how of the silicon microfabrication industry. This effect arises due the introduction of an intermediate band within silicon's 1.12 eV bandgap. However, gold hyperdoped silicon is metastable, which must be considered to avoid gold segregation. A process flow for creating silicon-based short wave infrared photodetectors was designed and executed. Three device layouts were designed, named the Teeth, Corner, and Busbar design. The process flow was designed for industrial compatibility, avoiding the use of electron beam lithography and ion implantation of transition metals. Microfabrication work was done at the University of Ottawa's NanoFab, except for ion implantation done commercially and pulsed laser mixing work done at Benet Laboratories in Watervliet, New York. External quantum efficiency and I-V measurements under 1310 nm laser illumination were performed on fabricated devices.

Statement of Originality

Unless otherwise stated, the results and work discussed in this thesis were obtained and performed personally during my MASc research project, under the supervision of Dr. Karin Hinzer and Dr. Jacob Krich. As far as I'm aware, they are original.

The research project is done in collaboration with the US Army's Benet Laboratories. The goal of the project is to design and execute a repeatable process flow for fabricating silicon-based infrared photodetectors using gold hyperdoping, and to subsequently characterize them with EQE and I-V measurements. This project aims to maximize industry compatibility, avoiding the use of serial processing steps when possible.

The SEM images and EDX measurements in figures 2.20 and 2.21 were taken by Dr. Mathieu de Lafontaine, postdoctoral fellow at the SUNLAB. The Simudo simulations in figures 3.3 and 3.4 were done by Dr. Jacob Krich. Finally, the aqua regia solution in figure 2.13 was mixed by Dr. Spyridon Ntais, lab manager at the University of Ottawa's NanoFab.

Acknowledgements

I would like to thank my principal investigator, Dr. Karin Hinzer, as well as my supervisors Dr. Mathieu de Lafontaine and Dr. Jacob Krich for their support and guidance during this project. I will always be grateful for the knowledge and wisdom they have taught me.

I would like to thank lab managers Dr. Spyridon Ntais of the NanoFab and Dr. Paige Wilson of the SUNLAB for the assistance and training that they have provided. I would also like to thank Dr. Pierre Berini for his advice and expertise.

I would like to thank Dr. Jeffrey Warrender from Benét Laboratories for performing the pulsed laser mixing process, as well as for his expertise with hyperdoped silicon.

I would like to thank my parents for their aid and encouragement and my brother, Harry Wu, for his assistance with device characterization. Finally, I would like to thank my girlfriend for all her support.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

PLM: Pulsed Laser Mixing/Melting

SWIR: Short Wave Infrared

EHP: Electron Hole Pair

HF: Hydrofluoric Acid

BOE: Buffered Oxide Etch

LPEG: Liquid Phase Epitaxial Growth

SEM: Scanning Electron Microscope

EDX: Energy Dispersive X-ray Spectroscopy

NA: Numerical Aperture

TLM: Transfer Length Method

RTA/RTP: Rapid Thermal Annealing/Rapid Thermal Processing

PVD: Physical Vapour Deposition

SCCM: Standard cubic centimeter

SRIM: Stopping Ranges of Ions in Matter

Chapter 1 Introduction

Silicon is one of the most useful elements to humanity. It forms the backbone of the electronics industry, it is frequently used to make alloys in the metallurgy industry, and it is present in our everyday lives in the form of concrete and ceramics. This is all for good reason: Silicon is the second most abundant element in the Earth's crust. Generally, it is found mixed with the most abundant element in the Earth's crust, oxygen, as silicon dioxide (SiO_2). It is of no surprise that humanity has dedicated considerable amounts of time and effort to discovering new ways to use silicon and its compounds, from the earliest rock tools to the newest cutting-edge computer chip.

It is unsurprising that silicon finds uses in the modern photonics industry [1]. Silicon based photodetectors are the standard for visible light detection, silicon solar panels are the dominant commercially available photovoltaic technology for terrestrial applications, and finally, most optical fibers are made from silica glass. However, there are things that silicon cannot do. The bandgap of silicon is 1.12 eV [2], which corresponds to a cutoff wavelength of 1100 nm: it is transparent at longer wavelengths. The usual operating spectrum of silicon photodetectors is 400 to 1100 nm. Photodetectors for longer wavelengths require narrow bandgap materials [3]; such as germanium (Ge), indium gallium arsenide (InGaAs), or mercury cadmium telluride (HgCdTe). These materials can be expensive, brittle, or toxic, limiting their applications. On the other hand, silicon is affordable, durable and nontoxic.

The portion of the electromagnetic spectrum from 1000 to 2500 nm is known as the short-wave infrared (SWIR) spectrum. This spectrum has multiple applications across the fields of imaging, telecom, and defense. For example, many things that are opaque to visible light are transparent to SWIR (such as monocrystalline silicon), allowing it to see through barriers that visible light cannot. While there are many applications that would see benefits by incorporating a SWIR detector, the required materials and processing capabilities to produce them are prohibitively expensive. Developing a silicon-based SWIR photodetector has the potential to open several new markets and applications in areas previously limited by economic unfeasibility.

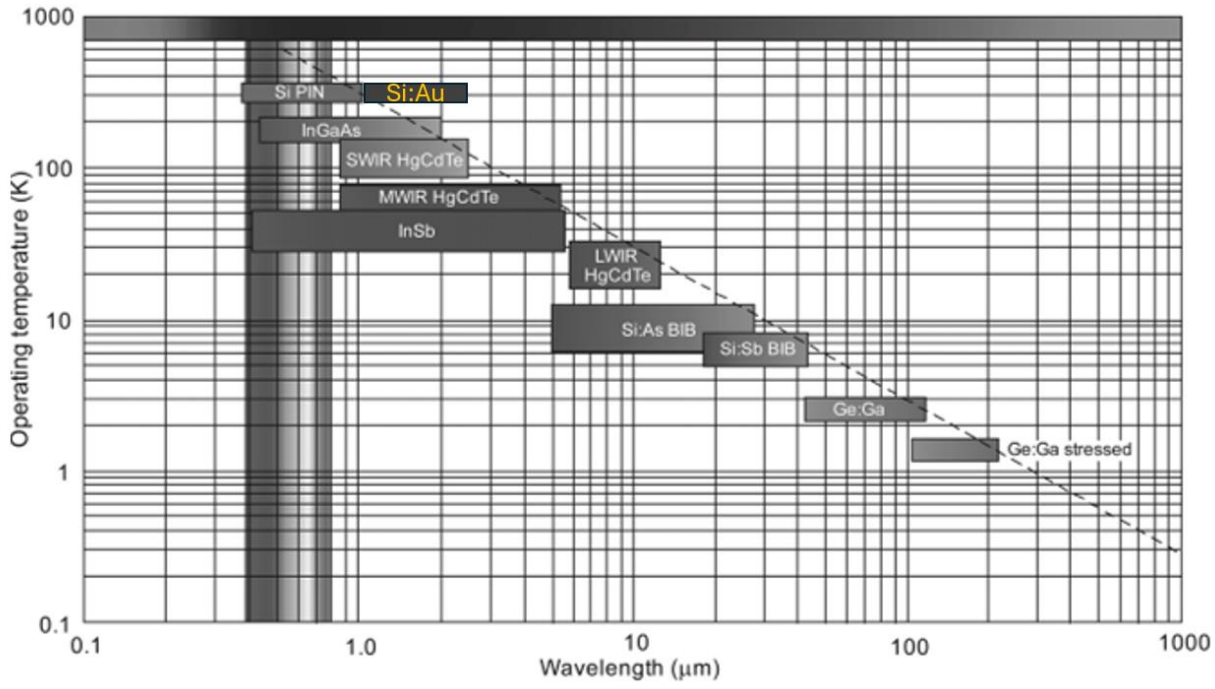

Figure 1.1: Common infrared detector materials by spectral response and operating temperature. As wavelength increases, operating temperature decreases. Adapted from [3].

Note that the operating temperature of infrared detectors gets lower as wavelength increases. This is because photodetectors based on narrow bandgap materials have large amounts of dark current, which overwhelms the desired infrared signal. Cooling the photodetector mitigates this but requires bulky cooling devices or a supply of cryogenic substances such as liquid nitrogen/helium. Infrared photodetectors based on hyperdoped silicon can be operated at room temperature.

Extending the absorption edge of silicon requires shrinking its effective bandgap. One way to do this is by hyperdoping, the process of incorporating dopants far beyond the solid solubility limit. This is generally done using pulsed laser mixing (PLM), a technique similar to laser annealing. Typically, dopants used for hyperdoping come from the transition metals or the chalcogens. These materials would normally be considered contaminants in a standard silicon foundry due to their ability to introduce deep level electronic traps into silicon's bandgap, however, when used for hyperdoping, the electronic traps transform into an intermediate band. This intermediate band enables the two-photon absorption mechanism, effectively extending the absorptive spectrum of silicon into the SWIR. Gold in particular is valued as a hyperdopant element due to its favourable diffusion speeds and segregation coefficient in silicon [4]. Several other elements have been studied as well for hyperdoping silicon.

Table 1.1: Commonly studied elements for hyperdoping.

Hyperdopant	Type	Source
Gold	Transition metal	[4], [5], [6]
Titanium	Transition metal	[6], [7]
Tellurium	Chalcogen	[6], [8], [9]
Sulphur	Chalcogen	[6], [10]
Selenium	Chalcogen	[6], [11]
Nitrogen	Pnictogen	[6], [12]

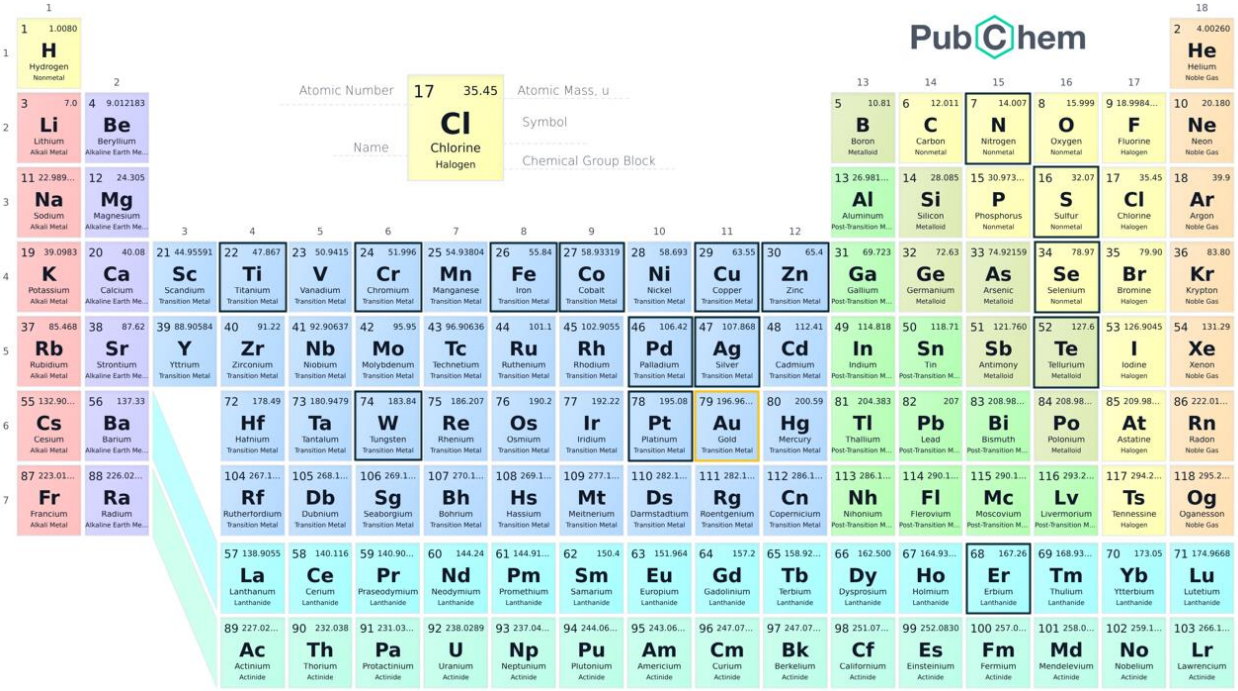

Figure 1.2: Periodic table of the elements, with some of the elements studied for hyperdoping of silicon indicated with a black border. Gold, the hyperdopant of choice for this work, has a gold border. Element lists derived from [4] and [6], figure adapted from [13].

Gold in particular has been extensively studied as a method of carrier lifetime control [14] and is the hyperdopant of choice for this work. Generally, gold is considered an unwanted common contaminant in silicon due to the electron and hole traps it introduces at 0.58 and 0.35 eV above the valence band [15] and its proximity to silicon as a contact metal. The acceptor trap is close to the middle of silicon's bandgap, which allows it to act efficiently as a recombination center. This central trap state is desirable for intermediate band formation, as it extends the absorption edge of silicon effectively. However, gold has low solid solubility in silicon at room temperature, necessitating specialized processes such as pulsed laser mixing (PLM) to achieve optically active concentrations. Furthermore, gold is a potent carrier lifetime killer in silicon: carrier lifetimes in gold hyperdoped silicon are generally shorter than 1 ns [16]. This process comes with its own difficulties and technical considerations, which have been evaluated and accounted for in this work.

The objective of this research is to design and execute a process flow for creating a SWIR photodetector using gold hyperdoped silicon. The process flow emphasizes repeatability, throughput and industry compatibility. For example, previous works for creating hyperdoped silicon devices introduce the hyperdopant to the silicon via ion implantation. However, in an industry setting, transition metals and chalcogens are forbidden elements in the ion implanters due to contamination risks. This work deposits the hyperdopant as a thin film using electron beam evaporation, which is suitable for use in industry. Finally, pulsed lasers are already commonplace in the microfabrication industry [17], which would allow the pulsed laser mixing process to be carried out.

This thesis predominantly focuses on the microfabrication aspects of the process. The process flow designed and performed for this work consists of 5 processes: Alignment mark etching, ion implantation, rear contact deposition and anneal, pulsed laser melting, and top contact deposition and anneal. Figure 1.3 provides a visual summary and a cross section of the device as it is being fabricated.

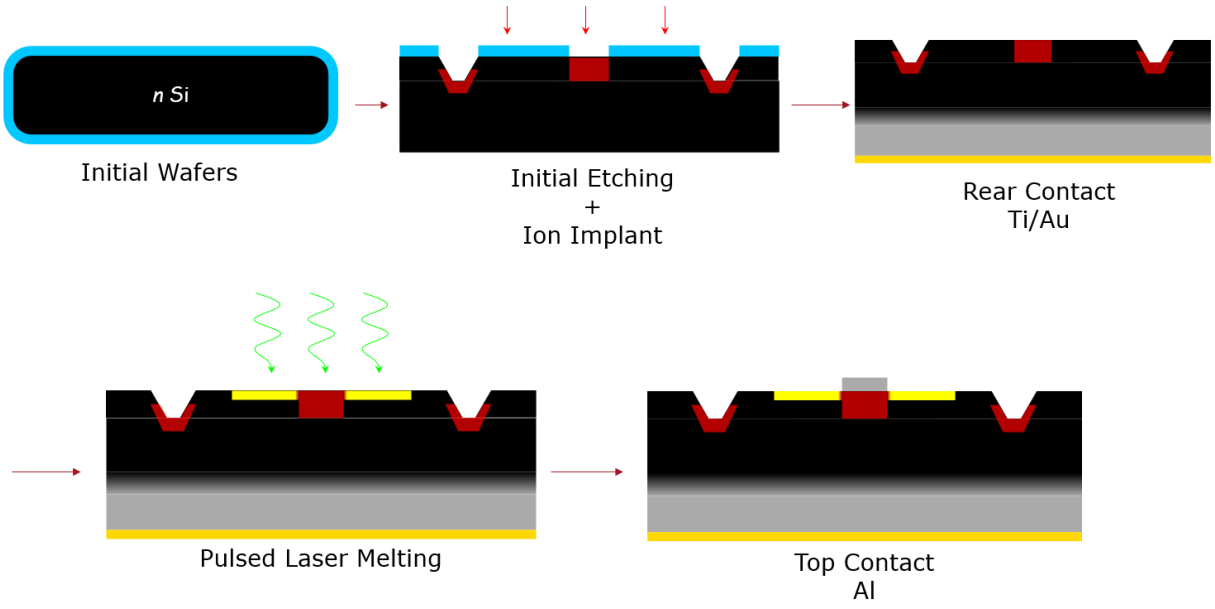

Figure 1.3: Process flow summary used in this work for fabricating gold hyperdoped silicon photodetectors.

Chapter 2 of this thesis will cover background topics necessary for understanding the work in this thesis. This includes the theories of semiconductor electronic behaviour, photodetector devices, PN diodes, deep level traps, Shockley Read Hall recombination (SRH) and intermediate bands. It will also include background information on fabrication processes such as physical vapour deposition (PVD), wet and dry etching chemistries, photolithography, silicon metallization and ohmic contacts, ion implantation and desired shallow state dopant profiles. Validation techniques such as ellipsometry, profilometry,

atomic force microscopy (AFM) and the transfer length method (TLM) will also be discussed.

Chapter 3 outlines the design methodology of the photodetector chip, how layouts were chosen to investigate the effects of dopant mixing and if the short carrier lifetime can be mitigated using interdigitated dopant structures. Substrate doping and ion implantation energy selection will be discussed as well, with the corresponding simulations. Etch chemistries and metallization recipe selection will be discussed.

Chapter 4 details the development of the fabrication process, such as experimental etch rates, mask development and production, ion implantation energy selection, metallization selection, and validation procedures for each process. Process validation results will be shown, such as specific contact resistivity measurements for metallization recipes and experimental etch rates. Photodetector characterization results will be presented as well, such as external quantum in the SWIR spectrum and dark current measurements as well as I-V measurements under 1310 nm laser illumination.

Finally, chapter 5 will conclude this thesis with some discussions as well as avenues for future works.

Chapter 2 Background Information

This chapter will contain background information required for understanding the work in this thesis. Section 2.1 contains background knowledge on the nature of crystalline semiconductors, section 2.2 describes the recombination mechanisms of electron hole pairs, section 2.3 presents the alteration of the electronic bands at PN or metal-semiconductor junctions as well as an introduction to the operation mechanism of photodetectors. These sections combined will provide a background understanding of standard photodetectors. Next, section 2.4 discusses gold hyperdoping and pulsed laser mixing in greater detail, along with the technical considerations required. Section 2.5 discusses microfabrication processes, many of which were used to produce the devices to be discussed in chapter 3. Section 2.6 discusses validation techniques used during the process flow to perform quality assurance after each step during the process flow. Finally, section 2.7 will briefly describe Monte Carlo simulations, which are used to model the ion implantation process used for this work.

2.1 Theory of Solids

As the name implies, a semiconductor is a material that conducts electricity "sometimes." The ability to control this "sometimes" using doping, light or electric potentials is what allows for the creation of semiconductor devices. While this is an oversimplification of how semiconductors operate, it serves as a good starting point for the theory of solids.

2.1.1 Crystalline Materials

Semiconductors are generally composed of monocrystalline materials, that is, materials made up of atoms arranged in structured and repeating lattices [18]. This repeating lattice provides a volume for electrons to roam around, allowing for the modification of the material's electrical conductivity. Crystalline materials exhibit different properties depending on how the lattice is oriented: for example, some crystallographic planes in silicon are known to be more resistant to etching techniques than others. As

wafers, round disks of material used as a starting substrate for microfabrication, are often crystalline, selecting appropriate crystal parameters is an important part of planning a process flow.

Each crystalline material can be characterized by the primitive cell of the lattice, the basic unit whose repetition forms the lattice. The shape of the primitive cell is generally determined by the elements present within the lattice. In silicon, each atom needs to bond to four other silicon atoms, which gives rise to the diamond cubic crystal structure. This crystal structure is shared with other group 14 elements such as germanium and carbon, due to their shared chemical bonding rules.

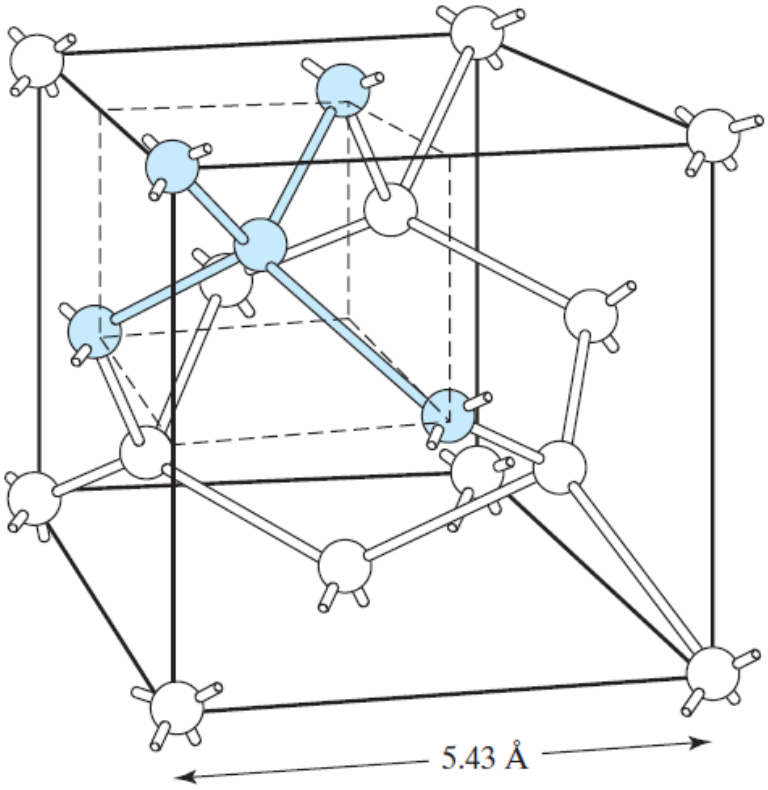

Figure 2.1: Diamond cubic unit cell of silicon. Each silicon atom has four neighbours, and the side length of the cube, or lattice constant, is 5.43 Å, or 0.543nm. Figure taken from [18].

The orientation of lattices are characterized by using Miller indices, a sequence of three numbers that indicate where the crystallographic plane intersects with the

coordinate axes. Each Miller index is the inverse of the intersection point: for example, a Miller index of (x, y, z) means that the plane intersects the coordinate system at 1/x, 1/y and 1/z. Most silicon wafers are cut along either the (100) or (111) planes. Photonic and logical devices are fabricated on (100) wafers, while some MEMS devices are fabricated on (111) wafers. Silicon wafers have wafer flats cut along the (110) plane.

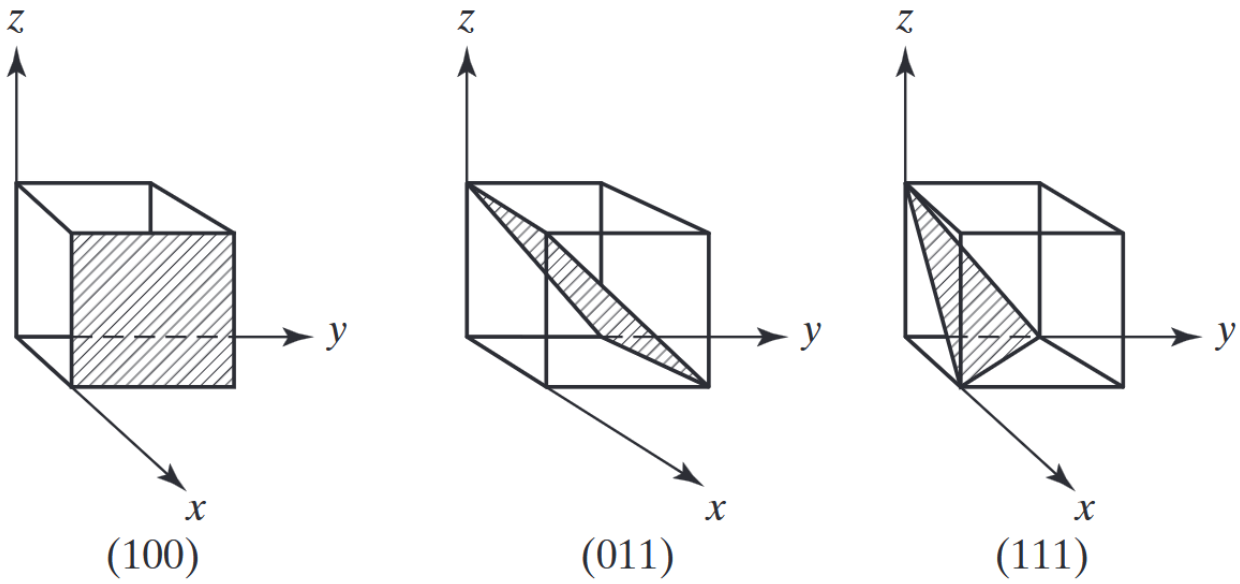

Figure 2.2: Schematic of the most common crystallographic planes for microfabrication purposes. Taken from [2].

2.1.2 Energy Bands in Semiconductors

A distinct property of semiconductors is the clear separation of allowed energy levels for electrons. As many atoms are brought together in a lattice, lower energy electron orbitals merge to form a continuous band of possible electronic states, known as the valence band. At absolute zero, all electrons would be locked within the covalent bonds of the lattice and the valence band would be completely full. As the band is full, electrons would have no adjacent empty electronic states to move to, meaning they cannot contribute to electrical conduction. Thus, at absolute zero, silicon behaves as an insulator.

The same merging happens to the higher energy orbitals, which produces the conduction band. At absolute zero, this band is empty as all electrons occupy lower energy

electronic states in the valence band. As the semiconductor heats up, random thermal vibrations in the lattice have a chance to thermally excite trapped electrons from the valence band to the conduction band. Excited electrons now in the conduction band have multiple available adjacent electronic states, so they are free to move around and thus contribute to electrical conduction. Furthermore, excited electrons leave behind a free electronic state that adjacent electrons can now move to. As valence electrons move to fill this new free electronic state, they leave behind their previous electronic states that other electrons can move to, and so forth. This empty electronic state, known as a "hole," behaves a positively charged quasi-particle that also contributes to electrical conductivity. This combination is known as an electron-hole pair (EHP).

However, a key characteristic of semiconductors is that between the valence and conduction bands, no valid electronic states exist. This feature is known as the bandgap. To excite an electron from the valence to the conduction band, the electron needs to receive sufficient energy to cross the bandgap. The bandgap of a semiconductor depends on the elemental composition of the semiconductor, with heavier elements having smaller bandgaps. In silicon, the bandgap is 1.12 eV (1.8×10^{-19} J).

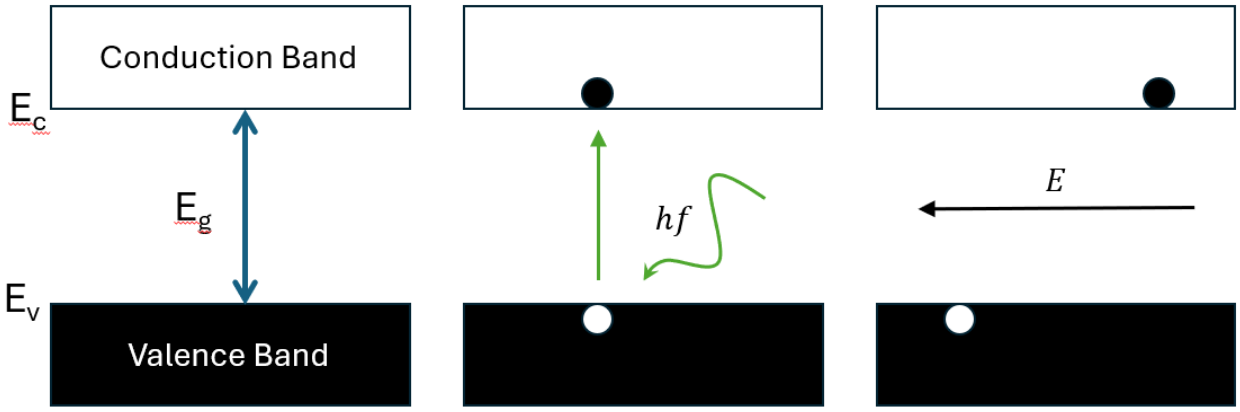

Figure 2.3: Photoexcitation of an EHP. A photon with energy $\boldsymbol{hf > E_g}$ excites an electron from the valence band to the conduction band. In the presence of an electric field, they separate, providing a measurable current.

This is why the electrical conductivity of semiconductors is highly variable. As the population of free charge carriers increases, the conductivity of the bulk semiconductor material increases as well. Carriers can be generated by thermal excitation, meaning that as the conductivity of semiconductors is directly proportional to temperature. This is in opposition to metals, whose conductivity is inversely proportional to temperature. However, charge carriers can be excited by other forms of energy as well. A photon with more energy than the bandgap can create an EHP, causing semiconductors under illumination to have higher conductivities than semiconductors in the dark. This process, known as photoexcitation, is exploited to create light detecting devices such as photodetectors and photoresistors.

2.1.3 Fermi Level

The Fermi level is another important parameter to consider. It is defined as the energy level at which an electronic state has a 50% chance to be occupied at equilibrium if one exists. By extension, at absolute zero no occupied electronic states exist above the Fermi level. This value is material dependent, and comes up in the Fermi-Dirac distribution [13]:

$$f(E) = \frac{1}{e^{E-E_F/kT} + 1}$$

Where *f(E)* is the probability of an electronic state at energy E being occupied, *k* is Boltzmann's constant, *T* is the temperature, and E_F is the Fermi level of the material.

For semiconductors and insulators, the Fermi level is normally at the center of the bandgap, while in metals, the Fermi level exists within the conduction band. As a result, metals have partially filled conduction bands even down to cryogenic temperatures, while semiconductors do not.

The Fermi level is important for describing the shape of the bands when electrically dissimilar materials are brought together. In a material system, the Fermi level must stay continuous throughout the system, which causes the electronic bands to bend at material

junctions. The shape of this bending and the resulting electronic band structure can be used to predict and model the performance of a semiconductor device. This bending even applies to the same bulk material of dissimilar doping types, as P type doping shifts the Fermi level towards the valence band while N type doping shifts towards the conduction band.

2.1.4 Doping

Permanent charge carrier populations can be created by intentionally introducing impurities into the semiconductor lattice, known as doping. In silicon, trivalent elements such as boron or gallium are known as acceptors as they accept an extra electron to form four covalent bonds, integrating themselves into the silicon lattice. Similarly, pentavalent elements such as phosphorus or arsenic are known as donors, as when they integrate themselves into the silicon lattice by forming four covalent bonds, they donate the extra electron. Acceptor and donor elements generate a permanent populations of holes and electrons, respectively.

In the context of energy bands, impurities introduce electronic states into the bandgap. Acceptor/donor elements create states close to the valence/conduction bands respectively and are desired to create a permanent charge carrier population. On the other hand, most elements create states deep within the bandgap and are undesired as the deep states interfere with device performance. As a rule of thumb, shallow states are within $3kT$ of either the valence or conduction bands, where k is Boltzmann's constant and T is the temperature. At room temperature (300K), this is roughly 0.075 eV.

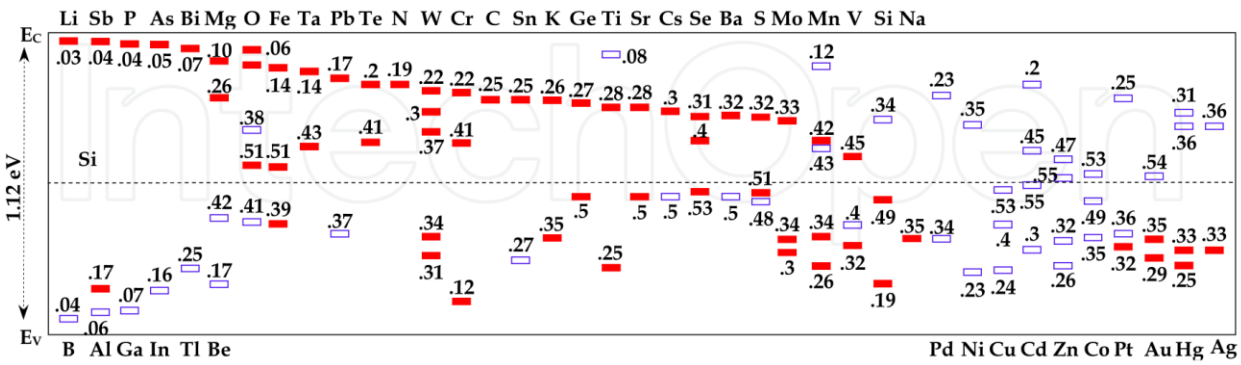

Figure 2.4: Electronic states introduced into the bandgap of silicon by dopant element. Solid rectangles indicate donor states, while empty rectangles indicate acceptor states. Taken from [19].

As standard dopants introduce donor or acceptor states close to the conduction or valence bands, it can be assumed at room temperature that all the states become thermally ionized. This means that the carrier concentration in doped semiconductors is equivalent to the concentration of dopant in the semiconductor. The carrier concentration in the absence of dopant is known as the intrinsic carrier concentration (n_i), which plays a role in determining the equilibrium concentrations of carriers in doped semiconductors. At equilibrium, the carrier concentration of a doped semiconductor follows the equation:

$$np = n_i^2$$

Where n is the free electron concentration and p is the free hole concentration. For silicon, the intrinsic carrier concentration is $n_i = 10^{10} cm^{-3}$[15].

2.1.5 Direct and Indirect Bandgaps

Not all bandgaps are made equal. It is not sufficient for an electron to move to a new electronic state in the conduction band by gaining the difference in energy alone. For a state transition to occur, the crystal momentum of the states needs to match as well. Such semiconductors are known as indirect bandgap semiconductors, meaning that the highest energy state in the valence band and the lowest energy state in the conduction band have different crystal momentums associated with them. As a result, excitation of a valence

electron requires both the energy of the bandgap and the crystal momentum difference be provided. Momentum is generally provided via phonons, a particle of lattice vibration, in a process known as a phonon-assisted transition. Since photoexcitation of valence electrons simultaneously requires energy and momentum, indirect bandgap materials are less efficient at absorbing light and exhibit temperature dependence for their spectral absorptance. Group 14 elemental semiconductors such as diamond, silicon and germanium have indirect bandgaps [20].

On the other hand, some semiconductors have matching crystal momentums between the highest energy state in the valence band and the lowest energy state in the conduction band. This is known as a direct bandgap semiconductor. Direct bandgaps do not require phonons to assist with excitation, so they are much more efficient at absorbing light. Furthermore, direct bandgaps are capable of radiative recombination, an important process that makes light emitting diodes and lasers possible. Direct bandgap semiconductors are often compounds, such as gallium arsenide (GaAs) or mercury cadmium telluride (HgCdTe).

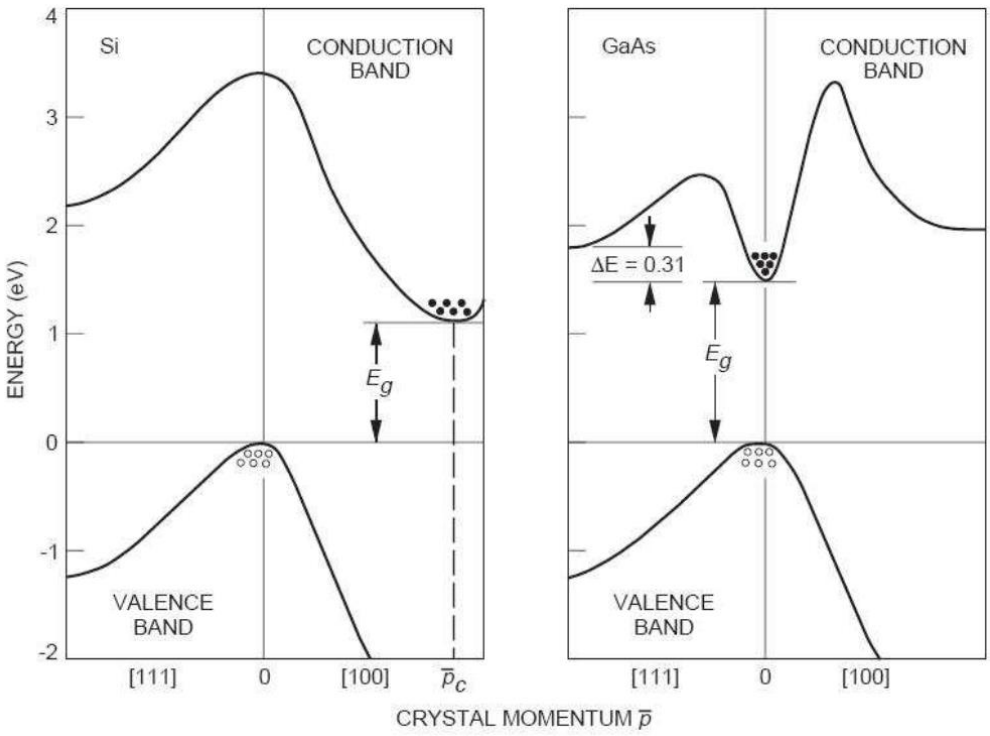

Figure 2.5: Energy – momentum graphs for silicon (indirect) and GaAs (direct). Note how GaAs has the same crystal momentum for the highest and lowest energy levels in the valence and conduction bands, whereas silicon does not. Taken from [21].

2.2 Recombination

Excited electrons cannot stay excited forever. An excited electron in the conduction band can fall into a hole and mutually annihilate, shedding at least as much energy as the bandgap. Recombination is a core parameter of all photonic semiconductor devices. Depending on the device, a fast or slow recombination rate is ideal. Recombination processes fall into two categories: radiative and non-radiative.

2.2.1 Non-radiative Recombination

As the name suggests, non-radiative recombination does not release energy in the form of radiation. This is the dominant form of recombination in indirect semiconductors. Most non-radiative recombination occurs through the Shockley Read Hall (SRH) [22] recombination process, also known as trap-assisted recombination, which uses deep level

states within the bandgap to assist recombination. These deep level states are created by unwanted elements in the substrate (see figure 2.3), necessitating cleanroom environments for the manufacture of semiconductor devices.

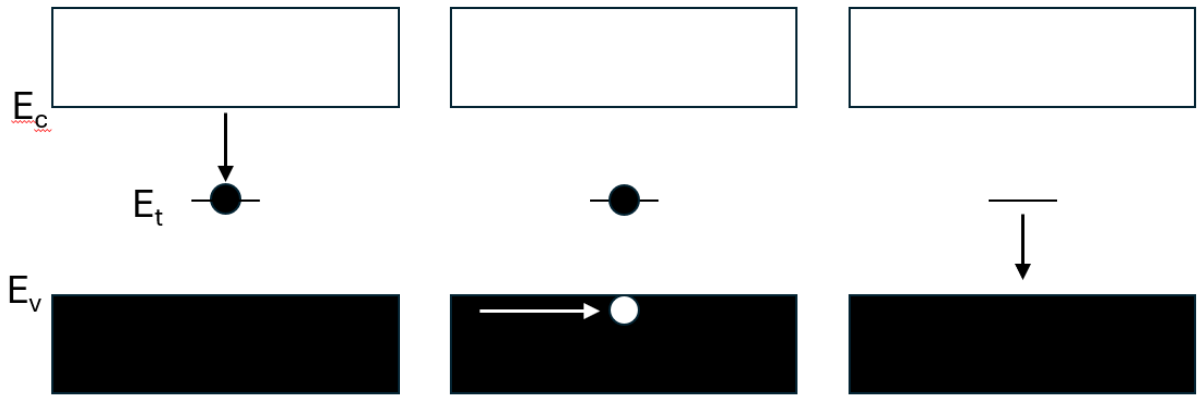

Figure 2.6: Shockley Read Hall, or trap assisted recombination. A trap state captures electrons from the conduction band, rendering them immobile. The trap is subsequently emptied into a nearby hole, completing the recombination process.

In many semiconductor devices, it is desirable to have a long carrier lifetime, meaning that the average time for the minority carrier species to recombine is long. A long carrier lifetime ensures that the average diffusion length is long, so carriers have a higher chance of being extracted from the device. In silicon, this value can be in the milliseconds for very pure samples (highest measured was 32ms) [23] and as impurities increase, goes down to the nanoseconds.

Auger recombination is another form of non-radiative recombination where an excited electron recombines with a hole and sheds the resulting energy to another electron. This electron then sheds the excess energy by colliding with the crystal lattice, releasing phonons and subsequently returning to the bottom of the conduction band. The likelihood of this process depends on the occupancy of the conduction band and is often negligible in most devices.

2.2.2 Radiative Recombination

On the other hand, radiative recombination releases energy in the form of light. When an electron recombines with a hole, it releases a photon carrying away the excess energy. This is the dominant form of recombination in direct bandgap semiconductors and thus makes these materials desirable for devices that emit light, such as light emitting diodes (LEDs) and lasers. As photon energy can be related to wavelength using Planck's law, $E = \frac{hc}{\lambda}$, the peak wavelength of a light emitting semiconductor device is directly related to the size of its bandgap.

2.3 PN Junctions

When P and N type semiconductors are brought together, charge carriers diffuse and recombine at the junction, forming a region that is depleted of charge carriers. This depleted region exhibits a built-in electric field that serves as the basis for many semiconductor devices such as photodetectors, diodes, and photovoltaic cells. As the photodetector in this work uses PN junctions, this section will discuss major aspects of the PN junction.

2.3.1 Device Energy Bands

Although a PN junction may be made of the same bulk material (Ex. Silicon), the doping difference is enough to make the material electrically dissimilar to itself. As nature abhors a discontinuity, the bands bend in a continuous manner over a length, W_0:

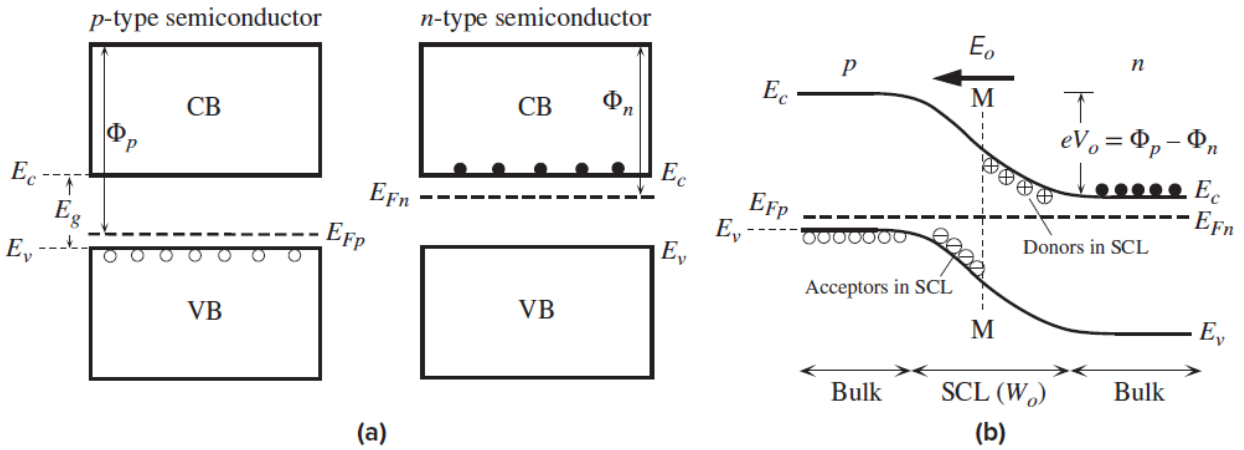

Figure 2.7: Band bending as a p and n-type semiconductor are brought together. (a) shows the bands of doped semiconductors with their shifted Fermi levels, and (b) shows how the bands bend as the doped semiconductors are brought together. Taken from [24].

The shifted bands form an energy barrier at the junction, determined by the difference in the shifted Fermi levels. The total potential of this field is known as the built-in voltage and depends on the bulk material used (silicon has 0.78 V). However, the distance over which this potential extends depends on the doping levels of the bulk material, with lower doping concentrations having a longer depleted region. Thus, the intensity of the electric field increases with higher doping, as the depletion width shrinks. In practice, it is common to strongly dope one side of the PN junction, such that the depletion region extends almost entirely into the other side. The width of the depletion region can be calculated using:

$$W = \left(\frac{2\epsilon(N_a + N_d)V_o}{eN_aN_d}\right)^{\frac{1}{2}}$$

Where W is the width of the depletion region, N_a and N_d are the doping concentrations of the p and n type sides, respectively, V_o is the built-in voltage of the junction, ε is the local electric permittivity, and e is the elementary charge.

2.3.2 Forward and Reverse Bias

By applying electrical potentials from an external source, the band structure of the PN junction can be further manipulated. External biases are often required for the operation of PN junction-based devices.

A forward bias occurs when electrical potential is applied against the built-in voltage, which lowers the potential barrier. This allows carriers to diffuse through the depletion region, resulting in an exponential current [24]:

$$J = J_0(\exp\left(\frac{qV}{kT}\right) - 1)$$

Where J_0 represents the reverse saturation current, a property related to the geometry of the junction. Forwards bias is relevant for diodes, as current can only flow in one direction. This allows for the creation of rectifying devices for the conversion of alternating current to direct current.

The opposite of forward bias is a reverse bias. In this configuration, a voltage is applied with the built-in field, extending the depletion region and the intensity of the electric field. Reverse biased PN junctions are used for photodetectors, where a large depletion region and strong electric field are desirable for absorption of incoming photons. Note that in reverse bias, a small leakage current will still be present, which arises from thermally generated carriers in the depletion region. This reverse leakage current is equivalent to the reverse saturation current.

2.3.3 Photodetectors

Photodetectors are devices built using reverse biased PN junctions designed to absorb light and output current. Using the strong built-in electric field and large depletion region produced by reverse bias, photodetectors absorb photons in the depletion region and the photogenerated carriers are separated by the built-in field. The carriers can then be

harvested at the terminals by an external circuit, producing a current that is directly proportional to the light absorbed in the depletion region.

Firstly, light arrives from an external source to the photosensitive region of the detector. As photodetectors are quantum devices, the light needs to be broken down into photon flux, which can be done using Planck's law [25]:

$$\Phi = \frac{Ihc}{\lambda}$$

Where Φ is the photon flux, *I* is the intensity of the light, *λ* and *c* are the wavelength and speed of light, and *h* is Planck's constant. As this light reaches the surface of the photodetector, some of it will be reflected. Photodetectors often come with antireflective coatings to minimize the effect, but it can be accounted for by multiplying the above equation with (1-Γ), where Γ is the fraction of reflected photons. Next, the internal quantum efficiency is defined as the amount of EHPs generated per photon:

$$\eta_i = \frac{G}{\Phi}$$

Where G is the rate of photogenerated carriers. This value is between 0 and 1 for typical PN photodetectors but can be greater than 1 in avalanche photodiodes. Not all of the generated carriers will be extracted from the device however, so an external quantum efficiency can be defined as well:

$$\eta_e = n_{ext}\eta_i$$

Where η_{ext} is the extraction efficiency, or a measure of how many photogenerated carriers inside the device can exit the device. This efficiency is dependent on device geometry, carrier mobilities and lifetime.

However, these parameters are not very intuitive to work with in practice. Lab instruments measure intensity and current, so it easier to use responsivity instead, which can be expressed using the equation:

$$R = \frac{extracted\ current}{optical\ intensity} = \frac{I_{elec}}{I_{opt}}$$

Responsivity can be related back to the external quantum efficiency using the equation:

$$R = \eta_e \frac{\lambda}{hc}$$

2.3.4 Dark Currents

Dark current refers to the current output of a photodetector even in the absence of illumination. This current is related to the reverse saturation current of the diode and arises from thermally generated charge carrier pairs within the photoactive region of the photodetector [25].

$$I_d = I_s[\exp\left(\frac{qV}{\beta kT}\right) - 1]$$

Where I_d is the dark current, I_s is the reverse saturation current of the diode, q is the elementary charge, V is the voltage applied to the photodetector, β is the ideality factor of the junction, k is Boltzmann's constant and T is the temperature.

The reverse saturation current arises from occupied electronic states in the conduction band at equilibrium, which can be calculated from the Fermi-Dirac distribution. It can be shown that a narrower bandgap results in a higher reverse saturation current, which means that dark current is the limiting factor for infrared photodetector designs. For every 10K increase in temperature, the saturation current approximately doubles. Thus, traditional infrared photodetectors are usually cooled to ensure a good signal to noise ratio for the device.

2.4 Hyperdoping and Intermediate Bands

Now that the basics of band theory have been introduced, hyperdoping and intermediate bands can be discussed in further detail. Recall that the valence and

conduction bands arise due to the interaction of bonding and antibonding orbitals in a densely packed crystalline solid. Each silicon atom forms four covalent bonds, and each of these bonds contributes four electronic states, but only two electrons. Electrons naturally seek the lowest energy state resulting causing the lower energy states to be completely occupied and the higher energy states to be completely empty in the absence of excitation. Thus, it can be said that the bandgap of silicon arises due to the tight packing of identical Si-Si bonds, where the bandgap energy is the energy needed to release an electron from a covalent bond.

Now, if other elements are added to the lattice, new states at different energies now exist. The best candidates are elements which have the same external electron shells as silicon (sp^3) but differ by one electron. For example, boron is said to introduce an acceptor state 0.04 eV above the valence (refer to figure 2.3). For this to be valid, boron must be substitutionally integrated into the silicon lattice, meaning that it replaces a silicon atom within the lattice. This also means it needs to make four covalent bonds to its neighbours. However, boron only has three bonding electrons available. The 0.04 eV value is the energy required for a nearby electron to escape its own bond and fill the available state in the B-Si bond.

Furthermore, an energy band is just many densely packed energy states, which themselves are made by covalent bonds. Thus, if the lattice of silicon were packed with a large quantity of substitutional foreign elements, an intermediate band within the bandgap would form. This intermediate band could then be exploited for applications previously limited by the large bandgap, such as long wavelength photodetectors.

2.4.1 Solid Solubility Limits

It should come as no surprise that atoms that are not silicon in a silicon lattice stress the lattice. A silicon lattice has a maximum concentration of tolerable foreign element, also known as the solid solubility limit. As impurities are added beyond the limit, the lattice begins to reject impurity atoms, causing them to segregate out of the lattice. These rejected atoms do not contribute to the formation of any intermediate band.

For a high solid solubility, the impurity atom should closely resemble the silicon atom both in size and electronic configuration. Phosphorus, silicon's neighbour on the periodic table, has a very high solid solubility in silicon and is often the n type dopant of choice, and so does boron [26], [27]. Aluminium has a high solubility as well, but the electronic states are incompletely ionized at room temperature [28] and it tends to form alloys with silicon instead [29]. As a result, aluminium is used as a contact material to silicon instead of as a dopant.

Unfortunately, these elements produce states close to either the conduction or valence band, neither of which are useful for intermediate band applications. Transition metals which do introduce useful states for intermediate band formation have low solid solubilities and high diffusion speeds [4], [30], making it impossible to produce crystalline silicon with sufficient concentrations of dopant using standard doping techniques. To produce super-saturated, or hyperdoped, silicon for intermediate band applications, more specialized annealing processes need to be used.

2.4.2 Pulsed Laser Mixing

The pulsed laser mixing (PLM) process is one such way to produce hyperdoped silicon. A nanosecond laser pulse with a specific laser fluence is used to melt silicon with a thin film of the desired dopant. As the liquid solubility of the hyperdopant is much higher than the solid solubility, the dopants quickly diffuse into the liquid silicon [31]. The silicon undergoes liquid phase epitaxy after the laser pulse, causing the dopant to be trapped in the silicon lattice before they have a chance to segregate, forming a super saturated solid solution of crystalline silicon. For this work, melt times were between 32 – 45 ns.

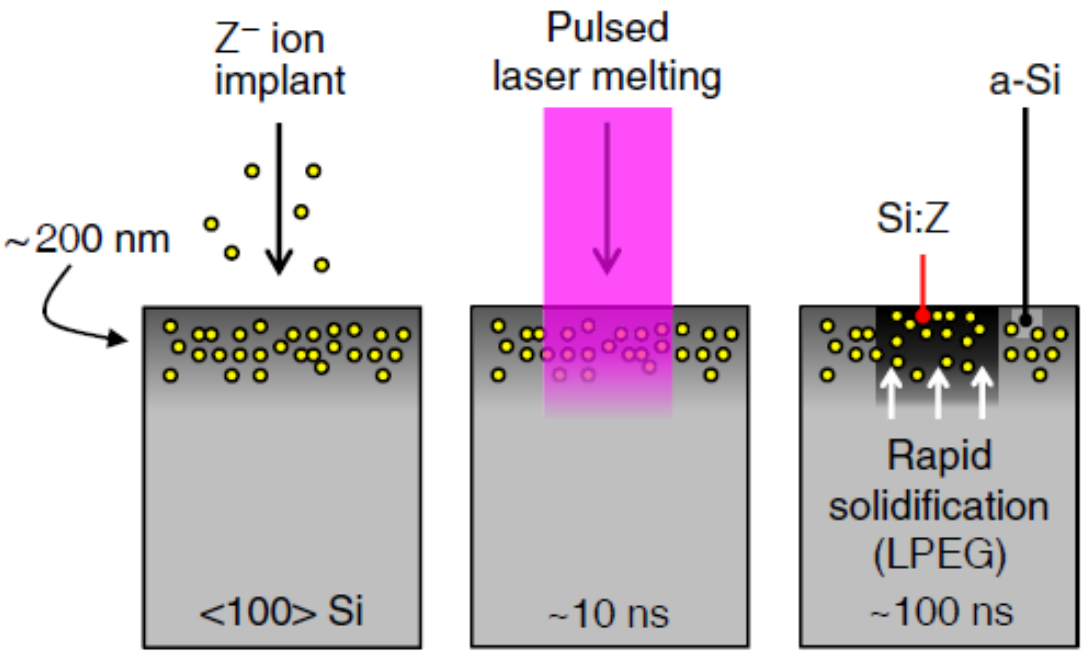

Figure 2.8: Cross section of the pulsed laser melting process. A desired dopant is ion implanted to concentrations above the solubility limit, resulting in an amorphized surface. This is followed by a nanosecond laser pulse, causing liquid phase epitaxial growth. Taken from [32].

Much former work has been done on pulsed laser melting, which first implants the dopant via ion implantation. This work focuses on pulsed laser mixing, where the dopant is first deposited as a thin film and then exposed to the laser pulse. By depositing the dopant as a thin film, the cost of ion implantation can be avoided, especially due to the special requirements of hyperdoping. However, this method does provide a thinner hyperdoped film, which will lower absorption.

2.4.3 Gold Hyperdoping

For this work, gold was selected to be the hyperdopant. Gold has many advantages over elements typically used for hyperdoping. Firstly, the segregation coefficient, which is the ratio between impurities in a liquid and impurities in a solid, is high for gold in silicon. This means that gold readily diffuses in liquid silicon but is trapped by the rapid

resolidification front induced by a laser pulse, allowing for concentrations above the solubility limit, which is under 10^{12} cm^{-3} at room temperature [33]. Next, gold creates an electronic state close to the center of the bandgap, making it ideal for extending the spectral absorptance of silicon. Finally, much previous work has been done on gold impurities in silicon, both as a method of carrier lifetime control and as gold is a common contaminant in the electronic industry.

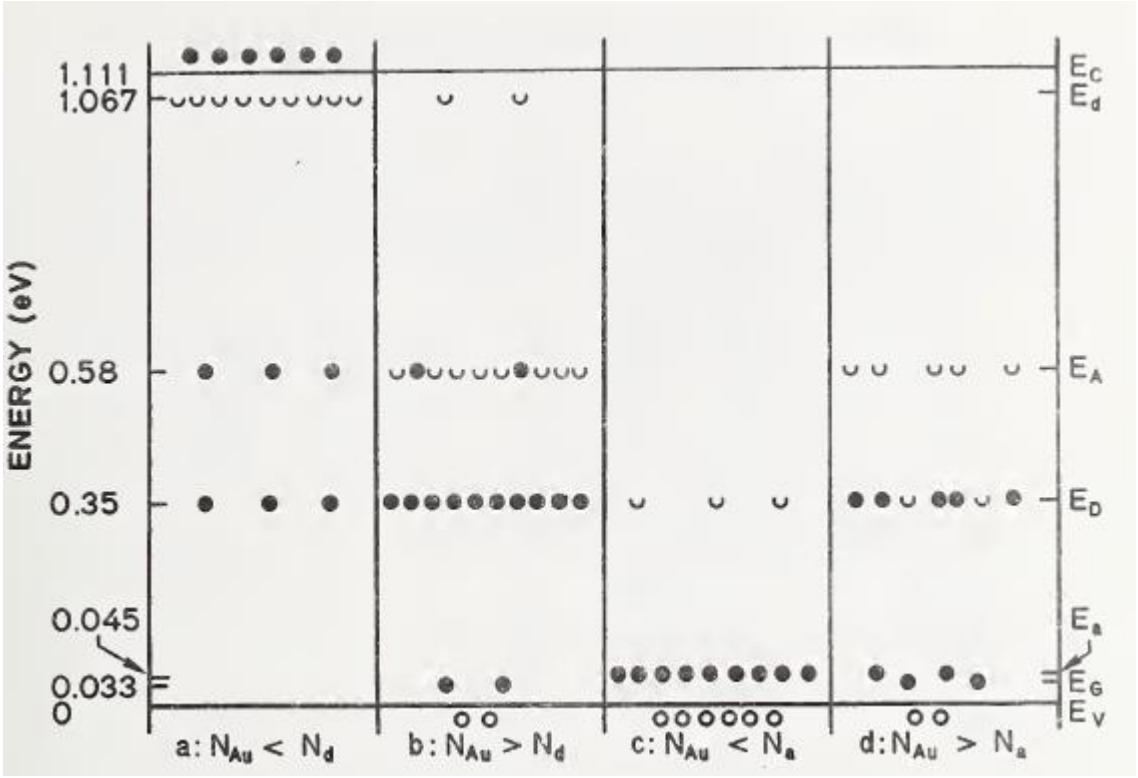

Figure 2.9: Band diagram of silicon with gold impurities, for varying doping concentrations. Taken from [15].

Figure 2.9 illustrates the band diagram of silicon when gold impurities are present, for varying concentrations relative to the background doping. It demonstrates the compensatory nature of gold in silicon: in n-type silicon, the acceptor state traps electrons from the dopant, while in p-type silicon the donor state fills holes in the valence band. It can be inferred that the carrier concentration of gold hyperdoped silicon is similar or lower than that of intrinsic silicon. E_c and E_v are the bottom and top of the conduction and

valence bands, E_A and E_D refer to the energy level of the deep traps introduced by gold and E_a and E_d refer to the energy level of the states introduced by the acceptor or donor dopant (boron or phosphorous). N_d, N_a and N_{Au} refer to the concentration of donor, acceptor or gold species.

Furthermore, gold hyperdoped silicon is metastable. At temperatures above 400 °C gold atoms begin to segregate out of the silicon lattice, rendering them optically inactive [32]. To maintain the integrity of the gold hyperdoped silicon layer, the thermal budget for processes following the pulsed laser mixing step was limited to 350 °C.

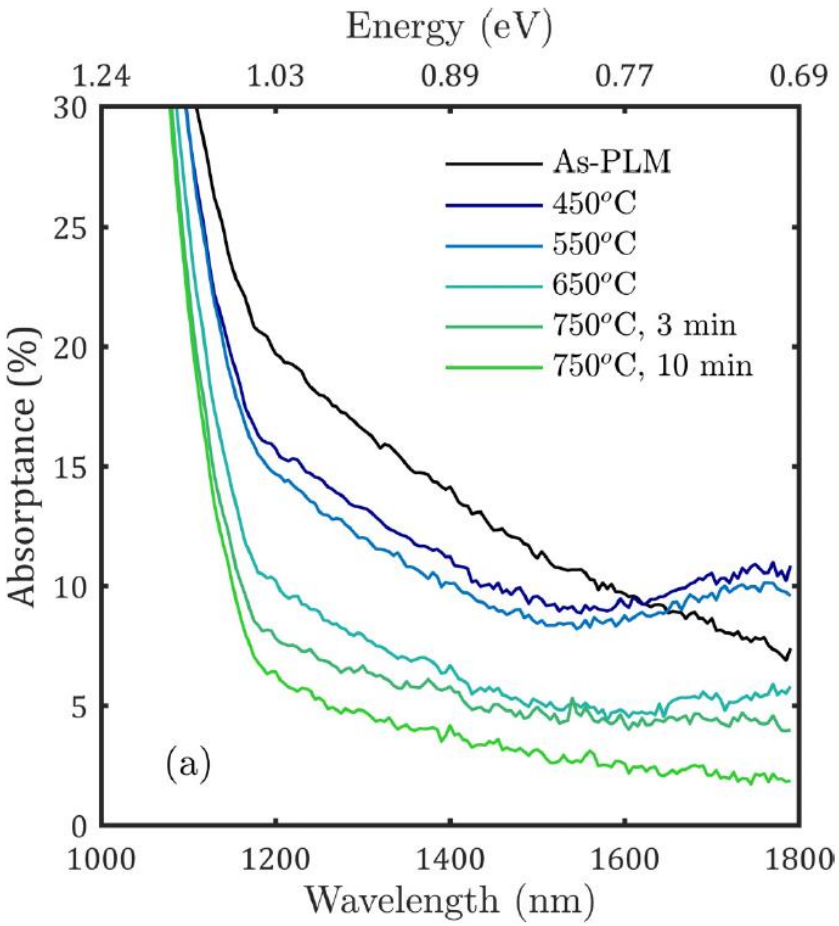

Figure 2.10: SWIR spectral absorptance of gold hyperdoped silicon for varying anneal temperatures. Annealing temperatures above 400 °C reduce the amount of optically active gold. Taken from [32].

The intermediate band in gold hyperdoped silicon affects the energy bands at material interfaces as well. In a pn junction, the intermediate band follows the energy band bending. At a metal-semiconductor junction, the intermediate band interfaces directly with the contact metal's intrinsic electron gas, which results in less energy band bending then would be typically expected of a metal-semiconductor interface [34]. Figure 2.11 illustrates the energy band structure of junctions incorporating gold hyperdoped silicon. The intermediate band is depicted in gold in a) and in red in b).

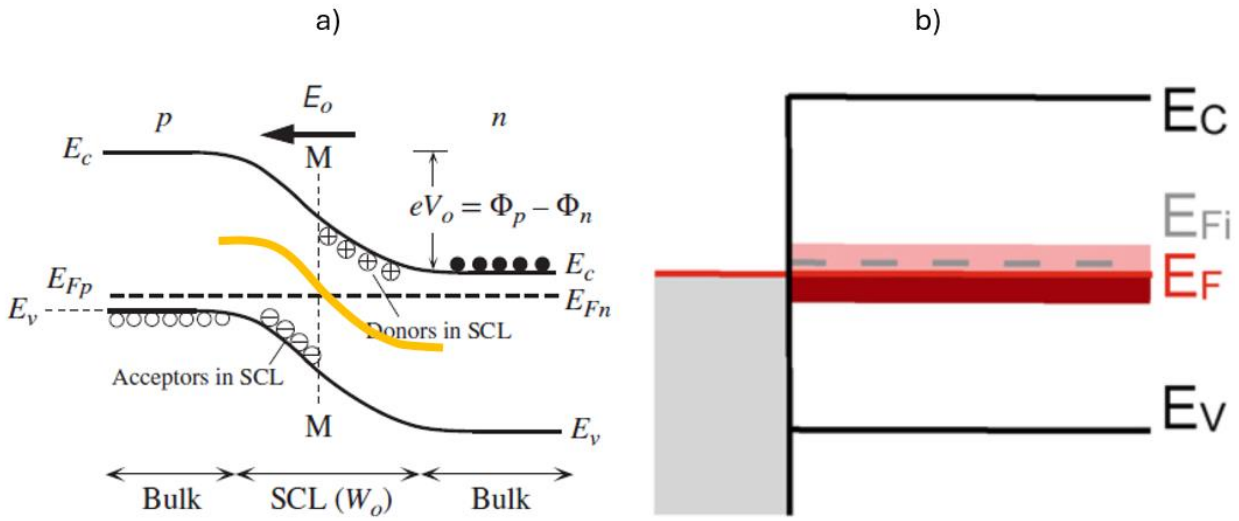

Figure 2.11: a) shows the energy band structure of a pn junction incorporating hyperdoped silicon, while b) shows the energy band structure of gold hyperdoped silicon – metal interface. E_{Fi} denotes the Fermi level of the intermediate band. a) adapted from [24], b) taken from [34]

2.5 Microfabrication

Fabricating devices on the micrometer scale is no small feat. Precision of this level cannot be achieved by the human hand and eye; highly specialized and accurate devices are needed. Furthermore, cleanroom environments and harsh cleaning techniques are required as contamination is a serious threat to microfabrication processes. Finally, all materials used need to be of extreme purity: bulk silicon for microfabrication is often said to be refined to "nine nines" of purity, or 99.9999999% pure. State of the art silicon foundries creating nanometer devices may even require up to "eleven nines" of purity. Even

though microfabrication is an expensive and time-consuming endeavour, the miniaturized devices produced have revolutionized and defined the modern world.

To produce a microscale device at industrial scales, a process flow must be created first. A process flow is a sequence of steps, or processes, that need to be applied to a substrate to create desired devices. The parameters of the substrate need to be carefully selected depending on the end device, such as its material, size, doping, crystal orientation, and more. Most microfabrication substrates are wafers: round, polished disks of extremely pure precursor material [35].

2.5.1 Photolithography

All forms of microfabrication rely on creating patterns in substrates to conduct fabrication processes in specific areas, either additive deposition processes such as Physical Vapour Deposition (PVD) or subtractive etching processes such as wet etching. This is known as lithography. Photolithography, the most common form of lithography used for modern microfabrication processes, uses ultraviolet (UV) light to create patterns on a photosensitive polymer layer, known as the photoresist. By placing the substrate in contact with a mask, it is possible to control which areas of the photoresist are exposed, triggering photochemical reactions that allow for pattern generation by soaking the exposed photoresist in a developer solution. Masks are generally made on a transparent soda-lime glass substrate with an opaque chromium layer containing the pattern. As exposition times are fast (< 5 min) and the entire sample is exposed all at once, photolithography is the industry standard process for creating patterns in photoresist. Photoresists consist of three key components: base resin, solvent, and photoactive compound. They are usually applied to substrates via spin coating: a quantity of photoresist is dispensed onto the substrate, which is subsequently spun at high speeds to create a thin, uniform layer.

Photoactive compounds determine the polarity of the photoresist: positive or negative. In a positive photoresist, exposed areas are removed by developer solution. The photoactive compound, upon exposure to UV light, converts to an acid which is soluble in an alkaline solution. This positive photoactive compound is usually diazonapthoquinine

(DNQ), which inhibits dissolution in alkaline solutions. The corresponding developer solution is an alkaline solution, usually some solution of tetramethylammonium hydroxide (TMAH) at 0.26M or 0.24M concentration.

Negative photoresists are the opposite of positive photoresists: Exposed areas resist dissolution by developer solution. Upon exposure to UV light, the photoactive compound initiates a cross-linking reaction, increasing the molecular weight of the polymer allowing it to resist dissolution by solvents. Accordingly, negative photoresist developers are based on organic solvents such as xylene, butyl acetate, or even acetone. The cross-linked polymer is difficult to remove via conventional means; an issue when it comes to processes further down the process flow. Aggressive organic removers such as piranha solution or oxygen plasma are often required to remove cross linked negative photoresist.

Base resins determine the thermal and mechanical properties of the photoresist film. This resin is usually a Novolak resin based on phenol and formaldehyde. Finally, the solvent determines the viscosity of the photoresist, an important parameter for determining the final film thickness. Thinner films provide better resolutions but may fail to protect the underlying substrate from aggressive processes. Final film thicknesses depend on both the speed of the spin coater and the photoresist viscosity:

$$t \; \alpha \; \sqrt{\frac{\eta}{\omega}}$$

Where t is the film thickness, η is the viscosity of the photoresist, and ω is the spin speed. Photoresist manufacturers generally provide several recommended spin speeds and the resulting film thicknesses for their products.

Lift-off resists such as LOR1A are special photoresists used for the lift-off process. These photoresists lack a photoactive compound, are used as the lower layer in a photoresist stack and readily dissolve in developer solution. This allows them to form undercuts by exploiting the isotropic nature of the developer solution, which is paired with

an anisotropic deposition process to separate desired deposited material from the undesired. As they lack a photoactive compound, they are unaffected by exposition to UV light. Lift-off processes are common in research settings, while industrial settings use dedicated plasma etchers instead.

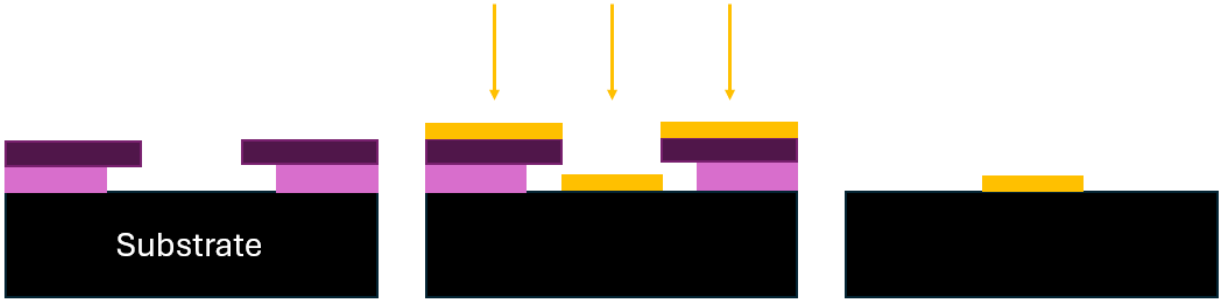

Figure 2.12: Lift off process. A lift-off resist and photoresist bilayer are used to pattern an anisotropic deposition process. The undercut separates masked and unmasked areas.

After a photoresist has been spun onto a substrate, it is then exposed to UV light to initiate the photoreaction. Recommended optical dosages are provided by the manufacturer and vary depending on resist thicknesses and the photoactive compound, although this value is around 100 mJ/cm^2 for DNQ based photoresists. Light passing through the mask is subject to Fresnel diffraction, which limits the linewidth and can be approximated using [35]:

$$l \approx \sqrt{\lambda\left(g + \frac{d}{2}\right)}$$

Where l is the minimum resolvable linewidth, λ is the wavelength of light, g is the gap between the mask and the substrate, and *d* is the thickness of the photoresist. Reducing *l* is done by reducing *d* (using a less viscous photoresist) or using a UV source with a shorter wavelength.

Currently, there are three major UV sources in use. The first is the economical mercury vapour lamp, which has spectral peaks at 365, 404.7, and 435.8 nm, also known as the I-line, H-line and G-line. As the semiconductor industry progressed, demands for shorter wavelengths brought about excimer laser photolithography, which can output wavelengths as short as 157 nm depending on the gas medium used [36]. This is known as deep UV (DUV) photolithography. Finally, modern state of the art systems use extreme UV (EUV) at 13.5 nm [37], achieved by striking a tin plasma with a pulsed laser. This work uses I-line mercury lamps to perform photolithography.

After a suitable pattern has been made, either an additive or subtractive process is subsequently performed. Additive processes add material to the substrate while subtractive processes remove material.

2.5.2 Wet Etching

Etching is the subtractive process of removing material from desired locations on a substrate. In the semiconductor industry, two types exist: wet and dry etching. Wet etching is done using reactive aqueous solutions that chemically react with the target material. The reaction product dissolves in the solution, allowing material underneath to continue reacting.

Etches are characterized by their selectivity, which is defined as the ratio between the amount of target material etched and the amount of masking material etched:

$$S = \frac{target\ etched}{mask\ etched}$$

Ideally, etch selectivity is infinite, meaning that the masking material is completely unaffected. This is possible for several wet etches, but rarely for dry etches. For instance, acetone is considered to have an infinite selectivity between photoresist and silicon. Lower etch selectivities require either thicker masks or harder masking materials. However, thicker masks have lower resolutions and harder masks can be difficult to remove post etch and may require more challenging deposition techniques.

Wet etching is the oldest and perhaps most obvious form of etching available: dip whatever is to be removed in a reactive solution. There is much more nuance to the process, however. The etchant, or the fluid doing the etching, must be carefully selected depending on the target material. Furthermore, as a chemical process, the etching rate is highly dependent on the local conditions, such as the temperature, concentration and stirring methods. Since most wet etching recipes are isotropic, or non-directional processes, the etchant will etch sideways at the same rate as down. It is thus important to calibrate the wet etch to use only the necessary amount of time, as any excessive time results in pattern sidewalls being etched away.

A common wet etching process is the use of hydrofluoric acid (HF) to strip oxides [35]. Fluorine is the only element with a higher electronegativity than oxygen, allowing it to remove most forms of oxide, including silicon's native oxide. This is a naturally forming layer of SiO_2 due to the oxygen in atmosphere and is 3 – 5 nm thick. Its presence interferes with metallization processes, thus it is necessary to remove it. The reaction between HF and silicon oxide is:

$$6\,HF + SiO_2 \rightarrow H_2SiF_6 + 2\,H_2O$$

This reaction produces fluorosilicate acid, which dissociates further to release volatile silicon tetrafluoride and regenerate two molecules of HF. This reaction consumes four fluorine atoms per silicon atom, causing the concentration of HF to drop quickly. To remedy this issue, HF solutions for etching SiO_2 are buffered with ammonium fluoride. The full solution is referred to as buffered oxide etch (BOE) and is commonly found in either as 61 or 10:1 formulations, representing the ratio of ammonium fluoride stock solution to HF stock solution. This etching recipe has an infinite selectivity between silicon oxide and silicon: once the etch reaches the silicon substrate, it hydrogenates the silicon surface and self terminates. The resulting hydrogenated silicon surface is hydrophobic, allowing it to be quickly distinguished from a hydrophilic oxidized silicon surface.

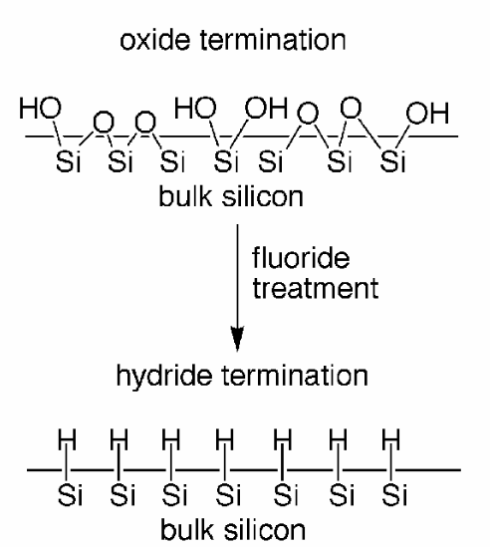

Figure 2.13: Silicon surface before and after hydrofluoric acid cleaning. The hydrogen terminated silicon surface prevents further etching and is hydrophobic. Taken from [38].

A couple more common wet etchants used in silicon microfabrication are piranha solution and aqua regia. Piranha solution is usually a 3:1 mix of sulphuric acid to hydrogen peroxide, and is a powerful oxidizer used to remove organic contaminants. Aqua regia is a 3:1 mix of hydrochloric acid to nitric acid and is used to remove metal contaminants, including gold. Both are fuming, hazardous and corrosive solutions that need to be prepared immediately before use and are generally used as a last resort when less aggressive cleaning processes fail.

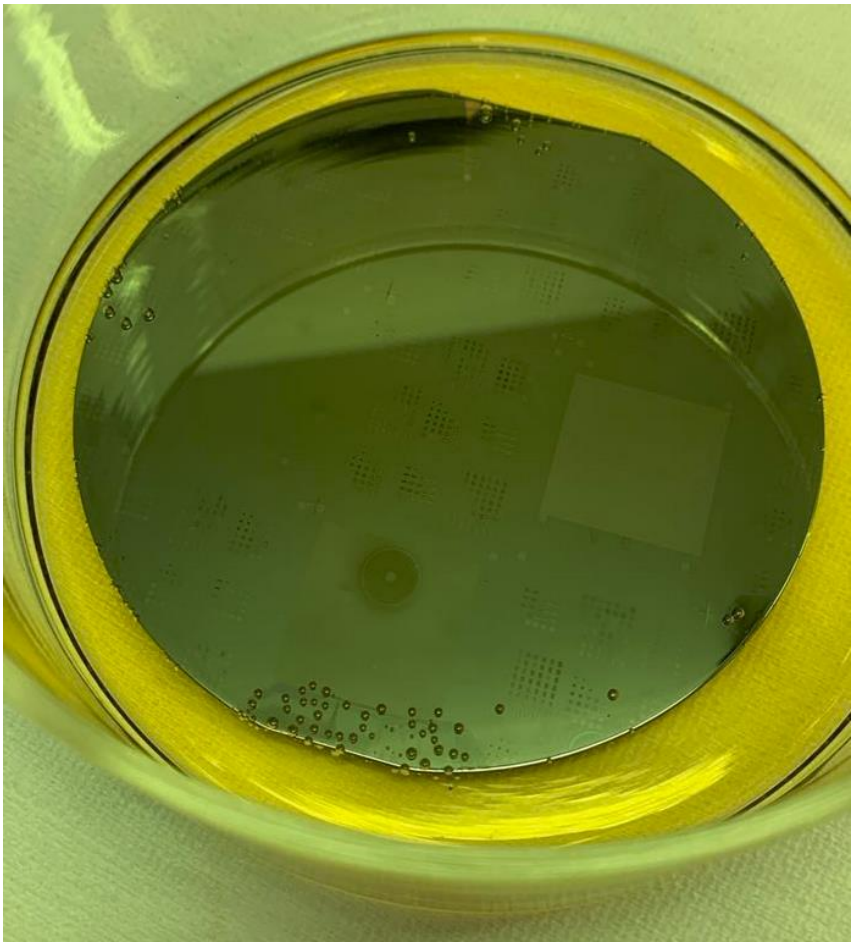

Figure 2.14: Aqua regia solution for dissolving metals. The gold colour indicates the formation of nitrosyl chloride (NOCl), which is the source of aqua regia's signature reactivity. Solution prepared by Spyridon Ntais, personal communications.

Not all wet etching processes are isotropic. For example, strong alkaline solutions such as potassium hydroxide (KOH) preferentially etches the (100) and (110) planes in silicon two orders of magnitude faster than the (111) plane. This causes the shape of the etch to resemble a trapezoidal prism, with side wall angles at 54.7° from the surface. This is the angle between the (100) and (111) planes. Heated KOH etches are often used for producing micro electrical mechanical systems (MEMS), which make use of the trapezoidal cavity for membranes and cantilevers.

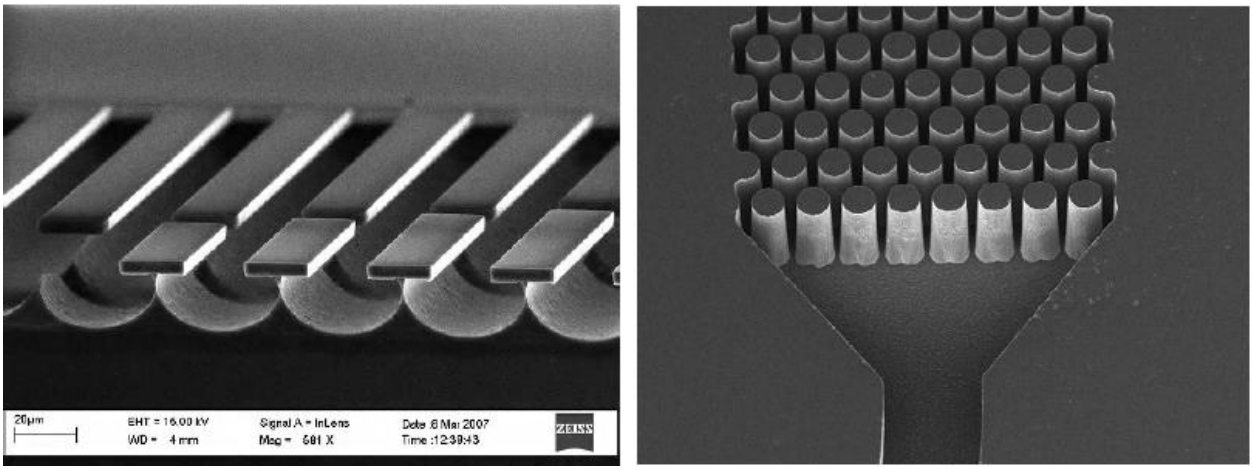

Figure 2.15: Isotropic etch (left) and anisotropic etch (right). Taken from [35].

This work uses room temperature KOH to create alignment marks at the start of the process flow. The etching reaction is:

$$Si + 2\,OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{-2} + 2H_2$$

As the reaction gives off hydrogen gas, bubbles forming in the etchant indicate successful etching of silicon.

2.5.3 Dry Etching

Dry etching, or plasma etching, is a comparatively newer process that uses a plasma to etch a target. It is often preferred over wet etching due to the cheaper cost of etchant gases and its anisotropic nature grants better control over small features sizes. However, a plasma etcher has a high upfront cost and requires sources of pressurized gases. Nevertheless, the semiconductor industry is moving towards exclusively using dry etching for commercial process flows.

To sustain a plasma, plasma etchers couple radio frequency (RF) power to a chamber containing the substrate to be etched and an atmosphere of gaseous precursor. The etching process has two parts: a physical etching part due to high energy ion impacts, and a chemical etching part due to high energy electrons. As ions resonate with 400 kHz power and electrons resonate with 13.56 MHz, the exact etching mechanisms can be

controlled by adjusting the power ratio of the frequencies. State of the art plasma etchers go one step further and use two separate sources to couple RF power to the plasma. A coil is placed around the chamber to supply inductively coupled power (ICP) at 13.56 MHz to the electrons, while another source at 400 kHz is placed underneath the sample to accelerate ions towards it [39].

Gaseous precursors for dry etching silicon are often fluorine rich molecules, such as carbon tetrafluoride (CF_4) or sulphur hexafluoride (SF_6), but other halogens such as chlorines or bromines can be used as well. After the RF power dissociates the etchant, the free, highly reactive fluorine atoms form silicon tetrafluoride (SiF_4), a gaseous product which is pumped away. Unlike wet etching with HF, the ion impact is strong enough to free the silicon atom from the lattice, exposing deeper layers for further etching. CF_4 and SF_6 leave behind a carbon or sulphur atom during this reaction, which is solid at room temperature and deposits on the substrate. To avoid this from happening, oxygen is added to the precursor gas mix to act as a "scavenger", forming gaseous CO_2 or SO_2 which can be pumped away.

Oxygen can also be used as a standalone precursor for plasma etching. Oxygen plasma cleaning, or "ashing", can be thought of as the plasma equivalent of a piranha solution clean: removing stubborn organic contaminants. This is quite useful as the second line of cleaning as it is safer and requires less setup than piranha, and for removing cross-linked negative photoresist.

For this work, plasma etching was intended to be used for creating mesa etches, a form of device isolation and passivation. This process is often used for solar cell process flows [40] to electrically isolate components from one another. A mask was made for this work, however due to the lower currents involved and the fragility of gold hyperdoped silicon, it would only be carried out after the first round of measurements if time permitted.

2.5.4 Physical Vapour Deposition

Physical vapour deposition (PVD) is a category of additive processes, meaning it adds material to the substrate. PVD processes eject material from a material source using

ion or electron beams and deposit it as a thin film on top of a substrate. These processes are usually done in vacuums to ensure that the mean free path of ejected atoms is longer than the distance between the source and the substrate. As PVD does not respect the stoichiometry of the source, PVD processes are mainly used to deposit single element thin films. PVD processes are clean and generate high quality films, but deposit material slowly and may require long vacuum pump down times [35].

Electron beam evaporation is the main deposition process used in this work. An electron beam is used to heat up a crucible containing a source material in a vacuum, allowing it to deposit on a sample above. This form of deposition is suitable for most metals such as titanium, gold and aluminium, which were used to produce the metalizations for this work. This process requires high vacuums (~10^{-6} torr) and deposits material at a rate of 0.1 – 0.5 nm/s. Due to the high vacuum, evaporation is an anisotropic deposition method, allowing lift-offs to be done afterwards for creating metallization patterns. Evaporation is popular in research settings where the film quality, cleanliness, and lift-off compatibility are valued and the low throughput rate is not as important.

Sputtering is another PVD process similar to electron beam evaporation but using an argon ion (Ar^+) beam instead of an electron beam. A negative bias is placed under the substrate to accelerate the ions towards the source material, ejecting material to be deposited. As no heating is required and only a low vacuum is needed (~10^{-3} torr), sputtering deposits material much faster (1 – 10 nm/s) than electron beam evaporation and is thus the preferred deposition method in industrial settings, where high throughput is valued. The low vacuum means that sputtering is more isotropic which hinders lift-off processes; this is not an issue in industry where dedicated plasma etchers are available for creating metallization patterns.

2.5.5 Ohmic Contact Formation

For semiconductor devices to be useful, some connection to the external world is needed. This is accomplished by depositing some conductive metal on the surface, which serves as a connection point to other devices. However, care must be taken when selecting

what metals to deposit. Ideally, a metal – semiconductor contact is ohmic, meaning it has linear I-V characteristic. An incorrect selection results in the formation of a Schottky diode instead, which is detrimental to the device.

The Schottky diode arises from the mismatch between a semiconductor and a metal's electronic band structure. In a metal, the valence and conduction bands are merged, and the Fermi level sits within the conduction band. As a result, metals always have mobile electrons – even at absolute zero – which is the origin of their conductivity. For semiconductors, the Fermi level sits within the bandgap and the conduction band is at a more energetic location. Just as in the case of a PN junction, nature abhors a discontinuity: the Fermi levels must match at the contact point, thus the electronic bands bend over some distance, resulting in the formation of an energy barrier.

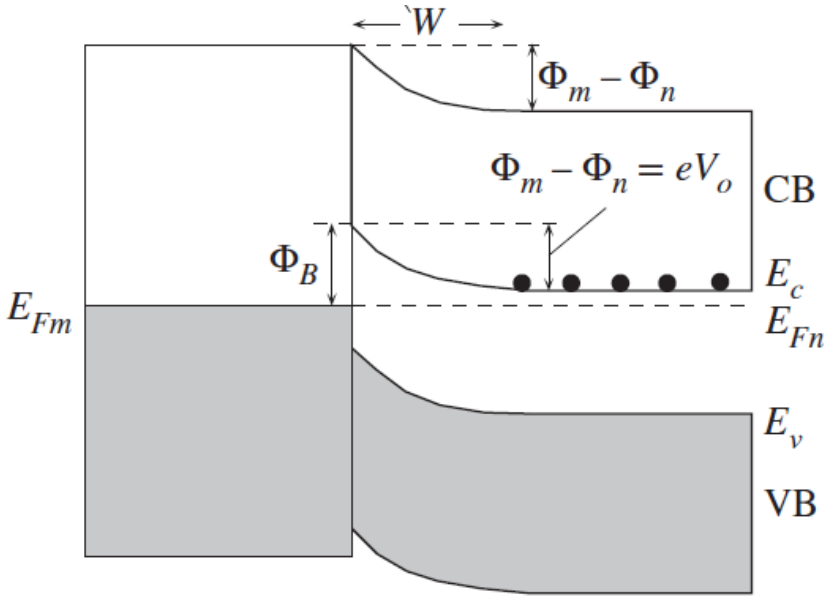

Figure 2.16: Band bending as an n type semiconductor is brought into contact with a metal. Similarly to a PN junction, a region depleted of mobile charge carriers of width W forms at the contact point. Shaded regions indicate filled electronic states. Taken from [24].

The height of the barrier, Φ_B, depends on the difference between the work function Φ_m of the metal and the electron affinity χ of the semiconductor, or the "depth" of the

conduction band. Note that this barrier is present for electrons moving from the metal to the semiconductor: electrons moving from the semiconductor to the metal see a reduced energy barrier by ($E_c - E_{fn}$). While Schottky diodes do have applications which make use of the rectifying properties of the energy barrier, they are also inadvertently created when an incorrect metal is selected for forming an ohmic contact to a semiconductor.

It is worth noting that an ohmic contact still has an energy potential barrier at the contact. No contact is perfectly ohmic, but as long as the potential barrier is small, the contact behaves ohmically for the operating ranges of the device. Furthermore, just as with PN junctions, the depleted region extends spatially into the semiconductor to a distance inversely proportional to the doping concentration. For lower doping concentrations, the width of the barrier is large and the dominant mechanism for traversing it is thermionic emission. This mechanism is inversely proportional to temperature, meaning that the contact resistivity of an ohmic contact decreases as temperature increases. Thus, ohmic contacts to lightly doped semiconductors have higher contact resistivities. Typically, resistivities of 10^{-4} to $10^{-6}\ \Omega\ cm^2$ are considered acceptable for ohmic contacts to lightly doped silicon.

At higher doping concentrations, the width of the barrier becomes small, which allows quantum tunneling to become the dominant transport mechanism. Resistivities in this regime can reach $10^{-9}\ \Omega\ cm^2$ or less, and metals that would make Schottky diodes on lower doping concentrations can now make ohmic contacts. The doping concentration at which quantum tunneling becomes dominant for silicon is roughly at 10^{19} to $10^{20}\ cm^{-3}$ [41].

In practice, the list of metals suitable for making ohmic contacts is quite limited. Titanium is often used on n type silicon due to its excellent adhesion, low Schottky barrier height (0.6 eV) [42], and ability to form a silicide given an appropriate anneal [43]. However, as it is one of the least conductive metals (2.3×10^6 S/m) [44], only a thin layer (~10 nm) is used to form the initial contact which is capped with a more conductive metal, such as copper or gold. For contacts to p type silicon, aluminium is often used. As it comes from the same element group as silicon's p type dopants, it readily forms ohmic contacts to p

type silicon. Comparable results have been found using gallium [45] and indium [46], although the melting point of the former and the price of the latter prevents widespread adoption.

2.5.6 Ion Implantation

Ion implantation is another additive process that is used to add, or implant dopant atoms into the silicon lattice. Dopant atoms are sourced from a plasma and accelerated by an electric field towards a target substrate. By adjusting the strength of the electric field and the dopant dosage, a precise dopant profile can be created within a target substrate. The ion implantation for this work was done commercially.

To prepare an ion implantation process, the implant energy, element, and implant angle need to be selected. Higher implant energies create deeper doped volumes, heavier elements implant shallower, and the ion beam may be tilted at some angle to avoid channeling effects. Notably, the standard implant angle for <100> silicon is 7°. These parameters are selected via Monte Carlo simulators such as the Stopping Range of Ions in Matter (SRIM) [47], which was used in this work to plan the implantation process.

2.5.7: Rapid Thermal Annealing

Rapid thermal annealing (RTA), or rapid thermal processing, is a process that provides excellent control over the temperature of a substrate. This process dates back to the 1990s [48] and has since become the industry standard for thermal processing. By using high powered lamps, samples can be brought to temperatures as high as 1000 °C within seconds and cooled down just as fast, although care needs to be taken to ensure thermal shock does not occur. The atmosphere in the RTA chamber is typically filled with inert gases as well such as nitrogen, argon or forming gas, which is a blend of nitrogen and hydrogen designed to scavenge oxides. Alternatively, an oxygen atmosphere can be used to create dry thermal oxide for silicon.

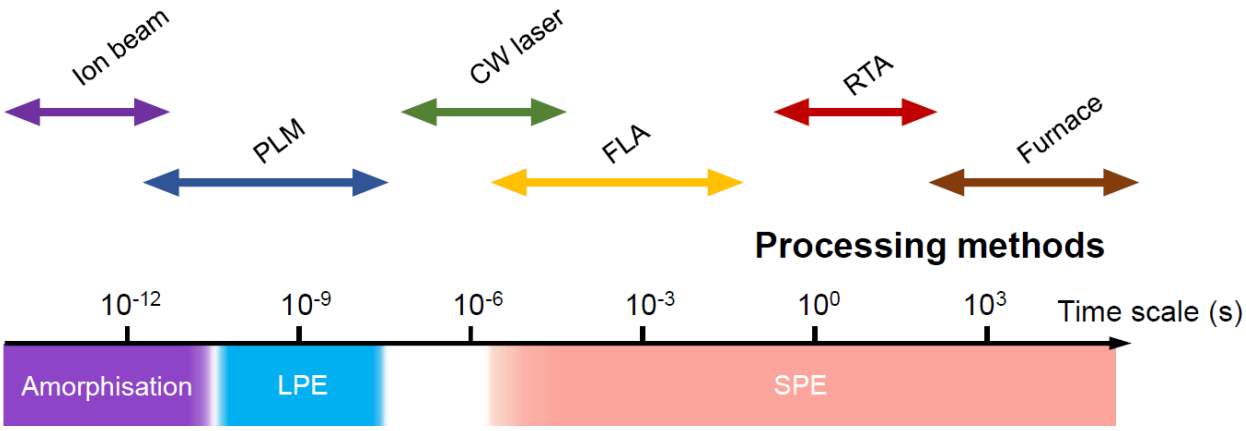

Figure 2.17: Thermal processing techniques by time scale and result. RTA, furnace and flash lamp annealing (FLA) cause solid phase epitaxy (SPE), while the relatively faster PLM causes liquid phase epitaxy (LPE).Taken from [49].

2.6 Validation Techniques

Proper quality assurance is necessary when developing process flows. Given the sizes and complexity of semiconductor physics involved, accurately determining whether a process was successful or not can be just as technically challenging as the process itself. Many process flows incorporate test structures for this reason; structures that are designed to provide information about the process that created them and nothing else.

2.6.1 Ellipsometry

Ellipsometry is a well-known technique for determining the thickness of thin films. When a thin film is struck with monochromatic elliptically polarized light, the reflected light experiences a phase shift depending on the refractive indices of the thin film layers. As refractive indices change depending on the wavelength of light, phase shifts are collected across a spectrum. These spectral phase shifts are then provided to an optical model of the thin film, which is used to calculate the thickness of the film. As ellipsometry measures phase shifts, its accuracy is not bound by the wavelength of light and can precisely measure nanometer thicknesses provided an accurate model exists. For common materials, including silicon oxide, many accurate and reliable models are available.

Interestingly, ellipsometry of silicon oxide can be done with the naked eye. Silicon oxide is known to change colour depending on its thickness, allowing its thickness to be estimated via ocular inspection.

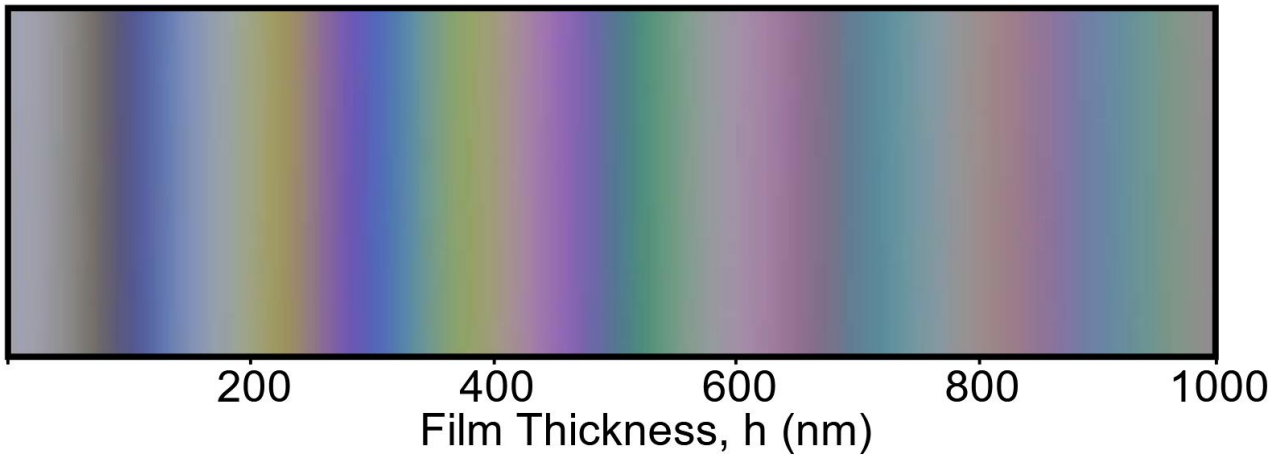

Figure 2.18: Apparent colour of silicon oxide to the naked eye by film thickness. Taken from [50].

2.6.2 Profilometry and Atomic Force Microscopy

Profilometers and atomic force microscopes are both instruments used to measure the profile of a surface. A stylus attached to a cantilever repeatedly taps the surface of the sample at some predetermined contact force while moving in a specified direction. The height of the stylus as it contacts the surface produces an analog signal via a transducer, from which the profile of the sample can be extracted [51]. From the profile, step heights from depositions or etches can be extracted, as well as the surface roughness. As these methods operate by tapping a stylus above the sample, they cannot be used to characterize undercut geometries.

The resolution of a profilometer is limited by the diameter of the stylus tip. It is not possible to accurately measure surface features that are smaller than the stylus tip, so a smaller tip allows for a higher resolution profile. However, smaller tips are more susceptible to wear and tear and more expensive than larger tips. Generally, profilometers

are used for measuring profiles with topographies in the 20 nm to 1 mm range. For higher resolutions, atomic force microscopes will need to be used instead.

Atomic force microscopy operates on a similar principle to profilometry: a stylus on a cantilever is repeatedly tapped at varying points on a surface and measurements taken to acquire a profile. However, instead of measuring the cantilever height via transducer, a laser is aimed at the tip. As the cantilever changes position depending on the surface of the sample, the amount of laser light reflected changes as well, from which the profile of the surface can be extracted. This allows for extremely precise measurements, down to the individual atom [52].

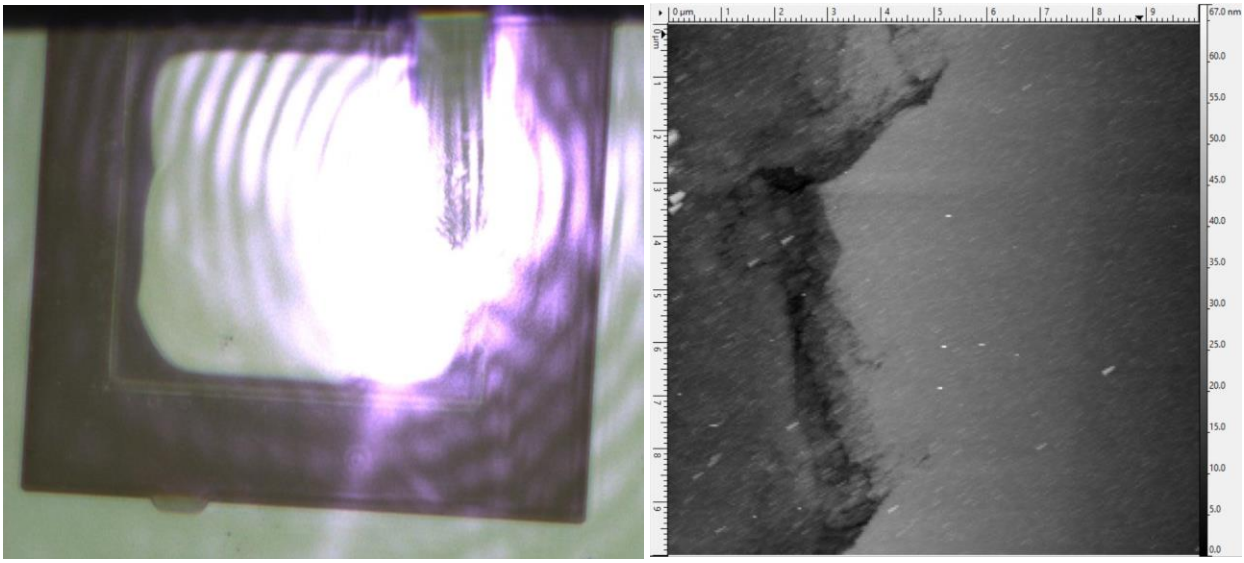

Figure 2.19: Discoloured gold film viewed through an optical microscope mounted on an AFM (left) and the resulting AFM scan (right). Note the laser focused on the AFM tip.

2.6.3 Transfer Length Method

The transfer length method (TLM) is a technique for characterizing the specific contact resistivity of metallizations, requiring specific test structures to be deposited on the substrate. These test structures consist of contact pads separated by predetermined gap. I-V measurements can be taken across each gap and, assuming the contact is ohmic, the resistance extracted. By plotting the extracted resistances against the known gap

lengths and performing a linear regression, the specific contact resistivity of the metallization can be extracted.

Initially, TLM structures were rectangular [53]. However, they have since been deprecated in favour of circular TLM structures due to the current crowding effect [54]. This phenomenon arises due to the fact that most current flows through the edge of the contact film, similarly to the skin effect in wires. As a result, the actual current cross section is not equivalent to the area of the contact pads, which leads to inaccurate measurements for the resistivity. Circular TLM structures can account for this, allowing for more accurate measurements of specific contact resistivity [55].

Figure 2.20: Current crowding effect for planar structures. Despite the fact that the metal contact pad is much larger, most of the current flows through the edge of the contact (highlighted in red).

2.6.4 Scanning Electron Microscopy

Although the optical microscope is an incredibly useful tool, they are inherently limited by the wavelength of visible light. The diffraction limit is defined as [56]:

$$d = \frac{\lambda}{2NA}$$

Where d is the maximum resolution of the microscope, λ is the wavelength of light, and NA is the numerical aperture of the microscope. For a perfect microscope with NA = 1 using green light (λ = 500 nm), the diffraction limit is 250 nm. For smaller resolutions,

shrinking the wavelength is possible, but optical wavelengths shorter than the visible are hazardous to humans and originate from dangerous and power-hungry sources.

Electrons can be used in the place of photons for higher resolution images. As electrons have mass, their wavelength is described by de Broglie's equation:

$$\lambda = \frac{h}{p}$$

An electron accelerated through a 2kV field as a wavelength of roughly 27 pm: less than the radius of an atom. Electron images are generally taken at 15 kV to 25 kV providing even shorter wavelengths, although relativistic effects need to be considered at these energies.

Scanning electron microscopy (SEM) is a common form of electron microscopy. A high energy electron beam is focused onto a sample, which creates secondary electrons due to the energetic collisions. These secondary electrons are subsequently collected by a detector, which allows a pixel to be formed. By rastering the electron beam across some area, an image can be formed. As secondary electrons have relatively low energies compared to the initial beam (< 50 eV [57]), the process is done in vacuum to increase their mean free path.

Most SEMs incorporate detectors for backscattered electrons as well. These are electrons from the initial beam that have been reflected backwards due to elastic collisions and can be distinguished from secondary electrons by the energy difference. Backscattered electrons provide contrast between elements, depending on the difference of their atomic numbers and thus can readily see thin films transparent under optical microscopes.

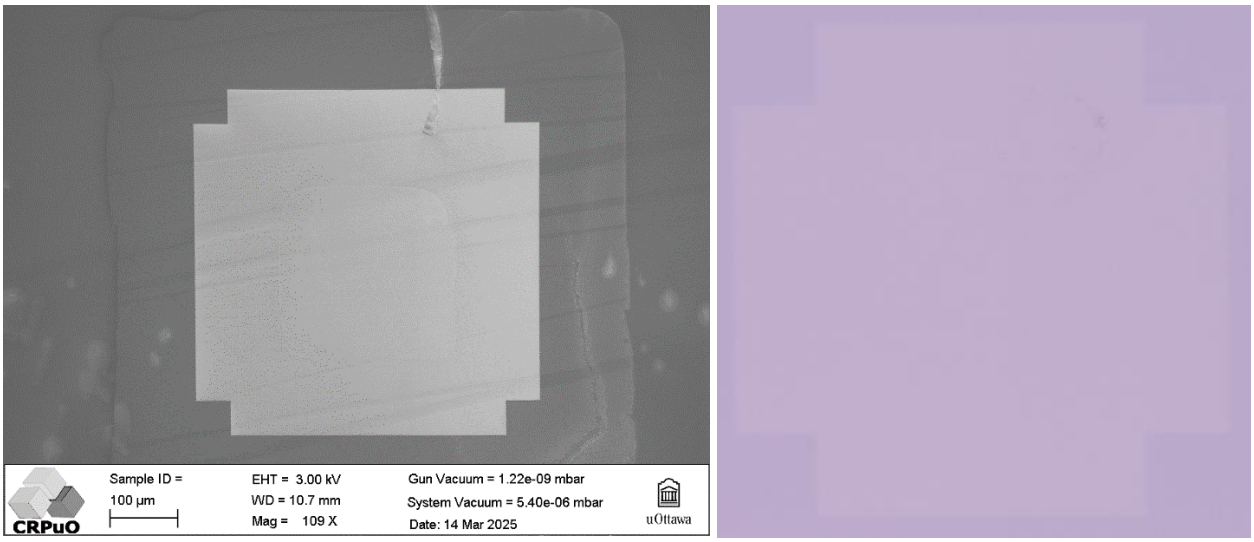

Figure 2.21: 1 nm thick gold thin film deposited on a silicon substrate viewed through an electron microscope (left) and optical microscope (right). High contrast is provided due to the atomic number difference between silicon (14) and gold (79). SEM image provided by Mathieu de Lafontaine, personal communications.

2.6.5 Energy Dispersive X-ray Spectroscopy

Secondary and backscattered electrons are not the only signals that an electron beam can produce. A high energy electron may knock an inner electron free (creating a secondary electron) from its atomic orbital and replace it within a higher energy orbital. The new electron rapidly decays to the newly vacant lower energy orbital, releasing the energy difference as an x-ray in the process. As each element has a distinct energy spacing between its orbitals, analysis of the x-ray spectrum reveals what elements are present in the sample by comparison to known elemental signatures. This process is known as energy dispersive x-ray spectroscopy (EDX).

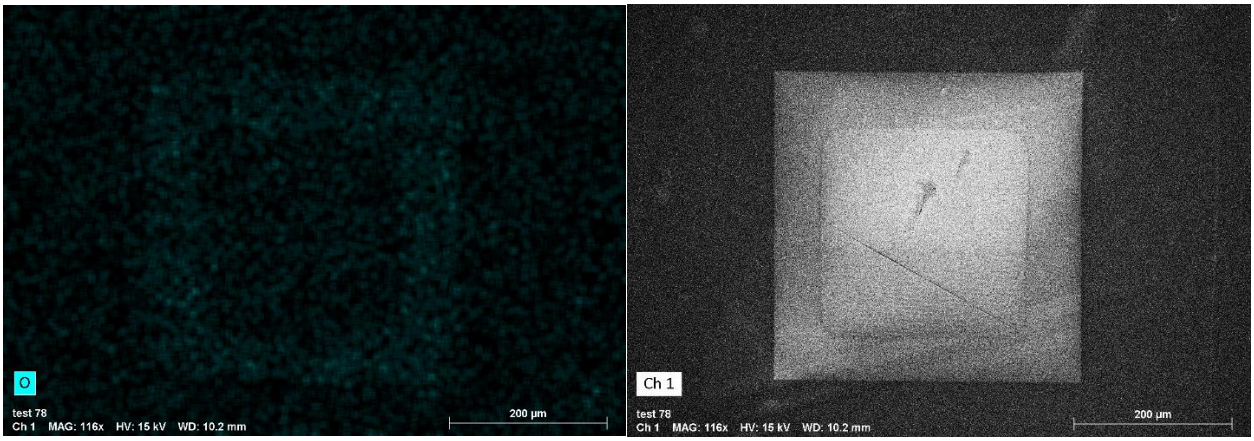

Figure 2.22: EDX (left) and SEM (right) images of a discoloured gold film. EDX reveals the reason for the discolouration is excess oxygen, likely in the form of silicon dioxide, underneath the discoloured areas. Images provided by Mathieu de Lafontaine, personal communications.

2.6.6 The Hall Effect

The Hall effect arises when an electrical current within a semiconductor is deflected by a magnetic field [58]. This produces a voltage which is transverse to the current, which can be used to extract useful parameters about the electrical properties of the conductor such as the charge carrier mobility, concentration and type of dopant. A typical test setup for measuring the Hall effect requires that the current, deflection voltage and magnetic field be orthogonal to each other:

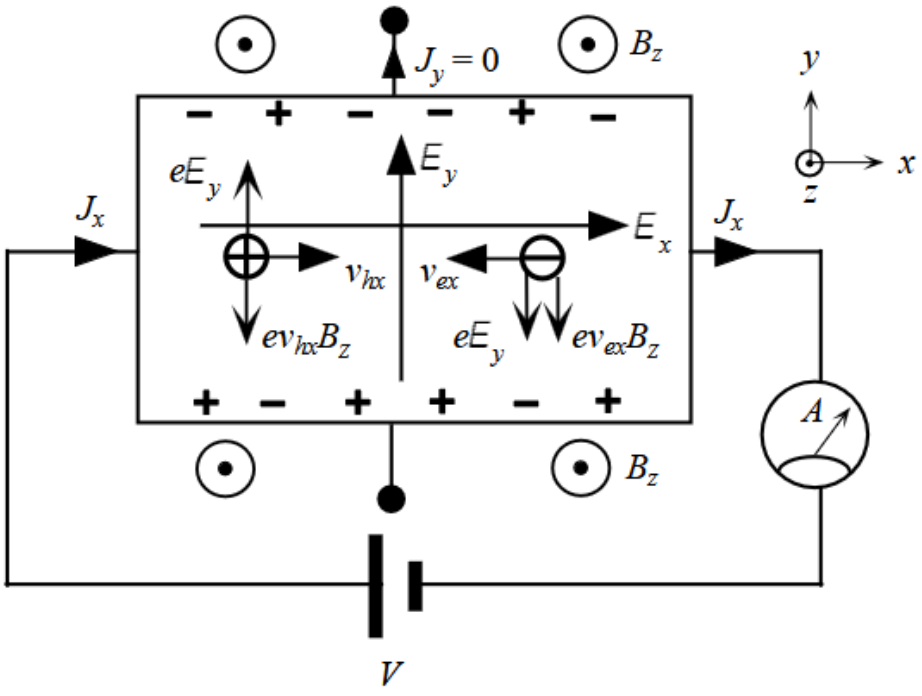

Figure 2.23: Test setup for measuring the Hall effect. A current travelling in the x direction (JX) is deflected by an orthogonal magnetic field in the z direction (Bz), resulting in a deflection voltage in the y direction (eEy) orthogonal to both. Taken from [59].

If the electric current, magnetic field strength and deflection voltage are known, the Hall coefficient R_H can easily be calculated:

$$R_H = \frac{E_y}{J_x B_z}$$

Where E_y is the electric field induced by the deflected current, J_x is the current density, and B_z is the strength of the magnetic field deflecting the current. The units of the Hall coefficient are usually expressed as m^3/C or Ω cm/G. This quantity can be related to the carrier properties by the following equation:

$$R_H = \frac{p\mu_h^2 - n\mu_e^2}{e(p\mu_h + n\mu_e)^2}$$

This can be expressed in the simpler form:

$$R_H = \frac{p - nb^2}{e(p + nb)^2}, b = \frac{\mu_e}{\mu_h}$$

Where p and n are the concentrations of holes and electrons, μ_h and μ_e are the mobilities of holes and electrons, and e is the elementary charge. In practice, a majority carrier dominates the equation, which allows for the minority carrier concentration to be approximated to zero. Positive Hall coefficients indicate holes are the majority carrier, while negative Hall coefficients indicate electrons are the majority carrier.

2.7: Monte Carlo Simulations

The Monte Carlo method is a probabilistic simulation technique used to model systems that may not have analytical models. By modeling the system as a series of probability density functions and generating a large number of random inputs, the output converges due to the law of large numbers. This technique was first invented during the Manhattan project for evaluating how neutrons travel through shielding material and was subsequently applied to many similar problems, such as evaluating how an ion beam travels through a silicon substrate. The general implementation of the method is as follows [60]:

1. Model the system as a series of probability density functions
2. Repeatedly and randomly sample
3. Tally the statistics of interest

For this work, SRIM [47] was used as the Monte Carlo simulator of choice for modelling the ion implantation process.

Chapter 3 Design Process

This chapter will cover the design process for creating the process flow for a short-wave infrared photodetector based on gold hyperdoped silicon. Several design criteria needed to be met not just due to the specific requirements of gold hyperdoped silicon, but also due to the availability of equipment and chemicals. The objective is to create a repeatable process flow using industry compatible equipment while minimizing process outsourcing.

Section 3.1 will discuss device layouts fabricated for this work. Section 3.2 will discuss substrate selection, why specific background doping concentrations and types were selected and the impact of crystal orientation. Section 3.3 discusses the design process for ion implantation such as selection of implant energies, thermal oxide thicknesses, and results of Monte Carlo simulations via SRIM. Section 3.4 discusses the design process for etching processes, selection of etches and their chemistry, calibration experiments and measurements. Section 3.5 discusses the design of the device metallization including which metals to use, annealing temperatures and times, layer thicknesses and the transfer length method (TLM) used to characterize the test metalizations.

3.1 Device Layouts

As discussed in chapter 2, photodetectors ideally have long carrier lifetimes. Ordinary silicon photodetectors achieve this by minimizing contamination, reducing the amount of deep level traps available to assist recombination. However, gold is known to reduce carrier lifetimes in silicon, heavily impacting the extraction efficiency of a gold hyperdoped silicon photodetector. To mitigate short carrier lifetimes, device layouts were designed to minimize the distance a photoexcited carrier needs to travel to exit a hyperdoped region.

First, the active area of each device was defined to be a 700 by 700 μm square, with 300 μm of guard space between devices. Three masks were defined for the photodetector

devices: *p*+/*n*+ doping, gold hyperdoping, and metallization. These three layers were varied to create three different categories of device layouts. The first is the Corner layout, which places four small metallization squares 150 by 150 µm at the corners of the active area, over a square ring of high doping. The gold hyperdoped area was then placed inside the ring. The second layout is the Busbar layout, which places two parallel busbars 700 by 150 µm on the edges of the active area, with the gold hyperdoping in between. Finally, the third layout is the Teeth layout, which is similar to the Busbar layout but additionally places interdigitated highly doped lines in the gold hyperdoped region.

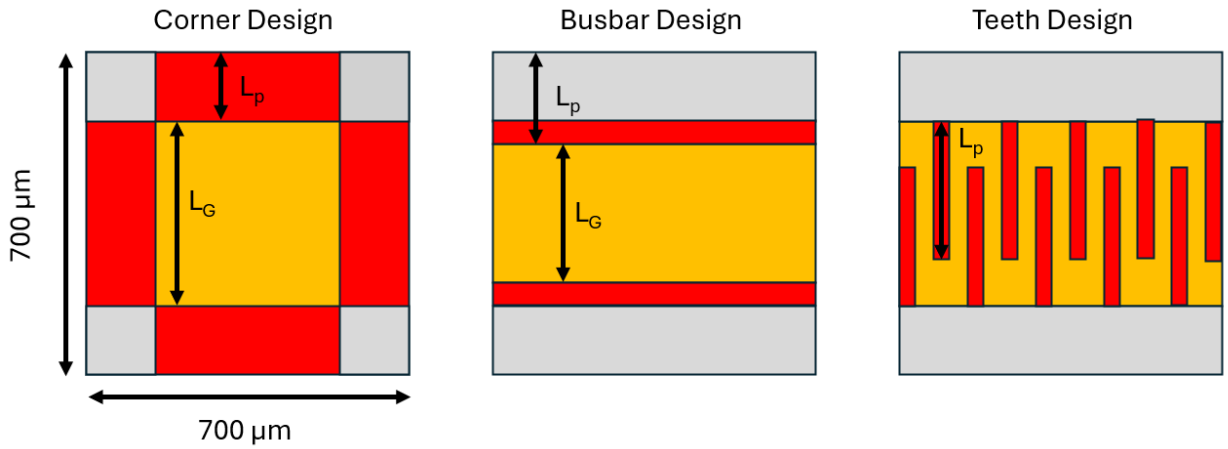

Figure 3.1: Device layout formats used for this work. Metal contact pads are shown in grey, the highly doped emitter is red, and gold hyperdoped silicon is gold.

Figure 3.1 depicts the layout formats used for this work. The Corner layout is a common layout used for standard photodetectors, while the Busbar layout is a common layout for solar cells. The goal of the interdigitated highly doped lines in the Teeth layout is to minimize the amount a photogenerated carrier spends in the hyperdoped region. By extending conductive "highways" into the gold hyperdoped region, carriers only need to travel a short distance before reaching a region where the carrier lifetime and mobility is large, increasing the amount of successfully extracted photogenerated carriers. Each layout format is

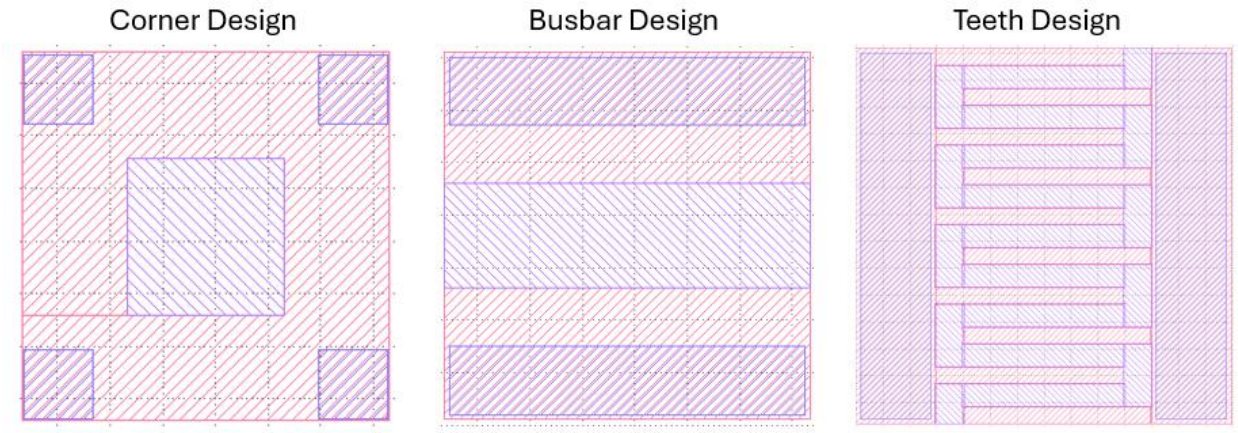

Figure 3.2: Overlaid masks for one iteration of each layout. Red indicates the area for ion implantation to form the emitter, backslashed purple indicates where the gold will be deposited for PLM and forward slashed purple indicates where the metal contact pads will be deposited.

Furthermore, each layout varies the dimensions of the highly doped and gold hyperdoped regions. This is done to investigate the effects of dopant mixing. For instance, the Corner layout varies the width of the highly doped ring and the width of the interior gold hyperdoped square, such that variations with no mixing, minimal mixing, full mixing, and several intermediate mixing cases are all present.

Table 3.1: Detailed device layout parameters.

Device layout	Emitter shape	Si:Au shape	Metallization shape
Corner	Square ring around outside of active area. L_p = 150, 200, 250, 300, 350 µm	Square centered in the active area. L_G = 100, 200, 300, 400, 500, 600, 700 µm	Four 150 x 150 µm contact pads at each corner of the active area.
Busbar	Two parallel rectangles extending from the top and bottom of the active area. L_p = 150, 200, 250, 300, 350 µm.	Single rectangle centered in the active area. L_G = 100, 200, 300, 400, 700 µm.	Two 150 x 700 µm contact bars at the top and bottom of the active area.
Teeth	Parallel rectangles 150 x 700 µm underneath the contact bars, with 10 interdigitated lines 34 µm wide, 40 µm apart extending into the active area. L_P = 100, 150, 200, 250, 300, 350, 400 µm.	Single rectangle centered in active area, with varying amounts of overlap or separation with the emitter. Overlap lengths: 4 ,2 µm, full overlap Separation lengths: 4, 2, 0 µm	Two 150 x 700 µm contact bars at the top and bottom of the active area.

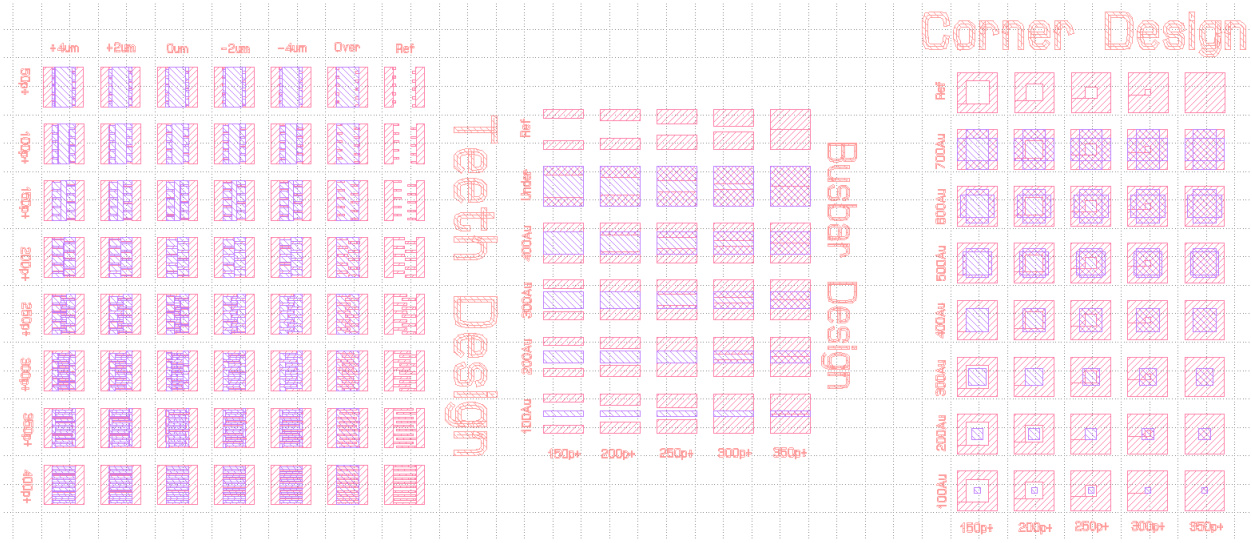

Figure 3.3: Mask image of a full device set. The purple mask layer shows where the gold hyperdoped silicon is, while the red mask layer shows where the doped areas (emitters) are. Lettering and numbers are part of the alignment etch.

Figure 3.3 shows all the combinations of each layout format. In total, there are 126 unique devices across the three layout formats. This includes unique reference layouts, which have identical emitter structure to their respective row/column but lack gold hyperdoping.

3.2 Substrate Selection

The beginning of any process flow is a blank wafer. This wafer is not a completely blank slate; it has its own parameters such as material, crystal orientation, and background doping, which need to be selected.

Material and crystal orientation were first selected. As the intent of the work is to create a device using gold hyperdoped silicon, the wafer evidently has to be silicon. The crystal orientation of the wafer surface was selected to be (100), which is the most common orientation for silicon devices. Additionally, it has been shown that the pulsed laser mixing process is most effective on this orientation [61], relative to the second most common wafer orientation (111).

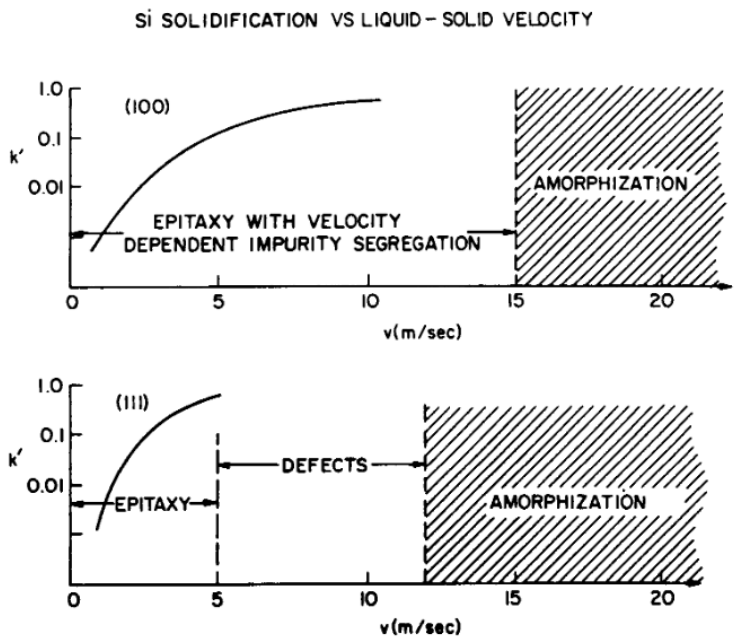

Figure 3.4: Resulting silicon solid after a pulsed laser melting depending on the velocity of the liquid-solid interface. The (111) crystal plane begins to form defective crystals at slower recrystallization speeds than the (100) plane, causing difficulties for hyperdoping. Taken from [61].

The final parameter to select is the wafer's background doping. Typical silicon photodetectors use lightly doped substrates (1 – 10 Ω cm) while implanting a highly doped region to create the PN junction, which causes the depletion/photosensitive region to only extend into the substrate. As the substrate is lightly doped, the depletion region extends far into the substrate, increasing the absorptive area. Furthermore, metallization can be placed on top of the highly doped areas for good ohmic contacts without blocking any incident light. Previous works creating hyperdoped silicon photodetectors have used lightly doped silicon wafers [5], [7], [10].

However, in a hyperdoped device the photosensitive region is independent of the PN junction geometry. As the carrier lifetime is low, it is more important to quickly separate charge carriers for extraction by intensifying the built-in electric field. It has been suggested that this can occur by increasing the substrate doping [8], which is further supported by

simulations done in Simudo [62], a Poisson/drift-diffusion device model for intermediate band materials created in house:

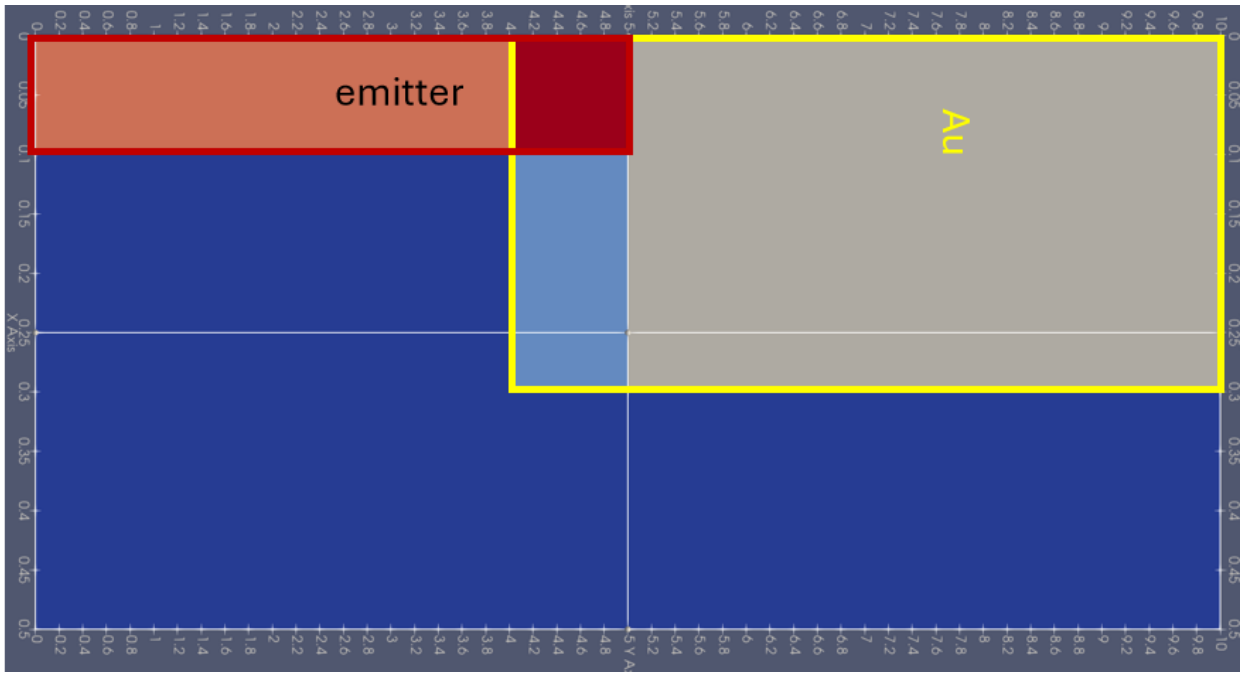

Figure 3.5: Poisson drift/diffusion model in Simudo of a contact between the gold hyperdoped area and a highly doped emitter. The gold concentration is exponentially decaying from the surface, while the emitter and substrate are uniformly doped. From Jacob J. Krich, personal communications.

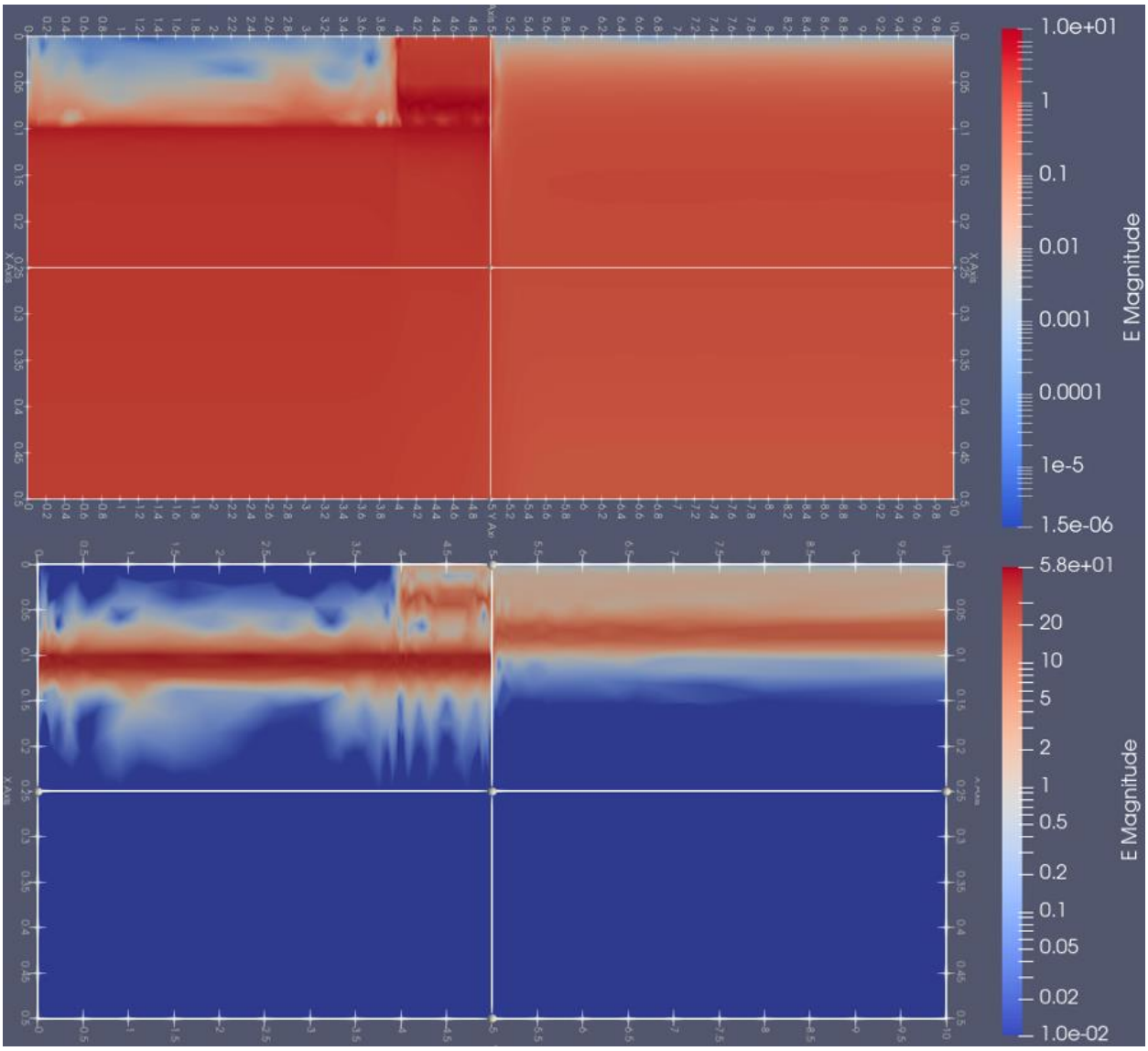

Figure 3.6: Electric field distribution for substrate doping concentrations of 10^{16} cm^{-3} (top) and 10^{18} cm^{-3} (bottom) as a function of position. Higher doping concentrations significantly increase the electric in the hyperdoped area. From Jacob J. Krich, personal communications.

Furthermore, gold is usually an amphoteric dopant in silicon, meaning it is capable of simultaneously behaving as a donor and as an acceptor. Thus, it is worth investigating if gold hyperdoped silicon devices can be fabricated on p type substrates, as previous works have exclusively focused on n type substrates.

Table 3.2: Substrates used for this work. All wafers are (100) silicon with 300 nm of thermal oxide.

Substrate Name	Doping	Source
1A	Phosphorous doped (n) 1 – 10 Ω cm	University Wafer
1B	Phosphorous doped (n) 1 – 10 Ω cm	University Wafer
2A	Antimony doped (n) 0.01 – 0.02 Ω cm	NOVA Electronic Materials
3A	Boron doped (p) 0.01 – 0.02 Ω cm	NOVA Electronic Materials

The Simudo simulations above show that despite the lateral device design, a built-in electric field still forms in the gold hyperdoped silicon layer. Thus, reverse bias can be applied during device operation to improve the charge collection efficiency. Currents can be measured using an ammeter. Figure 3.7 illustrates a typical setup for device operation in reverse bias with an ammeter to measure photogenerated current.

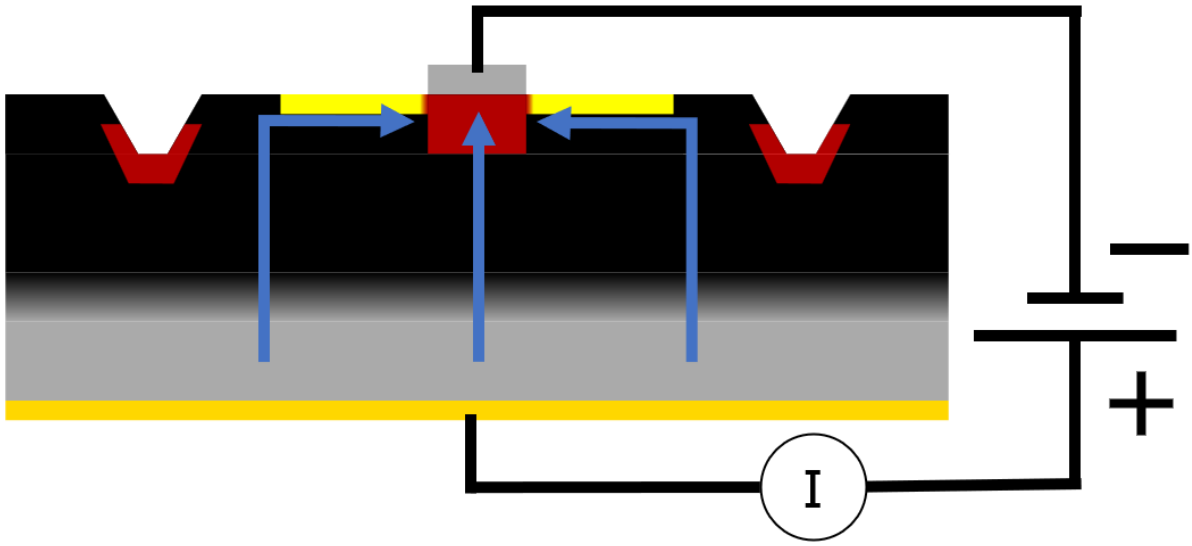

Figure 3.7: Cross section of a device during operating conditions. Blue arrows denote the field lines of the device's internal electric fields.

3.3 Ion Implantation Process Development

Ion implantation is an aggressive process that cannot be masked via typical photoresist masks. Harder masking materials such as silicon oxide are used instead, which can be readily grown via thermal oxidation on a silicon wafer prior to purchase. As BOE has excellent selectivity between silicon oxide and photoresist, a pattern can be created on top of the silicon oxide layer and etched into the silicon oxide to serve as the ion implantation mask. A suitable oxide thickness needs to be selected beforehand: thick enough to reliably block an ion implantation, but as thin as possible to minimize the required etch time, and thus the sidewall erosion due to isotropic nature of the HF wet etch. Monte Carlo simulators such as SRIM are used to predict and plan ion implantation processes.

As the University of Ottawa does not possess an ion beam for implantation, this step was outsourced. Initially, plans were made to have the implantation done at the University of Sherbrooke. However, I found out that their ion beam has a minimum implant

energy of 25 kV. SRIM produces the following graphs for a 25 kV boron implant:

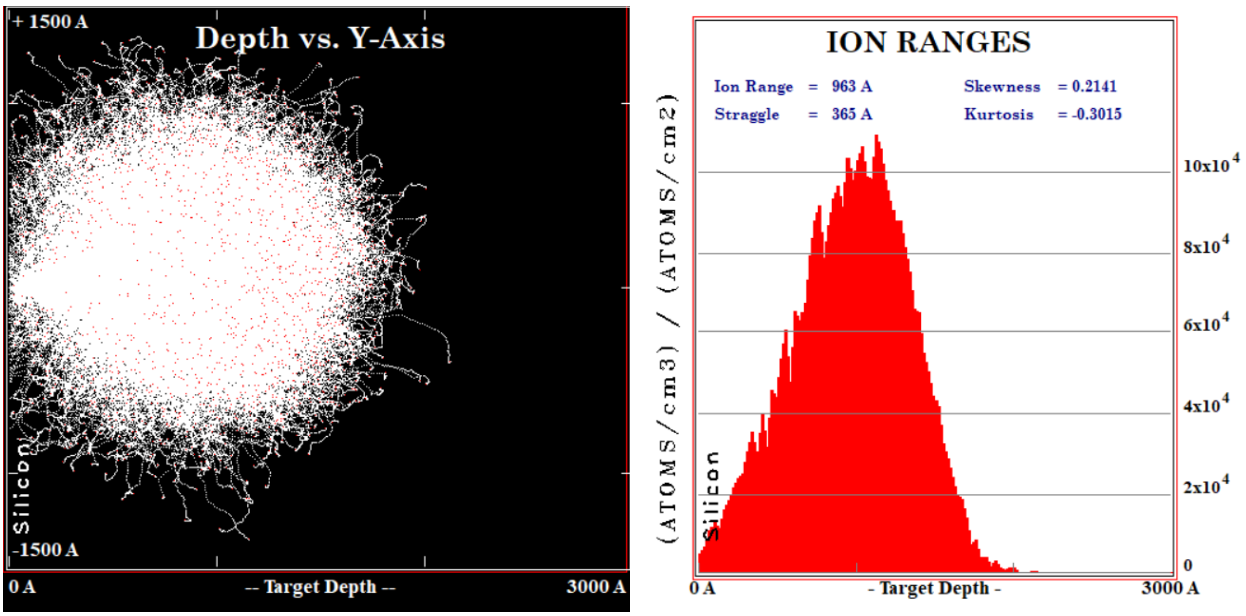

Figure 3.8: Raw SRIM Monte Carlo result (left) for a 25 kV boron implant into silicon and the resulting boron distribution histogram as a function of ion beam dosage (right).

This was problematic, as it is desirable to have a shallow implant as the hyperdoped gold region decays exponentially from the surface. The decision was made to perform the ion implantation step commercially with Cutting Edge Ions in the United States, as they were willing to perform the implantation with a 4 kV implant energy.

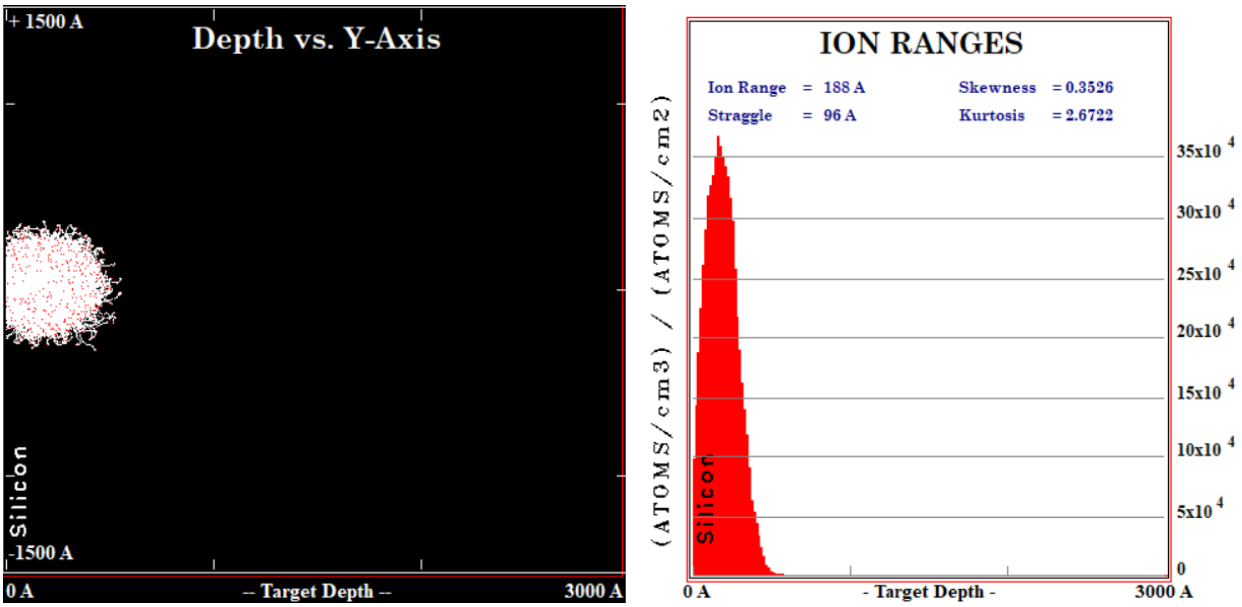

Figure 3.9: Raw SRIM Monte Carlo result (left) for a 4 kV boron implant into silicon and the resulting boron distribution histogram as a function of ion beam dosage (right).

As photoresist masks are insufficient to block an ion beam, a hard mask of silicon dioxide was used instead. Thermal oxidation is a well-known process which produces a thin layer of oxide on top of a silicon wafer of a desired thickness. Silicon wafers with varying amounts of pre-grown oxide are readily available on wafer supply catalogs. A 300 nm thermal oxide layer thickness was selected for this project as SRIM results show it is sufficient to block a 25 kV ion beam:

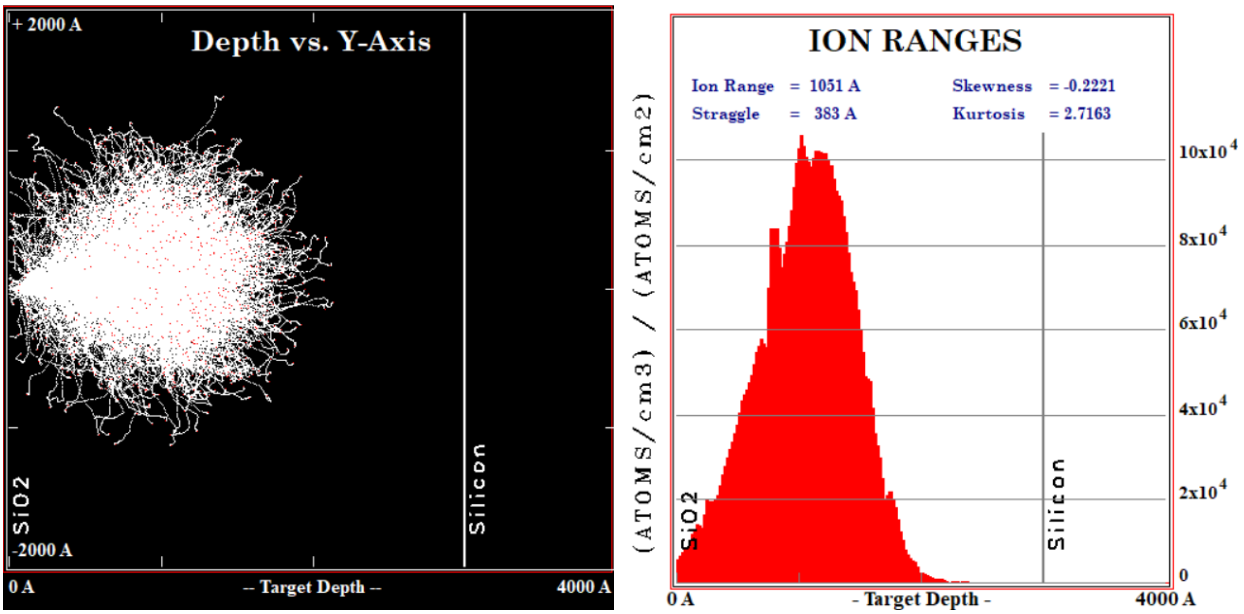

Figure 3.10: Raw SRIM Monte Carlo result (left) for a 25 kV boron implant masked by a 300 nm layer of silicon dioxide and the resulting dopant distribution histogram (right), 10000 trials. Note how the boron was completely stopped by the silicon dioxide layer.

Multiple lower energy implants were evaluated from 2 kV to 8 kV. The choice was made to perform the ion implantations at 4 kV, as 2 kV showed to be excessively shallow.

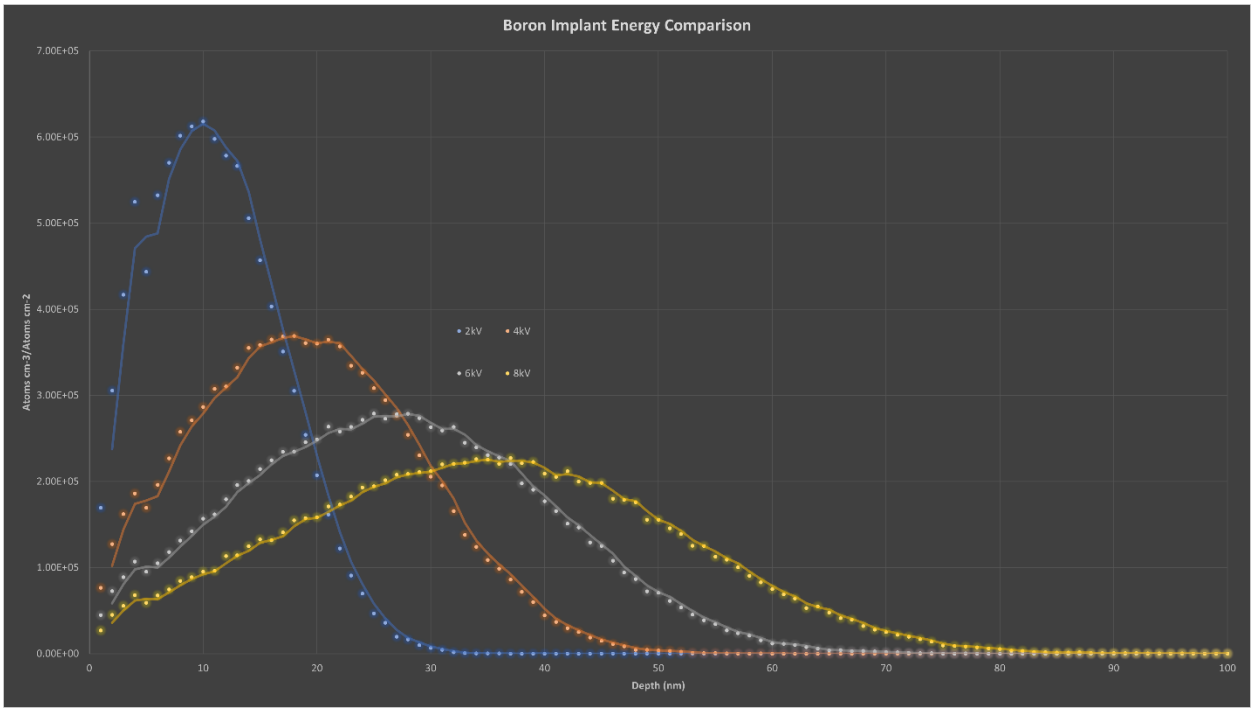

Figure 3.11: Aggregated Monte Carlo simulations from SRIM for a boron ion implantation process with varying implant energies.

3.4 Etch Process Design

As the process flow requires multiple patterns that need to be aligned to each other, it is necessary to etch alignment marks into the surface of the silicon as the first step of the process. An aqueous solution of 49% potassium hydroxide (KOH) was selected to accomplish this. A KOH etch is self terminating at the (111) silicon plane [63], which forms trapezoidal cavities with sidewalls at a 54.7° from the (100) surface. It is often heated to approximately 80 °C to increase the etching speed to micrometers per minute, but as the alignment marks do not need to be deep, only visible, room temperature KOH was used to simplify the process. Test samples were used to calibrate the process by varying etch times. Measurement of etch depths was done using profilometry. Alignment marks include both words to indicate the layout of each device, as well as symbols to provide XY and rotational alignment capabilities.

Figure 3.12: Optical microscope image post KOH etch calibration on a (100) test silicon wafer for 30 min. Alignment marks become clearly visible under the optical microscope, allowing subsequent patterns to be aligned.

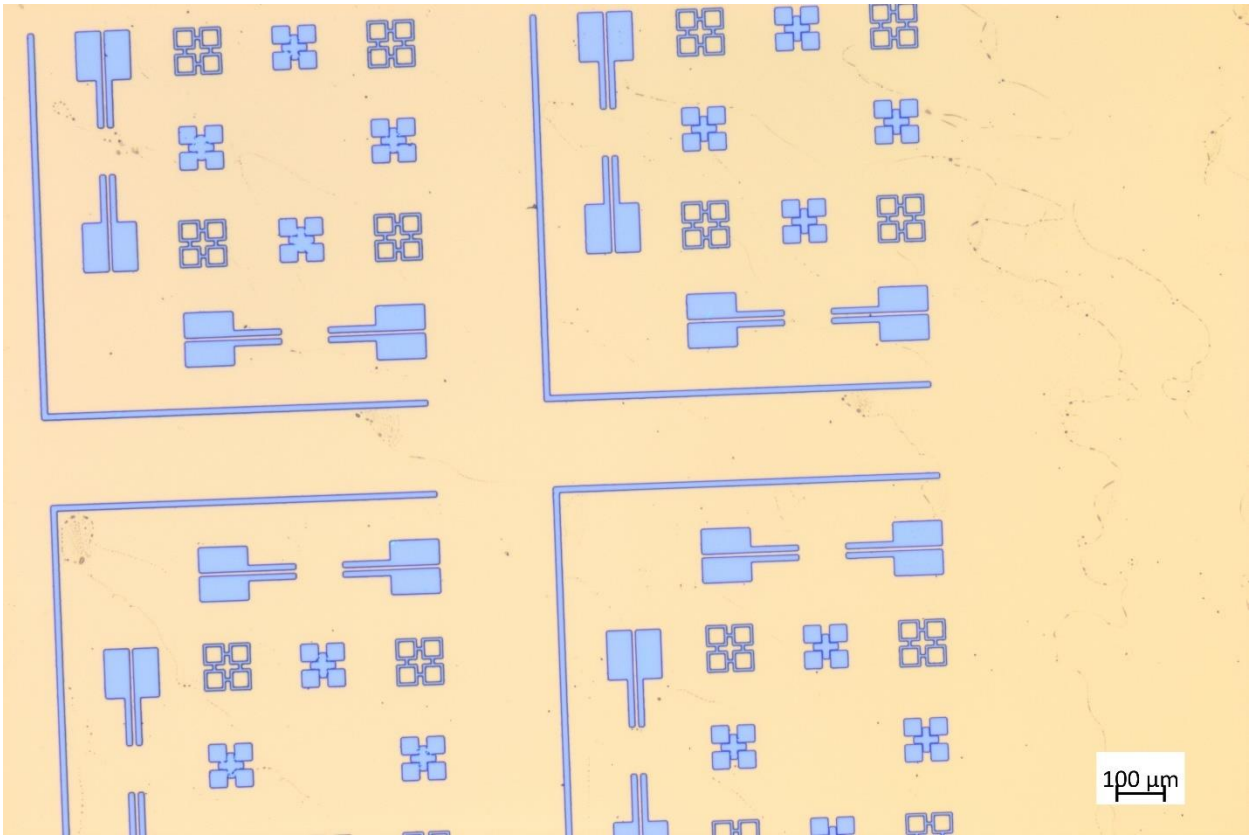

Figure 3.13: Pattern used to create alignment marks. Subsequent patterns in the process flow have “L” shapes designed to fit into the slots. Aligning to several marks allows for rotational alignment.

In addition, the HF etch on the thermal oxide needed to be calibrated as well. Due to the isotropic nature of the etch, sidewalls will be eroded at the same rate as the intended etch. It is essential to minimize etch time to maintain pattern fidelity.

Similarly to the KOH etch calibration, HF etch calibration was done by soaking the sample in HF for varying amounts of time and measuring the etch depth using profilometry.

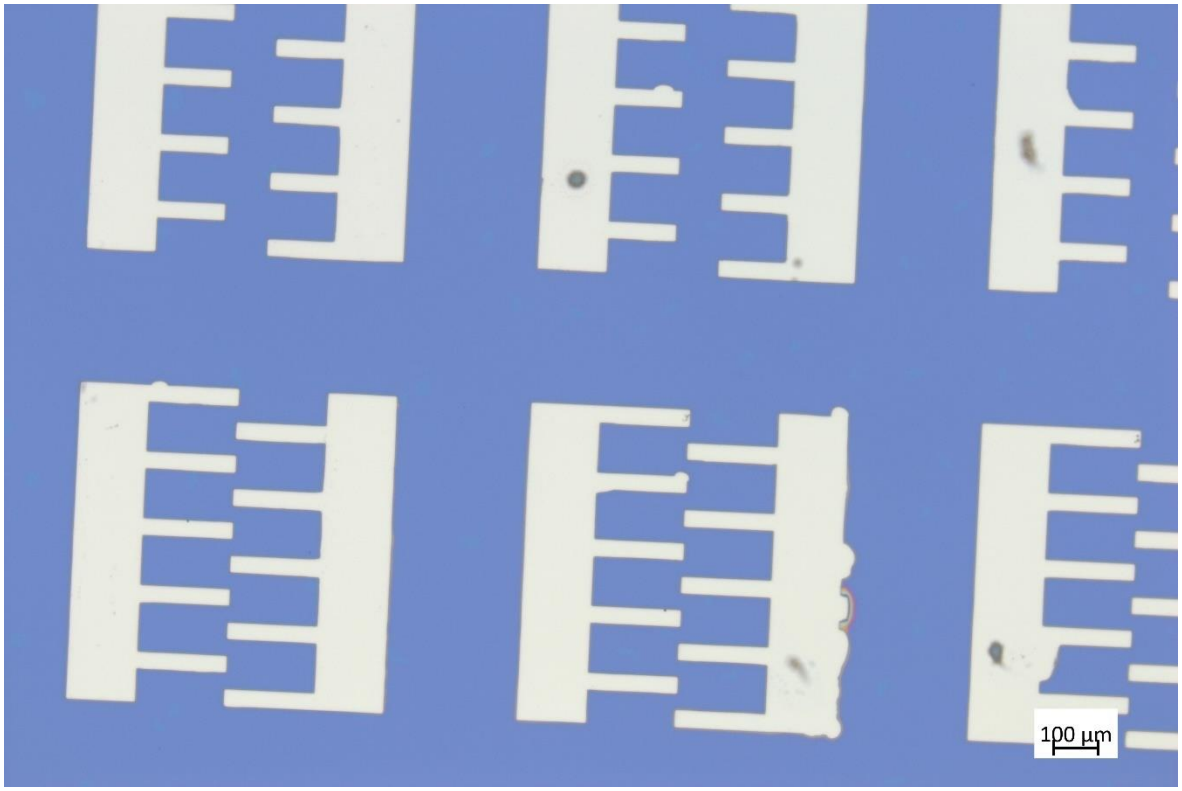

Figure 3.14: Top view optical microscope image of device wafer following ion implantation. Blue is the 300 nm silicon oxide mask, gray is the silicon substrate. Some damage to the silicon oxide mask is visible due to the ion beam.

3.5 Metallization Process Design

Metallization is an important part of every photonic device to either supply or extract charge carriers. As discussed in chapter 2, the choice of metal cannot be arbitrary; the metal and semiconductor must be compatible to form a proper ohmic contact. Furthermore, most metalizations require thermal anneals to restore crystallinity to the metal film or to bond with the silicon substrate. These requirements may clash with gold hyperdoped silicon, as gold segregates out of silicon when heated above 350 °C. Thus, the position of the metallization processes within the process flow needs to take into consideration this fact.

As the Fermi level shifts depending on the doping type of the silicon, different metals need to be used for contacts to p or n type silicon. Aluminium is the natural choice

of metal for this purpose: it belongs to the same element group as other p type dopants, it requires lower temperature anneals due to its lower melting point, and it readily bonds and alloys with silicon [64]. Furthermore, aluminium rapidly forms a passivating oxide in standard atmosphere, protecting the thin film. Aluminium was the standard contact metal for integrated circuits in the early days of the industry, however, has been supplanted by titanium copper bilayers due to electromigration issues as feature sizes shrunk [65]. As features sizes for this work are large enough for electromigration to not be a concern, aluminium was selected for as the p type contact metal.

Aluminium contacts to silicon are usually annealed at 425 °C. As this step was to be performed after the pulsed laser mixing process, this anneal would have exceeded the thermal budget of gold hyperdoped silicon. I experimentally verified that a lower temperature anneal at 300 °C would be sufficient to form an ohmic contact.

For the n type contact metal, titanium was selected based on prior work done at the NanoFab. Titanium is a standard contact metal for silicon in the semiconductor industry for salicide (self-aligned silicide) contact recipes [43]. A thin film of titanium on a silicon substrate will react during a sufficiently high temperature annealing process, forming $TiSi_2$. Titanium silicide has two distinct phases: C49, which forms at 700 °C and has high resistivity (60 – 300 μΩ cm) and C54, which forms at 800 °C and has a lower resistivity (13 – 20 μΩ cm). It has previously been reported that the C54 phase forms rapidly once the required temperature has been met [42], thus an 800 °C anneal for 5s was selected.

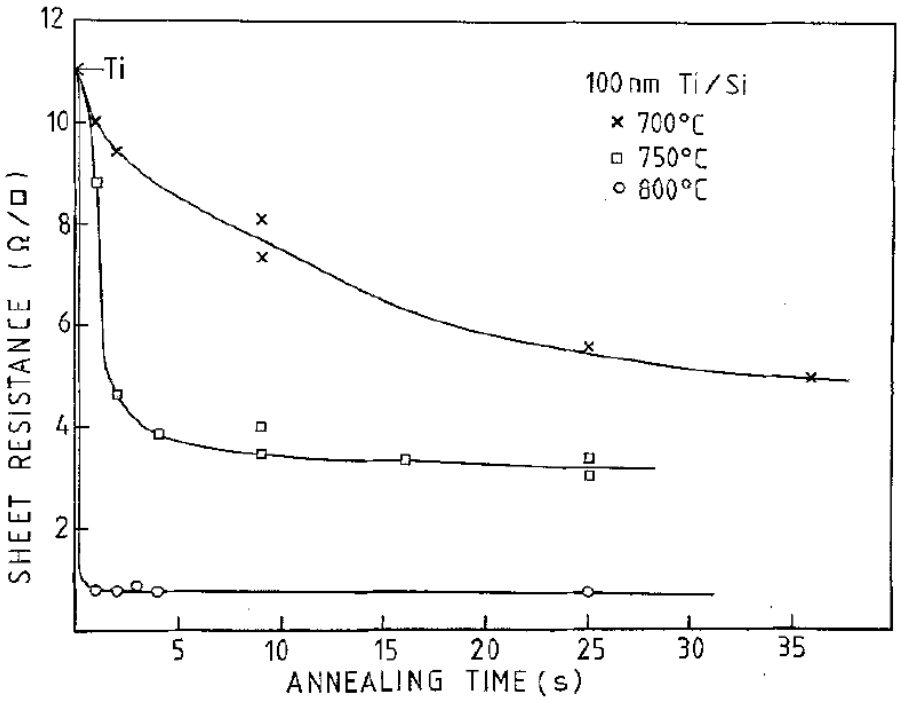

Figure 3.15: Sheet resistance of titanium silicide for varying anneal times and temperatures. Higher resistivities indicate the formation of the C49 phase, while lower resistivities indicate the formation of the C54 phase. Taken from [43].

Despite titanium's excellent adhesion and silicide formation, it also exhibits high resistivity for a metal. Thus, a thin titanium film is used to form the ohmic contact and to act as an adhesion and diffusion layer, while a more conductive metal such as copper or gold is deposited on top. The latter property is particularly important, as both gold and copper create deep electronic traps in silicon. I created and characterized both titanium copper and titanium gold bilayers for this work.

3.5.1 Transfer Length Method Calculations

To characterize the specific contact resistivity of the metallization recipes, the Transfer Length Method (TLM) was used. Circular TLM structures were deposited as a part of every metallization. Furthermore, metallization recipes were verified on test pieces of silicon prior to the process flow.

TLM requires that I-V measurements be taken across different gap lengths. The specific contact resistivity is determined using [55]:

$$\rho_c = R_s L_T^2$$

Where ρ_c is the specific contact resistivity, R_s is the sheet resistance of the semiconductor, and L_T is the transfer length. However, it is not possible to directly measure ρ_c or L_T. Instead, they are related to the total measured resistance by:

$$R_{tot} = \frac{R_s}{2\pi}\left[\ln\left(\frac{r+d}{r}\right) + L_T\left(\frac{1}{r} + \frac{1}{r+d}\right)\right]$$

Where r is the radius of the contact pad, d is the size of the gap and R_{tot} is the total measured resistance. As r and d are determined by the mask pattern and R_{tot} is easily measured, R_s can be extracted if L_T is known. L_T can be found by plotting extracted resistances for a variety of gaps and performing a linear regression. The x intercept of the linear regression will be $2L_T$.

The equation for the total resistance is unwieldy. If the gap is significantly smaller than the radius of the contact pad (d << r), the aforementioned equation can be approximated to:

$$R_{tot} = \frac{R_s}{2\pi r}\,[d + 2L_t]c$$

This approximation uses a first-order Taylor expansion on the natural logarithm in the original equation. It also requires the use of a correction factor, c, which is given by:

$$c = \frac{r}{d}\ln\left(\frac{r+d}{r}\right)$$

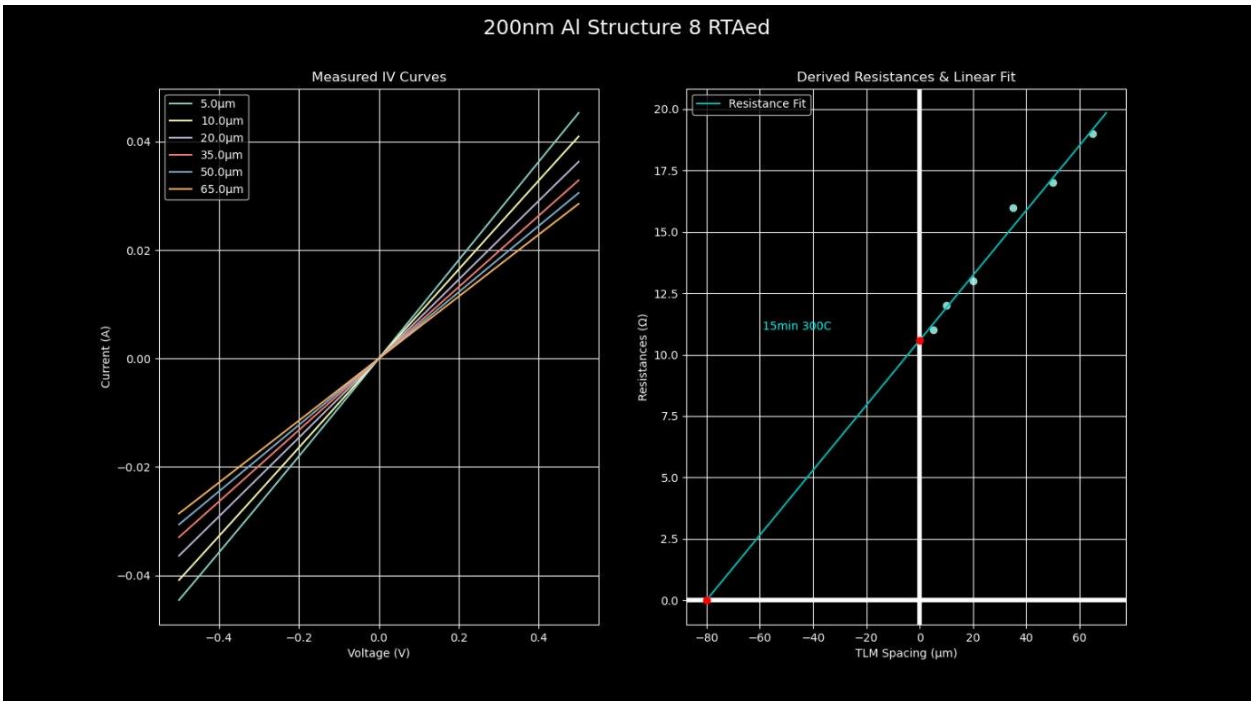

Figure 3.16: TLM performed on an aluminium contact using a variety of gap lengths. The graph on the left shows compiled I-V curves for varying gap lengths, while the graph on the right shows a linear regression performed on the extracted resistances.

Figure 3.14 shows the TLM method performed on experimental data for a 200 nm thick aluminium contact, after a 15 min anneal at 300 °C. As the I-V curves show ohmic behaviour, meaningful resistances can be derived from their slopes. These resistances are plotted against their corresponding gap length which allows a linear regression to be made. The transfer length, L_T, can be extracted from half the x intercept, 40 µm, which allows for the calculation of the average contact resistivity, $2.84 \times 10^{-6}\ \Omega\ cm^2$, for this set of TLM structures. This plot was generated using a Python script that I developed for automating TLM analysis.

3.6 Conclusion

This chapter discussed the design rationale of each process in the process flow. All the aforementioned work was done prior to individual process calibration, whose results will be discussed in chapter 4. Typical device layouts for photodetectors and solar cells

were used, as well as interdigitated doping structures. Substrates with different background doping were selected to investigate whether it would result in an increased field within the optically active areas of the device. Monte Carlo simulations using SRIM were used to select the energy and thermal oxide thickness for the ion implantation process. Finally, discussing the chemical and electrical properties of the etching and metallization processes were discussed as well for creating the alignment marks, ion implantation mask, and contact pads.

Chapter 4 Experimental Results and Issues

I performed much experimental work with a wide variety of equipment for this thesis. Chapter 4 covers the recipes used for each process, results of the process calibration and full process flow, and the issues that arose during the full process flow such as incomplete development of thick photoresist layers. See chapter 3 for the reasoning and design process of each process. EQE and I-V measurements from the final fabricated devices will be presented as well.

4.1 Photolithography Process

Two photolithography recipes were used during this work for pattern generation purposes. The first photoresist used is SPR220-7.0 [66], a positive, viscous, and commercially available photoresist. The second photoresist is SPR955 [67], a positive and fluid photoresist, used in tandem with LOR1A [68], a lift off resist, for creating undercut profiles. SPR220 and SPR955 are commercially available from Kayaku Advanced Materials and Dupont Electronic Materials Megaposit series of photoresists, whereas LOR1A belongs to Kayaku's LOR series of lift off resists.

UV exposition was done using the I-line (365 nm) of a mercury lamp. Masks were designed by Mathieu de Lafontaine and produced at the University of Alberta's NanoFab. I carried out the photolithography processes at the University of Ottawa's NanoFab with the available spin coater, mask aligner and materials. Prior to each UV exposition, the intensity of the lamp was measured and exposure time calculated.

4.1.1 SPR220

As the high viscosity of SPR220 causes it to form thick layers during spin coating, patterns derived from SPR220 were used to mask processes with aggressive chemicals, such as HF etching of SiO_2. It was also used as a protective layer without UV exposition during the backside metallization, dicing, and aqua regia cleaning processes.

Table 4.1: SPR220 recipe used for this work.

UV dosage	550 mJ/cm^2, 365 nm
Soft bake	115 °C, 90s
Spin speed	3000 RPM
Development	MF-24A, 60s (variable)
Remover	Remover 1165 / Acetone

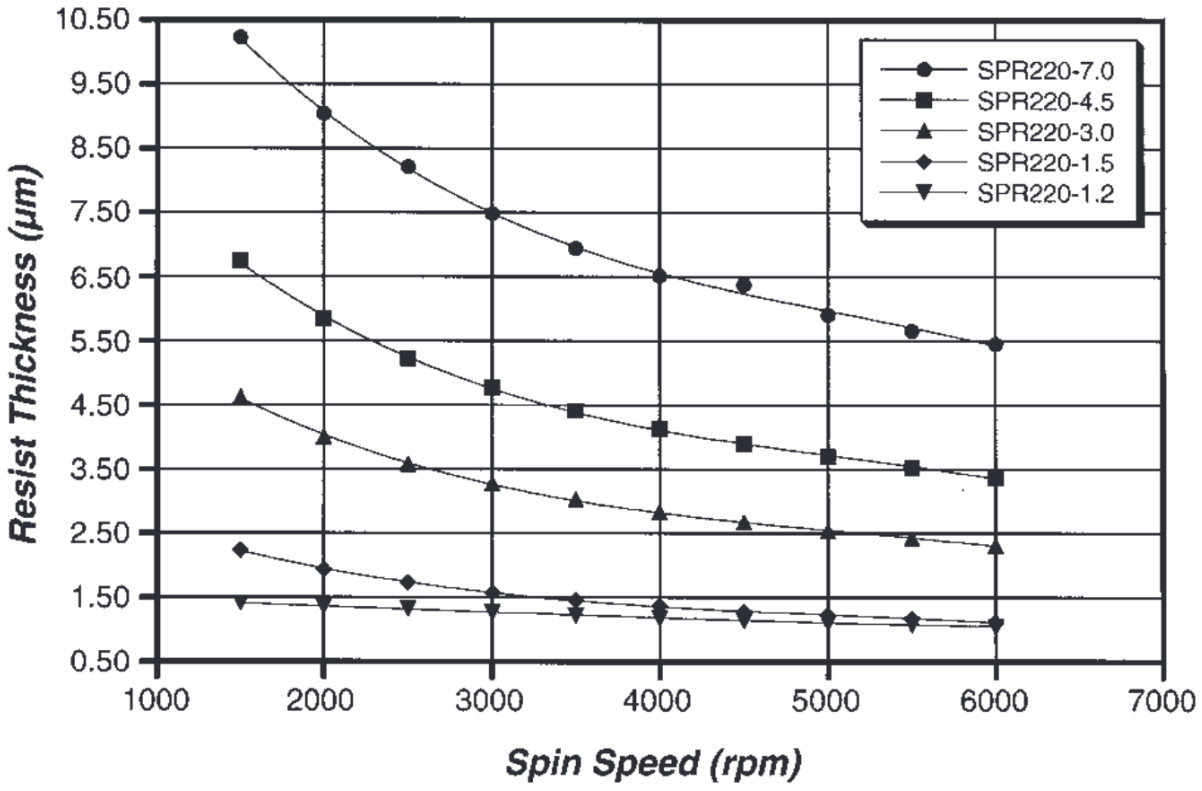

Figure 4.1: SPR220 film thicknesses for varying spin speeds and formulations. Taken from [66].

For spin speeds of 3000 RPM for SPR220-7.0, I found using profilometry that the resulting film thickness would be 7 – 8 µm. This correlates with the data provided by the manufacturer.

4.1.2 SPR955

SPR955 is a photoresist similar to SPR220. Both share the same photoactive compound and base resin, however the solvent for SPR955 is less viscous. This results in photoresist films that are much thinner, allowing for higher resolutions. For this work, SPR955 was always spun on top of LOR1A prior to metallization to allow lift-off processes.

Table 4.2: SPR955 recipe used for this work.

UV dosage	95 mJ/cm^2
Soft bake	90 °C, 5 min
Spin speed	3000 RPM
Development	MF-321, 45s
Remover	Remover 1165, Acetone

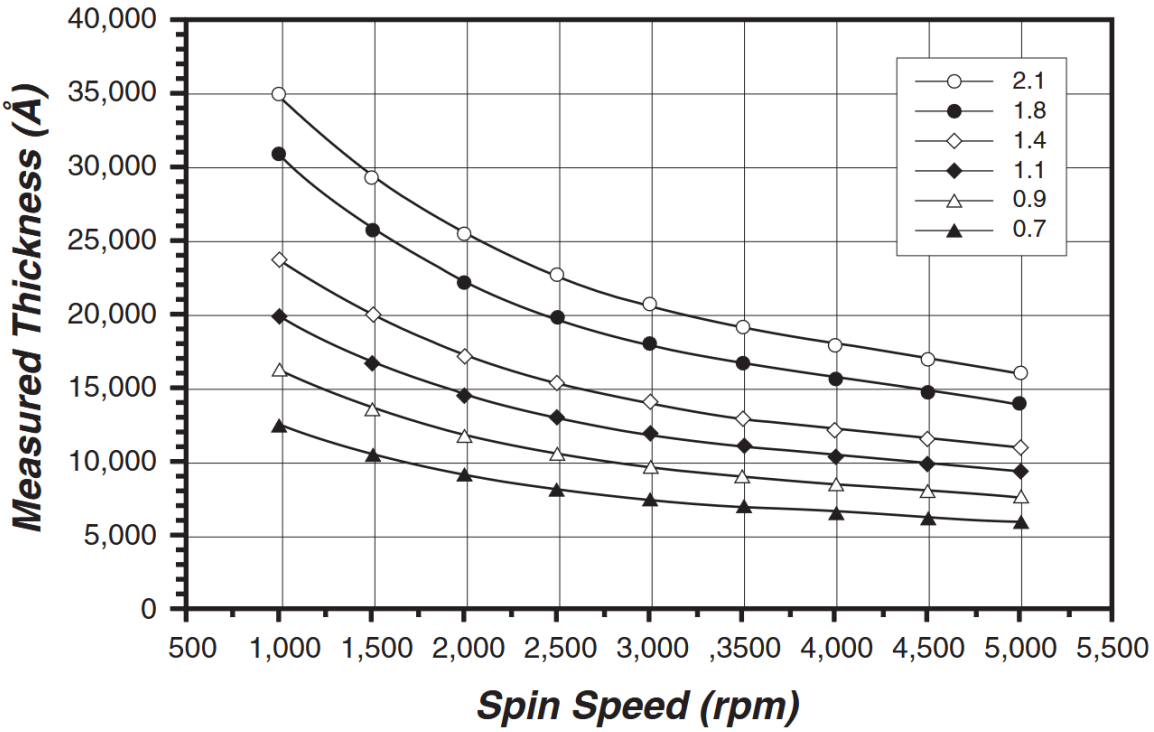

Figure 4.2: SPR955 film thicknesses for varying spin speeds and formulations. Taken from [67].

4.1.3 LOR1A

LOR1A is the least viscous lift-off resist of Kayaku's LOR series. This work uses LOR1A to create undercuts underneath a SPR955 layer, which contains patterns used for metallization. As it lacks a photoactive compound, it is unaffected by UV exposition.

Table 4.3: LOR1A recipe used for this work.

Soft Bake	170 °C, 5 min
Spin Speed	6000 RPM
Developer	MF-24A / MF-321
Remover	Remover 1165 / Acetone

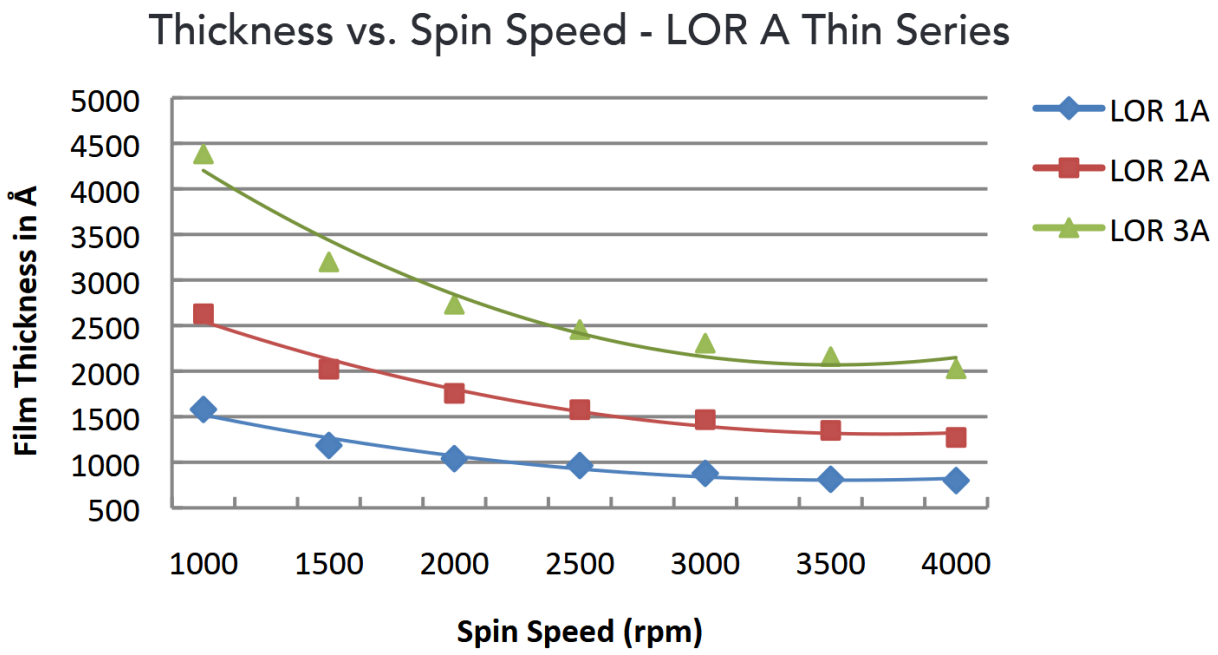

Figure 4.3: LOR A film thicknesses for varying spin speeds and formulations.Taken from [68].

4.1.4 Photolithography Issues

During the initial stages of the process flow, SPR220 was used for creating the patterns for HF etching of the thermal oxide. The first patterns for HF etching of the thermal oxide suffered from incomplete development of the photoresist layer. These issues did not arise during process calibration as calibration was done using small shards of silicon, while the full process flow used full wafers 100 mm in diameter.

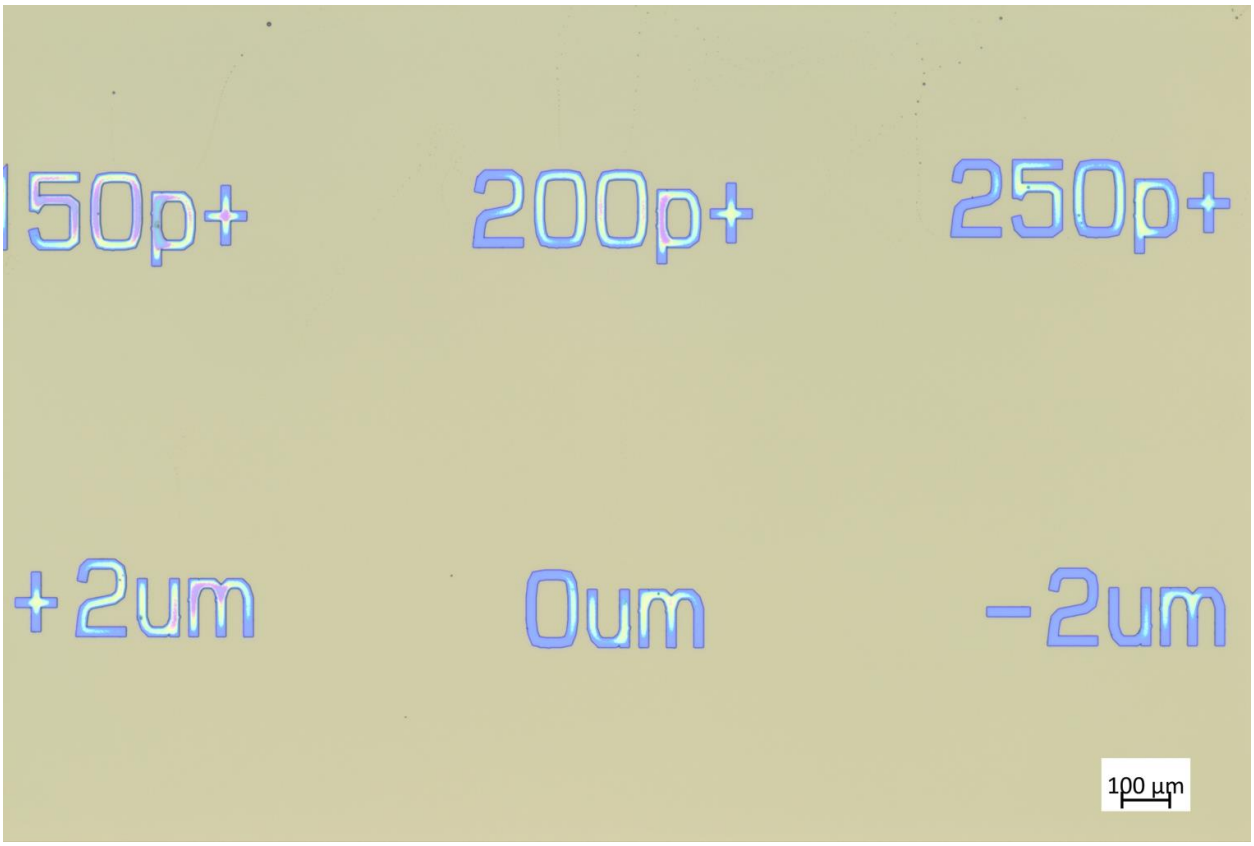

Figure 4.4: Optical microscope image of incomplete photoresist development. Blue is the underlying oxide, beige is a layer of SPR220 post development.

Interference fringes visible via optical microscope reveal the presence of a thin layer of photoresist within the exposed areas, indicating that the photoresist development process was incomplete. Incomplete development was caused by incomplete hydration of the photoresist layer post exposure. Positive photoresists are converted to an acidic compound upon exposure to UV light, which dissolves in an alkaline developer solution.

This acidification reaction requires water (see section 2.5.1). For thin layers and small samples this requirement can be ignored as ambient humidity will quickly hydrate the photoresist. However, for a large wafer and thick photoresist layer, the time between the hot plate and the mask aligner may not be sufficient to fully hydrate the photoresist layer. Dry photoresist does not dissolve in developer solution, even if it has been exposed to a sufficient UV dose. After this issue was discovered, subsequent samples were allowed to rest for 2 hours post soft bake to allow the SPR220 layer to hydrate from the ambient humidity.

Furthermore, it was found that the hot plates used for the soft bake were not perfectly uniform. The non-uniformity was insufficient to cause issues with smaller samples but caused some parts of the full wafer to be over/under baked. Using a temperature probe, it was found that parts of the hot plate were 10 °C colder than the set temperature of 115 °C (SPR220 soft bake). Subsequent soft bakes were done by checking the hot plate before with the temperature probe and placing the wafer on the most uniform temperature area.

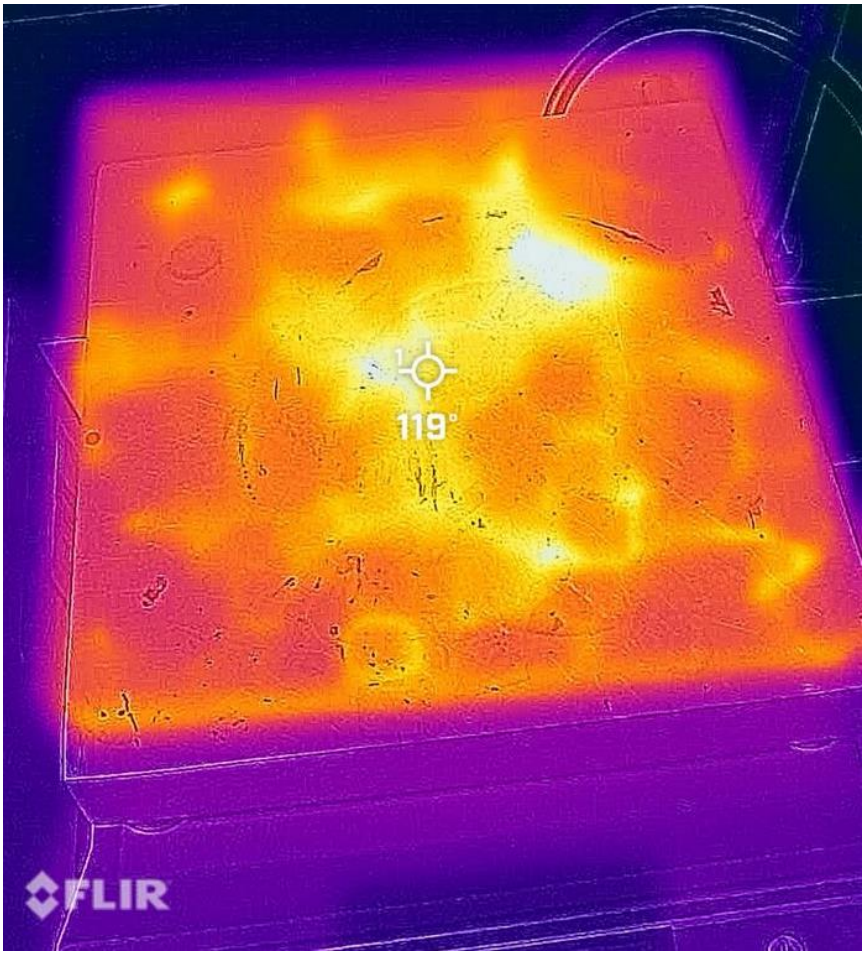

Figure 4.5: Thermal image taken using a FLIR ONE with an iPhone XR. The top right corner of the hot plate is hotter than the lower left corner.

4.2 Metallization Processes

Three metallization recipes for forming device contacts were used during this work. 200 nm of aluminium was used for creating contacts to p type silicon, while 10/50 nm of titanium and gold were used for creating contacts to n type silicon. Titanium copper bilayers were also investigated for use as a low temperature contact, in 10/100 nm and 30/100 nm thicknesses. All metalizations were deposited via electron beam evaporation using an Angstrom NexDep system and annealed using a Surface Science Integration Solaris 100 rapid thermal processing system.

Additionally, the NexDep system was used to deposit 1 nm of gold for pulsed laser mixing via thermal evaporation instead of electron beam evaporation. This step was immediately prior to PLM.

4.2.1 Aluminium Metallization

200 nm of aluminium was used to form contacts to p type silicon. These would form the top contacts for the device. As this process is to be done after the PLM process, a low temperature anneal is essential to maintain the integrity of the gold hyperdoped silicon. Aluminium has a lower melting point than most metals, and is usually annealed at 425 °C. In comparison, titanium contacts are annealed at 800 °C, thermal oxidation of silicon is done at 1000 °C, and dopant activation anneals are done at 1200 °C. However, 425 °C exceeds the thermal budget of gold hyperdoped silicon. I investigated whether the aluminium contact could be annealed at 300 °C prior to beginning the process flow. Figure 4.6 shows a TLM structure for testing the aluminium contact recipe. As aluminium rapidly develops a hard native oxide when exposed to air, probing the contact requires piercing the aforementioned oxide which damages the contact.

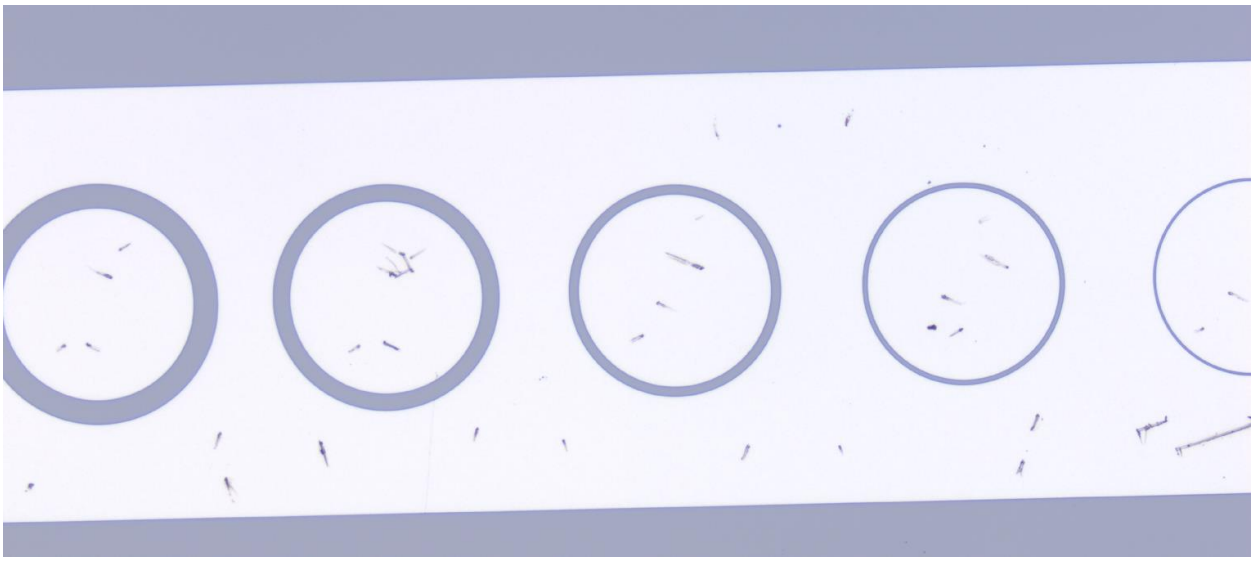

Figure 4.6: Optical microscope of a 200 nm aluminium film used for 4 probe I-V measurements for TLM.

Table 4.4: Aluminium metallization recipe used for this work.

Metals used	Aluminium
Metallization thickness	200 nm
Substrate	p-type silicon
Deposition process	Electron beam evaporation
Anneal recipe	300 °C, 15 min
Anneal atmosphere	10 sccm, N_2
Mean Pre-anneal contact Resistivity	Schottky
Mean post-anneal contact resistivity	$3.22 \times 10^{-6}\ \Omega\ cm^2$

As this recipe is intended for the final step of the process flow, the anneal would apply to the gold hyperdoped silicon as well. Shorter anneals were investigated as well to minimize the risk of thermal damage to the gold hyperdoped silicon. The recipe described in table 4.4 was attempted with a 10 min anneal instead of a 15 min anneal, resulting in an increase in mean specific contact resistivity from $3.22 \times 10^{-6}\ \Omega\ cm^2$ to $3.73 \times 10^{-6}\ \Omega\ cm^2$. However, not all contacts became ohmic, so the 15 min anneal was used to ensure ohmic properties.

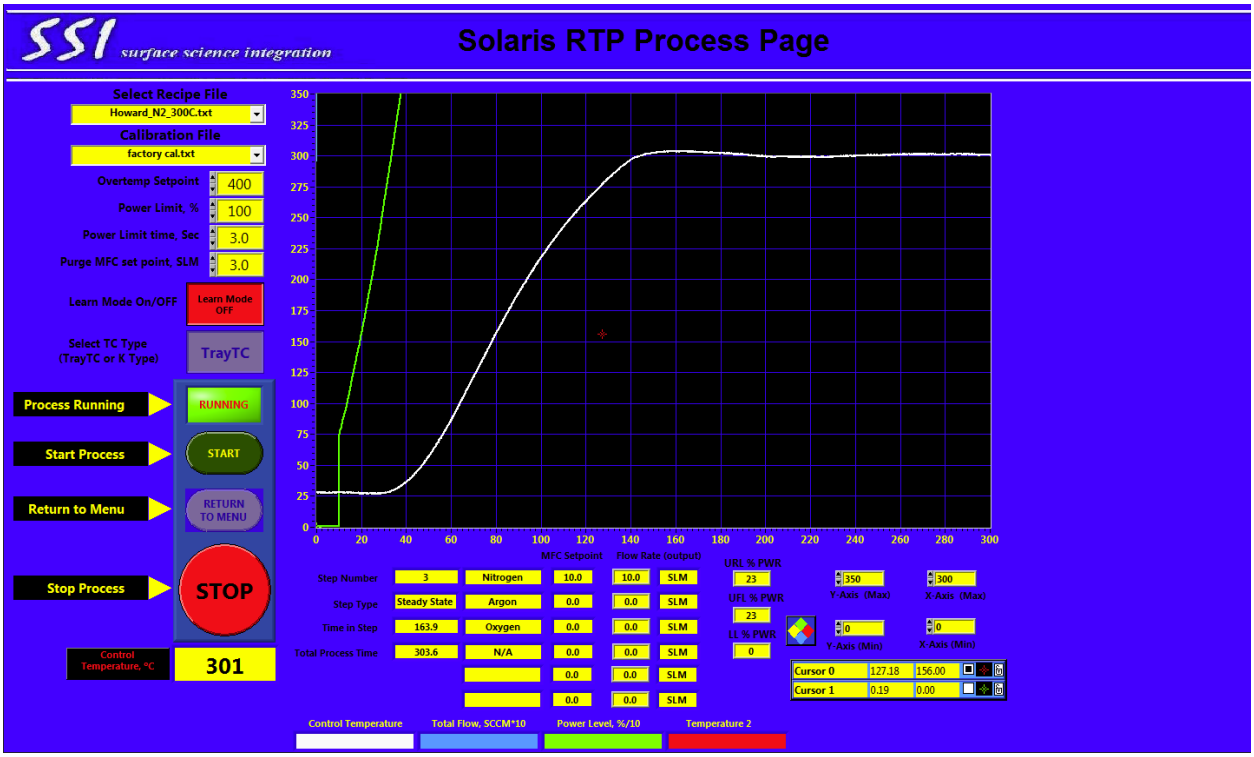

Figure 4.7: RTP temperature monitor for annealing a 200 nm aluminium contact. The system overshoots the desired setpoint of 300 °C by 3 °C, stabilizing at 300°C roughly a minute later.

4.2.2 Titanium Gold Metallization

For the n type silicon contact, a bilayer of titanium and gold was selected. As this contact is made prior to pulsed laser mixing, the thermal budget is high, allowing for titanium's required high temperature anneals. Titanium has excellent adhesion and ohmic contact forming properties, however, it has high electrical resistivity. A thin layer is used to form the initial contact and subsequently capped with a layer of gold.

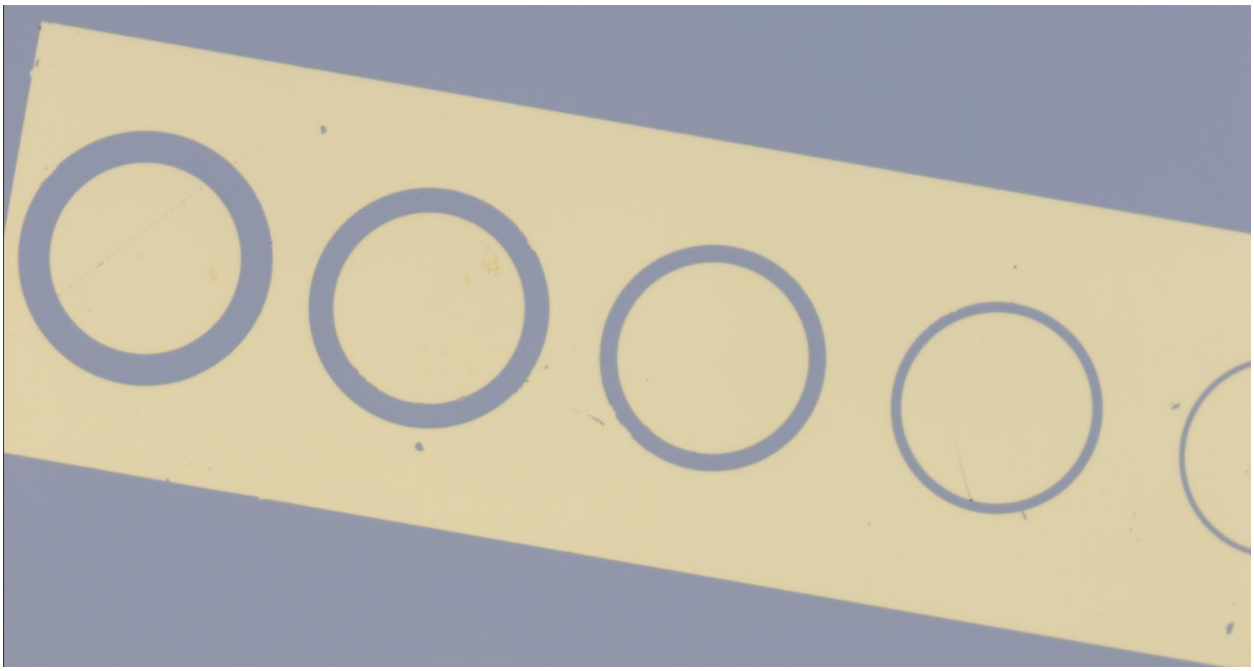

Figure 4.8: Optical microscope image of the 10/50 nm Ti/Au metallization bilayer for 4 probe I-V measurements for TLM. Gap sizes are the same as described in figure 4.6.

Table 4.5: Titanium gold bilayer metallization recipe used for this work.

Metals Used	Titanium / Gold
Metallization Thickness	10/50 nm
Substrate	n-type Silicon
Deposition Process	Electron Beam Evaporation
Anneal Recipe	800 °C, 5 s
Anneal Atmosphere	10 sccm, N_2
Mean Pre-anneal Contact Resistivity	Schottky
Mean Post-anneal Contact Resistivity	5.36×10^{-6} Ω cm^2

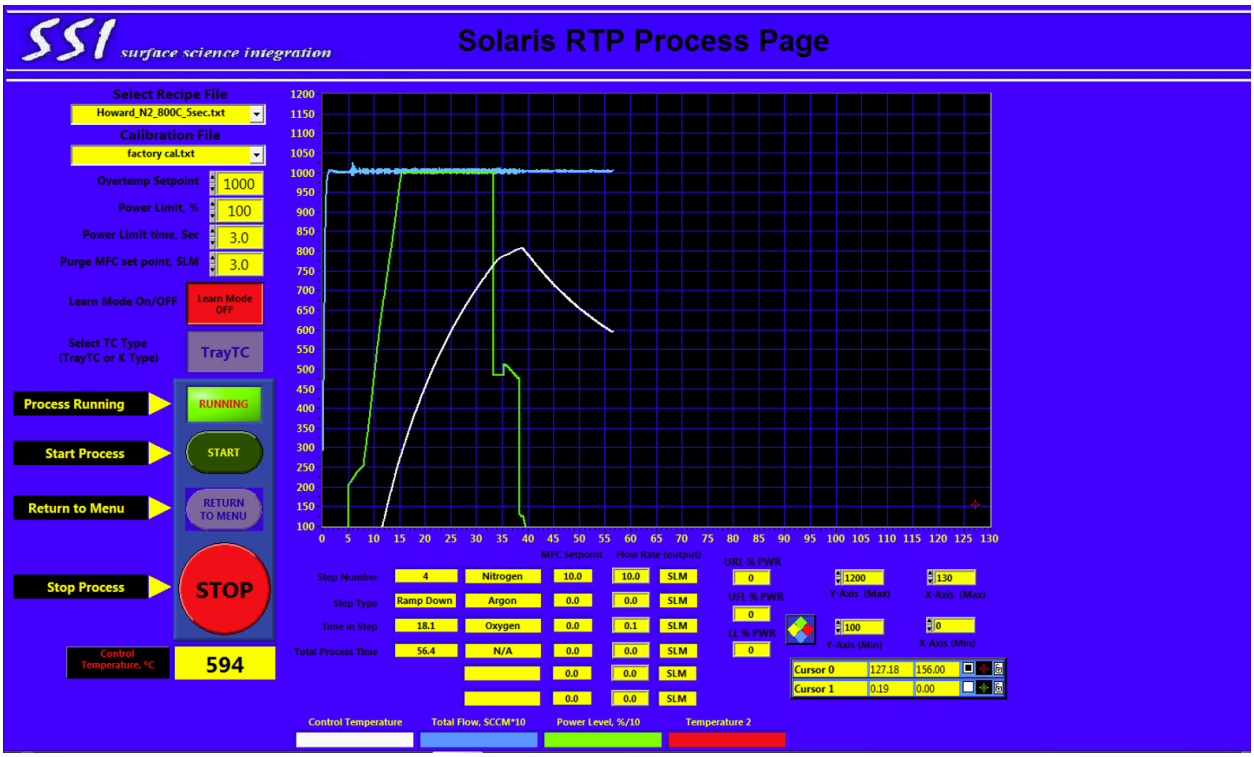

Figure 4.9: RTP temperature monitor for annealing a 10/50 nm Ti/Au contact. Due to the short anneal duration (5 s) and high thermal budget, the overshoot is negligible.

4.2.3 Titanium Copper Metallization

As one of the wafers has p type background doping instead of n type, a low temperature n type contact is needed. A titanium copper bilayer was investigated for this purpose. First, a 10/100 nm of Ti/Cu was made which was not ohmic even with an anneal. I noticed that after the anneal, the current dropped by an order of magnitude for the same voltage range, which is believed to be caused by copper diffusion across the titanium, contaminating the underlying silicon with deep level electronic traps. By increasing the thickness of the titanium to 30 nm, an ohmic contact was made without requiring an anneal. However, upon anneal, the contact loses its ohmic properties.

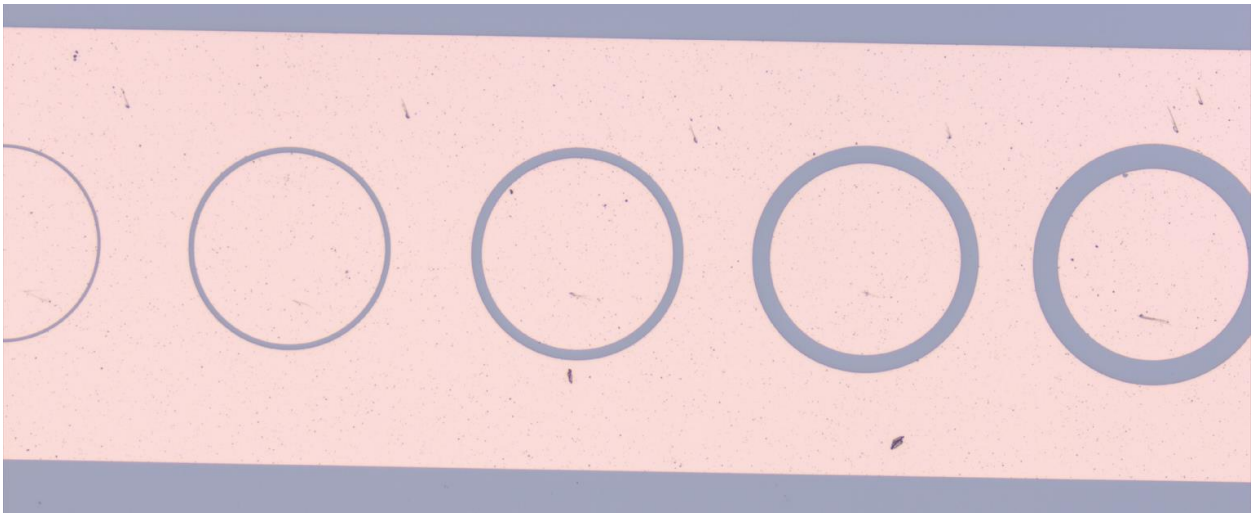

Figure 4.10: Optical microscope image of the 30/100 nm Ti/Cu metallization bilayer for 4 probe I-V measurements for TLM. Gap sizes are the same as described in figure 4.6.

Table 4.6: 10/100 nm titanium copper metallization recipe investigated for a low temperature n type contact.

Metals used	Titanium / Copper
Metallization thickness	10 / 100 nm
Substrate	n-type Silicon
Anneal recipe	300 °C, 2 min
Anneal atmosphere	10 sccm, N_2
Mean pre-anneal contact resistivity	Schottky
Mean post-anneal contact resistivity	Schottky (current decrease by 10x)

Increasing the thickness of the titanium creates an ohmic contact as deposited but loses ohmic properties upon anneal.

Table 4.7: 30/100 nm titanium copper metallization recipe investigated for a low temperature n type contact.

Metals Used	Titanium / Copper
Metallization Thickness	30 / 100 nm
Substrate	n-type Silicon
Anneal Recipe	300 °C, 2 min
Anneal Atmosphere	10 sccm, N_2
Mean Pre-anneal Contact Resistivity	8.87 x 10^{-6} Ω cm^2
Mean Post-anneal Contact Resistivity	Schottky

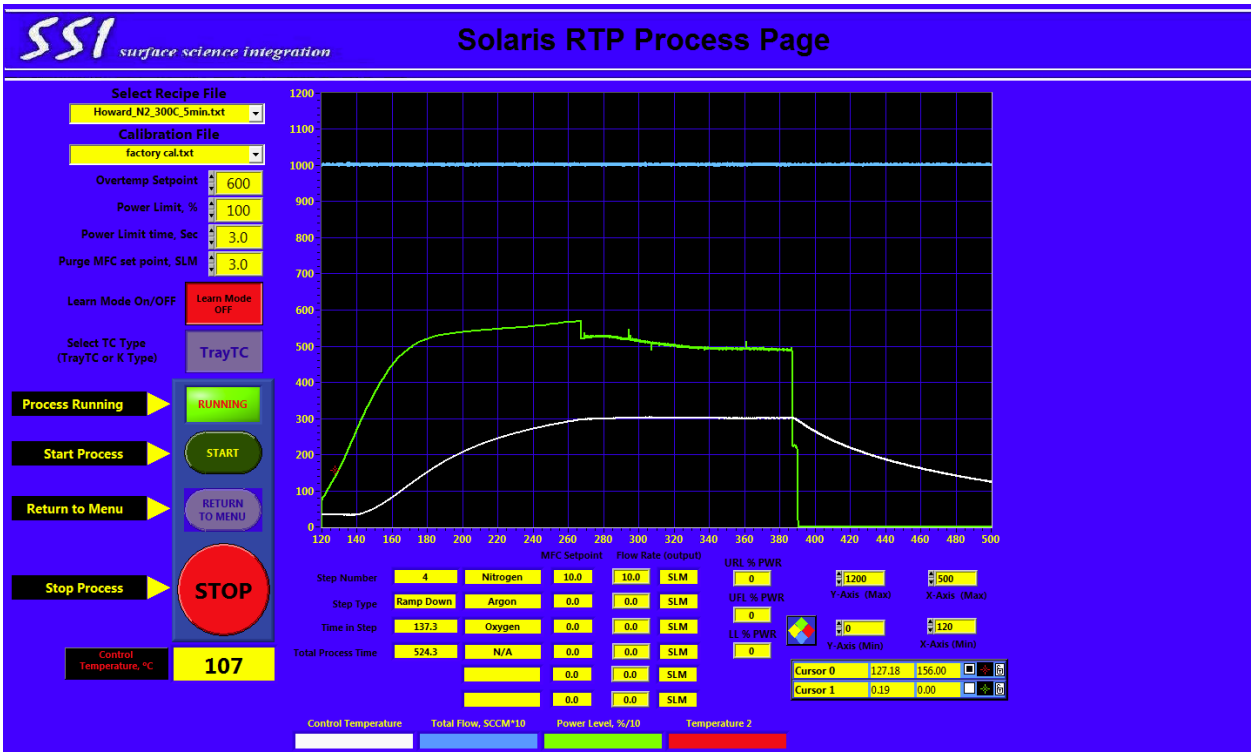

Figure 4.11: RTP temperature monitor for annealing a 30/100 nm Ti/Cu contact.

It's worth noting that Ti/Cu bilayers are used in the modern integrated circuits industry to form chip interconnects. Much previous work has gone into developing effective

adhesion barriers against copper diffusion [69]. However, industrial anneals are short and high temperature; similar to the Ti/Au recipe used. The short duration limits the diffusion of copper, while the high temperature forms a silicide, which pushes the contact deeper into the silicon. Thus, a long, low temperature anneal harms the contact instead of improving it.

4.3 Etch Calibrations

Two etching recipes were used during this work. Etching of silicon oxide was done using 10:1 buffered oxide etch for removing native oxide and creating the hard masks for ion implantation and alignment mark etching. Etching of the underlying silicon was done using 49% aqueous potassium hydroxide solution (KOH) for creating the alignment marks. As wet etches can exhibit huge variations, they were calibrated before beginning the process flow. All etches were done at room temperature (300K).

4.3.1 Wet Etching of Silicon Dioxide

Thermal oxidation is a common process for generating a thin film of silicon oxide on top of wafers. This layer of silicon dioxide is useful as a hard masking material for aggressive processes such as ion implantation or alignment mark etching, which are generally the first steps of any process flow. However, the process is chemically messy, which means that the etch rate can be highly variable. Thus, it is required to determine the etch rate for the current environment beforehand.

Average etch rate was determined by soaking multiple samples from the same source for varying amounts of time. Initial and final oxide thicknesses were determined using ellipsometry.

I had the privilege to visiting the National Cheung Kung University's Academy of Innovative Semiconductor and Sustainable Manufacturing (NCKU AISSM) in Tainan, Taiwan for their semiconductor summer school during my masters. I was able to witness thermal oxidation of a 100 mm silicon wafer firsthand, which I subsequently received as a gift. This wafer was used to help with etch calibrations for this work.

Table 4.8: Etch rates of thermal oxide using 10:1 BOE, by wafer source.

Commercial Retailer	Etch Rate
University Wafer	0.9 nm/s
Nova Electronic Materials	0.8 nm/s
NCKU AISSM	6 nm/s

University Wafer and Nova Electronic Materials are based in the United States, so their thermal oxidation processes are likely similar. The etch rate was significantly greater on the thermal oxide from Taiwan, likely due to the difference in processing equipment.

4.3.2 Wet Etching of Silicon

Strong alkaline solutions such as KOH are known to etch silicon anisotropically along the (111) plane. Etch rates are slow at room temperature but can etch micrometers per minute when heated, which is often used for creating cavities for MEMS devices. However, as the intended purpose of this etch is not depth but rather visibility, room temperature KOH was used to reduce the complexity and hazard of the process.

The gift wafer I received was used to calibrate the KOH etch as well. The surface crystal orientation of the wafer was discovered to be (111), which means the KOH etch rate will be low relative to the (100) wafers.

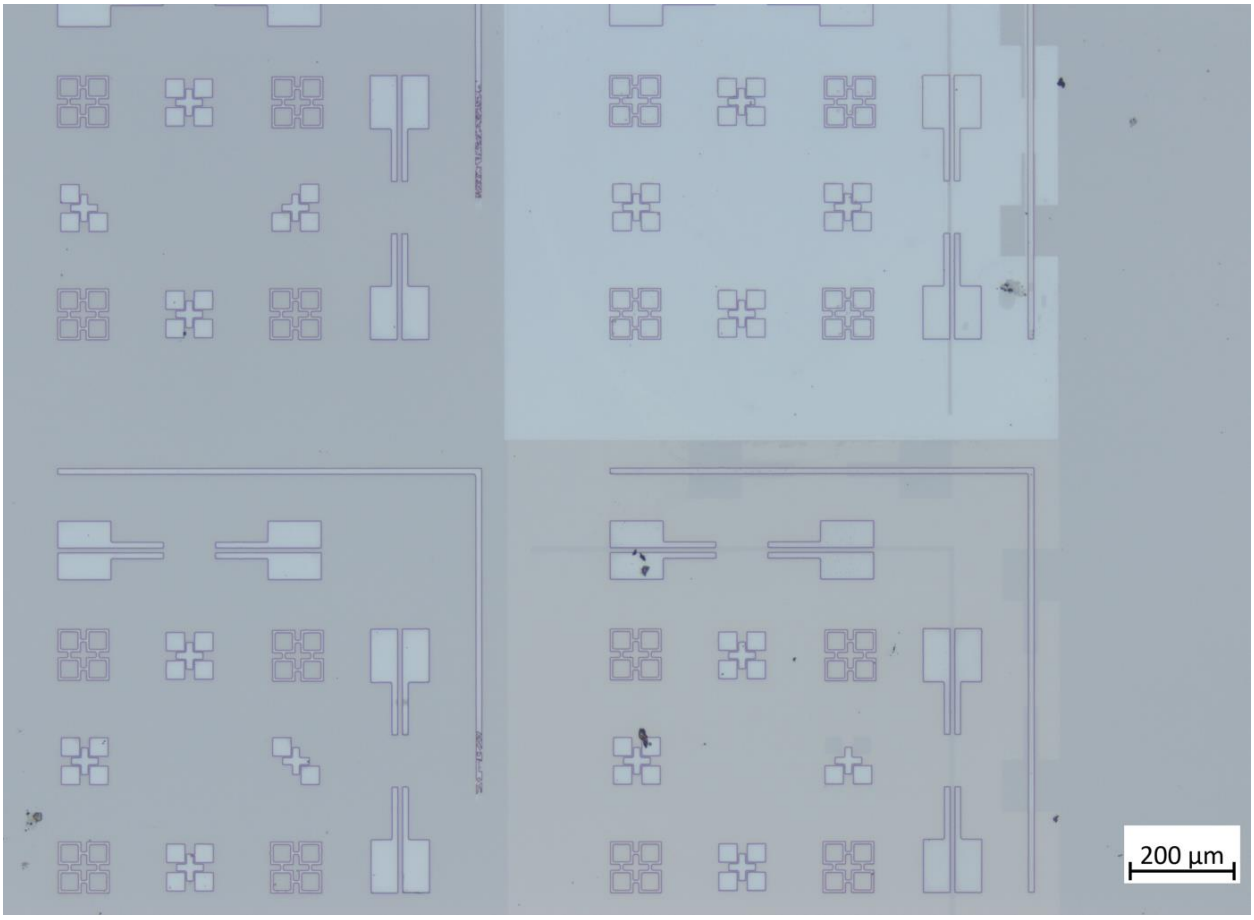

Figure 4.12: Optical microscope image of an alignment mark set used for this work. Two of the alignment marks have already been used for ion implantation (top right) and 1 nm gold thin film deposition (bottom right).

Table 4.9: Room temperature KOH etch rates on silicon with varying crystal orientation.

Surface Crystal Orientation	KOH Etch Rate (300K)
(100)	10 nm/s
(111)	2.5 nm/s

4.4 I-V Measurement Testbench

To verify that the process flow was properly conducted, characterization of the fabricated photodetectors was performed using a 1310 nm laser. I-V curves were measured using a four-probe measurement at the SUNLAB:

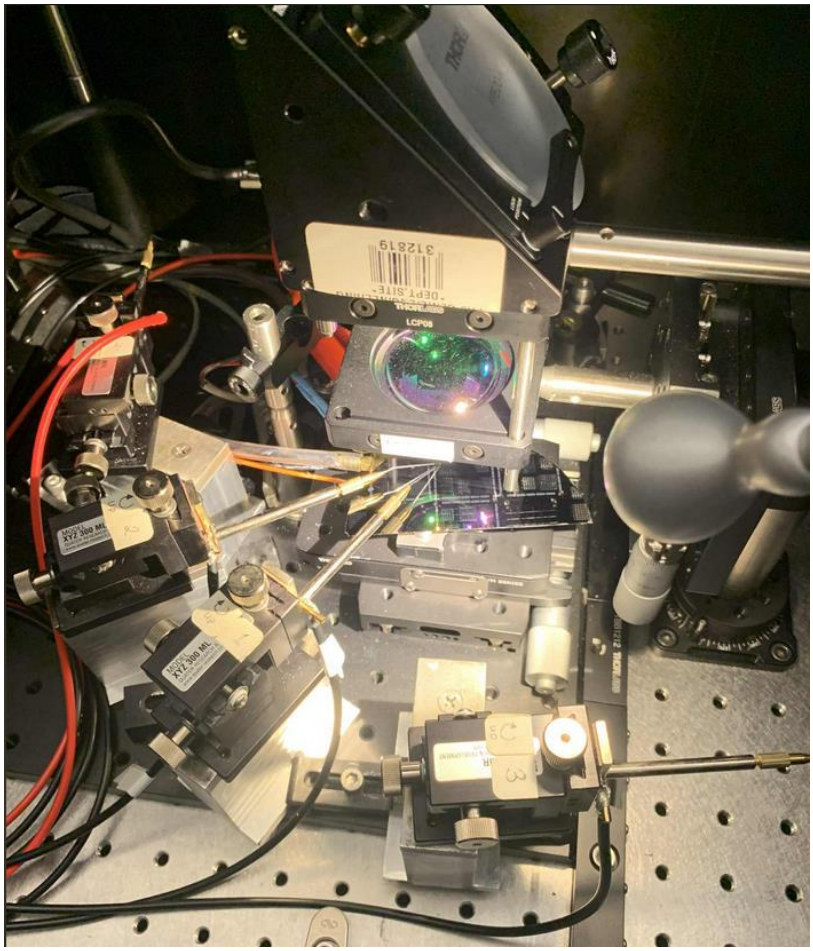

Figure 4.13: Measurement setup used to characterize the fabricated gold hyperdoped silicon photodetectors. This is the PPC station at the University of Ottawa's SUNLAB.

Figure 4.13 shows the measurement setup used to obtain the following results. The finished wafer with the gold hyperdoped silicon photodetectors is placed upon a brass sample plate, which provides the positive force and sense contacts. Two probes attached to micromanipulators (Quater Research, model XYZ300 ML) are used to contact the top aluminium contacts, which provides the grounded force and sense contacts. A pair of

optical components from ThorLabs (PFE20-M01 gold elliptical mirror, LA-1401-C -NBK7 plano-convex lens) focuses fiber-coupled light from the left onto the sample to a spot size of roughly 1 mm diameter. Not shown in figure 4.13 is an Olympus SZ61 stereo microscope, which is used to guide probe placement by hand on the device's contact pads using the micromanipulators. Finally, lighting for experimental setup is provided by an IKEA NÄVLINGE work lamp.

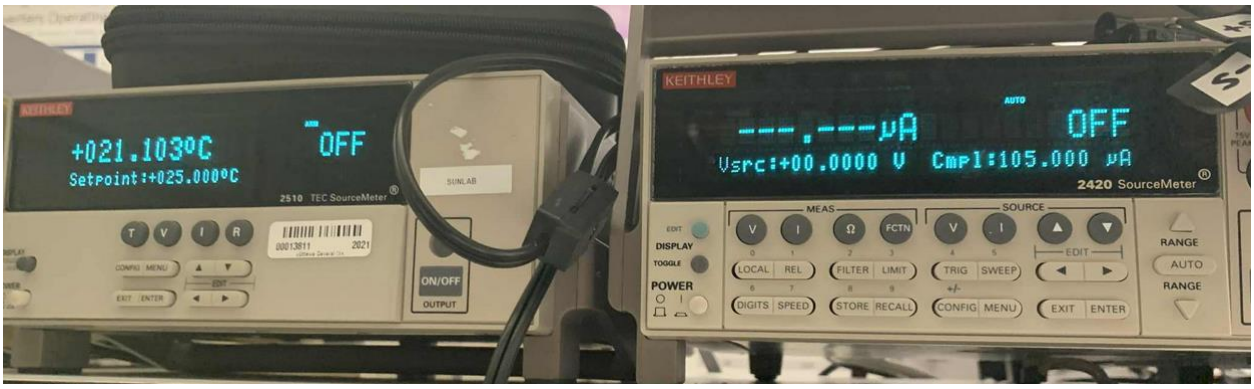

Figure 4.14: Keithley instruments used to characterize the fabricated gold hyperdoped silicon photodetectors. On the left is a 2510 TEC SourceMeter and on the right is a 2420 SourceMeter.

Figure 4.14 shows a pair of instruments from Keithley that were used during characterization. The 2510 TEC SourceMeter is used to control the temperature of the brass sample plate with a setpoint of 25 °C. The 2420 SourceMeter is a 4 wire multimeter used to apply the voltage biases and to measure the resulting current.

Figure 4.15: The 1310 nm laser used to provide the short-wave infrared illumination for characterization of the gold hyperdoped silicon devices.

The 1310 nm illumination was provided by a Dilas diode laser, model M1F4S22-1310.20-14C-SS5.2. Optical output was coupled to an optical fiber, which outputs into the experimental setup shown in figure 4.13. The power output of the laser as a function of laser current is approximately:

$$P_L(I) \approx 0.32(I - 9)$$

where P_L is the laser optical output in watts, and I is the laser diode's input current in amperes. For the following measurements, 12 A of laser current were used, which was measured to provide an optical power of 0.95W over a spot size of roughly 1 mm in diameter.

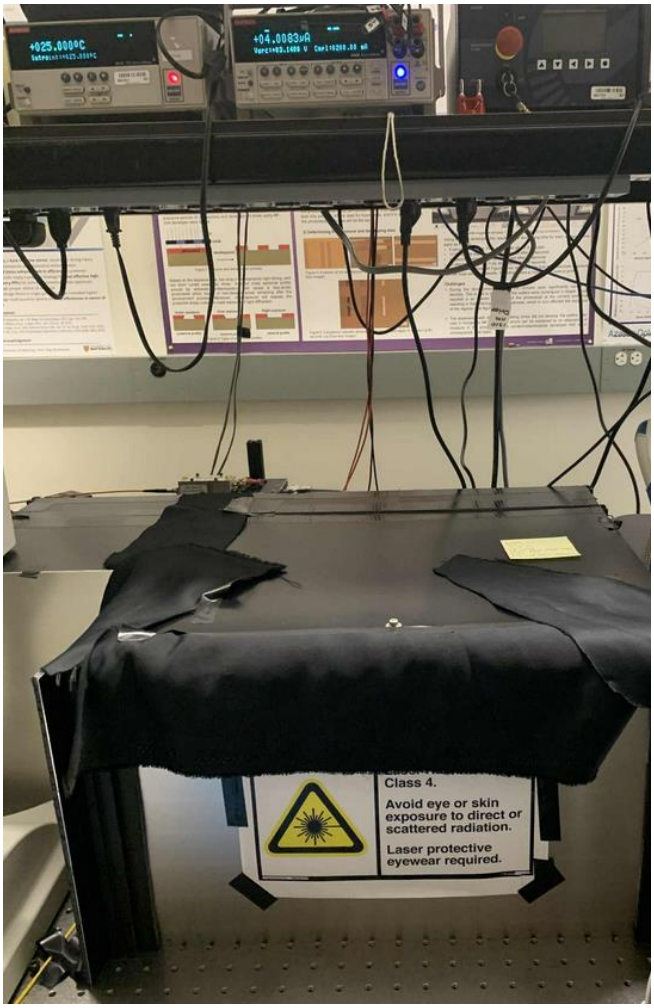

Figure 4.16: Enclosed testbench for both dark and light I-V measurements.

To obtain the following I-V curves, the selected device was contacted using the probes and micromanipulators as described above. Dark current measurements were taken by enclosing the entire testbench in a black box, with dark curtains to close the gaps in the box. This is shown in figure 4.16. I-V measurements were repeatedly taken backwards and forwards from 2 to -5 V of bias until the I-V curve stabilized (minimum of four times). Next, the laser was turned on and the I-V curve measured again from 2 to -5 V of bias. These were done to ensure diode behaviour and to electrically stabilize the device.

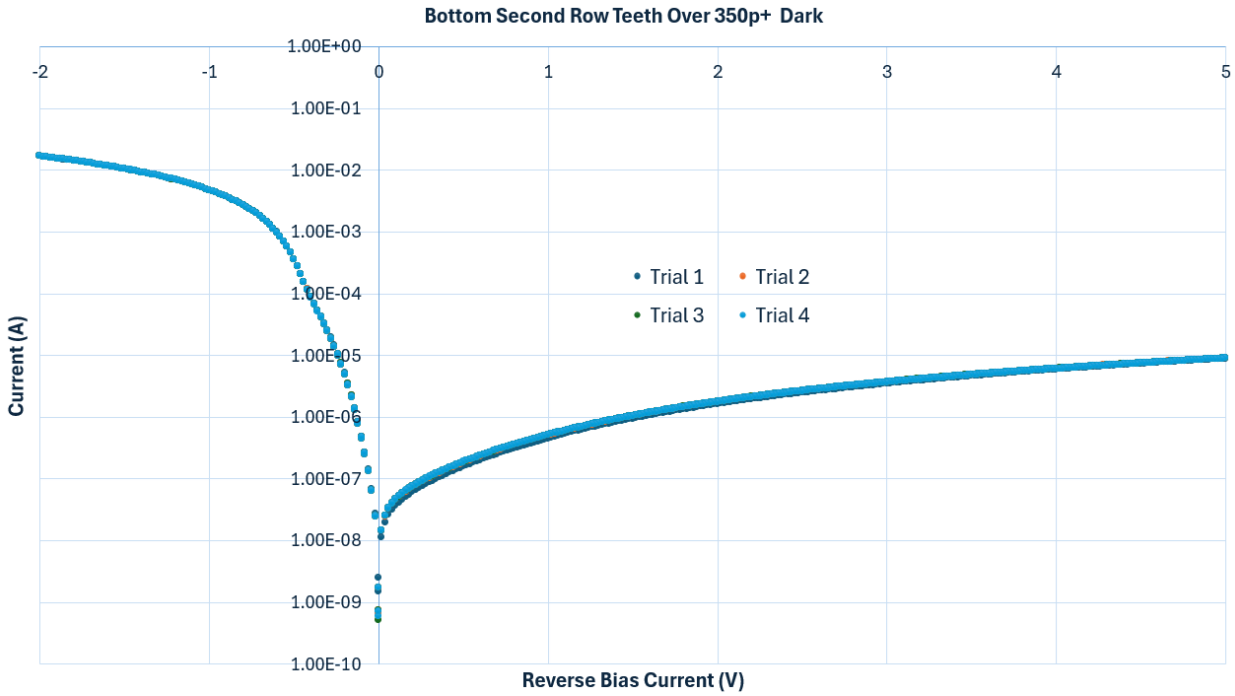

Figure 4.17: Dark current measurement for a device using the teeth design.

The dark current measurement for a teeth design is shown in figure 4.17. Four trials were done in order to stabilize the device. The effect was most prominent at lower reverse bias voltages. Devices were deemed sufficiently stable when a trial differed from the previous trial by less than 5%, on average, for a minimum of 4 trials.

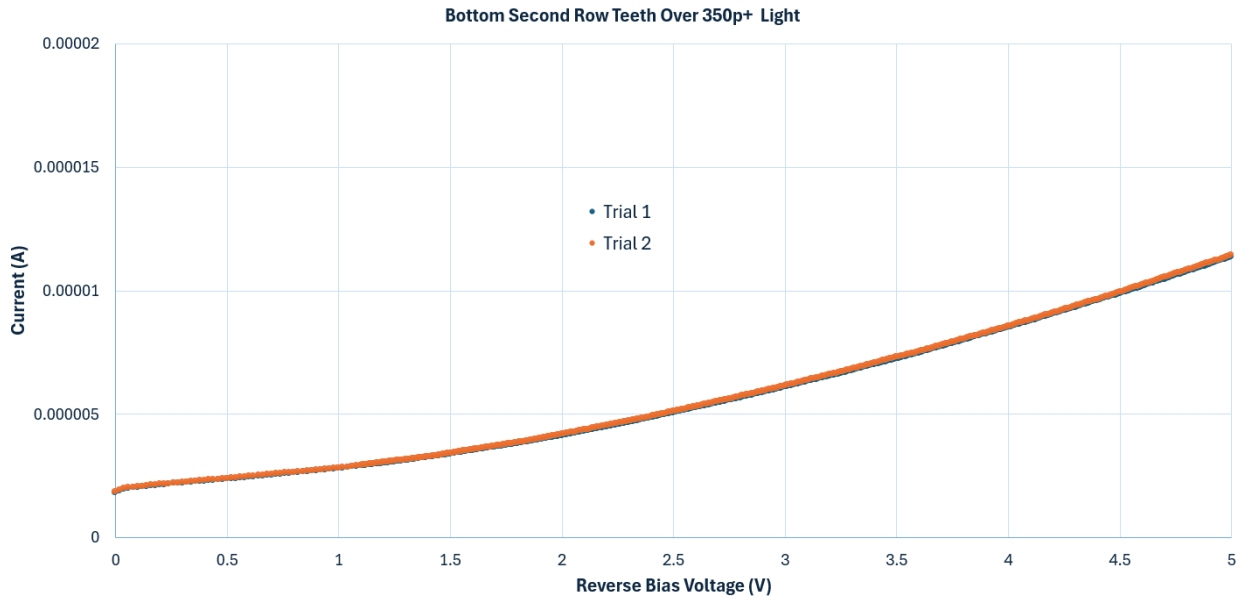

Figure 4.18: I-V measurement of the device in figure 4.17, under 1310 nm laser illumination.

I-V measurements under 1310 nm laser illumination were taken after the device under test was deemed acceptable. Alignment was done using a pilot light prior to the enclosement of the testbench, so the probes and sample were not moved between dark and light measurements. While the voltage bias ranged from 2 to -5 V, figure 4.18 only shows biases from 0 to -5 V to emphasize the operation regime of the device.

While the measured output power of the laser is 0.95 W, not all of the light enters the device. As the device does not have an antireflection coating, roughly 30% of light is reflected from the device. The reflectivity can be determined using:

$$R = \left| \frac{n_1 - n_2}{n_1 + n_2} \right|^2$$

At 1310 nm, silicon has a refractive index of 3.5 [70]. Using a refractive index of 1 for air, a reflectivity of 30.8% can be expected. Furthermore, as the spot size of the laser is larger than the photoactive areas of each device, not all the light will enter a photoactive area. This is complicated by the fact that each device has a differently sized photoactive area.

For the purposes of estimating a responsivity, I will assume that the entire power of the laser is uniformly distributed across the 1 mm spot size, which gives an intensity of 1.21 W/mm^2. This is multiplied by the area of the gold hyperdoped area to estimate the total optical power incident on each device. The photogenerated current is subsequently calculated using the difference between the dark and light currents at -5 V of reverse bias.

Table 4.10: Characterization results of light and dark I-V measurements for a variety of device layouts. The best performing layout is bolded.

	Dark Current at -5 V (A)	Light Current at -5V (A)	Photocurrent (A)	Photoactive area / Incident optical power	Responsivity (A/W)
Teeth – Over 350 p+	8.92E-6	1.14E-5	2.49E-6	0.28 mm2 / 0.2372 W	1.05E-5
Teeth – -4 µm 350 p+	**4.32E-6**	**2.30E-5**	**1.87E-5**	**0.1302 mm2 / 0.1106 W**	**1.69E-4**
Teeth – +2 µm 350 p+	2.54E-5	3.63E-5	1.09E-5	0.1764 mm2 / 0.1491 W	7.3E-5
Teeth – Over 300 p+	0.000283	0.000284	1.0E-6	0.28 mm2 / 0.2372 W	4.21E-6
Corner – 200Au 350p+	0.001417	0.001416	-1.0E-6	0.04 mm2 / 0.0332 W	0
Corner – 200Au 250p+	5.96E-5	6.24E-5	2.76E-6	0.04 mm2 / 0.0332 W	8.14E-5
Busbar – REF 250p+	3.39E-5	3.50E-5	1.13E-6	0 / 0	0
Busbar – 300Au 250p+	0.001033	0.001031	-2.508E-6	0.21 mm2 / 0.1779 W	0

Table 4.10 summarizes the characterization results for a representative sample of each device layout format. The best performing layout is the teeth design with 4 µm of separation between the p+ conductive “highways” and the photoactive gold hyperdoped silicon. This suggests that mixing p dopant and gold has a negative impact on device performance, and that interdigitated structures are effective for improving the performance

of gold hyperdoped silicon photodetectors. The next best performing device is the corner design with a 200 μm gold square inside a 250 μm thick square ring of p+ silicon. However, the responsivity of this device could be skewed by the small photoactive area, which leads to a small denominator for the responsivity calculation.

Furthermore, the presence of negative photocurrents and a positive photocurrent in the reference device suggests that noise is an issue. The laser powers used are expected to heat up the device under test, which increases the amount of thermally generated noise. From the negative current results shown in table 4.10, I will estimate this noise floor to be on the order of microamperes.

4.4.5 Shunted Devices

Some of the devices were shunted, meaning that their dark I-V curves were linear rather than diode-like. They arise due to an unwanted electrical connection between the front and back contacts of the device, which bypasses the diode and renders it optically inactive. Shunts are caused by errors in the process flow or defects in the wafer. Previously shown I-V measurements in section 4.3.4 removed the forwards bias I-V curve to focus on the effects of infrared illumination, however some devices were linear over positive and negative voltages:

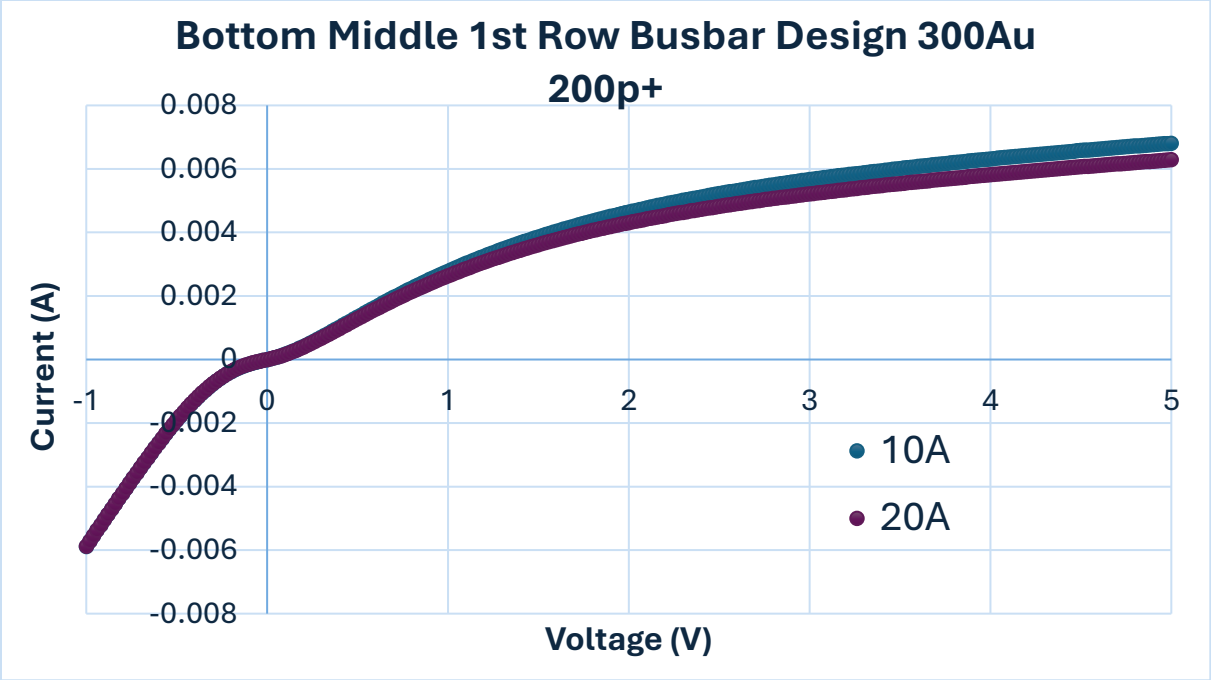

Figure 4.19: A shunted device. 10 and 20 A of laser current correspond to 0.3 and 3.3 W of laser power, respectively.

Figure 4.19 shows the I-V results for a shunted device. Due to the shunt, the reverse and forward currents are on the same order of magnitude, instead of the 3 – 4 orders of magnitude difference as shown in the previous chapter. This is usually caused by crystal defects or fabrication imperfections.

Chapter 5 Conclusion and Future Work

During this project, a repeatable, industry compatible process flow was designed, validated, and carried out to produce short wave (1000 – 2500 nm) infrared photodetectors from gold hyperdoped silicon. Short wave infrared light has several applications across the telecommunications, imaging, and defense fields. Photodetectors for these applications require materials with bandgaps smaller than silicon's, such as germanium, InGaAs, or HgCdTe. The rarity of these elements coupled with processing difficulties significantly raises the price of devices derived from them. It is preferable to make devices out of silicon due to its abundance, reliability, and available resources for silicon microfabrication. By introducing an intermediate band in silicon via gold hyperdoping, the spectral absorptance of silicon can be extended from 1100 to 2500 nm, allowing it to replace the less abundant materials listed above.

Prior work on hyperdoped silicon implanted the hyperdopant via ion implantation. While this is effective at producing the concentrations required for intermediate band formation to sufficient depth, the elements used as hyperdopants are forbidden in most ion implanters as they pose a significant contamination hazard. This work deposits the hyperdopant as a thin film via thermal evaporation which is a process compatible with industry. Furthermore, UV photolithography was used for creating patterns, increasing the throughput relative to electron beam lithography. Finally, picosecond pulsed lasers are already in use in the silicon microfabrication industry for the amorphization of crystalline silicon. Extending the pulse time to the nanosecond range would allow the pulsed laser mixing process to be done.

Standard silicon photodetector fabrication heavily emphasizes cleanliness; gold, in particular, is known to significantly decrease charge carrier lifetime [16]. Hyperdoped photodetectors have short carrier lifetimes, which hinders photodetector performance. Device layouts were designed to mitigate this effect by reducing the distance a photoexcited charge carrier needs to travel to leave the high gold doping to create current.

Photodetectors were characterized with EQE and I-V measurements. Reference samples without any gold but otherwise identical were characterized as well.

Devices were fabricated on four wafers with varying amounts of background doping. These include two lightly doped n type (1 – 10 Ω cm, phosphorous) wafers, one heavily doped n type (0.01 – 0.02 Ω cm, antimony) wafer, and one heavily doped p type (0.01 – 0.02 Ω cm, boron) wafer. Typical photodetector fabrication uses lightly doped n type silicon substrate combined with a strongly doped *p*+ emitter to create a large depletion (photoactive) region in the substrate, mitigating silicon's poor absorption coefficient. Since the photoactive volume for a hyperdoped photodetector is independent of the geometry of the PN diode, a strong built-in electric field in the hyperdoped region would be beneficial for efficiently separating photogenerated charges. Simulations show that increasing the substrate background doping achieves this by reducing the width of the depletion region.

I performed much work validating the processes to be used for this process flow, such as the metallization, etching, and ion implantation recipes. These recipes were designed with gold hyperdoped silicon in mind but are universally applicable to silicon microfabrication process flow. I also performed the EQE and I-V measurements myself, along with dicing needed to remove samples.

Future work could involve inverted photodetector designs. As the photoactive area is not determined by the PN diode, it may be possible to remove it completely and directly attach the hyperdoped area to a contact. Since gold is a dopant compensator, the hyperdoped area would act as a depletion region. Charge separation can be achieved by applying a reverse bias. Such a design would minimize the distance travelled by a photoexcited carrier before collection, mitigating the main issue of hyperdoped silicon. Similar structures have been achieved using a transparent graphene layer as the contact material, however graphene is not a standard material for the semiconductor industry. As ordinary silicon is transparent in the short infrared, it may be possible for the optical input to be on the other side of the wafer.

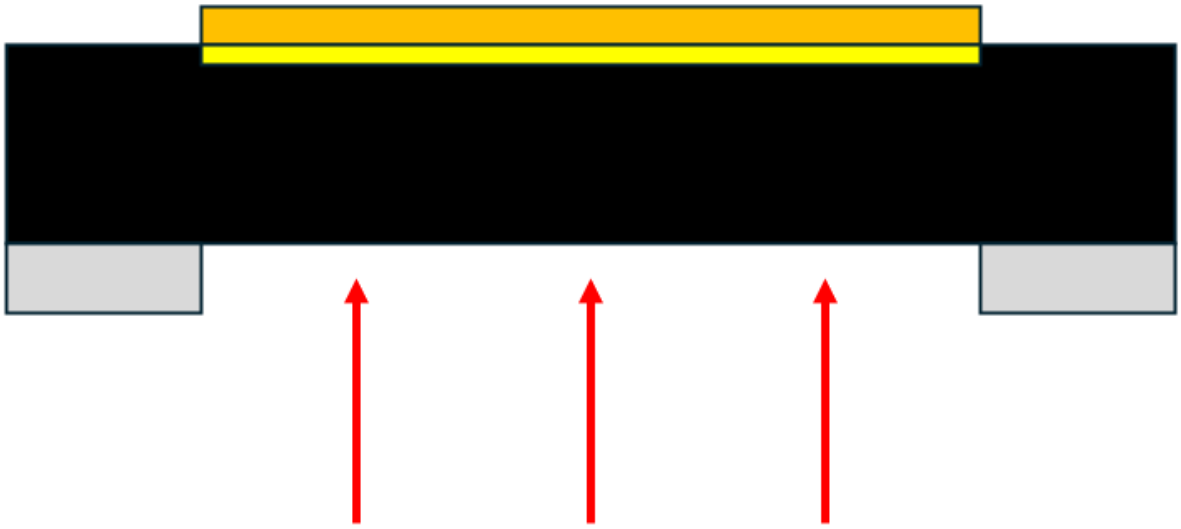

Figure 5.1: Proposed inverted photodetector design using gold hyperdoped silicon.

A new photodetector design is suggested in figure 5.1. By placing a contact directly on top of the gold hyperdoped silicon, the travel distance for a photoexcited carrier is minimized. Infrared light can be inputted through the silicon wafer, as silicon is transparent at these wavelengths. However, such a design would require a mask aligner with front-back alignment capabilities, which would complicate the required process flow. Nevertheless, new device designs are needed to increase the efficiency of devices based on gold hyperdoped silicon.

References

[1] S. Y. Siew *et al.*, "Review of Silicon Photonics Technology and Platform Development," *J. Lightwave Technol.*, vol. 39, no. 13, pp. 4374–4389, July 2021, doi: 10.1109/JLT.2021.3066203.

[2] G. Eranna, *Crystal Growth and Evaluation of Silicon for VLSI and ULSI*, 0 ed. CRC Press, 2014. doi: 10.1201/b17812.

[3] A. Rogalski, "Infrared Detector Characterization," in *2D Materials for Infrared and Terahertz Detectors*, 1st ed., CRC Press.

[4] D. Recht *et al.*, "Supersaturating silicon with transition metals by ion implantation and pulsed laser melting," *Journal of Applied Physics*, vol. 114, no. 12, p. 124903, Sept. 2013, doi: 10.1063/1.4821240.

[5] J. P. Mailoa *et al.*, "Room-temperature sub-band gap optoelectronic response of hyperdoped silicon," *Nat Commun*, vol. 5, no. 1, p. 3011, Jan. 2014, doi: 10.1038/ncomms4011.

[6] Z. Tong, M. Bu, Y. Zhang, D. Yang, and X. Pi, "Hyperdoped silicon: Processing, properties, and devices," *J. Semicond.*, vol. 43, no. 9, p. 093101, Sept. 2022, doi: 10.1088/1674-4926/43/9/093101.

[7] H. Castán *et al.*, "Experimental verification of intermediate band formation on titanium-implanted silicon," *Journal of Applied Physics*, vol. 113, no. 2, p. 024104, Jan. 2013, doi: 10.1063/1.4774241.

[8] H. Jiang *et al.*, "Ultrahigh Photogain Short-Wave Infrared Detectors Enabled by Integrating Graphene and Hyperdoped Silicon," *ACS Nano*, vol. 16, no. 8, pp. 12777–12785, Aug. 2022, doi: 10.1021/acsnano.2c04704.

[9] M. S. Shaikh *et al.*, "A high-performance all-silicon photodetector enabling telecom-wavelength detection at room temperature," Dec. 08, 2024, *arXiv*: arXiv:2412.05872. doi: 10.48550/arXiv.2412.05872.

[10] M. Tabbal, T. Kim, J. M. Warrender, M. J. Aziz, B. L. Cardozo, and R. S. Goldman, "Formation of single crystal sulfur supersaturated silicon based junctions by pulsed laser melting," *Journal of Vacuum Science & Technology B: Microelectronics and*

Nanometer Structures Processing, Measurement, and Phenomena, vol. 25, no. 6, pp. 1847–1852, Nov. 2007, doi: 10.1116/1.2796184.

[11] E. Ertekin *et al.*, "Insulator-to-Metal Transition in Selenium-Hyperdoped Silicon: Observation and Origin," *Phys. Rev. Lett.*, vol. 108, no. 2, p. 026401, Jan. 2012, doi: 10.1103/PhysRevLett.108.026401.

[12] J. W. Barkby *et al.*, "Fabrication of nitrogen-hyperdoped silicon by high-pressure gas immersion excimer laser doping," *Sci Rep*, vol. 14, no. 1, p. 19640, Aug. 2024, doi: 10.1038/s41598-024-69552-8.

[13] PubChem, "Periodic Table of Elements." Accessed: Apr. 25, 2025. [Online]. Available: https://pubchem.ncbi.nlm.nih.gov/periodic-table/

[14] S. Coffa, L. Calcagno, S. U. Campisano, G. Calleri, and G. Ferla, "Control of Minority Carrier Lifetime by Gold Implantation in Semiconductor Devices," *J. Electrochem. Soc.*, vol. 136, no. 7, pp. 2073–2075, July 1989, doi: 10.1149/1.2097180.

[15] W. R. Thurber, D. C. Lewis, and W. M. Bullis, "Resistivity and carrier lifetime in gold-doped silicon," National Bureau of Standards, Gaithersburg, MD, NBS IR 73-128, 1973. doi: 10.6028/NBS.IR.73-128.

[16] S. S. Dissanayake *et al.*, "Carrier lifetimes in gold–hyperdoped silicon—Influence of dopant incorporation methods and concentration profiles," *APL Materials*, vol. 10, no. 11, p. 111106, Nov. 2022, doi: 10.1063/5.0126461.

[17] M. Garcia-Lechuga *et al.*, "Amorphization and Ablation of Crystalline Silicon Using Ultrafast Lasers: Dependencies on the Pulse Duration and Irradiation Wavelength," *Laser & Photonics Reviews*, vol. 18, no. 11, p. 2301327, Nov. 2024, doi: 10.1002/lpor.202301327.

[18] C. Hu, *Modern semiconductor devices for integrated circuits*. Upper Saddle River, N.J: Prentice Hall, 2010.

[19] A. Karoui and A. Kechiantz, "Quantum Mechanics Design of Two Photon Processes Based Solar Cells," in *Some Applications of Quantum Mechanics*, M. R. Pahlavani, Ed., InTech, 2012. doi: 10.5772/33401.

[20] L.-D. Yuan, H.-X. Deng, S.-S. Li, S.-H. Wei, and J.-W. Luo, “Unified theory of direct or indirect band-gap nature of conventional semiconductors,” *Phys. Rev. B*, vol. 98, no. 24, p. 245203, Dec. 2018, doi: 10.1103/PhysRevB.98.245203.

[21] V. Chmill, “Radiation Tests of Semiconductor Detectors”.

[22] W. Shockley and W. T. Read, “Statistics of the Recombinations of Holes and Electrons,” *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sept. 1952, doi: 10.1103/PhysRev.87.835.

[23] A. Cuevas and D. Macdonald, “Measuring and interpreting the lifetime of silicon wafers,” *Solar Energy*, vol. 76, no. 1–3, pp. 255–262, Jan. 2004, doi: 10.1016/j.solener.2003.07.033.

[24] S. O. Kasap, *Principles of electronic materials and devices*, Fourth edition. New York, NY: McGraw-Hill, a business unit of The McGraw-Hill Companies, Inc, 2018.

[25] Z. Bielecki, K. Achtenberg, M. Kopytko, J. Mikołajczyk, J. Wojtas, and A. Rogalski, “Review of photodetectors characterization methods,” *Bulletin of the Polish Academy of Sciences Technical Sciences*, pp. 140534–140534, Feb. 2022, doi: 10.24425/bpasts.2022.140534.

[26] F. A. Trumbore, “Solid Solubilities of Impurity Elements in Germanium and Silicon*,” *Bell System Technical Journal*, vol. 39, no. 1, pp. 205–233, Jan. 1960, doi: 10.1002/j.1538-7305.1960.tb03928.x.

[27] G. L. Vick and K. M. Whittle, “Solid Solubility and Diffusion Coefficients of Boron in Silicon,” *J. Electrochem. Soc.*, vol. 116, no. 8, p. 1142, 1969, doi: 10.1149/1.2412239.

[28] M. Rüdiger, M. Rauer, C. Schmiga, M. Hermle, and S. W. Glunz, “Accurate modeling of aluminum-doped silicon,” *Energy Procedia*, vol. 8, pp. 527–532, 2011, doi: 10.1016/j.egypro.2011.06.177.

[29] L. A. Berthoud, “On the alloying of aluminium to silicon in the fabrication of integrated circuits,” *Microelectronics Reliability*, vol. 16, no. 2, pp. 165–171, Jan. 1977, doi: 10.1016/0026-2714(77)90419-X.

[30] E. R. Weber, “Transition metals in silicon”.

[31] K. Tang, E. J. Øvrelid, G. Tranell, and M. Tangstad, “Critical assessment of the impurity diffusivities in solid and liquid silicon,” *JOM*, vol. 61, no. 11, pp. 49–55, Nov. 2009, doi: 10.1007/s11837-009-0167-7.

[32] W. Yang *et al.*, “Au-rich filamentary behavior and associated subband gap optical absorption in hyperdoped Si,” *Phys. Rev. Materials*, vol. 1, no. 7, p. 074602, Dec. 2017, doi: 10.1103/PhysRevMaterials.1.074602.

[33] C. B. Collins, R. O. Carlson, and C. J. Gallagher, “Properties of Gold-Doped Silicon,” *Phys. Rev.*, vol. 105, no. 4, pp. 1168–1173, Feb. 1957, doi: 10.1103/PhysRev.105.1168.

[34] S. Q. Lim, J. M. Warrender, C. Notthoff, T. Ratcliff, J. S. Williams, and B. C. Johnson, “Room temperature electrical characteristics of gold-hyperdoped silicon,” *Journal of Applied Physics*, vol. 135, no. 9, p. 095704, Mar. 2024, doi: 10.1063/5.0196985.

[35] S. Franssila, *Introduction to Microfabrication*, 1st ed. Wiley, 2010. doi: 10.1002/9781119990413.

[36] D. Basting, *Excimer Laser Technology*. Berlin, Heidelberg: Springer Berlin / Heidelberg, 2005.

[37] O. O. Versolato, “Physics of laser-driven tin plasma sources of EUV radiation for nanolithography,” *Plasma Sources Sci. Technol.*, vol. 28, no. 8, p. 083001, Aug. 2019, doi: 10.1088/1361-6595/ab3302.

[38] J. M. Buriak, “Functionalization of Silicon Surfaces for Device Applications†”.

[39] A. Clarke, K. Hinzer, and M. De Lafontaine, “Review of plasma etching processes for III-V semiconductors.”

[40] M. De Lafontaine *et al.*, “Multijunction solar cell mesa isolation: Correlation between process, morphology and cell performance,” *Solar Energy Materials and Solar Cells*, vol. 239, p. 111643, June 2022, doi: 10.1016/j.solmat.2022.111643.

[41] C. Y. Chang and Y. K. Fang, “SPECIFIC CONTACT RESISTANCE OF METAL-SEMICONDUCTOR BARRIERS”.

[42] J. P. Gambino and E. G. Colgan, “Silicides and ohmic contacts,” *Materials Chemistry and Physics*, vol. 52, no. 2, pp. 99–146, Feb. 1998, doi: 10.1016/S0254-0584(98)80014-X.

[43] D. Levy, J. P. Ponpon, A. Grob, J. J. Grob, and R. Stuck, “Rapid thermal annealing and titanium silicide formation,” *Appl. Phys. A*, vol. 38, no. 1, pp. 23–29, Sept. 1985, doi: 10.1007/BF00618722.

[44] F. C. Walsh, “Electrode Reactions in Metal Finishing,” *Transactions of the IMF*, vol. 69, no. 3, pp. 107–110, Jan. 1991, doi: 10.1080/00202967.1991.11870904.

[45] M. F. Stuckings, B. Fischer, G. Giroult, A. Cuevas, M. J. Stocks, and A. W. Blakers, “Gallium Contacts on *p* -type silicon substrates,” *Progress in Photovoltaics*, vol. 9, no. 6, pp. 409–416, Nov. 2001, doi: 10.1002/pip.393.

[46] R. M. Panas and M. L. Culpepper, “Engineering Electrical Interfaces to Silicon via Indium Solder,” *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1977–1983, June 2015, doi: 10.1109/TED.2015.2421413.

[47] J. F. Ziegler, M. D. Ziegler, and J. P. Biersack, “SRIM – The stopping and range of ions in matter (2010),” *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 268, no. 11–12, pp. 1818–1823, June 2010, doi: 10.1016/j.nimb.2010.02.091.

[48] R. A. Levy, *Reduced Thermal Processing for ULSI*. in Nato Science Series B: Ser, no. v. 207. New York, NY: Springer, 1990.

[49] S. Q. Lim and J. S. Williams, “Electrical and Optical Doping of Silicon by Pulsed-Laser Melting,” *Micro*, vol. 2, no. 1, pp. 1–22, Dec. 2021, doi: 10.3390/micro2010001.

[50] J. Henrie, S. Kellis, S. M. Schultz, and A. Hawkins, “Electronic color charts for dielectric films on silicon,” *Opt. Express*, vol. 12, no. 7, p. 1464, Apr. 2004, doi: 10.1364/OPEX.12.001464.

[51] “Profilometry - an overview | ScienceDirect Topics.” Accessed: Apr. 26, 2025. [Online]. Available: https://www.sciencedirect.com/topics/chemical-engineering/profilometry

[52] F. J. Giessibl, “Atomic Resolution of the Silicon (111)-(7×7) Surface by Atomic Force Microscopy,” *Science*, vol. 267, no. 5194, pp. 68–71, Jan. 1995, doi: 10.1126/science.267.5194.68.

[53] G. K. Reeves and H. B. Harrison, “Obtaining the specific contact resistance from transmission line model measurements,” *IEEE Electron Device Lett.*, vol. 3, no. 5, pp. 111–113, May 1982, doi: 10.1109/EDL.1982.25502.

[54] H. Murrmann and D. Widmann, “Current crowding on metal contacts to planar devices,” *IEEE Trans. Electron Devices*, vol. 16, no. 12, pp. 1022–1024, Dec. 1969, doi: 10.1109/T-ED.1969.16904.

[55] J. H. Klootwijk and C. E. Timmering, “Merits and limitations of circular TLM structures for contact resistance determination for novel III-V HBTs,” in *Proceedings of the 2004 International Conference on Microelectronic Test Structures (IEEE Cat. No.04CH37516)*, Awaji Yumebutai, Japan: IEEE, 2004, pp. 247–252. doi: 10.1109/ICMTS.2004.1309489.

[56] Abbe, “*The Relation of Aperture and Power in the Microscope (continued) .**,” *Journal of the Royal Microscopical Society*, vol. 2, no. 4, pp. 460–473, Aug. 1882, doi: 10.1111/j.1365-2818.1882.tb04805.x.

[57] H. Seiler, “Secondary electron emission in the scanning electron microscope,” *Journal of Applied Physics*, vol. 54, no. 11, pp. R1–R18, Nov. 1983, doi: 10.1063/1.332840.

[58] E. H. Hall, “On a New Action of the Magnet on Electric Currents,” *American Journal of Mathematics*, vol. 2, no. 3, p. 287, Sept. 1879, doi: 10.2307/2369245.

[59] S. Kasap, “HALL EFFECT IN SEMICONDUCTORS,” 1990.

[60] R. L. Harrison, C. Granja, and C. Leroy, “Introduction to Monte Carlo Simulation,” presented at the NUCLEAR PHYSICS METHODS AND ACCELERATORS IN BIOLOGY AND MEDICINE: Fifth International Summer School on Nuclear Physics Methods and Accelerators in Biology and Medicine, Bratislava (Slovakia), 2010, pp. 17–21. doi: 10.1063/1.3295638.

[61] C. W. White, “(Invited) Laser Annealing of Semiconductors,” *Jpn. J. Appl. Phys.*, vol. 22, no. S1, p. 191, Jan. 1983, doi: 10.7567/JJAPS.22S1.191.

[62] E. C. Dumitrescu, M. M. Wilkins, and J. J. Krich, “Simudo: a device model for intermediate band materials,” *J Comput Electron*, vol. 19, no. 1, pp. 111–127, Mar. 2020, doi: 10.1007/s10825-019-01414-3.

[63] K. Biswas and S. Kal, “Etch characteristics of KOH, TMAH and dual doped TMAH for bulk micromachining of silicon,” *Microelectronics Journal*, vol. 37, no. 6, pp. 519–525, June 2006, doi: 10.1016/j.mejo.2005.07.012.

[64] J. L. Murray and A. J. McAlister, “The Al-Si (Aluminum-Silicon) system,” *Bulletin of Alloy Phase Diagrams*, vol. 5, no. 1, pp. 74–84, Feb. 1984, doi: 10.1007/BF02868729.

[65] G. M. Von Staszewski and N. E. Walsöe De Reca, “Electromigration mechanism in aluminium conductors,” *Solid-State Electronics*, vol. 23, no. 5, pp. 481–485, May 1980, doi: 10.1016/0038-1101(80)90085-4.

[66] “MEGAPOSIT™ SPR™220 SERIES i-LINE PHOTORESISTS,” DOW Chemical Company, Mar. 2014.

[67] “MEGAPOSITTM SPRTM955-CM SERIES PHOTORESIST,” DOW Chemical Company, Mar. 2014.

[68] “LOR PMGI Datasheet,” Kayaku Advanced Materials, Apr. 2024.

[69] C. Lee and Y.-L. Kuo, “The evolution of diffusion barriers in copper metallization,” *JOM*, vol. 59, no. 1, pp. 44–49, Jan. 2007, doi: 10.1007/s11837-007-0009-4.

[70] M. N. Polyanskiy, “Refractiveindex.info database of optical constants,” *Sci Data*, vol. 11, no. 1, p. 94, Jan. 2024, doi: 10.1038/s41597-023-02898-2.