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Investigation of HBT Preamplification for High Speed Optical Communication Systems

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A Thesis submitted to the Faculty of Graduate Studies and Postdoctoral Studies in partial fulfillment of the requirements for the degree of Doctor of Philosophy, Electrical Engineering

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Abstract

A noise analysis for a Common-Collector-Cascode traveling wave HBT preamplifier is developed, resulting in an expression for the preamplifier's equivalent input noise current density. A photoreceiver, consisting of a P-I-N and GaAs HBT MMIC distributed amplifier, was implemented using Nortel's GaAs HBT (f_T=70GHz) process. The noise performance of the P-I-N preamplifier was predicted based on the noise analysis equations. The P-I-N preamplifier, having a measured bandwidth of 22GHz, displayed a measured average equivalent input noise current density of 24 $pA/\sqrt{Hz}$. Good agreement was obtained between the predicted and measured noise performance. The analysis gives useful insight into the dominant noise contributions of the preamplifier.

An 8-stage HBT distributed amplifier was successfully developed. By considering the various issues involved in its design, a design procedure for monolithic distributed amplifiers is presented. The implementation of the HBT preamplifier is described and its measured results are given. From the excellent agreement between the predicted and measured performance, the design method is considered validated. The successful operation of the distributed amplifier, which provides 15dB gain and 35GHz 3dB bandwidth, fulfills the objective of experimental verification. The implemented photoreceiver is the first to have a P-I-N mounted on the MMIC chip.

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Finally, I wish to thank my husband and my son for their support, patience and understanding.

Acronyms

ATL	artificial transmission line
CCC	Common-Collector-Cascode
CPW	coplanar waveguide
DA	distributed amplifier
EBJ	emitter-base junction
FWHM	full width at half maximum
HBT	Heterojunction Bipolar Transistor
HEMT	high electron mobility transistor
MESFET	metal-semiconductor field-effect transistor
MMIC	monolithic microwave integrated circuit
NRZ	none return to zero
SDH	synchronous digital hierarchy
SLC	single layer capacitor
TRL	transmission line
TWA	traveling-wave amplifier
WDM	wavelength-division multiplexing

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Chapter 1 Introduction

1.1 Motivation

The development of world telephone networks during the twentieth century has led to many advances in the design of electrical communication systems. First, digital techniques replaced analog ones in the communications industry. Second, as the communication speed increases, optical communication systems have evolved rapidly in recent years. Fiber-optic communication systems are light-wave systems that employ optical fibers for information transmission. Optical communication systems use high carrier frequencies (~100THz) in the visible or near-infrared region of the electromagnetic spectrum [1]. Such systems have been deployed worldwide since 1980 and have revolutionized the technology behind telecommunications. Indeed, the optical fiber technology, together with microelectronics, is believed to be a major factor in the advent of the 'information age'. The dominant advantage of the fiber-optic communication system over other communication systems is the high speed. Today, commercial 10Gb/s systems are already available. Because of its high transmission capacity performance, the optical fiber communication system is becoming the backbone of the global communication network.

The growth of new services, such as Internet and multimedia, in information industry is continuously demanding higher capacity. During the 90's, the Internet has entered the mainstream of daily life in the world. New developments at the World Wide Web (WWW) Consortium are going to require more data and make the Web more appealing. The Internet, and above all the WWW, race ahead exponentially, burdening the circuit-switched public voice telephone network and stirring a hunger for fast public data networks. Therefore, the biggest challenge in the telecommunication industry is still to increase data transmission capacity and provide bandwidth on demand.

Increasing transmission capacity for optic systems can be achieved by two methods: transmitting multiple channels through the WDM (wavelength-division multiplexing) technique, or increasing per channel capacity. The channel bandwidth of optical communication systems is larger by a factor of nearly 10,000 than that of microwave systems. Current optic systems operate well below their channel capacity. Considerable increase in the transmission capacity of optic systems is expected to occur through multiple channels transmitted over the same fiber by use of WDM techniques. On other hand, as the semiconductor and microwave technology makes progress, the higher speed platform becomes possible to provide higher capacity for each channel.

High-speed integrated circuits are the key to large-capacity transmission systems. With the advancement of process technologies, research work have been done on high-speed devices with capabilities of 40 Gbit/s-class IC's or higher [2]. Descriptions of very-high-speed optical-communication systems requiring optical receivers operating at 40 Gbit/s have been published [3], [69]-[72]. Since a preamplifier plays an important role in a high-speed optical receiver, there is great interest in developing wideband preamplifiers for 40 Gbit/s receiver systems. Since Heterojunction Bipolar Transistor (HBT) has higher trans-conductance g_m and more uniform threshold voltage, compared to the metal-semiconductor field-effect transistor (MESFET) and high electron mobility transistor (HEMT), HBT monolithic microwave integrated circuit (MMIC) can achieve high per stage gain and direct coupling without use of reactive tuning techniques ---provided circuit operation is well below the device cutoff frequency. Other unique features of HBT are low flicker noise, and superior linearity and dynamic range for applications that require low inter-modulation distortion [4]. Therefore, HBT MMIC distributed amplifiers (DAs) are very attractive for optical communication applications. Actually, HBT distributed amplifiers have been applied to ultra high speed optical receiver systems. While some papers [5]-[8] have been published predicting the signal-noise performance of the MESFET optical distributed amplifiers, there is nothing similar published for the HBT optical DAs. Therefore, it is challenging and attractive to establish low-noise, ultra broadband HBT optical preamplifiers for high-speed receiver systems.

1.2 Objectives

The global objective of this thesis is to investigate design techniques for the HBT preamplifier, and to use these techniques to demonstrate a preamplifier for high-speed optical receivers using GaAs HBT distributed amplifier technology. As an optical receiver, a preamplifier needs to have high trans-impedance gain, very broad bandwidth, low noise, as well as low dispersion. Research towards the realization of preamplifiers involves a multitude of issues. The scope of this work includes theoretic analysis of HBT preamplifiers, the implementation of a HBT distributed amplifier in MMIC form, P-I-N diode characterization, as well as the integration of the preamplifier.

The proposed photoreceiver preamplifier is a combination of a P-I-N diode input with a HBT distributed amplifier. The first objective of this thesis is to define a preamplifier configuration with the new HBT gain cells, which allows high gain and wide bandwidth.

A theoretical analysis is required which adequately describes the behavior of this new preamplifier. Therefore, the second objective is to develop an analytical tool, which allows the design and optimization of HBT preamplifiers (or trans-impedance amplifiers), and the prediction of their performance such as trans-impedance gain, bandwidth, and noise.

A MMIC chip presents unique design challenges at such broad bandwidths and high frequencies. Complicated design approaches are required due to the distributed circuit elements and interconnection parasitics in the layout. To model the circuits more accurately, and predict the circuit performance more precisely, design tools such as EM simulators and circuit simulators are needed. Thus, the third objective of this thesis is to demonstrate a suitable MMIC design procedure by implementing a MMIC distributed amplifier using GaAs HBT process.

In order to predict the performance of the whole preamplifier, the P-I-N diode need to be characterized. Thus, the fourth objective is to investigate the measurement techniques for

the high-speed P-I-N photodetectors, such as optical response and input reflection coefficient measurement, so as to develop suitable modeling method to accurately characterize a P-I-N diode's performance.

To validate the principle of the new HBT preamplifier device, experimental verification must take place. The final objective of this thesis is therefore to fabricate the proposed preamplifier using GaAs HBT process, and practically demonstrate its operating characteristics so that the predicted performance can be confirmed.

1.3 Thesis Organization

Chapter 2 provides the background material for this thesis. Section 2.1 gives a perspective on the development of optical communication system. Section 2.2 presents basic concept of MMIC design, as well as its challenges. Different design techniques for distributed amplifier are reviewed in section 2.3.

Chapter 3 describes the design techniques employed in this thesis to implement HBT preamplifiers. A complete analysis for a HBT distributed amplifier performance is presented in this Chapter, which includes detailed study on gain, bandwidth and noise. First, in section 3.1, a new HBT gain cell configuration, the basic construction unit of a HBT distributed amplifier, is described. Its performance is characterized theoretically in terms of trans-impedance gain, bandwidth, and noise. Then, artificial transmission line model —— the m-derived low pass filter structure, which a DA bases its function on, is investigated in Section 3.2. Other design issues such as P-I-N diode input are discussed in Section 3.3. Finally, the performance of the whole HBT preamplifier is analyzed in Section 3.4 and 3.5.

Chapter 4 presents measurements performed to characterize the performance of a P-I-N diode. It includes input reflection coefficient measurement and optical response measurements for P-I-N diodes. The measurement procedure, measurement results, as

well as the derived model of the P-I-N diodes are presented. It provides both electrical model and optical model for the to-be used P-I-N diode.

Chapter 5 demonstrates the implementation of a P-I-N HBT preamplifier, having a measured bandwidth of 22 GHz and a measured average equivalent input noise current density of $24\, pA/\sqrt{Hz}$. Section 5.1 gives the design procedure for the preamplifier MMIC chip. Circuit design details, simulation results, as well as MMIC chip layout are described in Section5.2. The measurement results are presented in Section 5.3. The measured results are compared with the predicted results to verify the preamplifier design, and to validate the noise analysis.

Chapter 6 summarizes all the thesis work in conclusions. Future work is also suggested in this Chapter.

1.4 Contributions

A low noise P-I-N HBT preamplifier is required for upcoming optical communication systems. The objective of this thesis is to develop a theoretical noise analysis for a proposed HBT preamplifier using HBT distributed amplifier technology, and to implement such a P-I-N preamplifier to validate the noise analysis in this thesis. The main contributions of this work in pursuit of this objective are:

- Investigated HBT gain cell topologies based on loss compensation techniques.
- Developed a theoretical noise analysis for the proposed HBT Common-Collector-Cascode distributed preamplifier.
- Investigated the measurement techniques for high-speed P-I-N diodes.
- Developed a design procedure for MMIC chip.
- Implemented a photoreceiver using a P-I-N and GaAs HBT MMIC distributed amplifier combination, and experimentally verified the operation of the HBT MMIC DA and the overall preamplifier.

Chapter 2 Overview of Microwave Integrated Circuit Amplifiers for Optical Communication Applications

Optical fiber communication systems have evolved tremendously over the last two decades. Fiber-optic communication systems are light-wave systems that employ optical fibers for information transmission. Such systems have been deployed worldwide since 1980 and have indeed revolutionized the technology behind telecommunications. This chapter describes microwave integrated circuit amplifier in the context of modern optical communication system.

2.1 Evolution of Fiber-Optic Communication System

In today's world, optical fiber systems act as the backbone of the global telecommunication system. Together, lasers and optical fibers have dramatically increased the capacity of the international telephone system. With equally striking improvements in computing, the new communication technology has fueled the exponential growth of the phenomenon known as the Internet. Significant expansion of infrastructure data-transmission capacity is still necessary to meet the requirements of the 21st century's Internet's explosive growth.

Today's telecommunication systems can incorporate multiple wavelength channels spaced at 100 GHz (0.8nm) increments that are co-propagating on a single fiber. These multiple wavelength systems are referred to as wavelength division multiplexed (WDM) systems [1]. The data rates used in fiber have dramatically increased. On the electronics side, high-speed integrated circuits are the key to large-capacity transmission systems. The commercial state of the art for high-speed telecommunication systems has pushed

beyond the previous 2.5Gb/s rate to 10 Gb/s. Research efforts are focusing on the development of very-high-speed optical-communication systems requiring optical receivers operating at 40-100 Gbit/s. With the advancement of IC process technologies, it becomes possible to fabricate high-speed devices with capabilities of 40 Gbit/s or higher.

In optical transmission, the required maximum frequency of a base-band signal is determined by the bit rate of the data stream. It has been estimated that a bandwidth of at least 70% of the rate frequency is needed to equalize NRZ (None Return to Zero) signals [9]. This means that a bandwidth upper limit of more than 30 GHz is required for 40Gbit/s transmissions. On the other hand, the lower limit is determined by the section length in the stream, as well as many other factors such as the roll off characteristics of the amplifier, the performance of the dc regeneration circuit, and the sensitivity of the subsequent decision circuit. Overall, for 40Gbit/s transmission, the required lower frequency limit could be much less than 1 GHz [9]. Therefore, the required bandwidth of an optical preamplifier is extremely broad, making its design very challenging.

Figure 2-1 illustrates the block diagram of a direct detection digital light-wave receiver, in which the gain block placed before the linear channel amplifier is called "preamplifier". Distributed amplifier MMIC structures are attractive for use as preamplifiers for optical receiver applications operating in the Gig-bits region because of their potential to broaden the bandwidth and decrease noise [7]. High-speed optical receivers have been fabricated by using P-I-N diode and distributed amplifier combinations [5]-[8], [10]-[12], the equivalent circuit of which is shown in Figure 2-2.

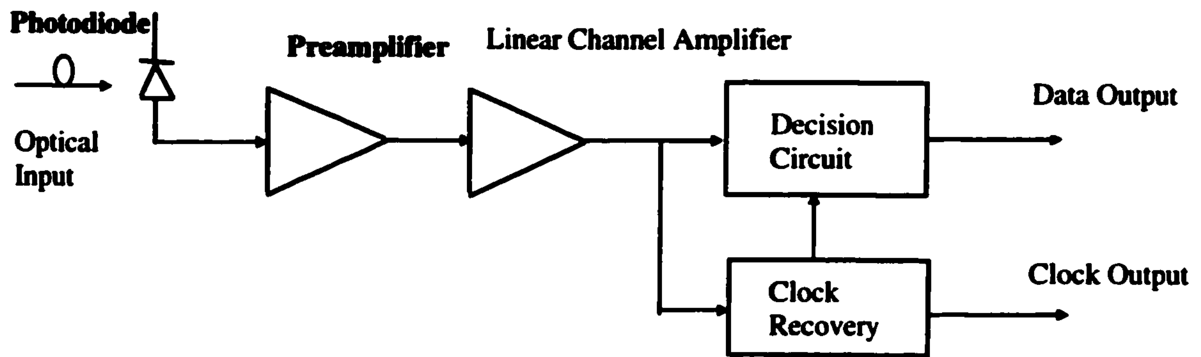


Figure 2-1 Block Diagram of Direct Detection Digital Light-wave Receiver

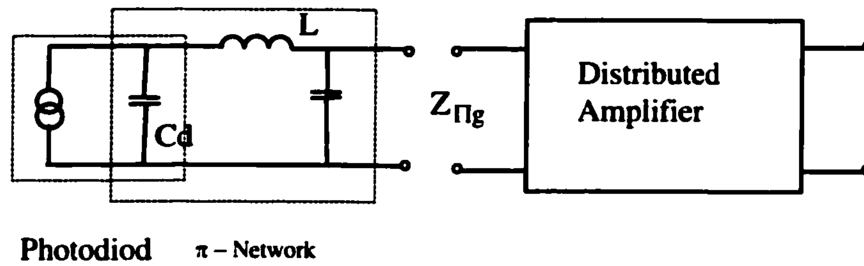


Figure 2-2 Preamplifier — distributed amplifier with unmatched P-I-N diode

2.2 MMIC Technology

Monolithic Microwave Integrated Circuits (MMICs) are integrated circuits that support components such as transmission lines, resistors, capacitors, inductors, field-effect or bipolar transistors and diodes of various types all on a single chip measuring a few millimeters per side at most [13]. MMIC circuits are a very important class of circuit that has grown swiftly in popularity in recent years. These circuits pose some unique design challenges in terms of economics, design precision, and manufacturing yield. MMIC requires a very complicated design process, because of following reasons [14]: (a) Many layout "parasitic" elements complicate the circuit's basic topology; (b) The active devices are not completely reproducible and vary with a degree of randomness from circuit to circuit; (c) Circuit elements at microwave frequencies are distributed by nature, and care must be taken to consider the "distributed" aspect of many so-called lumped elements. The predicted performance of a circuit is only as accurate as the model used to make the prediction. Further more, modeling in the world of microwave circuits is a very complicated process (and a fine art), which often involves exacting measurements as well as applying appropriate simplifying assumptions. Because MMIC circuits cannot be experimentally modified, their calculated performance must be extremely accurate and, at the same time, forgiving enough to deliver the specified performance despite process variations of certain key device parameters. MMIC design requires very special strategies that combine the best modeling and layout techniques with a statistically based yield analysis.

The heterojunction bipolar transistor (HBT) is a modified bipolar transistor that relies on the use of hetero-junctions for its operation [15]. In the HBT, the emitter and base are formed in a semiconductor with different band gaps. The emitter is in the wider band gap material. Parasitic resistance and capacitances in the HBT can be significantly lower than those in its silicon counterpart, which results in improvements of high frequency performance. HBTs with f_T, $f_{max} \approx$ 100 GHz-200 GHz have been used in the MMIC design [16]-[18]. Such bipolar devices have several performance features that are different from both MESFET and HEMT. HBT MMIC circuit architectures can be very

different, achieving high gain per stage and direct coupling without use of reactive tuning techniques due to transistor's excellent threshold voltage uniformity---provided circuit operation is well below the device cutoff frequency. Other unique features of HBT are low flicker noise, and superior linearity and dynamic range for applications that require low inter-modulation distortion [4]. Compared to the MESFET and HEMT, the GaAs HBT as a vertical bipolar device is not particularly suited for low-white-noise application. However, the HBT has higher trans-conductance g_m and lower (CE) output conductance g_o, compared to FETs.

Figure 2-3 shows a simplified model of a HBT device including noise sources [19]. Two correlated current noise sources are related to shot noise at the two junctions, and the thermal noise sources are associated with parasitic series resistances of the HBT. The base resistor r_b provide thermal noise according to the well known Nyquist relation. i_1 and i_2 represent the input and output current noise sources of the intrinsic device, respectively. The current noise source i_1 is related to the shot noise at the emitter-base (EB) junction due to electrons that recombine with holes inside the neutral base and to a lesser extent to holes injected into the emitter. The current noise source i_2 represents the shot noise generated at the collector-base (CE) junction due to collected electrons. These noise sources are characterized by their mean quadratic value in a bandwidth Δf centered on frequency f.

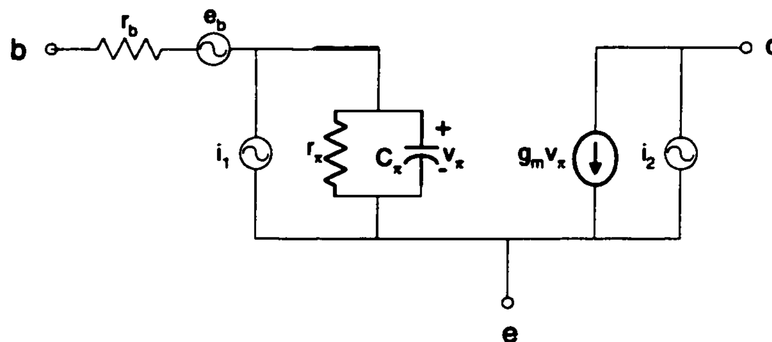


Figure 2-3 Noise model of a HBT device

Noise current densities for noise source i_1 and i_2 are given by equation (2–1) and (2–2) [19]:

$$\overline{i_1^{\ 2}} = 2qI_b = 2kTn_b g_\pi \qquad (2\text{–}1)$$

$$\overline{i_2^{\ 2}} = 2qI_c = 2kTn_c g_m \qquad (2\text{–}2)$$

$$\overline{i_1 \cdot i_2} = 2\frac{\beta}{\beta+1}q(I_b + I_c)e^{-j\omega\tau} - 2qI_c = 2kTg_m(n_e e^{-j\omega\tau} - n_c) \qquad (2\text{–}3)$$

The value of n_e being very close to the value of n_c and neglecting the time delay τ between base and collector, the correlation between i_1 and i_2 can then be neglected, too. Noise voltage density for noise source e_b is given by

$$\overline{e_b^{\ 2}} = 4kT \cdot r_b \qquad (2\text{–}4)$$

The collector current i_C of a HBT transistor is given by

$$i_C = I_S e^{v_{BE}/V_T}$$

The HBT device's parameter varies with geometry scaling of the device. The saturation current I_S is directly proportional to a transistor's EBJ (Emitter-Base Junction) area (that is, the device size), which is also referred to as the current scale factor. Two transistors that are identical except that one has an EBJ area twice that of the other will have saturation currents with a ration of 2. Thus for the same value of v_{BE}, the larger device will have a collector current twice that in the smaller device. Correspondingly, the larger device will have larger g_m, larger C_π, and smaller r_π. The components' values of the small signal model of a HBT device are determined by the geometry scaling of the transistor as well as the DC bias applied.

2.3 Distributed Amplifiers

Distributed amplifiers (DAs), also called traveling wave amplifiers (TWAs), offer ultra-broadband amplification. The reason that they offer outstanding gain bandwidth product is that they are not matched amplifiers and therefore not subject to Fano's bandwidth limit [14]. They are based on a different concept, that of combining the input trans-conductance of several transistors without combining its input capacitances. Distributed amplifies have been shown to provide very flat gain from dc to over 90GHz [20] -- a very significant result.

MMIC distributed amplifier design has been applied to wideband power amplifiers and active power combiners/dividers [21], wideband switches [22], active baluns for mixers [23], and wideband amplifiers for ultra high speed electro-optical communication [5]-[11], [24]. Due to the advancement of AlGaAs/GaAs HBT device and MMIC design technology, HBT distributed amplifiers with wide bandwidth performance have been demonstrated [25]-[29].

Distributed amplifier MMIC structures are attractive for use as preamplifiers for optical receiver applications operating in the multi-Gb/s region. While some papers have been published predicting the signal-noise performance of the MESFET optical distributed amplifiers [5]-[8], there isn't much work similar published for the HBT optical DAs. Therefore, it is challenging and attractive to establish low-noise, ultra broadband HBT optical preamplifiers.

A schematic representation of a basic FET distributed amplifier is shown in Figure 2-4. The gate and drain impedances of the FETs are absorbed into lossy artificial transmission lines by using lumped inductors as shown in Figure 2-4. The transmission line connected to the input is called the gate line, which is formed by shunt capacitances C_{gs} (FET's gate capacitance) and series inductances L_g. The transmission line connected to the output is called the drain line, which is created by shunt capacitances C_{ds} (FET's drain capacitance) and series inductances L_d. As the signal travels down the gate line, each

transistor is excited by the traveling voltage wave and transfers the signal to the drain line through its trans-conductance. If the phase velocities on the gate and drain lines are identical, then the signals on the drain line add in the forward direction as they arrive at the output. The reverse wave will be absorbed by the termination of the drain line. A systematic design approach for such a MESFET distributed amplifier is presented in [30], [31].

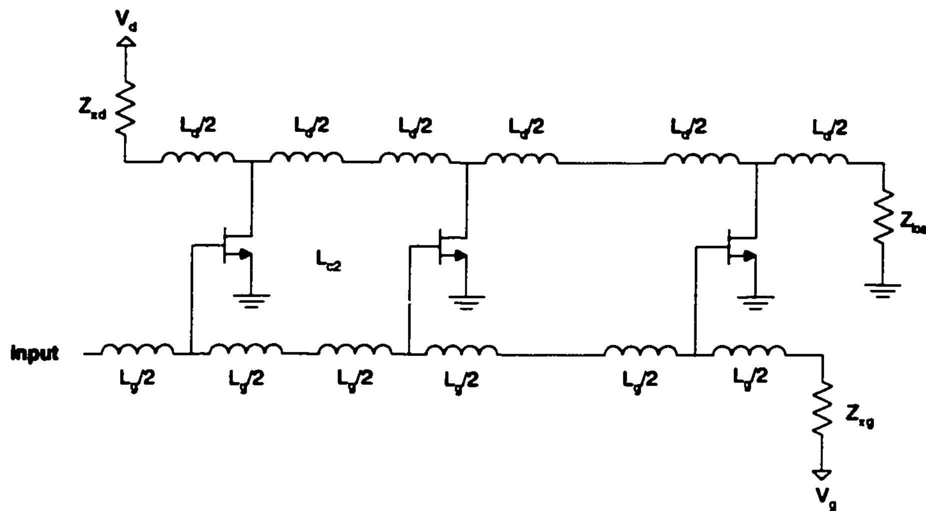


Figure 2-4 Schematic of FET distributed preamplifier

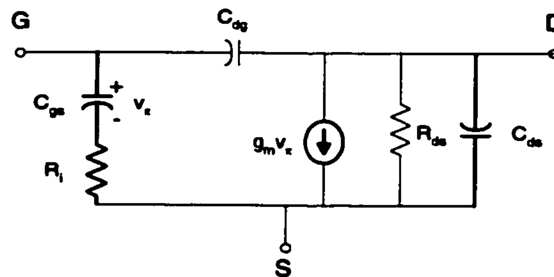


Figure 2-5 Simplified Small signal model of a MESFET

2.3.1 Techniques to extend DA's gain and bandwidth

The gain-bandwidth of a conventional distributed amplifier is limited by several factors such as: gain per cell, gate and drain line attenuations per cell, ATL impedance and cutoff frequencies. There are many FET DA design techniques for increasing the gain and the bandwidth, involving m-derived filter [32], capacitive coupling [33], [34], device bias and geometry scaling, attenuation compensation [31], [35], [36], drain line decline [37], modifying the MBE structure, and matrix distributed amplifier [38], [39] topologies.

A solution to extending the lower frequency response is to incorporate active loads to terminate the input and output transmission lines. In comparison to the conventional RC terminated DA, the active load terminations can significantly extend the flat gain and good return-loss response in frequency at the low edge [28].

In this Section, we give an introduction to some of those techniques used to increase distributed amplifier's gain and bandwidth.

a. M-derived filter construction [32], [40]

Basically, the transmission line configuration of a distributed amplifier can be modeled by a low pass filter, as shown in Figure 2-6. Such a low pass filter network can be considered as a periodic structure of a T-section, which is shown in Figure 2-7 (a). The T section shown in Figure 2-7 (a) is called constant k T section. If the network in Figure 2-6 is infinite, the input impedance of the network $Z(\omega)$ has a constant magnitude ($\sqrt{\frac{L}{C}}$) from zero frequency to ω_c, where it begins to roll off. Here, ω_c is the cutoff frequency of the filter, $\omega_c = 2/\sqrt{LC}$ [34].

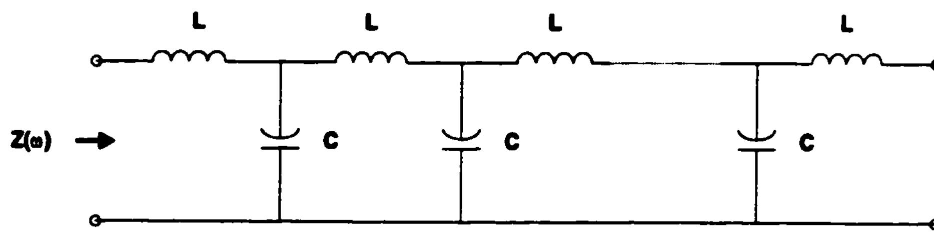
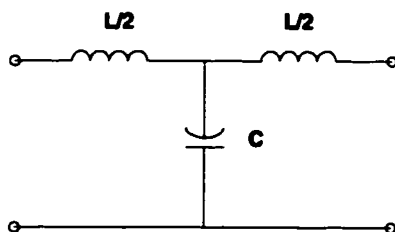


Figure 2-6 Realization of Z(ω) for maximum uniform gain

However, in practice, the coupling network can't be infinite. A resistive load must be used to terminate the structure on the right end. When the structure is terminated by $Z_0=\sqrt{L/C}$, the response Z(ω) is much worse than that of a network terminated with an ideal low pass filter. Significant improvement can be accomplished by utilizing an m-derived section [40]. Consider a low pass m-derived section, as shown in Figure 2-8. Like the constant k proto type shown in Figure 2-7, the m-derived section also has a pass-band up to ω_c. It has the same characteristic impedance as the constant k prototype, Z_{OT}.



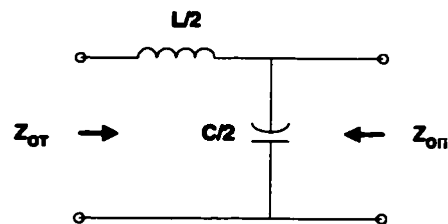
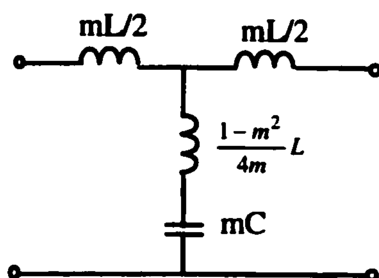


Figure 2-7 (a) Low-pass constant k T section (b) Its corresponding half section



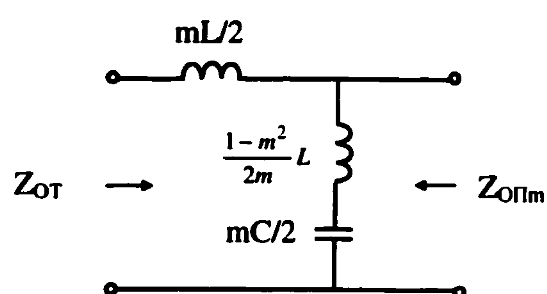


Figure 2-8 (a) Low-pass m-derived T section (b) Its corresponding half section

$$Z_{OT}=\sqrt{\frac{L}{C}\left(1-\frac{\omega^2}{\omega_c^2}\right)} \tag{2-5}$$

Where

$$\omega_c = 2/\sqrt{LC} \tag{2-6}$$

However, its mid-shunt image impedance $Z_{O\Pi m}$ is different from that of the constant k prototype, $Z_{O\Pi}$.

$$Z_{O\Pi}=\sqrt{\frac{L}{C}\left(1-\frac{\omega^2}{\omega_c^2}\right)^{-1}} \tag{2-7}$$

And

$$Z_{O\Pi m}=\sqrt{\frac{L}{C}}\frac{1-\omega^2/\omega_0^2}{\sqrt{1-\omega^2/\omega_c^2}} \tag{2-8}$$

Where

$$\omega_0 = \omega_c/\sqrt{1-m^2}$$

With m=0.6, $Z_{O\Pi m}$ gives a more uniform impedance over the pass-band than $Z_{O\Pi}$. Therefore, an m-derived half section may be used as a buffer stage to match a resistive load to a constant k filter. In the distributed amplifier design, an m-derived filter construction can be used as the modeling of the artificial transmission lines of DAs.

b. Attenuation compensation in DA design

For distributed amplifiers, the primary loss mechanisms of the two artificial lines are the transistor loadings. 'Negative resistance' (NR) circuit can lessen the line attenuation and can lead to increase of the amplifier gain-bandwidth product. Active impedances, characterized by frequency-dependent reactance and negative resistance, reduce the net

attenuation by compensating the signal losses due to the positive resistances of transistors. The negative resistance can be realized by a common-gate FET circuit. The theory is described in [31]. The schematic and the circuit model are shown in Figure 2-9. When driven at its drain terminal, such a circuit can provide a negative resistance and a capacitance over a wide band of frequencies.

The impedance Z_S and Z_G model the bias and termination loads. At very low frequencies, this common-gate circuit doesn't provide sufficient loss compensation. A large $|Z_S|$ is appropriate for NR compensation across very broad bands.

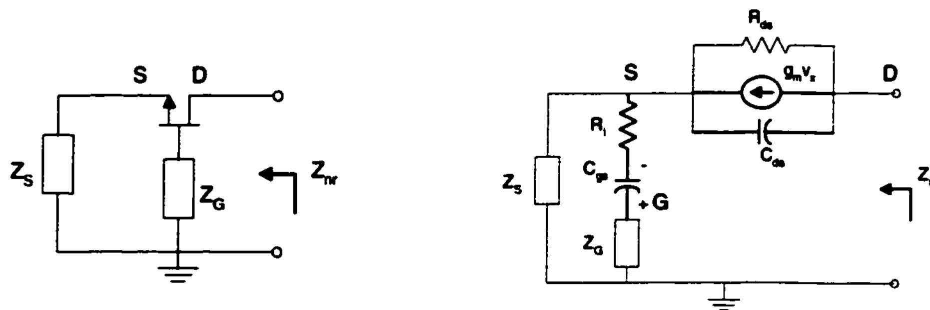


Figure 2-9 (a) A common-gate FET circuit. (b) Its equivalent circuit

Incorporating the common-gate NR circuit with a common-source FET gives a high gain cascode, providing output line loss compensation, as shown in Figure 2-10 [31]. This circuit configurations display negative resistance output impedances at moderate to high frequencies because of the common-gate FET output block.

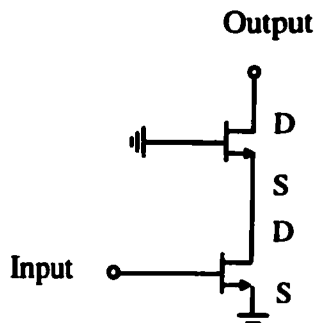


Figure 2-10 Cascode---the output line loss compensation circuit

The impact of negative resistance compensation is twofold. First, by lessening the attenuation on one or both of the lines, more sections can be usefully added to single DA stage. The second impact of NR loss compensation is an extension of the bandwidth. Broadband loss compensation on either DA line permits significant bandwidth increases.

Another proposed loss compensation circuit [35], [36] is constructed by cascode transistors and two additional transmission lines l_{cg} and l_{sd} , as shown in Figure 2-11(a). The equivalent circuit is shown in Figure 2-11(b). The negative resistance increases and gain is improved at high frequencies, due to l_{cg}. l_{sd} is used to keep the circuit stable.

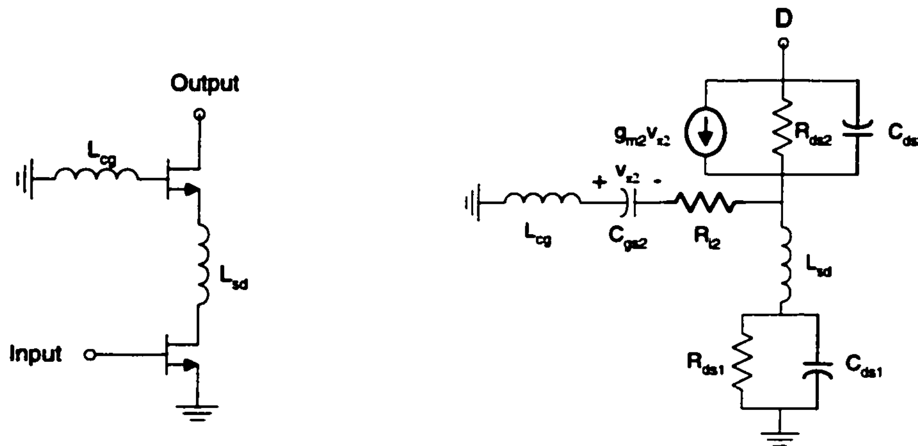


Figure 2-11 (a) Loss compensation circuit (b) Its simplified equivalent circuit

c. Declining drain line lengths DAs

While some distributed amplifier circuits employ identical delay line elements on both the gate and the drain side of the transistor and have their idle ports terminated with resistors that match the characteristic impedances of the artificial transmission lines, others do not. Actually, the drain line and the gate line can use different lengths of delay line elements with different characteristic impedances, respectively. They can also have

their idle ports terminated with resistors that don't match the characteristic impedances of the artificial transmission lines.

'The declining drain line length DA' design technique was described in [37]. In such a DA circuit, the lengths of the drain line elements become shorter the closer the link is located towards the output terminal of the gain block. This design result is obtained by optimizing the drain line elements to achieve better gain flatness and bandwidth. The improvement is believed to be due to the more synchronous phase conditions between the RF gate and RF drain voltages of the 'declining drain line length DA' circuit.

d. Capacitive-division DA design technique

The bandwidth of DAs can be extended at high frequencies by using Capacitive-division (C_i) DA design technique [33], [34], as shown in Figure 2-12. Additional series capacitances C_i at the gate terminal decrease the values of the shunt capacitances of the gate line and reduce the high-frequency roll-off.

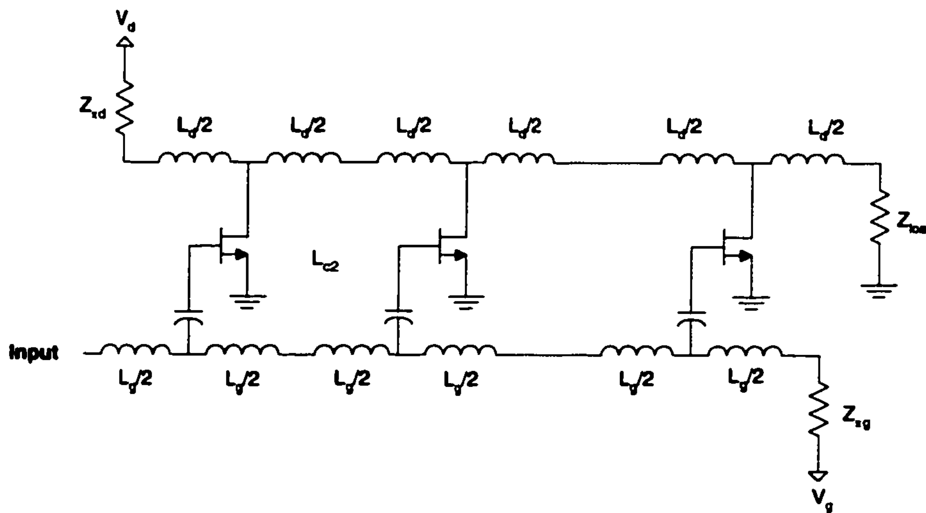


Figure 2-12 Basic capacitive-division DA circuit

However, the gain of the amplifier decreases, because the input signal voltage amplitude is divided by the additional capacitance. Besides, this type of amplifier cannot operate at very low frequency, and can't be used as a base-band amplifier in an SDH (synchronous digital hierarchy) transmission system.

2.3.2 Noise analysis of MESFET distributed preamplifier

The theoretical noise analysis of MESFET preamplifier has been described in [5], [8] and [41]. It has been shown that an improved noise performance can be obtained by increasing the gate line termination impedance. A MESFET distributed preamplifier with 100Ω gate impedance was demonstrated in [5].

A simplified schematic of the optical preamplifier is shown in Figure 2-13. The inductors L_g and the input capacitors of the MESFET C_{gs} form a transmission line with an impedance equal to $Z_{\pi g} = \sqrt{L_g / C_{gs}}$. Similarly, the drain line impedance is given by $Z_{\pi d} = \sqrt{L_d / C_{ds}}$.

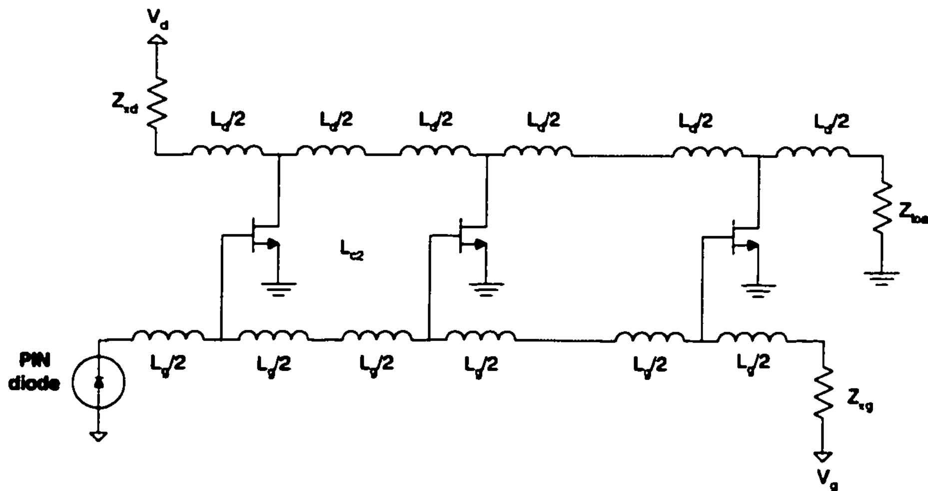


Figure 2-13 Distributed P-I-N preamplifier

The gate and drain lines are matched with the terminating resistors, equal to $Z_{\pi g}$ and $Z_{\pi d}$, so that input and output impedances of the preamplifier remain constant over a large

frequency bandwidth. The magnitude of the trans-impedance [5] in the pass-band is given by

$$\left|Z_{Tf}\right| = \frac{1}{2} g_m Z_{\pi g} Z_{\pi d} n \tag{2-9}$$

Where g_m is the trans-conductance of the MESFET and n is the number of MESFETs in the distributed preamplifier structure. The equivalent input noise current density of the distributed preamplifier is given by [5]

$$\begin{aligned} i^2 = & \left(1 + \frac{2}{n}\frac{\sin n\phi}{\sin\phi}\cos n\phi + \frac{1}{n^2}\left(\frac{\sin n\phi}{\sin\phi}\right)^2\right) i^2_{Z\pi g} \\ & + \frac{\left|Z\pi d\right|^2}{4\left|Z_{Tf}\right|^2} i^2_{Z\pi d} \\ & + \frac{1}{4}\sum_{r=1}^{n}\left(A(r,\phi)^2 + B(r,\phi)^2\right) i^2_g \\ & + \frac{n\left|Z\pi d\right|^2}{4\left|Z_{Tf}\right|^2} i^2_d \\ & + \frac{Z_{\pi d}}{2\left|Z_{Tf}\right|^2}\sum_{r=1}^{n}\mathrm{Re}\left(Z_{Tf}\left(A(r,\phi) + jB(r,\phi)\right)e^{j(n-2r-1)\phi} i_g i_d^*\right) \end{aligned} \tag{2-10}$$

Where

$$i^2_{Z_{\pi g}} = \frac{4kT}{Z_{\pi g}};$$

$$i^2_{Z_{\pi d}} = \frac{4kT}{Z_{\pi d}};$$

$$A(r,\phi) = \frac{(n-r+1)}{n}\cos(2r-1)\phi + \frac{\sin(r-1)\phi}{n\sin\phi}\cos(r-1)\phi + 1;$$

$$B(r,\phi) = \frac{(n-r+1)}{n}\sin(2r-1)\phi + \frac{\sin(r-1)\phi}{n\sin\phi}\sin(r-1)\phi;$$

$$\phi = \omega\sqrt{L_g C_{gs}} = \omega\sqrt{L_d C_{ds}}.$$

k is Boltzmann's constant, and T is temperature in degrees Kelvin. The first two terms of i^2 are the noise densities produced by the terminations $Z_{\pi g}$ and $Z_{\pi d}$. The remaining contributions are the noise sources produced by the MESFET. i_g^2 and i_d^2 are the gate and drain noise sources for the MESFET, and $i_g i_d^*$ is the correlation between the gate and drain noise sources [5]. $i^2_{Z_{\pi g}}$ dominates the noise contribution in i^2 [8]. Thus, the noise can be reduced by making the termination $Z_{\pi g}$ as large as possible. The effect of increasing $Z_{\pi g}$ is twofold:

- It increases the trans-impedance gain $|Z_{T0}|$.
- It reduces the magnitude of the second, fourth, and fifth noise terms in i^2.

That is why the noise performance of a preamplifier can be improved by increasing the gate line impedance. It should be noted that increasing $Z_{\pi g}$ would lead to high losses at high frequency, which is not desirable from the bandwidth point of view.

2.3.3 HBT distributed amplifier

The performance of distributed amplifiers using the HBT rather than MESFET as the active device has been reported [25]-[28]. While a large amount of work has been published predicting the performance of the MESFET DAs, there has not been as much similar work published for the HBT DA. Hence, it is beneficial to develop theory to predict the behavior of the HBT DAs for optical receivers.

The design of HBT distributed amplifiers is similar to MESFET/HEMT distributed amplifier design. The basic differences in their performance are determined by the inherent characteristics of the HBT and MESFET/HEMT devices. HBT devices characteristically have higher input capacitances and resistances leading to generally much poorer DA performance compared to an FET implementation. Because of the lossy input characteristics of the HBT device, the input transmission line attenuation is a major limit of gain-bandwidth performance in HBT DA's. Figure 2-14 shows a simplified small signal model of a HBT. The actual microwave model of a HBT including parasitic

elements is more complicated, which is used for MMIC design. The schematic of a conventional common-emitter HBT distributed amplifier is shown in Figure 2-15.

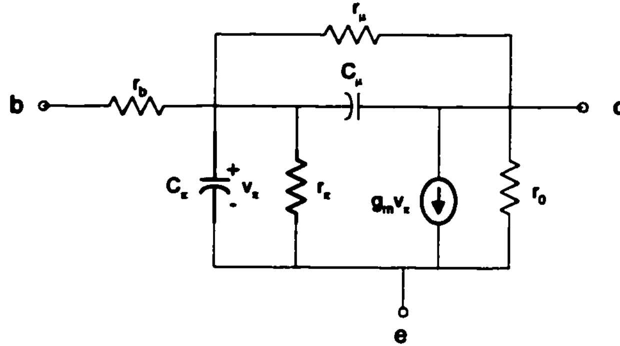


Figure 2-14 Simplified Small signal model of HBT

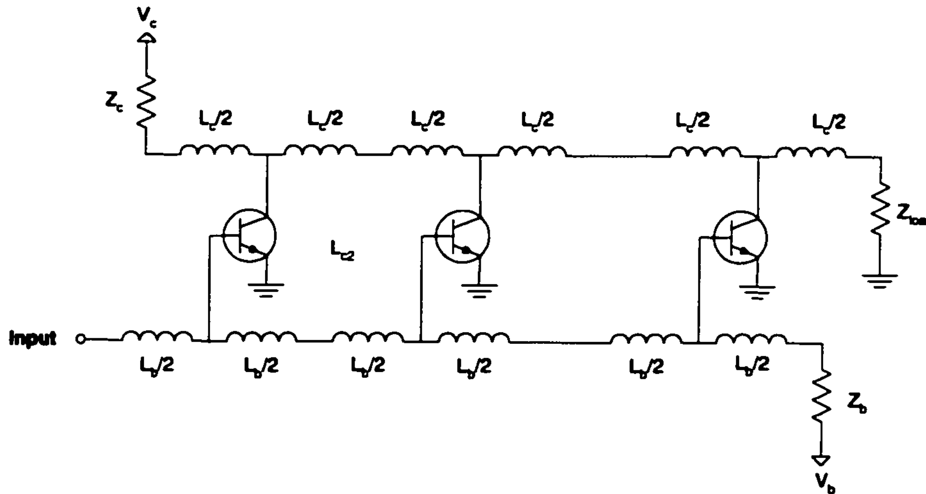


Figure 2-15 A conventional common-emitter HBT distributed preamplifier

There are several FET DA circuit techniques for increasing the gain and the bandwidth that can be applied to an HBT distributed amplifier. The techniques that have been applied to HBT DA's involve capacitive coupling, device bias and geometry scaling,

modifying the MBE structure to reflect a smaller input capacitance, and matrix distributed amplifier topologies. Most of these techniques involve reducing the input capacitance. An attenuation compensation technique has been used in the design of HBT DA [26]. It was shown that the gain-bandwidth product could be improved greatly by using this technique.

As reported in [26], the attenuation compensation techniques used in the design of HBT DA involve periodic loading of the input line with actively generated negative impedance on the input line, and using a cascode configuration to reduce the loss due to the output of the HBT device. For HBT's, the input attenuation compensation can be incorporated into the amplifying device configuration by means of an active impedance transformation.

Figure 2-16 illustrates a common-emitter device, which actively transforms a capacitive impedance at the emitter into a negative impedance at the base (input). The HBT device transforms the capacitor at the emitter to an impedance at the base of Q_1, which looks like a capacitor C in parallel with a series negative resistance $(-\tau_T/C)$ and negative capacitance $(-\alpha_0 C)$. α_0 is defined as the common-base current gain from collector to emitter, and τ_T is the reciprocal of the device cutoff frequency. The equivalent circuit of the transformed capacitive impedance is illustrated in Figure 2-17. Adequate attenuation compensation can be obtained when the base and emitter resistances of the HBT are canceled out by the negative resistance generated by the transformation. This results in an effective input impedance which has no real part.

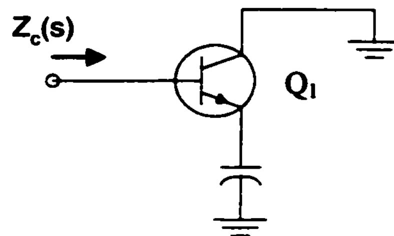


Figure 2-16 Active impedance transformation of a capacitance C

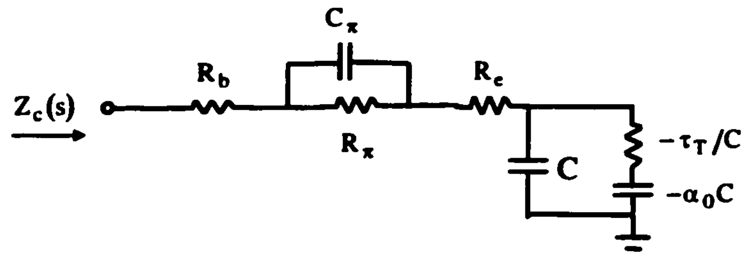


Figure 2-17 Effective equivalent circuit looking into the base of the HBT Q_1

In practice, a compact implementation of this technique can be realized by using a common-collector input transistor Q_1, which transforms the input capacitance of a transistor cascode. In addition, by using a common-collector transistor at the input, the Miller input capacitance is reduced. The cascode topology helps increase the output shunt resistance presented to the output transmission line, which results in low attenuation. Also, the common-base transistor of the cascode reduces the Miller Capacitance of common-emitter transistor, increasing the bandwidth. Figure 2-18 illustrates the configuration of HBT gain cell using this technique. Feedback resistance R_{FB} and base bypass capacitance C_{b1} are used to ensure the stability of the HBT cascode.

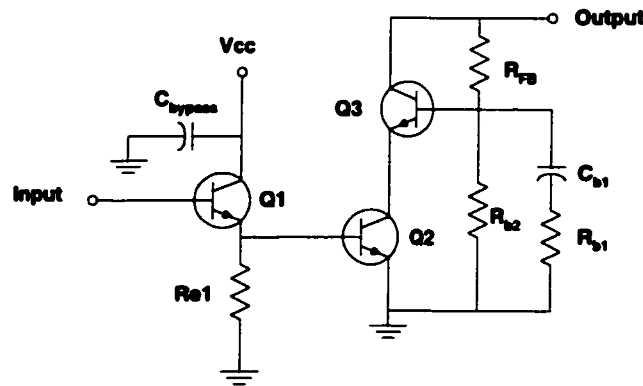


Figure 2-18 HBT gain cell topologies: emitter-follower/cascode transistor configuration

The HBT DA with 74GHz bandwidth has been implemented [42], but no work is published for the noise effect of loss compensation in HBT DAs. It would be beneficial to develop a theoretical analysis for noise performance of HBT optical preamplifier with ultra broad bandwidth.

Chapter 3 Analysis of Proposed Low Noise, Broadband Distributed Preamplifiers

The bandwidth of a HBT distributed amplifier is limited by several factors. The first one is the bandwidth of the LC filter, or the cutoff frequency of the transmission line structure for the DA input and output. The second is the high frequency loss of the HBT gain cell (a section of HBT distributed amplifier), which is not uniform versus frequency. As the frequency goes higher, the loss becomes larger significantly. The gain of the preamplifier is determined by the gain of each HBT gain cell as well as the number of the stages. Ideally, the more stages, the more gain. Actually, since the ATL has loss, the gain cell also consumes signal. When the consumption on the last cell is bigger than the cell's output signal, it is not beneficial to add more stages.

The HBT is a modified bipolar transistor. Its small signal model is similar to the BJT's, which is shown in Figure 3-1. The following relationships exist for the small signal model of a HBT device.

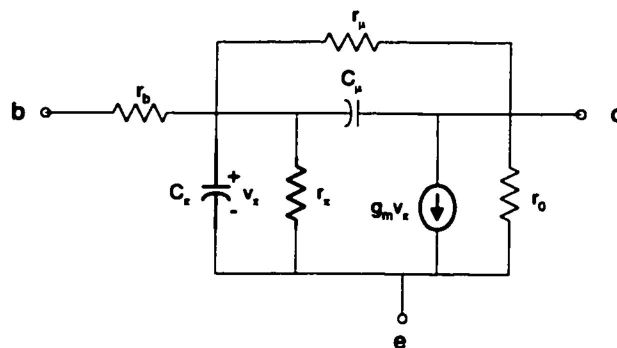


Figure 3-1 Simplified Small signal model of HBT

$$g_m = I_C / V_T \tag{3-1}$$

$$g_m r_\pi = \beta \tag{3-2}$$

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{3-3}$$

As discussed in Chapter 2, HBT devices characteristically have higher input capacitances and resistance compared to MESFET/HEMT devices. Therefore, the main limiting factors for a traditional HBT DA design are as follows:

- Input capacitance C_π and base resistance r_b, which limit the ultimate bandwidth cutoff frequency;
- The input transmission line attenuation factor which is determined to be dominated by the input loss of the device;
- The output transmission line attenuation factor.

The last two factors limit the number of sections that can be beneficially added to a DA to increase gain-bandwidth performance.

As discussed in Section 2.3.3, techniques for increasing the gain and bandwidth of HBT DAs include capacitive coupling, device bias and geometry scaling, modifying the MBE structure to reflect a smaller input capacitance, matrix distributed amplifier topologies [27], and attenuation compensation technique [26]. For the optical preamplifier application, the HBT distributed amplifier must operate at base-band. Therefore, a capacitive coupling topology can't be used. Modifying the MBE structure is not possible at the circuit design level and is not considered here. In this thesis, we examine ways of using device bias and geometry scaling technique, along with attenuation compensation technique to extend bandwidth for the HBT distributed amplifier design. With these techniques, the bandwidth of the DA can be extended.

3.1 Proposed Configuration of HBT gain cell

A novel configuration of HBT gain cell is suggested as shown in Figure 3-2 based on attenuation compensation technique in Section 2.3.3. From Figure 3-2, we can see that the HBT gain cell includes three stages of amplifier: the Common-Collector (Emitter Follower), Common-Emitter and Common-Base. Compared with Figure 2-18, the new configuration of the gain cell is simpler, and easy to implement. Instead of using shunt feedback resistance R_{FB} and R_{b2}, a series resistor R_{e2} is added at the emitter of the cascode to extend the cascode's bandwidth; a series inductance L_{e2} is used to ensure the stability of the cascode.

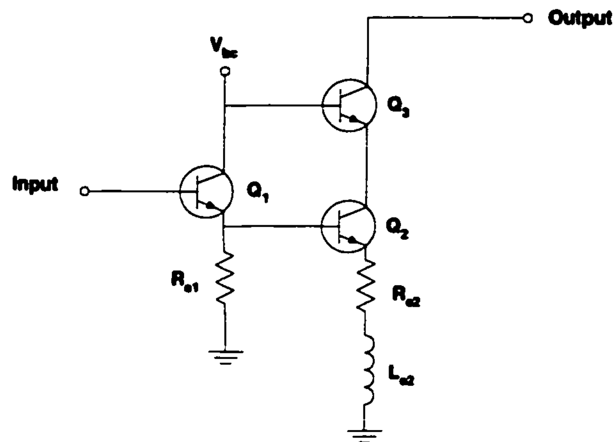


Figure 3-2 HBT gain cell topologies: emitter-follower/cascode configuration

Analysis begins by looking at the Common-Collector circuit first. The output voltage at the emitter follows the input voltage at the base. The voltage gain of the CC is less than but close to unity. Resistances are reflected from the emitter to the base circuit by multiplying them by (β+1). A capacitive load for the Common-Collector leads to a negative input conductance as described in [26].

The Common-emitter amplifier provides an input resistance of moderate value ($\approx (\beta+1)(r_e+R_e)$), a high trans-conductance (equal to g_m of the HBT), a high output resistance, high voltage and current gains; But its high frequency performance is severely limited by the collector to base capacitance of the transistor. Therefore, the CE configuration is utilized to provide the bulk of the required overall voltage gain. The resistor R_e between emitter and ground introduces negative feedback in the amplifier circuit. With R_e in the CE circuit, the gain decreases; and the gain A_v becomes less dependent in the value of β. A large signal can be applied at the input without risking nonlinear distortion. The high frequency response is significantly improved.

The Common-Base circuit accepts an input signal at a low input impedance level ($\approx r_e$) and delivering an almost equal (slightly smaller) current at the collector at a very high impedance level. The CB amplifier has a much high upper cutoff frequency than that of the CE circuit. Since its base is grounded, no Miller effect is present.

This gain cell configuration (CC-CE-CB) combines the advantages of the CC, CE and CB circuits. By using CC (Q_1) as the input buffer circuit, a negative input conductance results from the large capacitance (C_π) of CE circuit (Q_2). The input impedance of the gain cell is very high, which means less input loss. This is very important for the traveling wave amplifier's implementation. The CB (Q_3) circuit acts as a current buffer for the gain cell. Also, it provides very high output impedance for the gain cell. This will significantly reduce the loss presented to the output line of the traveling amplifier, which is helpful in extending the bandwidth of the DA. Therefore, a HBT distributed amplifier using this new configuration as gain cell has potential to obtain broader bandwidth.

We will derive the transconductance and the input impedance of this HBT gain cell configuration in Section 3.1.1 and Section 3.1.2, respectively.

3.1.1 Transconductance of the HBT gain cell

Neglecting L_{e2} and C_{μ} in the circuit of Figure 3-2, the small signal equivalent circuit of the HBT gain cell can be represented as a circuit shown in Figure 3-3.

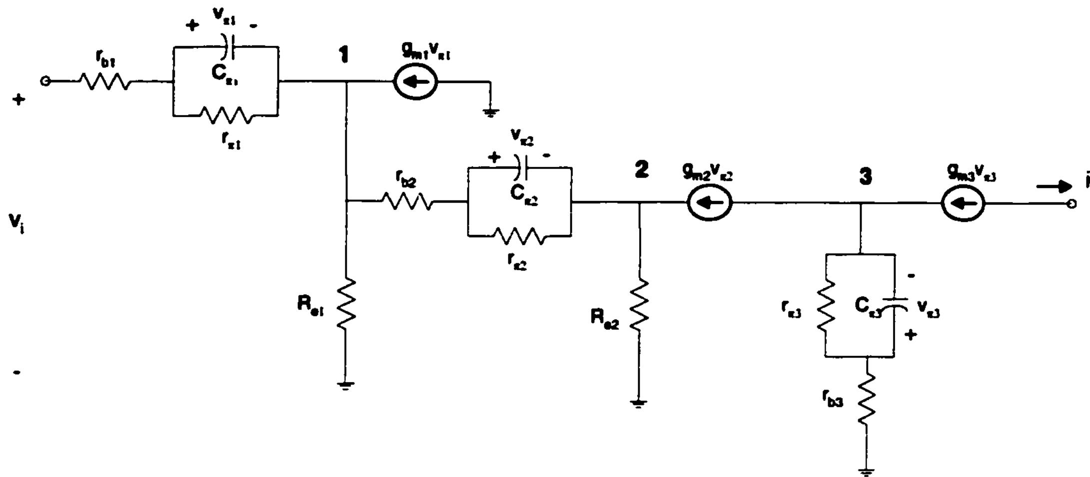


Figure 3-3 Small signal equivalent circuit of the HBT gain cell

Let

$$Y_{\pi 1} = \frac{1}{r_{\pi 1}} + j\omega C_{\pi 1} \quad (3\text{–}4a)$$

$$Y_{\pi 2} = \frac{1}{r_{\pi 2}} + j\omega C_{\pi 2} \quad (3\text{–}4b)$$

$$Y_{\pi 3} = \frac{1}{r_{\pi 3}} + j\omega C_{\pi 3} \quad (3\text{–}4c)$$

Applying circuit network theory to the circuit in Figure3-3, we can write

$$v_i = (Y_{\pi 1} \cdot v_{\pi 1}) \cdot r_{b1} + v_{\pi 1} + v_1 \quad (3\text{–}5)$$

$$v_1 = (Y_{\pi 2} \cdot v_{\pi 2}) \cdot r_{b2} + v_{\pi 2} + v_2 \quad (3\text{–}6)$$

At point 1,

$$Y_{\pi 1} \cdot v_{\pi 1} + g_{m1} \cdot v_{\pi 1} = \frac{v_1}{R_{e1}} + Y_{\pi 2} \cdot v_{\pi 2} \tag{3–7}$$

At point 2,

$$\frac{v_2}{R_{e2}} = Y_{\pi 2} \cdot v_{\pi 2} + g_{m2} \cdot v_{\pi 2}$$

or

$$v_2 = (Y_{\pi 2} \cdot v_{\pi 2} + g_{m2} \cdot v_{\pi 2}) \cdot R_{e2} \tag{3–8}$$

At point 3,

$$(Y_{\pi 3} + g_{m3}) \cdot v_{\pi 3} = g_{m2} \cdot v_{\pi 2} \tag{3–9}$$

Equation (3–7) can be represented as

$$v_1 = \left[(Y_{\pi 1} + g_{m1}) \cdot v_{\pi 1} - Y_{\pi 2} \cdot v_{\pi 2}\right] \cdot R_{e1} \tag{3–10}$$

Introducing (3–10) into (3–5) gives

$$v_i = \left[(Y_{\pi 1} \cdot r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) \cdot R_{e1}\right] \cdot v_{\pi 1} - Y_{\pi 2} \cdot R_{e1} \cdot v_{\pi 2} \tag{3–11}$$

Introducing (3–8), (3–10) into (3–6) gives

$$(Y_{\pi 1} + g_{m1}) R_{e1} \cdot v_{\pi 1} = [Y_{\pi 2} \cdot R_{e1} + (Y_{\pi 2} \cdot r_{b2} + 1) + (Y_{\pi 2} + g_{m2}) R_{e2}] \cdot v_{\pi 2} \tag{3–12}$$

Reducing $v_{\pi l}$ from (3–11) and (3–12) gives

$$v_{\pi 2} = \frac{(Y_{\pi 1} + g_{m1}) \cdot R_{e1} \cdot v_i}{(Y_{\pi 1} \cdot r_{b1} + 1) Y_{\pi 2} \cdot R_{e1} + \left[(Y_{\pi 1} \cdot r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) \cdot R_{e1}\right] \cdot \left[(Y_{\pi 2} \cdot r_{b2} + 1) + (Y_{\pi 2} + g_{m2}) \cdot R_{e2}\right]} \tag{3–13}$$

From (3–9), we know that

$$v_{\pi 3} = \frac{g_{m2} \cdot v_{\pi 2}}{\left(Y_{\pi 3} + g_{m3}\right)} \tag{3–14}$$

Therefore, the output current of the cell is equal to

$$i_i = -g_{m3} \cdot v_{\pi 3} = -\frac{g_{m2} \cdot g_{m3}}{(Y_{\pi 3} + g_{m3})} \cdot v_{\pi 2} \tag{3–15}$$

Introducing (3–13) into (3–15) gives

$$i_i = -G \cdot v_i \tag{3–16}$$

Where

$$G = \frac{g_{m2} g_{m3}}{\left(Y_{\pi 3} + g_{m3}\right)} \frac{(Y_{\pi 1} + g_{m1}) \cdot R_{e1}}{\left(Y_{\pi 1} r_{b1} + 1\right) Y_{\pi 2} \cdot R_{e1} + \left[\left(Y_{\pi 1} r_{b1} + 1\right) + \left(Y_{\pi 1} + g_{m1}\right) \cdot R_{e1}\right] \cdot \left[\left(Y_{\pi 2} r_{b2} + 1\right) + \left(Y_{\pi 2} + g_{m2}\right) \cdot R_{e2}\right]} \tag{3–17}$$

At low frequency, we have

$$g_{m1} + Y_{\pi 1} \approx g_{m1}, \qquad Y_{\pi 1} r_{b1} + 1 \approx 1 \tag{3–18a}$$

$$g_{m2} + Y_{\pi 2} \approx g_{m2}, \qquad Y_{\pi 2} r_{b2} + 1 \approx 1 \tag{3–18b}$$

$$g_{m3} + Y_{\pi 3} \approx g_{m3}, \qquad Y_{\pi 3} r_{b3} + 1 \approx 1 \tag{3–18c}$$

Then G can be reduced to

$$G = \frac{g_{m1} g_{m2} R_{e1}}{\left[Y_{\pi 2} R_{e1} + (1 + g_{m1} R_{e1}) \cdot (1 + g_{m2} R_{e2})\right]} \tag{3–19}$$

or

$$G = \frac{1}{\left[\dfrac{Y_{\pi 2}}{g_{m1} g_{m2}} + \left(\dfrac{1}{g_{m1} R_{e1}} + 1\right) \cdot \left(\dfrac{1}{g_{m2}} + R_{e2}\right)\right]} \tag{3-20}$$

Obviously, G increases as any one of g_{m1}, g_{m2}, and R_{e1} increases. G decreases as R_{e2} increases. In practical applications, Q_1 acts as an emitter-follower, and R_{e1} is very large.

Then, the voltage over R_{e1} is almost equal to the input voltage v_i, and the G can be approximated as

$$G = \frac{1}{\left[\frac{Y_{\pi 2}}{g_{m1} g_{m2}} + \left(\frac{1}{g_{m2}} + R_{e2}\right)\right]} \tag{3-21}$$

Since $g_{m2} r_{\pi 2} = \beta_2$, we can get

$$\frac{Y_{\pi 2}}{g_{m1} g_{m2}} = \frac{1}{g_{m1} g_{m2}} \left(\frac{1}{r_{\pi 2}} + j\omega C_{\pi 2}\right) = \frac{1}{g_{m1} \beta} + \frac{j\omega C_{\pi 2}}{g_{m1} g_{m2}}$$

At low frequency, obviously, $\frac{Y_{\pi 2}}{g_{m1} g_{m2}}$ is very small compared to $\frac{1}{g_{m2}} + R_{e2}$. Therefore, G essentially depends on g_{m2}, and R_{e2}.

Equation (3–18) is only valid at low to middle high frequencies (<10GHz). As frequency goes high, ωC_π becomes comparable to g_m. From Equation (3–17), we can see that $C_{\pi 2}$ and $C_{\pi 3}$ will cause G decrease as frequency goes high. This is a major factor that limits the 3dB bandwidth of the distributed amplifier.

3.1.2 Input impedance of the HBT gain cell

In this Section, we will derive the input impedance of the HBT gain cell.

From (3–12), (3–13), reducing $v_{\pi 2}$ gives

$$v_{\pi 1} = \frac{\left[Y_{\pi 2} R_{e1} + (Y_{\pi 2} r_{b2} + 1) + (Y_{\pi 2} + g_{m2}) \cdot R_{e2}\right] \cdot v_i}{(Y_{\pi 1} \cdot r_{b1} + 1) Y_{\pi 2} \cdot R_{e1} + \left[(Y_{\pi 1} \cdot r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) \cdot R_{e1}\right] \cdot \left[(Y_{\pi 2} \cdot r_{b2} + 1) + (Y_{\pi 2} + g_{m2}) \cdot R_{e2}\right]} \tag{3-22}$$

Therefore, the input impedance of the gain cell is equal to

$$Z_i = \frac{v_i}{i_{b1}} = \frac{v_i}{Y_{\pi 1} v_{\pi 1}}$$
$$= \frac{(Y_{\pi 1} r_{b1} + 1) Y_{\pi 2} \cdot R_{e1} + [(Y_{\pi 1} r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) \cdot R_{e1}] \cdot [(Y_{\pi 2} r_{b2} + 1) + (Y_{\pi 2} + g_{m2}) \cdot R_{e2}]}{Y_{\pi 1} \cdot [Y_{\pi 2} \cdot R_{e1} + (Y_{\pi 2} r_{b2} + 1) + (Y_{\pi 2} + g_{m2}) \cdot R_{e2}]} \quad (3-23)$$

Introducing (3–18) into (3–23) gives the expression of the input impedance of the gain cell at low to moderate high frequency,

$$Z_i = \frac{Y_{\pi 2} \cdot R_{e1} + [1 + g_{m1} \cdot R_{e1}] \cdot [1 + g_{m2} \cdot R_{e2}]}{Y_{\pi 1} \cdot [Y_{\pi 2} \cdot R_{e1} + 1 + g_{m2} \cdot R_{e2}]} \quad (3-24)$$

By introducing Equations (3–4) into Equation (3–24), Z_i actually can be written in following format

$$Z_i = \frac{1}{j\omega C_{\pi 1} + \frac{1}{r_{\pi 1}}} \left[1 + \frac{C_{\pi 1} g_{m1} (1 + g_{m2} R_{e2})}{\frac{C_{\pi 1}}{r_{\pi 2}} - \frac{C_{\pi 2}}{r_{\pi 1}} + C_{\pi 1} \frac{1 + g_{m2} R_{e2}}{R_{e1}}} \right] - \frac{C_{\pi 2} g_{m1} (1 + g_{m2} R_{e2})}{\left(j\omega C_{\pi 2} + \frac{1}{r_{\pi 2}} + \frac{1 + g_{m2} R_{e2}}{R_{e1}} \right) \left(\frac{C_{\pi 1}}{r_{\pi 2}} - \frac{C_{\pi 2}}{r_{\pi 1}} + C_{\pi 1} \frac{1 + g_{m2} R_{e2}}{R_{e1}} \right)} \quad (3-25)$$

At same bias conditions, noticing that $C_{\pi 1} r_{\pi 1} = C_{\pi 2} r_{\pi 2}$, then the input impedance of the cell is equal to

$$Z_i = \frac{1}{j\omega C_{\pi 1} + \frac{1}{r_{\pi 1}}} (1 + g_{m1} R_{e1}) - \frac{g_{m1} R_{e1} C_{\pi 2}}{\left(j\omega C_{\pi 2} + \frac{1}{r_{\pi 2}} + \frac{1 + g_{m2} R_{e2}}{R_{e1}} \right) C_{\pi 1}} \quad (3-26)$$

From (3-26), we can see that negative resistor and negative capacitance results from $C_{\pi 2}$. If we represent the HBT gain cell as a two-port network, the [Y] matrix of the two-port network can be approximately written as

$$[Y] = \begin{bmatrix} \frac{1}{Z_i} & 0 \\ G & 0 \end{bmatrix} \quad (3-27)$$

Equation (3–27) characterizes the small signal performance of the HBT gain cell.

3.1.3 Noise Model of the HBT gain cell

Figure 3-4 shows the equivalent circuit of the suggested HBT gain cell including noise sources.

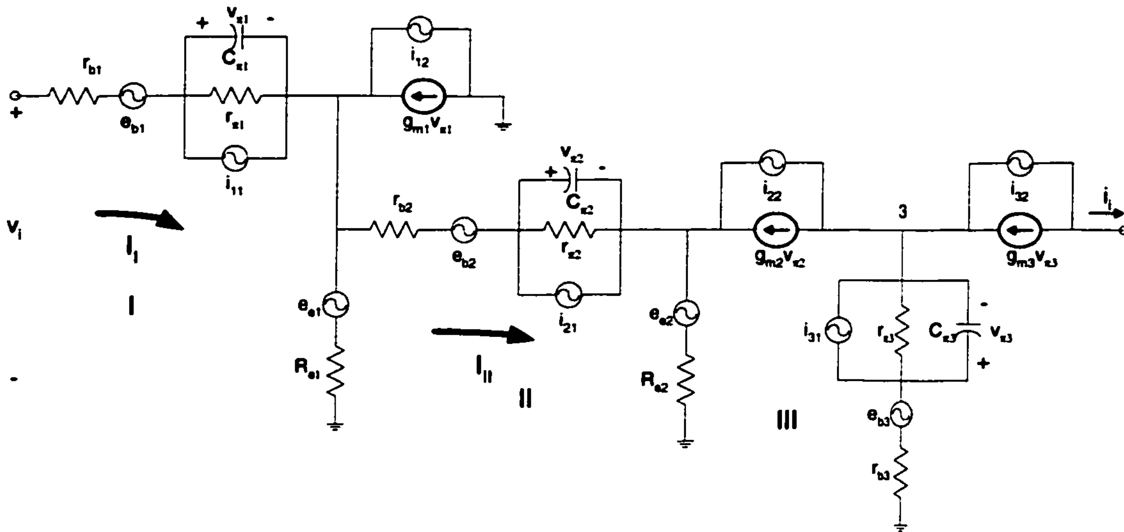


Figure 3-4 Equivalent circuit of HBT gain cell including noise sources

From Figure 3-4, we can see that there are several noise sources in this circuit: i_{11} and i_{12}, i_{21} and i_{22}, and i_{31} and i_{32} are the intrinsic noise sources of HBT device Q_1, Q_2, and Q_3, respectively. e_{bi} and e_{ei} are noise voltage density due to resistor r_{bi} or R_{ei}.

The noise model of the HBT gain cell (as shown in Figure 3-4) can be transformed into the conventional representation of Figure 3-5, which is more suitable for noise analysis of a preamplifier. In that case, the HBT is considered to be a noiseless two-port network

with two correlated voltage and current noise generators (e_{ni} and i_{ni}) connected at its input. The [Y] matrix of the noiseless two-port network in Figure 3-5 is described in Equation (3–27). The derivation of noise sources e_{ni} and i_{ni} can be carried out analytically from the original network of Figure 3-4 following the noisy network theory.

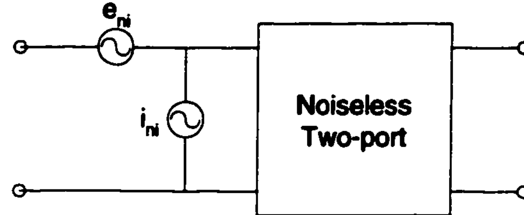


Figure 3-5 Chain representation of a noisy network for the HBT gain cell

Assume that source impedance and load impedance of the HBT gain cell are R_S and R_L, respectively. Noise analysis for the noise circuit in Figure 3-4 proceeds as follows:

For loop I, we have

$$i_I = i_{11} + Y_{\pi 1} v_{\pi 1} \tag{3–28}$$

$$i_I (R_S + r_{b1}) + e_{b1} + v_{\pi 1} + e_{e1} + (i_I + g_{m1} v_{\pi 1} + i_{12} - i_{II}) R_{e1} = 0 \tag{3–29}$$

For loop II, we can write

$$i_{II} = i_{21} + Y_{\pi 2} v_{\pi 2} \tag{3–30}$$

$$-(i_I + g_{m1} v_{\pi 1} + i_{12} - i_{II}) R_{e1} - e_{e1} + e_{b2} + i_{II} r_{b2} + v_{\pi 2} + e_{e2} + (i_{II} + g_{m2} v_{\pi 2} + i_{22}) R_{e2} = 0 \tag{3–31}$$

At point 3,

$$(g_{m3} v_{\pi 3} + i_{32}) + (Y_{\pi 3} v_{\pi 3} + i_{31}) = (g_{m2} v_{\pi 2} + i_{22}) \tag{3–32}$$

The output current is equal to

$$i_i = -(g_{m3}v_{\pi 3} + i_{32}) \tag{3-33}$$

Resolving Equations (3–28) to (3–33) gives output current i_i by

$$i_i = -\frac{g_{m3}}{(Y_{\pi 3} + g_{m3})}\left[\frac{g_{m2}(C_2 + C_3 R_S)}{C_0 + C_1 R_S} + (i_{22} - i_{31} - i_{32})\right] - i_{32} \tag{3-34}$$

Where

$$C_0 = (Y_{\pi 1} r_{b1} + 1) Y_{\pi 2} R_{e1} + [(Y_{\pi 1} r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) R_{e1}] \cdot [(Y_{\pi 2} r_{b2} + 1) + (Y_{\pi 2} + g_{m2}) R_{e2}] \tag{3-35}$$

$$C_1 = Y_{\pi 1} \cdot [Y_{\pi 2}(R_{e1} + r_{b2} + R_{e2}) + 1 + g_{m2} R_{e2}] \tag{3-36}$$

$$\begin{aligned} C_2 &= i_{11}(R_{e1} - r_{b1} g_{m1} R_{e1}) + i_{12} R_{e1}(Y_{\pi 1} r_{b1} + 1) \\ &- i_{21}\{(r_{b2} + R_{e2})[(Y_{\pi 1} r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) R_{e1}] + R_{e1}(Y_{\pi 1} r_{b1} + 1)\} \\ &- i_{22} R_{e2}\left[(Y_{\pi 1} r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) R_{e1}\right] - e_{b1} R_{e1}(Y_{\pi 1} + g_{m1}) + e_{e1}(Y_{\pi 1} r_{b1} + 1) \\ &- e_{b2}\left[(Y_{\pi 1} r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) R_{e1}\right] - e_{e2}\left[(Y_{\pi 1} r_{b1} + 1) + (Y_{\pi 1} + g_{m1}) R_{e1}\right] \end{aligned} \tag{3-37}$$

$$\begin{aligned} C_3 &= -i_{11} g_{m1} R_{e1} + i_{12} R_{e1} Y_{\pi 1} - i_{21}(R_{e1} + r_{b2} + R_{e2}) Y_{\pi 1} - i_{22} R_{e2} Y_{\pi 1} \\ &+ e_{e1} Y_{\pi 1} - e_{b2} Y_{\pi 1} - e_{e2} Y_{\pi 1} \end{aligned} \tag{3-38}$$

Under the same source impedance R_S and load impedance R_L conditions, we may represent the output noise of the noiseless two-port network in Figure 3-5 due to noise sources e_{ni} and i_{ni}.

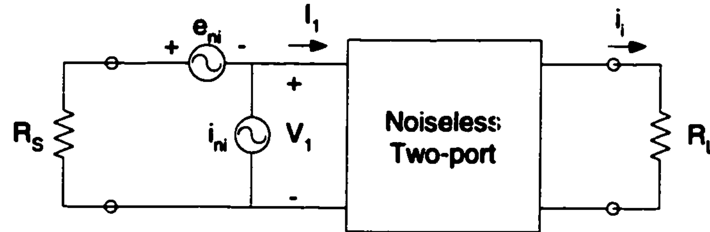


Figure 3-6 Chain representation of a noisy network for the HBT gain cell

Since the admittance matrix of the two-port noiseless network is equal to

$$[Y]=\begin{bmatrix} \frac{1}{Z_i} & 0 \\ G & 0 \end{bmatrix} \tag{3–27}$$

From Figure 3-6, we know that

$$I_1 = \frac{V_1}{Z_i} \tag{3–39}$$

$$I_1 = -i_{ni} + \frac{e_{ni} + V_1}{R_S} \tag{3–40}$$

Reducing I_1 from (3–39) and (3–40) gives

$$V_1 = -\left(i_{ni} - \frac{e_{ni}}{R_S}\right)\frac{Z_i R_S}{Z_i + R_S} \tag{3–41}$$

Then,

$$i_i = -GV_1 = GZ_i \frac{R_S i_{ni} - e_{ni}}{R_S + Z_i} \tag{3–42}$$

Introducing (3–17) and (3–23) into (3–42) gives

$$i_i = \frac{g_{m2} g_{m3}}{(Y_{\pi 3} + g_{m3})}\left[\frac{(Y_{\pi 1} + g_{m1})R_{e1}(R_S i_{ni} - e_{ni})}{C_0 + C_1 R_S}\right] \tag{3–43}$$

Let Equation (3–34) equal to Equation (3–43) for any value of R_S, we can get

$$i_{ni} = -\frac{g_{m2} g_{m3} C_3 + [g_{m3}(i_{22} - i_{31}) + i_{32} Y_{\pi 3}]C_1}{g_{m2} g_{m3}(Y_{\pi 1} + g_{m1})R_{e1}} \tag{3–44}$$

$$e_{ni} = \frac{g_{m2}g_{m3}C_2 + [g_{m3}(i_{22} - i_{31}) + i_{32}Y_{\pi 3}]C_0}{g_{m2}g_{m3}(Y_{\pi 1} + g_{m1})R_{e1}} \tag{3–45}$$

Introducing (3-38) into (3-44) gives

$$\begin{aligned} i_{ni} = &\frac{1}{(Y_{\pi 1} + g_{m1})R_{e1}}\{i_{11}(g_{m1}R_{e1}) - i_{12}(Y_{\pi 1}R_{e1}) + i_{21}(R_{e1} + r_{b2} + R_{e2})Y_{\pi 1} - e_{e1}Y_{\pi 1} + e_{b2}Y_{\pi 1} + e_{e2}Y_{\pi 1}\} \\ &- \frac{1}{g_{m2}g_{m3}(Y_{\pi 1} + g_{m1})R_{e1}}\{i_{22}(g_{m3}Y_{\pi 1})[Y_{\pi 2}(R_{e1} + R_{e2}) + (Y_{\pi 2}r_{b2} + 1)] - i_{31}(g_{m3}C_1) + i_{32}(Y_{\pi 3}C_1)\} \end{aligned} \tag{3–46}$$

Introducing (3-37) into (3-45) gives

$$\begin{aligned} e_{ni} = &\frac{1}{(Y_{\pi 1} + g_{m1})R_{e1}}\left\{\begin{matrix} i_{11}R_{e1}(1 - r_{b1}g_{m1}) + i_{12}R_{e1}(Y_{\pi 1}r_{b1} + 1) - i_{21}[A_0(r_{b2} + R_{e2}) + R_{e1}(Y_{\pi 1}r_{b1} + 1)] \\ - e_{b1}(Y_{\pi 1} + g_{m1})R_{e1} + e_{e1}(Y_{\pi 1}r_{b1} + 1) - e_{b2}A_0 - e_{e2}A_0 \end{matrix}\right\} \\ &+ \frac{1}{g_{m2}g_{m3}(Y_{\pi 1} + g_{m1})R_{e1}}\{i_{22}[g_{m3}C_0 - g_{m2}g_{m3}R_{e2}A_0] - i_{31}(g_{m3}C_0) + i_{32}(Y_{\pi 3}C_0)\} \end{aligned} \tag{3–47}$$

Where

$$A_0 = (Y_{\pi 1}r_{b1} + 1) + (Y_{\pi 1} + g_{m1})R_{e1} \tag{3–48}$$

Then, ignoring correlation between different noise sources, $\overline{i_{ni}^{\ 2}}$, $\overline{e_{ni}^{\ 2}}$ and $i_{ni}e_{ni}^{\ *}$ can be derived from i_{ni} and e_{ni} as

$$\begin{aligned} \overline{i_{ni}^{\ 2}} = &\left|\frac{1}{(Y_{\pi 1} + g_{m1})R_{e1}}\right|^2 \left\{\overline{i_{11}^{\ 2}}|g_{m1}R_{e1}|^2 + \overline{i_{12}^{\ 2}}|Y_{\pi 1}R_{e1}|^2 + \overline{i_{21}^{\ 2}}|(R_{e1} + r_{b2} + R_{e2})Y_{\pi 1}|^2 + \overline{e_{e1}^{\ 2}}|Y_{\pi 1}|^2 + \overline{e_{b2}^{\ 2}}|Y_{\pi 1}|^2 + \overline{e_{e2}^{\ 2}}|Y_{\pi 1}|^2\right\} \\ &+ \left|\frac{1}{g_{m2}g_{m3}(Y_{\pi 1} + g_{m1})R_{e1}}\right|^2 \left\{\overline{i_{22}^{\ 2}}|(g_{m3}Y_{\pi 1})[Y_{\pi 2}(R_{e1} + R_{e2}) + (Y_{\pi 2}r_{b2} + 1)]|^2 + \overline{i_{31}^{\ 2}}|g_{m3}C_1|^2 + \overline{i_{32}^{\ 2}}|Y_{\pi 3}C_1|^2\right\} \end{aligned} \tag{3–49}$$

$$\begin{aligned} \overline{e_{ni}^{\ 2}} = &\left|\frac{1}{(Y_{\pi 1} + g_{m1})R_{e1}}\right|^2 \left\{\begin{matrix} \overline{i_{11}^{\ 2}}|R_{e1}(1 - r_{b1}g_{m1})|^2 + \overline{i_{12}^{\ 2}}|R_{e1}(Y_{\pi 1}r_{b1} + 1)|^2 + \overline{i_{21}^{\ 2}}|A_0(r_{b2} + R_{e2}) + R_{e1}(Y_{\pi 1}r_{b1} + 1)|^2 \\ + \overline{e_{b1}^{\ 2}}|(Y_{\pi 1} + g_{m1})R_{e1}|^2 + \overline{e_{e1}^{\ 2}}|Y_{\pi 1}r_{b1} + 1|^2 + \overline{e_{b2}^{\ 2}}|A_0|^2 + \overline{e_{e2}^{\ 2}}|A_0|^2 \end{matrix}\right\} \\ &+ \left|\frac{1}{g_{m2}g_{m3}(Y_{\pi 1} + g_{m1})R_{e1}}\right|^2 \left\{\overline{i_{22}^{\ 2}}|g_{m3}C_0 - g_{m2}g_{m3}R_{e2}A_0|^2 + \overline{i_{31}^{\ 2}}|g_{m3}C_0|^2 + \overline{i_{32}^{\ 2}}|Y_{\pi 3}C_0|^2\right\} \end{aligned} \tag{3–50}$$

$$i_{ni}e_{ni}^{*} = \left|\frac{1}{(Y_{\pi 1}+g_{m1})R_{e1}}\right|^2 \left\{ \begin{array}{l} \overline{i_{11}^{2}}(g_{m1}R_{e1})[R_{e1}(1-r_{b1}g_{m1})]^{*} - \overline{i_{12}^{2}}(Y_{\pi 1}R_{e1})[R_{e1}(Y_{\pi 1}r_{b1}+1)]^{*} \\ -\overline{i_{21}^{2}}[(R_{e1}+r_{b2}+R_{e2})Y_{\pi 1}][A_0(r_{b2}+R_{e2})+R_{e1}(Y_{\pi 1}r_{b1}+1)]^{*} \\ -\overline{e_{e1}^{2}}Y_{\pi 1}(Y_{\pi 1}r_{b1}+1)^{*} - \overline{e_{b2}^{2}}Y_{\pi 1}A_0^{*} - \overline{e_{e2}^{2}}Y_{\pi 1}A_0^{*} \end{array} \right\} + \left|\frac{1}{g_{m2}g_{m3}(Y_{\pi 1}+g_{m1})R_{e1}}\right|^2 \left\{ \begin{array}{l} -\overline{i_{22}^{2}}g_{m3}Y_{\pi 1}[Y_{\pi 2}(R_{e1}+R_{e2})+(Y_{\pi 2}r_{b2}+1)][g_{m3}C_0-g_{m2}g_{m3}R_{e2}A_0]^{*} \\ +\overline{i_{31}^{2}}(g_{m3}C_1)(g_{m3}C_0)^{*} + \overline{i_{32}^{2}}(Y_{\pi 3}C_1)(Y_{\pi 3}C_0)^{*} \end{array} \right\} \quad (3\text{–}51)$$

We will use i_{ni} and e_{ni} to derive the HBT preamplifier's noise performance in Section 3.5.

3.1.4 DC bias and geometry scaling consideration

The objective of DC biasing and geometry scaling the HBT devices of a HBT gain cell is to optimize the HBT gain cell's performance. The components' values of the small signal model of a HBT device are determined by the geometry of the transistor as well as the DC bias applied. Therefore, the HBT gain cell's performance can be adjusted by changing the transistors' size as well as the DC bias.

First, we need appropriate effective input and output capacitances for the HBT gain cell, which will provide enough bandwidth for the DA. At the same time, the cell must provide adequate gain. From the input attenuation compensation point of view, we need to choose the transistors' size and bias them properly to get the adequate input attenuation compensation, which means to minimize the real part of the input impedance Z_i represented in Equation (3–26).

Since the base of the CB transistor Q_3 is grounded, the output admittance of the HBT gain cell is approximately equal to

$$Y_{out} = \frac{1}{r_{\mu 3}} + j\omega C_{\mu 3} \quad (3\text{–}52)$$

$C_{\mu 3}$ is the Collector-Base Junction Capacitance of the HBT device Q_3. In active-mode operation, the CBJ is reverse-biased; and its junction or depletion capacitance $C_{\mu 3}$

decreases as V_{CB} increases [15]. Therefore, the high frequency attenuation loss can be reduced by increasing V_{CB} across Q_3. Or the output attenuation loss of the gain cell can be reduced by increasing the DC bias voltage V_{CB} across transistor Q_3.

On the other hand, we need to consider the noise of the HBT gain cell. Since there are several intrinsic noise sources within the HBT gain cell as described in Section 3.1.3, the equivalent input noise current density that the HBT gain cells contribute to the preamplifier is much larger compared to the FETs DA. Therefore, we need reduce the noise of the gain cell as much as we can. From the noise model of a HBT device described at the beginning of this Chapter, we know that the noise current source i_1 and i_2 are proportional to the DC bias current I_b and I_c, respectively. Therefore, the transistors should be biased with the low DC currents from the noise point of view. However, reducing DC bias current will lead to low transistor gain as shown in Equation (3-1), as well as small output dynamic range. With all the factors considered, there have to be some tradeoffs for the gain cell's biasing and scaling.

3.2 Artificial Transmission Line Structure of DA

In section 3.1, we analyzed the HBT gain cell that will be used to build the DA. We now, consider the transmission line structure for the DA's input line and output line. As described in Chapter 2, the transmission line configuration of a distributed amplifier can be modeled by a low pass filter. In this thesis, m-derived LC filter construction is investigated for the DA application.

For the traveling-wave amplifier, the phase delay for the input/output line can be described by its propagation constant. Let's consider the phase delay of the ideal m-derived LC filter structure. The m-derived low pass T section described in Chapter 2 is redrawn here in Figure 3-7. In order to evaluate the cutoff frequency and characteristic impedance more conveniently, we use L_1, L_2 and C_{eq} to describe the m-derived section as shown in Figure 3-7.

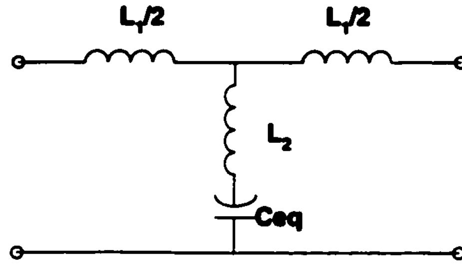


Figure 3-7 Low-pass m-derived T section

Comparing Figure 3-7 with Figure 2-7, we can write

$$L_1 = mL \tag{3–53a}$$

$$L_2 = \frac{1-m^2}{4m}L \tag{3–53b}$$

$$C_{eq} = mC \tag{3–53c}$$

Since

$$\omega_c = \frac{2}{\sqrt{LC}} \tag{2-6}$$

Replacing L and C with L_1, L_2 and C_{eq} in Equation (2-6), the cutoff frequency of the structure can be written in the following format:

$$\omega_c = \frac{2}{\sqrt{(L_1 + 4L_2)Ceq}} \tag{3–54}$$

Or

$$f_c = \frac{1}{\pi\sqrt{(L_1 + 4L_2)C_{eq}}} \tag{3–55}$$

The cutoff frequency f_c of the structure is the frequency transition point from the pass-band to stop-band for the LC low pass filter. Correspondingly, the characteristic impedance of the structure is

$$Z_0 = \sqrt{\frac{L_1}{C_{eq}}\left(1 - \frac{f^2}{f_c^2}\right)} \tag{3–56}$$

Now consider the propagation factor for the m-derived section. From Table 9.1 of David M. Pozar's *Microwave Engineering* [40], we know

$$e^{\gamma} = 1 + \frac{Z_1}{2Z_2} + \sqrt{\frac{Z_1}{Z_2}\left(1 + \frac{Z_1}{4Z_2}\right)} \tag{3–57}$$

For the low-pass m-derived filter,

$$Z_1 = j\omega L_1 \tag{3–58}$$

$$Z_2 = j\omega L_2 + \frac{1}{j\omega C_{eq}} \tag{3–59}$$

Then

$$\frac{Z_1}{Z_2} = \frac{j\omega L_1}{j\omega L_2 + \frac{1}{j\omega C_{eq}}} = -\frac{\omega^2 L_1 C_{eq}}{1 - \omega^2 L_2 C_{eq}} \tag{3–60}$$

and

$$1 + \frac{Z_1}{4Z_2} = 1 - \frac{\omega^2 L_1 C_{eq}}{4\left(1 - \omega^2 L_2 C_{eq}\right)} = \frac{4 - \omega^2 \left(L_1 + 4L_2\right) C_{eq}}{4\left(1 - \omega^2 L_2 C_{eq}\right)} \tag{3–61}$$

For $\omega < \omega_c$, we have $\frac{Z_1}{Z_2} < 0$, and $1 + \frac{Z_1}{4Z_2} > 0$. Therefore,

$$\left|e^{\gamma}\right|^2 = \left(1+\frac{Z_1}{2Z_2}\right)^2 - \frac{Z_1}{Z_2}\left(1+\frac{Z_1}{4Z_2}\right) = 1$$

$$\left|e^{\gamma}\right| = 1 \tag{3–62}$$

These results show γ is imaginary. Then

$$\gamma = \alpha + j\beta = j\beta \tag{3–63}$$

Thus, β can be calculated by

$$\cos\beta = 1 + \frac{Z_1}{2Z_2} = 1 - \frac{\omega^2 L_1 C_{eq}}{2\left(1-\omega^2 L_2 C_{eq}\right)} \tag{3–64}$$

For the traveling-wave amplifier, the phase delay for the input line and the output line has to be matched so that the output signal from each gain cell can add up in phase at the load, which means the propagation factor β is the same for input and output transmission lines. In order to get linear phase over broad bandwidth, the bandwidth of the DA has to be well below the cutoff frequency of the input and output transmission line structure. Usually, the 3dB bandwidth of the DA is about 70% of the cutoff frequency f_c of the transmission line [14]. In the implementation of the DA, there are several factors that contribute to the propagation factor of the transmission line structure, including input/output loss of the gain cell, the conductance loss of the circuit connections, as well as the parasitic elements of the circuit. The cutoff frequency of both lines usually should be around the same value to obtain a phase delay match.

A schematic of a distributed amplifier using HBT cells is illustrated in Figure 3-8, where the C_{eq} of Figure 3-7 is provided by the input or output capacitance of the gain cells.

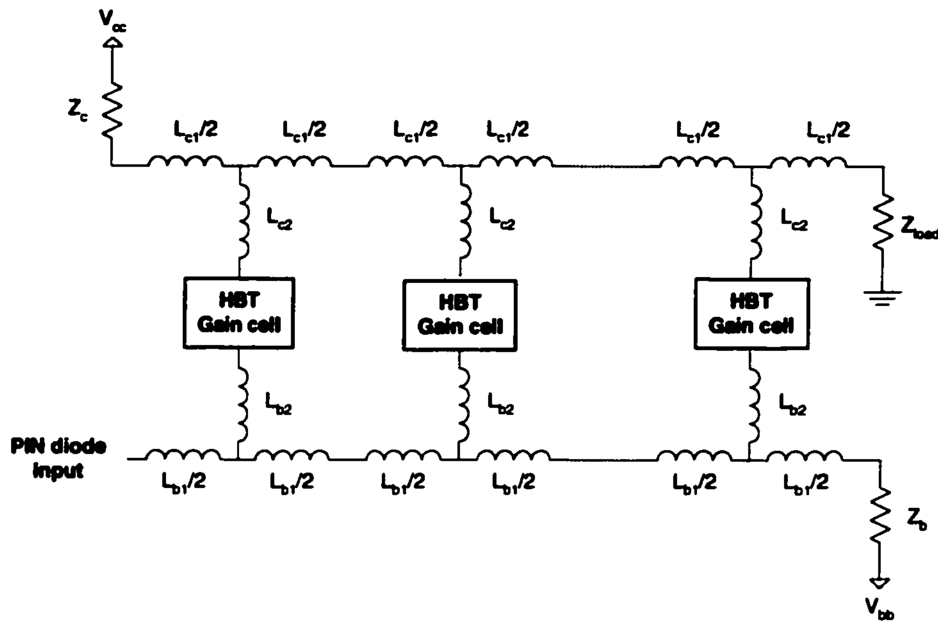


Figure 3-8 Schematic of a HBT distributed amplifier using HBT gain cells

The cutoff frequency of the input TRL structure is given by

$$f_{c_b} = \frac{1}{\pi\sqrt{(L_{b1} + 4L_{b2})C_{in}}} \tag{3–65}$$

Similarly, the cutoff frequency of the output TRL structure is given by

$$f_{c_c} = \frac{1}{\pi\sqrt{(L_{c1} + 4L_{c2})C_{out}}} \tag{3–66}$$

The inductors L_{b1}, L_{b2} and the equivalent input capacitor C_{in} of the HBT gain cell form the input transmission line with an impedance equal to

$$Z_b = \sqrt{L_{b1}/C_{in}} \quad (3\text{–}67)$$

Similarly, the output transmission line impedance is given by

$$Z_c = \sqrt{L_{c1}/C_{out}} \quad (3\text{–}68)$$

3.3 Preamplifier with Unmatched P-I-N diode input

MESFET distributed amplifiers have been used with the P-I-N photo diode to act as a preamplifier for the optical receiver application [5]-[8], [10], [11]. The distributed amplifier gives an alternative approach to a low noise, broad bandwidth photo-detection amplifier because of its unique structure [6]. Unlike the grounded source structure, the input impedance of the amplifier is the characteristic impedance of the transmission line, which is purely resistive and usually is 50Ω. Therefore no equalization circuit is required after the amplifier. The P-I-N photodiode is placed as the extended first stage of the input transmission line, and it will not give any reactive contribution to the input impedance since it is resistively terminated. The frequency response of the amplifier is flat up to its cut-off point.

A resistive source of the distributed amplifier can be obtained by building the P-I-N diode into a π-section network as shown in Figure 3-9. The P-I-N capacitance forms one shunt capacitor, a capacitor of identical capacitance is used as the second shunt component and the series inductance is selected so that the low frequency value of $Z_{\pi g}$ is equal to $50\,\Omega$, which is the input impedance of the distributed amplifier. If the left hand port of this network is terminated in a load equal to $Z_{\pi g}$ and the right hand port is connected to the distributed amplifier, then the P-I-N photo detector will effectively be integrated into the distributed amplifier gate line.

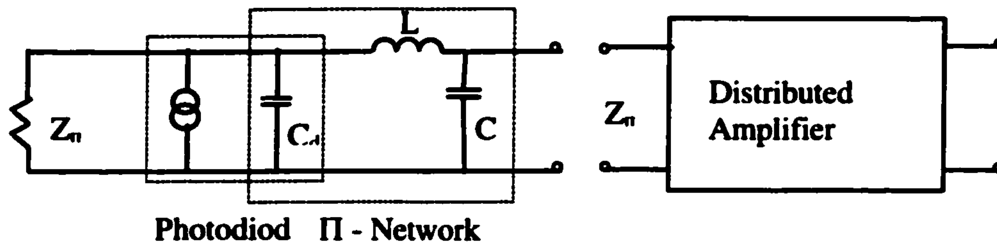


Figure 3-9 Distributed amplifier with π-section containing P-I-N diode

The optical receiver also can be the combination of a distributed amplifier and P-I-N diode with unmatched input termination as shown in Figure 3-10. For the unmatched-termination configuration, an un-encapsulated photodiode is embedded in a half π-section, which also behaves like an extension of the gate artificial transmission line. However, there is no matched termination at the input, and the input impedance to the gate line of the amplifier is totally unmatched. The advantages of this configuration is to increase the output signal, as well as to increase the output signal-to-noise ratio, as the distributed amplifier is driven by the total current from the photodiode, unlike the matched case in which half of the current was dissipated in the input termination.

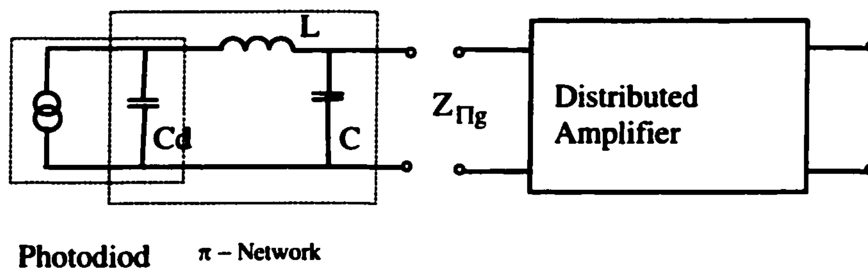


Figure 3-10 Distributed amplifier with unmatched P-I-N diode

The high-speed photodetector configurations have been fabricated by using a distributed amplifier and P-I-N photodiode combinations. Both input matched and unmatched

configurations have been investigated [10], [11]. The unmatched termination circuit gives more gain, and less average equivalent input noise current than the matched case. Therefore, we use the unmatched P-I-N distributed amplifier configuration for the designed HBT preamplifier.

A schematic of a preamplifier including a P-I-N and an HBT distributed amplifier is illustrated in Figure 3-11.

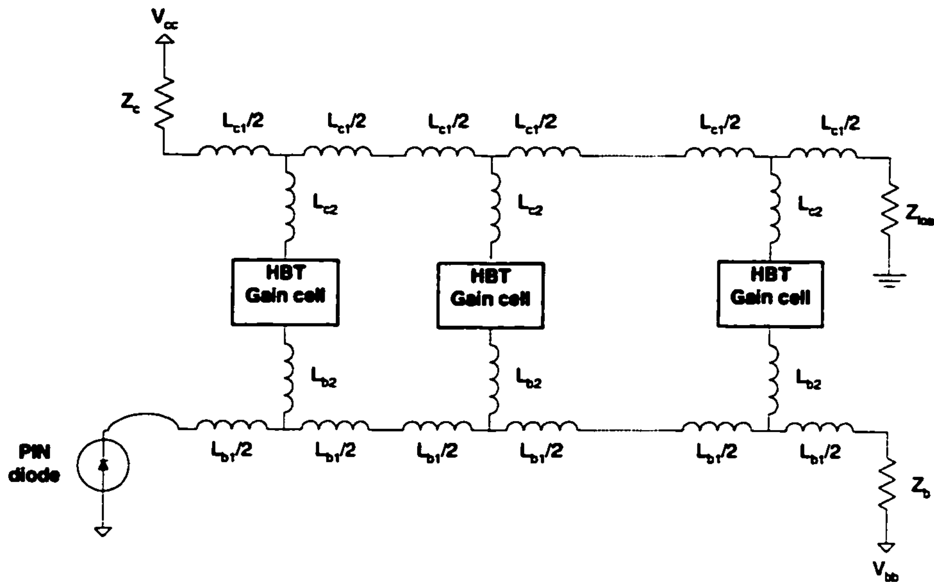


Figure 3-11 Preamplifier – P-I-N and HBT distributed amplifier combination

In Section 3.4 and Section 3.5, we will derive the trans-impedance gain and equivalent input noise current densities of the HBT preamplifier shown in Figure 3-11.

3.4 Trans-impedance Gain Analysis of the HBT Preamplifier

3.4.1 Forward Trans-impedance Gain

For optical receivers, the transimpedance gain, defined as the ratio of the output voltage signal to the input photocurrent, is given as the product of the amplifier's input impedance and voltage gain. In this Section, we will derive the trans-impedance gain of the HBT preamplifier shown in Figure 3-11 by following the similar analysis method as in [8].

For the ideal input transmission line of the DA, the voltage at the input of the ith HBT gain cell is given by

$$v_i = v_{in} \cdot e^{-j\left(i-\frac{1}{2}\right)\phi_b}, \quad i=1,2,\ldots,N \tag{3–69}$$

Then

$$i_i = -G \cdot v_{in} \cdot e^{-j\left(i-\frac{1}{2}\right)\phi_b} \tag{3–70}$$

i_{out} is defined as the total current delivered to the load by a DA with N stages, then following expression can be obtained under lossless ATL conditions

$$i_{out} = \frac{1}{2}\left[i_1 e^{-j\left(N-\frac{1}{2}\right)\phi_c} + i_2 e^{-j\left(N-\frac{3}{2}\right)\phi_c} + \cdots + i_N e^{-j\frac{1}{2}\phi_c}\right] \tag{3–71}$$

Substituting (3–70) into (3–71) gives

$$i_{out} = -\frac{1}{2} G \cdot v_{in} \cdot \left[e^{-j\left[\left(N-\frac{1}{2}\right)\phi_c + \frac{1}{2}\phi_b\right]} + e^{-j\left[\left(N-\frac{3}{2}\right)\phi_c + \frac{3}{2}\phi_b\right]} + \cdots + e^{-j\left[\frac{1}{2}\phi_c + \left(N-\frac{1}{2}\right)\phi_b\right]}\right] \tag{3–72}$$

Using the equation $\sum_{n=0}^{N-1} a_n = \frac{1-a^N}{1-a}$ gives

$$i_{out} = -\tfrac{1}{2} G \cdot v_{in} \cdot e^{-j\left[\left(N-\frac{1}{2}\right)\phi_c + \frac{1}{2}\phi_b\right]} \frac{e^{-j\frac{N}{2}(\phi_b - \phi_c)} \sin \frac{N}{2}(\phi_b - \phi_c)}{e^{-j\frac{1}{2}(\phi_b - \phi_c)} \sin \frac{1}{2}(\phi_b - \phi_c)} \tag{3–73}$$

Under the condition of phase matching, $\phi_b = \phi_c = \phi$, Equation (3–73) becomes

$$i_{out} = -\tfrac{1}{2} G \cdot v_{in} \cdot N \cdot e^{-jN\phi} \tag{3–74}$$

Since

$$v_{in} = i_s \cdot Z_{\pi b} \tag{3–75}$$

Where i_s is the source current. Then,

$$i_{out} = -\tfrac{1}{2} G \cdot (i_s \cdot Z_{\pi b}) \cdot N \cdot e^{-jN\phi} \tag{3–76}$$

$$v_{out} = i_{out} \cdot Z_{\pi c} = -\tfrac{1}{2} N \cdot G \cdot (Z_{\pi c} \cdot Z_{\pi b}) \cdot e^{-jN\phi} \cdot i_s \tag{3–77}$$

Therefore, the forward trans-impedance gain is obtained by

$$Z_f = \frac{v_{out}}{i_s} = -\tfrac{1}{2} N \cdot G \cdot (Z_{\pi c} \cdot Z_{\pi b}) \cdot e^{-jN\phi} \tag{3–78}$$

Obviously, the trans-impedance gain of the preamplifier is proportional to the HBT cell's trans-conductance G, base termination impedance $Z_{\pi b}$, and collector termination impedance $Z_{\pi c}$.

3.4.2 Reverse Trans-impedance Gain

The reverse trans-impedance gain of the distributed amplifier is defined as the ratio between the voltage that appears at the collector termination and the input current. The reason that we define and derive the reverse transimpedance gain for the DA is this

expression will be used in next section's HBT preamplifier's noise analysis. Under a similar analysis as the forward gain,

$$i_{\pi c} = \frac{1}{2}\left[i_1 e^{-j(\frac{1}{2}\phi_c)} + i_2 e^{-j(\frac{3}{2})\phi_c} + \cdots + i_N e^{-j(N-\frac{1}{2})\phi_c}\right] \tag{3-79}$$

Substituting (3-70) into (3-79) gives

$$i_{\pi c} = -\frac{1}{2} G \cdot v_{in} \cdot \left[e^{-j(\frac{1}{2}\phi_c + \frac{1}{2}\phi_b)} + e^{-j(\frac{3}{2}\phi_c + \frac{3}{2}\phi_b)} + \cdots + e^{-j(N-\frac{1}{2})(\phi_c + \phi_b)}\right] \tag{3-80}$$

$$i_{\pi c} = -\frac{1}{2} G \cdot v_{in} \cdot e^{-j\frac{N}{2}(\phi_c + \phi_b)} \frac{\sin\frac{N}{2}(\phi_b + \phi_c)}{\sin\frac{1}{2}(\phi_b + \phi_c)} \tag{3-81}$$

At $\phi_b = \phi_c = \phi$, we have

$$i_{\pi c} = -\frac{1}{2} G \cdot v_{in} \cdot e^{-jN\phi} \cdot \frac{\sin N\phi}{\sin\phi} \tag{3-82}$$

Then, the reverse transimpedance can be obtained as

$$Z_r = \frac{v_{\pi c}}{i_s} = -\frac{1}{2} G \cdot Z_{\pi b} \cdot Z_{\pi c} \cdot e^{-jN\phi} \cdot \frac{\sin N\phi}{\sin\phi} \tag{3-83}$$

3.5 Noise Analysis of HBT Preamplifiers

For the preamplifier, the input equivalent noise current density is used popularly to describe the noise performance rather than the noise figure. A noise analysis theory for the FET distributed amplifier was developed in [5], [8]. Here we are going to derive the input equivalent noise current densities for the suggested HBT preamplifier by following

the similar analysis method. This noise analysis for the HBT distributed amplifier is based on the noise network of the HBT gain cell, which is described in Section 3.1.3.

For the input unmatched preamplifier shown in Figure 3-11, the circuit includes following noise sources:

- Noise from the base termination $Z_{\pi b}$;
- Noise from the collector termination $Z_{\pi c}$;
- Noise from the HBT gain cell of the DA;

3.5.1 Noise from the base/collector line terminations

The base and collector terminations are resistive. Therefore, the single-sided thermal noise current densities are given by

$$|i_{z\pi b}|^2 = \frac{4kT}{Z_{\pi b}} \tag{3-84}$$

$$|i_{z\pi c}|^2 = \frac{4kT}{Z_{\pi c}} \tag{3-85}$$

The equivalent input noise current density from the base termination $Z_{\pi b}$ is given by [8]

$$|i_{n1}|^2 = \frac{|i_{z\pi b}|^2}{4}\left|1 + \frac{Z_r}{Z_f}e^{jN\phi}\right|^2 = \frac{|i_{z\pi b}|^2}{4}\left|1 + \frac{\sin N\phi}{N\sin\phi}e^{jN\phi}\right|^2 \tag{3-86}$$

The equivalent input noise current density from collector termination $Z_{\pi c}$ is equal to [8]

$$|i_{n2}|^2 = \frac{|i_{z\pi c}|^2}{4}\left|\frac{Z_{\pi c}}{Z_f}\right|^2 \tag{3-87}$$

3.5.2 Noise from the HBT gain cells

The total equivalent input noise density of the N HBT gain cells is equal to the square sum of each cell's noise density referred to the input. Consider the noise sources of rth stage HBT gain cell. As discussed in Section 3.1.1, the noise model of the HBT gain cell (shown in Figure 3-5) can be represented as a noiseless two-port network with a voltage noise generator (e_{ni}) and a current noise generator (i_{ni}) connected at its input, which is redrawn below.

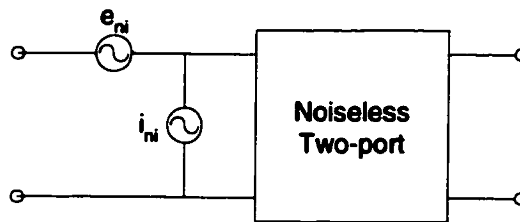


Figure 3-12 Chain representation of a noisy network for the HBT gain cell

First, let's consider the voltage noise generator e_{ni}'s noise contribution to the preamplifier. Since the HBT gain cell has very high input impedance, the voltage over the input of the two-port network due to the noise voltage e_{ni} is approximately e_{ni}. Therefore, the output current over the load due to e_{ni} is given by

$$i_{e_{ni}}{}^{r} = \frac{1}{2} G \cdot e_{ni} \cdot e^{-j\left(N-r+\frac{1}{2}\right)\theta_c} \tag{3-88}$$

The noise voltage over the load is

$$v_{e_{ni}}{}^{r} = i_{e_{ni}}^{r} Z_{\pi c} = \frac{1}{2} G \cdot e_{n} \cdot Z_{\pi c} e^{-j\left(N-r+\frac{1}{2}\right)\theta_c} \tag{3-89}$$

Now, we will look at the current noise generator i_{ni}'s noise contribution to the preamplifier. The noise current wave can be broken into three components. The first component is the forward traveling wave, which will produce an output voltage due to the forward trans-impedance gain. The second is the reverse traveling wave, which will produce an output voltage due to the reverse trans-impedance gain. Finally, the third component is the reflected wave, which is due to the reverse wave reflecting back from the open circuit at the input. This wave will produce an output voltage as a result of the forward trans-impedance gain, also.

Defining the output current due to the forward traveling wave as i_{out}^{for} results in the following expression,

$$i_{out}^{for} = \tfrac{1}{2}\left[i_r^{for} e^{-j\left(N-r+\frac{1}{2}\right)\phi_c} + i_{r+1}^{for} e^{-j\left(N-r-\frac{1}{2}\right)\phi_c} + \cdots + i_N^{for} e^{-j\frac{1}{2}\phi_c}\right] \quad (3\text{–}90)$$

Where i_{r+i}^{for} is the collector current due to forward traveling wave at $(r+i)^{th}$ cell's input, which is given by

$$i_{r+i}^{for} = G \cdot v_{r+1} = \tfrac{1}{2} G \cdot i_{ni} \cdot Z_{\pi b} \cdot e^{-j \cdot i \cdot \phi_b}, \quad i=0,1,2,\ldots,(N-r) \quad (3\text{–}91)$$

Using a similar method as used to derive the forward gain, we can obtain

$$i_{out}^{for} = \tfrac{(N-r+1)}{4} G \cdot i_{ni} \cdot Z_{\pi b} \cdot e^{-j \cdot (N-r+1)\phi} \quad (3\text{–}92)$$

Similarly, the output current due to reverse traveling wave, i_{out}^{rev} is given by

$$i_{out}^{rev} = \tfrac{1}{4} G \cdot i_{ni} Z_{\pi b} \frac{\sin(r-1)\phi}{\sin\phi} e^{-j \cdot (N+r-\frac{1}{2})\phi} e^{j(r-1)\phi} \quad (3\text{–}93)$$

The output current due to the reflected noise current wave can be shown to be,

$$i_{out}^{refl} = \tfrac{1}{4} G \cdot i_{ni} \cdot Z_{\pi b} \cdot e^{-j \cdot (N+r-\frac{1}{2})\phi} N \quad (3\text{–}94)$$

The total output current due to the noise current i_{ni} of the rth cell is

$$\begin{aligned} i_{out} &= i_{out}^{for} + i_{out}^{refl} + i_{out}^{rev} \\ &= \tfrac{1}{4} G \cdot i_{ni} Z_{sb} e^{-j\cdot(N+r-\frac{1}{2})\phi} \left[N + (N-r+1)e^{j(2r-1)\phi} + \frac{\sin(r-1)\phi}{\sin\phi} e^{j(r-1)\phi} \right] \end{aligned} \tag{3-95}$$

Therefore, the resulting output voltage is,

$$\begin{aligned} v_{out} &= i_{out} Z_{sc} \\ &= \tfrac{1}{4} N \cdot G \cdot i_{ni} Z_{sb} Z_{sc} e^{-j\cdot(N+r-\frac{1}{2})\phi} \left[1 + \frac{(N-r+1)}{N} e^{j(2r-1)\phi} + \frac{1}{N} \frac{\sin(r-1)\phi}{\sin\phi} e^{j(r-1)\phi} \right] \end{aligned} \tag{3-96}$$

Substituting the expression for trans-impedance gain in Equation (3–78) into (3–96) gives

$$v_{out} = \tfrac{1}{2} i_{ni} Z_f e^{-j\cdot(r-\frac{1}{2})\phi} C(r,\phi) \tag{3-97}$$

Where

$$C(r,\phi) = 1 + \frac{(N-r+1)}{N} e^{j(2r-1)\phi} + \frac{1}{N} \frac{\sin(r-1)\phi}{\sin\phi} e^{j(r-1)\phi} \tag{3-98}$$

Thus, the total output noise voltage due to the rth HBT gain cell is as follow,

$$v_{out}^{r} = \tfrac{1}{2} i_{ni} Z_f e^{-j\cdot(r-\frac{1}{2})\phi} C(r,\phi) + \frac{1}{2} G \cdot e_{ni} \cdot Z_{sc} e^{-j(N-r+\frac{1}{2})\phi} \tag{3-99}$$

The equivalent input noise current due to the output noise voltage in (3–99) is

$$\left| i_n^r \right|^2 = \frac{\left| i_{ni} \right|^2}{4} \left| C(r,\phi) \right|^2 + \frac{\left| e_{ni} \right|^2}{4} \left| \frac{GZ_{sc}}{Z_f} \right|^2 + \frac{1}{2} \mathrm{Re}\left[i_{ni} e_{ni}^{*} \left(\frac{GZ_{sc}}{Z_f} \right)^{*} C(r,\phi) e^{j(N-2r+1)\phi} \right] \tag{3-100}$$

Assuming that the noise sources for all the gain cells are the same, the total equivalent input noise current density of all HBT gain cells is equal to

$$\left|i_{n3}\right|^2 = \frac{\left|i_{ni}\right|^2}{4}\sum_{r=1}^{N}\left|C(r,\phi)\right|^2 + \frac{\left|e_{ni}\right|^2}{4}\left|\frac{GZ_{\pi}}{Z_f}\right|^2 N + \frac{1}{2}\sum_{r=1}^{N}\mathrm{Re}\left[i_{ni}e_{ni}^{*}\left(\frac{GZ_{\pi}}{Z_f}\right)^{*} C(r,\phi)e^{j(N-2r+1)\phi}\right] \quad (3-101)$$

Equation (3−86), (3−87), and (3−101) gives the total equivalent input noise current density of the preamplifier, which is

$$\sqrt{\left|i_n\right|^2} = \sqrt{\left|i_{n1}\right|^2 + \left|i_{n2}\right|^2 + \left|i_{n3}\right|^2}$$
$$= \sqrt{\frac{\left|i_{Z\pi b}\right|^2}{4}\left|1 + \frac{Z_r}{Z_f}e^{jN\phi}\right|^2 + \frac{\left|i_{Z\pi}\right|^2}{4}\left|\frac{Z_{\pi}}{Z_f}\right|^2 + \frac{\left|i_{ni}\right|^2}{4}\sum_{r=1}^{N}\left|C(r,\phi)\right|^2 + \frac{\left|e_{ni}\right|^2}{4}\left|\frac{GZ_{\pi}}{Z_f}\right|^2 N + \frac{1}{2}\sum_{r=1}^{N}\mathrm{Re}\left[i_{ni}e_{ni}^{*}\left(\frac{GZ_{\pi}}{Z_f}\right)^{*} C(r,\phi)e^{j(N-2r+1)\phi}\right]} \quad (3-102)$$

Where $\overline{i_{ni}^2}$, $\overline{e_{ni}^2}$ and $i_{ni}e_{ni}^{*}$ are given by Equations (3-49) to (3-51) in Section 3.1.3. The forward transimpedance gain Z_f of the DA was already derived in Section 3.1.3, which is represented in Equation (3-78).

$$Z_f = \frac{v_{out}}{i_s} = -\tfrac{1}{2}N \cdot G \cdot (Z_{\pi} \cdot Z_{\pi b}) \cdot e^{-jN\phi} \quad (3-78)$$

And

$$\left|i_{z\pi b}\right|^2 = \frac{4kT}{Z_{\pi b}} \quad (3-84)$$

Obviously, Z_f is proportional to $Z_{\pi b}$. $\left|i_{z\pi b}\right|^2$ is proportional to $\frac{1}{Z_{\pi b}}$. By checking Equation (3−102), we can easily see that increasing $Z_{\pi b}$ will decease the 1st, 2nd, 4th and 5th item of $\left|i_n\right|^2$. Therefore, the equivalent input noise current density of a HBT preamplifier can be reduced by increasing $Z_{\pi b}$. The effect of increasing $Z_{\pi b}$ is twofold: It increases the trans-impedance gain Z_f. At same time, it reduces the magnitude of the equivalent noise current density. However, increasing $Z_{\pi b}$ will lead low cutoff frequency for the input distributed structure, which will limit the bandwidth of a distributed amplifier.

The equivalent input noise current density of a HBT preamplifier, the details of which are designed in Chapter 5, was calculated based on Equation (3–102). Figure 3-13 shows Equation (3–102)'s five term's contribution to the equivalent input noise current density. Curves Term1 to Term5 represent 1st to 5th term of Equation (3–102), respectively. At low frequencies, the first term of Equation (3-102), the noise contribution of $Z_{\pi b}$ dominates the preamplifier's equivalent input noise current density. Terms 3, 4 and 5, the noise contributions of the gain cells, are small at low frequencies, and increase moderately with frequency. Thus, the gain cell's noise contribution dominates at high frequency. Compared to others, second term, $Z_{\pi c}$'s noise contribution is relatively small. In order to improve high frequency noise performance, the noise source of the gain cell should be reduced. This can be achieved by reducing the bias current of the HBTs.

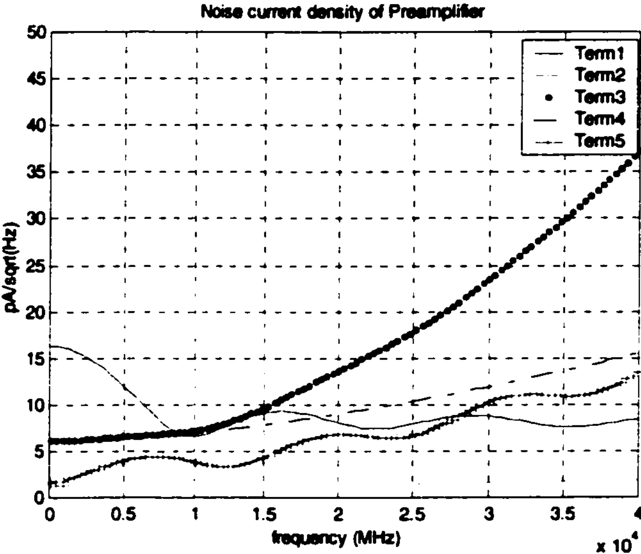


Figure 3-13 Equivalent input noise current density for the HBT preamplifier based on theoretical analysis

Figure 3-14 shows the comparison between the theoretically calculated result and the Hspice simulated result for the preamplifier's equivalent input noise current density. The Hspice curve accounts for artificial transmission line losses of the preamplifier, which

have not been included in the analytical expression. Therefore, the noise prediction by Hspice is higher, as expected. Nonetheless, the agreement is seem to be very good, within 5 $pA/\sqrt{Hz}$.

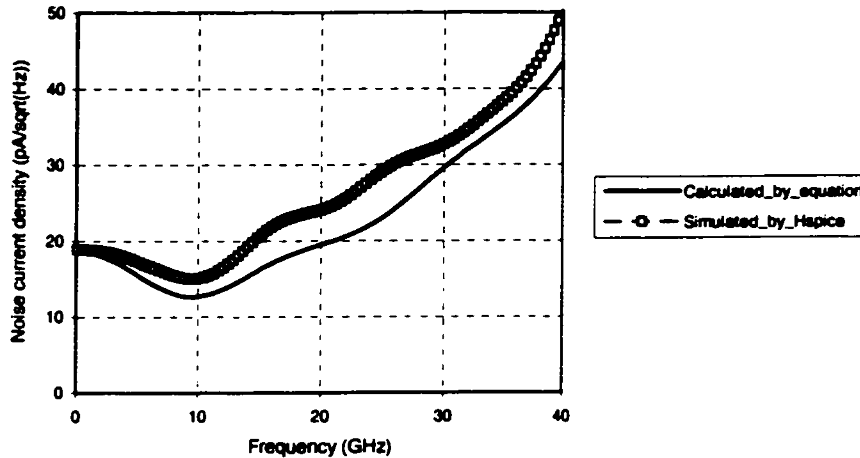


Figure 3-14 Equivalent input noise current densities --- theoretic analysis vs. Hspice simulation

3.6 Conclusion

The MMIC HBT preamplifier design involves many aspects of knowledge and different kind of techniques. In this Chapter, we investigated the techniques that were applied to this HBT preamplifier design, including small signal circuit analysis for the HBT gain cell, noise network theory analysis, as well as transmission line structure investigation. Detailed derivation of the gain and the equivalent input noise current density for the HBT preamplifier is described. Agreement between the noise analysis and Hspice simulation is good. These investigation results were used in the implementation of the designed HBT preamplifier. The analysis in this Chapter will be useful for other HBT distributed preamplifiers' design in future.

Chapter 4 Measurement Techniques for High Speed P-I-N photodiode

Broadband measurement systems of high-speed P-I-N photo-detectors are demonstrated using the pulse response and optical heterodyning techniques [43]. Short pulse (<2ps FWHM (full width at half maximum)) response of the P-I-N diode was measured at 1.5μm. Scalar measurement of the P-I-N diode in the frequency domain was implemented at 1.5μm, as well. The results of the two techniques are compared with the effects of the measurement equipment removed.

4.1 Introduction

To achieve ultrahigh speed optical communication systems, it is very important to develop wideband optical devices such as laser diodes, P-I-N photodiodes and preamplifiers. At the same time, it is necessary to characterize the response of these devices. A P-I-N photodiode plays an essential role in high-speed optical receivers, converting the input optical signal into electrical current. In order to achieve the predicted performance for a high-speed receiver system, it is important to have an accurate model for the P-I-N diode.

We are developing ultra-wide band preamplifiers, which together with P-I-N diodes are to be used in receivers of high-speed optical communication systems. Since any packaging will have an effect at high frequency, the chip circuit implementation calls for the P-I-N diodes to be connected to the preamplifiers directly at the chip level. Therefore, we need to characterize the unpackaged P-I-N diodes in order to specify appropriate preamplifier performance. This presents some difficulty for the diode measurements, especially with regard to the set up of the measurement. Microwave probes, a bias tee as well as connectors are needed for the P-I-N diode measurement.

Since these components each have a frequency response of their own, it is necessary to properly calibrate the measurement system in order to obtain an accurate measurement.

The modeling of the P-I-N photodiode can be divided into two parts: one is to measure the one-port S-parameter S_{11}, which provides the electrical equivalent model of the diode. From S_{11}, the parameters of the electrical model can be optimized by a circuit simulator. The second part is to measure the diode's response to an optical input signal, which leads to its transmission characteristics.

There are a number of photo-detector response measurement techniques [44]-[48]. Two different techniques were used in our measurements: pulse response (time domain) and optical heterodyning (frequency domain).

This Chapter first describes the reflection coefficient and optical response measurement techniques employed in our P-I-N diode characterization. Then, the broadband calibration results for the various components used in the experimental setup are presented. Finally, the optical response of a P-I-N diode is measured using the two techniques and the results are compared.

4.2 Measurement Procedure

The full characterization of a P-I-N diode requires determining its equivalent electrical model based on microwave reflection coefficient measurement, as well as its response to an optical input. Figure 4-1 shows the picture of the measured P-I-N diode.

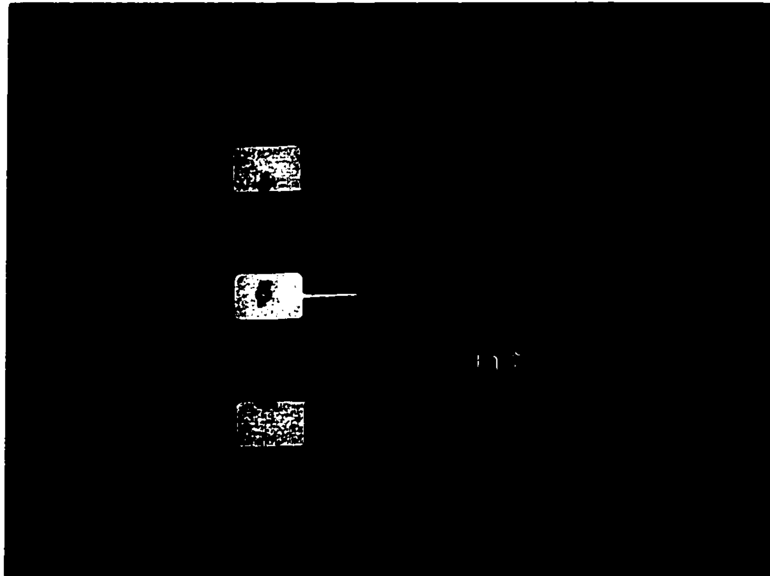


Figure 4-1 Picture of a P-I-N diode

4.2.1 Reflection Coefficient Measurement

The reflection coefficient S_{11} of the P-I-N diode provides the electrical parameters of the diode such as junction capacitance, series resistance, track inductance and parasitic capacitance, as shown in Figure 4-2 [11]. The S_{11} was measured up to 40 GHz using an HP8510C Network Analyzer. The electrical modeling of the P-I-N photodiode could then be derived from its S_{11} with the use of a circuit simulator and optimizer.

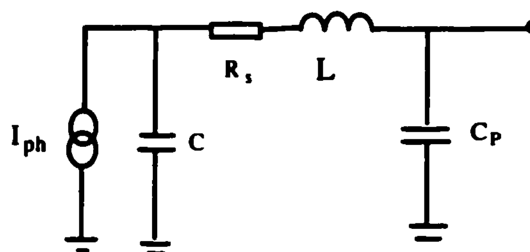


Figure 4-2 Electrical model of a P-I-N diode

The typical value for the derived electrical model of the measured P-I-N diodes with –5.0 V DC bias is listed in the Table 4-1. Although the equivalent circuit is sufficient for impedance matching purposes, it does not give the frequency response of the P-I-N diode to an optical input. This can be found from the optical response measurements given in the following section.

Table 4-1 Parameters of P-I-N diode electrical model

Diode ID	C_j (fF)	R_s (Ω)	L (nH)	C_p (fF)
a	51.6	14.2	0.152	0.0
b	56.8	25.0	0.131	0.0
c	59.7	18.6	0.114	0.0

4.2.2 Optical Response Measurement

As stated earlier, the pulse response [47], [48] and optical heterodyning [45]-[47] techniques were used for our measurements. Pulse response data can be converted into frequency domain response by using a Fourier Transform, which includes both the scalar (magnitude) information and phase information. This allows prediction of the influence of the detector on eye diagrams in a digital modulation scheme. On the other hand, the measurement with the optical heterodyne technique only offers the scalar information in the frequency domain.

Pulse Response Measurement

A short pulse (<2 ps full width at half maximum (FWHM)) response of the P-I-N diodes was measured at 1.5μm optical wavelength. The measurement system is shown schematically in Figure 4-3. A 1.5μm Soliton Erbium-doped Fiber Laser is used as a short optical pulse generator. The optical pulse signal is fed into a P-I-N diode biased at 5V, through a cleaved optic fiber. The electrical signal of the P-I-N diode goes through

wafer probes (Picoprobe, 40A-GSG-175), a short cable, a bias tee (Wiltron K250), then into a HP Sampling Oscilloscope. All the connectors used in the measurement systems are K connectors rated up to 40 GHz.

The response of the P-I-N diode to the 1.5μm short pulse, as measured by the oscilloscope, is a data record covering up to 10ns. Since the P-I-N diode is unmatched, and there are reflections due to the connectors along the signal path, reflected signals appear beyond 0.8ns. In order to reduce the errors caused by these reflections, only the first 0.8192 ns data record of the response is kept. The pulse response shown in Figure 4-4 is an averaged result over 512 samples. Figure 4-5 shows the input optical pulse used to generate the pulse response.

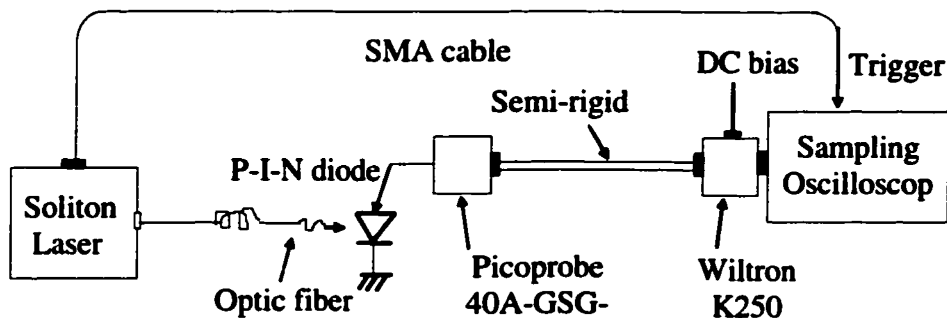


Figure 4-3 Schematic of pulse response measurement system

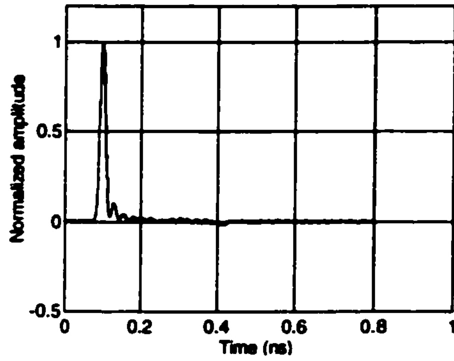


Figure 4-4 P-I-N diode's optical response

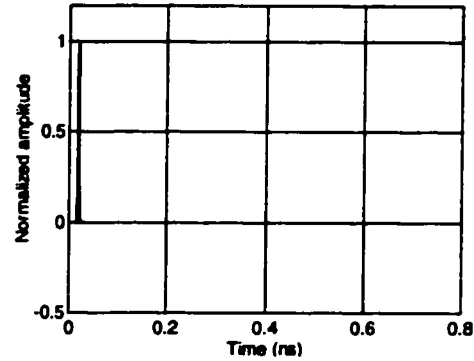


Figure 4-5 Input optical pulse (2-ps FWHM pulse)

If the measurement setup forms a linear system, the measured pulse response is the convolution of the optical pulse intensity waveform, with the impulse response of the photo-detector, probes, cable and bias Tee, oscilloscope sampling head, and timing jitter. Thus, the calibration of the system components is a necessary part of the measurement. Based on the above, the measured response is given by

$$h_{meas}(f) = h_{optic}(f) * h_{pin}(f) * h_{probe}(f) * h_{cable}(f) * h_{samp}(f) * h_{jit}(f)$$

Where * denotes convolution. The response of the P-I-N diode, $h_{pin}(f)$, can be deduced from the measured response $h_{meas}(f)$, by de-convolution of the effects of the remainder of the system [48], $h_{optic}(f)$, $h_{probe}(f)$, etc. De-convolution can be implemented in either the time domain or the frequency domain. We choose to use a fast Fourier transform to allow de-convolution in the frequency domain. The required Fourier transfer functions, corresponding to $h_{optic}(f)$, $h_{probe}(f)$, $h_{cable}(f)$, $h_{samp}(f)$ and $h_{jit}(f)$ are obtained in Section 4.3.

Optical Heterodyne Technique

The P-I-N diodes were also measured using the optical heterodyne technique at 1.5 μm. Our optical heterodyne measurements utilize two 1550 nm DFB Lasers beating as an optical swept frequency generator [45], [46]. The frequency of each laser is varied by controlling the temperature of the DFB Laser, and is monitored on an optic spectrum analyzer. By sweeping the optical frequency of one of the lasers, a frequency response of the P-I-N diode can be measured. The optical heterodyne measurement system is shown schematically in Figure 4-6. The output of the P-I-N diode containing an IF signal, is introduced into a spectrum analyzer.

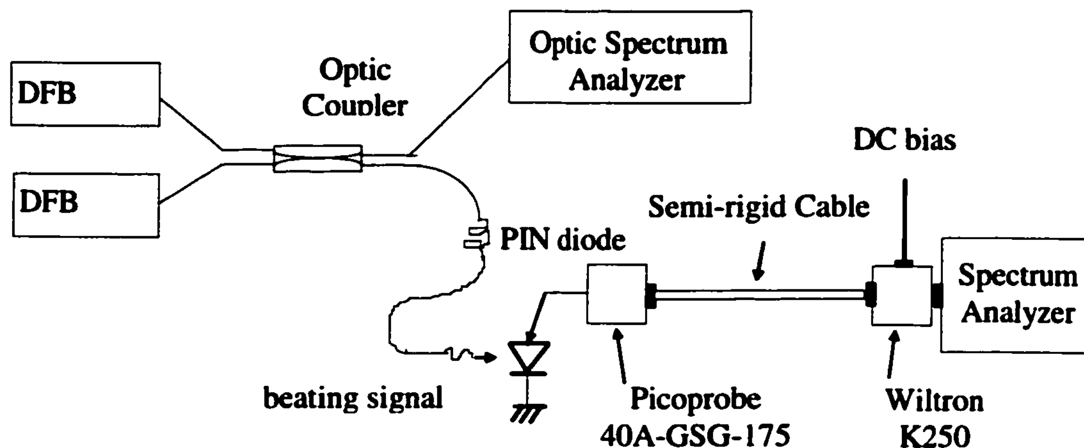


Figure 4-6 Schematic of optical heterodyne measurement system

4.3 Measurement Results

The measurement techniques described have been used to completely characterize a photo detector up to 40 GHz. Measurement of the reflection coefficient of the diode is a straightforward procedure, identical to any other on-wafer IC measurement, and will not be discussed further. An important part of the remaining techniques is the calibration of the measurement system.

4.3.1 Calibration

For the pulse response measurement, the calibration includes characterization of the probes, cable, bias tee, oscilloscope sampling head, as well as trigger jitters. For the optical heterodyne technique, only the calibration of the probes, cable and bias tee is needed. For the pulse response measurement, scalar de-convolution is used to obtain the frequency response with the effects of the measurement apparatus removed.

The frequency response of the oscilloscope sampling head was measured by sweeping the RF frequency of a microwave source. First, the input power level is accurately characterized by using a microwave power meter (up to 50 GHz). Second, the CW amplitude as a function of frequency is measured on the oscilloscope. Then, by normalizing the CW amplitudes at different frequencies to the same power level, the frequency response of the oscilloscope sampling head is obtained, as shown in Figure 4-7. It is seen that the oscilloscope introduces a loss of approximately 2dB at 40 GHz.

The attenuation of the probes, cable and bias Tee was measured using a network analyzer. The typical results are shown in Figure 4-8 and Figure 4-9, indicating that these components also contribute approximately 2dB attenuation at 40 GHz, respectively.

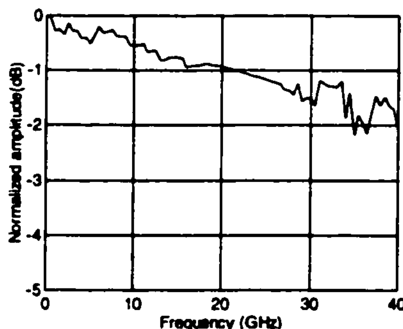


Figure 4-7 Frequency Response of Oscilloscope

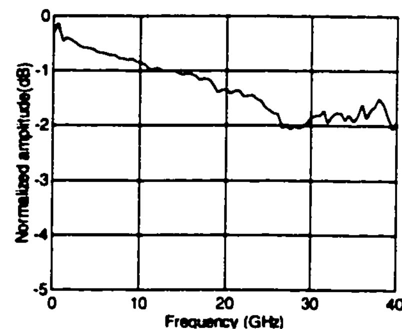


Figure 4-8 Attenuation of cable and bias Tee

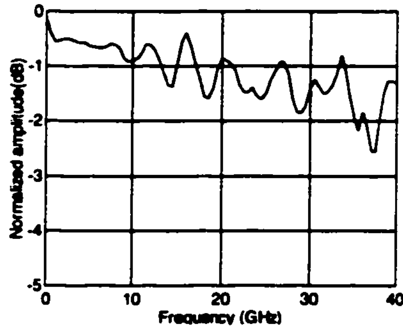


Figure 4-9 Attenuation of probe

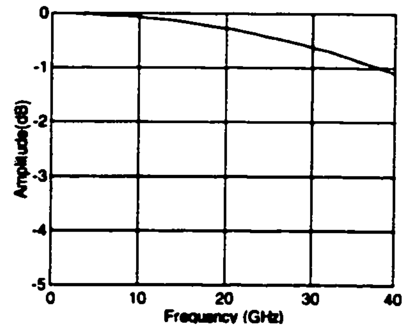


Figure 4-10 Effect of trigger jitter

The effect of oscilloscope timing jitter needs to be considered in the presence of averaging results [49]. Trigger jitter was measured as a time-domain histogram of the density of sampled points versus time on the falling edge of the pulse response signal, accumulated over a time internal. The jitter probability distribution function (internally generated by the HP54120 Sampling Oscilloscope) can be converted into frequency domain response by using a Fourier Transform. Figure 4-10 shows a typical contribution of trigger jitter. Finally, Figure 4-11 shows the frequency transformation of the input optical pulse shown in Figure 4-5.

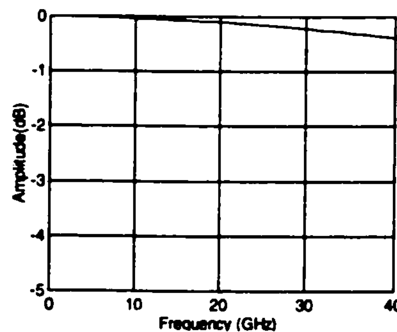
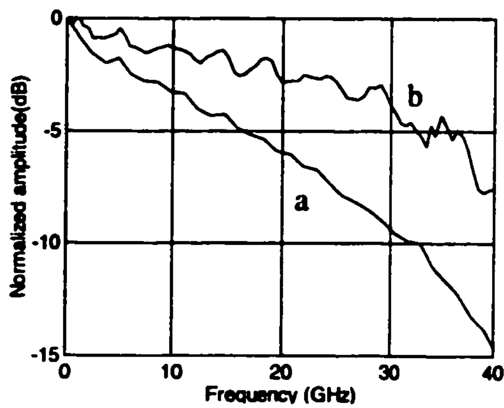


Figure 4-11 Fourier transfer function of the input optical pulse

4.3.2 The Optical Response of P-I-N Diode

For both sets of measurements, corrected results are obtained in the frequency domain. The corrected scalar results of the frequency response are compared. The measurement results are very reproducible. Figure 4-12 shows the frequency response of the P-I-N diode using pulse response technique before and after the calibration is applied. Figure 4-13 shows the frequency response of the P-I-N diode measured by the heterodyne technique, also with and without calibration. From these figures, we can see that the measurement results before and after calibration are quite different, especially at high frequency where the difference is as large as 7dB. Since the measurement goes up to 40 GHz, the attenuation of the system components becomes significant. The calibration of the measurement system is thus a very important part of the very high frequency measurement.

Figure 4-14 shows the corrected results at the frequency domain for both sets of measurements. The difference between two measurement results is within 2 dB. With proper use of gating in the pulse response measurement, the effects of spurious reflections caused by the unmatched P-I-N diode, connectors and other measurement system components can be nearly eliminated. These effects cannot be removed from the optical heterodyne technique. The results from pulse response measurement curve (a) are therefore preferred, and would be in the case of any unmatched device under test.



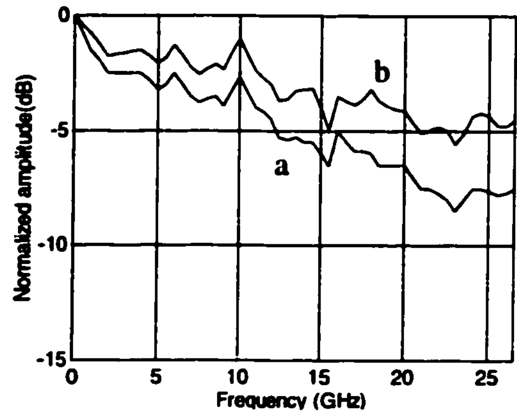


Figure 4-12 Frequency response of the P-I-N diode using pulse response technique.

a. Response before calibration.
b. Response after calibration

Figure 4-13 Frequency response of the P-I-N diode using the heterodyne technique.

a. Response before calibration.
b. Response after calibration

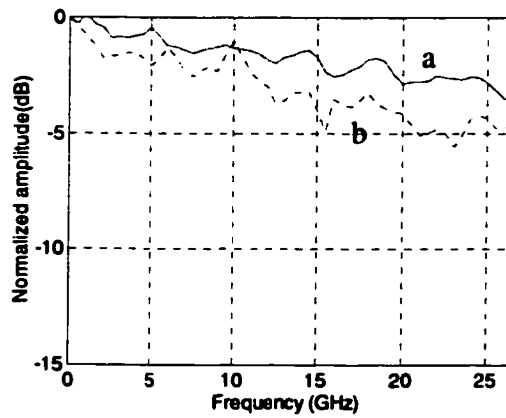


Figure 4-14 Frequency response of the P-I-N diode.

a. Measured using pulse response technique.
b. Measured using heterodyne technique

4.4 Conclusion

Broadband measurement techniques for P-I-N diodes have been described. The calibration results for typical components have been presented. The optical response of the P-I-N diode was measured up to 40GHz and 26GHz, based on two different techniques (pulse response and heterodyne). The pulse response technique is preferred since it eliminates the effects of reflections. The corrected scalar response results are compared in the frequency domain. The measurement results are very reproducible. The results obtained in this Chapter will be useful in the prediction of the photo-receiver performance in Chapter 5.

Chapter 5 Ultra Broadband HBT Preamplifier

The design procedure and implementation of a MMIC HBT preamplifier is demonstrated in this Chapter, which fulfills the third objective of the thesis. A P-I-N preamplifier is fabricated using Nortel's GaAs HBT process, and fully measured to validate the design principle, which fulfills the thesis's final objective. The fabricated HBT P-I-N preamplifier has a measured bandwidth of 22GHz, and average equivalent noise current density of 24 $pA/\sqrt{Hz}$ from 3GHz to 20GHz. Attenuation compensation techniques and CPW topology are used in the HBT DA MMIC design.

5.1 Design Procedure

Several CAD software packages are used during the implementation of the MMIC HBT preamplifier, which include circuit simulator Hspice, Libra, EM simulator Sonnet, and Cadence for layout. As part of high-speed optical receivers, the preamplifier works with base-band signal. The time domain output waveform is the key feature for the device's performance. Therefore, we choose Hspice for the overall circuit simulation. For the MMIC design, the circuit's parasitic parameters have a big effect on the circuit's overall performance. Therefore, EM simulation is required to derive more accurate models for some of the circuit elements, and these are subsequently incorporated into the Hspice simulation.

The design procedure for HBT preamplifiers is shown in the following Flowcharts of Figure 5-1 and Figure 5-2. First, we need to choose the appropriate HBT gain cell topology according to the designed distributed amplifier's requirement. The HBT gain cell is characterized by its S-parameter and input/output impedance. The preferred HBT gain cell architecture is obtained by optimizing the gain cell's structure, choosing right size of devices based on theoretical analysis, and tuning the devices' DC bias. Second, we need derive the lumped elements for the ideal distributed amplifier with required

bandwidth, gain, and low noise. We need select the number of the gain sections, as well as the characteristic impedance for the DA input/output transmission line. Then, the performance of the HBT preamplifier with the HBT gain cells and the lumped elements can be simulated using Hspice or EEsoft/Libra. For the first time try, the performance of the circuit is most likely unsatisfied to meet the specification requirement. Then, modify the lumped components or even change the HBT gain cell, re-do the circuit simulation to see if the performance is improved. It may take several cycles before good performance can be obtained. During this period, we maybe need go back to the first step to re-evaluate the HBT gain cells before re-simulating the whole circuit's performance. Once the performance of the circuit meets the specification, we can prepare for the MMIC layout.

Before performing MMIC layout, the lumped circuit elements need to be converted into the physical geometry of the metals. For example, the inductance needs change to a piece of high impedance transmission line. In this thesis, we choose CPW technique for the HBT preamplifier's layout due to CPW's several advantages as discussed in Section 5.2.4. Therefore, the inductance in the circuit can be represented by a piece of short CPW line with high impedance. The dimensions of capacitors and resistors can be obtained by scaling the components' value according to the sheet value of the capacitor layer and resistor metal (Nichrome for this design), respectively. By putting the HBT devices and the derived the physical components (or different pieces of metal) into the preliminary MMIC layout, we will find out that a lot of the interconnections exist in the layout. For such high frequency design (up to 40 GHz), these interconnections will have tremendous effects on the circuit's overall performance. Therefore, the EM simulation needs to be done for all the circuit components (except for the HBT devices), as well as the interconnections in order to consider the parasitic effects during the preamplifier design.

EM simulator Sonnet is used to perform the EM analysis in this preamplifier design project. EM simulation provides the S-parameters of the considered circuits, from which Spice models can be derived using EEsof. To extract a Spice model from a distributed

circuit's S-parameters, a model structure and the preliminary values for its elements need to be provided. Then, the EEsof can optimize the values of those elements by forcing the model's S-parameters to fit the measured S-parameters over a wide frequency range. The designed preamplifier is implemented using CPW technology. Since most of the circuit elements available for microstrip are not available for coplanar waveguide, substantial efforts and skills are required to derive the model structures of CPW circuits such as CPW T-junction as well as other CPW elements, which are used in the preamplifier implementation in this thesis. The detail models of these elements were illustrated in Section 5.2.4.

By incorporating the derived Spice models into the whole circuit schematic of the preamplifier, and re-doing the Hspice simulations, it's easily observed that circuit's performance is very different from what we obtained before the parasitic effects are included. Therefore, we need to modify the MMIC layout, re-do EM simulations for the circuit layout, derive spice models, and simulate whole circuit performance. Several design cycles as shown in Figure 5-1 and Figure 5-2 may be needed before the final MMIC layout can be obtained.

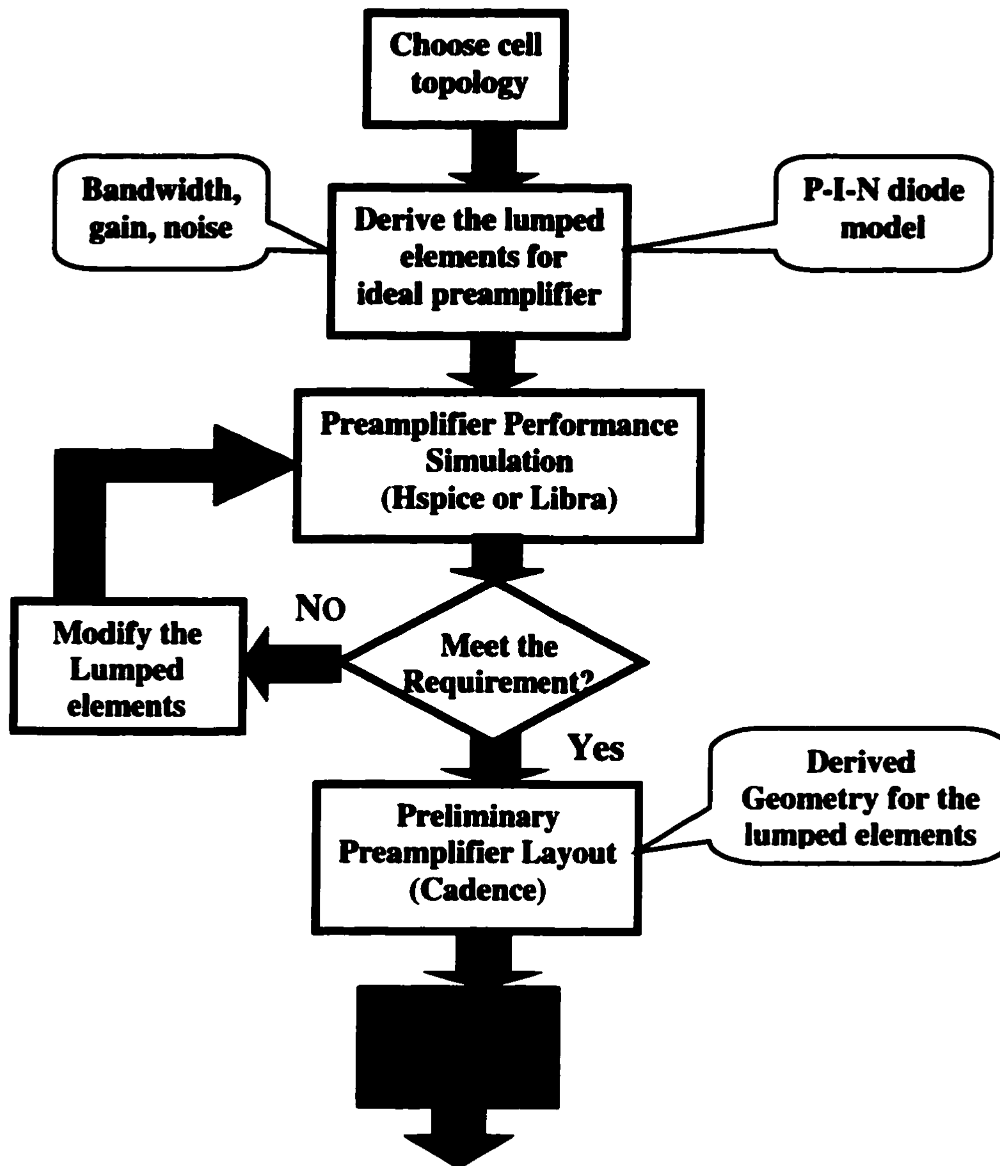


Figure 5-1 Design Procedure of HBT Preamplifier

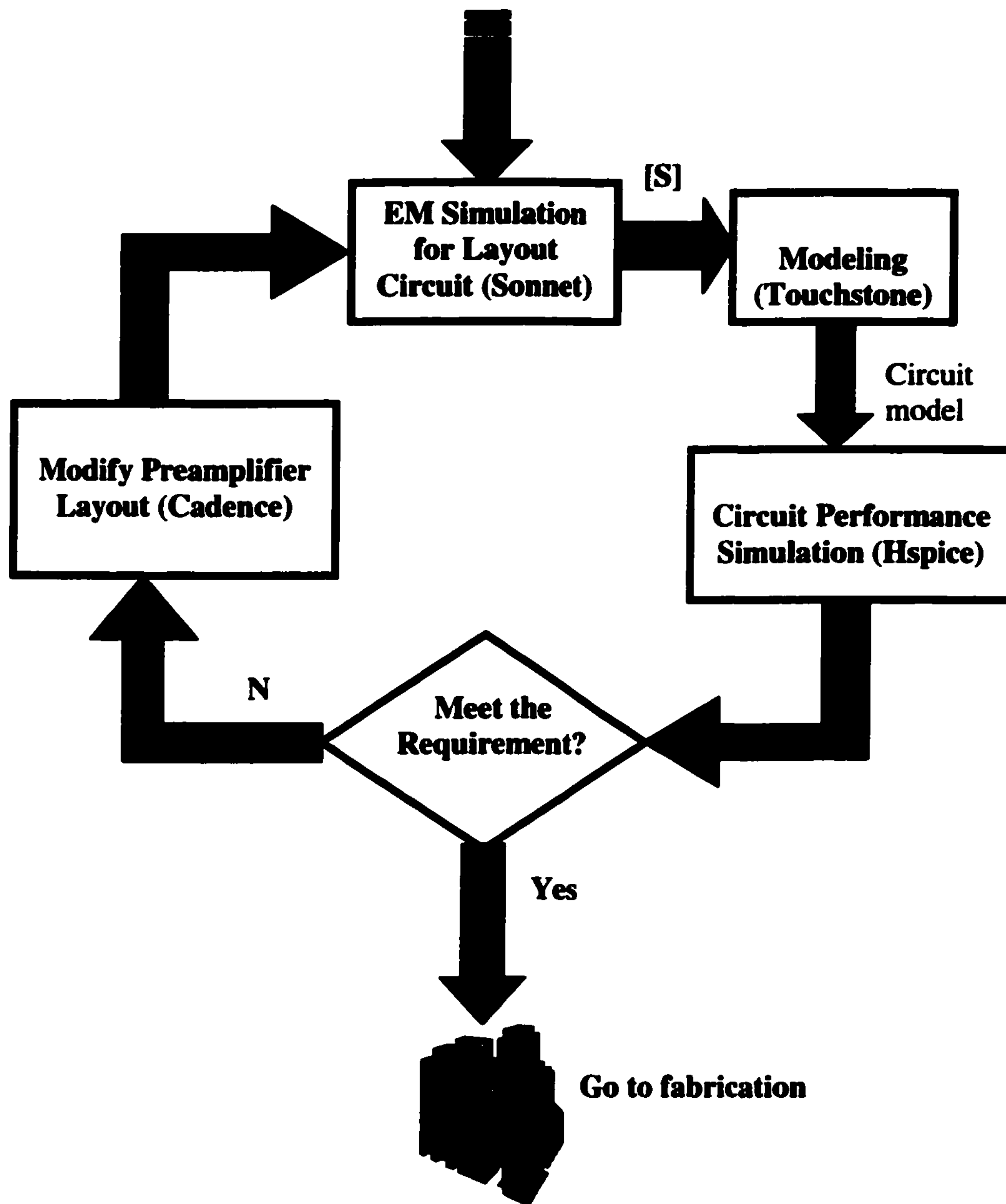


Figure 5-2 MMIC Design Cycle for HBT Preamplifier

5.2 The Implementation of GaAs HBT Preamplifier

5.2.1 HBT Device

The Nortel self-aligned HBT process [50], [51] has standard transistors with emitter area of 2x2 um^2, 3x3 um^2, and 3x6.5 um^2, which are primarily used for digital applications. The device's f_T is up to 70 GHz. It has the potential to develop high performance amplifier.

Figure 5-3 shows a small signal model of an HBT device. Table 5-1 shows the typical small signal parameters for those HBT devices. From Table 5-1, we can see that the C_π and g_π ($1/r_\pi$) of the devices are large for the distributed amplifier applications. If we use CE as stages to build an HBT distributed amplifier directly, the large input capacitance C_π and the base resistance r_b will limit the ultimate bandwidth cutoff frequency. Even using the smallest HBT device (2x2 um^2 emitter area), it is impossible to implement a 40 GHz bandwidth distributed amplifier with an input capacitance of 122fF. The 1972Ω of r_π will obviously introduce big input loss, which means the input transmission line attenuation factor is large. Therefore, we need use better HBT cell structure to build the desired distributed amplifier.

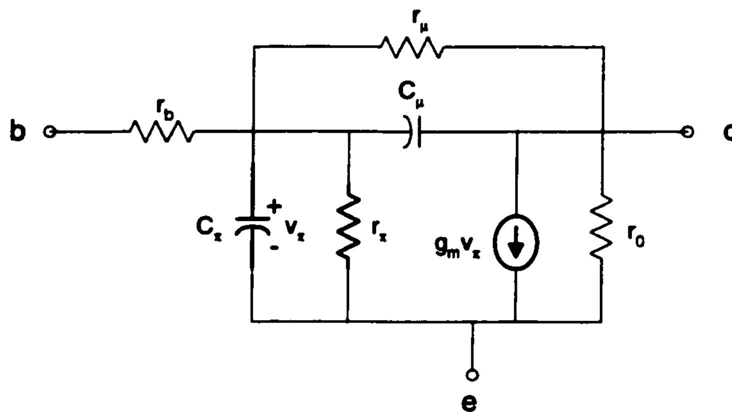


Figure 5-3 Simplified small signal model of HBT

Table 5-1 Typical small signal model parameters for different size of HBT devices

HBT emitter area (um^2)	2x2	6.5x3	6.5x3
I_c (mA)	1.42	2.86	5.80
V_{be} (V)	1.35	1.35	1.35
V_{ce} (V)	1.79	2.23	3.0
g_m (mS)	55	110	225
r_π (Ω)	1970	973	475
r_b (Ω)	14.0	9.31	5.88
r_o (Ω)	Infinite	Infinite	Infinite
C_π (fF)	122	261	571
C_μ (fF)	11.7	15.9	24.3
r_μ (MΩ)	100	100	100
β	109	108	107
f_t (GHz)	70.7	66.3	61.8

5.2.2 Configuration of HBT Gain Cell

As we discussed in Chapter 3, the configuration of HBT gain cell shown in Figure 3-2 combines the advantages of the Common-Collector (Emitter-Follower), Common-Emitter and Common-Base amplifiers. We redraw the HBT gain cell configuration below in Figure 5-4. This structure of HBT gain cell provides attenuation compensation for both the input and output transmission line of the HBT DA. In addition, it provides low input capacitance, increasing bandwidth.

By using a Common-Collector input transistor Q_1, the input capacitance of a transistor cascode was transformed into negative impedance at the base (input) of Q_1. Adequate attenuation compensation can be obtained when the base and emitter resistances of the

HBT Q_1 are canceled out by the negative resistance generated by the transformation. In addition, by using a Common-Collector transistor at the input, the Miller input capacitance is reduced. The cascode topology helps increase the output shunt resistance presented to the output transmission line, which results in low attenuation. Also, the common-base transistor of the cascode reduces the Miller Capacitance of common-emitter transistor, increasing the bandwidth. The inductance L_{e2} is added to stabilize the circuit. Therefore, the HBT gain cell with this configuration has potential to obtain broader bandwidth.

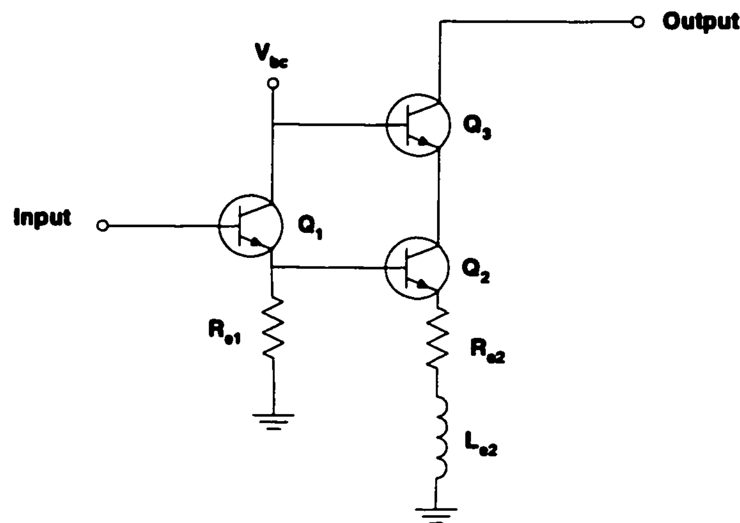


Figure 5-4 HBT gain cell topologies: Common-Collector/Cascode configuration

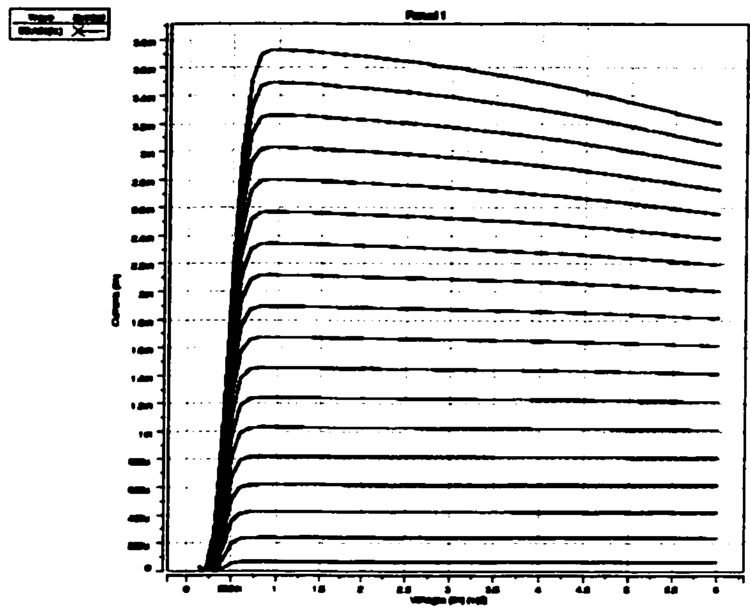
As discussed in Chapter 3, we need choose appropriate sizes of HBT devices for the gain cell and bias them properly to obtain the adequate gain, at the same time, get the adequate input/output attenuation compensation.

Since the CE circuit (Q_2) is utilized to provide the bulk of the required overall voltage gain, we need choose large HBT device as Q_2 if possible. As the CB circuit (Q_3) acts as a current buffer for the gain cell, same sizes of HBT devices must be used for Q_2 and Q_3.

From Equation (3–52), the output capacitance of the gain cell is approximately equal to $C_{\mu3}$. The Collector-Base Junction Capacitance C_{μ} is proportional to the emitter area of the HBT device. Therefore, the size of the Q_3 (or Q_2) is limited by the desired DA bandwidth. We choose to use two 3x6.5 um^2 HBT transistors as Q_2, and two 3x6.5 um^2 HBT transistors as Q_3. In order to reduce $C_{\mu3}$ and extend bandwidth, more DC voltage can be applied across Q_3 than Q_2. From Table 5-1, the total C_{μ} for two 3x6.5 um^2 HBT devices is about 52 fF, which is reasonable for a 50Ω system distributed amplifier with a bandwidth of 40GHz.

Now, we need make a decision on Q_1. After some investigations by simulating the input impedance of the HBT gain cell with different size of HBT device for Q_1, we use one 2x2 um^2 HBT as Q_1.

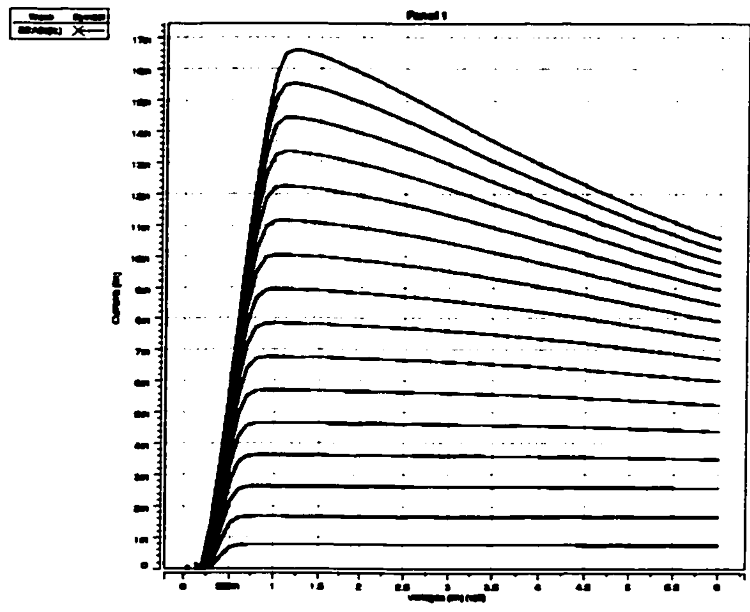
Figure 5-5 shows the I_C verse V_{CE} characteristics of these two different sizes of HBT devices. From the Equation (3–1), the g_m of the HBT device is proportional to the applied DC bias current I_C, which means more DC bias current provides more gain. From Equation (2–1) and (2–2), we know that more DC bias current means more shot noise from the device. From noise point view, we don't want to increase the DC bias current. Therefore, the tradeoff exists between the gain, bandwidth and the noise performance. The DC bias currents and bias voltages for each HBT transistors used in the gain cell are listed in Table 5-2.



I_b=
1uA
3uA
...
35uA

Typical operation point is around Ic=1.4mA.

a. 2x2 um^2 emitter area HBT



I_b=
10uA
20uA
...
160uA

Typical operation point is around Ic=6mA.

b. 6.5x3 um^2 emitter area HBT

Figure 5-5 I_C verse V_{CE} characteristics for HBTs

Table 5-2 DC biases and corresponding small signal parameters for HBT devices

HBT Transistor	Q_1 2x2 um^2	Q_2 Each 6.5x3 um^2	Q_3 Each6.5x3 um^2
I_c (mA)	1.42	5.86	5.80
V_{be} (V)	1.35	1.35	1.35
V_{ce} (V)	1.79	1.73	3.0
g_m (mS)	55	227	225
r_π (Ω)	1972	471	475
r_b (Ω)	14.0	5.88	5.88
r_o (Ω)	Infinite	Infinite	Infinite
C_π (fF)	122	495	571
C_μ (fF)	11.7	26.8	24.3
r_μ (MΩ)	100	100	100
β	109	107	107
f_t (GHz)	70.7	71.7	61.8

For the HBT gain cell shown in Figure 5-4, we use following devices and lumped components:

Q_1: one 2x2 um^2 HBT;

Q_2: two 3x6.5 um^2 HBT;

Q_3: two 3x6.5 um^2 HBT;

R_{e1}: 1300Ω resistor;

R_{e2}: 30Ω resistor;

L_{s2}: 0.05nH inductor.

Figure 5-6 shows the layout of the designed gain cell. Symmetrical structure is used for Q_2's layout (two HBT transistors), as well as Q_3's layout (two HBT transistors). Square-

sided spiral inductor is used to implement L_{s2} as shown in Figure 5-7. The layout of the inductor is analyzed by EM simulator (Sonnet). Figure 5-8 shows the equivalent model of the Square-sided spiral inductor, which is derived from the EM simulated S parameter. Actually, all the inter-connections of the gain cell are modeled by following the same procedure. The equivalent elements are included in the circuit simulation.

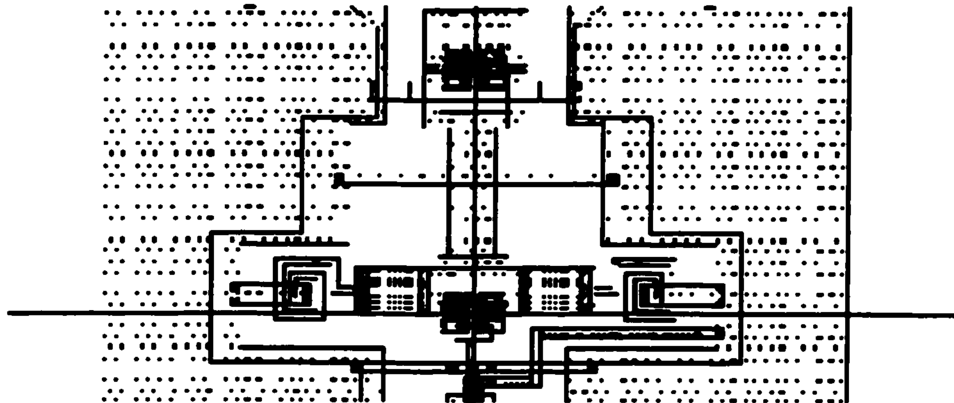


Figure 5-6 Layout of HBT gain cell

Figure 5-7 Layout of the inductor

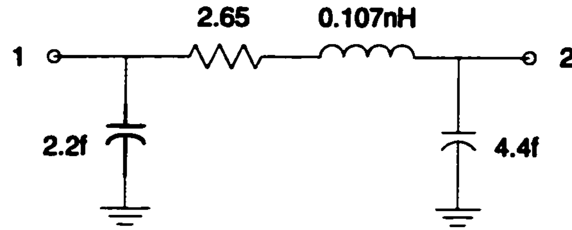


Figure 5-8 Equivalent model of the inductor

Figure 5-9 shows Hspice simulation results of the input and output admittance for the gain cell including all the parasitic effects from the layout. From Figure 5-9, we can see that the image part of output admittance is linear over the broadband frequencies, while the image part of input admittance is not linear over the frequencies, which means the output capacitance is constant over the frequencies, and the equivalent input capacitance is not constant over the frequencies. Also, there is enough negative resistance compensation up to 30 GHz for the input attenuation. Above 30 GHz, the input loss increases significantly.

We use the average value of the input capacitance over the frequencies for the distributed amplifier's theory analysis. From Figure 5-9, we get that

$$C_{in} \approx 56fF \tag{5-1}$$

$$C_{out} \approx 55fF \tag{5-2}$$

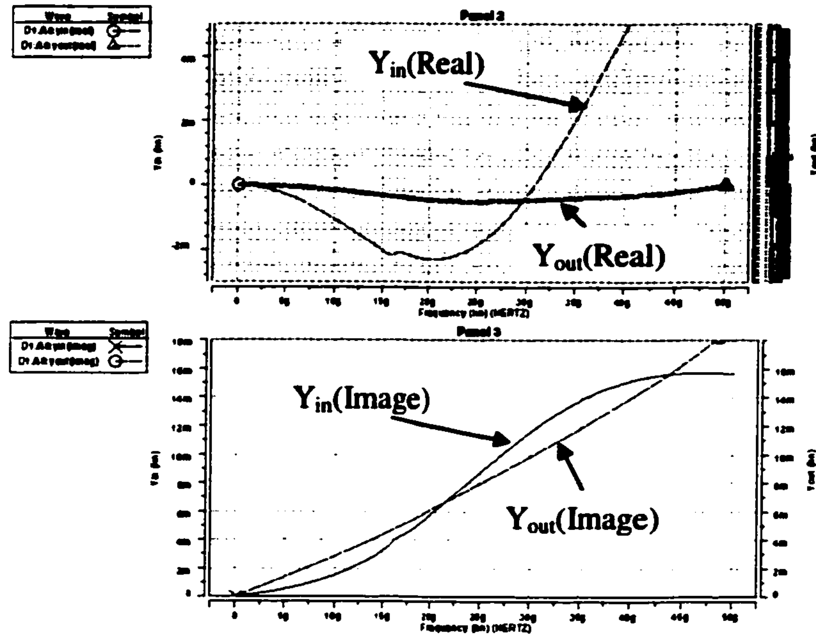


Figure 5-9 Input and output admittance of HBT gain cell

5.2.3 Distributed amplifiers using the HBT gain cells

A schematic of a distributed amplifier with the HBT gain cells is shown in Figure 5-10. The inductors L_{b1}, L_{b2} and the input capacitors of the HBT gain cell C_{in} form the input transmission line with impedance equal to

$$Z_b = \sqrt{L_{b1}/C_{in}} \tag{5-3}$$

Where C_{in} is the input capacitance of the gain cell. The cutoff frequency of the input transmission line is given by

$$f_{c_b} = \frac{1}{\pi\sqrt{(L_{b1} + 4L_{b2})C_{in}}} \tag{5-4}$$

Similarly, the inductors L_{c1}, L_{c2} and the output capacitors of the HBT gain cell C_{out} form the output transmission line with impedance equal to

$$Z_c = \sqrt{L_{c1}/C_{out}} \tag{5–5}$$

Where C_{out} is the output capacitance of the gain cell. The cutoff frequency of the output transmission line is given by

$$f_{c_c} = \frac{1}{\pi\sqrt{(L_{c1} + 4L_{c2})C_{out}}} \tag{5–6}$$

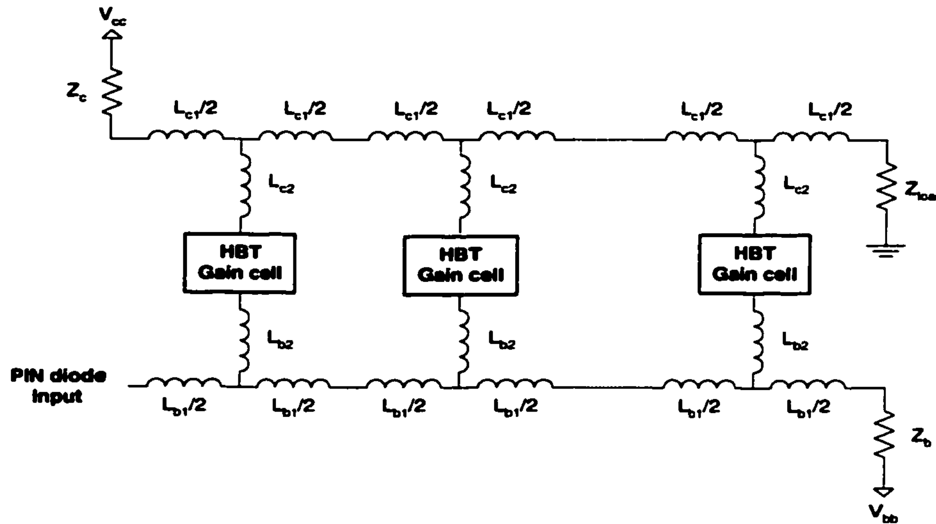


Figure 5-10 Equivalent circuit of the DA using HBT gain cells

Equation (5–4) and Equation (5–6) shows that the cutoff frequency of artificial input/output transmission line decreases due to L_{b2}/L_{c2}. In order to extend preamplifier's bandwidth, L_{b2}/L_{c2} should be kept as small as possible with the necessary interconnection and phase matching. For the traveling amplifier, the phase delay for the input transmission line and output transmission line has to be matched, so that the output signal from each gain cell can add up in phase on the load. As described in Chap 3, in order to

increase the trans-impedance gain and reduce noise current density of the preamplifier, we need increase the characteristic impedance of the input transmission line above 50 Ohm. The characteristic impedance of the output transmission line remains 50 Ohm. Therefore, the output transmission line has different characteristic impedance from the input transmission line. The equivalent input and output impedance of the gain cell is different, too. With these factors, it's very challenging to match the input line's phase delay to the outline over such broadband frequencies. We need tuning L_{b2}/L_{c2} to achieve phase match for input/output line.

Ignoring L_{b2}/L_{c2}, we can draw f_c vs. C curve shown in Figure 5-11, according to Equation (5–3) and (5–4). This figure illustrates relationship between characteristic impedance Z_0 of the TRL structure, the corresponding values of the C, as well as the cut off frequencies f_c. It shows: with the same value of C, higher characteristic impedance, then lower cut off frequency. Therefore, the impedance increasing for the input TRL is limited by the bandwidth requirement. Once again, tradeoff exists between gain, bandwidth, and noise. Table 5-3 lists the characteristic impedance Z_0 of the TRL structure, the corresponding values of the C and L, as well as the cut off frequencies f_c.

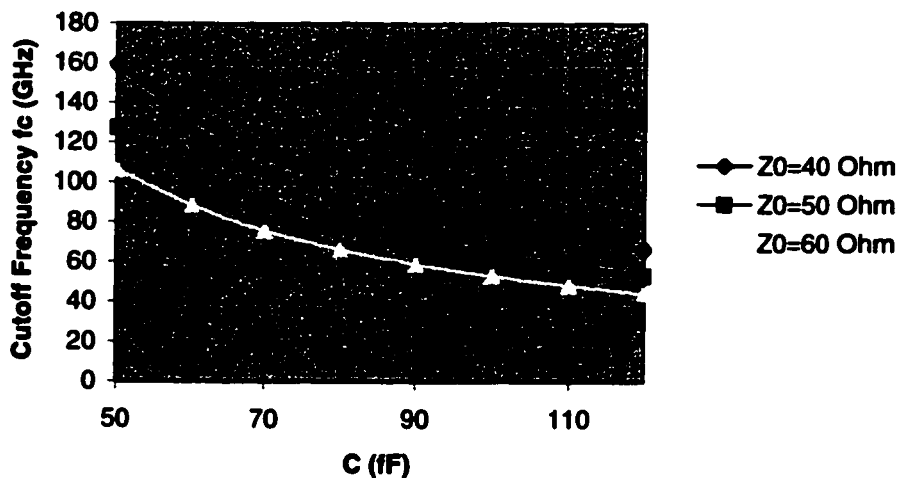


Figure 5-11 Cutoff frequency f_c vs. C and characteristic impedance Z_0

Since parasitic capacitance exists for all the interconnections of the preamplifier MMIC layout, the actual parallel capacitance per stage of artificial input/output TRL is much larger than C_{in}/C_{out}. An eight-stage HBT distributed amplifier with 60Ω input impedance and standard 50Ω output impedance is finally implemented and fabricated using CPW technology.

Table 5-3 Characteristic impedance and cutoff frequency vs. L and C

Z_o (Ω)	C (fF)	L (nH)	f_c (GHz)
40	80	0.128	99.5
	90	0.144	88.4
	100	0.160	79.6
50	80	0.2	79.6
	90	0.225	70.7
	100	0.25	63.7
60	80	0.288	66.3
	90	0.324	58.9
	100	0.360	53.1

5.2.4 CPW design technique

Coplanar waveguide (CPW) has been suggested as an alternative to microstrip line for millimeter-wave integrated circuits [52]. HBT distributed amplifier have been implemented by using CPW design technology [28], [29]. The CPW DA approach allows the design to be more easily modeled without full EM analysis and results in more simple and compact layout due to the absence of vias. The CPW design technique has many advantages [53]:

- Smaller chip size implementation

- Lower parasitic ground inductance
- Easier manufacturability because backside vias are not required
- Minimized interline coupling between transmission lines and proximity effects which simplifies the circuit modeling at millimeter wave.

The last advantage is especially attractive for millimeter-wave HBT DA because the small inductive line lengths normally required to construct a distributive network with the HBT gain cell's input capacitances are sensitive to the close proximity of backside vias and other microstrip components. In addition, the CPW doesn't inherently have higher conduction loss than microstrip line as misunderstood before [52]. Therefore, we use CPW technology for the HBT distributed amplifier's design in this thesis. A design topology for CPW HBT distributed amplifier is shown in, where transmission line lengths form the inductances (L's) of the derived sections.

CPW characteristic impedance depends roughly upon the ratio of inner conductor width to total cross section. CPW of several different sizes could have the same impedance. However, the smaller cross sections have higher conductor loss and thus a tradeoff exists between size and conductor loss [52].

One disadvantage of CPW is: the variety of circuit elements available for microstrip is not yet available for coplanar waveguide. In order to get an accurate model for the CPW element, EM simulator Sonet is used to do the EM analysis for all the passive circuits in this thesis. First, enter the CPW circuit's structure and substrate information into the Sonet input file, and do the EM simulation to obtain S-parameter for the circuit element. Then, use Eesoft to optimize the electrical equivalent model, force the model's S-parameter to fit the EM simulated S-parameter for this CPW element. In this thesis, a short CPW line is modeled as a π section with one series inductance and two parasitic shunt capacitors, which is shown in Figure 5-13. The CPW T-junction is modeled as a T section as shown in Figure 5-14.

The DA topology shown in Figure 5-10 contains only lumped elements: capacitors, inductors, and resistors. The CPW design topology for this distributed amplifier is illustrated in Figure 5-12. To realize such a circuit on a CPW substrate, the lumped elements must be replaced by their CPW distributed equivalents. The CPW elements always contain some parasitic elements. These parasitic must be considered in the over all circuit model, because they have a significant effect on performance. The inductors are realized using high impedance CPW lines. The high Z_0 "inductive" line is modeled as a π section as shown in Figure 5-13.

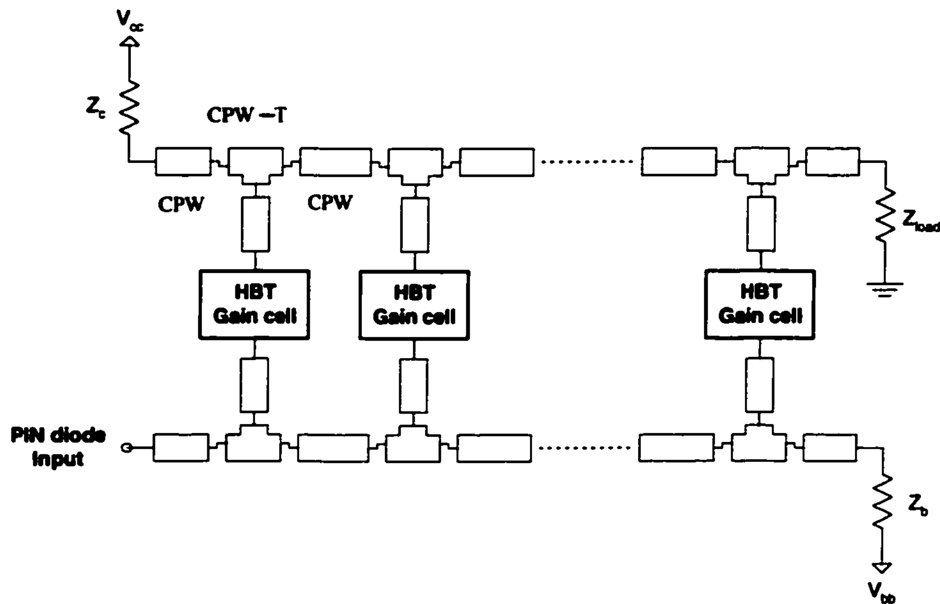


Figure 5-12 Design topology of the CPW HBT Distributed Amplifier

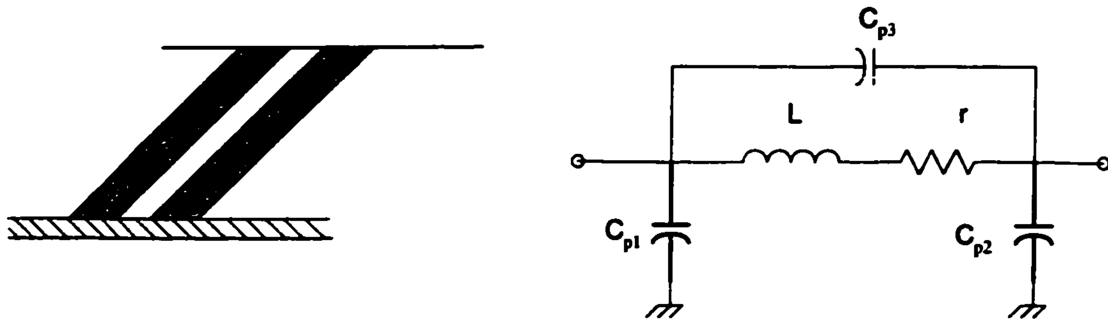


Figure 5-13 A short CPW line & its equivalent model

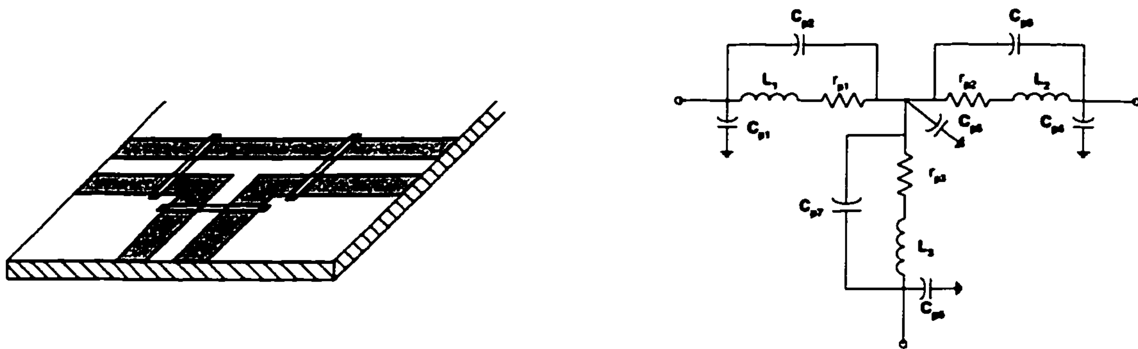


Figure 5-14 A CPW T-junction & its equivalent model

Actually, CPW T-junction structure was used in the DA implementation. Its equivalent circuit, which is obtained by the derivation procedure as described before, replaces L_{c1} and L_{c2} T-junction, and L_{b1} and L_{b2} T-junction in Figure 5-10, respectively. As an example of the Sonnet input file, the CPW T-junction structure is shown in Figure 5-15. In this design, two layers of metal are used for the MMIC layout interconnections. First level metal (Met1) is used for the Ground of CPW, and 2nd level metal (Met2) is used for the conduct line of CPW. The CPW ground is connected directly by Met1 lines at the cross section to surpass Odd mode. Because of these ground connections, the characteristic impedance of the CPW decreases significantly. The equivalent model of CPW T-junction is shown in Figure 5-14. The parameters of the CPW T-junction model

for the input/output TRL of the final DA layout are illustrated in Table 5-4. Figure 5-16 shows the actual layout of each HBT DA stage.

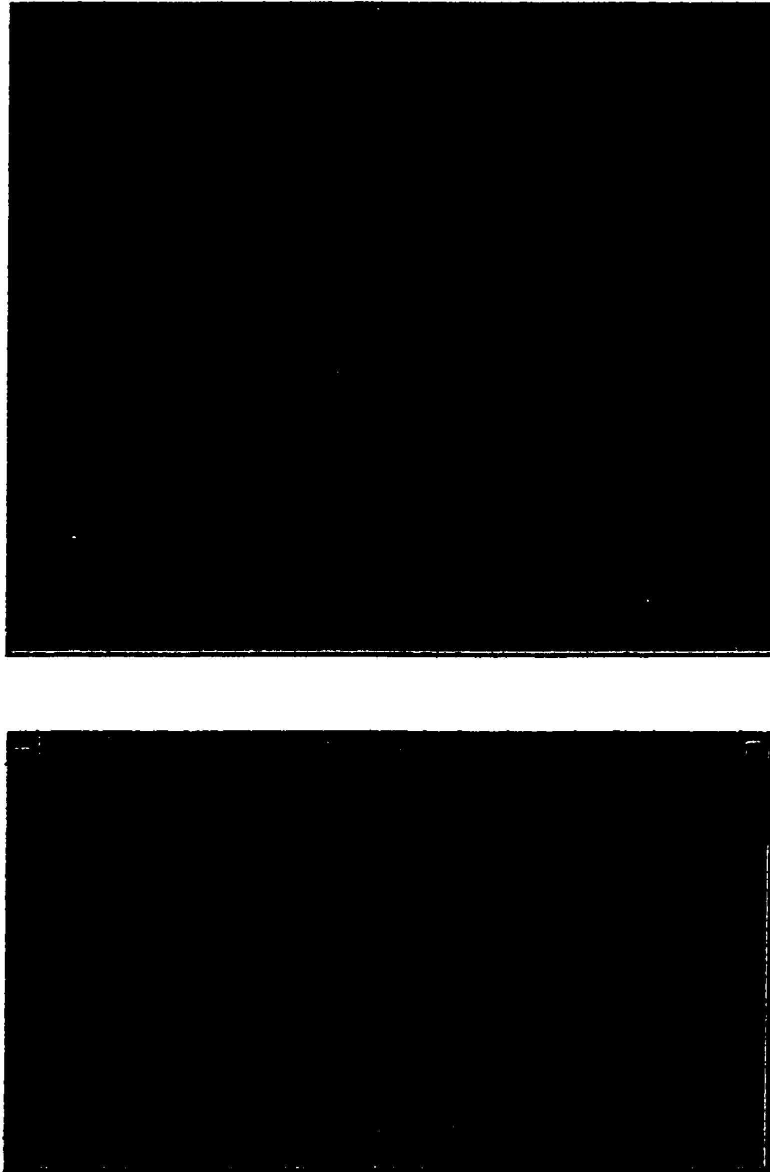


Figure 5-15 Sonnet Geometry of a CPW T-junction

Table 5-4 Parameters of CPW T-junction model for DA input/output TRL

Parameter	T-junction for Input Line	T-junction for Output Line
L_1, L_2 (nH)	0.108	0.114
r_{p1}, r_{p2} (Ω)	0.45	0.53
C_{p1}, C_{p4} (fF)	11.7	9.8
C_{p2}, C_{p3} (fF)	1.4	1.2
C_{p5} (fF)	0.0	0.0
L_3 (nH)	0.023	0.019
r_{p3} (Ω)	0.18	0.16
C_{p6} (fF)	22.4	21.2
C_{p7} (fF)	0.1	0.1

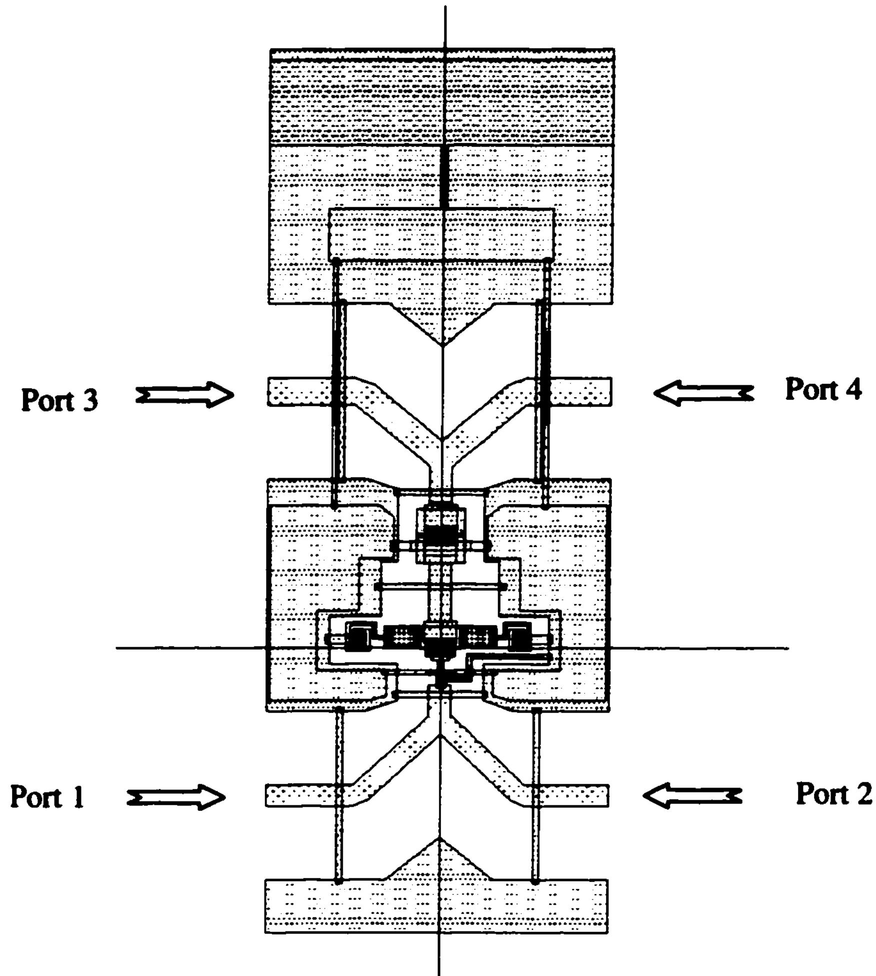
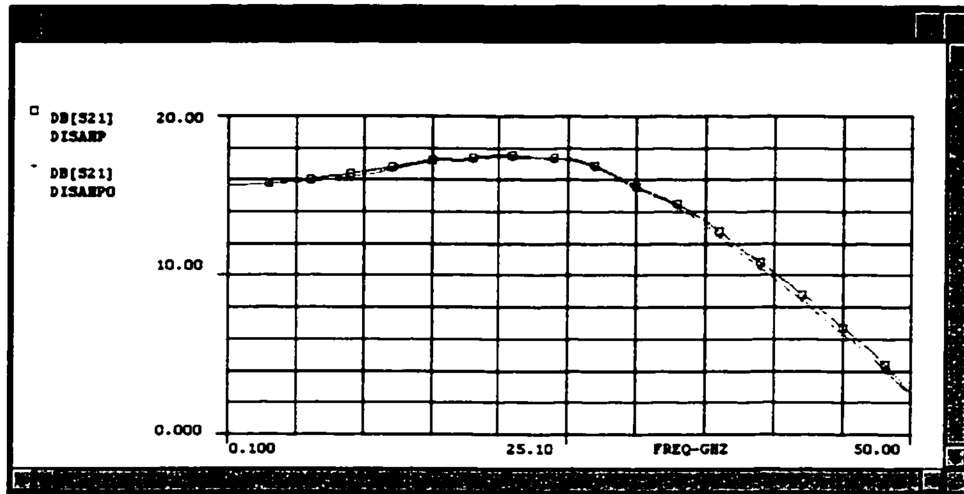


Figure 5-16 Layout of one DA stage including HBT gain cell and CPW T-junctions

To verify the CPW T-junction model, the following simulations are made in Libra. The S parameter of the DA is simulated both by a) Cascading the cells' S-parameter and T-junctions' S-parameter; b) Cascading the cells' S-parameter and T-junctions' equivalent model. The simulated S-parameters are compared in Figure 5-17. The results are very close, which means the equivalent model of the T-junction is good enough to be used in the Hspice simulation.

Figure 5-18 shows the phase delay of the DA input and output TRL. As shown in the figure, the phase of input line matched the phase of output line very well over the 0.1-50GHz frequency band.



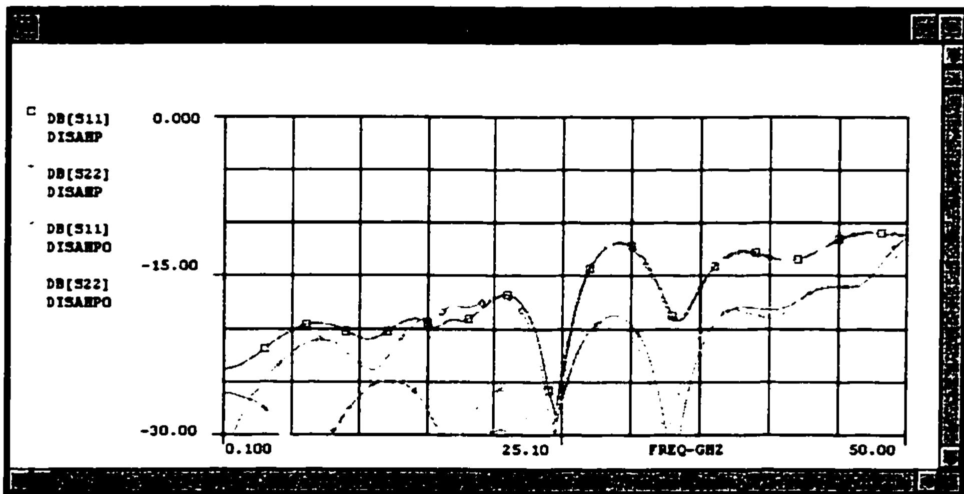


Figure 5-17 Simulated DA S-parameters using Libra

DISAMP—cascading the cell's S parameter and T-junctions' S-parameter;
DISAMPO—cascading the cell's S parameter and T-junctions' equivalent model

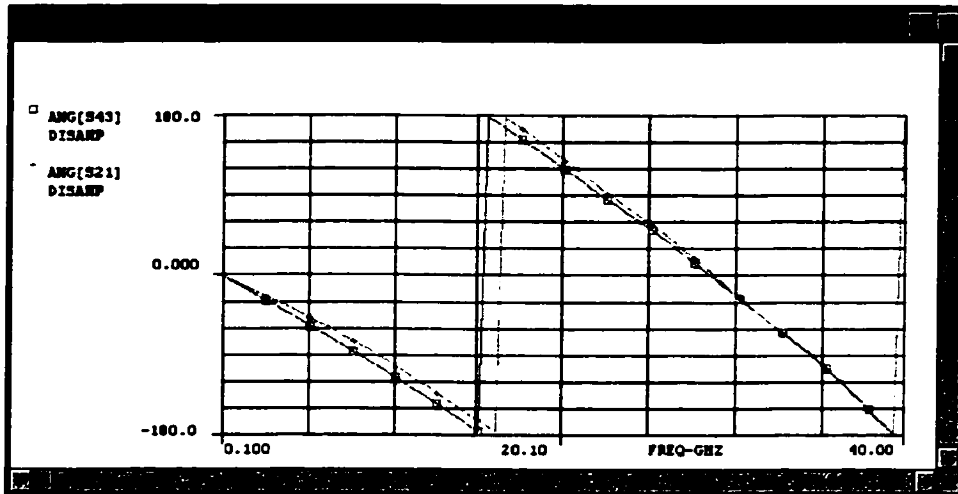


Figure 5-18 Phase delay of the DA input/output TRL simulated using Libra

ANG [S21]—phase delay of the input line
ANG [S43]—phase delay of the output line

5.2.5 Traveling Wave Terminations and Bias Networks

Since the designed HBT preamplifier functions at such broadband and high frequency (DC to 40 GHz), the input/output artificial transmission line of the HBT amplifier doesn't have uniform characteristic impedance over the entire frequency range. The input/output return loss can be improved by tuning the input/output line termination network to match to the impedance of the transmission line over frequencies. Since V_{cc} and V_{bb} are applied through the terminations of the input/output transmission line, these termination networks also act as decoupling circuits for the external DC supplies to provide AC ground. Therefore, the termination networks play important roles in the preamplifier's design. First, they must be matched to the impedance of the artificial transmission line over a broadband width. Second, they need be able to function as DC decoupling circuit.

There are four DC power supplies for the designed preamplifier. The names of the DC supplies as well as their function descriptions are listed in the table below.

Table 5-5 DC power supplies for the HBT preamplifier

Power Supply Name	Parameter	Voltage (V)	Current (mA)
V_{cc}	Bias voltage for the Collector line of HBT DA	10.2	92.8
V_{bb}	Bias voltage for the Base line of HBT DA	3.10	0.118
V_{bc}	Bias voltage for the Base of CB (Q_3), and collector of CC (Q_1)	4.6	12.4
V_{pin}	Bias voltage for the P-I-N diode	8.0	

Termination networks---Bias network for Vcc and Vbb

Figure 5-19 shows the termination networks for the designed preamplifier. In this design, the components of the bias networks were optimized, and finally tuned to proper values to achieve the best performance of the preamplifier. The parameters of the termination networks are listed in Table 5-6.

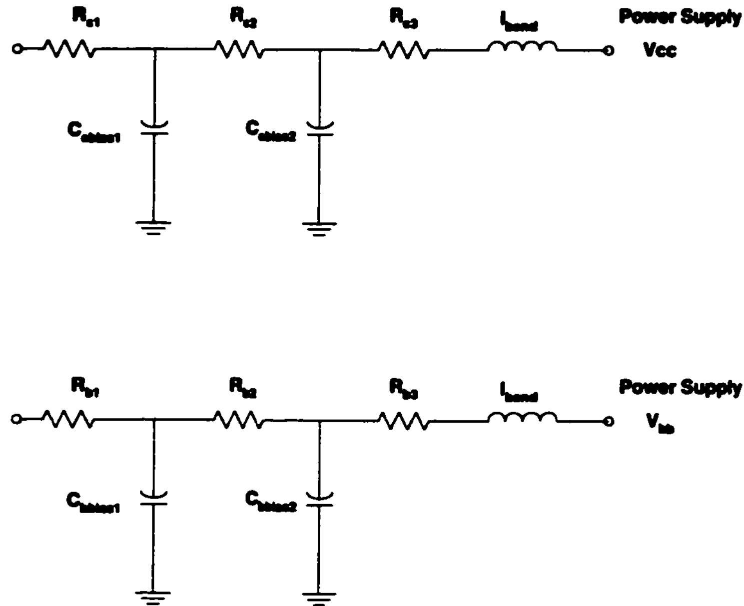


Figure 5-19 Output TRL & input TRL termination Network

Table 5-6 Parameters of the DA termination networks

Collector line termination network	Parameter Value	Base line termination network	Parameter Value
R_{c1} (Ω)	42	R_{b1} (Ω)	48
R_{c2} (Ω)	3.0	R_{b2} (Ω)	6.0
R_{c3} (Ω)	3.0	R_{b3} (Ω)	6.0
C_{cbias1} (pF)	4.08	C_{bbias1} (pF)	1.2
C_{cbias2} (pF)	2.65	C_{bbias2} (pF)	0.6

Bias network for Vbc

In order to avoid oscillation between different HBT DA stages, the bias network composed of resistors and decoupling capacitors is added for each stage's V_{bc}. The bias network for V_{bc} is illustrated in Figure 5-20. The parameters of the V_{bc} bias network are listed in Table 5-7. Similar bias network is used for the P-I-N diode's DC power supply V_{pin} with different parameter values.

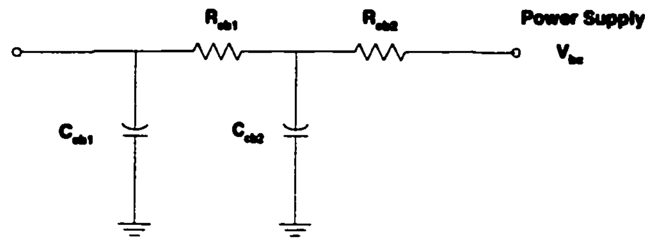


Figure 5-20 Bias network for V_{bc}

Table 5-7 Parameters of the bias network for V_{bc}

Component	Parameter Value
R_{cb1} (Ω)	500
R_{cb2} (Ω)	160
C_{cb1} (pF)	4.4
C_{cb2} (pF)	1.5

Figure 5.21 shows the schematic of the designed HBT distributed amplifier including all the termination and bias networks.

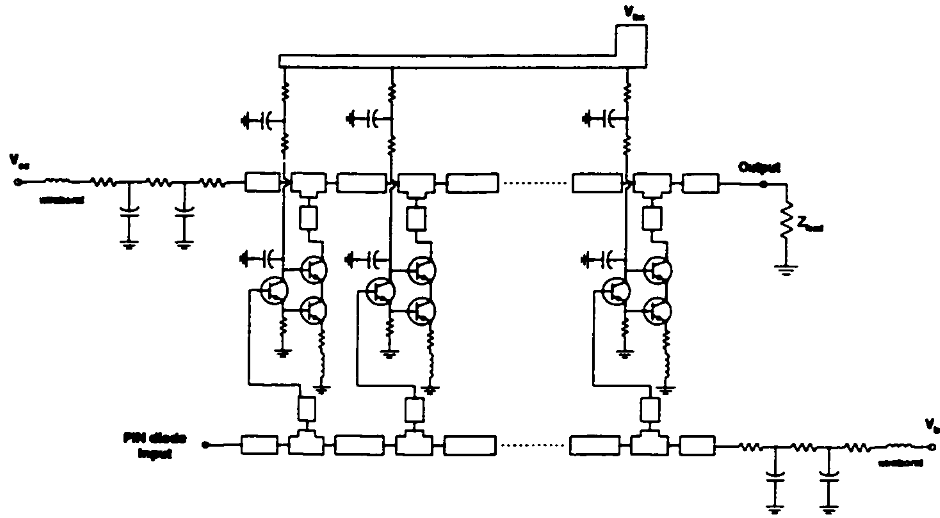


Figure 5-21 Schematic of HBT distributed amplifier

5.2.6 Simulation results

Since the preamplifier is an ultra broadband design, the input signal to it will be 40Gb/s data stream. Therefore, the time domain eye diagram is the most important performance that needs to be simulated. Based on this requirement, Hspice is used as the main circuit simulation tool in this design. Cadence is used for the chip layout.

In order to show that the equivalent input noise current density of the preamplifier can be reduced by increasing input line impedance, two preamplifiers with different input line characteristic impedance are designed. One is with 60Ω input line. And another is with 40Ω input line. Only 60Ω preamplifier is finally fabricated. The simulation results of these two preamplifiers are compared in Figure 5-22. Obviously, the noise performance of 60Ω preamplifier is much better than the 40Ω one. The equivalent input noise current density of 60Ω preamplifier is about $5\,pA/\sqrt{Hz}$ less than the 40Ω preamplifier over all frequencies. The 60Ω preamplifier also has higher trans-impedance gain than the 40Ω

one. The trans-impedance gain difference is about 3dBΩ. However, the 3dB bandwidth of 60Ω preamplifier is less than the 40Ω one, which is 33GHz against 36GHz.

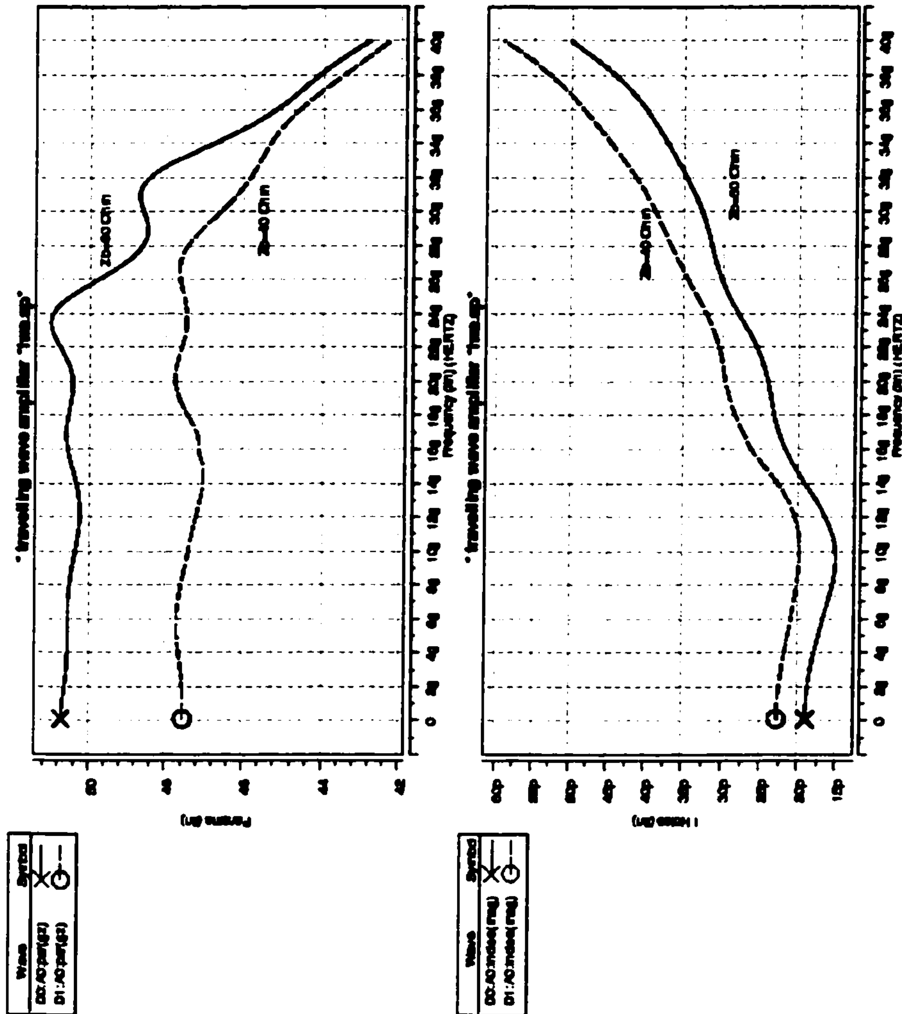


Figure 5-22 Simulation results of 60Ω preamplifier against 40Ω preamplifier

Figure 5-23 shows the final layout of the designed 60Ω HBT preamplifier. The dimension of the MMIC chip is 4.050 x 1.800mm^2. In order to reduce the length of the wire bond that connects P-I-N and the HBT distributed amplifier, a space is left for a P-I-N at the input of the DA so that the P-I-N can be mounted on the HBT distributed amplifier MMIC chip. Figure 5-24, 5-25 and 5-26 shows the simulated circuit performance corresponding to the final layout. Figure 5-24 shows the S parameter of the HBT distributed amplifier itself. The shown S11 is simulated in a 60Ω system. Figure 5-25 shows the trans-impedance gain and the equivalent input noise current density of the preamplifier, which includes the P-I-N (only electrical model, optical response of the P-_I-N not included), wire bond, and the HBT distributed amplifier. Figure 5-26 shows the preamplifier's output eye diagram, as well as time domain output waveform corresponding to ideal 40Gb/s NRZ input data signal. The simulation results are summarized in Table 5-8. The trans-impedance gain is 51dBΩ up to 25GHz with a ripple within 1 dB, which is very flat. The 3dB bandwidth for S21 is about 35GHz, which is a little higher than the 3dB bandwidth for the trans-impedance gain. Up to 40GHz, the input/output return loss is 11 dB and 19 dB, respectively. The average equivalent input noise current is 23 $pA/\sqrt{Hz}$.

Table 5-8 Simulation Results Summary for Preamplifier

Parameter	Conditions	Simulation Result
Trans-impedance Gain (dBΩ)	0.1 to 25 GHz	51
Input noise current density ($pA/\sqrt{Hz}$)	Average (100MHz to 30GHz)	23
3 dB bandwidth (GHz)		35
Small Signal Gain (dB)	0.1–28 GHz	16
Input Return Loss (dB)	0.1–40 GHz	11
Output Return Loss (dB)	0.1–40 GHz	19
Isolation (dB)		25

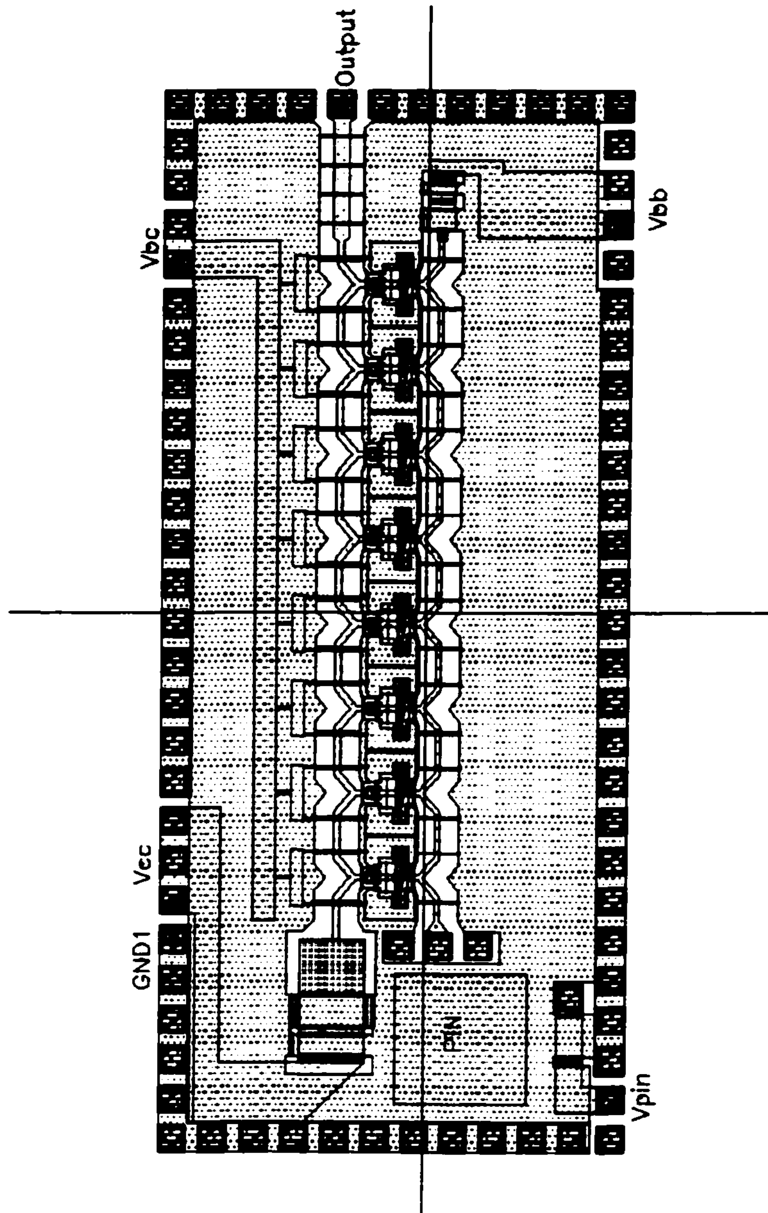


Figure 5-23 Layout of the Preamplifier

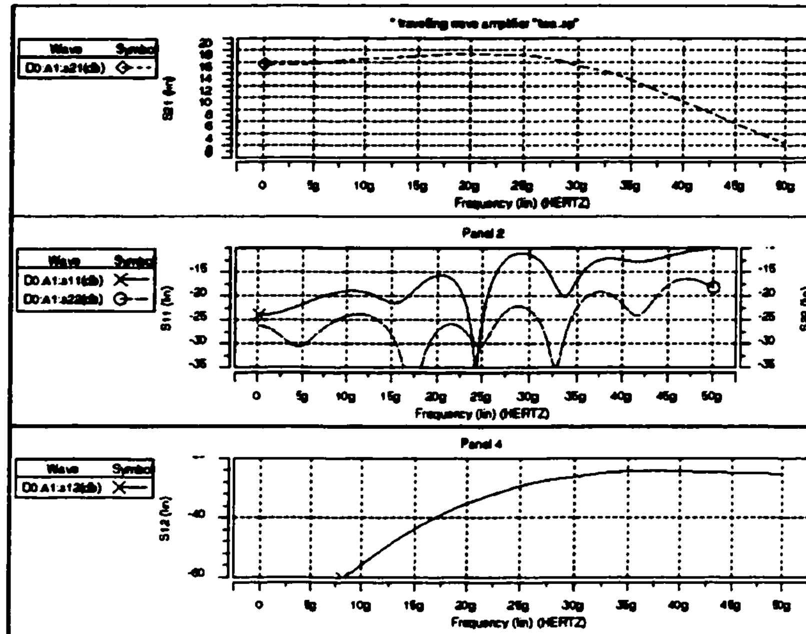


Figure 5-24 Simulated S-parameter of the distributed amplifier

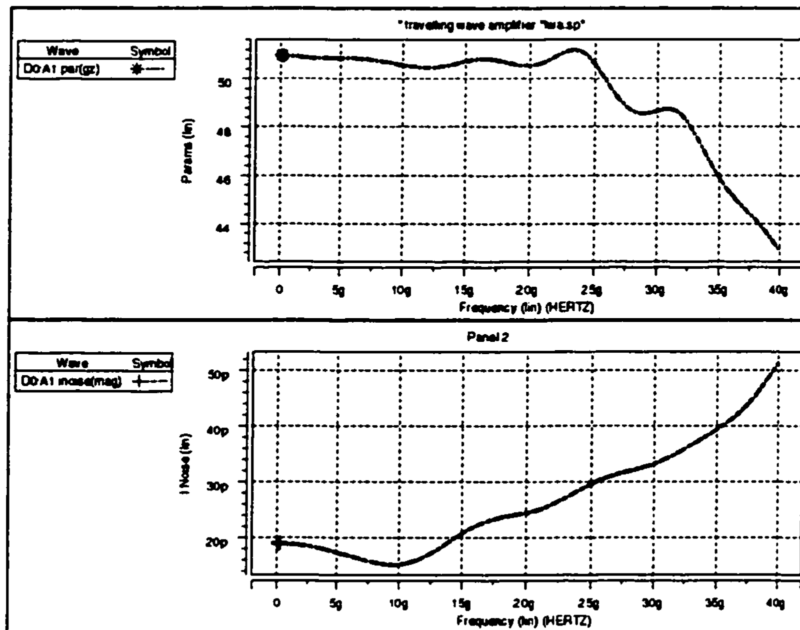


Figure 5-25 Simulated transimpedance gain and equivalent input noise current density of the preamplifier

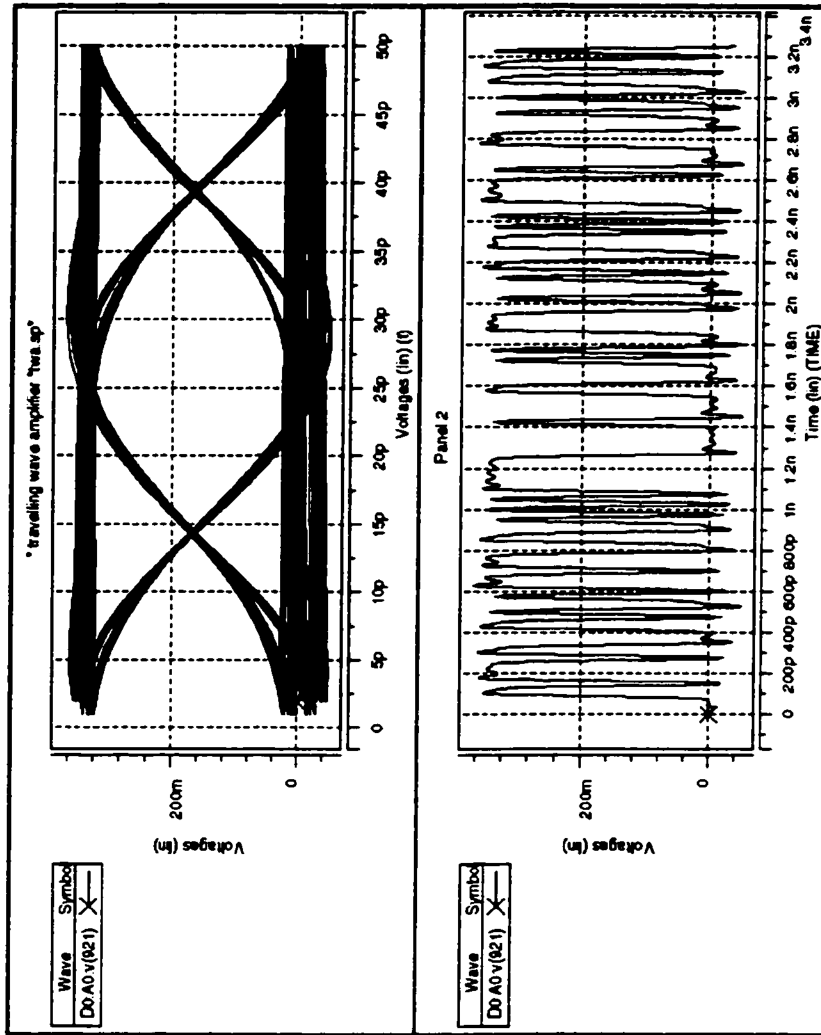


Figure 5-26 Simulated output eye diagram of the preamplifier

5.3 Measurement Results

5.3.1 S-parameters of a DA Cell

A single DA cell (without CPW T-junction) as shown in Figure 5-27 was fabricated and tested first. Figure 5-28 shows comparison between the simulation and test S-parameters for the cell. The measured S parameters are very close to the simulated results for the test cell.

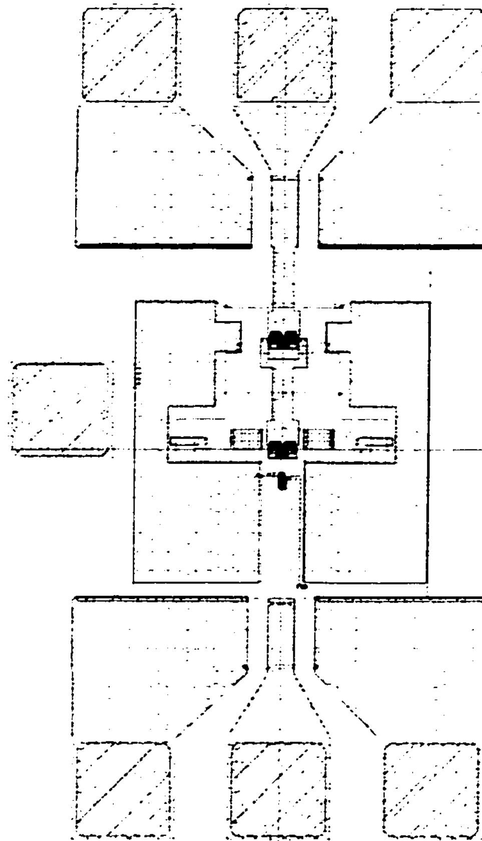


Figure 5-27 Layout of a DA test cell

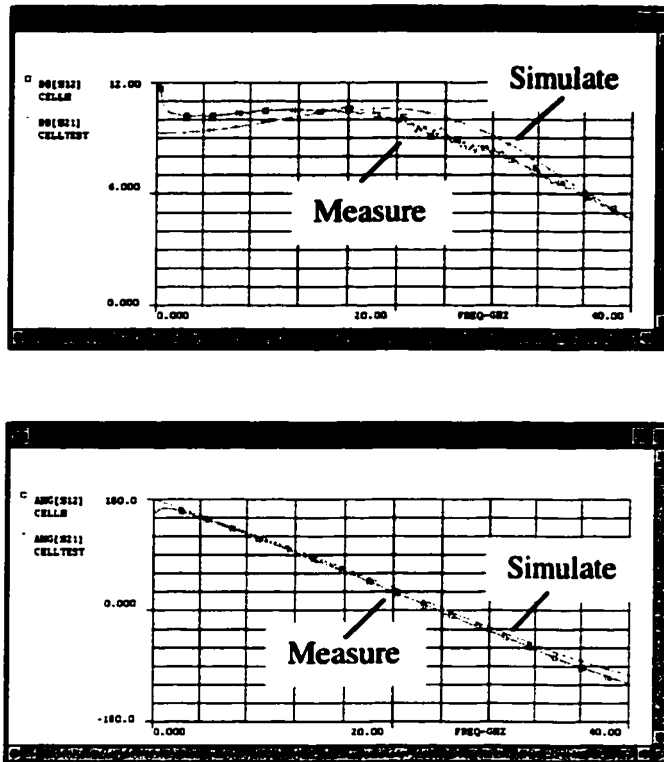


Figure 5-28 Measurement vs. simulation for a DA cell's S-parameters

5.3.2 S-parameters of HBT distributed amplifier

Figure 5-29 shows a picture of the fabricated HBT distributed amplifier MMIC chip. Figure 5-30 shows the measured S-parameters of the HBT distributed amplifier. The measured 3dB bandwidth of the HBT distributed amplifier is 35GHz, which is almost exact same as the simulated value. The difference between the measured S21 and simulated S21 is within 2dB. The measured input return loss S11 is good, which is below 15dB up to 30GHz and below 10dB up to 40GHz. The measured output return loss S22 is below 15dB up to 15GHz, below 7dB up to 40GHz. Basically, the design goals are achieved in the fabrication. The difference between measured and simulated S-parameters is likely due to the approximation of circuit modeling to actual circuit. The actual HBT process of Nortel was changed from the original design model. Even so, it still shows very good agreement between simulation and test results. The low frequency

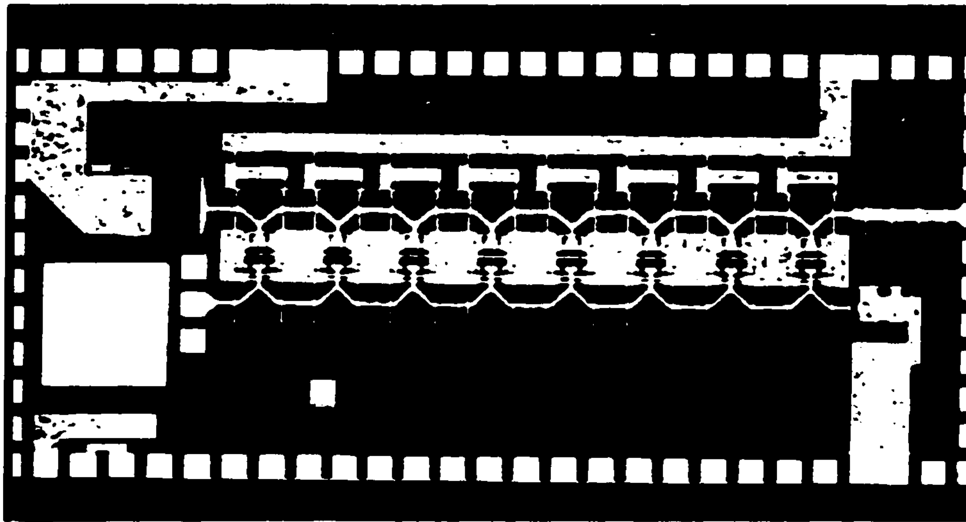


Figure 5-29 Micro photograph of the designed HBT distributed amplifier MMIC

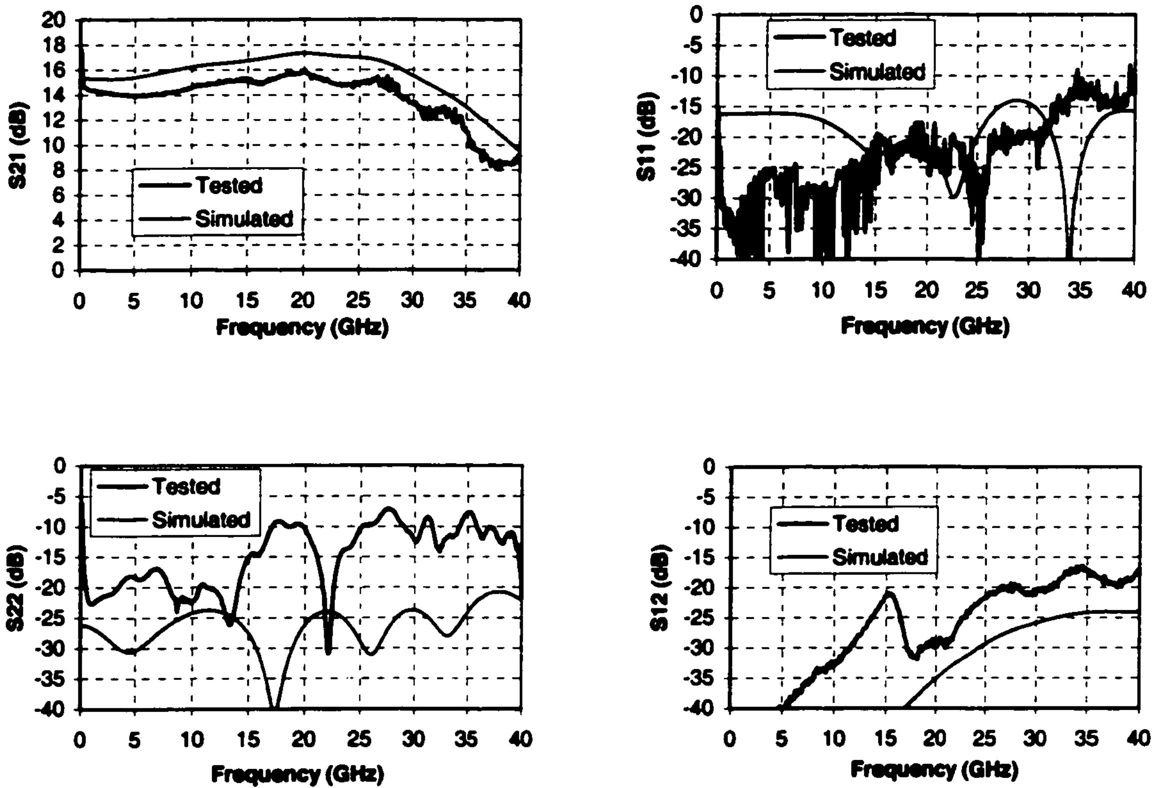


Figure 5-30 Measured vs. simulated S parameters of the designed HBT DA

(<1 GHz) gain drop is due to absence of off-chip decoupling caps on DC bias lines causing gain at low frequency to increase.

5.3.3 Optical Response of HBT P-I-N preamplifier

Figure 5-31 shows the picture of the fabricated HBT P-I-N preamplifier, which is a combination of an HBT distributed amplifier MMIC chip with a P-I-N diode mounted on the MMIC. The frequency response of the fabricated HBT P-I-N preamplifier was measured using an optical component analyzer. The optical power used for the test is 1.7mW at a1.5μm wavelength. Figure 5-32 shows the measured vs. simulated optical response of the photoreceiver. The P-I-N preamplifier's response exhibits a 3dB bandwidth of 22GHz (compared to 25GHz in simulation) and rolls off much more quickly than the predicted response. This discrepancy is discussed at the end of this Section. The measured frequency response is not flat at the low frequency end (within 3 GHz) due to the test method. During the preamplifier test, V_{cc} was applied to the MMIC chip's RF output line through bias-T instead of through the termination network. There was no off-chip decoupling single layer capacitance (SLC) connected to the V_{cc} pad. Therefore, the designed output TRL termination network didn't match to the ATL properly at low frequency. By adding an off-chip decoupling SLC, the low frequency response of the HBT P-I-N preamplifier will likely be improved.

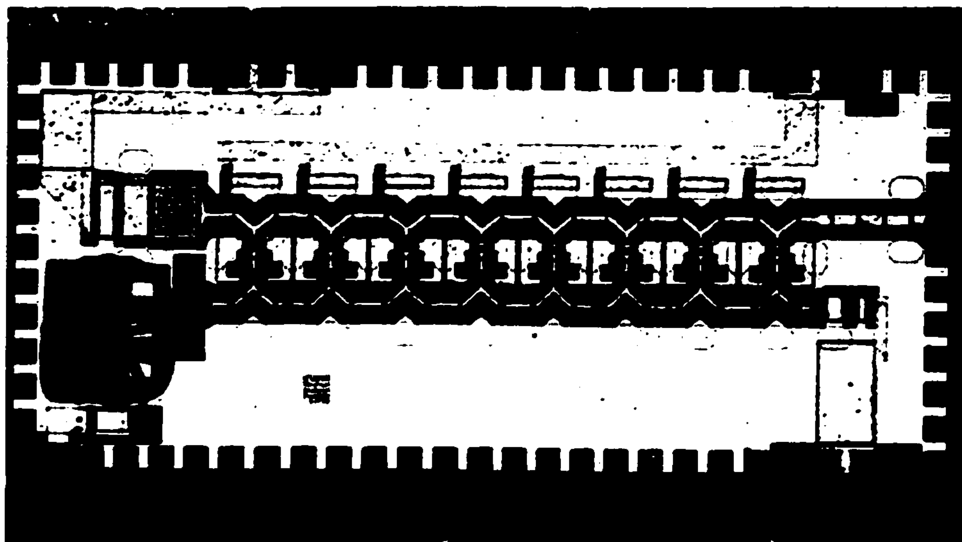


Figure 5-31 HBT preamplifier – P-I-N + HBT distributed amplifier MMIC chip

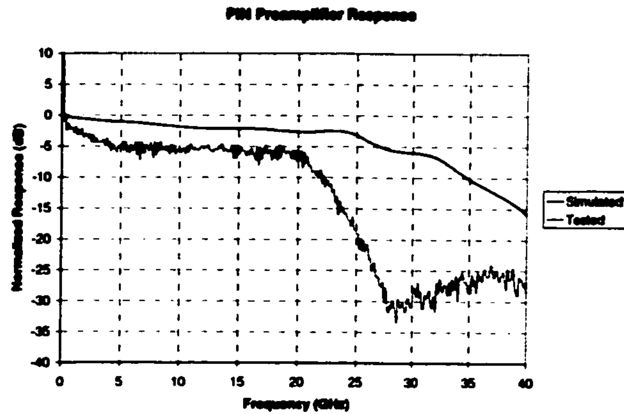
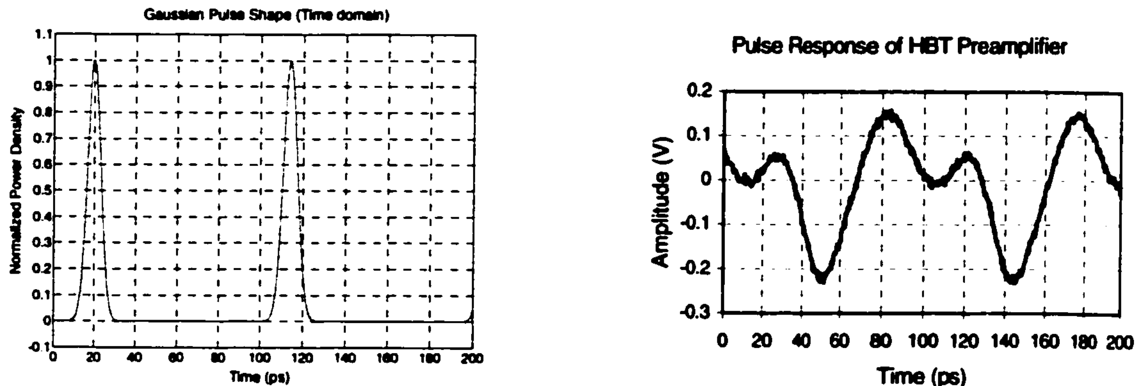


Figure 5-32 Measured vs. simulated optical response of the HBT P-I-N preamplifier

The HBT P-I-N preamplifier was also tested using optical pulse. The input signal is 7.75ps FWHM Gaussian pulse as shown in Figure 5-33a. The rate of the pulse sequence is 10.625Gbit/s. The average optical power is 0.17mW, while the optical power of the pulse is 1.7mW. Figure 5-33b shows the optical pulse response of the HBT P-I-N preamplifier measured by oscilloscope. Figure 5-34 shows the test setup and equipment used for the HBT P-I-N preamplifier test.



a. Input optical pulse

b. Output pulse response

Figure 5-33 Measured pulse response of the HBT P-I-N preamplifier

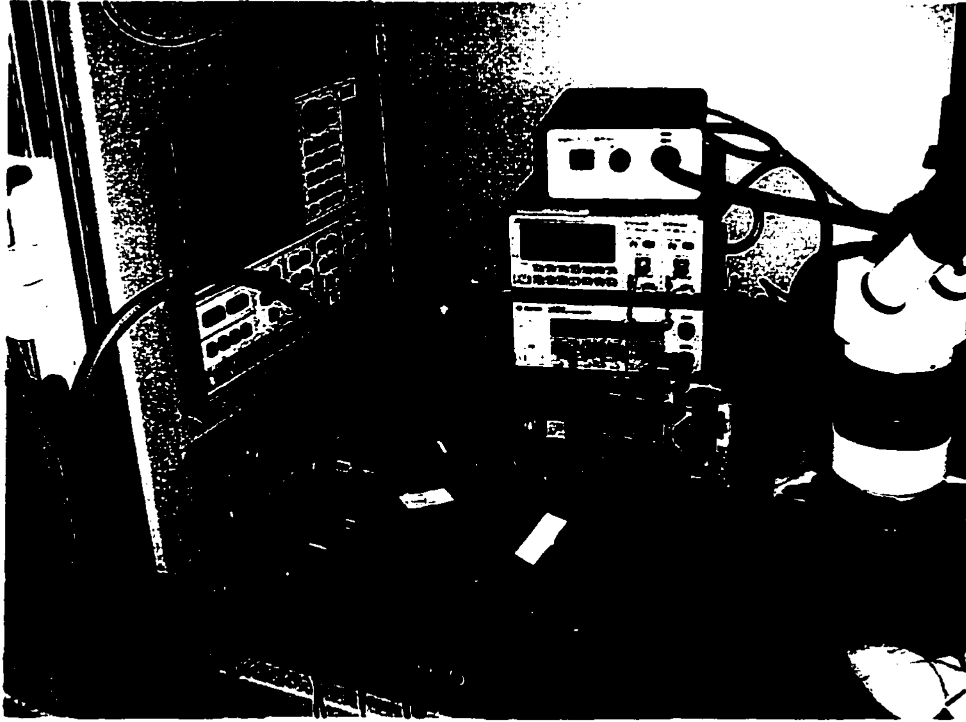


Figure 5-34 Test set up for HBT P-I-N preamplifier test

Discussion

Referring back to the unexpectedly narrow bandwidth of the optical response (Figure 5-32), this can only be explained by the P-I-N photodiode's bandwidth since the HBT distributed amplifier's electrical response matched simulation (S21 curve of Figure 5-30). The Nortel InGaAs P-I-N photodiode employed has a limited bandwidth due to its conventional vertically illuminated photodetector (VPD) structure [54]. It therefore cannot be expected to perform well at very high frequencies and traveling-wave photodetector structure should be employed instead [54]. However, the P-I-N characterization results of Chapter 4, which showed no such sharp rolloff, are inconsistent with the observed P-I-N preamplifier's performance. A possible explanation is that the operating conditions of the P-I-N diode during characterization were different than when it was employed in the preamplifier. For example, the P-I-N diode used a bias network in the final implementation which was not taken into account in the simulations. Also, wire bonds were used in the final circuit to connect the diode to the preamplifier input and to ground, whereas probes were employed for its characterization. The bias network and wire bonds can introduce significant parasitic effects beyond 20GHz and may be responsible for a resonance with the P-I-N's equivalent model elements at 27GHz.

5.3.4 Noise performance of HBT P-I-N preamplifier

The noise performance of the P-I-N preamplifier was measured to confirm the prediction. Both the measured and simulated equivalent input noise current density of the P-I-N preamplifier is shown in Figure 5-35. An average equivalent input noise current density of 24 $pA/\sqrt{Hz}$ was measured in the frequency range of 2–20GHz. At lower frequencies (below 3GHz), the measured noise appears much higher than expected. This is mainly due to the test setup, which allowed interfering radio frequency signals to be coupled into the circuit. Agreement is seen to be very good. This confirms the validity of the theoretical noise analysis for the proposed P-I-N HBT CCC preamplifier. We expect the analytical curve to be lower than the tested, because losses of ATL are not included in the

noise analysis. The fabricated MMIC was designed before the noise analysis had been completed. Therefore, further improvements to the noise performance of HBT P-I-N preamplifiers should be possible in future designs by exploiting the noise analysis fully.

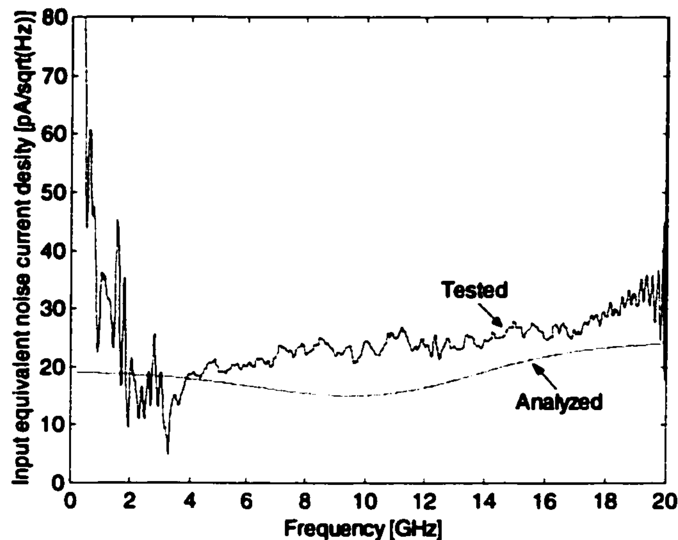


Figure 5-35 Measured vs. simulated equivalent input noise current density of the preamplifier

5.4 Conclusion

A photo receiver using a P-I-N and GaAs HBT CCC distributed amplifier combination is designed and implemented in this chapter, in which the three remaining thesis objectives have been met. In fulfillment of the first objective, a new 8-stage HBT distributed amplifier architecture is defined which offers potentially high gain and wide bandwidth. By considering the various issues involved in the design, a design procedure for MMIC chip is presented, thus achieving the third objective of the thesis. The preamplifier is analyzed using the analytical noise theory developed in Chapter 3. The performance of

the preamplifier is simulated by a commercially available EM simulator, as well as circuit CAD packages.

The implementation of the P-I-N HBT preamplifier is described. The measured results of the fabricated preamplifier are given. From the good agreement between the predicted and measured performance, the noise analysis and design method is considered validated. The successful operation of the HBT P-I-N preamplifier, which provides a 3dB bandwidth of 22GHz and an average equivalent input noise current density of 24 $pA/\sqrt{Hz}$, fulfills the final thesis objective of experimental verification. The designed P-I-N HBT preamplifier structure is the first to have a P-I-N mounted on the distributed amplifier MMIC chip.

Chapter 6 Conclusions and Future work

6.1 Thesis summary

This thesis has investigated the HBT distributed preamplifier design techniques for optical receiver applications, leading to a novel photoreceiver using a P-I-N and GaAs HBT distributed amplifier MMIC chip combination, which has been successfully demonstrated for optical systems.

Starting from a broad perspective, the evolution of optical communication system and MMIC development was reviewed in Chapter 2. It is concluded that the high-speed preamplifier is desired by optical communication system. The basic structure for an optical preamplifier is seen to be a P-I-N and a distributed amplifier combination. As high performance HBT devices evolve, the broad band HBT distributed amplifier has the potential for the high-speed applications.

The configuration of a novel high-speed HBT preamplifier is defined in Chapter 3 of the thesis. The techniques to extend bandwidth, increase trans-impedance gain, and improve noise performance for HBT preamplifiers are fully investigated. A theoretical noise analysis tool for the proposed HBT preamplifier is developed. First, a new HBT gain cell configuration (a combination of a CC and a Cascode) is described, which combines the advantages of the Common Collector circuit and the Cascode. This structure provides the required loss compensation for both input line and output line of a distributed amplifier. It has potential to build a broadband high gain distributed amplifier. The HBT gain cell's performance is characterized theoretically in terms of trans-impedance gain and input equivalent noise current densities. The artificial transmission line structure of a distributed amplifier, as well as P-I-N diode input integration circuit issues are also studied in this Chapter, respectively. Finally, the trans-impedance gain and input equivalent noise current density of the proposed HBT preamplifier are analyzed. The noise analysis gives useful insight into the dominant noise contributions of the HBT

preamplifier. The noise performance can be improved by increasing the input line's termination impedance. However, tradeoffs exist between a preamplifier's trans-impedance gain, bandwidth and noise performance.

As a construction element of the preamplifier, the P-I-N is fully characterized in Chapter 4. Broadband measurement techniques for P-I-N photo-detectors are investigated. Optical response measurements and input reflection coefficient measurement are performed for the P-I-N diode. Two different optical measurement methods —— pulse response and heterodyne are presented. The measurement results are compared between different methods. An electrical model of the P-I-N diode is derived from the measured input reflection coefficient S_{11}.

The implementation of a photoreceiver is described in Chapter 5. The photoreceiver is implemented as a combination of a P-I-N and the proposed HBT CCC distributed amplifier. An eight-stage HBT distributed amplifier MMIC is designed, and fabricated using Nortel's GaAs HBT process. The design procedure is presented. MMIC design requires unique design process due to its distributed circuit elements and many layout parasitic elements. Circuit modeling is a big challenge over such broad frequencies up to 40GHz. The EM simulator Sonnet, circuit simulator Hspice as well as EEsof are used to predict the preamplifier's performance with the guidance of the theoretic analysis in Chapter 3. The schematic design, chip layout and performance simulation for the preamplifier is interacted closely. The electrical model of the P-I-N diode as well as the wire bond inter-connections are integrated into the preamplifier circuit during the design so that their effects are included in the predicted performance of the HBT preamplifier. Finally, the P-I-N HBT preamplifier is fabricated and measured to confirm its predicted performance. The measurement results of the preamplifier are presented. Comparison between the measurement results and the predicted performance shows good agreement. Therefore, the noise analysis and design method is validated.

The implemented P-I-N HBT preamplifier in this thesis has a measured bandwidth of 22GHz, and measured average input equivalent noise current density of 24 $pA/\sqrt{Hz}$ in

the band of 2 - 20GHz. It is concluded that such a HBT preamplifier has good potential for the high-speed optical communication applications.

6.2 Future work

Although the goals of this study have been reached, the work pertaining to the high-speed preamplifier development is by no means complete. The following suggestions are made for furthering the work initiated here.

To further pursue the development of MMIC preamplifier, a MMIC integrating a P-I-N and HBT distributed amplifier in one chip should be developed so that the wire bond interconnection effects can be removed from a preamplifier's performance. In this thesis, the designed HBT preamplifier's performance is limited by the P-I-N diode's optical performance. A high performance P-I-N or other kind of photo detector should be investigated. A MMIC chip combining a broadband photo-detector and a HBT distributed amplifier will provide a high performance preamplifier for the optical receiver.

In order to achieve the noise performance benefits of the high input line impedance preamplifier, the termination impedance of the input line should be increased further. However, increasing input line impedance will lead to high losses for the input artificial transmission line. A technique to reduce the high impedance transmission line losses should be investigated.

In Chapter 3, a noise analysis theory is described for the proposed HBT preamplifier. Guided by this analysis theory, the HBT preamplifier's structure is defined. The noise performance of the designed P-I-N preamplifier is predicted based on this noise analysis theory. Further investigation based on this analytical noise expression should be made to find a way to improve the preamplifier's noise performance by reducing the HBT gain

cell's noise contribution. Since the structure of the HBT gain cell is complicated, it is beneficial to start with a HBT cell's performance characterization.

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