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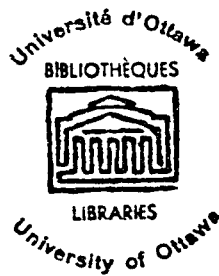
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A REMOTE PDP-8 INTERFACE

BY

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SUBMITTED TO THE DEPARTMENT OF  
ELECTRICAL ENGINEERING IN PARTIAL  
FULFILMENT OF THE REQUIREMENTS FOR  
THE DEGREE OF MASTER OF SCIENCE.



DEPARTMENT OF ELECTRICAL ENGINEERING  
FACULTY OF PURE AND APPLIED SCIENCE  
THE UNIVERSITY OF OTTAWA  
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NOTE:

THIS THESIS WAS TYPED ON A TELETYPE UNIT IN CONJUNCTION WITH A PDP-8 COMPUTER, USING THE DEC 8-1-S-BIN PROGRAM . THIS PROGRAM, CALLED "SYMBOLIC TAPE EDITOR", WAS DESIGNED TO HELP THE PROGRAMMER EDIT PROGRAMS WRITTEN IN SYMBOLIC LANGUAGE . IN OUR CASE, THIS PROGRAM WAS USED TO STORE ONE PAGE OF TEXT IN THE COMPUTER'S MEMORY, MODIFY THE TEXT LINE BY LINE, WHEN REQUIRED, AND THEN OUTPUT THE FINAL VERSION . THOUGH USEFUL, THIS PROGRAM IS FAR FROM BEING IDEAL . A PROGRAM DESIGNED SPECIFICALLY FOR THE PURPOSE OF EDITING WRITTEN TEXTS WOULD BE MOST DESIRABLE .

## ACKNOWLEDGEMENTS

I WISH TO THANK MY THESIS SUPERVISOR, DR. JAAN KRUUS, FOR HIS ADVICE AND PATIENCE, PROFESSOR THOMPSON FOR HIS COUNSELLING AND HIS FINANCIAL HELP IN THE PURCHASE OF THE INTEGRATED CIRCUITS USED, AS WELL AS ALL THE MEMBERS OF THE ELECTRICAL ENGINEERING DEPARTMENT, BOTH STAFF AND STUDENTS, FOR THEIR ASSISTANCE . THIS WORK WAS SUPPORTED BY NRC RESEARCH GRANTS A-2580 AND A-3379 .

## ABSTRACT

THIS THESIS DEALS WITH THE DESIGN AND CONSTRUCTION OF A COMMUNICATION SYSTEM FOR A DIGITAL EQUIPMENT CORPORATION PLP-3 DIGITAL COMPUTER. THE THESIS FIRST SHOWS THE GENERAL OPERATION OF THE COMPUTER AND THE SPECIFICATIONS OF THE REQUIRED SYSTEM AND THEN PROCEEDS TO STUDY VARIOUS POSSIBLE DESIGNS WHICH COULD MEET THE SPECIFICATIONS. THE DESIGNS ARE COMPARED AND THE ONE CONSIDERED BEST CHOSEN. THIS CHOSEN DESIGN IS FURTHER DEVELOPED AND ITS IMPLEMENTATION USING INTEGRATED CIRCUITS IS SHOWN IN DETAIL. THE DESIGN OF THE SYSTEM IS DISCUSSED AS A FUNCTION OF THE VARIOUS TASKS THAT THE SUBSYSTEMS MUST ACCOMPLISH.

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A.1	PDP-8 INSTRUCTIONS
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## 1. INTRODUCTION

THIS THESIS DEALS WITH A PROJECT BUILT TO SATISFY A DEFINITE NEED. THE NEED WAS THAT OF USING THE PDP-3 DIGITAL COMPUTER, LOCATED IN THE ELECTRICAL ENGINEERING DEPARTMENT, AS AN ON-LINE CONTROLLER FOR A HEAT EXCHANGER IN THE CHEMICAL ENGINEERING DEPARTMENT. THE DESIGN AND CONSTRUCTION OF A REMOTE INTERFACE FOR THE PDP-3 BUILT TO SATISFY THE ABOVE NEED IS DISCUSSED IN THIS THESIS.

A COMPUTER, TO SERVE AS AN ON-LINE CONTROLLER MUST SENSE DEVICES AND CONTROL A GIVEN SET OF PARAMETERS. IN THE PARTICULAR APPLICATION FOR WHICH THE SYSTEM WAS ORIGINALLY REQUIRED, SENSORS AT THE SITE OF THE EXPERIMENT PRODUCE ANALOG VOLTAGES WHICH CAN READILY BE CONVERTED INTO DIGITAL FORM BY MEANS OF AN ANALOG TO DIGITAL (A/D) CONVERTER. A MULTIPLEXER UNIT ALLOWS ONE CONVERTER TO SERVICE MANY CHANNELS OF ANALOG DATA, IN OUR CASE, UP TO 3 CHANNELS. IT IS ALSO POSSIBLE FOR THE EXPERIMENT TO USE SIMPLE ON-OFF CONTROLS, AND THESE ALSO MUST BE SENSED BY THE COMPUTER. IN THE OTHER DIRECTION THE COMPUTER HAS TO CONTROL DEVICES, SUCH AS VALVES, BY MEANS OF ANALOG VOLTAGES. THESE ANALOG SIGNALS CAN EASILY BE PRODUCED BY MEANS OF DIGITAL TO ANALOG (D/A) CONVERTERS. THE COMPUTER CAN ALSO HAVE SOME SWITCHING TASKS, SUCH AS ACTIVATING A RELAY.

IN ORDER TO ACCOMPLISH THESE VARIOUS TASKS, A REMOTE TERMINAL AS SIMILAR AS POSSIBLE TO THE PDP-8 'S PROGRAMMED DATA TRANSFER INTERFACE IS REQUIRED . FURTHERMORE , AND OF PRIMARY CONSIDERATION, THE PROGRAMMING INVOLVED IN USING THE REMOTE INTERFACE MUST BE AS SIMPLE AS POSSIBLE .

THOUGH THE HEAT EXCHANGER FOR WHICH THE SYSTEM WAS ORIGINALLY DESIGNED DID NOT NEED THIS SYSTEM'S FULL CAPACITIES, IT WAS FELT THAT THE CONSTRUCTION OF A GENERAL PURPOSE REMOTE INTERFACE CAPABLE OF SERVICING MANY REMOTE DEVICES WOULD RENDER THE PROJECT ALL THE MORE USEFUL TO THE ORIGINAL AND ITS FUTURE USERS.

## 2. PDP-8 OPERATION

### 2.1 GENERAL OPERATION

THE DIGITAL EQUIPMENT CORPORATION ( DEC ) PDP-8 IS A SMALL GENERAL PURPOSE DIGITAL COMPUTER WHICH USES 12 BIT WORDS, TWO'S COMPLEMENT ARITHMETIC AND A 4096 WORD<sup>1</sup> RANDOM ACCESS CORE MEMORY . THE COMPUTER HAS FOUR IMPORTANT REGISTERS; ITS OPERATION MAY BE DESCRIBED BY EXPLAINING THE FUNCTION OF EACH OF THESE REGISTERS .

THE PRINCIPAL REGISTER OF THE MACHINE IS THE TWELVE BIT ACCUMULATOR ( AC ). THE CONTENTS OF THIS REGISTER MAY BE CHANGED BY ARITHMETIC AND LOGIC OPERATIONS UNDER PROGRAM CONTROL . IT IS POSSIBLE TO DO THE FOLLOWING TO THE CONTENTS OF THE ACCUMULATOR:

- LOGICAL AND WITH
- LOGICAL OR WITH
- TWO'S COMPLEMENT ADD TO
- COMPLEMENT
- DEPOSIT IN CORE MEMORY
- SHIFT RIGHT OR LEFT
- INCREMENT
- CLEAR

1 - SMALL COMPUTER HANDBOOK, P. 33 , DEC

AS WILL BE SEEN IN THE NEXT SECTION, THE ACCUMULATOR SERVES AS A VITAL INPUT/OUTPUT REGISTER AS WELL .

THE MEMORY BUFFER ( MB ) REGISTER SERVES AS AN INTERFACE BETWEEN THE CORE MEMORY UNIT AND THE REST OF THE COMPUTER . ALL COMMUNICATIONS TO AND FROM THE MEMORY MUST GO THROUGH THE MB . THE ADDRESS OF THE LOCATION IN CORE MEMORY BEING SERVICED IS HELD IN THE MEMORY ADDRESS ( MA ) REGISTER .

NORMALLY, A PROGRAM, COMPOSED OF A SERIES OF TWELVE BIT CODES, IS STORED IN SUCCESSIVE MEMORY LOCATIONS. WHEN THE PROGRAM IS BEING EXECUTED, A REGISTER, THE PROGRAM COUNTER ( PC ) HOLDS THE ADDRESS OF THE LOCATION FROM WHICH THE NEXT INSTRUCTION IS TO BE TAKEN .

## 2.2 INPUT/OUTPUT ( I/O )

A LINKAGE EXISTS BETWEEN THE MACHINE AND THE OUTSIDE WORLD. THIS LINKAGE IS COMPRISED OF INPUT/OUTPUT EQUIPMENT CONNECTED TO THE COMPUTER THROUGH THE COMPUTER INTERFACE . EQUIPMENT SUCH AS TELETYPES, PUNCHES, TAPE READERS MAGNETIC DISCS AND MAGNETIC TAPES ARE ALL IN THIS GROUP . THE COMMUNICATION SYSTEM OF THIS THESIS IS ALSO AN I/O DEVICE.

A DEVICE MAY BE INTERFACED TO THE COMPUTER BY ONE OF TWO DIFFERENT LINKAGES . THE DATA BREAK FACILITIES ALLOW A DEVICE DIRECT AND EXTREMELY RAPID ACCESS TO AND FROM THE COMPUTER'S MEMORY, BUT THE TRANSFER OF DATA IS DONE INDEPENDENTLY OF THE PROGRAM BEING EXECUTED . THE TRANSFER MUST BE CONTROLLED BY THE EXTERNAL DEVICE . SINCE OUR COMMUNICATION SYSTEM DID NOT REQUIRE THE GREAT SPEED OF THIS FACILITY AND, MOREOVER, HAD TO BE UNDER PROGRAM CONTROL, THE ABOVE INTERFACING LINKAGE WAS DEEMED UNSATISFACTORY FOR OUR PURPOSE .

THE TERM " PROGRAMMED DATA TRANSFER" REFERS TO THE INPUT AND/OR OUTPUT OF DATA, UNDER PROGRAM CONTROL, BETWEEN THE COMPUTER AND AN EXTERNAL DEVICE . THE AC SERVES AS AN I/O REGISTER SINCE ALL PROGRAMMED DATA TRANSFERS MUST GO THROUGH IT. THE COMPUTER INTERFACE THEREFORE

CONTAINS BOTH AN INPUT TO AND AN OUTPUT FROM EACH BIT OF THE AC . THE INPUTS SERVE TO READ DATA INTO THE ACCUMULATOR AND THE OUTPUTS ALLOW THE STATE OF THE AC TO BE READ BY AN EXTERNAL DEVICE . THE COMPUTER INTERFACE ALSO HAS MB OUTPUTS WHICH ARE ACTIVATED WHENEVER AN I/O INSTRUCTION HAS JUST BEEN READ FROM CORE MEMORY . OTHER INTERFACE TERMINALS INCLUDE THE SKIP AND THE INTERRUPT REQUEST INPUTS, TO BE DISCUSSED LATER, AND OUTPUTS FOR THREE I/O PULSES DESIGNATED IOP 1, IOP 2, AND IOP 4 .

INPUT OUTPUT TRANSFER ( IOT ) INSTRUCTIONS ARE OF THE TYPES SHOWN BELOW:

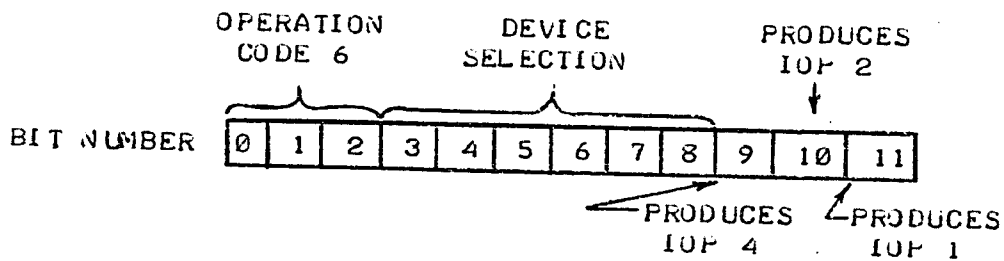


FIG. 2.2 -1 IOT INSTRUCTION BIT ASSIGNMENTS

AN OPERATION CODE OF 6 IN THE FIRST 3 BITS MEANS THAT IT IS AN IOT INSTRUCTION. WHEN SUCH AN INSTRUCTION IS ENCOUNTERED IN THE EXECUTION OF A PROGRAM THE MB OUTPUT TERMINALS ARE ACTIVATED . THE NEXT SIX BITS CORRESPOND TO THE CODE

OF THE I/O DEVICE WITH WHICH THE INSTRUCTION DEALS . EACH OF THE FINAL THREE BITS CAUSES THE GENERATION OF THE IOP PULSE CORRESPONDING TO IT . THESE PULSES OCCUR AT 1 - MICROSECOND INTERVALS WITH IOP 1, IF BIT 11 IS A 1, OCCURING FIRST, IOP 2 IF BIT 10 IS A 1, OCCURING SECOND AND IOP 4, IF BIT 9 IS A 1, OCCURING THIRD.

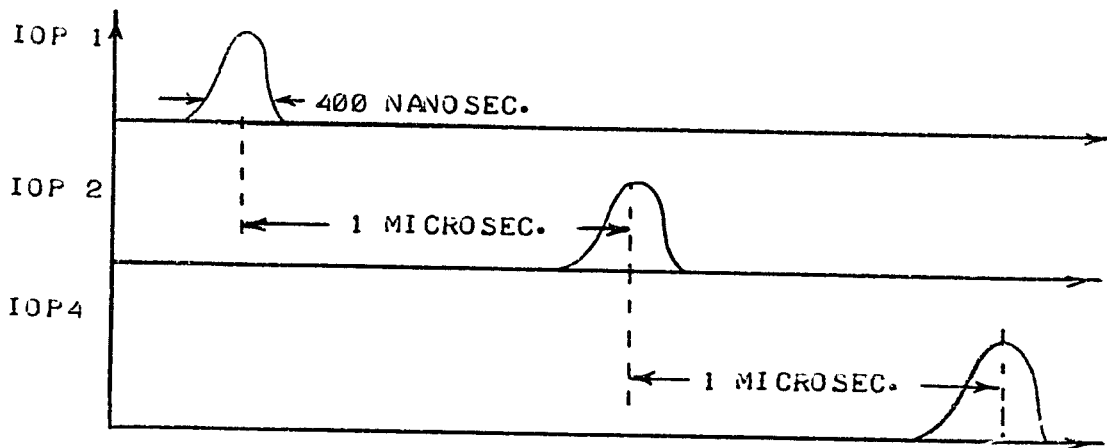


FIG. 2.2 - 2 IOP TIMING

TO EACH I/O DEVICE CORRESPONDS A DEVICE SELECTOR. EACH DEVICE SELECTOR IS CONNECTED TO THE MB OUTPUTS IN SUCH A WAY THAT IT IS ACTIVATED WHENEVER A CHOSEN DEVICE SELECTION CODE IS PRESENT IN MB 3 TO MB 8 . WHEN ACTIVATED THE DEVICE SELECTOR ENABLES THE IOP PULSES TO TRIGGER PULSE AMPLIFIERS TO PRODUCE STANDARD PULSES WHICH ARE NOW SPECIFIC TO THE DEVICE.

### 2.3 PROGRAM INTERRUPT (PI) AND INPUT/OUTPUT SKIP (IOS)

IN GENERAL, A DEVICE ASSOCIATED WITH THE COMPUTER HAS A FLIP-FLOP, CALLED A FLAG, WHICH THE DEVICE SETS WHEN IT REQUIRES SERVICING BY THE COMPUTER. THE GENERATION OF AN IOT PULSE CAN BE USED TO TEST THE STATUS OF A FLAG, AS SHOWN IN FIG. 2.3-1.

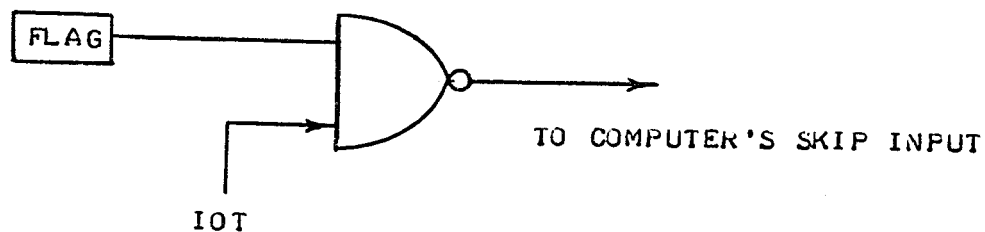


FIG. 2.3-1 SKIP UTILIZATION

THE OUTPUT OF THE GATE GROUNDS THE COMPUTER'S SKIP INPUT WHEN THE COMPUTER PRODUCES THE PROPER IOT PULSE TO THE GATE AND WHEN THE FLAG IS SET. THE EFFECT OF THIS GROUND PULSE ON THE SKIP INPUT CAUSES THE COMPUTER TO INCREMENT THE PROGRAM COUNTER AND SO SKIP THE NEXT INSTRUCTION IN THE PROGRAM. PROGRAMMING ASPECTS WILL BE COVERED IN A LATER SECTION.

THE PROGRAM INTERRUPT (PI) FACILITY, WHEN ENABLED BY THE PROGRAM, RELIEVES THE MAIN PROGRAM OF THE NEED FOR REPEATED FLAG CHECKS BY ALLOWING THE FLAGS TO AUTOMATICALLY CAUSE A PROGRAM INTERRUPT . AN INTERRUPT OCCURS WHENEVER THE FACILITY HAS BEEN ENABLED BY THE PROGRAM AND THE COMPUTER'S INTERRUPT REQUEST LINE IS BROUGHT TO GROUND . AN INTERRUPT CAUSES THE COMPUTER TO STORE THE PC IN LOCATION 0000 IN THE MEMORY CORE AND TO EXECUTE THE INSTRUCTION IN LOCATION 0001 . A PROGRAM USING THE PROGRAM INTERRUPT FEATURE IS INCLUDED IN ANOTHER SECTION .

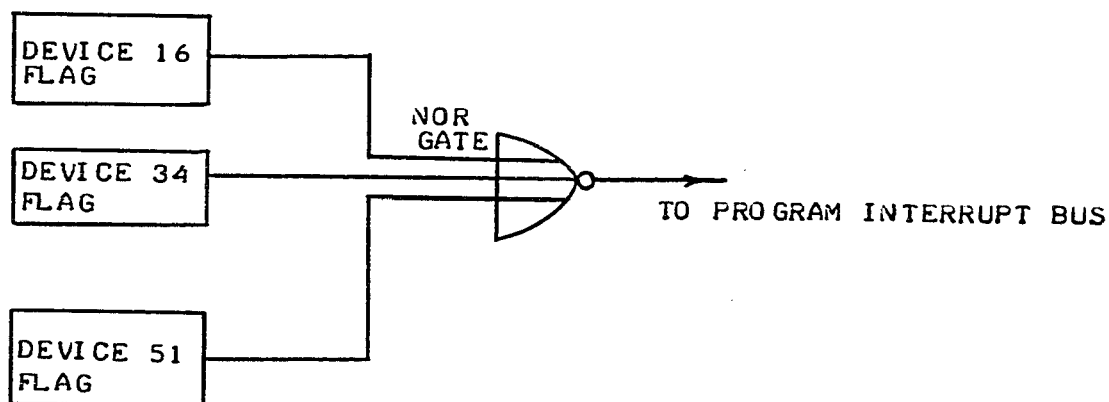


FIG. 2.3-2 MULTIPLE INPUTS TO PI

THE FACT THAT ANY ONE OF THE FLAGS IN THE ABOVE

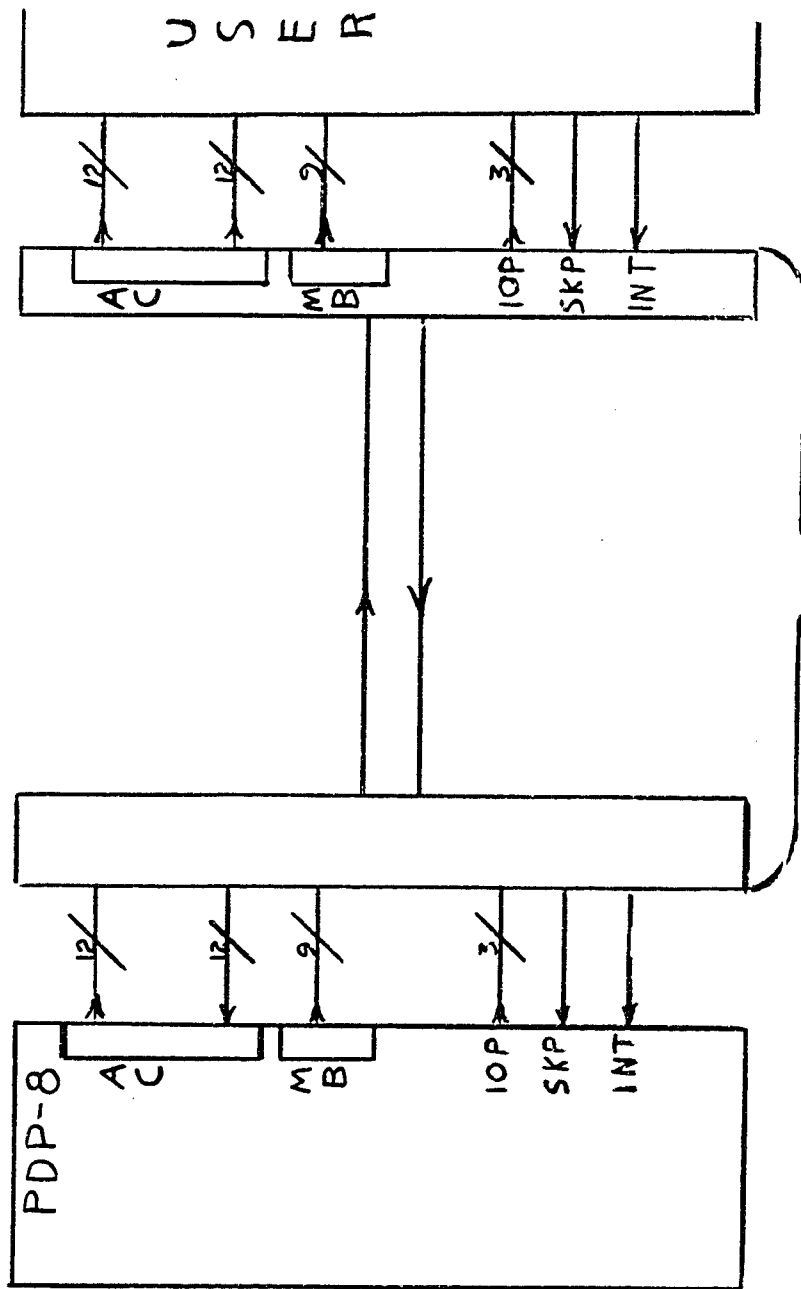
DIAGRAM IS SET WILL CAUSE A PROGRAM INTERRUPT. NORMALLY,  
THE COMPUTER WOULD BE PROGRAMMED SO AS TO DETERMINE BY  
MEANS OF THE SKIP FACILITY WHICH DEVICE GAVE THE  
INTERRUPT AND TO SERVICE THAT DEVICE .

### 3. DESIRED SYSTEM CHARACTERISTICS

#### 3.1 IDEAL REMOTE INTERFACE

THE REMOTE INTERFACE WAS TO BE USED TO LINK THE PDP-8 TO SOME EXPERIMENTS WHICH REQUIRED AN ON-LINE CONTROLLER . TO BE ADEQUATELY SERVICED BY THE COMPUTER, THESE EXPERIMENTS MUST MAKE USE OF AN INTERRUPT-LIKE FACILITY . FURTHERMORE, THE SYSTEM WAS TO HAVE THE ABILITY TO USE EXISTING EQUIPMENT NOW CONNECTED TO THE COMPUTER'S INTERFACE WITH LITTLE OR NO MODIFICATIONS TO THAT EQUIPMENT . IN THE IDEAL CASE PRESENTED IN FIG. 3.1-1, ALL INTERFACE CONNECTIONS USED IN PROGRAMMED DATA TRANSFERS WOULD BE BROUGHT TO THE USER AT THE REMOTE INTERFACE . THE IDEAL DATA LINK WOULD HAVE TO BE FAST ENOUGH TO KEEP THIS REMOTE TERMINAL IN STEP WITH THE COMPUTER .

THE COMPUTER INTERFACE HAS THE ABILITY TO SERVICE UP TO 64 I/O CHANNELS . THE REQUIRED REMOTE INTERFACE WOULD, HOWEVER, NEVER HAVE TO SERVICE THAT MANY DEVICES . IT WAS FELT THAT THE ABILITY TO PROVIDE 16 CHANNELS AT THE REMOTE INTERFACE <sup>W</sup>OULD BE ADEQUATE . FOR THIS PURPOSE, ONLY A FOUR BIT DEVICE SELECTION CODE IS REQUIRED, A SAVING OF TWO BITS . THIS WILL ALSO REDUCE THE HARDWARE COST .



NOTE:  $\frac{n}{-}$  signifies  $n$  parallel lines.

DATA LINK

Fig 3.1-1

### 3.2 PRACTICAL CONSIDERATIONS

THE DATA LINK BETWEEN THE REMOTE INTERFACE AND THE COMPUTER WILL, OF COURSE, HAVE CERTAIN SPEED LIMITATIONS . IN THE CASE OF THE SYSTEM'S ANTICIPATED USER THE ABILITY TO TRANSMIT ONE MESSAGE PER SECOND WOULD BE MORE THAN ADEQUATE . IN ORDER TO SATISFY ANTICIPATED FUTURE NEEDS, IT WAS DECIDED TO ESTABLISH A MINIMUM RATE OF 1000 BITS PER SECOND .

THE DATA LINK WILL ALSO INTRODUCE SOME TIME DELAY . LET US CONSIDER THE CASE OF AN I/O INSTRUCTION USED TO READ DATA FROM A BUFFER AT THE REMOTE SITE . IN THE IDEAL CASE, THE I/O INSTRUCTION AND ITS CORRESPONDING IOP PULSES WOULD APPEAR AT BOTH THE COMPUTER INTERFACE AND THE REMOTE INTERFACE AT THE SAME TIME .

IDEALLY, DATA READ FROM A DEVICE CONNECTED TO THE REMOTE INTERFACE WOULD INSTANTANEOUSLY BE TRANSFERRED TO THE COMPUTER . IN REALITY, THERE WOULD BE DELAYS IN BOTH DIRECTIONS OF COMMUNICATION . AN IDEAL SYSTEM OF THE TYPE SHOWN IN FIG. 3.1-1 CAN ONLY FUNCTION IF THE TOTAL DELAY FOR THE ABOVE IS LESS THAN 1 MICROSECOND. TO GET THIS MEANS A BANDWIDTH OF SEVERAL MEGAHERTZ .

THE SYSTEM'S ANTICIPATED USER ONLY REQUIRES THE SYSTEM TO HANDLE AT THE VERY MOST A FEW MESSAGES PER SECOND SO THAT THE USE OF SUCH A LARGE BANDWIDTH DATA LINK WOULD SEEM RIDICULOUS . IT WAS DECIDED TO DESIGN FOR A RATE OF 1000 BITS PER SECOND FOR EACH DIRECTION OF THE DATA LINK .

WITH THE DIRECT UTILIZATION OF THE PDP-8 INTERFACE THE TIME REQUIRED TO IDENTIFY WHICH DEVICE HAS PRODUCED AN INTERRUPT IS RATHER SHORT, ON THE AVERAGE, ABOUT 10 MICROSECONDS IF FOUR DEVICES WERE CONNECTED . WITH THE USE OF THE REMOTE INTERFACE, TO DO THE SAME IDENTIFYING SUBROUTINE COULD BE PROHIBITIVELY LONG DUE TO THE TIME REQUIRED TO SEND MANY DEVICE INTERROGATION CODES OVER THE COMMUNICATION CHANNEL . THE FINISHED SYSTEM WAS THEREFORE CALLED UPON TO ACHIEVE SOME FORM OF INTERRUPT SERVICING ITSELF .

OF PRIMARY CONSIDERATION IS EASE OF PROGRAMMING . TO THE USER, THE USE OF THE DATA LINK MUST BE AS SIMPLE AS POSSIBLE . THIS REQUIREMENT IS VITAL AND MUST BE MET IF THE SYSTEM IS TO BE OF ANY PRACTICAL USE .

### 3.3 SPECIFICATIONS

BASED ON THE PREVIOUS SECTION, WE MAY STATE THE BASIC SYSTEM SPECIFICATIONS:

- 1- MINIMUM TRANSMISSION RATE OF 1000 BITS PER SECOND .
- 2- SIXTEEN REMOTE I/O CHANNELS.
- 3- INTERRUPT SERVICING AT REMOTE INTERFACE .
- 4- PROGRAMMING EASE .

THE FIRST TWO POINTS ARE CHOSEN ARBITRARILY AS THE GRADE OF SERVICE WE WISH TO ACHIEVE. IT WAS FELT THAT THESE DESIGN OBJECTIVES WERE REALISTIC , CONSIDERING THE FUTURE USES TO WHICH THIS PROJECT COULD BE APPLIED. THE THIRD SPECIFICATION EVOLVED FROM THE FACT THAT THE REMOTE INTERFACE WAS TO BE AS SIMILAR AS POSSIBLE TO THE PDP-8 INTERFACE AND THAT THE INTERRUPT FEATURE IS ONE OF ITS PRINCIPAL CHARACTERISTICS. COMBINING THIS WITH THE FACT THAT THE DATA LINK WILL BE MUCH SLOWER THAN THE COMPUTER, IT BECAME EVIDENT THAT INTERRUPTS WOULD HAVE TO BE DEALT WITH AT THE REMOTE INTERFACE WITH NO DIRECT COMPUTER INTERVENTION. TO BE OF ANY USE THE FINAL SYSTEM MUST BE AS SIMPLE TO USE AS POSSIBLE, THUS A PRIMARY GOAL OF PROGRAMMING SIMPLICITY MUST BE MET BY THE SYSTEM. THIS FINAL SPECIFICATION MUST BE MET EVEN IF IT MEANS GREAT HARDWARE COMPLEXITY.

## 4. DATA TRANSMISSION SYSTEMS

## 4.1 POSSIBLE DESIGNS

MANY ALTERNATIVES WERE CONSIDERED IN ORDER TO ACHIEVE THE GIVEN SYSTEM SPECIFICATIONS. THE TABLE BELOW SHOWS THE ALTERNATIVES CONSIDERED.

MODE	CONDUCTOR	MEANS
PARALLEL	RADIO	FREQUENCY MULTIPLEX
SERIAL (SOFTWARE IMPLEMENTED)	SINGLE COAXIAL CABLE	TIME MULTIPLEX
	TWO COAXIAL CABLES	DIRECT
SERIAL (HARDWARE IMPLEMENTED)	SINGLE TELEPHONE LINE	
	TWO TELEPHONE LINES	
	MANY TELEPHONE LINES	

FIG. 4.1-1

THE ABOVE ALTERNATIVES CAN BE GROUPED INTO THREE

- SECTIONS: 1) RADIO  
2) PARALLEL WIRE TRANSMISSION  
3) SERIAL WIRE TRANSMISSION

#### 4.2 RADIO

THE POSSIBILITY OF USING A RADIO LINK BETWEEN THE COMPUTER SITE AND THE REMOTE SITE WAS CONSIDERED. RADIO TRANSMISSION COULD USE TIME MULTIPLEXING TO SHIFT OUT THE DATA SEQUENTIALLY OVER ONE CARRIER OR, ALTERNATIVELY, FREQUENCY MULTIPLEXING USING MANY SUBCARRIER FREQUENCIES COULD BE USED. THE USE OF A RADIO CHANNEL WOULD MEAN THE PURCHASE OF TWO TRANCEIVERS, AT A COST OF SEVERAL HUNDREDS OF DOLLARS EACH. EQUIPMENT AT EACH END OF THE RADIO LINK TO MULTIPLEX OUTGOING DATA AND RECONSTRUCT INCOMING DATA WOULD ALSO BE REQUIRED. FOR OUR PURPOSES, THE TOTAL COST OF A RADIO CHANNEL WAS CONSIDERED PROHIBITIVE; THUS THIS POSSIBILITY WAS RULED OUT.

#### 4.3 PARALLEL WIRE

ANOTHER WAY OF TRANSFERING DATA WOULD BE TO USE ONE CONDUCTOR PER BIT AND TRANSMIT DIRECTLY. BY THIS, WE MEAN THAT EACH OUTPUT WOULD HAVE A WIRE DIRECTLY CONNECTING IT TO ITS CORRESPONDING OUTPUT TERMINAL AT THE REMOTE SITE.

AS DISCUSSED IN THE PREVIOUS CHAPTER, WE HAVE A TOTAL OF 19 LOGICALLY INDEPENDENT OUTPUTS TO BE TRANSMITTED FROM THE REMOTE TO THE COMPUTER. THE COST OF RENTAL OR PURCHASE OF A CABLE WITH SUCH A LARGE NUMBER OF CONDUCTORS WAS DEEMED RATHER HIGH FOR ANY BUT THE SHORTEST DISTANCES.

ADDITIONAL DIFFICULTIES WOULD OCCUR WITH THIS SYSTEM DUE TO THE NEED TO COMPENSATE FOR TIME DELAYS ON THE TRANSMISSION LINES. AS AN EXAMPLE WE CAN CONSIDER THE EXECUTION OF READING DATA FROM A REMOTE DEVICE. THE COMPUTER WOULD HAVE TO WAIT AFTER ASKING FOR DATA TO ALLOW FOR TIME DELAYS IN THE LINE. IF INDEED THE DEVICE HAD NO DATA TO SEND, THEN THE WAIT WOULD HAVE BEEN IN VAIN. THE DELAY OVER TELEPHONE LINES WOULD BE IN THE ORDER OF 100 MICROSECONDS OVER A 100 METER LENGTH. THE VERY FACT THAT THE COMPUTER MUST WAIT TWICE THIS LENGTH OF TIME FOR EVERY I/O INSTRUCTION TO BE CARRIED OUT AT THE REMOTE AND THAT THIS MUST BE ACCOMPLISHED USING SOME RATHER COMPLEX SOFTWARE, REMOVES MOST OF THE ADVANTAGES WHICH THIS SYSTEM MAY HAVE SEEMED TO POSSESS. FURTHERMORE, DRIVING MANY PARALLEL WIRES CAUSES BOTH DRIVING AND CROSSTALK PROBLEMS.

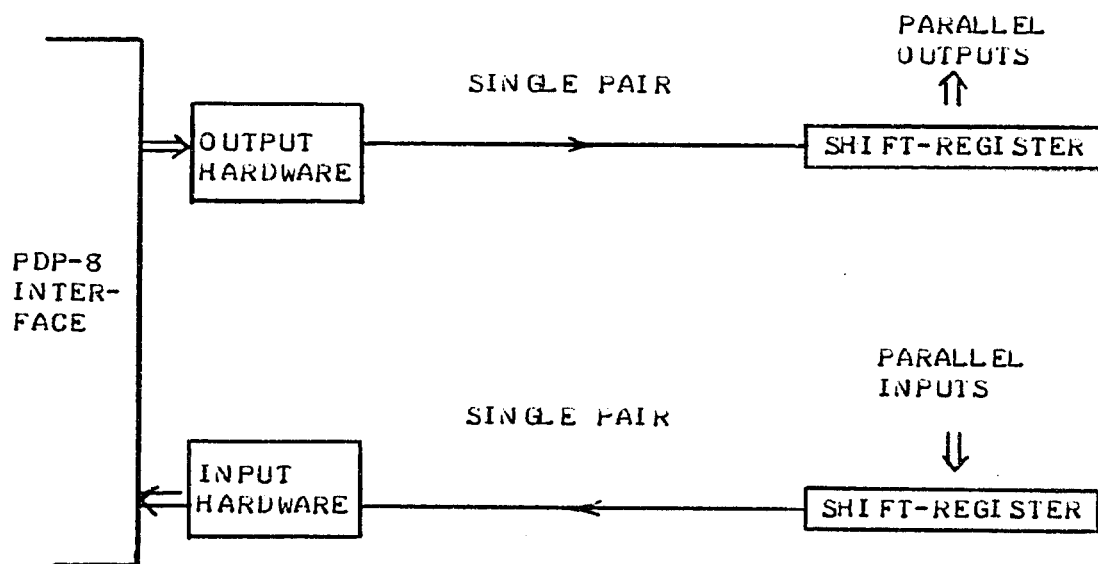
#### 4. 4 SERIAL WIRE TRANSMISSION

THE POSSIBILITIES NOT YET DISCUSSED ARE COAXIAL CABLES AND TELEPHONE LINE PAIRS. ESSENTIALLY THE DIFFERENCE BETWEEN THE TWO IS ONE OF BANDWIDTH. THE HIGHER FREQUENCY CAPABILITIES OF COAXIAL CABLES WOULD ENABLE VERY HIGH RATES OF DATA TRANSMISSION USING EITHER TIME MULTIPLEX OR FREQUENCY MULTIPLEX. THOUGH OVER SHORT DISTANCES COAXIAL CABLE IS NOT EXPENSIVE, RG/58-U COSTING ONLY \$13./1000FT., IT WAS FELT THAT SINCE THERE WAS NO NEED FOR THE ADDED BANDWIDTH OF COAXIAL CABLE, THE SYSTEM WOULD USE , AT LEAST INITIALLY , REGULAR TELEPHONE LINE PAIRS, AND SERIAL TRANSMISSION. IF EVER ANOTHER USER DESIRED FASTER TRANSMISSION RATES, COAXIAL CABLES COULD BE INSTALLED AND THE TRANSMISSION RATE INCREASED.

WE ARE LEFT WITH THE POSSIBILITY OF USING ONE TELEPHONE LINE PAIR AND TRANSMITTING IN FULL DUPLEX MODE OR USING TWO SEPARATE PAIRS, ONE FOR EACH DIRECTION OF DATA FLOW, AND TRANSMITTING IN SIMPLEX MODE OVER EACH ONE. THE LATTER WAS CHOSEN BECAUSE THE USE OF ONE TELEPHONE LINE PAIR IN FULL DUPLEX MODE WOULD ESSENTIALLY RENDER THE SERVICING OF INTERRUPTS AT THE REMOTE SITE VERY DIFFICULT, WOULD HALVE THE TRANSMISSION THROUGH-PUT RATE, AND WOULD GREATLY INCREASE THE SYSTEM COMPLEXITY.

## 4.5 CHOSEN SYSTEM

THUS, IT WAS DECIDED TO USE TWO TELEPHONE LINE PAIRS AND TRANSMIT DATA SERIALLY OVER THEM. AT THE REMOTE SITE SOME FORM OF EQUIPMENT IS NECESSARY TO CONVERT THE INCOMING DATA FROM SERIAL TO PARALLEL. AND THE OUTGOING DATA FROM PARALLEL TO SERIAL. AT THE COMPUTER SITE THESE TASKS COULD BE ACHIEVED EITHER BY THE COMPUTER WITH ADDITIONAL SOFTWARE OR BY ADDITIONAL HARDWARE. INDEED, THESE TASKS COULD BE ACHIEVED USING SOME HYBRID FORM OF THE ABOVE. REGARDLESS OF THE ABOVE CHOICE, THE SYSTEM WILL POSSESS THE FORM SHOWN IN THE FOLLOWING DIAGRAM.

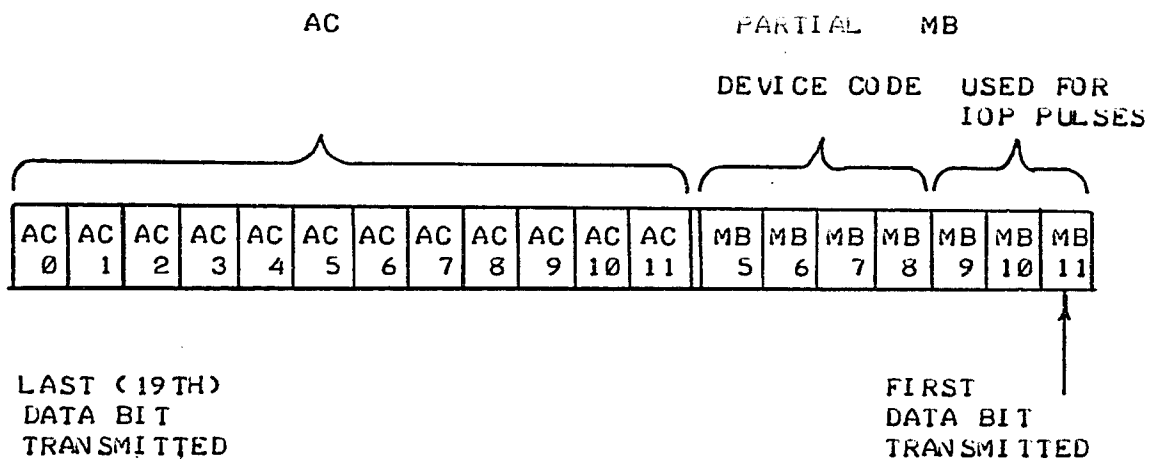


GENERAL SYSTEM FORM FIG. 4.5-1

## 4.6 HARDWARE VERSUS SOFTWARE IMPLEMENTATION

AS MENTIONED IN THE PREVIOUS SECTION, TWO WAYS OF IMPLEMENTING THE REQUIRED FUNCTIONS AT THE COMPUTER SITE ARE POSSIBLE: HARDWARE OR SOFTWARE. WE WILL FIRST CONSIDER THE TRANSMISSION OF A MESSAGE FROM THE PDP-8 TO THE REMOTE INTERFACE.

AS DISCUSSED IN THE SYSTEM CHARACTERISTICS OF SECTION 3.1, A COMPLETE TRANSMISSION WOULD CONSIST OF 12 ACCUMULATOR BITS, 3 BITS TO PRODUCE IOP PULSES AT THE REMOTE, AND A 4 BIT REMOTE DEVICE CODE. THEY COULD, AND INDEED ARE, SENT OUT AS DESCRIBED IN THE FOLLOWING DIAGRAM.



MESSAGE FORM FIG. 4-6-1

USING HARDWARE IMPLEMENTATION THE COMPUTER WOULD READ TWICE INTO AN EXTERNAL SHIFT REGISTER, ONCE FOR THE AC SECTION AND ONCE FOR THE MB SECTION . A SUBROUTINE TO DO THE ABOVE IS PRESENTED IN THE FOLLOWING CHAPTER . THE TOTAL EXECUTION TIME OF THE SUBROUTINE IS ABOUT 20 MICROSECONDS .

USING SOFTWARE IMPLEMENTATION, THE SERIALIZING COULD BE DONE BY THE COMPUTER AT A RATE DETERMINED BY AN INTERRUPT PRODUCING CLOCK . THE ONLY NEW HARDWARE REQUIRED WOULD BE THE CLOCK, A SINGLE BUFFER FLIP-FLOP CONNECTED TO THE LINE AND A FEW GATES SO THAT THE FOLLOWING CODES WOULD FUNCTION AS DESCRIBED:

6121 / SKIP ON CLOCK FLAG

6122 / START CLOCK, CLEAR FLAG, READ AC 11 INTO LINE BUFFER

6124 / STOP CLOCK, CLEAR FLAG, CLEAR BUFFER

( GIVEN THAT DEVICE NUMBER 12 HAS BEEN ALLOCATED TO THE UNIT . )

SUBROUTINES, WRITTEN IN PAL III, TO IMPLEMENT THE SERIALIZING, ARE GIVEN IN FIG. 4.6-2 . ESSENTIALLY, FOR EVERY MESSAGE SENT, THE COMPUTER WOULD HAVE TO DO SUBROUTINE "TRANS1" ONCE, THIS TO INITIATE THE TRANSMISSION, AND THEN DO SUBROUTINE "TRANS2" 19 TIMES TO SHIFT OUT THE DATA . EXECUTION TIME OF "TRANS1" IS ABOUT 25 MICROSECONDS AND OF "TRANS2" IS ABOUT 30

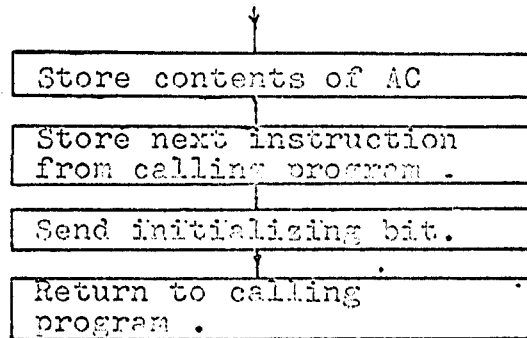
```

/ MAIN PROGRAM
.
.
JMS TRANS1
DXL          / MESSAGE TO BE SENT
.           / THE MAIN PROGRAM CONTINUES
.
.
/ SUBROUTINES
/ INTERRUPT SERVICE
ZERO, 0000
6121
JMP TRANS2
/ TRANSMIT SUBROUTINES
TRANS1, 0000
DCA T1      / STORE AC
TAD I TRANS1
DCA T2      / STORE DXL
IAC
6122      / SEND INITIALIZING BIT
CLA
TAD M7      / MINUS 7
DCA C1
TAD M19     / MINUS 19
DCA C2
TAD T1
JMP I TRANS1
M7, 7771
M19, 7755
TRANS2, DCA T3      / SAVE AC
RAL
DCA T4      / SAVE LINK
TAD T2
6122      / SEND OUT DATA
RAL        / SHIFT
DCA T2
ISZ C1
JMP .+3
TAD T1
DCA T2      / AC PLACED IN T2
ISZ C2      / END ?
JMP.+3
6124      / STOP CLOCK
JMP .+2
6122      / START CLOCK
TAD T4
RAR        / RESET LINK
TAD T3      / RESET AC
ION
JMP I Z ZERO

```

/( FIG. 4.6-2)

Trans1 Subroutine  
( called from main program )



Trans2 Subroutine  
( called by interrupt executive )

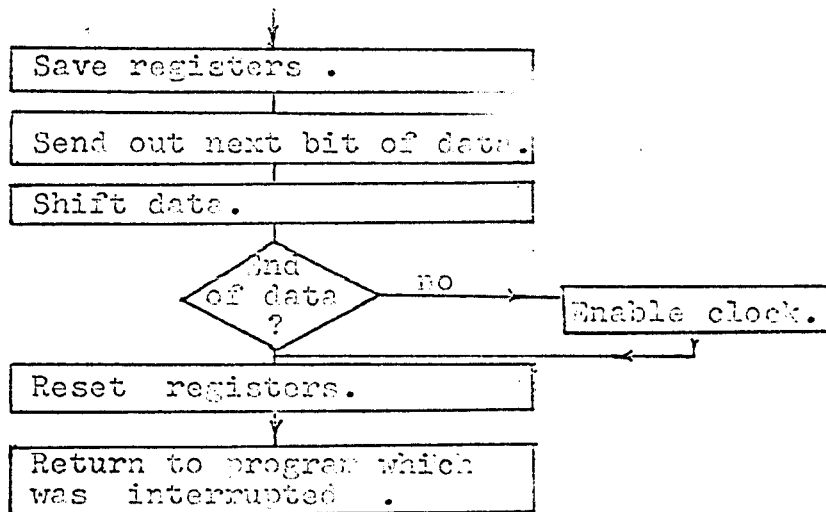


Fig. 4.6-2a  
Program flow-graph

MICROSECONDS . TOTAL EXECUTION TIME FOR ONE TRANSMISSION IS THUS ABOUT 600 MICROSECONDS . IN OTHER WORDS, THE COMPUTER MUST BE AWAY FROM THE MAIN PROGRAM FOR A TOTAL OF 600 MICROSECONDS DURING THE PROCESS OF A SINGLE TRANSMISSION .

AT A TRANSMISSION RATE OF 10K BITS/SECOND, A FULL TRANSMISSION WOULD TAKE 1.9 MILLISECONDS . AT THIS SPEED THE COMPUTER IS ALREADY BUSY 1/3 OF THE TIME TO SERVICE THE TRANSMITTER UNIT . ALLOTING AN EQUAL AMOUNT OF TIME FOR SERVICING THE RECEIVER UNIT AND ON THE AVERAGE 8 MICROSECONDS TO DETERMINE WHICH OF THE TWO UNITS, THE TRANSMITTER OR THE RECEIVER, CAUSED THE INTERRUPT, WE FIND THAT THE COMPUTER IS BUSY 100% OF THE TIME AT A TRANSMISSION RATE OF 10K BITS PER SECOND AND CANNOT DO ANYTHING ELSE .

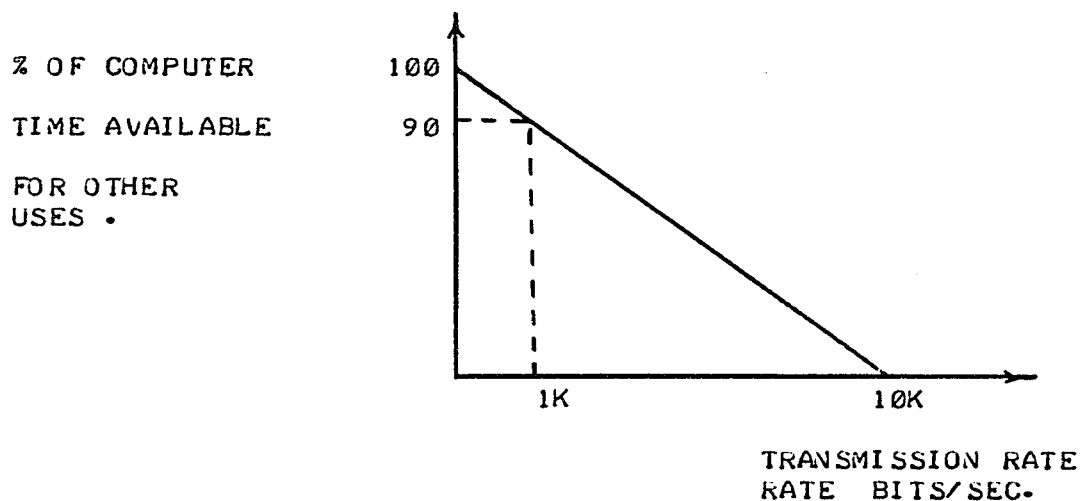


FIG. 4.6-3 COMPUTER TIME UTILIZATION

THE SYSTEM, USING SOFTWARE IMPLEMENTATION, WOULD HAVE AN UPPER BOUND OF 10K BITS PER SECOND ON THE TRANSMISSION RATE . EVEN AT A RATE OF 1K BITS PER SECOND, ALREADY 10% OF THE COMPUTER TIME IS TAKEN BY THE SUBROUTINES . BECAUSE OF THE ABOVE REASONS, AND SINCE THE DATA LINK WAS TO BE AS SIMPLE AS POSSIBLE FROM A SOFTWARE POINT OF VIEW, IT WAS DECIDED TO USE HARDWARE RATHER THAN SOFTWARE TO IMPLEMENT THE REQUIRED FUNCTIONS AT THE COMPUTER SITE . THE PRICE PAID FOR SOFTWARE SIMPLICITY IS HARDWARE COMPLEXITY .

## 5. DESIGN DEVELOPMENT

### 5.1 HARDWARE CHOICE

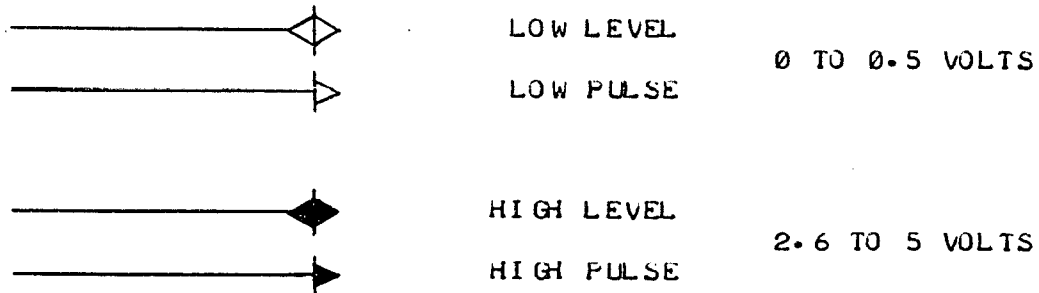
THE CHOSEN DESIGN MAKES USE OF A TOTAL OF FOUR SHIFT-REGISTERS AND A LARGE AMOUNT OF REQUIRED CONTROL LOGIC. BECAUSE OF THE AMOUNT OF EQUIPMENT TO BE BUILT, IT WAS DECIDED TO USE INTEGRATED CIRCUITS ( I.C. 'S ) TO ACHIEVE IMPORTANT SAVINGS AND TO GAIN EXPERIENCE IN USING THESE NEW DEVICES. MOTOROLA MC830P SERIES, USING DIODE-TRANSISTOR LOGIC (MDTL), I.C. 'S WERE CHOSEN ON A BASIS OF COST AND AVAILABILITY. THIS DECISION WAS TAKEN IN EARLY 1967. AT PRESENT THE PURCHASE OF I.C. MODULES, AVAILABLE FROM MANY SOURCES, INCLUDING DEC, AT QUITE REASONABLE COST, WOULD DEFINITELY BE A MUCH WISER DECISION.

AT THAT TIME HOWEVER, THE CHOICE WAS BETWEEN THE CHOSEN I.C. 'S AND STANDARD DEC R SERIES UNITS. A \$ 10.00 SAVING PER FLIP-FLOP WAS REALIZED BY BUYING THE I.C. 'S RATHER THAN THE DEC EQUIPMENT . IT WAS FELT THAT THIS PRICE ADVANTAGE WOULD MORE THAN OFFSET ANY ADDITIONAL COSTS, SUCH AS THAT OF LOGIC LEVEL CONVERTERS, WHICH WOULD BE INCURRED BECAUSE OF THE USE OF I.C. 'S. THERE ARE, IN THE FINAL SYSTEM, A LITTLE OVER 100 FLIP-FLOPS SO THAT JUST IN THOSE UNITS A SAVING OF \$ 1000.00 WAS REALIZED.

## 5.2 LOGIC LEVELS AND RELATIONS

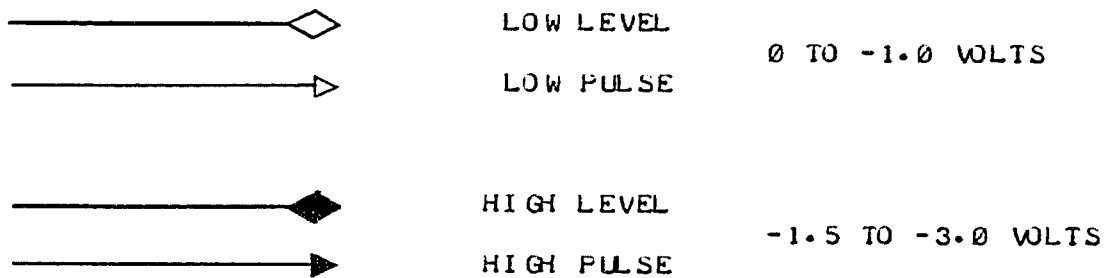
BELOW ARE SHOWN THE DIFFERENT SYMBOLS USED TO REPRESENT DIFFERENT LOGIC LEVELS.

## MOTOROLA MC830P SERIES



THE VOLTAGES ABOVE ARE WITH REFERENCE TO THE NEGATIVE OF THE I.C.'S POWER SUPPLY.

## DEC MODULES



THE DEC VOLTAGES ARE WITH RESPECT TO GROUND.

AT THE REMOTE INTERFACE IT WAS FELT THAT IT MAY BE DESIRABLE TO USE THE INTERFACE IN THE FUTURE WITH BOTH DEC R SERIES AND WITH EQUIPMENT USING INTEGRATED CIRCUITS. THE INTERFACE WAS CONSTRUCTED IN SUCH A WAY THAT IT COULD BE USED WITH BOTH TYPES. THIS CHOICE WAS FORTUNATE IN VIEW OF THE SUBSEQUENT AVAILABILITY OF DEC M SERIES MODULES AND OTHER EQUIPMENT USING I.C.'S. ALSO, SINCE THE REMOTE TERMINAL MAY BE AT A VERY ELECTRICALLY "NOISY" SITE, THE USE OF STANDARD DEC MODULES WAS DEEMED A SAFER DESIGN.

THE PART OF THE COMMUNICATION SYSTEM AT THE PDP-8 END, HOWEVER, HAD ONLY TO BE COMPATIBLE WITH THE STANDARD DEC LOGIC LEVELS, NOMINALLY 0 AND -3 VOLTS. DIRECT LOGIC LEVEL CONVERSION WAS ACHIEVED BY OFFSETTING THE I.C.'S POWER SUPPLY FROM GROUND, AS SHOWN BELOW

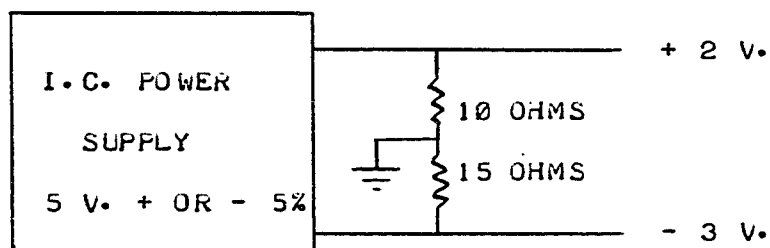


FIG. 5.2-1

THE PREVIOUS CIRCUIT IS SIMPLY A VOLTAGE DIVIDER CONNECTED TO AN UNGROUNDED SUPPLY. THE GROUND CONNECTION IN THE DIVIDER PRODUCES THE ABOVE VOLTAGES WITH RESPECT TO GROUND. NO PROBLEMS HAVE BEEN EXPERIENCED WITH THE USE OF THIS OFFSET POWER SUPPLY.

THE PREVIOUS CIRCUIT YIELDS THE FOLLOWING LOGIC LEVEL RELATIONSHIPS:

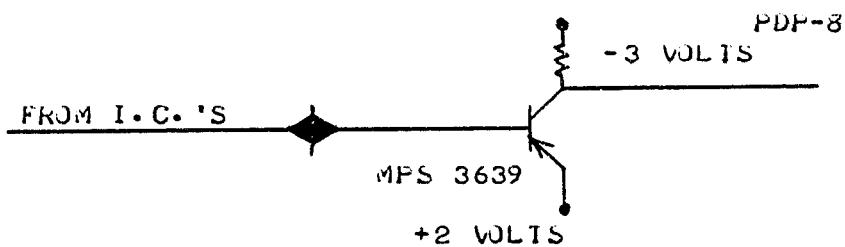


LOGIC LEVEL RELATIONS FIG. 5.2-2

A SIMILAR RELATIONSHIP HOLDS FOR PULSES.

THE PDP-8'S OUTPUT LINES CAN EASILY DRIVE THE INTEGRATED CIRCUITS SO THAT OUTPUTS FROM THE COMPUTER ARE CONNECTED DIRECTLY TO THE INTEGRATED CIRCUITS INPUTS.

INPUTS TO PDP-8'S ARE WIRES CONNECTED TO -3 VOLT MA. CLAMPED LOADS IN THE COMPUTER. AN INPUT OCCURS BY DRIVING A LINE TO GROUND. THE I.C.'S DO NOT POSSESS THE CURRENT DRIVING CAPABILITY TO DO THIS; THEREFORE THE FOLLOWING CIRCUIT WAS USED TO READ INTO THE PDP-8'S AC FROM THE I.C.'S .



INPUT CIRCUIT - FIG. 5.2 -3

BECAUSE OF THE I.C.'S POWER SUPPLY OFFSET, (SEE FIG. 5.2-1), THE TRANSISTOR BASE IS AT EITHER + 2 VOLTS, IN WHICH CASE THE TRANSISTOR DOES NOT CONDUCT, OR AT - 3 VOLTS, IN WHICH CASE THE TRANSISTOR CONDUCTS AND BRINGS THE PDP-8 INPUT LINE TO GROUND.

### 5.3 TIMING CONSIDERATIONS

WHEN A TRANSMISSION OCCURS, THE RECEIVER UNIT INVOLVED GENERATES A LOCAL CLOCK PULSE TO SHIFT-IN THE INCOMING DATA . SINCE THE TRANSMITTER AND RECEIVER CLOCK FREQUENCIES CAN NEVER BE EXACTLY THE SAME, THE EFFECT OF THIS MUST BE STUDIED .

LET US CONSIDER A MESSAGE CONSISTING OF THE 6052 I/O INSTRUCTION AND THE (AC) CONTAINING 101010101010 . THE MESSAGE AS SENT IN THE FORM SHOWN IN FIG. 4.5 -1 AND ITS CORRESPONDING TRANSMITTER CLOCK PULSES GIVEN IN FIG. 5.3 -1 . ALSO GIVEN ARE THE NECESSARY RECEIVER CLOCK PULSES . THE RECEIVER MUST SHIFT IN THE DATA IN THE MIDDLE OF THE "TIME SLOT" ALLOCATED TO A GIVEN BIT IN ORDER TO MINIMIZE THE POSSIBILITY OF READING THE WRONG MESSAGE . FOR A 20 BIT MESSAGE, IT MEANS THAT THE RECEIVER CLOCK MUST READ IN THE FINAL DATA BIT AT THE RIGHT TIME . THIS REQUIRES THAT THE TWO CLOCKS IN ONE CHANNEL MUST BE WITHIN 5% IN FREQUENCY OF ONE ANOTHER .

A MORE STRICT LIMIT MUST BE USED HOWEVER, SINCE THE SYSTEM DOES NOT HAVE A PARITY BIT TO DETECT ERRORS IN TRANSMISSION . A MAXIMUM FREQUENCY DIFFERENCE

OF 3% IS A MORE REALISTIC LIMIT TO ACHIEVE ANY RELIABILITY. THIS IS NOT DIFFICULT TO ACHIEVE WITH FIXED CLOCKS WITH VERY LIMITED FREQUENCY ADJUSTMENT BUT BECOMES MORE DIFFICULT WITH VARIABLE CLOCKS USING RC CIRCUITS .

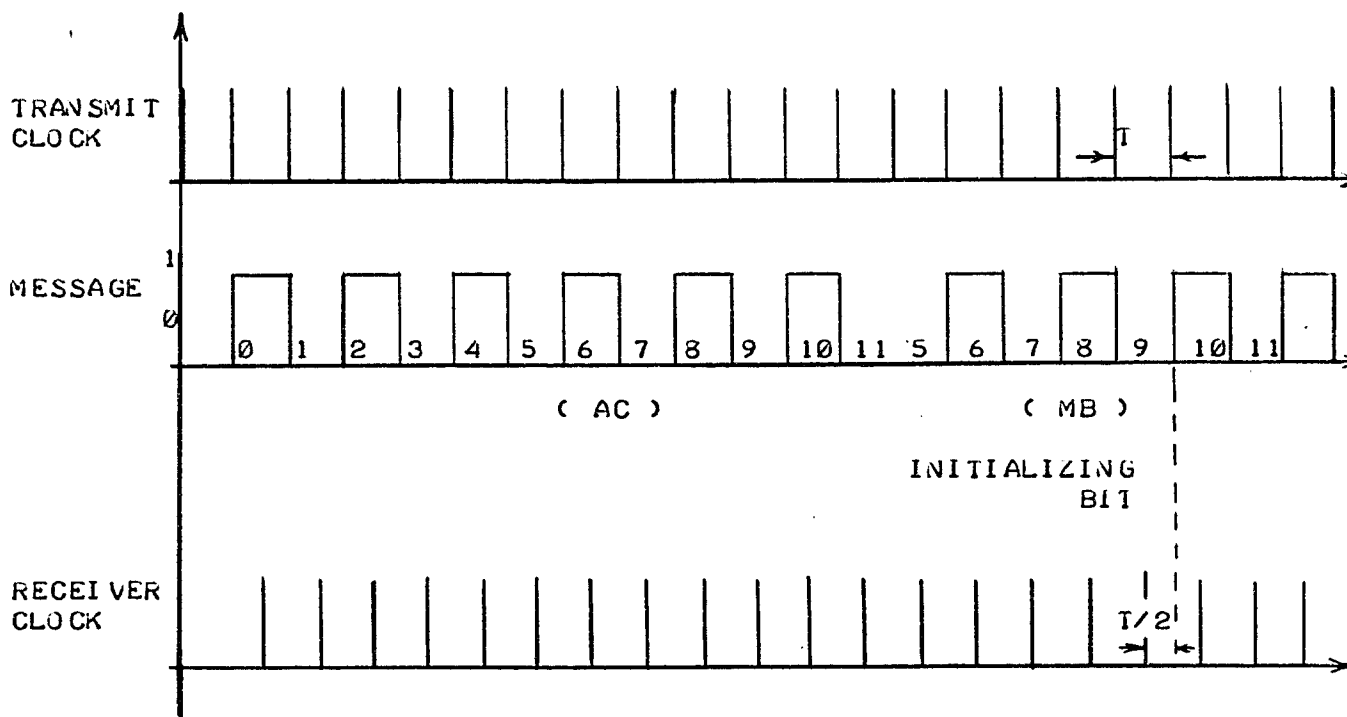


FIG. 5.3 -1 TIMING

IN FIG. 5.3 -1, IT MAY BE NOTICED THAT THE TRANSMITTER CLOCK HAS ONE EXTRA CLOCK PULSE AT THE END OF TRANSMISSION . THE TIME TAKEN FOR THIS EXTRA PULSE SERVES TO CLEARLY SEPARATE MESSAGES WHEN THE COMPUTER IS TRANSMITTING DATA CONTINUOUSLY . THE TRANSMISSION OF DATA FROM THE REMOTE TO THE COMPUTER FOLLOWS SIMILAR TIMING RULES .

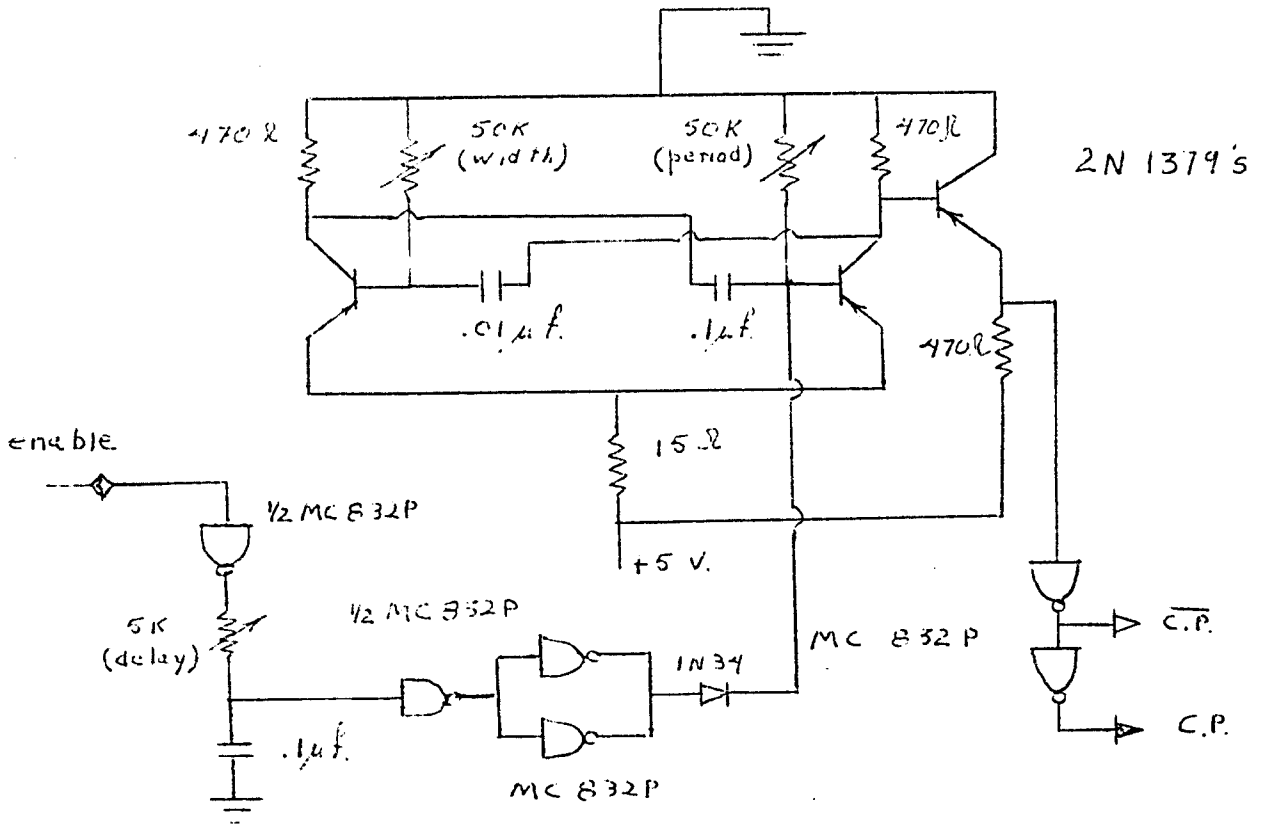


Fig 5.3-2  
Clock

## 6. DESIGN PROCEDURE

### 6.1 GENERAL DESIGN CONSIDERATIONS

ON THE BASIS OF ITS FUNCTIONS, THE SYSTEM MAY BE DIVIDED INTO FOUR SUBSYSTEMS. THE REMOTE INTERFACE IS TO BE AS SIMILAR AS POSSIBLE TO THE PDP-8 INTERFACE. THE VARIOUS FUNCTIONS OF THE SYSTEM AND THE SUBSYSTEMS ARE GIVEN BELOW:

#### PDP-8 TRANSMITTER

1. INPUT. RECEIVES PARALLEL DATA FROM COMPUTER INTERFACE.
2. OUTPUT. TRANSMITS DATA SERIALLY TO THE REMOTE RECEIVER.
3. CONTROL. STATUS IS MONITORED BY THE COMPUTER.

#### REMOTE RECEIVER

1. INPUT. RECEIVES SERIAL DATA FROM THE PDP-8 TRANSMITTER UNIT.
2. OUTPUT. OUTPUTS PARALLEL DATA TO THE REMOTE DEVICES.
3. CONTROL. PRODUCES IOP PULSES TO ACTIVATE THE REMOTE DEVICES.

## REMOTE TRANSMITTER

1. INPUT. RECEIVES PARALLEL DATA FROM REMOTE DEVICES UNDER ITS OWN CONTROL.
2. OUTPUT. TRANSMITS SERIAL DATA TO THE PDP-8 RECEIVER UNIT.
3. CONTROL. IS CONTROLLED BY REMOTE INTERRUPT SIGNALS.

## PDP-8 RECEIVER

1. INPUT. RECEIVES SERIAL DATA FROM REMOTE TRANSMITTER UNIT.
2. OUTPUT. OUTPUTS PARALLEL DATA TO THE COMPUTER.
3. CONTROL. STATUS IS MONITORED BY COMPUTER.

FROM THE BASIC FUNCTIONS WHICH EACH SUBSYSTEM MUST IMPLEMENT IT WAS DECIDED THAT EACH SUBSYSTEM SHOULD HAVE IN IT A SHIFT-REGISTER. IN THE CASE OF A TRANSMITTER UNIT, DATA SHOULD BE ENTERED IN PARALLEL INTO THE SHIFT-REGISTER AND READ OUT SERIALLY FROM THE SHIFT-REGISTER. IN THE CASE OF A RECEIVER UNIT, DATA IS TO BE ENTERED SERIALLY INTO ITS SHIFT-REGISTER AND IT IS TO BE AVAILABLE FOR PARALLEL READ OUT.

THE TRANSMISSION OF DATA TAKES PLACE FROM THE TRANSMITTER UNIT AT ONE END OF THE DATA LINK TO THE RECEIVER UNIT AT THE OTHER END. SOME GENERAL DESIGN DECISIONS HAVE TO BE MADE BEFORE

DESIGNING SPECIFIC SUBSYSTEMS. IT IS REQUIRED THAT EACH SUBSYSTEM HAVE A CLOCK TO PRODUCE SHIFT PULSES FOR THE SHIFT-REGISTER IN THAT SUBSYSTEM. ALL CLOCKS ARE TO BE INDEPENDENT TO ALLOW INDEPENDENT TRANSMISSION OF DATA. IT WAS DECIDED TO DESIGN CLOCKS OF SUFFICIENT STABILITY SO THAT FOR THE DURATION OF A MESSAGE BETWEEN A TRANSMITTER UNIT AND A RECEIVER UNIT THE TWO CLOCKS WOULD REMAIN SUFFICIENTLY SYNCHRONISED. THIS ASPECT IS DISCUSSED IN THE TIMING SECTION. IN ORDER TO ACHIEVE INITIAL SYNCHRONIZATION AT THE BEGINNING OF A MESSAGE, THE TRANSMITTER UNIT SENDS A "START OF MESSAGE" PULSE BEFORE SENDING ACTUAL DATA. THE RECEIVER UNIT USES THE BEGINNING OF A "START OF MESSAGE" PULSE AS AN INDICATION THAT IT SHOULD START SHIFTING IN DATA.

KEEPING IN MIND THE VARIOUS DESIGN DECISIONS MADE IN THIS SECTION WE CAN PROCEED TO DESIGN THE VARIOUS SUBSYSTEMS.

## 6.2 PDP-3 TRANSMITTER UNIT

FROM THE PREVIOUS SECTION WE KNOW THAT THE TRANSMITTER UNIT REQUIRES A SHIFT-REGISTER LONG ENOUGH TO CONTAIN ALL INFORMATION WHICH MAKES UP A COMPLETE MESSAGE TO THE REMOTE INTERFACE. THIS

```

                                /MAIN PROGRAM USING TRANSMIT SUBROUTINE
                                *200
0200  7000  NOP
0201  7000  NOP
0202  7000  NOP
0203  7000  NOP
0204  7000  NOP
0205  7000  NOP
0206  4300  JMS TRANSMIT
0207  6053  DKL
0210  7000  NOP
0211  7000  NOP
0212  7000  NOP
0213  7000  NOP

                                /THIS REPRESENTS THE MAIN BODY OF THE PROGRAM
                                /THIS INSTUCTION IS TO BE CARRIED OUT AT REMOTE
                                /THE MAIN PROGRAM CARRIES ON

                                /TRANSMIT SUBROUTINE
                                *300
0300  0000  TRANSMIT,0000
0301  6101  STF
0302  5301  JMP .-1
0303  6102  LTAC
0304  7200  CLA
0305  1700  TAD I TRANSMIT
0306  6104  LTMB
0307  2300  ISZ TRANSMIT
0310  5700  JMP I TRANSMIT

                                /SKIP ON TRANSMITTER READY FLAG
                                /LOAD TRANSMITTER A.C.
                                /DKL INSTRUCTION LOADED, TRANSMISSION STARTED.
                                /RETURN TO MAIN PROGRAM

```

FIG. 6.2-1  
TRANSMITTER UTILIZATION

Transmit subroutine

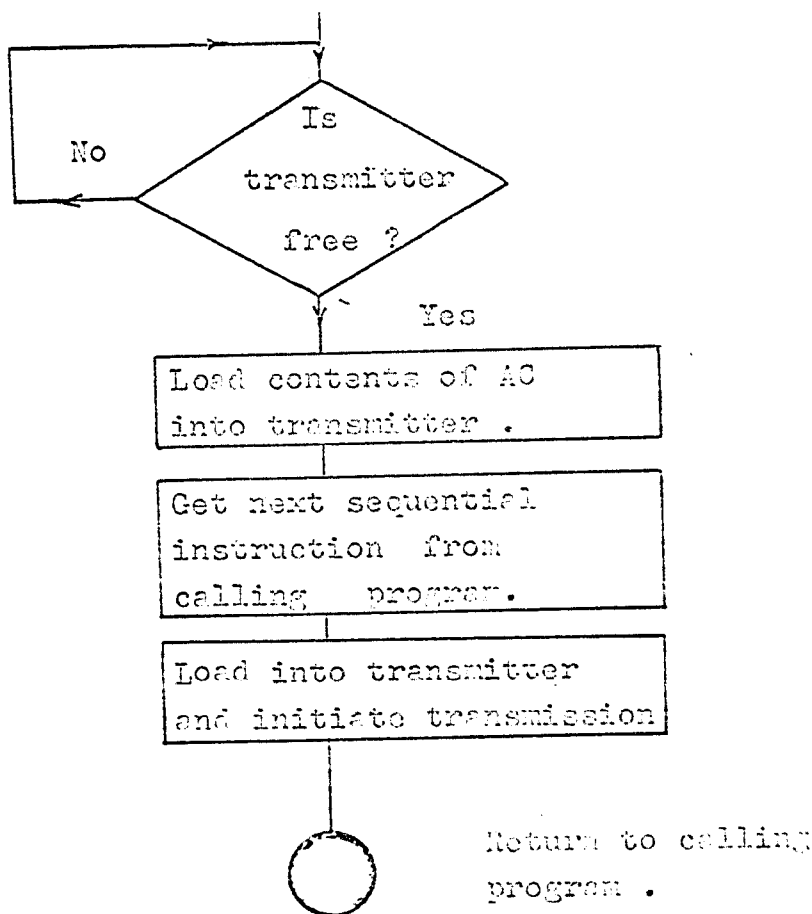


Fig. 6.2-1  
Program flow-graph

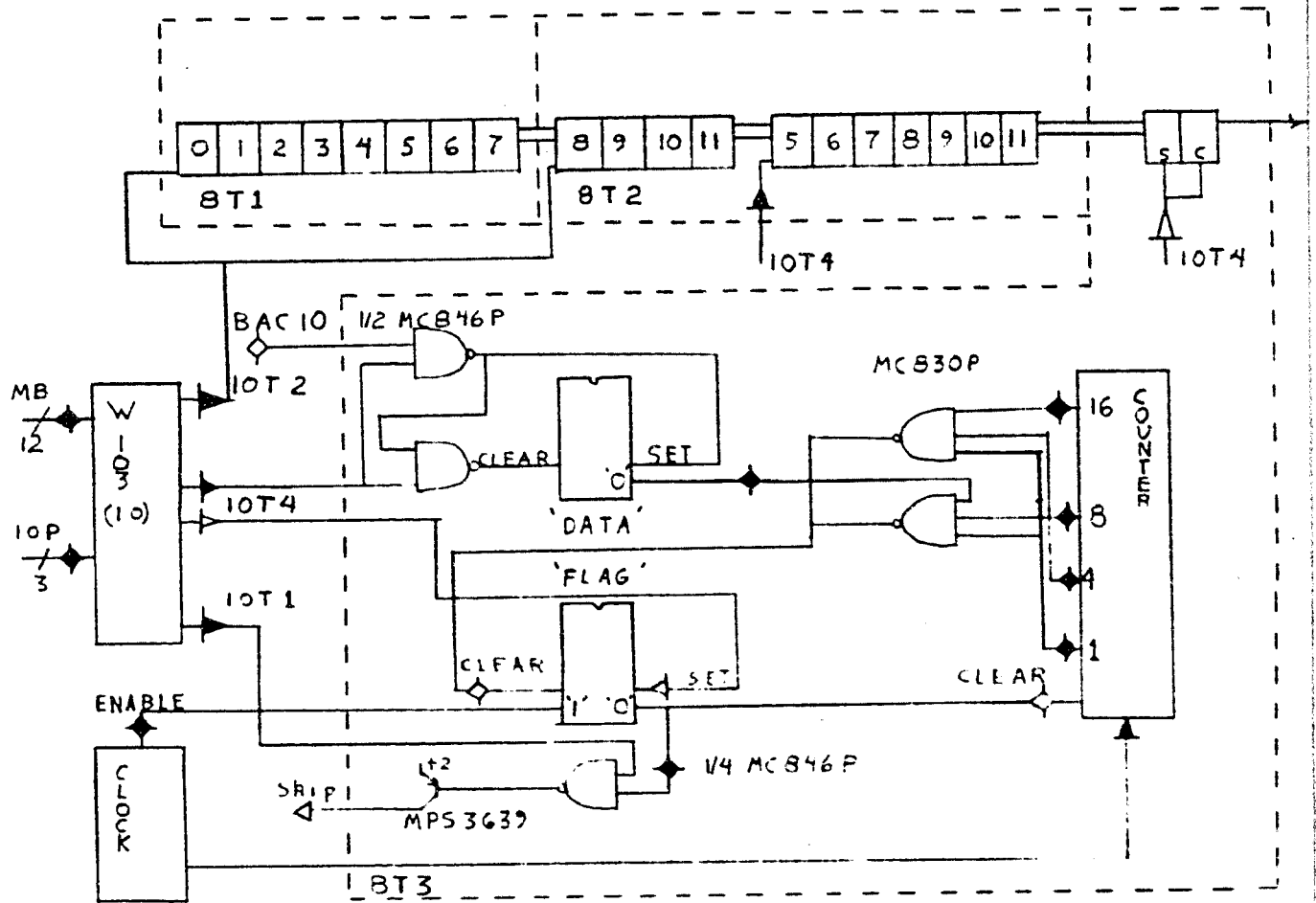


FIG. 6.2-2

PDP-8 TRANSMITTER UNIT

## INFORMATION CONSISTS OF:

CONTENTS OF AC	12 BITS
REMOTE DEVICE CODE	4 BITS
IOP GENERATION	3 BITS
TOTAL	19 DATA BITS

IT IS ALSO NECESSARY TO SEND A "START OF MESSAGE" INDICATION TO THE REMOTE RECEIVER. BY ADDING TWO MORE SHIFT-REGISTER STAGES IN FRONT OF THE DATA BITS AND INITIALIZING THESE PROPERLY WE CAN MAKE THE CONTENTS OF THE FIRST STAGE OF THE SHIFT-REGISTER CHANGE FROM 0 TO 1 AFTER THE FIRST SHIFT PULSE. THE PROPER INITIALHIZATION OF THE SHIFT-REGISTER CONSISTS IN CLEARING THE FIRST STAGE AND SETTING THE SECOND.

THE PDP-8 TRANSMITTER UNIT IS AN I/O UNIT CONNECTED TO THE COMPUTER INTERFACE. A DEVICE SELECTOR, DEC MODULE W103, AS PREVIOUSLY DISCUSSED IN SECTION 2.2, HAS BEEN ASSIGNED TO THIS UNIT. DEVICE CODE 10 HAS BEEN ARBITRARILY ASSIGNED TO THE PDP-8 TRANSMITTER UNIT. THE DEVICE SELECTOR IS SUCH THAT WHEN ITS DEVICE CODE, IN THIS CASE 10, IS PRESENT IN THE MB THEN IT WILL ALLOW THE IOP PULSES TO TRIGGER PULSE GENERATORS IN THE W103 MODULE. THESE GENERATORS THEN PRODUCE IOT PULSES WHICH ARE SPECIFIC TO THIS DEVICE.

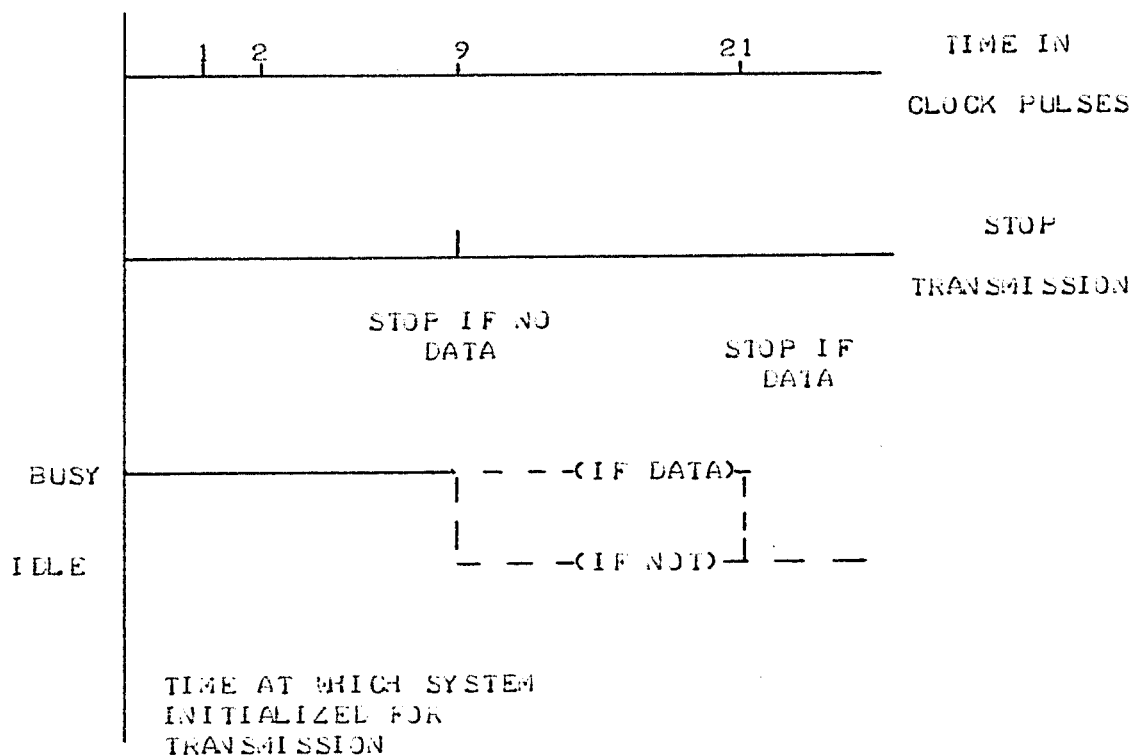
THUS IN THIS CASE THE FOLLOWING INSTRUCTIONS PRODUCE THE FOLLOWING IOT PULSES:

	IOT1	IOT2	IOT4
6101	1	0	0
6102	0	1	0
6103	1	1	0
6104	0	0	1
6105	1	0	1
6106	0	1	1
6107	1	1	1

TIMING BETWEEN IOT PULSES PRODUCED BY ONE INSTRUCTION IS THE SAME AS THAT OF THE IOP PULSES SHOWN IN FIG. 2.2-2. IT WAS DECIDED TO LOAD DATA INTO THE AC SECTION OF THE SHIFT-REGISTER. THUS IN THE PROGRAM OF FIG. 6.2-1, WHEN 6102 IS EXECUTED THE AC CONTAINS THE DATA WE WISH TO TRANSMIT. IT WAS DECIDED TO USE IOT4 TO LOAD THE MB SECTION OF THE SHIFT-REGISTER AND INITIATE A TRANSMISSION. THUS WHEN 6104 IS EXECUTED THE AC IS TO CONTAIN THE INSTRUCTION WE WISH TO TRANSMIT.

IN ORDER TO MAKE MORE EFFICIENT USE OF TIME IT WAS DECIDED TO SEND THE AC SECTION OF THE SHIFT-REGISTER ONLY WHEN IOP2 WAS TO BE EXECUTED AT THE REMOTE. BUT THIS INFORMATION IS IN

AC10 WHEN 6104 IS EXECUTED. THUS USING GATES 2 AND 3 IN FIG. 6.2-2 WE CAN USE IOT4 TO GATE THE CONTENTS OF AC10 IN A "DATA" FLIP-FLOP TO CONTROL THE LENGTH OF A TRANSMISSION CYCLE. A TRANSMISSION CYCLE IS REPRESENTED BELOW:



#### PDP-3 TRANSMITTER TIMING

THE REQUIRED TIMING SIGNALS ARE OBTAINED BY COUNTING THE SHIFT PULSES. A COUNTER, AS INTRODUCED IN THE PREVIOUS CHAPTER IS USED FOR THIS PURPOSE. THIS COUNTER IS ACTIVATED BY THE

TRAILING EDGES OF CLOCK PULSES SINCE ACTIONS ARE TO BE TAKEN AFTER A PULSE HAS OCCURED. A "FLAG" FLIP-FLOP IS NECESSARY FOR THE COMPUTER TO SENCE WETHER THE TRANSMITTER IS BUSY OR NOT. IN FIG. 6.2-2, GATE 5 CLEARS THE FLAG AFTER THE 9TH CLOCK PULSE, IF NO DATA IS TO BE SENT; OTHERWISE GATE 4 DOES IT AFTER THE 21ST CLOCK PULSE. CLEARING THE FLAG STOPS TRANSMISSION SINCE THE CLOCK IS ENABLED BY THE FLAG. WE CAN PRODUCE AN INPUT TO THE COMPUTER'S SKIP INPUT BY GATING IOT 1 AND THE FLAG'S OUTPUT THROUGH GATE 1. IF IOT1 IS PRODUCED AND THE FLAG IS SET, THEN A SKIP WILL RESULT. IF THE FLAG WERE NOT SET THEN NO PULSING OF THE COMPUTER'S SKIP INPUT WOULD FOLLOW. WE CAN THUS ASCERTAIN THE STATE OF THE FLAG. IOT1 IS PRODUCED WHENEVER 6101 IS EXECUTED IN A PROGRAM. THE COUNTER CAN BE PROPERLY CLEARED BY THE FLAG WHEN NO MESSAGE IS BEING SENT.

IN FIG. 6.2-2 THE SUBDIVISIONS OF THE SHIFT-REGISTER ARE DUE TO THE LIMITED NUMBER OF PINS PER CARD ON WHICH THESE SHIFT-REGISTER UNITS WERE BUILT.

### 6.3 REMOTE RECEIVER

AT THE REMOTE RECEIVER THE CIRCUIT MUST RECEIVE INFORMATION AS SENT BY THE PDP-8 TRANSMITTER UNIT AND REPRODUCE AS CLOSELY AS POSSIBLE THE PDP-8 INTERFACE. FROM THE PDP-8 TRANSMITTER WE RECEIVE FIRST A "START OF MESSAGE" BIT, THEN 7 BITS CORRESPONDING TO THE MB AND THEN AN OPTIONAL 12 BITS CORRESPONDING TO THE AC. BECAUSE OF THIS VARIABLE SECTION WE MUST HAVE TWO SEPARATE SHIFT-REGISTERS, ONE FOR THE MB AND ONE FOR THE AC. THE INITIALIZING BIT MUST START THE REMOTE RECEIVER. AFTER THAT THE MB SECTION OF THE MESSAGE MUST BE SHIFTED INTO ITS SHIFT-REGISTER. AT THIS POINT A DECISION IS MADE ON THE BASIS OF THE CONTENTS OF MB10 AS TO WHETHER DATA IS FORTHCOMING. IF MB10 CONTAINS A 0 THEN IOP2 WILL NOT BE PRODUCED AND SO BY THE DISCUSSION OF THE PREVIOUS SECTION NO DATA IS COMING. IF IOP10 IS A 1 HOWEVER, WE MUST SHIFT IN 12 MORE BITS OF DATA. THE CONTENTS OF THE MB MUST REMAIN UNCHANGED DURING THIS HOWEVER. THUS DURING THE RECEPTION OF A MESSAGE WITH DATA, ALTHOUGH 20 CLOCK PULSES ARE REQUIRED TO SHIFT IN THE DATA, ONLY THE FIRST 8 MAY BE APPLIED TO THE MB SECTION. THE END OF THE RECEPTION OF A

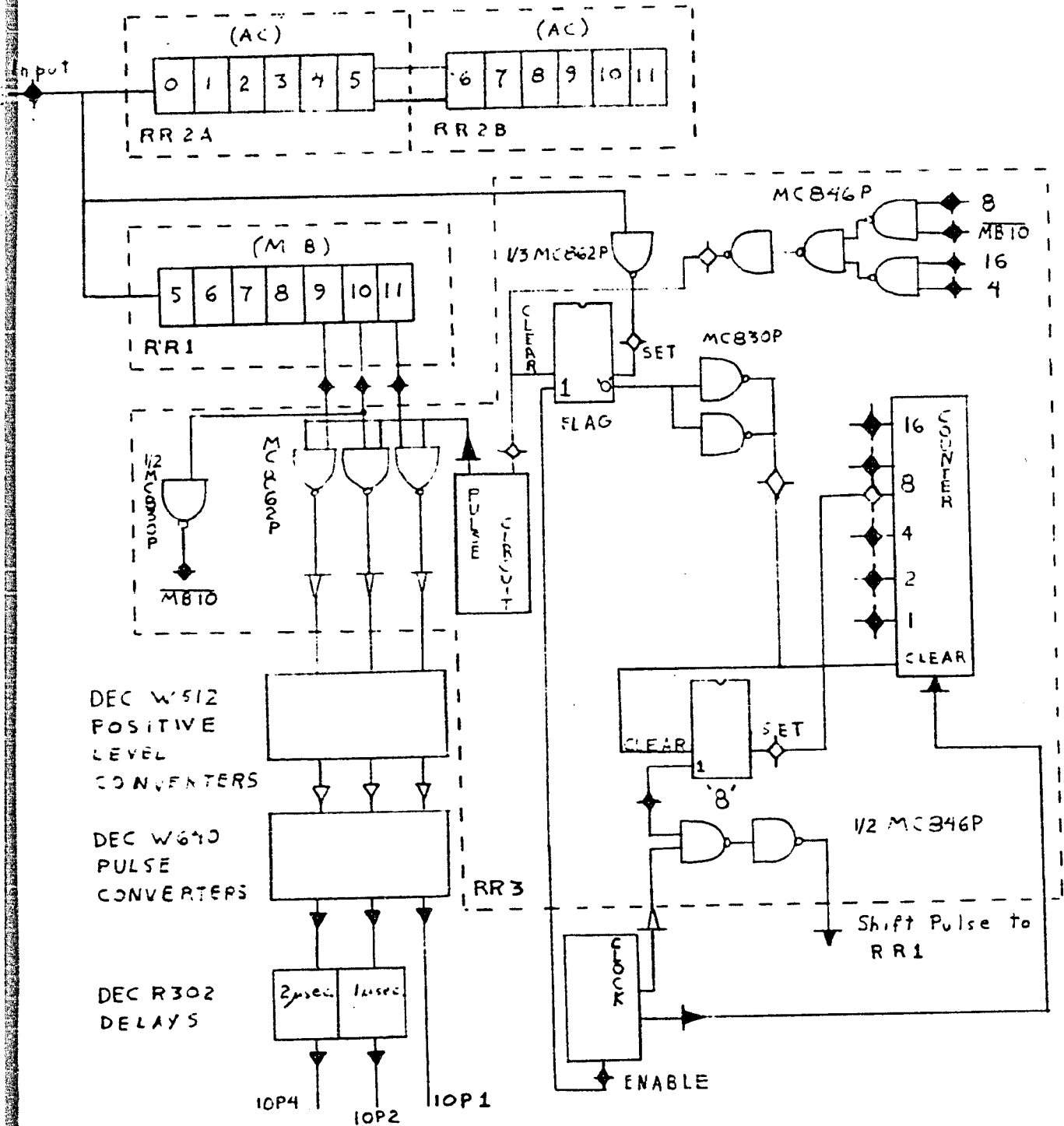
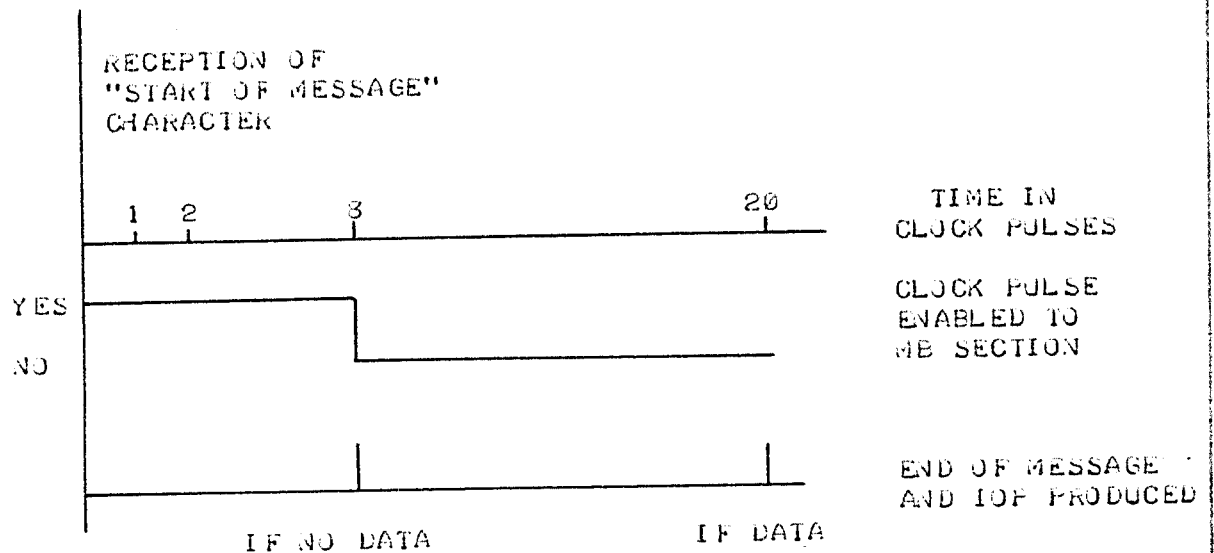


FIG. G.3-1

REMOTE RECEIVER

MESSAGE MUST ALSO RESULT IN THE PRODUCTION OF IOP PULSES. A TIMING CHART IS GIVEN BELOW.



#### REMOTE RECEIVER TIMING

THE RECEPTION OF A START OF MESSAGE PULSE SHOULD ACTIVATE THE RECEIVER. THIS IS DONE BY HAVING THE INPUT SET A FLAG BY MEANS OF GATE 5. THE FLAG IN TURN IS USED TO INITIATE THE CLOCK. THE FIRST 3 CLOCK PULSES SHIFT THE START PULSE THROUGH THE MB SECTION AND LEAVE THE ORIGINAL MB SECTION OF THE PDP-3 TRANSMITTER UNIT IN THIS MB SECTION. AFTER THE 3TH CLOCK PULSE THE 3 FLIP-FLOP IS SET. BY GATING THE SHIFT PULSES TO THE MB SECTION WITH THE STATE OF THE 3 FLIP-FLOP IN GATES 1 AND 2 WE CAN PROTECT THE CONTENTS OF THE MB FROM BEING MODIFIED BY THE REMAINING SHIFT PULSES. TWO POSSIBLE CONDITIONS EXIST TO END

A MESSAGE: 3TH PULSE OVER AND NO DATA , OR 20TH PULSE OVER. THE TWO CONDITIONS ARE "ORED" IN GATE 7 AND USED TO CLEAR THE FLAG BY MEANS OF GATE 6. AT THE SAME TIME THIS CLEAR SIGNAL IS USED TO INITIALIZE A PULSE CIRCUIT WHICH, GATING WITH MB 9, 10 AND 11 IN GATE 11, 12 AND 13 PRODUCE THE REQUIRED IOP PULSES. AFTER CONVERTING THESE PULSES TO DEC STANDARD PULSES BY MEANS OF CONVERTERS ( DEC W512 AND W640 MODULES ) PROPER DELAY CHARACTERISTICS , AS SHOWN IN FIG. 2.2-2, ARE INTRODUCED BY MEANS OF A DEC R302 MODULE. THE CLEARED FLAG IN TURN CLEARS THE 3 FLIP-FLOP AND THE COUNTER BY MEANS OF GATES 3 AND 4.

#### 6.4 REMOTE TRANSMITTER UNIT

THE REMOTE TRANSMITTER UNIT MUST ACT AS AN INPUT INTERFACE FOR THE REMOTE DEVICES. IT IS AT HIS POINT THAT DIFFERENCES BETWEEN THE ORIGINAL PDP-8 INTERFACE AND THE REMOTE INTERFACE MUST BE MADE. WHEREAS FOR INTERRUPT-PRODUCING DEVICES LOCATED AT THE COMPUTER SITE , THEIR STATE CAN BE SENSED DIRECTLY, FOR DEVICES LOCATED AT THE REMOTE SITE THE COMPUTER COULD NOT DO THIS WITHOUT USING A PROHIBITIVELY LARGE AMOUNT OF REAL TIME. AN ALTERNATE SYSTEM OF DECIDING WHICH REMOTE DEVICE IS IN THE STATE TO TRANSMIT DATA TO THE COMPUTER WAS ESTABLISHED. IT WAS DECIDED TO TRANSMIT THE REMOTE DEVICE

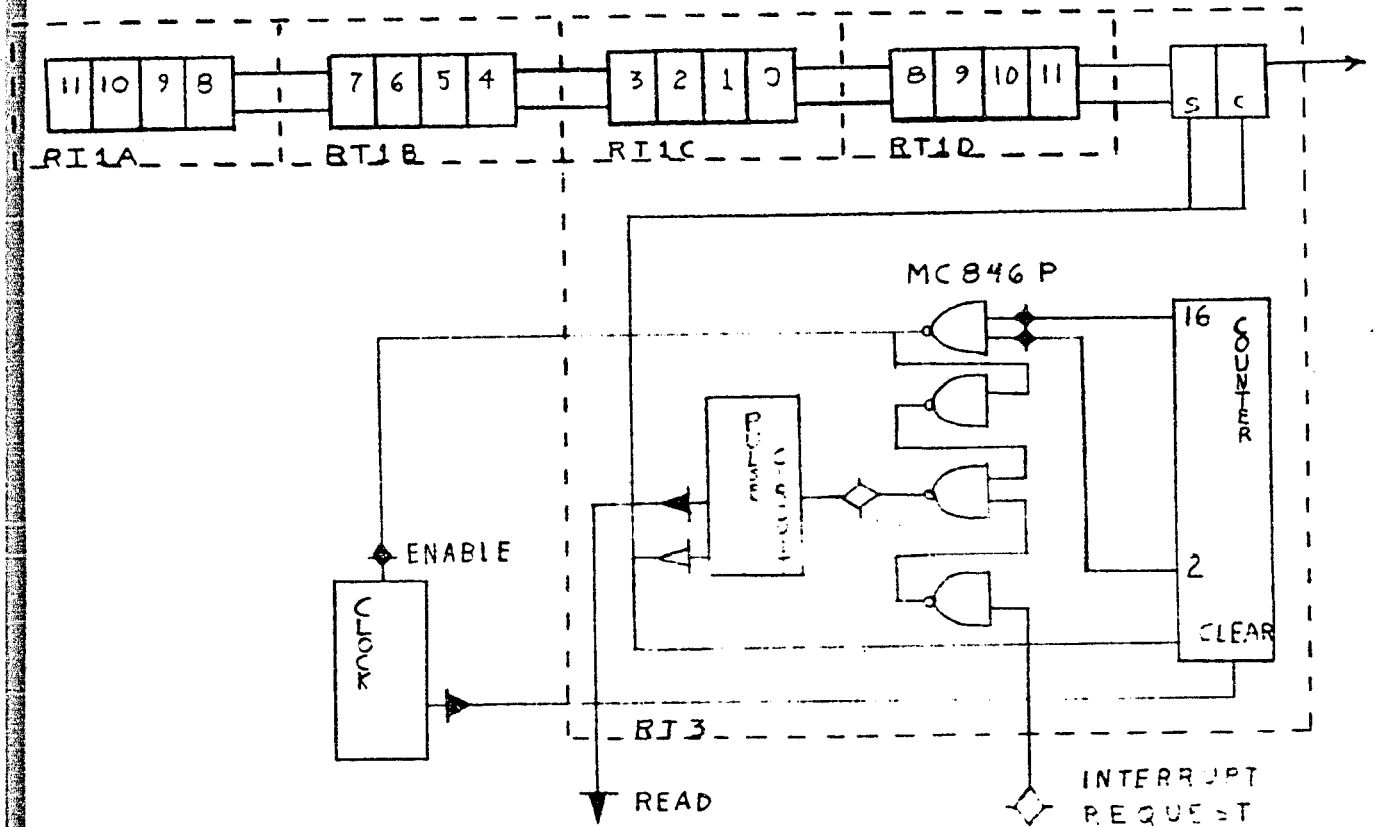


FIG. 6.4-1  
REMOTE TRANSMITTER

CODE ALONG WITH ITS DATA. WITH THIS INCREASE EACH REMOTE DEVICE NOW SEND A TOTAL OF 16 DATA BITS TO THE COMPUTER. REMOTE DEVICES MAY HAVE DATA READY TO BE SENT WHEN THE REMOTE TRANSMITTER IS ALREADY BUSY TRANSMITTING OTHER DATA. THEREFORE A PULSE PRODUCED BY THE REMOTE TRANSMITTER UNIT IS REQUIRED WHEN IT IS FREE AND SERVICE IS REQUIRED BY A REMOTE DEVICE. THUS AN INPUT, CALLED BY ANALOGY TO THE COMPUTER INTERFACE AN "INTERRUPT REQUEST INPUT" MUST BE PROVIDED FOR DEVICES TO REQUEST SERVICE FROM THE TRANSMITTER. AN OUTPUT SIGNAL CALLED A "READ PULSE" IS NECESSARY TO READ THE DEVICE'S DATA AND CODE NUMBER INTO THE TRANSMITTER UNIT AS SOON AS IT IS AVAILABLE. THE SHIFT-REGISTER CONSISTS OF 12 STAGES TO HOLD THE DEVICE DATA, 4 STAGES FOR THE DEVICE CODE, AND 2 LEADING STAGES TO PRODUCE A START OF MESSAGE INDICATION AS DISCUSSED PREVIOUSLY.

THE CIRCUIT DESIGN IS RATHER ELEGANT IN THAT IT USES NO OTHER MEMORY ELEMENTS IN THE CONTROL SECTION THAN THOSE REQUIRED BY THE COUNTER. A COMPLETE TRANSMISSION REQUIRES 18 CLOCK PULSES. AFTER THE 13TH CLOCK PULSE THE OUTPUT OF GATE 1 CHANGES STATE. THIS DISABLES THE CLOCK AND STOPS TRANSMISSION. IF AN INTERRUPT REQUEST SIGNAL NOW OCCURS AT THE INPUT TO GATE 4 IT WILL ENABLE THE PULSE CIRCUIT BY MEANS OF GATE 3. WERE THE CIRCUIT BUSY HOWEVER AND THE COUNTER NOT AT 13, THE INTERRUPT REQUEST SIGNAL COULD NOT PRODUCE A READ PULSE UNTIL THE TRANSMITTER BECAME IDLE.

THE USER UTILIZES THE READ PULSE TO READ THE DEVICE DATA AND THE DEVICE CODE INTO THE SHIFT-REGISTER. INTERNALLY, THIS PULSE INITIALIZES THE LEADING STAGES OF THE SHIFT-REGISTER AND CLEARS THE COUNTER. THUS THE GATE 1 OUTPUT CHANGES AND ENABLES THE CLOCK.

#### 6.5 PDP-8 RECEIVER UNIT

THIS UNIT RECEIVES FROM THE REMOTE TRANSMITTER A START OF MESSAGE BIT AND THEN 16 BITS OF DATA. THE START OF MESSAGE BIT MUST START THE RECEIVER AND THIS IS ACHIEVED BY SETTING A RUN FLIP-FLOP WITH THE INPUT BY MEANS OF GATE 2. THIS FLIP-FLOP IN TURN, INITIATES THE CLOCK WHICH SHIFTS DATA INTO THE SHIFT-REGISTER. AFTER 17 CLOCK PULSES, THE DATA IS FULLY ENTERED AND THE CLOCK MUST BE STOPPED. GATE 1 STOPS THE CLOCK BY TRIGGERING THE RUN FLIP-FLOP WHICH HAS A SIGNAL ON ITS CLEAR INPUT. THE COMPUTER MUST KNOW WHEN THE RECEIVER UNIT HAS DATA TO SUPPLY; DATA IS AVAILABLE TO THE COMPUTER IMMEDIATELY AFTER THE 17TH CLOCK PULSE.

PULSES TO READ THE CONTENTS OF THE SHIFT-REGISTER UNDER PROGRAM CONTROL ARE PRODUCED BY A W103 MODULE AND DEVICE CODE 11 HAS BEEN ALLOCATED TO THIS DEVICE. I0T2 WAS USED TO READ THE REMOTE DEVICE'S DATA INTO THE AC AND I0T4 TO READ THE REMOTE DEVICE CODE INTO THE AC.

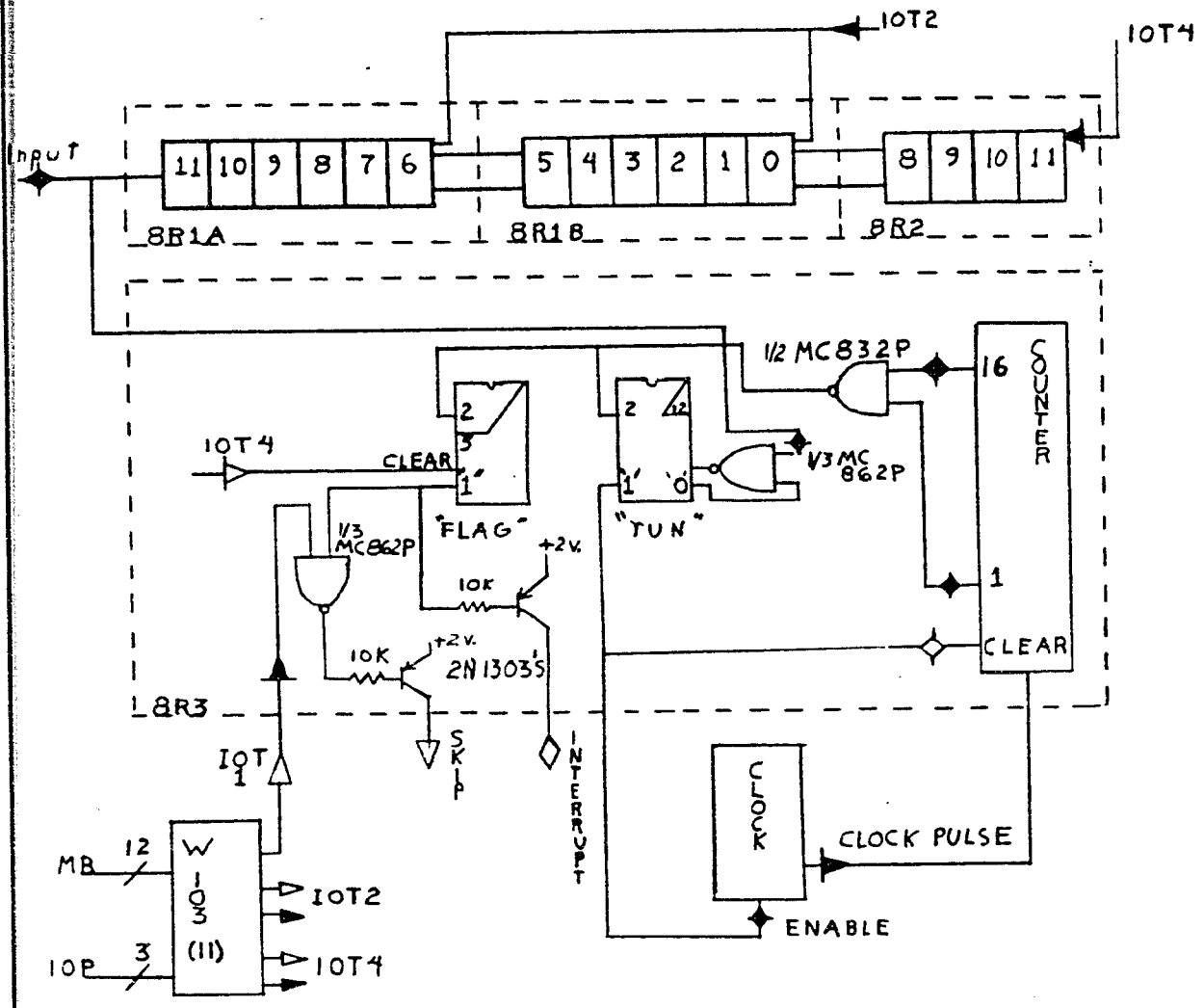


FIG. 6.5-1  
PDP-8- RECEIVER

A FLAG FLIP-FLOP MUST BE SET AFTER THE 17TH CLOCK PULSE TO SIGNAL THE COMPUTER THAT THE RECEIVER UNIT HAS DATA AVAILABLE. THIS FLAG IS SET AFTER THE 17TH CLOCK PULSE BECAUSE THE OUTPUT OF GATE 1 TRIGGERS IT AND AN INPUT IS ALWAYS PRESENT AT THE FLIP-FLOP'S SET TERMINAL. THE FLAG IS CLEARED BY MEANS OF IOT4, IE: WHEN THE COMPUTER HAS READ THE DATA. WHEN THE FLAG IS SET IT PRODUCES A COMPUTER INTERRUPT REQUEST. THE COMPUTER CAN TEST THIS UNIT'S STATUS BY MEANS OF IOT1. THE STATE OF THE FLAG AND IOT1 ARE GATED TOGETHER ONTO THE SKIP INPUT BY MEANS OF GATE 3. THE COMPUTER RECEIVES A PULSE ON THE SKIP INPUT AFTER PRODUCING IOT1 ONLY IF THE FLAG IS SET.

IN SUMMARY THIS SUBSYSTEM RECEIVES SERIAL DATA AND MAKES IT AVAILABLE IN PARALLEL FORM FOR THE COMPUTER. WHEN THE DATA IS AVAILABLE, IT PRODUCES AN INTERRUPT SIGNAL WHICH, BY APPROPRIATE PROGRAMMING LEADS TO UTILIZATION OF THE DATA PRODUCED BY THE REMOTE DEVICE.

## 7. CONCLUSION

THE DESIGN AND CONSTRUCTION OF THE VARIOUS SHIFT REGISTERS WITH THEIR ASSOCIATED READ-IN OR READ-OUT CIRCUITS WAS QUITE STRAIGHTFORWARD. NO PROBLEMS WERE EXPERIENCED WITH THEIR OPERATION. PARTICULARLY GRATIFYING WAS THE FACT THAT THE POWER SUPPLY OFFSET USED TO DIRECTLY CONVERT LOGIC LEVELS AT THE PDF-8 TERMINAL FUNCTIONED FLAWLESSLY. NO NOISE PROBLEMS DUE TO THIS OFFSET HAVE BEEN ENCOUNTERED.

PROBLEMS WERE ENCOUNTERED HOWEVER IN THE LOGIC ASSOCIATED WITH THE COMMUNICATION SYSTEM AS WELL AS WITH THE CLOCKS. THESE WERE MAINLY DUE TO WIRING ERRORS, FREQUENCY INSTABILITY AND PULSE TO PULSE JITTER. THE FINAL CLOCK CIRCUIT DOES OPERATE PROPERLY AT RATES IN THE RANGE FROM 1KHZ TO 2KHZ.

VARIOUS OTHER INTERESTING PROBLEMS OCCURRED. AS AN EXAMPLE, IN THE FIRST TESTS OF THE SYSTEM THE COMPUTER WOULD SOMETIMES GO COMPLETELY OUT OF CONTROL AND DESTROY ALL OPERATING SYSTEMS IN ITS MEMORY. THE CAUSE WAS SIMPLE: AN INT<sup>E</sup>RMITTENT SHORT CIRCUIT TO GROUND ON A WIRE CONNECTED TO THE COMPUTER'S SKIP INPUT. FINDING THE CAUSE WAS NO EASY TASK SINCE THE COMPUTER WAS CONTINUALLY BEING PUT OUT OF ACTION.

TRANSMISSION WAS ATTEMPTED USING TRANSFORMER COUPLING TO THE LINES IN ORDER TO AVOID GROUND LOOPS. THE TRANSFORMERS, HOWEVER, INTRODUCED A CERTAIN AMOUNT OF DISTORTION AND RINGING AT CERTAIN FREQUENCIES. THE FINAL SYSTEM USES D.C. COUPLING TO THE LINES. NO GROUND LOOP PROBLEMS HAVE BEEN EXPERIENCED.

THE BELL TELEPHONE COMPANY OF CANADA WOULD NOT ALLOW US TO USE THEIR LINES UNLESS WE USED AN A.C. CARRIER SYSTEM SUCH AS THE ONE THEY NORMALLY RENT FOR DATA TRANSMISSION. THAT BEING AGAINST THE SPIRIT OF THIS THESIS, PRIVATE LINES, ELECTRICALLY SIMILAR TO STANDARD AUTONOMOUS TELEPHONE LINES WERE SET UP. THE DISTANCE BETWEEN THE COMPUTER AND THE REMOTE TERMINAL IS ABOUT 125 METERS.

THOUGH INITIALLY DESIGNED TO FUNCTION AT A CLOCK RATE OF 1KHZ, THE SYSTEM WAS FOUND TO FUNCTION JUST AS WELL AT 2KHZ, THE MAXIMUM FREQUENCY OF THE CLOCKS USED.

IT WAS FELT THAT THE SYSTEM COULD OPERATE AT A CLOCK RATE OF 10KHZ OVER THE EXISTING LINES WITH NEW CLOCKS DESIGNED SPECIFICALLY FOR THAT FREQUENCY. WITH THE USE OF PROPERLY MATCHED COAXIAL CABLES AND FAST CLOCKS, THE SYSTEM COULD BE EXPECTED TO FUNCTION AT MUCH HIGHER SPEEDS.

APPENDIX

A.1 FDP-8 INSTRUCTIONS

MNEMONIC	OP. CODE	OPERATION
AND Y	0	LOGICAL AND Y WITH CONTENTS OF AC. LEAVE RESULT IN AC.
TAD Y	1	TWO'S COMPLEMENT ADD THE CONTENTS OF Y WITH THOSE OF AC. RESULT IN AC.
ISZ Y	2	INCREMENT LOCATION Y. SKIP NEXT INSTRUCTION IF RESULT 0.
DCA Y	3	DEPOSIT CONTENTS OF AC AT Y AND CLEAR AC.
JMS Y	4	CONTENTS OF PC DEPOSITED AT Y NEXT INSTRUCTION TAKEN FROM Y PLUS 1.
JMP Y	5	NEXT INSTRUCTION TAKEN FROM LOCATION Y.

OPERATION CODE 6 IS USED FOR INPUT - OUTPUT INSTRUCTIONS  
AND OPERATION CODE 7 FOR OTHER INSTRUCTIONS SUCH AS:

HLT	7402	HALT
CLA	7200	CLEAR AC.
CMA	7040	COMPLEMENT AC.
IAC	7001	INCREMENT AC.

A.2 SYSTEM PICTURES

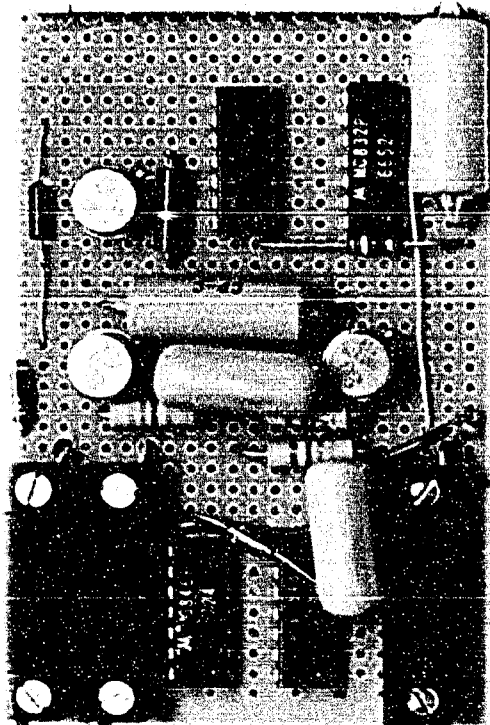


FIG. A. 2-1  
VARIABLE CLOCK  
1 TO 2 KHZ

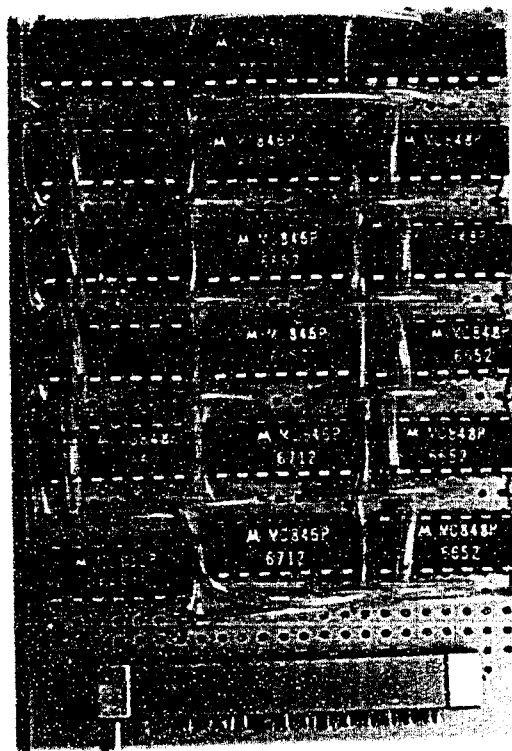


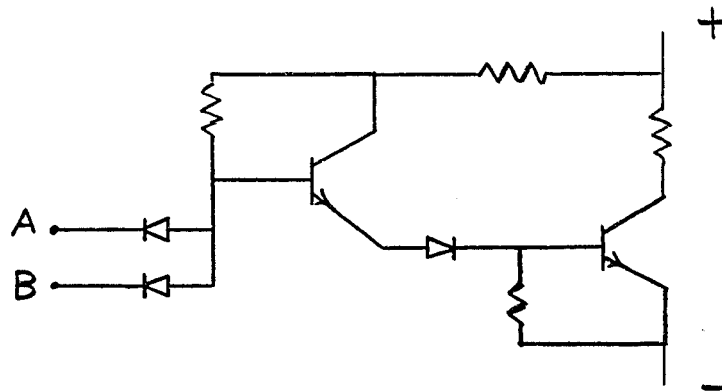
FIG. A. 2-2  
11 BIT SHIFT REGISTER



Fig. A. 2-3 GENERAL VIEW OF PDP-8 DATA LINK INTERFACE

### A.3 INTEGRATED CIRCUIT MODULES

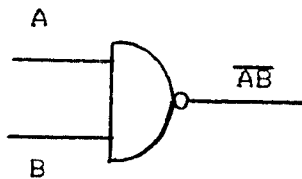
THE MDTL I.C. 'S USED WERE EITHER POSITIVE LEVEL NAND GATES OR FLIP-FLOPS. THE CONFIGURATION FOR ONE 2-INPUT NAND GATE IS GIVEN BELOW . 1



1/4 MC 846F FIG. A.3-1

IN THE ABOVE CIRCUIT, IF BOTH A AND B ARE CONNECTED TO A POSITIVE LOGIC VOLTAGE OR LEFT UNCONNECTED, THEN THE TRANSISTORS CONDUCT AND THE OUTPUT VOLTAGE IS NEAR THE NEGATIVE OF THE I.C. SUPPLY. IF EITHER INPUT IS CONNECTED TO THE NEGATIVE OF THE I.C. SUPPLY, THE TRANSISTORS DO NOT CONDUCT AND THE OUTPUT IS AT A HIGH VOLTAGE. INPUT AND OUTPUT CIRCUITRY FOR FLIP-FLOPS ARE SIMILAR TO THE ABOVE.

THE CIRCUIT OF FIG. A.3-1 IS REPRESENTED IN FIG.A.3-2.



NAND GATE FIG.A.3-2

THE DIFFERENT NAND GATE MODULES USED ARE GIVEN BELOW.

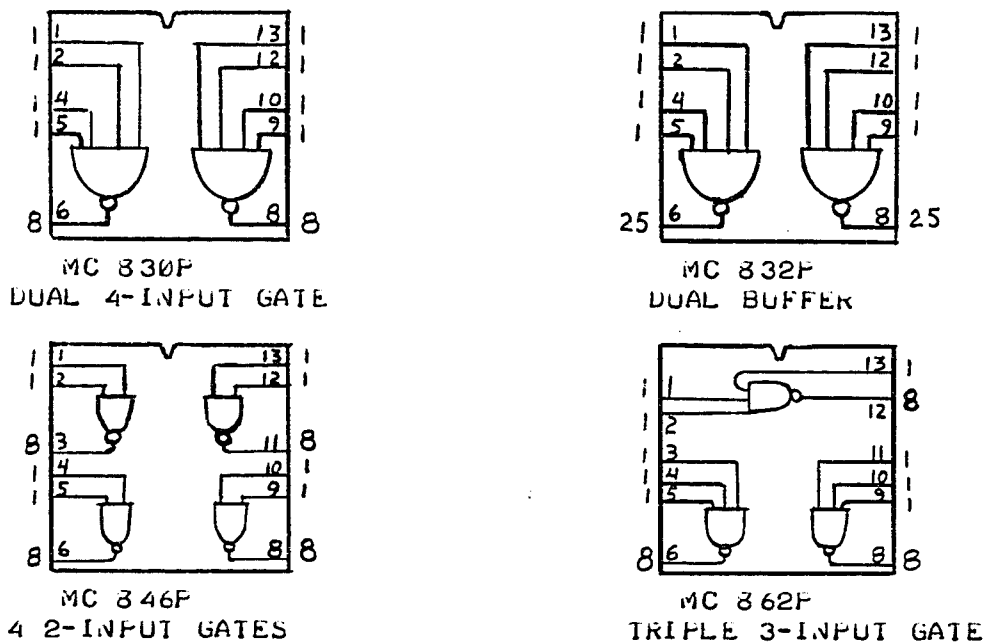


FIG. A.3-3

- NOTES: 1. POWER SUPPLY 5V. +/- 5%. POSITIVE TO PIN 14, NEG. TO 7.  
 2. NUMBER AT END OF TERMINALS INDICATES LOADING UNITS.  
 3. UNIT LOAD: -1.4 MA.

THE FLIP-FLOP MODULE USED IS SHOWN BELOW.

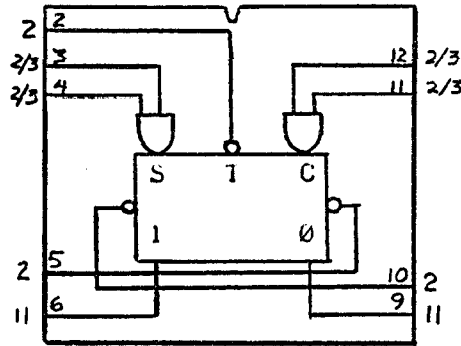


FIG. A-3-4  
MC 848P CLOCKED FLIP-FLOP

- NOTES: 1. PINS 3, 4, 11 & 12 ARE TRIGGERED INPUTS.  
2. DIRECT CLEAR INPUT ON PIN 5 AND DIRECT SET ON PIN 10 HAVE PRECEDENCE OVER TRIGGERED INPUTS.

USING THE FOLLOWING NOTATION

$$X(I) = \begin{cases} 1 & \text{WHEN PIN I IS HIGH} \\ 0 & \text{WHEN PIN I IS LOW} \end{cases}$$

AND

$$1 = \begin{cases} 1 & \text{WHEN PIN 2 GOES FROM HIGH TO LOW} \\ 0 & \text{OTHERWISE} \end{cases}$$

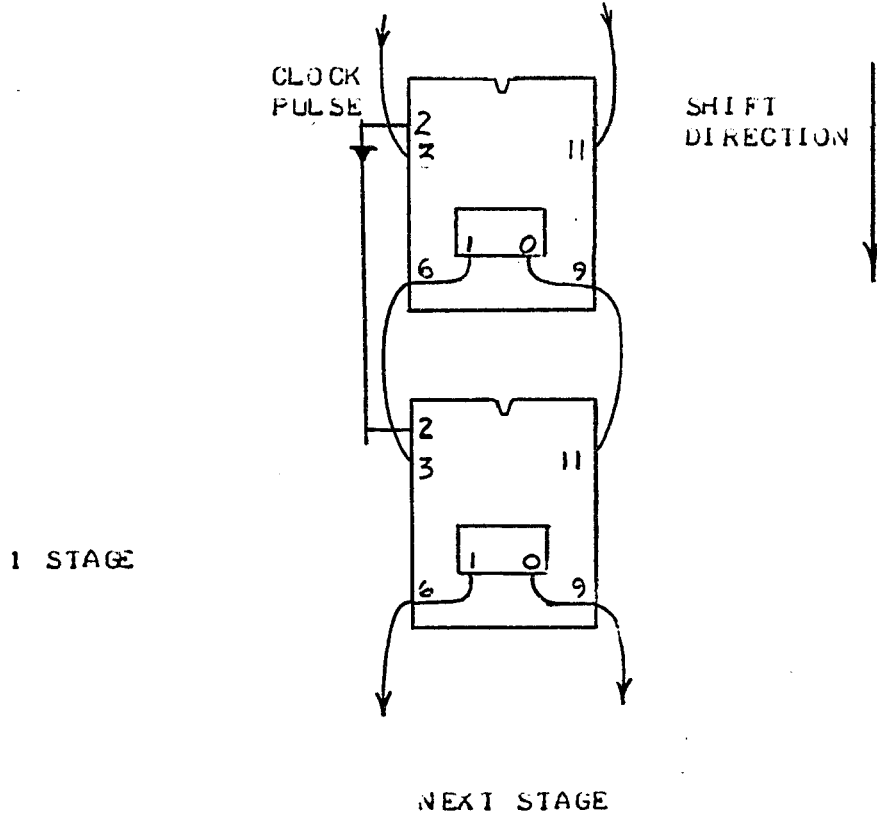
THE SET (S) AND CLEAR (C) FUNCTIONS ARE:

$$S = X(10) + X(3) * X(4) * 1$$

$$C = X(5) + X(11) * X(12) * 1$$

FROM THE ABOVE WE SEE THAT A LOW VOLTAGE ON PIN 10 SETS THE FLIP-FLOP AND A LOW VOLTAGE ON PIN 5 CLEARS THE FLIP-FLOP. THE ABOVE ARE SAID TO BE ASYNCHRONOUS INPUTS SINCE THEY FUNCTION INDEPENDENTLY OF THE TRIGGER.

• 4 LOGIC CIRCUIT ELEMENTS



SHIFT REGISTER FIG. A-4-1

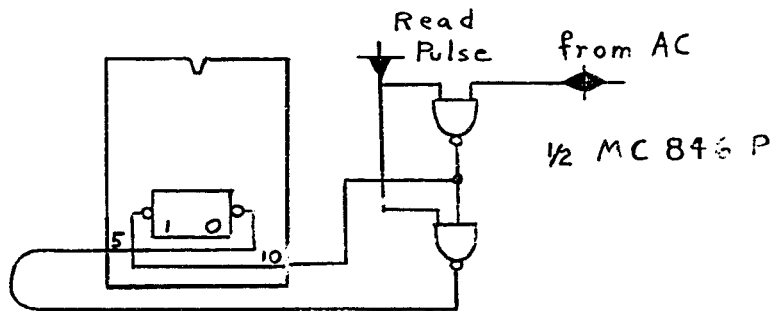


FIG. A-4-2  
READ-IN CIRCUIT FROM PDF-8 TO  
SHIFT-REGISTER (1 BIT)

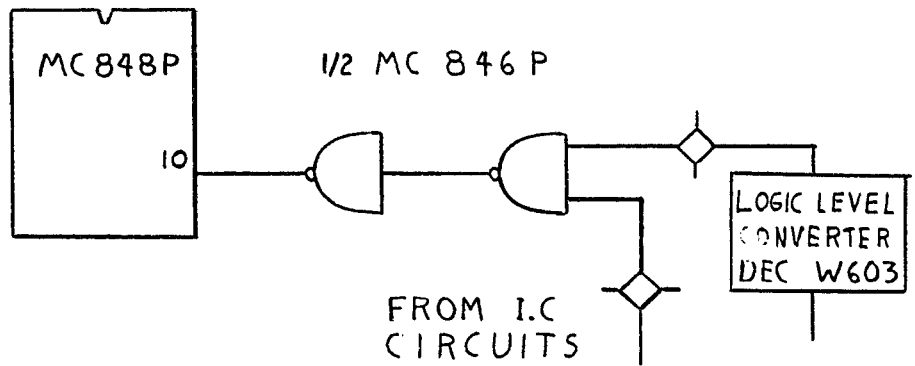


FIG. A.4-3  
READ-OUT CIRCUIT FROM SHIFT-REGISTER  
TO PDF -8 (AC)

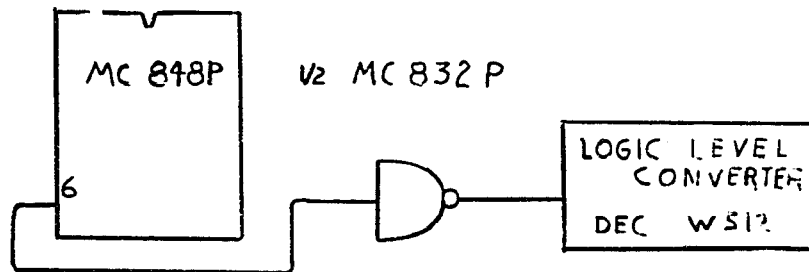


FIG. A.4-4  
INPUT CIRCUIT FROM REMOTE  
INTERFACE TO SHIFI-REGISTER

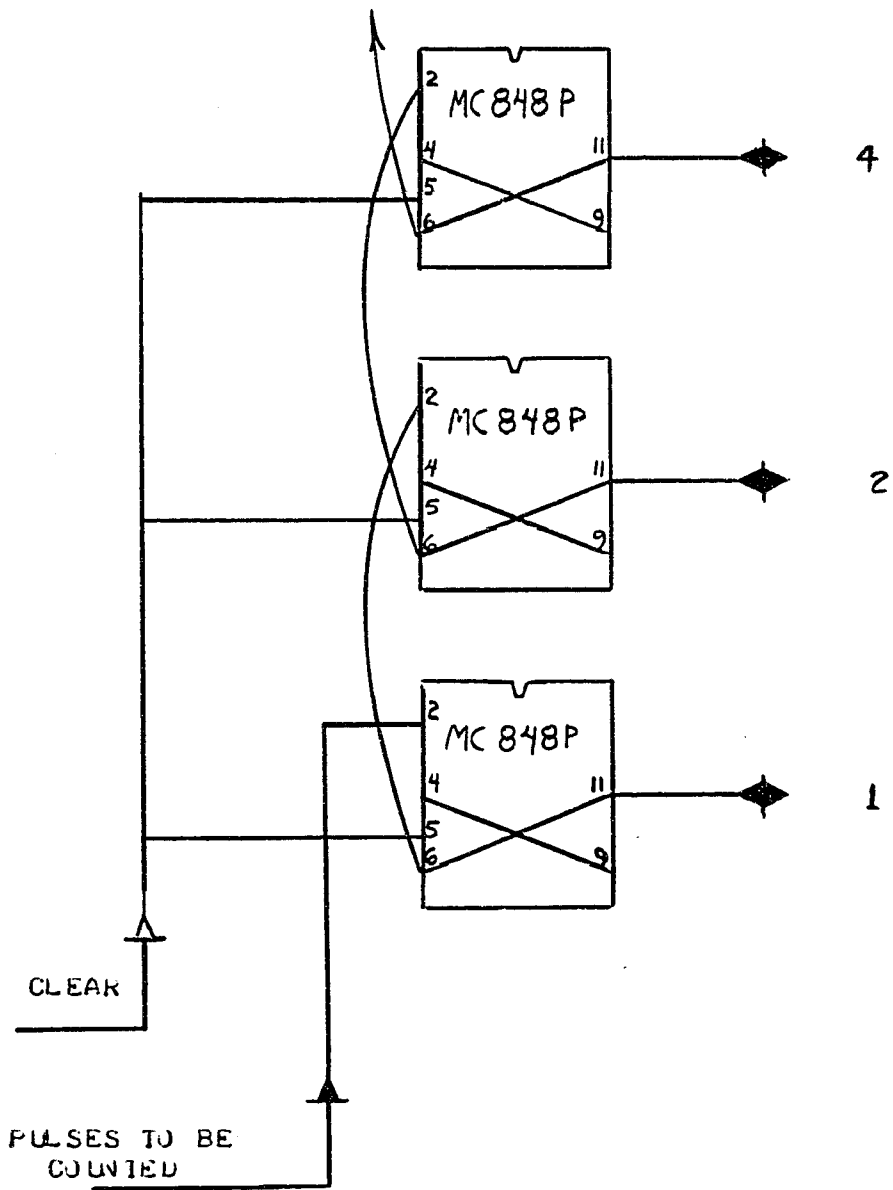


FIG. A. 4-5  
BINARY UP-COUNTER

NOTE: SHIFT-REGISTER CONNECTIONS NOT SHOWN IN  
FIG. A. 4-2 TO FIG. A. 4-5 INCLUSIVELY.

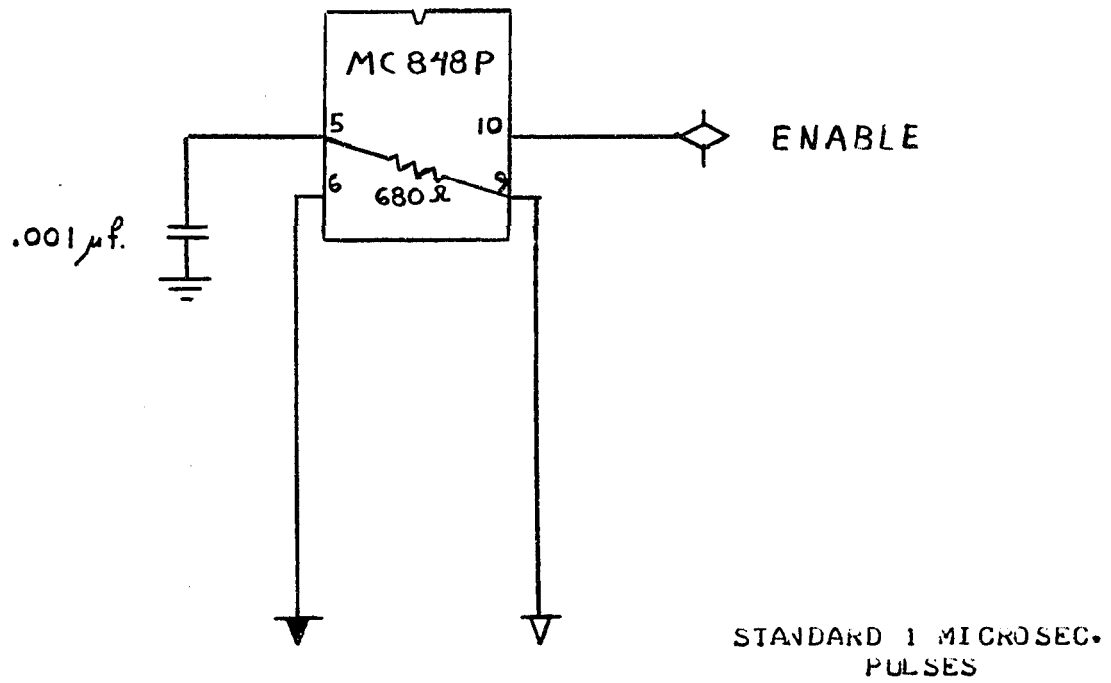


FIG. A.4-6  
PULSE CIRCUIT

## A.5 FURTHER SYMBOLOLOGY

THE SHIFT REGISTERS USED ARE ALL MADE UP OF STAGES INTERCONNECTED AS SHOWN IN FIG. .4-1 AND HAVING ASSOCIATED WITH EACH STAGE A CIRCUIT TO READ INTO OR FROM THE SHIFT REGISTER .

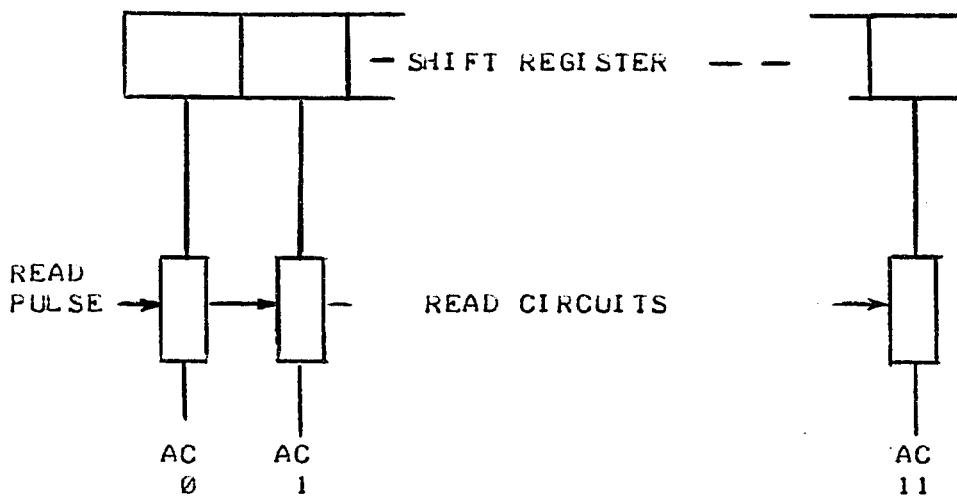
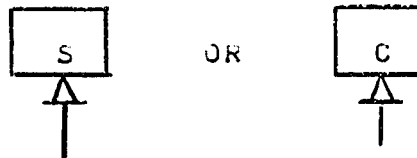


FIG. A.5 -1

THE ABOVE SHOWS A SHIFT REGISTER WITH READ GATES WHICH USE A COMMON READ PULSE . EACH INDIVIDUAL FLIP-FLOP IN THE SHIFT REGISTER HAS ASYNCHRONOUS SET AND CLEAR INPUTS .

CONNECTIONS TO ONE OF THESE INPUTS ON A FLIP-FLOP MAY BE PRESENTED BY



WHERE S STANDS FOR SET AND C STANDS FOR CLEAR .

IT IS POSSIBLE TO FURTHER SIMPLIFY THE PREVIOUS REPRESENTATION OF A SHIFT REGISTER TO YIELD FIG. A.5 -2 .

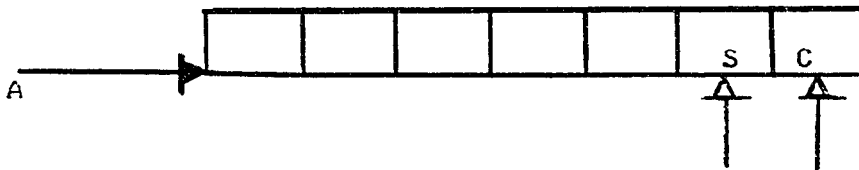


FIG. A.5 -2

THE ABOVE IS A 9 BIT SHIFT REGISTER . SHIFT DIRECTION IS FROM LEFT TO RIGHT . PULSE A REPRESENTS THE READ PULSE COMMON TO ALL STAGES OF THE SHIFT REGISTER . PULSE B IS A SET SIGNAL FOR THE SECOND STAGE FROM THE RIGHT AND PULSE C IS A CLEAR PULSE TO THE FINAL STAGE .

SYMBOLICALLY, A COUNTER AS SHOWN IN FIG. A.4 -5 MAY BE REPRESENTED BY THE FIG. A.5 -3 .

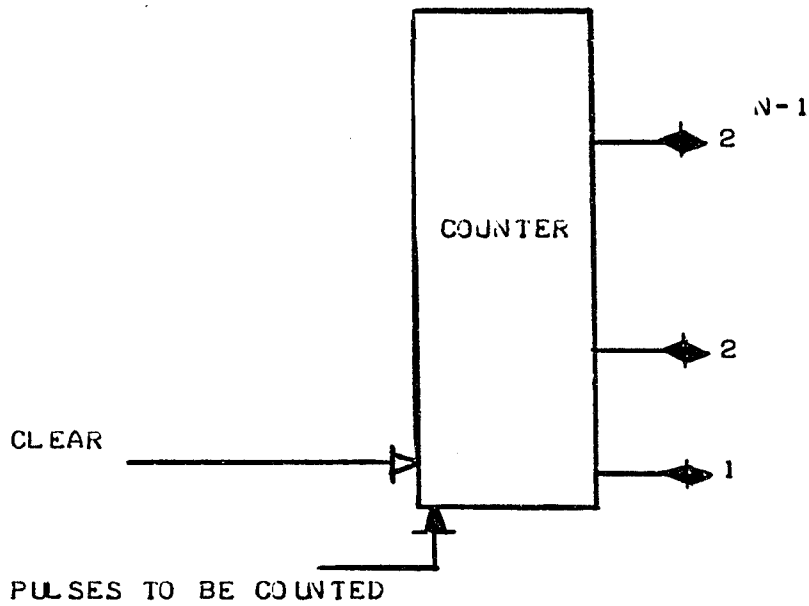


FIG. A.5 -3

THE PULSE CIRCUIT OF FIG. A.4 -6 MAY BE REPRESENTED BY FIG. .5 -4 .

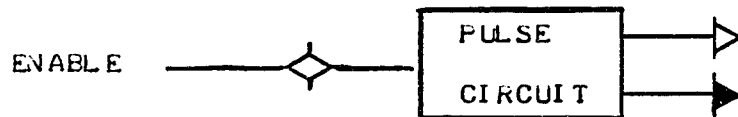


FIG. A.5 -4

THE VARIOUS CIRCUIT REPRESENTATIONS GIVEN ABOVE ARE USED IN THE FINAL DESIGN PRESENTATION FOR BOTH GRAPHICAL AND EXPLANATORY EASE .

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