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Modeling and Analysis of Packet Switch Architectures for Broadband ISDN.

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Abstract

In this thesis we analyze broadband switching architectures based on the Asynchronous Transfer Mode (ATM). Many architectures have been proposed in the literature for high-speed packet switches. We first review some of the these switch architectures and their performance. The high-performance switch architectures, in general, require that the buffers be placed at the output ports. These output buffered switches tend to have large hardware complexity or require high speedup in their operation. Our focus is on high-performance switch architectures with low speedup output buffers or a shared buffer.

An $N \times d$ ATM switch with finite output buffers is modeled as a discrete-time queue. The case $d = 1$ represents an ATM multiplexer with N input sources and a finite capacity buffer. Loading at the input as well as at the output is considered to be imbalanced, which greatly affects the switch performance especially the hot spot traffic pattern. We also consider the switch with reduced speedup. In this case, the number of cells going to an output buffer in one time slot is limited to $L << N$. This greatly simplifies the implementation of the switch.

The arrivals to an input port of the switch, besides being bursty, are correlated in the sense that a burst arriving to an output port brings with it several cells belonging to the same virtual connection. As a worst case, we assume that consecutive cells in a burst are heading to the same output port. This greatly affects the dimensioning of the switch buffer. The input process to each input port is modeled by an Interrupted Bernoulli Process (IBP).

We have developed an aggregation technique which allows the reduction of the state space that describes the arrival processes to the switch. This makes handling the output buffer driven by the induced process more manageable.

Traffic priorities in ATM networks is an important issue because such networks will support applications with diverse traffic characteristics. In the light of this, we consider traffic priorities in an output-buffered switch and in a completely shared-buffer switch.

The transient analysis of the output buffer is also studied by considering the mean time until buffer overflow. The switch architecture that has the maximum mean-time-to-blocking is favorable. The busy period of the output buffer is also characterized. In routing the whole burst to an output buffer, the output process becomes more bursty than the input process.

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List of Symbols

$N \times d$	the size of a switch
L	the speedup constraint of a switch
M	the buffer size of an output line
W^*	the aggregated transition matrix of the input sources
β	the transition probability from an idle state to an active state in the arrival process
α	the transition probability from an active state to an idle state in the arrival process
C^2	the squared coefficient of variation of the interarrival time of cells
ρ	the mean traffic rate at an input line of the switch , equivalently, the steady state probability that any slot contains a packet
r_b	the burstiness index of the arrival process
d_{ij}	the probability that a burst arriving at input i is destined to output queue j
Q_i	the transition matrix of the i^{th} arrival process
k	the number of cells arriving in a time slot destined to an output buffer
n	the number of cells in the output buffer at a given time slot
π^*	the steady state distribution of the queue obtained by the approximation

k_H	the number of high-priority cells at a given time slot
k_L	the number of low-priority cells at a given time slot
$N-\{i\}$	the remaining queues in a shared buffer
c_i	the number of cells that arrive at output queue i in a shared buffer
c_R	the number of cells that arrive at aggregate queue $N-\{i\}$ in a shared buffer
c_N	the number of cells that enter the shared buffer
d_i	the number of cells departing from queue i in a shared buffer
d_R	the number of cells departing from queue $N-\{i\}$ in a shared buffer
$P_{n_R}(l)$	probability that l queues are busy given that n_R cells are in the aggregate queue, $N-\{i\}$
b_i	probability that an arriving cell to the shared buffer is destined to queue i

Acronyms

BP	Bernoulli Process
IBP	Interrupted Bernoulli Process
ATM	Asynchronous Transfer Mode
ISDN	Integrated Service Digital Network
BISDN	Broadband-ISDN
VC	Virtual Circuit
FIFO	First-In-First-Out
HOL	Head Of the Line
VBR	Variable Bit Rate
LAN	Local Area Network
MC	Markov Chain
DCT	Discrete Cosine Transform
HP	High Priority
LP	Low Priority
MMBP	Markov Modulated Bernoulli Process
MPEG	Moving Picture Expert Group

Chapter 1

Introduction

1.1 Motivation

The Integrated Services Digital Network (ISDN) is an end-to-end (user-to-user) digital network which supports a wide range of services, including voice and data services. ISDN is based on data channels of 64 kbit/s each. ISDN is also specialized for a number of services; it only offers narrowband services (smaller than 2Mbits/s), so it is not capable of transmitting television signals (80 Mbits/s). However, even for the narrowband services, it is not really integrated- it uses separate packet switched and circuit switched networks. Only the access to the user (user-network interface) is really integrated.

Broadband ISDN (BISDN) is conceived to include the 64 kbit/s ISDN capabilities but in addition opens the door to applications with bit rate above 2 Mbit/s. In BISDN, channel bit rates from 45 Mbit/s to 622 Mbit/s are possible [3].

The implementation of BISDN also requires a flexible transfer mode on which a wide range of services with different traffic characteristics (burstiness, periodic, random) would depend on. The Asynchronous Transfer Mode (ATM) is considered the future transfer mode of the BISDN.

The BISDN also requires high speed, lightweight protocols that will reside on the edge (user premises) of the transport network. The high speed with which cells would be passing through the networks requires very fast protocols (e.g., flow control, congestion

control) to be implemented end-to-end, outside the network.

The concept of BISDN requires high-speed transmission lines (Gbits/s) and high-performance switches (Gbits/s). Current developments in fiber optics and optical devices has opened the door to fulfilling the transmission requirements. Now, the bottleneck is the switching nodes of the broadband networks.

A switching node of a telecommunication network receives packets from the incoming lines and directs them to an outgoing line based on the address attached to each incoming packet. The input controller of a packet switch extracts the output address and other status fields (e.g., priority) from the packet, assigns a local address to the packet, and routes the packet to its outgoing link. Because of the statistical arrival of the packets, buffering is important in a packet switch. The performance analysis (cell loss probability, mean cell delay) of such switches is essential. The broadband switches require throughput up to hundreds of Mbit/s per incoming line, packet loss probability less than 10^{-9}, and mean packet delay of few microseconds. Several fast packet switching architectures have been proposed. The performance analysis of such switches has been under consideration for sometime.

1.1.1 Definitions

broadband: '... a service or system requiring transmission channels capable of supporting bit rates greater than ISDN primary rate (1.5-2 Mbits/s)' [2].

ATM: 'Asynchronous transfer mode (ATM) is the transfer mode for implementing BISDN'. The term *transfer* comprises both transmission and switching aspects. The term *asynchronous* means that cells are multiplexed in an Asynchronous Time Divison Multiplexing way [2].

Cell: Is a fixed-size packet of 53 bytes which contains an information field and a control field (header, 5 bytes). The header contains a Virtual Connection Identifier, VCI, a Virtual Path Identifier, VPI, priority bit, and other parameters.

Switching technique: is the method of directing the cells from one switch element to another. It may be space switching, time switching, and frequency switching [24].

Virtual channel: 'A concept used to describe unidirectional transport of ATM cells associated by a common unique identifier value.' This identifier is called Virtual Channel Identifier (VCI) and is part of the cell header as mentioned above.

Virtual path: 'A concept used to describe unidirectional transport of cells belonging to virtual channels that are associated by a common unique identifier value.' This identifier is called Virtual Path Identifier (VPI) and is part of the cell header.

Virtual channel link: 'A means of unidirectional transport of ATM cells between a point where a VCI value is assigned and the point where that value is translated or removed.'

Virtual channel connection: 'A concatenation of VC links.'

VC switches: 'Switches that terminate both VC links and necessarily VP links, VPI and VCI translations are also performed.

1.2 Synchronous Transfer Mode Versus Asynchronous Transfer Mode

The CCITT Study Group XVIII names the switching and multiplexing aspects as the "Transfer Mode". The Synchronous Transfer Mode (STM) is based on synchronous time division switching and multiplexing. In STM, the time slots are allocated within a recurring structure (frame) to a service for the duration of a call. An STM channel is identified by the position of its time slots within a synchronous frame (Figure 1.1). Once the time

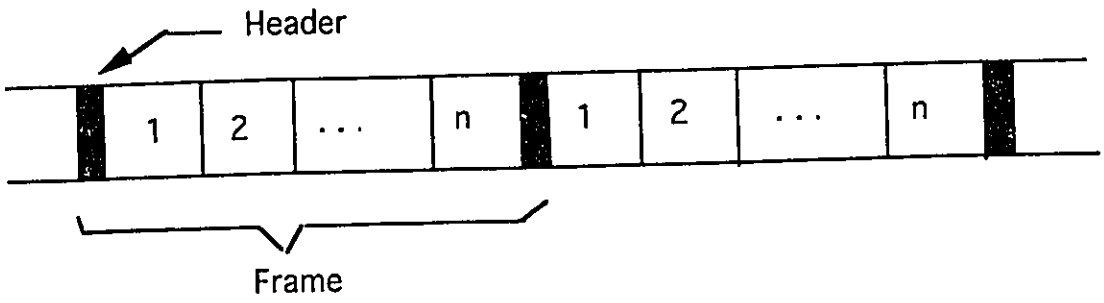

Figure 1.1: The structure of STM

slots are assigned for a given service, they are dedicated for the duration of the call. In order to support a variety of services with different information transfer rates, flexible assignment of a set of time slots to a channel for the switched service is possible. In this case, each channel consists of one or more slots per frame. Within a frame, the number of slots required for a service depends on the peak rate of the service. STM requires coordination of relatively complex mapping functions by both the user and the network sides of an interface [5].

In order to simplify the mapping function, STM advocates dividing the usable capacity into a limited number of fixed STM-based partitions, called containers. Each container would be permanently assigned a set of time slots. This is called multiple rate STM [5]. In order to increase the flexibility, the containers may be further subdivided. But channels could not span containers. The subdivision of containers can have some undesirable consequences. Multiple rate STM also complicates the switching systems. In terms of utilization of switching bandwidth on a per connection basis, it would be more efficient to deploy a separate switching fabric for each channel rate. However, deployment of multiple fabrics is undesirable from the perspective of the network as a whole, complicating management, provisioning and maintenance.

STM is best suited for continuous bit oriented services. Broadband ISDN, however, needs to support different types of traffic including bursty traffic. Peak rate allocation for each service results in very inefficient bandwidth utilization for the bursty services. The Asynchronous Transfer Mode (ATM) technique attempts to eliminate the limitations

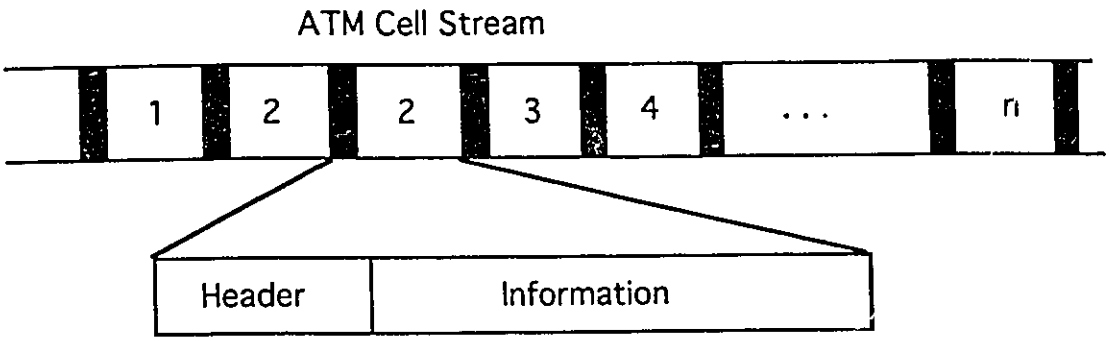

Figure 1.2: A multiplexed ATM cell stream

of STM. Usable capacity can be dynamically assigned on demand. A single fabric could conceivably be used to switch all services. The ATM-based networks may be engineered to take advantage of statistical gain among bursty services, while guaranteeing acceptable performance for continuous-bit-rate services.

In ATM, specific periodic time slots are not assigned to a channel. Usable capacity is segmented into fixed-size units called "slots". Each cell consists of a header containing network routing information, and an information field containing user data (Figure 1.2). These cells can be allocated to various services on demand. The Virtual Channel Identifier (VCI), in the header, is a label that is used like the STM time slot position for channel identification. Like a time slot number, a VCI value is locally significant to an interface and a cell may undergo VCI translation, analogous to the time slot interchange in STM, before it is transported over another interface.

ATM has some similarities to circuit switching and packet switching. It is intended to achieve time transparency for real-time applications as provided by the circuit switching technique while maintaining the bandwidth sharing flexibility of packet switching. Like circuit switching, ATM is basically a connection-oriented technique although it supports both connection-oriented and connectionless services. Like packet switching, an ATM cell is routed based on the routing information provided by the header.

The main problems apparent with the ATM networks are the variable delay associated with the time a cell spent in the network and the expense of interworking with existing networks.

Fiber transmission standards such as Synchronous Optical Network (SONET) can provide the reliable transmission structure to transport the ATM cells.

1.3 ATM switching

1.3.1 Definition of the ATM switching concept

The ATM switching is a modified packet switching. ATM switching is based on packet switching with the following modifications:

1. No error or flow control is performed on the links. These functions will be implemented at the end nodes of the networks.

2. Packets are of fixed size. Variable length packets are not allowed to be switched.

3. Connection oriented. A virtual circuit is assigned for the complete duration of the connection. The memory table (routing tables) is constructed at the connection setup time and will be the same for the complete duration of the connection, thus minimizing the processing time of the arriving packets.

4. Limited functions carried by the packet header. Since there is no distinction between cells other than the VC number, priority bit, and some other parameters, only one type of virtual circuit is supported in the node, thus minimizing the processing time of the arriving packets.

1.3.2 Switch Fundamentals

The basic model of the architecture of a switch (Figure 1.3) consists of switching elements and links, which together switch cells. A link transports cells without any other functions between switching elements. In contrast, a switching element performs routing and buffering or selecting of cells supplied by one or more incoming links. The collection of links (logical links or physical links) in a switch system is called the interconnection

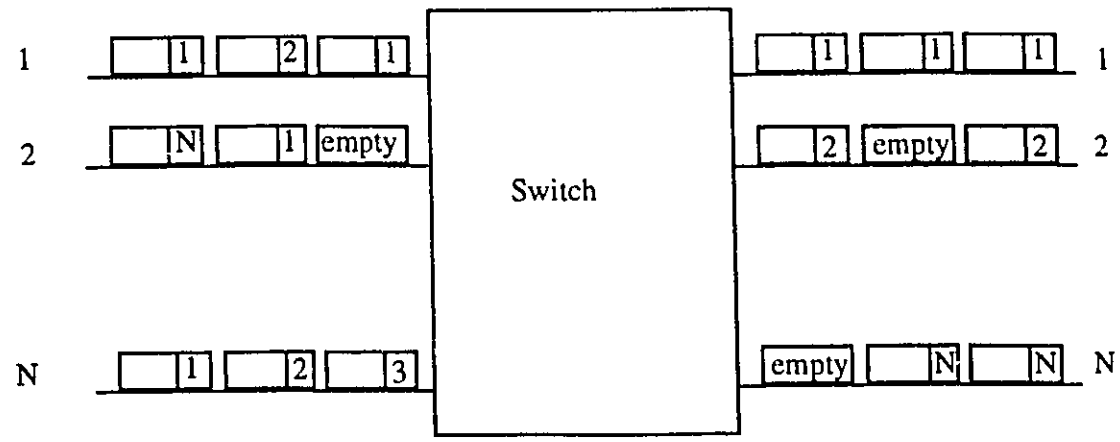

Figure 1.3: An $N \times N$ packet switch

fabric (switching fabric). A logical link is a "digital pipe" or a channel whose control is independent of all other logical links. A physical link is the link formed by a coaxial cable, or other. A single physical link may consists of several logical links. Other components of a full switching architecture such as call processing, line interfacing, and maintenance are not represented in this model.

1.4 Outline of the Thesis

Several switch architectures have been proposed in the literature for BISDN. The performance of a switch is primarily governed by its ability to cope with different types of blocking. In Chapter 2, we first discuss the various types of blockings and then present an overview of the fast packet switch architectures. These switches are classified as blocking and nonblocking switches. In Chapter 3, the performance of several packet switches are given.

Our interest is on Output-buffered Switches with completely partitioned buffer or completely shared buffer, which are of practical importance. Chapter 4 presents the performance of an output-buffered ATM switch with correlated imbalanced traffic and speedup constraint by using a novel and efficient aggregation algorithm.

Chapter 5 considers the transient analysis of the switch by considering the mean time until buffer overflow. The actual distribution of the busy and idle periods of the

output line of the switch are also analytically calculated.

Chapter 6 considers the priority analysis in a completely shared-buffer ATM switch and in a completely partitioned-buffer ATM switch. Finally, Chapter 7 concludes the thesis. Some suggestions for future research are also given.

1.5 List of Publications

Publications that have resulted from this research are:

I. I. Makhamreh, N. D. Georganas, and D. McDonald, "Analysis of an output-buffered packet switch under correlated bursty traffic and speedup." Accepted for publication in the IEE Proceedings-I Communications, Speech and Vision.

I. I. Makhamreh, D. McDonald, and N. D. Georganas, "Approximate analysis of a packet switch with finite output buffering and imbalanced correlated traffic." *Proc. IEEE ICC'94.* session 330.2, New Orleans, May 1994.

I. I. Makhamreh and N. D. Georganas, "Output traffic and Priority analysis for an output buffer in an ATM switch with correlated traffic." *Proc. 17th Biennial Symposium on Communications*, session 4.C, Kingston Ontario, May 1994.

I. I. Makhamreh, N. D. Georganas, and D. McDonald "Priority Analysis of a Shared-Buffer ATM Switch with Imbalanced Bursty Traffic." *Proc. the 1994 Canadian Conference on Electrical and Computer Engineering.* Halifax, Canada, Sept. 1994.

1.6 List of Contributions

The following contributions result from this thesis:

- A general analytical model of an Output-buffered ATM switch is considered:
  1. We assume imbalanced traffic loading at both the inputs, since this is what is happening in practice, and the outputs, since output 'hot-spots' may appear.
  2. Correlation of input cells is permitted, in the sense that all cells of an input burst are directed to the same output port, since an ATM switch may also be

used as a LAN, connecting for-example a video-codec output to a particular display device. The study with correlated traffic also presents a worst-case analysis for the uncorrelated traffic problem.

3. The analytical model assumes finite buffer size, which is the real situation.
4. The input traffic pattern in each switch port is modelled by an Interrupted Bernoulli Process (IBP), since that process captures real-ATM-traffic features such as burstiness, ON/OFF activity periods and cell correlation.

- The analytical study of such an ATM Switch requires the numerical solution of a high-dimensionality problem. To decrease the numerical complexity of this problem, we first provide a method where input-traffic destined for a given output port is aggregated into a single stochastic process. The aggregation method is not new in the literature, but we provide a novel approach for an efficient aggregation based on generating functions. Our approach results in a numerical complexity of the order of $(N+1)(M+1)$, as compared with the one of [13] given as $(2N)^N(M+1)$. Following this aggregation of input sources, the output buffer, driven now by the aggregated source, is studied and its performance measures are obtained.

  It is to be noted that this aggregation method gives an approximate analysis. It becomes, however, an exact analysis for the case of an ATM multiplexer, i.e., a switch with only one output port. To establish the validity of this analytical approximation, we compare its results with the ones of the exact analysis, for small switch cases since the exact method becomes numerically intractable for larger switch sizes. We also compare with simulation results. We find that the method gives good results for dimensioning the buffer of small to moderate switches. The approximation error is found to decrease with decreasing traffic rate or increasing burst lengths. Thus for high-burst, low-intensity traffic, the method is very appealing.

- Efficient buffer dimensioning of a switch for a given cell-loss probability, say 10^{-9}, for various cases (partitioned or shared buffer, with or without cell-priorities, with or without speedup constraints) is a most important engineering contribution of

this thesis. Dimensioning results is given for both the steady-state analysis, where the steady-state probability of cell-loss is the measure of interest, and the transient switch analysis, where the mean-time-to-buffer-congestion is important. The latter analysis is another major contribution of this thesis.

- Besides dimensioning the switch buffer with our efficient analytical method, several results about the behaviour of the switch are obtained. In Chapter 4, studying the case of completely partitioned buffer, the results show that the "hot spot" traffic routing greatly affects the switch performance, as compared to uniform output loading, with regards to cell loss probability and mean cell delay which both get worse. As noticed in other studies, the burst length greatly affects the cell loss probability and the mean cell delay. This is because more correlated cells are routed to the same output port.

- The completely partitioned buffer with speedup constraints is also studied. The results show that a speedup constraint of 4 gives almost the same performance (cell loss probability and mean cell delay) as compared to the complete speedup, N (the switch size). This result may be used for decreasing the implementation complexity of the switch.

- The transient analysis of the output buffer is studied. This study is important because it indicates to the switch designer the mean-time-to-buffer-overflow. This can be used for buffer dimensioning. We also find that the mean-time-to-buffer-overflow decreases as the switch size increases, for a constant load per output line.

- The characterization (busy and idle periods) of the output traffic process from such switches is also studied. The results show that the output traffic process cannot be adequately modeled by a two-state Markov chain. This result is important for performance evaluation of a multistage switch in which the output traffic of a stage is the input traffic to the following stage. It also provides an alternative method for calculating the cell loss probability in the output buffer without calculating the

steady state probability of the queue.

- The lossy period of the output line is the duration of time in which there are cell losses in every time slot. The lossless period, on the other hand, is the period of time in which there are no cell losses in its time slots. The results showed that the lossy period does not change if the buffer size is increased, while the lossless period increases with the buffer size.

- The above buffering techniques are also studied in a switch with two priority classes of traffic. The low-priority cells are served only when no high-priority cells are in the queue. We first analyze the case of a completely partitioned output buffer. We then analyze a completely shared output buffer switch. The results showe that the burst length has no effect on the cell loss probability of the low-priority traffic. But it negatively affects the mean cell delay of the low-priority traffic. On the other hand, the burst length negatively affects the high-priority traffic with regard to both the cell loss probability and mean cell delay .

Chapter 2

Review of Packet Switch Architectures

This chapter presents the packet switches which incorporate the ATM switching concept as their underlying switching technique to support a wide range of services with different bit rates. The switch architectures can be classified into internally blocking and internally non-blocking packet switches. Another classification of packet switches depends on the internal fabric structure. Under this classification are Banyan and buffered Banyan-based fabrics, Batcher Banyan-based fabrics, crossbar-based fabrics, central memory fabrics, and shared medium fabrics [6]. In this chapter we use both classifications.

2.1 Non-blocking Packet Switches

The basic model of a packet switch consists of an $N \times N$ switching element as shown in Figure 2.1. In general, a switching element consists of an interconnection network, an input controller (IC) for each incoming line, and an output controller (OC) for each outgoing line. The arriving cells to the switch are synchronized to the internal clock by the IC. The OC receives cells from the interconnection network and transports them to their destination. Buffering can be at the IC (input buffering) or at the OC (output buffering) or inside the interconnection network (internal buffering).

2.1.1 Types of Blocking in a Packet Switch

There are several types of cell blocking in a packet switch [11].

Internal Blocking A switching fabric is called internally nonblocking if it can provide a connection between a free input-output pair. otherwise it is called internally blocking. Figure 2.2 depicts an internally blocking packet switch. A packet arriving at an input line i can be blocked if the switch fabric has no free internal path during the time slot. The packet has to wait for the following time slots.

Output Blocking A packet arriving at an input i of a switch can be blocked because of other arrival(s) heading to the same output line as shown in Figure 2.3. The blocked packet will be served later according to the type of queueing in the switch.

Head-Of-Line Blocking A packet blocked at the input line because of the previous types of blocking might block other packets behind it from heading to their free destination. Figure 2.4 shows this situation.

2.1.2 Crossbar Packet Switches

A crossbar switch consists of N^2 buses arranged in a rectangular grid. An input line can be connected to any one of the output lines if the output line during a time slot is not occupied. The connection between an input and an output can be made by making a contact (for example by controlling an AND gate) at the crosspoint of the two corresponding lines. During a time slot, a maximum of N packets might arrive at the input lines and have the same output-line-destinational-address (OLDA). This situation is called output port contention. To deal with this phenomenon, one of these packets would be transferred to its OLDA and $N-1$ packets remain at the input Head-Of-Line (HOL) or transferred to an internal queue. HOL packets having the same OLDA are served in random, cyclic, or round-robin procedures. Another way to deal with the output buffer contention is to transfer all the contended packets to a destination simultaneously and buffer them all at the output port.

Input-Buffered Crossbar Switch In input buffering scheme as shown in Figure 2.5, arrived packets at an input line are queued at the IC; externally from the switching grid. The packets in an input queue would be served in a FIFO fashion. A collision occurs if two or more Head-Of-the-Line (HOL) cells compete simultaneously for the same output line. Then all but one of the cells are blocked. The cells behind the blocked HOL cell are also blocked even if they are destined for free (available) output line. This type of blocking is called HOL blocking.

HOL blocking can be overcome by replacing the FIFO buffers at the input by random access memories (RAMs). In this scheme, if the HOL cell is blocked, a cell from the corresponding input queue can be transferred to its free output. So cells blocked behind the blocked HOL cell can bypass the HOL cell. The disadvantage of the bypass strategy is that a complex input buffer control is required.

Output-Buffered Crossbar Switch In output buffer packet switch, packets are queued internally as shown in Figure 2.6. Each output queue serves the output line attached to it only. Output contention can occur in the switch if the number of cells in a time slot and destined to the same output line exceeds the number of free buffers at the output line. Switch architectures with output buffering have optimum throughput [7]. The throughput can reach up to the offered traffic load. The speed of the switching fabric is N times the speed of the input/output line. The buffer access time also should be reduced to accommodate up to N cells in a time slot.

Crosspoint-Buffered Crossbar Switch In a crossbar packet switch buffering is done at the crosspoints of the matrix as seen in Figure 2.7. This type of buffering avoids those cells hunting for different outputs influencing each other. When there are cells in more than one buffer belonging to the same output, an arbitrater is needed to select which cell to be served. No buffer sharing is possible in this scheme.

2.1.3 The Knockout Switch

The architecture of Knockout switch uses a fully interconnected topology to passively broadcast all input packets to all output ports. Each output consists of a module, Figure 2.8, called the bus interface [33]. The bus module consists of a packet filter in which all packets with different address than its output address are deleted. Packets which are accepted by the set of packet filters enter a concentrator. The concentrator with a concentration ratio of $N : L$ will accept a maximum of L packets. Specifically, if there are $k \leq L$ packets arriving in a time slot for a given output, all of these packets will emerge from the concentrator on outputs 1 to k. If $k > L$, then L packets will pass through the concentrator and $k - L$ packets will be dropped in the concentrator. The packets that pass through the concentrator are stored in a dedicated buffer and served according to the FIFO queueing discipline. The Knockout switch is an output-buffered switch. The performance study of the knockout switch shows that a concentrator of size $L = 8$ is sufficient to achieve a packet loss probability of 10^{-6} in the switch.

Many switch architectures based on the knockout principle have been proposed to build large size ATM switches in modular fashion. Here are some of these architectures.

Growable Packet Switch - The Growable Switch architecture [37] is depicted in (Figure 2.9), where a partition is made between a front-end cell distribution network and a column of output switch modules. The function of the distribution network is to route the incoming cells instantaneously to the output switch modules according to the destination addresses of the incoming cells. In order to achieve the best delay performance, buffers are provided only at the outputs of the output switch modules. The outputs are divided into groups of n lines each. Each output switch is of size $m \times n$, where m and n are chosen according to the tolerable cell loss rate, and the considerations involved in the implementation of the switch modules. In an $N \times N$ ATM switch, up to N cells can arrive simultaneously for a particular output group, but only a maximum of m cells can enter a given output switch module. The rest of the cells are knocked-out in the distribution network.

The SCOQ switch - A switch with Shared Concentration and Output Queueing (SCOQ) [35] is composed of a sorting network and L identical switching modules (Figure 2.10). The sorting network (SN) is an $N \times N$ Batcher network which sorts the incoming packets according to their destination addresses. The switching modules are all connected on the SN bus. Each of the switching modules concentrates and routes cells to a group of $K = N/L$ outputs. Each of the L switching modules has N input ports and K output ports and consists of three components: N packet filters, a routing network of L Banyan $K \times K$ switching elements, and K output buffers. The concentration is performed inside the switch module in such a way that at most L simultaneously arriving cells will be routed to each output buffer.

2.1.4 Central Memory based Switches

The following switch architectures are central-memory switches

Prelude Switch - The Prelude switch [27] is a shared buffer memory switch. The architecture of the Prelude switch consists of functional blocks such as, Figure 2.11, : framing, clock adaptation, phase alignment, supermultiplexing, buffer memory, control memory, and a demultiplexing stage. The main difference is that the buffer and the control memories are not cyclically operated, but operated as queues. The buffer memory is operated as a FIFO queue and the control memory is replaced by what can actually be described as a cell switch. The switching function is performed through the indirect addressing of the buffer memory across the control memory [25].

Cell loss may occur in a switching matrix when control queues associated to outgoing multiplexors overflow. These queues must be dimensioned for 32 to 64 cells to keep the cell loss probability less than 10^{-10} for traffic loads of 0.7 and 0.85 respectively, as shown in [26].

Hitachi's Shared Buffer Switch - In this switch architecture, the memory is fully shared by the output ports. Output queues are formed using linked lists. [15].

A serial to parallel (S/P) module performs serial-to-parallel data conversion. A header conversion module (HD CNV) determines which linked list will be put in. There are three other circuitries: the switching chip which contains memory and a multiplexer and a demultiplexer; the control chip which contains read and write registers, one pair for each buffer; and input address buffers which keep track of the status of the unused memory locations.

The cells, after passing the header converter are written one by one into the buffer according to the information provided by the header converter. Simultaneously, a new empty buffer address, if one is available, is supplied from the input address buffers to the control unit. Similarly, at each time slot one cell from each linked list is identified, and retrieved for transmission. Simultaneously, the read registers and the contents of the idle address buffers are updated.

Multicasting is supported by writing multiple copies of a cell to the shared memory.

2.1.5 The Batcher-Banyan based Switches

Beside a crossbar switch, a Batcher-Banyan network can be used for constructing an internally nonblocking and self-routing packet switch. Adding a Batcher network (sorting network) to the Banyan network (Figure 2.12) enables the building of an internally nonblocking switch. The following switches are examples of the Batcher-Banyan switches:

Starlite Switch The Startite switch is the very first switch fabric implemented using sort-Banyan network (Figure 2.13). It overcome the output port contention by using a trap network between the sorting network and the Eanyan network. The packets with repeated addresses are sent back to the sorting network and they again contend in the next slot. Packets are given priority based on their age.

Three-Phase Batcher-Banyan Network A switch architecture based on the the Batcher-Banyan network using a three-phase algorithm is proposed in [36]. The three-phase algorithm is used to resolve the output port contention. In the first phase, each input port i sends a short request packet. The requests are sorted by the Batcher

network and one request per output port is selected. In the second phase, the request packets which won the arbitration send an acknowledgment for their request. In the final phase, the full packets are transmitted through the same Batcher-Banyan network, without any conflict for the output ports. This switch is an input buffer switch.

Sunshine Switch The Sunshine switch, Figure 2.14, is based on a Batcher-Banyan network. It consists of one Batcher sorting network and k parallel Banyan networks [34]. The k parallel Banyan networks (can be looked at as a concentrator) provide k independent paths for cells to access the output queues located in each output port controller. If during a time slot more than k cells request a particular address, then the excess cells overflow into a recirculating queue (shared by all inputs) where cells will wait the next time slot to be resubmitted to the switch. The recirculating queue consists of the T parallel loops and the T dedicated inputs on the Batcher sorting network, each for one cell. The Sunshine switch is an output-buffered switch with concentration. Cells are arranged in order of destination address and priority in the Batcher sorting network. The following trap network resolves output port contention by selecting the k highest priority cells present for each destination address in a time slot. The concentrator separates cells to be recirculated from cells to be routed. The selector directs cells to either the recirculator queue or the set of banyan networks. The banyan networks route the cells to their destinations.

2.2 Blocking Packet Switches

This section describes some switching networks which are internally blocking.

2.2.1 The Banyan Switching Network

The banyan switching network is a self-routing network. Thus it could be suitable for high-performance packet switches. An arriving packet can traverse the banyan switching network in a fully-distributed control. Each packet has a destination address of n bits where $n = log_2 N$ and N is the switch size. Each bit in the address field will route

the packet up or down in each stage. There are n stages for a switch size of N. The disadvantage of the banyan networks is that they are internally blocking which has impact on their usage in high performance switches. A 16×16 banyan switching network can be seen in Figure 2.15. In a banyan network there is only one path that can connect a pair of input and output ports.

2.2.2 The Buffered-Banyan Switching Network

To deal with the blocking at the internal nodes in a banyan network, buffers can be added to the 2×2 switching elements inside the network. Buffering can be at the input ports of the switching elements and in this case it is called input-buffered banyan switching network or at the output ports of the switching elements and the resulting switch is called output-buffered banyan switching network. Also, buffers can be added both at the input and output ports of each switching elements and are called multi-buffered banyan switching network. Figure 2.16 shows a singled buffered Banyan network.

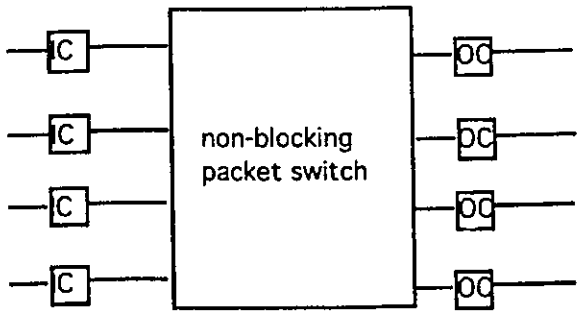

Figure 2.1: The basic model of a packet switch

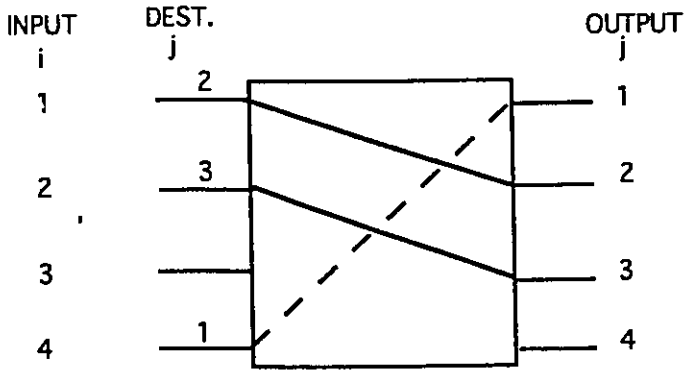

Figure 2.2: Internal Blocking

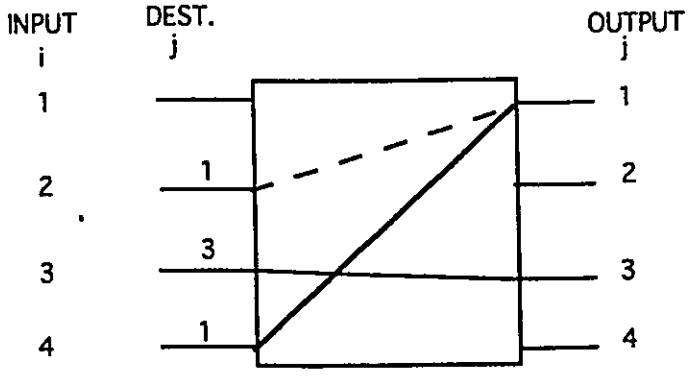

Figure 2.3: Output Blocking

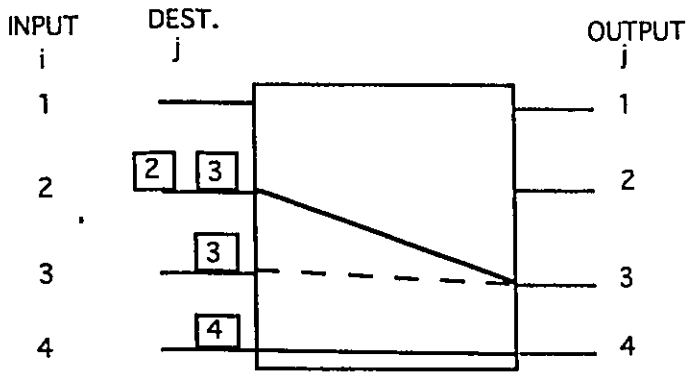

Figure 2.4: Head-Of-Line Blocking

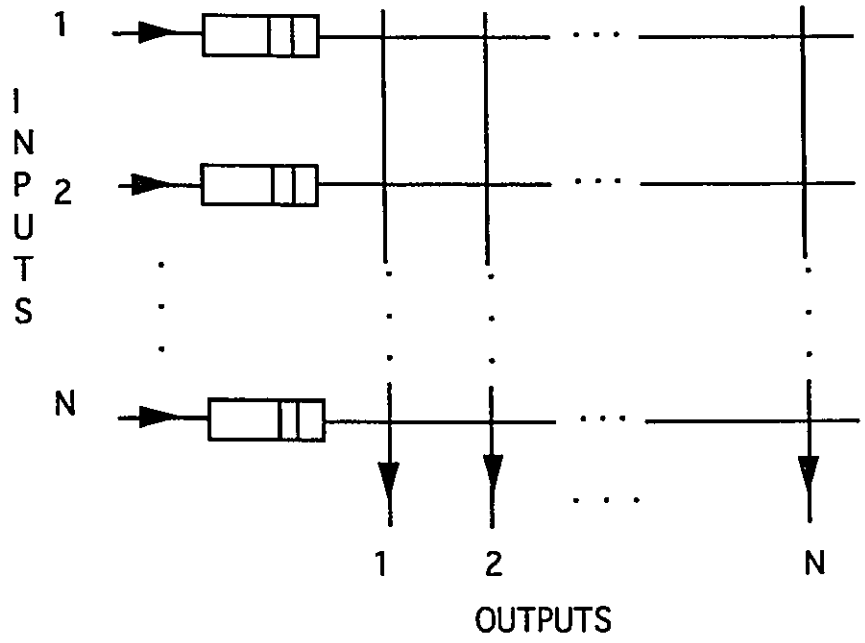

Figure 2.5: Crossbar packet switch with input buffers

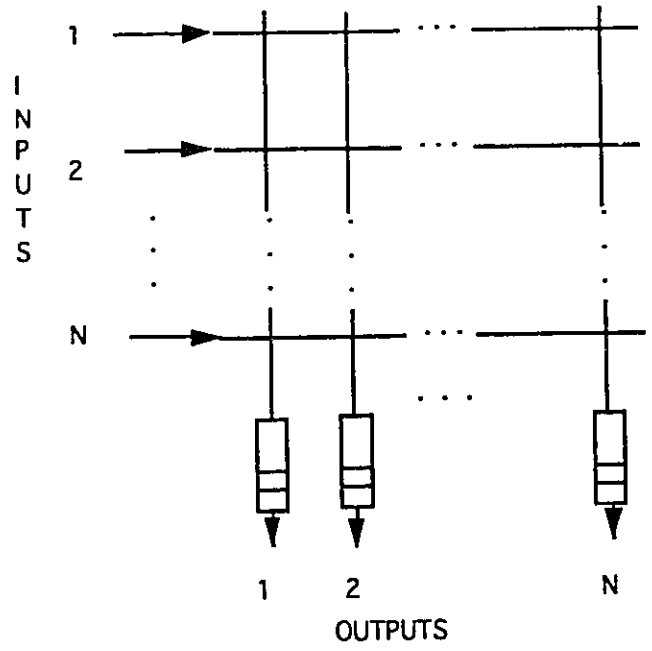

Figure 2.6: Crossbar packet switch with output buffers

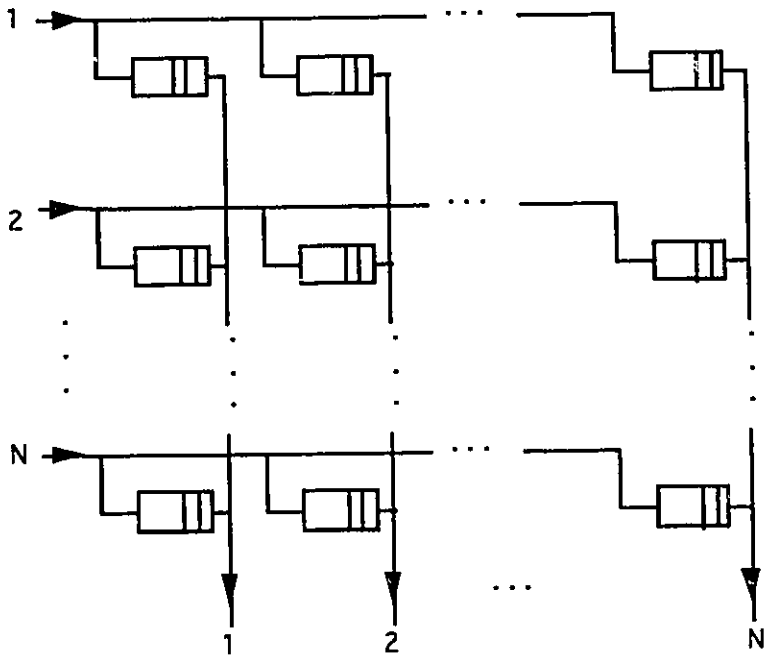

Figure 2.7: Crossbar packet switch with crosspoint buffers

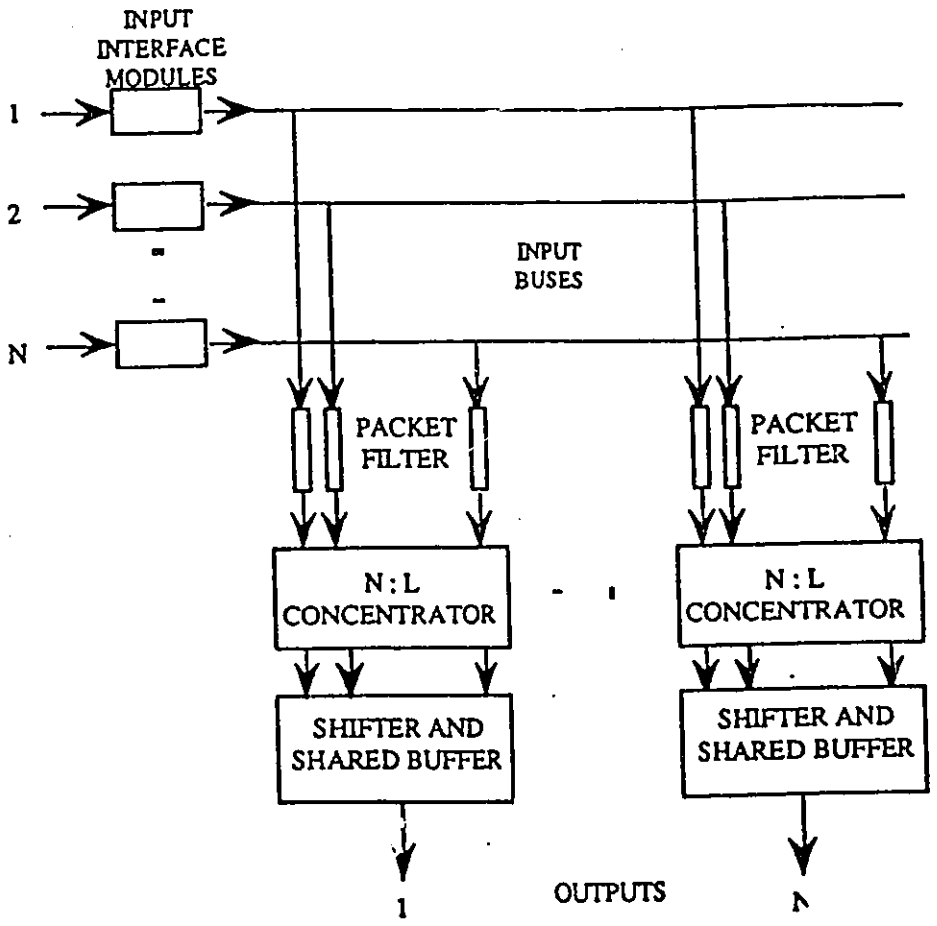

Figure 2.8: The Knockout Switch

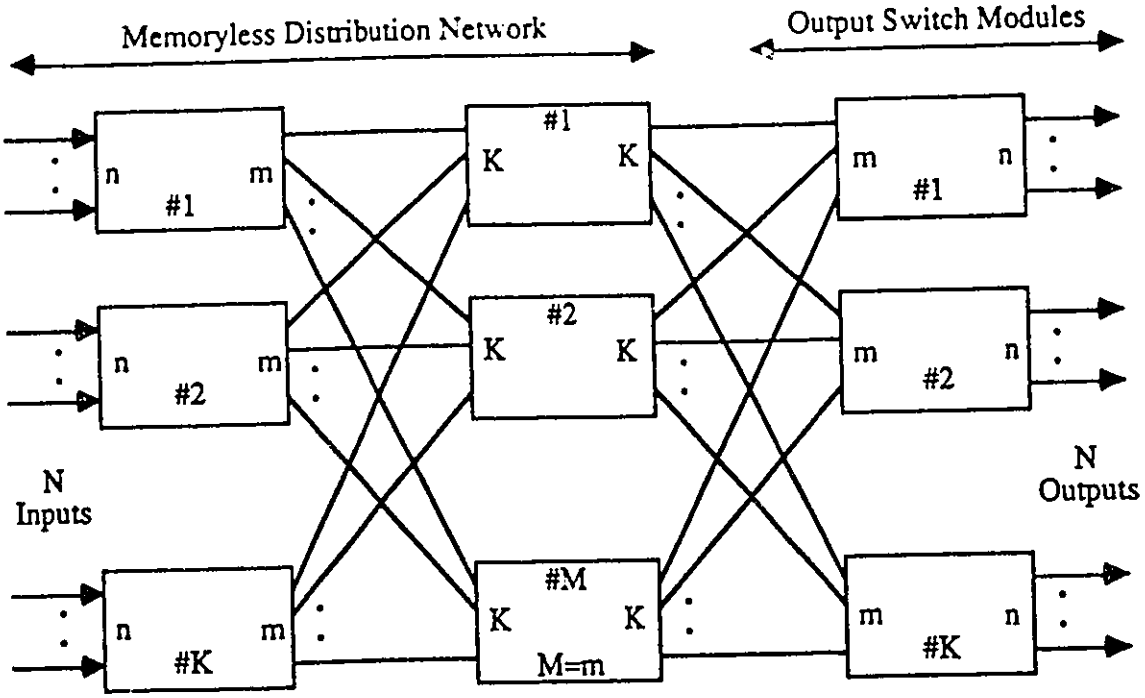

Figure 2.9: The Growable Packet Switch

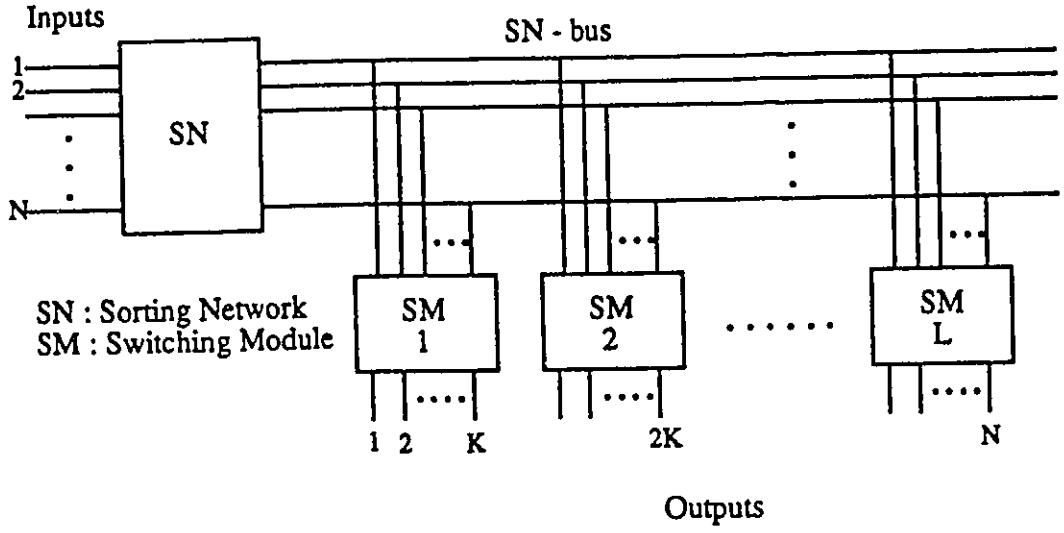

Figure 2.10: The SCOQ Switch

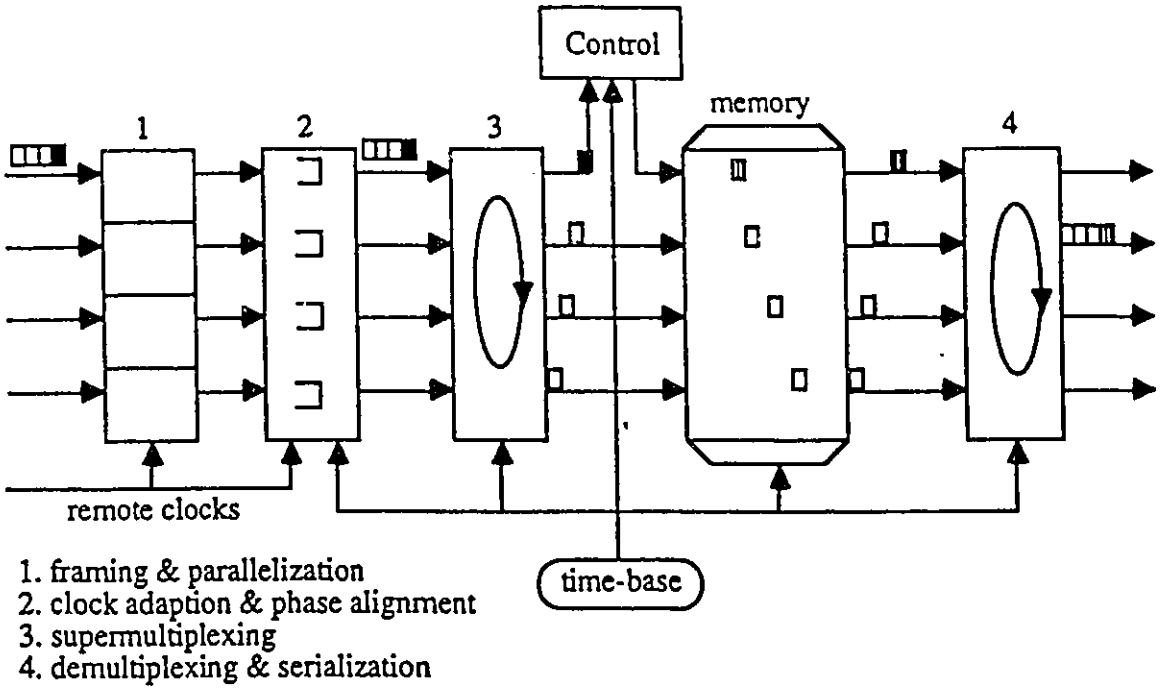

Figure 2.11: The Prelude Switch

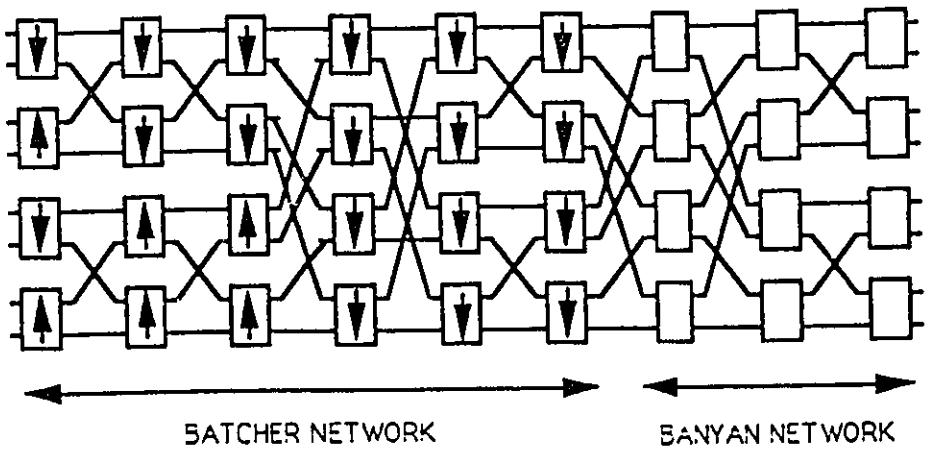

Figure 2.12: The Batcher-Banyan Network

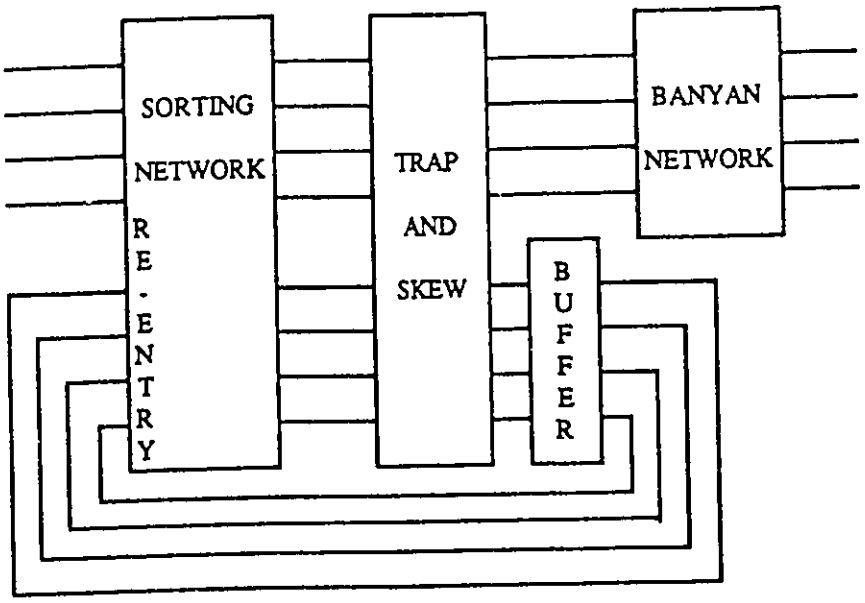

Figure 2.13: The Starlite Switch

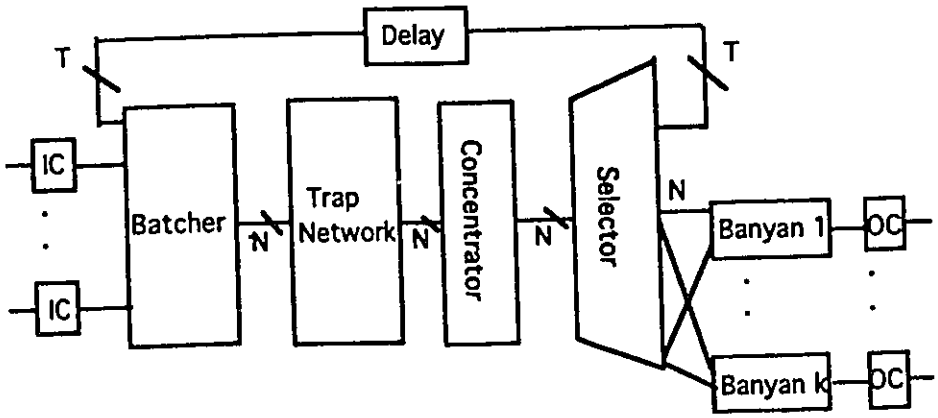

Figure 2.14: The Sunshine Switch

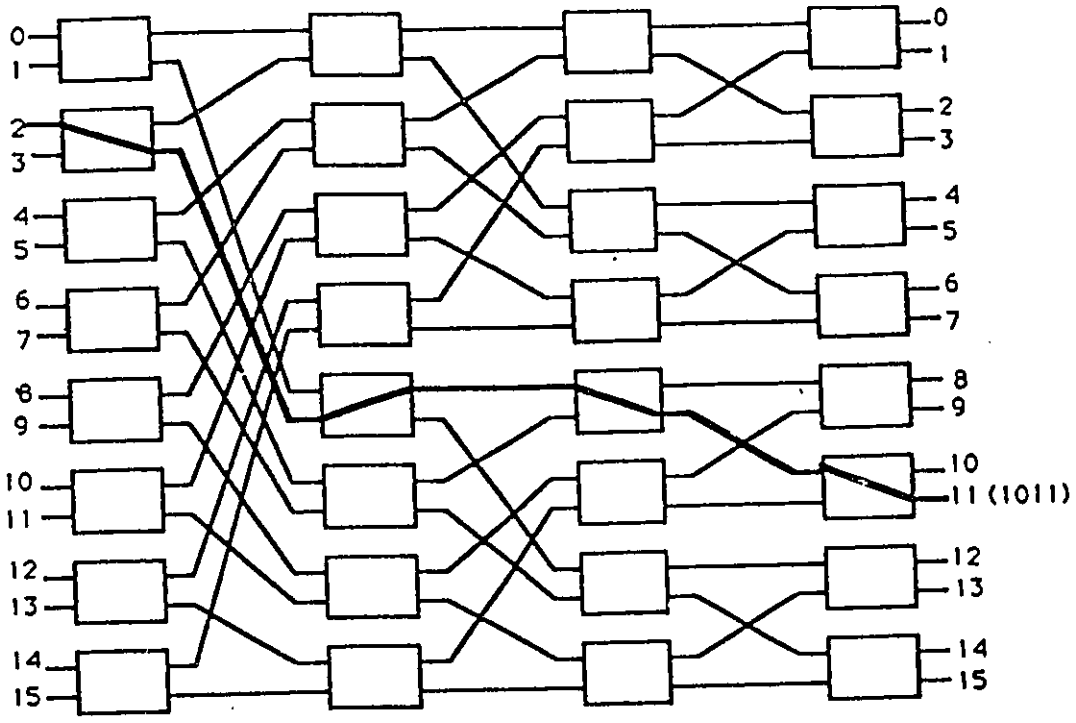

Figure 2.15: The Banyan Switching Network

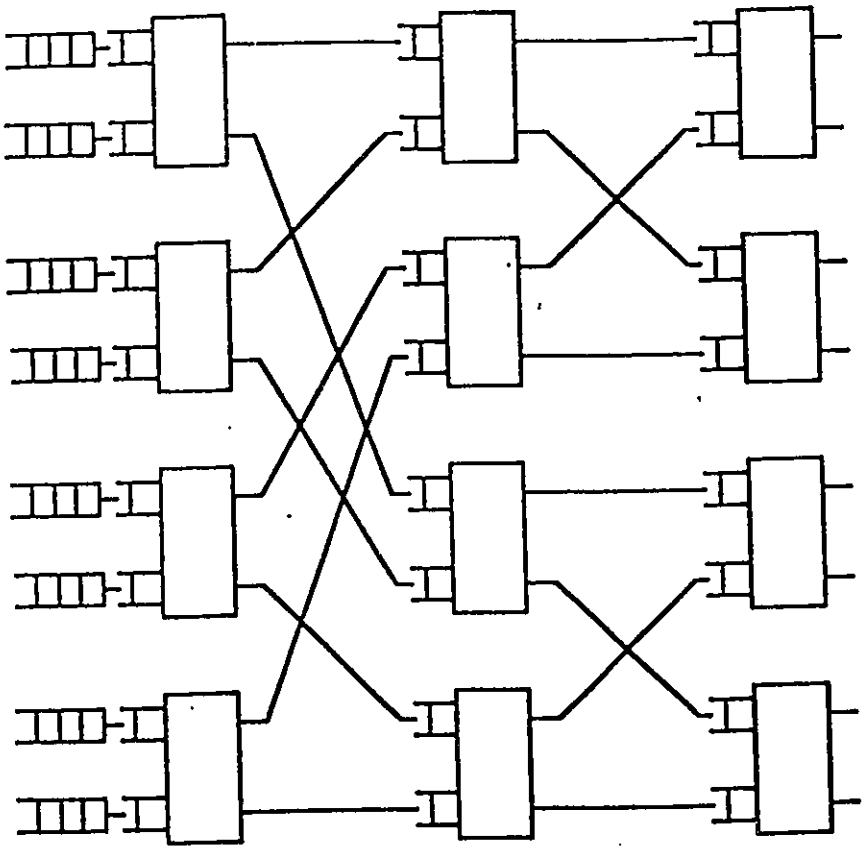

Figure 2.16: The Single-Buffered Banyan Switching Network

Chapter 3

Previous Work on Performance of Packet Switch Architectures

3.1 Multimedia Traffic Source Modeling

The basic problem of ATM networks is the statistical behavior of the cell arrival process, e.g. at a buffer where cells generated by several sources are multiplexed together. The ATM traffic can be described by a three-level hierarchical model [49]. The *call level* has a typical time scale of seconds up to hours, the *burst level* has a range from milliseconds up to seconds, and the *cell level* has a microseconds range. Each level has different impact on network implementation: the cell level traffic model can provide information for buffer sizing in ATM switches and multiplexers, the burst traffic model is used to study call admission strategies, and the call traffic model is related to link dimensioning [49][19].

3.1.1 Modeling a Bursty Traffic Source

Bernoulli Processes - In discrete-queueing models of ATM switches, the Bernoulli process (BP) is used to model traffic sources. The Bernoulli traffic source (called uniform traffic source or random traffic source) generates a cell at each time slot with probability p and with probability $1-p$ it does not generate a cell. Cells are generated independently from one time slot to another. The Bernoulli process is governed by a two-state Markov

chain (MC) which alternates between two geometrically distributed periods; busy period and idle periods as shown in Figure 3.1.

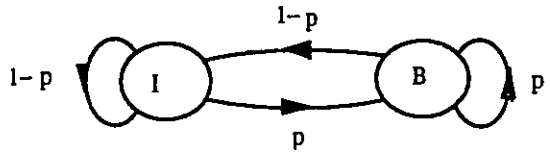

Figure 3.1: The Bernoulli Process

Interrupted Bernoulli Processes - Another traffic arrival process is the Interrupted Bernoulli Process (IBP). The interrupted Bernoulli source generates Bernoulli traffic with rate p during a geometrically distributed period with mean $1/\alpha$, called the busy period, and generates no cells during a geometrically distributed period with mean $1/\beta$ which is called the idle period. This is why it is called Interrupted Bernoulli Process. The IBP is governed by a two-state MC as shown in Figure 3.2.

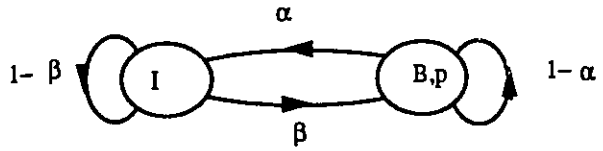

Figure 3.2: The Interrupted Bernoulli Process

Notice that even during the busy period of the IBP there could be empty slots. If the rate $p = 1$, then each time slot in the busy period contains a cell. The IBP is more flexible in modeling traffic arrival processes than the BP because it has three parameters (namely α, β, and p) that can be adjusted to fit the modeled arrival process. It can capture the burstiness of the arrival process more than the BP. The burstiness (variability) of a traffic source is usually defined to reflect the variation of the traffic source from idleness (inactive) to business (active). In this sense, the burstiness can be measured quantitively by

- the squared coefficient of variation of the interarrival time of cells.
- the length of the active period (burst length = $1/\alpha$).
- the ratio = peak bit rate / average bit rate.

The analysis of an ATM switch with IBP will depend on whether each cell in a burst is routed independently or all cells in a burst are directed to the same output line (sometimes called binary source). The second case can capture a correlated source in the sense that adjacent cells in a burst have the same destination.

Autoregressive Traffic Models - The autoregressive moving average process (ARMA) is used to model the output of a video codec. It has been adopted because the performance measures of a queueing system are most sensitive to the autocorrelation function of the arrival process [17]. The long-term mean, variance, and autocorrelation functions are measured from the cell output of the simulated video codec. These are then used to estimate the parameters of a mathematical model of an ARMA process.

Characterization of packetized voice traffic A packet voice source can be modeled by an interrupted renewal process which alternates between a silence period and a talkspurt period. Each of the periods has an exponential duration. The mean silence period is 650 ms and the mean talkspurt period is 352 ms. The voice packetization period is 16 ms. The packet size is 64 bytes with 32 kbits/s ADPCM coding. The arrival traffic voice process is very bursty (comparing to Poisson arrival process) with square coefficient of variation of the interarrival time $c^2 = 18.1$ compared to $c^2 = 1$ for a Poisson arrival process [22].

The aggregate packet arrival process resulting from the superposition of many independent voice packet processes is not a renewal process (each process alone is a renewal process because each time slot can contain a packet independently from previous time slots). As it has been observed before, this is to be expected because the instantaneous arrival rate in the aggregate packet voice arrival process at any time is a function of the number of voice sources in talkspurts, which fluctuates substantially.

3.1.2 Modeling Superposition Process

Markov Modulated Bernoulli Processes - The Markov Modulated Bernoulli Process (MMBP) is another candidate for modeling arrival processes to an ATM multiplexer or an ATM switch. The general model for an m-MMBP source consists of m states. During each state the source generates Bernoulli traffic, but each state has its own traffic rate $p_i, i = 1, 2, \ldots, m$. A three-state MMBP is shown in Figure 3.3.

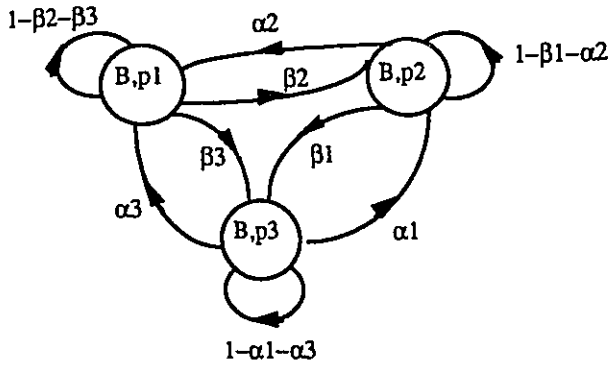

Figure 3.3: A Three-State Markov Modulated Bernoulli Process

The BP and the IBP are special cases of the 2-MMBP. The 2-MMBP has four operational parameters and it can capture more statistical parameters of an arrival traffic process than the BP or the IBP. It is usually used to model the superposition of several voice or video traffic sources. The superposition method depends on selecting the four parameters of the 2-MMBP in such a way to fit the first and/or the second statistical moments of the modeled traffic process. It could be also a suitable traffic model for a multiplexed line where the idleness does not sharply appear.

The superposition process of N arrival processes can be obtained by approximating the sum of the arrival processes by one arrival process. The superposition of a number of renewal processes generally does not result in a renewal process, hence one approach is to approximate the superimposed arrival processes by a single renewal process and the aim then is to analyze a GI/D/1/K queue [20] or using a Markov Modulated Poisson Process

(MMPP) and the aim is to analyze a MMPP/D/1/K queue [21]. Another approximating technique is the fluid-flow approximation [28]. The fluid-flow approximation looks to the flow of cells in the queue as a continuous process just as the flow of water in a dam. An application of the fluid-flow approximation technique in the performance analysis of a packet multiplexer can be found in [23]. The aggregation method that we have used depends on approximating the N arrival processes by a $N+1$-state Markov Chain (MC).

Self-Similar Traffic Models - Recent traffic measurements have revealed a new phenomenon. These measurements include analysis of hundreds of millions of observed packets over Ethernet LAN and an analysis of a few millions of observed frame data generated by VBR video services. In these studies, packet traffic appears to be statistically self-similar. This means that at every time scale ranging from a few milliseconds to minutes and hours, similar-looking traffic bursts are evident [67].

Potential implications of self-similar traffic on issues related to design, control, and performance of ATM networks are currently under study.

3.2 Performance of Input-Buffered Packet Switch

The performance of input-buffered switch is considerably affected by the Head-Of-Line blocking phenomenon. For a large switch size (N equal to infinity) the maximum throughput is 0.5858 [8]. This is because the cells that remain at the head of the queue in a time slot may block cells that are waiting behind the HOL cells even if their destination outputs are free. At a time slot, and if there are k cells whose destination is the same output line, say O_1, one cell will go through and the rest of $k-1$ cells will be waiting at the head of their queues. In the next time slot, one of $k-1$ HOL cells, besides new arrivals which have moved to the HOL of other queues, say v cells, and whose destination is O_1, will go through. So at the end of the second time slot, the number of input queues whose HOL cells have destination O_1 is $k-1+v-1$. These HOL cells block other cells waiting at the queues from reaching their destination even though their destination might be free. The HOL effect on switch size N [7] is shown in Table 3.1.

N	Maximum Throughput
2	0.7500
3	0.6825
4	0.6553
5	0.6399
6	0.6302
7	0.6234
8	0.6184
∞	0.5858

Table 3.1: The maximum throughput versus switch size with input queueing and FIFO buffers

The HOL blocking phenomena can be tickled if at each time slot the $k-1$ cells are discarded. By this strategy the maximum throughput attained is 0.632 [8]. Actually, by dropping the HOL cells which do not go through in each time slot, one may think that the throughput will decrease because we are losing cells. This is true but above certain utilization level the effect of the number of discarded cells becomes less dominant and an increase in the throughput is attained.

The previous throughput figures assume that if more than HOL cells request to be transferred to the same output, one of them will be selected randomly. Other arbitration strategies which can be applied are:

Cyclic: The queues are served in a cyclic order.

Queue dependent: The HOL cell from the longest queue will be served first. The actual lengths of the buffers requesting the same output line have to be compared.

Delay dependent: This is a global FIFO strategy taking into account all the buffers that feed one output.

A comparison obtained by simulation of the performance of the different arbitration strategies can be seen in Figure 3.4 [19].

A nonuniform traffic analysis of an input-buffered packet switch is in [43]. In this study the maximum throughput with nonuniform traffic is less than 58.6 per cent.

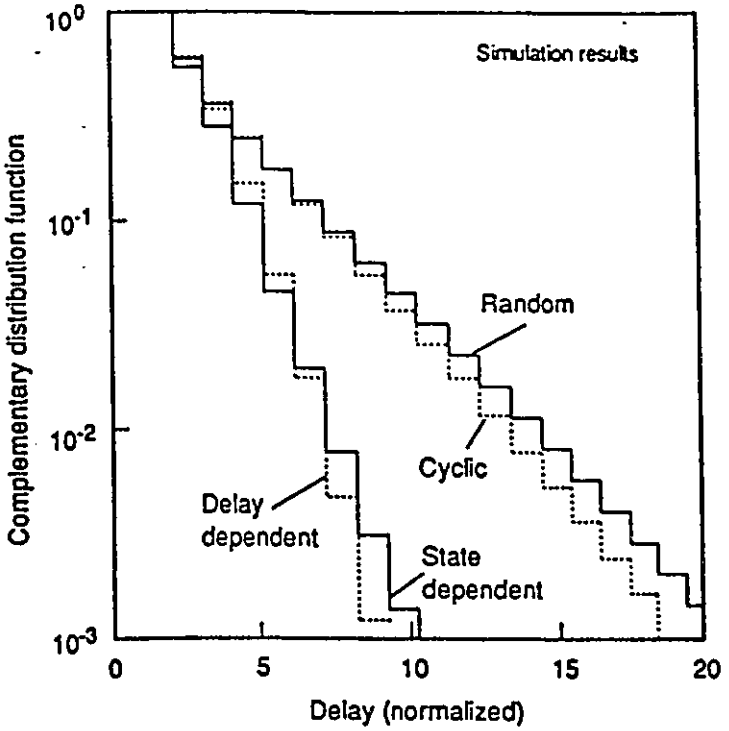

Figure 3.4: The delay-performance of different arbitration strategies

3.3 Performance of Output-Buffered Packet Switch

A crossbar packet switch with output buffers or a central memory packet switch with complete partitioning has a maximum throughput which can reach the offered traffic at the input, i.e., the throughput is 1.0. The speed of the switch fabric is N, the switch size. The output-buffered packet switch achieves a better throughput/delay performance than the input-buffered packet switch. But on the other hand, it requires the switching fabric to work on speeds equal to N times the speed of an input/output line in comparison with the input-buffered switching fabric which works at the same speed of an input/output line. This is because that in output-buffered switch, up to N cells may arrive to a destination

in a time slot. In an input-buffered switch, the arriving cells are buffered at the input and only one cell is transfered to its destination. Figure 3.5 shows the cell loss probability versus the buffer size b for different switch sizes with uniform traffic of load 0.8.

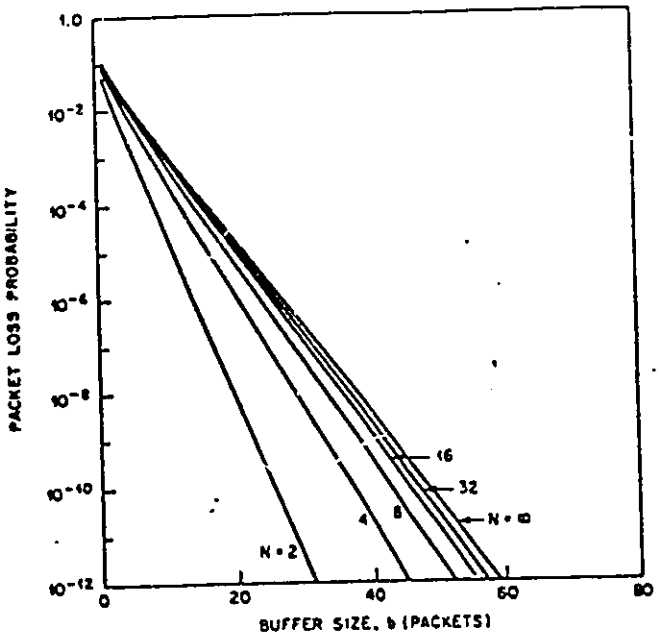

Figure 3.5: The cell loss probability versus the buffer size in an output-buffered packet switch.

3.4 Performance of Input-output buffered Packet Switch with speedup

This type of switch combines both input and output queueing. An input-output buffered switch with correlated traffic is studied in [60]. The primary aim is to achieve the best possible performance by output queueing. However, economic considerations might require restrictions on output queueing (speed of the switching fabrics) in favor of additional input queueing. The input buffers are implemented at the input controller outside the switching fabric. However, the output buffers are (in general) part of the switching fabric and they account for the total complexity of the switching fabrics because they require

L	Maximum Throughput
1	0.5858
2	0.8845
3	0.9755
4	0.9956
5	0.9993
6	0.9999
∞	1.0000

Table 3.2: Maximum throughput of non-blocking packet switch with input and output buffers ($N = \infty$)

the existence of buffers with high-speed access time. In VLSI technology, the buffer space within the fabric is the cost-sensitive factor. However, studies have shown that output buffers of relatively small size, b cells, are sufficient for closely approaching the optimum delay/ throughput performance of large (infinite) output buffers. Thus, the amount of speed-up or parallelism required can be limited to a factor of $b << N$, N is the switch size. In the case of Knockout switch [33] the amount of parallelism required is about 8 with no input queueing. In [42], an $N \times N$ packet switch with input and output buffers is analyzed. They assume infinite switch size and that the speedup factor is greater or equal to the output buffer size. Also, packet losses due to output buffer overflow are avoided by a backpressure mechanism which causes packets to wait in additional input buffers if the output buffers are full. Table 3.2 shows the maximum throughput for several speedup factors L [9]. The results in the Table show that L should be greater than or equal to 3 in order to achieve a throughput of 0.9 with a packet loss probability of no more than some value, say 10^{-6}.

3.5 Performance of a Shared Memory Switch

In a shared buffer packet switch, a pool of buffers is available to all output lines of the switch. The following buffer-sharing schemes have been considered [14]. The first is *complete sharing*, which is such that an arriving packet is accepted if any buffer space is available, independent of the output line to which it is directed. The *complete sharing* performs better than the fully dedicated output buffers (*complete partitioning*) under normal traffic conditions and for balanced inputs. In [15], it has been shown that the completely sharing scheme reduces the required memory quantity to 0.14 of that required using the *complete partitioning* scheme. A discrete-time queueing model of the shared buffer with complete sharing and bursty traffic has been analyzed in [13]. The study in [16] shows that the number of buffers required with complete sharing, for random traffic, would be over-estimated by as much as 30 percent at 90 percent traffic load if the negative correlation that naturally exists, for this type of traffic, between packet streams destined for different output ports were not taken into account. The drawback of complete sharing is when the traffic is unbalanced. It results in most of the space being occupied by packets waiting for output lines with higher input rates. It also fails in securing a full utilization of all output lines.

To avoid the possible monopoly of the entire space by any particular output line, a constraint is imposed on the number of buffers that a particular output line can capture. This is the third scheme which is *sharing with maximum queue*. The fourth scheme; *sharing with minimum allocation*, guarantees at any time that there be a space allocated to any output line. But its disadvantage is that it does not secure other output lines from the monopoly of traffic for a particular output line to capture the rest of the space. The fifth scheme is *sharing with maximum queue and minimum allocation*. A shared-buffer memory switch with maximum queue and minimum allocation is proposed in [39].

Table 3.3 shows the buffer size for packet switches with different buffering strategies (central, input, output) assuming an average load of 85 per cent at each input and cell loss probability of 10^{-9} [48].

Switch type	$N \times N = 16 \times 16$
Central memory	113 cells (47.92 kbits)
Input buffer	320 cells (135.68 kbits)
Output buffer	896 cells (379.91 kbits)

Table 3.3: Buffer size requirements

Chapter 4

Analysis of an Output-Buffered ATM Switch with Correlated Bursty Traffic and Speedup

We apply an aggregation method to analyze an output-buffered ATM access switch with correlated imbalanced traffic. Each input port of the switch is assumed to be driven by an Interrupted Bernoulli Process and every cell in a burst is directed to the same output port. The mean throughput, delay, and cell loss probability are calculated numerically for a switch driven by an equivalent aggregated source. The switch with speedup constraints is analyzed. The approximation to the original system is shown to be excellent.

4.1 Introduction

Several previous studies of self-routing packet switches have usually assumed random input traffic (no correlation between adjacent cells) [8]. The input traffic to an ATM switch is usually a multiplexed traffic from several previous sources and thus can be modeled by an uncorrelated (random) traffic. If, however, the switch is fed directly with traffic from unmultiplexed multimedia sources, with bursty behavior, then contiguous cells of a burst may belong to the same source and will have to be switched to the same output port.

This chapter considers the above case of correlated and bursty input traffic (see also [29]). It should be noted that this correlated traffic provides a worst case scenario for input traffic to a switch. However, the case of uncorrelated traffic can be easily incorporated in the analysis.

The analysis of an output-buffered space-division switch with correlated traffic was studied by Hou and Lucantoni [29]. With the assumption of an infinite buffer and balanced traffic sources, they used the matrix-geometric method for their analysis. Chen and Mark [30] have also studied an output-buffered space-division switch with finite and infinite buffers. With the assumption of balanced (i.e., homogeneous) traffic sources, an approximate approach based on the moment generating functions was proposed. Linear state equations were also used to solve the steady state distribution. Hong, et al. [13], have applied a decomposition and aggregation technique to study a shared-buffer ATM switch with random imbalanced traffic sources where the traffic is modeled as an Interrupted Bernoulli Process (IBP).

In this chapter, we consider an output-buffered switch. Each input traffic process is modeled as an Interrupted Bernoulli Process. The traffic sources may have different traffic parameters (i.e., imbalanced input loading) and different routing probabilities (i.e., imbalanced output loading). Finite buffers are assumed at the output ports. We use a decomposition and aggregation process, similar to [13], but our computational method is much simpler. Correlation is also introduced to the traffic by switching an entire burst to the same output. Contrary to the analysis in [29], the switch is analyzed with respect to the traffic parameters of the input sources at the switch (i.e., IBPs). In [29] and [30], they used what is called binary sources at the input of an output queue without relating their parameters to those of the input traffic sources at the input ports. It is true that both have the same burst length but the idle period is not the same.

This chapter is organized as follows: Section 4.2 describes the switch model. In Section 4.3 (i.e., model analysis) the exact algorithm, based on a complete state description of the discrete-time queueing model of the switch, is described. Section 4.4 considers the case of random traffic. In Section 4.5, the algorithm validation is provided. The ATM

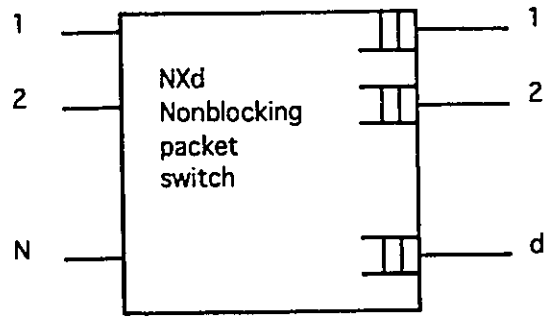

Figure 4.1: Switch Model.

multiplexer is discussed in Section 4.6. The switch performance parameters are given in Section 4.7. Numerical results are given in Section 4.8. Section 4.9 considers the switch with speedup constraint.

4.2 Model Description

4.2.1 Switch Model

We consider a discrete-time model of an ATM switch placed at an access node to a broadband network. The switch is a self-routing $N \times d$ ATM switch, $d = 1, \cdots, N$ and each output port has a dedicated buffer of size M cells (Figure 4.1). The time is slotted in units of cell service time. The speed of the output ports is equal to the speed of the input ports. We model a central memory switch with completely partitioned buffer. The switch fabric allows a maximum of N cells arriving to reach their destination outputs in one time slot without blocking. A cell leaves its queue after receiving service in one time slot of service. Cells are served according to the first-in-first-out (FIFO) strategy. A cell arriving at a full queue which is lost.

4.2.2 Input Traffic Modeling

Each input traffic source is modeled by an Interrupted Bernoulli Process ($IBP_i, i = 1, \cdots, N$) with parameters α_i and β_i as shown in Figure 4.2, where the states also shows

the destination of cells. During an idle period (I), no packets arrive at the inputs. During a burst period (B), packets arrive with rate λ_i. In our analysis $\lambda_i = 1$. In this case, a cell arrives in every slot during a burst at the input. The steady state probability that any slot contains a packet, ρ_i, is given by:

$$\rho_i = \frac{\beta_i/\alpha_i}{(1+\beta_i/\alpha_i)} \tag{4.1}$$

and the average burst length is $1/\alpha_i$. In this thesis, the mean burst length is taken as the burstiness index, $r_b(i)$. The squared coefficient of variation (i.e., the variance divided by the square of the mean), C_i^2, of the interarrival time between cells is:

$$C_i^2 = \frac{2/\alpha_i - 1}{(1+\beta_i/\alpha_i)^2} - \frac{\beta_i/\alpha_i}{(1+\beta_i/\alpha_i)^2} \tag{4.2}$$

The assumption of IBP captures some characteristics of real traffic such as burstiness, ON/OFF periods, and correlation.

We assume that a new burst arriving at input port i will be directed to output port j with a probability d_{ij}. All the cells in the burst go to the same port. The mean traffic load (average cell rate) at the output queue j is

$$TL_j = \sum_{i=1}^{N} d_{ij}\rho_i \tag{4.3}$$

Notice that $\sum_{j=1}^{N} d_{ij} = 1$.

4.3 Model Analysis

4.3.1 Numerical Solutions

The state space S of the discrete-time queueing model of the switch (Figure 4.3) is described immediately after the beginning of each time slot (Figure 4.4) by vectors $(\underline{w};\underline{n}) = (w_1,...,w_N;n_1,...,n_d)$, where w_i is the state of the i^{th} arrival process and n_j is the number of cells in the j^{th} output buffer, $0 < n_j \leq M, j = 1,\ldots,d$. w_i is a subvector (x_i, y_i) where x_i is the state of the i^{th} arrival process, and y_i is the output destination port

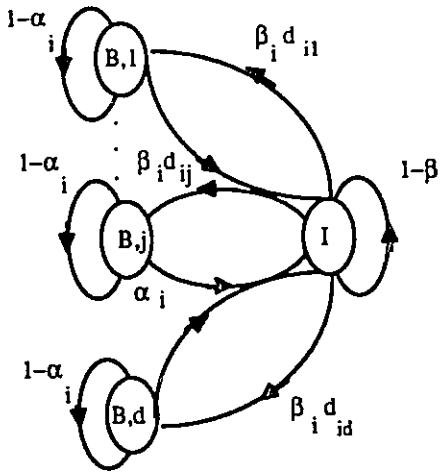

Figure 4.2: The Markov chain with $d+1$ states that describes, for one input, jointly the IBP_i and the destination of the burst.

of the last cell produced by arrival process i. Hence, $x_i \in \{0,1\}$ where state 0 represents a silence and state 1 represents a burst and $y_i \in \{1,2,\cdots,d\}$.

Let Q_i be the transition matrix of the i^{th} arrival process governed by the Markov chain as in Figure 4.2. $W(\underline{w^a},\underline{w^b})$ is the transition probability from state $\underline{w^a} = ((x_1^a,y_1^a),\ldots,(x_N^a,y_N^a))$ to the state $\underline{w^b} = ((x_1^b,y_1^b),\ldots,(x_N^b,y_N^b))$. Then, with the assumption that the N arrival processes are independent, $W(\underline{w^a},\underline{w^b})$ can be calculated by using the following equation:

$$W(\underline{w^a},\underline{w^b}) = \prod_{i=1}^{N} Q_i((x_i^a,y_i^a),(x_i^b,y_i^b)) \tag{4.4}$$

where for $1 \le j,k \le d$,

$$Q_i((1,j),(1,j)) = 1-\alpha_i \tag{4.5}$$

$$Q_i((1,j),(0,j)) = \alpha_i \tag{4.6}$$

$$Q_i((1,j),(1,y)) = 0 \; y \neq j \tag{4.7}$$

$$Q_i((0,j),(0,j)) = 1-\beta_i \tag{4.8}$$

$$Q_i((0,j),(1,k)) = \beta_i d_{ik} \tag{4.9}$$

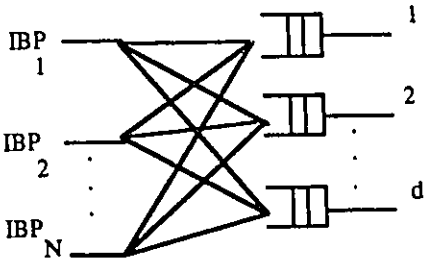

Figure 4.3: Queueing model of the switch.

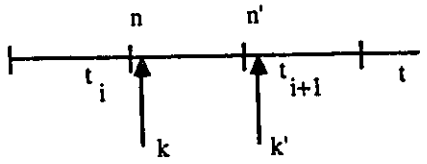

Figure 4.4: State-time relation.

Note that, $\pi_W(\underline{w})$, the steady state probability of state $\underline{w}$, can be obtained by:

$$\pi_W(\underline{w}) = \prod_{i=1}^{N} \pi_i[(x_i, y_i)] \tag{4.10}$$

Where, $\pi_i(x_i, y_i)$ is the steady state of the state (x_i, y_i) for the i^{th} source so $\pi_i(0, j) = (1 - \rho_i)d_{ij}$ and $\pi_i(1, j) = \rho_i d_{ij}$ for $i \in \{1, 2, \ldots, N\}$ and $j \in \{1, \ldots, d\}$. Notice that equation (4.7) forces all the cells in the same input burst to be switched to the same output queue (see also [29]).

The transition probabilities of the matrix $P((\underline{w}^a; \underline{n}^a); (\underline{w}^b; \underline{n}^b))$ of the full queueing model can be obtained by considering that $n_j^b = min\{(n_j^a - 1, 0)^+ + k, M\}$, where $k = \sum_{i=1}^{N} \chi\{x_i = 1, y_i = j\}$ is the number of sources in burst mode with their cell destination at a given time slot being queue j. $\chi\{\}$ is an indicator function. The steady state distribution $\underline{\pi}(\underline{w}; \underline{n})$ can be computed numerically by solving the linear system $\underline{\pi}P = \underline{\pi}$, where P is the transition matrix of the system.

The difficulty in solving this system of equations is that the size of matrix P becomes very large as the switch size increases. The state space size is $(2d)^N.(M + 1)^d$, which is

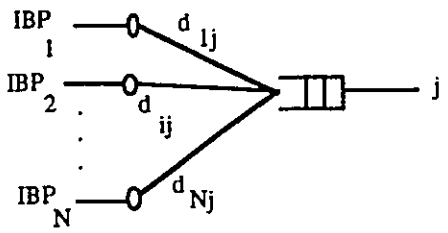

Figure 4.5: Queueing model of subsystem j.

even larger than the state space size describing the switch with random traffic assumption (i.e., $2^N.(M+1)^d$) [13].

4.3.2 Approximate Analysis Algorithm by Decomposition and Aggregation

To reduce the state space size, decompose the queueing model of the switch into d subsystems, one for each queue as shown in (Figure 4.5). Each subsystem is then analyzed separately. The results of all subsystems are then combined to get the analysis of the switch. The state space associated with one subsystem can be further reduced by aggregating the N arrival processes, defined by the transition matrix W, into one arrival process. The state space of the induced arrival process is $k, k = 0, 1, ..., N$. If the induced arrival process is in state k, then there are k cells arriving at queue j and for simplicity we may assume $j = 1$.

The transition matrix, W^*, of the aggregated process can be induced from W as follows (Figure 4.6): let S_W be the state space associated with W, and let S_{W^*} be the induced state space. Then, each state in S_{W^*}, say $k = i$, represents the aggregation of all states in S_W, with exactly i arrivals destined to queue j. The transition probability, $W^*(i, i')$, between state i and state i' in the induced space can be calculated from:

$$W^*(i,i') = \frac{\sum_{\underline{w}^a \in H} \pi_W(\underline{w}^a) \sum_{\underline{w}^b \in H'} W(\underline{w}^a, \underline{w}^b)}{\sum_{\underline{w}^a \in H} \pi_W(\underline{w}^a)} \tag{4.11}$$

where $H = \{\underline{w}^a; f_j(\underline{w}^a) = i\}$, $H' = \{\underline{w}^b; f_j(\underline{w}^b) = i'\}$ where f_j denotes the map from S_W

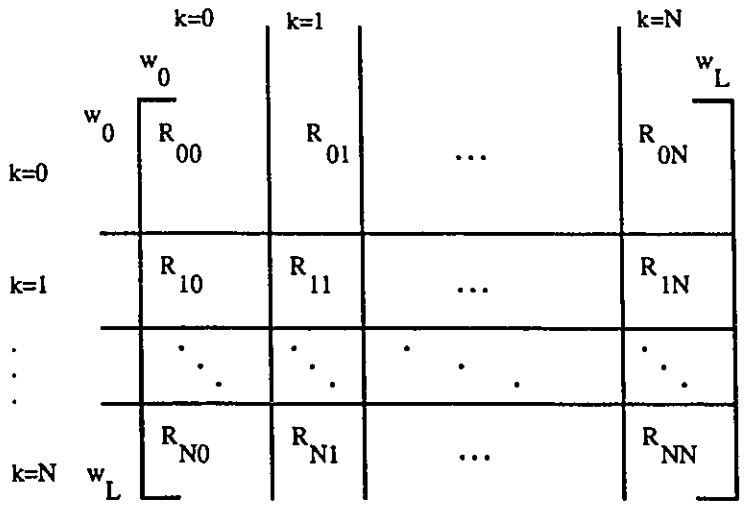

Figure 4.6: Inducing the aggregated transition matrix, W^*, from matrix W.

to S_{W^*} such that $f_j(\underline{w}^a) = k$ if k bursts are directed to output port j.

The steady state probability of a state k in the induced space is given by

$$\pi^*_W(k) = \sum_{\underline{w}^a \in H} \pi_W(\underline{w}^a) \tag{4.12}$$

The state of the output queue j driven by the aggregated source can now be described by (k,n), where k is the number of cells arriving at queue j immediately after the beginning of the slot and n is the queue length of queue j at that time. We assume that the service time is one slot and that arrivals have to wait one slot before service starts. The queue length immediately after the end of the slot is, therefore, $min\{(n-1,0)^+ + k, M\}$. The transition probability between any two states of the queue is

$$P^*((k,n);(k',n')) = W^*_{kk'}\chi\{n' = min\{(n-1,0)^+ + k, M\}\} \tag{4.13}$$

where, (k',n') is the state of queue j in the next slot and $\chi\{\}$ is an indicator function. P^* is a transition kernel on the state space $\{(k,n) : 0 \leq k \leq N, 0 \leq n \leq M\}$.

The difficulty with generating W^* from W is the huge amount of processing time and storage. The number of operations and storage to generate W^* can be reduced to $6N^2$ multiplicative operations, as follows. First, the steady state probabilities of the aggregated

source, $\pi^*_W, j = 0, 1, \ldots, N$ can be calculated in $2N^2$ operations by multiplying recursively from the following equation:

$$\begin{aligned}\sum_{i=0}^{N} \pi^*_W(i)s^i &= \prod_{i=1}^{N} [\sum_y \pi_i(0,y) + \sum_{y \neq j} \pi_i(1,y) + \pi_i(1,j)s] \\ &= \prod_i^N [(1-\rho_i) + \rho_i(1-d_{ij}) + \rho_i d_{ij} s] \end{aligned} \tag{4.14}$$

Equation 4.14 calculates the induced steady state probability generating function in terms of the steady state probability generating functions of the input traffic processes. Since the input traffic processes are assumed independent, then the steady state moment generating function of the total number of arrivals is the product of the individual steady state moment generating functions.

The induced transition probability generating function can be calculated in terms of the transition probability generating functions of the input traffic processes by the following equation:

$$\sum_{i=0}^{N} \sum_{l=-i}^{N-i} s^i t^l \pi^*_W(i) W^*(i, i+l) = \prod_{i=1}^{N} [A_i + B_i t + C_i s + D_i s t^{-1}] \tag{4.15}$$

where:

$$A_i = \sum_{(x,y) \in F, (x',y') \in F'} \pi_i(x,y) Q_i((x,y),(x',y')) \tag{4.16}$$

$$B_i = \sum_{(x,y) \in F} \pi_i(x,y) Q_i((x,y),(1,j)) \tag{4.17}$$

$$C_i = \pi_i(1,j) Q_i((1,j),(1,j)) \tag{4.18}$$

$$D_i = \sum_{(x',y') \in F'} \pi_i(1,j)_i Q_i((1,j)(x',y')) \tag{4.19}$$

where $F = \{(x,y) \neq (1,j)\}$ and $F' = \{(x',y') \neq (1,j)\}$. It takes roughly $4N^2$ calculations to get the coefficients of $s^i t^l$. Also, since the input traffic processes are assumed independent, then the steady state moment generating function of state transition of the

N arrival sources is equal to the product of the individual state transition moment generating functions. A_i is the transition probability that source i is idle in the current time slot given that it was idle in the previous time slot. B_i is the transition probability that source i is busy in the current time slot given that it was idle in the previous time slot. C_i is the transition probability that source i is busy in the current time slot given that it was busy in the previous time slot. D_i is the transition probability that source i is idle in the current time slot given that it was busy in the previous time slot.

Now, by dividing the coefficients in equation (4.15) by $\pi^*_W(i)$ in equation (4.14), we get the transition probabilities $W^*(i, i+l)$ of the matrix W^*.

The coefficients A_i, B_i, C_i, and D_i characterize the traffic arrival process driving queue j and originated from input line i. If the input traffic sources are identical, $W^*(i, i')$ will reduce to an equation found in [29]. Once W^* is constructed, the steady state probabilities, $\pi^*(k, n)$, of the queue driven by the aggregated process can be obtained by numerically solving the linear system of equations $\underline{\pi^*}P = \underline{\pi^*}$. The size of this system is $(N+1)(M+1)$. This numerical approach is much more efficient than the one in [13] which requires $(2d)^N$ operations for the calculation of W^*.

4.4 The Case of Multiplexed, Uncorrelated Traffic

In this section, cells belonging to a burst are assumed to be routed independently from other cells in the same burst. This is the case of uncorrelated (random) traffic where the input to a switch is an output of previous multiplexing stage. The speed of the sources of the multiplexing stage are assumed to be close which causes that adjacent cells in a burst are belonging to different destinations. The aim of this section is to compare two cases. The first case is where each arriving cell is routed independently from other arriving cells in the same port and in the second case each arriving burst is routed independently from other arriving bursts as in the previous section.

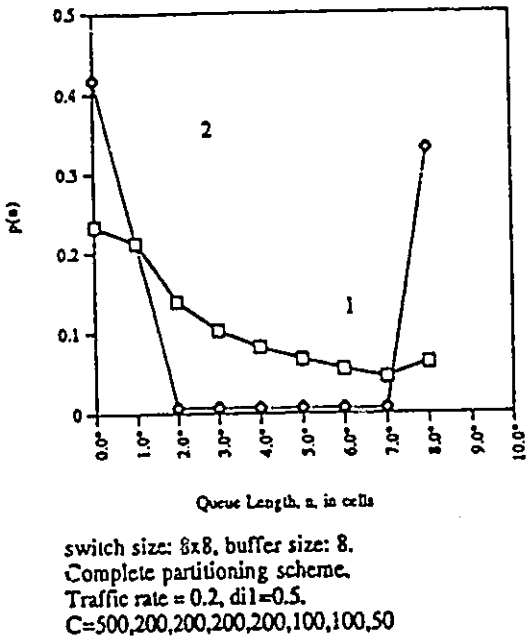

Figure 4.7: Queue length distribution for the uncorrelated case label 1 and the correlated case label 2.

To analyze the first case, the following changes are needed in the previous section:

$$W(\underline{w^a}, \underline{w^b}) = \prod_{i=1}^{N} Q_i((x_i^a, y_i^a), (x_i^b, y_i^b)) \tag{4.20}$$

where for $1 \leq j, k \leq d$,

$$Q_i((1,j),(1,j)) = (1-\alpha_i)d_{ij} \tag{4.21}$$

$$Q_i((1,j),(0,j)) = \alpha_i \tag{4.22}$$

$$Q_i((1,j),(1,y)) = (1-\alpha_i)d_{iy},\ y \neq j \tag{4.23}$$

$$Q_i((0,j),(0,j)) = 1-\beta_i \tag{4.24}$$

$$Q_i((0,j),(1,k)) = \beta_i d_{ik} \tag{4.25}$$

Notice that, 4.21 and 4.23 are modified.

Figure 4.7 shows the queue length distribution for the correlated and the uncorrelated traffic. In Figure 4.8, the cell loss probability is shown under correlated and uncorrelated traffic.

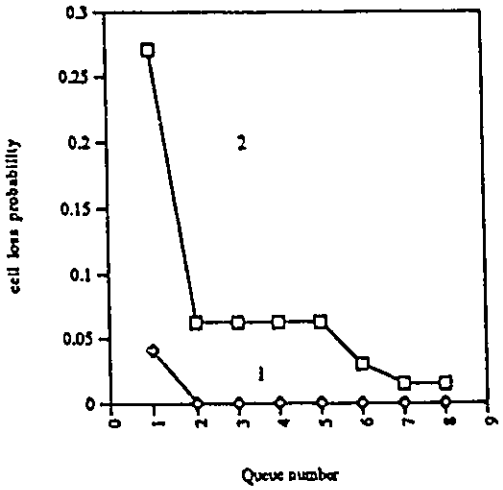

Figure 4.8: Cell loss probability for the uncorrelated case label 1 and the correlated case label 2. The switch size is 8×8 and each number in the x-axis represent an output queue

4.5 Algorithm Validation

In Table 4.1, the error between the exact and the approximate results is shown for different values of β/α and $1/\alpha$. The error is defined by

$$error = \sum_{i=0}^{M} \left(\frac{\pi^*(i) - \pi(i)}{\pi(i)}\right)^2 \pi(i)$$

Where $\pi(i)$ and $\pi^*(i)$ are the steady state distribution of the queue obtained by the exact and the approximate analysis, respectively. In general, we have found that the error of the algorithm depends on the burst length and on the packet rate of the input traffic sources. The general trend is that the algorithm is more accurate for large burst length. Also, as the traffic rate increases, the error starts to increase. An interesting feature of the matrix $P(k,n)$ is that most of its entries are zeros. Also, the structure of the matrix, that describe the aggregated traffic, indicates that the probability that more than two traffic sources change their states in the next time slot is very small. This gives the matrix a structure where the entries of the main diagonal and the other two or three secondary diagonals are very small.

β/α	$1/\alpha = 10$	20	30	50	70	90	200
0.25	0.0	0.0	0.0	0.0	0.0	0.0	0.0
0.5	0.00002	0.0	0.0	0.0	0.0	0.0	0.0
1	0.0004	0.00016	0.00011	0.00011	0.00012	0.00014	0.00017
2	0.0038	0.0015	0.001	0.0009	0.001	0.001	0.0013
4	0.017	0.006	0.004	0.003	0.0033	0.004	0.005
5	0.024		0.005	0.0038	0.0043	0.0048	
8	0.0427		0.0093	0.0058	0.0064	0.0074	

Table 4.1: The error (five decimal points) for a 2×2 switch and $M = 10$.

(Figure 4.9) compares the cell loss probability obtained by simulation with QNAP simulation package and by approximate analysis for a switch size of 8×8. The simulation models the assumptions of the switch model.

Figures 4.10 and 4.11 show the mean cell delay and buffer throughput versus buffer size. The two curves in each graph represent results obtained by applying approximate and exact analysis. The exact analysis was obtained by solving the large linear system of equations $\underline{\pi}P = \underline{\pi}$. We tried switch sizes of only 2×2 and 4×2. The limitation on storage capacity was the reason for choosing small switch sizes. In both cases, the results show a good approximation. The linear system of equations was solved using a DEC station for switch sizes 2×2, 4×4, and 8×8 and using an IBM 3090 mainframe for switch sizes 16×16 and 32×32. This linear system of equations was solved using the Gauss-Seidl method. The analysis shows that the trend of the error is inversely proportional to the traffic mean burst length and proportional to the traffic load.

Figure 4.12 plots the decreasing cumulative probability distribution , $Pr\{$queue length $>$ L$\}$. We notice that the tail of the distribution obtained from approximate analysis is higher than that of the exact analysis. This is true for a certain range of the parameters α_i and β_i. This result is of interest since it implies that the approximate analysis overestimates (on the safe side) the probability that the queue length is greater than a specific length, compared with the actual probability.

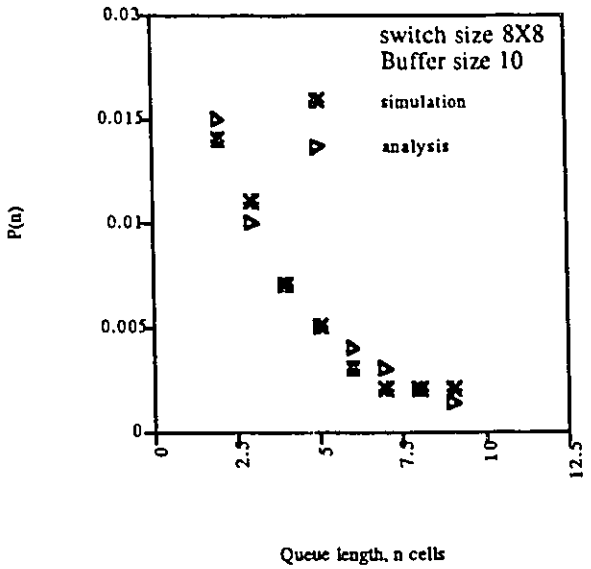

Figure 4.9: Cell loss probability obtained by simulation and analysis for an 8×8 switch with a buffer size of 10.

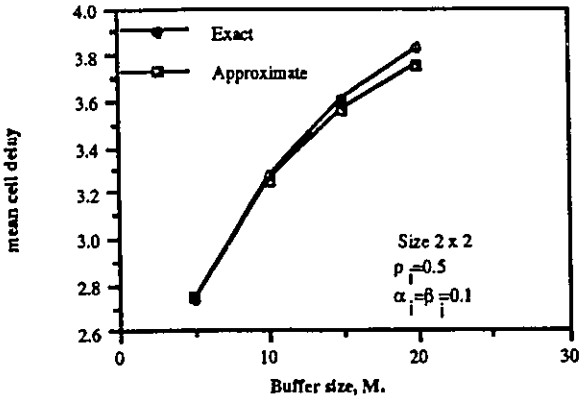

Figure 4.10: Mean cell delay vs. buffer size, M.

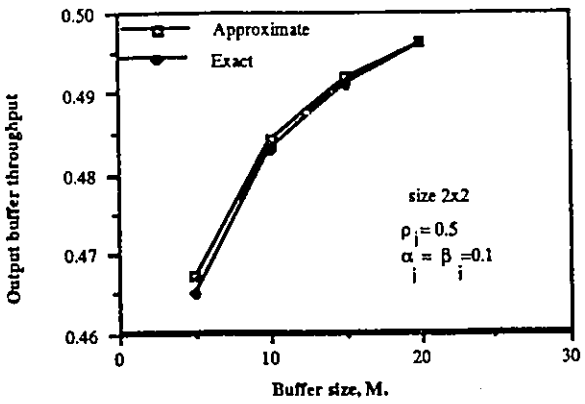

Figure 4.11: Buffer throughput vs. buffer size, M.

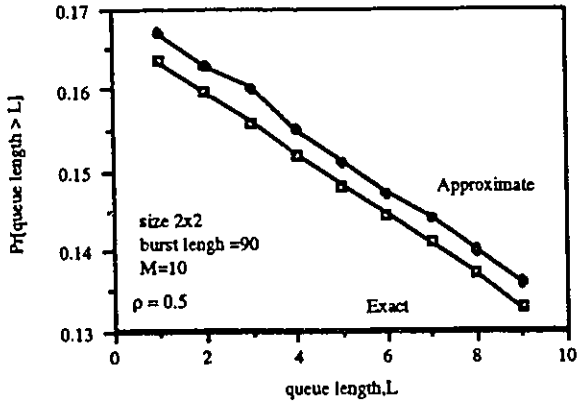

Figure 4.12: Queue length decreasing cumulated distribution.

4.6 ATM Multiplexer

The function of an ATM multiplexer is to merge the incoming streams of packets into one high-speed stream by using a buffer with a FIFO discipline. A statistical multiplexer is an important component in a packet network. Usually the input traffic to an access switch is fed to it by an ATM multiplexer. The traffics from several customers are statistically multiplexed and fed to an input line of an access switch. If the speed of the input lines are close, then the packets at the output are most likely to be uncorrelated (adjacent cells are coming from different sources). If the traffic sources are a mixture of high-speed and low-speed traffic, then the low-speed packets at the output are far apart while the high-speed packets are close.

An ATM multiplexer will provide four classes of services at the ATM adaptation layer (AAL) [51]. Each class is different from the other by providing different QoS (bound on the end-to-end delay for example).

The analysis of an ATM multiplexer can be obtained in this chapter by either setting the routing probabilities, say to buffer 1, $d_{i1} = 1$ for all i, or by setting the number of output lines $d = 1$. It is to be noted that now the aggregation method gives exact results, as compared to the case of a switch ($d > 1$).

4.7 Switch Performance

The performance of ATM switches is measured by the cell loss probability and the mean cell delay. The cell loss probability is defined as the ratio between the expected (mean) number of lost cells and the expected total number of arrivals and can be obtained as in [13]by:

$$P_{loss} = \frac{\sum_k \sum_n [max(n-1,0) + k - M]^+ \pi^*(k,n)}{\sum_k \sum_n k\pi^*(k,n)} \tag{4.26}$$

The mean cell delay is defined to be mean delay among those cells which enter the buffer and this may also be calculated as in [13]. The expected number of cells which

enter the buffer per time slot is

$$C_E = \sum_k \sum_n min\{k, M-n+1\}\pi^*(k,n) \tag{4.27}$$

The expected number of those cells which enter the buffer wait exactly r slots is

$$C_r = \sum_{n=0}^{r+1} \sum_{k=r+1-n'}^{N} \pi^*(k,n) \tag{4.28}$$

where $n' = max(0, n-1)$. The probability that a cell which enters the buffer is delayed exactly r slots before transmission (i.e., the delay distribution) is $P_r = C_r/C_E$. The expected delay is

$$D = \sum_{r=1}^{M} rP_r \tag{4.29}$$

The queue length distribution, $\pi^*(n)$, can be easily found from $\pi^*(k,n)$. The throughput of the buffer is $1 - \pi^*(0)$

4.8 Numerical results

Equiprobable routing is assumed in the following graphs. Figure 4.13 plots the cell loss probability against buffer size, M, for different switch sizes. The parameters of the arrival process are set such that $\rho_i = 0.5$ and $r_b(i) = 5, i = 1, \cdots, N/2$ and $\rho_i = 0.1$ and $r_b(i) = 4, i = N/2+1, \cdots, N$. The graph shows a similar tendency as that noticed in analyzing an output-buffered packet switch with random traffic; the cell loss probability is higher for a larger switch size. The second observation is that, as the switch size increases, the curves of the cell loss probability become closer. The cell loss probability is seen to decrease exponentially as the buffer size increases.

Figures 4.14 and 4.15 are plotted to study the effect of the burstiness index (correlation) of IBP on switch performance. The switch size was 16 × 16 and the buffer size was 50. We notice that for a given traffic load both mean cell delay and cell loss probability increase with the burstiness index. The graphs show that mean cell delay and the cell loss probability increase with traffic load (in these graphs $\rho_i = 0.1$ and $r_b(i) = 10, i = N/2+1, \cdots, N$).

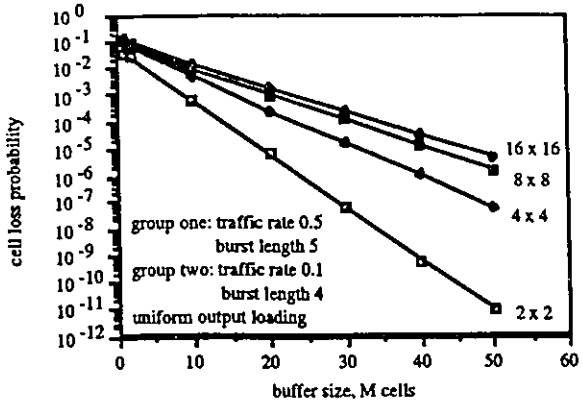

Figure 4.13: Cell loss probability vs. buffer size, M, for different switch sizes.

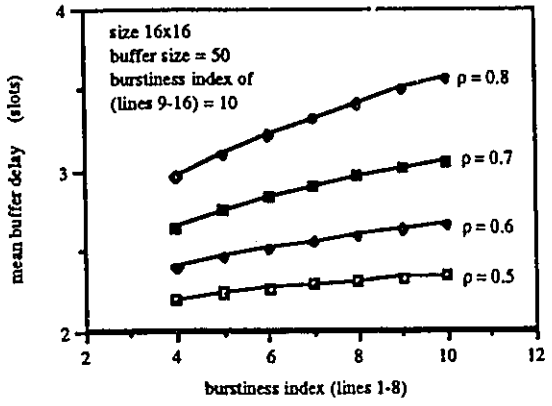

Figure 4.14: Mean cell delay vs. burstiness index (correlation) for different traffic loads.

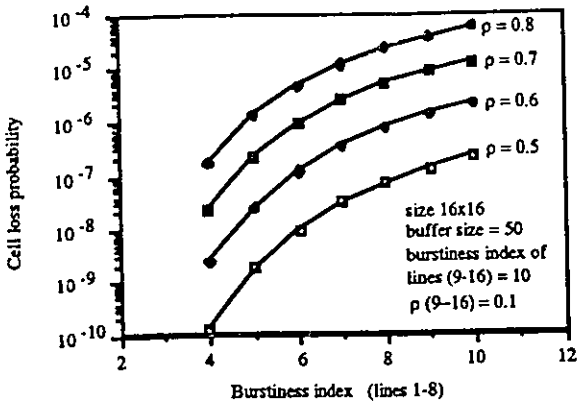

Figure 4.15: Cell loss probability vs. burstiness index (correlation) for different traffic loads.

4.8.1 Effect of Traffic Imbalance (nonuniform traffic)

The model we have presented in this chapter is general. Many parameters can be changed, for example, the distribution of the traffic rates at the input lines, the routing probabilities, and the burst length. Some traffic patterns are of interest in the literature, for example, the bi-group imbalance [39], point-to-point / uniform traffic pattern, and hot spot traffic [58].

The bi-group traffic pattern can be input imbalance or output imbalance. In input imbalance, the input lines are divided into two groups with size N_1, N_2 where $N_1+N_2 = N$. Also, the sum of the total traffic load at buffer 1 is kept a constant. The traffic rates in each group are uniformly distributed, but are different from group 1 to group 2.

The numerical results show that the cell loss probability is slightly improved when the ratio of the traffic rates between the two groups increases (Figure 4.16).

In output imbalance, the traffic rates at the input lines are uniform, but the routing probabilities are changed between the two groups. The numerical results show that the cell loss probability increases when the routing probability of group 1 is increased (Figure 4.17). This is because more traffic is routed to the output buffer.

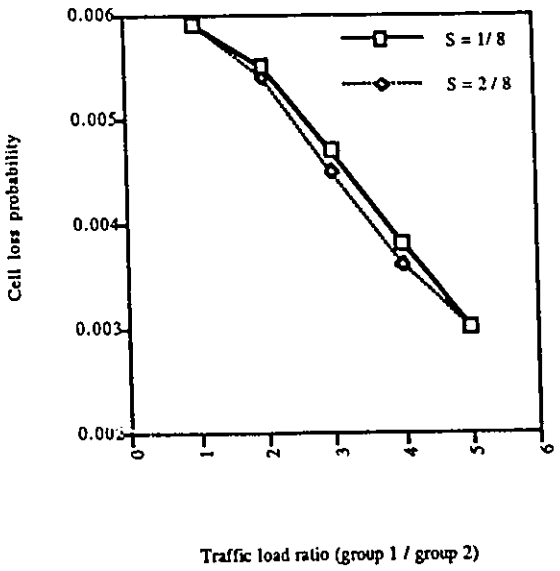

Figure 4.16: Bi-group input imbalance.

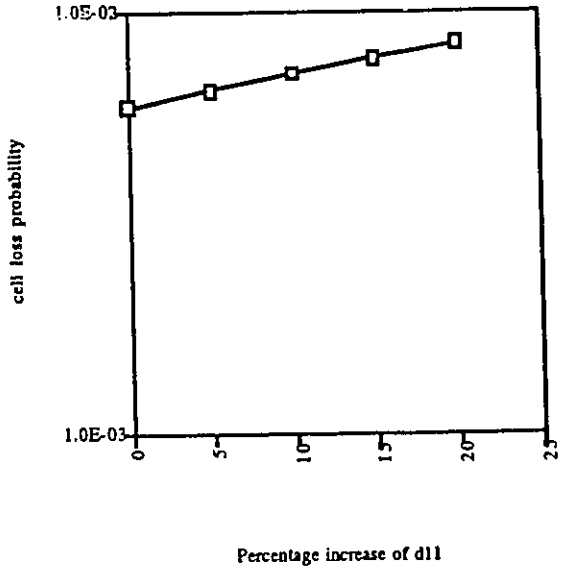

Figure 4.17: Bi-group output imbalance.

4.9 Analysis of a completely partitioned buffer switch with speedup constraints

An ATM switch with output buffers is known to have an optimum performance, however it requires the switch fabric to handle N cells at a time slot (i.e., speed of N). For practical reasons, the switch fabric may operate $L \leq N$ times the speed of the input/output links. In this section, we consider a completely partitioned buffer switch with speedup constraints. The switch fabric can transfer $1 \leq L \leq N$ cells in one time slot, speedup constraint of L.

The main contribution of this analysis, is to study the effect of speedup constraint on switch performance and the effect of traffic imbalances on the speedup constraint.

4.9.1 Numerical Analysis

Let the number of cells in a time slot routed to the same output concentrator module and before they are concentrated be $0 \leq k_b \leq N$. We notice that the transition matrix associated with$k$ is W^* which is as calculated in a previous section. The number of cells in a time slot reached to the output buffer after the speedin up be $0 \leq k_a \leq L$, where L is the speedup factor. The transition matrix, V^*, of the aggregated traffic just *after the speeding up* can be obtained from W^* by setting:

for $i, j = 0, ..., L-1$

$$V^*(i,j) = W^*(i,j) \tag{4.30}$$

$$V^*(L,j) = \frac{\sum_{i>L-1} \pi^*(i) W^*(i,j)}{\sum_{i>L-1} \pi^*(i)} \tag{4.31}$$

$$V^*(i,L) = \sum_{j>L-1} W^*(i,j) \tag{4.32}$$

$$V^*(L,L) = \frac{\sum_{i>L-1} \pi^*(i) \sum_{j>L-1} W^*(i,j)}{\sum_{i>L-1} \pi^*(i)} \tag{4.33}$$

Once V^* is constructed, the steady state probabilities, $\pi^*(k_a, n)$, of the queue driven by the aggregated process can be obtained by numerically solving the linear system of equations $\underline{\pi^*} P = \underline{\pi^*}$. The size of this system is $(L+1)(M+1)$.

4.9.2 Switch Performance

The cell loss probability can be obtained by:

$$P_{loss} = 1 - \frac{C_1 - C_2}{C_3} \tag{4.34}$$

The cell loss probability only in the concentrator(a module performing speedup) is:

$$P_{loss}(duetospeedup) = 1 - \frac{C_1}{C_3} \tag{4.35}$$

where C_1 is the expected number of cells destined to output j. C_2 is the expected number of cell loss due only to finite buffer. C_3 is the expected number of arrivals at the switch. C_3 equals the traffic load. $C_1 = \sum_k \sum_n k\pi^*(k,n)$ and $C_2 = \sum_k \sum_n [max(n-1,0) + k - M]^+ \pi^*(k,n)$.

4.9.3 Numerical Results

(Figures 4.19 and 4.20) are plotted to study the effect of the burstiness index of IBP on switch performance. The switch size is 16 × 16 and the buffer size M is 50. The concentration ratio $N : L$ is 16:4. $\rho_i = 0.1$ and $r_b(i) = 10, i = N/2 + 1, \cdots, N$. The routing probabilities, $d_{ij} = 1/N$. We notice that, for a given traffic load both mean cell delay and cell loss probability increase with the burstiness index. The graphs show that mean cell delay and the cell loss probability increase with traffic load.

(Figure 4.21) shows the mean cell delay vs. traffic rate for different concentration ratios. The switch size is 16x16 and buffer size $M = 75$. The graph shows that a speedup factor of $L > 3$ guarantees an optimum mean cell delay performance. This means that $L = 4$ is sufficient. Similar results were obtained in [9] for uniform random traffic.

To study the effect of the speedup constraints on the cell loss probability, the following cases are considered: The traffic load is kept constant and equal to 0.7. In Case 1 (homogeneous loading) group one (input lines 1-8) has individual traffic rate 0.7, individual burst length equal to 10, and uniform output loading equal to $1/N$. Group two (input lines 9-16) has similar parameters as those of group one. Case 2 (imbalanced traffic rates) as in case 1, but the individual traffic rate in group one increased to 0.8 and that of group

two decreased to 0.6 (the traffic load still equals 0.7). The results obtained from these different cases are the same for the above parameters. Different switch sizes are tried.

The cell loss probability in the concentrator is shown in (Figure 4.22) to decrease as a function of L. The total cell loss probability (in the concentrator and the output buffer) reaches its maximum limit for concentrator size equal to 7-8. This result indicates that operating the output-buffered ATM switch with $L = 7 - 8$ is sufficient to obtain the cell loss probability performance obtained by operating the switch with a full speedup factor.

4.9.4 Effect of Point-to-point/Uniform Traffic

The point-to-point/uniform traffic pattern represents an imbalanced traffic pattern where one input port directs its whole traffic to a particular output port while the traffic of other input ports is uniformly routed. The existence of such traffic pattern affects the size of the concentrator slightly because only one concentrator output will be occupied by the point-to-point connection while the others are free to serve the other connections.

4.9.5 Effect of Hot Spot Traffic

The hot spot traffic occurs when all the input ports direct more traffic to a particular output port (Hot spot), while the other output ports receive cells uniformly. Figure 4.18 shows the cell loss probability as more traffic is directed to the hot spot. Hot spot traffic affects the required size of the concentrator. For a worst case example, let the routing probability to the hot spot be 1, then the concentrator size needed to carry all this traffic is N.

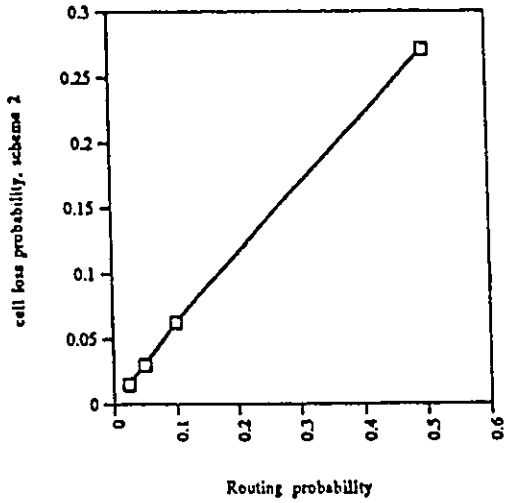

Figure 4.18: Cell loss probability for the Hot spot port

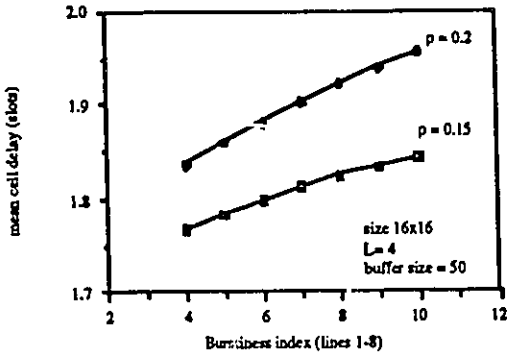

Figure 4.19: Mean cell delay vs. burstiness index for different traffic loads.

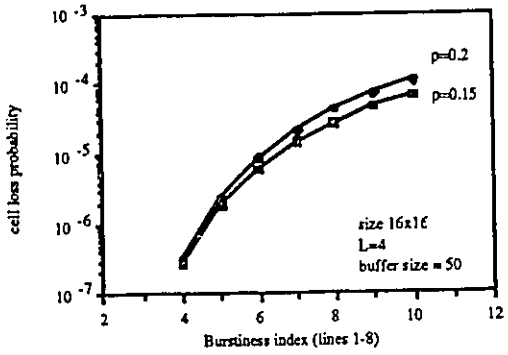

Figure 4.20: Cell loss probability in the buffer vs. burstiness index for different traffic loads.

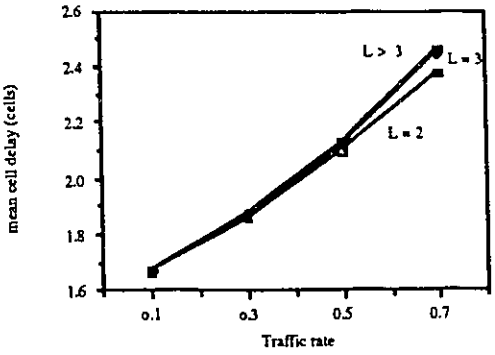

Figure 4.21: Mean cell delay vs. traffic rate for different speedup, L. Switch size 16×16 and buffer size of 75.

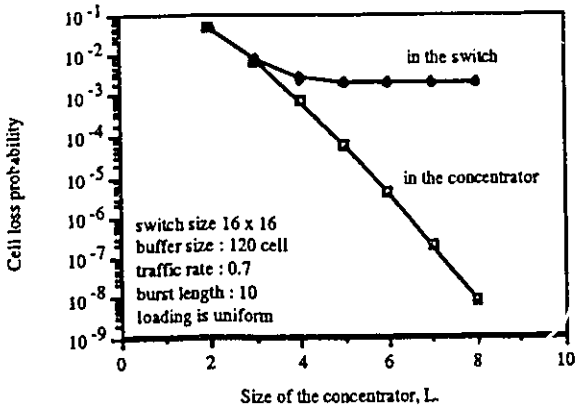

Figure 4.22: Cell loss probability with speedup.

Chapter 5

Transient and Busy Period Analysis of an ATM Switch

In the first part of this chapter the transient analysis of an output-buffered ATM switch is studied. This study is important because an ATM switch will be loaded by several bursty traffic sources. Although the probability of having a large number of bursts arriving simultaneously at the output buffer is very small, this rare event can still occur. The occurance of this rare situation will cause severe cell losses in a short time which can be unacceptable for some services such as video. Calculating the mean time until buffer overflow can provide the switch designer with the frequency and expected time for this rare event to occur.

The second part of this chapter characterizes the output traffic of the output buffer which is the departure process of X/D/1/M queueing system, where X is the aggregated arrival process which is a N+1-state MC, D is the deterministic distribution, and M is the queue size.

5.1 Transient Analysis: Mean Time to buffer overflow

In this section, we investigate the transient analysis of the switch by considering the mean transient time to buffer overflow. It is the mean time to buffer overflow from the time the switch is turned on.

The blocking states are those states $(k,n) \in S^*$ where $S^* = \{(n,k) : 0 \leq n \leq M, 0 \leq k \leq N\}$ to which a transition from another state will cause cell loss. A transition from state (k,n) to state (k',n') will cause cell loss if $max(n-1,0)+k > M$. Transitions to nonblocking states do not cause cell loss. Let $\gamma(k,n)$ be the mean time to reach queue length q given that the state of the switch was (k,n). The vector $\underline{\gamma}(k,n)$, $0 \leq k \leq N$ and $0 \leq n < q$ satisfies [65]:

$$(I-Q)\underline{\gamma} = \underline{-1} \tag{5.1}$$

where Q is a submatrix of P with $0 \leq k \leq N$ and $0 \leq n < q$ as shown in (Figure 5.1) and I is the identity matrix. This system of equations is solved by using the Gauss-Jordan method.

The mean time, τ_q, to reach queue length q can, then, be calculated as follows:

$$\tau_q = \frac{\sum \gamma(k,n)\pi^*(k,n)}{\sum \pi^*(k,n)} \tag{5.2}$$

where the sum is taken for $0 \leq k \leq N$ and $0 \leq n < q$. $\pi^*(k,n)$ are the steady state probabilities of the state (k,n). The mean time to reach blocking can be calculated by setting $q = M$.

5.1.1 Transient Analysis: Numerical Results

Table 5.1 shows the increase in the mean time to buffer overflow for different buffer sizes $M = 30, 40, 50, 60$. The switch size is 8×8. The burst length of the input traffic is 10 for lines 1-4 and 5 for lines 5-8. The traffic rate is 0.15 for lines 1-4 and 0.1 for the input lines 5-8. $d_{ij} = 1/N$ (i.e., equiprobable routing).

The mean time to reach queue length q is shown in Figure 5.2. The results show that the time taken to increase the queue length by one increases exponentially.

In Table 5.2, the effect of the burst length, for fixed traffic load, on the mean time to reach blocking is shown. As expected, the results show that the longer the burst length, the smaller the time to reach blocking is.

Figure 5.3 shows the mean time to reach blocking vs. switch size. It shows that as the switch size increases from 2×2 to 32×32, the mean time to blocking drops from 60,000 time slots to about 12,000 time slots.

buffer size, M cells	τ_M (slots)
30	406464.7
40	2553248.0
50	15066980.0
60	85455330.0

Table 5.1: Mean time to reach blocking vs. buffer size for a 8×8 switch and traffic rate of 0.15.

burst length (cells)	τ_M (slots)
5	5.38467 E9
6	1.318106 E9
7	4.905218 E8
8	2.357097 E8
9	1.339332 E8
10	8.545533 E7

Table 5.2: Mean time to reach blocking vs. burst length for a 8×8 switch. $M = 60$. Burst length for lines 5-8 equals to 5. The traffic rate is 0.1

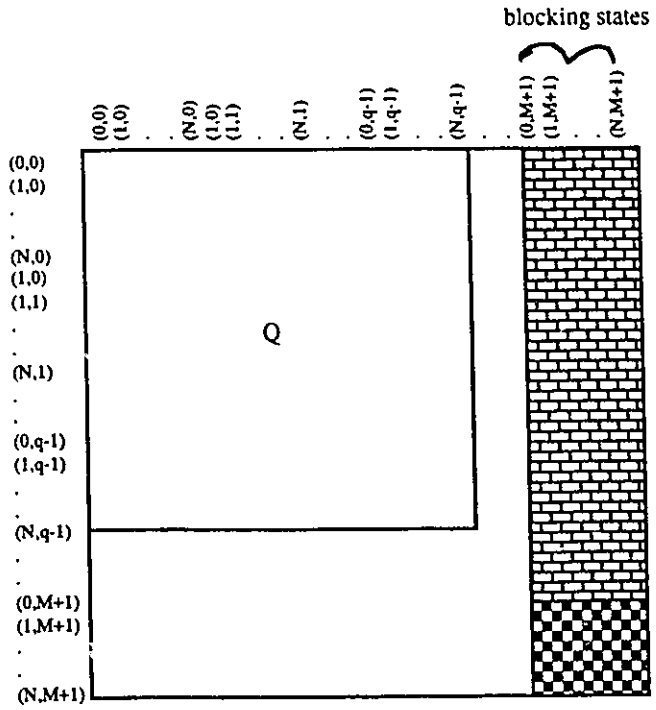

Figure 5.1: The transition matrices P and Q as defined to calculate the mean time to reach queue length q.

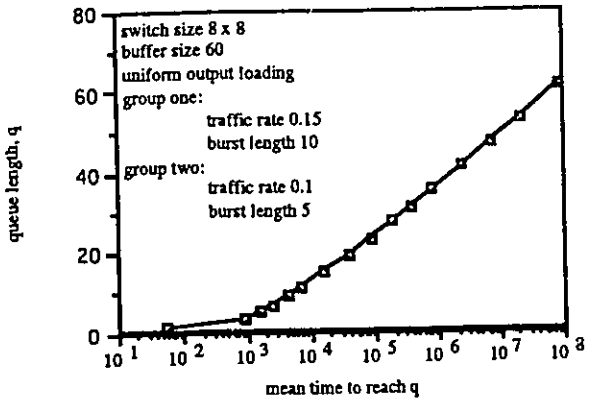

Figure 5.2: Queue length, q vs. mean time to reach q.

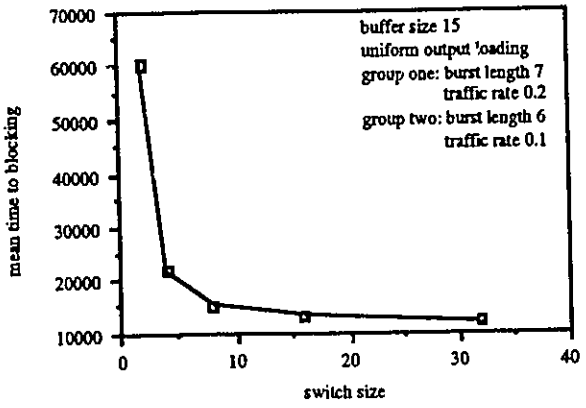

Figure 5.3: Mean time to blocking vs. switch size.

5.2 Busy and Idle Period Analysis

In this part, we derive analytically the actual distribution of the busy and idle periods for each output buffer of an $N \times d$ access switch with correlated imbalanced traffic [45].

Recent studies have dealt with the cell loss behavior and on characterizing the output traffic of the ATM switch [46] under uniform loading. The importance of characterizing the output traffic of the ATM switch stems from the point that a network access switch is usually connected to other nodal switches in the broadband network. Thus the output traffic of the access switch is the input traffic to a nodal switch connected to it. Another importance of such a study is that an ATM switch may consist of several stages of switching elements as in a buffered Banyan switching architecture. In such a switching network, the output traffic of a switching element is the input traffic to the next switching element in the next stage.

5.2.1 Busy Period Analysis: Actual Analysis

By definition, an idle state is a state $s_o = (k, 0) \in S_o$ where $S_o = \{(k, n); 0 \leq k \leq N, n = 0\}$ is a subspace of the state space, S, describing the switch. $S = \{(k, n); 0 \leq k \leq N, 0 \leq n \leq M\}$, where n is the number of cells in the tagged output queue and k is the state of the aggregated traffic source whose destination is the tagged output buffer. From the definition, an idle state is a state where the number of cells in the output buffer equals to zero regardless of the state of the aggregated input traffic process. A busy state, by definition, $s' = (k, n) \in S - S_o, n \neq 0$, is a state where the buffer is not empty regardless of the state of the aggregated input traffic process.

We identify all states $s_1 \in S_1$ into which a one-step transition is possible from the idle states, $s_o \in S_o$. From the definition, $S_1 = \{(k, n); 0 \leq n \leq N, 0 \leq k \leq N\}$ is a subspace of the busy state space $S - S_o$. We notice that the idle state $(0, 0)$ cannot be reached in one-step transition by any busy state. The converse is also true that no busy

state can be reached from the idle state $(0,0)$ in a single transition.

Let us define $f_m^{s_o}(s)$ to be the probability that it takes exactly m steps to reach the idle state s_o given that the initial state is s. The values of $f_m^{s_o}(s)$ can be found iteratively by the following relation [47]:

$$f_m^{s_o}(s) = \begin{cases} \sum_{s' \in S - S_o} f_{m-1}^{s_o}(s') p(s, s') & , m = 2, 3, \ldots \\ p(s, s_o) & , m = 1, s \in S - S_o \end{cases} \tag{5.3}$$

where $p(s, s')$ is the one-step transition probability as calculated in the transition matrix P.

The conditional probability, $B(m|s_o)$, that the length of the busy period is m given that the busy period starts from the idle state s_o is:

$$B(m|s_o) = \sum_{s_1 \in S_1} \sum_{s_i \in S_o} f_m^{s_i}(s_1) \frac{p(s_o, s_1)}{1 - \sum_{s \in S_o - \{(0,0)\}} p(s_o, s)} \tag{5.4}$$

The unconditional distribution, $B(m)$, of the busy period can be calculated , by summing over all idle states in S_o from which a busy period can be initiated, as follows.

$$B(m) = \sum_{s_o \in S_o} B(m|s_o) \frac{\pi_W^*(s_o)}{\sum_{s \in S_o - \{(0,0)\}} \pi_W^*(s)} \tag{5.5}$$

The idle period distribution can be calculated by the same procedure. We notice that the idle period comes from the idle state $(0,0)$ and the contribution of the other idle states (i.e.,(k,0)) could be negligible. Thus the idle period distribution is geometric with a mean $I = \frac{1}{1 - p(0,0)}$. The throughput of the output line is $\gamma = \frac{B}{(B+I)}$. The cell loss probability can,then, be calculated from knowing the mean busy and idle periods as follows

$$P_{loss} = \frac{TL_j - \gamma}{TL_j} \tag{5.6}$$

where $TL_j = \sum_{i=1}^{N} \rho_i d_{ij}$ is the total traffic load at queue j. The cell loss probability can be also calculated from the steady state probability of the idle states by $P_{loss} = \frac{TL_j - (1 - \pi^*(0))}{TL_j}$. The throughput $\gamma = 1 - \pi^*(0)$.

5.2.2 Busy Period Analysis: Approximate Geometric Model

The busy period distribution obtained in the actual model is the actual distribution. In the following derivation of the busy period distribution, both the busy period and the idle period are assumed to have geometrical distributions with mean $1/p$ and $1/q$, respectively. In this model, the state of the output queue is described by two state Markov chain; busy state and idle state. The transition probability from the busy state to the idle state equals to p. And the transition probability from the idle state to the busy state equals to q. The values of p and q can be calculated as follows:

$$p = \frac{\sum_{s \in S - S_o} \pi(s) \sum_{s_o \in S_o} p(s, s_o)}{\sum_{s \in S - S_o} \pi(s)} \tag{5.7}$$

$$q = \frac{\sum_{s_o \in S_o} \pi(s_o) \sum_{s \in S - S_o} p(s_o, s)}{\sum_{s_o \in S_o} \pi(s_o)} \tag{5.8}$$

The busy period distribution is $B(m) = (1-p)^m p$ and the idle period distribution is $I(m) = (1-q)^m q$ for $m = 1, 2, \ldots$.

5.2.3 Busy period: Numerical Results

This analysis extends the analysis of [46] to the case of having nonuniform traffic loading at the input and nonuniform traffic routing at the output. Each new burst will be routed to its destination with a probability $1/N$.

The objective of Figures 5.4 and 5.5 is to compare the busy period distribution obtained from actual and geometrical analysis. It shows that the two-state Markov chain model of the busy period does not adequately approximate the actual busy period distribution (obtained by the actual model).

(Figure 5.6) shows the effect of the mean input burst length on the mean busy period (actual) of the output process. (Figure 5.7) shows that the actual mean busy period increases with the the buffer size.

The square coefficient of variation of the length of the busy period of the output traffic versus the square coefficient of variation of the burst length of the input traffic is

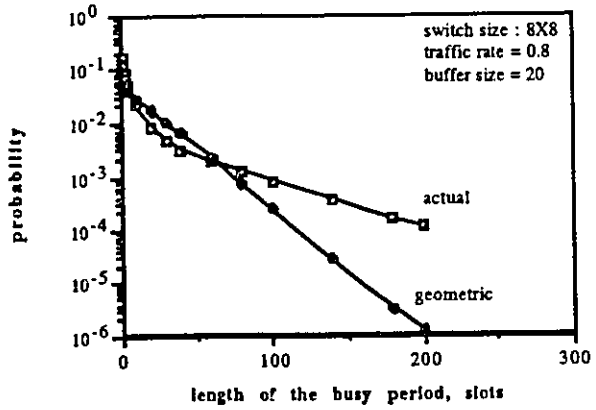

Figure 5.4: Comparison between the actual distribution of the busy period and the two-state model with traffic rate equal to 0.8.

shown in Figure 5.8. It indicates that the output traffic is more bursty than the input traffic. This result is true when we consider the burstiness of the output traffic for all the virtual channels. Actually the burstiness of the output traffic per virtual channel is less than the burstiness of the input traffic for a single virtual channel. The buffer smoothes the traffic per virtual channel.

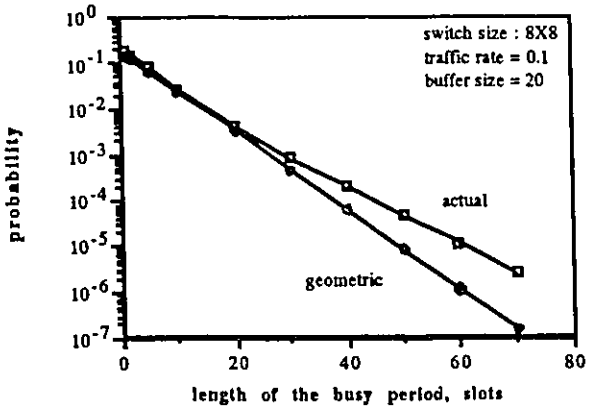

Figure 5.5: Comparison between the actual distribution of the busy period and the two-state model with traffic rate equal to 0.1.

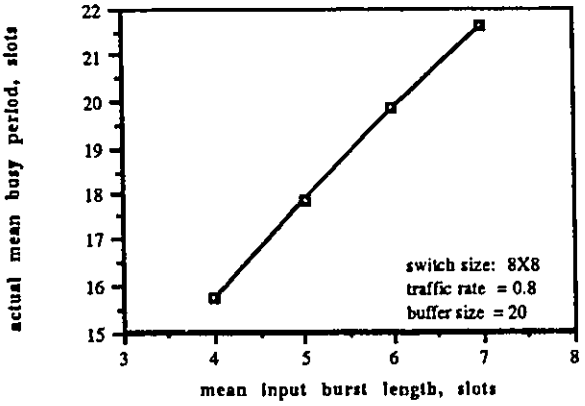

Figure 5.6: The mean busy period(actual) versus the mean input burst length.

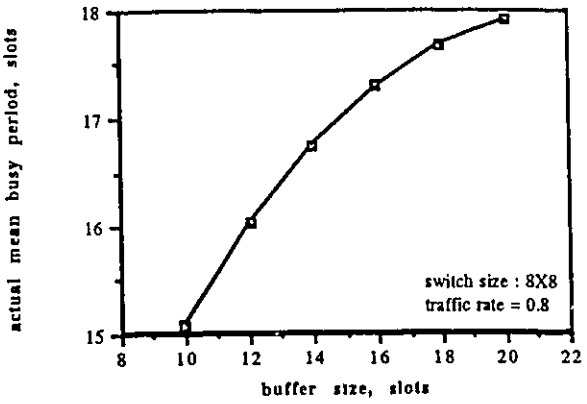

Figure 5.7: The mean busy period(actual) versus the buffer size.

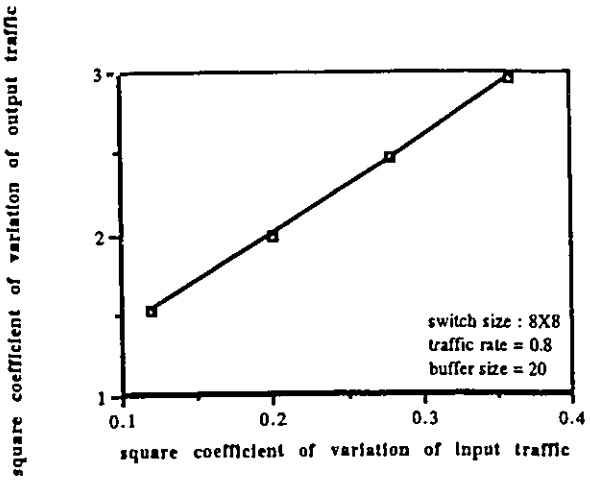

Figure 5.8: The square coefficient of variation of the length of the busy period of the output traffic versus the square coefficient of variation of the burst length of the input traffic.

Chapter 6

Priority Analysis of an ATM Switch with Bursty Traffic

The first part of this chapter considers priority analysis of an ATM switch with complete partitioned buffer. In the next part, we will consider priority in a shared-memory switch.

6.1 Introduction

The need of traffic priorities in a packet network can occur in different cases. For a particular service (for example video), the user can mark a cell as a high-priority if this cell is important to him and he can mark a cell as low-priority if it is not so important. For example, in the two-layer DCT coding scheme of a video source, after getting the coded cells, these cells will be identified into two layers. The first layer corresponds to cells with high variance; these are the high-priority cells. The second layer is the low-priority cells which are the cells with low content of information. This priority provision will help an access buffer to discard low-priority cells whenever the buffer overflows. Also, video packets cannot allow large delays.

In another service such as electronic mail, packets can tolerate long delays but not high cell loss probabilities [55].

6.2 Priorities in ATM Networks

An ATM cell has a cell loss priority bit in its header. This priority bit at the ATM level allows the designer to identify the cell either as a high-priority cell or a low-priority cell.

Different traffic classes are provided by the ATM Adaptation Layer (AAL). Each class can have different QoS parameters. For example, different cell loss probability and different end-to-end delay. If a priority protocol is proposed to account for all these traffic classes, then this protocol could be complex. In high-speed networks, simple but efficient protocols are preferred. In this direction, it has been suggested to decouple cell loss priority and delay priority. In this chapter, the emphasis is on decoupling the delay and the cell loss priorities.

The delay classes are provided at the connection set-up time and remain the same for the whole duration of the connection.

Priority in an ATM network can be:

Delay priority: Cells in a queue are served such that the high priority (HP) cells have small queueing delays at the expense of low-priority (LP) cells. In long distance connections, the queueing delay has small contribution to the end-to-end transfer delay because of the large transmission delay. On the other hand, the delay variation introduced by the buffers along a connection could be of significance to some traffic.

Loss Priority: In loss priorities, the HP cells are served in a way to reduce their cell loss priority at the expense of LP cells. The following loss priority mechanisms are proposed [54]: In the push-out mechanism, a HP cell arriving to a full buffer can replace an LP cell which is queued in the buffer. This means that HP cells can be out of sequence, which requires some buffer management scheme. The other proposed loss priority mechanism is the threshold scheme [54]. In this scheme, a threshold queue length, T, is assumed. Whenever the queue length, both of HP and LP cells, exceeds this threshold value, the buffer will accept more HP cells only. The new LP cells arriving at the queue are lost. In other words, the buffer is partitioned into two parts; one part (of size T) is shared between LP and HP cells and one part is dedicated to HP cells only.

This chapter is organized as follows: Section 6.3 is devoted to a completely partitioned buffer switch with priorities. Section 6.4 is devoted to a shared-buffer switch with priorities .

6.3 Switch with Completely Partitioned Output Buffer and Two Priority Classes of Traffic

6.3.1 Switch Model

The model of the switch is as shown in Figure 6.1. A cell arriving at an output buffer of the switch is assumed to be a HP cell or a LP cell. The interest here is in the service-priority scheme (delay-priority scheme). HP cells will be served before LP cells even if they arrive later than LP cells. LP cells will be blocked until the last arrival of HP cell is served.

6.3.2 Model Analysis

Numerical Solution of the HP Traffic

The aggregate source that drives the output buffer may consist of up to k cells in a time slot. In a time slot, we assume that the amount of HP and LP traffics are $k_H = pk$ and $k_L = (1-p)k$, respectively, where p is a constant and has the range $0 \leq p \leq 1$. The state space of the HP queue driven by k_H is (k_H, n_H), where n_H is the HP queue length. The transition probabilities of the HP traffic follow the procedure of the LP traffic as will be described below and by replacing $1-p$ by p. The state space of k_H is $\{0, 1, 2, \ldots, N\}$.

The solution of this system follows the same procedure as described in Chapter 4, since HP traffic does not care for the presence of LP traffic.

Numerical Solution of the LP Traffic

The state describing the LP queue driven by the LP aggregated source is (k_L, n_L, r) where r is the state of the HP queue; $r = 0$, when the HP queue is empty (idle) and $r = 1$, when the HP queue is not empty (busy). The state space of k_L is $\{0, 1, 2, \ldots, N\}$. The transition probabilities of r can be obtained by looking at the state space of the HP queue, identifying the idle states and the busy states and then reducing this matrix into a matrix R of size 2×2. The entries of R are the transition probabilities between $r = 0$ and $r = 1$.

The transition probabilities for the LP aggregated traffic, $W_L^*(k_L' = i'/k_L = i)$ can be found using the following procedure:

- step 1: Calculate the transition matrix W^*.
- step 2: Find

  $\pi_W^*(k), k = 0, 1, \ldots, N$, by solving $\pi_W^* W^* = \pi_W^*$
- step 3: Calculate

  $$prob(k_L = i/k = j) = \begin{pmatrix} j \\ i \end{pmatrix} (1-p)^i p^{j-i} \text{ for } i < j, j = 0, 1, \ldots, N.$$
- step 4: calculate the steady state probabilities,

  $\pi_L^*(k_L = i) = \sum_{j=0}^{j=N} \pi_W^*(k = j) prob(k_L = i/k = j)$
- step 5: Calculate

  $prob(k = j/k_L = i) = \pi_W^*(k = j) \frac{prob(k_L = i/k = j)}{\pi^*(k_L = i)}$ for $i < j, j = 0, 1, \ldots, N$.
- step 6: Calculate the transition probabilities:

  $W_L^*(k_L' = i'/k_L = i) =$

  $\sum_{j' > i'} \sum_{j > i} prob(k_L' = i'/k' = j') W^*(j'/j) prob(k = j/k_L = i)$

Step 6 makes use of the relation (see for example [52])

$$P(A, B, C, D) = P(A/B, C, D) P(B/C, D) P(C/D) p(D)$$

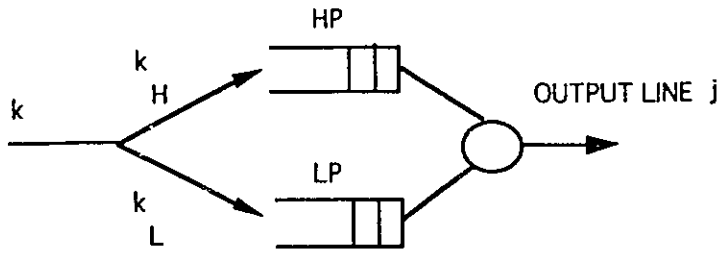

Figure 6.1: Switch Model.

The transition probabilities $P_L[(k_L, n_L, r); (k_L', n_L', r')]$ can know be computed from

$$P_L[(k_L, n_L, r); (k_L', n_L', r')] = P_L[(k_L, n_L); (k_L', n_L')]R(r, r') \tag{6.1}$$

The transition probabilities $P_L[(k_L, n_L); (k_L', n_L')]$ can also be computed following the procedure in Chapter 4.

The steady state of the LP queue can now be found by solving the system of equations $\pi P_L = \pi$.

Numerical results

Figure 6.2 shows that the cell loss probability increases both for the HP and the LP traffic as the rate of the HP traffic increases. Figure 6.3 shows the mean cell delay of the LP traffic decreases while it increases for the HP traffic as the rate of the HP traffic increases. This is because the load of the LP traffic decreases. The effect of the burst length on the performance can be seen in Figures 6.4 and 6.5. Figure 6.4 shows that the burst length has no effect on the cell loss probability of the LP traffic. But from Figure 6.5, the burst length affect the mean cell delay.

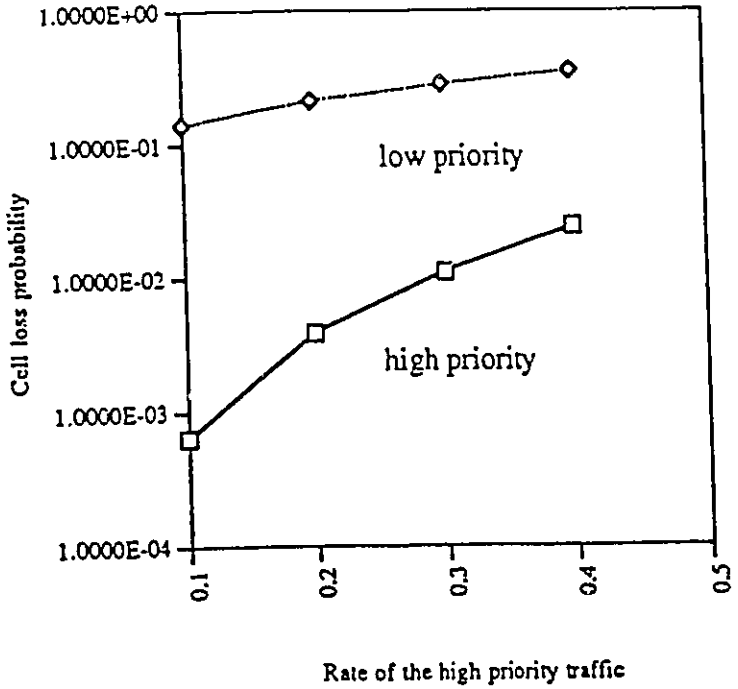

Figure 6.2: Cell loss probability vs. the rate of the HP traffic .

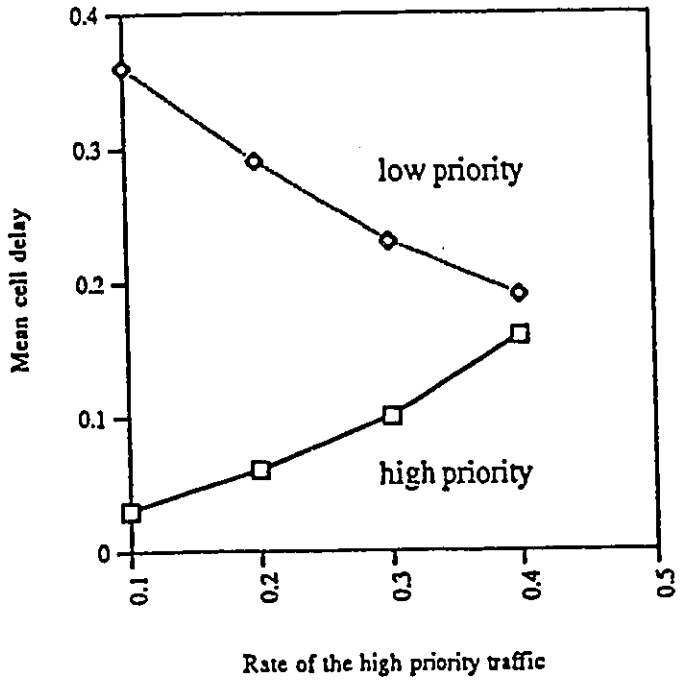

Figure 6.3: Mean cell delay vs therate of HP traffic.

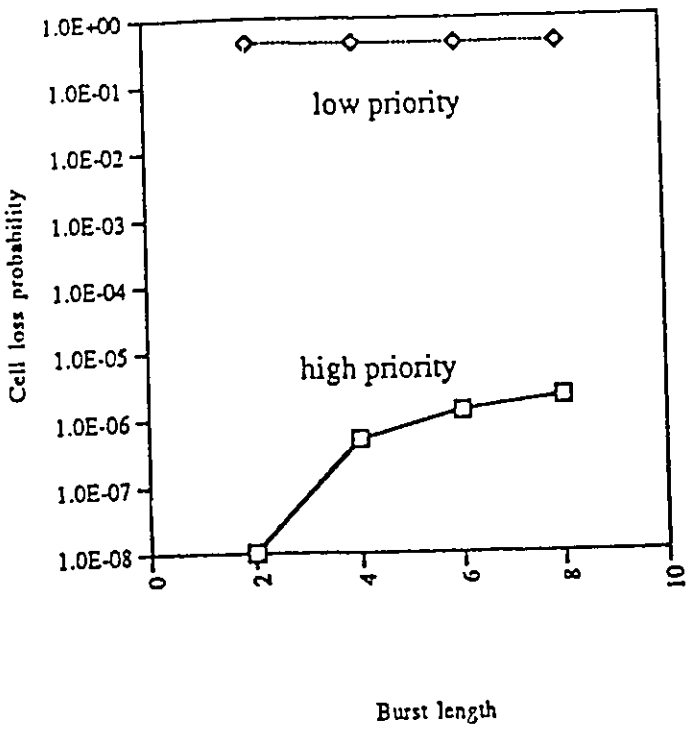

Figure 6.4: Cell loss probability vs. burst length.

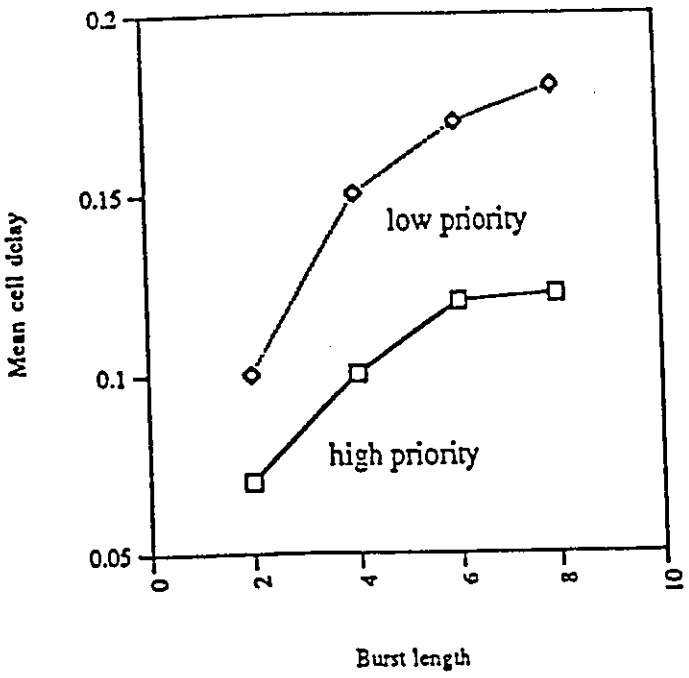

Figure 6.5: Mean cell delay vs. burst length.

6.4 Priorities in a Shared Buffer ATM Switch

In the following, we give the model and its analysis of a shared-buffer switch with two priorities. The analysis of the shared buffer without priorities is summarized in Appendix A which is based on [13].

An arrival cell in a time slot to the switch is considered of higher priority (HP) with probability p or of lower priority (LP) with probability $1-p$. A LP cell in queue i will be served after all HP cells in that queue have been served. A HP cell arriving to a full buffer will replace an existing LP cell. Both LP cells and HP cells share a common buffer of size M. Our approach uses the method in [13] and enhances it to consider priorities as follows. We use the following notation (we follow the notation used in [13]) : n^H is total number of HP cells in the shared buffer, n_i^H is the number of HP cells in the i^{th} queue. k^H is the number of HP cells arrived in a time slot to the shared buffer. n_R^H is the number of HP cells in $N-\{i\}$. k^L is the number of LP cells arrived in a time slot to the shared buffer. The notations with superscript H means high-priority and with superscript L means low-priority. c_i^L and c_R^L are the number of LP cells that arrive at queue i and $N-\{i\}$ respectively, c_N^L is the number of LP cells that enter the whole system without blocking, n_R^L is the number of LP cells in $N-\{i\}$, d_i^L and d_R^L are the number of LP cells to depart from queue i and $N-\{i\}$, respectively. All random variables are considered at time slot t except $n_R^{'H}$, $n_R^{'L}$, and $c_R^{'L}$ which are considered at the time $t+1$.

- Consider only the high-priority traffic class and use the method in [13] to compute

$$Prob\{(k^H, n_i^H, n^H); (k^{'H}, n_i^{'H}, n^{'H})\} \tag{6.2}$$

  From the computation we obtain: $P_{n_R^H}^H(l) = P[l$ HP queues are busy $]$, for $l = 0, 1, \ldots, N-1$ and $R_{n^H,n^{'H}} = P\{n^H; n^{'H}\}$ and r_i which is the transition probability between empty and nonempty states for HP queue i.

- Consider now the low-priority traffic:

The following algorithm generates the transition probability matrix of the LP traffic in queue i:

Algorithm

first: augment the state space $(k^L, n_i^L, n^L, r_i, n^H)$,

where

$$r_i = \begin{cases} 0, & \text{if no HP cells in queue i} \\ 1, & \text{otherwise} \end{cases}$$

second: generate the transition probabilities for

$n^H = 0, 1, \ldots, M$;

$n^L = 0, 1, \ldots, M - n^H$; $n_i^L = 0, 1, \ldots, n^L$.

- step 0: initialize $P[(k^L, n_i^L, n^L, r_i, n^H); (k'^L, n_i'^L, n'^L, r_i', n'^H)] = 0$
- step 1: $c_i^L = n_i'^L + d_i^L - n_i^L$

  where

$$d_i^L = \begin{cases} 1, & \text{if } n_i^L \neq 0 \text{ and } r_i = 0 \\ 0, & \text{otherwise} \end{cases}$$

- step 2:

  For $d_R^L = 1, 2, \ldots, (N-1, n_R^L)$

  Begin

  $c_R^L = n_R'^L + d_R^L - n_R^L$

  if $c_i^L + c_R^L = k^L$ (no LP cells are blocked) then

$$P[(k^L, n_i^L, n^L, r_i, n^H); (k'^L, n_i'^L, n'^L, r_i', n'^H)] =$$

$$P[(k^L, n_i^L, n^L, r_i, n^H); (k'^L, n_i'^L, n'^L, r_i', n'^H)] +$$

$$R_{k^L k'^L} R_{n^H n'^H} R_{r_i r_i'}$$

$$P_{n_R^L}^L(d_R)[\binom{k_L}{c_i^L} b_i^{c_i^L} (1 - b_i)^{k_L - c_i^L}] \qquad (6.3)$$

if $c_i^L + c_R^L < k^L$ (LP cells are blocked) then

$c_N^L = c_i^L + c_R^L$

$$P[(k^L, n_i^L, n^L, r_i, n^H); (k'^L, n_i'^L, n'^L, r_i', n'^H)] =$$
$$P[(k^L, n_i^L, n^L, r_i, n^H); (k'^L, n_i'^L, n'^L, r_i', n'^H)] +$$
$$R_{k^L k'^L} R_{n^H n'^H} R_{r_i r_i'} P_{n_R^L}^L(d_R) \tag{6.4}$$

$$\sum_{k_i^L=c_i^L}^{k^L} \left[\binom{k_L}{k_i^L} b_i^{k_i^L} (1-b_i)^{k^L - k_i^L} \frac{\binom{k_i^L}{c_i^L}\binom{k_L - k_i^L}{c_R^L}}{\binom{k_L}{c_N^L}} \right]$$

End;

where $P_{n_R^L}^L(d_R)$ =Prob.$\{d_R$ LP cells will depart from the queues $N-\{i\}\}$ =Prob.$\{d_R$ LP cells are at the head of some queues in $N-\{i\}$ and there are no HP cells in these queues$\}$ and is given by:

$$P_{n_R^L}^L(d_R) = \sum_{l=0}^{N-1} \sum_{i=0}^{n_R^L} P_1 P_2 P_{n_R^H}^H(l) \tag{6.5}$$

where

$P_1 = Prob.\{i$ LP cells falling in queues $N-\{i\}$ that do not have HP cells, given that there are l queues that have HP cells $\}$

$P_2 = \{d_R$ queues will be occupied by LP cells only given that i LP cells were offered to $N-1-l$ queues$\}$

Then by [66] and with reference to Figure 6.6

$P_2 = Prob.\{n-m$ slots are occupied when r balls are thrown into n slots $\}$

$= \{d_R$ queues will be occupied by LP cells only given that i LP cells were offered to $N-1-l$ queues$\}$

$$= \binom{n}{m} \sum_{v=0}^{n-m} (-1)^v \binom{n-m}{v} (1 - \tfrac{m+v}{n})^r$$

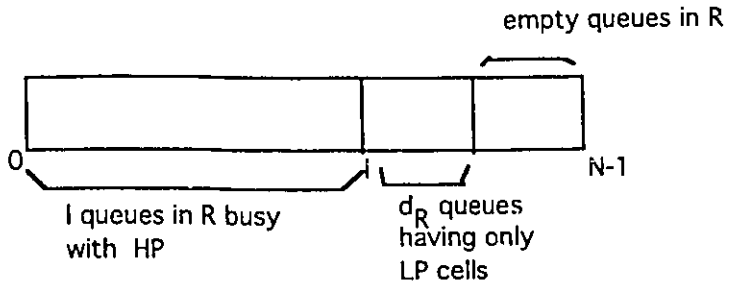

Figure 6.6: The LP cells as distributed in the remaining queues.

$$= \begin{pmatrix} N-1-l \\ d_R \end{pmatrix} \sum_{v=o}^{d_R} (-1)^v \begin{pmatrix} d_R \\ v \end{pmatrix} (1 - \tfrac{N-1-l-d_R+v}{N-1-l})^i$$

This gives the following expression

$P^L_{n^L_R}(d_R)$ =Prob.$\{d_R$ LP cells will depart from the queues $N - \{i\}\}$ =

Prob.$\{d_R$ LP cells are at the head of some queues in $N - \{i\}$ and there are no HP cells in these queues$\}$ and is given by:

$$P^L_{n^L_R}(d_R) = \sum_{l=0}^{N-1} \sum_{i=0}^{n^L_R} \begin{pmatrix} n^L_R \\ i \end{pmatrix} (\frac{l}{N-1})^{n^L_R - i} (\frac{N-1-l}{N-1})^i \begin{pmatrix} N-1-l \\ N-1-l-d_R \end{pmatrix} (\frac{d_R}{N-1-l})^i \sum_{m=0}^{d_R} \begin{pmatrix} d_R \\ m \end{pmatrix} (-1)^m (\frac{d_R - m}{d_R})^i P^H_{n^H_R}(l) \quad (6.6)$$

Once the transition probability matrix is set up, the steady state probability vector is obtained numerically. The state space is of size $(N+1)\sum_{i=0}^{M}(M-i+1)(M-i+2)$. Which is higher than the state space of the shared buffer without priorities which is $\frac{(N+1)(M+1)(M+2)}{2}$.

The overall algorithm is as follows:

```
Algorithm

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- step 1: Calculate the probability distribution of busy queues with LP cells at the head-of-line, $P^L_{n^L_R}(l)$ for $l = 0, 1, \ldots, N-1$ from Equation 7.6.

- step 2: Generate the transition probability matrix for each queue i using the above algorithm and calculate the steady state distribution $\pi_i(k^L, n_i^L, n^L, r_i, n^H)$ using the overrelaxation method

- step 3: Calculate the individual and the global queue length distribution as given by:

$$\pi_i(n_i^L) = \sum_{k^L=0}^{N} \sum_{n^L=n_i^L}^{M} \sum_{n^H=0}^{M-n^L} \sum_{r_i=0}^{1} \pi_i(k^L, n_i^L, n^L, r_i, n^H) \tag{6.7}$$

and

$$\pi_i(n^L) = \sum_{k^L=0}^{N} \sum_{n_i^L=0}^{n^L} \sum_{r_i=0}^{1} \sum_{n^H=0}^{M-n^L} \pi_i(k^L, n_i^L, n^L, r_i, n^H) \tag{6.8}$$

- step 4: Compute the steady-state measures - such as cell loss probability for HP and LP cells, etc.

6.4.1 Numerical Results

The following graphs are for a switch size of 4 × 4. The switch size is reasonable from the practical point of view for a local ATM or a small backbone ATM environment (e.g., OCRInet in Ottawa). The incoming traffic to the switch is divided equally between LP and HP traffic. The burst length of the traffic at input ports 1 and 2 is 390 cells and at input ports 3 and 4 is 156 cells. The total traffic rate at the input of the buffer is 0.8 (0.2 at each input line).

Figure 6.7 shows the queue length distribution for the high-priority and low priority traffic. During the time when the HP buffer is empty, the server is busy serving the LP cells if any. The probability of empty buffer is expected to decrease when the traffic rate gets larger. The graph shows that the low-priority cells wait in the queue more than the high-priority cells and this is because of the priority service discipline.

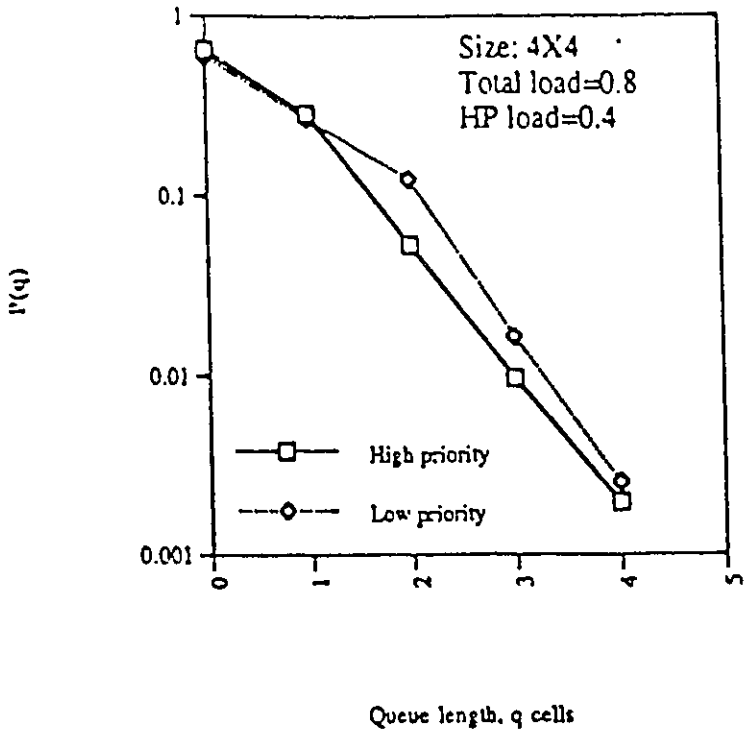

Figure 6.7: Queue length distribution (log scale) for the high-priority traffic and low-priority traffic.

Figure 6.8 shows the cell loss probability for different buffer sizes for the high-priority, low-priority traffic, and the total traffic. We calculated for a buffer size up to 10 cells because of computer memory allocation. This size of buffer gives 10^{-7} HP loss rate and 10^{-3} LP loss rate. Extrapolating the results obtained, we find that buffer of 30 cells gives total cell loss probability of less than 10^{-9} for both HP and LP traffic.

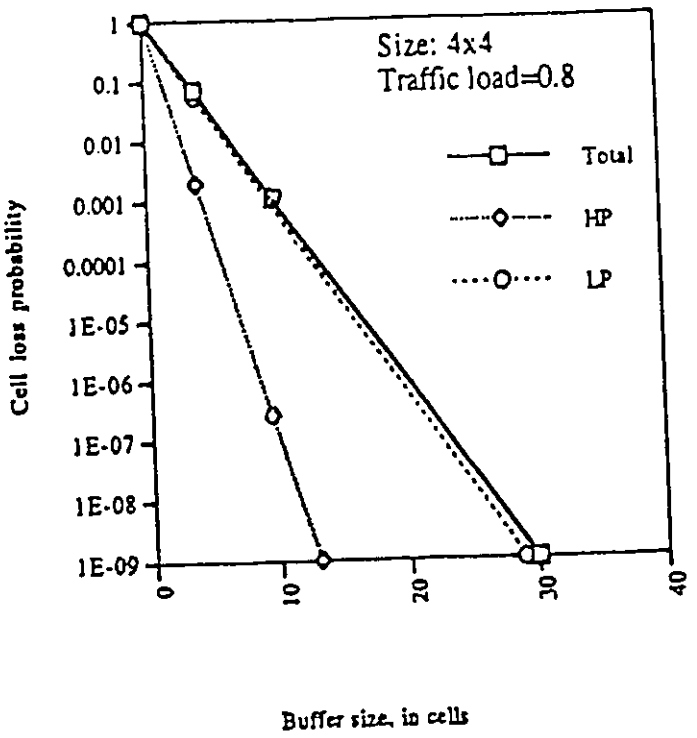

Figure 6.8: Cell loss probability (log scale) versus the buffer size for the high-priority and low-priority traffic and total traffic.

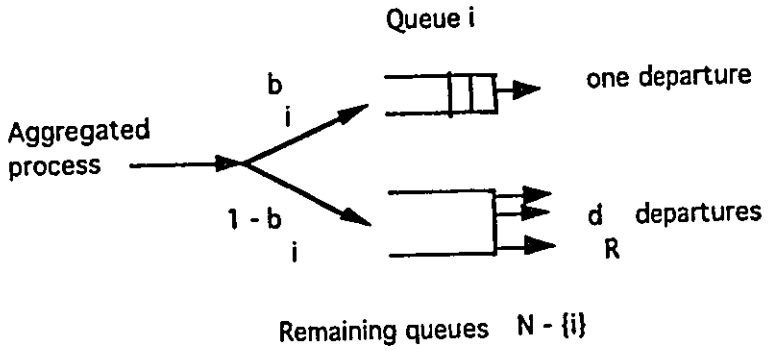

Figure 6.9: Queueing model of subsystem i.

Chapter 7

Conclusions

In this thesis, two classes of output-buffered ATM switches were considered and analytically studied, namely the ones of the completely partitioned and the completely shared output buffer. Interest in these classes was motivated by the practical importance and advantages of output-buffered ATM switches, although input-buffered ones have also been used in some ATM switch implementations.

The switches of those classes were considered with or without input traffic priorities. The priority issue is very important for switch manufacturers, as there are applications which require different switch priority treatment of different data streams. For example, Constant-Bit-Rate (CBR) vs Variable-Bit-Rate(VBR) traffic, real-time vs non-real-time traffic, or Intra (I) Frame MPEG-coded cells vs cells of Predicted(P) and Bidirectionally-Predicted(B) Frames.

The switch model considered was general:

- We assumed imbalanced traffic loading at both the inputs, since this is what is happening in practice, and the outputs, since output 'hot-spots' may appear.
- Correlation of input cells was permitted, in the sense that all cells of an input burst are directed to the same output port, since an ATM switch may also be used as a LAN, connecting for-example a video-codec output to a particular display device. The study with correlated traffic also presents a worst-case analysis for the uncorrelated traffic problem.

- The analytical model assumed finite buffer size, which is the real situation.
- The input traffic pattern in each switch port was modelled by an Interrupted Bernoulli Process (IBP), since that process captures real-ATM-traffic features such as burstiness, ON/OFF activity periods and cell correlation.

The analytical study of such an ATM Switch requires the numerical solution of a high-dimensionality problem. To decrease the numerical complexity of this problem, we have first provided a method where input-traffic destined for a given output port is aggregated into a single stochastic process. The aggregation method is not new in the literature, but we have provided a novel approach for an efficient aggregation based on generating functions. Our approach results in a numerical complexity of the order of $(N+1)(M+1)$, as compared with the one of [12] given as $(2N)^N(M+1)$. Following this aggregation of input sources, the output buffer, driven now by the aggregated source, was studied and its performance measures were obtained.

It is to be noted that this aggregation method gives an approximate analysis. It becomes, however, an exact analysis for the case of an ATM multiplexer, i.e., a switch with only one output port. To establish the validity of this analytical approximation, we compared its results with the ones of the exact analysis, for small switch cases since the exact method becomes numerically intractable for larger switch sizes. We have also compared with simulation results. We have found that the method gives good results for dimensioning the buffer of small to moderate switches. It should be noted here that small switches (2x2 or 3x3) are used, for example, not only as Local-ATM ones but also as ATM backbone switches for OCRInet and CANARIE, the Ottawa and National ATM research testbeds , respectively. The approximation error was found to decrease with decreasing traffic rate or increasing burst lengths. Thus for high-burst, low-intensity traffic, the method is very appealing.

The numerical complexity of the analytical solution was higher in the case of a shared-output-buffer switch, as compared with the completely partitioned-buffer case. Also the complexity significantly increased when cell-priority was modelled and results

obtained. With todays computer workstations, however, the analytical approach, for small to moderate switch sizes, can give useful performance results much faster than computer simulation. Using larger memories and faster computers, for example with the newest 1200 MIPS DEC Alpha chip, the method could be efficiently used for larger switch sizes as well.

Efficient buffer dimensioning of a switch for a given cell-loss probability, say 10^{-9}, for various cases (partitioned or shared buffer, with or without cell-priorities, with or without speedup constraints) is a most important engineering contribution of this thesis. Dimensioning results were given for both the steady-state analysis, where the steady-state probability of cell-loss is the measure of interest, and the transient switch analysis, where the mean-time-to-buffer-congestion is important. The latter analysis is another major contribution of this thesis.

Beside dimensioning the switch buffer with our efficient analytical method, several results about the behaviour of the switch were obtained. In Chapter 4, studying the case of completely partitioned buffer, the results show that the 'hot spot' traffic routing greatly affects the switch performance as compared to uniform output loading, with regards to cell loss probability and mean cell delay which both get worse. As noticed in other studies, the burst length greatly affects the cell loss probability and the mean cell delay. This is because more correlated cells are routed to the same output port.

In Chapter 4, the completely partitioned buffer with speedup constraints was also studied. The results show that a speedup constraint of 4 gives almost the same performance (cell loss probability and mean cell delay) as compared to the complete speedup, N (the switch size). This result may be used for decreasing the implementation complexity of the switch.

In Chapter 5, the transient analysis of the output buffer was studied. This study is important because it indicates to the switch designer the mean-time-to-buffer-overflow (a reliability measure). This can be used for buffer dimensioning. We have also found that the mean-time-to-buffer-overflow decreases as the switch size increases, for a constant load per output line. This interesting result is due to the following. As the switch size

increases, the variance of the interarrival time of the input traffic at an output buffer gets higher. This causes a higher probability of having several cells arriving at the buffer at the same time slot and thus decreases the mean-time-to-buffer-overflow. Also the mean-time-to-buffer-overflow decreases as the switch burst length increases, and it increases as the switch buffer increases.

The characterization (busy and idle periods) of the output traffic process from such switches was also studied. The results show that the output traffic process cannot be adequately modeled by a two-state Markov chain. This result is important for performance evaluation of a multistage switch in which the output traffic of a stage is the input traffic to the following stage. It also provides an alternative method for calculating the cell loss probability in the output buffer without calculating the steady state probability of the queue. The results showed that the burstiness (measured by either the burst length or by the squared coefficient of variation) of the output process is higher than the burstiness of the input process.

The lossy period of the output line is the duration of time in which there are cell losses in every time slot. The lossless period, on the other hand, is the period of time in which there are no cell losses in its time slots. The results showed that the lossy period does not change if the buffer size is increased, while the lossless period increases with the buffer size.

In Chapter 6, the above buffering techniques were studied in a switch with two priority classes of traffic. The low-priority cells are served only when no high-priority cells are in the queue. We first analyzed the case of a completely partitioned output buffer. We then analyzed a completely shared output buffer switch. The results showed that the burst length has no effect on the cell loss probability of the low-priority traffic. But it negatively affects the mean cell delay of the low-priority traffic. On the other hand, the burst length negatively affects the high-priority traffic with regards to both cell loss probability and mean cell delay.

Suggestions for Further Research

- The numerical complexity of the analytical method increases when the switch size

and/or the buffer size increase. We suggest for further research to look into techniques allowing further decreasing the numerical complexity of the problem.

- To consider a shared-buffer switch with traffic priority classes and with priority threshold. The priority scheme, considered in the thesis, can be relaxed by adding a threshold, T, at the HP buffer. In this case, LP cells will be served as long as the number of HP cells in the buffer is less than or equal to the threshold T.

- To consider individual arrival processes modeled by the Markov Modulated Bernouli Process (MMBP). The MMBP captures correlated interarrival times but could complicate the analysis.

- To consider applying the IBP or MMBP to analyze a switch with both input buffers and output buffers. The previously reported analyses of such a switch assumed Bernoulli arrival traffic.

Appendix A

Analysis of a Shared Buffer ATM Switch [13]

We summarize here the approach of [13], analyzing a shared-buffer switch without priorities. The shared memory is decomposed into N subsystems, one for each output queue. The queue under the study is the *ith* queue. The remaining queues will be denoted by the symbol $N - \{i\}$ or simply R. In order to study queue i in isolation, we need to know how many cells are in $N - \{i\}$. The model of a subsystem is as shown in (Figure A.1). The state of a subsystem i is described by the vector (k, n_i, n), where k is the number of cells arriving in a time slot to the shared buffer (the state of the aggregated source), n_i is the number of cells in the *ith* queue, and n is the total number of cells in the entire buffer. Each queue can occupy the total memory size, M cells, (complete sharing). The total number of states in the subsystem is $\frac{(N+1)(M+1)(M+2)}{2}$.

In order to calculate the transition from state (k, n_i, n) to state (k', n_i', n'), we need to find the number of cells that depart from the queue $N-\{i\}$. From the state description (k, n_i, n), we only know that there are $n_R = n - n_i$ cells in $N - \{i\}$. We do not know how these cells are distributed over the $N - \{i\}$ queues. For instance, all the cells could be in the same queue. In this case only one cell will depart at the end of the next time slot. The probability distribution of l busy queues in $N - \{i\}$ will be denoted by $P_{n_R}(l)$. The distribution used for $P_{n_R}(l)$ is the one that maximizes the entropy function

$\sum_{l=1}^{N-1} P_{x_i}(l) ln(P_{x_i})$ subject to the constraints that the area under the distribution is 1 and that that mean of the distribution is known.

$$P_{n_R}(l) = \frac{e^{-l\delta}}{Z} \tag{A.1}$$

for $l = 1, \ldots, min(N-1, n_R)$ where

$$Z = e^{-\delta} + e^{-2\delta} + \ldots + e^{-min(N-1,n_R)\delta} \tag{A.2}$$

The mean number of cells in the remaining queue is estimated as

$$f_i(n_R, \beta) = (1-\beta) + \beta g_i(n_R) \tag{A.3}$$

. where $0 \leq \beta \leq 1$ and $g_i(n_R)$ is the mean number of non-empty queues in $N - \{i\}$ as calculated by

$$g_i(n_R) = \sum_{l=1, l\neq i}^{N} [1 - (\frac{\sum_{j=1, j\neq i, l}^{N} \rho_j}{\sum_{j=1, j\neq i}^{N} \rho_j})^{n_R}] \tag{A.4}$$

where ρ_j is the average arrival rate to the j^{th} queue.

The algorithm that computes the transition probability from (k, n_i, n) to (k', n_i', n'), is summarized below. We use the following notation: c_i and c_R are the number of cells that arrive at queue i and $N - \{i\}$ respectively, c_N is the number of cells that enter the whole system without blocking, n_R is the number of cells in $N - \{i\}$, d_i and d_R are the number of cells to depart from queue i and $N - \{i\}$ respectively. All random variables are considered at time t except n_R', and c_R' which are considered at the time $t+1$.

Algorithm 1

- step 0: $P[(k, n_i, n); (k', n_i', n')] = 0$
- step 1: $c_i = n_i + d_i - n_i$, where
  $d_i = 1$, if $n_i \neq 0$, or $d_i = 0$, 0therwise.
- step 2: For $d_R = 1, 2, \ldots, Min(N-1, n_R)$

Begin

$c_R = n_R + d_R - n_R$

if $c_i + c_R = k$ (if no cells are blocked) then

$$P[(k,n_i,n);(k',n_i',n')] = P[(k,n_i,n);(k',n_i',n')] + R_{kk'}P_{n_i}(d_R)[\binom{k}{c_i} b_i^{c_i}(1-b_i)^{k-c_i}] \quad \text{(A.5)}$$

if $c_i + c_R < k$ (if cells are blocked) then

$$c_N = c_i + c_R$$

$$P[(k,n_i,n);(k',n_i',n')] = P[(k,n_i,n);(k',n_i',n')] + R_{kk'}P_{n_R}(d_R) \sum_{k_i=c_i}^{k} \binom{k}{k_i} b_i^{k_i}(1-b_i)^{k-k_i} \frac{\binom{k_i}{c_i}\binom{k-k_i}{c_R}}{\binom{k}{c_N}} \quad \text{(A.6)}$$

End;

Once the transition probability matrix, $P[(k,n_i,n);(k',n_i',n')]$, is set up, the steady state probability vector is obtained numerically.

The overall algorithm is as follows:

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Algorithm
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- step 0: $\beta_L^0 = 0$ and $\beta_H^0 = 1$ and s=0
- step 1: s=s+1, $\beta_M^s = (\beta_L^{s-1} + \beta_H^{s-1})/2$ and calculate $f_i^s(n_R, \beta_M^s)$ for $n_R = 1,\ldots,M$ and $i = 1,2,\ldots,N$ using Equation A.3
- step 2: Calculate the probability distribution of busy queues, $P_{n_R}(l)$ as in Equation A.1
- step 3: Generate the transition probability matrix for each queue i using algorithm 1 and solve for the steady state distribution $\pi_i(k,n_i,n)$ using the overrelaxation method

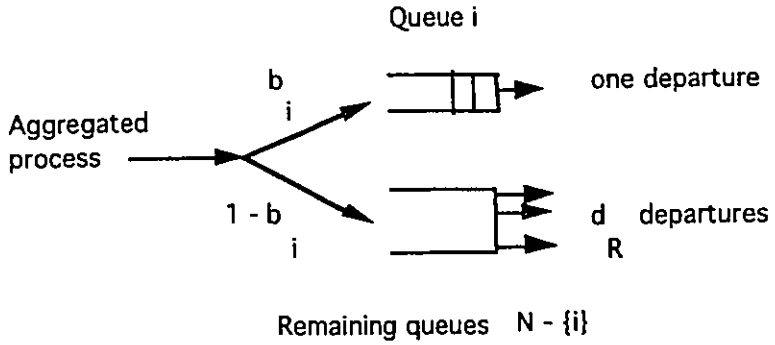

Figure A.1: Queueing model of subsystem i.

- step 4: Calculate E_1 and E_2 as in Equations A.7 and A.8
- step 5: Convergence test:

If $|E_1 - E_2| \leq TOL$ then STOP, else

If $E_1 < E_2$ then set

$$\beta_H^s = \beta_M^s,$$

$$\beta_L^s = \beta_L^{s-1}\text{ , GO TO step 1, else}$$

If $E_1 > E_2$ then set

$$\beta_H^s = \beta_H^{s-1},$$

$$\beta_L^s = \beta_M^s\text{, Go TO step 1}$$

where E_1 and E_2 are the mean number of cells in the total buffer as calculated from the individual queues and from the global queue respectively defined as follows:

$$E_1 = \sum_{i=1}^{N} \sum_{n_i=1}^{M} n_i \pi_i(n_i) \tag{A.7}$$

$$E_2 = \frac{1}{N} \sum_{i=1}^{N} \sum_{n=1}^{M} n \pi_i(n) \tag{A.8}$$

Table A1 shows approximate and simulation results for the queue 1 of an 8×8 switch with buffer size of 8.

n	$P_1(n)$(approx.)	(simulation)
0	.3329	.3264
1	.1993	.1971
2	.0595	.0572
3	.0509	.0480
4	.0501	.0445
5	.0599	.0524
6	.0830	.0821
7	.1067	.1225
8	.0576	.0699

Table A.1: Approximate and simulation results for the queue 1 of an 8×8 switch and $M = 8$ [13, Table 2].

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