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FUZZY-NEURAL TOOL FOR TOPOLOGY EXTRACTION OF RF AND MICROWAVE TRANSISTORS

Ji Limin, B. Eng.,

A thesis submitted to the
Faculty of Graduate and Postdoctoral Studies
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Abstract

Today, the increasing need for advanced high-frequency communication technologies leads to a continuous development of new and more complex models for active devices such as RF and microwave transistors [1]. Parameter extraction for small-signal electrical equivalent circuit modeling has been deeply studied and numerous techniques have been developed. However, it is still difficult to determine all the small-signal model elements with a high degree of certainty.

In this thesis, an efficient tool is presented for transistor model extraction and characterization. Fast and accurate, the adopted technique couples neural networks and fuzzy theory to extract the most suitable small-signal equivalent circuit topology of RF/microwave field effect and heterojunction bipolar transistors. By combining the Fuzzy c-means method [2] and the neural representation of a transistor behavior [3], the small-signal equivalent circuit parameters are efficiently evaluated through a fuzzy-neural network, based on the selection of the most suitable circuit topology of the active device.

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List of Acronyms

ADS	Advanced Design System
ANN	Artificial Neural Networks
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
DC	Direct Current
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GHz	Giga Hertz
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
InP	Indium Phosphide
JFET	Junction Field Effect Transistor
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
RF	Radio Frequency
Si	Silicon

List of Symbols

C_{bep} The coupling between the base-emitter interconnection layer of the heterojunction bipolar transistor

C_{bcp} The coupling between the base-collector interconnection layer of the heterojunction bipolar transistor

$C_{bc'}$ The interconnection capacitance between the base and the collector.

C_{be} The charging of the base-emitter capacitance of the heterojunction bipolar transistor

C_{bc} The effective intrinsic capacitance of the heterojunction bipolar transistor

C_{cep} The coupling between the collector-emitter interconnection layer of the heterojunction bipolar transistor

C_{ds} The drain-to-source capacitance of the field effect transistor

C_{ex} The effective extrinsic capacitance of the heterojunction bipolar transistor

C_{gd} The gate-to-source capacitance of the field effect transistor

C_{gs} The gate-to-source capacitance of the field effect transistor

C_{pds} The parasitic drain-to-source capacitance of the field effect transistor

C_{pgs} The parasitic gate-to-source capacitance of the field effect transistor

C_{pgd} The parasitic gate-to-drain capacitance of the field effect transistor

f The Frequency

g_m: The device transconductance of the field effect transistor

L_d: The drain parasitic inductance of the field effect transistor

L_g: The gate parasitic inductance of the field effect transistor

L_s: The source parasitic inductance of the field effect transistor.

L_b The base parasitic inductance of the heterojunction bipolar transistor

L_c The collector parasitic inductance of the heterojunction bipolar transistor

L_e The emitter parasitic inductance of the heterojunction bipolar transistor

$n+$ The heavily doped semiconductor with donor impurities

R_b The base contact resistance of the heterojunction bipolar transistor

R_{bc} The combined intrinsic and extrinsic base resistance of the heterojunction bipolar transistor

R_{be} The base-emitter resistance of the heterojunction bipolar transistor

R_{bi} The intrinsic base resistance

R_{b2} The metal-semiconductor capacitance of the heterojunction bipolar transistor

R_{c1} The collector resistance of the heterojunction bipolar transistor

R_d : The drain parasitic resistance of the field effect transistor

R_{ds} : The output resistance of the field effect transistor

R_e The extrinsic emitter resistance of the heterojunction bipolar transistor

R_{fd} The differential resistance of the gate-to-drain diodes of the field effect transistor

R_g : The gate parasitic resistance of the field effect transistor

R_{gs} The differential resistance of the gate-to-source of the field effect transistor

R_{gd} The resistor of the feedback capacitance of the field effect transistor

R_s : The source parasitic resistance of the field effect transistor

V_{ds} The DC drain-to-source voltage of the field effect transistor

V_{gs} The DC gate-to-source voltage of the field effect transistor

ω The angular frequency

τ : The transconductance delay.

Chapter 1

INTRODUCTION

This information age is characterized by ever-increasing need for advanced high-frequency communication technologies. Such a trend leads to a continuous development of new and more complex models for active devices such as Field Effect Transistors (FETs) and Heterojunction Bipolar Transistors (HBTs) [1].

FET, either a Junction FET (JFET), a Metal-Oxide Semiconductor FET (MOSFET), a Metal-Semiconductor FET (MESFET) or a High Electron Mobility device (HEMT), is a three-terminal semiconductor with terminals labeled gate, source and drain that acts either as an amplifier or digital switch. The input signal is connected to the gate and the output is taken from either the source or the drain. It is controlled by voltage rather than current. The flow of working current through a semiconductor channel is switched and regulated by the effect of an electric field exerted by electric charge in a region close to the channel called the gate; and used to build integrated circuits such as operational amplifiers. One of the major characteristics of a FET is that it has an extremely high input resistance and therefore, has no loading on previous circuitry.

HBT is a transistor design that is used in GaAs, SiGe, and InP process technologies to provide higher performance than traditional MESFET or CMOS processes.

1.1 Motivation

The work in this thesis concentrates on small signal models of those two types of transistors. Small signal models describe the transistor operation in the linear region. For FET in linear region, a small Gate-Source voltage will produce a linear change in the Drain-Source current. At a certain point, if the Gate-Source voltage is allowed to increase, the Drain-Source current change is no longer linear and the small signal model no longer applies. Similarly, for HBT in active region, the current flowing into the base results in a collector current which is β times larger and the transistor acts as a current amplifier here. Moreover, the emitter-base voltage and the collector current have an exponential relationship. Those models set the bias of the transistor and assume that none of the circuit elements vary with the voltage or with the frequency.

Before any device model can be used, values of its internal equivalent electrical circuit parameters must be determined. The process of determining these parameters is called *parameter extraction*. Parameter extraction for small-signal electrical equivalent circuit characterization has been deeply studied and numerous techniques have been developed. The two main approaches used in this area are direct extraction [4] and optimization-based extraction [5].

Direct-extraction techniques rely on two sets of cold S-parameter measurements. These measurements are made with the gate at both pinch-off and at a suitable forward bias. The data and simplifications in the model are used to calculate the extrinsic bias-independent elements of the transistor model. The intrinsic elements are calculated after de-embedding the extrinsic elements using the equations derived in [4]. This method provides good approximate values for the more dominant model elements such as the intrinsic capacitors, and it is fast and simple to implement. However, the technique cannot determine all the extrinsic elements uniquely as mentioned in [6], [7], and [8] for the FET and in [9] and [10] for the HBT.

Optimization-based parameter extraction is computationally more intensive but sensitive to the choice of optimization starting values that Niekerk, du Preez and Schreurs discussed in

[11]. Though several promising optimization-based extraction methods that are insensitive to starting values have recently been published, [6], [8], [10], it is still difficult to determine all the model elements with a high degree of certainty. This is especially true for the parasitic elements. The phenomenon is due to the small influence that these elements have on the measured data and thus it is independent of the optimization method used. Therefore, the parameter values are easily influenced by measurement uncertainties. These effects cause traditional multidimensional optimizers to be numerically ill conditioned.

Fuzzy Neural Networks (FNN) has been recently recognized as a useful vehicle for efficient modeling and design [12]. Both neural networks and fuzzy logic are universal estimators; they can approximate any nonlinear function to any prescribed accuracy, provided that sufficient hidden neurons and fuzzy rules are available. Recent results show that the fusion procedure of these two different technologies seems to be very effective for nonlinear systems identification [13], [14], [15]. By combining the Fuzzy c-means method [16] and the neural representation of a transistor behavior [3], the small-signal equivalent circuit parameters are efficiently evaluated through a fuzzy-neural network, based on selection of the most suitable circuit topology of the active device.

In this thesis, traditional and intelligent modeling procedures were combined together for the extraction of the most suitable small-signal equivalent circuit topology of RF and microwave transistors. This work is applied to the area of small-signal modeling of FETs and HBTs.

1.2 Thesis Overview

This thesis is organized to introduce a technique that couples neural networks and fuzzy theory to extract the most suitable small-signal equivalent circuit topology of RF and microwave transistors.

The thesis consists of 6 chapters. Chapters 2 and 3 contain a summary of the primary design building blocks of the heterojunction bipolar transistor and the field effect transistor

respectively. The main goal of those two chapters is to provide the operation of the transistors as well as to introduce the device models.

In Chapter 4, an overview of the adopted method is presented. Our method is explained and compared with the existing methods. The supporting data is listed and explained with details in Chapter 5.

Finally, a conclusion is presented in Chapter 6, followed with suggestions for future work.

1.3 Thesis Contribution

Two primary contributions for the modeling of FETs and HBTs are presented in this thesis in order to efficiently predict the most reliable equivalent circuit for a transistor, given a set of S-parameters.

First, use ANN to set up a relationship between extra parameters, parameters beside those in the standard model, and the S-parameters. In this thesis, we defined the most widely used equivalent circuit topology as the standard topology. Besides, a topology library is set up with various topologies different from the standard one. Those additional topologies were collected from different technical papers related to small-signal transistor modeling. The parameter values of the standard topology were extracted using direct parameter extraction methods while the value of extra parameters were extracted using ANN with S-parameters and frequency as inputs and the extra parameter values as outputs. This process will be explained in chapter 4 with details.

Second, fuzzy logic was applied in the process of selecting most suitable model given certain S-parameters. In this work, a grading system was built up based on Fuzzy C-Means Clustering (FCM) theory to identify the most suitable topology. The score was scaled from 1 to 10 depending on the error between the S-parameters of each model in the library and the measured S-parameters. The model with the highest score would be the most suitable model. Specified steps will be strengthened in chapter 4.

1.4 Publications

The above work resulted in the following publications:

1 L. Ji, M.C.E. Yagoub "Combined fuzzy-neural approach for optimal RF/microwave transistor modeling," *WSEAS Trans. on Electronics*, Vol. 1, N°4, pp. 627-232, Oct. 2004.

2 S. Gaoua, L. Ji, F.A. Mohammadi, M.C.E. Yagoub, “Reliable fuzzy neural-based RF/microwave transistor modeling,” *5th IEEE Mediterranean Microwave Symposium*, Athens, Greece, Sept. 6-8, 2005.

3 Z. Cheng, L. Ji, S. Gaoua, F.A. Mohammadi, M.C.E. Yagoub, “Robust framework for efficient RF/microwave system modeling using neural- and fuzzy-based CAD tools,” *4th Int. Conf. on Electronics, Signal Processing and Control*, Rio de Janeiro, Brazil, April 25-27, 2005.

4 L. Ji, M.C.E. Yagoub "Combined fuzzy-neural approach for optimal RF/microwave transistor modeling," *4th Int. Conf. on Electronics, Hardware, Wireless & Optical Communications*, Salzburg, Austria, February 13-15, 2005.

5 L. Ji, M.C.E. Yagoub, “Efficient fuzzy-neural tool for optimum topology extraction of RF/microwave transistors,” *IEEE Int. Conf. on Communication, Computer and Power*, Feb. 14-16, 2005, Muscat, Oman.

Chapter 2

CHARACTERIZATION OF THE HETEROJUNCTION BIPOLAR TRANSISTOR

2.1 Introduction

Heterojunction Bipolar Transistors (HBTs) are very attractive candidates for digital, analog, and power applications due to their excellent switching speed combined with high current driving capabilities. An accurate small-signal HBT model is very important for designing a practical circuit with good accuracy, evaluating the process technology, and optimizing the design of the device.

With the increasing use of HBT in RF and microwave design and the need for more advanced systems, an accurate small-signal model becomes a key factor in circuit and system design area. Numerical Optimization Methods are the most commonly used small-signal parameter extraction techniques [10]. But such techniques might result in nonphysical and/or non-unique values of the extracted components. Furthermore, the optimization process is largely dependent on the initial values of the optimized variables. Therefore, another kind of extraction method which ensures unique and accurate values of all the circuit elements is of considerable importance.

Several approaches for a more accurate and more physical parameter extraction method are suggested in the literatures.

Costa [17] has used several test structures to systematically de-embed the intrinsic HBT from its surrounding extrinsic and parasitic elements. However, this method requires three test structures for each device size on the wafer, ignores the non-uniformity across the wafer, and may involve an additional processing mask in some self-aligned technologies.

Pehlke and Pavlidis [18] developed an analytic approach to extract the T-shaped equivalent circuit elements of the HBT. Though attractive in many aspects, this method had two major disadvantages. First, the method was still relying on optimization to find the parameters of the emitter branch and elements of the delay time. Second, the distributed nature of the base resistance and base-collector capacitance was not taken into account. This last assumption may result in a negative collector series resistance and/or a nonphysical frequency behavior of the calculated emitter block [19].

2.2 HBT Structure

Depending on the way it was doped, one can class HBTs into two types: the *npn* and the *pnp* transistors. The *npn* Heterojunction Bipolar Transistor is a three-terminal device. It has two *n*-regions, named the *emitter* and the *collector* respectively. The *p*-type base region is between the two. Different from the corresponding source and drain region of the FET, the emitter and collector regions are not interchangeable. The *pnp* structure is the converse to the *npn*, and has the *n*-type region between the two *p*-regions. Since the *pnp* type is less used, the following discussion concentrates on the *npn* type only.

The operation of the device can be classified into three conditions/modes:

- In the *cut-off* mode, both junctions are reverse biased, no current flows into or out of the device, and therefore the transistor can be considered as *off*.

- In the *active* mode, the current flowing into the base results in a collector current which is β times larger and the transistor acts as a current amplifier here. Moreover, the emitter-base voltage and the collector current have an exponential relationship. But in the reverse active condition, this current gain is small and virtually nonexistent ($\beta \approx 1$) in contrast to the forward-active mode.

- In the *saturation* mode, there is a substantial droop in current gain. The low value of the emitter-collector voltage is a typical sign of this mode.

2.3 The Standard Small-Signal Model

Developing a small-signal equivalent electrical circuit is one of the major ways to get an efficient tool for RF and microwave circuit design. For more uniformity and flexibility, several researchers adopted the principle of a "universal" small-signal equivalent electrical circuit, called here the standard HBT small-signal model, or topology #1, and shown in Figure 2.1 [20], [21], [22]. This circuit topology is derived from the general physical behavior of the real device and known as the first-order representation of the device, which is considered to be sufficiently accurate for most applications.

The equivalent circuit can be divided into two parts, the extrinsic part and the intrinsic part. The extrinsic part includes $C_{bep}, C_{cep}, C_{bcp}, L_b, L_e, L_c, R_b, R_e$ and R_c. Other parameters form the intrinsic circuit.

In the extrinsic part, R_e is the extrinsic emitter resistance, which consists of the contact resistance and emitter region resistance. The extrinsic collector resistance was divided into three parts: R_{c1}, R_{c2}, and R_{c3}, due to the *n*-collector, the n^+ access region, and the collector contact respectively. Those three resistances are lumped together as R_c, as shown in Figure 2.1. Similarly, the extrinsic base resistance consists of a contact resistance R_{b1}, and an access resistance R_{b2}. R_{b1} and R_{b2} are lumped together as R_b, as shown in Figure 2.1. $C_{bep}, C_{bcp}, C_{cep}$ model the coupling between the base-emitter, the base-collector, and the

collector-emitter interconnection layer. L_e, L_b, L_c are the contact leads of the emitter, base, and collector, respectively.

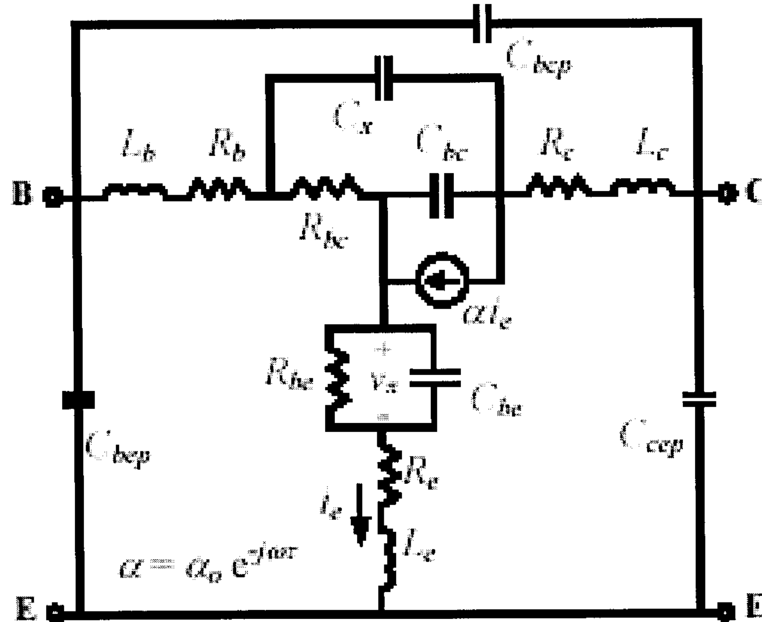


Figure 2.1 HBT Standard Topology

In the intrinsic part, R_{bc} is the intrinsic base resistance. The distribution effect of the base-collector junction is modeled by the elements R_{bi}, R_{bx}, C_{bc}. α_0, τ, ϖ are three parameters of the current gain. The major delay component associated with the device capacitance is associated with the charging of the base-emitter capacitance C_{be}. In the case of switching transistors, C_{be} is dominated by the base-emitter depletion capacitance, whereas for the emitter followers it is dominated by the diffusion capacitance. Correspondingly, R_{be} is the base-emitter resistance. C_{bc} is the effective intrinsic capacitance and C_{ex} is the effective extrinsic capacitance.

However, due to the ever increasing need for more advanced and complex functions, such standard equivalent circuit is no longer accurate. Therefore, a library of HBT small-signal models will be introduced in the next section to further accurately model the second-order behaviors of the HBT which can play a significant rule in many specific applications. The differences between the standard model and those models mainly concentrate on the intrinsic part while the extrinsic circuits remain the same in most cases.

2.4 HBT Small-Signal Model Library

In this work, we selected four additional models beside the standard one for HBT small-signal model library. Based on the most usable frequency range, fabrication technology and application area of HBTs, these circuit topologies should be able to provide a good prediction of any measured small-signal S-parameters. The difference between the standard model and the other four models will be stated after each model's Figure.

2.4.1 HBT Small-Signal Equivalent Circuit Topology #2

The structure of this second equivalent circuit is shown in Figure 2.2 [21]. This topology is different from the standard one in the Feedback network that is composed of R_{bc}, R_{b1}, C_{bc} in topology #2, while it is R_{bc}, C_x, C_{bc} in the standard topology. This topology highlights the extraction problem and allows for a simple analytical direct extraction formulation.

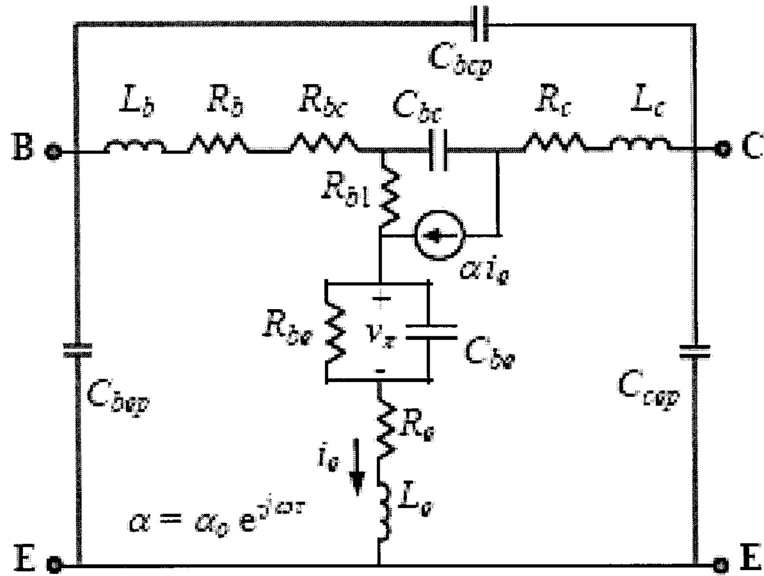


Figure 2.2 HBT Circuit Topology #2

Basically, these two feedback networks could be related mathematically and share the same extraction limitations but differ in feedback influence.

2.4.2 HBT Small-Signal Equivalent Circuit Topology #3

The different parameters in the third model are C_{b1}, R_{b2}, R_{c1} [24]. To be specific, the base-contact impedance is modeled by a parallel RC network (R_b and C_{b1}) here. The base contact resistance, R_b, and the combined intrinsic and extrinsic base resistance, R_{bc}, give the total base series resistance. The lumped, parallel RC combination model for the base contact is derived from Berger's lossy transmission line model [24]. The proposed base contact model was verified by comparing computed and experimental values of the real part of the RF impedance between the base and the collector, R_{bc}. Another parallel RC network (C_{bc} and R_{b2}) represents the metal-semiconductor capacitance. R_{c1} stands for the collector resistance in the intrinsic circuit.

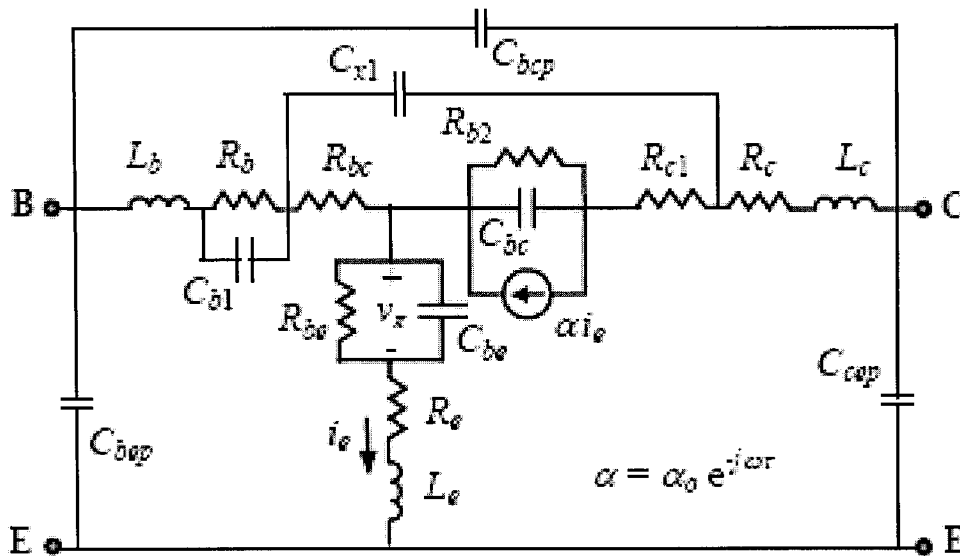


Figure 2.3 HBT Circuit Topology #3

For the InP-based HBT technology, parameters like high intrinsic base resistance, high base-collector junction resistance, and relatively small extrinsic base-collector junction capacitance prohibit users to utilize some important approximations by standard topology. Still, the effectiveness of evaluating chemical etching in devices could not be realized in standard topology. Therefore, topology #3 is presented here to address those problems. The most attracting point of this topology is the modeling of collector resistance in the intrinsic part of the circuit.

2.4.3 HBT Small-Signal Equivalent Circuit Topology #4

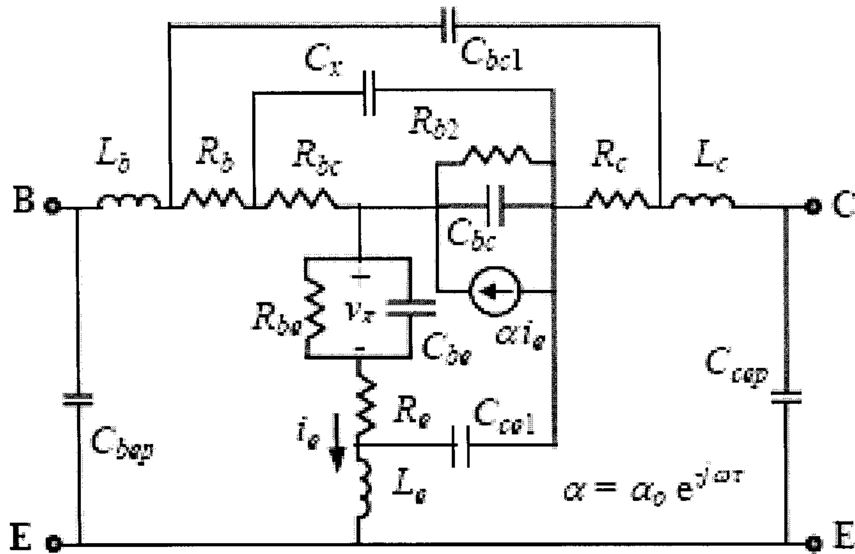


Figure 2.4 HBT Circuit Topology #4

R_{b2}, C_{bc1} and C_{ce1} are the parameters in topology #4 that are different from the standard model [25]. Same with the topology #3, R_{b2} represents the metal-semiconductor capacitance together with C_{bc}, C_{bc1} is in the extrinsic part of the circuit and stands for the interconnection capacitance between the base and the collector. Similar to C_{bc1}, C_{ce1} represents the interconnection capacitance between the collector and the emitter.

This topology provides a complete transistor equivalent circuit with the extrinsic capacitances and inductances modeling the on-wafer coplanar pad structure. Also it validates the lumped element model for the coplanar pad structure. Thus it pays more attention than others to the interconnection capacitances and has better performance in situations stated above.

2.4.4 HBT Small-Signal Equivalent Circuit Topology #5

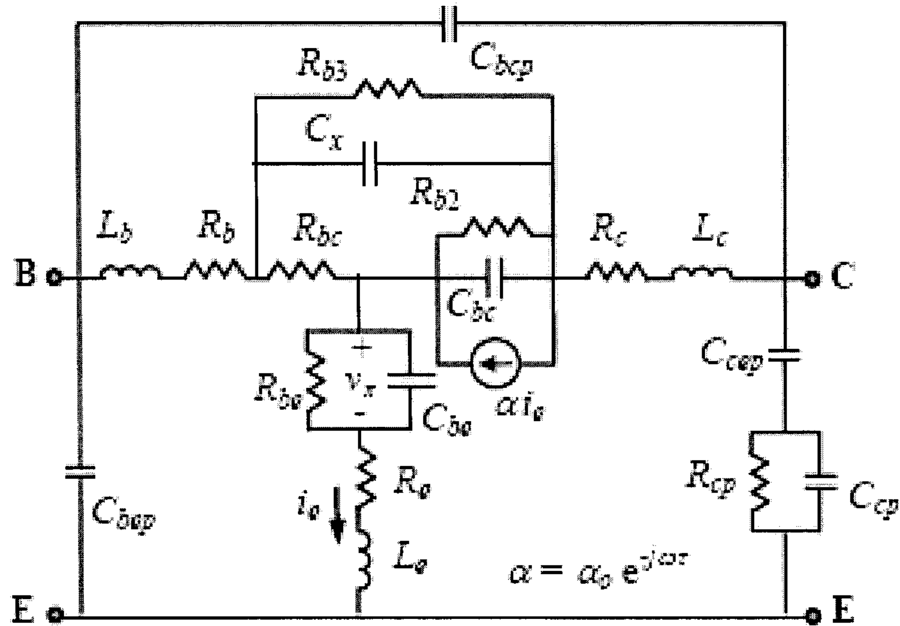


Figure 2.5 HBT circuit topology #5

SiGe HBT gains its popularity in the wireless communication devices implementation for its low-cost, high performance and high integration with base-band. Accurate device model is required to fully characterize the designed circuit, especially at high power and high frequency. The fifth model has a major change in the extrinsic part and meets those requirements [26]. The substrate network R_{cp} and C_{cp} depicts the substrate effect at collector for Si/SiGe HBT, which cannot be ignored due to the lossy substrate in certain circumstances while this effect has not being considered in GaAs and InP HBT. Furthermore, these two parameters are bias independent.

R_{b2}, R_{b3} are the two different parameters that describe the resistance in C_{bc}, C_x respectively.

Due to the added substrate network, this model is the most applicable when substrate effect has to be considered.

2.5 Conclusion

This chapter introduced the basic physical information about the bipolar transistor and its most widely used electrical equivalent circuits. The definition of the so-called standard topology and the small-signal circuit library which was used in this work are introduced in details. Those definitions will be used later in the examples to prove the efficiency and accuracy of the proposed method. The following chapter talks about the Field Effect Transistor.

Chapter 3

CHARACTERIZATION OF THE FIELD EFFECT TRANSISTOR

3.1 Introduction

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET or MOS, for short), the Metal-Semiconductor Field-Effect Transistor (MESFET or MES, for short) and the High Electron Mobility Transistor (HEMT) are certainly the workhorses of contemporary analog and digital RF and microwave design. Their major assets are their integration density, low power consumption and a relatively simple manufacturing process, which make it possible to produce large and complex circuits in an economical way. Due to mature and low-cost Si technologies, MOSFET's are currently recognized as promising core devices for RF circuit applications [1], while MESFETs and HEMTs are promising candidates for microwave power amplification, with applications ranging from satellite links to wireless communications, from highways to electronic warfare. Also, they have a potential for low frequency high voltage (up to 1 kV) switching power control [4].

The modeling of the transistor is a key point of high-frequency circuits Computer Aided Design (CAD). The elaboration of an equivalent electrical model begins with the choice of a circuit topology generally consisting of lumped elements. The element values are obtained either from device physics or by comparison to experimental measurements. Knowledge of

the small-signal equivalent circuit of a field effect transistor is very useful for the device performance analysis in designing of microwave circuits and characterizing the device technological process.

3.2 MOSFET Structure

The *n*-type source and drain regions are implanted into a *p*-type substrate (often called the *body*). There is a thin layer of silicon dioxide (SiO_2) between the source and the drain. The *gate* of the transistor is made of a conductive material. A thick layer of SiO_2 (called the *field oxide*) and a reverse-biased *np*-diode, formed by adding an extra p^+ region, insulate neighboring devices from each other [27].

Basically, the NMOS transistor can act as a switch. Applying a voltage that is larger than the *threshold voltage,* V_T , to the gate forms a conducting channel between the drain and source: the switch is closed. The larger the voltage differences between the gate and source, the smaller the channel resistance and the larger the current. The channel doesn't exist if the gate voltage is lower than the threshold voltage. Under this condition, the switch is open.

3.3 MESFET Structure

Three metal electrode contacts are made to a thin semiconductor active channel layer. The contacts are labeled "source", "gate", and "drain". For microwave and millimeter wave applications, the thin active layer is almost always *n*-type GaAs material [4].

The carrier flows from source to drain is controlled by a Schottky metal gate. The control of the channel is obtained by varying the depletion layer width underneath the metal contact which modulates the thickness of the conducting channel and thereby the current. The key advantage of the MESFET is the higher mobility of the carriers in the channel as compared to the MOSFET. The higher mobility leads to a higher current, transconductance and transit frequency of the device. The disadvantage of the MESFET structure is the presence of the Schottky metal gate. It limits the forward bias voltage on the gate to the turn-on voltage of

the Schottky diode. This turn-on voltage is typically 0.7 V for GaAs Schottky diodes. The threshold voltage therefore must be lower than this turn-on voltage.

3.4 HEMT Structure

High Electron Mobility Transistors (HEMTs) have emerged as a promising candidate for microwave power amplification. Also, they have a potential for low frequency high voltage (up to 1 kV) switching power control. The unique feature of the HEMT is channel formation from carriers accumulated along a grossly asymmetric heterojunction, i.e. a junction between a heavily doped high band-gap and a lightly doped low band-gap region [4].

HEMT also uses a Shottky barrier diode to isolate the channel from the gate and has similar advantages as the MESFET. The primary difference is that the channel is not a simply doped region, but instead consists of carriers which come from a doped region with a higher band gap [4].

3.5 FET Modeling

Since MOSFETs, MESFETs, and HEMTs have similar small-signal electrical equivalent circuits, we will further refer to them as FET devices. Usually, a FET device is considered to be a three-terminal one with gate, drain, and source ports. Actually, there is a fourth terminal, the substrate. It is usually not shown on the schematics as it is generally connected to a dc supply that is identical for all devices of the same type [27].

For FET devices, main physical phenomena such as current modulation, charge accumulation and delays are taken into account in the intrinsic part of the circuit, which usually has a simple pi topology, while the extrinsic part gives the behavior of parasitic elements. However a better representation of FETs would include the distributed effects in the channel under the gate, but it leads to a rather complicated equivalent circuit and/or to an increase in the extraction cost of the model. The most widely used FET small-signal circuit models for RF and microwave circuit design will be discussed in this chapter.

3.6 The Standard Small-Signal Model

Small-signal models describe the transistor operation in the saturation region. In this region, a small Gate-Source voltage will produce a linear change in the Drain-Source current. At a certain point, if the Gate-Source voltage is allowed to increase, the Drain-Source current change is no longer linear and the small-signal model no longer applies. Small-signal models set the bias of the transistor and assume that none of the circuit elements varies with voltage or frequency. Thus, it is a task of biasing the transistor, measuring the S-parameters over a certain frequency range, and extracting the electrical equivalent circuit model to represent the device.

The standard model or circuit topology #1, represented in Figure 3.1, is the most widely used model [4], [28]. The circuit topology is used to predict the device small-signal first-order behavior. The topology is divided into two groups of elements: the extrinsic (or parasitic) elements and the intrinsic elements that represent the bulk of the device.

The following is a list of the topology elements and their description [4]:

(*Extrinsic elements*:)

L_s : is the source parasitic inductance.

L_d : is the drain parasitic inductance.

L_g : is the gate parasitic inductance.

R_s : is the source parasitic resistance.

R_d : is the drain parasitic resistance.

R_g : is the gate parasitic resistance.

C_{pds} : is the drain-to-source parasitic capacitance.

C_{pgs} : is the gate-to-source depletion capacitance.

(*Intrinsic elements*:)

C_{gs} : is the gate-to-source parasitic capacitance.

C_{gd} : is the gate-to-drain depletion capacitance.

C_{ds} : is the drain-to-source depletion capacitance.

R_i : is the charging resistance.

g_m : is the device transconductance.

τ : is the transconductance delay.

R_{ds} : is the output resistance.

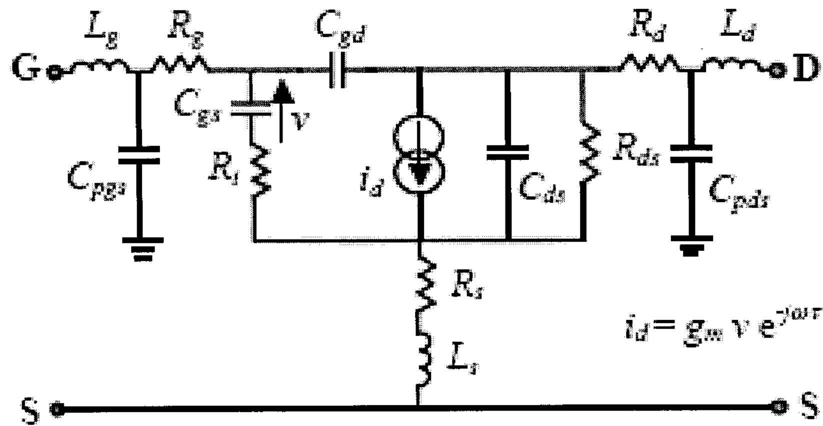


Figure 3.1 FET Standard Topology

3.7 FET Small-Signal Model Library

In this work, three models were selected besides the standard one for FET small-signal model library. The difference between the standard model and the other three models will be stated after each model's figure.

3.7.1 FET Small-Signal Equivalent Circuit Topology #2

The structure of topology #2 is shown in Figure 3.2 [29]. The difference between this topology and the standard one is that it includes the effects of the differential resistances of the gate-to-source and gate-to-drain as well as the serial resistance of the feedback

capacitance. For operating points with positive gate bias, the differential resistances of the gate-to-source and gate-to-drain diodes are modeled by the resistances R_{gs} and R_{fd}. To ensure a smooth transition from the symmetric "cold model" to operating points in the saturation region, the resistor of the feedback capacitance R_{gd} is included.

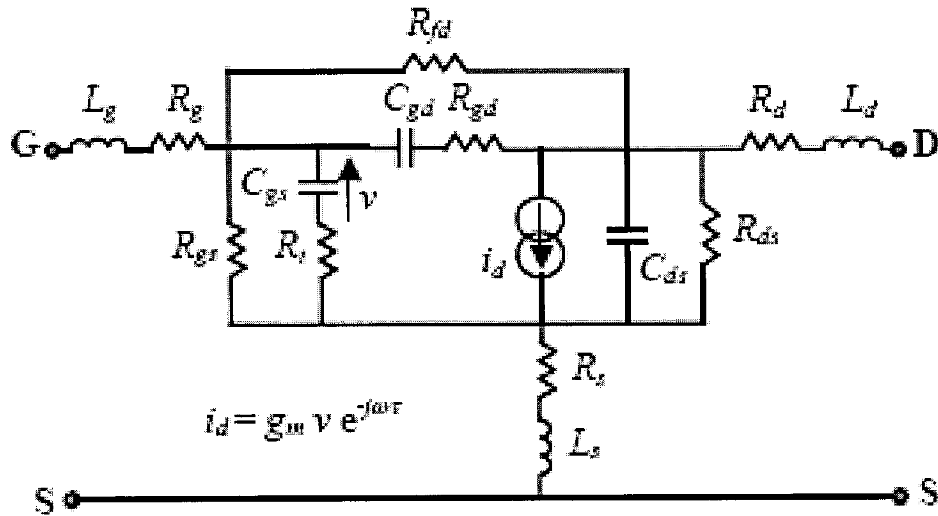


Figure 3.2 FET Circuit Topology #2

This extended equivalent circuit takes into account the gate current of positive biased transistors as well as the symmetrical nature of the devices at low drain voltages. Since the operating point for maximum transconductance and highest transit frequency is at positive biased gate, the gate current cannot be neglect. Another problem occurs in switching applications, when the drain to source voltage of the FET comes close to 0V. In this case the symmetrical nature of the physical device has to be reflected in the equivalent circuit. Therefore, this model is most suitable in the case of modeling transistors with positive gate bias and has better performance than the standard model in simulating the transition of operating points from the symmetric "cold model" to in the saturation region.

3.7.2 FET Small-Signal Equivalent Circuit Topology #3

Figure 3.3 shows the FET circuit topology #3 [30]. Similar to topology #2, it includes the differential resistances of the gate-to-source, gate-to-drain and the serial resistance of the

feedback capacitance. Furthermore, this topology considers the effects of pad capacitances ($C_{gdp}, C_{pgs}, C_{pds}$).

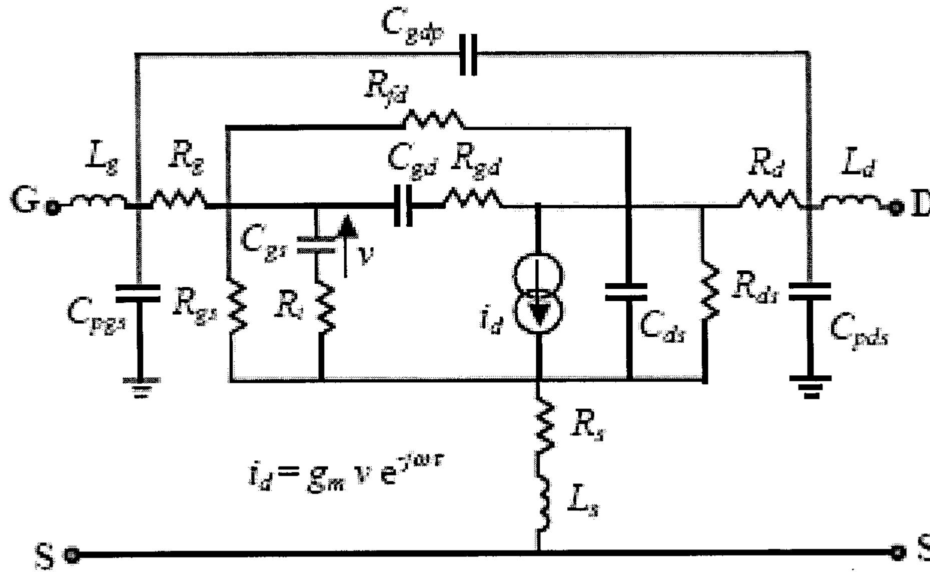


Figure 3.3 FET Circuit Topology #3

Consequently, we have chosen the topology of Figure 3.3 for its completeness and versatility in the following cases. Broad-band modeling of millimeter-wave FET's requires that parasitic elements such as the pad capacitances are taken into account; also, some high performance devices such as InP-based FET's often have rather leaky gates, the reverse current of which must be modeled by the resistances R_{fd}, R_{gs}.

3.7.3 FET Small-Signal Equivalent Circuit Topology #4

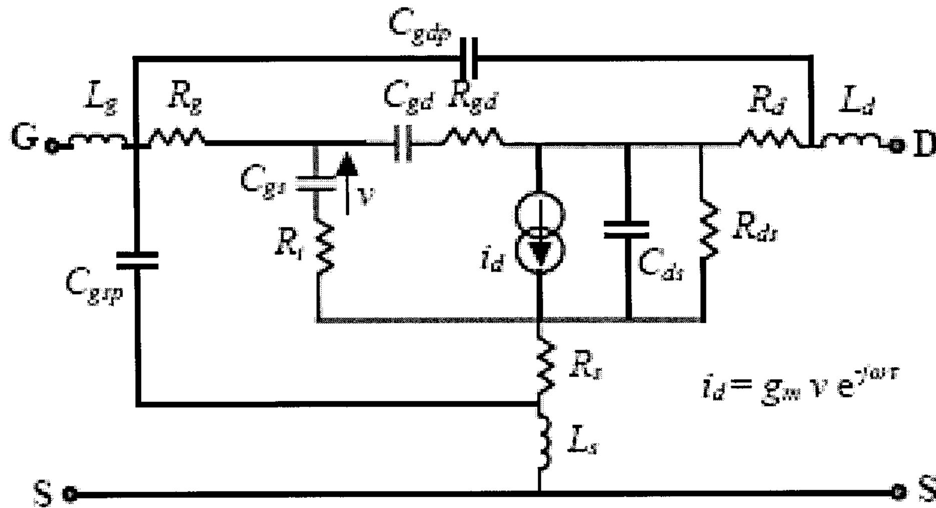


Figure 3.4 FET circuit topology #4

The topology #4 is presented in Figure 3.4 [31]. The mounting of the FET is modeled by two sets of lossless parasitics here. The first set includes the inductors L_g, L_d and L_s representing bonding wire inductances. The second set includes capacitors C_{gsp} and C_{gdp} representing the capacitances between the three bonding pads. Also, the resistor of the feedback capacitance R_{gd} is included for the smooth transition from the symmetric "cold model" to operating points in the saturation region.

The new equivalent circuit is the simplest electrical topology that accounts for the distributive nature of the channel potential. It extends the usefulness of basic table-based models into the millimeter-wave range, without sacrificing the good reported behavior at low frequencies. Since model bandwidth can be increased with more complex intrinsic circuit topologies, it is necessary to add the nonlinear diodes conductance to account for forward and breakdown behavior. Consequently, it reproduces more accurately the intrinsic feedback than the classical models and allows us to model the distributed gate current with everyone of the depletion channel region associated capacitances.

3.8 Conclusion

In this chapter, we have described FET devices in details. MOS, MES, and HEM transistors are voltage-controlled devices. Based on the value of the gate-source voltage with respect to a threshold voltage V_T, three operation regions have been identified: *cut-off*, *linear*, and *saturation*. One of the most enticing properties of such transistors is that it approximates a voltage-controlled switch. This two-state operation matches the concepts of binary digital logic.

Four different topologies of FET small-signal equivalent circuit are presented and compared. Each one has a special focus on certain properties. Consequently, every model is suitable for specified cases.

In next chapter, an original method for efficient transistor (i.e., FET and HBT) extraction and modeling will be presented.

Chapter 4

TECHNIQUES FOR MODELING RF AND MICROWAVE TRANSISTORS

4.1 Introduction

This chapter introduces a novel RF and microwave modeling method based on the existing extracting methods. It has been proven to be efficient and accurate and most importantly, robust in selecting the most suitable model. This work mainly applies to small-signal models.

In section 4.2, the basic parameter extraction method for FET and HBT will be strengthened. The application of neural network in this method will be explained in section 4.3. Finally, the utilization of fuzzy logic, the major contribution of this work, will be highlighted in section 4.4.

4.2 Parameter Extraction

Parameter extraction is a technique whereby element values of a transistor model topology are found. In this technique, a set of small-signal S-parameter measurements are performed for the device over the desired modeling frequency range. The values of the equivalent circuit elements are found such that they best fit the set of previously measured S-

parameters. In fitting an equivalent circuit to a set of measured S-parameters, one should determine as many elements as possible before resorting to optimization techniques.

4.2.1 Parameter Extraction Method for the Field Effect Transistor

The first step of the proposed method is a direct parameter extraction of the standard FET topology using the well-known technique described in [4]. An optimization loop is added for the extraction of the extrinsic parameters. The S-parameters of the standard topology (denoted as S_{ij}^{s}, i, j = 1, 2, where *s* stands for *standard*) are then compared to the measured S-parameters (denoted as S_{ij}^{m}, i, j = 1, 2, where *m* stands for *measured*). If no acceptable accuracy is achieved, the standard topology is then not sufficient to efficiently model the transistor. Therefore, a second step would be selecting a new circuit topology for the active device from a given library. Since the equivalent circuit is often specific to a given type of transistor and it is puzzling to decide which one is most suitable to be used in one specific work, we created a library of FET equivalent circuit topologies. Three of the most often used models are displayed in section 3.7.

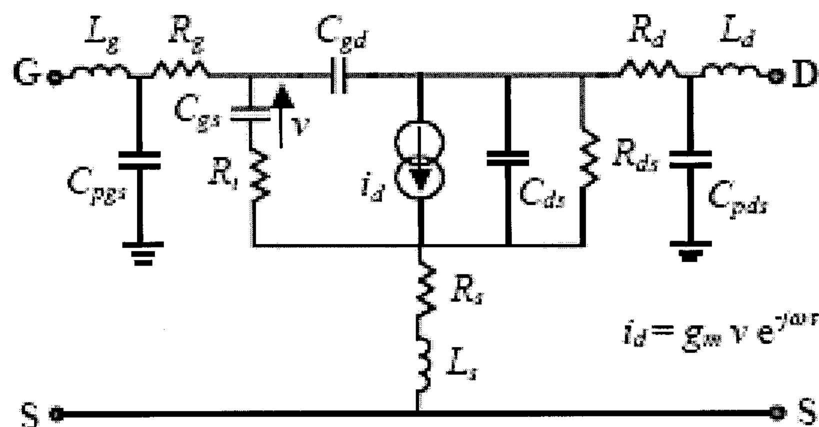


Figure 4.1 FET Standard Topology

First, transform the measured S parameters into Y parameters [4]:

$$Y_{11} = \frac{(1-S_{11})*(1+S_{22})+S_{12}*S_{21}}{(1+S_{11})*(1+S_{22})-S_{12}*S_{21}} \quad (4.1)$$

$$Y_{12} = \frac{-2*S_{12}}{(1+S_{11})*(1+S_{22})-S_{12}*S_{21}} \quad (4.2)$$

$$Y_{21} = \frac{-2*S_{21}}{(1+S_{11})*(1+S_{22})-S_{12}*S_{21}} \quad (4.3)$$

$$Y_{22} = \frac{(1+S_{11})*(1-S_{22})+S_{12}*S_{21}}{(1+S_{11})*(1+S_{22})-S_{12}*S_{21}} \quad (4.4)$$

Y_{iji} stands for the imaginary part of Y_{ij} and Y_{ijr} stands for the real part of Y_{ij}. Those expressions are remaining the same for S-parameters and Z-parameters. Then the intrinsic parameters can be extracted following the functions below [4]:

$$C_{gd} = -Y_{12i} / \omega \quad (4.5)$$

$$C_{ds} = Y_{22i} / \omega - C_{gd} \quad (4.6)$$

$$C_{gs} = Y_{11i} / \omega - C_{gd} \quad (4.7)$$

$$g_{ds} = Y_{22r} \quad (4.8)$$

$$R_i = \frac{1-\sqrt{1-4*Y_{11r}{}^2/(\omega*C_{gs})^2}}{2*Y_{11r}} \quad (4.9)$$

$$g_{m1} = Y_{21r} - Y_{21i}*R_i*C_{gs}*\omega - \omega^2*C_{gd}*C_{gs}*R_i \quad (4.10)$$

$$g_{m2} = Y_{21r}*R_i*C_{gs}*\omega + Y_{21i} + \omega*C_{gd} \quad (4.11)$$

$$g_m = \sqrt{g_{m1}^2 + g_{m2}^2} \quad (4.12)$$

$$\tau = -a\tan(g_{m2} / g_{m1}) / \omega \quad (4.13)$$

An optimization step is used in the extraction of the extrinsic parameters $L_s, L_g \, and \, L_d$.

$$L_s = m_1 * (Z_{12i} - z_{12i}) / \omega + (1 - m_1) * (Z_{21i} - z_{21i}) / \omega \quad (4.14)$$

$$L_g = (Z_{11i} - z_{11i}) / \omega - L_s \quad (4.15)$$

$$L_d = (Z_{22i} - z_{22i}) / \omega - L_s \quad (4.16)$$

where:

Z_{ij}: the extrinsic Z parameter;

z_{ij}: the intrinsic Z parameter;

m_1 is the weighting factor.

The goal of this optimization is the minimization of the difference between the calculated S-parameters and the measured S-parameters.

Following is the computing of intrinsic modeled Y-parameters from circuit elements found in the former step using Equations 4.17 to 4.20

$$Y_{11i} = R_i C_{gs}^2 \omega^2 / D + j\omega(C_{gs} / D + C_{gd}) \quad (4.17)$$

$$Y_{12i} = -j\omega C_{gd} \quad (4.18)$$

$$Y_{21i} = \{ g_m e^{(-jw\tau)} / (1 + jR_i C_{gs} \omega) \} - j\omega C_{gd} \quad (4.19)$$

$$Y_{22i} = g_{ds} + j\omega(C_{ds} + C_{gd}) \quad (4.20)$$

where $D = 1 + \omega^2 C_{gs}^2 R_i^2$. Convert Y-parameters to Z-parameters, thus the extrinsic device Z-parameters can be expressed in terms of the intrinsic Z-parameters:

$$Z_{11} = Z_{11i} + (R_g + R_s) + j\omega(L_g + L_s) \quad (4.21)$$

$$Z_{12} = Z_{12i} + R_s + j\omega L_s \quad (4.22)$$

$$Z_{21} = Z_{21i} + R_s + j\omega L_s \tag{4.23}$$

$$Z_{22} = Z_{22i} + (R_d + R_s) + j\omega(L_d + L_s) \tag{4.24}$$

Convert extrinsic modeled Z-parameters back to S-parameters. This set of S-parameters is the modeled S-parameters.

4.2.2 Parameter Extraction Method for Heterojunction Bipolar Transistor

As for the FET, the equivalent standard topology of HBT is shown in Figure 4.2 [22]. Similar to the extraction process of FET, the philosophy behind the method is to determine as many resistive elements as possible without resorting to S-parameter fitting (here also, the S-parameters of the standard topology are denoted as S_{ij}^{s}, i, j = 1, 2, while the measured parameters are denoted as S_{ij}^{m}, i, j = 1, 2). The parameters in HBT standard model are calculated in two steps; the direct extraction method is first applied, followed by a small optimization method to update the parameter values in order that the difference between the measured S-parameters and the modeled S-parameters minimized.

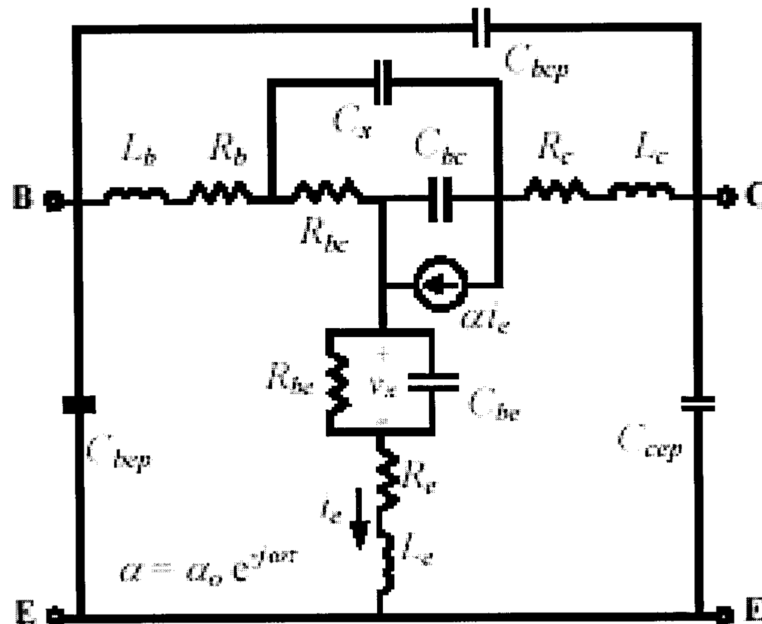


Figure 4.2 HBT Standard Topology

4.2.2.1 Extrinsic Parameter Extraction

The first step in the extraction process here is converting S-parameters to Z-parameters [4]. The extrinsic parameters are extracted from Z-parameters of the HBT's under cutoff operation. The behavior of the deembedded Z-parameters is then analyzed to extract all the intrinsic parameters.

The collector lead conductor L_c can be calculated by

$$L_c = \mathrm{Im}(Z_{22} - Z_{21}) / \omega \quad (4.25)$$

This straightforward method is not as accurate as expected and will be optimized after the rest of parameters obtained [22].

From the first-order approximation, L_b could be easily extracted from imaginary part of $Z_{11} - Z_{12}$ in the middle-frequency range [32]. That is

$$L_b = \mathrm{Im}(Z_{11} - Z_{12}) / \omega \quad (4.26)$$

L_e can be obtained from the imaginary part of Z_{12} in the lower middle-frequency range.

$$L_e = \mathrm{Im}(Z_{12}) / \omega \quad (4.27)$$

Figure 4.3 shows a plot of $\omega \mathrm{Im}(Z_{11} - Z_{12})$, $\omega \mathrm{Im}(Z_{22} - Z_{21})$, and $\omega \mathrm{Im}(Z_{12})$ versus ω^2.

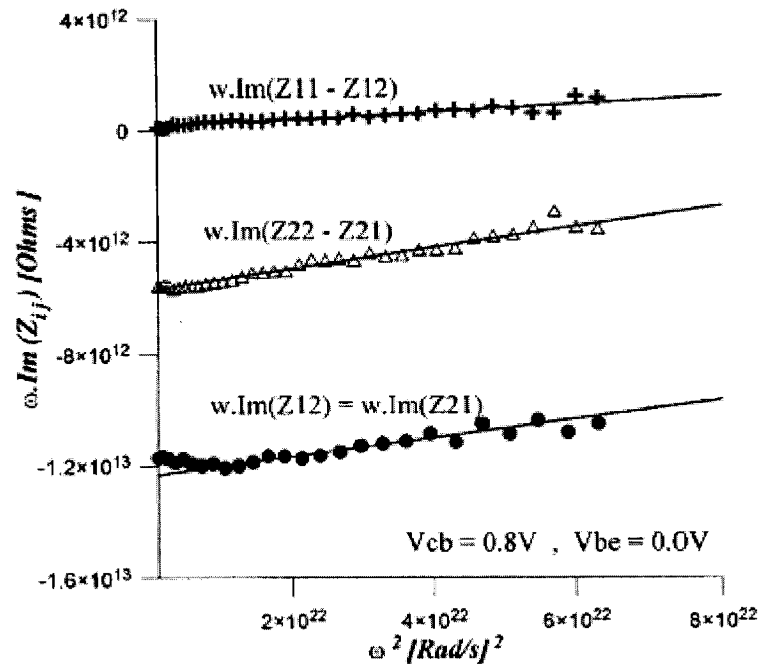


Figure 4.3 Plot of $\omega \mathrm{Im}(Z_{ij})$ versus w^2 under Cold-HBT Condition

At high frequencies under cold condition, the real parts of $(Z_{11} - Z_{12})$, $(Z_{22} - Z_{21})$ and Z_{12} saturate at R_b, R_c and R_e respectively (see Figure 4.4). The values of those three parameters could be first estimated by the following functions:

$$R_b = \mathrm{Re}(Z_{11} - Z_{12}) \tag{4.28}$$

$$R_c = \mathrm{Re}(Z_{22} - Z_{21}) \tag{4.29}$$

$$R_e = \mathrm{Re}(Z_{12}) \tag{4.30}$$

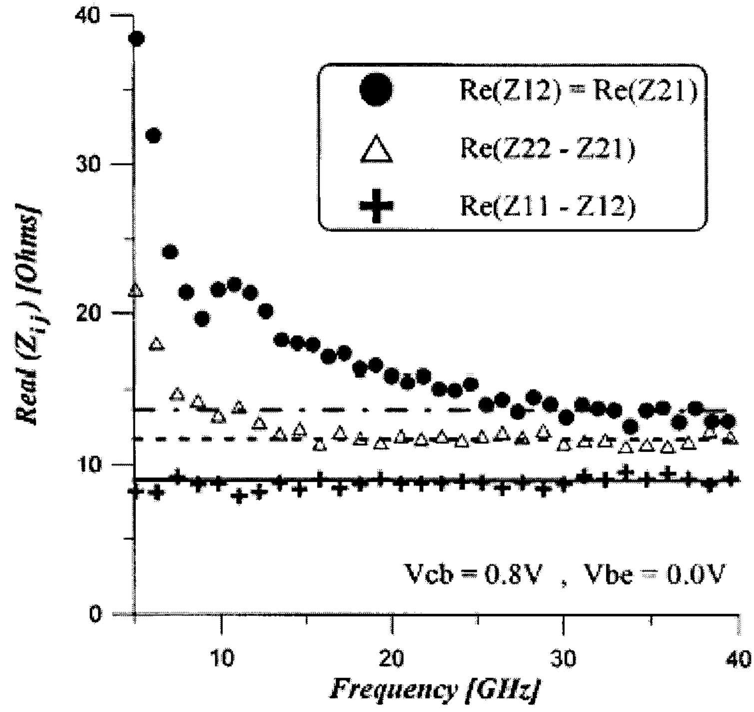


Figure 4.4 Real-parts of Z-parameters as a Function of Frequency Obtained under Cold-HBT Condition

4.2.2.2 Intrinsic Parameter Extraction

The intrinsic Z-parameters are obtained by relations 4.31 and 4.32.

$$Z_{\text{int}} = Z_{total} - Z_{ext} \tag{4.31}$$

$$Z_{ext} = \begin{bmatrix} R_e + R_b + j\omega L_e + j\omega L_b & R_e + j\omega L_e \\ R_e + j\omega L_e & R_e + R_c + j\omega L_e + j\omega L_c \end{bmatrix} \tag{4.32}$$

Based on the adopted HBT equivalent circuit, the intrinsic elements at each frequency point are derived. The detailed expressions are given as follows:

$$\alpha_0 = -\frac{\text{Re}(a)}{\cos(\omega\tau)} \tag{4.33}$$

$$\tau = \frac{1}{\omega}\tan^{-1}\left[-\frac{\mathrm{Im}(a)}{\mathrm{Re}(a)}\right] \tag{4.34}$$

$$C_{ex} = \frac{\mathrm{Re}(c)}{\omega[\mathrm{Im}(d)\,\mathrm{Re}(c) + \mathrm{Im}(d)\,\mathrm{Re}(c)]} \tag{4.35}$$

$$C_{bc} = \frac{\mathrm{Re}(d)}{\omega[\mathrm{Im}(d)\,\mathrm{Re}(c) - \mathrm{Re}(d)\,\mathrm{Im}(c)]} - 2C_{ex} \tag{4.36}$$

$$R_b = jb/(\omega C_{bc}) \tag{4.37}$$

$$R_{be} = -\frac{[\mathrm{Re}(e)]^2 + [\mathrm{Im}(e)]^2}{\mathrm{Re}(e)} \tag{4.38}$$

$$C_{be} = \frac{\mathrm{Im}(e)}{\omega\{[\mathrm{Re}(e)]^2 + [\mathrm{Im}(e)]^2\}} \tag{4.39}$$

where

$$a = \frac{Z_{\mathrm{int}\,12} - Z_{\mathrm{int}\,21}}{Z_{\mathrm{int}\,22} - Z_{\mathrm{int}\,21}} \tag{4.40}$$

$$b = \frac{Z_{\mathrm{int}\,11} - Z_{\mathrm{int}\,12}}{Z_{\mathrm{int}\,22} - Z_{\mathrm{int}\,21}} \tag{4.41}$$

$$c = Z_{\mathrm{int}\,22} - Z_{\mathrm{int}\,21} \tag{4.42}$$

$$d = Z_{\mathrm{int}\,22} - Z_{\mathrm{int}\,21} + Z_{\mathrm{int}\,11} - Z_{\mathrm{int}\,12} \tag{4.43}$$

$$e = -Z_{\mathrm{int}\,12} + \frac{\mathrm{Re}[(Z_{\mathrm{int}\,22} - Z_{\mathrm{int}\,21} + Z_{\mathrm{int}\,11} - Z_{\mathrm{int}\,12})(Z_{\mathrm{int}\,12} - Z_{\mathrm{int}\,21})(Z_{\mathrm{int}\,12} - Z_{\mathrm{int}\,11})]}{\mathrm{Re}[(Z_{\mathrm{int}\,22} - Z_{\mathrm{int}\,21})((Z_{\mathrm{int}\,22} - Z_{\mathrm{int}\,21})]} \tag{4.44}$$

The measured intrinsic Z-parameters are calculated as follows:

$$Z_{\mathrm{int}\,11} = \frac{[(1-\alpha)Z_{bc} + Z_{ex}]R_b}{Z_{bc} + Z_{ex} + R_b} + Z_{be} \tag{4.45}$$

$$Z_{\mathrm{int}\,12} = \frac{(1-\alpha)Z_{bc}R_b}{Z_{bc} + Z_{ex} + R_b} + Z_{be} \tag{4.46}$$

$$Z_{\text{int}\,21} = \frac{\left[-\alpha Z_{ex} + (1-\alpha)R_b\right]Z_{bc}}{Z_{bc} + Z_{ex} + R_b} + Z_{be} \tag{4.47}$$

$$Z_{\text{int}\,22} = \frac{(1-\alpha)Z_{bc}(Z_{ex} + R_b)}{Z_{bc} + Z_{ex} + R_b} + Z_{be} \tag{4.48}$$

$$Z_{be} = \frac{R_{be}}{1 + j\omega R_{be}C_{be}} \tag{4.49}$$

$$Z_{bc} = \frac{1}{j\omega C_{bc}} \tag{4.50}$$

$$Z_{ex} = \frac{1}{j\omega C_{ex}} \tag{4.51}$$

The total measured Z-parameters could be derived from equation 4.31. All the parameter values are updated by an optimization step by minimizing the difference between modeled and measured S-parameters.

4.3 Artificial Neural Network (ANN) Approach

Recently, artificial neural networks were introduced to the RF/microwave community, opening the door for an unconventional approach to RF/microwave computer-aided design. In this short span, the domain of this field has expanded considerably, successfully encompassing topics such as radar applications, modeling, measurement, circuit designing, and optimization problems [33], [34], [35].

4.3.1 Review of Artificial Neural Network (ANN)

ANNs are computational tools that learn from experience (training), generalize from previous examples to new ones, and abstract essential characteristics from input containing relevant data. Although neural networks can serve to further the understanding of brain functions, engineers are interested in neural networks for problem solving. Because of their massively parallel nature, ANNs can perform computations at high speed. Because of their adaptive nature, neural networks can adapt to changes in data and learn the characteristics of

input signals. Furthermore, due to their nonlinear nature, they can perform functional approximation and signal filtering operations, which are beyond optimal linear techniques.

In its most general form, a neural network is a machine that is designed to model the way in which the brain performs a particular task or function of interest. The network is usually implemented using electronic components or simulated in software on a digital computer. The following definition of neural networks may be offered [36]: "A neural network is a massively parallel distributed processor that has a natural propensity for storing experiential knowledge and making it available for use. It resembles the brain in two respects: (1) knowledge is acquired by the network through a learning process, and (2) interneuron connection strengths known as synaptic weights are used to store the knowledge."

Let **x** be a n-vector $\{x_i, i = 1, \ldots, n\}$ containing the external inputs and **y** be an m-vector $\{y_k, k = 1, \ldots, m\}$ containing the outputs from the output neurons. The original problem can be expressed as [36]

$$y = f(x) \tag{4.52}$$

while the neural network model for the problem is

$$y_{NN} = \tilde{y}(x, \omega) \tag{4.53}$$

where **w** is a N_w-vector $\{w_i, i = 1, \ldots, N_w\}$ containing all the weight parameters representing the connections in the NN. The definition of **w** and the way in which $\mathbf{y}_{NN}$ is computed from **x** and **w** determines the structure of the NN. The most commonly used neural network configuration is the Multi Layer Perceptrons (MLP) [36].

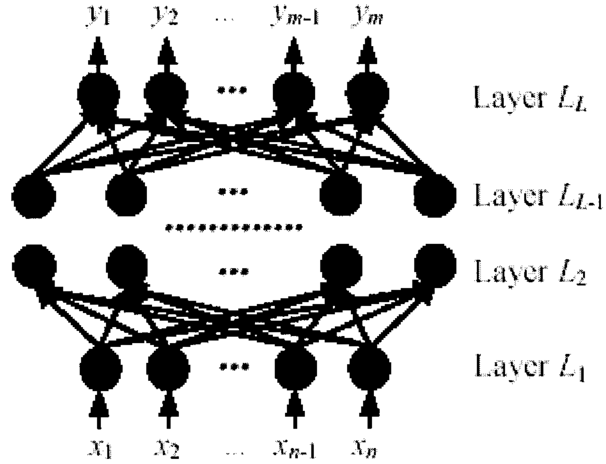


Figure 4.5 Structure of the MLP Neural Network

In the MLP structure, the neurons are grouped into layers as shown in Fig. 4.5. The layer L_1 is the input layer. The layers from L_2 to L_{L-1} are called hidden layers, while the last layer L_L, called the output layer, contain the response of the device to be modeled. The various layers are placed end to end with neuron connections between them. For such a neural network, the function given by Equation 4.52 is calculated on the basis of the layer of entry while using [36]

$$z_i^l = x_i \qquad i = 1,...,N_1, \quad n = N_1 \qquad (4.54)$$

z_i^1 is the output of the ith neuron of the input layer, and while proceeding layer by layer, the output at the end of layer L_L is given by

$$z_j^l = \sigma\left(\sum_{k=0}^{N_{l-1}} w_{jk}^l \, z_k^{l-1} + w_{j0}^l\right) \qquad j = 1,..., N_l, \quad m = N_l, \quad l = 1,..., L \qquad (4.55)$$

to reach the output layer that gives

$$y_k = z_k^L \qquad k = 1,...,N_l, \quad m = N_l \qquad (4.56)$$

In these relations, N_l is the number of neurons in the layer L_l, w_{jk} represents the weight of the connection between the kth neuron of the layer L_{l-1} and the jth neuron of the layer L_l. In [31], the function σ is known as the activation function of the neuron. It is usually equivalent to a sigmoid function for the hidden layers, a relay function for the input layer, and a linear function for the output layer.

4.3.2 Application of ANN in Parameter Extraction

Let $\{\Omega^s\}$ be the set of elements Ω_p^s $(p = 1, \ldots, P_s)$ in the standard topology. A symbolic code was developed in [37] to derive the following nonlinear functions analytically

$$S_{ij}^{\mathbf{k}} = f_{ij}^{\mathbf{k}}\left(S_{ij}^{\mathbf{s}}, \{\Omega^{\mathbf{k}}\}\right) \quad i, j = 1,2 \quad k = 1,\ldots,4 \tag{4.57}$$

where $\{\Omega^{\mathbf{k}}\}$ is the set of the $P_{\mathbf{k}}$ extra elements added in circuit #$(k\text{-}1)$ in comparison with the standard topology

$$\{\Omega^1\}_{FET} = \{R_{fd}, R_{gd}, R_{gs}\}\Big|_{C_{pgs}=C_{pds}=0}$$

$$\{\Omega^2\}_{FET} = \{R_{fd}, R_{gd}, R_{gs}, C_{gdp}\}$$

$$\{\Omega^3\}_{FET} = \{R_{gd}, C_{gdp}, C_{gsp}\}\Big|_{C_{pgs}=C_{pds}=0}$$

$$\{\Omega^1\}_{HBT} = \{R_{bc}\}\Big|_{C_{bcp}=C_{cep}=C_{bep}=0}$$

$$\{\Omega^2\}_{HBT} = \{C_{b1}, R_{b2}, R_{c1}\}\Big|_{C_{bcp}=C_{cep}=C_{bep}=0}$$

$$\{\Omega^3\}_{HBT} = \{C_{bc1}, R_{b2}, C_{ce1}\}\Big|_{C_{bcp}=C_{cep}=C_{bep}=0}$$

$$\{\Omega^4\}_{HBT} = \{R_{b3}, R_{b2}, R_{cp}, C_{cp}\}\Big|_{C_{bcp}=C_{cep}=C_{bep}=0}$$

in order to evaluate the alternative fuzzy criteria.

$$E^{\mathbf{k,s}} = \sum_{i=1}^{2}\sum_{j=1}^{2}\left[\mathrm{Re}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{s}}\right)\right]^2 + \left[\mathrm{Im}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{s}}\right)\right]^2 \tag{4.58}$$

The above relations depend *only* on the values of the P_k elements of set $\{\Omega^k\}$. However, since relations (4.57) are strongly interdependent, highly nonlinear, multi-dimensional, and require a huge combination of values to be accurately evaluated, we used artificial neural networks to learn these quantities [36].

By allocating values to the standard S^s parameters and varying the value of each element Ω_p^k (p = 1, ..., P_k) of set $\{\Omega^k\}$, we compute the S^k parameters and therefore, the difference $\{S^k - S^s\}$. The resulting data in the form of

$$Tr^k = \left[\underbrace{\mathrm{Re}\left(S_{ij}^k - S_{ij}^s\right), \mathrm{Im}\left(S_{ij}^k - S_{ij}^s\right)}_{8\,\text{inputs}\ (i,\,j=1,2)}, \underbrace{\Omega_1^k, \ldots, \Omega_{P_k}^k}_{P_k\ \text{outputs}} \right] \tag{4.59}$$

is submitted to a three-layer (MLP3) neural network structure for training using the *Neuromodeler* tool [38] (Fig. 4.6 (a)).

The input layer has 9 neurons (the 4 real and 4 imaginary parts in (4.57) and the operating frequency f) while the output layer contains P_k neurons. The hidden layer is composed of 22 to 45 neurons depending on the circuit data file under training.

It has to be noted that once the inputs and outputs are identified, three sets of data namely, the training data, the validation data, and the test data, need to be generated for the neural network development. Training data is used to guide the training process, i.e., to update the neural network weights during training. Validation data is used to monitor the quality of the neural model during training. Test data is used to examine the final quality of the developed model.

Suppose the range of input parameters over which the neural model would be used is $[\boldsymbol{x}_{min}, \boldsymbol{x}_{max}]$. Therefore, validation data, test data, and training data should be generated in the same range as well, selecting a sampling strategy and an adequate step size. Grid, star, central-composite, or random distributions are possible.

Prior to further discussion, two points had to be considered in the present work. First, the input parameter space is of high-dimension and the step sizes should be small enough to assure good convergence. This will lead to a too large number of combinations of input parameters. Second, even after selecting the most suitable topology, the values of the elements of set $\{\Omega^{s}\}$ obtained after the first round of extraction, i.e., use the standard topology need to be tuned in the final circuit along with the neural outputs, i.e., the elements of set $\{\Omega^{k}\}$.

An optimization loop is then essential. Therefore, instead of generating large data files required for a classical neural development, we used the values of the following vector

$$\Omega = \left[\Omega_1^{k},\ldots,\Omega_{P_k}^{k},\Omega_1^{s},\ldots,\Omega_{P_s}^{s}\right]$$

as starting vector for the final optimization loop. Since this vector is very close to the final solution, this procedure will assure very fast convergence.

4.4 Application of Fuzzy Logic

4.4.1 Review of Fuzzy C-Means Clustering Technique

Fuzzy logic is a superset of conventional logic that has been extended to handle the concept of partial truth-truth values between “completely true” and “completely false”. As well, a fuzzy expert system is an expert system that uses a collection of fuzzy membership functions and rules to reason about data.

Fuzzy c-means (FCM) is the most used data clustering technique wherein each data point belongs to a cluster to some degree that is specified by a membership grade [39]. It provides a method of how to group data points that populate some multidimensional space into a specific number of different clusters. The idea of fuzzy clustering is to divide the data into fuzzy partitions, which overlap with each cluster. Therefore, the containment of each data to each cluster is defined by a membership grade in {0, 1}. Clustering in unlabeled data $X = \{x_i, i = 1, \ldots, N\}$ is the assignment of c number of partition labels to the vectors in X.

The problem of fuzzy clustering is to find the optimum membership matrix U = [$u_{ij} \in$ [0, 1], i = 1, ..., c; j = 1, ..., N] which minimizes the function 4.59.

$$J_m(U,v) = \sum_{k=1}^{N}\sum_{i=1}^{c}(u_{ik})^m \|x_k - v_i\|^2 \tag{4.60}$$

where m is an exponent that controls the degree of fuzziness, u_{ik} describes the belongness of x_i to cluster k,

$$u_{ik} = \left(\sum_{j=1}^{c}\left[\frac{\|x_k - v_i\|}{\|x_k - v_j\|}\right]^{\frac{2}{m-1}}\right)^{-1} \tag{4.61}$$

and v_i is the centroid of ith cluster,

$$v_i = \frac{\sum_{k=1}^{N}(u_{ik})^m x_k}{\sum_{k=1}^{N}(u_{ik})^m} \tag{4.62}$$

4.4.2 Application of FCM in This Work

In this work, FCM would be an efficient tool to identify the most suitable topology based on the following approach: For any circuit #k (k = 1, ..., 4), the related $S^{\mathbf{k}}$ matrix would be compared to the input $S^{\mathbf{m}}$ matrix over the whole frequency range, and each element of the two resulting 2x2 error matrices $E^{\mathbf{k},\mathbf{Re}}$ and $E^{\mathbf{k},\mathbf{Im}}$,

$$E_{ij}^{\mathbf{k},\mathbf{Re}} = \mathrm{Re}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{m}}\right) \quad i,j = 1,2 \tag{4.63}$$

$$E_{ij}^{\mathbf{k},\mathbf{Im}} = \mathrm{Im}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{m}}\right) \quad i,j = 1,2 \tag{4.64}$$

would receive a score scaled from 1 to 10 depending on its value.

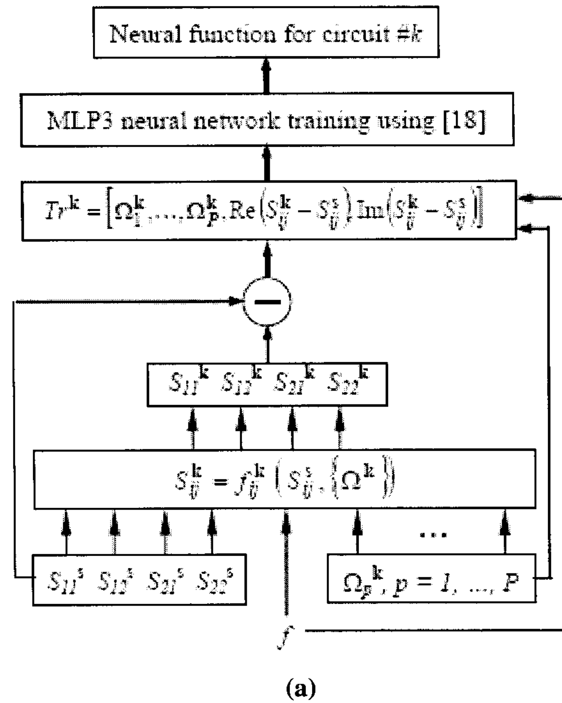
Therefore, the topology #k with smallest $E^{\mathbf{k},\,\mathbf{m}}$,

$$E^{\mathbf{k},\mathbf{m}} = \sum_{i=1}^{2}\sum_{j=1}^{2}\left[\mathrm{Re}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{m}}\right)\right]^2 + \left[\mathrm{Im}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{m}}\right)\right]^2 \tag{4.65}$$

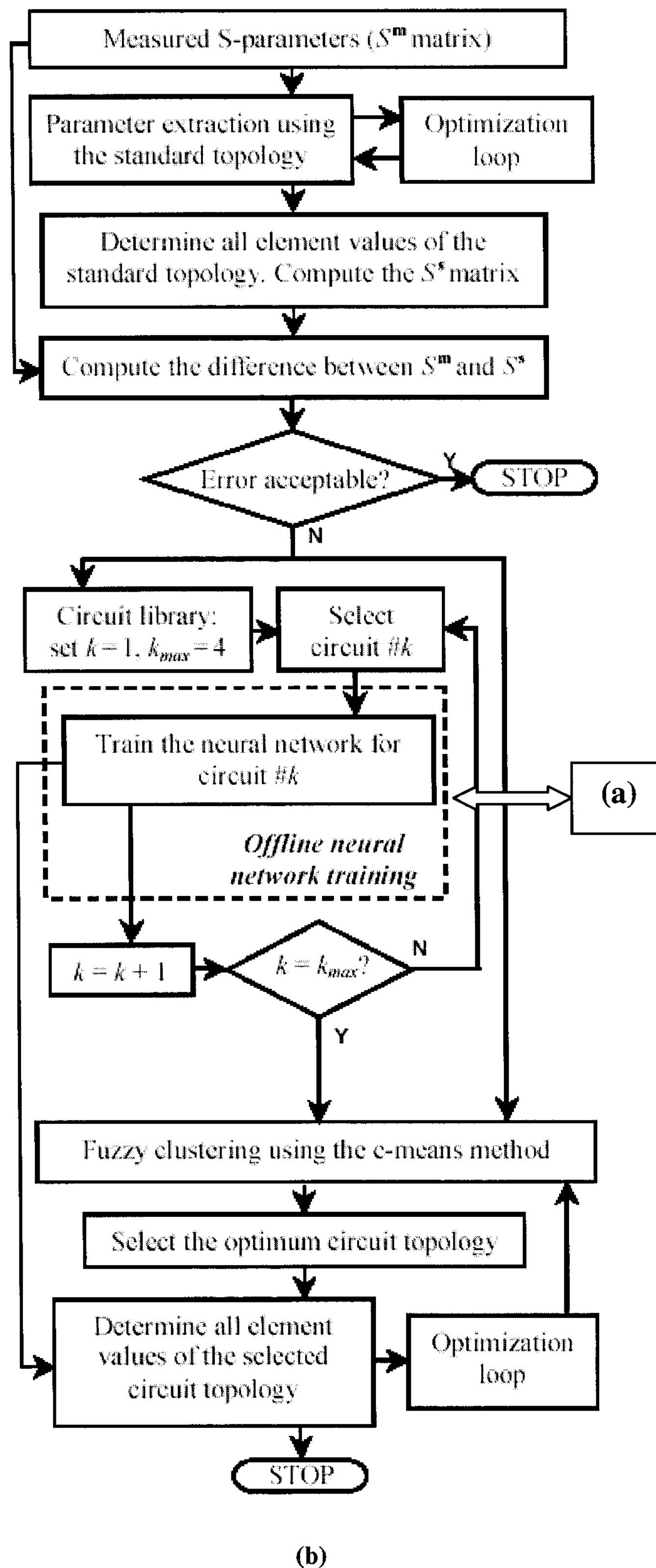
i.e., smallest score, would be selected as the most adequate circuit.

4.5 Proposed Method

The algorithm of the proposed method is shown in Figure 4.6. In this flow chart, the symbolic computation computed in Maple [37] was done by a PhD student. The rest was our contribution.



(a)



(b)

Figure 4.6 (a) Generation of the Neural Model for Circuit #k

(b) Algorithm of the adopted Method

4.6 Conclusion

In this chapter, a combined fuzzy-neural tool has been used for determining the most suitable small-signal FET equivalent circuit topology. By combining the Fuzzy c-means method [16] and the neural representation of a transistor behavior [3], the small-signal equivalent circuit parameters are efficiently evaluated through a fuzzy-neural network, based on an optimum selection of the more appropriate circuit topology of the active device. The method has been proven to be fast and accurate and three examples are listed for each transistor in the following chapter.

Chapter 5

Experiments and Results

5.1 Introduction

The adopted method described in this work was implemented and tested on HBT and FET, three examples for each. Those six examples will be presented with detailed explanations followed by the supporting data.

As previously mentioned, our new method for determining the transistors' small-signal equivalent circuits is quite suitable for microwave wafer probing equipment. However, since such a system is not yet in operation in our laboratory, the method was developed using data generated by ADS and assumed to be the measured input data except for the third FET example, which is obtained from datasheet provided by *Excelics* Semiconductor Company.

The implementation of the proposed method is written in C++ programming language and runs on MS-Windows operating systems. The executing time for this method varies depending on the size of the measured data and the requirement of the accuracy. Still, our method is proven to be efficient and accurate based on those examples.

5.2 HBT Examples

5.2.1 First Example for HBT

The data used in this example is collected from [22]. As the parameter values provided by [22] is from the standard topology, we use HBT small signal standard equivalent circuit with those parameter values to simulate in ADS with the frequency range of 1 to 15 GHz. In [22], the modeled AlGaAs/GaAs HBT contains two emitter fingers, each of which is 2mm wide and 10mm long. The biasing condition is $I_C = 15mA$ and $V_{CE} = 3V$.

After applying our method, the HBT topology #1, the standard topology, is selected as the most suitable topology and the element values extracted using our work are listed in Table 5.1 together with the original values of the measured data. The comparison among the measured S-parameters and the simulated S-parameters from four different topologies is presented in Figures 5.1- 5.8. The closest agreement between the measured (original data) and the simulated S-parameters from the standard topology is noted from these figures.

We use the following signs to present the original data and data from different topologies in all the figures listed in this chapter:

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— -- · —)	**Topology #3**
(—)	**Topology #4**
(— · —)	**Topology #5**

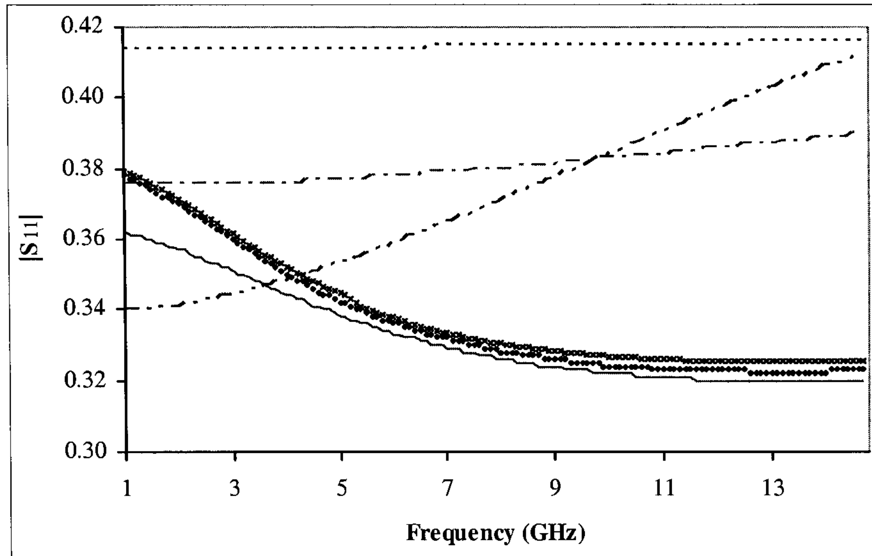


Figure 5.1 Magnitude of S11 in HBT Example 1

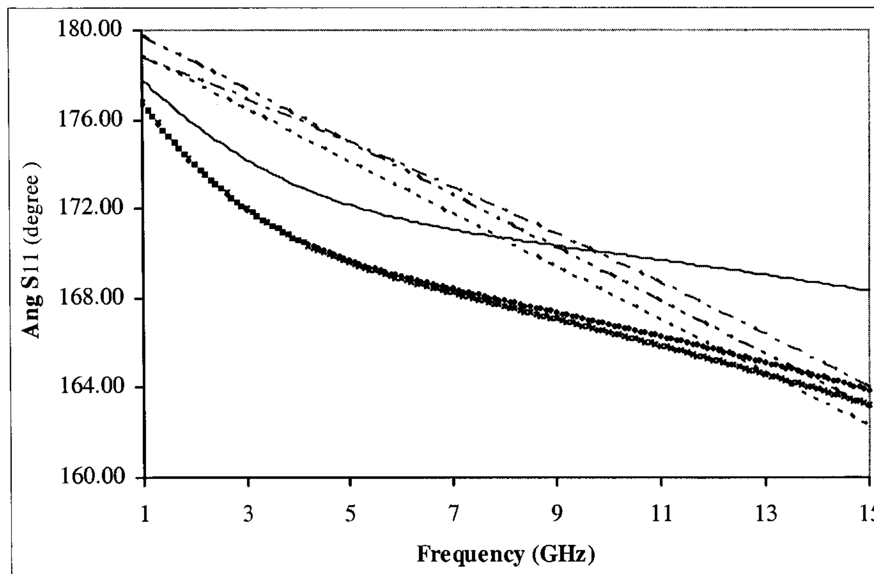


Figure 5.2 Angle of S11 in HBT Example 1

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

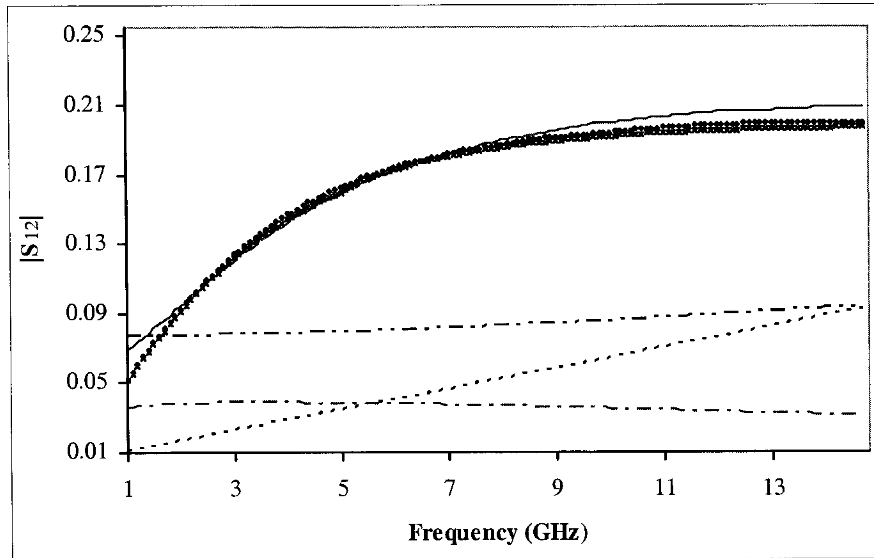


Figure 5.3 Magnitude of S12 in HBT Example 1

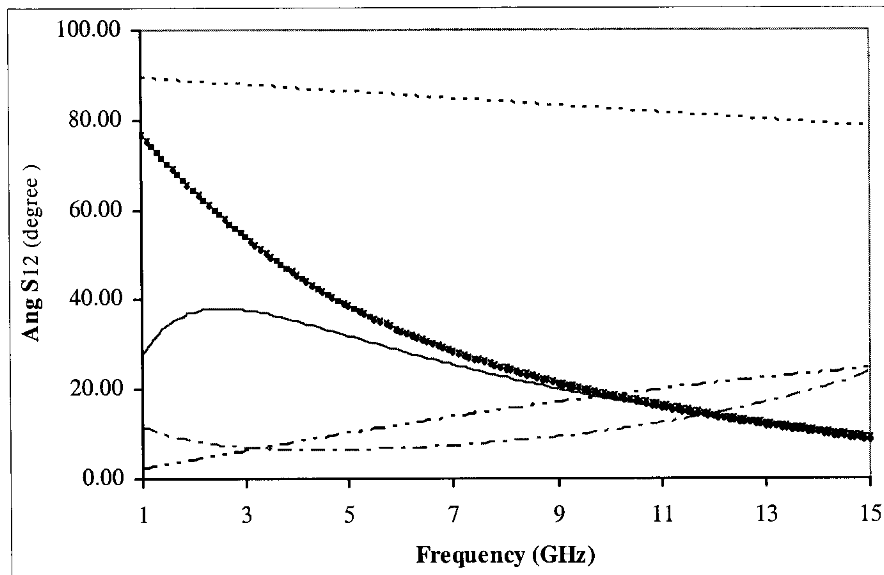


Figure 5.4 Angle of S12 in HBT Example 1

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— ⁻- —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

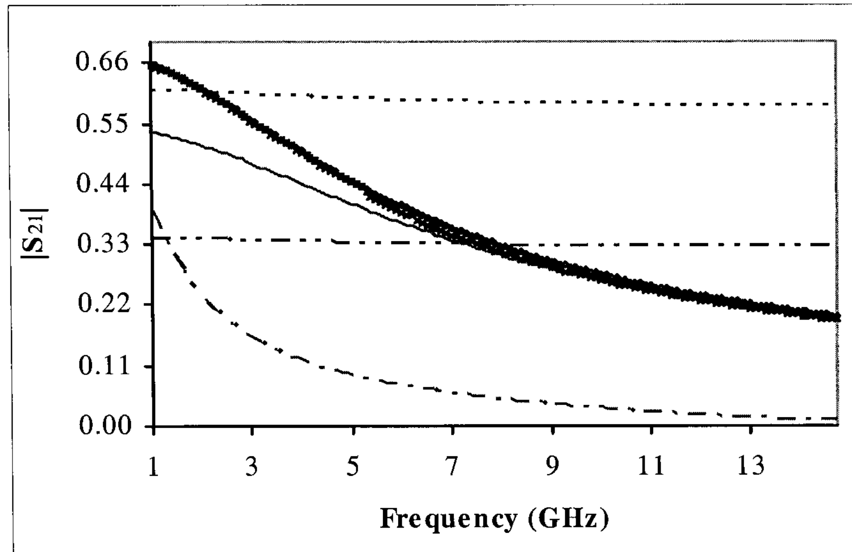


Figure 5.5 Magnitude of S21 in HBT Example 1

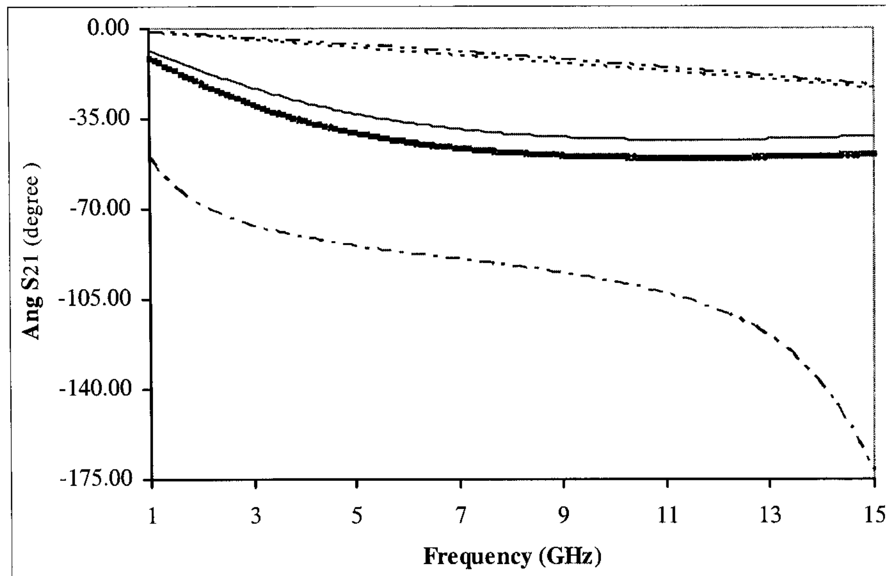


Figure 5.6 Angle of S21 in HBT Example 1

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— -- - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

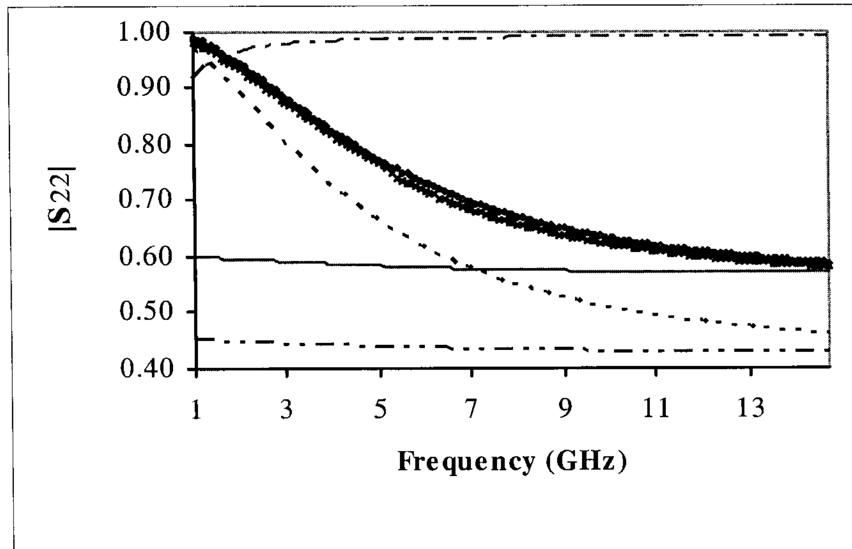


Figure 5.7 Magnitude of S22 in HBT Example 1

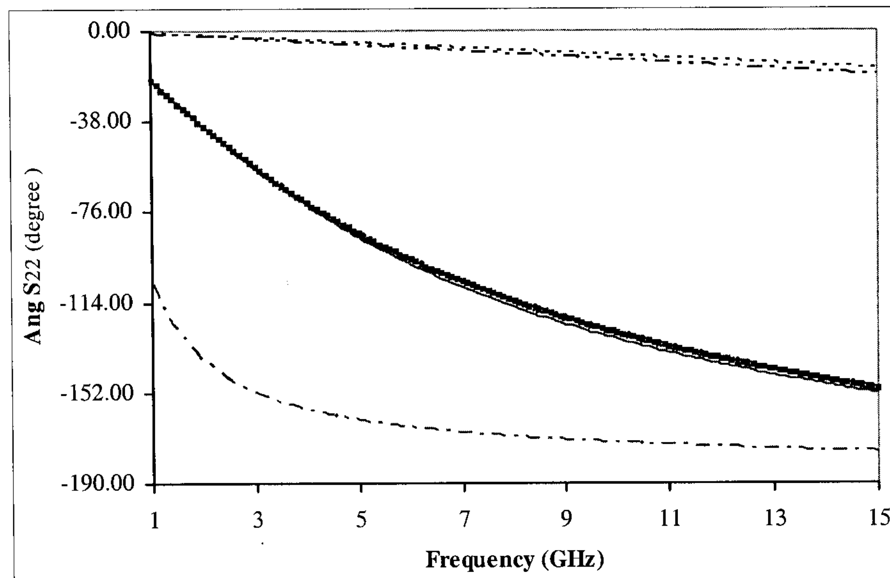


Figure 5.8 Angle of S22 in HBT Example 1

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— -- - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

name	original	extracted
R_e (Ohm)	5.34622	5.35561
R_c (Ohm)	9.576	9.5824
R_b (Ohm)	8.753	8.42922
L_e (pH)	15.18	14.1
L_c (pH)	50.41	50.7
L_b (pH)	45.534	44.8
C_{be} (pF)	0.649	0.661
C_x (pF)	0.023	0.0238
C_{bc} (pF)	0.047	0.0477
α_0	0.951	0.958224
τ (pS)	4.809	4.94
R_{be} (Ohm)	4.203	4.3751
R_{bc} (Ohm)	8.673	8.95604

Table 5.1 Parameter Values in HBT Example 1

5.2.2 Second Example for HBT

We use the data from [24] in this example. Here, an InP/InGaAs HBT is characterized which was fabricated from metal organic vapor phase epitaxy (MOVPE)-grown material, with $2\times10\,\mu m^2$ emitter area. The parameter values are provided in HBT topology #3 and thus simulated in ADS using the third topology from the HBT small-signal equivalent circuit library. The frequency range is 1 to 15 GHz.

The results of our method shows that the most suitable topology in this example is topology #3, which is exactly the topology used in generating original S-parameter data. The resulting parameter values are presented in Table 5.2 in comparison with the parameter values from the paper. The differences among the original S-parameters and the simulated S-parameters are shown in Figure 5.9- 5.16. It can be seen that the model #3 tracks the original data fairly well.

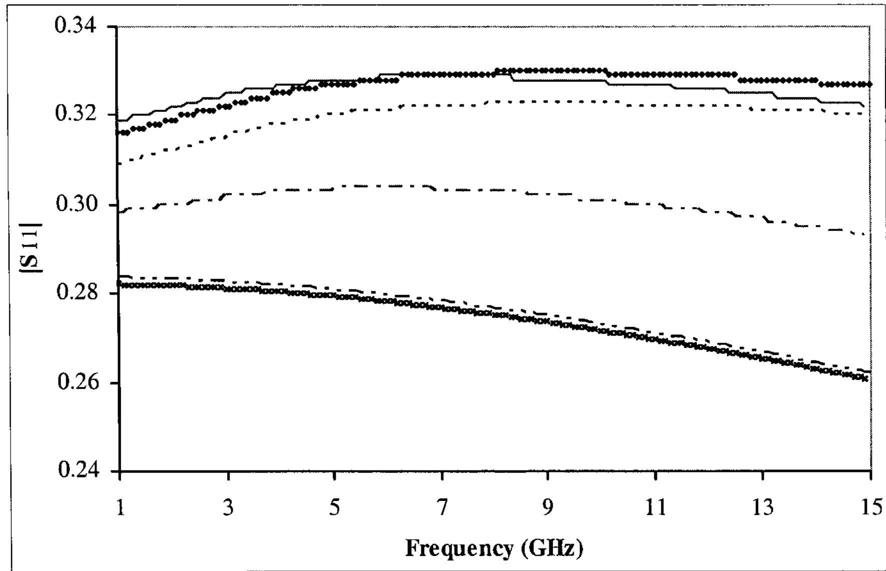


Figure 5.9 Magnitude of S11 in HBT Example 2

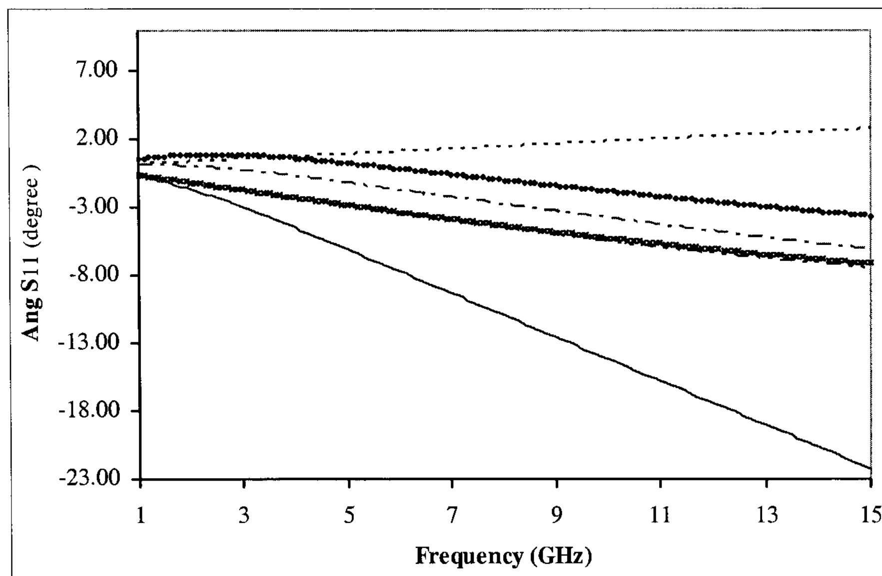


Figure 5.10 Angle of S11 in HBT Example 2

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— -- —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

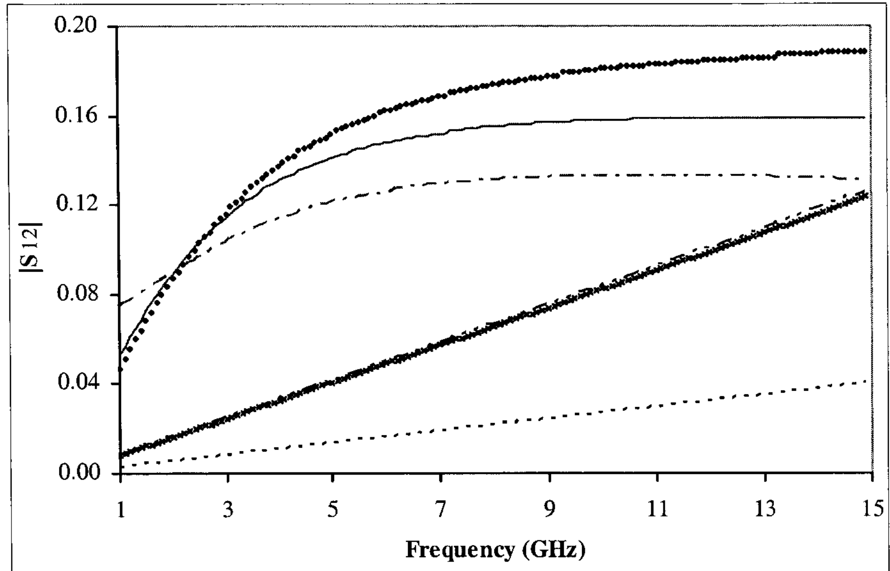


Figure 5.11 Magnitude of S12 in HBT Example 2

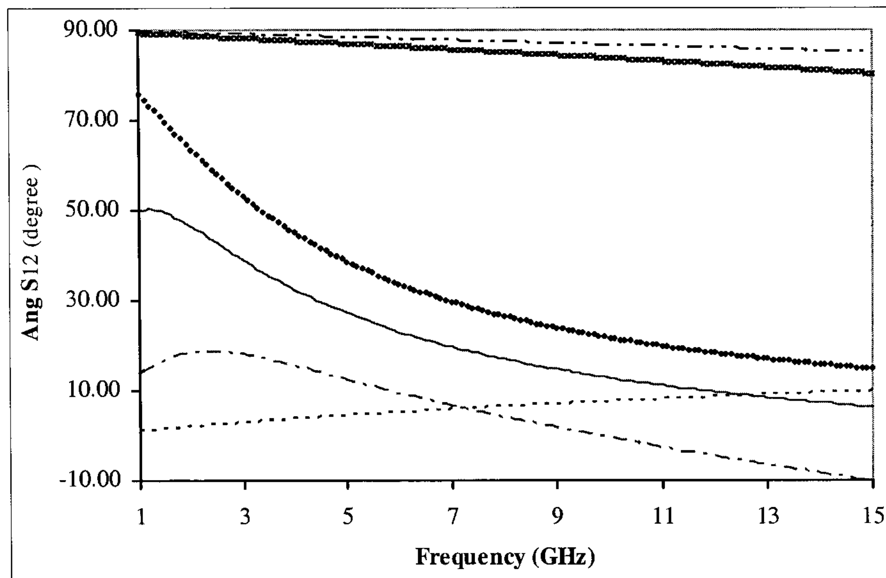


Figure 5.12 Angle of S12 in HBT Example 2

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

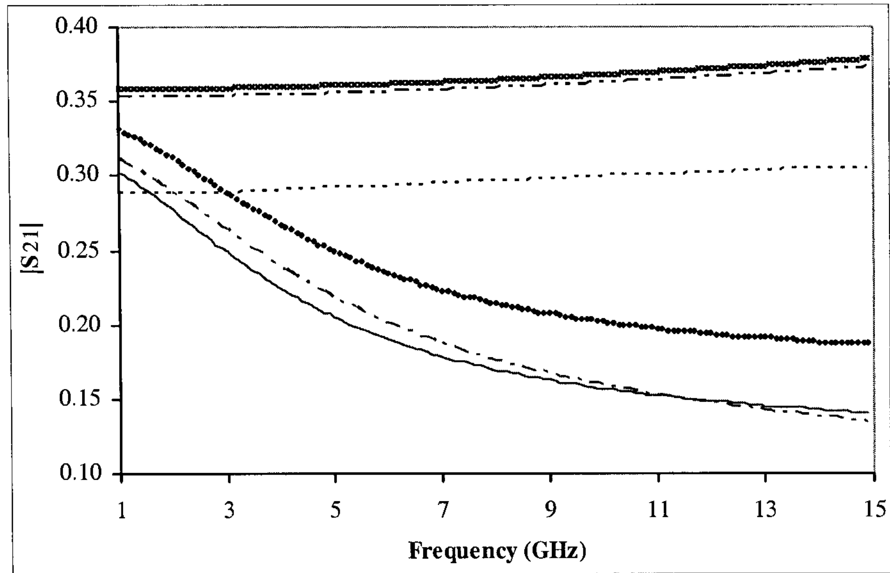


Figure 5.13 Magnitude of S21 in HBT Example 2

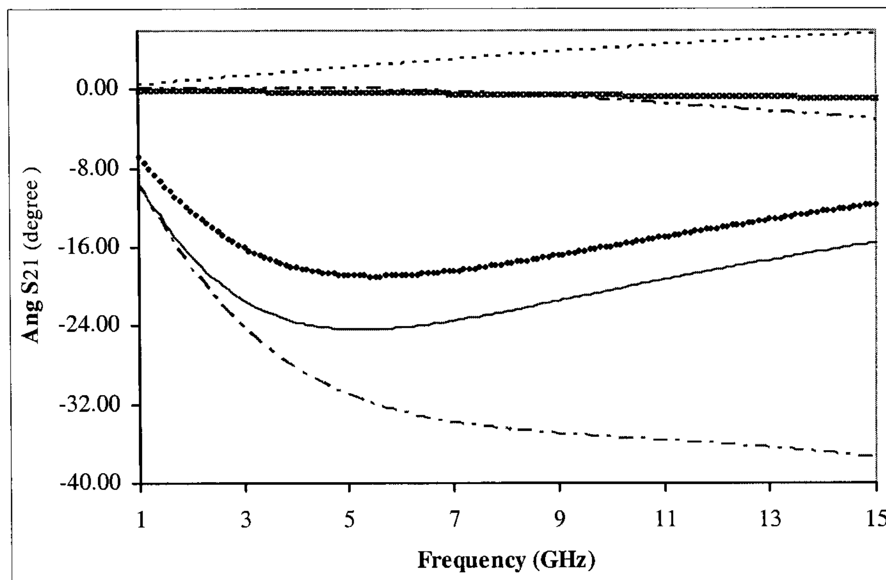


Figure 5.14 Angle of S21 in HBT Example 2

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— -- —)	**Topology #3**
(—)	**Topology #4**
(—-—)	**Topology #5**

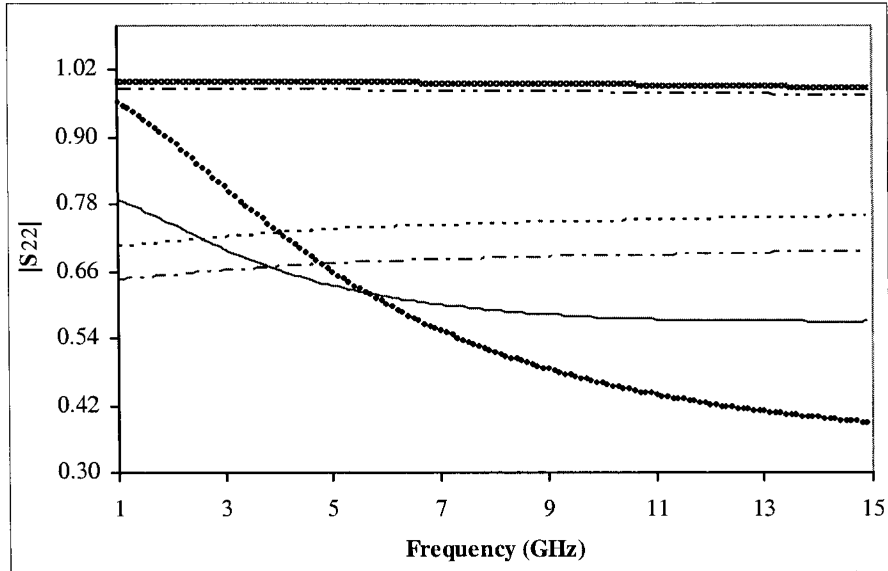


Figure 5.15 Magnitude of S22 in HBT Example 2

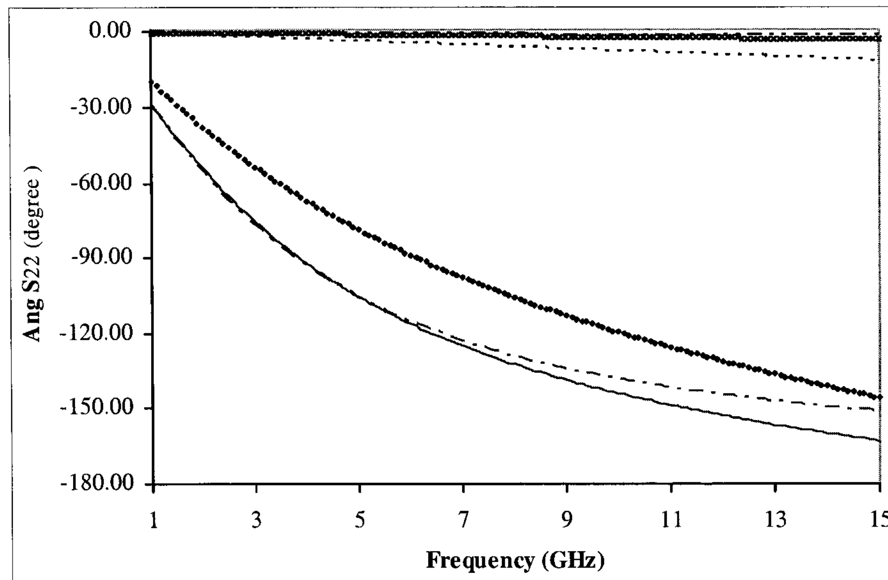


Figure 5.16 Angle of S22 in HBT Example 2

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— -- - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

Name	Original	Extracted
R_b (Ohm)	1.03E+01	1.36E+01
R_e (Ohm)	1.10E+01	1.09E+01
R_c (Ohm)	7.00E+00	7.15E+00
L_b (pH)	5.20E+01	5.03E+01
L_e (pH)	3.50E+01	3.42E+01
L_c (pH)	5.50E+01	5.70E+01
C_{b1} (pF)	6.80E-01	7.04E-01
τ (ps)	6.60E-01	6.67E-01
α_0	9.95E-01	1.00E+00
R_{bc} (Ohm)	7.00E+01	7.66E+01
C_{bc} (fF)	7.00E+00	7.39E+00
R_{b2} (Ohm)	1.00E+06	1.07E+06
C_{be} (fF)	5.30E+01	5.48E+01
R_{be} (Ohm)	7.00E+00	7.81E+00
C_{x1} (fF)	2.20E+01	2.57E+01
R_{c1} (Ohm)	5.00E+00	5.21E+00

Table 5.2 Parameter values in HBT example 2

5.2.3 Third Example for HBT

InP/GaInAs HBTs with emitter area $1\times10\,\mu m^2$ are modeled in this example at $V_{CE}=1.5V$ and $I_C=8.7\,mA$. The parameter values are provided by [25] using topology #4. Still, we use this set of parameter values to generate the original S-parameters in ADS with frequency range 1 to 15 GHz. The result of employing the proposed method shows that the simulated S-parameters from topology #4 best suits the original S-parameters and thus topology #4 is the most suitable one in this case. The comparisons of the S-parameters are shown in Figure 5.17-5.24. The parameter values in this example are given in Table 5.3.

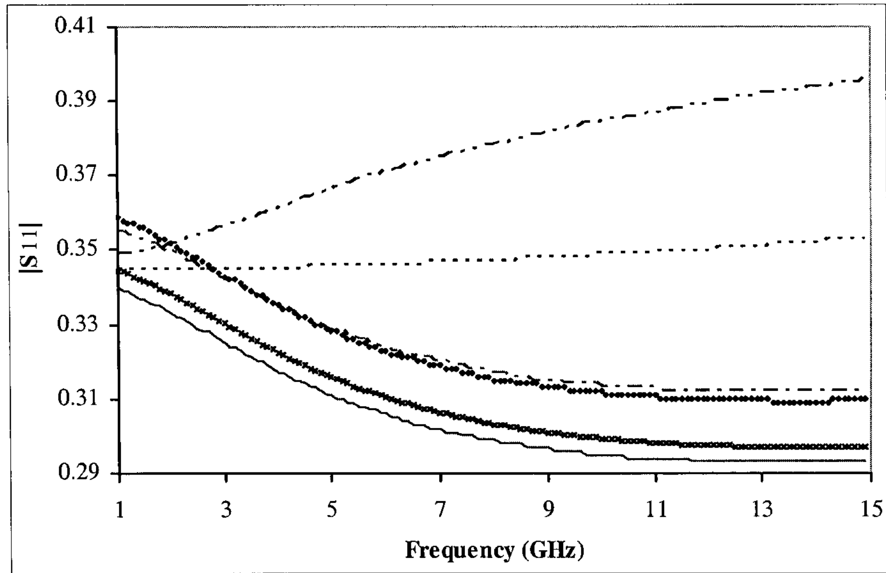


Figure 5.17 Magnitude of S11 in HBT Example 3

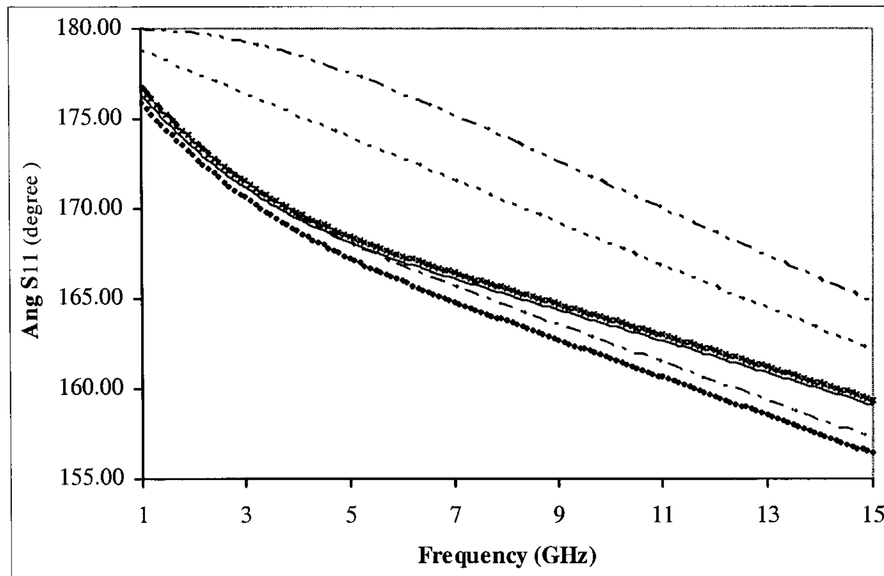


Figure 5.18 Angle of S11 in HBT Example 3

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

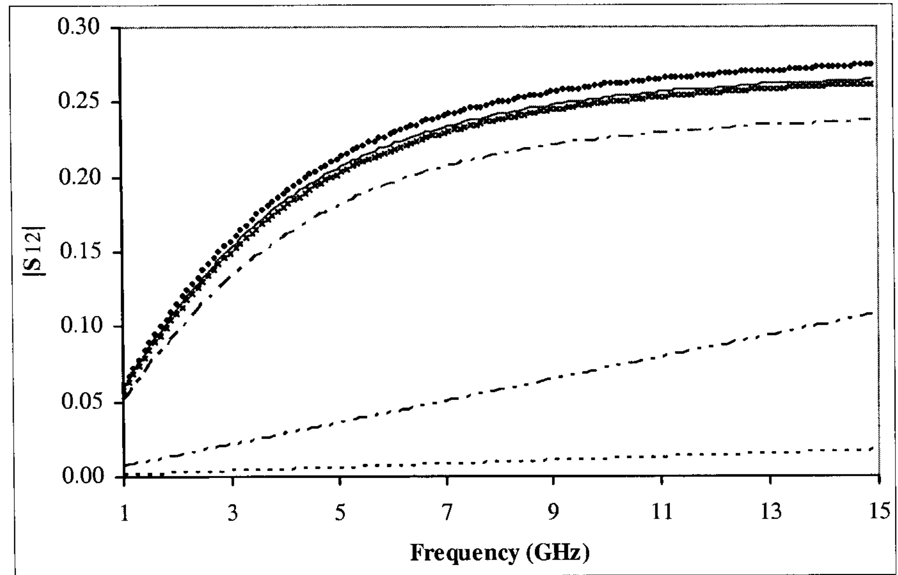


Figure 5.19 Magnitude of S12 in HBT Example 3

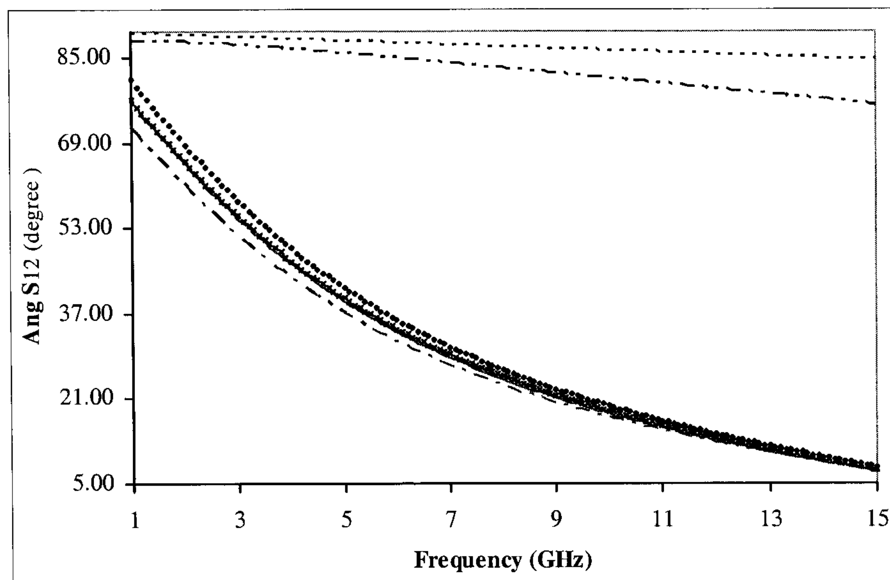


Figure 5.20 Angle of S12 in HBT Example 3

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

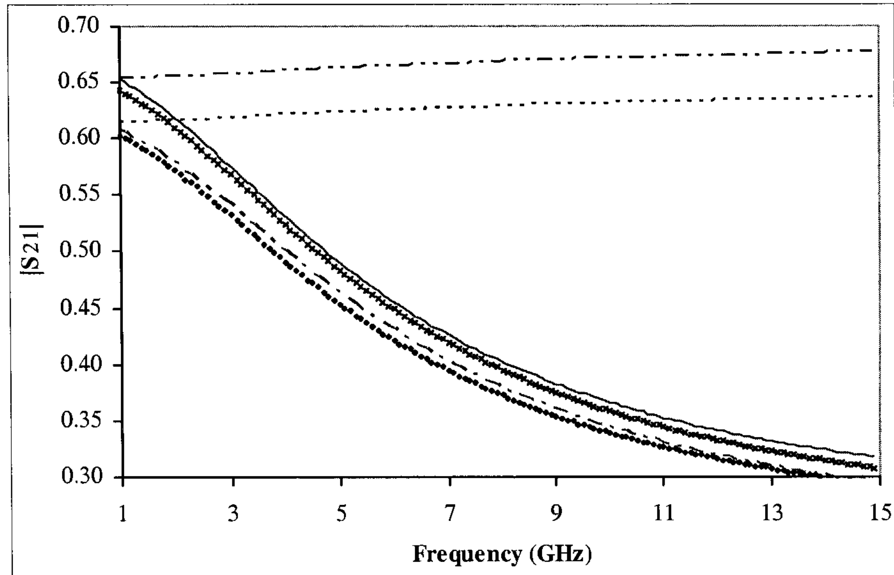


Figure 5.21Magnitude of S21 in HBT Example 3

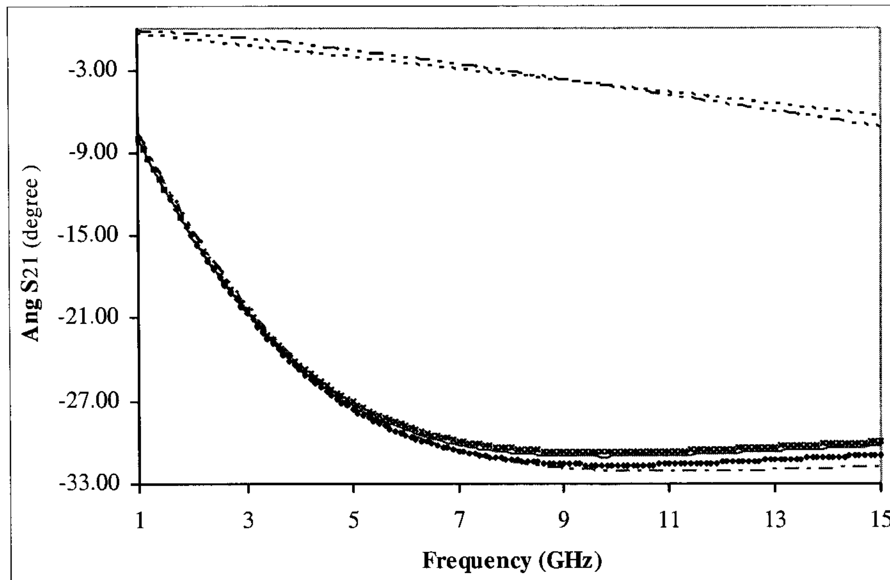


Figure 5.22 Angle of S21 in HBT Example 3

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

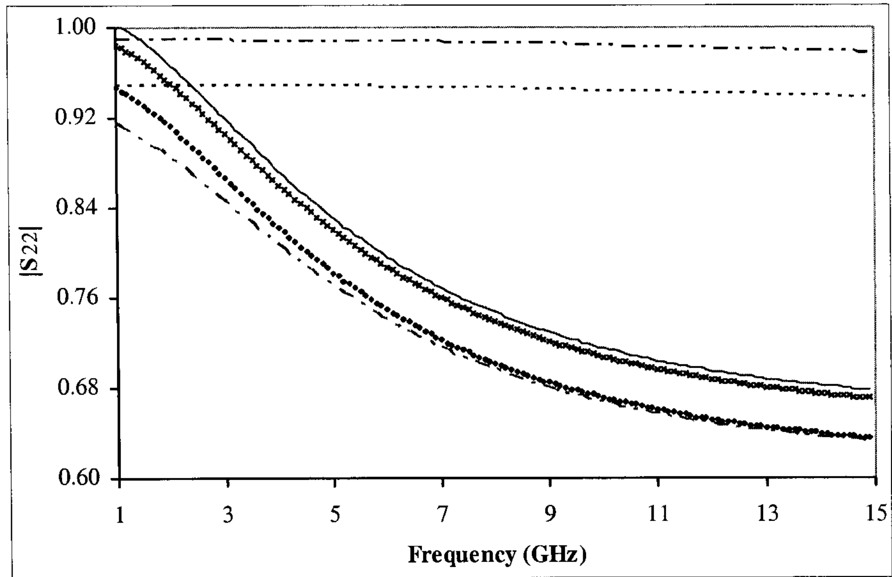


Figure 5.23 Magnitude of S22 in HBT Example 3

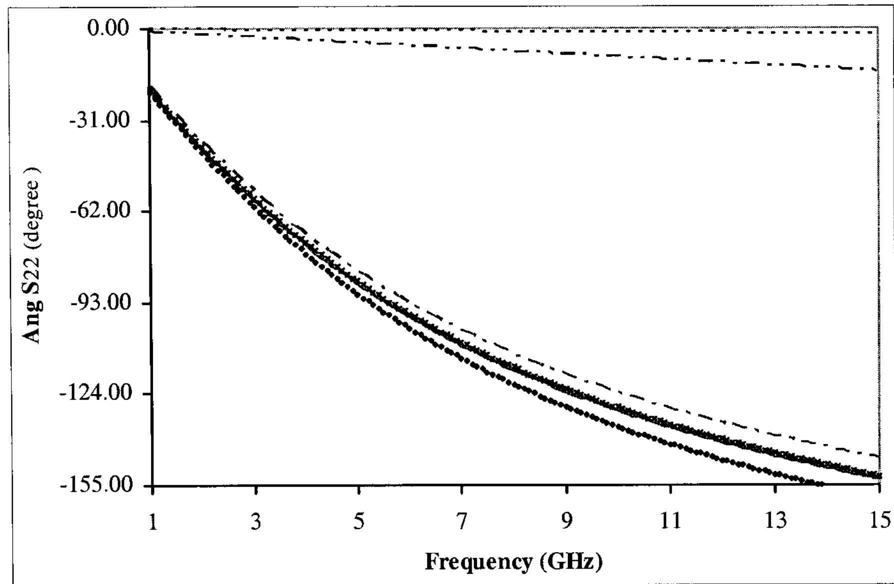


Figure 5.24 Angle of S22 in HBT Example 3

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**
(— - —)	**Topology #5**

Name	Original	Extracted
R_b (Ohm)	2.6	2.50612
L_b (pH)	60	60.6711
R_c (Ohm)	0.85	0.898718
L_c (pH)	65	67.3676
R_e (Ohm)	8.73	8.9191
L_e (pH)	1.8	1.81585
C_{bc1} (fF)	2	1.63547
C_{ce1} (fF)	3	3.36447
R_{bc} (Ohm)	15.4	15.5211
C_x (fF)	31	35.7776
C_{bc} (fF)	5.1	5.72441
R_{b2} (kOhm)	30	30.3549
C_{be} (fF)	10	8.99109
R_{be} (Ohm)	3.4	3.37499
α_0	0.947	0.927491
τ (ps)	0.64	0.608245

Table 5.3 Parameter Values in HBT example 3

5.3 FET Examples

5.3.1 First Example for FET

The first example for FET uses the data from [30] which models a $0.6\mu m$ heterostructure FET with $V_{ds} = 1.00V$, $V_{gs} = 0.60V$ and $I_{ds} = 5.17mA$. The topology used here is the standard one. The frequency range is from 1 to 15 GHz. As noted, best agreement is obtained for the simulated S-parameters from topology #1 and the original S-parameters. Figure 5.25- 5.32 give the direct comparison of simulated S-parameters for different topologies and the original one. The parameters are outlined in Table 5.4.

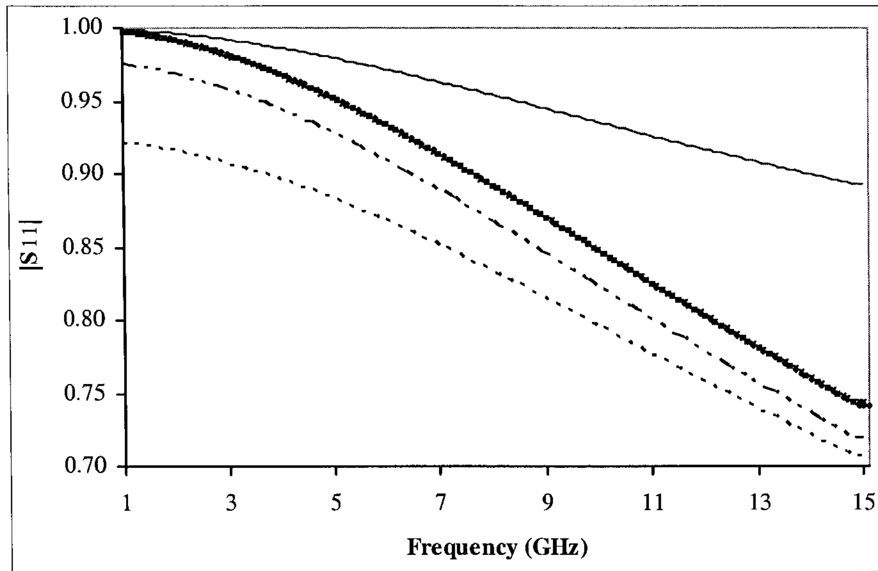


Figure 5.25 Magnitude of S11 in FET Example 1

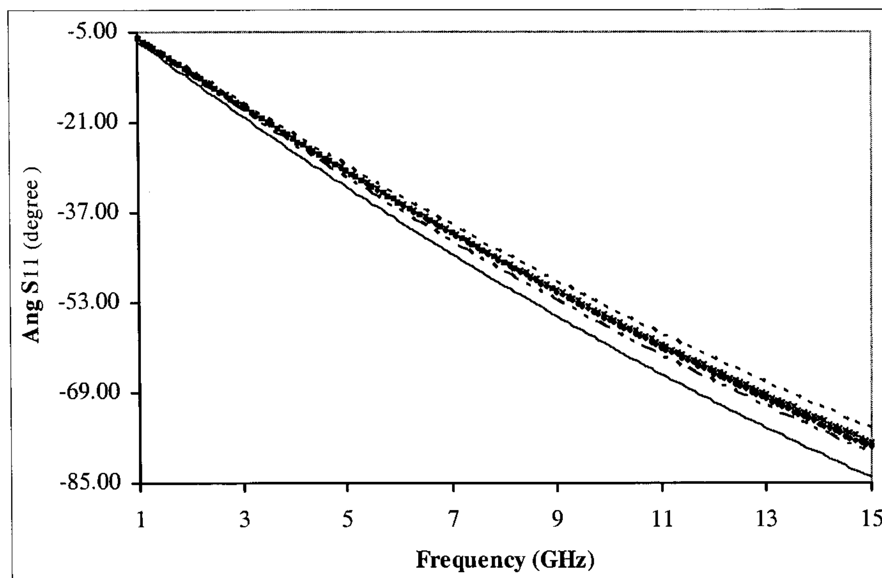


Figure 5.26 Angle of S11 in FET Example 1

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— – - —)	**Topology #3**
(—)	**Topology #4**

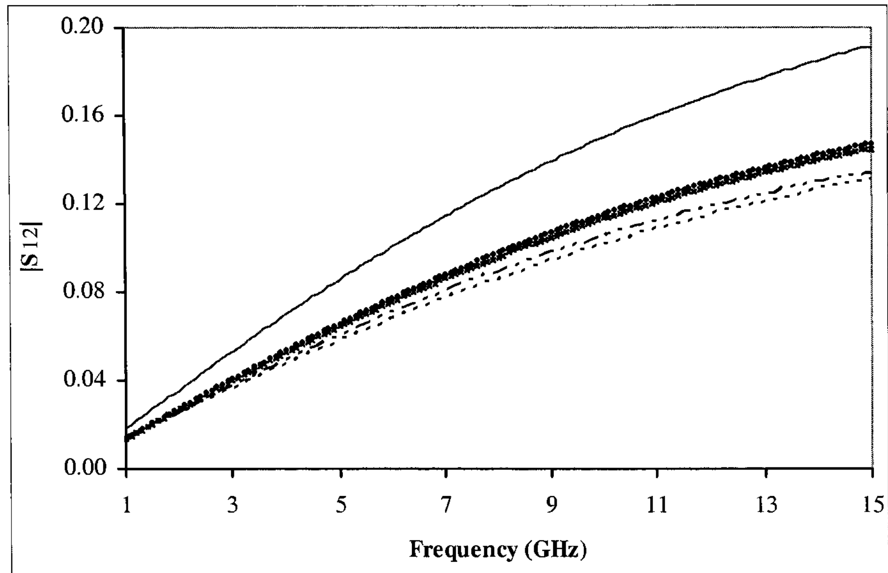


Figure 5.27 Magnitude of S12 in FET Example 1

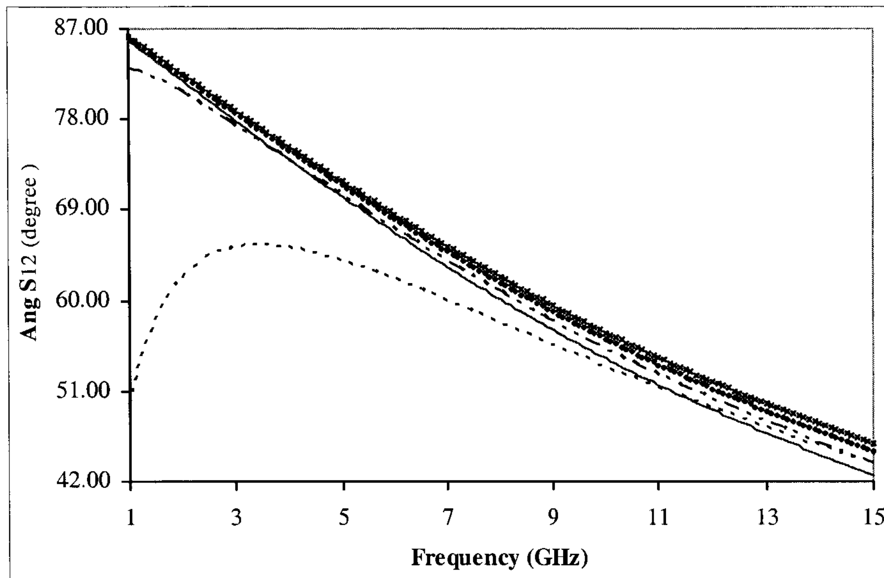


Figure 5.28 Angle of S12 in FET Example 1

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**

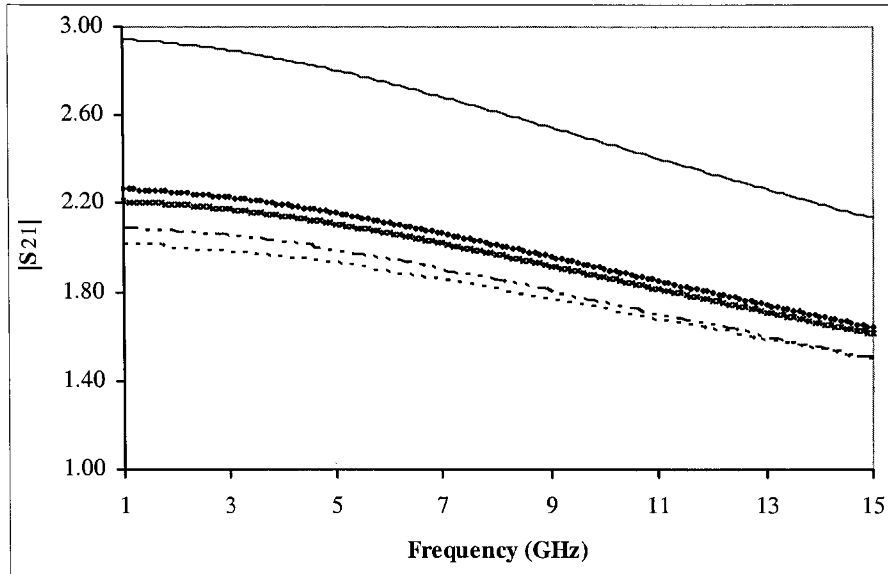


Figure 5.29 Magnitude of S21 in FET Example 1

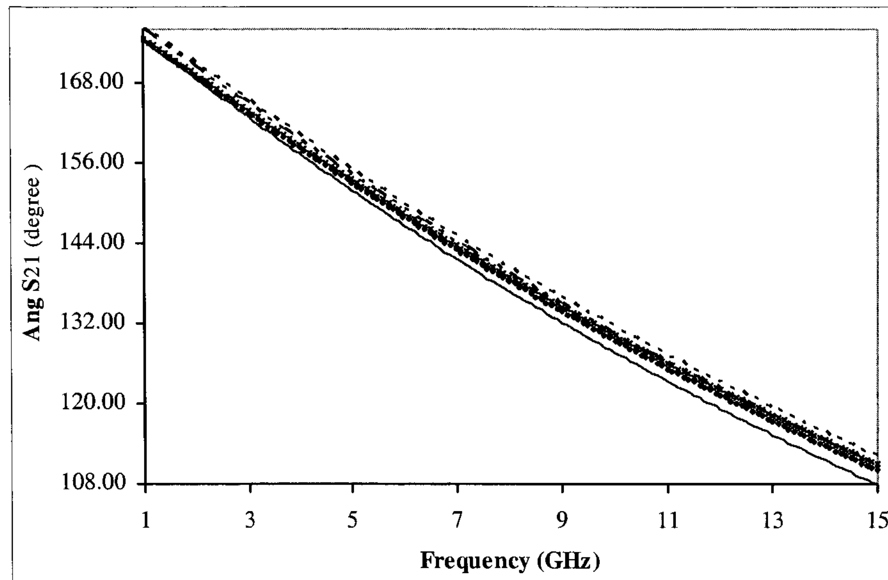


Figure 5.30 Angle of S21 in FET Example 1

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— ‒ - —)	**Topology #3**
(—)	**Topology #4**

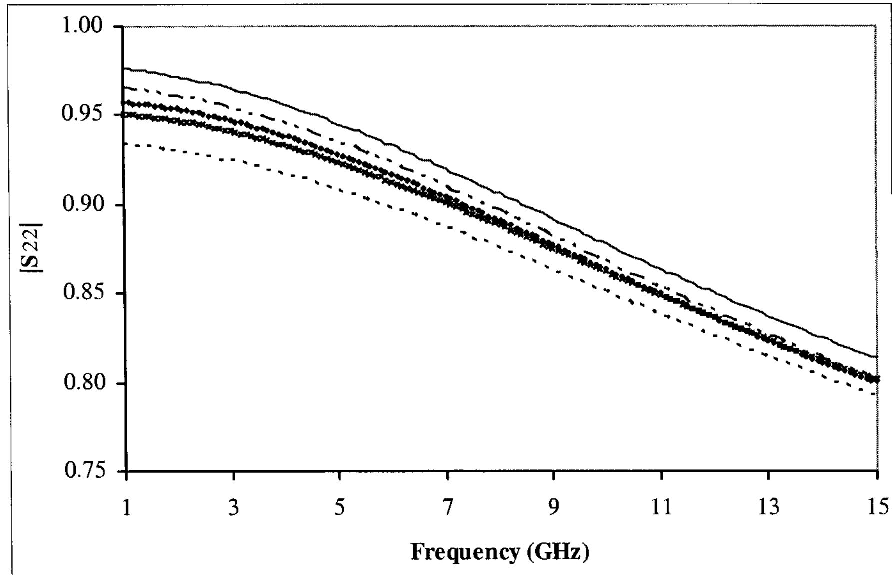


Figure 5.31 Magnitude of S22 in FET Example 1

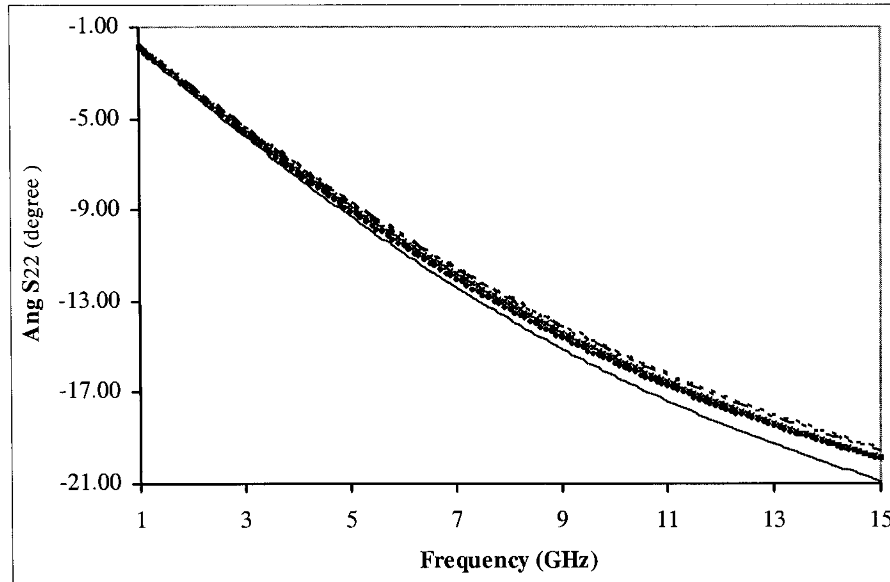


Figure 5.32 Angle of S22 in FET Example 1

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**

Name	Original	Extracted
R_s (Ohm)	10.6	10.547
R_d (Ohm)	12.4	12.338
R_g (Ohm)	4.2	4.179
L_s (pH)	0	0.000971
L_d (pH)	23.5	23.6912
L_g (pH)	44.8	45.1782
R_i (Ohm)	9.5	8.99848
g_m (mS)	30.31	31.2839
g_{ds} (mS)	0.66	0.572505
τ (pS)	1.61	1.70401
C_{gs} (fF)	152.58	156.293
C_{gd} (fF)	21.42	21.8938
C_{ds} (fF)	3.78	3.5789

Table 5.4 Parameter Values in FET example1

5.3.2 Second Example for FET

We use the data provided in [40] here. [40] models AlGaAs/InGaAs-GaAs PHEMT with bias point at $V_{gs} = 0.3V$, $V_{ds} = 2V$. The model used here is topology #3. The frequency range is from 1 to 15 GHz.

Still, our method works steady and selected topology #3 as the most suitable one. In figure 5.33-5.40, best agreement could be found between the original data and the one simulated by topology #3.

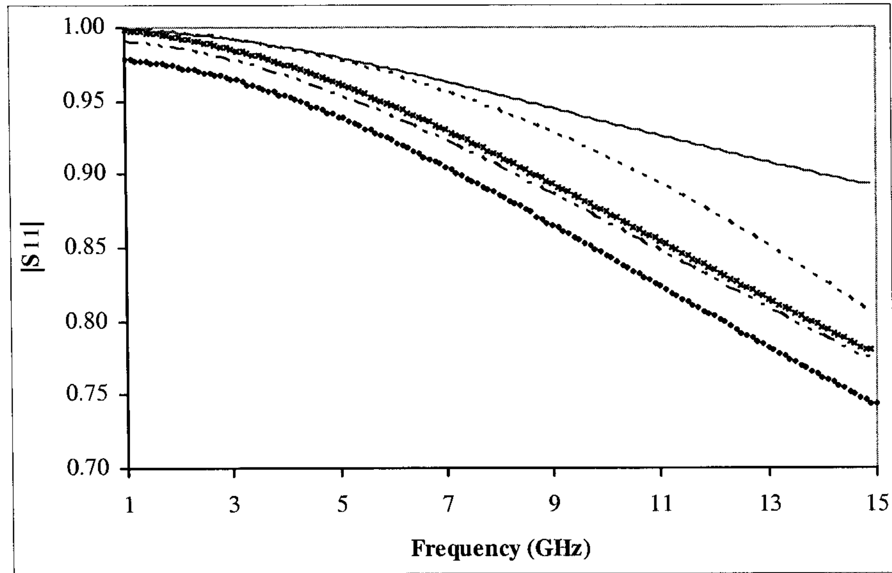


Figure 5.33 Magnitude of S11 in FET Example 2

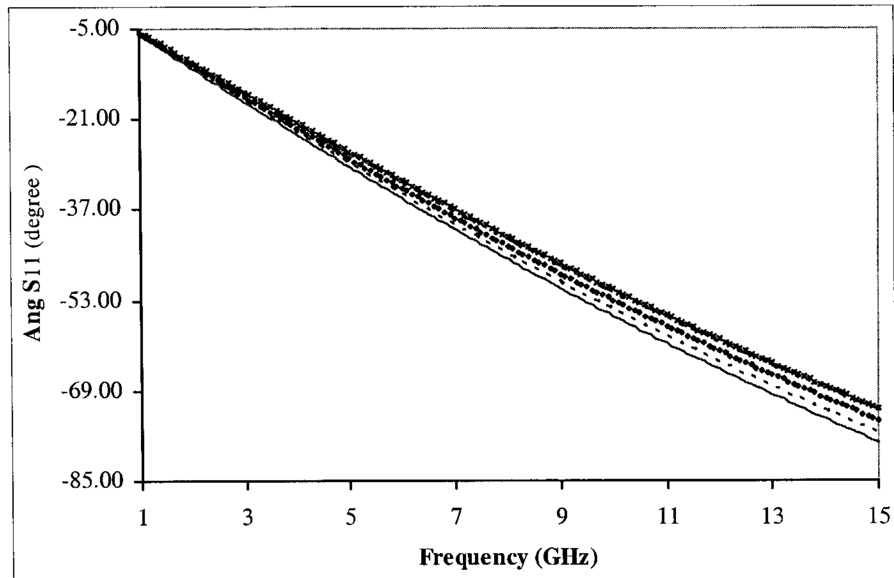


Figure 5.34 Angle of S11 in FET Example 2

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**

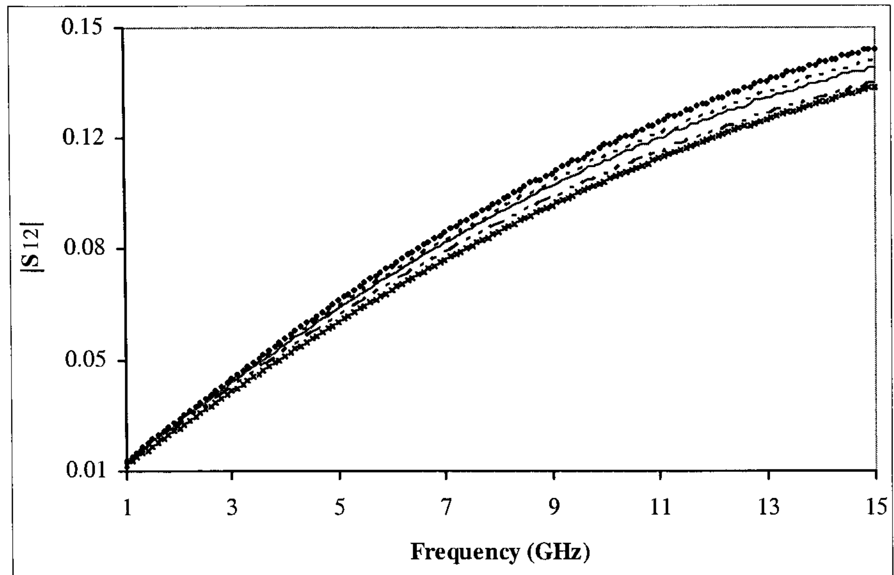


Figure 5.35 Magnitude of S12 in FET Example 2

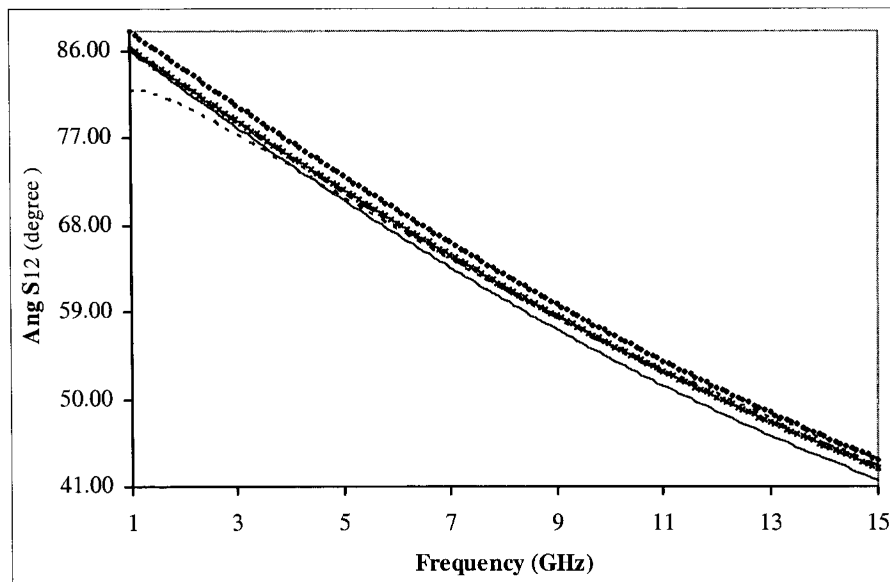


Figure 5.36 Angle of S12 in FET Example 2

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**

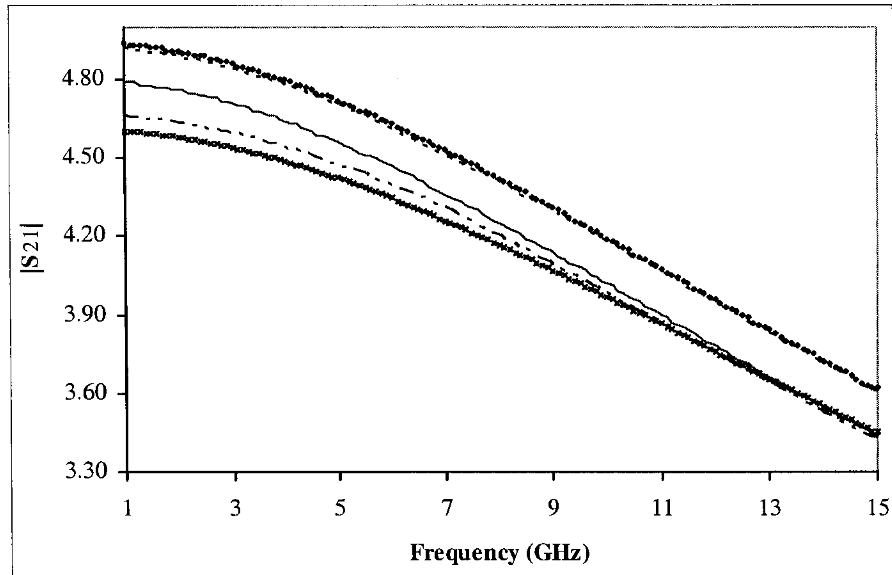


Figure 5.37 Magnitude of S21 in FET Example 2

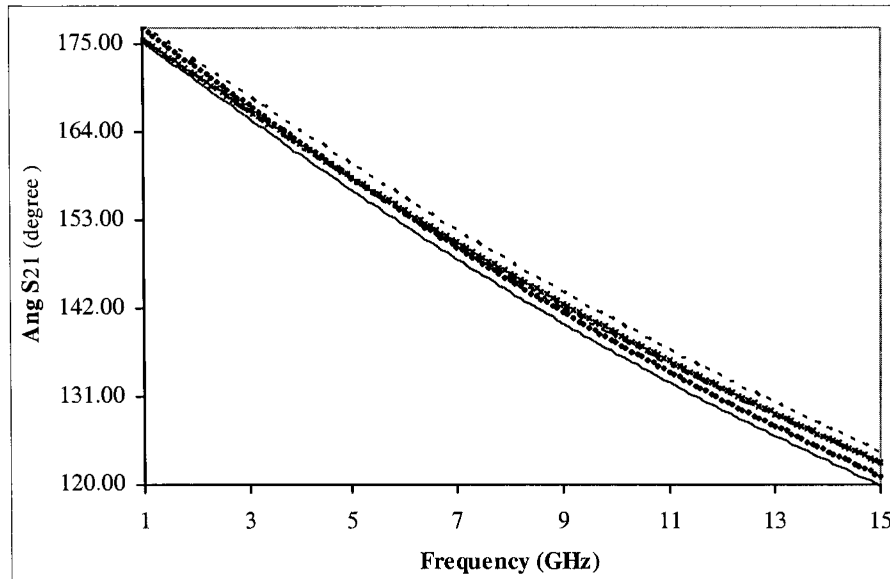


Figure 5.38 Angle of S21 in FET Example 2

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(‒ ‒ - ‒)	**Topology #3**
(—)	**Topology #4**

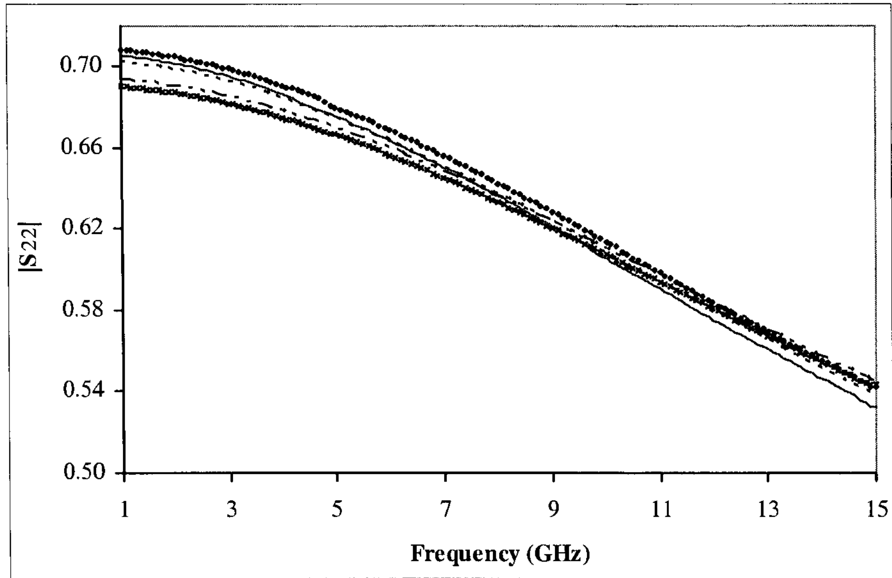


Figure 5.39 Magnitude of S22 in FET Example 2

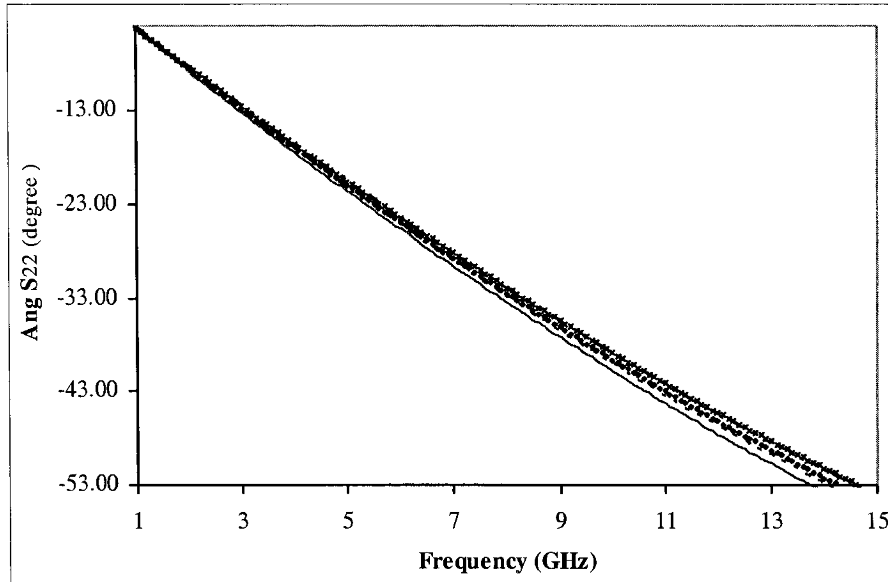


Figure 5.40 Angle of S22 in FET Example 2

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**

Name	Original	Extracted
L_g (nH)	0.0479	0.041933
R_g (Ohm)	7.97	8.13905
L_s (nH)	0.011	0.015668
R_s (Ohm)	2.68	2.73685
L_d (nH)	0.0257	0.01991
R_d (Ohm)	4.14	4.22748
C_{gdp} (fF)	3.01	2.91
R_{gs} (MOhm)	394	389.147
C_{gs} (fF)	86.4	85.3014
R_i (Ohm)	1.55	1.51087
R_{fd} (MOhm)	485	494.662
C_{gd} (fF)	18.8	22.7066
R_{gd} (Ohm)	10.4	8.84081
g_m (mS)	65.8	67.2806
τ (pS)	0.0977	0.069152
R_{ds} (Ohm)	227	233.077
C_{ds} (fF)	30.8	28.2091

Table 5.5 Parameter Values in FET example 2

5.3.3 Third Example for FET using datasheet

The device to be characterized is FET EPA018A GaAs power MESFET from *Excilics* Semiconductor Company. S-parameter for this device up to a frequency of 20 GHz at a bias point of $V_{ds} = 6V$ and $I_{ds} = 25mA$.

Our method showed that circuit #3 is the most appropriate which achieved a quite close agreement as expected, with a smaller final error, shown in Figure 5.41-5.48. The extracted values of circuit #3 is outlined in Table 5.6.

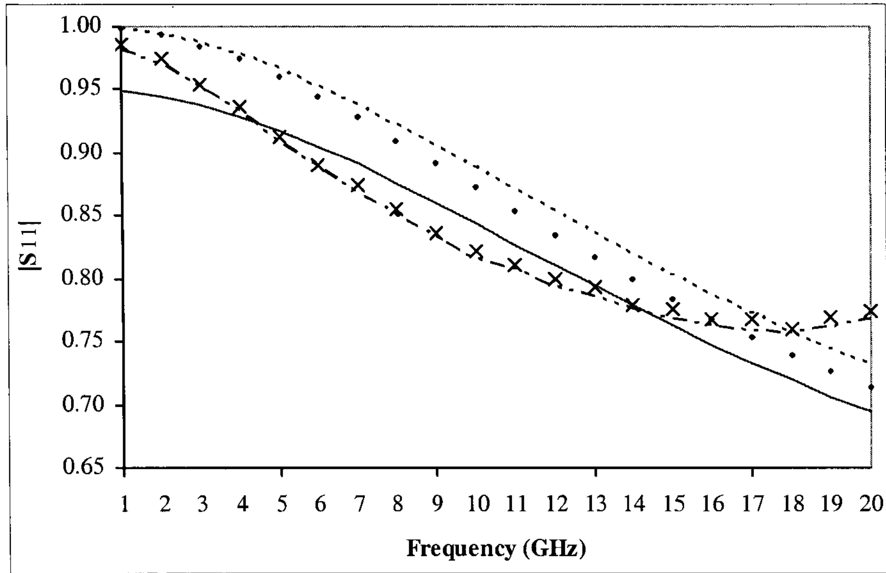


Figure 5.41 Magnitude of S11 in FET Example 3

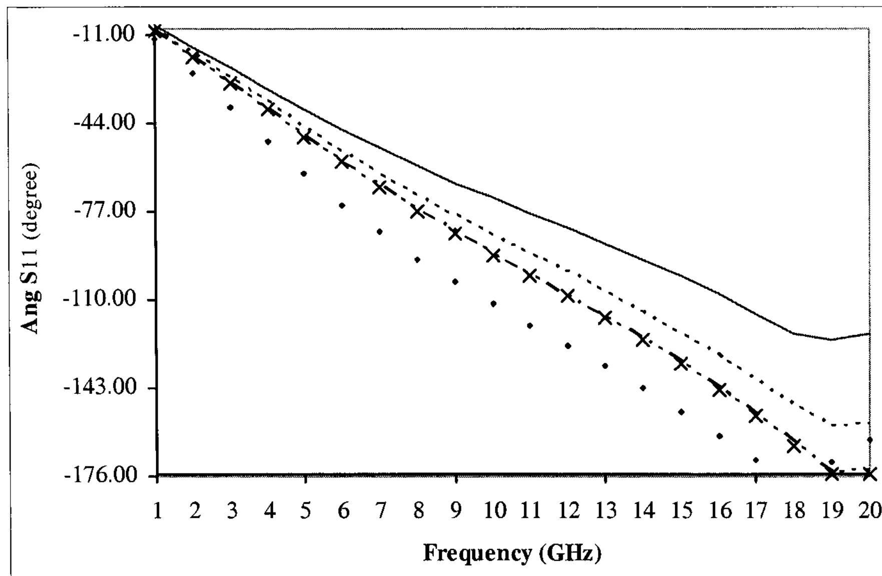


Figure 5.42 Angle of S11 in FET Example 3

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - - —)	**Topology #3**
(—)	**Topology #4**

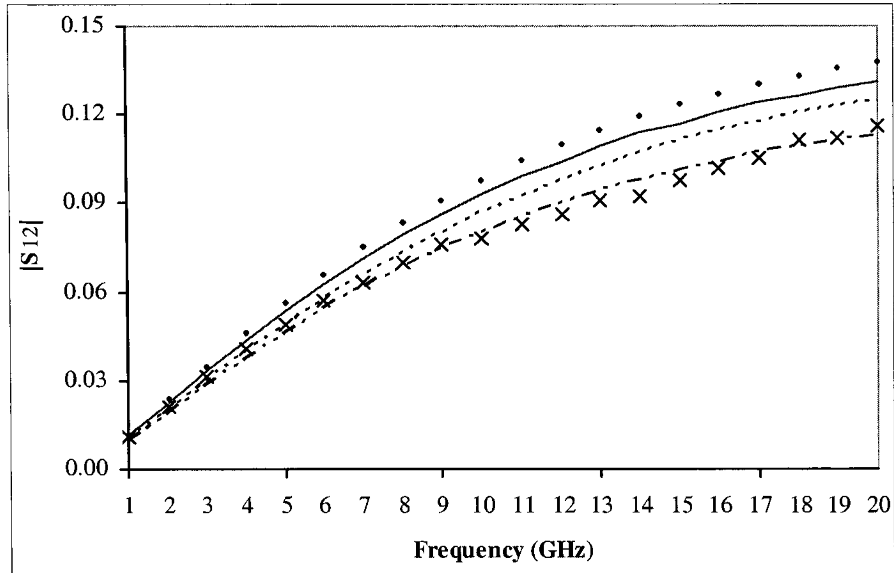


Figure 5.43 Magnitude of S12 in FET Example 3

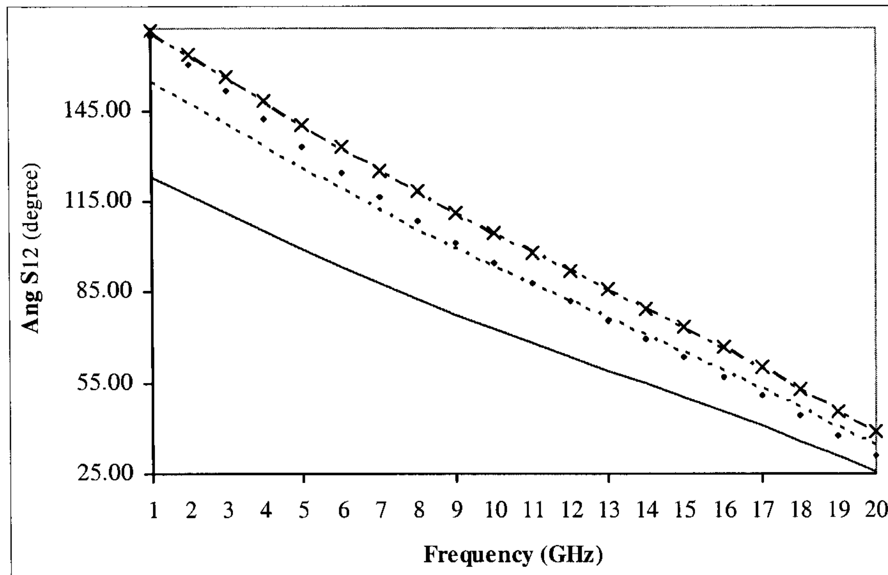


Figure 5.44 Angle of S12 in FET Example 3

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - . —)	**Topology #3**
(—)	**Topology #4**

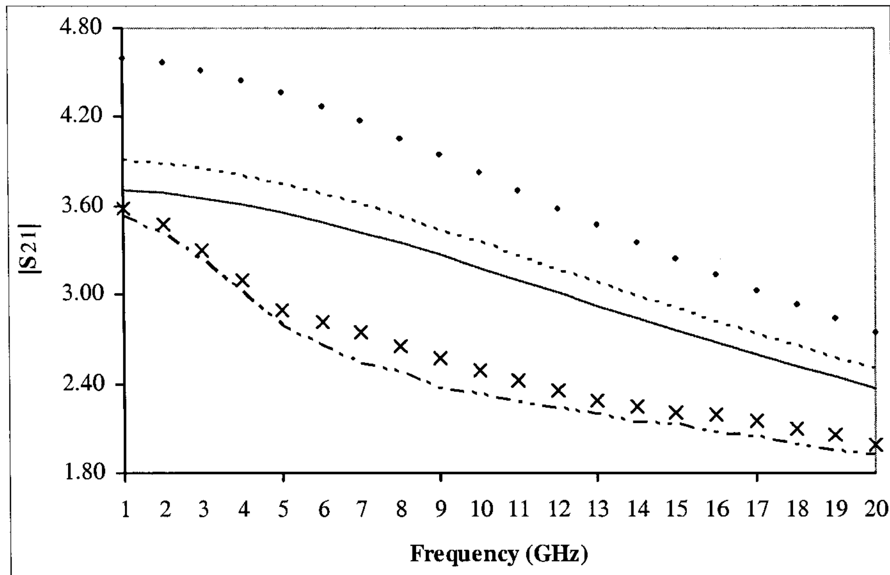


Figure 5.45 Magnitude of S21 in FET Example 3

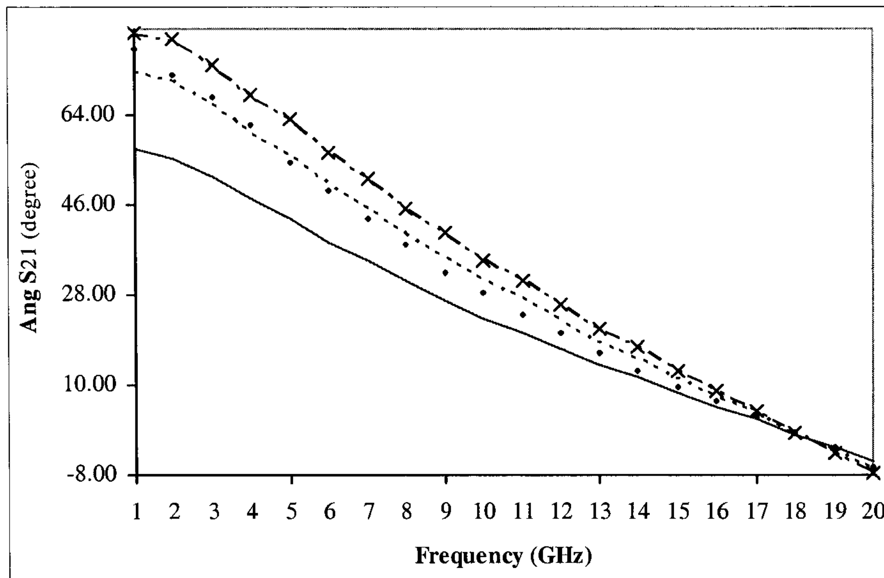


Figure 5.46 Angle of S21 in FET Example 3

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(— - —)	**Topology #3**
(—)	**Topology #4**

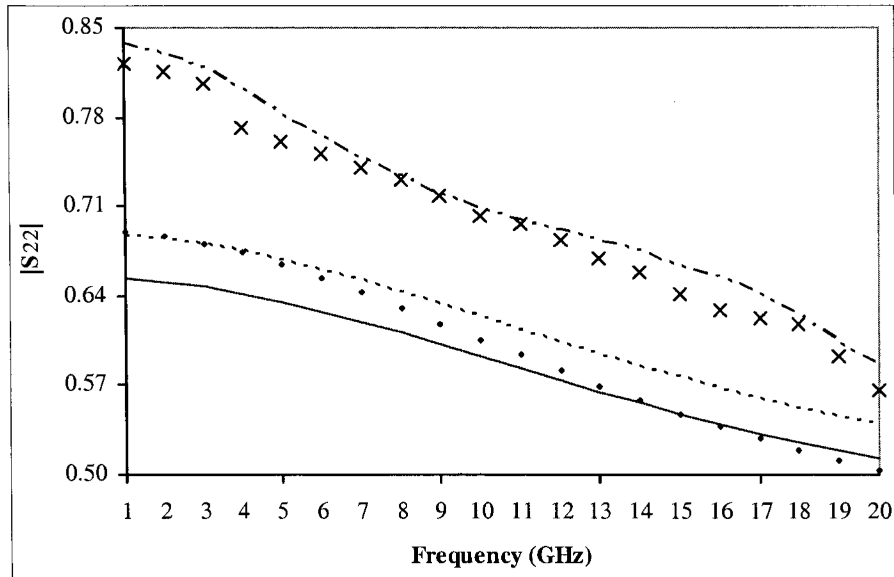


Figure 5.47 Magnitude of S22 in FET Example 3

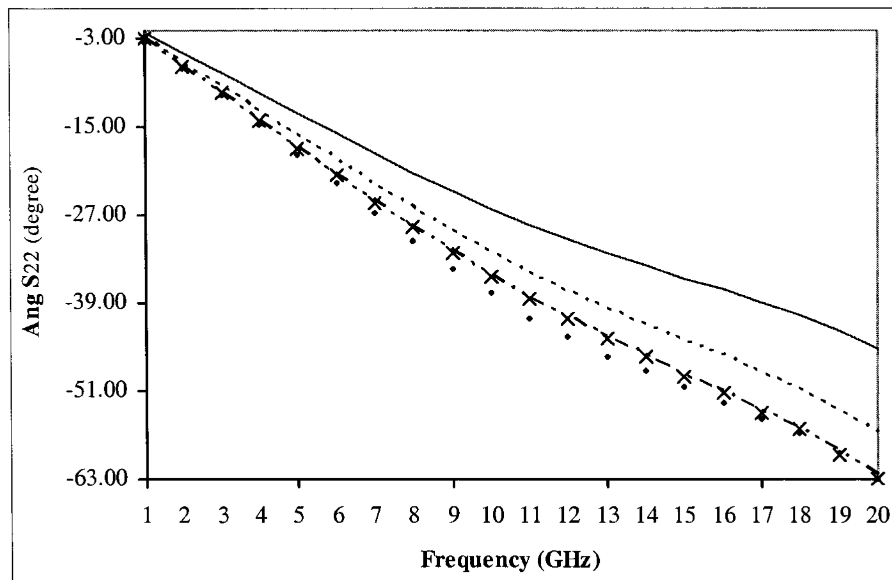


Figure 5.48 Angle of S22 in FET Example 3

(*)	**Original data**
(•)	**Topology #1**
(---)	**Topology #2**
(‒ ‒ - ‒)	**Topology #3**
(—)	**Topology #4**

Name	Extracted
R_g (Ω)	9.1
R_s (Ω)	7.3
R_d (Ω)	13.2
L_s (nH)	0.441
L_d (nH)	0.447
L_g (nH)	0.258
C_{gsp} (pF)	0.0397
C_{gdp} (pF)	0.001
C_{gs} (pF)	0.215
C_{gd} (pF)	0.0211
C_{ds} (pF)	0.101
g_m (mS)	27.3
τ(ps)	1.25
R_i (Ω)	15.1
R_{gd} (Ω)	43.6
R_{ds} (Ω)	218

Table 5.6 Parameter Values in FET example 3

5.4 Conclusion

In this chapter, the adopted method is applied to six different examples. The measured S-parameters in those examples are either from paper or datasheet. As shown in the results, our method is proven to be accurate and reliable to both the FET and HBT models. As well, this work is fast and provides unique solutions.

In addition, the choice of different topologies plays a critical role in the modeling process based on the comparison of different topologies' modeled S-parameters. It influences the accuracy as well as the efficiency of the experiment results. Though the difference between the modeled S-parameters from different topologies is very small in some examples, our work is proven to be capable of selecting the exact best one among all the topologies, due to the usage of fuzzy logic.

In next chapter, the summary of this work and the suggestions of the future work will be addressed thoroughly.

Chapter 6

CONCLUSIONS AND FUTURE WORK

6.1 Summary

A novel modeling method has been developed which selects a suitable RF and microwave small-signal transistor model from measured S-parameters. In the existing methods, only one equivalent circuit topology is included. In practice, however, users have different needs. The included model might not be the best choice for every application. The adopted method selects several typical topologies for different transistors and employs Fuzzy Logic to select the most suitable model for different cases. Still, Neural Networks are applied in the parameter extracting process, which offer significant advantages in speed, accuracy, and suitability to computer-aided design.

In Chapter 5, we showed that our method is able to consistently provide excellent model fitting and the results displayed excellent agreement between the model and the experimental data. This is demonstrated on HBT and on FET.

For the development of analog and digital integrated circuits, an accurate device model is a valuable tool. As the range of applications constantly widens, the need for accurate transistor models is a key factor for their successful employment in systems. The adopted method has the ability to catch up with the development steps by increasing or changing the transistors' equivalent circuit topology library and thus own a wide application area. To sum up, not only efficient and accurate, the adopted method is also proven to be steady and flexible.

6.2 Future Work

Equivalent circuit optimization is a major part of the semiconductor industry and software. Companies have teams of engineers dedicated to solving the equivalent problem. The results obtained in our study are not able to cover all the issues in device modeling. However, they represent a starting point for the research activities that could be included in the future work.

Our work shed light on the selection of most suitable topology for the topology library. As mentioned above, this can be accomplished by adding latest models into the existing library or through revising of the existing models based on demands.

The second area that this research sheds light on is the application of Neural Networks. The Neural Model used in this work is MLP, a basic model in Neural Network area. Other Neural Models, Knowledge Based Neural Networks (KBNN) as an example, could be employed to reduce the size of training data and still reach good accuracy.

This study has not considered the effects of noise. However, noise performance of devices is essential for efficient communication systems. This calls for the development of device models that incorporates the noise effects (noise models). Though separate noise models for transistors have been studied and even combined with large-signal models, few small signal models mentioned it in existing studies. Therefore, the combination of transistors' small-signal model and noise model is a good challenge for the future work.

Another very exciting direction for future work would be to include the nonlinear effects in our existing models. Such extension will make the proposed approach much complete but would certainly require using load pull measurements data.

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