

# **Contributions to the Design of RF Power Amplifiers**

by

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*"I do not think there is any thrill that can go through the human heart like that felt by the inventor as he sees some creation of the brain unfolding to success ..."*

*Nikola Tesla, 1856 - 1943*

## **ABSTRACT**

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In this thesis we introduce a two-way Doherty amplifier architecture with multiple feedbacks for digital predistortion based on impedance-inverting directional coupler (transcoupler). The tunable two-way Doherty amplifier with a tuned circulator-based impedance inverter is presented. Compact N-way Doherty architectures that subsume impedance inverter and offset line functionality into output matching networks are derived. Comprehensive N-way Doherty amplifier design and analysis techniques based on load-pull characterization of active devices and impedance modulation effects are developed. These techniques were then applied to the design of a two-way Doherty amplifier and a three-way Doherty amplifier which were manufactured and their performance measured and compared to the amplifier performance specifications and simulated results.

Index terms - Power amplifier (PA), Doherty amplifier, load-pull measurement, efficiency enhancement, peak-to-average, impedance matching, linearity, impedance modulation.

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# TABLE OF CONTENTS

Chapter 1 .....	1
Introduction.....	1
1.1    Role of RF Power Amplifiers in Wireless Networks.....	1
1.2    RF Power Amplifiers of Interest in this Thesis .....	1
1.3    Existing Efficiency Enhancement Techniques for Power Amplifiers .....	2
1.3.1    Single Active Device Power Amplifiers.....	2
1.3.2    Load Impedance Modulation .....	3
1.3.3    Drain Voltage Modulation .....	4
1.3.4    Constant Envelope Outphasing (Chireix Method).....	4
1.4    Limitations of Existing RF Power Amplifiers .....	5
1.4.1    Complex Modulation Signal Properties.....	5
1.4.2    Peak-to-Average Ratio (PAR) and Signal Statistics .....	6
1.5    The PA Design Scenario as Observed from the Literature.....	7
1.6    Overview of the Thesis .....	10
1.7    References for Chapter 1 .....	13
2    Conventional Doherty-Type Power Amplifier concepts and Design Methods .....	15
2.1    Introductory Remarks .....	15
2.2    The Need for, and Mechanism of, Load Impedance Modulation .....	15
2.3    Two-Way Doherty Amplifier Architectures .....	17
2.3.1    Basic Ideas .....	17
2.3.2    Symmetric Two-Way Doherty Amplifier .....	22
2.3.3    Asymmetric Two-Way Doherty Amplifier.....	23
2.4    N-Way Doherty Amplifier .....	25
2.5    Input Signal Conditioning.....	25
2.6    Active Device Requirements .....	28
2.6.1    Introduction.....	28
2.6.2    Main Device selection considerations .....	28
2.6.3    Peak Device selection Considerations .....	29
2.7    Existing Design Methods for Conventional Doherty Power Amplifiers as Perceived from the Available Literature.....	29

2.8	Conclusions.....	34
2.9	References for Chapter 2 .....	35
Chapter 3.....		37
3	Improvements to standard Two-Way Doherty Amplifiers .....	37
3.1	Introduction.....	37
3.2	Transcoupler .....	38
3.2.1	Introduction.....	38
3.2.2	Transcoupler Analysis and Operation.....	39
3.2.3	Use of the Transcouplers as Impedance Transformers and Inverters .....	47
3.2.4	Reasons why a cascade of a coupler and an impedance inverter will not behave as an impedance inverter .....	54
3.2.5	Application of transcouplers in Chireix Amplifier .....	57
3.3	Tunable Two-way Doherty Amplifier with a Circulator as an Impedance Inverting Element.....	59
3.3.1	Introduction.....	59
3.3.2	Tunable Two-Way Doherty Amplifier .....	59
3.3.3	Performance of the Tunable Circulator Impedance Inverter .....	63
3.4	Conclusions.....	68
3.5	References for Chapter 3 .....	69
Chapter 4.....		70
4	Compact Implementation of Existing Doherty Architectures .....	70
4.1	Introduction.....	70
4.2	Two-Way Compact Doherty Amplifier .....	72
4.3	Compact Three-Way Doherty Amplifier: Main Amplifier Replaced by another Two-Way Doherty Amplifier .....	84
4.4	Compact Three-Way Doherty Amplifier: Peak Amplifier Replaced by another Two-Way Doherty Amplifier .....	87
4.5	N-Way Compact Doherty Amplifier (Arbitrary Expansion).....	96
4.5.1	Preliminary Remarks .....	96
4.5.2	First Example of a Sub-Optimal Expansion .....	96
4.5.3	Second Example of a Sub-Optimal Expansion.....	101

4.5.4	Improved Course of Action .....	101
4.6	Compact N-Way Doherty Amplifier: Last Peak Amplifier of (N-1)-Way Doherty Replaced by a Two-Way Doherty Amplifier.....	103
4.7	Conclusion .....	109
4.8	References for Chapter 4 .....	110
Chapter 5	.....	112
5	Doherty Amplifier Design Synthesis Techniques Based on Transistor Load-Pull Measurements .....	112
5.1	Introduction.....	112
5.2	Load-Pull Data Needed.....	115
5.3	Two-Way Fixed Input Power Split Doherty Design.....	122
5.3.1	Two-Way Doherty Amplifier with Fixed Input Power split.....	122
5.3.2	Design of a Fixed Input Power Split Two-way Doherty Amplifier.....	123
5.3.3	Generic Matching Network.....	127
5.3.4	Scattering Matrix for Input Matching Networks and Node Matching Network	128
5.3.5	Main Device Impedance Modulation Ratio $N_M$ Derivation.....	132
5.3.6	S Matrix for Main Output Matching Network.....	134
5.3.7	Scattering Matrix for Peak Output Matching Network.....	138
5.3.8	Network Phase Delay.....	141
5.3.9	Design Technique for a Two-Way Doherty Amplifier.....	146
5.4	Two-Way Controlled Main Device Compression Doherty Design.....	149
5.5	Three-Way, Fixed-Input-Power-Split, Doherty Design.....	152
5.6	Conclusions.....	166
5.7	References for Chapter 5 .....	167
Chapter 6	.....	168
6	Doherty Amplifier Analysis Techniques Based on Transistor Load-pull Measurements .....	168
6.1	Introduction.....	168
6.2	Passive Network and Load-Pull Data Interactions .....	169
6.3	Two-Way Fixed Input Power Split Doherty Analysis.....	173

6.3.1	Description of the Analysis Procedure .....	173
6.3.2	Example Applications of the Analysis Procedure .....	184
6.4	Two-Way Controlled Main Device Compression Doherty Analysis .....	195
6.5	Three-Way Fixed Input Power Split Doherty Analysis .....	200
6.6	Conclusions.....	214
6.7	References for Chapter 6 .....	215
Chapter 7	.....	216
7	General conclusions .....	216
7.1	Summary of the Contributions of the Thesis .....	216
7.2	Future Work .....	217

Figure 1: Calculated envelope of a 10MHz wide 6.5dB PAR LTE in time domain (1000 samples) .....	6
Figure 2: Calculated energy content versus sample amplitude (proportional to how often samples of certain amplitude occur) of an 10MHz wide, 6.5dB PAR LTE signal.....	7
Figure 3: Two current sources feeding a common load.....	16
Figure 4: Inverting the dependence of impedance seen by the current source $I_1$ on the current from source $I_2$ .....	17
Figure 5: Conventional Two-Way Doherty Amplifier Architecture .....	19
Figure 6: Conventional two-way Doherty amplifier.....	21
Figure 7: Generic microstrip implementation of a conventional two-way Doherty amplifier .....	22
Figure 8 Conventional fixed-input-split two-way Doherty amplifier with digital predistortion feedback loop.....	26
Figure 9: Digital Doherty Power Amplifier Architecture.....	28
Figure 10 Conventional approach Doherty amplifier performance predictions .....	32
Figure 11 Proposed approach Doherty amplifier performance predictions.....	33
Figure 12: Comparison between a Quarter-wave Transformer Impedance Inverter and a Transcoupler (after ) Impedance Inverter (coupler design after [34], [35], [36], [37]) .....	39
Figure 13: Classical Doherty Combiner with Cascaded Coupler Functionality.....	39
Figure 14: Classical Doherty Combiner with Cascaded Coupler Functionality in microstrip layout implementation .....	40

Figure 15: Calculated performance of classical Doherty combiner with cascaded coupler.  
Note that " $DB(|S(1,1)|)$ " denotes  $|S_{11}|$  in dB, and so forth. .... 40

Figure 16: Calculated input impedance of classical Doherty combiner with cascaded  
coupler. Note that " $Re(|ZIN(1)|)$ " denotes the real part of the input impedance at port  
1, and so forth ..... 41

Figure 17: Wideband Doherty combiner with cascaded coupler ..... 42

Figure 18: Calculated S-parameter performance of wideband Doherty combiner with  
cascaded coupler. Note that " $DB(|S(1,1)|)$ " denotes  $|S_{11}|$  in dB, and so forth..... 43

Figure 19: Calculated input impedance performance of wideband Doherty combiner with  
cascaded coupler. . Note that " $Re(|ZIN(1)|)$ " denotes the real part of the input  
impedance at port 1, and so forth..... 44

Figure 20: Calculated S-parameters of a Doherty node transformer based on a wideband  
Transcoupler microstrip implementation layout ..... 45

Figure 21: Calculated input impedance at port 1 of a Doherty node transformer based on  
a wideband Transcoupler microstrip implementation layout..... 46

Figure 22: The classical implementation of the Doherty amplifier ..... 48

Figure 23: The Digital Doherty implementation of the Doherty amplifier. Note that the  
transcoupler elements shown are block diagram elements not actual layouts [39]. . 49

Figure 24: Improved Bandwidth Doherty Combiner with 50ohm/30dB Main  
Transcoupler and 35.35ohm/30dB Output Transcoupler..... 49

Figure 25: Combining output network of a Doherty amplifier containing two  
transcouplers ..... 50

Figure 26: Quarter-wave transformer impedance inverter..... 54

Figure 27: Quarter-wave transformer impedance inverter cascaded with a directional coupler.....	55
Figure 28: Impedance inverting/transforming directional coupler .....	56
Figure 29: Functional diagram of a Chireix Amplifier [40] .....	57
Figure 30: Functional diagram of a Chireix Amplifier with transcouplers .....	58
Figure 31: Block diagram of a Two-Way Doherty amplifier with circulator-based impedance inverter after [42].....	60
Figure 32: Functional diagram of the circulator-based impedance inverter. The multiple arms are meant to indicate multiple reflected and transmitted signals. ....	61
Figure 33: Circulator based impedance inverter with associated tuning circuit.....	62
Figure 34: Measured circulator frequency response.....	64
Figure 35: Calculated frequency response of a circulator with enhanced (6dB improvement) match and isolation.....	65
Figure 36: Calculated frequency response of the circulator-based inverter tuned to 2300MHz, compared to that of the quarter-wave transformer (QWT) inverter .....	65
Figure 37: Calculated frequency response of the circulator-based inverter tuned to 2500MHz, compared to that of the quarter-wave transformer (QWT) inverter .....	66
Figure 38: Calculated frequency response of the circulator-based inverter tuned to 2700MHz, compared to that of the quarter-wave transformer (QWT) inverter .....	66
Figure 39: Circulator-based inverter tuned over the entire band with its impedance inverting performance displayed over 20MHz wide channels .....	67

Figure 40: Calculated circulator-based inverter with 6dB enhanced Return Loss and Isolation tuned over the entire band with its impedance inverting performance displayed over 20MHz wide channels ..... 67

Figure 41: Compact two-way Doherty amplifier ..... 73

Figure 42: Generic microstrip implementation of compact two-way Doherty amplifier . 73

Figure 43: Main branch design with an implicit and explicit use of impedance inversion. The lower two diagrams are an actual layout for a design frequency of 748MHz. By implicit use of impedance inversion we mean the compact approach..... 74

Figure 44: Computed performance comparison between the implicit and explicit impedance inversion implementations..... 75

Figure 45 Measurement setup ..... 79

Figure 46: Simulated and measured gain and drain efficiency for a two-way compact Doherty amplifier. No bench tuning or other modifications were performed on the measured amplifier..... 80

Figure 47: Comparison of simulated and measured gain and efficiency of a two-way compact Doherty amplifier with the peak device input matching network of the fabricated amplifier tuned to improve gain linearity ..... 81

Figure 48: Uncorrected output spectrum of the two-way compact Doherty amplifier..... 82

Figure 49: Corrected output spectrum of the two-way compact Doherty amplifier by means of digital predistortion ..... 83

Figure 50: Block diagram of a conventional three-way Doherty amplifier ..... 84

Figure 51: Generic microstrip implementation of a possible three-way Doherty amplifier derived from a two-way Doherty by replacing its main branch by another two-way Doherty amplifier..... 85

Figure 52: Block diagram of a new compact three-way Doherty design derived from a two-way Doherty by replacing its main branch by another two-way Doherty amplifier ..... 86

Figure 53: Generic microstrip implementation of a new compact three-way Doherty amplifier derived from a two-way Doherty amplifier by replacing its main amplifier by another two-way Doherty amplifier ..... 86

Figure 54: Block diagram of a conventional three-way Doherty design, derived from a two-way Doherty by replacing its peak amplifier by another two-way Doherty ..... 87

Figure 55: Generic microstrip implementation of an existing three-way Doherty amplifier derived from a two-way Doherty by replacing its peak amplifier by another two-way Doherty ..... 88

Figure 56: Block diagram of a new compact three-way Doherty design derived from a two-way Doherty by replacing its peak amplifier by another two-way Doherty ..... 89

Figure 57: Generic microstrip implementation of a new compact three-way Doherty derived from a two-way Doherty by replacing its peak amplifier by another two-way Doherty ..... 89

Figure 58: Pulsed CW signal regime measurements of gain and efficiency performance of the compact three-way Doherty amplifier ..... 93

Figure 59: Modulated signal regime measurements of gain and efficiency performance of the compact three-way Doherty amplifier ..... 93

Figure 60: Spectral performance of the compact three-way Doherty amplifier .....	94
Figure 61: Spectral performance of the compact three-way Doherty amplifier over carrier frequency (constant input power to the amplifier).....	94
Figure 62: Variation in modulated signal gain of the compact three-way Doherty amplifier over frequency (constant input power to the amplifier chain) .....	95
Figure 63: Block diagram of the compact N-way Doherty amplifier obtained from an (N- 1)-way Doherty amplifier by replacing its main branch by another two-way Doherty .....	97
Figure 64: Block diagram for impedance modulation behaviour analysis .....	98
Figure 65: Block diagram of the compact N-way Doherty amplifier obtained from (N-1)- way Doherty amplifier by replacing its first peak branch by another two-way Doherty amplifier .....	102
Figure 66: Block diagram of the new compact N-way Doherty design derived from an (N-1)-way Doherty by replacing its last peak amplifier by another two-way Doherty .....	103
Figure 67: Block diagram for impedance modulation behaviour analysis .....	104
Figure 68: Class-AB constant compression load-pull contours for (a) 1dB compression and (b) 5.3dB compression .....	120
Figure 69: Class C constant compression load-pull contours for (a) 0.6dB compression and (b) 2.3dB compression .....	121
Figure 70: Block diagram of a fixed-input-conditioning power-split, two-way Doherty amplifier .....	122
Figure 71: A generic two-port network with associated notation (after [62]) .....	127

Figure 72: A generic two-port matching network with associated notation .....	142
Figure 73: Two-way Doherty design synthesis procedure flow diagram .....	146
Figure 74: Gain profiles in a two-way Doherty amplifier .....	150
Figure 75: Block diagram of a dynamic-input-conditioning power-split two-way Doherty amplifier .....	151
Figure 76: Block diagram of a fixed-input-conditioning power-split, three-way Doherty amplifier .....	152
Figure 77: Three-way Doherty design synthesis procedure flow diagram .....	163
Figure 78: Block diagram of input-to-output load-pull data interaction in two-way Doherty amplifier architecture .....	171
Figure 79: Block diagram of input-to-output load-pull data interaction in three-way Doherty amplifier architecture .....	172
Figure 80: Two-way Doherty analysis flow chart .....	174
Figure 81: Schematic of the two-way Doherty output combining network with associated notation .....	177
Figure 82: Performance of the four different two-way Doherty amplifiers, designed for different gate bias voltages (of the peak device) and adjusted input power split ...	185
Figure 83: Performance of the four different two-way Doherty amplifiers, designed for different gate bias voltages (of the peak device) but fixed 3dB input power split .	185
Figure 84: Two-way Doherty with 3dB input power split versus two-way Doherty with adjusted input power split performance comparison. The amplifiers compared are those designed for the peak device gate biases of 1.3V .....	186

Figure 85: Main and peak device gain performance in two-way Doherty amplifiers (with different peak device gate bias and adjusted input power split) as a function of the output power of the complete amplifier..... 188

Figure 86: Main and peak device gain performance in two-way Doherty amplifiers with peak device gate bias sweep and 3dB input power split..... 189

Figure 87: Main and peak device power performance in two-way Doherty amplifiers (with different peak device gate bias and adjusted input power split) as a function of the output power of the complete amplifier..... 190

Figure 88: Main and peak device power performance in two-way Doherty amplifiers (with different peak device gate bias and 3dB input power split) as a function of the output power of the complete amplifier..... 191

Figure 89: Main and peak device compression performance in two-way Doherty amplifiers (with different peak device gate bias and adjusted input power split) as a function of the output power of the complete amplifier. .... 192

Figure 90: Main and peak device compression performance in two-way Doherty amplifiers (with different peak device gate bias and 3dB input power split) as a function of the output power of the complete amplifier. .... 193

Figure 91: Comparison of simulated and measured gain and efficiency of a two-way compact Doherty amplifier with the peak device input matching network of the fabricated amplifier tuned to improve gain linearity ..... 194

Figure 92: Schematic of the two-way Doherty output combining network with associated notation ..... 195

Figure 93: Three-way Doherty analysis flow chart ..... 201

Figure 94: Schematic of the three-way Doherty output combining network with  
associated notation ..... 204

# Chapter 1

## Introduction

### ***1.1 Role of RF Power Amplifiers in Wireless Networks***

The radio communication portion of the wireless network is referred to as the air interface. The geographical area of the wireless network coverage is based on a system of cells which cover geographical locales of varying size. They can be as small as a single floor of a building (as in Pico-cells) or a large area with a radius of several kilometres (as in Macro-cells). The use of cells is done for the purpose of frequency spectrum reuse, maximization of number of users, and feasibility of hardware implementation. To provide RF coverage for the users within a cell the base-station needs to provide an appropriate amount of RF power to its antenna system. Power amplifiers (PA) increase the power available from the radio transmit module, which is on the order of milli-watts, to tens of watts at the output of the amplifier. These power levels are necessary to overcome losses in the duplexer and antenna system, and to provide enough power for communication with user mobiles within the cell. The PA modules need to be low cost, efficient, and spurious emissions free. These requirements are to some extent in conflict with each other, making the design of power amplifiers for wireless networks presents quite a challenge.

### ***1.2 RF Power Amplifiers of Interest in this Thesis***

This research work is focused on design techniques for PAs used in wireless base-stations. Power amplifier designs based on RF integrated circuit technology intended for implementation in handheld “terminals” that provide output power in the mW range, are not of interest in the thesis. We will focus on macro-cell PA designs featuring average output power of between 20W to 100W<sup>1</sup>, supporting modulated signal peak-to-average

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<sup>1</sup> These power levels are necessary to provide adequate coverage for macro-cells with radii of up to 30km

ratios of at least 6.5dB, and providing gains of 10 to 20dB along with high efficiency at power back-off, while maintaining a bandwidth of at least 10%.

### **1.3 Existing Efficiency Enhancement Techniques for Power Amplifiers**

#### **1.3.1 Single Active Device Power Amplifiers**

In a class-A amplifier, the active device is biased in such a way that it is in its active state for all signal power levels (device conduction is  $360^\circ$  of the signal cycle). Class-A amplifiers provide high gain, linear amplification and maximum theoretical efficiency of 50% at peak envelope power (PEP), however the efficiency decreases quickly when signal power is backed-off or signal has a high peak-to-average ratio PAR (10% at 10dB PAR) [1].

Class-AB amplifiers have the active device biased so that the conduction angle of the device is between  $180^\circ$  and  $360^\circ$ . Class-AB amplifier provides high gain and maximum PEP efficiency between 50% and 78% depending on the biasing conditions. This configuration is a trade-off between class-A and class-B.

Class-B amplifiers have the biasing such that the active device conduction angle is exactly  $180^\circ$  (the device acts like a half-wave rectifier). Class-B amplifiers provide linear gain and have maximum PEP efficiency of 78%. The efficiency of Class-B amplifiers for signals with high PAR is considerably better than that of class-A amplifiers (e.g. 28% versus 5%) [1].

Class-C amplifiers are biased in a manner that the active device conduction angle is less than  $180^\circ$ . The maximum PEP efficiency is higher than 78% however this comes at the expense of lower gain and gain linearity [1].

To retain the gain and gain linearity but also improve the amplifier efficiency, several efficiency enhancement methods have been devised. The three most common ones are briefly described next. The existing versions of these methods are discussed in references [2] through [9] given at the end of the present chapter.

### 1.3.2 Load Impedance Modulation

Given a constant input power an RF amplifier exhibits a change in gain, efficiency, and power delivered depending on the load impedance presented at the output of the amplifier. For a fixed load impedance the efficiency of operation will increase with an increase in output power reaching maximum efficiency at peak envelope power. For lower power signals the efficiency will be low, and for signals close to amplifier saturation level the efficiency will be high, provided the output DC supply voltage remains constant. The increase in load impedance keeps transistor close to saturation as the output power delivered by the transistor decreases thus maintaining the efficiency of operation even at power levels significantly lower than that of the device's maximum power capability. If the load impedance can be adjusted dynamically in accordance with input signal level changes, a high efficiency of operation can be maintained over the dynamic range of the signal. Doherty amplifier configurations [1], [4 p.290], [10], [11] which are the subject of this thesis, use impedance modulation to achieve efficiency enhancement. Doherty power amplifiers<sup>2</sup> can offer high efficiency of operation over a wide range of output power levels. Since the output power is obtained by means of combining signals from multiple active devices, the power requirement for each device is decreased, the heat produced is spread over multiple devices and is thus more easily dissipated. The high efficiency of operation lowers the DC power consumption and provides a smaller thermal footprint (which results in a smaller physical size for the heatsink). The number of devices used, and their nominal power (the amount of power they can provide), gain, and efficiency, will affect the gain and efficiency performance of the resulting Doherty amplifier.

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<sup>2</sup> Doherty amplifiers offer high efficiency of operation by relying on load impedance modulation capability that is achieved by means of appropriate combining of RF signals from two or more amplifiers that are activated and contribute the output RF power in accordance with the amplitude of the input RF signal.

### 1.3.3 Drain Voltage Modulation

If the modulation of the load impedance is not possible then changing the voltage of the output DC power supply, envelope tracking (ET) [1], [4], represents an approach of maintaining the high efficiency of operation over the dynamic range of the RF signal. For a fixed load and fixed DC power supply voltage the power dissipated by the transistor will be high for low power signals because the transistor needs to dissipate power proportional to the difference between the fixed DC power supply voltage and the comparatively low signal voltage. However if the voltage of the power supply is lowered for low power signals, and increased for the high power signals, the power dissipation in the transistor can be minimized and the efficiency of operation maintained over the dynamic range of the signal. In order to maintain the overall system efficiency the envelope modulator must be highly efficient.

### 1.3.4 Constant Envelope Outphasing (Chireix Method)

The constant envelope outphasing method [1], [4], [12] uses two amplifiers that amplify phase modulated constant envelope signals which, when combined, produce desired signal amplitude at the output. Because the individual amplifiers operate under constant envelope conditions they can be designed to operate at maximum efficiency at all times. This method of obtaining a high efficiency of operation is sometimes called linear amplification with non-linear components (LINC) because the amplifiers used in the two branches can be highly non-linear (deep class C or switched-mode power amplifiers). These amplifiers require tightly controlled phasing of the input signals because the difference in the phase between the constituent amplifier branches will be converted to information carrying amplitude modulation<sup>3</sup> after the signal combining.

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<sup>3</sup> Combining essentially converts phase modulation (constant envelope) of individual branches into amplitude modulation (varying envelope) of the combined output signal

## **1.4 Limitations of Existing RF Power Amplifiers**

The amplifiers that amplify signals with high peak-to-average power ratios (PAR) will suffer from poor efficiency at average power levels. Signals produced by the complex modulation schemes used in modern wireless have such high peak-to-average power ratios [19]. Envelope tracking amplifiers provide high efficiency mode of operation for the RF section by modulating the voltage of the power supply, however the envelope modulator must be capable of handling high power and be highly efficient at the same time, so the challenge of obtaining high efficiency is only shifted from the RF section to the envelope modulator. The outphasing modulation technique requires two separate Tx chains to carry individually phase-modulated input signals to two branch amplifiers, the output signals from each branch must be combined in a reactive combiner to attain high efficiency of operation. The main issue with the outphasing modulation technique is the complexity of implementation. The Doherty amplifier on the other hand provides efficiency enhancement with minimal increase in complexity. It has proven itself to be quite robust with respect to trade-offs in the design specifications, as well as with respect to variations in the manufacturing process of the active devices and power amplifiers themselves.

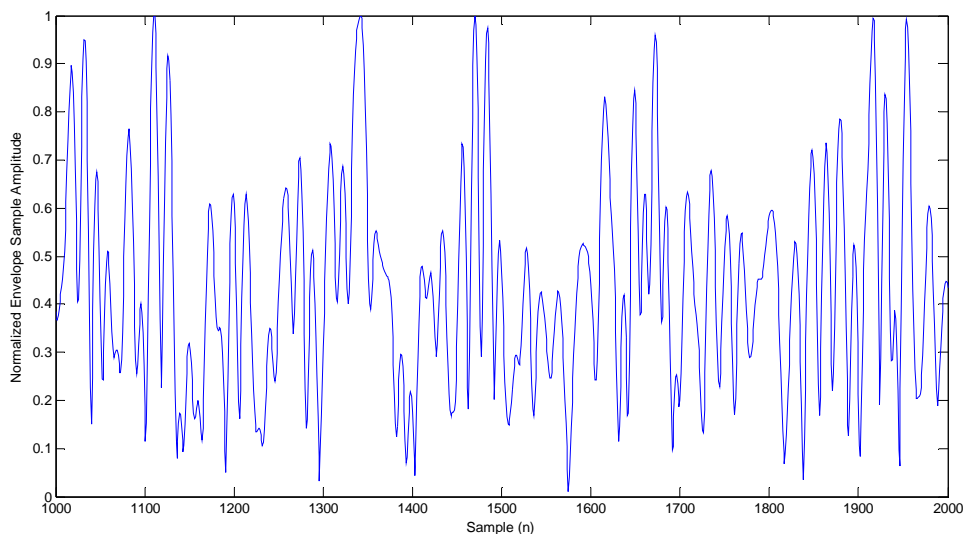
In the next two sections we will see what aspects of the modulated signals contribute to high peak-to-average ratios of the signals in modern telecommunications.

### **1.4.1 Complex Modulation Signal Properties**

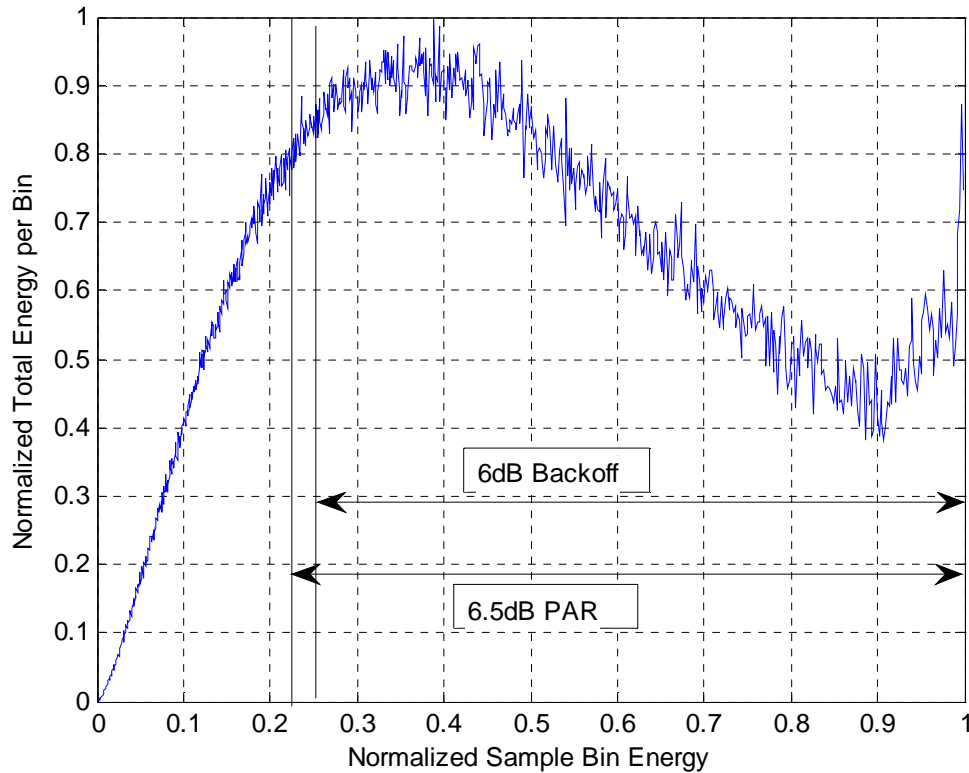
Due to high spectral efficiency requirements of modern wireless networks complex modulation schemes need to be used. These are based on some form of quadrature amplitude modulation (QAM). The modulation is digital in the sense that amplitude levels are discrete and two orthogonal carriers at the same frequency are used, each modulated by an independent set of data bits called the "I" and "Q" (in-phase carrier and quadrature carrier). This type of modulation yields a square constellation (2x2 for QPSK, 4x4 for 16QAM, 8x8 for 64QAM, and 16x16 for 256QAM) [13 p.357]. Since these are amplitude modulated signals they will inherently exhibit non-zero peak-to-average ratios.

## 1.4.2 Peak-to-Average Ratio (PAR) and Signal Statistics

Orthogonal Frequency Division Multiplex (OFDM) signals [13 p.556] are used in Long Term Evolution (LTE) and Worldwide Interoperability for Microwave Access (WiMAX) wireless communication standards. Wideband Code Division Multiple Access (wCDMA) [13 p.769] signals are used in Universal Mobile Telecommunications System (UMTS) standard. Each one of the above multi-user signals will combine multiple signals from Section 1.4.1 into a complex wideband signal which will have certain peak to average ratio [19] and signal statistics associated with it (but definitely higher than PARs of the individual user signals), and the performance of the amplifier will be heavily dependent on these parameters. The amplifier needs to be designed for specific PAR value. Due to the signal statistics most of the signal's energy is contained in the average amplitude samples (due to relatively frequent occurrence and average amplitude) and in large amplitude samples (even though large compared to average amplitude samples, they have less frequent occurrence). The amplifier needs to have a sufficiently high saturation power to handle signal peaks without clipping (clipping introduces distortions and contributes to spurious emissions), while maintaining high efficiency at average power levels for overall efficiency performance. Figure 1 depicts the envelope (1000 samples long) of a 10MHz wide, 6.5dB PAR LTE signal. The energy content for the previously mentioned signal is shown in Figure 2.



**Figure 1: Calculated envelope of a 10MHz wide 6.5dB PAR LTE in time domain (1000 samples)**



**Figure 2: Calculated energy content versus sample amplitude (proportional to how often samples of certain amplitude occur) of an 10MHz wide, 6.5dB PAR LTE signal**

### **1.5 The PA Design Scenario as Observed from the Literature**

The Doherty amplifier consists of passive networks (e.g. consisting of microstrip lines and lumped capacitors) and active devices. The passive network components can be modelled using S-parameters. The highly non-linear active devices, which are operated under large-signal conditions, are more difficult to model. CAD models for the transistors have been placed in three categories [5, p.9]. Physical models where the detailed device physics of specific fabrication process is modelled. Equivalent circuit models, where the device physics is modelled by an interconnection of circuit elements. And behavioural models, where a set of mathematical expressions (not necessarily related to the device physics) is fitted to the measured characteristics of the device. As a power amplifier designer, one does not have access to the physics of the active devices supplied by vendors, and what little about the physics of the device is forthcoming from vendors is

usually incomplete and most likely proprietary. The best of the above-mentioned options (but not necessarily the most practical) is the behavioural model. In order to be useful, behavioural models need to cover a range of biases, a range of output powers, a range of input powers, and must in some way describe the sensitivity of the device to the intended signal statistics. Devices are regularly coming on the market with major advances in performance, and not just small improvements. It is then not possible to simply “tweak” an existing behavioural model of an existing device. It takes a while for a behavioural model of a specific device to become available. Such models take much time to develop, and so are usually made available by a vendor once the device has been on the market for some time, by which time the PA designer’s organisation will already have lost the desired competitive edge!

In an ideal world, one of the above-mentioned models would be available in complete form when it is needed. For the moment suppose this is so. If we have a complete active device model, then a non-linear circuit analysis software package such as AWR [14] or ADS [15] can be used to completely analyze a PA. In principle the designer could carefully define an objective function that, when minimized, provides a PA that satisfies all the desired specifications. The non-linear circuit analysis tool, with the behavioural model of the device included, could then be linked to numerical optimisation algorithms and the above objective function minimized. This is unfortunately not yet feasible in practice since there would be a large number of optimisation variables. However, if a design procedure could be devised so that the amplifier can be decomposed into its constituent functional components, such as individual matching networks, that would make the optimization of these smaller units a much more feasible procedure. In the absence of reliable transistor models, the conventional design approach calls for use of load-pull measurements to characterize the active devices in order to make the design decisions. Unless the designers have a load-pull setup at their disposal to perform the necessary measurements, they will usually have to rely on load-pull data provided by the device vendor. Vendors will usually provide class-AB 1dB (3dB) constant compression load-pull contours or, in the case of more complete data set availability, entire power sweep load-pull measurement set. From this data set the designer must extract enough information to complete the design. Unfortunately class-C load-pull characterization is

usually unavailable and certain assumptions need to be made (about for example input power split, class-C device gain, input bias, etc) to complete design. Some of the assumptions that may later cause the design consistency issues are:

- The default use of 3dB input splitter implying that the gain of the class-C biased peak branch device is equal to that of the class-AB main branch device.
- Estimating the performance of the class-C biased peak branch device based on class-AB load-pull data.
- Neglecting the effects the input bias of the class-C device will have on its performance.
- Automatically expecting 6dB back-off from a symmetrical Doherty amplifier design, etc.

During the conventional design, most time and effort is spent designing the matching networks based on the impedance selections some of which are made based on the above-mentioned assumptions. In the absence of the active device models it is not possible to entirely predict the performance of the completed Doherty amplifier, at best an estimate of the high power performance and the performance at power back-off is available. Some examples of the conventional design can be found in [16], [17], [18].

A significant advantage of the design approach developed in this thesis is that the complete characterization of the gain, efficiency, and phase response versus output power is available for both pulsed CW and modulated signal excitations. In addition, the performance characterization of the individual devices is available during the design process. We will show that this allows one to predict to a large extent the performance of the complete amplifier and identify possible sources of performance issues for the amplifier without sophisticated modelling tools. Other also computable quantities include the efficiency performance under modulated signal regime of operation (using a sample-by-sample approach), the compression levels of the individual transistors in the PA, and the efficiencies of the individual transistors. All this is available without actually building the PA; whereas the conventional approach will only provide performance estimates at only two particular points.

Perhaps more importantly from the design viewpoint is that the new procedure makes it possible to actually design the PA so that the gain is more linear without

sacrificing much of the efficiency, something that is not easy to achieve with the conventional method.

## **1.6 Overview of the Thesis**

Chapter 2 of the thesis contains a review of the conventional Doherty amplifier configurations and design methods.

Chapter 3 introduces three novel ideas.

- The construction and application of transcouplers in Doherty type power amplifiers is first described. These transcouplers perform impedance inversion and predistortion feedback signal coupling simultaneously and thus can be inserted into the combiners of Doherty amplifiers without disrupting their functionality. This cannot be achieved with a standard cascaded combination of an impedance inverter and a directional coupler presently used at the output of conventional Doherty combiners.
- It is then shown that the use of transcouplers enables the sampling of the main<sup>4</sup> amplifier's output signal prior to its being combined with the peak amplifier's output signal, and allows for main amplifier specific predistortion to be applied.
- Next the use of circulators as impedance inverters (circulators will act as impedance inverters if their ports are purposefully mismatched) in Doherty type amplifiers is presented. The conventional quarter-wave transformer-based impedance inverters are band-limited and when in place in the physical circuit they cannot easily be tuned. Circulators on the other hand are wide band compared to quarter-wave impedance inverters and a tuning circuit terminating the third port of the circulator can be used to tune the comparably narrow-band

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<sup>4</sup> We mentioned in Section 1.3.2 that a Doherty amplifier consists of a combination of two or more amplifiers. In the two-way Doherty amplifier these are referred to as the main amplifier and the peak amplifier. More background on conventional forms of these configurations will be provided in Chapter 2. The new compact forms of these Doherty architectures that are introduced and designed in this thesis are described in Chapters 4 through 6.

impedance inverting response of the circulator within its much wider operation bandwidth.

Chapter 4 is dedicated to the new compact implementation of main and peak device matching networks in N-way Doherty amplifiers, resulting in more compact Doherty amplifiers. In the conventional Doherty amplifier design the output section of main branch consists of three distinct parts: a matching network, an offset line, and a quarter-wave impedance inverter. The output section of the peak branch consists of a cascade of a matching network and an offset line. Each of these constituent sections of the matching networks of the two branches has certain functionality. In this chapter we will present techniques to combine all the functionalities of the above described cascades into a single network for each branch that performs all the necessary impedance transformations needed to convert combining-node side impedances into appropriate device side impedances, with benefits of increased bandwidth, lower insertion loss, and a smaller circuit footprint. These compact designs facilitate expansion of two-way Doherty designs into N-way Doherty designs in a systematic fashion. There are many ways to extend the two-way Doherty amplifier configuration into an N-way Doherty architecture, until now insufficient attention appears to have been paid to determining which is the best one as far as the resulting performance is concerned. We will show through analysis in Chapter 4 which configuration is the superior to all others. In this chapter we will demonstrate, both in simulation and experimentally, performance of compact two-way and three-way Doherty amplifiers designed using the new design methods that will be the subject of Chapter 5 and Chapter 6.

Chapter 5 develops new Doherty amplifier design techniques based on transistor characterization data obtained through load-pull measurement techniques and load impedance modulation at the combining node(s) of the Doherty amplifier. The synthesis of all relevant circuit parameters for main and peak output and input matching networks, power splitters, node matching network as well as complete determination of transistor biasing conditions will be covered in detail, from theoretical calculations to actual circuit implementation. We will cover fixed-input-power split Doherty designs, and controlled-main-device-compression designs for two-way and three-way Doherty amplifiers. A

greatly improved design procedure for N-way Doherty amplifiers has been developed. It is novel in the sense that it uses accurate characterization of the constituent active devices by means of vector load-pull measurements, it provides a consistent set of design requirements, and it generates representative S-parameter models for all functional blocks of the amplifier architecture subject to performance specification and Doherty architecture related constraints. This allows designer to focus on the architecture performance optimization (amplifier can be designed literally by a few clicks of a mouse). Once the amplifier has been optimized through a number of quick design iterations, only then the designer proceeds to implement the actual amplifier circuit.

In Chapter 6 the circuit analysis techniques for two-way and three-way Doherty amplifiers will be described allowing for full characterization of the amplifier performance based on microwave circuit theory and the device load-pull data. The circuit analysis yields AM-AM and AM-PM<sup>5</sup>, and efficiency response, as well as amplifier frequency response thus providing the designer with adequate amount of information to assess the amplifier's performance with a high degree of certainty without necessity of building physical prototypes. An accompanying new N-way Doherty analysis technique that allows for complete performance analysis of N-way Doherty amplifiers ('complete' being the key word) has been presented. It uses active device load-pull data and S-parameters representation of the passive part of the amplifier network to simulate the performance of the amplifier without the need to implement circuitry. This allows the designer to explore interaction of various parameters that influence the performance of the amplifier and to find the best combination that suits the performance specifications the best.

Finally, Chapter 7 summarises the contributions of this thesis to the design of Doherty power amplifiers. These are drawn from the material in Chapters 3, 4, 5, and 6. Some ideas and suggestions for future work on the subject are also provided.

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<sup>5</sup> AM-AM is the amplifier gain response versus output power. AM-PM is the amplifier phase response versus output power.

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# Chapter 2

## 2 Conventional Doherty-Type Power Amplifier concepts and Design Methods

### 2.1 *Introductory Remarks*

The goal of this chapter is to clearly convey the state-of-the-art in Doherty-type PA configurations and design methods, properly summarize the limitations of such conventional design methods, and then list<sup>6</sup> in what way the research described in this thesis contributes to the overcoming of some of these limitations.

In Section 2.2 we will describe the load impedance modulation effect and its application as a PA efficiency enhancement mechanism.

Section 2.3 covers basic ideas behind two-way Doherty architectures.

In Section 2.4 N-way Doherty architecture is described along with its benefits and challenges.

Section 2.5 will address input signal conditioning in two-way Doherty amplifiers.

In Section 2.6 we will talk about the active device requirements when it comes to designing Doherty amplifiers.

Section 2.7 summarizes conventional PA design methods, including their limitations.

### 2.2 *The Need for, and Mechanism of, Load Impedance Modulation*

The efficiency of operation of the active device in a power amplifier is a function of the output signal power level. The closer the signal output power level is to the device

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<sup>6</sup> The details of which will be described in depth in subsequent chapters.

saturation levels the more efficient is the active device operation. The active device saturation level is determined by, among other parameters, the voltage of the DC power supply connected to the output terminal of the active device (collector or drain, depending on the device type) and by the load impedance presented to the device. Now if the DC power supply voltage and other parameters influencing the device saturation power level are fixed, the saturation power level (and associated device efficiency of operation) can be controlled by the change of the load impedance. An ability to modulate the load impedance in such a way that the device is kept close to its saturation state for all output signal power levels would yield an amplifier that could operate with high efficiency almost independently of the output signal power levels.

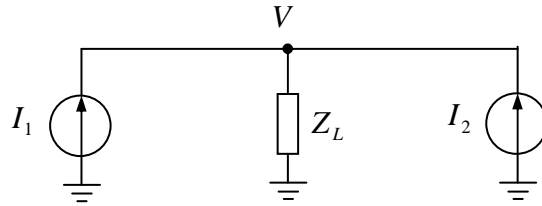
The circuit in Figure 3 depicts two current sources feeding a single load at a common node. The current through the load is equal to the sum of the currents from each of the current sources. When both current sources are turned on the load current is given by  $I_L = I_1 + I_2$  and the voltage across the load by  $V = Z_L (I_1 + I_2)$ . The impedances seen by current sources  $I_1$  and  $I_2$  are thus

$$Z_{L1} = \frac{V}{I_1} = Z_L \left( 1 + \frac{I_2}{I_1} \right)$$

and

$$Z_{L2} = \frac{V}{I_2} = Z_L \left( 1 + \frac{I_1}{I_2} \right)$$

respectively. This means that the load impedance seen by source  $I_1$  can be modulated by changing the current from the source  $I_2$ . Namely if we increase  $I_2$  the load impedance  $Z_{L1}$  seen by source  $I_1$  will increase and if we decrease  $I_2$  the load impedance  $Z_{L1}$  seen by source  $I_1$  will decrease.



**Figure 3: Two current sources feeding a common load**

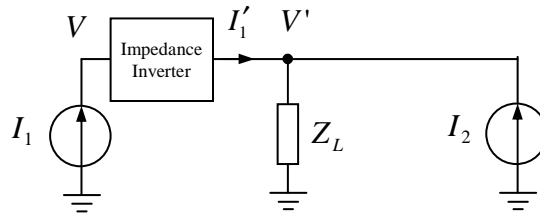
If we insert an impedance inverter with a characteristic impedance  $Z_0$  into the  $I_1$  branch (Figure 4) we will get the inverse relation between  $I_2$  and impedance seen by the source  $I_1$ . That is, if we increase  $I_2$  the impedance seen by source  $I_1$  will decrease and if we decrease  $I_2$  the impedance seen by source  $I_1$  will increase. On the node side of the impedance inverter, the load impedance seen by the current source  $I_1$  branch is given by

$$Z'_{L1} = \frac{V'}{I'_1} = \frac{I'_1 + I_2}{I'_1} Z_L$$

There is an increase in this impedance with an increase in  $I_2$ . However, on the source side of the impedance inverter<sup>7</sup> we have the relationship

$$Z_{L1} = \frac{Z_0^2}{Z'_{L1}} = \frac{I'_1}{I'_1 + I_2} \frac{Z_0^2}{Z_L}$$

which reveals that the load impedance seen by source  $I_1$  will decrease with an increase in current  $I_2$ .



**Figure 4: Inverting the dependence of impedance seen by the current source  $I_1$  on the current from source  $I_2$**

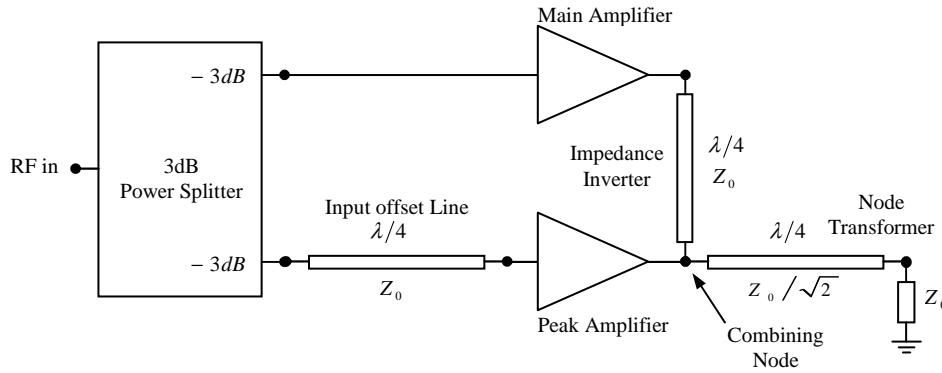
## 2.3 Two-Way Doherty Amplifier Architectures

### 2.3.1 Basic Ideas

The inverse impedance behaviour described in Section 2.2 can be exploited to make high power amplifiers operate more efficiently. Amplifiers are most efficient when they operate close to the maximum instantaneous output power they were designed for. The efficiency of the amplifier decreases significantly as the output power level is

<sup>7</sup> Assuming  $Z_0$  quarter-wave transformer impedance inverter is used.

backed-off from the maximum level. This makes amplifier efficiency a function of output power level. For a given output power level (significantly lower than the maximum), everything else being equal, an amplifier will be more efficient if the load impedance seen by the amplifier is high in effect lowering the amplifier power saturation level. However, keeping the load impedance high when output power levels increase will make the amplifier saturate at a lower output power level than that for which it was originally designed. When the amplifier operates in a lower power regime the load impedance is increased to improve the efficiency and when amplifier operates in a higher power regime the load impedance is decreased in order to avoid saturation. In other words the load impedance needs to be made higher when the output signal power is low and needs to be made lower when the output signal power is high. This load impedance modulation as a function of the signal power level is achieved by the Doherty amplifier architecture shown in Figure 5 [20], [21], [22], in a similar manner to that of the circuit shown in Figure 4. The roles of current sources  $I_1$  and  $I_2$  from Figure 4 are taken by the main amplifier and the peak amplifier, respectively. In the low power regime, the peak amplifier is inactive and the main amplifier sees high load impedance which results in better efficiency at low power levels. In the high power regime, the peak amplifier is active and the main amplifier sees the lower load impedance as the result of load pulling effect which prevents saturation at high power levels. Figure 5 shows constituent parts of a fixed-input-power split Doherty amplifier with a  $Z_0$  quarter-wave transformer connecting the outputs of the main and peak amplifiers acting as an impedance inverter, and a  $Z_0/\sqrt{2}$  quarter-wave transformer acting as a node transformer to provide appropriate node impedance ( $Z_0/2$  in this case).



**Figure 5: Conventional Two-Way Doherty Amplifier Architecture**

For an amplifier to be broadband each of the constituent components shown in Figure 5 needs to be broadband. Since an impedance inverter is a constituent part of the Doherty architecture, its bandwidth will limit the overall bandwidth of the amplifier. In the current state of the art the impedance inversion in Doherty amplifier architectures is implemented using a quarter-wave transformer<sup>8</sup>, as in fact indicated in Figure 5. Impedance inversion using a quarter-wave transformer is accomplished by destructive combining of the reflected waves at the input side and constructive combining of transmitted waves at the output side of the impedance inverter. This works perfectly at the center frequency, but for signals that significantly deviate from the center frequency the combining becomes less perfect and the impedance inversion properties of the transformer degrade (thus limiting the bandwidth of operation). Changing either the characteristic impedance or the length of the transformer cannot be done dynamically.

Figure 6 shows a more detailed block diagram of a conventional two-way Doherty amplifier. The main amplifier branch actually consists of a cascade of a main input matching network (IMN), a main amplifier active device (e.g. transistor), a main output matching network (OMN), a main offset line, and a quarter-wave transformer that acts as an impedance inverter. The peak amplifier branch consists of a cascade of a peak input matching network, a peak amplifier active device, a peak output matching network, and a peak offset line. Output signals from the main and peak amplifier branches are combined at the node where main and peak branches meet, and the resulting combined signal is

<sup>8</sup> The impedance inversion bandwidth of a quarter-wave transformer is usually assumed to be 10%

delivered to the load through a network consisting of a cascade of an output quarter-wave transformer  $Z_{01}$  and an interconnecting transmission line of characteristic impedance numerically equal to the load impedance  $Z_L$ .

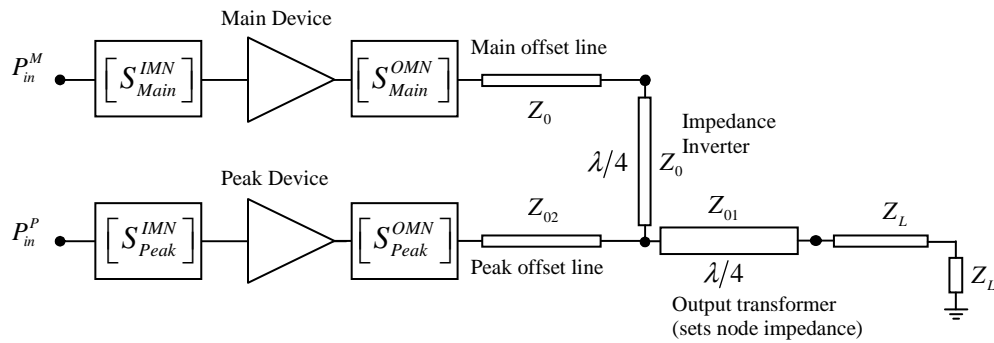
In the case of the typical implementation of the Doherty amplifier in Figure 6, for a particular signal frequency (or one or more particular ranges of signal frequencies), the main and peak input matching networks perform impedance transformation to convert from the relatively high system impedance levels (usually  $50\Omega$ ) presented to the input of the amplifier down to the relatively low impedance levels (e.g.  $2\Omega$ ) suitable for appropriate power transfer to (that is, appropriate excitation of) the main and peak amplifier devices. Similarly, the main and peak output matching networks perform an impedance transformation to convert from the relatively low impedance levels of the main and peak amplifier devices back to the relatively high system impedance levels to achieve appropriate power extraction (that is, achieve appropriate power delivery) from the devices. Note that, in general, the impedance levels associated with the main amplifier branch may be different from the corresponding impedance levels associated with the peak amplifier branch.

Main and peak offset lines provide appropriate impedance transformations at low power levels, increasing the efficiency of operation for the main branch and providing high loading impedance for the peak branch when the peak device is in its off-state, to minimize the loading on the main branch. The quarter-wave transformer in the main branch performs impedance inversion. For example, for a particular design, the quarter-wave transformer performs impedance inversion at low power levels from  $Z_0/2$  to  $2Z_0$  and at high power level from  $Z_0$  to  $Z_0$ . The output quarter-wave transformer performs another impedance transformation to ensure that the load impedance  $Z_L$  is transformed into the appropriate node impedance (which in this case would be  $Z_0/2$ ). The main and peak input impedance matching networks are implemented to enable proper RF power delivery to main and peak amplifier devices respectively.

Doherty amplifier is a specific type of amplifier with a capability to provide enhanced efficiency performance for signals that have high peak-to-average ratios. The Doherty amplifier consists of two or more parallel branches each of which contains an active

device with a progressively lower bias (class-AB, class-B, class-C of various depths). The active device in the branch that is biased in class-AB is referred to as Main or Carrier device. The devices in remaining branches are called Peak devices and are class-C biased to various extents. A class-AB bias for the main amplifier device is selected to improve gain linearity, mostly to avoid undesired gain expansion on the main device. A class-C bias for the peak device is selected to increase efficiency (no quiescent current) and to "delay" peak device conduction onset so it does not turn on before the main device reaches saturation at average power level.

Figure 7 shows a generic microstrip implementation<sup>9</sup> of a conventional two-way Doherty amplifier.



**Figure 6: Conventional two-way Doherty amplifier**

<sup>9</sup> Throughout this and succeeding chapters we will refer to, and show diagrams of, "generic microstrip implementations" of different amplifier configurations. By this we mean that this shows only roughly what a possible implementation in microstrip might look like, but that details are not shown. In later sections of the thesis when we discuss the performance of hardware implementations or certain Doherty amplifiers we will not only discuss such generic implementations but the actual specific ones.

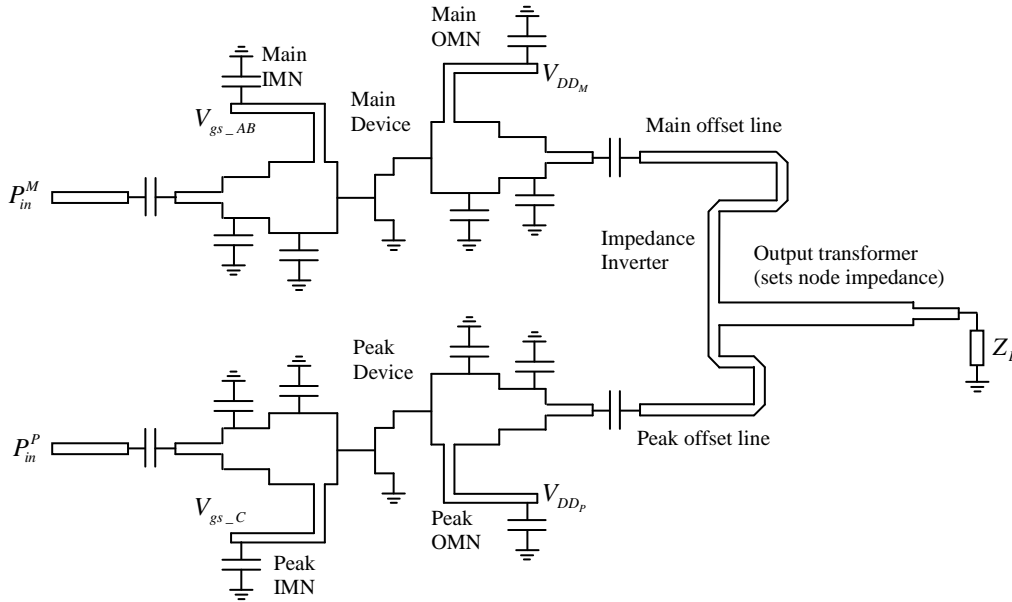


Figure 7: Generic microstrip implementation of a conventional two-way Doherty amplifier

### 2.3.2 Symmetric Two-Way Doherty Amplifier

Two-way Doherty amplifiers consist of two amplifier branches, the main (carrier) amplifier and one peak amplifier. The symmetric amplifier has identical devices used in its main and peak amplifiers. The symmetry is reflected in the fact that at maximum power both main and peak devices deliver the same amount of output power (thus the maximum output of the Doherty amplifier is 3dB higher than the maximum power that can be provided by either one of its individual devices). The load impedance presented to the main device for low output signal power levels is twice that of the load impedance presented to the main device at maximum output power level. Since the load impedance for low power level output signals is twice that at the maximum power, the saturation power level for the main device in the low power regime is approximately half of its maximum power. In the efficiency curve<sup>10</sup> for the two-way Doherty amplifier there are two distinct efficiency peaks: the first one is reached when the main device reaches saturation while being loaded with high load impedance of the low power regime (at half of the maximum power handling of the device), and the second one is reached when both

<sup>10</sup> The example of an efficiency curve (i.e. Doherty amplifier efficiency plotted versus output power) is shown in Figure 11 of section 2.7

main and peak device reach saturation at nominal load impedance (high power regime). In the case of ideally symmetric two-way Doherty, the spacing between two efficiency peaks is 6dB. In practice however this back-off will depend on several factors. When implemented with physical devices, in the case when both main and peak device are set to provide the same amount of maximum output power, the high efficiency power back-off of the Doherty amplifier is 3dB higher than the power back-off the main transistor has between its high power point and high efficiency point in the load-pull contours. The actual devices usually do not have 3dB spacing between maximum power point and maximum efficiency point (i.e. 2:1 load modulation does not produce 3dB power back-off) which needs to be remedied by implementing load modulation ratios higher than 2:1.

As stated previously, a well designed symmetric Doherty amplifier should provide a high efficiency at power back-off of close to 6dB, however the signals used in wireless communications usually have Peak-to-Average ratios that are mostly higher than 6dB [36] (even with crest reduction measures applied) and the symmetric Doherty amplifier will have high efficiency performance only at nominal power of the modulated signal (i.e. highest average power of the modulated signal for which the amplifier is designed) with no ability to provide high efficiency performance at lower signal average power. To remedy this problem, asymmetric Doherty amplifiers need to be employed.

### **2.3.3 Asymmetric Two-Way Doherty Amplifier**

An asymmetric amplifier employs devices different in size, with smaller device used in its main and a larger device in its peak amplifier. The high efficiency power back-off is equal to the ratio of the combined maximum output power from both devices and the output power level at which main device saturates when operating in high impedance mode. For example, if the peak device is twice the size of the main device, when both devices are at maximum, the output power will be three times that of the maximum main device power, and if the Doherty combining network load impedance modulation capabilities are such that main device goes into saturation at one third of its maximum power (while the peak device is in the off-state) then the high efficiency power back-off will be equal to a factor of 9 or 9.54dB. If we assume that the maximum efficiency is

equal to that of the symmetrical amplifier we can see that the amplifier will retain high efficiency of operation even if the signal with 3.54dB lower power (but with the same Peak-to-Average Ratio) is applied to it (this will cause the decrease in efficiency in a symmetric amplifier).

Even though we can increase the high efficiency power back-off by means of asymmetric design there are some drawbacks associated with its use. All other things being equal, devices with higher power handling capability are less efficient than their smaller counterparts. The consequence of this is the sag in the efficiency curve<sup>11</sup> between two efficiency peaks (main device high impedance saturation and maximum output power point). To avoid the sag in the efficiency curve, and to provide high power while using smaller devices, N-way Doherty is used.

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<sup>11</sup> The example of an efficiency curve (i.e. Doherty amplifier efficiency plotted versus output power) is shown in Figure 11 of section 2.7

## **2.4 N-Way Doherty Amplifier**

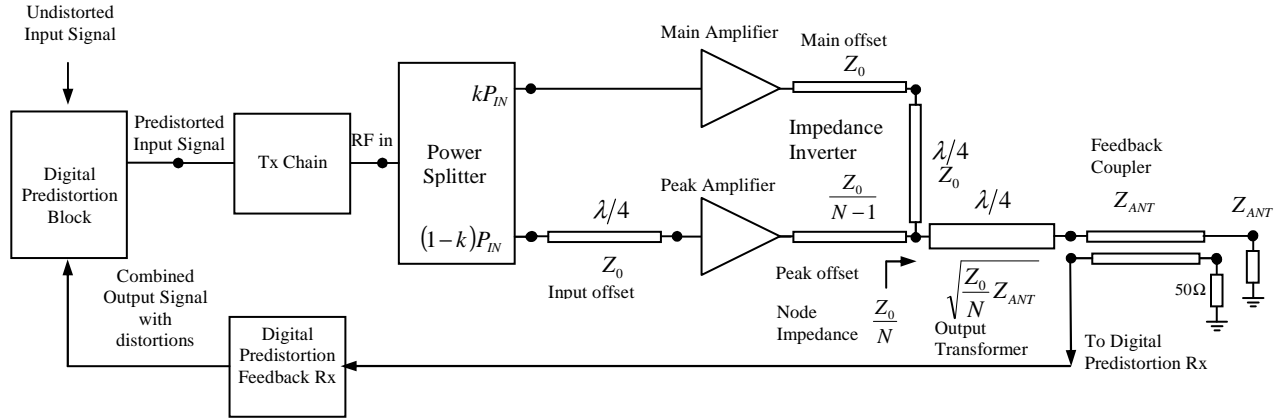
N-way Doherty amplifiers consist of one main amplifier and multiple peak amplifiers connected through an impedance modulating and output signal combining network. The task of this network is to combine signals from all branches in phase so that maximum output power is obtained from the output powers available from the individual branches, and to present a decreasing load impedance to all active devices whenever the output power increases (in order to maintain devices as close to saturation as possible). N-way Doherty amplifiers are discussed in this thesis, but we will discuss any detailed background on the conventional forms of these configurations on a “just in time” basis when it is needed in Chapter 4.

## **2.5 Input Signal Conditioning**

Input conditioning refers to the control over amplitude and phase of the input signals to each branch of the Doherty amplifier. The fixed-input conditioning implies that the amplitude ratio of input signals and their phase relationship are adjusted for one power level at a single frequency (e.g. by means of a hardware RF splitter and an input phase offset line). There is no ability to make any adjustments to the input signal if the power levels or signal frequency range changes.

Up to this point we have concentrated on the performance of the Doherty combiner. In a basic Doherty design the input signal is simply split between the branches and the phase of the two signals adjusted (by appropriately sizing the lengths of the input transmission lines to each of the branches) in order to achieve in-phase combining of the output signals of the branches. This type of signal phase equalization only works at a single power level because the active device will have different phase delay under different biasing conditions, and to minimize the power losses, the phases are usually equalized at the highest power levels. In a “digital” Doherty power amplifier design [23], [24] (Figure 9) each branch has a dedicated transmit (Tx) chain so that the input signals can be independently adjusted to accommodate idiosyncrasies of the devices under various biasing conditions. The signal phase in each branch can be adjusted at all power

levels for optimal combining at the output. Also, the signals can be pre-distorted independently to correct better for distortions in each branch<sup>12</sup>.



**Figure 8 Conventional fixed-input-split two-way Doherty amplifier with digital predistortion feedback loop**

The impedance modulation ratio<sup>13</sup>  $N$  is the ratio of the main amplifier branch loading impedances at high power operation (when both main and peak amplifiers deliver maximum power to the load) to that of high efficiency operation (when the main amplifier operates at power back-off with high efficiency and peak amplifier branch is inactive).  $N$  can be calculated as the ratio of Doherty peak envelope power to main

amplifier peak envelope power or in mathematical terms  $N = \frac{P_P^{DOH}}{P_P^M} = \frac{P_P^M + P_P^P}{P_P^M}$ . The

power back-off of a given Doherty amplifier can then be calculated using the expression  $20\log N$  which for a symmetric two-way Doherty amplifier would translate to 6dB

( $20\log 2 = 6$ ). For an asymmetric Doherty amplifier with the peak amplifier delivering twice the power of the main amplifier ( $N = 3$ ) the power back-off is 9.54dB

( $20\log 3 = 9.54$ )<sup>14</sup>.

<sup>12</sup> It will be shown in Chapter 3 that the transcoupler concepts developed there substantially improves the situation.

<sup>13</sup> In later chapters we will be referring to various impedance modulation ratios such as: combining node impedance modulation ratio  $N_{comb}$ , main device impedance combining ratio  $N_M$ , etc

<sup>14</sup> Note that these expressions are for the entire Doherty amplifier hence  $20\log N$

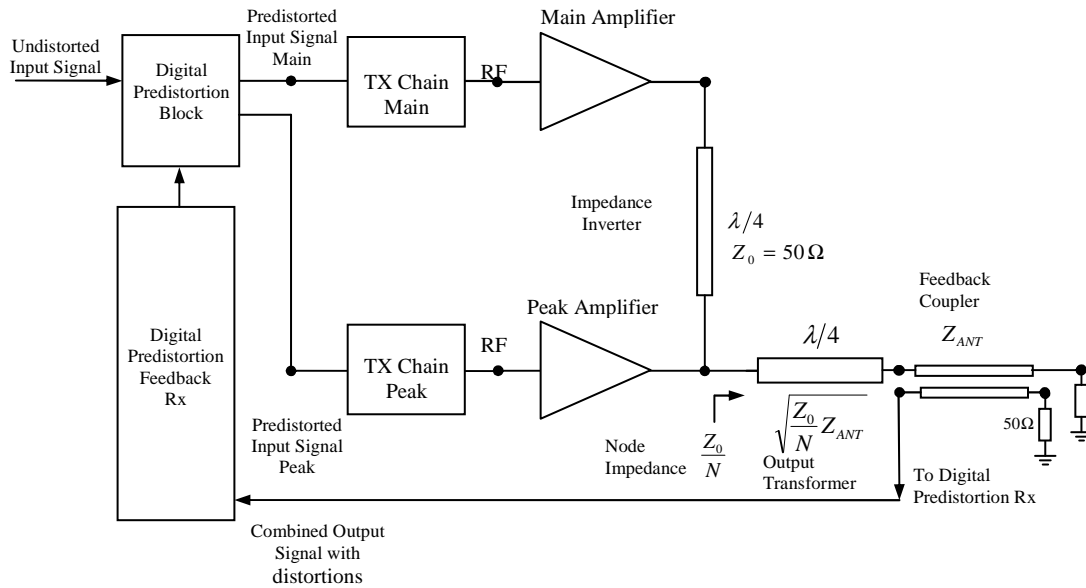
The main output matching network transforms impedance  $Z_0$  to a load impedance to which the main device can deliver maximum power. By attaching a  $Z_0$  offset line to the output of the main matching network and adjusting its length, the suitable transformation of a load impedance (e.g.  $2Z_0$  for symmetric two-way Doherty amplifier) into the load impedance with which main device operates with high efficiency at power back-off is achieved.

The peak output matching network transforms impedance  $Z_0$  to a load impedance to which the peak device can deliver maximum power. By attaching a  $Z_0$  offset line to the output of the peak matching network and adjusting its length the transformation of an off-state peak device impedance into a high impedance is achieved.

Input signal splitting needs to ensure that prescribed output power levels for each branch are achieved taking into account the gain of each branch.

The phase equalization between branches is performed to ensure that signals from the two branches combine in-phase at the combining node (to increase efficiency and to provide proper load impedance modulation that is essential for optimal operation of Doherty amplifiers).

The digital predistortion (DPD) represents the means of linearizing the nonlinear behaviour of amplifiers. The linearization is achieved by distorting the input signal in the manner opposite to that of the amplifier (where amplifier compresses the signal the predistorter expands it, and vice versa). The predistortion relies on the knowledge of the amplifier behaviour (calibration or feedback) to correct the distortion introduced by the amplifier. The current state of the art samples the already combined signal from the output of the Doherty combiner and sends it back to the predistortion module where the distorted signal is compared to its undistorted version, the distortions are assessed and correction applied to the incoming signal. The digital Doherty allows for individual predistortion of main and peak devices and transcoupler circuit (discussed in the next chapter) allows for sampling of individual signals. The benefits are better predistortion and better control over AM-PM behaviour. The costs are additional hardware and processing.



**Figure 9: Digital Doherty Power Amplifier Architecture**

## 2.6 Active Device Requirements

### 2.6.1 Introduction

Devices must exhibit properties that make them useful in the design of Doherty amplifiers. Each device will have certain set of properties that make it suitable or non-suitable for Doherty architecture design. The device properties are mainly assessed from the device load-pull contours.

### 2.6.2 Main Device selection considerations

The main device efficiency determines the maximum efficiency that can be achieved in the Doherty amplifier at power back-off (i.e. when the main device goes into saturation in the high load impedance regime and the peak device is inactive). It is desirable that the gain of the main device increases from the point of the maximum deliverable power toward the point of the maximum efficiency (this will help offset gain drop due to input signal split). The power back-off for the given load impedance

modulation ratio  $N$  for the main device should be  $10\log N$  (i.e. 3dB for  $N = 2$ , and 4.77dB for  $N = 3$ )<sup>15</sup>.

### 2.6.3 Peak Device selection Considerations

Peak device off state impedance should be such that it can be easily converted to high impedance by means of offset lines. The power ramp up of the peak device needs to be such that the main device load impedance is properly modulated (this may need to be adjusted through the input signal conditioning). The device gain in class-C should be as high as possible. AM-PM curve should be of similar shape to that of the main device (if a different peak device is used for example in an asymmetric Doherty)

## 2.7 Existing Design Methods for Conventional Doherty Power Amplifiers as Perceived from the Available Literature

This section is in a way a continuation of what has already been said in Section 1.5. It is important to remark here by that by design procedure we do not merely mean an analysis method. Much has been written about analysis, but much less has been published on complete design procedures. By complete we mean one that will allow us to take the performance requirements and come up with an amplifier that, when constructed, will work as intended without much further intervention on the part of the designer.

There are some methods (albeit not complete ones, as will be noted below) that have been described in books [25 pp.466-489], journals [26], [27], and conferences [28]. One approach uses the various I-V curves of the active device instead of load-pull data. If one has a complete set of such data that is fully representative of the device's dynamic behaviour at microwave frequencies as can be obtained from load-pull data then this approach would be fine. But this is usually not the case. Device vendors do not provide such data, and so designers would need to acquire it themselves. Examples of this approach use (e.g. [25], [26]) are all applied to low power (typically 1W) devices.

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<sup>15</sup> Note that these expressions are for the main device only, hence  $10\log N$  expression is used

Measured efficiencies are significantly lower than predicted, but this is not commented on in the associated literature. This is a serious limitation.

Far better are those methods based on load-pull data for the active device rather than I-V curves. The first step in such procedures is to obtain the design data for the active device when it is operated in class-AB, using load-pull techniques. This data is presented as a set of constant compression contours (e.g. 1dB, or 3dB). If a load-pull measurement set-up is available a designer would obtain a sample of the active device and measure the necessary load-pull data. Alternatively load-pull data can be obtained from the vendor, usually as a text file in the form of a class-AB power sweep, or in the form of the constant compression load-pull contours. Also used are the class-C off-state impedances, which is a single point of data at each of the frequencies of interest; existing design procedures do not appear to use load-pull data for class-C operation of the device. There are several reasons why this might be so. It could be because vendors do not provide class-C load-pull data, which might mean that such vendors do not think it is necessary and so do not measure it, or they have problems measuring it (of a technical nature, or otherwise), or simply because no one is requesting it<sup>16</sup>. The class-AB load-pull data is used to extract the following impedance values:

- $Z_{MP}$  - The high power load impedance of the active device used in the design of the main amplifier.
- $Z_{ME}$  - The high efficiency load impedance of the active device used in the design of the main amplifier.

The single value related to class-C operation is

- $Z_{PP}$  - The high power load impedance of the active device used in the design of the peak amplifier.

Off-state output impedance measurement

- $Z_{OFF}$  - The off-state output impedance of the active device used in the design of the peak amplifier.

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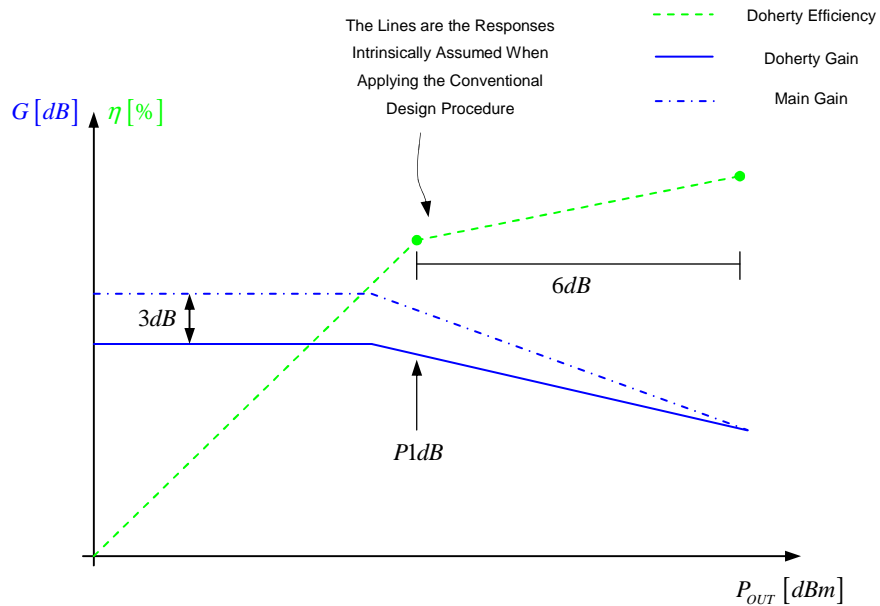
<sup>16</sup> We will show in Chapters 5 and 6 that class-C load-pull data can be used to arrive at complete design procedures.

The next step in the existing load-pull based design procedure is the assumption that  $Z_{MP} = Z_{PP}$ . This will only be true if the maximum power levels and gain of the main and peak amplifiers are the same, which is in fact not the case in practice due to different bias of the main and peak devices (class-AB for the former and class-C for the latter). It is necessary to make this assumption if, as previously mentioned, load-pull data for the active device is not available for class-C operation, in spite of the fact that it is the bias with which the peak amplifier device of a Doherty amplifier operates. Once the above impedances are known it is possible to design the passive matching networks. At this stage the conventional design procedure is complete.

When a PA designed via this procedure is constructed and tested it is usually found to not satisfy the performance specifications (one example of this is in [26]) to which it was supposed to have been designed. The reason is that the assumptions involved in the design are not self-consistent, as a result the active devices end up being used in states that do not satisfy the assumptions made during the design process (and in which the designer never intended them to operate). Much adjustment on the bench is thus required. The problem is that at that stage one has limited insight as to what is actually wrong with the design and limited means to remedy the issue. Eventually one may end up with a PA that “works” but is not optimal in any sense.

The conventional design procedure ties down just two points on the efficiency and gain curves versus output power curve in Figure 10. The hope is that these points are actually achieved. However, this will only be so if the assumptions on which the design procedure was based are approximately fulfilled. Otherwise even these two points may miss the prediction targets. The first data point for the Doherty amplifier efficiency in Figure 10 is at 6dB output power back-off  $\eta_{DOH} = \eta_{main} \{Z_{ME}\}$ . The second efficiency data point is for the maximum output power  $\eta_{DOH} = \eta_{main} \{Z_{MP}\} = \eta_{peak} \{Z_{PP}\}$  (the device performance is assumed to be the same for both main and peak device). The first data point for the Doherty amplifier gain in Figure 10 is at 6dB output power back-off  $G_{DOH} = G_{main} \{Z_{ME}\} - 3dB$  (for the input split of 3dB). The second gain data point is for the maximum output power  $G_{DOH} = G_{main} \{Z_{MP}\} = G_{peak} \{Z_{PP}\}$  (the device performance is

assumed to be the same for both main and peak device). However, main and peak devices will not have the same performance thus the prediction will be inaccurate.



**Figure 10 Conventional approach Doherty amplifier performance predictions**

It is assumed that the signals entering the combining node are in-phase, and (for the symmetric design) that they are equal in magnitude but the designer cannot do much to make that true. The procedure does not tell us what value of input bias to use for the peak device.

Using the procedure, the designer does not know what the optimal source impedance value  $Z_s$  for the peak device is, thus it is not possible to design the optimal input matching network for the peak amplifier. Because is not known what the gain profile of the peak device it is not known what the appropriate input power split is, and so the designer has to make further assumptions. To compensate for the lack of the characterization of the peak device under class-C biasing conditions designer's only choice is to implicitly assume that it is the same as that of the device used in the main amplifier even though in the latter operates in class-AB mode and under completely different compression conditions.

The conventional design procedure can be described in almost Churchillian terms as being too little design, based on too many assumptions, using too little data. It appears

to have been used since about 2004, when the Doherty architecture had a resurgence<sup>17</sup>. Prior to that classical class-AB power amplifiers had been used for wireless base-stations. A complete and practical design procedure is described in Chapter 5 of this thesis, and an accompanying analysis procedure is described in Chapter 6 that allows one to reliably predict the actual performance indicators of the designed amplifier that one can be assured will be closely achieved when the amplifier design is actually constructed. We can contrast the prediction from the conventional design approach depicted in Figure 10 to that of the proposed approach in this thesis depicted in Figure 11 and conclude that much more reliable performance predictions can be obtained using the proposed approach.

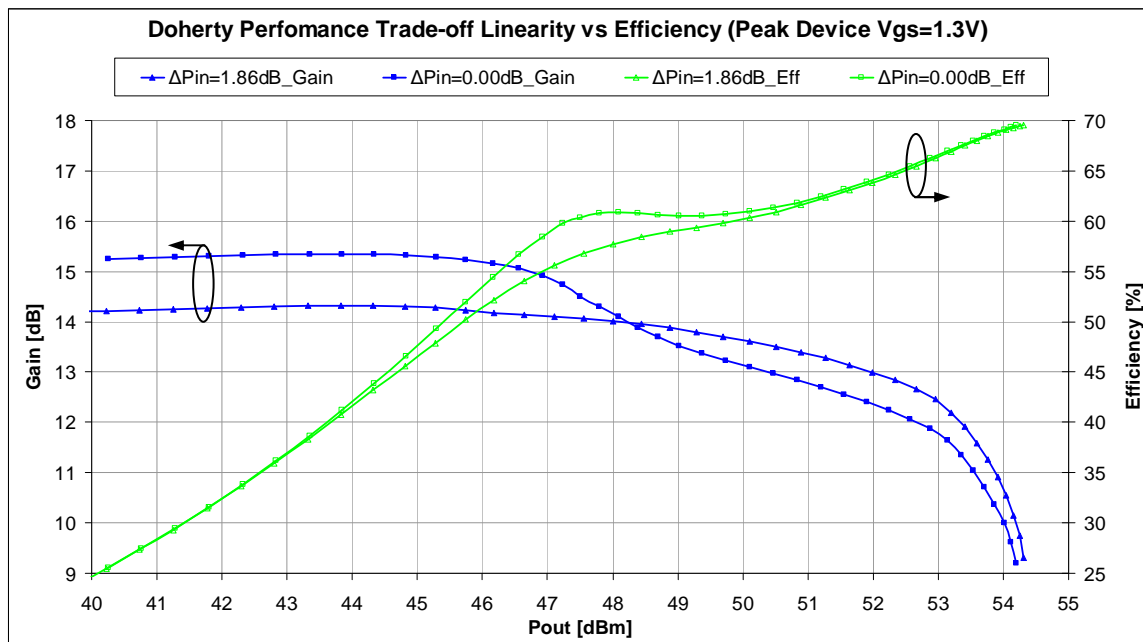


Figure 11 Proposed approach Doherty amplifier performance predictions

<sup>17</sup> The basic idea having been invented by William H. Doherty (1907 – 2000) at the Bell Telephone Laboratories in 1936 for use with vacuum tube devices.

## **2.8 Conclusions**

This chapter has introduced the concept of impedance modulation, and showed how it is used in conventional Doherty amplifier architectures. The essence of existing design procedures was described and their limitations pointed out. Ways in which the contributions of the present thesis overcome these limitations have been described earlier in Section 1.6.

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## Chapter 3

### 3 Improvements to standard Two-Way Doherty Amplifiers

#### 3.1 Introduction

The conventional two-way Doherty amplifier contains an impedance inverter that is implemented using a quarter-wave transformer. In this chapter we will introduce two separate improvements to the impedance inverting element by adding extra functionality to its impedance inversion capability, or making it tunable over frequency.

The component we refer to as a transcoupler is a combination of a directional coupler and a quarter-wave impedance inverter is introduced in Section 3.2. It provides impedance inversion for impedance modulation functionality of the two-way Doherty amplifier and it simultaneously provides the feedback for the digital base-band predistortion algorithms.

Quarter-wave impedance inverters are band limited<sup>18</sup> due to their physical properties, namely that impedance inversion depends on multiple reflection cancellations which can only be achieved for certain physical lengths and characteristic impedances of the transformer. In Section 3.3 a circulator with its third port terminated in a tuning circuit that can be used as a tunable impedance inverter is introduced.

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<sup>18</sup> Usually 10% bandwidth is assumed

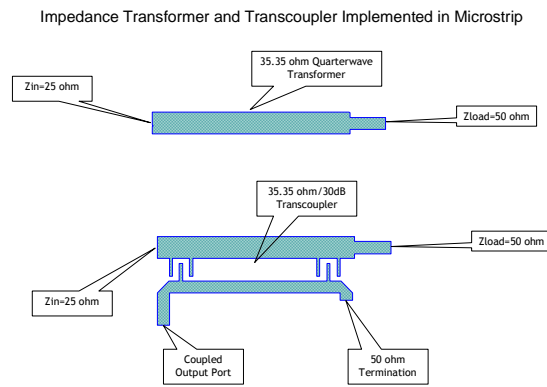
## **3.2 Transcoupler**

### **3.2.1 Introduction**

A transcoupler is a combination of an impedance transformer and a directional coupler. The combination of these two functionalities is achieved by designing an appropriately mismatched quarter-wave long directional coupler that simultaneously provides impedance inversion (due to quarter-wave length and impedance mismatch) and appropriate amount of coupling necessary to provide feedback signal for digital predistortion purposes. In the conventional approach these two functionalities are implemented by cascading a quarter-wave transformer and a directional coupler which takes additional space and increases the insertion loss (due to longer path of the cascaded components). Specifically, cascading of an impedance inverter and a directional coupler in Doherty amplifiers limits the sampling location of the signal to the output of the Doherty combiner where the signal is already combined and individual distortions from the main and peak amplifiers sections cannot be distinguished. To correct the distortions originating from the main and peak amplifiers separately, the signals from each section must be sampled prior to combining. Since the main amplifier branch contains an impedance inverter preceded by an offset line, which are precisely sized to satisfy specific characteristics of the device load-pull contours, inserting a directional coupler into the structure to sample the main signal is next to impossible. However, using a transcoupler in this situation enables us to achieve impedance inversion and, in the same footprint, provide necessary signal coupling without disturbing the performance of the inverter that has to adhere to prescribed geometry dictated by the load-pull contours. This way we can sample the main signal and the combined signal simultaneously, and from this gathered data calculate the signal transfer characteristics of the peak amplifier. Once the main and peak amplifier signal transfer characteristics are known, separate predistortion can be applied to each section, thus yielding improved performance.

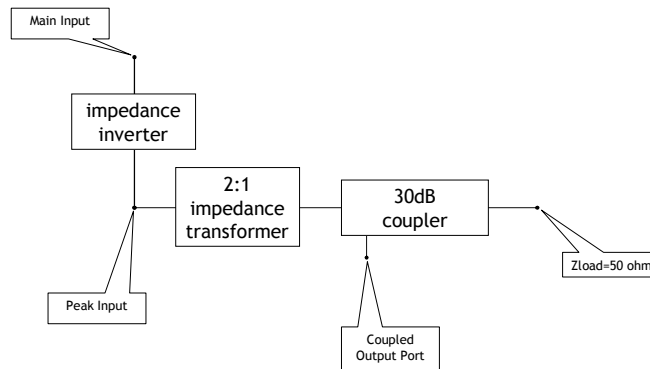
### 3.2.2 Transcoupler Analysis and Operation

A comparison between the microstrip layout of an ordinary quarter-wave transformer as an impedance inverter and a transcoupler is shown in the Figure 12. Both circuits invert impedance from 50ohm to 25ohm (with respect to their geometric mean of  $Z_0 = 35.35\Omega$  according to  $Z_{IN} = \frac{Z_0^2}{Z_L}$ ) but transcoupler performs additional signal coupling that is necessary for predistortion feedback purposes. We next show how it can be used in the Doherty amplifier configuration.



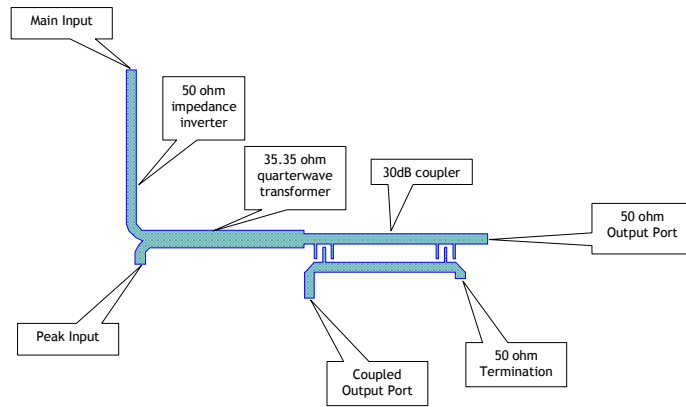
**Figure 12: Comparison between a Quarter-wave Transformer Impedance Inverter and a Transcoupler (after ) Impedance Inverter (coupler design after [35], [36], [37], [38])**

Before discussing the details of the transcoupler design we will first examine what can be achieved using a conventional Doherty combiner cascaded with a directional coupler. The block diagram in Figure 13 depicts the constituent parts of a Doherty combiner with a cascaded 30dB coupler.

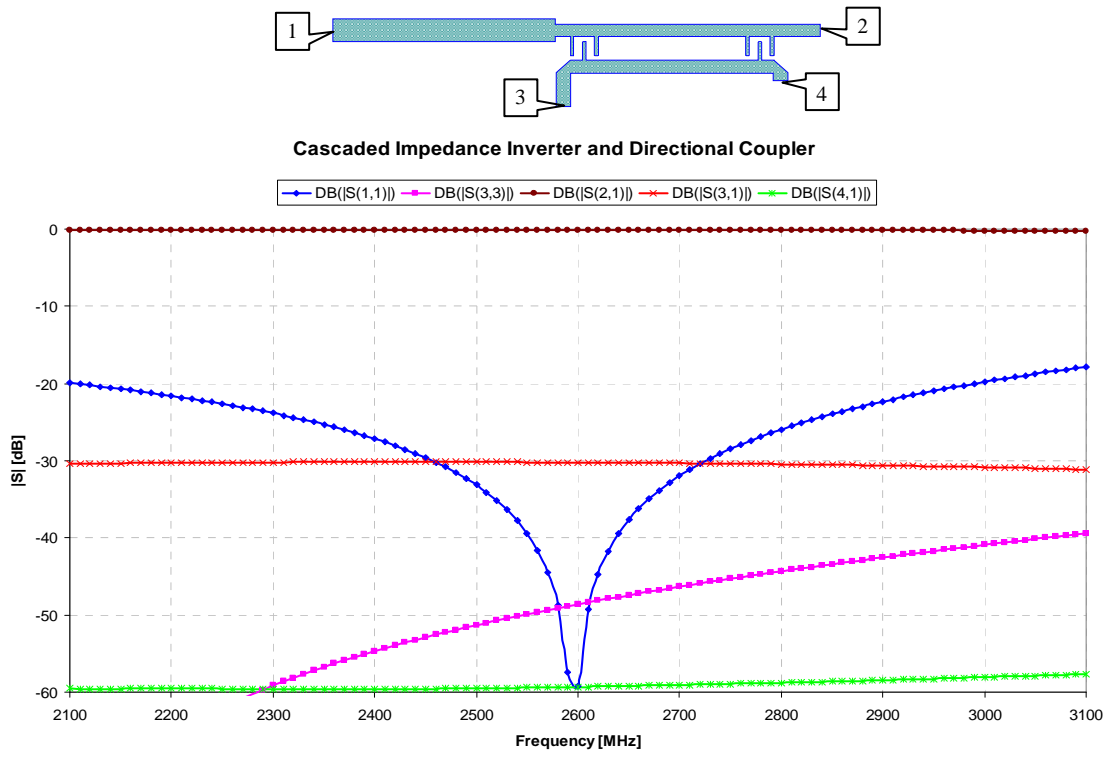


**Figure 13: Classical Doherty Combiner with Cascaded Coupler Functionality**

The microstrip layout of the Doherty combiner with a cascaded output directional coupler is shown in Figure 14.



**Figure 14: Classical Doherty Combiner with Cascaded Coupler Functionality in microstrip layout implementation**



**Figure 15: Calculated performance of classical Doherty combiner with cascaded coupler. Note that " $DB(|S(1,1)|)$ " denotes  $|S_{11}|$  in dB, and so forth.**

The S-parameters of the classical Doherty combiner with a cascaded coupler (with port numbering indicated) are shown Figure 15. The coupling factor is  $30dB$ , the isolation<sup>19</sup> is better than  $25dB$ , the return loss at port one is better than  $20dB$ , and the return loss on the coupled port 3 is better than  $40dB$ . The input impedance (at port 1) over frequency for the combiner with the cascaded directional coupler is given in Figure 16. The real part of the input impedance is very close to  $25\Omega$  over the  $1GHz$  band centered at  $2.6GHz$ , but the imaginary part varies from  $-5\Omega$  to  $5\Omega$  and this variation of the imaginary part may cause some issues in the operation of Doherty amplifiers.

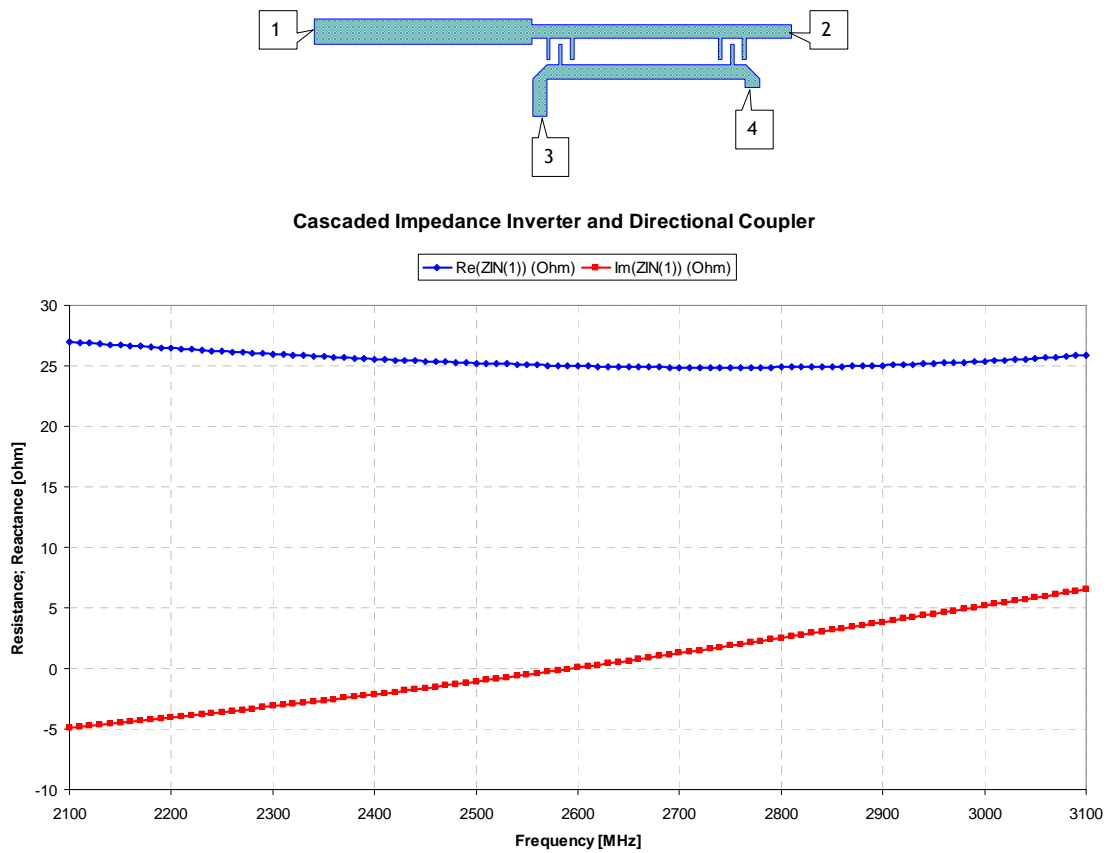
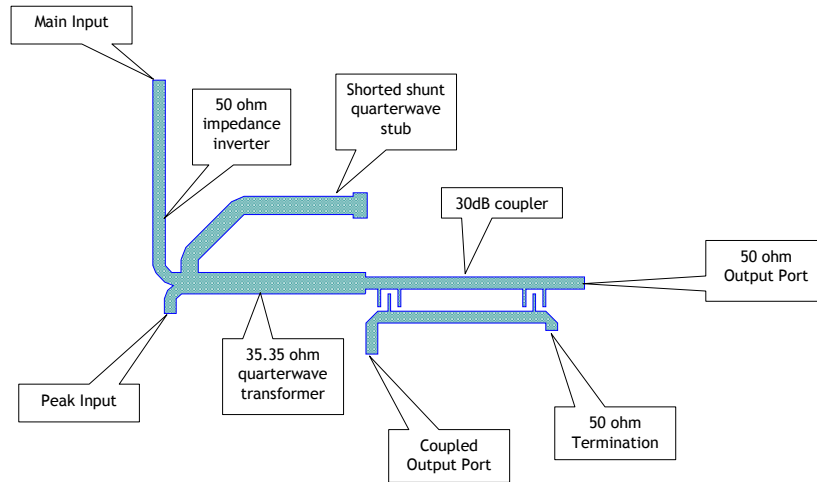


Figure 16: Calculated input impedance of classical Doherty combiner with cascaded coupler. Note that " $\text{Re}(|ZIN(1)|)$ " denotes the real part of the input impedance at port 1, and so forth

<sup>19</sup> Given by  $20 \log \left( \frac{|S_{31}|}{|S_{41}|} \right)$

To minimize the variation of the imaginary part of the impedance at port 1 and, hence, broaden the operating band of the combiner with cascaded coupler a shorted shunt quarter-wave stub is added as shown in Figure 17.

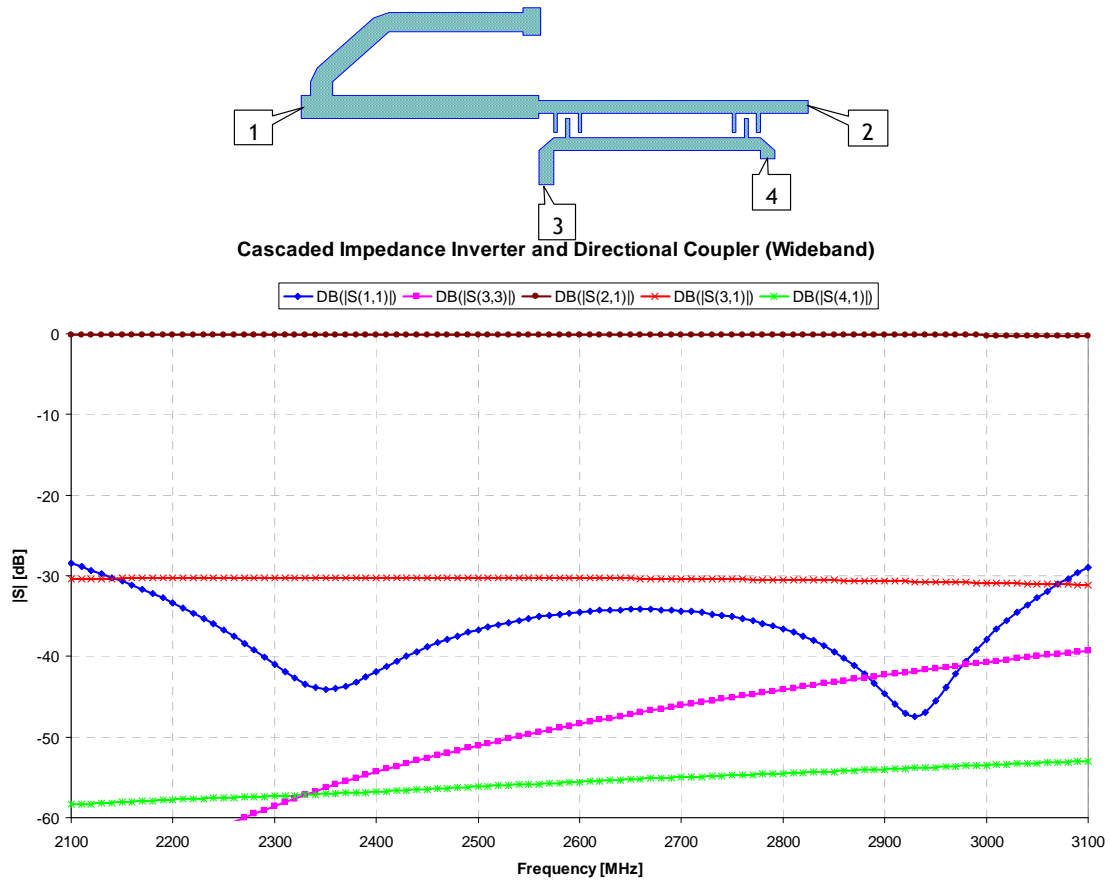


**Figure 17: Wideband Doherty combiner with cascaded coupler**

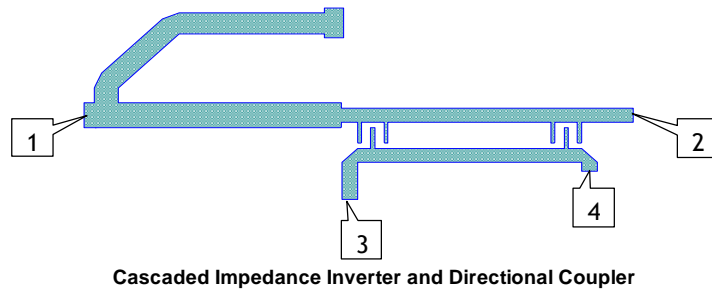
The S-parameters of the broadband combiner with the cascaded directional coupler are shown in Figure 18. The coupling factor is unchanged at  $30dB$ , the return loss at port 1 improved to better than  $30dB$  over almost the entire band, the coupled port 3 return loss remained better than  $40dB$ , the isolation<sup>20</sup> is better than  $20dB$  (the isolation performance was not included into the coupler design optimization process and it is likely it could be improved by including it in the optimization routine).

The input impedance at port 1, shown in Figure 19, is very close to  $25\Omega$  over the entire band. The real part varies between  $24$  and  $27\Omega$ , and the imaginary part stays very close to zero (from  $-1.5$  to  $0.6\Omega$ ).

<sup>20</sup> Given by  $20\log\left(\frac{|S_{31}|}{|S_{41}|}\right)$



**Figure 18: Calculated S-parameter performance of wideband Doherty combiner with cascaded coupler. Note that "DB(|S(1,1)|)" denotes  $|S_{11}|$  in dB, and so forth.**



Cascaded Impedance Inverter and Directional Coupler

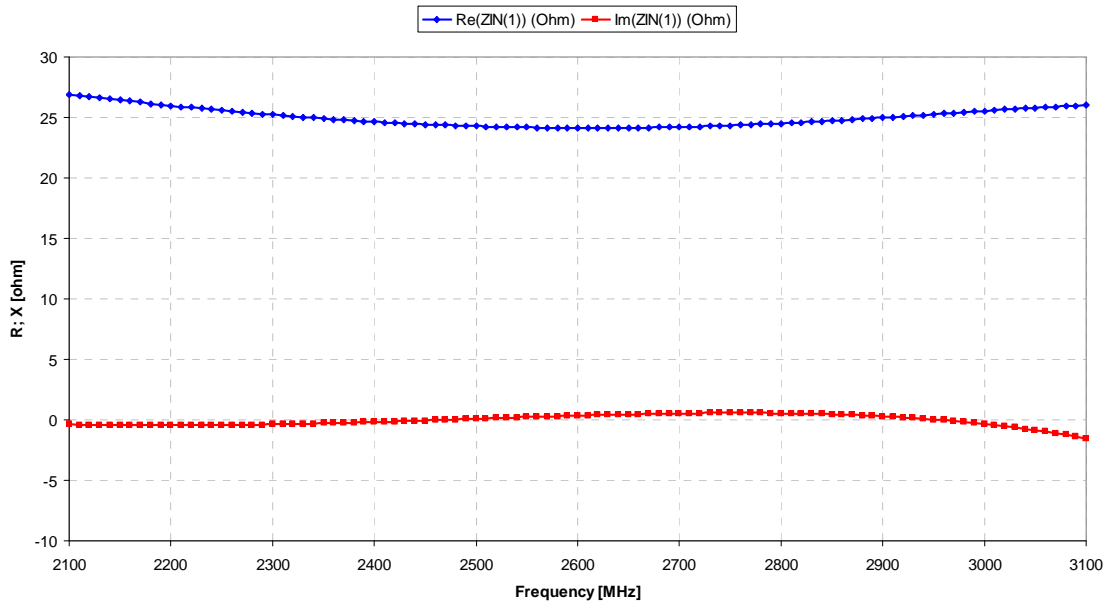
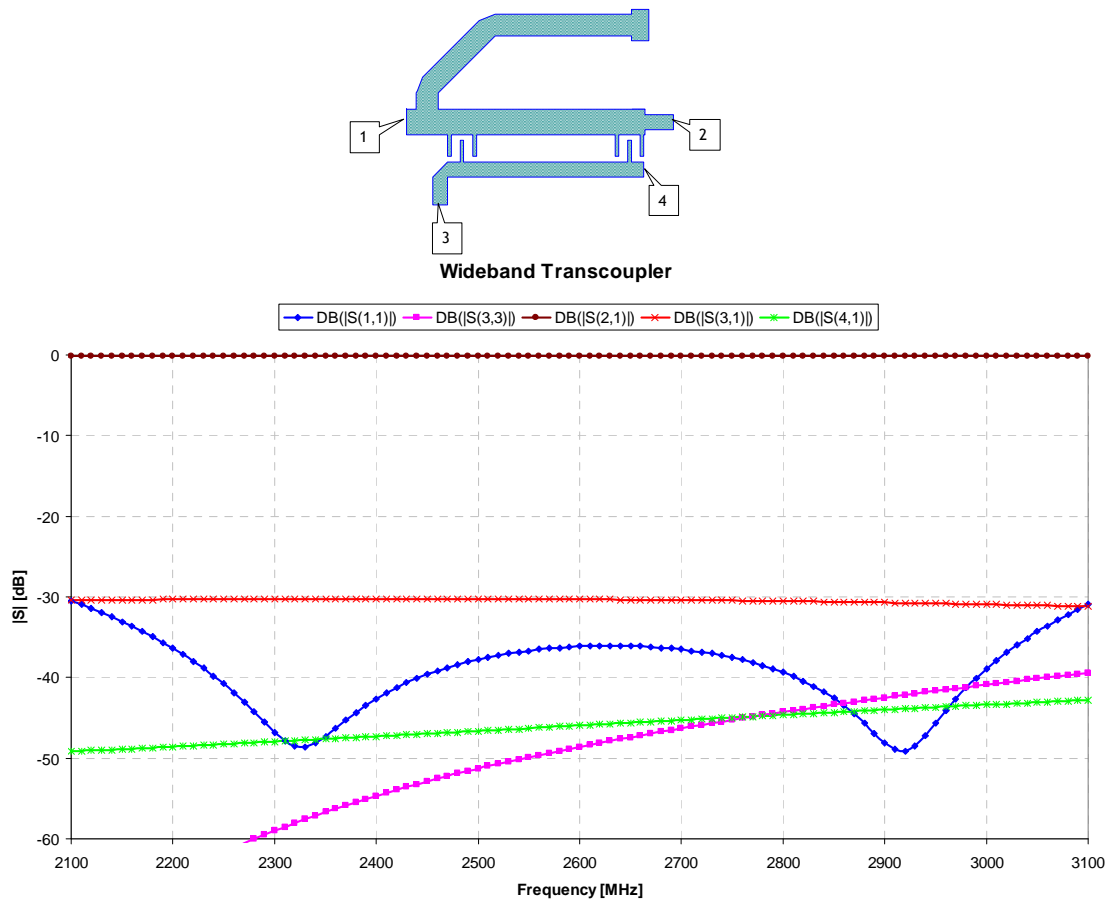


Figure 19: Calculated input impedance performance of wideband Doherty combiner with cascaded coupler. Note that " $\text{Re}(\text{ZIN}(1))$ " denotes the real part of the input impedance at port 1, and so forth

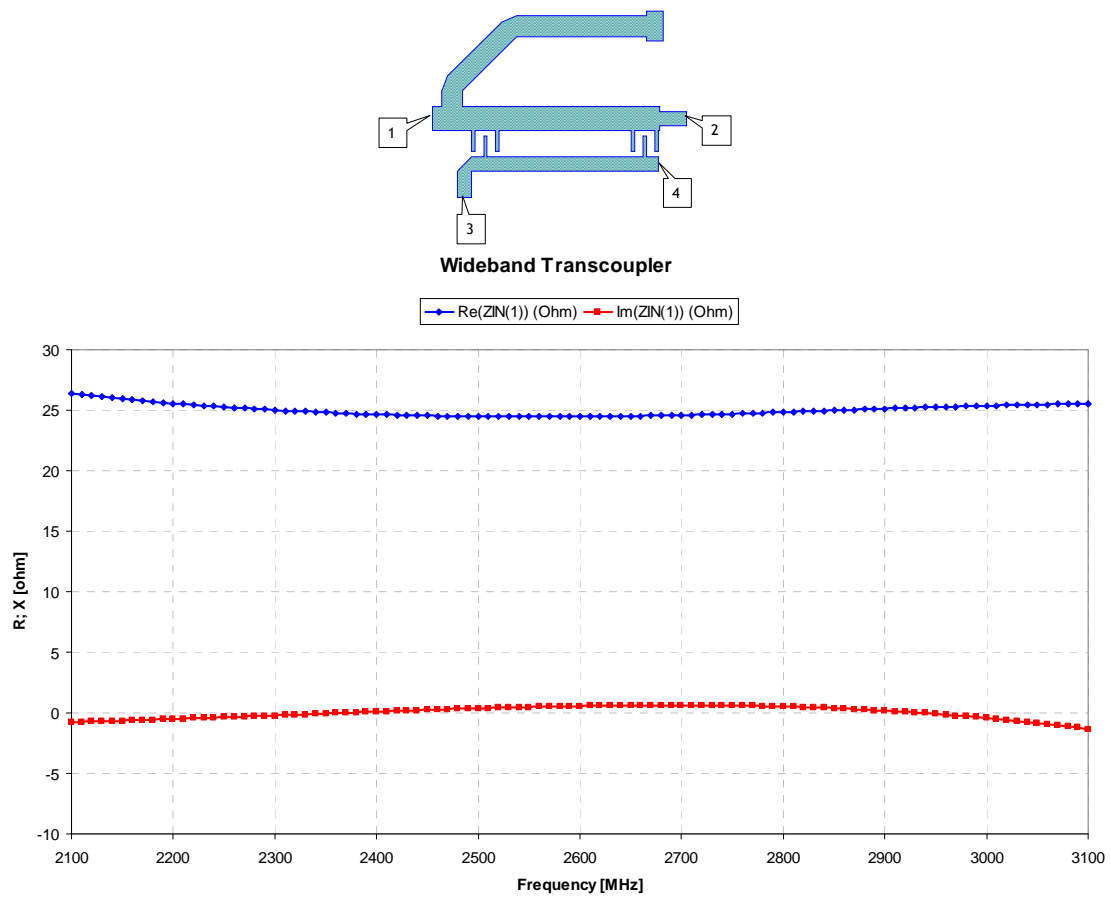
Now that we have examined the performance of the conventional combiner-coupler cascade we turn our attention to the performance of the Doherty node transformer based on a transcoupler. The microstrip layout implementation of the transcoupler is shown in Figure 20. To preserve wideband performance of the combiner the shorted shunt quarter-wave stub is added (same as in the case of the cascaded coupler in Figure 17). As mentioned before the mismatched coupler which we refer to as transcoupler, combines the impedance transforming capability of a quarter-wave transformer with a coupling capability of a directional coupler in one device, as shown in Figure 20.

The S-parameter performance of the transcoupler shown in Figure 20 indicates a better than  $30dB$  return loss at port 1 over the entire  $1GHz$  band centered at  $2.6GHz$ , the coupling factor remains close to  $30dB$  over the band, the return loss at the coupling port is better than  $40dB$ , and there is a slight degradation in the isolation<sup>21</sup> to around  $12dB$  at the high end of the frequency band, but as noted earlier the isolation performance was not included into the optimization routine and could probably be improved upon by its inclusion in the optimization process.



**Figure 20: Calculated S-parameters of a Doherty node transformer based on a wideband Transcoupler microstrip implementation layout**

<sup>21</sup> Given by  $20 \log \left( \frac{|S_{31}|}{|S_{41}|} \right)$



**Figure 21: Calculated input impedance at port 1 of a Doherty node transformer based on a wideband Transcoupler microstrip implementation layout**

The input impedance of the transcoupler is very close to  $25\Omega$  over the entire band which indicates broadband operation. Thus far we have only presented transcoupler as a replacement for the node impedance transformer and cascaded directional coupler.

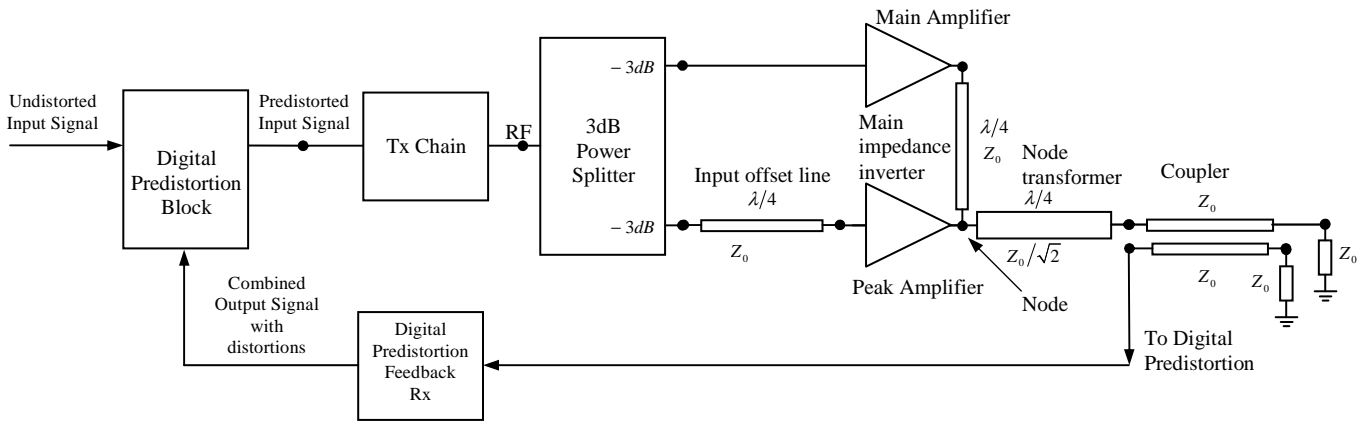
### 3.2.3 Use of the Transcouplers as Impedance Transformers and Inverters

We will use a transcoupler as a Doherty amplifier node transformer where it will replace the current implementation of the node transformer consisting of the cascaded combination of a quarter-wave impedance transformer and a directional coupler. Another transcoupler will be used to replace the main amplifier impedance inverter. When in place, the transcouplers will provide necessary impedance transformations while simultaneously providing feedback signals for digital predistortion purposes.

In the classic Doherty combiner, the signal is only sampled at the output, after the signals from the main and peak branch are already combined, and thus it is impossible to distinguish the distortion contributions coming from the main amplifier device from those coming from the peak amplifier device. In a classical Doherty amplifier the distinction between distortions coming from main or peak device may not have significance because the same signal is fed to both devices. However, in more advanced version of Doherty amplifiers [39], [40], (known as "digital Doherty amplifiers") the signals are fed to the main and peak amplifiers separately, and there would be a benefit to distinguishing the distortions produced by the main device from those produced by the peak device because the appropriate correction could then be applied to the main and peak devices separately to achieve an improvement in performance. To separate the distortions according to their origins we would need to sample the signals at two distinct locations simultaneously and thus obtain knowledge of the main and peak signals as they are before they are combined. The first sampling location is in the main branch and the sampling is achieved by replacing a  $Z_0$  quarter-wave transformer in the Doherty combiner with a  $Z_0$  transcoupler which will simultaneously work as an impedance inverter and as a directional coupler. This sampled signal will be a function of both main and peak signal, and will provide us with the first of the two equations necessary to resolve the main branch and peak branch signals. The second equation comes from sampling the combined signal at the output node transformer. The two equations are linearly independent and can be used to calculate the load currents of each branch at the combining node (and hence the

instantaneous power that each branch contributes). A detailed circuit analysis will be presented shortly.

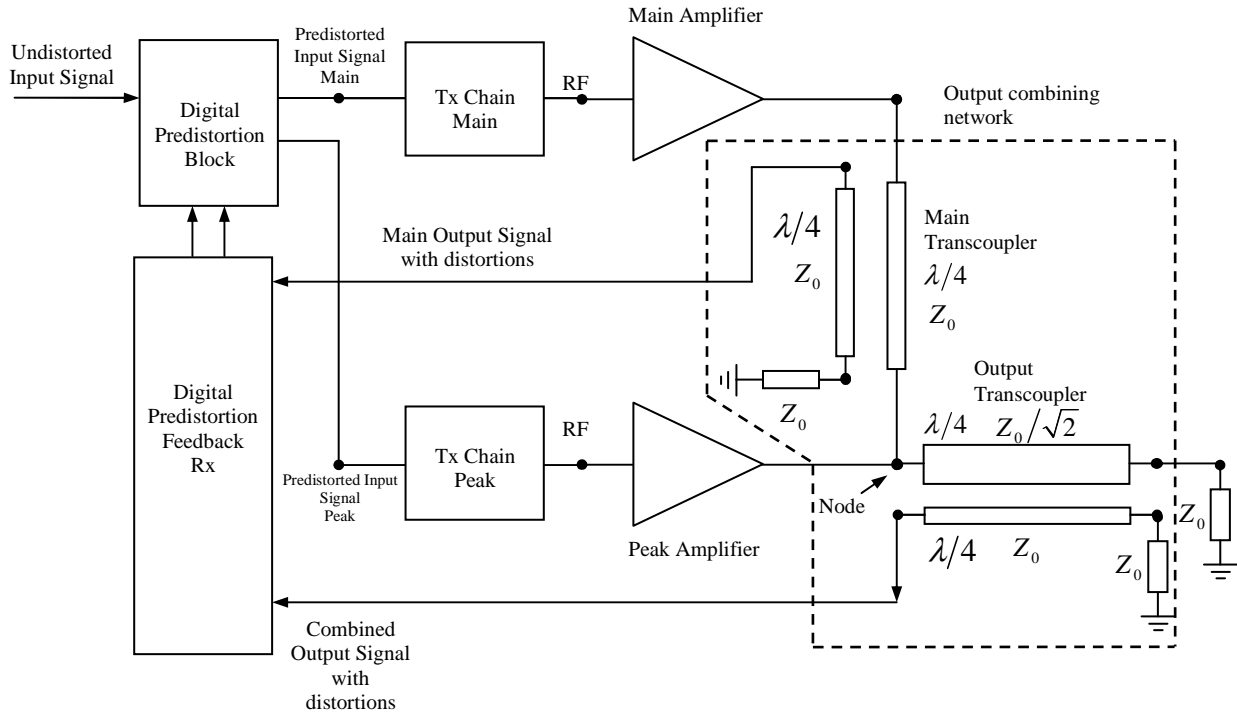
The classical implementation of the Doherty amplifier is shown in Figure 22. The input signal is split between the main and peak branches, amplified and combined to yield the output signal which is then sampled and sent to the predistortion receiver. Based on this feedback the input signal is predistorted and sent to the amplifier. In this implementation there is no way to correct for the main and peak distortions separately.



**Figure 22: The classical implementation of the Doherty amplifier**

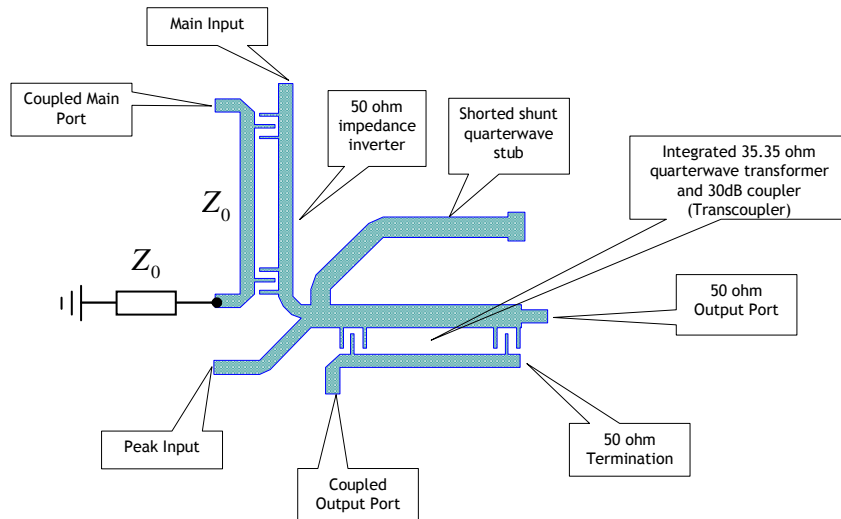
Once the combined output signal, with distortions resulting from amplifier nonlinearities, is sampled and sent through a digital predistortion receiver to the digital predistortion block. In the digital predistortion block the distorted signal is compared to its undistorted copy and appropriate modifications are applied to the input signal (predistortion) that will decrease the amount of the distortion present in the combined output signal. This solution features a single Tx chain and the common signal is fed to both main and peak amplifiers thus individual predistortion for main and peak amplifiers is not possible.

In the advanced implementation of the digital Doherty we propose (Figure 23), two separate input signals are applied, one to the main and one to the peak branch, the signals are amplified by their respective devices, sampled by the transcouplers and sent to two predistortion receivers, and then combined to yield the output signal. Based on the separate feedback the input signals are specifically predistorted according to their respective device distortion profiles. The above mentioned implementation is shown in Figure 23.



**Figure 23: The Digital Doherty implementation of the Doherty amplifier. Note that the transcoupler elements shown are block diagram elements not actual layouts [41].**

A microstrip layout implementation of the output combining network from Figure 23 is shown in Figure 24



**Figure 24: Improved Bandwidth Doherty Combiner with 50ohm/30dB Main Transcoupler and 35.35ohm/30dB Output Transcoupler**



The load reflection coefficient is given by

$$(3) \quad \Gamma_L = S_{11}^C = -\frac{1}{3}$$

The load impedance at the node is then

$$(4) \quad Z_L = Z_0 \frac{1 + \Gamma_L}{1 - \Gamma_L} = Z_0 \frac{1 - \frac{1}{3}}{1 + \frac{1}{3}} = \frac{Z_0}{2}$$

The voltage at the node can then be expressed in terms of the current from the main and peak branch load side currents  $I_{LM}$  and  $I_{LP}$  respectively and the node impedance  $Z_L$ , as

$$(5) \quad V = (I_{LM} + I_{LP})Z_L = (I_{LM} + I_{LP})\frac{Z_0}{2}$$

The impedance loading the main branch of the Doherty amplifier is given by

$$(6) \quad Z_{LM} = \frac{V}{I_{LM}} = \frac{I_{LM} + I_{LP}}{I_{LM}} \frac{Z_0}{2}$$

The corresponding reflection coefficient there is then

$$(7) \quad \Gamma_{LM} = \frac{Z_{LM} - Z_0}{Z_{LM} + Z_0} = \frac{\frac{I_{LM} + I_{LP}}{I_{LM}} \frac{Z_0}{2} - Z_0}{\frac{I_{LM} + I_{LP}}{I_{LM}} \frac{Z_0}{2} + Z_0} = \frac{I_{LM} + I_{LP} - 2I_{LM}}{I_{LM} + I_{LP} + 2I_{LM}} = \frac{I_{LP} - I_{LM}}{I_{LP} + 3I_{LM}}$$

We can now calculate the voltage on the main device side of the main branch transcoupler in three steps as

$$(8) \quad V_M = \frac{1 + S_{11}^M - (S_{22}^M + S_{11}^M S_{22}^M - S_{12}^M S_{21}^M) \Gamma_{LM}}{S_{21}^M (1 + \Gamma_{LM})} V = \frac{1 + (-j)(-j) \Gamma_{LM}}{-j(1 + \Gamma_{LM})} (I_{LM} + I_{LP}) \frac{Z_0}{2}$$

$$(9) \quad V_M = j \frac{1 - \Gamma_{LM}}{1 + \Gamma_{LM}} (I_{LM} + I_{LP}) \frac{Z_0}{2} = j \frac{I_{LP} + 3I_{LM} - I_{LP} + I_{LM}}{I_{LP} + 3I_{LM} + I_{LP} - I_{LM}} (I_{LM} + I_{LP}) \frac{Z_0}{2}$$

$$(10) \quad V_M = j \frac{4I_{LM}}{2(I_{LM} + I_{LP})} (I_{LM} + I_{LP}) \frac{Z_0}{2} = jZ_0 I_{LM}$$

The reflection coefficient on the device side is given by

$$(11) \quad \Gamma_M = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LM}}{1 - S_{22}^M \Gamma_{LM}} = (-j)(-j)\Gamma_{LM} = -\Gamma_{LM}$$

and so from (7) it is

$$(12) \quad \Gamma_M = \frac{I_{LM} - I_{LP}}{I_{LP} + 3I_{LM}}$$

In order to find the voltage incident on the device side of the main branch transcoupler we note that

$$(13) \quad V_M = V_M^+ + V_M^- = V_M^+ (1 + \Gamma_M)$$

thus we can write

$$(14) \quad V_M^+ = \frac{V_M}{(1 + \Gamma_M)} = \frac{jI_{LM}Z_0}{1 + \frac{I_{LM} - I_{LP}}{I_{LP} + 3I_{LM}}} = j\frac{Z_0}{4}(I_{LP} + 3I_{LM})$$

which simplifies to

$$(15) \quad V_M^+ = j\frac{Z_0}{4}(I_{LP} + 3I_{LM})$$

$V_M^+$  is known from the measured coupled signal by the means of the receiver attached to the coupled port. This gives us the first equation that will allow us to calculate the branch currents  $I_{LP}$  and  $I_{LM}$  at the combining node. At the node side of the node transcoupler the voltage is given by

$$(16) \quad V = V_L^+ + V_L^- = V_L^+ (1 + \Gamma_L) = (I_{LM} + I_{LP})\frac{Z_0}{2}$$

thus we have

$$(17) \quad V_L^+ = \frac{(I_{LM} + I_{LP})Z_0}{1 + \Gamma_L} \frac{1}{2} = (I_{LM} + I_{LP})\frac{Z_0}{2\left(1 - \frac{1}{3}\right)}$$

which simplifies to

$$(18) \quad V_L^+ = \frac{3Z_0}{4}(I_{LM} + I_{LP})$$

$V_L^+$  is known from the measured coupled signal by means of the receiver attached to the coupled port. This gives us the second equation that will allow us to calculate the branch currents  $I_{LP}$  and  $I_{LM}$  at the combining node.

Expressions (15) and (18) are the two equations needed to solve for main and peak branch currents at the combining node. We can rewrite them in the forms

$$(19) \quad 3I_{LM} + I_{LP} = -j\frac{4}{Z_0}V_M^+$$

and

$$(20) \quad I_{LM} + I_{LP} = \frac{4}{3Z_0}V_L^+$$

Solving for  $I_{LM}$  and  $I_{LP}$  we get

$$(21) \quad I_{LM} = -\frac{2}{3Z_0}(V_L^+ + 3jV_M^+)$$

and

$$(22) \quad I_{LP} = \frac{2}{Z_0}(V_L^+ + jV_M^+)$$

The load currents of the two branches are now known in terms of sampled incident voltages  $V_M^+$  and  $V_L^+$ .

The combined output signal  $V_L^+$ , and the main output signal  $V_M^+$  both with the corresponding distortions resulting from amplifier nonlinearities are sampled and sent through a digital predistortion receiver (the receiver block will have two receivers, one for each feedback signal) to the digital predistortion block. In the digital predistortion block, each distorted signal is compared to the undistorted copy of the signal and the appropriate modifications are applied to the input signals (predistortion) of the main and

peak branches that will result in the decrease of the distortion present in the combined output signal. This solution features two Tx chains (one for main branch and one for peak branch) with each branch being excited by appropriately predistorted input signals.

### 3.2.4 Reasons why a cascade of a coupler and an impedance inverter will not behave as an impedance inverter

In the situation where a transition from a  $2Z_0$  impedance domain to a  $\frac{Z_0}{2}$  domain is required, an impedance inverter with a characteristic impedance  $Z_0$  can be used to provide matching via the impedance inverting relationship  $Z_{IN} = \frac{Z_0^2}{Z_L}$ . We will use the impedance values that are common in the design of symmetric two-way Doherty amplifiers (e.g.  $100\Omega$  for the main amplifier high efficiency load,  $50\Omega$  for the characteristic impedance of the main quarter-wave impedance inverter, and  $25\Omega$  for the node impedance) for the above mentioned domains as depicted in Figure 26.

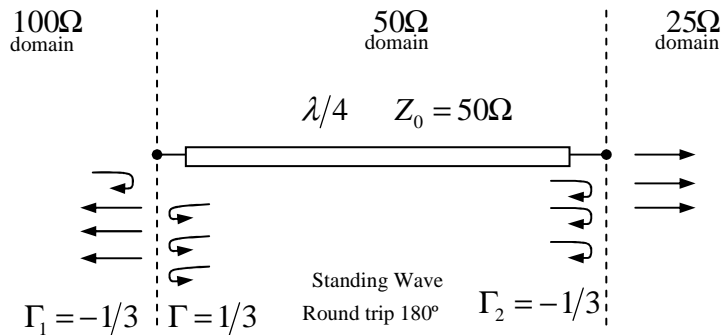
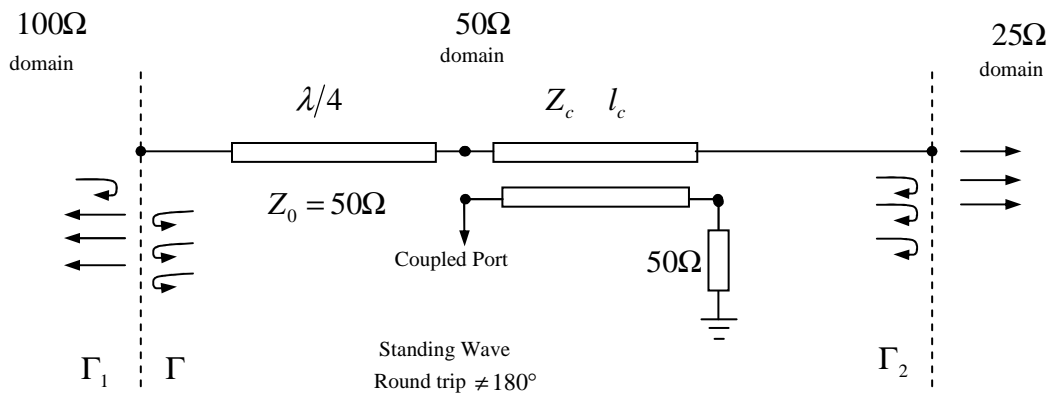


Figure 26: Quarter-wave transformer impedance inverter

To have the perfect impedance inversion the reflected waves in the  $100\Omega$  domain must cancel each other and transmitted waves in the  $25\Omega$  domain must combine constructively. The reflection coefficients and propagation delays between interfaces must be set properly, i.e.  $\Gamma_1 = \Gamma_2$  and round trip delay must be  $180^\circ$ , to achieve the perfect cancellation of reflected waves and perfect combining of transmitted waves. If  $\Gamma_1 \neq \Gamma_2$

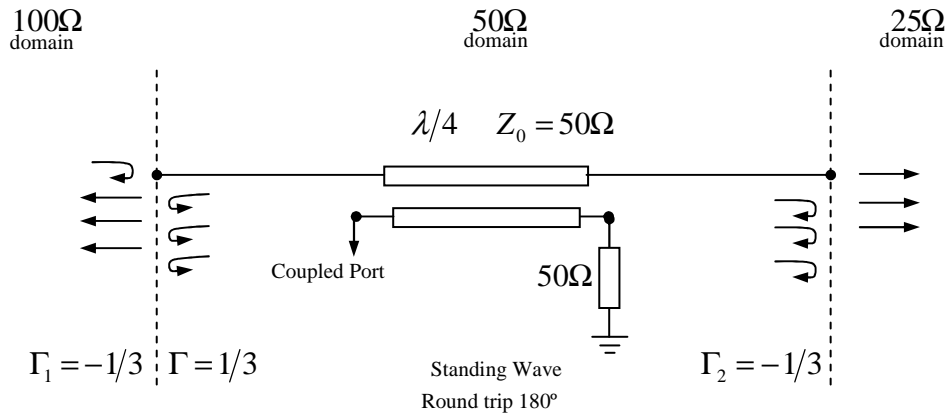
and/or the round trip is not equal to  $180^\circ$  the impedance inversion will not be ideal. In the case of the quarter-wave impedance inverter in Figure 26,  $\Gamma_1 = \Gamma_2 = -1/3$  and since the line length is  $90^\circ$ , that makes the round trip exactly  $180^\circ$ , thus satisfying both conditions simultaneously and providing perfect impedance inversion.

If we desire to sample the signal from the  $100\Omega$  domain that is incident on  $50\Omega$  domain we need to cascade the  $50\Omega$  impedance inverter with a directional coupler that has a characteristic impedance  $Z_c$  and length  $l_c$  as shown in Figure 27. In the case where  $Z_c = 50\Omega$  and  $l_c$  is a multiple of  $180^\circ$ , the conditions for perfect inversion, namely  $\Gamma_1 = \Gamma_2 = -1/3$  and a round trip being a multiple of  $180^\circ$ , are satisfied albeit at the expense of decreased bandwidth. The decrease in bandwidth stems from the increase in length of the structure in Figure 27 compared to that of the structure in Figure 26. However, if either one of the conditions,  $Z_c = 50\Omega$  and  $l_c$  being a multiple of  $180^\circ$ , is not satisfied the perfect impedance inversion will not occur. Thus if we do not want to sacrifice bandwidth of operation we cannot use a cascade of an impedance inverter and a directional coupler to simultaneously achieve impedance inversion and signal sampling.



**Figure 27: Quarter-wave transformer impedance inverter cascaded with a directional coupler**

In order to maintain bandwidth performance while simultaneously having impedance inversion and signal sampling capability we can use the structure in Figure 28.

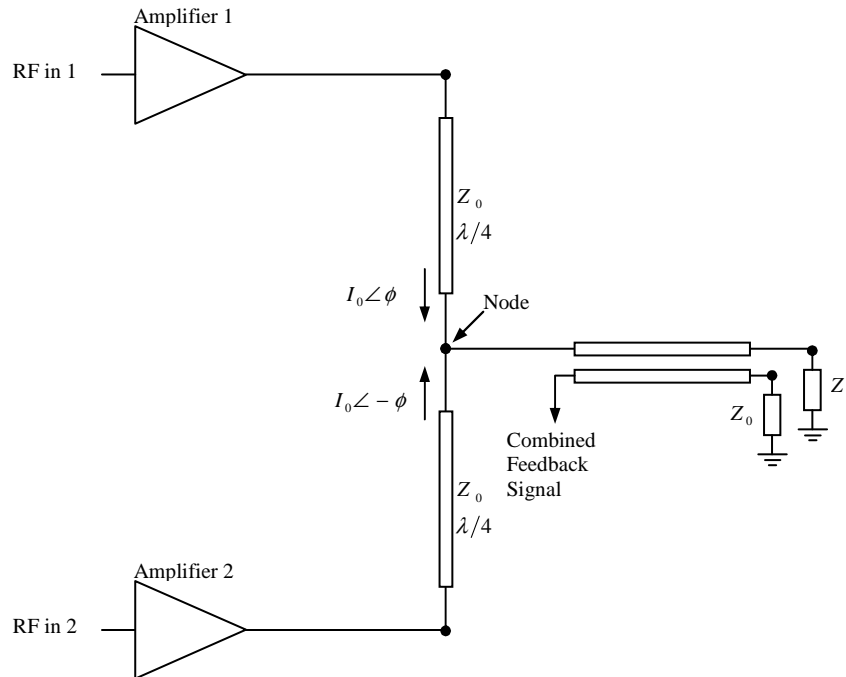


**Figure 28: Impedance inverting/transforming directional coupler**

The main branch of the directional coupler in Figure 28 is  $50\Omega$  quarter-wave transformer which automatically satisfies the ideal impedance inverting conditions,  $\Gamma_1 = \Gamma_2 = -1/3$  due to  $50\Omega$  characteristic impedance, and since the line length is  $90^\circ$  the round trip is exactly  $180^\circ$ . The coupled branch is there to provide signal coupling for the feedback purposes. The length of the coupled line and its proximity to the main branch are determined in such a way to provide sufficient feedback signal levels while maintaining the minimum impact on impedance inverting capability of the main branch.

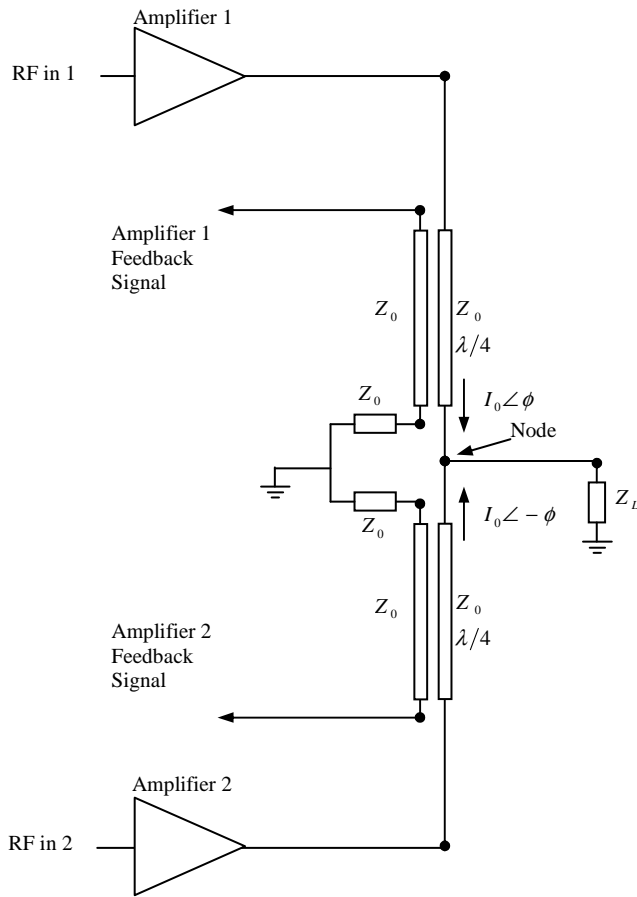
### 3.2.5 Application of transcouplers in Chireix Amplifier

A Chireix amplifier in Figure 29 combines two complex-conjugate constant envelope signals in order to obtain an amplitude modulated combined output signal. Combining of the complex-conjugate signals from Amplifiers 1 and 2 at the node, and inverting the modulated branch load impedances by the corresponding quarter-wave transformers presents the amplifiers 1 and 2 with load impedances that are associated with the high-power operation of the amplifiers 1 and 2 (currents combine in phase at the node,  $\phi = 0^\circ$ ), or moving toward impedances associated with the high efficiency operation of the amplifiers (current combining is out-of-phase by an increasing amount with increase in  $\phi$ ).



**Figure 29: Functional diagram of a Chireix Amplifier [42]**

To accurately create the desired amplitude modulation of the combined output signal (from the distinct phase information contained in the signal from each branch) the precise control of the branch signal phase shifts at the combining node is essential. The transcouplers can be used to provide a feedback signal from each branch and allow for an explicit control and correction of the phase for each signal before combining as shown in Figure 30.



**Figure 30: Functional diagram of a Chireix Amplifier with transcouplers**

Transcouplers can be used in any amplifier architecture that combines output signals from multiple branches of amplifying elements, uses impedance modulation and inversion as a means of increasing the efficiency of operation of the individual amplifying elements and uses feedback-based digital pre-distortion to optimize amplifier spectral performance (minimize spurious emissions). Examples of these amplifying architectures are (but not limited to) the Doherty and Chireix amplifiers as discussed above.

### ***3.3 Tunable Two-way Doherty Amplifier with a Circulator as an Impedance Inverting Element***

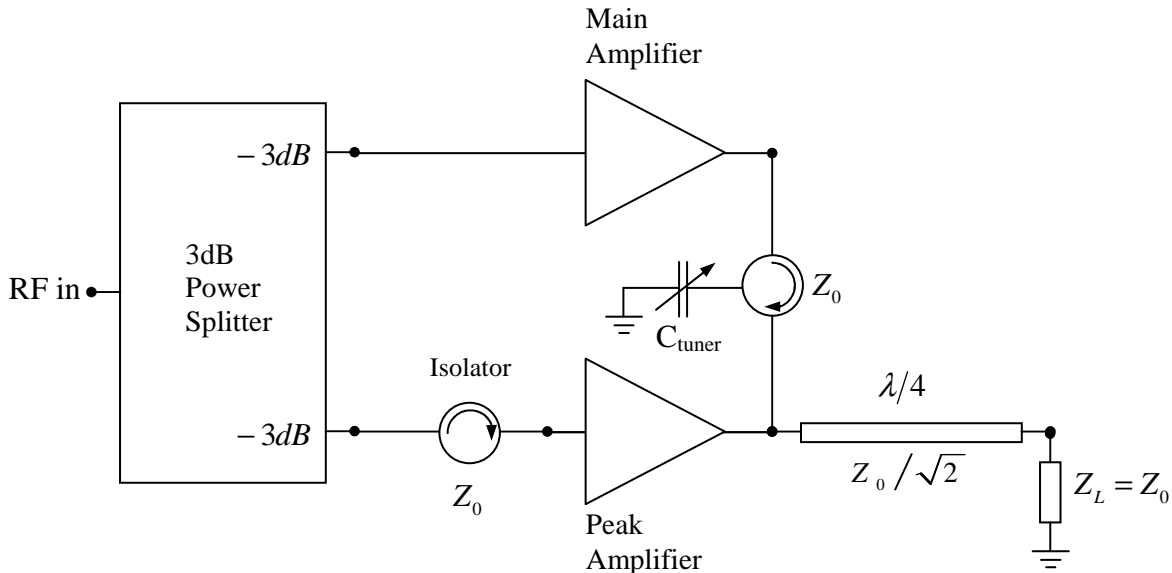
#### **3.3.1 Introduction**

Quarter-wave impedance inverters are band limited due to their physical properties, namely that impedance inversion depends on multiple reflection cancellations which can only be achieved for certain physical lengths and characteristic impedances of the transformer. A circulator with its third port terminated in a tuning circuit can be used as a tunable impedance inverter.

#### **3.3.2 Tunable Two-Way Doherty Amplifier**

High capacity wireless systems use modulated signals that exhibit high peak to average power ratios, which will cause power amplifiers to operate at low efficiency if certain efficiency enhancing features are not employed. The Doherty amplifier architecture utilizes the impedance modulation effect between the main and peak amplifier to modulate the load impedance seen by the main amplifier in accordance with the instantaneous input RF power. This results in higher efficiency of operation. The original Doherty design relies on a quarter-wave transformer to perform the impedance inversion necessary to achieve proper load modulation. Quarter-wave transformers are inherently narrowband structures (up to 10% of bandwidth) and are not dynamically tunable. To overcome the bandwidth limitation of quarter-wave impedance inverters, a tunable circulator-based impedance inverter is introduced here. The tunable circulator-based impedance inverter provides a narrowband impedance inversion (the bandwidth of the impedance inversion depends on the phase response of the circulator) but is tunable over the amplitude bandwidth of the circulator, thus making it more suitable for implementation in tunable Doherty architecture amplifiers. The tunability is achieved by terminating the third port of the circulator in a tuning circuit (usually consisting of two variable capacitors separated by a length of transmission line). The circulator has a broadband amplitude response and can provide tunable impedance inversion over its

amplitude bandwidth, thus making the design of a tunable broadband Doherty amplifier feasible. The block diagram of the suggested two-way Doherty amplifier employing a circulator-based tunable impedance inverter is given in Figure 31. We next discuss this idea in more detail.



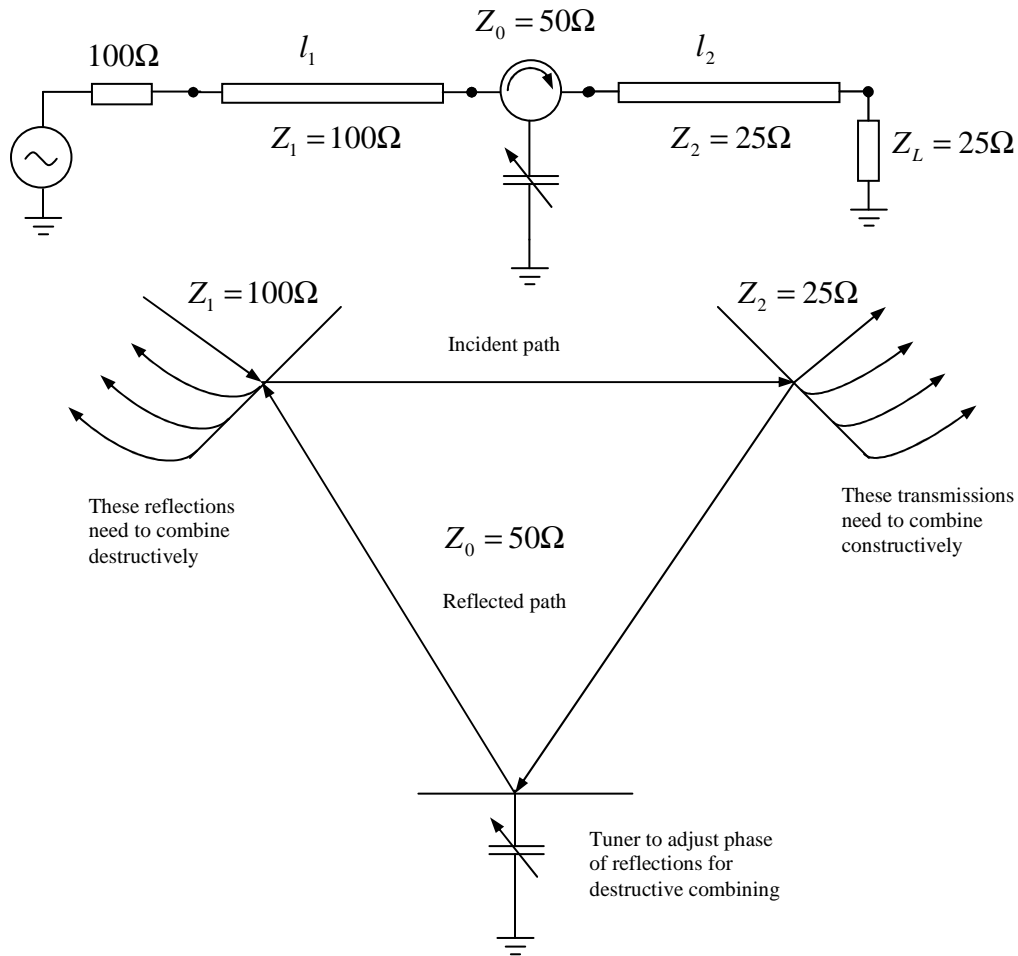
**Figure 31: Block diagram of a Two-Way Doherty amplifier with circulator-based impedance inverter after [44]**

The basic idea is to use the non-reciprocal property of a circulator to implement impedance inversion functionality that is necessary for proper operation of a Doherty amplifier. Circulators usually have a broadband amplitude response (e.g. 30%) which can be used to provide impedance inversion bandwidth<sup>22</sup> of, for example 2%, that can be tuned over the wider amplitude bandwidth and thus extend the fixed 10% bandwidth available from quarter-wave transformer impedance inverter.

The proper alignment of reflections at the input of the impedance inverter is essential for its correct operation. Splitting the incident and reflected paths provides us with an ability to dynamically tune the performance of the impedance inverter. A circulator is used to split the incident and reflected paths, and its third port is terminated in a tuning circuit which allows for dynamic phase tuning of the reflected waves in order

<sup>22</sup> Note: circulator-based impedance inverter provides a narrowband impedance inversion that can be tuned over the much wider circulator bandwidth

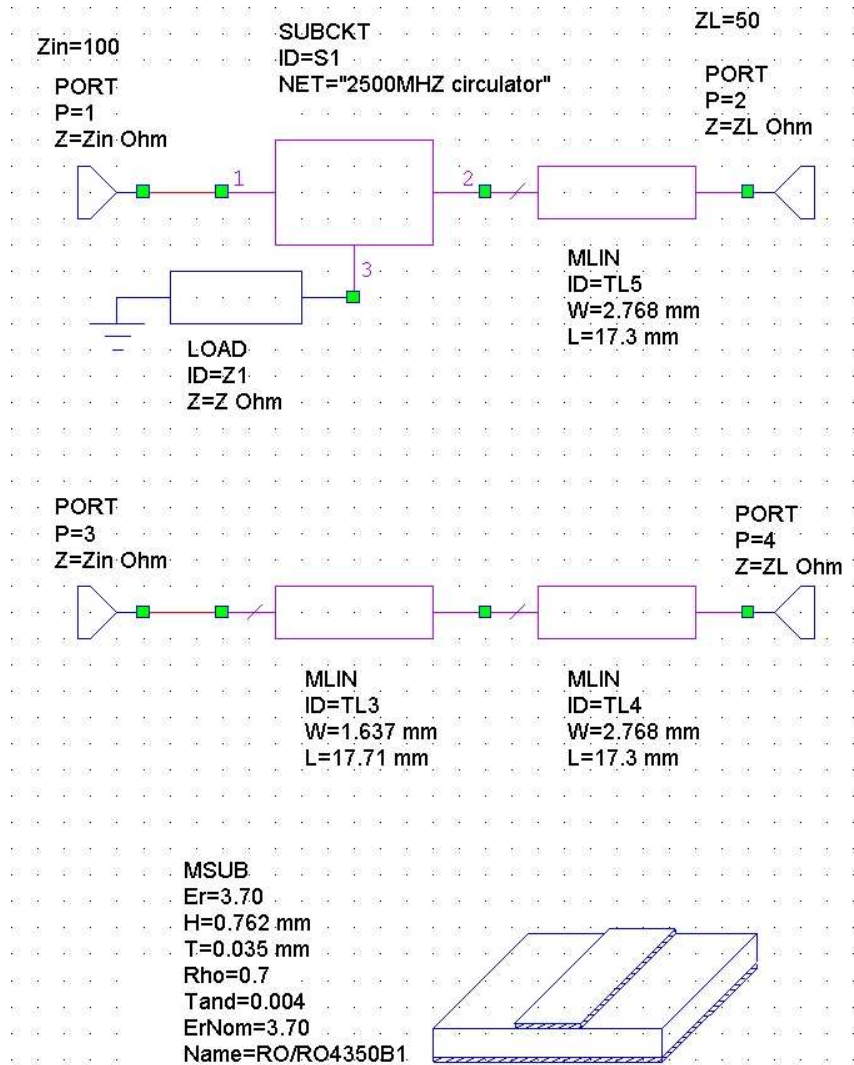
to achieve the destructive combining of the reflected waves at the input and thus obtain proper impedance inversion.



**Figure 32: Functional diagram of the circulator-based impedance inverter. The multiple arms are meant to indicate multiple reflected and transmitted signals.**

The wave bounces between three interfaces, and the incident and reflected waves undergo different phase shifts. The third port of the circulator is terminated in a tuning circuit consisting of two variable capacitors separated by a section of a microstrip line; for simplicity this is depicted by a single variable capacitor symbol in Figure 32. The reflection phase shift is adjusted for destructive combining at the input of the impedance inverter. When used as a main amplifier impedance inverter in a two-way Doherty amplifier as shown in Figure 31, the circulator is only mismatched in the low-power regime when the peak amplifier is inactive and the circulator is loaded by  $25\Omega$  node impedance. In the high-power regime peak amplifier is active and it modulates the load impedance seen by the circulator to  $50\Omega$  thus eliminating the reflections at high power.

The variable capacitors in the tuning circuits are therefore only exposed to reflected waves at low power levels. The schematic implementation of the circulator based impedance inverter and its quarter-wave counterpart is shown in Figure 33.



**Figure 33: Circulator based impedance inverter with associated tuning circuit**

The measured S-parameters of the circulator are imported into a circuit simulator; the third port of the circulator is terminated in a variable impedance load that represents the capacitive tuning circuit whose reactance can be adjusted externally. The second port of the circulator is terminated in the node impedance that is obtained by transforming 50Ω load into 25Ω node impedance by means of a microstrip transmission line whose length and width are adjusted to produce 35.4Ω quarter-wave transformer. The input

impedance performance of the circulator-based impedance inverter is monitored at the first port of the circulator. For the comparison purposes the second impedance inverting circuit was constructed where a section of a microstrip transmission line whose length and width are adjusted in a way to obtain the characteristics of  $50\Omega$  quarter-wave impedance inverter.

### 3.3.3 Performance of the Tunable Circulator Impedance Inverter

To verify the performance of a circulator as an impedance inverter the S-parameters of a  $2500\text{MHz}$  circulator were measured and imported into a circuit solver as an S-parameter file. The frequency response of the circulator is shown in Figure 34. The circulator has better than  $20\text{dB}$  return loss and isolation between  $2100\text{MHz}$  and  $2800\text{MHz}$  (a bandwidth of better than  $700\text{MHz}$  or circa 29%). The circulator used was CS-2500 SMA packaged circulator manufactured by e-Meca [45].

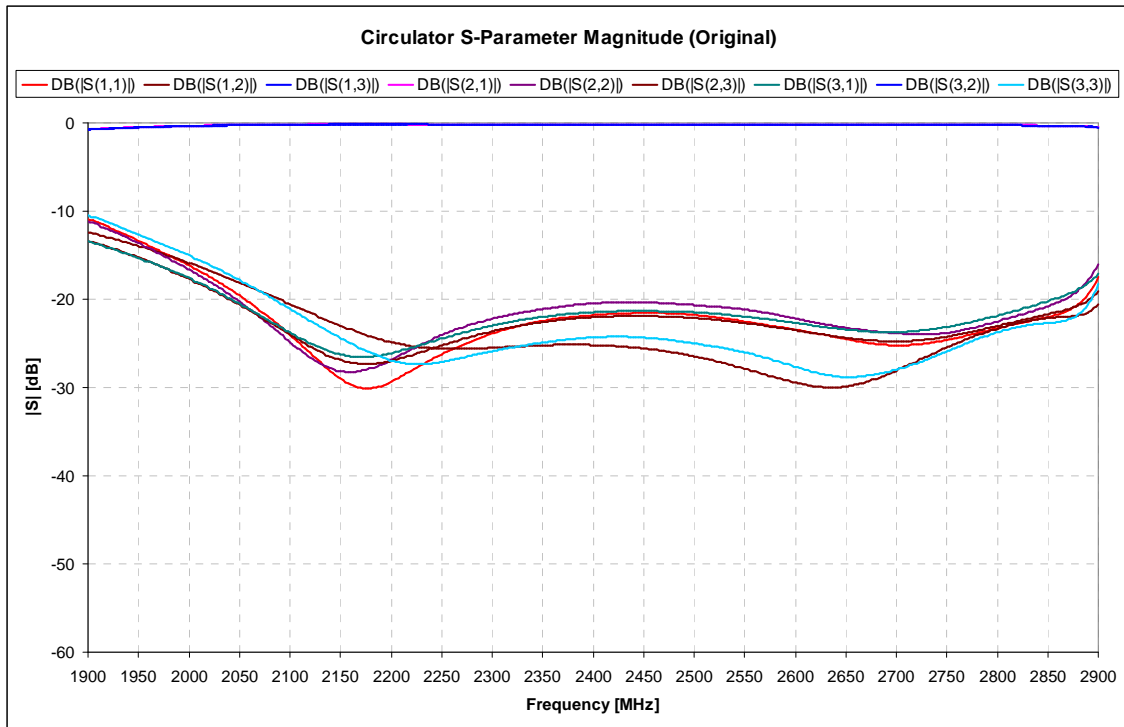
To investigate the effects of non-ideal matching and isolation parameters of the circulator under test, these parameters were artificially scaled by a factor of 2 thus yielding a  $6\text{dB}$  improvement in match and isolation over the original circulator. The frequency response of the circulator with  $6\text{dB}$  improved matching and isolation is shown in Figure 35.

Using the enhanced circulator S-parameters in the circulator block of Figure 33, and adjusting the value of the tuning capacitors, we can tune the impedance inverter to resonate at  $2300\text{MHz}$ . The overall frequency response is shown in Figure 36.

From Figure 36 we can see that over the  $20\text{MHz}$  band centered at  $2300\text{MHz}$  the real part of the input impedance of the circulator-based inverter is almost identical to that of the quarter-wave impedance inverter. The imaginary part of the input impedance of the circulator-based inverter is significantly lower than that of the quarter-wave inverter. As predicted the impedance inversion bandwidth of the circulator is significantly narrower compared to the quarter-wave transformer inverter mainly due to the circulator phase response ( $\angle S_{21}$ ,  $\angle S_{32}$ , and  $\angle S_{13}$ ). Next we tune the circulator-based impedance inverter to  $2500\text{MHz}$  and we observe (in Figure 37) similar impedance inverting behaviour to that of the previous case.

Finally we tune the circulator-based impedance inverter to  $2700\text{MHz}$  to verify the performance at the high end of the band (Figure 38) which is quite similar to that of the two previous cases. The circulator-based inverter input impedance real part tracks the real part of the quarter-wave inverter impedance, where as the imaginary part can be tuned out at a desired frequency in the case of the circulator based inverter.

For a better overview of the performance of the circulator-based impedance inverter we divided the entire band of interest into a number of  $20\text{MHz}$  channels and tuned the inverter to each of these channels, and captured the performance of the inverter for each one of these channels. The results are shown in Figure 39 and Figure 40.



**Figure 34: Measured circulator frequency response**

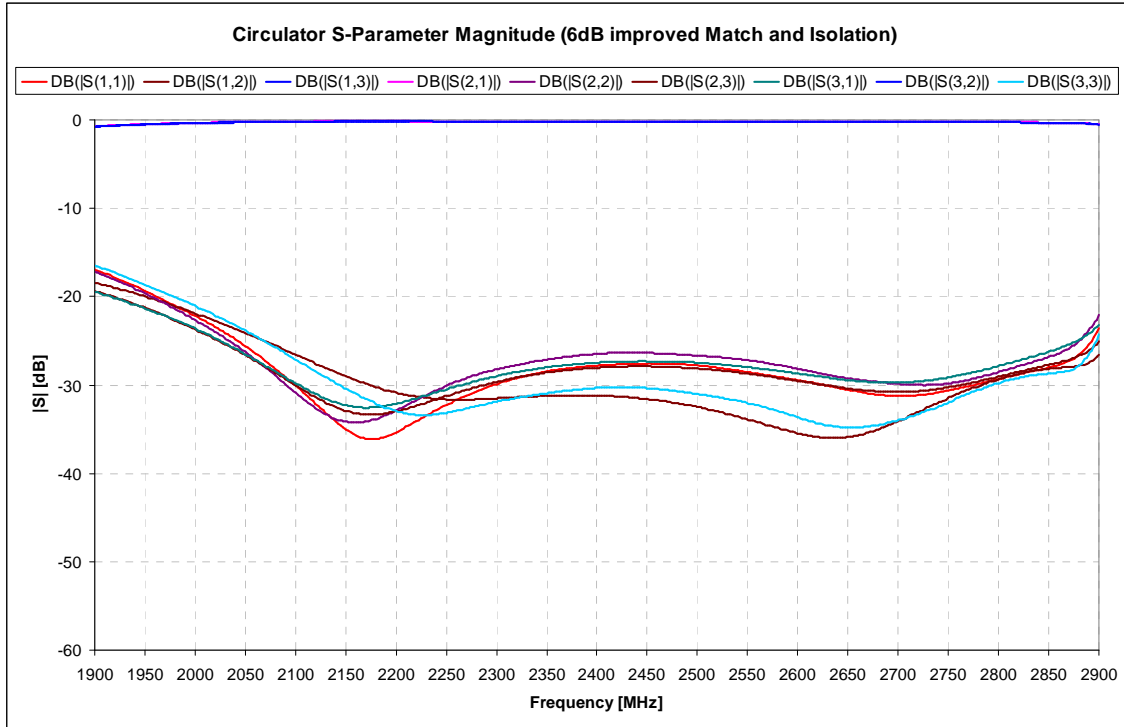


Figure 35: Calculated frequency response of a circulator with enhanced (6dB improvement) match and isolation

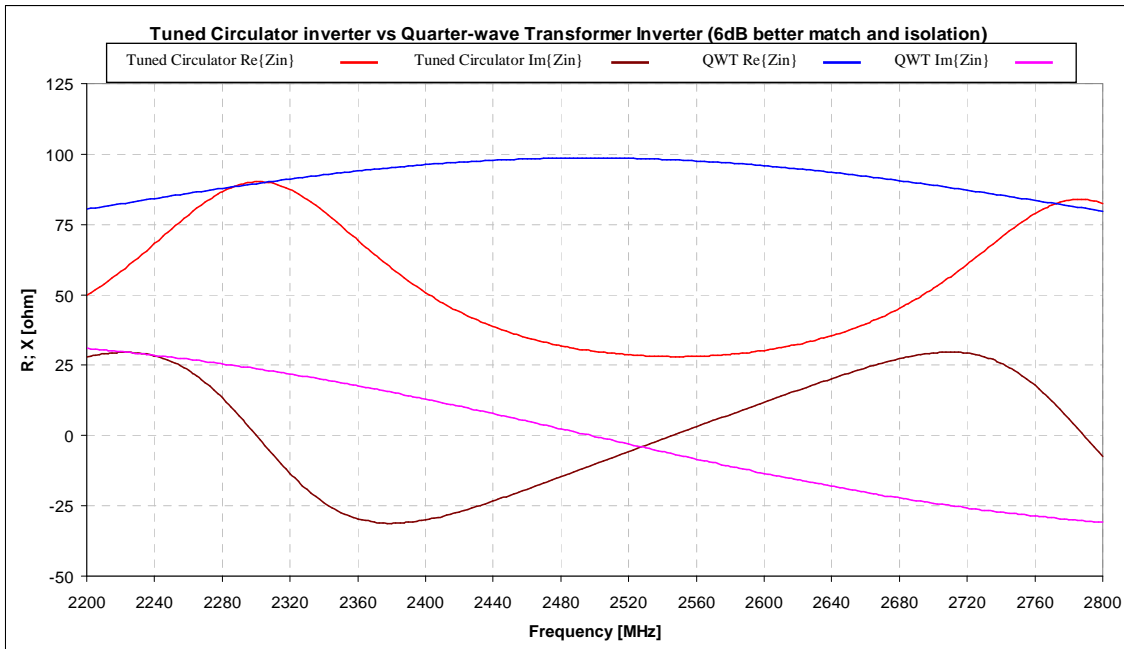
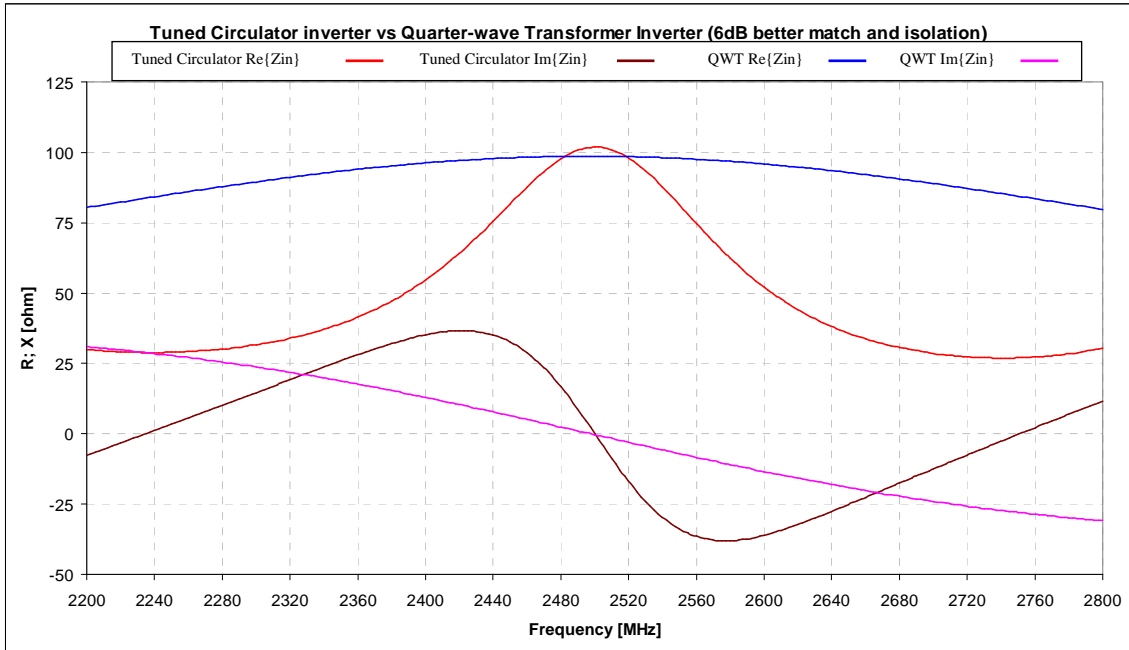
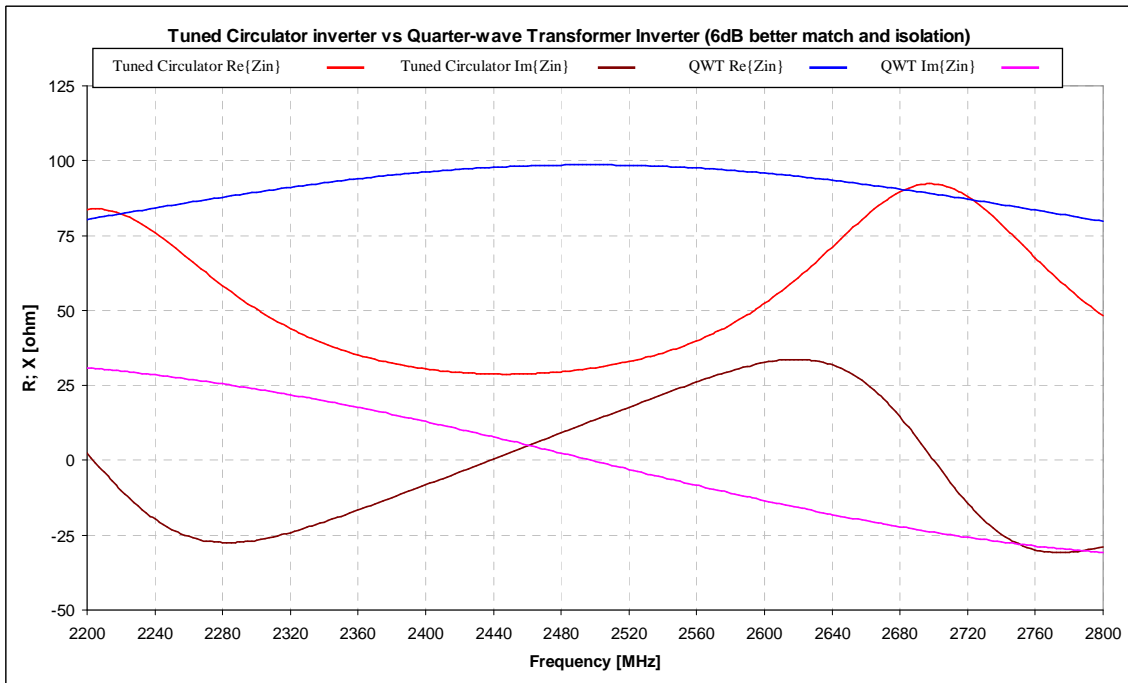


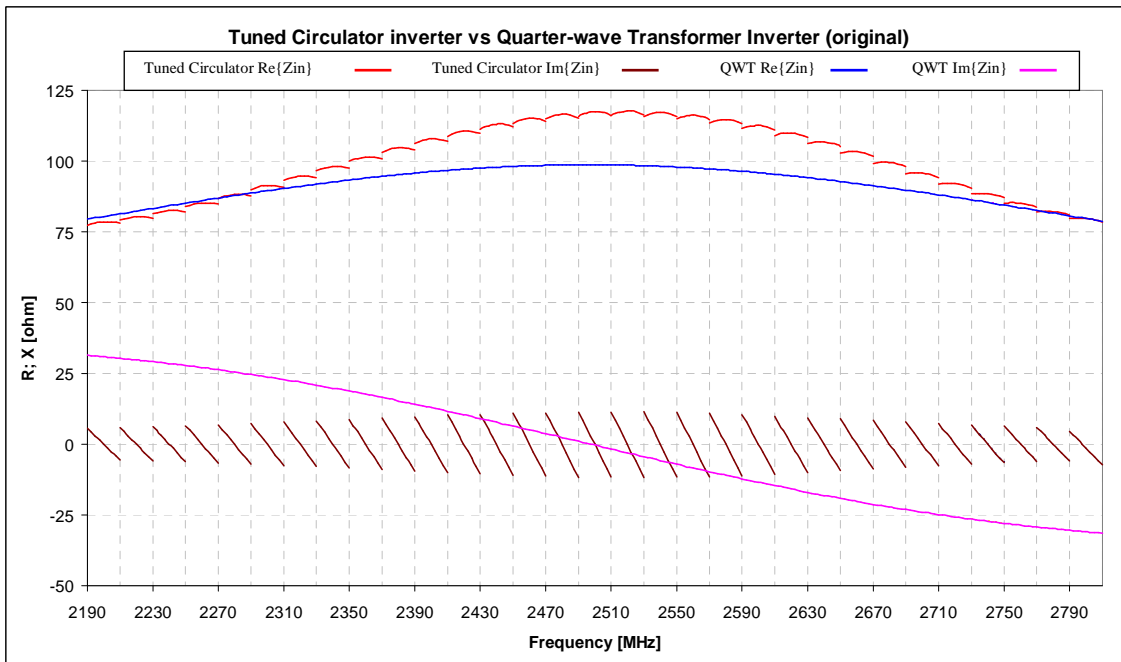
Figure 36: Calculated frequency response of the circulator-based inverter tuned to 2300MHz, compared to that of the quarter-wave transformer (QWT) inverter



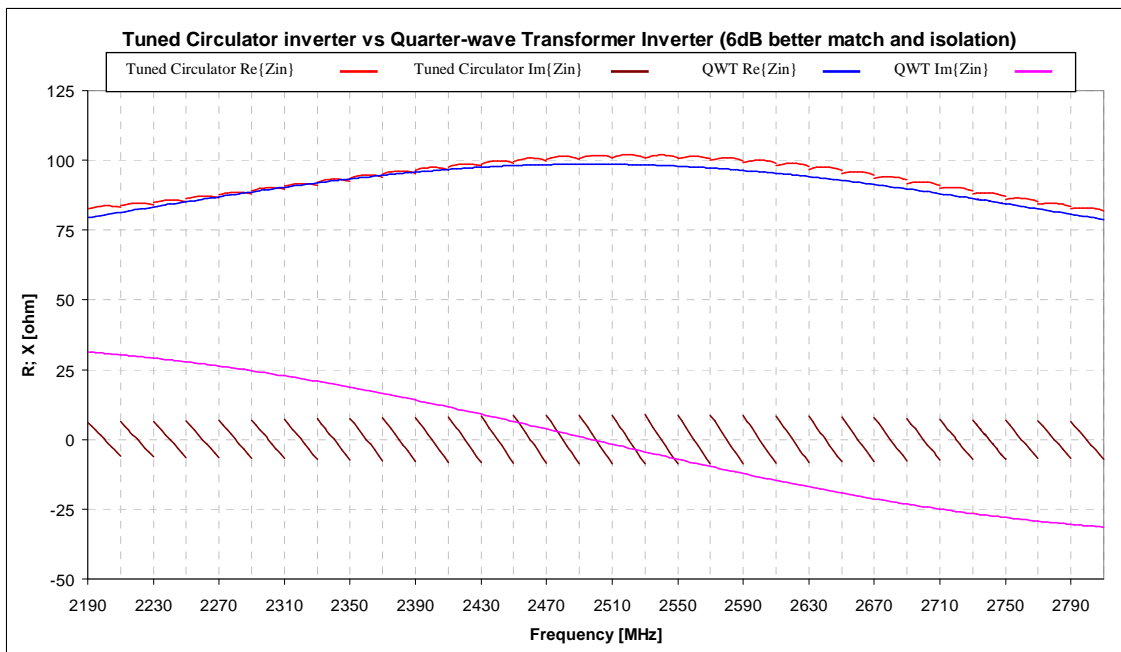
**Figure 37: Calculated frequency response of the circulator-based inverter tuned to 2500MHz, compared to that of the quarter-wave transformer (QWT) inverter**



**Figure 38: Calculated frequency response of the circulator-based inverter tuned to 2700MHz, compared to that of the quarter-wave transformer (QWT) inverter**



**Figure 39: Circulator-based inverter tuned over the entire band with its impedance inverting performance displayed over 20MHz wide channels**



**Figure 40: Calculated circulator-based inverter with 6dB enhanced Return Loss and Isolation tuned over the entire band with its impedance inverting performance displayed over 20MHz wide channels**

By comparing the performance of the circulator-based inverter in Figure 39 (original S-parameters of the circulator) and the performance of the inverter with enhanced matching and isolation in Figure 40, we can see that return loss and isolation parameters play a significant role in the performance of the circulator-based impedance inverter which was expected based on the analysis done in section 3.5.2.

### **3.4 Conclusions**

Three novel concepts have been introduced in this chapter.

The first is the concept of a transcoupler, which combines the performance of an impedance inverter and a coupler.

The second concept uses two of these transcouplers to couple out (that is, to sample) the amplified signals at two points on the output side of the main and peak amplifiers of a Doherty amplifier. A circuit analysis then showed how these sampled complex voltages can be used to determine the actual complex peak-amplifier and main-amplifier currents at the combining node. It was shown how these separate feedback signals can be used to individually pre-distort the signals entering the main-amplifier and peak-amplifier devices of a so-called “digital Doherty” amplifier, according to the individual profiles of the active devices used in the main- and peak-amplifiers. It was demonstrated why transcouplers are necessary, namely that use of a conventional impedance inverter in cascade with a coupler does not satisfy the proper requirements. It was also shown how such transcouplers can be used to improve the performance of a Chireix amplifier architecture as well.

The third concept was a method of using circulators to create tunable impedance inverters. Although the instantaneous bandwidth of the Doherty amplifier that uses such inverters is not extended, it represents the first time an approach has been devised to realise tunable power amplifiers in this way.

In the course of the thesis research the above-mentioned contributions spawned insights that have been used to develop the superior techniques described theoretically, and validated experimentally, in the chapters that follow. Thus, although the ideas of this chapter are valid in their own right, they have not been pursued any further.

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([http://www.e-meca.com/specs\\_iso\\_cir/specs\\_iso\\_cir.php?ID=128&SpecsID=4](http://www.e-meca.com/specs_iso_cir/specs_iso_cir.php?ID=128&SpecsID=4))

## Chapter 4

# 4 Compact Implementation of Existing Doherty Architectures

### 4.1 Introduction

This chapter is dedicated to compact implementation of main and peak matching networks in N-way Doherty amplifiers.

In the standard two-way Doherty amplifier the output section of the main branch consists of three distinct parts: a matching network, an offset line, and a quarter-wave impedance inverter. Similarly, the output section of the peak branch consists of a cascade of a matching network and an offset line. Each of the constituent parts of the cascaded sections has to provide a particular functionality. In this chapter we will present techniques to combine all the functionalities of the above-mentioned constituent parts of the output section of the main branch (and similarly for the output section of the peak branch) into a single network that performs all the necessary impedance transformations needed to convert the combining-node side impedances into appropriate device side impedances. The benefits of these compact implementations include increased bandwidth, a lower insertion loss, and a smaller circuit footprint. These compact designs also facilitate the expansion of the two-way Doherty architecture into N-way architectures in a systematic fashion.

Section 4.2 introduces the two-way compact Doherty amplifier architecture. The main matching network of the compact two-way Doherty amplifier does not rely on the explicit use of quarter-wave transformer and an offset line combination to provide impedance transformations necessary for proper operation of the main device. Similarly the peak matching network of this architecture does not rely on explicit use of an offset line to provide impedance transformations necessary for proper operation of the peak device. The absence of the quarter-wave transformer and offset lines makes main and peak device output matching networks physically smaller with added benefit of lower

loss and increased bandwidth. The compact two-way Doherty amplifier circuit was built as a proof of concept and its simulated and measured performance is presented.

Section 4.3 presents the expansion of the compact two-way Doherty amplifier into a compact three-way Doherty amplifier by means of replacing its main amplifier by another compact two-way Doherty amplifier. The comparison is made between the layouts of the compact implementation and the conventional implementation using quarter-wave transformers and offset lines.

Section 4.4 describes the expansion of the compact two-way Doherty amplifier into a compact three-way Doherty amplifier by means of replacing its peak amplifier by another compact two-way Doherty amplifier. The comparison is made between the layouts of the compact implementation and the conventional implementation using quarter-wave transformers and offset lines. Using this method of expansion the three-way amplifier circuit was constructed as a proof of concept and its simulated and measured performance is presented.

Two particular ways of suboptimal expansion of (N-1)-way Doherty amplifiers into N-way Doherty amplifiers are examined in Section 4.5 along with the reasons that make them suboptimal.

Section 4.6 provides description of the optimal expansion of (N-1)-way Doherty amplifiers into N-way Doherty amplifiers along with the explanation what makes it optimal.

Finally, Section 4.7 concludes the chapter.

Throughout the chapter we will refer to, and show diagrams of, what we have called "generic microstrip implementations" of the various amplifier configurations. These are used simply to illustrate the differences between compact and conventional implementations of the output sections of the branches. Such generic layouts do not precisely represent the details of any specific physical circuits, albeit close representations of what the final physical layouts would be. However, in this chapter we also show the measured performance of compact two-way and three-way Doherty amplifiers. Obviously, these do not merely utilise generic microstrip layouts but carefully

designed ones. The compact two-way and three-way Doherty amplifier designs whose simulated and measured performances are presented in Section 4.2 and Section 4.4 were designed using the new Doherty amplifier synthesis and analysis methods that will be the subject of Chapter 5 and Chapter 6. The physical circuit simulations and optimizations used were done using the calculations that form part of these design methods, and *Microwave Office Software* of Applied Wave Research (AWR).

## **4.2 Two-Way Compact Doherty Amplifier**

Figure 41 shows the block diagram of the compact two-way Doherty being proposed here. As in the conventional ("non-compact") two-way Doherty amplifier described in Section 2.3, the main amplifier branch consists of a cascade of a main input matching network, a main amplifier device, and a main output matching network, while the peak amplifier branch consists of a cascade of a peak input matching network, a peak amplifier device, and a peak output matching network. Output signals from the main and peak amplifier branches are combined at the node where main and peak branches meet, and the resulting combined signal is delivered to the load through a wideband node matching network.

However, in this compact Doherty amplifier, the main output matching network is specifically designed to simultaneously perform the impedance transformation function of the main output matching network, the function of main offset line, and the impedance inversion function of quarter-wave transformer of the conventional Doherty amplifier. In other words the functionality of the quarter-wave impedance inverter and the main offset line are subsumed into a single network element. Similarly, the functionality of the peak offset line of the conventional Doherty amplifier is subsumed into the design of the peak output matching network in this compact Doherty amplifier.

Since the main branch of the compact Doherty amplifier does not explicitly include a quarter-wave transformer and an offset line, the main output matching network can be designed to have a broader bandwidth compared to that in a conventional Doherty main branch cascade. Also, the output quarter-wave transformer of the conventional

Doherty amplifier can be replaced by a broadband node matching network, thus increasing the overall bandwidth of the Doherty amplifier.

Figure 42 shows a schematic diagram of a generic microstrip layout of one possible implementation of the compact two-way Doherty amplifier. As an example of the "compacting" process we consider the example shown in Figure 43. It illustrates how the existing main branch output matching network is replaced by a compact version.

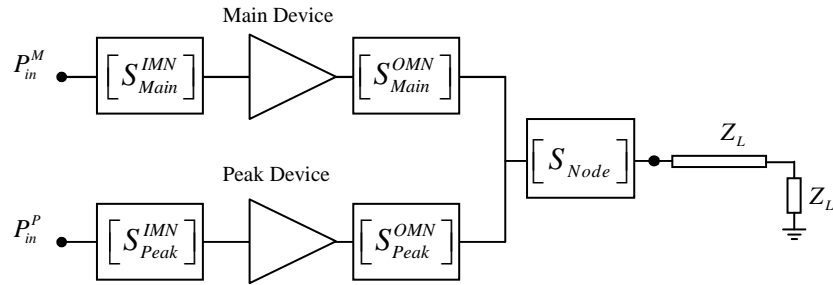


Figure 41: Compact two-way Doherty amplifier

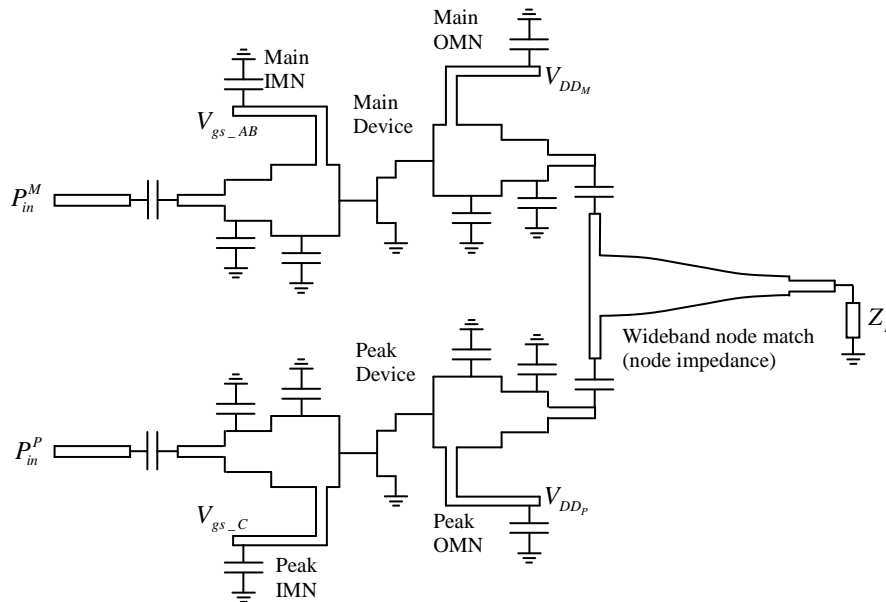
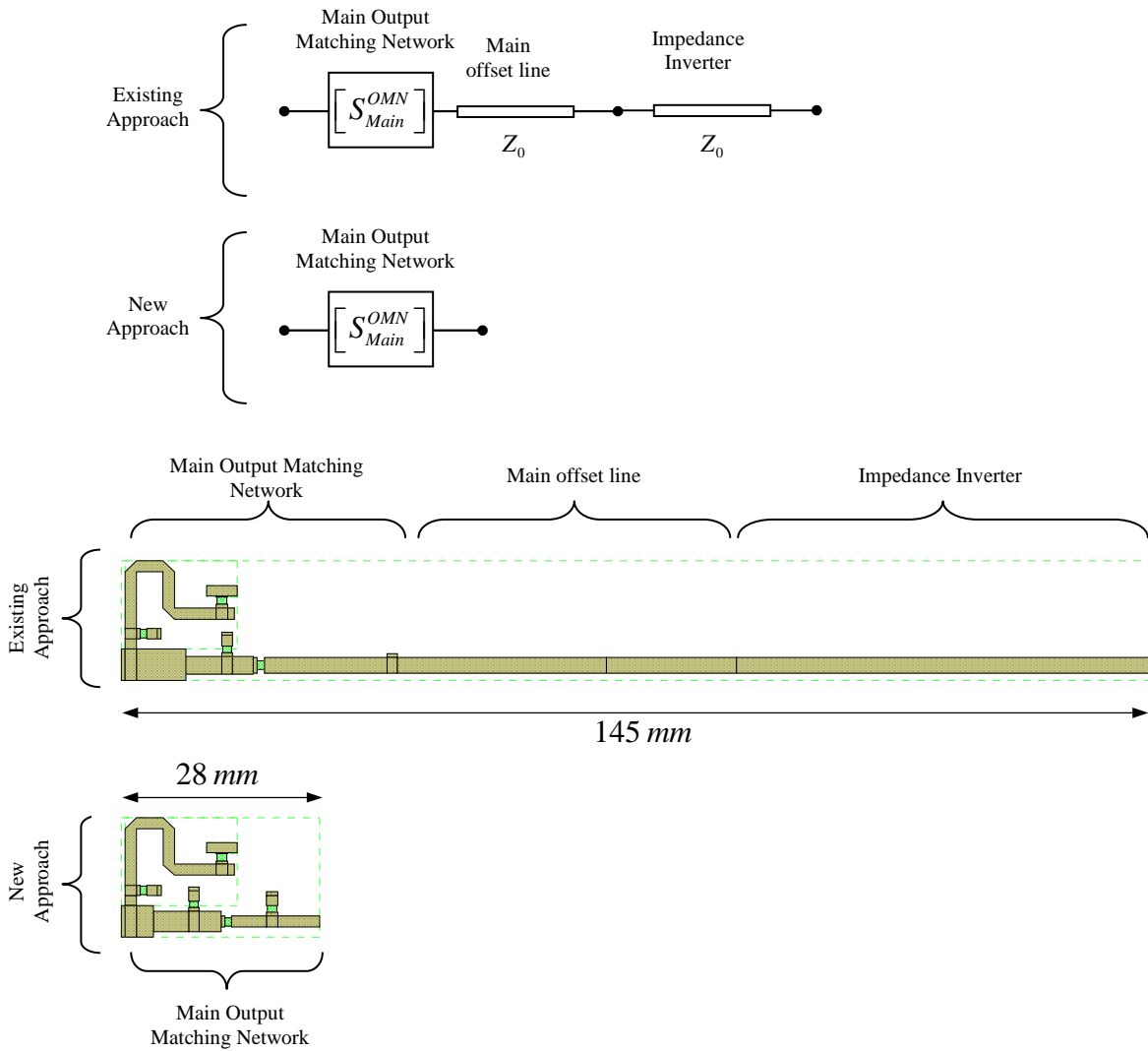


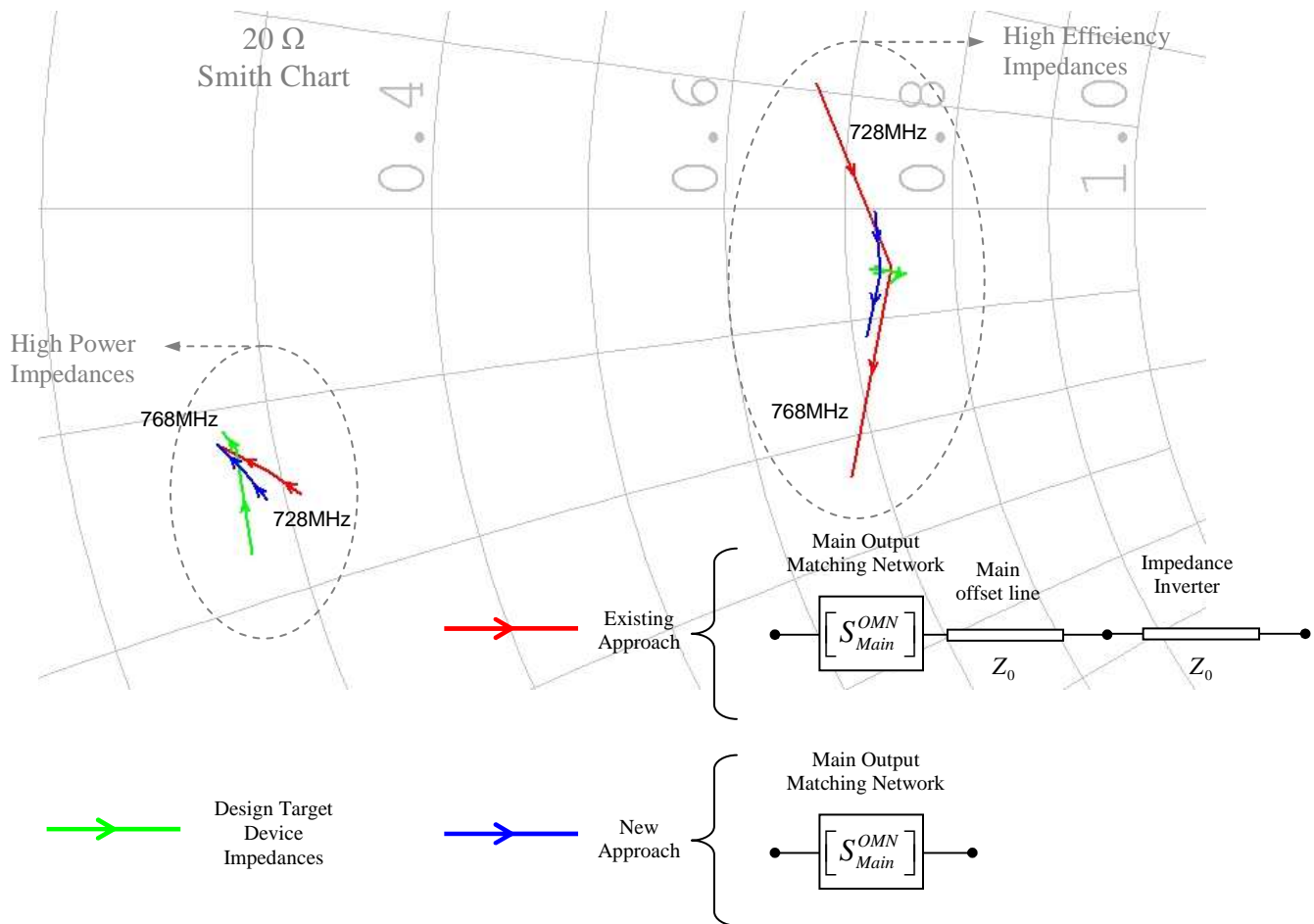
Figure 42: Generic microstrip implementation of compact two-way Doherty amplifier



**Figure 43: Main branch design with an implicit and explicit use of impedance inversion. The lower two diagrams are an actual layout for a design frequency of 748MHz. By implicit use of impedance inversion we mean the compact approach**

The new approach produces the shortest possible transmission line length given the target impedances, and available component and layout restrictions. If the existing approach already provides the shortest solution the new approach will automatically give the same solution as the existing approach. In other words, the new approach is a more general design approach than the existing approach; the existing approach solution set will be a subset of the solution set of the new approach.

Because of the shorter transmission line lengths above, the new approach will yield designs that have lower insertion loss and wider bandwidth<sup>23</sup>. For the main matching network implementations shown in Figure 43, the calculated insertion loss was 0.03dB for the compact approach versus 0.06dB for the existing approach. For the same reasons the compact main output matching network also has a smaller footprint on the printed circuit board (PCB). It is 28mm for the new design approach versus 145mm for the existing design approach as illustrated in Figure 43. The main branch impedance behaviour of the same circuit in Figure 43 over frequency is shown in Figure 44.



**Figure 44: Computed performance comparison between the implicit and explicit impedance inversion implementations**

<sup>23</sup> The lower insertion loss and wider bandwidth are the main features of the new compact approach, the reduction in PCB footprint is beneficial but not the main motivation for introducing compact approach

The new design approach produces a solution that has a lower impedance spread over frequency (given the target impedances, available component and layout restrictions) compared to the existing design approach. This is especially noticeable for the impedances in the “high efficiency impedance” region where the existing design solution significantly deviates from the target impedances. Because of the lower impedance spread over frequency, the new approach solution is considered more wideband than the solution provided by the existing design approach.

Depending on the particular implementation, the compact two-way Doherty amplifier is able to provide one or more of the following advantages over its conventional counterpart:

- Reduced insertion loss and hence less waste heat generated;
- Lower impedance spread over frequency, and hence wider frequency bandwidth of operation;
- Smaller amplifier footprint and hence smaller PCB layout and cost;
- Higher factory yield; and
- Easier fabrication and tuning.

The design of the main and peak output matching networks may be optimized for maximal frequency bandwidth, minimal insertion loss, as well as minimal occupied real-estate by reducing the overall size (length) of the network for each branch.

The main matching network optimization is performed to satisfy two conditions simultaneously. The first condition is to transform the combining node impedance (lightly loaded by the off-state impedance of the peak branch) to an impedance associated with a high-efficiency performance of the main amplifier device, and the second condition is to transform the modulated combining node impedance (this impedance will be higher compared to the previous case due to power contribution from the peak branch) to an impedance associated with a high-power performance of the main amplifier device.

The peak matching network optimization is also performed to satisfy two conditions simultaneously. The first condition is to transform the off-state impedance of the peak device to a high impedance to avoid excessive loading of the combining node, and the second condition is to transform the modulated combining node impedance (this

impedance will be modulated due to power contribution from the main branch) to an impedance associated with a high-power performance the peak device.

The implementation of a compact network, such as the main output matching network of the compact Doherty amplifier, that combines the functionality of a matching network, an offset line, and an impedance inverter into one network element, can be done with the aid of an optimizer for the best results to be achieved (most compact, most broadband, etc.). The process involves determining the proper impedance values for low-power conditions (high efficiency) and high-power conditions (high power) based on the power amplifier specifications and the transistor characteristics over frequency. The selection is such that the desired performance can be achieved under the specified conditions, and is subject to tradeoffs between conflicting performance parameters.

A two-way Doherty amplifier was designed using the compact matching network configuration of Figure 41. The design target for the modulated signal output power was  $49.5\text{dBm}$  and for the peak power (saturation power)  $56\text{dBm}$ . The design was based on the load-pull measurements of one active device under two biasing conditions: class AB for the main device functionality and class-C for the peak device functionality<sup>24</sup>. Figure 46 shows the simulated<sup>25</sup> and initial measured results for the two-way compact Doherty amplifier without any modifications compared to the circuit used in simulation (no bench tuning). The deviation of the measured performance from the simulated performance in Figure 46 indicated that there was an issue with the implementation of the peak input matching network. The implementation of the peak input matching network was found to be different from the condition under which the peak device was load-pulled. One of the capacitors in the peak input matching network was identified as a cause of the deviation and was replaced by another capacitor of proper value, no changes to microstrip copper traces were made. Figure 47 compares the simulated and measured results for the two-way compact Doherty amplifier with the peak input matching network restored to its

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<sup>24</sup> As mentioned earlier, the new design methods developed in this thesis, which are described in detail in Chapters 5 and 6, were used for the amplifiers whose measured performance is shown in the present chapter.

<sup>25</sup> The simulation was performed using analysis techniques based on active device load-pull data developed in Chapter 6

intended functionality. The change in the peak device input matching network resulted in realignment of measured gain performance under pulsed CW and modulated signal conditions with simulated gain and efficiency performance (Figure 47). Thus the new idea of a compact two-way Doherty has been experimentally validated. Aside from the smaller PCB footprint of the compact design the removal of the quarter-wave transformer and the offset line in the main output matching network, whose combined length at the frequency of operation ( $2655\text{MHz}$ ) is approximately  $2.5\text{cm}$ , resulted in the loss reduction of approximately  $0.1\text{dB}$  for the RO43050B  $30\text{mil}$  thick RF substrate [48] we used in the design that has microstrip insertion loss of  $0.1\text{dB}/\text{inch}$ . The compact design approach, in this particular case, allowed us to implement the main and peak matching networks using only microstrip transmission line sections, no shunt lumped components (capacitors) were used. This reduces cost, improves the reliability, and lowers the variation in performance due to variability of components used which in turn should improve the fabrication yield.

The agreement between the measured and the simulated gain in the pulsed RF regime of operation (Figure 47) is very good; the simulated gain is higher because we used lossless matching networks to obtain simulated results. The pulsed RF gain variation over frequency is less than  $1.5\text{dB}$  (the specification called for gain variation over frequency of less than  $3\text{dB}$ ) and it translated to the modulated signal regime gain variation over frequency of  $1\text{dB}$ . The measured modulated signal regime drain efficiency of  $53\%$  was slightly better than targeted value of  $50\%$  which was achieved in the simulation<sup>26</sup>.

The pulsed CW signal used to obtain the gain versus output power had a period of  $100\mu\text{s}$  and a duty-cycle of  $10\%$ . The modulated signal used for testing was an LTE signal with bandwidth of  $10\text{MHz}$  and a peak-to-average power ratio of  $6.5\text{dB}$ .

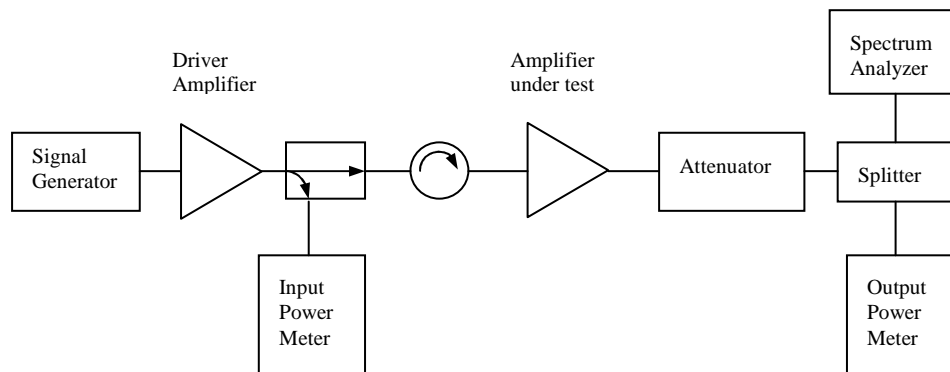
The signal from the signal generator [49] was passed through a driver amplifier and then fed to the compact Doherty amplifier under test. The input and output power were

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<sup>26</sup> The difference in simulated and measured gain is due to simulation being done using lossless passive networks and due to device to device variation in gain. The difference in measured and simulated efficiency stems from device to device differences in performance. Device efficiency can vary up to  $5\%$  from device to device.

measured using channels A and B of the power meter [50], respectively, the difference was recorded as the gain of the amplifier and the reading from channel B as the output power of the amplifier under test. The spectrum analyzer [51] was used to observe the spectral characteristics of the output signal. The block diagram of the setup is shown in Figure 45.

The spectrum of the LTE signal with bandwidth of  $10\text{MHz}$  and a peak-to-average power ratio of  $6.5\text{dB}$  after it has passed through the amplifier is given in Figure 48. The adjacent channels "ACP Up" and "ACP Low" are centered at  $11\text{MHz}$  offsets with respect to the center frequency of the signal ( $2655\text{MHz}$ ) and are  $10\text{MHz}$  wide. Alternate channels "ALT1 Up"/"ALT1 Low" and "ALT2 Up"/"ALT2 Low" are centered at  $22\text{MHz}$  and  $33\text{MHz}$  offsets respectively and are also  $10\text{MHz}$  wide. Adjacent channel powers relative to the carrier channel are  $-22.69\text{dBc}$  and  $-24.62\text{dBc}$  for the upper and lower adjacent channels respectively. This amount of uncorrected distortion is not acceptable according to regulatory standards, and predistortion techniques need to be used to make the amplifier performance adequate from the spurious emissions point of view. This is always done in practice, as was mentioned in section 2.5 so we will next do this here.



**Figure 45 Amplifier measurement setup**

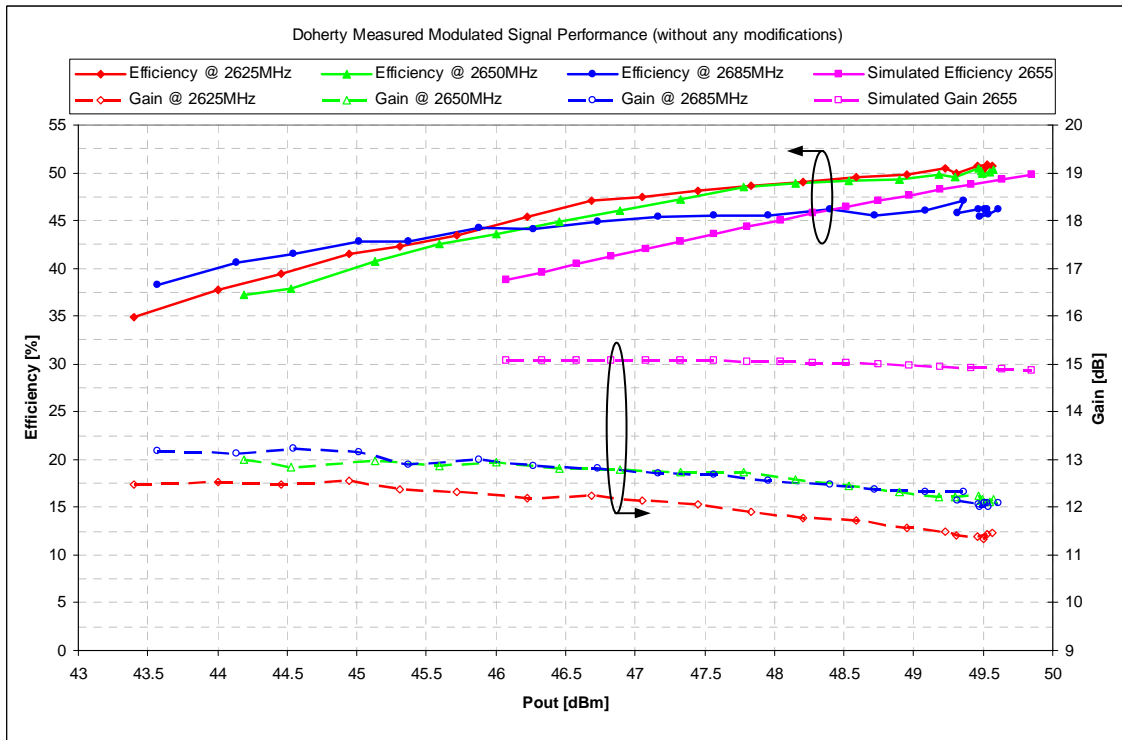
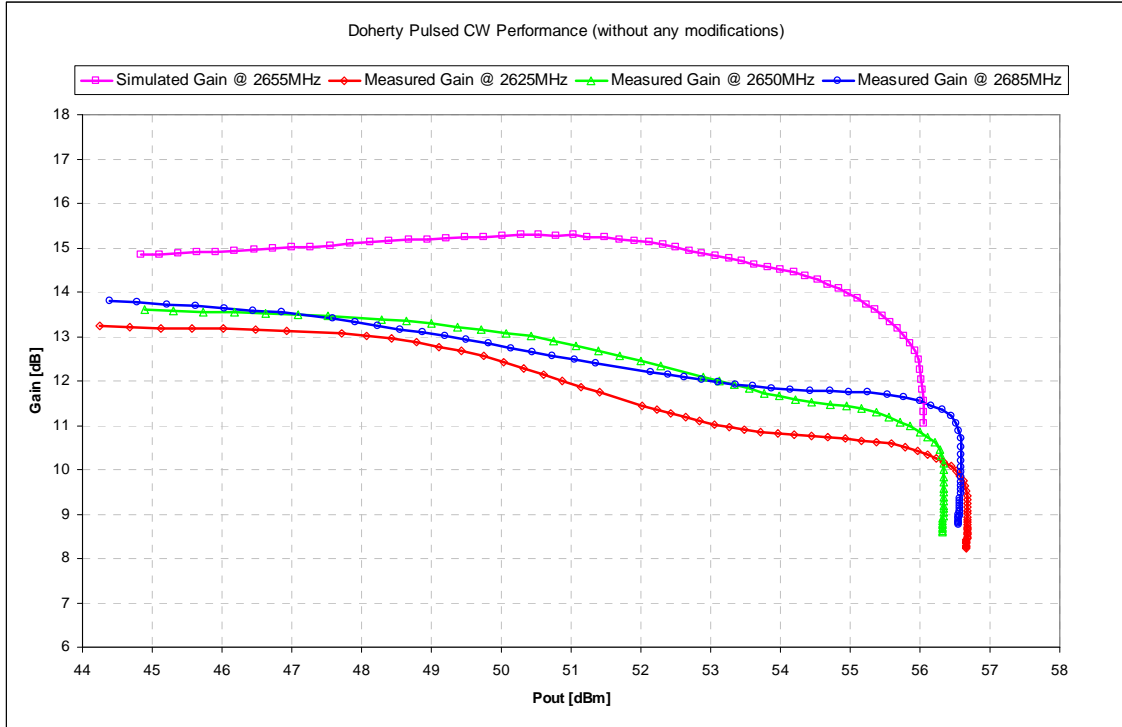
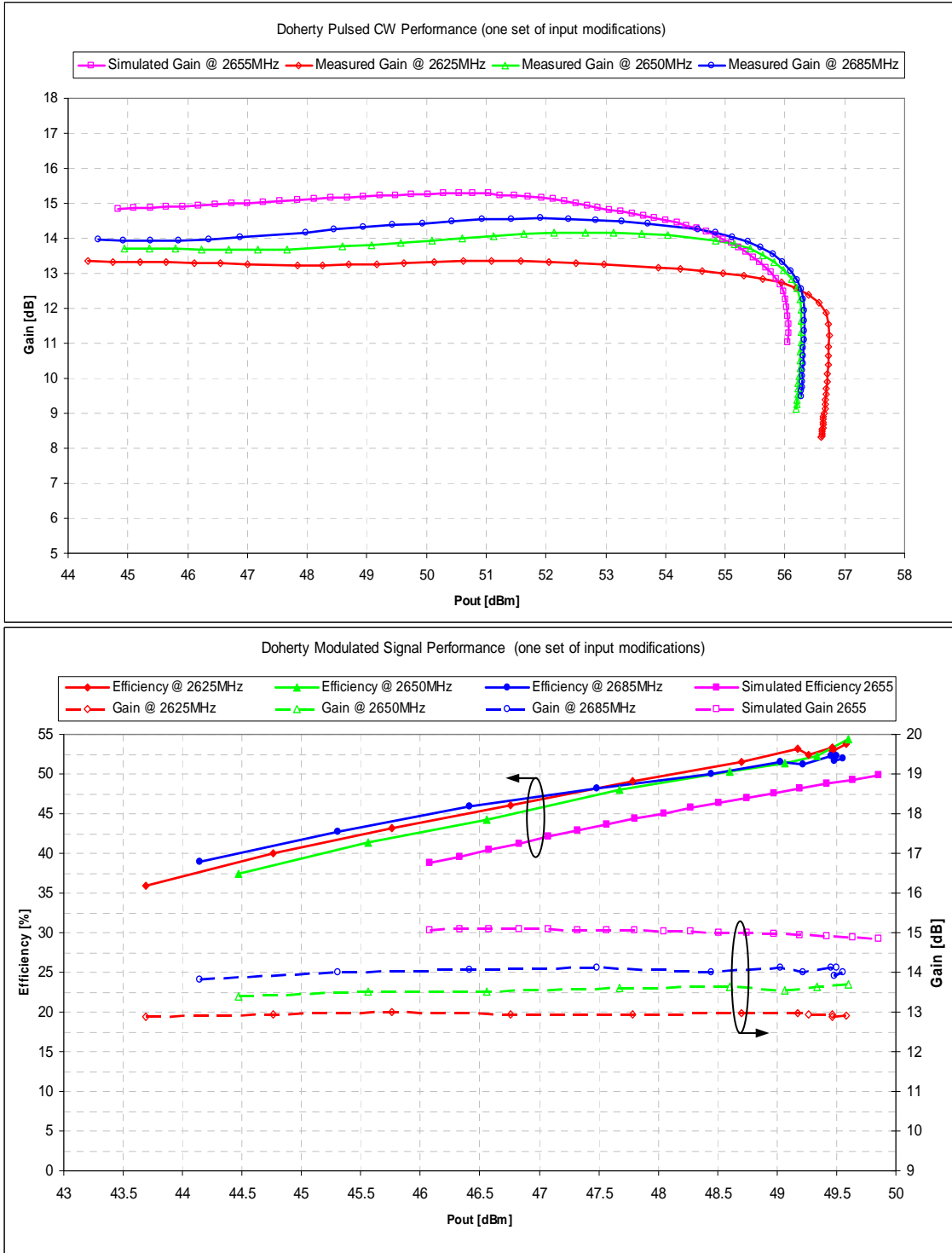
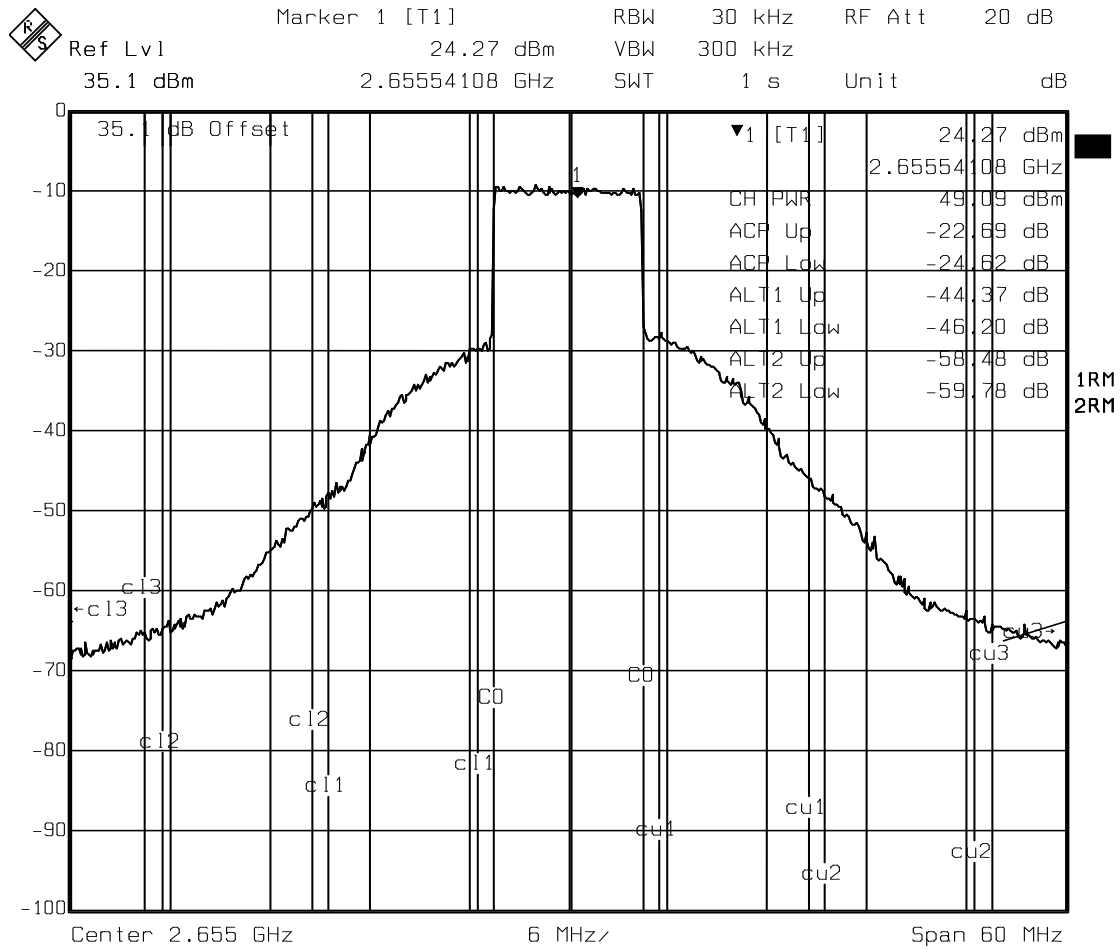


Figure 46: Simulated and measured gain and drain efficiency for a two-way compact Doherty amplifier. No bench tuning or other modifications were performed on the measured amplifier.

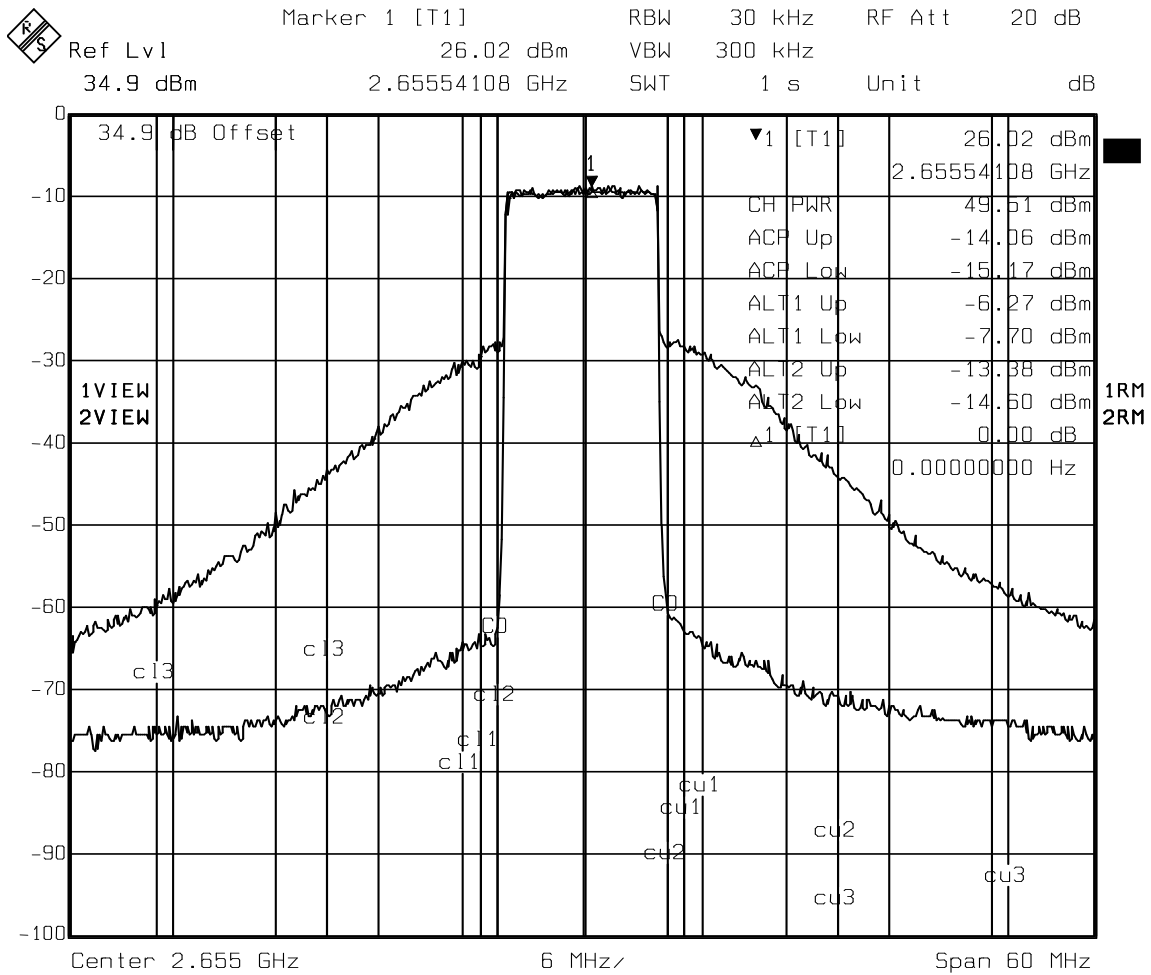


**Figure 47: Comparison of simulated and measured gain and efficiency of a two-way compact Doherty amplifier with the peak device input matching network of the fabricated amplifier tuned to improve gain linearity**



**Figure 48: Uncorrected output spectrum of the two-way compact Doherty amplifier**

The output spectrum when the input signal is predistorted is shown in Figure 49 (with the original spectrum retained for comparison purposes). The adjacent channels "ACP Up" and "ACP Low" are offset by 6.5MHz from the center frequency and 1MHz wide with absolute power of -14.06dBm and -15.17dBm for the upper and lower adjacent channels, respectively. Alternate channels "ALT1 Up"/"ALT1 Low" and "ALT2 Up"/"ALT2 Low" are offset by 10MHz and 20MHz from the center frequency and 10MHz wide. The level of the spurious emissions close to the edge of the carrier channel is reduced by more than 30dB indicating that the amplifier spectral performance can be sufficiently improved by means of the input signal predistortion to meet the regulatory requirements.



**Figure 49: Corrected output spectrum of the two-way compact Doherty amplifier by means of digital predistortion**

With the output power of 89.1W and with predistortion applied to obtain the output spectrum shown in Figure 49, a drain efficiency of 53.2% was obtained for the amplifier, which is slightly better than 50% predicted by the simulation.

### 4.3 Compact Three-Way Doherty Amplifier: Main Amplifier Replaced by another Two-Way Doherty Amplifier

A three-way Doherty architecture can be derived from a two-way Doherty architecture [53], [54], [55], by replacing the main branch of the original two-way Doherty amplifier by another two-way Doherty amplifier<sup>27</sup>. The resulting three-way Doherty design block diagram is shown in Figure 50 for the conventional design.

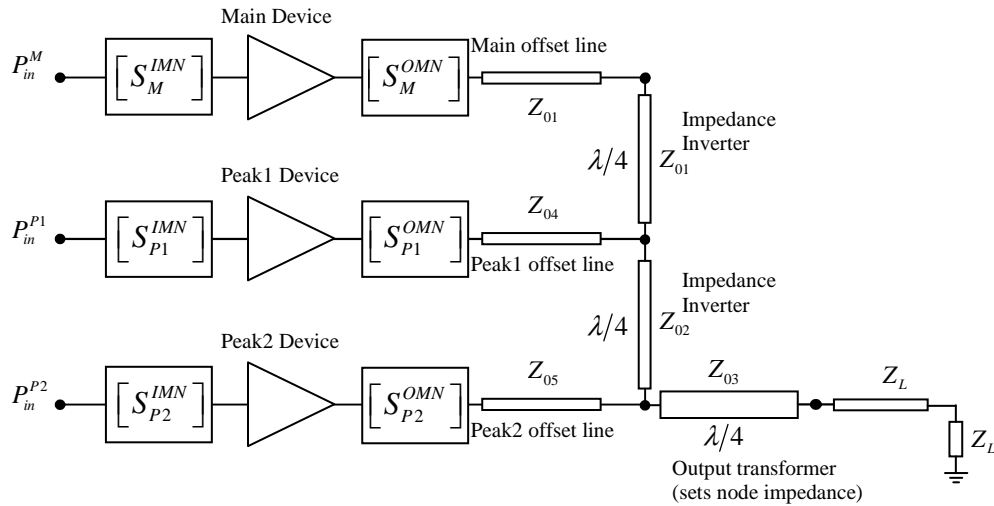
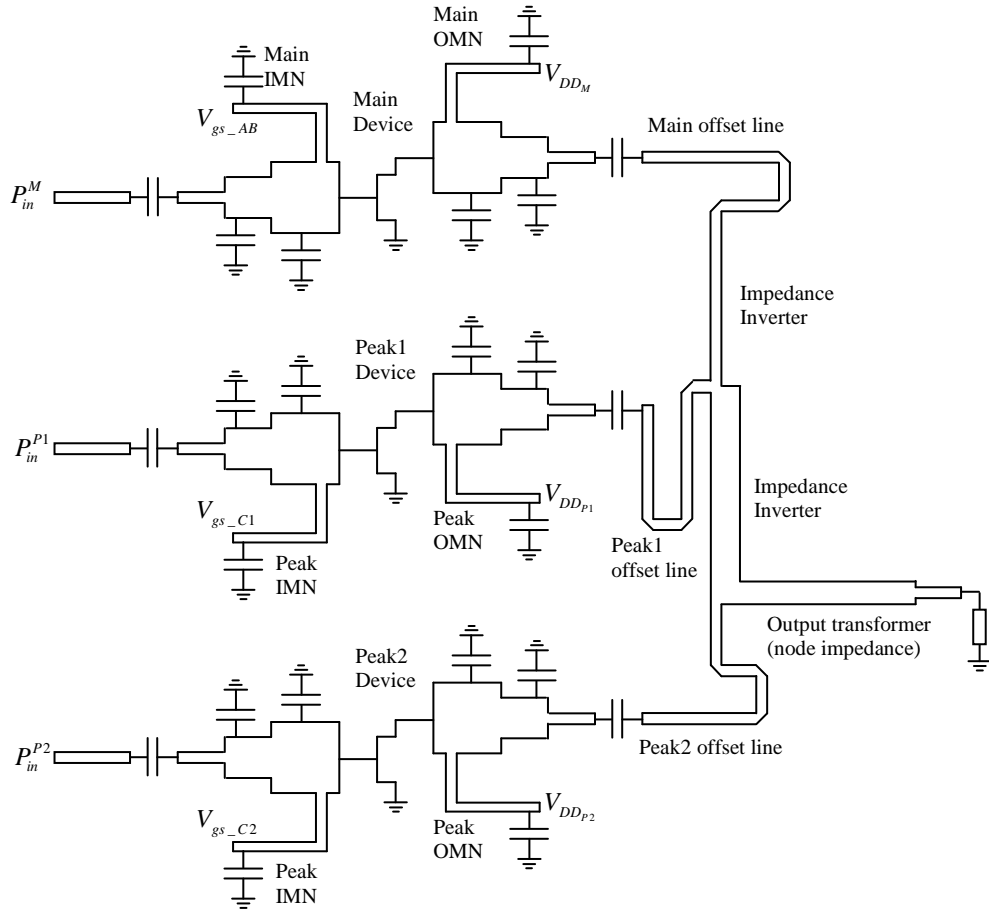


Figure 50: Block diagram of a conventional three-way Doherty amplifier

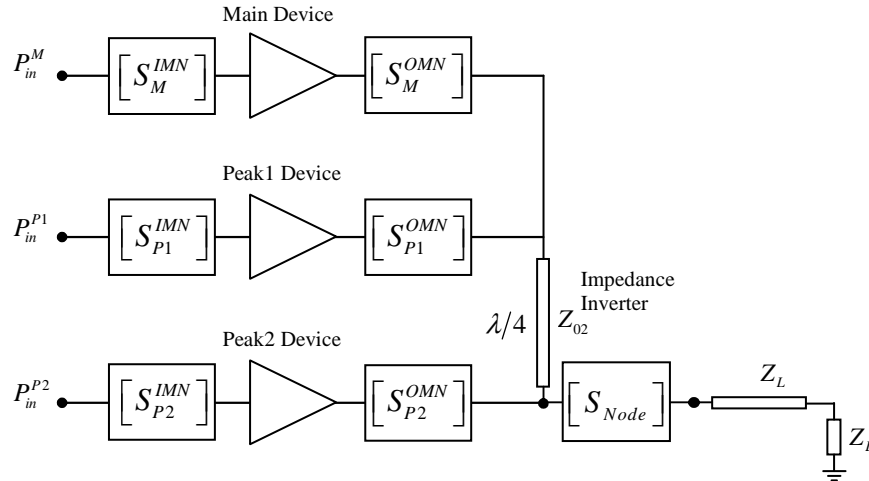
Compared to the original two-way Doherty design, the layout of the derived three-way design is more demanding of PCB real estate. A possible generic microstrip implementation of this conventional three-way Doherty configuration is shown in Figure 51.

<sup>27</sup> Another possible three-way configuration, where it is the peak amplifier that is replaced by another two-way Doherty amplifier, is discussed in section 4.4. Experimental results will be shown for that case. The reason for selecting that particular case will be clear from the analysis in sections 4.5 and 4.6.

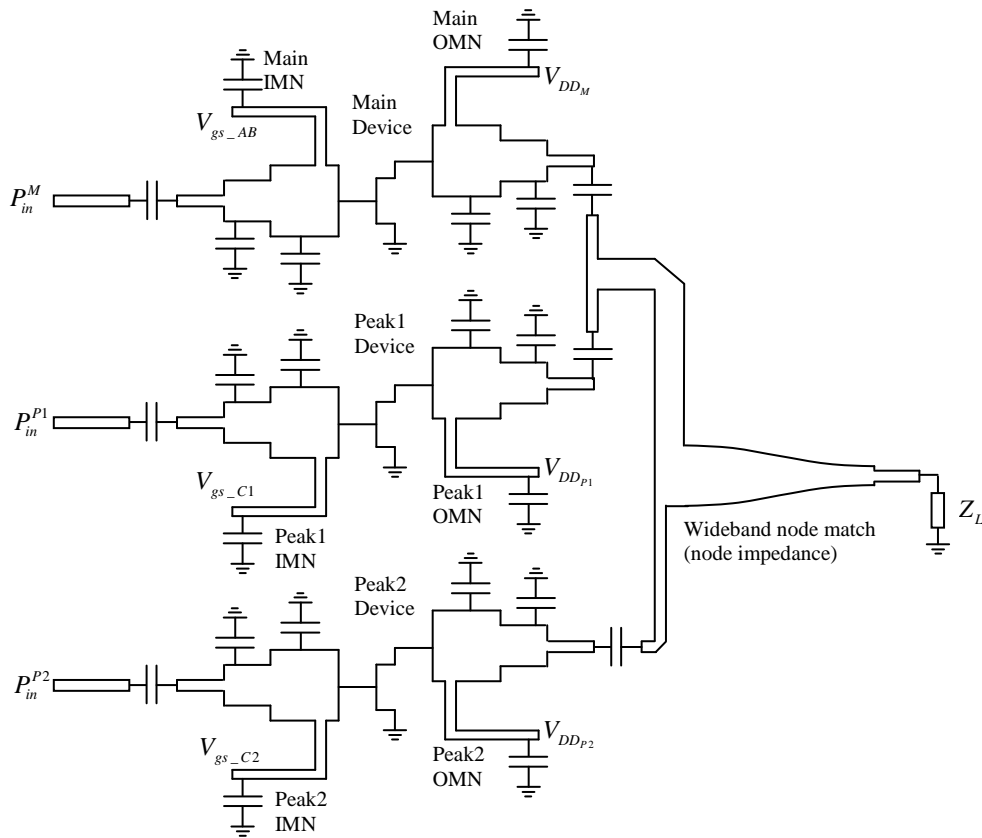


**Figure 51: Generic microstrip implementation of a possible three-way Doherty amplifier derived from a two-way Doherty by replacing its main branch by another two-way Doherty amplifier**

As it can be seen from the generic layout depiction of the three-way Doherty amplifier in Figure 51 the explicit inclusion of the quarter-wave transformers and offset lines makes the layout quite involved, and the designers are forced to meander the lines in order to fit everything in usually limited footprint available on the PCB. To avoid this cramped design, a compact implementation of this three-way Doherty configuration is proposed as represented by the block diagram in Figure 52. Same as for the compact two-way case in Section 4.2, the functionality of the quarter-wave transformers and offset lines is subsumed into their respective matching network blocks. A generic microstrip implementation of this compact three-way Doherty is shown in Figure 53. While maintaining the impedance transformation goals for the design of the output combining network, this configuration indeed gives a much more compact microstrip layout.



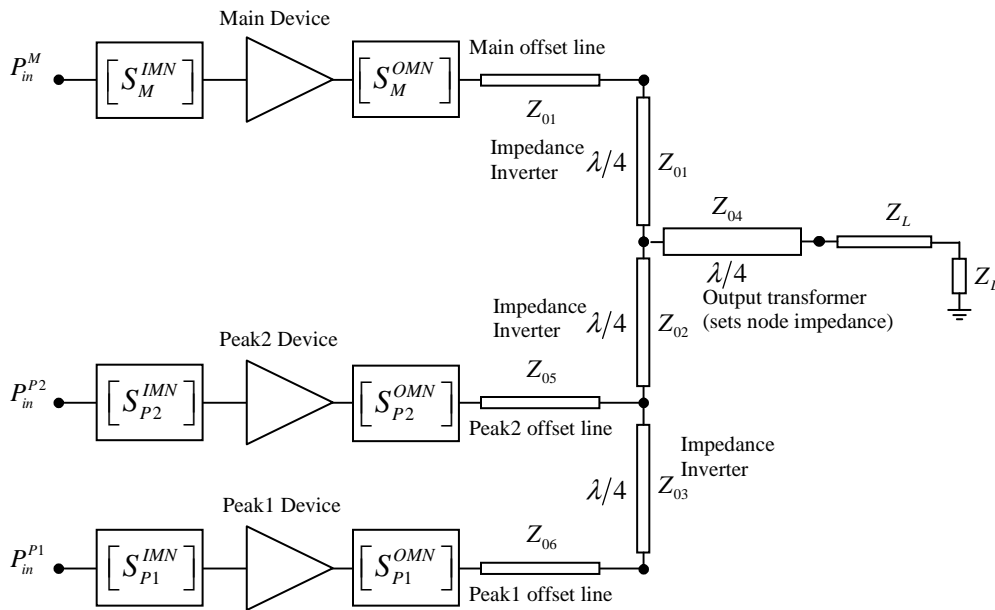
**Figure 52: Block diagram of a new compact three-way Doherty design derived from a two-way Doherty by replacing its main branch by another two-way Doherty amplifier**



**Figure 53: Generic microstrip implementation of a new compact three-way Doherty amplifier derived from a two-way Doherty amplifier by replacing its main amplifier by another two-way Doherty amplifier**

#### 4.4 Compact Three-Way Doherty Amplifier: Peak Amplifier Replaced by another Two-Way Doherty Amplifier

Another way to produce a three-way Doherty architecture from a two-way Doherty one is to replace the peak branch of the original two-way Doherty amplifier by another two-way Doherty amplifier [56], [57]. The resulting three-way Doherty design block diagram is shown in Figure 54 for the conventional case. Note how peak branches 1 and 2 are swapped to make alignment of the devices along their vertical axes possible.



**Figure 54: Block diagram of a conventional three-way Doherty design, derived from a two-way Doherty by replacing its peak amplifier by another two-way Doherty**

Compared to the original two-way Doherty design, and the first variant of a three-way Doherty amplifier described in Section 4.3, the layout of this second variant of the three-way design in Figure 54 is even more demanding as far as PCB real estate space since we have an additional quarter-wave transformer to contend with. A possible generic microstrip implementation of this three-way Doherty is shown in Figure 55.

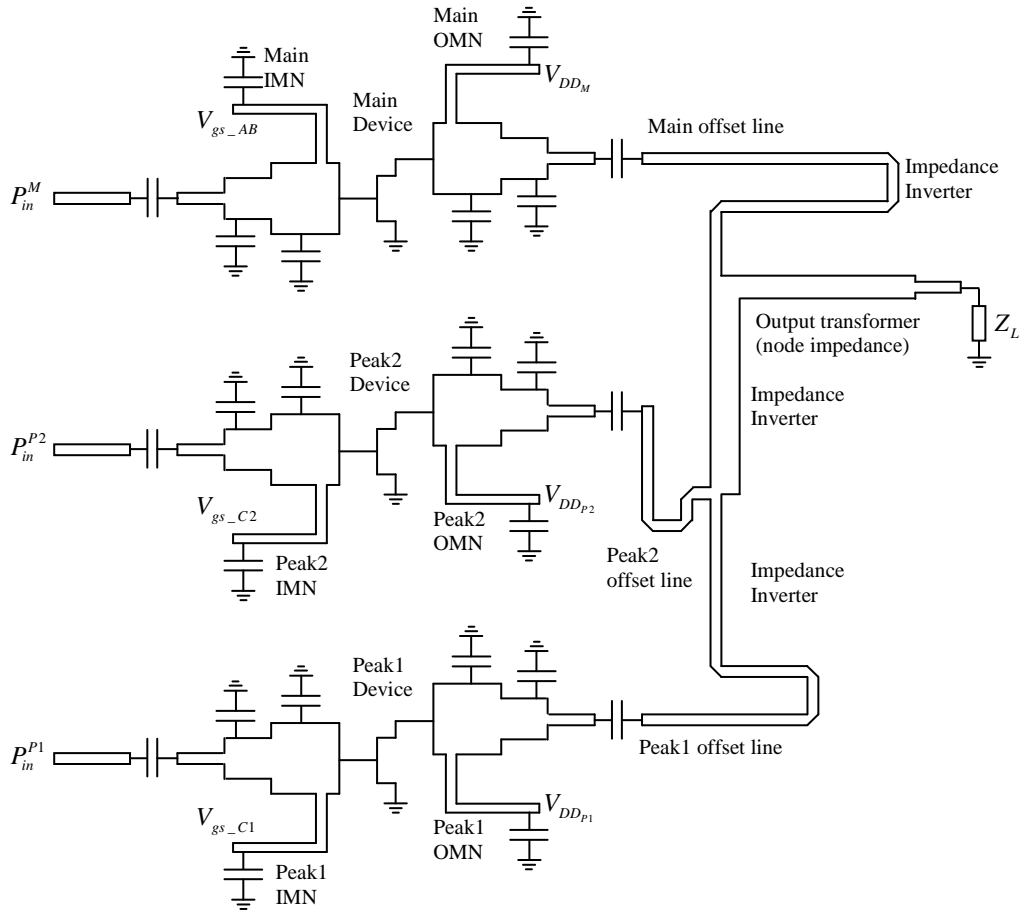
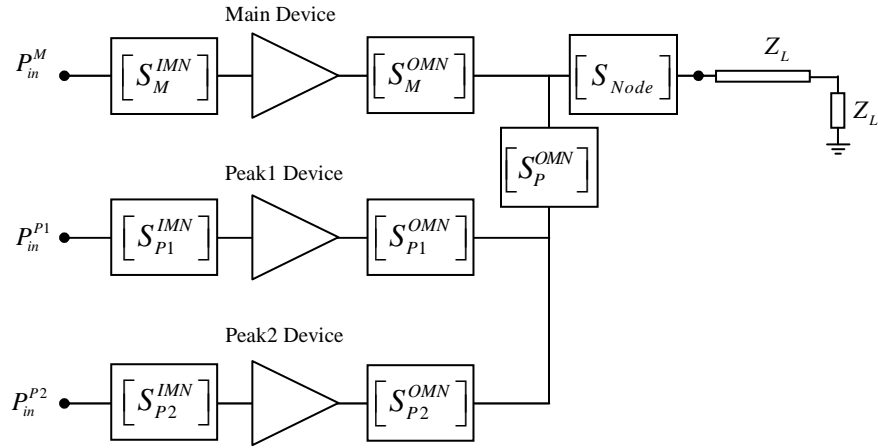
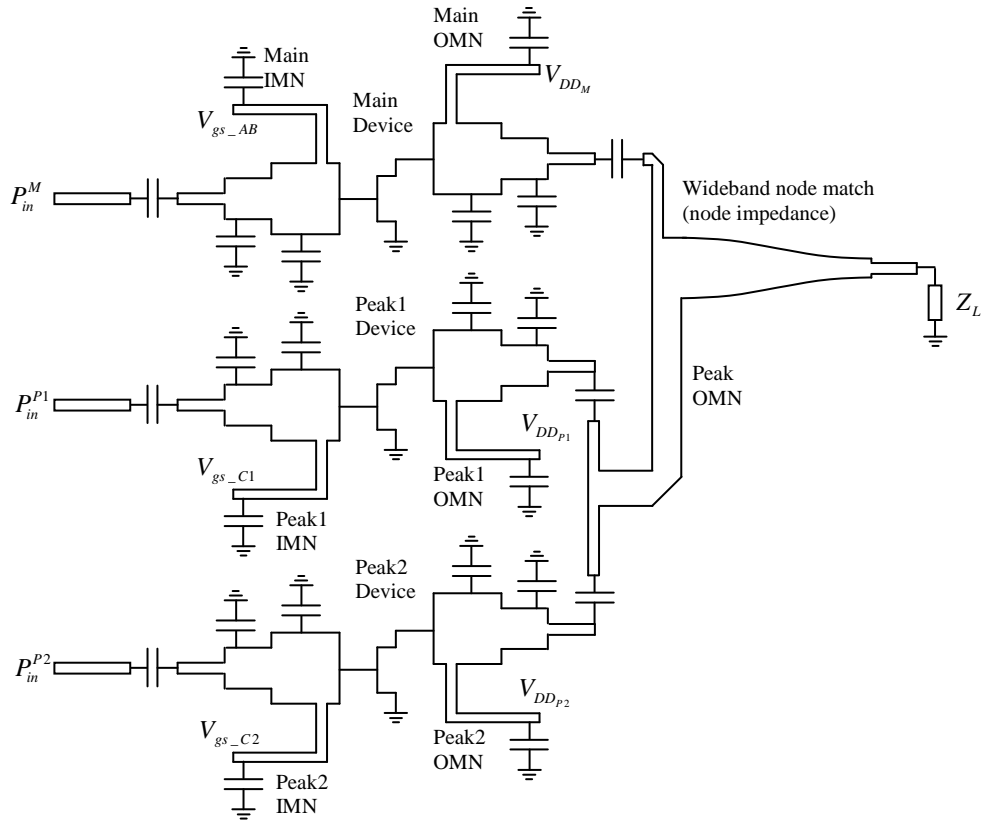


Figure 55: Generic microstrip implementation of an existing three-way Doherty amplifier derived from a two-way Doherty by replacing its peak amplifier by another two-way Doherty



**Figure 56: Block diagram of a new compact three-way Doherty design derived from a two-way Doherty by replacing its peak amplifier by another two-way Doherty**



**Figure 57: Generic microstrip implementation of a new compact three-way Doherty derived from a two-way Doherty by replacing its peak amplifier by another two-way Doherty**

As can be seen, the explicit inclusion of the quarter-wave transformers and offset lines makes the layout quite involved, even when compared to the first three-way variant discussed in Section 4.3, due to the additional quarter-wave transformer in the peak combining network. Once again designers are forced to meander the lines in order to fit everything in the limited footprint available on the PCB. Thus we propose the compact version of this three-way Doherty configuration in the form of the block diagram shown in Figure 56. We note that:

- The functionality and structure of the cascade of main output matching network, main offset line, and the main quarter-wave impedance inverter of Figure 54 are subsumed into main output matching network of Figure 56.
- The functionality and structure of the cascade of the second peak output matching network and the second peak offset line of Figure 54 are subsumed into the second peak output matching network of Figure 56.
- The functionality and structure of the cascade of the first peak output matching network, the first peak offset line as well as the first peak quarter-wave impedance inverter of Figure 54 are subsumed into the first peak output matching network of Figure 56.
- The peak quarter-wave impedance inverter of Figure 54 is replaced by the common peak output matching network of Figure 56. It performs the necessary impedance transformations under both low output power and high output power conditions.
- The output quarter-wave transformer of Figure 54 is replaced by the wideband node matching network of Figure 56.
- The peak amplifier branches of Figure 56 and Figure 54 are swapped to maintain the vertical device alignment which is important in the laying out of the amplifier.

The first peak output matching network converts the off-state impedance of the first peak amplifier device to a short circuit (low impedance), and it converts the load impedance seen by the first peak amplifier branch under a maximum power condition into an impedance associated with a high-power performance of the first peak amplifier device. The second peak output matching network converts the off-state impedance of the second peak amplifier device to an open circuit (high impedance), and it converts the

load impedance seen by the second peak amplifier branch under maximum power condition into an impedance associated with a high-power performance of the second peak amplifier device.

Similarly, the common peak output matching network converts the parallel combination of the off-state impedances from the peak amplifier branches into an open circuit (high impedance) at the combining node, and it converts the load impedance seen at the combining node under maximum power conditions into a value equal to the parallel connection of the load impedances of the peak branches. In other words, what the peak networks do for the individual peak branches, the common network does for the “parallel” connection of the peak branches.

Figure 57 shows a possible generic microstrip implementation of the three-way Doherty amplifier of Figure 56. Its physical compactness is clear if compared to that in Figure 55.

The three-way Doherty arrangement shown in Figure 57 has been designed using the Doherty amplifier synthesis and analysis techniques described in Chapter 5 and Chapter 6. The design target for the modulated signal output power was  $47\text{dBm}$  and peak power (saturation power)  $53.5\text{dBm}$ . The design was based on the load-pull measurements of one active device under three biasing conditions: class-AB for the main device functionality, a "shallow" class-C for the first peak device functionality, and a "deep" class-C for the second peak device functionality<sup>28</sup>. Figure 58 compares the simulated and measured gain and efficiency performance of the compact three-way Doherty amplifier in the pulsed CW regime of operation, and Figure 59 shows measured results in the modulated signal regime of operation. The pulsed CW signal used to obtain the gain and efficiency versus output power had a period of  $100\mu\text{s}$  and a duty-cycle of 10%. The modulated signal used for testing was an LTE signal with bandwidth of  $10\text{MHz}$  and a peak-to-average power ratio of  $6.5\text{dB}$ . Thus the new idea of a compact three-way Doherty amplifier has been validated experimentally.

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<sup>28</sup> In order to ensure proper turn-on timing for the peak devices the input bias for each device needs to be set to a certain level. The "depth" of the class-C bias for the peak device will determine at which input RF power level the device starts to conduct and begins to act as an amplifier (e.g. peak device biased in a "shallow" class-C will start conducting at lower input RF power level than a peak device biased in a "deep" class-C).

Aside from the smaller PCB footprint of the compact design the removal of the three quarter-wave transformers and three offset lines in the main and peak output matching networks, whose combined length at the frequency of operation ( $768\text{MHz}$ ) is approximately  $20\text{cm}$ , resulted in the loss reduction of approximately  $0.2\text{dB}$  for the RO43050B  $30\text{mil}$  thick RF substrate [48] we used in the design that has microstrip insertion loss of  $0.025\text{dB/inch}$  at  $1\text{GHz}$ .

The agreement between the measured and the simulated gain in the pulsed RF regime of operation (Figure 58) is good; the simulated gain is approximately  $1.5\text{dB}$  higher because we used lossless matching networks to obtain simulated results, the loss contribution from the input splitter alone was measured at  $0.35\text{dB}$ , the losses of the input and output matching networks also contribute to the gain discrepancy. High and flat gain is maintained versus output power resulting in good gain linearity especially when it comes to a three-way Doherty. The pulsed RF and modulated gain variation over frequency is less than  $1\text{dB}$ . The measured modulated signal regime drain efficiency of  $45\%$  at  $47\text{dBm}$  output power and  $38\%$  at  $44\text{dBm}$  output power ( $3\text{dB}$  power back-off). The maximum output power achieved was  $200\text{W}$  which indicates efficient power combining of the signals from all three devices (the nominal power rating for the devices used was  $70\text{W}$ )

The pulsed CW signal used to obtain the gain versus output power had a period of  $100\mu\text{s}$  and a duty-cycle of  $10\%$ . The modulated signal used for testing is an LTE signal with bandwidth of  $10\text{MHz}$  and a peak-to-average power ratio of  $6.5\text{dB}$ .

The signal generator [49], the power meter [50], and the spectrum analyzer [51] were used to capture the measurement results summarized in Figure 58 and Figure 59. The block diagram of the setup was identical to that shown in Figure 45.

The measured spectral performance of the compact three-way Doherty for a single carrier is shown in Figure 60, and the performance over frequency is shown in Figure 61. To emphasize the modulated signal gain flatness over frequency Figure 62 provides more detailed view of the signal power levels within each carrier. The drop in gain towards the higher frequency end is expected from the gain curves in Figure 59.

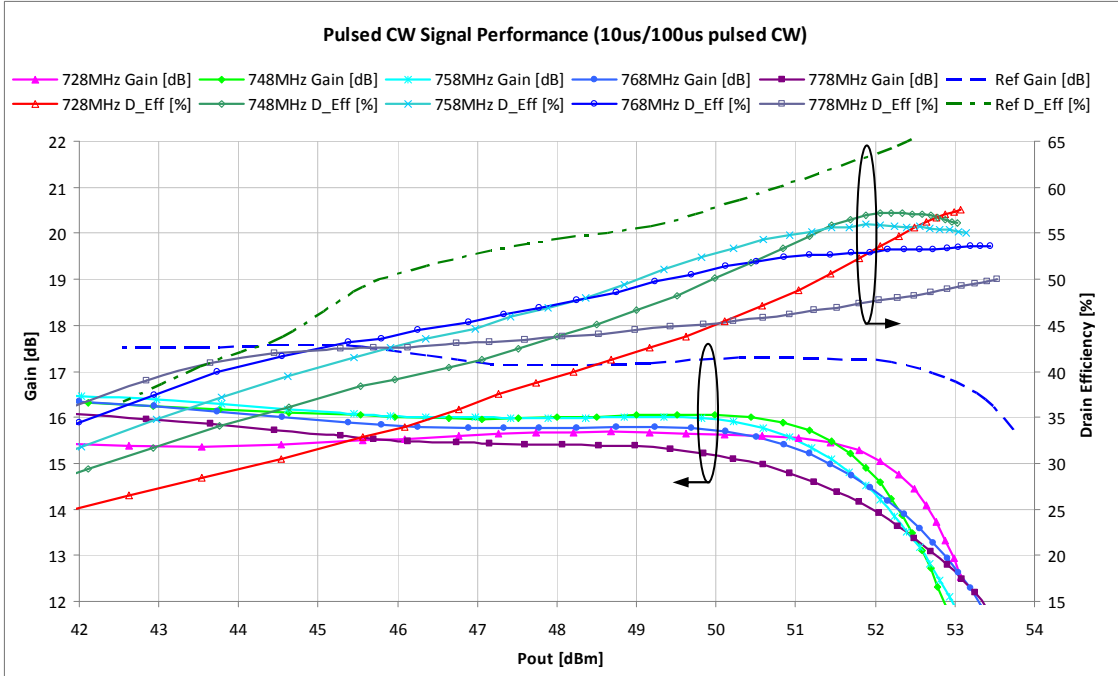


Figure 58: Pulsed CW signal regime measurements of gain and efficiency performance of the compact three-way Doherty amplifier

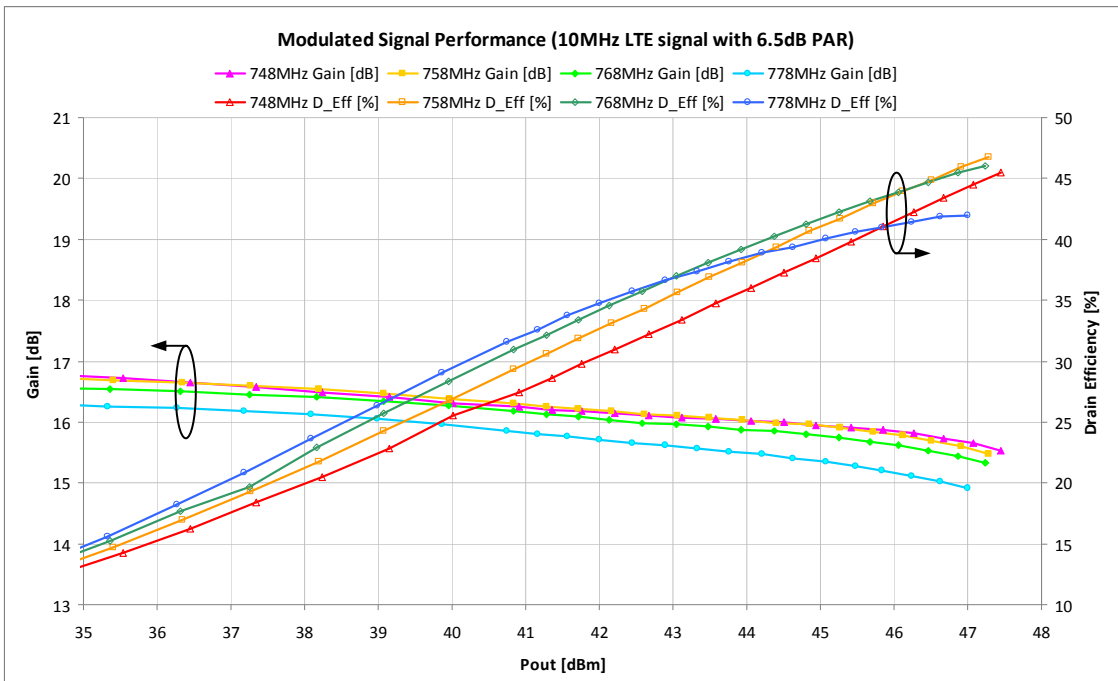
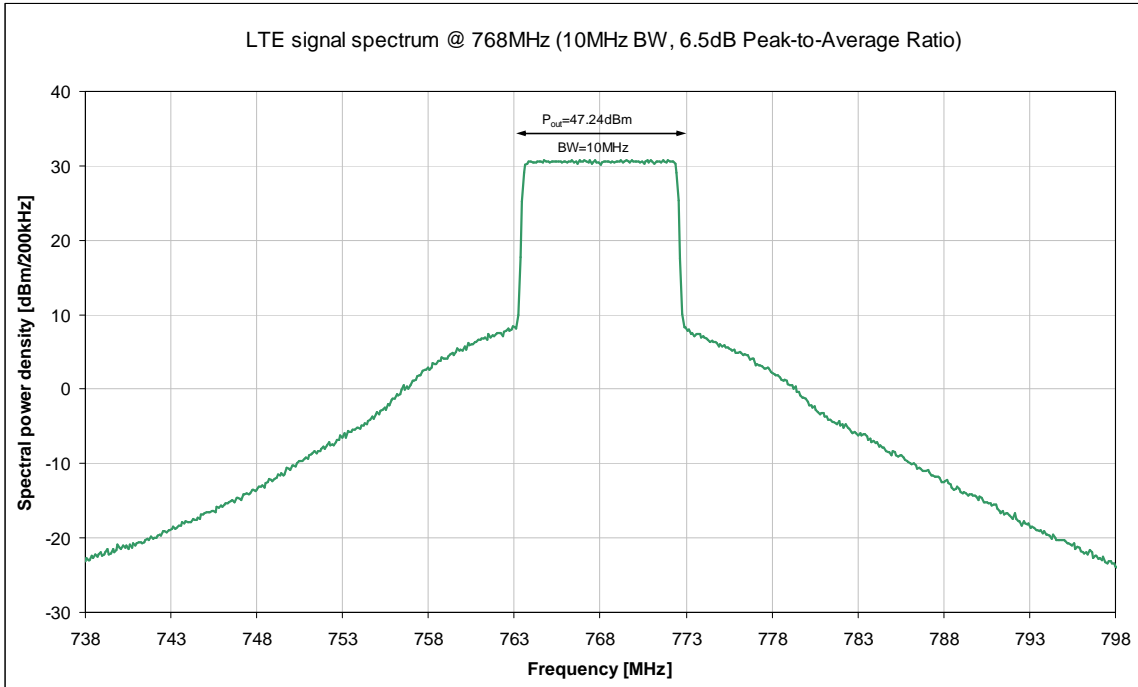
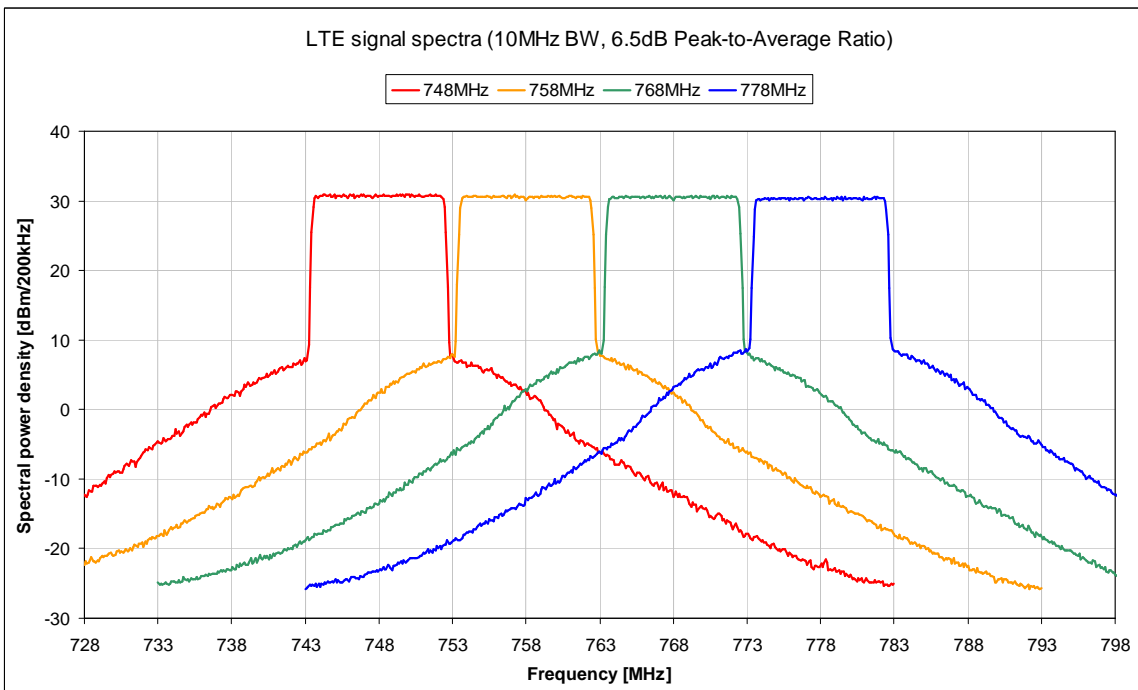


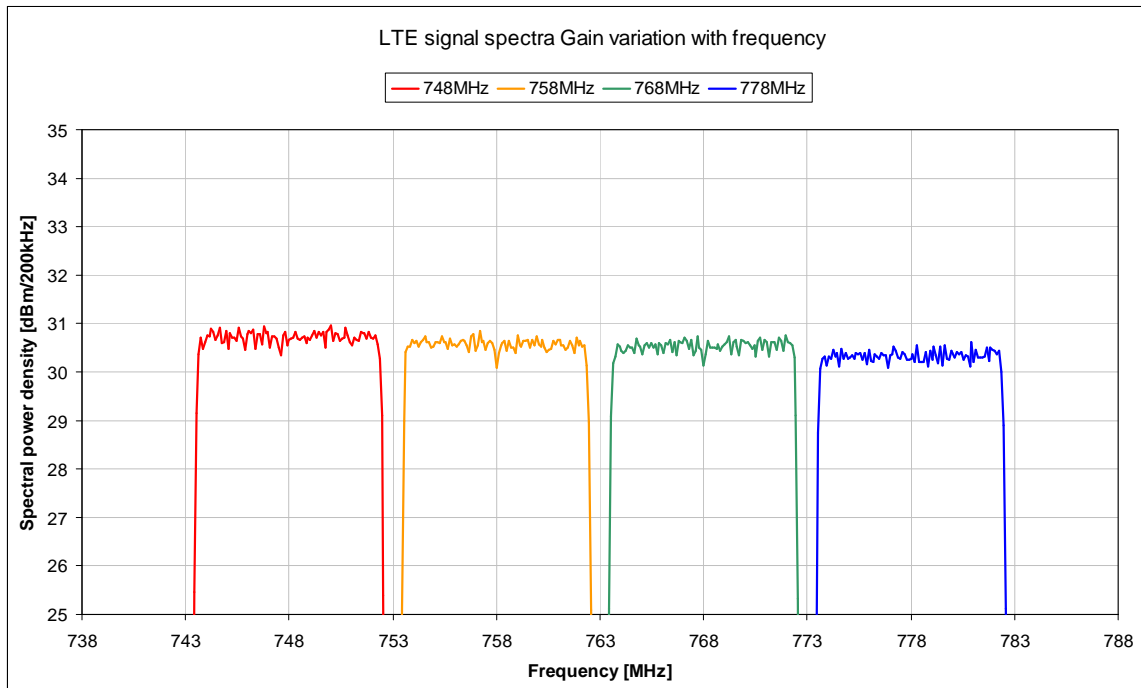
Figure 59: Modulated signal regime measurements of gain and efficiency performance of the compact three-way Doherty amplifier



**Figure 60: Spectral performance of the compact three-way Doherty amplifier**



**Figure 61: Spectral performance of the compact three-way Doherty amplifier over carrier frequency (constant input power to the amplifier)**



**Figure 62: Variation in modulated signal gain of the compact three-way Doherty amplifier over frequency (constant input power to the amplifier chain)**

## **4.5 N-Way Compact Doherty Amplifier (Arbitrary Expansion)**

### **4.5.1 Preliminary Remarks**

We have seen in Section 4.3 and 4.4 that a three-way Doherty amplifier can be obtained from a two-way Doherty amplifier by replacing either the main device branch or the peak device branch by another two-way Doherty amplifier. Expanding a three-way Doherty into a four-way Doherty can be achieved by replacing any of its three branches by another two-way Doherty amplifier. As stated in Section 2.4, N-way Doherty amplifiers have been proposed in many publications [53], [54], [55] and patents [56]. However, the larger the value of N, the more possible ways there are to configure the N-way amplifier. What is sorely missing from the above-mentioned publications, and those like it, are the details as to why a specific N-way configuration was selected, and how it performs. The result of this lack of attention to detail is that many configurations that have been suggested are sub-optimal. We will demonstrate this for two examples in the sub-sections below, where we will show by analysis why they are sub-optimal. Section 4.6 will show the optimal way to configure N-way Doherty amplifiers<sup>29</sup>.

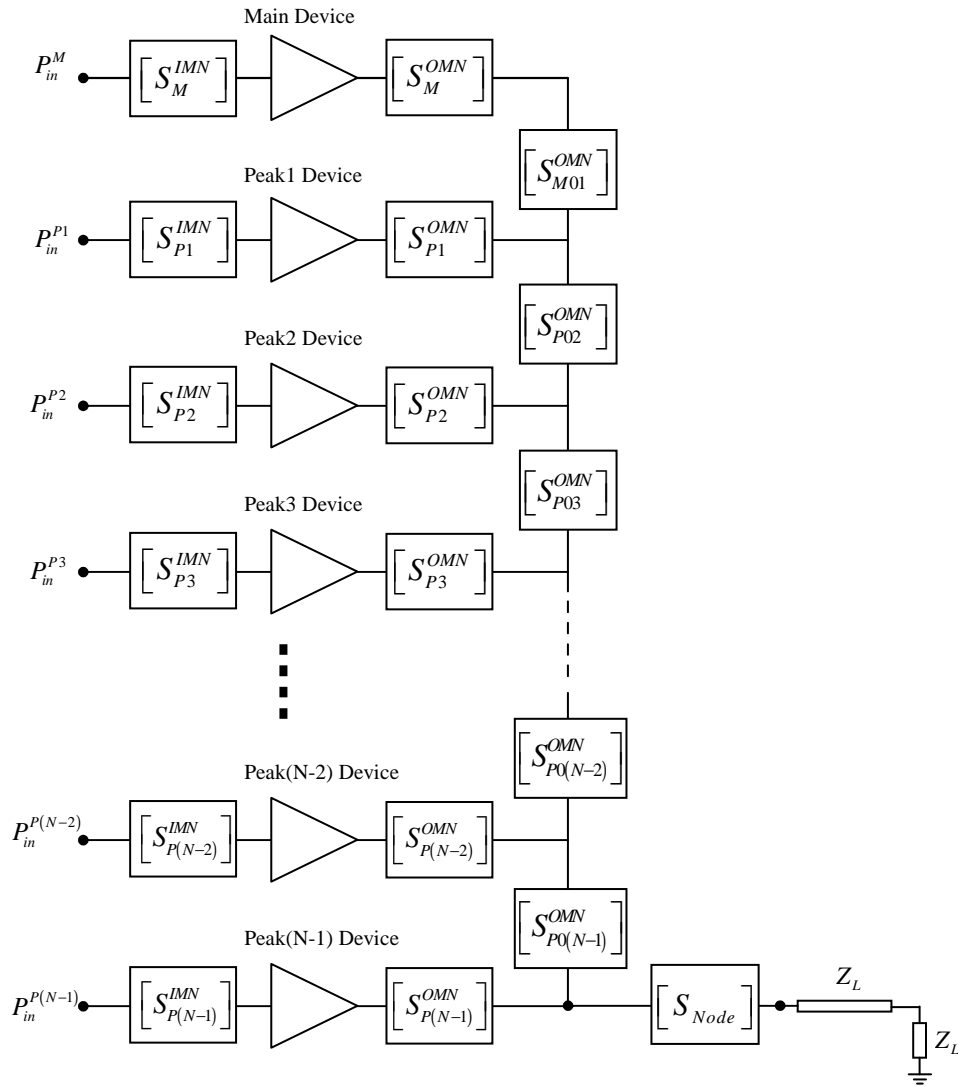
### **4.5.2 First Example of a Sub-Optimal Expansion**

One way of expanding a two-way Doherty into an N-way Doherty amplifier is to successively replace the main device branch of the (N-1)-way Doherty to obtain the N-way Doherty [55]. The result of the first substitution was already shown in Figure 52. Continuing the main device branch substitution on the amplifier resulting from each iteration we obtain the structure shown in Figure 63. The first indication that the architecture in Figure 63 might be suboptimal is the fact that the main device which is active for all signal power levels (class-AB bias) is farthest away from the node where the load is attached, thus experiencing the highest loss levels in the output path of all the

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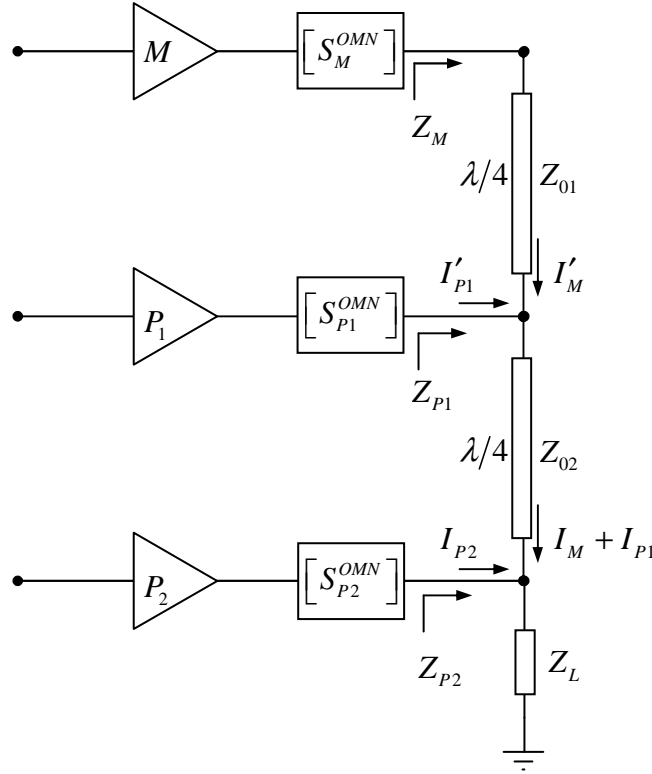
<sup>29</sup> Note that here, and in the remainder of the thesis, it will be only the compact forms of the various amplifier configurations that we will be concerned with.

devices present in the architecture. This will negatively affect the gain of the Doherty amplifier at all signal power levels. The second problem with this architecture is more subtle, and lies in the non-monotonic impedance modulation for the main device (and most likely for several adjacent peak devices for large N). In order to illustrate this non-monotonic impedance modulation for the main device in this type of N-way Doherty amplifier we will analyse the three-way scenario as depicted in Figure 64.



**Figure 63: Block diagram of the compact N-way Doherty amplifier obtained from an (N-1)-way Doherty amplifier by replacing its main branch by another two-way Doherty**

General calculations of impedances presented to the main and peak amplifiers for various output signal levels<sup>30</sup>.



**Figure 64: Block diagram for impedance modulation behaviour analysis**

The impedance seen by the main device as a function of branch currents at the various nodes of the circuit as indicated in Figure 64 is given by

$$(23) \quad Z_M = \frac{Z_{01}^2}{\frac{I'_M + I'_{P_1}}{I'_M} \frac{Z_{02}^2}{\frac{I_M + I_{P_1} + I_{P_2}}{I_M + I_{P_1}} Z_L}}$$

which simplifies to

$$(24) \quad Z_M = \frac{I'_M}{I'_M + I'_{P_1}} \frac{I_M + I_{P_1} + I_{P_2}}{I_M + I_{P_1}} \frac{Z_{01}^2}{Z_{02}^2} Z_L$$

<sup>30</sup> Currents at each of the combining nodes are assumed to be in-phase, more general treatment of currents at combining nodes is covered in Appendix A

The impedance seen by the first peak device as a function of branch currents is

$$(25) \quad Z_{P1} = \frac{I'_M + I'_{P1}}{I'_{P1}} \frac{Z_{02}^2}{\frac{I_M + I_{P1} + I_{P2}}{I_M + I_{P1}}} Z_L$$

which in turn becomes

$$(26) \quad Z_{P1} = \frac{I'_M + I'_{P1}}{I'_{P1}} \frac{I_M + I_{P1}}{I_M + I_{P1} + I_{P2}} \frac{Z_{02}^2}{Z_L}$$

Finally, impedance seen by the second peak device is

$$(27) \quad Z_{P2} = \frac{I_M + I_{P1} + I_{P2}}{I_{P2}} Z_L$$

A low output power level implies that only the main amplifier is active and both peak amplifiers are off. In that case we have:  $I_M \neq 0$ ,  $I'_M \neq 0$  and  $I'_{P1} = I_{P1} = I_{P2} = 0$ . Thus the impedances in (24), (26), and (27) become

$$(28) \quad Z_M = \frac{Z_{01}^2}{Z_{02}^2} Z_L; \quad Z_{P1} = \infty; \quad Z_{P2} = \infty$$

An intermediate output power level implies that main and first peak amplifiers are active but the second peak amplifier is off. In that case:  $I_M \neq 0$ ,  $I'_M \neq 0$ ,  $I_{P1} \neq 0$ ,  $I'_{P1} \neq 0$  and  $I_{P2} = 0$ . Therefore we have

$$(29) \quad Z_M = \frac{I'_M}{I'_M + I'_{P1}} \frac{Z_{01}^2}{Z_{02}^2} Z_L; \quad Z_{P1} = \frac{I'_M + I'_{P1}}{I'_{P1}} \frac{Z_{02}^2}{Z_L}; \quad Z_{P2} = \infty$$

At high output power level all amplifiers are active, and so:  $I_M \neq 0$ ,  $I'_M \neq 0$ ,  $I_{P1} \neq 0$ ,  $I'_{P1} \neq 0$  and  $I_{P2} \neq 0$ . As a result

$$(30) \quad Z_M = \frac{I'_M}{I'_M + I'_{P1}} \frac{I_M + I_{P1} + I_{P2}}{I_M + I_{P1}} \frac{Z_{01}^2}{Z_{02}^2} Z_L$$

$$(31) \quad Z_{P1} = \frac{I'_M + I'_{P1}}{I'_{P1}} \frac{I_M + I_{P1}}{I_M + I_{P1} + I_{P2}} \frac{Z_{02}^2}{Z_L}$$

and

$$(32) \quad Z_{P2} = \frac{I_M + I_{P1} + I_{P2}}{I_{P2}} Z_L$$

The main device impedance modulation ratio (ratio between impedance seen by the main device in the low power state to that seen in the high power state) is given by

$$(33) \quad N_M = \frac{\frac{Z_{01}^2}{Z_{02}^2} Z_L}{\frac{I'_M}{I'_M + I'_{P1}} \frac{I_M + I_{P1} + I_{P2}}{I_M + I_{P1}} \frac{Z_{01}^2}{Z_{02}^2} Z_L} = \frac{(I'_M + I'_{P1})(I_M + I_{P1})}{I'_M (I_M + I_{P1} + I_{P2})}$$

In the symmetric case ( $I'_M = I'_{P1}$  and  $I_M = I_{P1} = I_{P2}$ ) the main device impedance modulation ratio is

$$(34) \quad N_M = \frac{(I'_M + I'_{P1})(I_M + I_{P1})}{I'_M (I_M + I_{P1} + I_{P2})} = \frac{4}{3}$$

This is actually lower than that of the symmetric two-way Doherty ( $N_M = 2$ ) and so is not optimal for maximizing the amplifier efficiency performance.

The only way to increase the main device impedance modulation ratio is to use an asymmetric configuration where the first peak device must be larger than the main device. Increasing the size of the second peak device will decrease the main device modulation ratio. Having the first peak device larger than the main will cause the impedance presented to main amplifier to non-monotonically decrease with an increase in the output power levels. This can be seen by comparing expressions for  $Z_M$  in intermediate and high power cases. This means that if the main amplifier output matching

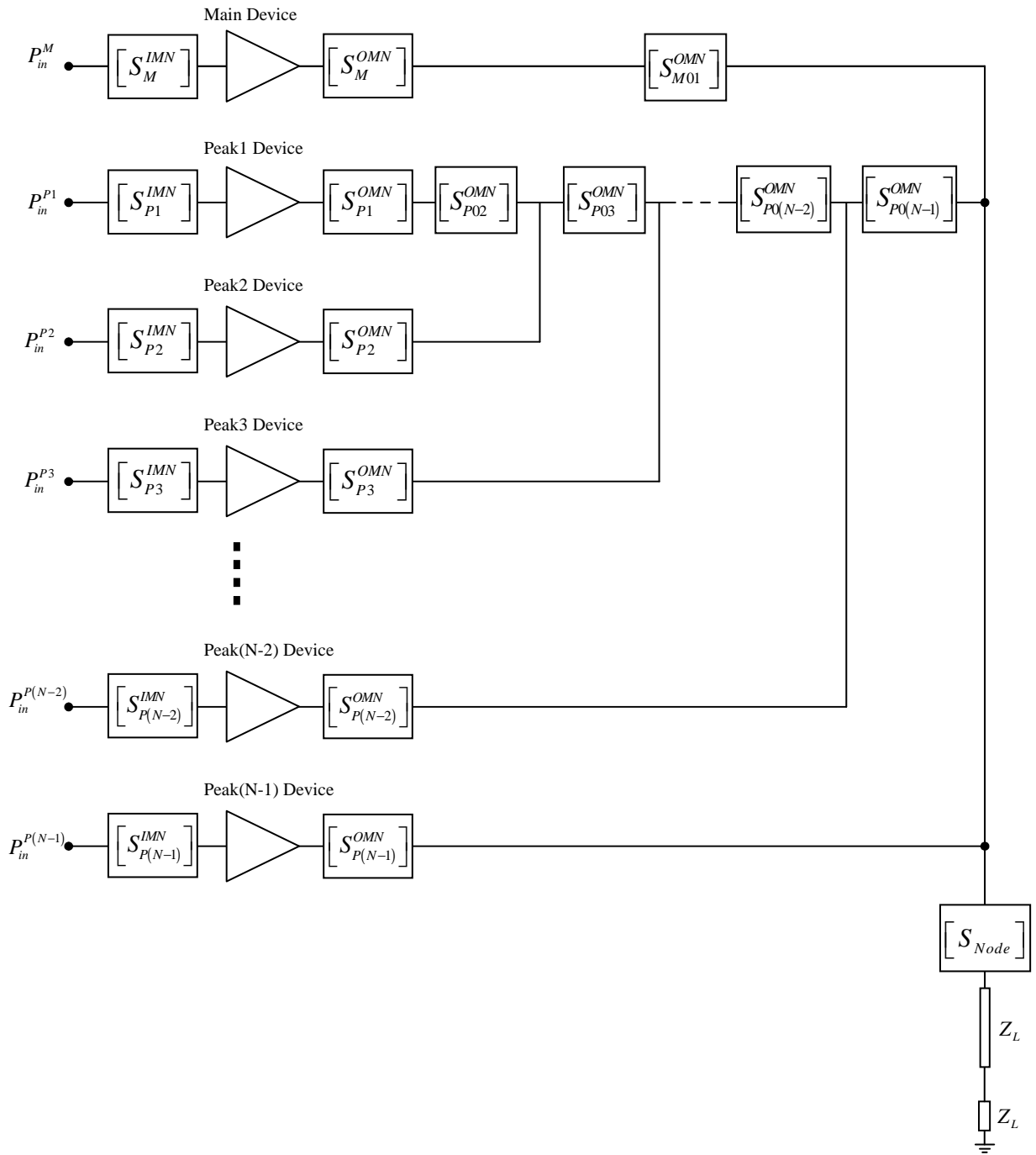
network is designed to saturate the main amplifier at the intermediate output power level it will clip the signal at high output power levels. If it is designed to saturate the main amplifier at the high output power level it will not be as efficient at the intermediate power level.

### 4.5.3 Second Example of a Sub-Optimal Expansion

Another way of expanding two-way Doherty into an N-way Doherty is to successively replace the first peak device branch of the (N-1)-way Doherty to obtain an N-way Doherty [56]. The result of the first substitution was already shown in Figure 57. Continuing the first peak device branch substitution on the amplifier resulting from each iteration we obtain the structure shown in Figure 65. The first indication that the architecture in Figure 65 is suboptimal is the fact that the first peak device, which is the most active of all peak devices (shallowest Class-C bias), is farthest away from the node where the load is attached. It thus experiences the highest loss levels in the output path of all the peak devices present in the architecture. The second problem with this architecture is similar to the previous case, and lies in the non-monotonic impedance modulation for the first peak device. All the drawbacks described in the previous case as applying to the main device now apply to the first peak device in the present case.

### 4.5.4 Improved Course of Action

We have described only two out of many other similarly sub-optimal ways to expand to an N-way Doherty amplifier from a two-way Doherty amplifier. The N-way Doherty obtained through an arbitrary expansion ([58], [59]) where any one of the devices in the (N-1)-way Doherty (with exception of the last peak device) is replaced by a two-way Doherty will suffer to various extents from the drawbacks described for the two cases discussed above. In the next section we will describe a better way to generate N-way Doherty amplifiers.



**Figure 65: Block diagram of the compact N-way Doherty amplifier obtained from (N-1)-way Doherty amplifier by replacing its first peak branch by another two-way Doherty amplifier**

#### 4.6 Compact N-Way Doherty Amplifier: Last Peak Amplifier of (N-1)-Way Doherty Replaced by a Two-Way Doherty Amplifier

As shown in Figure 66, the architecture of the compact three-way Doherty amplifier of Figure 56 can be extended to a general  $N$ -way compact Doherty amplifier (having a main amplifier branch and  $(N-1)$  peak amplifier branches, where  $N \geq 3$ ), using the design-extension technique of repeatedly replacing the last peak amplifier branch of the  $(N-1)$ -way Doherty amplifier by another two-way Doherty amplifier.

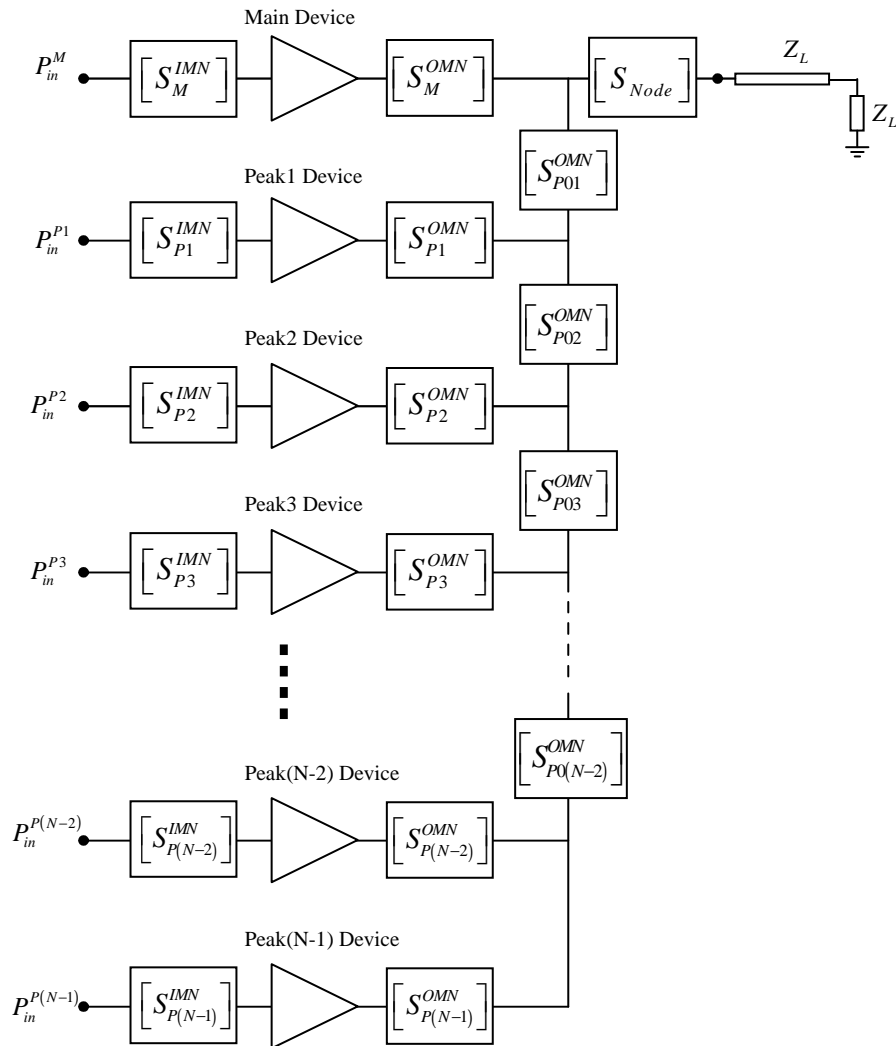


Figure 66: Block diagram of the new compact N-way Doherty design derived from an (N-1)-way Doherty by replacing its last peak amplifier by another two-way Doherty

Extending the design by replacing the last peak amplifier branch by another two-way Doherty amplifier has a consequence that the main device is directly connected to the main combining node, and the peak devices that turn on earlier are closer to the main combining node, which is desirable.

Note that, in Figure 66, the first peak amplifier branch is connected to the main amplifier branch by a first common peak output matching network and each other peak amplifier branch is connected to its preceding peak amplifier branch by a common peak output matching network, except for the last two peak amplifier branches, which are not interconnected by a corresponding common peak output matching network. The functionality of that last common peak output matching network may be said to be subsumed the peak output matching network of the last peak amplifier branch.

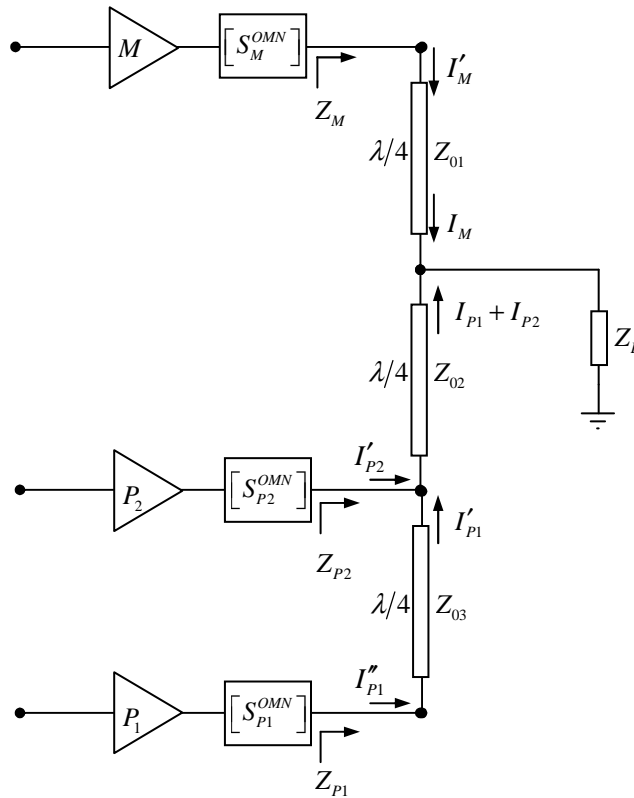


Figure 67: Block diagram for impedance modulation behaviour analysis

We will once again analyze the impedances presented to the main and peak amplifier devices for various output signal level scenarios for the three-way realisation of Figure 66, namely that shown in Figure 54.

The impedance seen by the main device as a function of the branch currents at the various nodes of the circuit in Figure 67<sup>31</sup> is given by

$$(35) \quad Z_M = \frac{Z_{01}^2}{\frac{I_M + I_{P1} + I_{P2}}{I_M} Z_L}$$

which simplifies to

$$(36) \quad Z_M = \frac{I_M}{I_M + I_{P1} + I_{P2}} \frac{Z_{01}^2}{Z_L}$$

The impedance seen by the first peak device is similarly given by

$$(37) \quad Z_{P1} = \frac{Z_{03}^2}{\frac{I'_{P1} + I'_{P2}}{I'_{P1}} \frac{Z_{02}^2}{\frac{I_M + I_{P1} + I_{P2}}{I_{P1} + I_{P2}} Z_L}}$$

which reduces to

$$(38) \quad Z_{P1} = \frac{I'_{P1}}{I'_{P1} + I'_{P2}} \frac{I_M + I_{P1} + I_{P2}}{I_{P1} + I_{P2}} \frac{Z_{03}^2}{Z_{02}^2} Z_L$$

The impedance seen by the second peak device as a function of branch currents is given by the expression

$$(39) \quad Z_{P2} = \frac{I'_{P1} + I'_{P2}}{I'_{P2}} \frac{Z_{02}^2}{\frac{I_M + I_{P1} + I_{P2}}{I_{P1} + I_{P2}} Z_L}$$

which can be written as

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<sup>31</sup> Currents at each of the combining nodes are assumed to be in-phase, more general treatment of currents at combining nodes is covered in Appendix A

$$(40) \quad Z_{P2} = \frac{I'_{P1} + I'_{P2}}{I'_{P2}} \frac{I_{P1} + I_{P2}}{I_M + I_{P1} + I_{P2}} \frac{Z_{02}^2}{Z_L}$$

A low output power level would mean that only the main amplifier is active and both peak amplifiers are off. In that case we have  $I_M \neq 0$ ,  $I'_M \neq 0$  and  $I''_{P1} = I'_{P1} = I_{P1} = I'_{P2} = I_{P2} = 0$ . Expressions (36), (38), and (40) then become

$$(41) \quad Z_M = \frac{Z_{01}^2}{Z_L}; \quad Z_{P1} = \infty; \quad Z_{P2} = \infty$$

At intermediate output power levels the main and first peak amplifiers are active, and the second peak is off. In that case we have  $I_M \neq 0$ ,  $I'_M \neq 0$ ,  $I_{P1} \neq 0$ ,  $I'_{P1} \neq 0$ ,  $I''_{P1} \neq 0$ ,  $I_{P2} = 0$  and  $I'_{P2} = 0$ , and expressions (36), (38), and (40) become

$$(42) \quad Z_M = \frac{I_M}{I_M + I_{P1}} \frac{Z_{01}^2}{Z_L}; \quad Z_{P1} = \frac{I_M + I_{P1}}{I_{P1}} \frac{Z_{03}^2}{Z_{02}^2} Z_L; \quad Z_{P2} = \infty$$

A high output power level requires that all amplifiers are active. In that case we have  $I_M \neq 0$ ,  $I'_M \neq 0$ ,  $I_{P1} \neq 0$ ,  $I'_{P1} \neq 0$ ,  $I''_{P1} \neq 0$ ,  $I_{P2} \neq 0$  and  $I'_{P2} \neq 0$ , so that

$$(43) \quad Z_M = \frac{I_M}{I_M + I_{P1} + I_{P2}} \frac{Z_{01}^2}{Z_L}$$

$$(44) \quad Z_{P1} = \frac{I'_{P1}}{I'_{P1} + I'_{P2}} \frac{I_M + I_{P1} + I_{P2}}{I_{P1} + I_{P2}} \frac{Z_{03}^2}{Z_{02}^2} Z_L$$

and

$$(45) \quad Z_{P2} = \frac{I'_{P1} + I'_{P2}}{I'_{P2}} \frac{I_{P1} + I_{P2}}{I_M + I_{P1} + I_{P2}} \frac{Z_{02}^2}{Z_L}$$

The main device impedance modulation ratio (ratio of impedance seen by the main device in the low power state to that of the high power state) is given by

$$(46) \quad N_M = \frac{\frac{Z_{01}^2}{Z_L}}{\frac{I_M}{I_M + I_{P1} + I_{P2}} \frac{Z_{01}^2}{Z_L}} = \frac{I_M + I_{P1} + I_{P2}}{I_M}$$

In the symmetric case ( $I_M = I_{P1} = I_{P2}$ ) this gives

$$(47) \quad N_M = 3$$

This is equal to that of the two-to-one asymmetric two-way Doherty, and is optimal for maximizing the amplifier efficiency performance.

To further illustrate that all devices experience monotonic impedance modulation we will assign the specific characteristic impedance values

$$(48) \quad Z_{01} = Z_0; \quad Z_{02} = \frac{Z_0}{2}; \quad Z_{03} = Z_0; \quad Z_L = \frac{Z_0}{3}$$

to the each of the quarter-wave transformers in Figure 67 to produce the symmetric design that will load each device with  $Z_0$  at the amplifier's maximum power level when each device is providing equal power contribution.

Under low output power level conditions this would result in

$$(49) \quad Z_M = \frac{Z_{01}^2}{Z_L} = 3Z_0; \quad Z_{P1} = \infty; \quad Z_{P2} = \infty$$

Under intermediate output power level conditions (assuming  $I_M = I_{P1}$ ) we would have

$$(50) \quad Z_M = \frac{I_M}{I_M + I_{P1}} \frac{Z_{01}^2}{Z_L} = \frac{3}{2}Z_0; \quad Z_{P1} = \frac{I_M + I_{P1}}{I_{P1}} \frac{Z_{03}^2}{Z_{02}^2} Z_L = \frac{8}{3}Z_0; \quad Z_{P2} = \infty$$

Under high output power level conditions (assuming  $I_M = I_{P1} = I_{P2}$  and  $I'_{P1} = I'_{P2}$ ) we would have

$$(51) \quad Z_M = \frac{I_M}{I_M + I_{P1} + I_{P2}} \frac{Z_{01}^2}{Z_L} = \frac{1}{3} \frac{Z_0^2}{\frac{Z_0}{3}} = Z_0$$

$$(52) \quad Z_{P1} = \frac{I'_{P1}}{I'_{P1} + I'_{P2}} \frac{I_M + I_{P1} + I_{P2}}{I_{P1} + I_{P2}} \frac{Z_{03}^2}{Z_{02}^2} Z_L = \frac{1}{2} \frac{3}{2} \frac{Z_0^2}{Z_0} \frac{Z_0}{3} = Z_0$$

and

$$(53) \quad Z_{P2} = \frac{I'_{P1} + I'_{P2}}{I'_{P2}} \frac{I_{P1} + I_{P2}}{I_M + I_{P1} + I_{P2}} \frac{Z_{02}^2}{Z_L} = 2 \frac{2}{3} \frac{Z_0^2}{Z_0} = Z_0$$

This configuration provides monotonically decreasing load impedance presented to each individual amplifier with increasing output power. This allows for design of output matching networks that can keep each individual amplifier as close to saturation as possible (thus operating with high efficiency) for all output power level situations.

By using three identical devices in the symmetrical design with 3-to-1 load modulation of the main device, and provided that the main device does indeed have a power back-off capability of  $4.77dB$  (that corresponds to 3-to-1 load modulation), the achievable maximum efficiency power back-off becomes  $9.54dB$ . This yields a maximum power equal to three times that of the single device, most importantly maintaining the high efficiency over the upper  $9.54dB$  of the amplifier power range. This means that the modulated signal with a  $6.5dB$  peak-to-average ratio can be backed-off  $3dB$  in power without penalty in efficiency.

## **4.7 Conclusion**

Although the conventional two-way, three-way and N-way Doherty amplifiers are known in the literature, we believe that these configurations have not been subjected to critical analysis and so have been less understood than could have been the case.

What we have called the compact versions of these amplifiers has been introduced in this chapter for the first time. Although this new idea is based on not cascading separate impedance inverters and offset lines to form the output sections of the amplifier branches, it is more than this. It allows one to achieve optimal impedance modulation through an optimization process rather than preconceived notions of what the constituent parts (namely inverters and offset lines) must separately do before being cascaded. This has been demonstrated both in simulation and experimentally in this chapter for compact two-way and three-way Doherty amplifiers designed using the new design methods that will be the subject of Chapter 5 and Chapter 6. The physical circuit simulations and optimizations used were done using the Microwave Office Software of Applied Wave Research (AWR), as previously mentioned in Chapter 3.

There are many ways to extend the two-way amplifier configuration into an N-way Doherty amplifier, but no references have been found that examine precisely which approach is the best. This has been done in the present chapter. We have shown through analysis which expansion method is superior to all others.

## **4.8 References for Chapter 4**

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## Chapter 5

# 5 Doherty Amplifier Design Synthesis Techniques Based on Transistor Load-Pull Measurements

### 5.1 Introduction

The need for better design procedures for Doherty amplifiers has been argued in Section 1.5 and 2.7. In this chapter we will introduce such improved Doherty amplifier design techniques, that will take us from the amplifier performance design specifications, through use of load-pull data that characterizes the active devices, the impedance modulation effects that take place at amplifier's combining node(s) to the functional design of the amplifier. We will use amplifier performance specifications<sup>32</sup>, together with active device load-pull data<sup>33</sup> along with constraining conditions related to impedance modulation ratio at amplifier node(s) and the related impedance modulation that the main device itself undergoes (that make the amplifier design viable), to obtain the S-parameters required of each of the passive circuit blocks for the amplifier configurations in Figure 70, Figure 75, and Figure 76

The authors of [60] and [61] are also concerned with reducing the physical size of the output combining networks of Doherty amplifiers. In [60] a length of line is retained as part of an impedance inverter, but the structure is shortened compared to a quarter-wavelength by loading it with shunt capacitors. In [61] the quarter wave impedance inverter is completely implemented using lumped components (that is, there is no transmission line used) but the inverter is still explicitly used. The work closest to that developed in this chapter is that published in [62], which appears to have been completed sometime after that described in this chapter [63]. At any rate, the treatment in [62] is

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<sup>32</sup> such as maximum output power, efficiency, gain, gain linearity, etc

<sup>33</sup> that characterizes the behaviour of the active devices

based on certain assumptions which are not necessary for the more general method of calculation adopted here.

In section 5.2 we discuss what load-pull data is necessary (for the design procedure) for each of the devices in the amplifier, along with suggestions for the selection of impedance points from the data sets that will lead to a viable final design and fulfillment of the performance specifications. “It might be thought that load-pull techniques, along with the slide rule and the slotted line, would be teetering on the brink of extinction due to the availability and almost universal intrusion of the (modelling) approach into RF circuit design. Judging, however, by the continuing evolution and availability of more complex and versatile commercial load-pull hardware, it would seem that this is a preserve which has successfully survived the (modelling) revolution”. This comment<sup>34</sup> was made in 2006, but remains true at the time of the writing of this thesis. In this thesis we will develop an improved design method based on measured load-pull data that allows subsequent analysis based on analytical expressions without the need for additional models of the active device. If a behavioural (or other) model is indeed available then the model can be load-pulled (“virtual” load-pulling) and this data used to do the PA design via the new method. Unfortunately, such device models are usually only accessible from vendors for devices that have been around for some time. It is true that, at the time of the writing of this thesis, at least one vendor will provide device models prior to actual production devices being available. In such cases the model can be load-pulled and the new design method used. If the actual transistors are available it is best to load-pull the actual device of course, but pre-production device samples are seldom forthcoming from vendors.

Section 5.3 deals with the design of a fixed-input-power-split Doherty amplifier. The design procedure is subdivided into several sections:

- Section 5.3.1 provides the description of the *fixed-input-power-split* two-way Doherty amplifier and its constituent parts.

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<sup>34</sup> S.C.Cripps, *RF Power Amplifiers for Wireless Communications* (Artech House Inc., 2006) 2<sup>nd</sup> Edition.

- In section 5.3.2 the input split ratio, and the main combining node impedance modulation ratio  $N_{comb}$  calculations based on the selection of certain impedance points<sup>35</sup> in the load-pull data are presented. Without class-C load-pull data (which is generally unavailable or ignored) neither can be accurately determined.
- Standard expressions used for dealing with two-port matching networks characterized by S-parameters are given in Section 5.3.3.
- The calculation of S-parameters of main input matching network, peak input matching network and the node transformer based on impedances  $Z_S^M$ ,  $Z_S^P$ , and  $Z_{node}$  respectively is shown in Section 5.3.4. In the standard approach these are implemented as circuits which is time consuming and inflexible.
- The derivation of the main device impedance modulation ratio, based on the selection of the main device high-power impedance  $Z_{MP}$  and high-efficiency impedance  $Z_{ME}$  from the main device load-pull contours, is described in Section 5.3.5. In the standard approach this is assumed to be an integer disregarding the actual value of the combining node impedance modulation ratio.
- The derivation of the closed form expressions that will yield the S-parameters required for the main output matching network, based on the selection of the main device high-power impedance  $Z_{MP}$ , the high-efficiency impedance  $Z_{ME}$ , the designer-selected impedance  $Z_{node}$ , and the main device impedance modulation ratio  $N_M$ , is presented in Section 5.3.6. In the standard approach the time consuming circuit implementation is used thus limiting the number of variations that can be examined.
- The derivation of the closed form expressions that will yield the S-parameters required of the peak output matching network, based on the selection of the peak device high-power impedance  $Z_{PP}$ , the peak device off-state impedance  $Z_{OFF}$ , the designer-selected impedance  $Z_{node}$ , the peak device impedance modulation ratio

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<sup>35</sup> Main device high-power impedance  $Z_{MP}$ , and peak device high-power impedance  $Z_{PP}$ , and associated performance parameters from the load-pull data sets of each device

$N_p$ , and the main node impedance modulation ratio  $N_{comb}$ , is given in Section 5.3.7. In the standard approach the time consuming circuit implementation is used thus limiting the number of variations that can be examined.

- The derivation of the port voltage transfer function of an S-parameter characterized two-port network terminated in arbitrary load that yields the voltage phase delay is given in Section 5.3.8. This is needed to complete the design process. The standard approach deals with this after the prototype is built.
- The design process flowchart summarizing the complete design procedure is provided in Section 5.3.9.

Based on the expressions derived in Section 5.3, but incorporating additional degrees of freedom available from the independently controlled inputs to the main and peak devices, we present in Section 5.4 the design procedure for a *controlled-main-device-compression two-way* Doherty amplifier.

The design procedure for the *fixed-input-power-split three-way* Doherty amplifier, as an extension to the fixed-input-conditioning fixed power-split two-way Doherty amplifier, with the additional complexities fully addressed, is the subject of Section 5.5.

Section 5.6 provides some conclusions for the chapter, with references listed in Section 5.7.

## **5.2 Load-Pull Data Needed**

To design a two-way Doherty at least three sets of load-pull contours are used at each frequency of interest. For the main device, two sets of constant-compression load-pull contours are used, for example, high-compression ( $3dB$  compression or higher) load-pull contours for selection of impedance  $Z_{MP}$  that is associated with high-power performance of the main device and low-compression (circa  $1dB$  compression) load-pull contours for selection of impedance  $Z_{ME}$  associated with high-efficiency performance of the main device that are obtained for the main device operating under class-AB bias conditions. The compression value that is used to describe constant compression contours is the amount of gain decrease from the maximum level. For the peak device, one set of constant-compression load-pull contours obtained under class-C bias conditions is used,

for example, high-power, 1dB-compression contours, to obtain impedance  $Z_{pp}$  that is associated with the high-power operation of the peak device. The measurement of the peak device off-state impedance  $Z_{OFF}$  for the low-power operation is needed to characterize the loading the peak branch will exert on the main branch while the peak device is disabled. Because a class-C device has a lower gain, it will undergo lower compression compared to the main device. For the case of the peak device, 1dB compression can be considered high compression.

Load-pull data is obtained for the devices that will be used in the amplifier design and construction. The devices are measured under the same (or similar) biasing and power conditions under which they are intended to be used. The load-pull data consists of input power sweeps done for each of the load impedances presented to the device. The load-pull setup consists of a vector signal generator, source impedance transformer (e.g., the source tuner cascaded with the device input fixture), the device under test (e.g., transistor), load impedance transformer (e.g., the device output fixture cascaded with the load tuner), and vector a signal receiver. A set of load impedances to characterize the device under test is selected. Several trial measurements may be required to determine the optimal set of load impedances. Once the device is biased for desired operating conditions, for each of the load impedances presented to the device by the load impedance transformer, the input power is swept over a prescribed range, and various performance parameters of the transistor are recorded (e.g., output power, gain, efficiency, AM-PM, insertion phase, drain current, etc.). The measurements are performed according to the following nesting:

```
Set bias
  Set frequency
    Set load impedance
      Sweep input power and collect measured data
    Next load impedance
  Next frequency
Next bias
```

The measurements are taken for various biasing conditions (class-AB, class-B, class-C of various depths<sup>36</sup>). The measurements are often done for more than one frequency to get better characterization over frequency. The data sets obtained at each frequency of interest are used to characterize amplifier performance at that frequency. For each value of load impedance, the device (keeping the same input power conditions) will have different performance regarding output power, gain, and efficiency. From the load-pull data the designer chooses the main device load impedance  $Z_{MP}$  with associated output power, gain and efficiency that satisfy the high-power requirement for the main device. Another impedance  $Z_{ME}$  is selected for the main device with associated output power, gain and efficiency but this time to satisfy the high-efficiency requirement at power back-off for the main device. For the peak device impedance  $Z_{PP}$  associated with high power performance of the peak device is selected.

In the design synthesis procedure, the load-pull data are plotted in constant-compression contour format to facilitate the visual selection of the impedances. This is similar to topographical maps with constant elevation contours, where it becomes easy to locate mountain peaks or plateaus. Since the Doherty amplifier synthesis procedure is only based on selection of several discrete impedance points ( $Z_{MP}$  for the main device high-power performance,  $Z_{ME}$  for the main device high-efficiency performance, and  $Z_{PP}$  for the peak device high power performance) the captured load-pull data needs to only extensive enough to capture regions of interest where main device has high power and high efficiency performance and the peak device high power performance. To synthesise N-way Doherty amplifier two sets of constant compression contours are needed for the main device load impedance selections: high-compression contours for high power performance ( $Z_{MP}$ ) and low-compression contours for high efficiency performance ( $Z_{ME}$ ). For each of the peak devices one set of constant compression contours is needed for selection of high power performance loading impedances ( $Z_{PP}$ ), the off-state impedance  $Z_{POFF}$  also needs to be measured.

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<sup>36</sup> Usually the device input terminal class-C bias is expressed relative to class-AB bias by indicating the difference of the class-C and class-AB bias (class-C=Class-AB-1V or simply AB-1V).

In the analysis procedure, the load-pull data are plotted in constant-input-power contour format to facilitate the tracking of the load impedance modulation effects that result from convergence calculations in the passive circuit part of the network (main matching network, peak matching network, node matching network). The impedance modulation for the main device will usually involve only impedances in the region between the main device high power operation load impedance  $Z_{MP}$  and high efficiency operation load impedance  $Z_{ME}$ . For symmetric two-way Doherty designs this impedance region may not be very extensive and collected load-pull data set needs only be large enough to encompass an area in impedance space sufficient to contain the  $Z_{MP}$  and  $Z_{ME}$  along with other loading impedances lying on various possible trajectories that impedance modulation process may take the main device through in the course of Doherty amplifier operation. However in the case of asymmetric two-way Doherty amplifiers or N-way Doherty amplifier the separation between  $Z_{MP}$  and  $Z_{ME}$  for the main device can be quite substantial and captured load-pull data set will need to be larger to accommodate it.

For the peak devices the load-pull data set needs to cover as much of the smith chart as possible because of the more extreme impedance modulation that peak device undergoes<sup>37</sup>. For N-way Doherty amplifiers the class-C data needs to be obtained for various values of gate bias and possibly for various values of drain bias. The power sweep does not have to have the same number of points as the impedances are swept through the smith chart, impedances close to the high-power point will have full set of power points where as the impedances quite distant from the high power points may be characterized by a reduced set of power points (because the device operates at low power levels for these particular points).

Example of impedance selection for the design of a three-way Doherty main amplifier ( $Z_{MP}$ ) in class-AB (quiescent drain current of approximately 1200mA) from

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<sup>37</sup> This is due to the fact that the peak device load impedance starts from the edge of the smith chart in the off-state, and it traverses the  $Z'_{POFF}$  (complex conjugate of the peak device off-state impedance  $Z_{POFF}$ ) on its way to  $Z_{PP}$  which it reaches when the peak device is in high power mode of operation.

constant compression load-pull contours for  $1dB$  and  $5.3dB$  compression are shown in Figure 68.

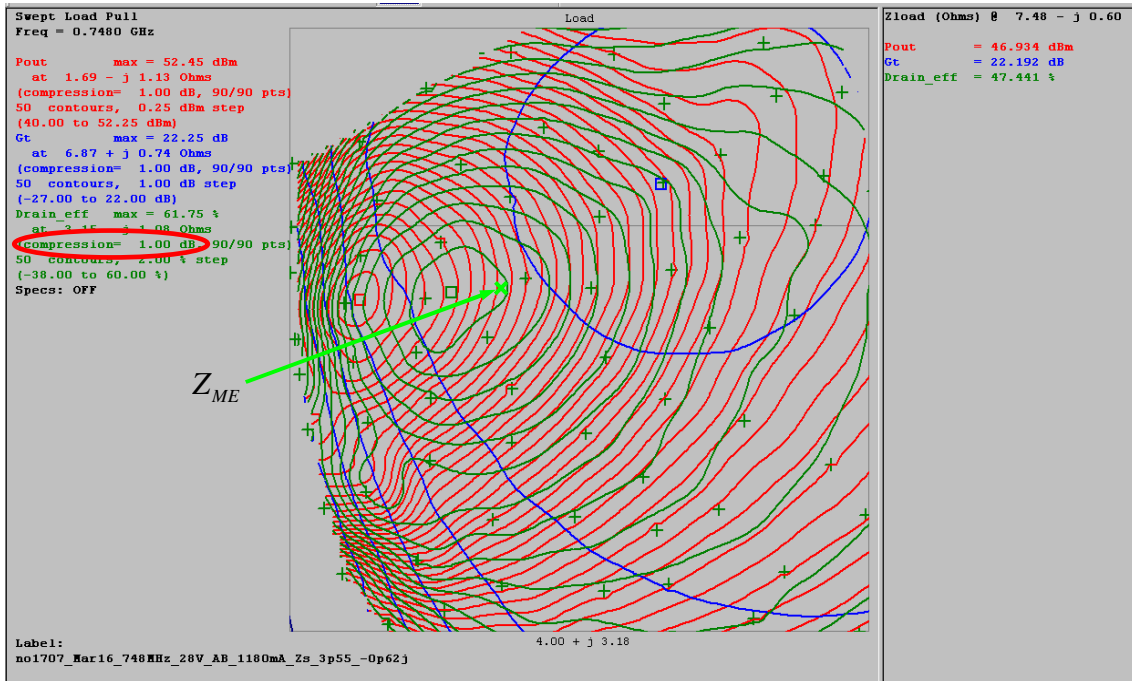
Example of impedance selection for the design of a three-way Doherty peak amplifiers, the first peak device ( $Z_{PP1}$ ), and the second peak device ( $Z_{PP2}$ ) in class-C (obtained for gate bias voltages of  $-1.75V$  and  $-1V$  relative to the class-AB bias) constant compression load-pull contours for  $0.6dB$  and  $2.3dB$  compression are shown in Figure 69. These sets of load-pull data were used in the design of a three-way Doherty amplifier hence multiple class-C load-pull contours under various gate bias conditions.

The sample of the load-pull data in text format is shown in Table 1.

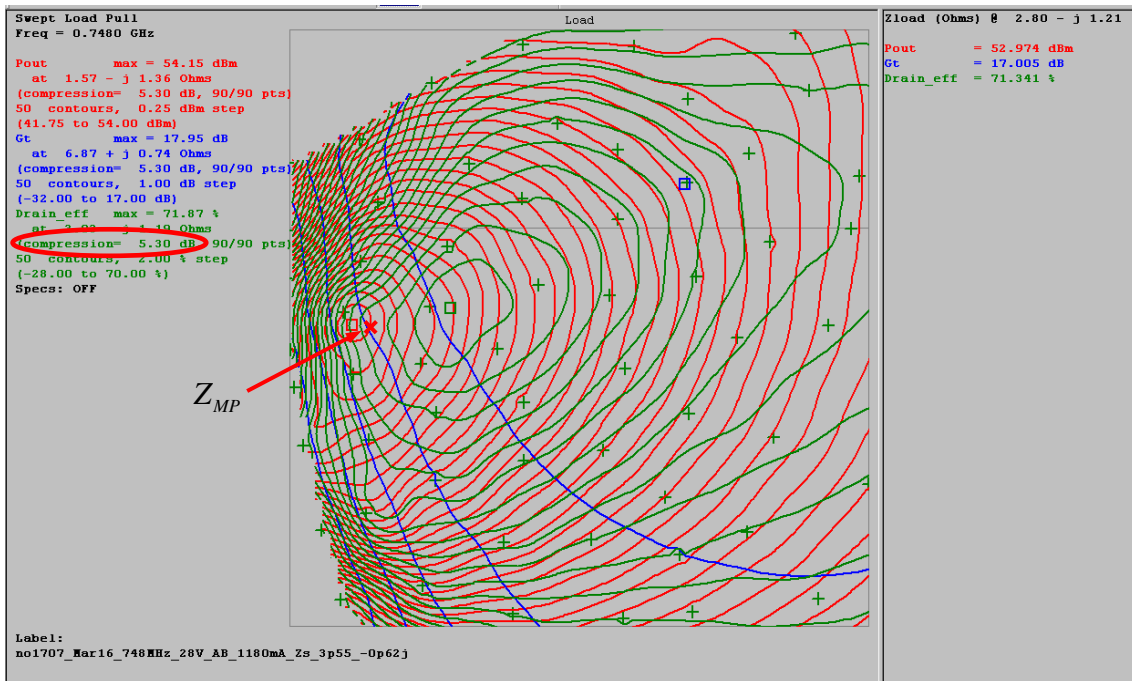
gamma_src1		gamma_ld1		Pin_av	Pout	Gt	Eff	Vinph	Voutph	T_ph
Re	Im	Re	Im	[dBm]	[dBm]	[dB]	[%]	[rad]	[rad]	[rad]
-0.8511	-0.0359	-0.9270	-0.1683	40.500	51.897	11.397	59.920	-2.486	-4.095	-1.610
-0.8511	-0.0359	-0.9270	-0.1683	41.000	51.972	10.972	60.166	-2.486	-4.100	-1.614
-0.8511	-0.0359	-0.9270	-0.1683	41.500	52.039	10.539	60.386	-2.487	-4.105	-1.618
-0.8511	-0.0359	-0.9270	-0.1683	42.000	52.099	10.099	60.586	-2.488	-4.110	-1.623
-0.8511	-0.0359	-0.9270	-0.1683	42.500	52.154	9.654	60.768	-2.488	-4.115	-1.627
-0.8511	-0.0359	-0.9270	-0.1683	43.000	52.203	9.203	60.931	-2.489	-4.119	-1.630
-0.8511	-0.0359	-0.9270	-0.1683	43.500	52.246	8.746	61.071	-2.490	-4.123	-1.634
-0.8511	-0.0359	-0.9270	-0.1683	44.000	52.283	8.283	61.185	-2.490	-4.127	-1.637
-0.8511	-0.0359	-0.9270	-0.1683	44.500	52.313	7.813	61.276	-2.491	-4.130	-1.639
-0.8511	-0.0359	-0.9270	-0.1683	45.000	52.333	7.333	61.351	-2.491	-4.133	-1.643

**Table 1: Load-pull data sample**

The first two columns in Table 1 represent the source reflection coefficient as complex numbers in Cartesian format. The next two columns represent the load reflection coefficient as such complex numbers. The available input power in  $dBm$  is shown in the fifth column. The sixth column contains the measured power delivered to the load in  $dBm$ . Gain in  $dB$ , shown in the seventh column is the difference between power delivered to the load and available input power. The efficiency shown in the eighth column is the ratio of the RF power delivered to the load and the DC power consumed, expressed as a percentage. The remaining three columns contain phase information, namely that for the input voltage, the output voltage, and their difference (that is, the phase delay), respectively.

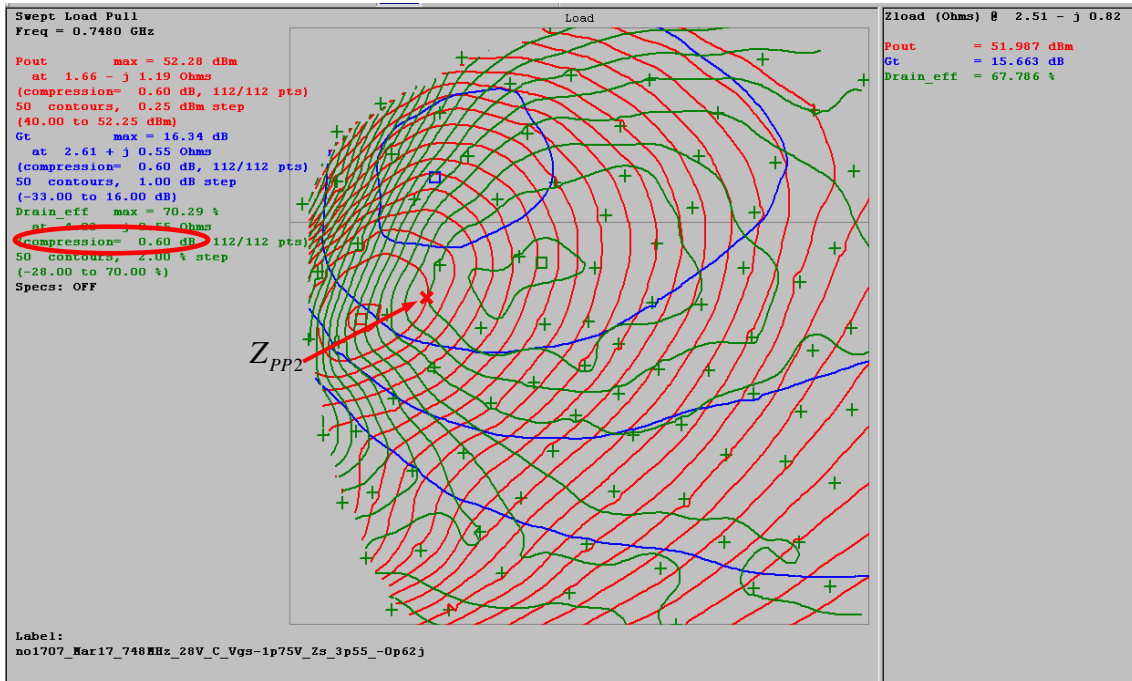


(a)

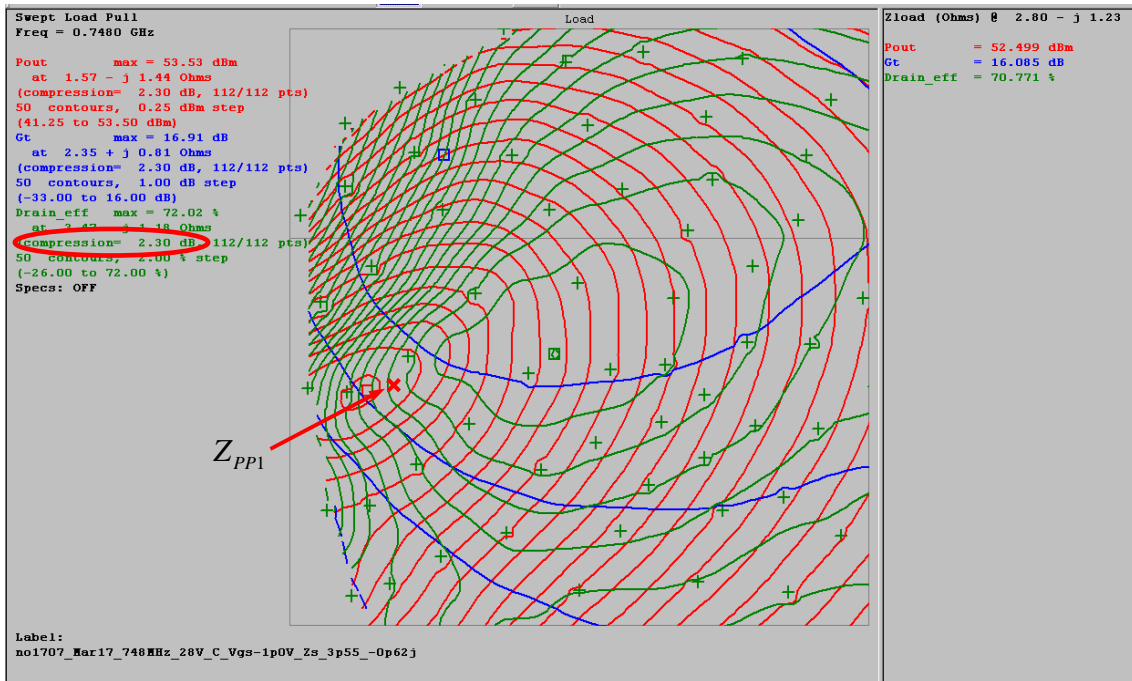


(b)

Figure 68: Class-AB constant compression load-pull contours for (a) 1dB compression and (b) 5.3dB compression



(a)



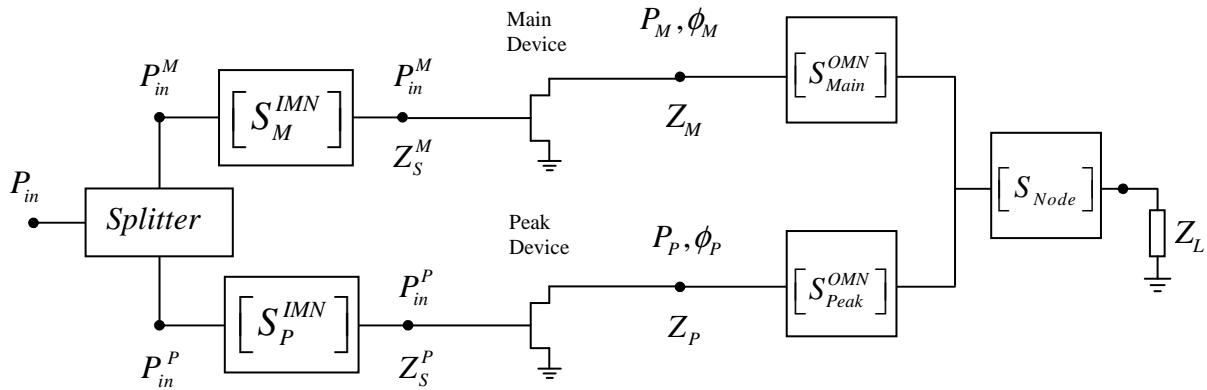
(b)

Figure 69: Class C constant compression load-pull contours for (a) 0.6dB compression and (b) 2.3dB compression

## 5.3 Two-Way Fixed Input Power Split Doherty Design

### 5.3.1 Two-Way Doherty Amplifier with Fixed Input Power split

Figure 70 shows a block diagram of a fixed-input power-split, two-way Doherty amplifier having. This architecture was introduced in Section 4.2<sup>38</sup>. a main amplifier branch and a peak amplifier branch.



**Figure 70: Block diagram of a fixed-input-conditioning power-split, two-way Doherty amplifier**

An input signal is applied to an input power splitter, which splits the input signal power, according to a fixed ratio, between the main amplifier branch and the peak amplifier branch.

For low signal power operation, the peak amplifier branch is inactive (e.g. this is achieved by biasing the peak device in class-C), such that all amplification is provided by the main amplifier branch. During high signal power operation, the peak amplifier branch is active (e.g., the signal amplitude is large enough to turn on the peak amplifier device), and so amplification is provided by both the main amplifier branch and the peak amplifier branch. The intended intermittent operation of the peak amplifier device as a function of the input power is achieved by operating it as a class-C amplifier, while the main amplifier device functions as a class-AB amplifier. To achieve higher efficiency, some of the high linearity of operation of class-A mode is traded off for efficiency by going to class-AB mode. The trade-off could be anywhere between class-A and class-B, hence,

<sup>38</sup> Note that all the Doherty amplifier configurations discussed hereafter in this thesis are the compact forms introduced in Chapter 4.

class-AB which can vary from very close to class-A to very close to class-B. This is the designer's choice. The goal of the Section 5.3 is to present the complete new design procedure for a two-way Doherty amplifier. Although it is meant as a summarising diagram, the flow chart presented in Figure 73 at the end of this section might serve as a convenient guide when reading the quantitative details.

### 5.3.2 Design of a Fixed Input Power Split Two-way Doherty Amplifier

The design of the two-way Doherty amplifier of Figure 70 focuses on three main regions of the architecture: the input power splitter, the main and peak output matching networks, and the node matching network. The output combining network (consisting of the main, peak, and node matching networks) is designed based on the combining node impedance modulation ratio<sup>39</sup>  $N_{comb}$ , which is a function of the maximum power delivered by the main and peak branches. The designer will select an appropriate value for the combining node impedance modulation ratio  $N_{comb}$  based on power and efficiency specifications. To obtain the desired value of  $N_{comb}$  the designer will use, as will be shown below, the high-compression main and peak amplifier device load-pull contours (for example,  $3dB$  for the main device and  $1dB$  for the peak device) to make a selection of loading impedances for the main and peak devices in order to realize specified maximum output power requirement. The value is not uniquely determined and could have any value in the range 1.5 to about 4. However, we will see that values ranging between about 2 and 3 turn out to be the best for use with practical devices.

The input power splitter is designed to provide input power for each device to produce output power levels that will achieve the impedance modulation range for which the node matching network was designed. Because the peak device, which is biased in class-C mode of operation, has a lower gain than the main device, and because the impedance modulation ratio may need to be greater than 2 for the amplifier to satisfy the

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<sup>39</sup> Note that this is not the same as the main device impedance modulation ratio  $N_M$  nor the peak device impedance modulation ratio  $N_P$ .

efficiency requirement at an output power level that is backed off from the amplifier's maximum power, the input power splitter generally provides unequal power splitting that steers more input power toward the peak device. The ratio of input power  $P_{IN}^P$  to the peak device, to the input power  $P_{IN}^M$  to the main device, is determined from the maximum output power provided by the main device  $P_P^M$ , the corresponding main device gain  $G^M$ , the maximum output power provided by the peak device  $P_P^P$ , and the corresponding peak device gain  $G^P$ . This is easily seen to be

$$(54) \quad \frac{P_{IN}^P}{P_{IN}^M} = \frac{\frac{P_P^P}{G^P}}{\frac{P_P^M}{G^M}} = \frac{G^M P_P^P}{G^P P_P^M}$$

The load-pull data needed for the design of the two-way Doherty amplifier has been outlined in Section 5.2. A set of high-compression (3dB or higher) class-AB load pull contours is used to select the main device loading impedance  $Z_{MP}$  with which the main device can operate in the high power regime. A set of low-compression (1dB or so) class-AB contours is used to select the main device loading impedance  $Z_{ME}$  with which the main device can operate in high-efficiency regime at low power. The impedance  $Z_{ME}$  will have a lower power associated with it; whereas, the impedance  $Z_{MP}$  may have lower efficiency associated with it. As the input power increases the main device is presented with impedance  $Z_{ME}$  until it reaches 1dB compression; at which point, the peak branch becomes active and starts modulating the load impedance of the main branch from the high-efficiency/low-power  $Z_{LME}$  point toward the impedance point  $Z_{LMP}$ <sup>40</sup> associated with high power operation, while increasing the compression of the main device whose load impedance will eventually become  $Z_{MP}$  in 3dB compression (or higher) contours. For the peak device, one set of constant-compression load-pull contours obtained under

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<sup>40</sup> Thorough out the thesis we will refer to the combining node side impedances with a subscript starting with "L" (standing for Load, e.g.  $Z_{LMP}$ ,  $Z_{LPP}$ ,  $Z_{LPOFF}$ , etc), while the corresponding device side impedances will be denoted by omitting "L" from the subscript (e.g.  $Z_{MP}$ ,  $Z_{PP}$ ,  $Z_{POFF}$ , etc)

class-C bias conditions is used, for example, high-power  $1dB$ -compression contours, as well as measurement of the off-state impedance of peak device for low-power operations during which peak device is disabled. Because a class-C device has lower gain, it will undergo lower compression. Since the peak device has lower maximum gain due to its class-C bias, it cannot be compressed too much before its gain becomes inadequate. Hence,  $1dB$  compression is considered high for the peak device.

Load-pull data is obtained for the devices that will be used in the amplifier design and construction. The devices are measured under the same (or similar) biasing and power conditions under which they are intended to be used. The measured data provides the relationship between input and the output of the active device under various loading conditions, such as those that occur in the Doherty amplifier where two branches interact at the node. The data allows us to calculate the response from the transistor based on the interactions of the branch signals at the combining node which are power dependent. The data obtained at each frequency of interest is used to characterize amplifier performance at that frequency. For each load impedance, the device (keeping the same input power conditions) will have different performance regarding output power, gain, and efficiency. The designer needs to select such device load impedances that the main and peak devices can deliver performance sufficient to meet the amplifier specifications. Load-pull data allows the designer to pick a load impedance for which the main device performance satisfies the high-power requirement ( $Z_{MP}$ ), a load impedance for which the main device performance satisfies the high-efficiency requirement at power back-off ( $Z_{ME}$ ), as well as impedances for which performance one or more peak devices satisfies the high-power requirement ( $Z_{PPn}$ ). In the design synthesis procedure, the load-pull data are plotted in constant-compression contour format to facilitate the visual selection of the impedances. This is similar to constant elevation contours in topographical maps, where it becomes easy to locate mountain peaks or plateaus. In the analysis procedure<sup>41</sup>, the load-pull data are plotted in constant-input-power contour format to facilitate location of new impedances that result from convergence calculations in the passive circuit part of the network (main matching network, peak matching network, node matching network).

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<sup>41</sup> To be discussed in Chapter 6.

Once the designer makes the impedance selection based on the amplifier specifications, subject of course to restrictions imposed by the synthesis algorithm (to ensure that the solution can be implemented), the analysis algorithm will calculate the response of the amplifier that results from the designer's selections.

The impedance modulation ratio  $N_{comb}$  of the output combining network determines the range of impedances  $Z_{node} \leq Z_{LM} \leq N_{comb} Z_{node}$  that will load the main output matching network, where  $Z_{node}$  is the impedance at combining node looking towards node matching network, and  $Z_{LM}$  is the load impedance of the main branch (defined in section 2.3), which varies between  $Z_{node}$  and  $N_{comb} Z_{node}$  as input power  $P_{in}$  increases. The combining-network impedance modulation ratio  $N_{comb}$  is defined as

$$(55) \quad N_{comb} = \frac{P_P^M + P_P^P}{P_P^M},$$

where  $P_P^M$  is the maximum output power of the main device (dependent on  $Z_{MP}$ ) and  $P_P^P$  is the maximum output power of the peak device (dependent on  $Z_{PP}$ ).  $P_P^M$  comes from the high-compression (3dB or higher usually) main device load-pull contours, while  $P_P^P$  comes from the high-compression (0.3dB to 1dB or so) peak device load-pull contours.

The value of the combining-network impedance modulation ratio  $N_{comb}$  is affected by the selection of the high-power, main impedance  $Z_{MP}$  using the main-device, 3dB (high-compression) load-pull contours and by the selection of the high-power peak impedance  $Z_{PP}$  using the peak-device 1dB (high-compression) load-pull contours, because the selection of these impedances will change the amount of power delivered by the devices.

In addition, using the main-device 1dB (low-compression) load-pull contours, the high-efficiency main impedance  $Z_{ME}$  is selected to satisfy the efficiency requirement at the power back-off level.

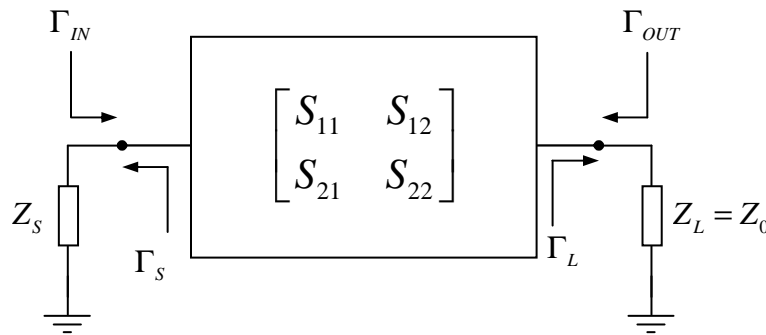
Where:

- $Z_{PP}$  is the impedance presented to the peak device during high-power operation;

- $Z_{MP}$  is the impedance presented to the main device during high-power operation;  
and
- $Z_{ME}$  is the impedance presented to the main device during average-power, high-efficiency operation.

### 5.3.3 Generic Matching Network

Figure 71 shows a generic matching network terminated in a source impedance  $Z_S$  and load impedance  $Z_L$ , and their respective voltage reflection coefficients  $\Gamma_S$  and  $\Gamma_L$ .



**Figure 71: A generic two-port network with associated notation (after [64])**

The transfer function of each of the five matching networks may be represented by an S matrix that transforms complex incident voltages into complex reflected voltages according to Equation (56) as follows:

$$(56) \quad \begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \quad [64 \text{ p.174}]$$

where  $V_1^+$  and  $V_2^+$  are the complex voltage waves incident on ports 1 and 2, respectively,  $V_1^-$  and  $V_2^-$  are the complex voltage waves reflected from ports 1 and 2, respectively, and  $S_{ij}$  are the four S-matrix parameters. From these voltages and S-parameters, the relevant impedances can be derived for matching networks, and vice-versa.

The input and output voltage reflection coefficients  $\Gamma_{IN}$  and  $\Gamma_{OUT}$  [64 p.174] for this generic matching network in Figure 71 are given by

$$(57) \quad \Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$$

and

$$(58) \quad \Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S},$$

where  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ , and  $S_{22}$  are the elements of the network S matrix. We will need (57) and (58) in Section 5.3.4.

### 5.3.4 Scattering Matrix for Input Matching Networks and Node Matching Network

Since the main and peak input matching networks and the node matching network, convert the system reference impedance  $Z_0$  (usually  $50\Omega$ ) to arbitrary known impedance, the calculations for these three networks can be done in the same way.

The main input matching network converts the output impedance of the main branch of the splitter (usually  $Z_0$ ) to the known source impedance  $Z_{SM}$  to be presented to the input of the main device. Note that the source impedance  $Z_{SM}$  is the impedance looking into the main input matching network from the main device side in Figure 70. As stated in Section 5.2, the source impedance  $Z_{SM}$  is known from the load-pull data, so the impedance conversion performed by the main input matching network is from  $Z_0$  to  $Z_{SM}$ .

The peak input matching network converts the output impedance of the peak branch of the splitter (usually  $Z_0$ ) to the known source impedance  $Z_{SP}$  to be presented to the input of peak device. Note that the source impedance  $Z_{SP}$  is the impedance looking into peak input matching network from the peak device side in Figure 70. This source

impedance  $Z_{SP}$  is also known from the load-pull data, so the impedance conversion performed by the peak input matching network is from  $Z_0$  to  $Z_{SP}$ . Going in the opposite direction, the node matching network converts a known output load impedance  $Z_L$  (usually  $Z_0$ ) to a known calculated node impedance  $Z_{node}$  at the combining node.

In essence, this impedance transformation process is the same for all three matching networks; only the target impedance changes (being either  $Z_{SM}$ ,  $Z_{SP}$ , or  $Z_{node}$ ). Referring to Figure 71, the output load impedance  $Z_L$  always equals to  $Z_0$ , and  $Z_{IN}$  always corresponds to either  $Z_{SM}$  or  $Z_{SP}$  at the respective device input, or  $Z_{node}$  at the combining node. Thus, for the main and peak input matching networks, the output load of Figure 71 corresponds to the upstream, splitter side of the network, whereas for the node matching network the output load corresponds to the output load of Figure 70 at the downstream side of the network.

We next derive some general (and known) expressions from S-parameter theory, and then indicate their application to the input matching networks and the combining node output matching network. For an output load impedance  $Z_L$  equal to the system reference impedance  $Z_0$ , the load voltage reflection coefficient  $\Gamma_L = 0$ . Substituting  $\Gamma_L = 0$  into expression (52) the expected result is

$$(59) \quad S_{11} = \Gamma_{IN}. \quad [64 \text{ p.174}]$$

In other words, the parameter  $S_{11}$  will be equal to the input voltage reflection coefficient  $\Gamma_{IN}$ , which is known from the load-pull data. In the case of a complex conjugate match,  $\Gamma_S = \Gamma'_{IN}$  and  $\Gamma_{OUT} = 0$ , where the prime indicates complex conjugation. The case of complex conjugate match is the condition that maximizes the power transfer, but other conditions can be used. In those other cases,  $\Gamma_S$  and  $\Gamma_{OUT}$  will be specified differently but the rest of the calculation is done in the same way, with results that will reflect changes in the specification of  $\Gamma_S$  and  $\Gamma_{OUT}$ . Applying the equalities  $\Gamma_S = \Gamma'_{IN}$  and  $\Gamma_{OUT} = 0$  to expression (58) yields

$$(60) \quad \Gamma_{OUT} = S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1-S_{11}\Gamma_S} = S_{22} + \frac{S_{21}S_{12}\Gamma'_{IN}}{1-\Gamma_{IN}\Gamma'_{IN}} = S_{22} + \frac{S_{21}S_{12}\Gamma'_{IN}}{1-|\Gamma_{IN}|^2} = 0.$$

Solving expression (60) for  $S_{22}$  gives

$$(61) \quad S_{22} = -\frac{S_{21}S_{12}\Gamma'_{IN}}{1-|\Gamma_{IN}|^2}.$$

Since the S matrix for a lossless, passive circuit is unitary, we have  $[S']^T = [S]^{-1}$ . In other words, the complex-conjugate transpose of a unitary S-matrix will be equal to the inverse of that S-matrix. Since the product of an S matrix and its inverse is equal to the identity matrix, multiplying  $[S']^T = [S]^{-1}$  from the left by  $[S]$  produces the well-known condition [64]

$$(62) \quad \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} S'_{11} & S'_{21} \\ S'_{12} & S'_{22} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

which of course means that

$$(63) \quad |S_{11}|^2 + |S_{12}|^2 = 1,$$

$$(64) \quad S_{11}S'_{21} + S_{12}S'_{22} = 0,$$

$$(65) \quad S'_{11}S_{21} + S'_{12}S_{22} = 0,$$

and

$$(66) \quad |S_{21}|^2 + |S_{22}|^2 = 1.$$

The matching networks are reciprocal which implies  $S_{21} = S_{12}$ , this also follows from the unitary properties of the matrix. Applying this equality together with expressions (59) and (63) yields

$$(67) \quad |S_{21}|^2 = |S_{12}|^2 = |S_{21}S_{12}| = 1 - |S_{11}|^2 = 1 - |\Gamma_{IN}|^2.$$

Expression (67) implies that

$$(68) \quad S_{21}S_{12} = |S_{21}S_{12}|e^{j\phi} = (1 - |\Gamma_{IN}|^2)e^{j\phi},$$

where  $\phi$  is the phase of the complex quantity on the left hand side, which is a function of the network electrical length and is related to the phase and time delay of the signals propagating through the network. Higher insertion phase is associated with longer delay. Since  $S_{21} = S_{12}$ , expression (68) implies that

$$(69) \quad S_{12} = S_{21} = \sqrt{1 - |\Gamma_{IN}|^2} e^{j\frac{\phi}{2}}.$$

Substituting (69) into expression (61) provides us with

$$(70) \quad S_{22} = -\frac{S_{21}S_{12}\Gamma'_{IN}}{1 - |\Gamma_{IN}|^2} = -\frac{(1 - |\Gamma_{IN}|^2)e^{j\phi}\Gamma'_{IN}}{1 - |\Gamma_{IN}|^2} = -\Gamma'_{IN}e^{j\phi}.$$

Individually, for the main input matching network, the peak input matching network, and the node matching network, the required S matrix parameters  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ , and  $S_{22}$  can be found from the input voltage reflection coefficient  $\Gamma_{IN}$  using expressions (59), (69), and (70), since  $\Gamma_{IN}$  is known from the load-pull data. The phase  $\phi$  is not constrained by our initial conditions, and it can be used, as in the case of peak input matching network, for phase equalization between the main and peak branches to ensure that currents from the main and peak branches combine at the combining node in phase.

### 5.3.5 Main Device Impedance Modulation Ratio $N_M$ Derivation

To design a properly functioning main amplifier (in the two-way Doherty amplifier) two impedance points need to be carefully selected in the main device load-pull contours to satisfy the Doherty amplifier specifications. The main-device impedance modulation ratio  $N_M$  is related to the range of impedances presented to the main device and depends on the choice of the high-power and high-efficiency main-device impedances  $Z_{MP}$  and  $Z_{ME}$ , but is independent from the high-power peak-device impedance  $Z_{PP}$ . Impedance  $Z_{ME}$  is selected from the low compression main device load-pull contours; under its loading the main device exhibits high efficiency of operation under low power conditions (and is limited to a relatively low power output). Impedance  $Z_{MP}$  is selected from the high compression main device load-pull contours; under its loading the main device is capable of providing close to maximum of output power (and will have relatively high efficiency of operation due to the high power output levels). The impedance modulation ratio  $N_M$  of the main device based on the above selection of  $Z_{MP}$  and  $Z_{ME}$  can be described in what follows.

For the high power case going, from the load toward the source,  $Z_0$  is transformed into  $Z_{MP}$ . Then using  $\Gamma_{IN} = \Gamma_{MP}$  and  $\Gamma_L = 0$  in (57) we get

$$(71) \quad \Gamma_{IN} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \Rightarrow \Gamma_{MP} = S_{11}$$

For the high efficiency case going from the load toward source, some real impedance  $Z$  (not equal to  $Z_0$ ) is transformed into  $Z_{ME}$ . Then using  $\Gamma_{IN} = \Gamma_{ME}$  and  $\Gamma_L = \Gamma$  in (57) we get

$$(72) \quad \Gamma_{IN} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \Rightarrow \Gamma_{ME} = \Gamma_{MP} + \frac{S_{21}S_{12}\Gamma}{1 - S_{22}\Gamma} \Rightarrow \Gamma_{ME} - \Gamma_{MP} = \frac{S_{21}S_{12}\Gamma}{1 - S_{22}\Gamma}$$

For the high power case going from the source toward the load,  $Z'_{MP}$  is transformed into  $Z_0$ . Then using  $\Gamma_S = \Gamma'_{MP}$  and  $\Gamma_{OUT} = 0$  in (58), with help from (67) and (71), we get

$$(73) \quad \Gamma_{OUT} = S_{22} + \frac{S_{21}S_{12}\Gamma'_{MP}}{1-S_{11}\Gamma'_{MP}} = S_{22} + \frac{(1-|\Gamma_{MP}|^2)\Gamma'_{MP}e^{j\phi}}{1-|\Gamma_{MP}|^2} = S_{22} + \Gamma'_{MP}e^{j\phi} = 0$$

and

$$(74) \quad S_{22} = -\Gamma'_{MP}e^{j\phi}$$

For the high efficiency case going from the source toward the load,  $Z'_{ME}$  is transformed into the real impedance  $Z$ . Then using  $\Gamma_S = \Gamma'_{ME}$  and  $\Gamma_{OUT} = \Gamma$  in (58) with help from (67) and (71) we get

$$(75) \quad \Gamma_{OUT} = S_{22} + \frac{S_{21}S_{12}\Gamma'_{ME}}{1-S_{11}\Gamma'_{ME}} = -\Gamma'_{MP}e^{j\phi} + \frac{(1-|\Gamma_{MP}|^2)\Gamma'_{ME}e^{j\phi}}{1-\Gamma_{MP}\Gamma'_{ME}} = \frac{\Gamma'_{ME} - \Gamma'_{MP}}{1-\Gamma_{MP}\Gamma'_{ME}}e^{j\phi} = \Gamma$$

$$(76) \quad \Gamma = \frac{\Gamma'_E - \Gamma'_P}{1 - \Gamma_P \Gamma'_E} e^{j\phi} \quad |\Gamma| = \left| \frac{\Gamma'_E - \Gamma'_P}{1 - \Gamma_P \Gamma'_E} \right| \quad N_M = \frac{1 + |\Gamma|}{1 - |\Gamma|}$$

Now that the value  $|\Gamma|$  is known in terms of user selected  $\Gamma_{MP}$  and  $\Gamma_{ME}$  we can calculate the corresponding main device impedance modulation ratio

$$(77) \quad N_M = \frac{1 + |\Gamma|}{1 - |\Gamma|} = \frac{|1 - \Gamma_{MP}\Gamma'_{ME}| + |\Gamma'_{ME} - \Gamma'_{MP}|}{|1 - \Gamma_{MP}\Gamma'_{ME}| - |\Gamma'_{ME} - \Gamma'_{MP}|},$$

where

$$(78) \quad |\Gamma| = \left| \frac{\Gamma'_{ME} - \Gamma'_{MP}}{1 - \Gamma_{MP}\Gamma'_{ME}} \right|,$$

and where the prime symbol (') represents complex conjugation, and the symbol  $\Gamma_{xx}$  represents the voltage reflection coefficient, which is related to the impedance  $Z_{xx}$  by

$$(79) \quad \Gamma_{xx} = \frac{Z_{xx} - Z_0}{Z_{xx} + Z_0},$$

where  $Z_0$  is the system reference impedance (usually 50Ω).

To design an amplifier that will yield the targeted performance, impedances  $Z_{MP}$ ,  $Z_{PP}$ , and  $Z_{ME}$  cannot be selected independently. Rather, the selections of impedances

must be such that the condition  $N_M = N_{comb}$  is satisfied. In other words,

$$N_M = \frac{1+|\Gamma|}{1-|\Gamma|} = \frac{P_P^M + P_P^P}{P_P^M} = N_{comb} = N.$$

If not, the amplifier will still work, but the achieved performance might deviate from the targeted values.

Based on the condition  $N_M = N_{comb}$ , and associated impedance selections that make this condition true, the S matrices for the main, peak, and node matching networks in the output combining network can be calculated. The S matrices can be calculated for impedance values selected even if the  $N_M = N_{comb}$  condition is not satisfied. The designer can then see the consequences of this non-ideal choice by running the analysis algorithm<sup>42</sup> and deciding whether to alter the design or keep it as is. After establishing the input power split ratio, the impedance modulation ratio, and the values of impedances  $Z_{MP}$ ,  $Z_{PP}$ , and  $Z_{ME}$ , we can proceed with the design of the input power splitter, the main and peak input matching networks, the main and peak output matching networks, and the combining node matching network as well as the determination of the delay compensation for the phase difference between the two branches. These steps are discussed in Section 5.3.6 through Section 5.3.8 except for those already dealt with in Section 5.3.4. The whole procedure is summarised by the flow chart in Figure 73 of Section 5.3.9.

### 5.3.6 S Matrix for Main Output Matching Network

The S matrix  $S^M$  for the main output matching network is given by

$$(80) \quad S^M = \begin{bmatrix} S_{11}^M & S_{12}^M \\ S_{21}^M & S_{22}^M \end{bmatrix}$$

During high-power operation, going from the combining node toward the main device, the main output matching network converts the high-power main branch load impedance  $Z_{LMP}$  into the high-power main-device impedance  $Z_{MP}$ . During high-efficiency

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<sup>42</sup> The subject of Chapter 6

operation, going from the combining node toward the main device, the main output matching network converts the high-efficiency main branch load impedance  $Z_{LME}$  into the high-efficiency main-device impedance  $Z_{ME}$ . The main-device impedances  $Z_{MP}$  and  $Z_{ME}$  are known from the load-pull data selections, the high-power main load impedance  $Z_{LMP}$  is user determined (usually  $Z_0$ ), and the high-efficiency main load impedance is  $Z_{LME} = Z_{LMP} / N_M$ .

According to (79), the respective voltage reflection coefficients  $\Gamma_{LMP}$ ,  $\Gamma_{LME}$ ,  $\Gamma_{MP}$ , and  $\Gamma_{ME}$  for the four impedances  $Z_{LMP}$ ,  $Z_{LME}$ ,  $Z_{MP}$ , and  $Z_{ME}$  can of course be calculated using

$$(81) \quad \Gamma_{LMP} = \frac{Z_{LMP} - Z_0}{Z_{LMP} + Z_0},$$

$$(82) \quad \Gamma_{LME} = \frac{Z_{LME} - Z_0}{Z_{LME} + Z_0},$$

$$(83) \quad \Gamma_{MP} = \frac{Z_{MP} - Z_0}{Z_{MP} + Z_0},$$

and

$$(84) \quad \Gamma_{ME} = \frac{Z_{ME} - Z_0}{Z_{ME} + Z_0}.$$

For the main output matching network, for high-power operation, we have (referring to Figure 71 for reminder of the definitions)

$$(85) \quad \Gamma_L = \Gamma_{LMP},$$

$$(86) \quad \Gamma_S = \Gamma'_{MP},$$

$$(87) \quad \Gamma_{IN} = \Gamma_{MP},$$

and

$$(88) \quad \Gamma_{OUT} = \Gamma'_{MLP}.$$

Substituting equations (85) and (87) into equation (57) yields

$$(89) \quad \Gamma_{MP} = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LMP}}{1 - S_{22}^M \Gamma_{LMP}}.$$

Similarly, substituting equations (86) and (88) into equation (58)

$$(90) \quad \Gamma'_{LMP} = S_{22}^M + \frac{S_{12}^M S_{21}^M \Gamma'_{MP}}{1 - S_{11}^M \Gamma'_{MP}}.$$

Referring to Figure 71, for the main output matching network in high-efficiency operation we have

$$(91) \quad \Gamma_L = \Gamma_{LME},$$

$$(92) \quad \Gamma_S = \Gamma'_{ME},$$

$$(93) \quad \Gamma_{IN} = \Gamma_{ME},$$

$$(94) \quad \Gamma_{OUT} = \Gamma'_{LME}.$$

Substituting equations (91) and (93) into equation (57) gives us

$$(95) \quad \Gamma_{ME} = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LME}}{1 - S_{22}^M \Gamma_{LME}}.$$

Similarly, substituting equations (92) and (94) into equation (58) results in

$$(96) \quad \Gamma'_{LME} = S_{22}^M + \frac{S_{12}^M S_{21}^M \Gamma'_{ME}}{1 - S_{11}^M \Gamma'_{ME}}.$$

Subtracting equation (95) from equation (89) we obtain

$$(97) \quad \Gamma_{MP} - \Gamma_{ME} = S_{12}^M S_{21}^M \left( \frac{\Gamma_{LMP}}{1 - S_{22}^M \Gamma_{LMP}} - \frac{\Gamma_{LME}}{1 - S_{22}^M \Gamma_{LME}} \right).$$

Subtracting equation (96) from equation (90) we get

$$(98) \quad \Gamma'_{LMP} - \Gamma'_{LME} = S_{12}^M S_{21}^M \left( \frac{\Gamma'_{MP}}{1 - S_{11}^M \Gamma'_{MP}} - \frac{\Gamma'_{ME}}{1 - S_{11}^M \Gamma'_{ME}} \right).$$

We next rearrange (97) to take form

$$(99) \quad S_{12}^M S_{21}^M = \frac{(\Gamma_{MP} - \Gamma_{ME})(1 - S_{22}^M \Gamma_{LMP})(1 - S_{22}^M \Gamma_{LME})}{\Gamma_{LMP} - \Gamma_{LME}}.$$

Substituting equation (99) into equation (89), and rearranging yields

$$(100) \quad S_{11}^M = \Gamma_{MP} - \frac{(\Gamma_{MP} - \Gamma_{ME})(1 - S_{22}^M \Gamma_{LME})\Gamma_{LMP}}{\Gamma_{LMP} - \Gamma_{LME}}.$$

Rearranging equation (90) allows us to write

$$(101) \quad S_{22}^M = \Gamma'_{LMP} - \frac{S_{21}^M S_{12}^M \Gamma'_{MP}}{1 - S_{11}^M \Gamma'_{MP}}.$$

It then follows that substituting equations (99) and (100) into equation (101) yields equation (102) gives (with  $S_{22}^M$  still on both sides of the equation)

$$(102) \quad S_{22}^M = \Gamma'_{LMP} - \frac{(\Gamma_{MP} - \Gamma_{ME})(1 - S_{22}^M \Gamma_{LMP})(1 - S_{22}^M \Gamma_{LME})\Gamma'_{MP}}{(\Gamma_{LMP} - \Gamma_{LME})(1 - |\Gamma_{MP}|^2) + (\Gamma_{MP} - \Gamma_{ME})(1 - S_{22}^M \Gamma_{LME})\Gamma_{LMP}\Gamma'_{MP}}.$$

Solving (102) for the matrix parameter  $S_{22}^M$  finally offers us the expression

$$(103) \quad S_{22}^M = \frac{|\Gamma_{LMP}|^2 - \Gamma'_{LMP}\Gamma_{LME} + |\Gamma_{MP}|^2 \Gamma'_{LMP}\Gamma_{LME} - |\Gamma_{LMP}|^2 \Gamma'_{MP}\Gamma_{ME} - |\Gamma_{MP}|^2 \Gamma'_{MP}\Gamma_{ME}}{\Gamma_{LMP} - \Gamma_{LME} - |\Gamma_{MP}|^2 |\Gamma_{LMP}|^2 \Gamma_{LME} - |\Gamma_{LMP}|^2 \Gamma'_{MP}\Gamma_{ME}\Gamma_{LME} - \Gamma_{LMP} |\Gamma_{MP}|^2 + \Gamma'_{MP}\Gamma_{ME}\Gamma_{LME}}.$$

Once the matrix parameter  $S_{22}^M$  is calculated using equation (103) from the voltage reflection coefficients  $\Gamma_{ME}$ ,  $\Gamma_{MP}$ ,  $\Gamma_{LMP}$ , and  $\Gamma_{LME}$  given by equations (81)-(84), and assuming that the network is reciprocal so that  $S_{21}^M = S_{12}^M$ , the remaining matrix parameters  $S_{11}^M$ ,  $S_{12}^M$ , and  $S_{21}^M$  can be calculated using equations (99) and (100).

### 5.3.7 Scattering Matrix for Peak Output Matching Network

The scattering matrix  $S^P$  for the peak output matching network is given by

$$(104) \quad S^P = \begin{bmatrix} S_{11}^P & S_{12}^P \\ S_{21}^P & S_{22}^P \end{bmatrix}$$

During high-power operation, going from the combining node toward the peak device, the peak output matching network converts the high-power peak branch load impedance  $Z_{LPP}$  into the high-power peak-device impedance  $Z_{PP}$ . During high-efficiency operation the peak device is off, going from the peak device to toward the combining node, the peak output matching network converts the peak-device off-state impedance  $Z_{POFF}$  into the off-state peak load impedance  $Z_{LPOFF}$ .

The high-power peak-device impedance  $Z_{PP}$  is known from the load-pull data selections. The high-power peak branch load impedance  $Z_{LPP}$  is a function of the user-selected, high-power main load impedance  $Z_{LMP}$  (see previous section) and is given by

$$(105) \quad Z_{LPP} = Z_{LMP} / (N_{comb} - 1).$$

The peak-device off-state impedance  $Z_{POFF}$  is directly measured from the peak device, and the off-state peak load impedance  $Z_{LPOFF}$  is given by  $Z_{LPOFF} = N_p Z_{LPP}$ , where

$$(106) \quad N_p = \frac{1 + |\Gamma|}{1 - |\Gamma|}$$

and

$$(107) \quad |\Gamma| = \left| \frac{\Gamma_{POFF} - \Gamma'_{PP}}{1 - \Gamma_{PP} \Gamma_{POFF}} \right|$$

According to equation (79), the respective voltage reflection coefficients  $\Gamma_{LPP}$ ,  $\Gamma_{LPOFF}$ ,  $\Gamma_{PP}$ , and  $\Gamma_{POFF}$  related to the four impedances  $Z_{LPP}$ ,  $Z_{LPOFF}$ ,  $Z_{PP}$ , and  $Z_{POFF}$  can be calculated using (108)-(111) as

$$(108) \quad \Gamma_{LPP} = \frac{Z_{LPP} - Z_0}{Z_{LPP} + Z_0},$$

$$(109) \quad \Gamma_{LPOFF} = \frac{Z_{LPOFF} - Z_0}{Z_{LPOFF} + Z_0},$$

$$(110) \quad \Gamma_{PP} = \frac{Z_{PP} - Z_0}{Z_{PP} + Z_0},$$

and

$$(111) \quad \Gamma_{POFF} = \frac{Z_{POFF} - Z_0}{Z_{POFF} + Z_0}.$$

Referring to Figure 71, for the peak output matching network, for high-power operation

$$(112) \quad \Gamma_L = \Gamma_{LPP},$$

$$(113) \quad \Gamma_S = \Gamma'_{PP},$$

$$(114) \quad \Gamma_{IN} = \Gamma_{PP},$$

$$(115) \quad \Gamma_{OUT} = \Gamma'_{LPP}.$$

Substituting equations (112) and (114) into equation (57) yields

$$(116) \quad \Gamma_{PP} = S_{11}^P + \frac{S_{12}^P S_{21}^P \Gamma_{LPP}}{1 - S_{22}^P \Gamma_{LPP}}.$$

Similarly, substituting equations (113) and (115) into equation (58) we get

$$(117) \quad \Gamma'_{LPP} = S_{22}^P + \frac{S_{12}^P S_{21}^P \Gamma'_{PP}}{1 - S_{11}^P \Gamma'_{PP}}.$$

Referring to Figure 71, for the peak output matching network, for high-efficiency operation we have

$$(118) \quad \Gamma_L = \Gamma'_{LPOFF},$$

$$(119) \quad \Gamma_S = \Gamma_{POFF},$$

$$(120) \quad \Gamma_{IN} = \Gamma'_{POFF},$$

$$(121) \quad \Gamma_{OUT} = \Gamma_{LPOFF},$$

Substituting equations (118) and (120) into equation (57) yields

$$(122) \quad \Gamma'_{POFF} = S_{11}^P + \frac{S_{12}^P S_{21}^P \Gamma'_{LPOFF}}{1 - S_{22}^P \Gamma'_{LPOFF}}.$$

Similarly, substituting equations (119) and (121) into equation (58) gives us

$$(123) \quad \Gamma_{LPOFF} = S_{22}^P + \frac{S_{12}^P S_{21}^P \Gamma_{POFF}}{1 - S_{11}^P \Gamma_{POFF}}.$$

Subtracting equation (122) from equation (116) provides the expression

$$(124) \quad \Gamma_{PP} - \Gamma'_{POFF} = S_{12}^P S_{21}^P \left( \frac{\Gamma_{LPP}}{1 - S_{22}^P \Gamma_{LPP}} - \frac{\Gamma'_{LPOFF}}{1 - S_{22}^P \Gamma'_{LPOFF}} \right).$$

We then rearrange equation (124) to get

$$(125) \quad S_{12}^P S_{21}^P = \frac{(\Gamma_{PP} - \Gamma'_{POFF})(1 - S_{22}^P \Gamma_{LPP})(1 - S_{22}^P \Gamma'_{LPOFF})}{\Gamma_{LPP} - \Gamma'_{LPOFF}}.$$

Substituting Equation (125) into equation (116), and rearranging, leads to

$$(126) \quad S_{11}^P = \Gamma_{PP} - \frac{(\Gamma_{PP} - \Gamma'_{POFF})(1 - S_{22}^P \Gamma'_{LPOFF}) \Gamma_{LPP}}{\Gamma_{LPP} - \Gamma'_{LPOFF}}.$$

Rearranging equation (123) yields equation (127) allows us to write

$$(127) \quad S_{22}^P = \Gamma_{LPOFF} - \frac{S_{21}^P S_{12}^P \Gamma_{POFF}}{1 - S_{11}^P \Gamma_{POFF}}.$$

Substituting equations (125) and (126) into equation (127) yields

$$(128) \quad S_{22}^P = \Gamma_{LPOFF} - \frac{(\Gamma_{PP} - \Gamma'_{POFF})(1 - S_{22}^P \Gamma_{LPP})(1 - S_{22}^P \Gamma'_{LPOFF}) \Gamma_{POFF}}{(\Gamma_{LPP} - \Gamma'_{LPOFF})(1 - \Gamma_{PP} \Gamma_{POFF}) + (\Gamma_{PP} - \Gamma'_{POFF})(1 - S_{22}^P \Gamma'_{LPOFF}) \Gamma_{LPP} \Gamma_{POFF}}.$$

Solving equation (128) for the matrix parameter  $S_{22}^P$  finally yields the result

(129)

$$S_{22}^P = \frac{\Gamma_{PP}\Gamma_{POFF}|\Gamma_{LPOFF}|^2 - |\Gamma_{LPOFF}|^2 - \Gamma_{LPP}\Gamma_{LPOFF}|\Gamma_{POFF}|^2 + \Gamma_{LPP}\Gamma_{LPOFF} + |\Gamma_{POFF}|^2 - \Gamma_{PP}\Gamma_{POFF}}{\Gamma_{LPP}\Gamma_{POFF}\Gamma_{PP}|\Gamma_{LPOFF}|^2 - \Gamma_{LPP}|\Gamma_{POFF}|^2|\Gamma_{LPOFF}|^2 + \Gamma_{LPP} - \Gamma'_{LPOFF} - \Gamma_{LPP}\Gamma_{PP}\Gamma_{POFF} + |\Gamma_{POFF}|^2\Gamma'_{LPOFF}}$$

Once the matrix parameter  $S_{22}^P$  is calculated using equation (129) from the voltage reflection coefficients  $\Gamma_{PP}$ ,  $\Gamma_{POFF}$ ,  $\Gamma_{LPP}$ , and  $\Gamma_{LPOFF}$  given by equations (108)-(111), and assuming that the network is reciprocal such that  $S_{21}^P = S_{12}^P$ , the remaining matrix parameters  $S_{11}^P$ ,  $S_{12}^P$ , and  $S_{21}^P$  can be calculated using equations (125) and (126).

### 5.3.8 Network Phase Delay

After determining the proper input power split between the main and peak branches, and the S matrices for all five of the different matching networks in the amplifier, what remains to be determined is the phase delay for each branch.

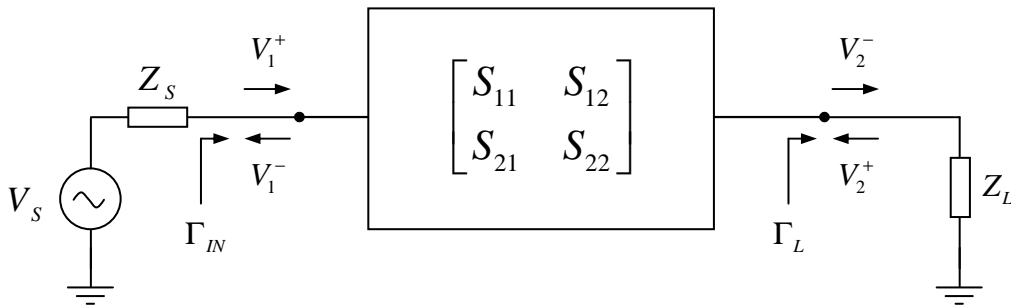
Contributions to the phase delay in the main branch come from the main input matching network loaded by the input impedance of the main amplifier device (biased in class-AB), the main device itself, and the main output matching network terminated by the main branch load impedance looking into the combining node away from the main output matching network. Recall that the main branch load impedance is a function of the main device output power  $P_M$ , the peak device output power  $P_p$ , the combining node impedance  $Z_{node}$ , and the off-state peak load impedance  $Z_{LPOFF}$ .

Contributions to the phase delay in the peak branch come from the peak input matching network loaded by the input impedance of the peak amplifier device (biased in class-C), the peak device itself, and the peak output matching network terminated by the peak branch load impedance looking into the combining node away from the peak output matching network. The peak branch load impedance is of course also a function of the main device output power  $P_M$ , the peak device output power  $P_p$ , the combining node impedance  $Z_{node}$ , and off-state peak load impedance  $Z_{LPOFF}$ .

In a typical application, the goal is to achieve a prescribed level of phase matching between the main and peak branches. Since there is no guarantee that the phase

delays from the two branches will automatically fulfill such a condition, one of the two branches can be additionally delayed inserting an input phase offset line (the function of which will be subsumed into the corresponding input matching network) or a phase shifter<sup>43</sup>. The phase delay contributions of amplifier active devices are measured during the load-pull process. The phase delay contribution from the individual passive two-port networks characterized by their known S matrices can be calculated since the load impedances are known, this we next show. Although the derivation is elementary, we have not found it written down explicitly anywhere, and it is needed in the less-elementary derivations that follow.

Figure 72 shows a generic matching network having input port connected to a generator having impedance  $Z_S$  and output port terminated in an output load having impedance  $Z_L$  with corresponding voltage reflection coefficient  $\Gamma_L$ , where generator is applying complex voltage signal  $V_S$ . The input voltage reflection coefficient  $\Gamma_{IN}$  for matching network is given by previous equation (79), where  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ , and  $S_{22}$  are the coefficients of the S matrix of the matching network.



**Figure 72: A generic two-port matching network with associated notation**

A complex voltage wave  $V_n$  at a port  $n$  of a matching network is given by

$$(130) \quad V_n = V_n^+ + V_n^- \quad [64 \text{ p.174}]$$

<sup>43</sup> Or by means of digital signal processing in case of independent input to the main and peak branches.

where  $V_n^+$  is the voltage wave heading towards the matching network and incident on port  $n$ , and  $V_n^-$  is the voltage wave reflected from port  $n$  and heading away from the matching network.

The input voltage reflection coefficient  $\Gamma_{IN}$  is by definition:

$$(131) \quad \Gamma_{IN} = \frac{V_1^-}{V_1^+}.$$

Similarly, the load voltage reflection coefficient  $\Gamma_L$  is by definition

$$(132) \quad \Gamma_L = \frac{V_2^+}{V_2^-}.$$

Substituting equation (131) into equation (130) for Port 1 yields

$$(133) \quad V_1 = V_1^+ + V_1^- = V_1^+ (1 + \Gamma_{IN}).$$

Rearranging Equation (79) for impedance  $Z_{IN}$  produces

$$(134) \quad Z_{IN} = Z_0 \frac{1 + \Gamma_{IN}}{1 - \Gamma_{IN}}$$

Substituting equation (57) into equation (134) gives us

$$(135) \quad Z_{IN} = Z_0 \frac{(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{12}S_{21}\Gamma_L}{(1 - S_{11})(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L}$$

The relationship between the voltage wave  $V_1$  at Port 1 and the source voltage wave  $V_S$  of the input RF signal is then

(136)

$$V_1 = \frac{Z_{IN}}{Z_{IN} + Z_S} V_S = \frac{Z_0 [(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L] V_S}{Z_0 [(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L] + Z_S [(1 - S_{11})(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_L]}$$

Substituting equation (57) into equation (133) on the other hand gives

$$(137) \quad V_1 = V_1^+ + V_1^- = V_1^+ (1 + \Gamma_{IN}) = V_1^+ \frac{(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L}$$

Substituting  $V_1$  from equation (137) in place of  $V_1$  in equation (136) and solving for  $V_1^+$  yields the expression

$$(138) \quad V_1^+ = \frac{Z_0(1 - S_{22}\Gamma_L)V_S}{Z_0[(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L] + Z_S[(1 - S_{11})(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_L]}$$

From the relationship  $V_2^- = S_{21}V_1^+ + S_{22}V_2^+$ , and the definition (132), we obtain

$$(139) \quad V_2^- = \frac{S_{21}V_1^+}{1 - S_{22}\Gamma_L}.$$

Substituting the expression for  $V_1^+$  from the equation (138) into equation (139) provides

$$(140) \quad V_2^- = \frac{S_{21}V_1^+}{1 - S_{22}\Gamma_L} = \frac{Z_0S_{21}V_S}{Z_0[(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L] + Z_S[(1 - S_{11})(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_L]}$$

The definition (132) along with (140), gives

$$(141) \quad V_2^+ = \Gamma_L V_2^- = \frac{Z_0S_{21}\Gamma_L V_S}{Z_0[(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L] + Z_S[(1 - S_{11})(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_L]}$$

Substituting equations (140) and (141) into equation (130) for Port 2 yields

$$(142) \quad V_2 = V_2^+ + V_2^- = \frac{Z_0S_{21}(1 + \Gamma_L)V_S}{Z_0[(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L] + Z_S[(1 - S_{11})(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_L]}$$

Dividing equation (142) by equation (136) produces

$$(143) \quad \frac{V_2}{V_1} = \frac{S_{21}(1 + \Gamma_L)}{(1 + S_{11})(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L} = \frac{S_{21}(1 + \Gamma_L)}{1 + S_{11} - (S_{22} + S_{11}S_{22} - S_{21}S_{12})\Gamma_L}$$

this complex ratio of voltages can be represented as

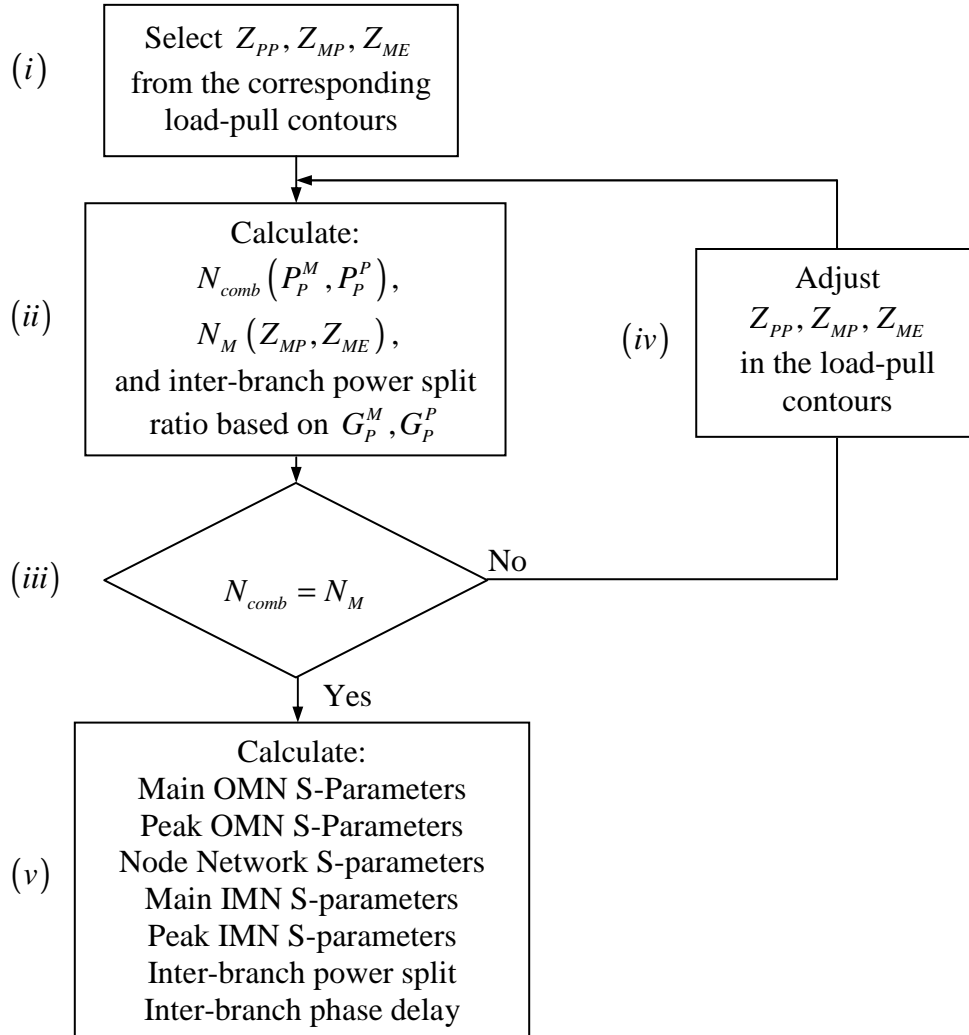
$$(144) \quad \frac{V_2}{V_1} = \left| \frac{V_2}{V_1} \right| e^{j(\phi_2 - \phi_1)}$$

where  $\phi_1$  is the phase of the voltage wave at Port 1 and  $\phi_2$  is the phase of the voltage wave at Port 2. Substitution of (144) into (143) finally gives us

$$(145) \quad \left| \frac{V_2}{V_1} \right| e^{j(\phi_2 - \phi_1)} = \left| \frac{S_{21}(1 + \Gamma_L)}{1 + S_{11} - (S_{22} + S_{11}S_{22} - S_{21}S_{12})\Gamma_L} \right| e^{j\phi}$$

where the phase delay  $\Delta\phi = \phi_2 - \phi_1 = \phi$  is the phase delay of the matching network. Since the S matrices of the five matching networks in the amplifier became known during the design process, equation (145) can be used to determine the phase delay across each matching network. Expression (145) will be used in Section 5.3.9 and Section 6.3

### 5.3.9 Design Technique for a Two-Way Doherty Amplifier



**Figure 73: Two-way Doherty design synthesis procedure flow diagram<sup>44</sup>**

Figure 73 shows a flow diagram that summarises the design technique for the two-way Doherty amplifier of Figure 70. The procedure has been implemented in software.

<sup>44</sup> Impedances  $Z_{PP}$  and  $Z_{MP}$  are associated with the peak device high output power  $P_P^P$  and the main device high output power  $P_M^P$  respectively

The main and peak input matching networks are designed using previously described technique (Section 5.3.4) in accordance with the respective values of the source impedances corresponding to those under which the devices were load-pulled. The combining node matching network is designed based on selected node impedance using the previously described technique (Section 5.3.4). Based on the device load-pull contours the designer decides how the power contributions are split between the main and peak devices under the maximum power conditions. Once the input power split that satisfies requirements for maximum power levels is determined, it remains fixed. The impedance for the maximum peak power  $Z_{PP}$  may also remain fixed throughout the remainder of the design procedure.

An iterative loop is implemented to determine the main and peak impedance values  $Z_{PP}$ ,  $Z_{MP}$ , and  $Z_{ME}$  that satisfy the condition that the node impedance modulation ratio  $N_{comb}$  at the combining node is equal to the main device impedance modulation ratio  $N_M$  between  $Z_{MP}$  and  $Z_{ME}$ .

First we initialize the values for the three impedances  $Z_{PP}$ ,  $Z_{MP}$ , and  $Z_{ME}$ <sup>45</sup> from the corresponding load-pull contours [Figure 73 block (i)]. These initial selections are made by educated guesses based on the device load-pull performance and the amplifier specifications. For example, if we need to design a 200W amplifier, we may start with an impedance  $Z_{MP}$  for which the main device has output power capability of 100W and an impedance  $Z_{PP}$  for which the peak device has output power capability of 100W. There are multiple impedances that satisfy this power condition, but the resulting amplifiers may substantially differ in gain and efficiency, and so an iterative process of further selection is used. The power ratio between the main and peak device may change, which will lead to further iterations in the selection process.

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<sup>45</sup> In the existing approach to the design of two-way amplifiers  $Z_{MP}$  is selected from the 1dB load-pull contours (since those are readily available from the device vendors),  $Z_{PP}$  is assumed equal to  $Z_{MP}$  due to lack of class-C load-pull data,  $Z_{ME}$  is also selected from 1dB load-pull contours, and input split is assumed to be 3dB. These assumptions are not consistent and there is no iterative process to correct the issue in the design phase, the inconsistencies will become apparent during the prototype phase.

The node impedance modulation ratio  $N_{comb}$  and the main device impedance modulation ratio  $N_M$  are calculated using equations (55) and (77), respectively [Figure 73 block (ii)].

Then one determines whether the node impedance modulation ratio  $N_{comb}$  sufficiently matches the main device impedance ratio  $N_M$ , to within a specified threshold percentage [Figure 73 block (iii)]. If not, then processing continues, where one or more of the three impedances  $Z_{PP}$ ,  $Z_{MP}$ , and  $Z_{ME}$  are adjusted using the corresponding load-pull contours (Figure 73 block (iv)). In the software that has been developed to implement this design procedure the impedances  $Z_{PP}$ ,  $Z_{MP}$ , and  $Z_{ME}$  are moved in the impedance space of the load-pull contours by means of user-controlled cursors. Moving a cursor in the corresponding load-pull contour plot will alter the value of the selected impedance thus effecting the change in the associated output power, gain and efficiency, which will cause the algorithm to re-evaluate matching network S-parameter values, values of  $N_{comb}$ ,  $N_M$ , and all other parameters of the circuit that are dependent on these impedances and the transistor performance parameters from the load-pull data associated with these impedances. Processing then returns to determine the impedance modulation ratio  $N_{comb}$  and the main device impedance modulation ratio  $N_M$  using the updated impedances.

When it is determined that the node impedance modulation ratio  $N_{comb}$  sufficiently close in value to the main device impedance modulation ratio  $N_M$ , processing proceeds to determine the S matrices for the main and peak output matching networks, the inter-branch power split (implemented by power splitter), and the inter-branch phase delay based on the final values for the three impedances  $Z_{PP}$ ,  $Z_{MP}$ , and  $Z_{ME}$  determined by using the techniques described previously [Figure 73 block (v)] which completes the design procedure.

The analysis procedure to be described in Chapter 6 has also been implemented in software, and so the resulting amplifier performance (to be shown in Section 6.3.2 for eight different two-way Doherty amplifiers designed via the above procedure) can be viewed immediately.

## 5.4 Two-Way Controlled Main Device Compression Doherty Design

In general the fixed-input-power-split implementation of the Doherty amplifier discussed in Section 5.3 allows us to provide the ideal input power split ratio for the nonlinear active devices in the Doherty amplifier at only one output power level  $P_{out}$  due to RF hardware implementation of the input power splitter, which is a linear passive circuit whose power splitting ratio is independent of the power level. The power splitting ratio will vary with frequency as expected with a all distributed circuits. The phase compensation necessary to ensure that signals from the main and peak branches combine constructively (in-phase) is implemented using passive phase offset transmission lines. The deviations from the ideal power split and phasing for every output power level will result in lower linearity due to increased active device gain compression and lower efficiency due to partial destructive combining of the signals.

In the fixed-input-power-split Doherty amplifier design, based on power, symmetry, gain and gain flatness considerations, an input power split ratio and phase offset that will result in certain gain compression state of the devices are selected. The peak device needs to be biased in class-C to prevent it from being active while input power is low, however this limits the peak device maximum achievable gain (Figure 74)<sup>46</sup>. There is a trade-off between gain flatness/linearity and efficiency. The compression of the devices is only characterized by fixed upper limit but the compression behaviour below the limit is out of designer's control.

To remedy the above-mentioned issues of the fixed input power split Doherty amplifier the controlled main device compression two-way Doherty amplifier is introduced as shown in Figure 75. Figure 74 reveals how the gain of the main and peak devices affects the overall gain of the Doherty amplifier. The main device provides the bulk of the gain, whereas the peak device improves the gain linearity by modulating the load impedance of the main branch thus lowering the compression the main device would otherwise undergo. The main device undergoes gain compression and the peak device

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<sup>46</sup> The gain performance of a two-way Doherty amplifier shown in Figure 74 is obtained using analysis techniques described in Chapter 6

exhibits the gain expansion. By properly biasing and exciting the peak device the rate of main device gain compression can be matched by the rate of the peak device expansion resulting in linear gain of the Doherty amplifier. Since main and peak device of the amplifier in Figure 75 have inputs whose amplitude and phase can be adjusted independently, constructive combining can be achieved at any power level, the peak device can be biased in class-B (thus increasing its gain) and power split between the devices can be such that the overall gain of the Doherty amplifier is linear.

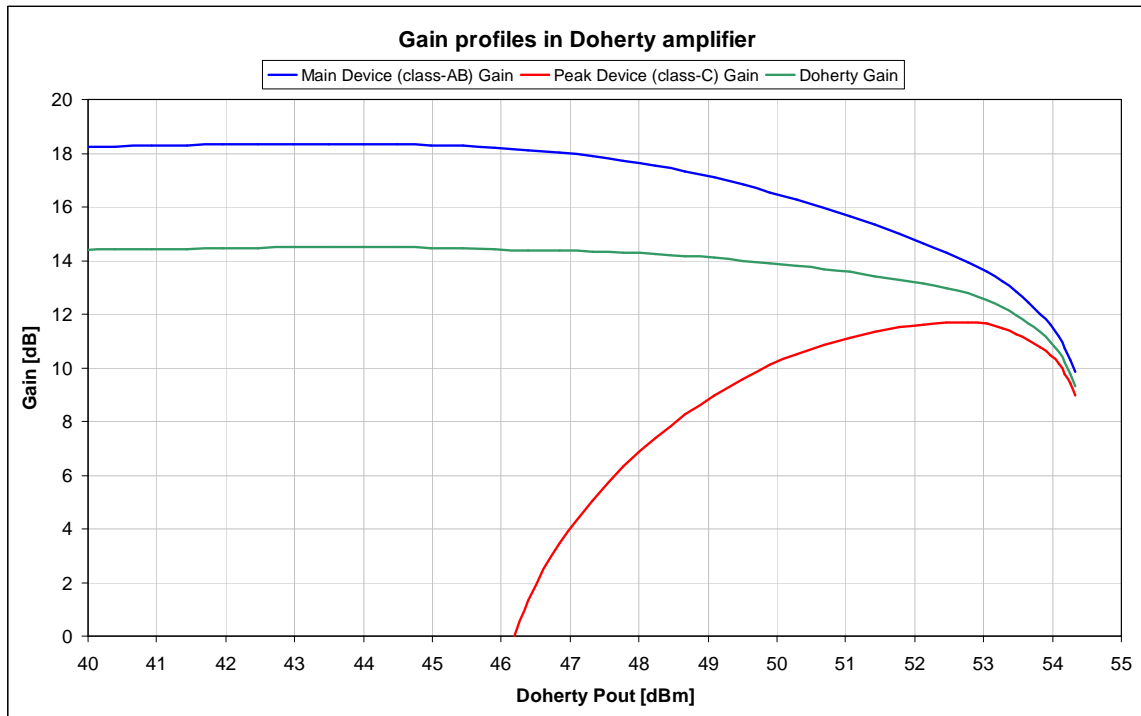
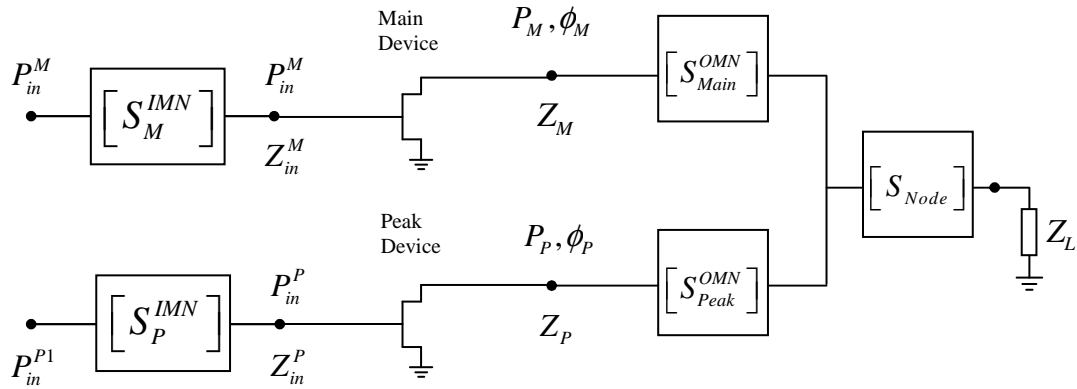


Figure 74: Gain profiles in a two-way Doherty amplifier



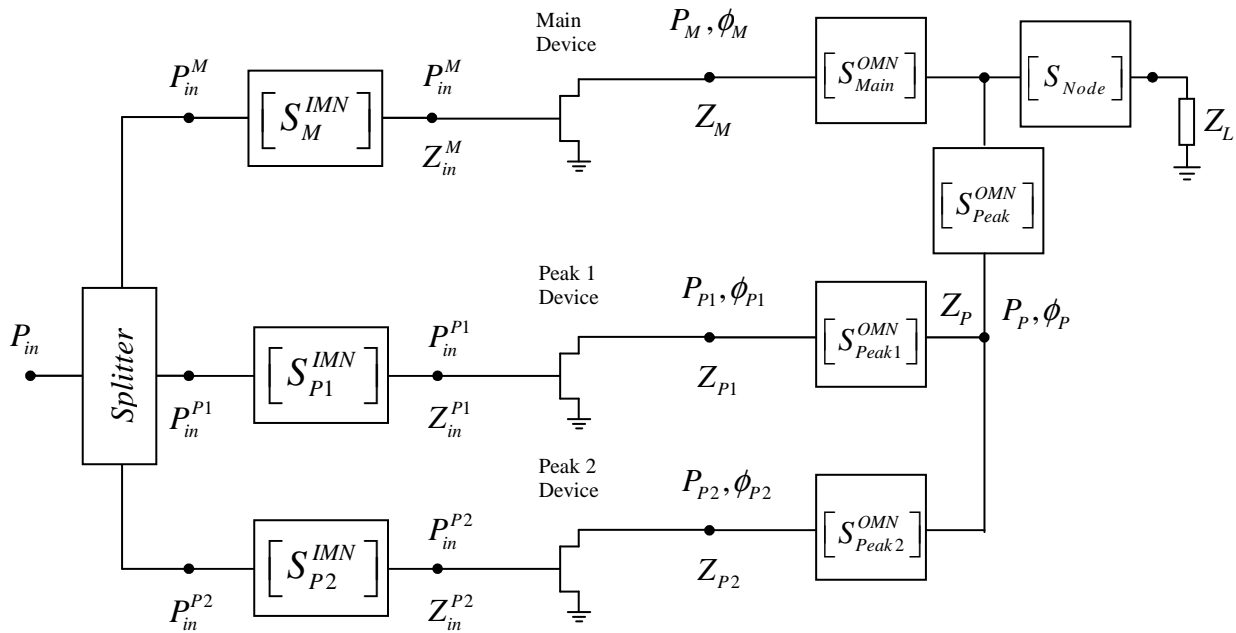
**Figure 75: Block diagram of a dynamic-input-conditioning power-split two-way Doherty amplifier**

The criteria for impedance selection remains the same as previously described in Section 5.3.2 but the compression level of the main device high power load-pull contours can be lower, and the compression state of the main device can be controlled which will result in improved linearity of the Doherty amplifier. As the main device starts to compress the peak device is excited with just enough input signal that would supply enough additional power and gain expansion from the peak device to prevent the Doherty amplifier gain from being compressed, and thus maintaining the linearity and spectral integrity of the output signal.

By having the independently adjustable input amplitude and phase for the main and peak device input signals the linearity performance and in-phase combining of the signals at the combining node where the two branches of the amplifier meet can be maintained over frequency better than was the case of the fixed input power split amplifier. The amplitude ratio and phase relationship between main and peak device branches over output power and frequency ranges will be determined during the analysis portion of the amplifier design process, in particular in Section 6.3.2.

## 5.5 Three-Way, Fixed-Input-Power-Split, Doherty Design

Figure 76 shows a block diagram of a fixed-input-power-split, three-way Doherty amplifier having a main amplifier branch and two peak amplifier branches connected to the main branch through a common peak network.



**Figure 76: Block diagram of a fixed-input-conditioning power-split, three-way Doherty amplifier**

Main amplifier branch consists of a cascade of a main input matching network, a main amplifier device, and a main output matching network. The first peak amplifier branch consists of a cascade of a peak input matching network, the first peak amplifier device, and a peak output matching network. The second peak amplifier branch consists of a cascade of a peak input matching network, the second peak amplifier device, and a peak output matching network. The common peak network interconnects the two peak branches with the main branch and the node network as shown in Figure 76. An input signal is applied to a three-way input power splitter, which splits the input signal power according to fixed ratios between the main amplifier branch and two peak amplifier branches. Output signals from the two peak branches are combined at the peak combining node into a common peak signal which is then combined with the main branch signal at

the main combining node, and the resulting combined signal is delivered to the output load through node matching network.

For low signal power operation, both peak amplifier branches are inactive (e.g., this is achieved by biasing peak devices in class-C), such that all amplification is provided by main amplifier branch. During intermediate signal power operation, the first peak amplifier branch is active (e.g., the signal amplitude is large enough to turn on the first peak amplifier device) while the second peak branch remains inactive (due to deeper class-C bias compared to the first device), such that amplification is provided by both main amplifier branch and the first peak amplifier branch. During the high power of operation all branches are active and contribute to overall amplification. The intended intermittent operation of the peak amplifier devices as a function of the input power is achieved by operating them in two different as class-C regimes, while main amplifier device functions as a class-AB amplifier.

The design of the three-way Doherty amplifier of Figure 76 focuses on three main regions of the architecture: input power splitter, main and peak output matching networks (consisting of four S parameter blocks), and the node matching network. The output combining network (consisting of the main, first peak, second peak, common peak and node matching networks) is designed based on the main combining node impedance modulation ratio  $N_{comb}$ , and what we have called the peak combining node impedance modulation ratio  $N_{Pcomb}$ , which are functions of the maximum power delivered by the main and peak branches  $P_P^M$ ,  $P_P^{P1}$  and  $P_P^{P2}$  respectively. The impedance modulation ratios are selected using the high-compression main and peak amplifier device load-pull contours (for example, 5dB for the main device and 3dB for the first peak device and 1dB for the second peak device) in order to realize the given specification of maximum output power requirements. The designer selects an appropriate value for the impedance modulation ratios  $N_{comb}$  and  $N_{Pcomb}$  based on the power and efficiency specifications. The values of these ratios are not uniquely determined and could have any value in the range from about 1.5 to about 4 for the main impedance modulation ratio  $N_{comb}$ , and from about 1.5 to about 3 for the peak impedance modulation ratio  $N_{Pcomb}$ . Since the

main and peak devices operate under different biasing conditions, they will have different gains at different power levels.

The input power splitter is designed to provide input power for each device to produce output power levels that will achieve the impedance modulation range for which the combining node matching network was designed. Because the peak devices, which are biased in class-C mode of operation, have a lower gain than the main device, and because the main impedance modulation ratio is greater than 2 for the amplifier to satisfy the efficiency requirement at an output power level that is backed off from the amplifier's maximum power, the input power splitter generally provides unequal power splitting that steers more input power toward the peak devices. The input power for each device is determined in terms of the maximum power provided by the main device  $P_p^M$ , the corresponding main device gain  $G_p^M$ , the maximum power provided by the first peak device  $P_p^{P1}$ , its corresponding gain  $G_p^{P1}$ , the maximum power provided by the second peak device  $P_p^{P2}$ , and its corresponding gain  $G_p^{P2}$ , which are related via

$$(146) \quad P_{IN}^M = P_{IN} \frac{P_p^M G_p^{P1} G_p^{P2}}{P_p^M G_p^{P1} G_p^{P2} + P_p^{P1} G_p^M G_p^{P2} + P_p^{P2} G_p^M G_p^{P1}},$$

$$(147) \quad P_{IN}^{P1} = P_{IN} \frac{P_p^{P1} G_p^M G_p^{P2}}{P_p^M G_p^{P1} G_p^{P2} + P_p^{P1} G_p^M G_p^{P2} + P_p^{P2} G_p^M G_p^{P1}},$$

and

$$(148) \quad P_{IN}^{P2} = P_{IN} \frac{P_p^{P2} G_p^M G_p^{P1}}{P_p^M G_p^{P1} G_p^{P2} + P_p^{P1} G_p^M G_p^{P2} + P_p^{P2} G_p^M G_p^{P1}}.$$

At least four sets of load-pull contours are used at each frequency of interest. For the main device, two sets of constant-compression load-pull contours are used, for example, high-compression (5dB compression or higher) load-pull contours for selection of the high-power impedance  $Z_{MP}$  and low-compression (circa 1dB compression) load-pull contours for the high-efficiency impedance  $Z_{ME}$  that are obtained for the main device operating under class-AB bias conditions.

For each of the peak devices, one set of constant-compression load-pull contours obtained under two different class-C bias conditions is used to obtain high-power impedances  $Z_{PP1}$  and  $Z_{PP2}$ , for example, high-power, 3dB-compression contours for the first peak device and 1dB compression contours for the second peak device, as well as measurement of the off-state impedance ( $Z_{P1OFF}$ , and  $Z_{P2OFF}$ ) for each of the peak devices for low-power operations during which peak devices are inactive. Because class-C biased devices have lower gain, they will undergo lower compression. Since peak devices have lower maximum gain due to their class-C bias, they cannot be compressed too much before their gain becomes inadequate. Hence, 1dB to 3dB compressions are considered high for the peak devices.

Load-pull data is obtained for the devices that will be used in the amplifier design and construction. The devices are measured under the same (or similar) biasing and power conditions under which they are intended to be used. The measured data provides the relationship between input and the output of the active device under various loading conditions, such as those that occur in the Doherty amplifier where multiple branches interact at multiple nodes. The data allows us to calculate the responses from transistors based on the interactions of the branch signals at combining nodes. The data obtained at each frequency of interest is used to characterize amplifier performance at that frequency. Load-pull data allows the designer to pick an impedance  $Z_{MP}$  that satisfies the high-power requirement for the main device, an impedance  $Z_{ME}$  that satisfies the high-efficiency requirement at power back-off for the main device, as well as impedances  $Z_{PPn}$  that satisfy the high-power requirement for one or more peak devices.

In the design synthesis procedure, the load-pull data are plotted in constant-compression contour format to facilitate the visual selection of the impedances. In the analysis procedure, the load-pull data are plotted in constant-input-power contour format to facilitate location of new impedances that result from convergence calculations in the passive circuit part of the combining network (the main matching network, peak matching networks, the node matching network). Once the designer makes the impedance selection based on amplifier specifications and subject to restrictions imposed by the synthesis algorithm (to ensure that the solution can be implemented), the analysis

algorithm<sup>47</sup> will calculate the response of the amplifier that results from the designer's selections. The impedance selection consists of choosing the following:

- $Z_{PP2}$  the impedance presented to the second peak device during high-power operation;
- $Z_{PP1}$  the impedance presented to the first peak device during high-power operation;
- $Z_{MP}$  the impedance presented to the main device during high-power operations;  
and
- $Z_{ME}$  the impedance presented to the main device during average-power, high-efficiency operation.

The main combining node impedance modulation ratio  $N_{comb}$  of the output combining network determines the range of impedances  $Z_{node} \leq Z_{LM} \leq N_{comb}Z_{node}$  that will load the main output matching network, where  $Z_{node}$  is the impedance at combining node looking towards node matching network, and  $Z_{LM}$  is the load impedance of the main branch, which varies between  $Z_{node}$  and  $N_{comb}Z_{node}$  as input power  $P_{in}$  increases. The main combining node impedance modulation ratio  $N_{comb}$  is defined as

$$(149) \quad N_{comb} = \frac{P_P^M + P_{P1}^P + P_{P2}^P}{P_P^M},$$

where  $P_P^M$  is the maximum output power of the main device,  $P_{P1}^P$  and  $P_{P2}^P$  are the maximum output power of the first and second peak device respectively.  $P_P^M$  comes from the high-compression (5dB or higher usually) main device load-pull contours by selecting appropriate value of  $Z_{MP}$ ,  $P_{P1}^P$  comes from the high-compression (around 3dB) first peak device load-pull contours by selecting appropriate value of  $Z_{PP1}$ , while  $P_{P2}^P$  comes from

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<sup>47</sup> Described in Chapter 6

the high-compression (0.3dB to 1dB or so) second peak device load-pull contours by selecting appropriate value of  $Z_{PP2}$ .

The value of the main combining node impedance modulation ratio  $N_{comb}$  is affected by the selection of the high-power, main impedance  $Z_{MP}$  using the main-device, 3dB (high-compression) load-pull contours and by the selection of the high-power peak impedance  $Z_{PP1}$  and  $Z_{PP2}$  using the first peak-device 3dB (high-compression) load-pull contours and the second peak device 1dB (high-compression) load-pull contours, because the selection of these impedances will change the amount of power delivered by the devices. In addition, using the main-device 1dB (low-compression) load-pull contours, the high-efficiency main impedance  $Z_{ME}$  is selected to satisfy the main device efficiency requirement at the power back-off level.

The main combining node impedance modulation ratio  $N_{comb}$  determines the range of impedances  $Z_{node} \frac{N_{comb}}{N_{comb} - 1} \leq Z_{LP} < OC$ <sup>48</sup> that will load the common peak output matching network, where  $Z_{node}$  is the impedance at the combining node looking towards node matching network, and  $Z_{LP}$  is the load impedance of the peak branch, which decreases from high impedance (open circuit) down to  $Z_{node} \frac{N_{comb}}{N_{comb} - 1}$  as the input power  $P_{in}$  increases.

The peak impedance modulation ratio  $N_{Pcomb}$  of the output combining network determines the range of impedances  $0 \leq Z_{LP1} \leq N_{Pcomb} Z_{Pnode}$  that will load the first peak device output matching network, where  $Z_{Pnode}$  is the impedance at the peak combining node looking towards the main combining node, and  $Z_{LP1}$  is the load impedance of the first peak branch, which increases from low impedance (short circuit) up to  $N_{Pcomb} Z_{Pnode}$  as the input power  $P_{in}$  increases. The peak combining node impedance modulation ratio  $N_{Pcomb}$  is defined as:

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<sup>48</sup> OC stands for open circuit which implies high impedance state

$$(150) \quad N_{P_{comb}} = \frac{P_P^{P1} + P_P^{P2}}{P_P^{P1}},$$

The peak combining node peak impedance modulation ratio  $N_{P_{comb}}$  of the output combining network determines the range of impedances  $Z_{P_{node}} \frac{N_{P_{comb}}}{N_{P_{comb}} - 1} \leq Z_{LP2} < OC$  that will load the second peak device output matching network, where  $Z_{P_{node}}$  is the impedance at the peak combining node looking towards the main combining node, and  $Z_{LP2}$  is the load impedance of the first peak branch, which decreases from close to open circuit down to  $Z_{P_{node}} \frac{N_{P_{comb}}}{N_{P_{comb}} - 1}$  as the input power  $P_{in}$  increases. From the above considerations we have the following sets of impedance values that will allow us to calculate the S parameters for each of the four matching networks in the output combining network of the three-way Doherty amplifier.

- **Main Matching Network**

The load-side high power impedance

$$(151) \quad Z_{LMP} = N_{comb} Z_{node}$$

The load-side high efficiency impedance

$$(152) \quad Z_{LME} = Z_{node}$$

The device-side high power impedance  $Z_{MP}$  is selected from the main device high-compression load-pull contours. The device-side high efficiency impedance  $Z_{ME}$  is selected from the main device low-compression load-pull contours. Using the above impedances, converted to corresponding voltage reflection coefficients  $\Gamma_{LMP}$ ,  $\Gamma_{MP}$ ,  $\Gamma_{LME}$ ,  $\Gamma_{ME}$ , with  $\Gamma_{LMP}$  and  $\Gamma_{LME}$  being related through  $N_M = N_{comb}$  where  $N_M = \frac{1+|\Gamma|}{1-|\Gamma|}$  with  $|\Gamma| = \left| \frac{\Gamma'_{ME} - \Gamma'_{MP}}{1 - \Gamma_{MP}\Gamma'_{ME}} \right|$ , along with expressions derived in Section 5.3.6 we can calculate S-parameters for the main matching network.

- **Common Peak Matching Network**

The load-side high power impedance

$$(153) \quad Z_{LPP} = \frac{N_{comb}}{N_{comb} - 1} Z_{node}$$

The device-side high power impedance (user selected)

$$(154) \quad Z_{PP} = Z_{Pnode}$$

The device-side off-state impedance

$$(155) \quad Z_{POFF} = \frac{Z_{LP1OFF} Z_{LP2OFF}}{Z_{LP1OFF} + Z_{LP2OFF}}$$

The load side off-state impedance

$$(156) \quad Z_{LPOFF} = N_p Z_{LPP}$$

Using the above impedances, converted to corresponding voltage reflection coefficients  $\Gamma_{LPP}$ ,  $\Gamma_{LPOFF}$ ,  $\Gamma_{POFF}$ ,  $\Gamma_{PP}$ , where  $\Gamma_{LPP}$  and  $\Gamma_{LPOFF}$  are related

through  $N_p = \frac{1+|\Gamma|}{1-|\Gamma|}$  with  $|\Gamma| = \left| \frac{\Gamma_{POFF} - \Gamma'_{PP}}{1 - \Gamma_{PP} \Gamma_{POFF}} \right|$  resulting in  $Z_{LPOFF} = N_p Z_{LPP}$ ,

along with expressions derived in section 5.3.7 we can calculate S-parameters for the common peak matching network.

- **The First Peak Matching Network**

The load-side high power impedance

$$(157) \quad Z_{LPP1} = N_{Pcomb} Z_{Pnode}$$

The device-side high power impedance  $Z_{PP1}$  is selected from the first device high-compression load-pull contours. The device-side off-state impedance  $Z_{P1OFF}$  is measured directly on the device.

The load-side off-state impedance

$$(158) \quad Z_{LP1OFF} = \frac{Z_{LPP1}}{N_{P1}}$$

Using the above impedances, converted to corresponding voltage reflection coefficients  $\Gamma_{LPP1}$ ,  $\Gamma_{LP1OFF}$ ,  $\Gamma_{P1OFF}$ ,  $\Gamma_{PP1}$ , where  $\Gamma_{LPP1}$  and  $\Gamma_{LP1OFF}$  are related

through  $N_{P1} = \frac{1+|\Gamma|}{1-|\Gamma|}$  where  $|\Gamma| = \left| \frac{\Gamma_{P1OFF} - \Gamma'_{PP1}}{1 - \Gamma_{PP1}\Gamma_{P1OFF}} \right|$  resulting in  $Z_{LP1OFF} = \frac{Z_{LPP1}}{N_{P1}}$ ,

along with expressions derived in section 5.3.7 we can calculate S-parameters for the first peak matching network.

- ***The Second Peak Matching Network***

The load-side high power impedance

$$(159) \quad Z_{LPP2} = \frac{N_{Pcomb}}{N_{Pcomb} - 1} Z_{Pnode}$$

The device-side high power impedance  $Z_{PP2}$  is selected from the second device load-pull data. The device-side off-state impedance  $Z_{P2OFF}$  is measured directly on the device.

The load-side off-state impedance

$$(160) \quad Z_{LP2OFF} = N_{P2} Z_{LPP2}$$

Using the above impedances, converted to corresponding voltage reflection coefficients  $\Gamma_{LPP2}$ ,  $\Gamma_{LP2OFF}$ ,  $\Gamma_{P2OFF}$ ,  $\Gamma_{PP2}$ , where  $\Gamma_{LPP2}$  and  $\Gamma_{LP2OFF}$  are

related through  $N_{P2} = \frac{1+|\Gamma|}{1-|\Gamma|}$  where  $|\Gamma| = \left| \frac{\Gamma_{P2OFF} - \Gamma'_{PP2}}{1 - \Gamma_{PP2}\Gamma_{P2OFF}} \right|$  resulting in

$Z_{LP2OFF} = N_{P2} Z_{LPP2}$ , along with expressions derived in section 5.3.7 we can calculate S-parameters for the second peak matching network

Assuming a symmetric three-way Doherty design implies  $N_{comb} = 3$  and  $N_{Pcomb} = 2$ . By definition  $Z_{node} = \frac{Z_0}{N_{comb}}$  and  $Z_{Pnode} = \frac{Z_0}{N_{Pcomb}}$ , and so we get the following sets of impedances for each matching network:

- **Main Matching Network**

The load-side high power impedance (user selected)

$$(161) \quad Z_{LMP} = Z_0$$

The load-side high efficiency impedance

$$(162) \quad Z_{LME} = \frac{Z_0}{3}$$

The device-side high power impedance  $Z_{MP}$  is selected from the main device load-pull data. The device-side high efficiency impedance  $Z_{ME}$  is selected from the main device load-pull data.

- **Common Peak Matching Network**

The load-side high power impedance

$$(163) \quad Z_{LPP} = \frac{Z_0}{2}$$

The device-side high power impedance

$$(164) \quad Z_{PP} = \frac{Z_0}{2}$$

The device-side off-state impedance

$$(165) \quad Z_{POFF} = \frac{Z_{LP1OFF} Z_{LP2OFF}}{Z_{LP1OFF} + Z_{LP2OFF}}$$

The load-side off-state impedance

$$(166) \quad Z_{LPOFF} = N_P \frac{Z_0}{2} \quad \text{where} \quad N_P = \frac{1+|\Gamma|}{1-|\Gamma|} \quad \text{with} \quad |\Gamma| = \left| \frac{\Gamma_{POFF} - \Gamma'_{PP}}{1 - \Gamma_{PP} \Gamma_{POFF}} \right|$$

- ***The First Peak Matching Network***

The load-side high power impedance (user selected)

$$(167) \quad Z_{LPP1} = Z_0$$

The device-side high power impedance  $Z_{PP1}$  is selected from the first device load-pull data. The device-side off-state impedance  $Z_{P1OFF}$  is measured directly on the device.

The load-side off-state impedance

$$(168) \quad Z_{LP1OFF} = \frac{Z_0}{N_{P1}} \quad \text{where} \quad N_{P1} = \frac{1+|\Gamma|}{1-|\Gamma|} \quad \text{with} \quad |\Gamma| = \left| \frac{\Gamma_{P1OFF} - \Gamma'_{PP1}}{1 - \Gamma_{PP1} \Gamma_{P1OFF}} \right|$$

- ***The Second Peak Matching Network***

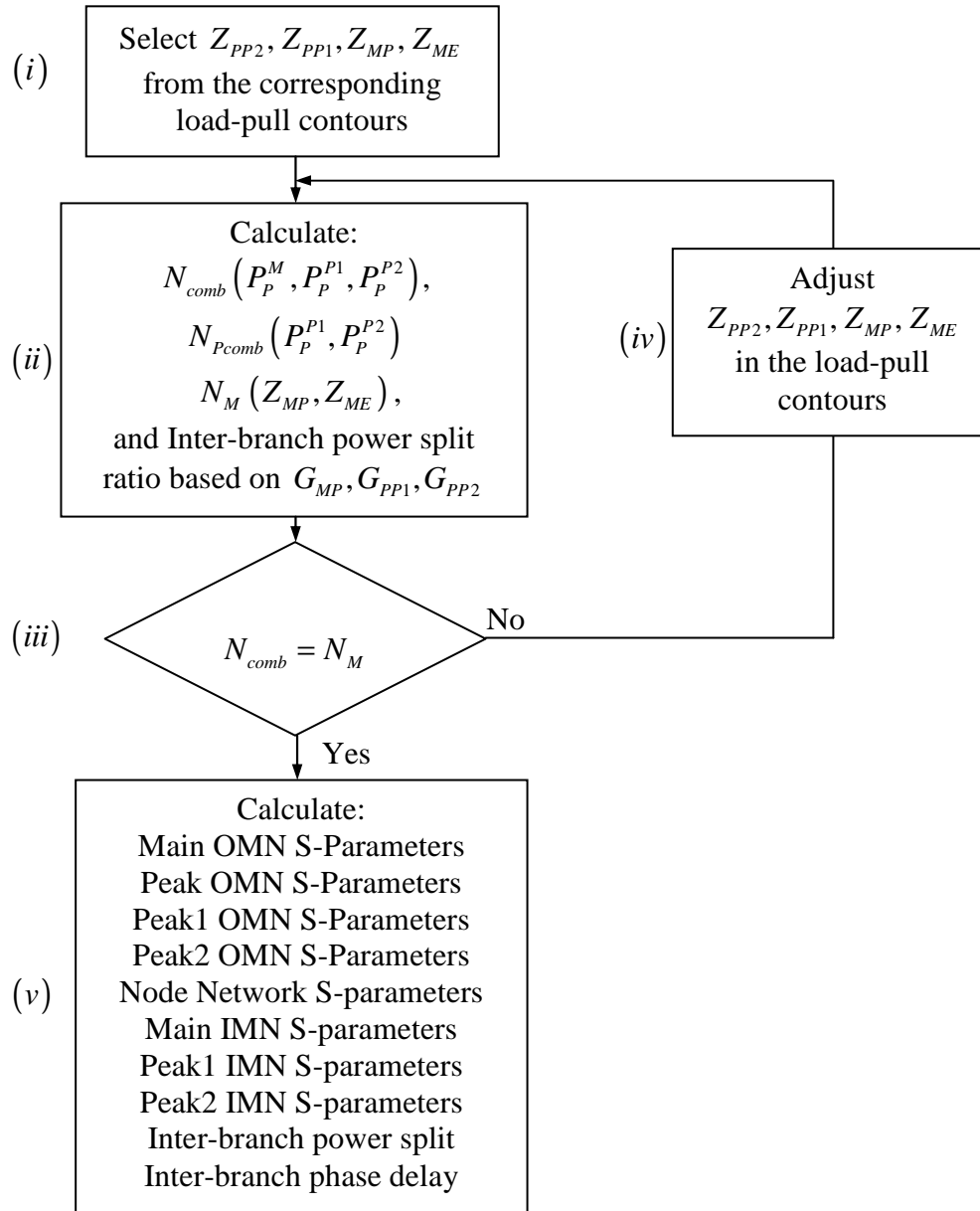
The load-side high power impedance

$$(169) \quad Z_{LPP2} = Z_0$$

The device-side high power impedance  $Z_{PP2}$  is selected from the second device load-pull data. The device-side off-state impedance  $Z_{P2OFF}$  is measured directly on the device.

Load side off-state impedance

$$(170) \quad Z_{LP2OFF} = N_{P2} Z_0 \quad \text{where} \quad N_{P2} = \frac{1+|\Gamma|}{1-|\Gamma|} \quad \text{with} \quad |\Gamma| = \left| \frac{\Gamma_{P2OFF} - \Gamma'_{PP2}}{1 - \Gamma_{PP2} \Gamma_{P2OFF}} \right|$$



**Figure 77: Three-way Doherty design synthesis procedure flow diagram**

Figure 77 shows a flow diagram of the technique for designing three-way Doherty amplifier of Figure 76. This summary is similar to that for the two-way case in Section 5.3.9, *mutatis mutandis*.

The main and peak input matching networks are designed as described in Section 5.3.4 in accordance with the respective values of the source impedances corresponding to those under which the devices were load-pulled. The combining node matching network

is designed based on the selected node impedance as described in Section 5.3.4. Based on the device load-pull contours the designer decides how the power contributions are split between the main and peak devices under the maximum power conditions.

An iterative loop is implemented to determine the main device impedances  $Z_{MP}$ , and  $Z_{ME}$  and impedances  $Z_{PP1}$ , and  $Z_{PP2}$  for the peak devices, that satisfy the condition that the main combining node impedance modulation ratio  $N_{comb}$  is equal to the main device impedance modulation ratio  $N_M$ .

First we initialize the values for the four impedances  $Z_{PP2}$ ,  $Z_{PP1}$ ,  $Z_{MP}$ , and  $Z_{ME}$  from the corresponding load-pull contours [Figure 77 block (i)]. These initial selections are made by educated guesses based on the device load-pull performance and the amplifier specifications. For example, if we need to design a 300W amplifier, we may start with an impedance that enables the main device to deliver 100W of output power and impedances for each of the peak devices that enable them to deliver 100W each. There are multiple impedances that satisfy these power conditions, but the amplifiers resulting from different selections may substantially differ in gain and efficiency, which and so an iterative process of further selection is used. The power ratio between the main and peak devices may change, which will lead to further iterations in the selection process.

The main combining node impedance modulation ratio  $N_{comb}$  and the main device impedance modulation ratio  $N_M$  are calculated using expressions (149) and (77), respectively [Figure 77 block (ii)].

Then one determines whether the main combining node impedance modulation ratio  $N_{comb}$  is sufficiently close in value to the main device impedance ratio [Figure 79 block (iii)]. If not, then processing continues, where one or more of the impedances  $Z_{MP}$ ,  $Z_{ME}$ ,  $Z_{PP1}$ , and  $Z_{PP2}$  are adjusted using the corresponding load-pull contours [Figure 77 block (iv)]. In the software implementation of this design procedure the impedances  $Z_{MP}$ ,  $Z_{ME}$ ,  $Z_{PP1}$ , and  $Z_{PP2}$  are moved in the impedance space of the load-pull contours by means of user-controlled cursors. Moving a cursor in the corresponding load-pull contour plot will alter the value of the selected impedance thus effecting the change in the

associated output power, gain and efficiency, which will cause the algorithm to re-evaluate matching network S-parameter values, values of  $N_{comb}$ ,  $N_M$ , and all other parameters of the circuit that are dependent on these impedances and the associated transistor performance parameters from the load-pull data. Processing then returns to determine the main combining node impedance modulation ratio  $N_{comb}$  and the main device impedance modulation ratio  $N_M$  using the updated impedances.

When one determines that the main combining node impedance modulation ratio  $N_{comb}$  is sufficiently close in value to the main device impedance modulation ratio  $N_M$ , then processing continues to finalize the S matrices for the main and all the peak output matching networks, the inter-branch power split (implemented by input power splitter), and the inter-branch phase delay based on the final values for the impedances  $Z_{MP}$ ,  $Z_{ME}$ ,  $Z_{PP1}$ , and  $Z_{PP2}$  determined by using the techniques described previously [Figure 77 block (v)] which completes the design procedure. This completes the design procedure.

The corresponding analysis procedure, used to calculate the performance of the three-way Doherty configurations designed using the above procedure, is described in Section 6.5.

## **5.6 Conclusions**

Standard design procedures for the Doherty amplifiers presented in the literature make certain number of assumptions that may not hold true in all cases, for all devices or for certain design goals. Also, documented procedures mostly focus on the output combining network with its impedance inverters and offset lines to make sure that certain impedance modulation ratios are achieved but neglect to take in the account the effects the active device biasing has on the gain of each branch of the amplifier, output power capabilities of each active device, gain compression state of the device, etc. Certain parts of the topology are selected by default like 3dB 90° hybrid as an input power splitter, or 50ohm quarter-wave impedance inverter in the output of the main branch network in the case of a symmetric two-way Doherty design, and may cause the performance of the amplifier after the implementation to deviate from the performance predicted by the design procedure resulting in certain performance specification not being met.

We introduce a comprehensive design procedure for Doherty amplifiers that relies on load-pull characterization of the active devices. The design procedure relies on a number of performance specifications to derive which operating conditions must be satisfied to achieve desired amplifier performance. It eliminates all unnecessary assumptions and allows us to design every part of the amplifier topology to perform precisely how it needs to perform in order to make the amplifier operate according to design specification.

The closed form expressions for calculation of S-parameters for each matching network in the Doherty amplifier topology are presented and they allow us to focus on the Doherty amplifier design without having to implement each of the networks as physical circuit for every iteration of the Doherty amplifier design. This convenience allows us to explore many trade-offs in the performance parameter space of the amplifier before settling for the final design which will then be implemented as a physical circuit.

We expanded the fixed-input-power-split two-way Doherty amplifier design procedure to fixed-input-power-split three-way Doherty amplifier design (and by extension to fixed-input-power-split N-way Doherty amplifier design using the expansion techniques presented in 4.6) as well as to so-called digital Doherty amplifier design that

allows us to fully condition the behaviour of the main device by means of dynamically controlled inputs to both main and peak device.

## **5.7 References for Chapter 5**

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## Chapter 6

# 6 Doherty Amplifier Analysis Techniques Based on Transistor Load-pull Measurements

### 6.1 Introduction

Standard circuit simulators rely on active device models that may not be available immediately when new active devices enter production, and thus the designer may not have the ability to use commercial simulators to verify the amplifier's performance. Also, device models may not be as accurate as measured load-pull data, and will not necessarily reflect the device performance variation due to production process variability (which is important in yield analysis). In this chapter we will introduce Doherty amplifier analysis technique that will allow us to analyze the performance of Doherty amplifiers and individual active devices within the amplifiers based on the known S-parameters of the amplifier passive networks and the load-pull data characterizing the constituent active devices. We will perform input power sweeps in order to calculate output power, efficiency, gain profile (AM-AM characteristic of the amplifier), gain compression, and phase response (AM-PM) of the Doherty amplifier and its active devices individually. An example of using load-pull data to characterize active devices is available in [65], the intent was to generate behavioural models of active devices without specifics of how the devices will be used. An application of load-pull data analysis to two-way Doherty amplifier optimization is provided in [66] with a small collection of results reported. An extensive analysis of a high-power two-way Doherty is presented in [67], authors used load-pull data in conjunction with X-parameter framework to generate models and carry out the performance analysis. It is not exactly clear whether scalar or vector load-pull data was used, the instrumentation setup indicates scalar measurements with possibility of expansion to vector measurement capability. There are no details how the off-state impedance of the peak device was handled.

In section 6.2 we discuss the interactions between the passive parts of the amplifier with the active parts through the load-pull data representing the behaviour of the active devices in absence of active device equivalent circuits or models.

Section 6.3 deals with the analysis of a fixed input power split two-way Doherty amplifier. The analysis procedure focuses on the output combining network because that is where all the complex interactions between main and peak device signals take place. The analysis results obtained for several variants of the amplifier designed for a given set specifications is shown with description how certain aspects of the design are affected by various parameters such as bias, and input power split ratio.

Based on previously derived expressions and with additional degrees of freedom available from the independently controlled inputs to the main and peak device we present the analysis procedure for a controlled-main-device-compression two-way Doherty amplifier in section 6.4.

The analysis procedure for the fixed input power split three-way Doherty amplifier as an extension of fixed input power split two-way Doherty amplifier with additional complexities being addressed is shown in section 6.5.

## **6.2 *Passive Network and Load-Pull Data Interactions***

Once all the S-parameter blocks have been determined during the synthesis portion of the design cycle we wish to analyze the performance of the Doherty Amplifier architectures. An analysis procedure that enables us to do this is developed here. It will be constructed based on the block diagram depictions in Figure 78 (two-way Doherty) and Figure 79 (three-way Doherty). The upper block diagram in each of the figures represents the full amplifier circuit that could be analysed using a circuit solver if the transistor models are available, the passive networks being fully characterized by the two-port S-parameter blocks from the design procedure. In the absence of an accurate transistor equivalent circuit we can combine the load-pull data (to provide the relationship between the transistor input and output parameters) and passive circuit theory (to model the input and output passive networks), using the transistor load-pull

measurements of output power and phase delay in order to excite the output combining network, to predict the amplifier performance and that of its constituent branches.

The transistor load-pull data provides connection between the input power  $P_{in}^M$  presented to the input of the main device from the input matching network with the known source impedance  $Z_S^M$  and output power  $P_M$  that excites the device side of the main output matching network. The values of the main device load impedance  $Z_M$  and transmission phase  $\phi_M$  are known. It fulfills the function of the transistor equivalent circuit. Similarly, load-pull data provides connection between input power  $P_{in}^P$  presented to the input of the peak device from the input matching network with the known source impedance  $Z_S^P$  and output power  $P_p$  that excites the device side of the peak output matching network. The values of the peak device load impedance  $Z_p$  and transmission  $\phi_p$  are known. It fulfills the function of the transistor equivalent circuit of the peak device. In the three-way Doherty there are two peak devices with associated load-pull parameters denoted by  $Z_S^{P1}$ ,  $P_{in}^{P1}$ ,  $P_{P1}$ ,  $Z_{P1}$ ,  $\phi_{P1}$  for the first peak device which is biased in class-C with an input voltage  $V_{gs\_P1}$  and  $Z_S^{P2}$ ,  $P_{in}^{P2}$ ,  $P_{P2}$ ,  $Z_{P2}$ ,  $\phi_{P2}$  for the second peak device which is biased in class-C with an input voltage  $V_{gs\_P2}$ . We presented the block diagrams for two-way and three-way Doherty amplifier architectures but this procedure can be extended to N-way architectures.

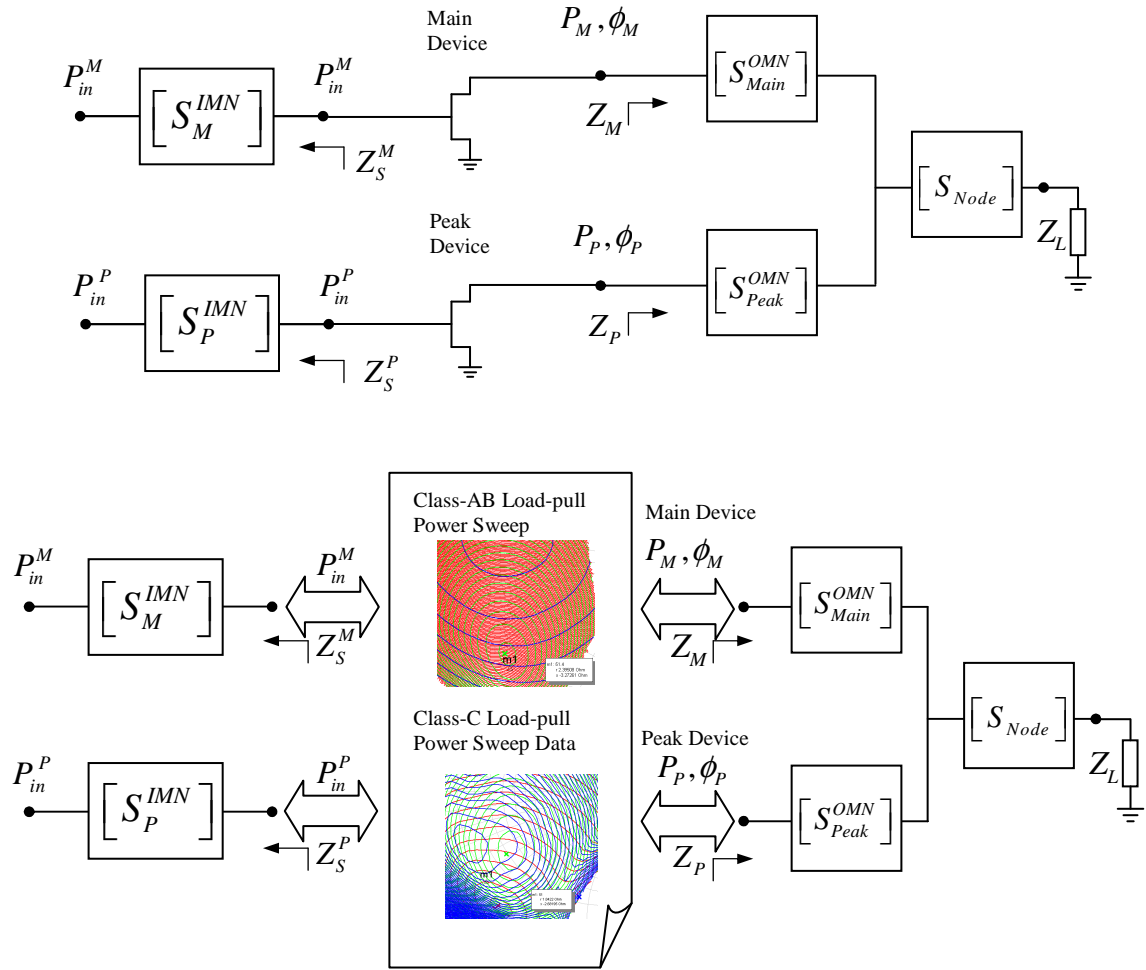
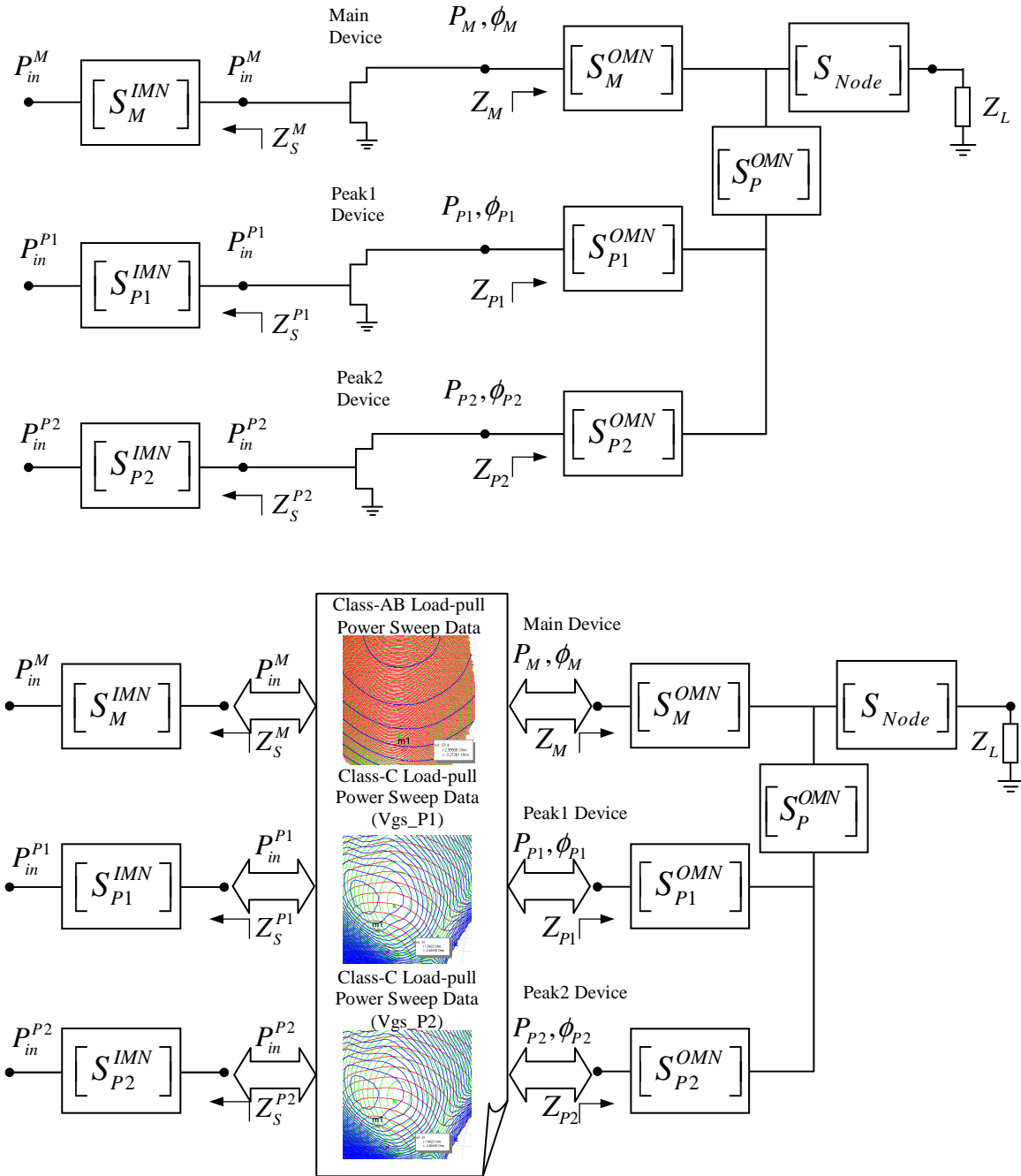


Figure 78: Block diagram of input-to-output load-pull data interaction in two-way Doherty amplifier architecture



**Figure 79: Block diagram of input-to-output load-pull data interaction in three-way Doherty amplifier architecture**

## 6.3 Two-Way Fixed Input Power Split Doherty Analysis

### 6.3.1 Description of the Analysis Procedure

Once the two-way Doherty amplifier of Figure 70 has been designed using the design technique whose flow diagram is shown in Figure 73, appropriate sets of load-pull data can be used to analyze the amplifier to establish the relationships between the values  $P_{in}^M$  and  $Z_S^M$  on the input side and the values  $P_M$ ,  $Z_M$ , and  $\phi_M$  on the output side of the main device and also between the values  $P_{in}^P$  and  $Z_S^P$  on input side and the values  $P_P$ ,  $Z_P$ , and  $\phi_P$  on the output side of the peak device.

Figure 80 shows a flow diagram of the technique for analyzing the two-way Doherty amplifier of Figure 70. The analysis technique consists of two nested loops: an outer loop in which the amplifier is analyzed at different input power levels and an inner loop in which the impedance levels for the main and peak output matching networks are iteratively evaluated for a particular input power level until those impedance levels converge to steady-state values.

In the analysis technique, the input power ( $P_{in}$ ) sweep starts at the maximum power level ( $P_{inMax}$ ) for the amplifier, and is decremented for each iteration of the outer loop for a specified number of iteration steps designed to bring the input power level down to an appropriate minimum power level for the amplifier. The sweep starts from the maximum (rather than some other level) power level because the impedances  $Z_M$  and  $Z_P$  are well defined for this power level in the design procedure of Figure 73, which ensures that, in the absence of error in the design, the analysis technique will rapidly (if not immediately) converge to satisfy the inner loop condition [Figure 80 block (vi)] for the first iteration of the outer loop.

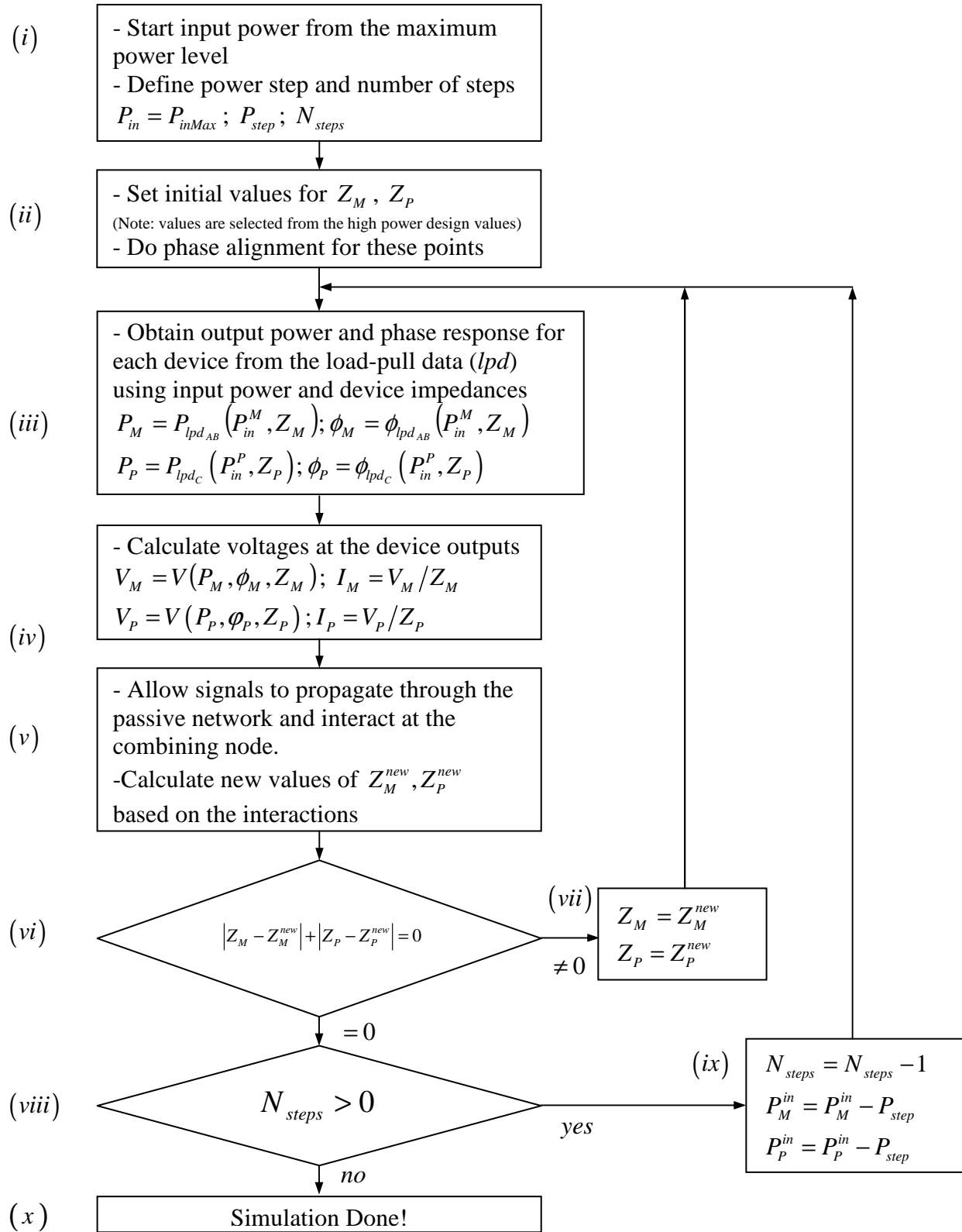


Figure 80: Two-way Doherty analysis flow chart

If the design is done using design technique of Figure 73, then the initial  $Z_M$  and  $Z_p$  values will be, respectively, equal to the final values of  $Z_{MP}$  and  $Z_{PP}$  from the design procedure. If an external design is used (that is, a design done using some other technique), then educated guesses for the initial impedance values  $Z_M$  and  $Z_p$  are used to start the iterative process. For each subsequent iteration of the outer loop, the steady-state main and peak output matching network impedance values  $Z_M^{new}$  and  $Z_p^{new}$  determined during the previous outer-loop iteration are retained as the initial values for the first iteration of the inner loop.

In particular, the analysis procedure begins with initialization of the input power level  $P_{in}$  to the maximum power level  $P_{inMax}$  [Figure 80 block (i)]. Based on the known power split performed by input power splitter, the magnitudes of the main branch input power level  $P_{IN}^M$  and the peak branch input power level  $P_{IN}^P$  can be determined from the input power level  $P_{in}$ . In addition,  $P_{step}$  of each power level decrement and the number  $N_{step}$  of such decrements for the analysis is specified in the same block. Note that, for this explanation, all powers are expressed in *dBm* or other suitable units.

Next [Figure 80 block (ii)] the impedance value  $Z_M$  presented to the main amplifier device and the impedance value  $Z_p$  presented to the peak amplifier device are initialized to values for high-power operations determined during design procedure of Figure 73. In addition, phase alignments for the main and peak branches are performed during this step. Equation (145) is used to calculate the phase delay of each S-parameter block within each branch under the varying load conditions that they experience during the amplifier operation. The sum of the phase delays for each S-parameter block in a branch will give the overall phase delay for the branch. Since there are two (or more) branches, and we want the signals to combine at the combining node(s) under specified phase conditions (in-phase, or otherwise specified, phase relation), the phase of each peak amplifier branch may need to be adjusted with respect to the main branch to achieve the required phase conditions. For in-phase alignment, for example, if the main branch has a delay of  $97^\circ$  and the peak branch has a delay of  $85^\circ$ , then in order to make the currents combine in-phase at the combining node, the peak branch can be delayed by  $12^\circ$  by

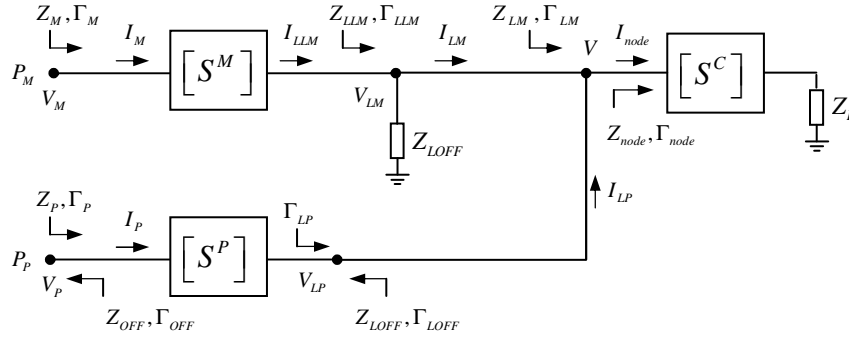
delaying the peak input signal by  $12^\circ$ . The change in the peak input signal phase will change the loading conditions for each of the branches resulting in a new delay for the main branch of, for example,  $95^\circ$  and a new delay for the peak branch (with the previous delay correction of  $12^\circ$ ) of  $98^\circ$ , an additional delay correction of  $-3^\circ$  can be applied to the peak branch (for a net delay correction of  $9^\circ$ ), such that the delay for the main branch is now  $96^\circ$  and the delay for the peak branch is now  $96^\circ$ , at which point phase alignment is completed (if the alignment is not achieved at this point the iterations continue until the alignment is achieved). This is done directly by monitoring the branch currents at the combining node. In the phase-alignment process,  $Z_M$  and  $Z_P$  will change due to impedance modulation effect at the combining node caused by the phase changes being applied to the peak signal.

If the proper design impedances are not known (e.g., because the amplifier was designed using a technique other than design technique of Figure 73) then phase alignment needs to be guessed as well and we need to go through iterations to achieve convergence and if necessary re-evaluate our phasing guess. By examining the constant input power load-pull contours for the main and peak devices, the most plausible values for impedances  $Z_M$  and  $Z_P$  for high-power performance can be determined. The phase offset needed for an in-phase combining is then determined by examining the initial phase mismatch of the calculated values for currents  $I_{LM}$  and  $I_{LP}$  at the combining node in Figure 81 and using it adjust the input phase offset of the peak input signal to obtain convergence for this initial value of the input power. The technique does not yet proceed to a full input power sweep. Changes are made in the phase alignment if necessary and the iterations continue at the initial input power level until a desirable phase alignment is achieved. Only then does the technique proceed to the full input power sweep.

In the next step [Figure 80 block (iii)], the output power  $P_M$  and phase response  $\phi_M$  of the main amplifier device are determined from the load-pull data (e.g.,  $P_{lpdAB}$ ,  $\phi_{lpdAB}$  for the main device biased in class-AB) using the main branch input power level  $P_{IN}^M$  and the main amplifier device impedance level  $Z_M$ . The power and phase values are read from the load-pull power sweeps. These parameters are directly measured in the active device load-pull process with some level of interpolation applied. Similarly, the

output power  $P_p$  and phase response  $\phi_p$  of the peak amplifier device are determined from the load-pull data (e.g.,  $P_{pdC}$ ,  $\phi_{pdC}$  for the peak device biased in class-C) using the peak branch input power level  $P_{IN}^P$  and the peak amplifier device impedance level  $Z_p$ .

Next [Figure 80 block (iv)] the voltages  $V_M$  and  $V_p$  and currents  $I_M$  and  $I_p$  output from the main and peak amplifier devices are determined.



**Figure 81: Schematic of the two-way Doherty output combining network with associated notation**

Figure 81 shows a block diagram representing passive output combining network of the two-way Doherty amplifier. In Figure 81, load  $Z_{LOFF}$  represents the loading on the main branch contributed by the peak branch when the peak branch is disabled ( $I_{LP} = 0$ ).

For the main branch going from the main device toward the combining node, calculations for converting the main device impedance  $Z_M$  into the main voltage reflection coefficient  $\Gamma_M$ , and vice versa, can be done using

$$(171) \quad \Gamma_M = \frac{Z_M - Z_0}{Z_M + Z_0}$$

$$(172) \quad Z_M = Z_0 \frac{1 + \Gamma_M}{1 - \Gamma_M} = \frac{V_M}{I_M} = |Z_M| e^{j\phi_{Z_M}}$$

The complex power  $S_M$  of the main device has a real part  $P_M$  that is known from the main device load-pull data, and an imaginary part  $Q_M$  that is unknown. However,

$S_M$  is also given by  $\frac{|V_M|^2}{2Z'_M}$ <sup>49</sup> in which the impedance  $Z_M$  is known from load-pull data.

Known values of  $P_M$  and  $Z_M$  allow the calculation of  $V_M$  and  $I_M = \frac{V_M}{Z_M}$ , which are used in the circuit analysis of the output combining network. Thus the complex power  $S_M$  of the main device is given by

$$(173) \quad S_M = P_M + jQ_M = \frac{|V_M|^2}{2Z'_M} = \frac{|I_M|^2 Z_M}{2} = \frac{V_M I'_M}{2}$$

The main device voltage  $V_M$  is calculated from the known main device power  $P_M$  and the main device impedance  $Z_M$  as

$$(174) \quad V_M = |V_M| e^{j\phi_M} = \sqrt{\frac{2P_M}{\text{Re}\{Z_M\}}} |Z_M| e^{j\phi_M}$$

We are at liberty to select the phase of  $V_M$  as the reference phase, and so can (without loss of generality) set  $\phi_M = 0$ . Then (174) becomes

$$(175) \quad V_M = \sqrt{\frac{2P_M}{\text{Re}\{Z_M\}}} |Z_M|$$

For the peak branch going from the peak device toward the combining node, calculations for converting the peak device impedance  $Z_p$  into the peak voltage reflection coefficient  $\Gamma_p$ , and vice versa, can be done using

$$(176) \quad \Gamma_p = \frac{Z_p - Z_0}{Z_p + Z_0}$$

and

$$(177) \quad Z_p = Z_0 \frac{1 + \Gamma_p}{1 - \Gamma_p} = \frac{V_p}{I_p}$$

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<sup>49</sup> Note that the prime symbol denotes complex conjugation

The complex power  $S_p$  of the peak device has a real part  $P_p$  that is known from the peak device load-pull data, and an imaginary part  $Q_p$  that is unknown. However,  $S_p$  is also given by  $\frac{|V_p|^2}{2Z'_p}$  in which the impedance  $Z_p$  is known from load-pull data. Known values of  $P_p$  and  $Z_p$  allow the calculation of  $V_p$  and  $I_p = \frac{V_p}{Z_p}$ , which are used in the circuit analysis of output combining network. Thus the complex power  $S_p$  of the peak device is given by

$$(178) \quad S_p = P_p + jQ_p = \frac{|V_p|^2}{2Z'_p} = \frac{|I_p|^2 Z_p}{2} = \frac{V_p I'_p}{2}$$

The peak device voltage  $V_p$  is calculated from the known peak device power  $P_p$  and peak device impedance  $Z_p$  as

$$(179) \quad V_p = |V_p| e^{j\phi_p} = \sqrt{\frac{2P_p}{\text{Re}\{Z_p}\}} |Z_p| e^{j\phi_p}$$

Once the voltages and currents on the device side for each branch are known, currents on the node side of each branch can be determined, which allows for the calculation of loading impedances for each branch and in turn the calculation of the new impedances presented to the devices. The signals are allowed to propagate through the passive network formed by the main and peak output matching networks, the node matching network, and output load, and new values ( $Z_M^{new}$  and  $Z_p^{new}$ ) for the main and peak amplifier device impedance levels are determined (Figure 80 block (v)).

Load side main voltages, currents, and impedances are calculated from the known main device side voltages, currents, impedances, and the S-parameters of the main output matching network. Since  $V_M$ ,  $I_M$ ,  $Z_M$ , and  $\Gamma_M$  are known on the device side of the main output matching network, and the S-parameters  $[S^M]$  of the network are known as well, quantities  $V_{LM}$ ,  $I_{LLM}$ ,  $Z_{LLM}$ , and  $\Gamma_{LLM}$  can be calculated on the node side of the network in the manner detailed below. Calculations to obtain  $Z_{LOFF}$  are done to account for the

loading effect at the combining node due to the off-state impedance of the peak device transformed through the network.

The relation between  $\Gamma_M$  and  $\Gamma_{LLM}$  is derived from the definition of the S-parameters using (57), and is given by

$$(180) \quad \Gamma_M = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LLM}}{1 - S_{22}^M \Gamma_{LLM}}$$

Rearranging Equation (180) to express  $\Gamma_{LLM}$  in terms of  $\Gamma_M$  yields

$$(181) \quad \Gamma_{LLM} = \frac{\Gamma_M - S_{11}^M}{S_{12}^M S_{21}^M + S_{22}^M (\Gamma_M - S_{11}^M)}$$

where the corresponding impedance  $Z_{LLM}$  is given by

$$(182) \quad Z_{LLM} = Z_0 \frac{1 + \Gamma_{LLM}}{1 - \Gamma_{LLM}}$$

Using Equation (143),  $V_{LM}$  can be expressed in terms of  $V_M$ , and used to calculate current  $I_{LLM}$  according to

$$(183) \quad V_{LM} = \frac{S_{21}^M (1 + \Gamma_{LLM}) V_M}{1 + S_{11}^M - (S_{22}^M + S_{11}^M S_{22}^M - S_{12}^M S_{21}^M) \Gamma_{LLM}}$$

and

$$(184) \quad I_{LLM} = \frac{V_{LM}}{Z_{LLM}}$$

From the peak device side, off-state impedance  $Z_{OFF}$  of the peak device is transformed into  $Z_{LOFF}$  loading the main branch using

$$(185) \quad Z_{OFF} = Z_0 \frac{1 + \Gamma_{OFF}}{1 - \Gamma_{OFF}} \quad \Gamma_{OFF} = \frac{Z_{OFF} - Z_0}{Z_{OFF} + Z_0}$$

$$(186) \quad \Gamma_{LOFF} = S_{22}^P + \frac{S_{12}^P S_{21}^P \Gamma_{OFF}}{1 - S_{11}^P \Gamma_{OFF}} \quad Z_{LOFF} = Z_0 \frac{1 + \Gamma_{LOFF}}{1 - \Gamma_{LOFF}}$$

The main branch load impedance  $Z_{LM}$  is expressed in terms of  $Z_{LLM}$  and  $Z_{LOFF}$ , where  $Z_{LLM}$  is given by a parallel connection of  $Z_{LM}$  and  $Z_{LOFF}$ . The main branch load current  $I_{LM}$  entering the combining node is derived from the current  $I_{LLM}$  entering the current divider formed by  $Z_{LM}$  and  $Z_{LOFF}$  as

$$(187) \quad Z_{LM} = \frac{Z_{LLM}Z_{LOFF}}{Z_{LOFF} - Z_{LLM}}; \quad I_{LM} = \frac{Z_{LOFF} - Z_{LLM}}{Z_{LOFF}} I_{LLM}$$

Load-side peak voltages, currents, and impedances are calculated from the known peak device side voltages, currents, impedances, and the S-parameters of the peak output matching network. Since  $V_p$ ,  $I_p$ ,  $Z_p$ , and  $\Gamma_p$  are known on the device side of the peak output matching network and the S-parameters  $[S^P]$  of the network are known, quantities  $V_{LP}$ ,  $I_{LP}$ ,  $Z_{LP}$ , and  $\Gamma_{LP}$  can be calculated on the node side of the network by using the circuit analysis provided below, which is similar to that used for the main branch expression derivations presented above. The  $Z_{node}$  calculation is the result of an impedance transformation through a network with known S-parameters, and so

$$(188) \quad \Gamma_p = S_{11}^P + \frac{S_{12}^P S_{21}^P \Gamma_{LP}}{1 - S_{22}^P \Gamma_{LP}} \Rightarrow \Gamma_{LP} = \frac{\Gamma_p - S_{11}^P}{S_{12}^P S_{21}^P + S_{22}^P (\Gamma_p - S_{11}^P)}; \quad Z_{LP} = Z_0 \frac{1 + \Gamma_{LP}}{1 - \Gamma_{LP}}$$

$$(189) \quad V_{LP} = \frac{S_{21}^P (1 + \Gamma_{LP}) V_p}{1 + S_{11}^P - (S_{22}^P + S_{11}^P S_{22}^P - S_{12}^P S_{21}^P) \Gamma_{LP}}; \quad I_{LP} = \frac{V_{LP}}{Z_{LP}}$$

and

$$(190) \quad \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}; \quad \Gamma_{node} = S_{11}^C + \frac{S_{12}^C S_{21}^C \Gamma_L}{1 - S_{22}^C \Gamma_L}; \quad Z_{node} = Z_0 \frac{1 + \Gamma_{node}}{1 - \Gamma_{node}}$$

The new main and peak branch load impedances  $Z_{LM}$ ,  $Z_{LLM}$ , and  $Z_{LP}$  are calculated using previously calculated values of  $I_{LM}$ ,  $I_{LP}$  as

$$(191) \quad V = (I_{LM} + I_{LP}) Z_{node};^{50} \quad Z_{LM} = \frac{V}{I_{LM}}; \quad Z_{LP} = \frac{V}{I_{LP}}$$

---

<sup>50</sup>  $V$  is the combining node voltage

$$(192) \quad Z_{LLM} = \frac{Z_{LM} Z_{LOFF}}{Z_{LM} + Z_{LOFF}}; \quad \Gamma_{LLM} = \frac{Z_{LLM} - Z_0}{Z_{LLM} + Z_0};$$

The new main and peak device side impedances  $Z_M$  and  $Z_P$  are calculated based on the new main and peak branch load impedances  $Z_{LLM}$  and  $Z_{LP}$  by transforming these impedances through the main and peak output matching networks back to the main and peak device side to obtain new device-side impedances  $Z_M$  and  $Z_P$ , respectively. The sequence of calculations can be summarized as

$$(193) \quad \Gamma_M = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LLM}}{1 - S_{22}^M \Gamma_{LLM}}; \quad Z_M = Z_0 \frac{1 + \Gamma_M}{1 - \Gamma_M}$$

and

$$(194) \quad \Gamma_{LP} = \frac{Z_{LP} - Z_0}{Z_{LP} + Z_0}; \quad \Gamma_P = S_{11}^P + \frac{S_{12}^P S_{21}^P \Gamma_{LP}}{1 - S_{22}^P \Gamma_{LP}}; \quad Z_P = Z_0 \frac{1 + \Gamma_P}{1 - \Gamma_P}$$

It is next determined whether the new main and peak amplifier device impedance levels  $Z_M^{new}$  and  $Z_P^{new}$  sufficiently match the corresponding previous impedance levels  $Z_M$  and  $Z_P$  [Figure 80 block (vi)]. This is done by determining whether the corresponding values are equal to within a specified threshold level. If the different pairs of impedance levels do not all agree sufficiently closely, it means that the inner loop is not yet complete and processing continues to the next step [Figure 80 block (vii)], where the main and peak amplifier device impedance levels  $Z_M$  and  $Z_P$  are updated to be equal to the new values  $Z_M^{new}$  and  $Z_P^{new}$  determined in the previous step. Processing then iterates using the updated impedance levels.

If it is determined that the different pairs of impedance levels do in fact agree sufficiently well, then the inner loop is complete for the current input power level  $P_{in}$ , and processing continues to determine whether the number  $N_{steps}$  of remaining steps is greater than zero [Figure 80 block (viii)]. If the number of steps is greater than zero, then the outer loop is not yet complete, and the processing continues to the next step [Figure 80 block (ix)], where the number of steps, and the main and peak branch input power levels are decremented for the next iteration of the outer loop. The processing then

returns to repeat steps of the inner loop [Figure 80 blocks (iii) through (vi)] for the new outer-loop iteration. For every instance of the inner loop convergence the output power, gain, efficiency, compression, and other relevant performance parameters of the two-way Doherty amplifier and its constituent devices are calculated from the interpolated device load-pull data, and calculated currents and voltages in the passive portion of the network. The results are tabulated and can be readily displayed as will be shown in Section 6.3.2., if it is determined that the number of steps  $N_{steps}$  has reached zero, then the analysis algorithm is complete and processing terminates.

Note that Doherty amplifiers designed using design technique summarized in Figure 73 can be analyzed using the analysis technique of Figure 80 and/or using any other suitable analysis technique. Similarly, the analysis technique can be used to analyze Doherty amplifiers designed using any other suitable design technique. Although the analysis technique has been described in the context of two-way Doherty amplifiers these techniques can be extended to apply to  $N$ -way Doherty amplifiers having a main amplifier branch and  $(N-1)$  peak amplifier branches. This will be shown in Section 6.5 for the three-way case (that is, for  $N = 3$ )

Although the analysis technique has been described in the context of fixed input conditioning, it can be applied to other implementations, such as static adjustable input conditioning and dynamic input conditioning. Static adjustable input conditioning implies that the amplitude ratio of the input signals, and their phase relationship, are adjusted for one power level at a frequency of interest. The user can specify a change of input settings with frequency. Dynamic adjustable input conditioning implies that the amplitude ratio of the input signals, and their phase relationship, are specified for all power levels and frequencies of interest. The user can specify a change of input settings with power and frequency. Each of the three different scenarios has its own set of goals and restrictions, and they can all be addressed using the principles and calculations of Chapter 5 (for design) and the present Chapter (for analysis purposes).

## 6.3.2 Example Applications of the Analysis Procedure

### *A. Calculated Performance of the Complete Amplifier*

A two-way fixed input split Doherty amplifier was designed using the techniques from Section 5.3.2 and analyzed using the procedure just described. The design specifications for the Doherty amplifier design were: maximum output power 54dBm (symmetric configuration with each device contributing 51dBm at maximum power), maximized efficiency at 6dB power back-off, maximized gain, and maximized gain linearity (minimized gain compression of the devices). The gate bias of the peak device was swept from 1.1V to 1.4V in 0.1V increments and load-pull data obtained for each case. For each value of the peak device gate bias the optimized peak output matching network was designed and the optimal input power split calculated (2.39dB, 2.13dB, 1.86dB, and 1.57dB more power to the peak branch with increasing gate bias, respectively) to meet the specifications (i.e. for each device to deliver 51dBm for the maximum of 54dBm as specified). The calculated gain and efficiency performance of the four Doherty amplifier designs is shown in Figure 82. The efficiency for all designs is better than 55% at 6dB back-off (48dBm), and the gain compression is on the order of 3.5dB. The gain increases with increasing peak device gate bias and the efficiency in the intermediate power region decreases with increasing peak gate bias, which means that efficiency can be traded off for gain/gain linearity and vice-versa.

Using the same specifications another set of two-way fixed input split Doherty amplifiers was designed by the procedure of Section 5.3.2 for four different peak device gate biases 1.1V to 1.4V in 0.1V increments, but the input power split was not optimized for each value of the gate bias. Instead 3dB splitter (equal input power to each branch) was used in all cases. This is a common case in the design when off-the-shelf parts are used and it is not possible to select arbitrary splitting ratios. The gain and efficiency performance of the four Doherty amplifier designs is shown in Figure 83. The efficiency for all designs is better than 60% at 6dB back-off (48dBm), but the gain compression is now on the order of 5.2dB. The gain increases with increasing peak device gate bias, and the efficiency in the intermediate power region decreases with increasing peak gate bias, which again reveals that efficiency can be traded off for gain/gain linearity, and vice-

versa. The higher efficiency for the 3dB input power split designs comes at the expense of poorer gain linearity compared to the adjusted input power split designs.

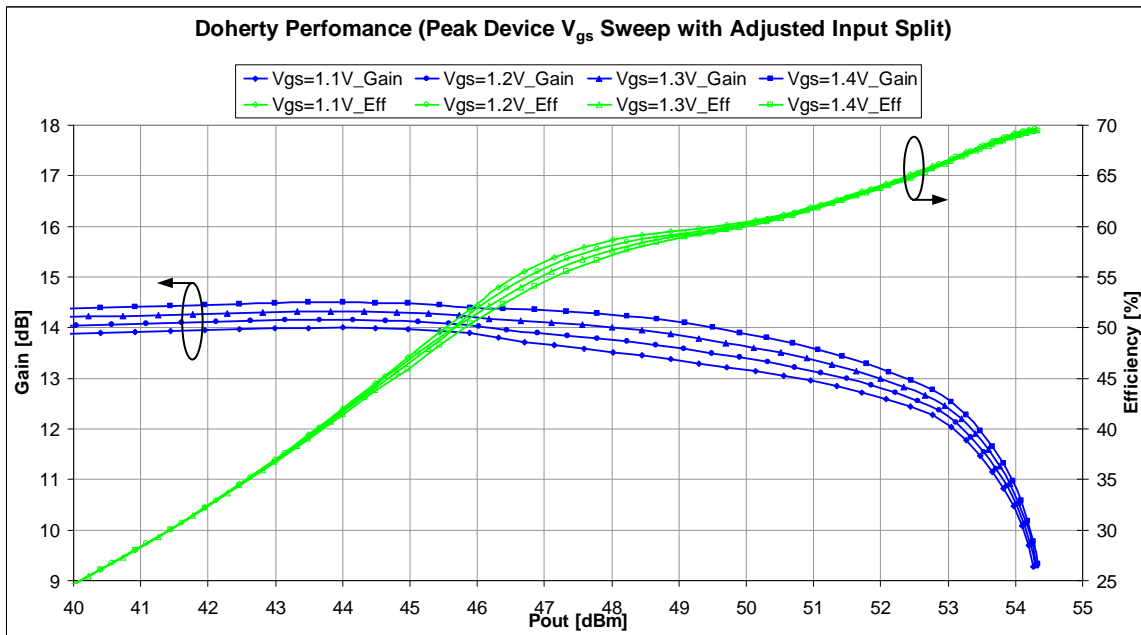


Figure 82: Performance of the four different two-way Doherty amplifiers, designed for different gate bias voltages (of the peak device) and adjusted input power split

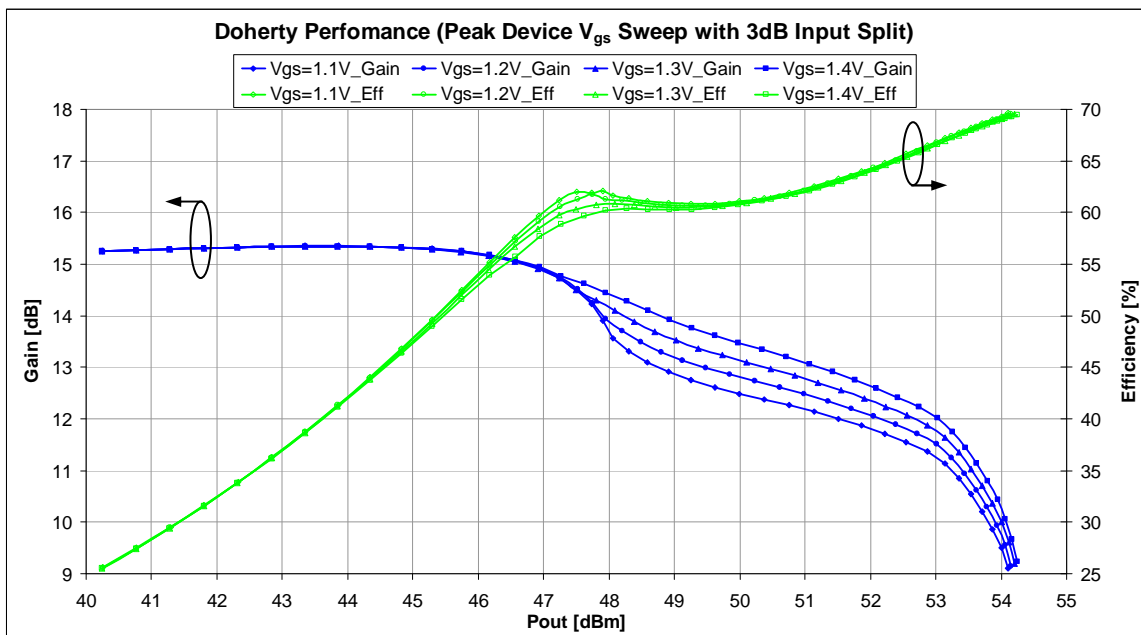
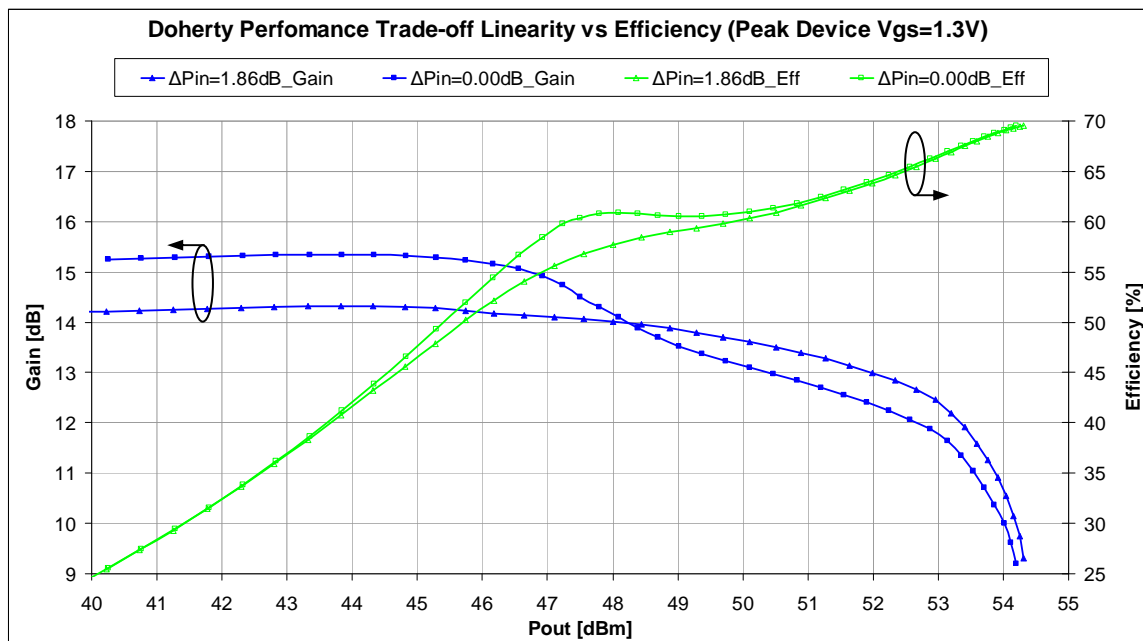


Figure 83: Performance of the four different two-way Doherty amplifiers, designed for different gate bias voltages (of the peak device) but fixed 3dB input power split

To emphasize the efficiency to gain linearity trade-off the performance of the adjusted input split (1.86dB more power to the peak branch) and 3dB input split (equal input power to each branch) two-way Doherty designs for the same value of the peak device gate bias (1.3V) are shown in Figure 84. The power splitter in the adjusted input power split design steers more power to the peak device (which due to its class-C bias has lower gain than the main device biased in class-AB) and thus lowers the gain for the lower signal levels but increases the gain in the higher signal power region thus improving the overall linearity. For the intermediate power levels there is around a 4% difference in efficiency that diminishes as the amplifiers approach their maximum power levels. The more pronounced efficiency peak for the 3dB input split design is because of the rapid compression of the main device due to the delayed conduction onset of the peak device caused by the lower peak device input power levels compared to the adjusted input split design which steers 1.86dB more power to the peak device than to the main device.



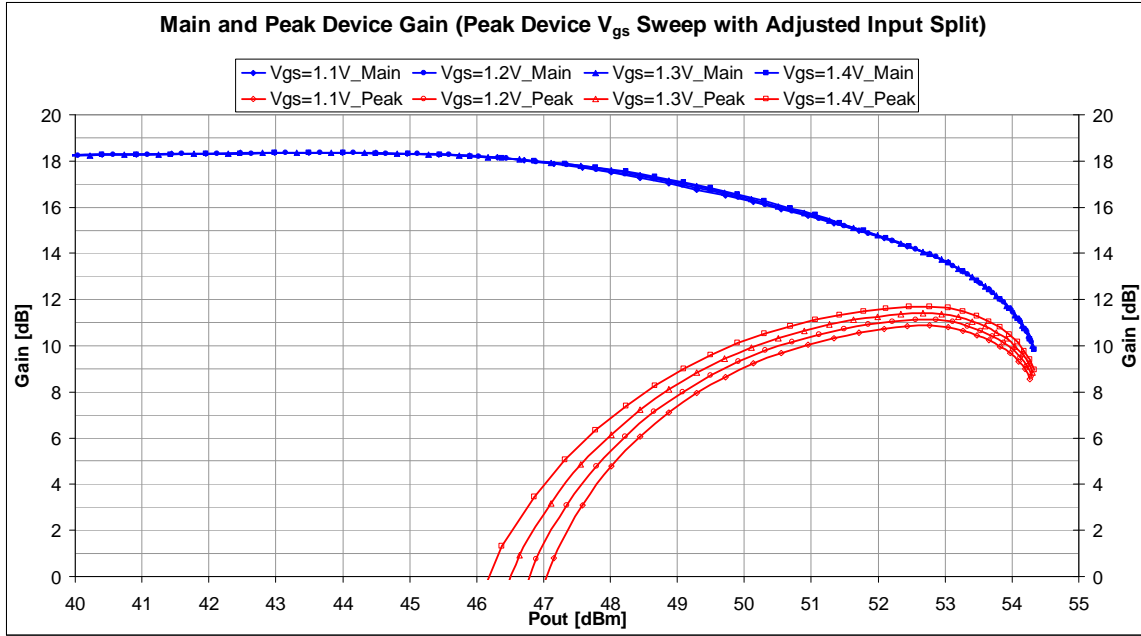
**Figure 84: Two-way Doherty with 3dB input power split versus two-way Doherty with adjusted input power split performance comparison. The amplifiers compared are those designed for the peak device gate biases of 1.3V.**

### ***B. Calculated Performance of the Individual Active Devices in the Amplifier***

The previous results were for the performance of the two-way Doherty amplifier as a whole. We next present the individual gain performance of the main and peak devices separately. This main and peak device gain performance with the adjusted input power split (2.39dB, 2.13dB, 1.86dB, and 1.57dB more power to the peak branch with increasing gate bias respectively) two-way Doherty designs is shown in Figure 85. Recall that the four designs were done for different values of the peak device gate bias, as indicated in Figure 85. The lower the peak device gate bias the larger the value of  $P_{out}$  (output power of the complete amplifier) before the peak device turns on. This allows the main device to reach the high efficiency range of operation. The gain of the peak device decreases with a decrease of the peak device gate bias (deeper class-C bias implies lower gain); to compensate for the gain loss the input power splitter steers more power to the peak device (partially cancelling the onset adjustment). From the Figure 85 we can see that gain of the peak device drops by approximately 0.25dB for every 0.1V of the peak device gate bias decrease, there is also a corresponding 0.25dBm "delay"<sup>51</sup> in the peak device conduction onset for every 0.1V in the gate bias decrease. Even though we lowered the gain of the peak device by trying to adjust the onset of the conduction of the peak device, we compensated for the loss of gain by supplying more input power to the peak device and thus maintained the gain compression of the main device almost independent from the gain changes of the peak device. This means the linearity did not suffer at the expense of overall lower Doherty gain, as can be seen from Figure 82.

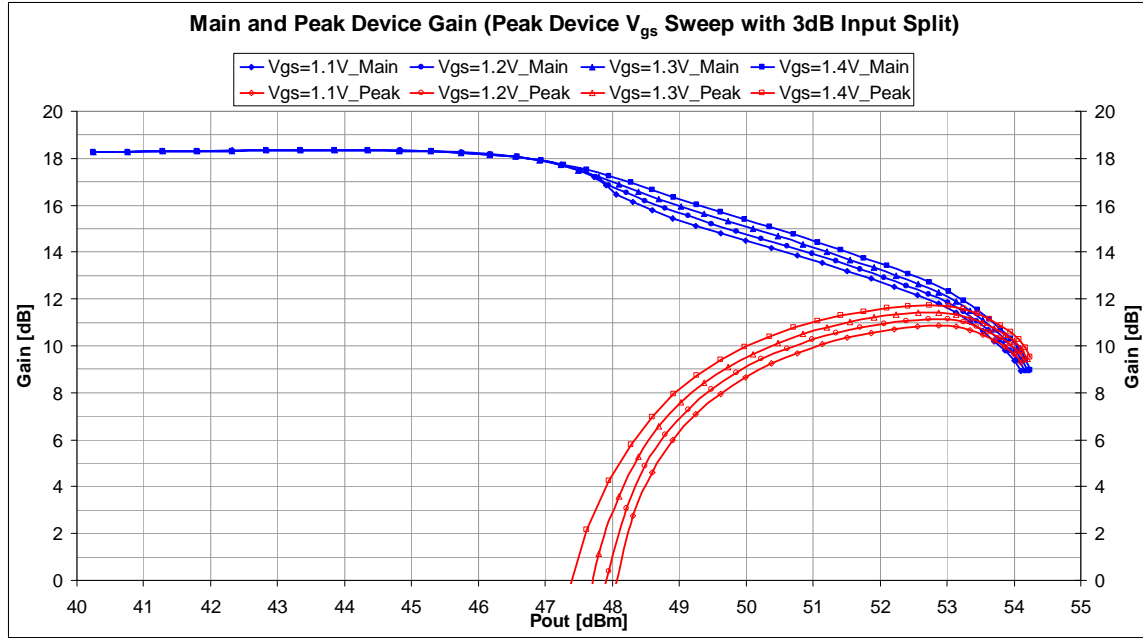
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<sup>51</sup> By "delay" here we do not mean a timing issue, but the fact that the onset of conduction of the peak device occurs at power levels 0.25dBm higher for each 0.1V decrease in gate bias voltage.



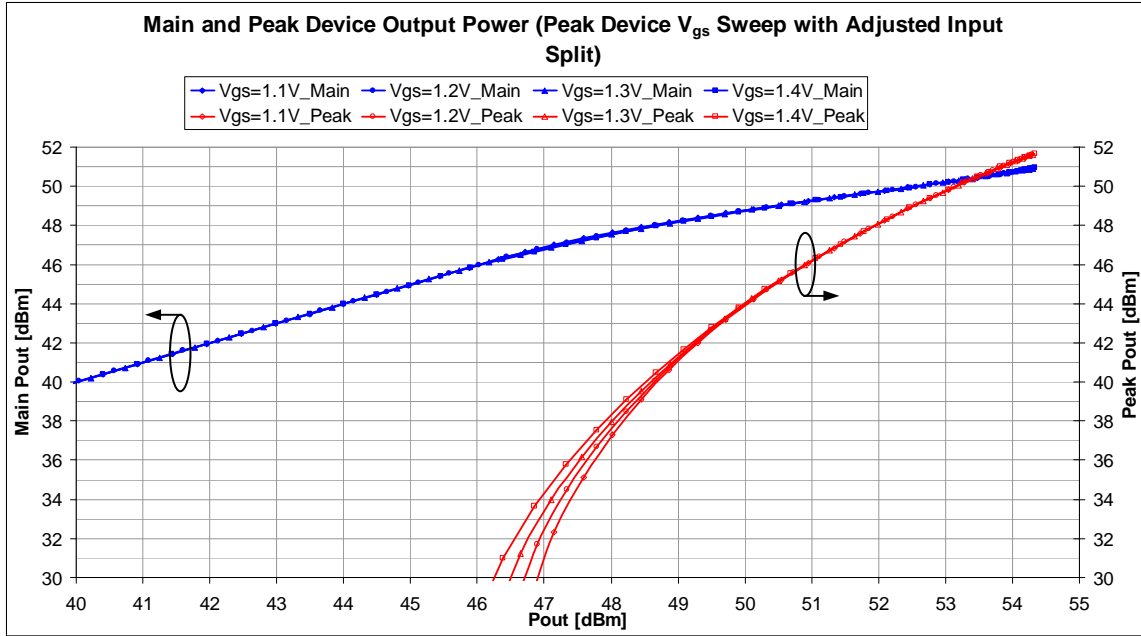
**Figure 85: Main and peak device gain performance in two-way Doherty amplifiers (with different peak device gate bias and adjusted input power split) as a function of the output power of the complete amplifier.**

The main and peak device gain performance with the 3dB input power split (equal input power to each branch) two-way Doherty designs is shown in Figure 86. Recall that the four designs were done for different values of the peak device gate bias, as indicated in Figure 86. The lower the peak device gate bias the larger the value of  $P_{out}$  (output power of the complete amplifier) before the peak device turns on. This allows the main device to reach the high efficiency range of operation. The gain of the peak device decreases with decrease of the peak device gate bias (deeper class-C bias implies lower gain). In this design we did not compensate for the gain loss by adjusting the input power split. From the Figure 86 we can see that gain of the peak device drops by approximately 0.25dB for every 0.1V of the peak device gate bias decrease, there is also a corresponding 0.2dBm "delay" in the peak device conduction onset for every 0.1V in the gate bias decrease. Since we did not compensate for the lower gain of the peak device by adjusting the input power levels the main device suffers a higher rate of compression (compared to compensated input power split case), which increases by approximately 0.25dB for every 0.1V of decrease of the peak device gate bias.



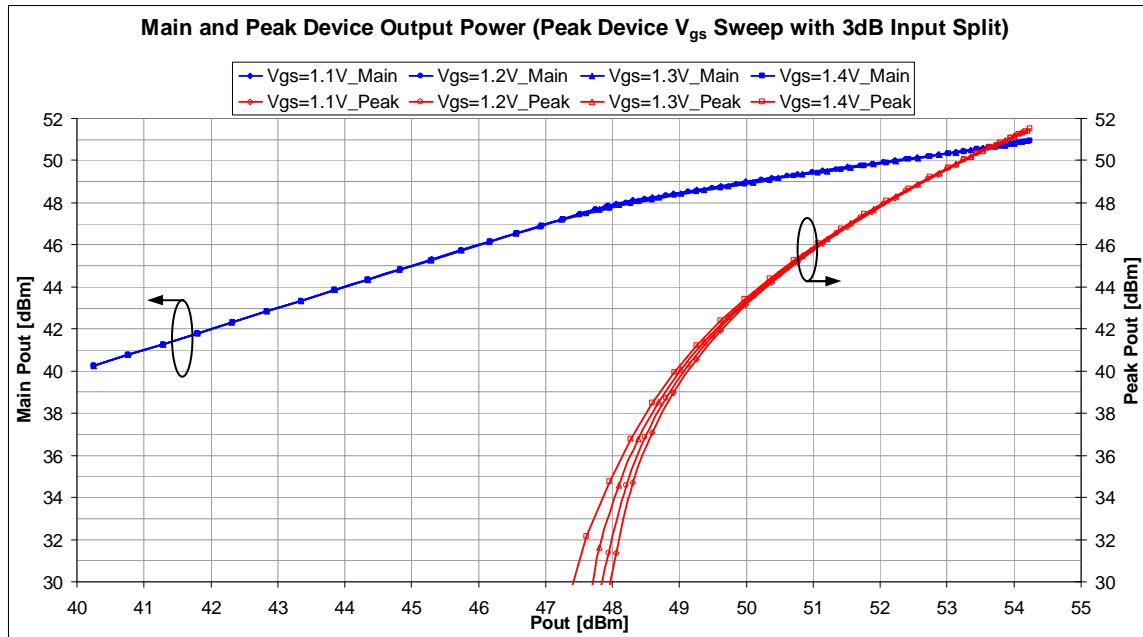
**Figure 86: Main and peak device gain performance in two-way Doherty amplifiers with peak device gate bias sweep and 3dB input power split**

The main and peak device power performance with the adjusted input power split (2.39dB, 2.13dB, 1.86dB, and 1.57dB more power to the peak branch with increasing gate bias respectively) two-way Doherty designs is shown in Figure 87. Recall that the four designs were done for different values of the peak device gate bias, as indicated in Figure 87. The lower the peak device gate bias the larger the value of  $P_{out}$  (output power of the complete amplifier) before the peak device turns on. This allows the main device to reach the high efficiency range of operation. The gain of the peak device decreases with a decrease of the peak device gate bias (deeper class-C bias implies lower gain); to compensate for the gain loss the input power splitter steers more power to the peak device (partially cancelling the onset adjustment). We can see that main device gradually transitions from a low power linear mode of operation (when its output power is lower than 46dBm) to a high power nonlinear mode, thanks to the load impedance modulation caused by the power contribution from the peak device. Without such load impedance modulation the main device would remain in the high efficiency regime of operation under which it cannot deliver sufficiently high output power to meet the design specification and as a consequence it would also experience a severe compression.



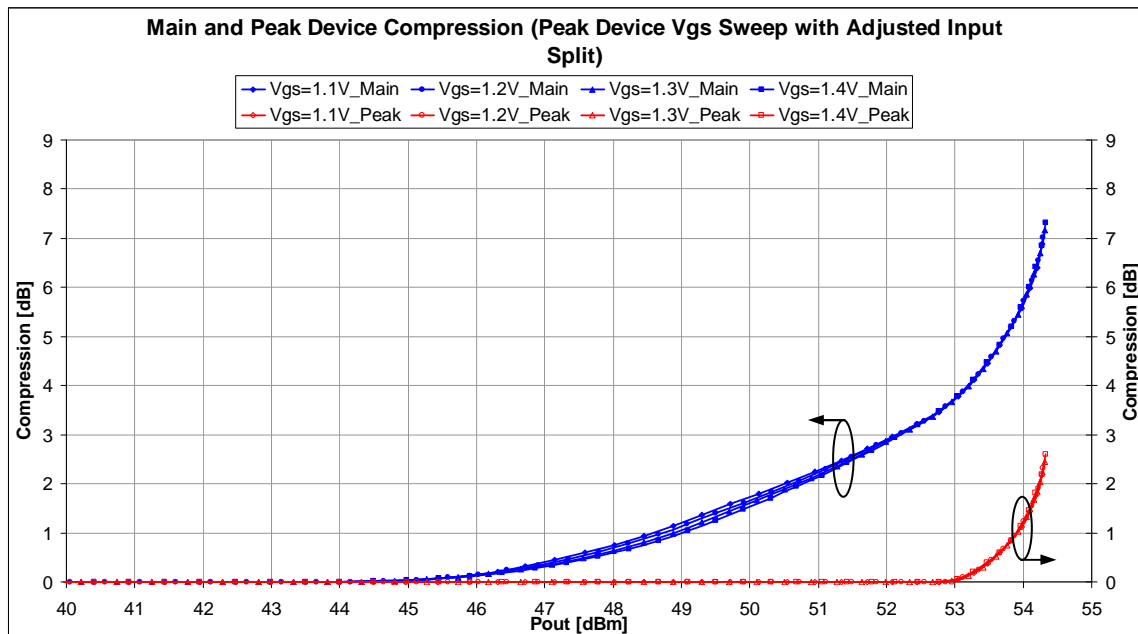
**Figure 87: Main and peak device power performance in two-way Doherty amplifiers (with different peak device gate bias and adjusted input power split) as a function of the output power of the complete amplifier.**

The main and peak device power performance with the 3dB input power split (equal input power to each branch) two-way Doherty designs is shown in Figure 88. Recall that the four designs were done for different values of the peak device gate bias, as indicated in Figure 88. The lower the peak device gate bias the larger the value of  $P_{out}$  (output power of the complete amplifier) before the peak device turns on. This allows the main device to reach the high efficiency range of operation. The gain of the peak device decreases with a decrease of the peak device gate bias (deeper class-C bias implies lower gain). From the Figure 88 we can see that main device sharply transitions from a low power linear mode of operation (when its output power is lower than 48dBm) to a high power nonlinear mode thanks to the load impedance modulation caused by the power contribution from the peak device.



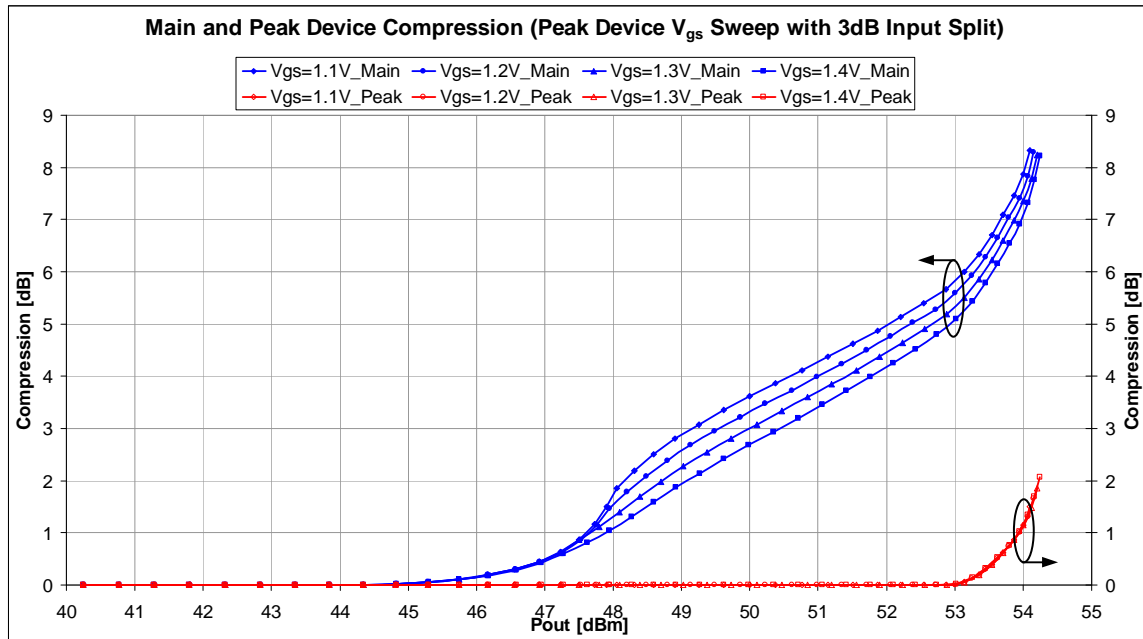
**Figure 88: Main and peak device power performance in two-way Doherty amplifiers (with different peak device gate bias and 3dB input power split) as a function of the output power of the complete amplifier.**

The main and peak device compression performance with the adjusted input power split (2.39dB, 2.13dB, 1.86dB, and 1.57dB more power to the peak branch respectively with increasing gate bias) two-way Doherty designs is shown in Figure 89. Recall that the input power split, the main device matching network and peak device matching network were designed to maintain the main device and peak device compression levels below 5.5dB and 1dB, respectively, for Doherty output power levels below 54dBm. Keeping the device compression levels at these values provided gain linearity shown in Figure 82. To achieve targeted device compression levels the input power split compensation is essential.



**Figure 89: Main and peak device compression performance in two-way Doherty amplifiers (with different peak device gate bias and adjusted input power split) as a function of the output power of the complete amplifier.**

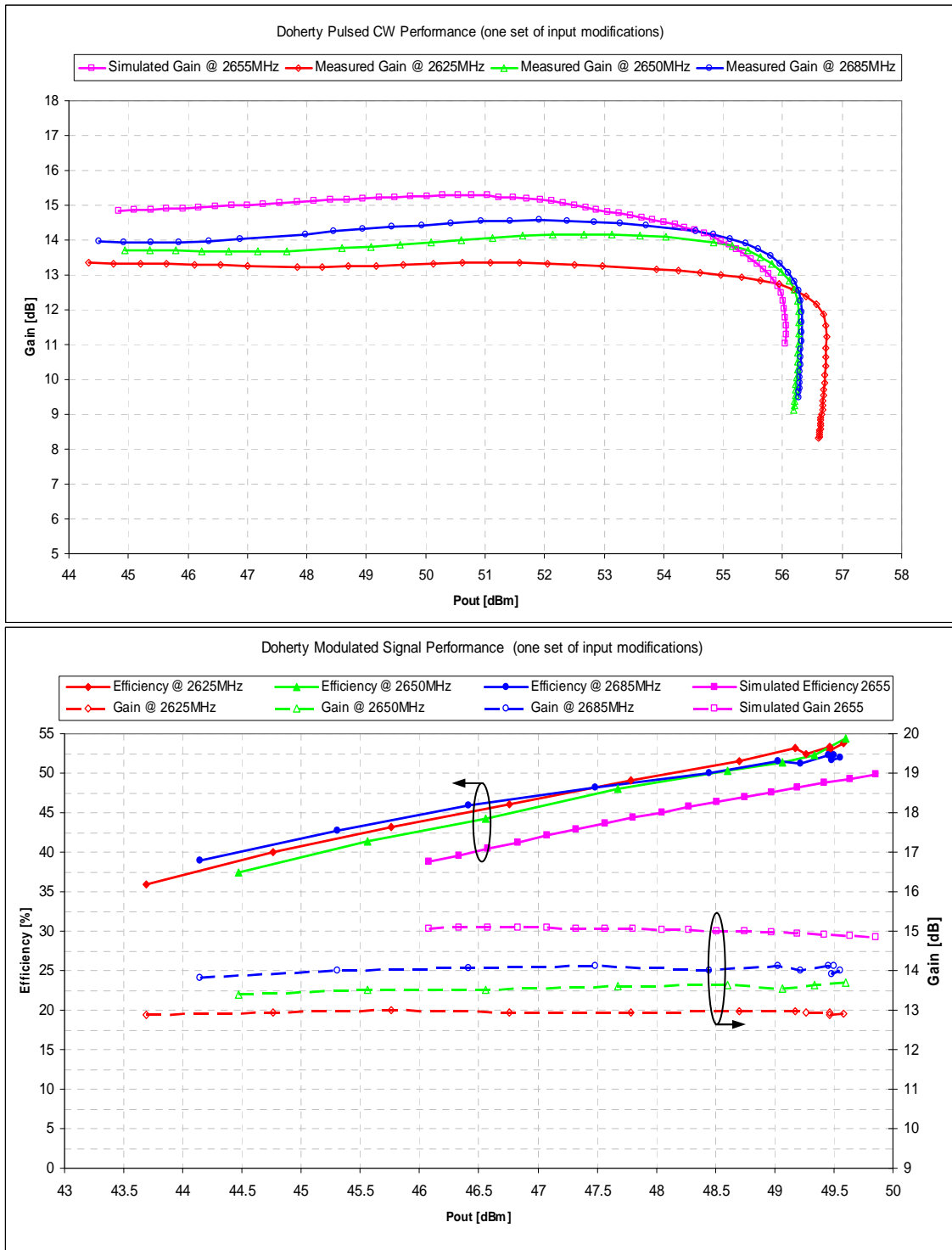
The main and peak device compression performance with the 3dB power split (equal input power to each branch) two-way Doherty designs is shown in Figure 90. Once again, we recall that the main device matching network and peak device matching network were designed to maintain the main device and peak device compression levels below 5.5dB and 1dB, respectively, for the Doherty amplifier output power levels below 54dBm. However, the input power split was fixed at 3dB and this caused an increased compression of the main device (the peak device could not provide sufficient load impedance modulation due to lower gain) of greater than 7dB at the maximum Doherty power level of 54dBm. The increased compression of the main device is the main cause of poorer gain linearity of the Doherty amplifiers shown in Figure 83. These designs were of course purposefully done to demonstrate how useful the analysis technique is in checking a design before implementation.



**Figure 90: Main and peak device compression performance in two-way Doherty amplifiers (with different peak device gate bias and 3dB input power split) as a function of the output power of the complete amplifier.**

### *C. Comparison of Calculated and Measured Performance*

A two-way fixed-input-split Doherty amplifier was designed using the techniques from Section 5.3.2, analyzed using the procedure just described, manufactured and then measured. The design specifications for the Doherty amplifier design were: maximum output power 56dBm (symmetric configuration with each device contributing 53dBm at maximum power), maximized efficiency at 6dB power back-off, maximized gain, and maximized gain linearity (minimized gain compression of the devices). The input power split used was 3dB (off the shelf 3dB hybrid). The calculated and measured gain and efficiency performance is shown in Figure 91. The measured efficiency of 53% is slightly better than simulated performance of 50%. The measured gain is 1.5dB lower than simulated but that was expected because the simulated matching networks were lossless.



**Figure 91: Comparison of simulated and measured gain and efficiency of a two-way compact Doherty amplifier with the peak device input matching network of the fabricated amplifier tuned to improve gain linearity**



$$(195) \quad Z_{LM}(n) = \left( 1 + n \frac{N_M - 1}{N_{steps}} \right) Z_{node}$$

where  $n$  indicates the current instance of  $Z_{LM}(n)$  under analysis. The linear form of main device compression progression is defined as

$$(196) \quad COMP(n) = COMP_{start} + n \frac{COMP_{stop} - COMP_{start}}{N_{steps}}$$

where  $n$  is the current instance of compression  $COMP(n)$  associated with  $Z_{LM}(n)$ .

Determining  $Z_M$  from known  $Z_{LM}$  is accomplished by

$$(197) \quad Z_{LLM} = \frac{Z_{LM} Z_{LOFF}}{Z_{LM} + Z_{LOFF}} \quad \Gamma_{LLM} = \frac{Z_{LLM} - Z_0}{Z_{LLM} + Z_0}$$

and

$$(198) \quad \Gamma_M = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LLM}}{1 - S_{22}^M \Gamma_{LLM}} \quad Z_M = Z_0 \frac{1 + \Gamma_M}{1 - \Gamma_M}$$

Now that the values of  $Z_M(n)$  and  $COMP(n)$  are known the constant compression load-pull data can be used to determine the output power  $P_M(n)$  of the main device. Once the output power of the main device is determined from the constant compression load-pull contours we can proceed to calculate the remaining parameters relevant to the main branch of the amplifier under these conditions. The complex power sourced by the main device is given by

$$(199) \quad S_M = P_M + jQ_M = \frac{|V_M|^2}{2Z'_M} = \frac{|I_M|^2 Z_M}{2} = \frac{V_M I'_M}{2}$$

The voltage on the main device side is given by

$$(200) \quad V_M = |V_M| e^{j\phi_M} = \sqrt{\frac{2P_M}{\text{Re}\{Z_M\}}} |Z_M| e^{j\phi_M}$$

if we use  $\phi_M$  as the reference phase ( $\phi_M = 0$ ) then the device side voltage is given by

$$(201) \quad V_M = \sqrt{\frac{2P_M}{\text{Re}\{Z_M\}}} |Z_M|$$

Expressing the load side reflection coefficient in terms of the known device side reflection coefficient we get

$$(202) \quad \Gamma_M = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LLM}}{1 - S_{22}^M \Gamma_{LLM}} \quad \Rightarrow \quad \Gamma_{LLM} = \frac{\Gamma_M - S_{11}^M}{S_{12}^M S_{21}^M + S_{22}^M (\Gamma_M - S_{11}^M)}$$

We can then calculate the corresponding load side impedance for the main branch as

$$(203) \quad Z_{LLM} = Z_0 \frac{1 + \Gamma_{LLM}}{1 - \Gamma_{LLM}}$$

From the known device side voltage and known S-parameters of the main output matching network we can calculate the main load side voltage by

$$(204) \quad V_{LM} = \frac{S_{21}^M (1 + \Gamma_{LLM}) V_M}{1 + S_{11}^M - (S_{22}^M + S_{11}^M S_{22}^M - S_{12}^M S_{21}^M) \Gamma_{LLM}}$$

and the corresponding current is then

$$(205) \quad I_{LLM} = \frac{V_{LM}}{Z_{LLM}}$$

Off-state reflection coefficient on the peak device side is given by

$$(206) \quad \Gamma_{OFF} = \frac{Z_{OFF} - Z_0}{Z_{OFF} + Z_0}$$

The off-state coefficient on the load side of the peak output matching and the corresponding impedance are given by

$$(207) \quad \Gamma_{LOFF} = S_{22}^P + \frac{S_{12}^P S_{21}^P \Gamma_{OFF}}{1 - S_{11}^P \Gamma_{OFF}} \quad Z_{LOFF} = Z_0 \frac{1 + \Gamma_{LOFF}}{1 - \Gamma_{LOFF}}$$

Impedance seen by the main branch at the combining node and its load current are obtained from

$$(208) \quad Z_{LM} = \frac{Z_{LLM} Z_{LOFF}}{Z_{LOFF} - Z_{LLM}} \quad I_{LM} = \frac{Z_{LOFF} - Z_{LLM}}{Z_{LOFF}} I_{LLM}$$

Now that the relevant parameters for the main branch are all known we can proceed to determine the corresponding peak branch parameters that will support the above-calculated main branch parameters. The node impedance is given by the following

$$(209) \quad \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \quad \Gamma_{node} = S_{11}^C + \frac{S_{12}^C S_{21}^C \Gamma_L}{1 - S_{22}^C \Gamma_L} \quad Z_{node} = Z_0 \frac{1 + \Gamma_{node}}{1 - \Gamma_{node}}$$

From the known  $I_{LM}$ ,  $Z_{LM}$ , and  $Z_{node}$  we can calculate the necessary peak branch load side current using

$$(210) \quad Z_{LM} = \frac{I_{LM} + I_{LP}}{I_{LM}} Z_{node} \quad \Rightarrow \quad I_{LP} = \frac{Z_{LM} - Z_{node}}{Z_{node}} I_{LM}$$

then the peak branch load impedance is calculated

$$(211) \quad Z_{LP} = \frac{I_{LM} + I_{LP}}{I_{LP}} Z_{node} \quad \Gamma_{LP} = \frac{Z_{LP} - Z_0}{Z_{LP} + Z_0}$$

Since the two branches are connected to the combining node the load voltages must be equal

$$(212) \quad V_{LP} = V_{LM} = (I_{LM} + I_{LP}) Z_{node}$$

This allows us to determine the device side voltage

$$(213) \quad V_P = \frac{1 + S_{11}^P - (S_{22}^P + S_{11}^P S_{22}^P - S_{12}^P S_{21}^P) \Gamma_{LP}}{S_{21}^P (1 + \Gamma_{LP})} V_{LP}$$

and the corresponding peak device reflection coefficient and impedance

$$(214) \quad \Gamma_P = S_{11}^P + \frac{S_{12}^P S_{21}^P \Gamma_{LP}}{1 - S_{22}^P \Gamma_{LP}} \quad Z_P = Z_0 \frac{1 + \Gamma_P}{1 - \Gamma_P}$$

from which we can calculate the power the peak device must deliver

$$(215) \quad S_P = P_P + jQ_P = \frac{|V_P|^2}{2Z_P'} \Rightarrow \quad P_P = \text{Re} \left\{ \frac{|V_P|^2}{2Z_P'} \right\}$$

from the load-pull measurement we can determine the insertion phase for the device

$$(216) \quad \phi_P = \angle V_P$$

This procedure will be repeated for every one of the  $n$  instances and will yield  $P_p(n)$ , and  $\phi_p(n)$  values for each instance that will ensure that main device is conditioned as specified at every power level.

From the now known sets of the peak device output power  $P_p(n)$  and associated phase  $\phi_p(n)$  values the peak device input power set  $P_{in}^P(n)$  and input phase set  $\phi_{in}^P(n)$  from the peak device load-pull data can be derived. Similarly we can obtain the main device input power set  $P_{in}^M(n)$  and input phase set  $\phi_{in}^M(n)$  from the known sets of  $P_M(n)$  and associated phase  $\phi_M(n)$ . Now that we have the input power and phase sets for both devices we can utilize the dynamic input conditioning to control the main device compression for enhanced gain linearity performance, and guarantee in-phase combining for enhanced efficiency for all power levels.

## 6.5 Three-Way Fixed Input Power Split Doherty Analysis

Once the three-way Doherty amplifier of Figure 76 has been designed, using the design technique whose flow diagram is shown in Figure 77, appropriate sets of load-pull data can be used to analyze the amplifier to establish the relationships between the values  $P_{in}^M$  and  $Z_{in}^M$  on the input side and the values  $P_M$ ,  $Z_M$ , and  $\phi_M$  on the output side of the main device, between the values  $P_{in}^{P1}$  and  $Z_{in}^{P1}$  on input side and the values  $P_{P1}$ ,  $Z_{P1}$ , and  $\phi_{P1}$  on the output side of the first peak device, as well as between the values  $P_{in}^{P2}$  and  $Z_{in}^{P2}$  on input side and the values  $P_{P2}$ ,  $Z_{P2}$ , and  $\phi_{P2}$  on the output side of the second peak device.

Figure 93 shows a flow diagram of a technique for analyzing the three-way Doherty amplifier of Figure 76. The analysis technique consists of two nested loops: an outer loop in which the amplifier is analyzed at different input power levels and an inner loop in which the impedance levels for the main and each of the peak output matching networks are iteratively adjusted for a particular input power level until those impedance levels converge to steady-state values.

In the analysis technique, the input power ( $P_{in}$ ) sweep starts at the maximum power level ( $P_{inMax}$ ) for the amplifier, and is decremented for each iteration of the outer loop for a specified number of iteration steps designed to bring the input power level down to an appropriate minimum power level for the amplifier analysis. The sweep starts from the maximum (rather than some other) power level because the impedances  $Z_M$ ,  $Z_{P1}$ , and  $Z_{P2}$  are well defined for this power level in the design procedure of Figure 77, which ensures that, in the absence of error in the design, the analysis technique will rapidly (if not immediately) converge to satisfy the inner loop condition [Figure 93 block (vi)] for the first iteration of the outer loop.

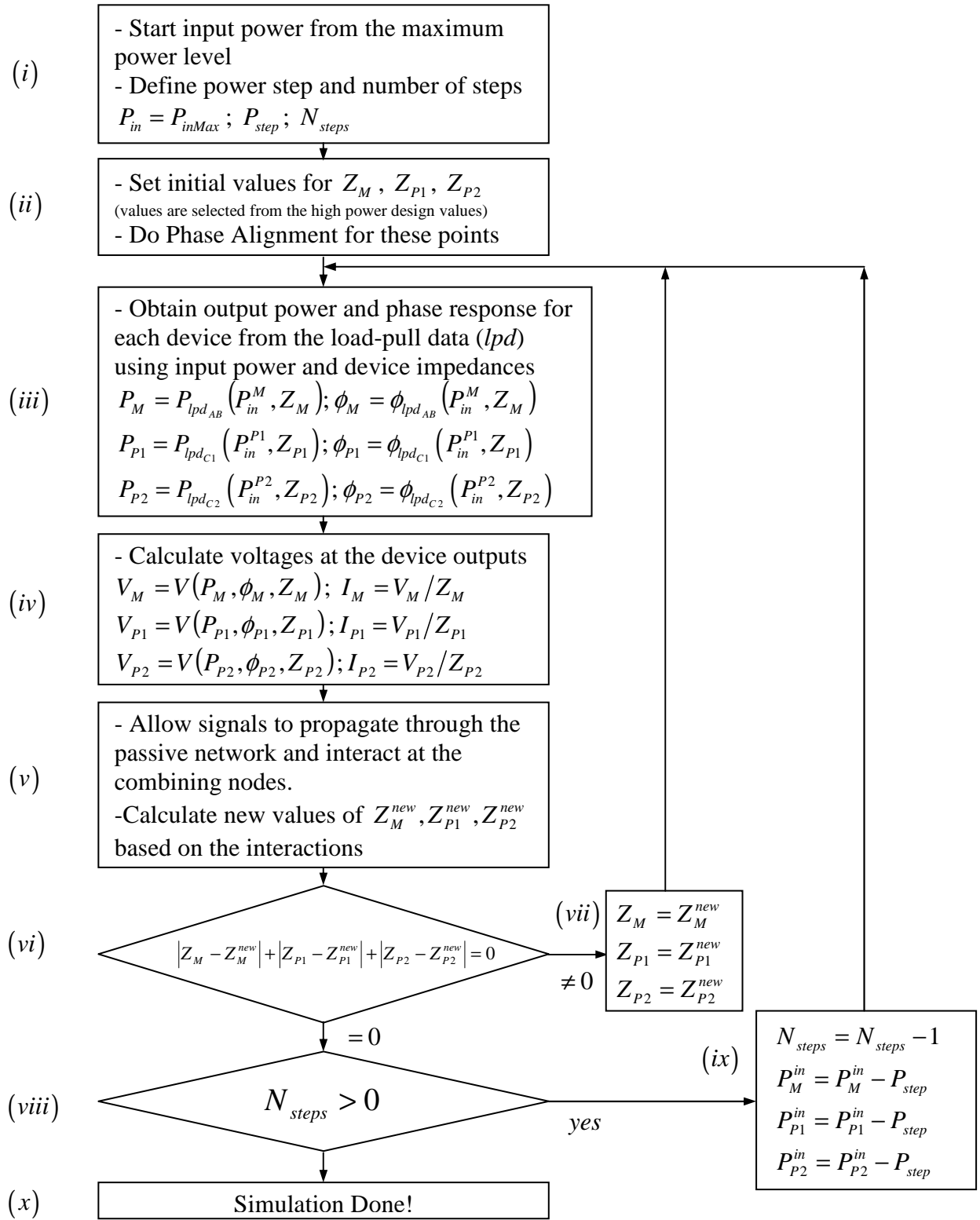


Figure 93: Three-way Doherty analysis flow chart

If the design is done using technique of Figure 77, then the initial  $Z_M$ ,  $Z_{P_1}$  and  $Z_{P_2}$  values will be, respectively, equal to the final values of  $Z_{MP}$ ,  $Z_{PP_1}$ , and  $Z_{PP_2}$  from the design technique. If an external design is used (that is, a design done using some other technique), then educated guesses for the impedance values  $Z_{MP}$ ,  $Z_{PP_1}$ , and  $Z_{PP_2}$  are used to start the iterative process. For each subsequent iteration of the outer loop, the steady-state main and peak output matching network impedance levels  $Z_M^{new}$ ,  $Z_{P_1}^{new}$ , and  $Z_{P_2}^{new}$  determined during the previous outer-loop iteration are retained as the initial values for the first iteration of the inner loop.

In particular, the analysis procedure begins with initialization of the input power level  $P_{in}$  to the maximum power level  $P_{inMax}$  [Figure 93 block (i)]. Based on the known power split performed by the input power splitter, the magnitudes of the main branch input power level  $P_{IN}^M$  and the two peak branch input power levels  $P_{IN}^{P_1}$  and  $P_{IN}^{P_2}$  can be determined from the input power level  $P_{in}$  and calculated input splitter ratios (146), (147), (148). In addition,  $P_{step}$  of each power level decrement, and the number  $N_{step}$  of such decrements for the analysis, is specified in the same block. Note that, for this explanation, all powers are expressed in *dBm* or other suitable relative units.

Next [Figure 93 block (ii)] the impedance value  $Z_M$  presented to the main amplifier device and the impedance values  $Z_{P_1}$ , and  $Z_{P_2}$  presented to the first and second peak amplifier devices, respectively, are initialized to values for high-power operations determined during design technique of Figure 77. In addition, phase alignments for the main and peak branches are performed during this step. Equation (145) is used to calculate the phase delay of each S-parameter block within each branch under the varying load conditions that they experience during the amplifier operation. The sum of the phase delays for each S-parameter block in a branch will give the overall phase delay for the branch. Since there are three branches, and we want the signals to combine at the combining nodes under specified phase conditions (in-phase or otherwise specified phase relation), the phase of each peak branch may need to be adjusted with respect to the main branch to achieve the specified phase conditions.

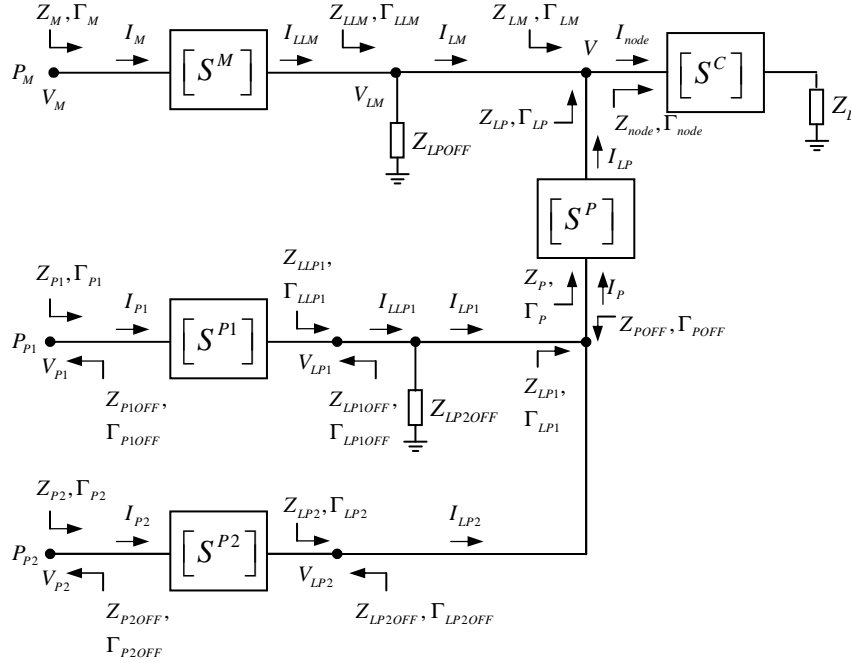
If the proper design impedances are not known, e.g., because the amplifier was designed using a technique other than design technique of Figure 77, then the phase alignment needs to be initialized to a plausible value as well and we need to go through iterations to achieve convergence. Looking at the constant input power load-pull contours for the main and each of the peak devices, the most plausible values for impedances  $Z_M$ ,  $Z_{P1}$ , and  $Z_{P2}$  for high-power performance are determined. The phase offset needed for an in-phase combining condition is then determined by observing the initial phase mismatch of the calculated currents at the combining node and using it to obtain convergence for this initial value of the input power. The technique does not yet proceed to a full input power sweep. Changes are made in phase alignment if necessary and the convergence is repeated at the initial input power level. This is done until a desirable phase alignment is achieved. Only then does the technique proceed to the full input power sweep.

In the next step [Figure 93 block (iii)], the output power  $P_M$  and phase response  $\phi_M$  of the main amplifier device are determined from the load-pull data (e.g.,  $P_{lpdAB}$ ,  $\phi_{lpdAB}$  for the main device biased in Class-AB) using the main branch input power level  $P_{IN}^M$  and the main amplifier device impedance level  $Z_M$ . The power and phase values are read from the load-pull power sweeps. These parameters are directly measured in the active device load-pull process with some level of interpolation possibly involved. Similarly, the output powers  $P_{P1}$  and  $P_{P2}$ , as well as phase responses  $\phi_{P1}$ , and  $\phi_{P2}$  of both peak amplifier devices are determined from the load-pull data (e.g.,  $P_{lpdC1}$ ,  $\phi_{lpdC1}$  for the first peak device biased in shallow class-C, and  $P_{lpdC2}$ ,  $\phi_{lpdC2}$  for the second peak device biased in deep class-C<sup>52</sup>) using the peak branch input powers level  $P_{IN}^{P1}$  and  $P_{IN}^{P2}$  as well as the peak amplifier device impedance levels  $Z_{P1}$  and  $Z_{P2}$ .

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<sup>52</sup> The onset of the conduction for the two peak devices in the three-way Doherty needs to be staggered to maintain high efficiency of operation for backed-off power levels. The first peak device biased in shallow class-C will turn on at a lower power level than the second peak device biased in deep class-C.

Next [Figure 93 block (iv)] the voltages  $V_M$ ,  $V_{P1}$ , and  $V_{P2}$  along with corresponding currents  $I_M$ ,  $I_{P1}$ , and  $I_{P2}$  from the main and both peak amplifier devices are determined.



**Figure 94: Schematic of the three-way Doherty output combining network with associated notation**

Figure 94 shows a block diagram representing passive output combining network of the three-way Doherty amplifier. In Figure 94, loads  $Z_{LPOFF}$  and  $Z_{LP2OFF}$  represent the combined peak loading on the main branch contributed by both peak branches in the inactive state, and the loading on the first peak branch from the second peak branch in the inactive state, respectively.

For the main branch going from the main device toward the combining node, calculations for converting the main device impedance  $Z_M$  into the main voltage reflection coefficient  $\Gamma_M$ , and vice versa, are given by

$$(217) \quad Z_M = Z_0 \frac{1 + \Gamma_M}{1 - \Gamma_M} = \frac{V_M}{I_M} = |Z_M| e^{j\phi_{Z_M}} \quad \Gamma_M = \frac{Z_M - Z_0}{Z_M + Z_0}$$

The complex power  $S_M$  of the main device has a real part  $P_M$  that is known from the load-pull data and an imaginary part  $Q_M$  that is unknown. However,  $S_M$  is also given

by  $\frac{|V_M|^2}{2Z'_M}$ <sup>53</sup> in which the impedance  $Z_M$  is known from the load-pull data. Known values of  $P_M$  and  $Z_M$  allow the calculation of  $V_M$  and  $I_M = \frac{V_M}{Z_M}$ , which are used in the circuit analysis of output combining network. As such, the complex power  $S_M$  of the main device is given by

$$(218) \quad S_M = P_M + jQ_M = \frac{|V_M|^2}{2Z'_M} = \frac{|I_M|^2 Z_M}{2} = \frac{V_M I'_M}{2}$$

and the voltage  $V_M$  of the main device is then

$$(219) \quad V_M = |V_M| e^{j\phi_M} = \sqrt{\frac{2P_M}{\text{Re}\{Z_M\}}} |Z_M| e^{j\phi_M}$$

We are at liberty to select the phase of  $V_M$  as the reference phase, and so can (without loss of generality) set  $\phi_M = 0$ . Then (219) becomes

$$(220) \quad V_M = \sqrt{\frac{2P_M}{\text{Re}\{Z_M\}}} |Z_M|$$

Once the voltages and currents on the device side for each branch are known, currents on the node side of each branch can be determined, which enables the calculation of the loading impedances for each branch and in turn allow for the calculation of new impedances presented to the devices. The signals are allowed to propagate through the passive network formed by the main and the first and second peak output matching networks, the common peak matching network, the node matching network, and output load, and new values  $Z_M^{new}$ ,  $Z_{P1}^{new}$ , and  $Z_{P2}^{new}$  for the main and both peak amplifier devices impedance levels are determined [Figure 93 block (v)].

Since  $V_M$ ,  $I_M$ ,  $Z_M$ , and  $\Gamma_M$  are known on the device side of the main output matching network and the S-parameters  $[S^M]$  of the network are known as well,  $V_{LLM}$ ,  $I_{LLM}$ ,  $Z_{LLM}$ , and  $\Gamma_{LLM}$  can be calculated on the node side of network in the manner

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<sup>53</sup> Note that prime denotes complex conjugation

detailed below. The relation between  $\Gamma_M$  and  $\Gamma_{LLM}$  is derived from the definition of the S-parameters (Figure 71) and given by

$$(221) \quad \Gamma_M = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LLM}}{1 - S_{22}^M \Gamma_{LLM}}; \quad \Gamma_{LLM} = \frac{\Gamma_M - S_{11}^M}{S_{12}^M S_{21}^M + S_{22}^M (\Gamma_M - S_{11}^M)};$$

$$Z_{LLM} = Z_0 \frac{1 + \Gamma_{LLM}}{1 - \Gamma_{LLM}}$$

Using expression (143),  $V_{LM}$  can be expressed in terms of  $V_M$ , and used to calculate  $I_{LLM}$  according to

$$(222) \quad V_{LM} = \frac{S_{21}^M (1 + \Gamma_{LLM}) V_M}{1 + S_{11}^M - (S_{22}^M + S_{11}^M S_{22}^M - S_{12}^M S_{21}^M) \Gamma_{LLM}}; \quad I_{LLM} = \frac{V_{LM}}{Z_{LLM}}$$

Calculations to obtain  $Z_{LPOFF}$  are done to account for the combined loading effect at the main combining node due to the off-state impedances of the two peak devices transformed through their respective peak matching networks and the common peak matching network. From the first peak device side, the off-state impedance  $Z_{P1OFF}$  of the first peak device is transformed into  $Z_{LP1OFF}$  at the load side of the first peak matching network as follows

$$(223) \quad \Gamma_{P1OFF} = \frac{Z_{P1OFF} - Z_0}{Z_{P1OFF} + Z_0}; \quad \Gamma_{LP1OFF} = S_{22}^{P1} + \frac{S_{12}^{P1} S_{12}^{P1} \Gamma_{P1OFF}}{1 - S_{11}^{P1} \Gamma_{P1OFF}};$$

$$Z_{LP1OFF} = Z_0 \frac{1 + \Gamma_{LP1OFF}}{1 - \Gamma_{LP1OFF}}$$

From the second peak device side, the off-state impedance  $Z_{P2OFF}$  of the second peak device is transformed into  $Z_{LP2OFF}$  at the load side of the second peak matching network as follows:

$$(224) \quad \Gamma_{P2OFF} = \frac{Z_{P2OFF} - Z_0}{Z_{P2OFF} + Z_0}; \quad \Gamma_{LP2OFF} = S_{22}^{P2} + \frac{S_{12}^{P2} S_{12}^{P2} \Gamma_{P2OFF}}{1 - S_{11}^{P2} \Gamma_{P2OFF}};$$

$$Z_{LP2OFF} = Z_0 \frac{1 + \Gamma_{LP2OFF}}{1 - \Gamma_{LP2OFF}}$$

From the device side of the common peak network, the combined off-state impedance  $Z_{POFF}$ , which is a parallel combination of  $Z_{LP1OFF}$  and  $Z_{LP2OFF}$  given by (225), is transformed into  $Z_{LPOFF}$  loading the main branch given by(226)

$$(225) \quad Z_{POFF} = \frac{Z_{LP1OFF}Z_{LP2OFF}}{Z_{LP1OFF} + Z_{LP2OFF}}; \quad \Gamma_{POFF} = \frac{Z_{POFF} - Z_0}{Z_{POFF} + Z_0};$$

and

$$(226) \quad \Gamma_{LPOFF} = S_{22}^P + \frac{S_{12}^P S_{12}^P \Gamma_{POFF}}{1 - S_{11}^P \Gamma_{POFF}}; \quad Z_{LPOFF} = Z_0 \frac{1 + \Gamma_{LPOFF}}{1 - \Gamma_{LPOFF}}$$

The main branch load impedance  $Z_{LM}$  is expressed in terms of  $Z_{LLM}$  and  $Z_{LPOFF}$ , where  $Z_{LLM}$  is given by a parallel connection of  $Z_{LM}$  and  $Z_{LPOFF}$ . The main branch load current  $I_{LM}$  entering the combining node is derived from the current  $I_{LLM}$  entering the current divider formed by  $Z_{LM}$  and  $Z_{LPOFF}$  as follows

$$(227) \quad Z_{LM} = \frac{Z_{LLM}Z_{LOFF}}{Z_{LOFF} - Z_{LLM}}; \quad I_{LM} = \frac{Z_{LPOFF} - Z_{LLM}}{Z_{LPOFF}} I_{LLM}$$

For the first peak branch going from the peak device toward the combining node, calculations for converting the peak device impedance  $Z_{p1}$  into the corresponding voltage reflection coefficient  $\Gamma_{p1}$ , and vice versa, are given by

$$(228) \quad Z_{p1} = Z_0 \frac{1 + \Gamma_{p1}}{1 - \Gamma_{p1}} = \frac{V_{p1}}{I_{p1}} = |Z_{p1}| e^{j\phi_{Z_{p1}}} \quad \Gamma_{p1} = \frac{Z_{p1} - Z_0}{Z_{p1} + Z_0}$$

The complex power  $S_{p1}$  of the first peak device has a real part  $P_{p1}$  that is known from the load-pull data and an imaginary part  $Q_{p1}$  that is unknown. However,  $S_{p1}$  is also given by

$\frac{|V_{p1}|^2}{2Z'_{p1}}$  in which the impedance  $Z_{p1}$  is known from the load-pull data. Known values of

$P_{p1}$  and  $Z_{p1}$  allow for the calculation of  $V_{p1}$  and  $I_{p1} = \frac{V_{p1}}{Z_{p1}}$ , which are used in the circuit

analysis of output combining network.

As such, the complex power  $S_{P_1}$  of the peak device is given by

$$(229) \quad S_{P_1} = P_{P_1} + jQ_{P_1} = \frac{|V_{P_1}|^2}{2Z'_{P_1}} = \frac{|I_{P_1}|^2 Z_{P_1}}{2} = \frac{V_{P_1} I'_{P_1}}{2}$$

The first peak device voltage  $V_{P_1}$  is calculated from the known first peak device power  $P_{P_1}$  and first peak device impedance  $Z_{P_1}$  (complex power  $S_{P_1}$  is fully determined by known  $P_{P_1}$  and  $Z_{P_1}$ ) as follows

$$(230) \quad V_{P_1} = |V_{P_1}| e^{j\phi_{P_1}} = \sqrt{\frac{2P_{P_1}}{\text{Re}\{Z_{P_1}\}}} |Z_{P_1}| e^{j\phi_{P_1}}$$

Since  $V_{P_1}$ ,  $I_{P_1}$ ,  $Z_{P_1}$ , and  $\Gamma_{P_1}$  are known on the device side of the first peak output matching network and the S-parameters  $[S^{P_1}]$  of the network are known,  $V_{LP_1}$ ,  $I_{LP_1}$ ,  $Z_{LP_1}$ , and  $\Gamma_{LP_1}$  can be calculated on the node side of the first peak network by using the expressions (231), (232), (233). The manner in which the first peak device expressions are derived is similar to that used for the main branch expression derivations.

$$(231) \quad \Gamma_{P_1} = S_{11}^{P_1} + \frac{S_{12}^{P_1} S_{21}^{P_1} \Gamma_{LLP_1}}{1 - S_{22}^{P_1} \Gamma_{LLP_1}} \quad \Rightarrow \quad \Gamma_{LLP_1} = \frac{\Gamma_{P_1} - S_{11}^{P_1}}{S_{12}^{P_1} S_{21}^{P_1} + S_{22}^{P_1} (\Gamma_{P_1} - S_{11}^{P_1})};$$

$$Z_{LLP_1} = Z_0 \frac{1 + \Gamma_{LLP_1}}{1 - \Gamma_{LLP_1}}$$

$$(232) \quad V_{LP_1} = \frac{S_{21}^{P_1} (1 + \Gamma_{LLP_1}) V_{P_1}}{1 + S_{11}^{P_1} - (S_{22}^{P_1} + S_{11}^{P_1} S_{22}^{P_1} - S_{12}^{P_1} S_{21}^{P_1}) \Gamma_{LLP_1}}; \quad I_{LLP_1} = \frac{V_{LP_1}}{Z_{LLP_1}}$$

$$(233) \quad Z_{LP_1} = \frac{Z_{LLP_1} Z_{LP1OFF}}{Z_{LP1OFF} - Z_{LLP_1}}; \quad I_{LP_1} = \frac{Z_{LP1OFF} - Z_{LLP_1}}{Z_{LP1OFF}} I_{LLP_1}$$

For the second peak branch going from the peak device toward the peak combining node, the calculations for converting the peak device impedance  $Z_{P2}$  into the peak voltage reflection coefficient  $\Gamma_{P2}$ , and vice versa, are given by

$$(234) \quad Z_{P2} = Z_0 \frac{1 + \Gamma_{P2}}{1 - \Gamma_{P2}} = \frac{V_{P2}}{I_{P2}} = |Z_{P2}| e^{j\phi_{Z_{P2}}} \quad \Gamma_{P2} = \frac{Z_{P2} - Z_0}{Z_{P2} + Z_0}$$

The complex power  $S_{P2}$  of the second peak device has a real part  $P_{P2}$  that is known from the load-pull data and an imaginary part  $Q_{P2}$  that is unknown. However,  $S_{P2}$  is also given by  $\frac{|V_{P2}|^2}{2Z'_{P2}}$  in which the impedance  $Z_{P2}$  is known from the load-pull data. Known values

of  $P_{P2}$  and  $Z_{P2}$  allow for the calculation of  $V_{P2}$  and  $I_{P2} = \frac{V_{P2}}{Z_{P2}}$ , which are used in the circuit analysis of output combining network. As such, the complex power  $S_{P2}$  of the second peak device is given by

$$(235) \quad S_{P2} = P_{P2} + jQ_{P2} = \frac{|V_{P2}|^2}{2Z'_{P2}} = \frac{|I_{P2}|^2 Z_{P2}}{2} = \frac{V_{P2} I'_{P2}}{2}$$

The second peak device voltage  $V_{P2}$  is calculated from the known second peak device power  $P_{P2}$  and the second peak device impedance  $Z_{P2}$  (complex power  $S_{P2}$  is fully determined by known  $P_{P2}$  and  $Z_{P2}$ ) as follows.

$$(236) \quad V_{P2} = |V_{P2}| e^{j\phi_{P2}} = \sqrt{\frac{2P_{P2}}{\text{Re}\{Z_{P2}\}}} |Z_{P2}| e^{j\phi_{P2}}$$

Since  $V_{P2}$ ,  $I_{P2}$ ,  $Z_{P2}$ , and  $\Gamma_{P2}$  are known on the device side of the second peak output matching network and the S-parameters  $[S^{P2}]$  of the network,  $V_{LP2}$ ,  $I_{LP2}$ ,  $Z_{LP2}$ , and  $\Gamma_{LP2}$  can be calculated on the peak node side of the network by using the expressions (237), (238), which result from circuit analysis. The manner in which the second peak device expressions are derived is similar to that used for the main branch expression derivations.

$$(237) \quad \Gamma_{P2} = S_{11}^{P2} + \frac{S_{12}^{P2} S_{21}^{P2} \Gamma_{LP2}}{1 - S_{22}^{P2} \Gamma_{LP2}}; \quad \Rightarrow \quad \Gamma_{LP2} = \frac{\Gamma_{P2} - S_{11}^{P2}}{S_{12}^{P2} S_{21}^{P2} + S_{22}^{P2} (\Gamma_{P2} - S_{11}^{P2})};$$

$$Z_{LP2} = Z_0 \frac{1 + \Gamma_{LP2}}{1 - \Gamma_{LP2}}$$

$$(238) \quad V_{LP2} = \frac{S_{21}^{P2} (1 + \Gamma_{LP2}) V_{P2}}{1 + S_{11}^{P2} - (S_{22}^{P2} + S_{11}^{P2} S_{22}^{P2} - S_{12}^{P2} S_{21}^{P2}) \Gamma_{LP2}}; \quad I_{LP2} = \frac{V_{LP2}}{Z_{LP2}}$$

The device side impedance  $Z_P$  and voltage  $V_P$  of the common peak matching network are calculated from the known load side impedances  $Z_{LP1}$ ,  $Z_{LP2}$  and currents  $I_{LP1}$ ,  $I_{LP2}$  from the first and the second peak branches as follows:

$$(239) \quad Z_P = \frac{Z_{LP1} Z_{LP2}}{Z_{LP1} + Z_{LP2}}; \quad \Gamma_P = \frac{Z_P - Z_0}{Z_P + Z_0}; \quad V_P = (I_{LP1} + I_{LP2}) Z_P$$

From the known  $V_P$ ,  $Z_P$ , and  $\Gamma_P$  on the device side of the common peak output matching network and the S-parameters  $[S^P]$  of the network,  $V_{LP}$ ,  $I_{LP}$ ,  $Z_{LP}$ , and  $\Gamma_{LP}$  can be calculated on the main node side of the network by using the expressions below. The manner in which the common peak device expressions are derived is similar to that used for the main branch expression derivations.

$$(240) \quad \Gamma_P = S_{11}^P + \frac{S_{12}^P S_{21}^P \Gamma_{LP}}{1 - S_{22}^P \Gamma_{LP}} \Rightarrow \quad \Gamma_{LP} = \frac{\Gamma_P - S_{11}^P}{S_{12}^P S_{21}^P + S_{22}^P (\Gamma_P - S_{11}^P)};$$

$$Z_{LP} = Z_0 \frac{1 + \Gamma_{LP}}{1 - \Gamma_{LP}}$$

$$(241) \quad V_{LP} = \frac{S_{21}^P (1 + \Gamma_{LP}) V_P}{1 + S_{11}^P - (S_{22}^P + S_{11}^P S_{22}^P - S_{12}^P S_{21}^P) \Gamma_{LP}}; \quad I_{LP} = \frac{V_{LP}}{Z_{LP}}$$

The  $Z_{node}$  calculation is the result of an impedance transformation through the node network with known S-parameters.

$$(242) \quad \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}; \quad \Gamma_{node} = S_{11}^C + \frac{S_{12}^C S_{21}^C \Gamma_L}{1 - S_{22}^C \Gamma_L}; \quad Z_{node} = Z_0 \frac{1 + \Gamma_{node}}{1 - \Gamma_{node}}$$

The new main and common peak branch load impedances  $Z_{LM}$ ,  $Z_{LLM}$ , and  $Z_{LP}$  are calculated using the newly calculated main combining node voltage  $V$  and currents  $I_{LM}$ ,  $I_{LP}$  as follows

$$(243) \quad V = (I_{LM} + I_{LP})Z_{node}; \quad Z_{LM} = \frac{V}{I_{LM}}; \quad Z_{LP} = \frac{V}{I_{LP}}$$

$$Z_{LLM} = \frac{Z_{LM}Z_{LPOFF}}{Z_{LM} + Z_{LPOFF}}; \quad \Gamma_{LLM} = \frac{Z_{LLM} - Z_0}{Z_{LLM} + Z_0};$$

The new main and common peak device side impedances  $Z_M$  and  $Z_P$  are calculated based on the new main and common peak branch load impedances  $Z_{LLM}$  and  $Z_{LP}$  by transforming these impedances through the main and common peak output matching networks back to the main and common peak device side to obtain the new device-side impedances  $Z_M$  and  $Z_P$ , respectively.

$$(244) \quad \Gamma_M = S_{11}^M + \frac{S_{12}^M S_{21}^M \Gamma_{LLM}}{1 - S_{22}^M \Gamma_{LLM}}; \quad Z_M = Z_0 \frac{1 + \Gamma_M}{1 - \Gamma_M}$$

$$(245) \quad \Gamma_{LP} = \frac{Z_{LP} - Z_0}{Z_{LP} + Z_0}; \quad \Gamma_P = S_{11}^P + \frac{S_{12}^P S_{21}^P \Gamma_{LP}}{1 - S_{22}^P \Gamma_{LP}}; \quad Z_P = Z_0 \frac{1 + \Gamma_P}{1 - \Gamma_P}$$

The new first peak and second peak branch load impedances  $Z_{LP1}$ ,  $Z_{LLP1}$ , and  $Z_{LP2}$  are calculated using the newly calculated main node voltage  $V_P$  and currents  $I_{LP1}$ ,  $I_{LP2}$  as follows:

$$(246) \quad V_P = (I_{LP1} + I_{LP2})Z_P$$

$$(247) \quad Z_{LP1} = \frac{V_P}{I_{LP1}}; \quad Z_{LLP1} = \frac{Z_{LP1}Z_{LP1OFF}}{Z_{LP1} + Z_{LP1OFF}}; \quad \Gamma_{LLP1} = \frac{Z_{LLP1} - Z_0}{Z_{LLP1} + Z_0}$$

The new first peak and second peak device side impedances  $Z_{P1}$  and  $Z_{P2}$  are calculated based on the new first peak and second peak branch load impedances  $Z_{LLP1}$  and  $Z_{LP2}$  by transforming these impedances through the first peak and the second peak output matching networks back to the first peak and second peak device side to obtain new device-side impedances  $Z_{P1}$  and  $Z_{P2}$ , respectively.

$$(248) \quad \Gamma_{P1} = S_{11}^{P1} + \frac{S_{12}^{P1} S_{21}^{P1} \Gamma_{LLP1}}{1 - S_{22}^{P1} \Gamma_{LLP1}}; \quad Z_{P1} = Z_0 \frac{1 + \Gamma_{P1}}{1 - \Gamma_{P1}}$$

$$(249) \quad Z_{LP2} = \frac{V_P}{I_{LP2}}; \quad \Gamma_{LP2} = \frac{Z_{LP2} - Z_0}{Z_{LP2} + Z_0};$$

$$\Gamma_{P2} = S_{11}^{P2} + \frac{S_{12}^{P2} S_{21}^{P2} \Gamma_{LP2}}{1 - S_{22}^{P2} \Gamma_{LP2}}; \quad Z_{P2} = Z_0 \frac{1 + \Gamma_{P2}}{1 - \Gamma_{P2}}$$

It is next determined whether the new main and peak amplifier devices impedance levels  $Z_M^{new}$ ,  $Z_{P1}^{new}$ , and  $Z_{P2}^{new}$  sufficiently match the corresponding previous impedance levels  $Z_M$ ,  $Z_{P1}$ , and  $Z_{P2}$  [Figure 93 block (vi)]. This is done by determining whether the corresponding values are equal to within a specified threshold level. If the different pairs of impedance levels do not all agree sufficiently closely, it means that the inner loop is not yet complete and processing continues to the next step [Figure 93 block (vii)], where the main and peak amplifier device impedance levels  $Z_M$ ,  $Z_{P1}$ , and  $Z_{P2}$  are updated to be equal to the new values  $Z_M^{new}$ ,  $Z_{P1}^{new}$ , and  $Z_{P2}^{new}$  determined in the previous step. Processing then iterates using the updated impedance levels. If it is determined that the different pairs of impedance levels do in fact sufficiently well, then the inner loop is complete for the current input power level  $P_{in}$ , and processing continues to determine whether the number  $N_{steps}$  of remaining steps is greater than zero [Figure 93 block (viii)]. If the number of steps is greater than zero, then the outer loop is not yet complete, and processing continues to the next step [Figure 93 block (ix)], where the number of steps, and the main and peak branch input power levels, are decremented for the next iteration of the outer loop. Processing then returns to repeat steps of the inner loop (Figure 93

blocks (iii) through (vi)) for the new outer-loop iteration. If it is determined that the number of steps  $N_{steps}$  has reached zero, then the analysis algorithm is complete and processing terminates. For every instance of the inner loop convergence the output power, gain, efficiency, compression, and other relevant performance parameters of the two-way Doherty amplifier and its constituent devices are calculated from the interpolated device load-pull data, and calculated currents and voltages in the passive portion of the network. The results are tabulated and can be readily displayed.

Note that Doherty amplifiers designed using design technique summarized in Figure 77 can be analyzed using the analysis technique of Figure 93 and/or using any other suitable analysis technique. Similarly, the analysis technique can be used to analyze Doherty amplifiers designed using any other suitable design technique. Although design technique and analysis technique have been described in the context of three-way Doherty amplifiers, in general those techniques can be extended to apply to  $N$ -way Doherty amplifiers having a main amplifier branch and  $(N-1)$  peak amplifier branches.

Although the analysis technique has been described in the context of fixed input conditioning, it can be applied to other implementations, such as static adjustable input conditioning and dynamic input conditioning. Static adjustable input conditioning implies that the amplitude ratio of the input signals, and their phase relationship, are adjusted for one power level at a frequency of interest. The user can specify a change of input settings with frequency. Dynamic adjustable input conditioning implies that the amplitude ratio of the input signals, and their phase relationship, are specified for all power levels and frequencies of interest. The user can specify a change of input settings with power and frequency. Each of the three different scenarios has its own set of goals and restrictions, and they can all be addressed using the principles and calculations of Chapter 5 (for design) and the present Chapter (for analysis purposes).

## **6.6 Conclusions**

Analysis procedures for fixed input power two-way and three-way (extendable to N-way) Doherty amplifiers as well as two-way digital Doherty amplifier based on active device load-pull data and known S-parameters of the matching networks within the Doherty amplifier topology are presented. These iterative analysis procedures allow us to obtain the performance parameters of the Doherty amplifiers such as output power, gain, gain linearity, efficiency, device compression levels, branch phase alignment, spectral performance, etc. The analysis procedures presented here are complementary to the synthesis techniques presented in Chapter 5 in the process of Doherty amplifier design. They are formulated to handle the load impedance modulation and active device off-state conditions that are specific for Doherty amplifier architecture.

The circuit analysis yields both input/output power sweep response as well as amplifier frequency response thus providing the designer with adequate amount of information to assess the amplifier's performance with a high degree of certainty without necessity of building physical prototypes. The performance of the amplifier excited by pulsed-CW or modulated RF signals can be assessed.

Standard circuit simulators rely on active device models that may not be available immediately when new devices enter the production and thus the designer may not have the ability to use commercial simulators to verify the amplifiers performance. Also models may not be as accurate and they do not necessarily reflect the device performance variation due to production process variability which is important in yield analysis (some model parameters may be available for yield analysis but not always).

## **6.7 References for Chapter 6**

- [65] J. Liu, L. P. Dunleavy, H. Arslan, "Large-Signal Behavioral Modeling of Nonlinear Amplifiers Based on Load-Pull AM-AM and AM-PM Measurements", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 54, No. 8, August 2006, pp. 3191-3196
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- [67] M. N. Marbell, M. Simcoe, R. Wilson, M. Chidurala, S. Ward, "A Load-Pull-based Behavioral Model for Doherty PA Design", 978-1-61284 11 2011 IEEE

## Chapter 7

### 7 General conclusions

#### 7.1 *Summary of the Contributions of the Thesis*

The principal contributions of this thesis are as follows:

- Compact versions of N-way Doherty amplifiers have been introduced for the first time. Although this new idea is based on non-explicit use of impedance inverters and offset lines to form the output sections of the amplifier branches, it is more than this. It allows one to achieve the best impedance modulation through optimization process rather than preconceived notions of what the constituent parts (namely inverters and offset lines) must separately do before being cascaded. This has been demonstrated both in simulation and experimentally in Chapter 4 for compact two-way and three-way Doherty amplifiers.
- There are many ways to extend the two-way Doherty amplifier configuration into an N-way Doherty architecture, until now insufficient attention appears to have been paid to determining which is the best one as far as the resulting performance is concerned. We have shown through analysis in Chapter 4 which configuration is the superior to all others.
- A greatly improved design procedure for N-way Doherty amplifiers has been developed. It is novel in the sense that it uses accurate characterization of the constituent active devices using vector load-pull measurements, provides a consistent set of design requirements, generates representative S-parameter models for all functional blocks of the amplifier architecture subject to performance specification and Doherty architecture related constraints, and allows designer to focus on the architecture performance optimization (amplifier can be designed literally by a few clicks of a mouse). Once the amplifier has been

optimized through a number of quick design iterations, only then the designer proceeds to implement the actual amplifier circuit.

- An accompanying new N-way Doherty analysis technique that allows for complete performance analysis of N-way Doherty amplifiers ('complete' being the key word) has been presented. It uses active device load-pull data and S-parameters representation of the passive part of the amplifier network to simulate the performance of the amplifier without the need to implement circuitry. This allows the designer to explore interaction of various parameters that influence the performance of the amplifier and to find the best combination that suits the performance specifications the best.

**Some of the secondary contributions of the thesis are as follows:**

- Transcoupler element has been introduced, and its application in Digital Doherty amplifiers has been demonstrated.
- Use of circulators as tunable impedance inverters was presented along with their application in two-way Doherty amplifiers

## **7.2 Future Work**

- Even though we found that fundamental load-pull was sufficiently accurate to provide good agreement between simulated and measured performance of the amplifiers designed using methods presented in this thesis, the harmonic load-pull may be worth pursuing in the cases where the performance requirements are very demanding.
- Expand analysis of Chapter 6 beyond three-way Doherty and try to determine practical limits for N in an N-way Doherty.

## Appendix A: A Note on Certain Circuit Analyses

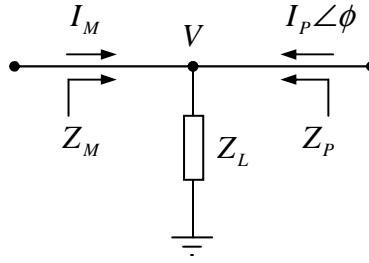


Figure D.1 : Current combining node notation

In the circuit analysis in Section 3.2.2, Section 5.3.2, Section 6.3, as well as Section 6.5, we perform a circuit analysis in a manner that might seem to ignore the phasor properties of the currents. That this is not so is clarified in this appendix.

If the current  $I_M$  in the main branch is used as a reference it may be assumed to be real. We can write the current in the peak branch as  $I_P \angle \phi$ . In other words, the peak branch current has some phase offset  $\phi$  with respect to the main current  $I_M$ . With this phase shown explicitly  $I_P$  will be the magnitude of the peak current and so is a real quantity. The voltage at the node is then

$$V = (I_M + I_P \angle \phi) Z_L$$

and hence the impedance seen by the main branch is

$$Z_M = \frac{V}{I_M} = \frac{I_M + I_P \angle \phi}{I_M} Z_L = \left( 1 + \frac{I_P}{I_M} \angle \phi \right) Z_L$$

The impedance seen by the peak branch is

$$Z_P = \frac{V}{I_P \angle \phi} = \frac{I_M + I_P \angle \phi}{I_P \angle \phi} Z_L = \left( 1 + \frac{I_M}{I_P} \angle -\phi \right) Z_L$$

When  $I_M = I_P$  and there is in-phase combining (that is,  $\phi = 0^\circ$ ) we have

$$Z_M = \frac{V}{I_M} = \frac{I_M + I_M \angle 0^\circ}{I_M} Z_L = 2Z_L$$

and

$$Z_P = \frac{V}{I_P \angle \phi} = \frac{I_M + I_M \angle 0^\circ}{I_M \angle 0^\circ} Z_L = 2Z_L = Z_M$$

In other words, the main and peak branch impedances are equal (and real if  $Z_L$  is real).

When  $I_M = I_P$  and there is out-of-phase combining ( $\phi \neq 0^\circ$ ) we have

$$Z_M = \frac{V}{I_M} = \frac{I_M + I_M \angle \phi}{I_M} Z_L = (1 + 1 \angle \phi) Z_L$$

and

$$Z_P = \frac{V}{I_P \angle \phi} = \frac{I_M + I_M \angle \phi}{I_M \angle \phi} Z_L = (1 + 1 \angle -\phi) Z_L = Z'_M$$

In other words the main and peak branch impedances are complex conjugates of each other (if  $Z_L$  is real).

More generally, if we have  $I_P = kI_M$  (where  $0 \leq k < 1$ ) and we have out-of-phase combining ( $\phi \neq 0^\circ$ ) we have

$$Z_M = \frac{V}{I_M} = \frac{I_M + kI_M \angle \phi}{I_M} Z_L = (1 + k \angle \phi) Z_L$$

and

$$Z_P = \frac{V}{I_P \angle \phi} = \frac{I_M + I_M \angle \phi}{I_M \angle \phi} Z_L = \left(1 + \frac{1}{k} \angle -\phi\right) Z_L$$

So the main branch impedance will have a smaller reactive component of the opposite sign to that of the peak branch impedance. If the main branch impedance is inductive the peak branch impedance will be capacitive, and vice-versa. But the peak branch impedance will be more reactive than the main branch impedance in either situation, assuming  $Z_L$  is real.

We can always compensate for the phase difference by appropriately adjusting the input phase of the peak device (by means of an offset line or a phase shifter) and restore in-phase combining of currents (to maximize power delivered and keep impedances real). In the analysis that is done in the section of the thesis mentioned at the start of this appendix the in-phase condition is assumed. Not only does this simplify the analysis, but this condition is also a goal of the design process.