ACTIVE TUNING ELEMENTS FOR INTEGRATED
BROADCAST FREQUENCY RECEIVERS

by

C. S. Yap

Submitted in partial fulfillment of the requirements for the degree of Master of Science

Department of Electrical Engineering,
Faculty of Pure and Applied Science,
The University of Ottawa,
Ottawa, Canada
© C. S. Yap 1972
ACTIVE TUNING ELEMENTS FOR INTEGRATED
BROADCAST FREQUENCY RECEIVERS
ABSTRACT

Recent developments in phase-locked loop systems have permitted the complete integration of broadcast receivers, except for antenna tuning. This thesis investigates techniques, for tuning the antenna, which are compatible with integrated circuit technology. In particular, forms of immittance converter are studied and their performance evaluated in relation to the above application. It is concluded that a new current-amplifier form of positive immittance converter provides a reasonable compromise between the requirements of the tuning system and the integrated circuit technology.
ACKNOWLEDGEMENT

The author wishes to express his sincere thanks to his thesis supervisor Professor P. M. Thompson for his patient guidance and encouragement in the preparation of this thesis, Mr. W. Peil of the General Electric Company, Advanced Research Laboratory, Syracuse, N.Y. for the formulation of the problem investigated and Mr. J. G. Mlacak of Bell Northern Research for encouragement in completing the thesis while the author was employed by his company.
LIST OF SYMBOLS

A  one amplifier immittance amplifier feedback factor
B  total loop gain of an immittance converter
Dp, Dh  diffusion constants for holes and electrons respectively
fo, wo  resonant frequency of a total tuning system
G  conductance
G11, G22  are g parameters of a two port network
G21, G12  are g parameters of a two port network
GI  current amplifier gain
Gv  voltage amplifier gain
i1  small signal input current
io  small signal output current
I1  input current at port 1 etc.
IB  transistor base current
IC  transistor collector current
Io  diode saturation current
k  \(1.38 \times 10^{-23}\) joule/0K, Boltzmann's constant
K  a constant equals to \(\frac{kT}{q}\)
L  inductance
Ln  diffusion length of electrons in P-region
Lp  diffusion length of holes in N-region
M  gain of current attenuator
np0  donor carrier density in the P-region
pno  acceptor carrier density in the N-region
\( q \)  
1.6 \times 10^{-19} \text{ coulomb, electron charge}

\( Q \)  
Q-factor of a tuned circuit

\( r \)  
resistance

\( r_1 \)  
input resistance of amplifier

\( r_L \)  
series loss of antenna

\( r_o \)  
output resistance of amplifier

\( r_p \)  
total resistance at the shunt port of an immittance converter

\( r_{se} \)  
total resistance at the series port of an immittance converter

\( t_d \)  
time delay in a complete feedback loop of an immittance converter

\( v_1 \)  
small signal input voltage

\( v_o \)  
small signal output voltage

\( V_1 \)  
input voltage at port 1 etc

\( Y_1 \)  
admittance measured at port 1 etc

\( Y_L \)  
load admittance

\( Y_o \)  
output admittance

\( Y_{11}, Y_{12} \)  
are admittance parameters for a two port network

\( Y_{21}, Y_{22} \)  
modulus of the respective Y parameters

\( Z_1 \)  
impedance measured at port 1 etc

\( Z_L \)  
load impedance

\( Z_o \)  
output impedance etc.

\( \alpha \)  
current gain of a transistor in the common base connection

\( \beta \)  
current gain of a transistor in the common emitter connection
\( \tau_b \) minority carrier life time in the base of a transistor

\( \tau_\eta \) minority carrier transit time through the base of a transistor

\( \theta \) phase delay angle in a complete feedback loop of an immittance converter
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTRODUCTION</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>CHAPTER 1: THEORY OF IMMITTANCE CONVERTERS</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>1.0</td>
<td>Introduction</td>
<td>3</td>
</tr>
<tr>
<td>1.1</td>
<td>Classical Active Network Theory Approach</td>
<td>3</td>
</tr>
<tr>
<td>1.1.1</td>
<td>Immittance Converters</td>
<td>6</td>
</tr>
<tr>
<td>1.1.2</td>
<td>Voltage Inversion Negative Immittance Converters</td>
<td>6</td>
</tr>
<tr>
<td>1.1.3</td>
<td>Current Inversion Negative Immittance Converters</td>
<td>7</td>
</tr>
<tr>
<td>1.1.4</td>
<td>Effect of Time Delay in High Pass Form</td>
<td>8</td>
</tr>
<tr>
<td>1.1.5</td>
<td>Effect of Time Delay in Low Pass Form</td>
<td>10</td>
</tr>
<tr>
<td>1.2</td>
<td>Control Theory Approach</td>
<td>11</td>
</tr>
<tr>
<td>1.2.1</td>
<td>Two Amplifier Immittance Converters</td>
<td>14</td>
</tr>
<tr>
<td>1.2.2</td>
<td>One Amplifier Immittance Converters</td>
<td>16</td>
</tr>
<tr>
<td>1.2.3</td>
<td>Effect of Time Delay in One Amplifier Immittance Converters</td>
<td>20</td>
</tr>
<tr>
<td>1.3</td>
<td>Stability Considerations</td>
<td>23</td>
</tr>
<tr>
<td>1.3.1</td>
<td>Nyquist Criterion</td>
<td>24</td>
</tr>
<tr>
<td>1.3.2</td>
<td>Bode Criterion</td>
<td>25</td>
</tr>
<tr>
<td>1.3.3</td>
<td>Bode and Nyquist Criteria Applied to Loss Less Two Amplifier Immittance Converters to Tune a Ferrite Rod Antenna</td>
<td>28</td>
</tr>
<tr>
<td>1.4</td>
<td>Circuit Analysis for the Complete Antenna Tuning Systems Using Two Practical Amplifier Immittance Converters</td>
<td>30</td>
</tr>
</tbody>
</table>
(I) Effect of Time Delay as a Loss Factor ........................................ 30
(II) Equivalent Circuits ............................................................... 31
(III) Using Bode and Nyquist Criteria to Examine Their Stabilities ...... 37

1.4.1 Circuit Analysis for the Complete Antenna Tuning System Using One Amplifier Negative Immittance Converter ....................... 38

1.5 Gyrators ........................................................................... 41
1.5.1 Gyrator Formed by Cascading an NIC with an NII .................. 42
1.5.2 Transconductance Gyrator and Transresistance Gyrator .......... 44
1.5.3 Stability Considerations for Gyrators ............................... 47
1.5.4 Effect of Time Delay in Gyrators ................................. 48
1.5.5 Remarks .................................................................. 50

CHAPTER 2: RECEIVING SYSTEMS WITH ACTIVE TUNING ELEMENTS ................................................................. 53

2.1 Introduction ................................................................ 53
2.1.1 Phase-locked-loop ..................................................... 54
2.1.2 A Synchronous AM Detecting System ....................... 56
2.1.3 Tracking the Antenna with the Local Oscillator ............ 58

CHAPTER 3: CIRCUIT REALIZATION ........................................... 62

3.1 Introduction ................................................................ 62
3.1.1 Realization of the Two Amplifier Immittance Converters .......... 63
3.1.2 Unity Gain Voltage Amplifier ................................. 63
3.1.3 Constant Current Sources ........................................ 68
3.1.4 Unity Gain Current Amplifier ............................... 73
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1.5</td>
<td>Current Gain Attenuator</td>
<td>75</td>
</tr>
<tr>
<td>3.1.6</td>
<td>Current Amplifier With a Gain Greater Than Unity</td>
<td>82</td>
</tr>
<tr>
<td>3.2</td>
<td>Realization for the One Amplifier Immittance Converters</td>
<td>84</td>
</tr>
<tr>
<td>3.2.1</td>
<td>A Complete Circuit for the One Amplifier Negative Immittance Converter</td>
<td>89</td>
</tr>
<tr>
<td>3.2.2</td>
<td>A Complete Circuit for the One Current Amplifier Positive Imittance Converter</td>
<td>91</td>
</tr>
<tr>
<td>3.3</td>
<td>Circuit Realization for the Gyrator</td>
<td>95</td>
</tr>
<tr>
<td></td>
<td><strong>CHAPTER 4: RESULTS AND CONCLUSION</strong></td>
<td>100</td>
</tr>
<tr>
<td>4.1</td>
<td>Introduction</td>
<td>100</td>
</tr>
<tr>
<td>4.1.1</td>
<td>Circuit Parameters</td>
<td>100</td>
</tr>
<tr>
<td>4.1.2</td>
<td>Performance Curves for One Amplifier Immittance Converters</td>
<td>101</td>
</tr>
<tr>
<td></td>
<td>(I) One Amplifier Negative Immittance Converter</td>
<td>102</td>
</tr>
<tr>
<td></td>
<td>(II) One Amplifier Positive Immittance Converter</td>
<td>103</td>
</tr>
<tr>
<td>4.2</td>
<td>Concluding Remarks</td>
<td>103</td>
</tr>
</tbody>
</table>
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>A general two port network</td>
<td>4</td>
</tr>
<tr>
<td>1.2</td>
<td>Hybrid g equivalent circuit for a two port network</td>
<td>4</td>
</tr>
<tr>
<td>1.3</td>
<td>An ideal positive immittance converter</td>
<td>6</td>
</tr>
<tr>
<td>1.4</td>
<td>An ideal voltage inversion negative immittance converter</td>
<td>7</td>
</tr>
<tr>
<td>1.5</td>
<td>An ideal current inversion negative immittance converter</td>
<td>7</td>
</tr>
<tr>
<td>1.6</td>
<td>An immittance converter used to tune a ferrite rod antenna (high pass form)</td>
<td>9</td>
</tr>
<tr>
<td>1.7</td>
<td>Equivalent circuit of Fig. 1.6</td>
<td>10</td>
</tr>
<tr>
<td>1.8</td>
<td>An equivalent circuit of Fig. 1.2 when partitioned into a voltage and current amplifier</td>
<td>11</td>
</tr>
<tr>
<td>1.9</td>
<td>A two port network arranged to have an input admittance</td>
<td>12</td>
</tr>
<tr>
<td>1.10</td>
<td>Reciprocal relationship of I₂ and v₁</td>
<td>12</td>
</tr>
<tr>
<td>1.11</td>
<td>A control form representation of the immittance converter of Fig. 1.8</td>
<td>14</td>
</tr>
<tr>
<td>1.12</td>
<td>Another control form representation of the immittance converter of Fig. 1.8</td>
<td>15</td>
</tr>
<tr>
<td>1.13</td>
<td>An immittance converter formed from Fig. 1.11 by removing the current amplifier</td>
<td>16</td>
</tr>
<tr>
<td>1.14</td>
<td>An immittance converter formed from Fig. 1.11 by removing the voltage amplifier</td>
<td>16</td>
</tr>
<tr>
<td>1.15</td>
<td>An immittance converter formed from Fig. 1.12 by removing the voltage amplifier</td>
<td>16</td>
</tr>
<tr>
<td>1.16</td>
<td>An immittance converter formed from Fig. 1.12 by removing the voltage amplifier</td>
<td>16</td>
</tr>
<tr>
<td>Section</td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>---------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>1.17</td>
<td>$Y_I$ represented by $G_Y$ and $G_Y G_Y$ in parallel</td>
<td>17</td>
</tr>
<tr>
<td>1.18</td>
<td>$Y_I$ represented by $G_Y$ and $-G_Y G_Y$ in parallel</td>
<td>18</td>
</tr>
<tr>
<td>1.19</td>
<td>$Z_I$ represented by $G_Z$ and $G_I G_Z$ in series</td>
<td>18</td>
</tr>
<tr>
<td>1.20</td>
<td>$Z_I$ represented by $G_Z$ and $-G_I G_Z$ in series</td>
<td>19</td>
</tr>
<tr>
<td>1.21</td>
<td>A simple passive immittance treated as a single transfer immittance</td>
<td>19</td>
</tr>
<tr>
<td>1.22</td>
<td>The circuit configuration of Fig. 1.13</td>
<td>20</td>
</tr>
<tr>
<td>1.23</td>
<td>The circuit configuration of Fig. 1.14</td>
<td>20</td>
</tr>
<tr>
<td>1.24</td>
<td>Is the circuit configuration of Fig. 1.15</td>
<td>20</td>
</tr>
<tr>
<td>1.25</td>
<td>Is the circuit configuration of Fig. 1.16</td>
<td>20</td>
</tr>
<tr>
<td>1.26</td>
<td>Nyquist locus of a stable system</td>
<td>25</td>
</tr>
<tr>
<td>1.27</td>
<td>Nyquist locus of an unstable system</td>
<td>25</td>
</tr>
<tr>
<td>1.28</td>
<td>Nyquist locus of a conditionally stable system</td>
<td>25</td>
</tr>
<tr>
<td>1.29</td>
<td>Straight line approximation in Bode plot</td>
<td>27</td>
</tr>
<tr>
<td>1.30</td>
<td>An immittance converter arranged to tune an antenna in (a) High pass form (b) low pass form</td>
<td>28</td>
</tr>
<tr>
<td>1.31</td>
<td>Bode magnitude plot for the high pass form</td>
<td>29</td>
</tr>
<tr>
<td>1.32</td>
<td>Bode magnitude plot for the low pass form</td>
<td>29</td>
</tr>
<tr>
<td>1.33</td>
<td>Nyquist locus for the high pass form</td>
<td>30</td>
</tr>
<tr>
<td>1.34</td>
<td>Nyquist locus for the low pass form</td>
<td>30</td>
</tr>
<tr>
<td>1.35</td>
<td>Vector diagram to illustrate the effect of phase delay</td>
<td>31</td>
</tr>
<tr>
<td>1.36</td>
<td>(a) Equivalent circuit for the high pass form</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>(b) Equivalent circuit for the low pass form</td>
<td>32</td>
</tr>
<tr>
<td>1.37</td>
<td>(a) Equivalent circuit for the high pass form which can be simplified into (b)</td>
<td>34</td>
</tr>
<tr>
<td></td>
<td>(b) Equivalent circuit for the low pass form which can be simplified into (d)</td>
<td>34</td>
</tr>
</tbody>
</table>
1.38 (a) & (b) are respectively the Nyquist locus for the complete antenna tuning system using immittance converter arranged in the high pass form and low pass form. Fig. 1.38 (c) & (d) are the Bode curves for the forms respectively.

36

1.39 One amplifier voltage controlled negative immittance converter (with losses) employed to tune an antenna .............................................

38

1.40 Equivalent circuit of Fig. 1.39 ..........................................

39

1.41 Simplified equivalent circuit of Fig. 1.40 ..........

40

1.42 Nyquist locus for the one amplifier voltage controlled negative immittance converter .............

41

1.43 Symbol for a gyrator ........................................

42

1.44 A gyrator formed by cascading an NIC with an NII ........................................

43

1.45 A transconductance gyrator formed by two voltage controlled current sources .....................

44

1.46 A voltage controlled current source decomposed into a voltage and a current amplifier with a passive conductance between them ....................

45

1.47 Four port configuration of a gyrator formed by two voltage and two current amplifiers ..........

46

1.48 Nyquist plots for the transresistance gyrator and transconductance gyrator when terminated with two capacitors ...........................................

48

2.1 A general form of phase-locked systems ...........

53

2.2 A block diagram of phase-locked loop system ....

54

2.3 A basic synchronous detecting system .............

56

2.4 A complete synchronous AM detector ..............

57

3.1 A system diagram for the immittance converter in the high pass form to tune the antenna ........

63

3.2 A unity gain voltage amplifier ......................

64

3.3 Effect of amplifier loss on LC circuit ............

65
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.4</td>
<td>A circuit diagram of a unity gain voltage amplifier</td>
<td>66</td>
</tr>
<tr>
<td>3.5</td>
<td>A unity gain voltage amplifier with high input impedance</td>
<td>67</td>
</tr>
<tr>
<td>3.6</td>
<td>A constant current source</td>
<td>68</td>
</tr>
<tr>
<td>3.7</td>
<td>Characteristic of an ideal constant current source</td>
<td>68</td>
</tr>
<tr>
<td>3.8</td>
<td>Output characteristic of a common base transistor</td>
<td>70</td>
</tr>
<tr>
<td>3.9</td>
<td>Output characteristic of a common emitter transistor</td>
<td>71</td>
</tr>
<tr>
<td>3.10</td>
<td>Constant current sources</td>
<td>72</td>
</tr>
<tr>
<td>3.11</td>
<td>A unity gain current amplifier</td>
<td>73</td>
</tr>
<tr>
<td>3.12</td>
<td>A current gain attenuator</td>
<td>75</td>
</tr>
<tr>
<td>3.13</td>
<td>Dc voltage and current relation of an ideal pn junction</td>
<td>76</td>
</tr>
<tr>
<td>3.14</td>
<td>Two emitter coupled pairs on a chip with bias arrangement</td>
<td>80</td>
</tr>
<tr>
<td>3.15</td>
<td>A current gain attenuator with cascode output</td>
<td>81</td>
</tr>
<tr>
<td>3.16</td>
<td>A current amplifier with a gain greater than unity</td>
<td>82</td>
</tr>
<tr>
<td>3.17</td>
<td>Circuit diagram of a current amplifier with a gain greater than unity</td>
<td>83</td>
</tr>
<tr>
<td>3.18</td>
<td>A voltage controlled negative immittance converter</td>
<td>86</td>
</tr>
<tr>
<td>3.19</td>
<td>A current controlled negative immittance converter</td>
<td>86</td>
</tr>
<tr>
<td>3.20</td>
<td>(a) Vector diagram for a voltage controlled negative immittance converter (b) Equivalent input admittance for (a)</td>
<td>87</td>
</tr>
<tr>
<td>3.21</td>
<td>(a) Vector diagram for a voltage controlled negative immittance converter with a phase delay angle ( \theta_1 ) (b) Equivalent input admittance for (a)</td>
<td>88</td>
</tr>
</tbody>
</table>
3.22 Vector diagram to find the circuit Q of Fig. 3.21 (a) .............................................. 89

3.23 A system diagram for the one amplifier negative immittance converter to tune the antenna. (a) Voltage controlled (b) Current controlled ......................................................... 90

3.24 A complete circuit for the one amplifier negative immittance converter ............................. 91

3.25 A block diagram of a one current amplifier positive immittance converter to tune an antenna ................................................................. 92

3.26 A typical circuit for a one current amplifier positive immittance converter employed to tune an antenna ................................................................. 93

3.27 Equivalent circuits for Fig. 3.26 ...................... 93

3.28 Vector diagram to find the circuit Q of Fig. 3.26 ......................................................... 94

3.29 A block diagram of the transconductance gyrator to tune the antenna of inductance L1 .. 95

3.30 Equivalent circuit for Fig. 3.29 ...................... 96

3.31 Final equivalent circuit for Fig. 3.29 ........... 97

4.1 Input resistance of the current amplifier and output resistance of the voltage amplifier against frequency ......................................................... 97

4.2 Unloaded Q of the ferrite rod antenna ............ 108

4.3 Q-factor of the one current amplifier negative immittance converter used to tune a ferrite rod antenna ................................................................. 109

4.4 Input resistance $r_1$ of the current amplifier against frequency for the required $Q$, $C=470\,\text{pF}$, $L=0.7\,\text{mH}$, $t_d=1\,\text{nS}$, unloaded Q of the antenna (Fig. 4.2) ................................................. 110

4.5 Input resistance $r_1$ of the current amplifier for the required $Q$, $C=470\,\text{pF}$, $L=0.7\,\text{mH}$, $t_d=4\,\text{nS}$. Unloaded Q of antenna (Fig. 4.2) .... 111
4.6 Q-factor of the one current amplifier positive
immittance converter used to tune a ferrite
rod antenna .................................................. 112
# LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>The immittances due to time delay for the above four configurations employed to tune an antenna</td>
<td>22</td>
</tr>
<tr>
<td>1.2</td>
<td>Losses of the high pass form and low pass form referred to the shunt port and series port respectively</td>
<td>35</td>
</tr>
<tr>
<td>1.3</td>
<td>Losses of the one amplifier negative immittance converter employed to tune an antenna</td>
<td>40</td>
</tr>
<tr>
<td>1.4</td>
<td>Summary of the configurations for one amplifier immittance converters, two amplifier immittance converters and immittance gyrators</td>
<td>51</td>
</tr>
<tr>
<td>2.1</td>
<td>Three feasible sets of active tuning elements</td>
<td>59</td>
</tr>
<tr>
<td>3.1</td>
<td>Preferred amplifier characteristics for one amplifier immittance converter</td>
<td>85</td>
</tr>
<tr>
<td>4.1</td>
<td>Measured circuit parameters</td>
<td>99</td>
</tr>
</tbody>
</table>
INTRODUCTION

The development of integrated circuit technology is having a profound effect on the design of integrated receiving systems. The conventional tuning systems of discrete component receivers are being replaced by systems where the overall bandwidth is determined at the detector (ref. 0.1, 0.2, 0.3). However, amplification is found to be desirable between the antenna system and the detector and intermodulation distortion can be introduced if large interfering signals are present. This interference can be reduced by antenna tuning and this thesis is concerned with integrated circuit methods for its implementation.

Several forms of antenna systems are suitable for broadcast receivers, but the tuned ferrite rod is presently the most economical. The antenna must always be tuned to the same frequency as the detection system, so tracking is an important consideration in the choice of a tuning system. Because integrated receiver systems must contain amplifiers, they are also a good choice for the tuning system. Thus the thesis will consider the design of active circuit tuning systems for ferrite rod antennas, within the constraints of integrated circuit batch of fabrication technology.

Active circuit tuning systems contain amplifiers which change the immittance of one element of a tuned circuit
as presented to another. The amplifiers are connected in a feedback configuration and because the batch fabrication implies that they are not compensated, system stability is an important design consideration. For this reason, the thesis will depart from the more conventional active network synthesis approach, in favour of one more related to control theory. All elements will be treated as imperfect transducers in a feedback loop and the immittances at input ports derived on this basis.

Chapter 1 presents the theory of immittance converter in two approaches. The first approach uses the classical network theory. The second uses an approach based on control philosophy. Using the second approach several forms of immittance converter are developed. Chapter 2 presents receiving systems with active tuning elements using phase locked-loop techniques and shows possible ways of tracking the antenna with the local oscillator. Chapter 3 deals with the circuit realizations of the immittance converters. Chapter 4 presents the results and performance characteristics of immittance converter employed to tune antennas. The thesis concludes with the results achieved and an indication of which forms of immittance converter are most promising for antenna tuning systems.
CHAPTER 1

THEORY OF IMMITTANCE CONVERTERS

1.0 Introduction

In this chapter immittance converters are considered, using two separate approaches. First, it is treated as a two port network using classical active network theory (ref. 1.1 - 1.9). This treatment develops a description of the port characteristics of a converter without reference to the practical realization. However, the converter is realized as a feedback circuit and the second treatment approaches immittance converters more from the point of view of control theory. The converter is considered as a system of transducers and an immittance is a voltage to current, or current to voltage transducer, with the input and output at the same port. Then the introduction of amplifiers into the system can change the magnitude and sign of the immittance as measured at the input-output port.

1.1 Classical Active Network Theory Approach

In classical network theory, the immittance converter is considered as a two port linear active network as shown in Fig. 1.1, together with the positive sign and direction for the voltages and currents at the two ports. For an ideal immittance converter, the
immittance measured at one port is equal to the immittance at the other port multiplied by a constant which may be positive or negative.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{general_two_port_network.png}
\caption{A general two port network}
\label{fig:general_two_port_network}
\end{figure}

For a general treatment, the voltages and currents at the two ports may be conveniently related by the $g$ parameters method (1.10).

The hybrid $g$ equivalent circuit is shown in Fig. 1.2.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{hybrid_g_equivalent_circuit.png}
\caption{Hybrid $g$ equivalent circuit for a two port network}
\label{fig:hybrid_g_equivalent_circuit}
\end{figure}

$g_{12}I_2$ is a current controlled source at port 1 and $g_{21}V_1$ is a voltage controlled source at port 2. The two ports are defined by
\[ I_1 = \varepsilon_{11} V_1 + \varepsilon_{12} I_2 \quad \cdots \cdots \cdots \quad (1.1) \]
\[ V_2 = \varepsilon_{21} V_1 + \varepsilon_{22} I_2 \quad \cdots \cdots \cdots \quad (1.2) \]

where the \( \varepsilon \) parameters are defined by
\[ \varepsilon_{11} = \left. \frac{I_1}{V_1} \right|_{I_2=0} \quad ; \quad \varepsilon_{12} = \left. \frac{I_1}{I_2} \right|_{V_1=0} \]
\[ \varepsilon_{21} = \left. \frac{V_2}{V_1} \right|_{I_2=0} \quad \& \quad \varepsilon_{22} = \left. \frac{V_2}{I_2} \right|_{V_1=0} \]

\( \varepsilon_{12} \) and \( \varepsilon_{21} \) are dimensionless current and voltage ratios, and \( \varepsilon_{11} \) has the dimension admittance and \( \varepsilon_{22} \) of impedance. If port 2 is terminated with a passive load \( Z_L \), according to the sign defined in Fig. 1.2,
\[ Z_L = -\frac{V_2}{I_2} \quad \cdots \cdots \cdots \cdots \quad (1.3) \]

Solving (1.1), (1.2) and (1.3), the admittance measured at port 1
\[ Y_1 = \left. \frac{I_1}{V_1} \right|_{V_2} = \varepsilon_{11} - \frac{\varepsilon_{12} \varepsilon_{21}}{Z_2 + \varepsilon_{22}} \quad \cdots \cdots \cdots \cdots \quad (1.4) \]

If \( \varepsilon_{11} = 0, \ \varepsilon_{22} = 0 \)
\[ Y_1 = -\frac{\varepsilon_{12} \varepsilon_{21}}{Z_2} \quad \cdots \cdots \cdots \cdots \quad (1.5) \]
or
\[ Z_1 = -\frac{Z_L}{\varepsilon_{12} \varepsilon_{21}} \quad \cdots \cdots \cdots \cdots \quad (1.7) \]

(1.5) states the necessary and sufficient conditions for the two ports to be an ideal impedance converter.

If port 1 is terminated with an impedance \( Z_L \), it
can be shown that the input impedance at port 2

\[ Z_2 = \frac{g_{22} \cdot g_{21}}{g_{11} + 1/Z_L} \]  \hspace{1cm} (1.8)

and \[ Z_2 = -g_{12} \cdot g_{21} Z_L \]  \hspace{1cm} (1.9)

if the conditions for 1.5 are satisfied.

1.1.1 Immittance Converters

If \( g_{11} = 0 \), \( g_{22} = 0 \), \( g_{21} \) is positive and \( g_{12} \) is negative, the above becomes a positive immittance converter. These conditions are shown in Fig. 1.3. There is no inversion in voltage across or current through the load with respect to the voltage or current at port 1.

1.1.2 Voltage Inversion Negative Immittance Converters

If \( g_{11} = 0 \), \( g_{22} = 0 \), \( g_{12} \) and \( g_{21} \) are negative, the above becomes a voltage inversion negative immittance converter. These conditions are shown in Fig. 1.4. There is no current inversion at either port but the voltage at port 2 is inverted with respect to that at port 1.
Fig. 1.4 An ideal voltage inversion negative immittance converter

1.1.3 Current Inversion Negative Immittance Converters

If $\xi_{11} = 0$, $\xi_{22} = 0$, $\xi_{12}$ and $\xi_{21}$ are positive, the above becomes a current inversion negative immittance converter. These conditions are shown in Fig. 1.5. There is no voltage inversion at either port, but the direction for the current $I_2$ through the load is opposite to that of $I_1$.

Fig. 1.5 An ideal current inversion negative immittance converter

In the above treatment, it is assumed that $\xi_{11} = \xi_{22} = 0$. In practical realizations, $\xi_{11}$ and $\xi_{22}$ are finite and their effects on $Z_1$ and $Z_2$ are seen from 1.4.
and 1.8. However, their values can be made zero at a single frequency by network compensation techniques.

1.1.4 Effect of Time Delay in High Pass Form

The amplifiers are imperfect i.e. \( g_{11} \) and \( g_{22} \) are finite, and all amplifiers introduce a time delay. Now consider the effect of \( g_{11} \), \( g_{22} \) and the time delay on the overall system when the positive immittance converter is used to tune the ferrite rod antenna. High pass form (Fig. 1.6) is first considered in which port 2 is terminated with a capacitance \( C \), and port 1 with an inductance \( L \). Thus \( Z_L = \frac{1}{j\omega C} \).

Because of delay \( g_{12} \cdot g_{21} \) can be written as

\[
g_{12} \cdot g_{21} = (g_{12} - j\tau_{12})(g_{21} + j\tau_{21})
\]

\[
= G_{12}e^{-j\theta_{12}} G_{21}e^{-j\theta_{21}}
\]

\[
= Be^{-j\theta} \quad \text{where} \quad B = G_{12} \cdot G_{21}
\]

\[
\theta = \theta_{12} + \theta_{21} = \omega t_{d1} + \omega t_{d2}
\]

\( t_{d1} \), \( t_{d2} \) are time delays in the amplifiers.

\[
g_{12} \cdot g_{21} = B(1-j\theta) \quad \text{if} \ \theta \ \text{is small} \quad \quad \quad \quad \quad (1.10)
\]

Substituting \( Z_L \) and 1.10 in 1.4

\[
Y_1 = g_{11} + \frac{B(1-j\theta)}{1/j\omega C + g_{22}}
\]

on normalizing the denominator and expanding

\[
Y_1 = g_{11} + \frac{B(\omega^2 C \theta + \omega^2 C^2 g_{22} + j\omega C - j\omega^2 C^2 \theta g_{22})}{1 + (g_{22} \omega C)^2}
\]
\[ g_{11} + \frac{B \omega C \theta}{1 + (g_{22} \omega C)^2} + \frac{B \omega^2 C^2 g_{22}}{1 + (g_{22} \omega C)^2} + \frac{j \omega C B}{1 + (g_{22} \omega C)^2} - \frac{j \omega^2 C^2 \theta g_{22}}{1 + (g_{22} \omega C)^2} \ldots \ldots (1.11) \]

\[ \frac{j \omega^2 C^2 \theta g_{22}}{1 + (g_{22} \omega C)^2} \] can be neglected. As \((g_{22} \omega C)^2 \ll 1\), (1.11) can be approximated as

\[ Y_1 \approx g_{11} + B \omega^2 C^2 g_{22} + B \omega C \theta + j B \omega C \ldots \ldots \ldots (1.12) \]

The first, second and third term of (1.12) represents the losses due to \(g_{11}\), \(g_{22}\) and the delay respectively. None introduces a negative admittance, so the system is inherently stable. These losses merely reduces the system Q.

Let the total loss

\[ g_t = g_L + g_{11} + B \omega C \theta + B \omega^2 C^2 g_{22} \ldots \ldots (1.13) \]

where \(g_L = \frac{r_L}{2 L^2}\) the loss of the antenna. Fig. 1.7 is the equivalent circuit for Fig. 1.6.

![Diagram](image)

**Fig. 1.6** An immittance converter used to tune a ferrite rod antenna (high pass form)
Fig. 1.7  Equivalent circuit of Fig. 1.6

The overall Q of the system

\[ Q = \frac{1}{\omega I g_1} = \frac{\omega BC}{g_1} \quad \ldots \quad (1.14) \]

and the resonant frequency

\[ f_0 = \frac{1}{2 \pi \sqrt{LCB}} \quad \ldots \quad (1.15) \]

1.1.5 Effect of Time Delay in Low Pass Form

We will now examine the low pass form in which port 2 is terminated with the antenna \( L \) whose series loss is \( R_L \). By the similar procedure as before

\[ Y_1 = g_{11} + \frac{B(g_{22}+R_L)}{(R_L+g_{22})^2 + \omega^2 L^2} - \frac{B \omega L \theta}{(R_L+g_{22})^2 + \omega^2 L^2} \]

\[ - \frac{j \omega L B}{(R_L+g_{22})^2 + \omega^2 L^2} \quad \ldots \quad (1.16) \]

as \( \omega^2 L^2 >> (R_L+g_{22})^2 \), (1.16) can be approximated as

\[ Y_1 = g_{11} + \frac{B(g_{22}+R_L)}{\omega^2 L^2} - \frac{B \theta}{\omega L} - \frac{jB}{\omega L} \quad \ldots \quad (1.17) \]
\textit{1.2 Control Theory Approach}

The voltage controlled source $g_{21}V_1$ and the current controlled source $g_{12}I_2$ in the Hybrid equivalent circuit of Fig. 1.2 can be partitioned as shown in Fig. 1.8 using a voltage amplifier and a current amplifier. This method of partitioning the controlled sources into voltage and current amplifiers leads to a convenient means of circuit realization.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{circuit_diagram}
\caption{An equivalent circuit of Fig. 1.2 when partitioned into a voltage and current amplifier}
\end{figure}

A feedback loop is formed if the two ports are terminated with immittances. Voltage applied at port 1 is amplified and becomes $V_2$ at port 2. The immittance terminated at port 2 will transform $V_2$ into a current $I_2$, which will be amplified and becomes $I_1$ at port 1, thus completing the feedback loop. Because of the existence of this feedback loop, control theory can be applied to advantage to determine its
terminal characteristics and system stability (ref. 1.11, 1.12, 1.13).

Every element within the loop is considered as a transducer. The immittances are considered as voltage to current or current to voltage transducers with the input and output at the same port. The following example will help to illustrate this point. A voltage controlled current source, such as a field effect transistor has a transfer admittance, which can be expressed as $\frac{i_2}{v_1}$. When the output port is connected in parallel with the input port, so that feedback is negative, as shown in Fig. 1.9, the input has the characteristic of an admittance $\frac{i_2}{v_1}$ as shown in Fig. 1.10. The input

![Diagram of a voltage controlled source](image)

**Fig. 1.9** A two port network arranged to have an input admittance

immittance is reciprocal, that is, for an input current there is a corresponding voltage and vice versa. Thus, it is

![Graph of reciprocal relationship](image)

**Fig. 1.10** Reciprocal relationship of $i_2$ and $v_1$
impossible to deduce, from input immittance measurements, whether the two port of Fig. 1.9 has a transfer admittance or a transfer impedance, or whether the device is voltage or current controlled. However, if the feedback were positive and the input immittance becomes negative, the voltage and current relationship is no longer reciprocal and it is possible to deduce whether the device has a transfer admittance or impedance from the input immittance measurements. If it is a voltage controlled negative admittance $Y_2$, the system will be stable if it is driven by a voltage source but unstable if driven by a current source. The condition of stability is

$$|Y_1 + Y_0| > 0 \quad \text{.......................... (1.18)}$$

where $Y_0$ is the output admittance of the driving source.

If the input is a current controlled negative impedance $Z_1$, the condition of stability is

$$|Z_1 + Z_0| > 0 \quad \text{.......................... (1.19)}$$

where $Z_0$ is the output impedance of the driving source.

The foregoing discussion is concerned with the stability criteria for an immittance converter at a single operating frequency. However, a practical converter must be stable at all frequencies and must meet the general stability criteria of e.g. Bode (ref. 1.14) and Nyquist (ref. 1.15). Thus, in order to perform a complete design, an approach more oriented to control theory and suitable for determining both the overall stability criteria and the
terminal characteristics will prove convenient.

1.2.1 Two Amplifier Immittance Converters

The immittance converter in Fig. 1.8 can be drawn in control form as shown in Fig. 1.11, which is a single loop feedback system. All the circuit elements in the system are treated as transducers. The system contains a voltage amplifier, a current amplifier and a transfer conductance $G_Y$. The voltage amplifier is the voltage controlled voltage source of figure 1.8 which has a gain $G_Y = \frac{V_2}{V_1} \left| \begin{array}{c} I_2 = 0 \end{array} \right.$, the current amplifier is the current controlled current source which has a gain $G_I = \frac{I_1}{I_2} \left| \begin{array}{c} V_1 = 0 \end{array} \right.$ and the transfer admittance $G_Y$ is the terminating admittance $Y$. Note that a one-port immittance $G_Y$ is now treated as a two-port transducer. This is possible because it is placed in a zero impedance loop and its input and output are different quantities.

![Diagram](image)

Fig. 1.11 A control form representation of the immittance converter of Fig. 1.8

Because the transfer function of the voltage and current amplifiers are pure numbers, being in series with $G_Y$, they do not change the dimension of $G_Y$, but modify its
magnitude by the product of their transfer functions $G_1G_Y$. Thus the dotted box in Fig. 1.11 is a transfer conductance $G_1G_Y G_Y$.

With the output feedback to the input, they are at the same port and the system becomes an admittance.

$$Y_1 = -G_Y G_1 G_Y \quad \cdots \cdots \cdots \cdots \quad (1.20)$$

Alternatively the $V$ and $I$ relationship at the input may be stated in terms of a transfer resistance $G_Z$ as shown in Fig. 1.12.

![Diagram](image)

Fig. 1.12 Another control form representation of the immittance converter of Fig. 1.8

$$Z_1 = G_Y G_1 G_Z \quad \cdots \cdots \cdots \cdots \quad (1.21)$$

The following two points are noted for the above two configurations:

1. In both cases the transfer conductance or resistance is placed between the two controlled sources. So that it is isolated from the input of the system.

2. The sign of $Y_1$ or $Z_1$ depends on the sense of the feedback. $Y_1$ or $Z_1$ is positive if the feedback is negative and negative if the feedback is positive.
1.2.2 One Amplifier Imittance Converters

As the transfer function of the voltage and current amplifiers are pure numbers, removing a voltage or a current amplifier does not affect the dimensions of the transfer function of the series chain in Fig. 1.11 and Fig. 1.12, but reduces it by a factor equal to the gain of the amplifier removed. By doing so, four different forms of imittance converter are formed. Fig. 1.13 and Fig. 1.14 are formed respectively by removing a current and a voltage amplifier from Fig. 1.11, and Fig. 1.15 and Fig. 1.16 are similarly formed from Fig. 1.12.

Fig. 1.13 An imittance converter formed from Fig. 1.11 by removing the current amplifier

Fig. 1.14 An imittance converter formed from Fig. 1.11 by removing the voltage amplifier

Fig. 1.15 An imittance converter formed from Fig. 1.12 by removing the voltage amplifier

Fig. 1.16 An imittance converter formed from Fig. 1.12 by removing the voltage amplifier

The input imittance of Fig. 1.13, 1.14, 1.15, 1.16 are
respectively
\[ Y_1 = G_y(l+G_y), \quad Y_1 = G_y(l+G_l), \quad Z_1 = -G_z(l+G_l), \quad Z_1 = G_z(l+G_y), \]
i.e., as an amplifier is removed, the original transfer immittance \( G_y \) or \( G_z \) is seen directly by the input. Thus the input immittance can be partitioned into two components: one is \( G_y \) or \( G_z \), the other is a converted immittance introduced by the amplifier. For the configuration shown in Fig. 1.13, with negative feedback (i.e., the amplifier gain \( G_y \) is negative), thus
\[
Y_1 = \frac{i_0}{V_1} = G_y - (G_y G_y) \\
= G_y + G_y G_y \quad \cdots \cdots \quad (1.22)
\]
Eq. 1.22 can be represented by Fig. 1.17 where \( G_y \) and \( G_y G_y \) are in parallel,

![Diagram](image)

Fig. 1.17 \( Y_1 \) represented by \( G_y \) and \( G_y G_y \) in parallel with positive feedback (\( G_y \) is positive), thus
\[
Y_1 = G_y - (G_y G_y) = G_y - G_y G_y \quad \cdots \cdots \quad (1.23)
\]
Eq. 1.23 can be represented by Fig. 1.18 where \( G_y \) and \(-G_y G_y \) are in parallel.
Fig. 1.18  $Y_1$ represented by $G_Y$ and $-G_YG_Y$ in parallel

For the configuration shown in Fig. 1.14 with negative feedback (the current amplifier is inverted or $G_I$ is positive), thus

$$Y_1 = G_Y + (G_I G_Y) = G_Y + G_I G_Y \quad \cdots \cdots \cdots \cdots \quad (1.24)$$

With positive feedback (the current amplifier is non-inverted or $G_I$ is negative), thus

$$Y_1 = G_Y + (G_I G_Y) = G_Y - G_I G_Y \quad \cdots \cdots \cdots \cdots \quad (1.25)$$

Eq. 1.24 & 1.25 can be similarly represented as shown in Fig. 1.17 and Fig. 1.18 respectively.

For Fig. 1.15, with negative feedback ($G_I$ is positive), thus

$$Z_1 = G_Z + (G_I G_Z) = G_Z + G_I G_Z \quad \cdots \cdots \cdots \cdots \quad (1.26)$$

Eq. 1.26 can be represented by Fig. 1.19 where $G_Z$ and $G_I G_Z$ are in series.

Fig. 1.19  $Z_1$ represented by $G_Z$ and $G_I G_Z$ in series
With positive feedback ($G_I$ is negative), thus

$$Z_1 = G_Z + (G_I G_Z) = G_Z - G_I G_Z \quad \cdots \cdots \cdots \quad (1.27)$$

Eq. 1.27 can be represented by Fig. 1.20 where $G_Z$ and $-G_I G_Z$ are in series.

---

For Fig. 1.16 with negative feedback ($G_v$ is positive), $G_v G_Z$ is positive, thus

$$Z_1 = G_Z + (G_v G_Z) = G_Z + G_v G_Z \quad \cdots \cdots \cdots \quad (1.28)$$

With positive feedback ($G_v$ is negative), thus

$$Z_1 = G_Z + (G_v G_Z) = G_Z - G_v G_Z \quad \cdots \cdots \cdots \quad (1.29)$$

Eq. 1.28 and 1.29 can be similarly represented by Fig. 1.19 and 1.20 respectively.

The trivial case of a simple passive immittance is treated as a single transfer immittance $G_Y$ or $G_Z$ with the output and input connected to the same port, as shown in Fig. 1.21 (a) & (b).

---

Fig. 1.21  A simple passive immittance treated as a single transfer immittance
The sense of the feedback is always taken to be negative.

The circuit configuration for the one amplifier immittance converter in Fig. 1.13 to 1.16 are shown respectively in Fig. 1.22 to 1.25.

![Fig. 1.22](image1)

![Fig. 1.23](image2)

![Fig. 1.24](image3)

![Fig. 1.25](image4)

Figs. 1.22, 1.23, 1.24 and 1.25 are the circuit configurations of Figs. 1.13, 1.14, 1.15 and 1.16 respectively.

1.2.3 Effect of Time Delay in One Amplifier Immittance Converters

Since all amplifiers introduce a time delay $t_d$, the current gain $G_I$ is complex and can be expressed as

$$G_I = G_I^* - jX_I$$

$$= B_I e^{-j \theta_I}$$

$$= B_I (1 - j \theta_I) \quad \text{......... (1.30)}$$

If $\theta_I$ is small,
where \( B_I = \sqrt{G_I^2 + X_I^2} \)

and \( \theta_I = \tan \frac{-1X_I}{G_I} \)

\[ \omega t_d \]

Similarly, the voltage gain

\[ G_V = B_V e^{-j\theta_V} \]

\[ = B_V(1-j\theta_V) \quad \cdots \quad (1.31) \]

Substituting eq. 1.30 & 1.31 in eq. 1.23, 1.25, 1.27 & 1.29 (assuming positive feedback in all cases), we obtain respectively

\[ Y_1 = G_Y - G_Y[B_V(1-j\theta_V)] = G_Y - G_Y B_V + j G_Y B_V \theta_V \quad (1.32) \]

\[ Y_1 = G_Y - G_Y[B_I(1-j\theta_I)] = G_Y - G_Y B_I + j G_Y B_I \theta_I \quad (1.33) \]

\[ Z_1 = G_Z - G_Z[B_I(1-j\theta_I)] = G_Z - G_Z B_I + j G_Z B_I \theta_I \quad (1.34) \]

\[ Z_1 = G_Z - G_Z[B_V(1-j\theta_V)] = G_Z - G_Z B_V + j G_Z B_V \theta_V \quad (1.35) \]

The immittances due to the time delay for the above four configurations employed to tune a ferrite rod antenna are tabulated in Table 1.1. If the feedback is negative, the sign is changed. An alternative approach to account for the time delay is given in section 1.4.2.

A general comment on system stability can now be made. As in the two amplifier immittance converters, in the cases where the time delay introduces positive immittances, the system is inherently stable but it lowers the system Q
<table>
<thead>
<tr>
<th>Equivalent Resistance Due to Time Delay</th>
<th>Gy</th>
<th>Gz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\frac{1}{j\omega C}$</td>
<td>$\frac{1}{j\omega L}$</td>
<td>$\frac{1}{j\omega L}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Equivalent Conductance Due to Time Delay</th>
<th>Gy</th>
<th>Gz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{1}{j\omega L}$</td>
<td>$\frac{1}{j\omega L}$</td>
<td>$\frac{1}{j\omega L}$</td>
</tr>
</tbody>
</table>

Table 1.1 The immittances due to time delay for the above configurations employed to tune an antenna.
whereas in the cases where the time delay introduces negative immittance, the system Q is increased as it approaches instability.

1.3.0 Stability Considerations

The basis of a closed loop system stability is determined by the roots of the characteristic equations of the closed loop response. The Nyquist Criterion and Bode Criteria (ref. 1.14 and 1.15) are convenient criteria which can yield system stability information from the characteristic equations.

For a system whose open loop gain is $G(S)$ and feedback factor $H(S)$ the closed loop response can be stated as

$$\frac{\text{output}}{\text{input}} = \frac{G(S)}{1 + G(S)H(S)} \quad \text{........................} \quad (1.36)$$

and the characteristic equation is

$$1 + G(S) H(S) = 0 \quad \text{..................} \quad (1.37)$$

The roots of the characteristic equation are the poles of 1.36, thus the relation of the roots and the system response (stability) can be stated as:

1. If all the roots are in the left half of the $S$-plane, the transient will die out and the system is stable.

2. If more than one pair of roots are on the imaginary axis the response is undamped sinusoidal oscillations and the system is considered unstable.

3. If one or more roots are in the right half of the $S$-plane, the response will increase with time and the system
is unstable.

Physically all linear systems have a limit of linearity. Once they become unstable, they saturate and the loop gain $G(S)H(S)$ is reduced to unity.

1.3.1 Nyquist Criterion

Nyquist criterion is a convenient technique to discover if the characteristic equations has any roots in the right half of the S-plane. Following the Nyquist path in the clockwise direction, the magnitude and angle of $G(S)H(S)$ are plotted in the $G(S)H(S)$ plane, a Nyquist diagram is obtained. The Nyquist locus will make $N = Z - P$ encirclements of the critical point $(-1,0)$, where

$$Z = \text{number of zeros of the characteristic equation in the right half plane.}$$

$$P = \text{number of poles of } \frac{H(S)}{G(S)} \text{ in the right half of the S-plane.}$$

The encirclement of $(-1,0)$ is clockwise if $(Z-P) > 0$ and anticlockwise if $(Z-P) < 0$.

For most systems $G(S)$ and $H(S)$ are stable functions, i.e. $P = 0$. For a stable system $N$ must be zero. Thus, assuming $P = 0$, Fig. 1.26 shows the Nyquist locus for a stable system as it does not encircle the critical point in an clockwise direction; Fig. 1.27 shows the Nyquist locus for an unstable system which makes an clockwise encirclement of the critical point and Fig. 1.28 shows the Nyquist locus for a conditional stable system.
A conditionally stable system is undesirable in practice, because once oscillation starts, the system saturates and reduces the loop gain $G(S) H(S)$ to $1 \angle -180^\circ$ and oscillations persist.

1.3.2 Bode Criterion

If the transfer function is a minimum phase function, which is defined as one which does not have any poles or zeros in the right half of the S-plane, or the relationship between the magnitude and phase is unique, Bode criterion can be applied to determine the system closed loop stability.
In general, \( G(S) H(S) \) can be stated as
\[
G(S) H(S) = \frac{K'(S+z_1)(S+z_2) \cdots (S+z_m)}{S^{\ell'}(S+p_1)(S+p_2) \cdots (S+p_n)} \quad \cdots \quad (1.38)
\]
where \( K' \) is a constant and \( \ell' \) is a positive integer. The \( z \)'s and \( p \)'s may be zero, real or complex conjugate. Under sinusoidal conditions, \( S = j\omega \), Eq. 1.38 can be written as
\[
G(S) H(S) = \frac{K(1+j\omega/z_1)(1+j\omega/z_2) \cdots (1+j\omega/z_m)}{(j\omega)^{\ell'}(1+j\omega/p_1)(1+j\omega/p_2) \cdots (1+j\omega/p_n)} \quad \cdots \quad (1.39)
\]
where \( K = K' \prod_{i=1}^{m} \frac{z_i}{z_i} / \prod_{i=1}^{n} p_i \)

The magnitude is given by
\[
20 \log_{10} \left[ G(j\omega)H(j\omega) \right] = 20 \log_{10} K + 20 \log_{10} \left[ 1 + \frac{j\omega}{z_1} \right] + \cdots \\
-20 \log_{10} \left[ 1 + \frac{j\omega}{z_m} \right] - 20 \log_{10} (j\omega)^{\ell'} - 20 \log_{10} \left[ 1 + \frac{j\omega}{p_1} \right] \\
-20 \log_{10} \left[ 1 + \frac{j\omega}{p_n} \right] \quad \cdots \quad (1.40)
\]

and the phase is given by
\[
\arg \left[ G(j\omega) H(j\omega) \right] = \arg K + \arg \left[ 1 + \frac{j\omega}{z_1} \right] + \cdots \\
+\arg \left[ 1 + \frac{j\omega}{z_m} \right] - \arg (j\omega)^{\ell'} - \arg \left[ 1 + \frac{j\omega}{p_1} \right] \\
- \arg \left[ 1 + \frac{j\omega}{p_n} \right] \quad \cdots \quad (1.41)
\]

A pair of complex zeros in 1.38 consists of two terms in 1.40 & 1.41 which can be replaced respectively by
\[
20 \log_{10} \left[ 1 - \left( \frac{w}{w_z} \right)^2 + j2 \frac{\omega}{w_z} \right]
\]
and \[ \arg \left[ 1 - \left( \frac{\omega}{\omega_z} \right)^2 + 2j \frac{\omega}{\omega_z} \right] \]

A pair of complex poles in 1.38 consists of two terms in 1.40 & 1.41 which can be replaced respectively by

\[ 20 \log_{10} \left[ \frac{1}{1 - \left( \frac{\omega}{\omega_p} \right)^2 + 2j \frac{\omega}{\omega_p}} \right] \]

and \[ \arg \left[ \frac{1}{1 - \left( \frac{\omega}{\omega_p} \right)^2 + 2j \frac{\omega}{\omega_p}} \right] \]

Plotting 1.40 in dB. and 1.41 in degrees vs log\( \omega \) separately form the Bode plot, e.g. as shown in Fig. 1.29. For most practical purposes, straight line approximations are adequate.

![Bode Plot Diagram](image)

Fig. 1.29  Straight line approximation in Bode plot

The closed loop system is unstable if the magnitude is greater than zero dB. when the phase is -180°. This corresponds to the Nyquist locus encircles the critical point.
(-1, 0). In order to be stable, the magnitude must be less than zero db. when the phase is -180°.

1.3.3 Bode & Nyquist Criteria Applied to Two Amplifier Immittance Converters.

An immittance converter can be used to tune a ferrite rod antenna in two possible forms, the high pass and the low pass form as shown respectively in Fig. 1.30 (a) and (b). They are similar with the interchange of the L and C and the two forms will be considered in detail below.

(a) First consider immittance converter systems employing practical inductances and capacitances and ideal voltage and current amplifiers, i.e., the voltage amplifier has infinite input impedance and zero output impedance and has no delay and the current amplifier has zero input impedance and infinite output impedance and there is no delay.

Then the L and C separately introduces a phase shift of almost 90° at the tuned frequency. In the high pass case the
phase shift is leading and in the low pass case the phase shift is lagging. The Bode magnitude plot for the above two cases are shown in Fig. 1.31 and Fig. 1.32 respectively.

The slope is 12 \text{ db/oct.} in both cases. It is positive for the high pass case and negative for the low pass case. AB is the operating region. As the slope is rising at 12 \text{ db/oct.} in the high pass case, in order not to violate the Bode

![Bode Magnitude Plots](image)

**Fig. 1.31** Bode Magnitude plot for the high pass form  
**Fig. 1.32** Bode Magnitude plot for the low pass form

Criterion of stability the magnitude must decrease to zero \text{ db.} when the phase is $-180^\circ$. This problem does not exist in the low pass case as the L and C cause the magnitude to fall at a rate of $-12 \text{ db/oct.}$ right to zero \text{ db.} satisfying the Bode Criteria of stability.

(b) **Systems employing practical amplifiers**

Practical amplifiers have finite input and output impedances, which introduce a loss into the system as will be discussed later, and a time delay $t_d$ which adds a lagging phase angle $\theta = \omega t_d$ radians to the loop. The time delay
modifies the Nyquist locus for the two forms as shown dotted in Fig. 1.33 & Fig. 1.34 respectively.

Fig. 1.33 Nyquist locus for the high pass form

Fig. 1.34 Nyquist locus for the low pass form

It is seen that the time delay renders the low pass form potentially unstable as the Nyquist locus will exceed -180° phase shift, but increases the system stability in the high pass case. Equivalently it can be said that the time delay introduces a loss to the high pass form and a gain (negative immittance) to the low pass form (refer to section 1.1.4 and 1.1.5).

1.4 Circuit Analysis for the Complete Antenna Tuning System Using Two Practical Amplifier Immittance Converters

(I) Effect of Time Delay as a Loss Factor

At any frequency \( \omega \), the time delay \( t_d \) through the circuit can be represented by an equivalent resistance \( r_T = \omega^2 L t_d \) or \( r_T = \frac{\theta}{\omega_c} \) in series with the inductance \( L \) of the antenna or the capacitance \( C \). As shown in Fig. 1.35,
\( \theta \) is the phase angle due to the delay \( t_d \). As

\[
Q = \frac{\omega L}{r_T} = \frac{1}{\omega C r_T} = \frac{1}{\tan \theta} \approx \frac{1}{\theta}
\]

The approximation is valid if

\[
\theta < \frac{\pi}{36} \text{ rad or } 5^0, \quad \therefore r_T = \omega L \theta = \omega^2 L t_d
\]

as \( \theta = \omega t_d \)

or

\[
r_T = \frac{\theta}{\omega C} = \frac{\omega t_d}{\omega C} = \frac{t_d}{C} \quad \cdots \cdots \cdots (1.42)
\]

which is positive in the high pass form and negative in the low pass form.

---

Fig. 1.35 Vector diagram to illustrate the effect of phase delay

(II) Equivalent Circuits

As the immittance converter is used to synthesize a variable capacitor to tune the antenna with an inductance \( L \), it is convenient to draw the equivalent circuit for the system with the immittance and converter losses all referred to the port in which the antenna is terminated. There are two convenient methods to handle these losses and by these methods they can be partitioned as explained below. Because
at the shunt port, the input of the voltage amplifier is in parallel with the output of the current amplifier, and at the series port the input of the current amplifier is in series with output of the voltage amplifier, it is convenient to express the input immittance at the above two ports as \( y_1 = \frac{i_0}{V_1} \) and \( z_1 = \frac{V_0}{i_1} \) respectively. Thus it is also convenient to represent the losses in the high pass form by a conductance \( g \) shunting the tuned system as shown in Fig. 1.36 (a) while in the low pass form by a resistance \( r \) in series with the tuned system as shown in Fig. 1.36(b). \( g \) and \( r \) can be expressed respectively by Eq. 1.43 and 1.44 as the sum of the losses.

\[
\begin{align*}
\text{Fig. 1.36} & \quad \text{(a) Equivalent circuit for the high pass form} \\
& \quad \text{(b) Equivalent circuit for the low pass form}
\end{align*}
\]

\[
\begin{align*}
g &= g_1 + g_2 + \ldots + g_n \quad \text{(1.43)} \\
r &= r_1 + r_2 + \ldots + r_n \quad \text{(1.44)}
\end{align*}
\]

where \( g_1, \ldots, g_n; r_1, \ldots, r_n \) are the various losses in the amplifiers referred to the shunt port and the series port respectively.

The equivalent circuit for the high pass form is shown in Fig. 1.37 (a) in which the admittances and losses are all
referred to the shunt port. The admittance transformation ratio from the series to shunt port is $B$ (eq. 1.20, $B = G_y G_I$). The equivalent circuit for the low pass form is shown in Fig. 1.37 (c) in which the impedances and losses are all referred to the series port. The impedance transformation ratios from the shunt port to the series port is $B$ (eq. 1.21) Fig. 1.37 (a) and (c) can be simplified to Fig. 1.37 (b) and (d) respectively, where $g$ and $r$ are given by Eq. 1.43 and 1.44

$n = 5$ as only five losses due to the imperfections of the amplifiers are considered important.

$g_1, r_1$ - Equivalent shunt conductive and series resistive loss of the antenna respectively

$g_2, r_2$ - Equivalent shunt conductive and series resistive loss due to time delay

$g_3, r_3$ - Equivalent shunt conductive and series resistive loss at the shunt port

$g_4, r_4$ - Equivalent shunt conductive and series resistive loss due to output resistance (in series) with the series port

$g_5, r_5$ - Equivalent shunt conductive and series resistive loss due to the loss shunting the series port

Their values are tabulated in Table 1.2. The corresponding $Q$ and the tuned frequency for the two forms are respectively,

$$Q_{HP} = \frac{1}{\omega L_g}, \quad f_{HP} = \frac{1}{2\pi \sqrt{LCB}} \quad \text{............... (1.45)}$$

and

$$Q_{LP} = \frac{\omega L}{r}, \quad f_{LP} = \frac{1}{2\pi \sqrt{LC/\beta}} \quad \text{............... (1.46)}$$
Fig. 1.37  (a) Equivalent circuit for the high pass form which can be simplified into (b)

(c) Equivalent circuit for the low pass form which can be simplified into (d)
<table>
<thead>
<tr>
<th>Admittance Transformed From Series Port to Shunt Port</th>
<th>Impedance Transformed From Shunt Port to Series Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ g_1 = g_L = \frac{r_L}{(\omega L)^2} ]</td>
<td>[ r_1 = r_L ]</td>
</tr>
<tr>
<td>[ g_2 = g_T = \frac{\omega^2 L t_d}{(\omega L)^2} = \frac{t_d}{L} = r_T ]</td>
<td>[ r_2 = -\omega^2 L t_d = r_T ]</td>
</tr>
<tr>
<td>[ g_3 = g_p = \frac{1}{r_p} ]</td>
<td>[ r_3 = \frac{B}{\omega^2 c^2 r_p} ]</td>
</tr>
<tr>
<td>[ g_4 = g_{se} = \omega^2 c^2 B r_{se} ]</td>
<td>[ r_4 = r_{se} ]</td>
</tr>
<tr>
<td>[ g_5 = g_{sh} = \frac{B}{r_{sh}} ]</td>
<td>[ r_5 = \frac{B L}{C r_{sh}} ]</td>
</tr>
</tbody>
</table>

\[ r_L \] is the series loss of \[ \omega L \] |
\[ t_d \] is the loop delay time |
\[ r_p \] is the total resistance at the shunt port |
\[ r_{se} \] is the total output series resistance at the series port |
\[ r_{sh} \] is the total resistance shunting the series port |

Table 1.2 Losses of the High Pass Form and Low Pass Form Referred to the Shunt Port and Series Port Respectively
Fig. 1.38 (a) and (b) are respectively the Nyquist locus for the complete antenna tuning system using immittance converter arranged in the high pass form and low pass form. Fig. 1.38 (c) and (d) are the Bode curves for the two forms respectively.
(III) Using Bode and Nyquist Criteria to Examine Their Stabilities

Due to $L$ and $C$, the phase shift of the loop at low frequency is almost $180^\circ$ leading in the high pass form and $180^\circ$ lagging in the low pass form, owing to the series resistive losses in $L$ and the losses at the shunt and series port of the converter, while the magnitude increases at $12 \text{ db/oct}$ in the high pass form and decreases at $-12 \text{ db/oct}$ in the low pass form. As the frequency increases and, if there is no time delay, the Nyquist loci for the two forms are as shown dotted in Fig. 1.38 (a) & (b). Because of the time delay introducing a phase lag angle $\theta = \omega t_d$, the actual Nyquist locus for the high pass form deviates from the negative real axis at $\omega = \omega_1$, while that for the low pass form will cross the negative real axis, causing the system to be conditionally stable. As the frequency increases, the magnitude and phase angle of the Nyquist loci for the two forms continue to change as mentioned above until $\omega = \omega_2$ the stray capacitance $C_s$ across $L$ comes into effect, which reduces the Nyquist locus magnitude by $6 \text{ db/oct}$ in the high pass form and increases it by $6 \text{ db/oct}$ in the low pass form and $C_s$ also adds $90^\circ$ phase lag in the high pass form and $90^\circ$ phase lead in the low pass form. The amplifiers roll off at $6 \text{ db/oct}$ at the high frequency end. Thus the Nyquist locus for the two forms are as shown in the figures. Without $C_s$, the Nyquist locus for the two forms are shown dashed in the figures. It is seen that $C_s$
restores the stability in the high pass form. The corresponding Bode Curves for the two forms are shown in Fig. 1.38 (c) & (d) respectively.

1.4.1 Circuit Analysis for the Complete Antenna Tuning System Using One Amplifier Negative Impedance Converter

The one amplifier voltage controlled negative impedance converter employed to tune an antenna is shown in Fig. 1.39. (The reason for the choice is given in section 3.2).

![Circuit Diagram](image)

Fig. 1.39 One amplifier voltage controlled negative impedance converter (with losses) employed to tune an antenna

The imperfections of the current amplifiers are

- \( r_1 \) - input resistance of the amplifier
- \( r_o \) - output resistance of the amplifier
- \( t_d \) - time delay in the amplifier

The equivalent circuit for Fig. 1.39 is shown in Fig. 1.40, where
the losses can be represented by

\[ y = y_1 + y_2 + \ldots + y_n \quad (1.47) \]

\( n \) is the number of losses and in this case \( n = 5 \) as only five losses are considered important and where

- \( y_1 \) - equivalent shunt admittance of the antenna
- \( y_2 \) - equivalent shunt admittance of the input of the amplifier
- \( y_3 \) - converted value of \( y_2 \)
- \( y_4 \) - equivalent shunt admittance of the output of the amplifier
- \( y_5 \) - equivalent shunt admittance due to time delay
- \( C_2 \) - converted value of \( C_1 = - A C_1 \)

The above losses are tabulated in Table 1.3
\[ y_1 = \frac{r_L}{(\omega L)^2} \]

- \( r_L \) is the series loss of \( L \)

\[ y_2 = \frac{1}{(\omega c)^2 r_1} \]

- \( r_1 \) is the input resistance of the amplifier

\[ y_3 = -A \cdot y_1 \]

- \( -A \) is the gain of the amplifier or the feedback factor

\[ y_4 = y_o = \frac{1}{y_0} \]

- \( r_o \) is the output resistance of the amplifier

\[ y_5 = y_T = -\frac{C}{t_d} \cdot A \]

- \( t_d \) is the amplifier delay time

**Table 1.3** Losses of the one amplifier negative immittance converter employed to tune an antenna

Fig. 1.40 can be simplified to Fig. 1.41 and the condition for the system stability is

\[ y \gg 0 \]

i.e., \( (y_1 + y_2 + y_3 + y_4 + y_5) \gg 0 \)

![Simplified equivalent circuit](image)

**Fig. 1.41** Simplified equivalent circuit of Fig. 1.40

The Nyquist locus for the one amplifier voltage-controlled negative immittance converter used to tune a
ferrite rod antenna is shown in Fig. 1.42. Curve a is the Nyquist locus if the losses in the antenna and the input and output impedance of the current amplifier are considered. Curve b is the Nyquist locus if the time delay in the amplifier is also considered but with negative feedback; it is seen that this will reduce the system Q. As \( G_1 \) increases, it is tilted more to the right. Curve C is the Nyquist locus if time delay in the amplifier is considered but with positive feedback. As \( G_1 \) increases it is tilted to the left. It is seen that the system Q is increased as it goes towards instability.

1.5 Gyrators

An ideal gyrator is an active 2 port linear element and its transmission matrix has been defined (ref. 1.16) by

\[
\begin{bmatrix}
A_{gy}
\end{bmatrix} = \begin{bmatrix}
0 & + \frac{1}{G} \\
+G & 0
\end{bmatrix}
\] (1.48)
where $G$ is the gyration conductance. The symbol has been used for a gyror is shown in Fig. 1.43.

![Diagram](image)

**Fig. 1.43** Symbol for a gyror

The equation for the two ports can be written in matrix form as

$$
\begin{bmatrix}
V_1 \\
I_1
\end{bmatrix} =
\begin{bmatrix}
0 & \frac{1}{G} \\
G & 0
\end{bmatrix}
\begin{bmatrix}
V_2 \\
-I_2
\end{bmatrix}
\tag{1.49}
$$

Eq. 1.49 can be split into two equations:

$$
I_1 = GV_2 \\
I_2 = -GV_1
\tag{1.50}
$$

The input impedance at port 1 is

$$
Z_1 = \frac{V_1}{I_1} = \frac{-I_2/G}{GV_2} = \frac{1}{G^2} \cdot \frac{1}{-V_2/I_2} = \frac{1}{G^2Z_2} \tag{1.51}
$$

Eq. 1.51 shows the well known impedance inversion characteristics of a gyror.

**1.5.1 Gyror formed by cascading an NIC with an NII**

It is of interest that impedance inversion can also
be obtained by cascading a negative immittance converter (NIC) with a negative immittance inverter (NII) (ref. 1.17, 1.18, 1.19) as shown in Fig. 1.44. i.e.,

Fig. 1.44 A gyrator formed by cascading an NIC with an NII

This is shown below by manipulating the transmission matrix \([ A ]\). For an NII with impedance inversion ratio \(1/H\), the equation for the two ports expressed in matrix form is

\[
\begin{bmatrix}
V_1 \\
I_1
\end{bmatrix} = \begin{bmatrix}
0 & + \frac{1}{\sqrt{H}} \\
-\sqrt{H} & 0
\end{bmatrix} \begin{bmatrix}
V_2 \\
-I_2
\end{bmatrix} 
\]

where the transmission matrix

\[
\begin{bmatrix}
A_{\text{NII}}
\end{bmatrix} = \begin{bmatrix}
0 & + \frac{1}{\sqrt{H}} \\
-\sqrt{H} & 0
\end{bmatrix} 
\]

The transmission matrix for an NIC with conversion ratio \(K\) is given by

\[
\begin{bmatrix}
A_{\text{NIC}}
\end{bmatrix} = \begin{bmatrix}
\pm \sqrt{K} & 0 \\
0 & + \frac{1}{\sqrt{K}}
\end{bmatrix} 
\]
When cascading an NIC with an NII, their transmission matrixes multiply, thus

\[
\begin{pmatrix}
A_{NIC} \\
A_{NII}
\end{pmatrix} = \begin{pmatrix}
\pm \sqrt{K} & 0 \\
0 & \mp \sqrt{K}
\end{pmatrix} \begin{pmatrix}
0 & \pm \frac{1}{\sqrt{H}} \\
\mp \sqrt{H} & 0
\end{pmatrix}
\]

\[
= \begin{pmatrix}
0 & \pm \frac{\sqrt{K}}{\sqrt{H}} \\
\frac{\sqrt{H}}{K} & 0
\end{pmatrix}
\]

(1.55)

The right hand side of eq. 1.55 is the transmission matrix of a gyrator of gyration conductance \( G = \frac{\sqrt{H}}{K} \).

However, this is not an economical way to realize a gyrator.

1.5.2 Transconductance gyrator and transresistance gyrator

As with immittance converters there are two types of gyrator (ref. 1.20):

Transconductance gyrator

As indicated by eq. 1.50, a transconductance gyrator can be formed by two voltage controlled current sources (ref. 1.21, 1.22) or two transconductances connected back to back as shown in Fig. 1.45 one with no phase inversion and one with phase inversion.

![Diagram](image)

Fig. 1.45 A transconductance gyrator formed by two voltage controlled current sources
A voltage controlled current source can be decomposed into a voltage amplifier and a current amplifier with a passive conductance $g$ between them as shown in Fig. 1.46.

![Diagram](image)

**Fig. 1.46** A voltage controlled current source decomposed into a voltage and a current amplifier with a passive conductance between them.

The transconductance

$$G = G_v g G_I$$

where $G_v$ and $G_I$ are the gain of the voltage and current amplifier respectively. Thus if the two passive conductances are brought out of the gyrator and each forms a port, the original two port device becomes a four port device (ref. 1.20) as shown in Fig. 1.47. The transconductance gyrator is formed by port 1 and port 3 when port 2 and port 4 are terminated by passive conductances. The transfer resistance gyrator is formed by port 2 and port 4 when port 1 and port 3 are terminated with resistances as will be discussed in the next section.
Fig. 1.47 Four port configuration of a gyrator formed by two voltage and two current amplifiers

For the transconductance gyrator, the input admittance at port I is given by

\[ Y_1 = Y_2 Y_4 \cdot G_{V1} G_{V2} \cdot G_{I1} G_{I2} \cdot \frac{1}{Y_3} \]  
(1.57)

\[ Y_1 = G^2 \frac{1}{Y_3} \]  
(1.58)

Assuming \( Y_2 = Y_4 = g \) and \( G = Y_2 G_{V1} G_{I1} = Y_4 G_{V2} G_{I2} \), where \( G_{V1}, G_{V2}, G_{I1} \) & \( G_{I2} \) are the gain of the voltage amplifiers \( V_1 \), \( V_2 \) and current amplifiers \( I_1 \) and \( I_2 \) respectively. Eq. 1.58 shows that it has the characteristic of admittance inversion.

Eq. 1.57 indicates that:

(1) If \( Y_3 \) and \( Y_4 \) are conductances, port 1 and port 2 become an admittance converter.
(2) If \( Y_3 \) and \( Y_2 \) are conductances, port 1 and port 4 become an admittance converter.

**Transresistance gyrator**

If port 1 and port 3 of Fig. 1.47 are terminated with resistances, then port 2 and port 4 form a transfer resistance gyrator because it now consists of two current controlled voltage sources. The input impedance at port 2, when port 4 is terminated with \( Z_4 \), is given by

\[
Z_2 = \frac{Z_1 Z_3}{Z_4} G_{V1} G_{V2} G_{I1} G_{I2} \quad \text{.......... (1.59)}
\]

\[
Z_2 = \frac{R^2}{Z_4} \quad \text{................................. (1.60)}
\]

if \( Z_1 = Z_3 = r \) and \( Z = Z_1 G_{V1} G_{I2} = Z_3 G_{V2} G_{I1} \).

Eq. 1.59 indicates that:

(1) If \( Z_4 \) and \( Z_3 \) are resistance, then port 1 and port 2 become an impedance converter.

(2) If \( Z_4 \) and \( Z_1 \) are resistance, then port 2 and port 3 become an impedance converter.

1.5.3 Stability Considerations for Gyrators

A gyrator can be terminated with two capacitors to form a resonant circuit. In the transconductance gyrator, the two capacitors will introduce a 180° phase lag while in the transfer resistance gyrator 180° phase lead. The Nyquist plots for the above two cases are shown in Fig. 1.48. The time delay \( t_d \) in the four amplifiers will introduce a phase lag angle \( \theta \) (\( \theta = \omega t_d \)), which will bring the Nyquist curve of
the transconductance gyrator across the negative real axis
and brings that of the transresistance gyrator away from the
axis, as shown dotted in the figure. According to the Nyquist
stability criterion, the transfer conductance gyrator employed
in this way is unstable.

![Nyquist locus diagram]

Fig. 1.48 Nyquist locus for the transresistance gyrator and transconductance gyrator when terminated
with two capacitors.

1.5.4 Effect of Time Delay in Gyrators

The immittances due to the time delay $t_d$ in the
transresistance gyrator and transconductance gyrator will be
deduced below.

Let $Y_{12}$ and $Y_{21}$ be the transfer admittance for the
transconductance gyrator and $Z_{12}$ and $Z_{21}$ be the transfer
impedance for the transresistance gyrator. They can also be
written as

\begin{align*}
Y_{12} &= y_{21} e^{-j\Theta_{12}} \\
Y_{21} &= y_{21} e^{-j\Theta_{21}} \\
Z_{12} &= z_{12} e^{-j\Theta_{12}} \\
Z_{21} &= z_{21} e^{-j\Theta_{21}}
\end{align*} \quad (1.61)
where $y_{12}$, $y_{21}$, $z_{12}$ and $z_{21}$ are the modulus of the $Y_{12}$, $Y_{21}$, $Z_{12}$ and $Z_{21}$ respectively and $\theta_{ij}$ is the phase shift from point i to j in the circuit.

Consider the input admittance $Y_1$ (eq. 1.58) of a transconductance gyrator when loaded with a capacitor $C$.

\[
Y_1 = \frac{y_{12} e^{-j\theta_{12}} y_{21} e^{-j\theta_{21}}}{j\omega C}
\]

\[
= \frac{y_{12} y_{21}}{j\omega C} e^{-j(\theta_{12} + \theta_{21})}
\]

Let $\theta_{12} + \theta_{21} = \theta = \omega t_d$

\[
= \frac{y_{12} y_{21}}{j\omega C} e^{-j\theta} = \frac{y_{12} y_{21}}{j\omega C} (1-j\theta) \text{ if } \theta \text{ is small}
\]

\[
= \frac{y_{12} y_{21}}{j\omega C} - \frac{y_{12} y_{21} \theta}{\omega C}
\]

\[
= \frac{y_{12} y_{21}}{j\omega C} - \frac{y_{12} y_{21} t_d}{C} \quad \text{............ (1.62)}
\]

The first term on the R. H. S. of eq. 1.62 is the simulated inductance and the second is a negative conductance due to the time delay $t_d$, which will cause instability.

Similarly, for the transfer resistance gyrator, by using eq. 1.60, it can be shown that

\[
Z_1 = \frac{z_{12} z_{21} e^{-j\theta}}{z_3}
\]

\[
Z_1 = z_{12} z_{21} \frac{j\omega C + z_{12} z_{21} \omega \theta}{C} \quad \text{... (1.63)}
\]
Eq. 1.63 shows that the time delay introduces a positive resistance \( z_{12} z_{21} \omega C \theta \). The Q of the simulated inductance is

\[
Q = \frac{z_{12} z_{21} \omega C}{z_{12} z_{21} \omega C \theta} = \frac{1}{\theta}, \quad \theta \text{ in radian/sec.}
\]

which is inversely proportional to the phase delay \( \theta \).

### 1.5.5 Remarks

In both types of gyrators, the two reactances placed at the input and output port tune each other because each will gyrate an inductance (or capacitance) from the capacitor (or inductor) terminated at the output port to tune the capacitor (or inductor) terminated at the input port. Meanwhile, the gyrator will also gyrate the inverse of the reactance placed at the input port to tune the reactance terminated at the output port. Although both types of the gyrator perform the same gyration function, they have different properties. In the transconductance gyrator, time delay will introduce a negative conductance when both ports are terminated with capacitors and thus they may be unstable; but the time delay will introduce a positive resistance when both ports are terminated with inductors. For the transfer resistance gyrator the situation is reversed.

A summary of the configurations for one amplifier immittance converters, two amplifier immittance converters and the gyrators is given in Table 1.4.
<table>
<thead>
<tr>
<th>Type of Input Immittance</th>
<th>Single Passive Impedance</th>
<th>Single Amplifier Impedance Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$Y$</td>
<td>$Z$</td>
</tr>
<tr>
<td>Condition of Stability</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Controlled</td>
<td>$V$</td>
<td>$I$</td>
</tr>
<tr>
<td>Loop Gain</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Impedance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Due to Active Component</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Amplifiers</td>
<td>$V$</td>
<td>$I$</td>
</tr>
<tr>
<td>Block Diagrams</td>
<td><img src="image1.png" alt="Diagram" /></td>
<td><img src="image2.png" alt="Diagram" /></td>
</tr>
<tr>
<td>Input Impedance</td>
<td>$Y$</td>
<td>$Z$</td>
</tr>
</tbody>
</table>

**Table 1.4** Summary of the configurations for one amplifier immittance converters, two amplifier immittance converters and immittance gyrators.
<table>
<thead>
<tr>
<th>Two Amplifier Immittance Converter</th>
<th>Immittance Gyror</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Y</strong></td>
<td><strong>Z</strong></td>
<td><strong>Y</strong></td>
</tr>
<tr>
<td>$(\text{Real} Y_L + \text{Real} Y_I) &gt; 0$</td>
<td>$(\text{Real} Z_L + \text{Real} Z_I) &gt; 0$</td>
<td>$(\text{Real} Y_L + \text{Real} Y_I) &gt; 0$</td>
</tr>
<tr>
<td>$V$</td>
<td>$I$</td>
<td>$V$</td>
</tr>
<tr>
<td>$-$</td>
<td>$+$</td>
<td>$-$</td>
</tr>
<tr>
<td>$+$</td>
<td>$-$</td>
<td>$-$</td>
</tr>
<tr>
<td>$V + I$</td>
<td>$V + I$</td>
<td>$2(V + I)$</td>
</tr>
</tbody>
</table>

\[ Y_1 = G_Y \frac{G_V}{G_I} \]

\[ Z_1 = G_V \frac{G_I}{G_Z} \]

\[ Y_1 = \frac{G^2}{Y_3} \]

\[ G = G_{V1} \frac{g}{G_{II}} \]

\[ = G_{V2} \frac{g}{G_{I2}} \]

\[ Z_1 = \frac{R^2}{Z_3 G_{V1}} \]

\[ R = G_{II} \frac{r}{G_{V2}} \]
CHAPTER 2

RECEIVING SYSTEMS WITH ACTIVE TUNING ELEMENTS

2.1 Introduction

The introduction to the thesis gives reasons why synchronous detection systems and phase-locked-loops will be used in integrated broadcast receivers and why active tuning will be desirable for the antenna systems. Since the active circuit tuning systems which are the subject of the thesis will be used with phase-locked receiver systems, this chapter will be concerned with these systems.

The above mentioned phase-locked systems may take many forms, but they all have the general form shown in Fig. 2.1, i.e., the system provides a signal which tunes the local oscillator to the correct frequency and the same signal may be used to tune the antenna system. If the receiver is a

![Diagram](image)

Fig. 2.1 A general form of phase-locked systems.
tuned-radio-frequency system, the local oscillator is tuned to the same frequency, as is the antenna.

This chapter will open with the general theory of phase-locked-loop systems. Then a particular system will be used as an example and finally possible tuning systems which appear to meet the requirements of the receiver system will be discussed (ref. 2.1).

An important requirement is that the antenna must be automatically tuned to the local oscillator frequency, that is, the local oscillator must track the antenna and this can be obtained by active tuning elements such as immittance converters and gyrators.

2.1.1 Phase-locked-loop

A block diagram of phase-locked-loop system is shown in Fig. 2.2 (ref. 2.2). Phase-locked loop techniques have been well developed in the literature (ref. 2.3, 2.4, 2.5, 2.6). The principle of operation is briefly as follows. The phase comparator compares the instantaneous phase of the

\[ V_s(t) = E_s \sin \omega_s t \]

\[ V_o(t) = E_0 \sin (\omega_0 t + \phi_0) \]

Fig. 2.2 A block diagram of phase-locked loop system
incoming signal with that of the voltage controlled oscillator (VCO) output and produces an error voltage proportional to the phase difference of the two input signals. The error voltage is filtered to reduce noise and high frequency components and then amplified. The amplifier output is used to control the VCO forming a corrective feedback loop so that the VCO varies in such a direction to reduce the phase difference between the incoming signal and its output frequency until they are locked or synchronized, if the input signal is close to the free-running frequency of the VCO or it is within its capture range. This brings out the following two significant features which make the phase-locked loop techniques compatible with the integrated circuit technology.

(a) Since the VCO automatically tunes to the carrier signal, the system does not demand high accuracy and high stability of component values which can be accomplished by integrated circuit without difficulty.

(b) Since the centre frequency $f_o$ of the synchronization detector is equal to the carrier signal, the frequency conversion is directly from radio frequency to audio and no intermediate frequency stage is needed. The bandwidth of the radio frequency signal is determined by the low pass or audio filter.
2.1.2 A Synchronous AM Detecting System

A basic synchronous AM detecting system (ref. 2.7) is shown in Fig. 2.3. The received signal $V_s(t)$ and the synchronous local oscillator output $V_o(t)$ are mixed in the mixer, producing the desired output $V_m(t)$ which is filtered and then amplified to the desired level. The above process can be expressed mathematically as follows:

Let $V_s(t) = A_c \left[1 + S(t)\right] \cos (\omega_c t + \theta_c)$

$V_o(t) = A_o \cos (\omega_o t + \theta_o)$ \hspace{1cm} (2.1)

The mixer output is given by

$V_m(t) = A_c A_o \left[1 + S(t)\right] \cos (\omega_c t + \theta_c) \cos (\omega_o t + \theta_o)$

$= \frac{A_c A_o}{2} \left[1 + S(t)\right] \left\{ \cos \left[ (\omega_c + \omega_o) t + \theta_c + \theta_o \right] + \cos \left[ (\omega_c - \omega_o) t + \theta_c - \theta_o \right] \right\}$ \hspace{1cm} (2.2)

Because of synchronization $\omega_o = \omega_c$

$V_m(t) = \frac{A_c A_o}{2} \left[1 + S(t)\right] \cos (2\omega_c t + \theta_c + \theta_o)$

$+ \frac{A_c A_o}{2} \cos (\theta_c - \theta_o) + \frac{A_c A_o}{2} S(t) \cos (\theta_c - \theta_o)$ \hspace{1cm} (2.3)
After filtering, the output is

\[ V_m(t) = \frac{1}{2} A_c A_0 S(t) \cos(\theta_c - \theta_0) \]

\[ = CS(t) \cos \theta_f \] ............................. (2.4)

where \( C = \frac{1}{2} A_c A_0 \) and \( \theta_f = \theta_c - \theta_0 \). \( \theta_f \) is the phase difference between the received carrier and the local oscillator frequency. \( V_m(t) \) is maximum when \( \theta_f = 0 \) and zero when \( \theta_f = 90^\circ \).

Thus to obtain the maximum output not only the oscillator frequency must be equal to the carrier frequency but also the phase angle of the oscillator frequency must be equal to that of the carrier frequency. Fig. 2.4 is a complete AM synchronous detecting system which meets the requirements. It is a two phase synchronous detection system: the in-phase and the quadrature-phase.

Fig. 2.4  A complete synchronous AM detector
If there is no frequency and phase difference between the received carrier and the local oscillator, the in-phase channel will give maximum audio output while the quadrature-phase channel give zero output due to the 90° phase shift in it. The phase detector will produce no phase-correcting voltage. If there is a phase error in the local oscillator output, the audio output in the in-phase channel is reduced while some will present in the quadrature phase channel. The phase detector will produce a dc phase correcting voltage whose magnitude depends on the phase error and whose sign depends on the sign of the phase error. After passing through the automatic phase control (APC) filter, the dc voltage is applied to the varactor thereby correcting the phase angle of the local oscillator frequency. Such a phase control loop will not only control the local oscillator phase angle but also correct its frequency over a few KHz in AM broadcast band.

2.1.3 Tracking the Antenna with the Local Oscillator

Active tuning elements such as immittance converters which can change the magnitude of the immittance of one element of a tuned circuit can be used to tune the antenna or the local oscillator. Gyrator is another form of active tuning element which can change the inverted magnitude of an immittance, which is one element of a tuned circuit, can also be used to tune the antenna or the local oscillator. However, it is easier to track two similar active tuning elements fabricated on a silicon ship than if they are of different kind.
Thus with two similar active tuning elements on a chip, one is used for the antenna tuner and one for the local oscillator, the tracking problem will be solved. There are three feasible sets of active tuning elements listed in Table 2.1 that could be used for this tracking purposes.

<table>
<thead>
<tr>
<th>CASE</th>
<th>ANTENNA</th>
<th>LOCAL OSCILLATOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>![IC circuit diagram]</td>
<td>![IC circuit diagram]</td>
</tr>
<tr>
<td>2</td>
<td>![IC circuit diagram]</td>
<td>![GY circuit diagram]</td>
</tr>
<tr>
<td>3</td>
<td>![GY circuit diagram]</td>
<td>![GY circuit diagram]</td>
</tr>
</tbody>
</table>

Table 2.1 Three feasible sets of active tuning elements

Case I Employs two identical immittance converters as the active tuning elements and two identical pairs of passive elements L and C. Due to fabrication discrepancies, final tracking adjustments can be made by trimming the trimmer across C or adjusting the inductance in the local oscillator. Good screening for this inductance is essential.
Case II  An immittance converter is used to tune the antenna and a gyrator is used for the local oscillator. This scheme replaces one inductor with a capacitor and thus has the following advantages:

(1) Capacitors can be made in integrated circuits but inductors cannot.

(2) Inductors are generally more expensive than capacitors.

(3) It eliminates the screening problem for the inductor.

The screening problem for the capacitor is not difficult. Because of the very small distance between its two plates, its stray capacitance associated with the nearby objects is small compared with its original value and screening can be done by proper arrangement of the two plates and earthing one of them, thus eliminating the external electrostatic effects. But inductors will extract and store electromagnetic energy from the space and also have mutual coupling with its nearby objects and thus it needs careful screening by housing it properly in an earthed high conductivity metal can. However, as this scheme employs two different active elements, it is not so easy for them to track as for one with two similar active elements.

Case III  Two identical gyrators are employed, one for the antenna tuner and one for the oscillator. Both inductors are on the antenna tuner. One of them may be screened or both unscreened (thus eliminating the screening problem)
and placed 90° to each other in order to produce a better receiving field pattern. Final tracking adjustments can be made by trimming the trimmers added across the two capacitors.
CHAPTER 3

CIRCUIT REALIZATION

3.1 Introduction

This chapter will consider the circuit realization of the immittance converters and gyrators treated in Chapter 1. The immittance converters and gyrators are partitioned into voltage and current amplifiers which are the basic building blocks. In addition, constant current sources and current gain control are employed in all the circuit realizations. They are also considered as basic building blocks. Thus, it is most convenient to realize these blocks first and then employ them to realize the separate immittance converters and gyrators. The capacitors and inductors terminated at the series and shunt ports are conventional passive elements and need no further description.

It was shown in Chapter 1 that there are two possible forms to employ the immittance converter to tune the antenna, i.e., the high pass form and the low pass form. It was shown that the time delay in the high pass form introduces a loss factor whereas in the low pass form a negative parasitic impedance. Thus for reasons of stability the high pass form is preferred and chosen for realizations.
3.1.1 Realizations of the High Pass Form Two Amplifier Immittance Converter

A block diagram of a convenient two amplifier immittance converter system is shown in Fig. 3.1. It consists of a unity gain voltage amplifier, unity gain current amplifier, current gain control, constant current sources, voltage level shifting and phase inversion for overall negative feedback.

3.1.2 Voltage Amplifier

The block diagram of a unity gain voltage amplifier is shown in Fig. 3.2 and its ideal characteristics are input impedance $Z_1 = \infty$, output impedance $Z_0 = 0$ and time delay $t_d = 0$. Because $Z_1 = \infty$ and $Z_0 = 0$, its current gain and
power gain are infinite.

![A unity gain voltage amplifier](image)

**Fig. 3.2** A unity gain voltage amplifier

Unity gain (ref. 3.1) is employed, because it is easy to obtain by using a differential amplifier with a feedback factor $\mu = -1$ (obtained by returning the output to one of the inputs as shown in Fig. 3.2). For example, if the voltage gain $G_v = 10^6$, the amplifier gain $G_{vo}$ with feedback factor $\mu = -1$ is

$$G_{vo} = \frac{G_v}{1-\mu G_v} = \frac{10^6}{1+10^6} = 0.999999$$

which is accurate to 0.0001%. If $G_v = \infty$, $G_{vo} = 1$. Component variations due to temperature changes or aging may cause considerable changes in $G_v$ but negligible changes in $G_{vo}$, i.e. the unity gain is insensitive to component variations. This is an important characteristic as the imittance conversion ratio depends on the amplifier gain.

As the current gain $A_i$ of a voltage amplifier is
closely related to the performance of an active tuning circuit, the following will consider

(1) the relation of $A_i$ of the voltage amplifier, its input impedance $Z_1$ and output impedance $Z_0$, and

(2) the relation of $A_i$ and the $Q$ of a LC tuned circuit, when they are incorporated in an active tuning loop.

(1) Since the current gain $A_i$ remains unchanged with or without the series voltage negative feedback, the feedback will increase $Z_1$ by the same factor that $Z_0$ is reduced. Thus, when $G_{VO} = 1$

$$\frac{i_0}{i_1} = A_{i_0} = A_i$$

But

$$\frac{i_0}{i_1} = \frac{Z_1}{Z_0}$$

Thus

$$A_{i_0} = A_i = \frac{Z_1}{Z_0} \quad \text{............... (3.1)}$$

(2) If the amplifier is used in active tuning and assuming a lossless LC circuit, $Z_0$ will be in series with the LC circuit and $Z_1$ in shunt with it as shown in Fig. 3.3. The final $Q$ of the circuit is given by

![Diagram](image)

Fig. 3.3 Effect of amplifier loss on LC circuit
\[ Q = \frac{\omega L}{(\omega L)^2 + Z_0} \] ........................ (3.2)

if \( Z_1 \gg \omega L \)

As seen from eq. 3.1, a large current gain is required for high \( Q \). Field effect transistors have an extremely high \( A_i \) \( (A_i = 10^6 \), say). However, they are not generally compatible with integrated circuits. Thus bipolar transistors will be considered, but because of their small current gain \( (A_i \approx 10^2) \), three cascaded stages will be required to have the same order of current gain as that of a single field effect transistor. The increased number of stages will increase the time delay \( t_d \). As shown in sections 1.1.4, 1.2.3 and 1.5.4, \( t_d \) can introduce a positive or negative immittances. Thus extra losses or instability may be introduced. So a compromise has to be sought between \( A_i \) and \( t_d \). The circuit diagram is shown in Fig. 3.4. A simple

Fig. 3.4 A circuit diagram of a unity gain voltage amplifier
differential amplifier is employed to avoid time delay. As a large ratio of $Z_1/Z_0$ is required for high $Q$, a large current gain $A_1$ is needed. High $Z_1$ is obtained by adding an emitter follower $Q_4$ to the input of the differential pair and also by returning the $Q_4$ collector to that of $Q_2$ as shown dotted in Fig. 3.5 so that the negative feedback will eliminate the effect of $C_{bc}$ of $Q_4$ on $Z_1$. Assuming the output is terminated in a low impedance (Ref. 3.5)

![Circuit Diagram]

**Fig. 3.5** A unity gain voltage amplifier with high input impedance

\[
Z_{1V} \approx 2 \beta r_e (\beta) = 2 \beta^2 r_e \tag{3.3}
\]

where \( r_e = \frac{26}{I_B(\text{ma})} \)

\( \beta \) = current gain of $Q_1$, $Q_2$, $Q_3$ and $Q_4$ (assumed equal)
It is noted that in Fig. 3.4 and 3.5 all resistors are replaced by constant current sources. To provide bias currents $I_1$, $I_2$, and $I_3$ ordinary constant current sources shown in Fig. 3.10 (a) and (b) will suffice, but to bias $I_4$ a constant current source with a $10 \times 10^6$ output resistance will be required so that its shunting effect across the series port will be negligible. As constant current sources will be required in the rest of the realizations, we will discuss them in the following section. As the output impedance of the voltage amplifier $Z_0$ is the same as the input impedance $Z_1$ of the current amplifier, it is considered in section 3.1.4.

### 3.1.3 Constant Current Sources

The function of a constant current source (ref. 3.2) is to provide a constant bias current for a circuit. Its circuit symbol is shown in Fig. 3.6. Its ideal practical characteristics (shown in Fig. 3.7) are

1. Its ac output impedance $R_o = \frac{\Delta V_o}{\Delta I_o} = \infty$ over the operating range.
2. Its dc resistance $R_{dc} = \frac{V_o}{I_o}$ should be small.
3. The lowest operating voltage $V_o$ should be small.

![Fig. 3.6 A constant current source](image)

![Fig. 3.7 Characteristic of an ideal practical constant current source](image)
The above mentioned characteristics for a constant current source are not obtainable but may be approximated in practice. Non-ideal constant current sources are realized by

(1) A resistor and a DC power supply

(2) The collector of a transistor

The second method gives much superior characteristics than the former.

(I) **Constant current source formed by a resistor and a DC power supply**

In this method \( R_o = R_{dc} \). In order to have a constant current of 1 mA and \( R_o = 1 \) mA, a DC power supply of \( 1 \times 10^{-3} \times 10^6 = 10^3 \) volts is required. This example illustrates the drawback of this method.

(II) **Constant current source formed by the collector of a transistor**

A. **By the collector of a common base transistor**

The output characteristics of a common base transistor is shown in Fig. 3.8. In the active region (emitter base forward biased, collector base reverse biased), the output resistance of the collector is given by

\[
R_o = r_b + r_c - \frac{r_b \left( r_b + \alpha r_c \right)}{R_s + r_e + r_b} \quad \cdots \quad (3.4)
\]

where \( r_b \) = the base resistance

\( r_c \) = the collector resistance

\( r_e \) = the emitter resistance

and \( R_s \) = the input source resistance

\( R_o \) is of the order of megohms and provides a
good constant current source which needs a dc supply voltage of the order of one volt only. The small slope of the output characteristics in the active region is due to the following:

(a) As $I_c = \alpha I_E$, the decrease of the base width (because the space charge in the collector base junction increases towards the base as $V_{CB}$ increases) reduces the chance of carriers recombination in the base and thus increases the $\alpha$ as $V_{CB}$ increases.

(b) The decrease in base width, as $V_{CB}$ increases, increases the charge gradient in the base and thus increases the minority carriers $I_E$ injected across the emitter junction.

![Graph](image)

Fig. 3.8 Output characteristic of a common base transistor
B. By the collector of a common emitter transistor

The output characteristics of a common emitter of a transistor is shown in Fig. 3.9. The active region, which is beyond the knee of the curves, can be used as a constant current source with an output impedance

\[ r_o = r_c (1 - \alpha) + r_e \frac{R_s + r_b + \alpha r_c}{R_s + r_b + r_e} \]

In this region, the slope of the curves is larger than those in the common base configuration because the base width modulation effect on \( I_C \) by \( V_{BE} \) mentioned above is more serious in this case. Because \( I_C = \beta I_B \), assuming \( \alpha = 0.98 \), 0.5% change in \( \alpha \) will cause 34% change in \( \beta \).

Although common base configuration provides higher source impedance, the common emitter configuration is preferred as this form is conveniently fabricated in integrated circuit. However, stabilizing circuits can be employed to improve the output impedance.

![Output characteristic of a common emitter transistor](image-url)
Three constant current sources (ref. 3.2) are shown in Fig. 3.10. In Fig. 3.10 (a), $R_3$ stabilizes the emitter current of $Q_1$, it is a good constant current source but not economical in integrated form as it employs three resistors. Fig. 3.10 (b) shows a practical constant current source, the emitter current of $Q_2$ is stabilized by that of $Q_1$ which is connected as a diode. If $Q_1$ and $Q_2$ are identical, $i \approx \frac{V_a + V_b}{R}$ Fig. 3.10 (c) is a cascode form constant current source whose output impedance is more than $10 \, \text{M} \Omega$ because of the following:

1. The collector of $Q_5$ is employed as the emitter load for $Q_6$ which stabilizes the emitter current of $Q_6$ extremely well.

2. The Darlington pair $Q_6$ and $Q_7$ increases the current gain of the composite transistor. The higher the current gain the less effect of $I_B$ on $R_0$. If $\beta = \infty$, $I_B = 0$ then $I_C = I_E$, the output characteristics are horizontal and $R_0 = \infty$.

Fig. 3.10  Constant current sources
3.1.4 Unity Gain Current Amplifier

The ideal characteristics of a unity gain current amplifier are $Z_1 = 0$, $Z_0 = \infty$ and $t_d = 0$. In practice, this means a low value of $Z_1$, a high value of $Z_0$, a small time delay $t_d$ and a gain close to unity. These appear to match the characteristics of a common base transistor amplifier. However, the common base amplifier alone does not provide the required high $Z_0$ and low $Z_1$. Other circuit techniques such as negative feedback are employed to reduce $Z_1$ and cascode form output to increase $Z_0$. Fig. 3.11 shows the circuit diagram of the current amplifier. The large time delay is avoided by the short feedback loop and the high cut-off frequency of the common base configuration.

![A unity gain current amplifier](image)

Fig. 3.11 A unity gain current amplifier

$Q_1$ is a voltage amplifier whose output is fed back to the base of the common base amplifier $Q_2$ in order to obtain low $Z_1$. Bias is provided by the constant current sources.
An approximate treatment is given below.

\[ Z_1 = \frac{V_1}{i_1} \] where \( V_1 \) is the input voltage and \( i_1 \) the input current.

But \( v_1 \approx i_{c1} r_{e1} \), thus \( Z_1 \approx \frac{i_{c1} r_{e1}}{i_1} \)

But \( i_{c1} \approx \frac{i_{e2}}{\beta_2} \) thus \( Z_1 \approx \frac{i_{e2}}{\beta_2} \cdot \frac{r_{e1}}{i_1} \)

But \( i_{e2} \approx i_1 \), thus \( Z_1 \approx \frac{r_{e1}}{\beta_2} \) \(............... \) (3.5)

Experimentally \( Z_1 \) given by eq. 3.5 is valid at low frequencies, but increases at high frequencies (see Fig. 4.1) and reduces the Q to an unacceptable value. This is unexplainable by the well known relation \( \beta = \frac{f_\alpha}{f_\beta} \) (where \( \beta \) is the common emitter current gain at low frequency, \( f_\alpha \) is the 3 db \( \alpha \) cut off frequency and \( f_\beta \) is the 3 db \( \beta \) cut off frequency).

As \( f_\alpha = 600 \) MHz for transistors 2N918 and \( \beta = 100 \), then \( f_\beta = 6 \) MHz. But experimentally \( f_\beta = 1.3 \) MHz. Evidently, the parasitic effects due to the stray capacitances \( C_{be1} \) and \( C_{be2} \) at the emitter base of \( Q_1 \) and \( Q_2 \) at high frequencies must be considered. \( C_{be2} \) has a larger shunting effect on \( Z_1 \) as its capacitance is magnified by the voltage gain \( G_v \) of \( Q_1 \). Thus the total stray admittance shunting the input is

\[ Y_{Sh} = j\omega C_{be1} + j\omega C_{be2} (1+G_v) \] \(............... \) (3.6)

In future work, accurate circuit analysis and redesign the amplifier for low \( Z_1 \) throughout the operating frequency range are required.
3.1.5 Current Gain Attenuator

A method used to control the current gain is shown in Fig. 3.12. This is a conventional method which is used by integrated circuit manufacturers (ref. 3.3) eg., in receiver automatic gain control systems.

![Diagram of current gain attenuator]

**Fig. 3.12** A current gain attenuator

The current gain $M$ is defined by

$$M \approx \frac{I_{c1}}{I_{c1} + I_{c2}} \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (3.7)$$

where $I_{c1} + I_{c2} \approx I_{E1} + I_{E2} = I_{dc}$ is supplied by the constant current source and $1 \geq M > 0$.

The ratio of the collector currents $\frac{I_{c1}}{I_{c2}}$ can be controlled by a differential bias voltage $(V_{1} - V_{2})$ at the bases of $Q_1$ and $Q_2$; the relation between the bias and the current gain is developed below.

It is well known that the dc voltage current relation (Fig. 3.13) for an ideal pn junction is given by

$$I = I_{0}^{\text{1}} \left( e^{qV/kT} - 1 \right) \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (3.8)$$
Fig. 3.13  dc voltage and current relation of an ideal pn junction

where \( q = 1.6 \times 10^{-19} \) Coulomb, the electron charge
\( V \) = the applied voltage across the pn junction
\( k = 1.38 \times 10^{-23} \) joule/°K, Boltzmann's constant

\[
I_0' = A'q \left( \frac{p_0D_p}{L_p} + \frac{n_0D_n}{L_n} \right) \text{ the saturation current}
\]

where \( A' \) = area of the junction in cm\(^2\)
\( p_0 \) = acceptor carrier density (cm\(^{-3}\)) in the N region
\( n_0 \) = donor carrier density (cm\(^{-3}\)) in the P region
\( D_p \) & \( D_n \) = diffusion constants for holes and electrons respectively
\( L_p \) = diffusion length of holes in the N region in cm
\( L_n \) = diffusion length of electron carriers in the P region in cm

For the same type of npn transistors and assuming uniformity of the emitter base junction, the collector
The currents of $Q_1$ and $Q_2$ are respectively,

$$I_{c1} = \beta_{11} I_{B1} = \frac{\tau_{B1}}{\tau_{\eta 1}} I_{o1} (e^{\frac{qV_1}{kT_1}} - 1)$$

$$= \frac{\tau_{B1}}{\tau_{\eta 1}} A_1 q \left( \frac{P_{n01}D_p}{I_{p1}} + \frac{n_{p01}D_n}{I_{n1}} \right) (e^{\frac{qV_1}{kT_1}} - 1) \ldots (3.9)$$

And

$$I_{c2} = \beta_{22} I_{B2} = \frac{\tau_{B2}}{\tau_{\eta 2}} \cdot I_{o2} \left( e^{\frac{qV_2}{kT_2}} - 1 \right)$$

$$= \frac{\tau_{B2}}{\tau_{\eta 2}} A_2 q \left( \frac{P_{n02}D_p}{I_{p2}} + \frac{n_{p02}D_n}{I_{n2}} \right) (e^{\frac{qV_2}{kT_2}} - 1) \ldots (3.10)$$

where

$\tau_{B1}, \tau_{B2}$ electron carrier life time in the base of $Q_1$ and $Q_2$ respectively

$\tau_{\eta 1}, \tau_{\eta 2}$ electron carrier transit time through the base of $Q_1$ and $Q_2$ respectively

From eq. 3.9 and 3.10

$$I_{c1} = \frac{\tau_{B1}}{\tau_{\eta 1}} A_1 q \left( \frac{P_{n01}D_p}{I_{p1}} + \frac{n_{p01}D_n}{I_{n1}} \right) (e^{\frac{qV_1}{kT_1}} - 1)$$

$$I_{c2} = \frac{\tau_{B2}}{\tau_{\eta 2}} A_2 q \left( \frac{P_{n02}D_p}{I_{p2}} + \frac{n_{p02}D_n}{I_{n2}} \right) (e^{\frac{qV_2}{kT_2}} - 1)$$

$$\log_e \frac{I_{c1}}{I_{c2}} = \log_e \frac{\tau_{B1}}{\tau_{\eta 1}} A_1 q \left( \frac{P_{n01}D_p}{I_{p1}} + \frac{n_{p01}D_n}{I_{n1}} \right)$$

$$\frac{\tau_{B2}}{\tau_{\eta 2}} A_2 q \left( \frac{P_{n02}D_p}{I_{p2}} + \frac{n_{p02}D_n}{I_{n2}} \right)$$

$$+ \frac{q}{k} \left( \frac{V_1}{T_1} - \frac{V_2}{T_2} \right) \ldots \ldots \ldots \ldots (3.11)$$
In integrated circuit Q_1 and Q_2 are fabricated on a silicon chip. Since they are made under the same diffusion and doping conditions, then the following equalities hold within a reasonable degree of accuracy, certainly better than 1%.

\[
\begin{align*}
\gamma_{B1} &= \gamma_{B2} \\
\gamma_{n1} &= \gamma_{n2} \\
P_{n01} &= P_{n02} \\
N_{p01} &= N_{p02} \\
L_{p1} &= L_{p2} \\
L_{n1} &= L_{n2} \\
\text{Also} \quad T_1 &= T_2 = T
\end{align*}
\]

(3.12)

since both the junctions are on the same chip. However, because of the limitations of the photolithography, the equality \( A_1 = A_2 \) may not hold to the same degree of accuracy.

Using eq. 3.12, eq. 3.11 becomes

\[
\log_e \frac{I_{c1}}{I_{c2}} = \log \frac{A_1}{A_2} + \frac{q}{kT} (V_1 - V_2)
\]

\[
\log_e \frac{I_{c1}A_2^*}{I_{c2}A_1^*} = k' (V_1 - V_2)
\]

(3.13)

where \( \frac{q}{kT} = k' \), a constant. Eq. 3.13 shows that the dc collector current \( I_{c1} \) and \( I_{c2} \) divides in such a way that the
logarithm of the ratio \( \frac{I_{c1}^2}{I_{c2}^2} \) is proportional to the dc differential bias \((V_1 - V_2)\). If ac signal currents are superimposed on \(I_{c1}\) and \(I_{c2}\), it is shown below that they will divide in the same ratio as that of \(I_{c1}\) and \(I_{c2}\). From eq. 3.8, the small signal resistance of the diode is

\[ r = \frac{dV}{dI} = \frac{kT}{q} \cdot \frac{1}{I} \]

Thus the small signal resistance of the emitter and base of \(Q_1\) is

\[ r_1 = \frac{dV_1}{dI_{E1}} = \frac{kT}{q} \cdot \frac{1}{I_{E1}} = \frac{K}{I_{E1}} \]

where \(K = \frac{kT}{q}\)

Similarly,

\[ r_2 = \frac{K}{I_{E2}} \]

\[ \therefore \frac{r_1}{r_2} = \frac{I_{E2}}{I_{E1}} \approx \frac{I_{c2}}{I_{c1}} \]

\[ \hspace{1cm} (3.14) \]

If a signal voltage \(v_1\) is applied at the emitter of \(Q_1\) and \(Q_2\)

\[ i_1 = \frac{v_1}{r_1} \text{ and } i_2 = \frac{v_1}{r_2} \]

Thus

\[ \frac{i_1}{i_2} = \frac{r_2}{r_1} \]

\[ \hspace{1cm} (3.15) \]
Using 3.13, 3.14 and 3.15,

\[ \log_e \frac{i_1}{i_2} = \log_e \frac{Ic1}{Ic2} = \log_e \frac{A_1}{A_2} + K(V_1-V_2), \]

\[ \log_e \frac{i_2A_1'}{i_1A_2'} = \log_e \frac{Ic1A_1'}{Ic2A_2'} = K(V_1-V_2) \quad \ldots \ldots \ldots \quad (3.16) \]

Eq. 3.16 (see also eq. 3.9 and 3.10) is used to determine the current gain \( M \) which is defined by eq. 3.7. Thus when \( V_2 = 0, Ic2 = 0 \), then \( M \approx 1 \). Also when \( V_2 \) increases, \( Ic2 \) increases and \( M \) decreases.

Two emitter coupled pairs fabricated on a chip and with a common bias arrangement as shown in Fig. 3.14, one pair can be used for example, the current gain control on the antenna tuning system (sect. 2.1.4) and the other pair for the current gain control in the local oscillator.

Using eq. 3.16

\[ \log_e \frac{Ic1}{Ic2} \cdot \frac{A_2}{A_1} = \log_e \frac{Ic3A_4'}{Ic4A_3'} = K(V_1-V_2) \quad \ldots \ldots \quad (3.17) \]

Fig. 3.14 Two emitter coupled pairs on a chip with a common bias arrangement
Providing \( \frac{A_2}{A_1} = \frac{A_3}{A_4} \) then \( \frac{I_{c1}}{I_{c2}} = \frac{I_{c3}}{I_{c4}} \) perfect tracking can be obtained. But because of the resolution limitations of the photolithography (usually \( A_1 \approx A_2 \approx A_3 \approx A_4 \)) transistor capacitors may have to be added to the fixed capacitors in the immittance converters (see table 2.1) to obtain satisfactory tracking between the antenna and the oscillator.

**Cascode output to increase output impedance**

Because of the small input resistance \( r_e \) at the emitters of \( Q_1 \) and \( Q_2 \), the collector output impedance of \( Q_1 \)

\[
r_o = r_c (1 - \alpha) + r_e \cdot \frac{R_S + r_b + \alpha r_c}{R_S + r_p + r_e}
\]

is not high enough to meet the requirements. A cascode (ref. 3.4) form output is shown in Fig. 3.15. The collector output impedance \( r_o \) of \( Q_1 \), is employed as the emitter load,

---

**Fig. 3.15** A current gain attenuator with cascode output

\( r_e \) of \( Q_3 \), thus obtaining the high output impedance. Alterna-
tively, the tracking mentioned above may be obtained by a feedback technique which will force the ratio \( \frac{I_{c3}}{I_{c4}} \) to equal \( \frac{I_{c1}}{I_{c2}} \). By this method the stringent requirement on the similarity of the four PN junctions is eliminated.

3.1.6 Current Amplifier with a Gain Greater Than Unity

The ideal port characteristics of this amplifier are the same as those of the unity gain current amplifier discussed in the previous section, except that it has a gain greater than unity. Its block diagram is shown in Fig. 3.16. Because a low input resistance is required, the input is a unity gain amplifier and is followed by a stage with a gain greater than unity. A circuit diagram is shown in Fig. 3.17. The current gain \( G_I \) is determined primarily by \( R_1 \) and \( R_2 \), providing the conditions stated below are met.

![Diagram](image-url)

**Fig. 3.16** A current amplifier with a gain greater than unity
Fig. 3.17 Circuit diagram of a current amplifier with a gain greater than unity

The input resistance at the base of $Q_2$ is given by

$$r_{12} = \beta (r_e + R_2)$$

neglecting parasitic effects associated with the base of $Q_2$.

The current gain of the complete amplifier is given by

$$G_I \approx \frac{i_{o2}}{i_{ll}}$$

$$\approx \beta_2 \cdot \frac{R_1}{\beta_2 (r_e + R_2) + R_1}$$

assuming $Q_1$ has a unity gain

$$\approx \frac{R_1}{R_2} \text{ if } R_2 \gg r_e \text{ & } \beta_2 R_2 \gg R_1 \ldots \ldots (3.18)$$

Note that by using more devices to increase the current gain, the time delay is also increased. The input resistance is similar to that of the unity gain current amplifier.
3.2 Realization for the One Amplifier Immittance Converters

Eight different kinds of one amplifier immittance converter were developed in Chapter 1. A single amplifier is used to modify the value of the capacitor to tune the antenna from the broadcast band frequency of about 0.5 MHz to 1.5 MHz, and a 10:1 ratio in the change of the capacitor value is required if the stray capacitance of the antenna is considered. The characteristics of the amplifiers suitable for the eight configurations are tabulated in Table 3.1. In the integrated circuit form, bipolar transistors will be used. From Table 3.1, the voltage controlled negative immittance converter and the current controlled negative immittance converter appear to match the characteristics of a common base bipolar transistor. It is noted that in the configurations, it is possible to realize the current gain required with very small phase delay. As shown in section 1.1.4, 1.2.3, 1.3.3 and 1.5.4, time delay can introduce parasitic immittances. From Table 1.1, for voltage controlled negative immittance converter if \( G_Y = j\omega C \) (Fig. 3.18), the time delay \( t_d \) introduces a negative conductance

\[-\omega C\theta_{IBI} (\theta_I = t_d \omega) ; \text{ if } G_Y = \frac{1}{j\omega L} \text{, a positive conductance} \frac{\theta_{IBI}}{\omega L}.\]

For the current controlled negative immittance converter, when \( G_Z = \frac{1}{j\omega C} \) (Fig. 3.19), the time delay introduces a positive resistance \( \frac{\theta_{IBI}}{\omega C} \); when \( G_Z = j\omega L \), a negative resistance \(-\omega L\theta_{IBI}\).
<table>
<thead>
<tr>
<th>Sense of Feedback</th>
<th>Voltage Controlled</th>
<th>Current Controlled</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Type</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Amplifier Employed</td>
<td>V</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>V</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>I</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>Amplifier Gain for 10:1 change in the Capacitor Value</td>
<td>0 to 0</td>
<td>0 to 0</td>
</tr>
<tr>
<td></td>
<td>-9 to +0.9</td>
<td>+9 to -0.9</td>
</tr>
<tr>
<td>Preferred Amplifier Input Impedance</td>
<td>∞</td>
<td>∞</td>
</tr>
<tr>
<td>Preferred Amplifier Output Impedance</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Preferred Amplifier Time Delay</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Table 3.1** Preferred Amplifier Characteristics for One Amplifier Impittance Converter
Fig. 3.18 A voltage controlled negative impedance converter

Fig. 3.19 A current controlled negative impedance converter

Note that the magnitude of the immittances due to the time delay \( t_d \) are proportional to the product of the phase delay \( \theta = \omega t_d \) and the amplifier gain \( B_I \). Thus \( t_d \) must be reduced so that it does not cause system instability where it introduces negative immittances; and causes minimum circuit losses, required by high \( Q \), where it introduces positive immittances.

Alternatively, the effect of time delay \( t_d \) can be shown by a vector diagram. For example, for the voltage controlled negative impedance converter (Fig. 3.18), if the amplifier has no delay, Fig. 3.20 (a) shows its vector diagram. \( C \) is the passive capacitance and \( G \) is the circuit losses represented as a conductance in parallel with \( C \). \( OP \) is the input current to a different scale. Because of positive feedback, the current amplifier introduces a current \( OP' \) \( (OP' = A \times OP, A \) is the feedback factor\) in opposite phase to \( OP \), a negative capaci-
tance \(-AC\) and a negative conductance \(-AG\). The equivalent input admittance is shown in Fig. 3.20(b). \(t_d\) will cause a phase lagging angle \(\theta_1\) as shown in Fig. 3.21(a). \(OP\) is the input current and \(OP''\), the current feedback by the amplifier, is displaced \(\theta_1\) from its initial position \(OP'\) and it introduces a negative conductance \(-G_t\). The equivalent input admittance is shown in Fig. 3.21(b).

**Fig. 3.20**
(a) Vector diagram for a voltage controlled negative immittance converter
(b) Equivalent input admittance for (a)
Fig. 3.21  (a) Vector diagram for a voltage controlled negative immittance converter with a phase delay angle $\theta_1$

(b) Equivalent input admittance for (a)

Methods of finding the overall circuit $Q$

There are two methods of finding the overall $Q$ of one amplifier immittance converter used in active tuning.

Method I:

Each circuit loss can be represented as a resistance in series with the tuned circuit or as a conductance in shunt with the tuned circuit as in Fig. 3.21 (b), where the overall circuit $Q$ can be expressed as

$$Q = \frac{\omega C}{G_{\text{total}}}$$

where $G_{\text{total}}$ is the sum of the shunt conductances.
Method II

Each circuit loss can be expressed as an angle. If the sum of the angles $\theta_{\text{total}} \leq \frac{\pi}{36}$ rad, the overall circuit $Q \approx \frac{1}{\theta_{\text{total}}}$ can be easily found by drawing a vector diagram. E.g., for Fig. 3.21 (a), the vector diagram is shown in Fig. 3.22, where $\theta_1$ is the angle due to the input resistance $r_1$ of the current amplifier and the antenna loss. $\theta_t$ is due to the time delay. OP is the input current vector and OP$''$ is the output current vector. Because of positive feedback, the resultant is OR. If $\theta_2 \leq \frac{\pi}{36}$ rad, $Q \approx \frac{1}{\theta_2}$

Fig. 3.22 Vector diagram to find the circuit $Q$ of Fig. 3.21 (a)

3.3.1 A Complete Circuit for the One Current Amplifier Negative Immittance Converter

The system diagram for the voltage controlled negative immittance converter and current controlled negative immittance converter employed to tune the antenna are shown
in Fig. 3.23 (a) and (b) respectively. They consist of a current amplifier and a current attenuator.

Note that in Fig. 3.23 (a), L is in parallel with the attenuator output and C is in series with the amplifier input while in Fig. 3.23 (b), C is in parallel with the attenuator output and L in series with the amplifier input. In Fig. 3.23 (a) L has one end grounded, but in Fig. 3.23 (b), C has one end grounded. The time delay introduces a negative conductance $-\omega Cq^B_1$ in Fig. 3.23 (a) and a positive resistance $\frac{\theta_1 B_1}{\omega C}$ in Fig. 3.23 (b). Interchanging the positions for L and C in Fig. 3.23 (a), Fig. 3.23 (b) results and vice versa.

![Diagram](image.png)

(a)  

**Fig. 3.23** A system diagram for the one amplifier negative immittance converter to tune the antenna.  
(a) Voltage controlled  
(b) Current controlled
Fig. 3.24 A complete circuit for the one amplifier negative immittance converter

The circuit realization for the voltage controlled negative immittance converter of Fig. 3.23 (a) is shown in Fig. 3.24. Interchanging the positions of L and C results the realization for Fig. 3.23 (b). Thus an additional good constant current source in parallel with C is needed to bias the collector current of Q5 in this latter case; also an additional dc blocking capacitor in series with L is required. Thus the realization shown in Fig. 3.24 is preferred.

3.2.2 A Circuit for the One Current Amplifier Positive Immittance Converter

A block diagram for a one current amplifier positive immittance converter to tune a ferrite rod antenna is shown
in Fig. 3.25. It consists of the current amplifier of Fig. 3.16 and the current attenuator of Fig. 3.15 to control the resonant frequency. A typical circuit diagram is shown in Fig. 3.26. A block diagram and an equivalent circuit are shown in Fig. 3.27. Note that the value of C (∼20 pf) used in this circuit is much smaller than for the negative immittance converter and that it may be possible to integrate it.
Fig. 3.26  A typical circuit for a one current amplifier positive immittance converter employed to tune an antenna.

Fig. 3.27  Equivalent circuits for Fig. 3.26.
The overall $Q$ of the circuit is found by the vector diagram shown in Fig. 3.28. OP is the input current vector, $\theta_1$ is due to the amplifier input resistance and the antenna loss, OP' is the output current vector with no delay and OP'' is the output current vector with a phase delay angle $\theta_t$. The resultant input current vector OR is the vector sum of OP and OP''.

If $\theta_2 \leq \frac{\pi}{36}$ rad, the overall tuned circuit $Q \approx \frac{1}{\theta_2}$.

Fig. 3.28. Vector diagram to find the circuit $Q$ of Fig. 3.26
3.3 Circuit Realization for the Gyrorator

As shown in Fig. 1.47, a gyrorator can be formed by two voltage and two current amplifiers. The block diagram of the transconductance gyrorator to tune the antenna of inductance $L_1$ is shown in Fig. 3.29.

![Block diagram of the transconductance gyrorator to tune the antenna of inductance L1](image)

Fig. 3.29 A block diagram of the transconductance gyrorator to tune the antenna of inductance $L_1$

It is now shown that the effect of the input conductance $g_{11}$, the output conductance $g_{22}$, and the phase delay $\theta$ on the Q-factor of the circuit shown in Fig. 3.29. For simplicity, parasitic immittances are neglected. Thus

$$Y_{12} \cdot Y_{21} = Y_{12} Y_{21} e^{-j\theta}$$

$$= y^2 (1 - j\theta) \text{ .................. (3.19)}$$

where $y = Y_{12} = Y_{21}$ and $e^{-j\theta} = 1 - j\theta$ for small $\theta$.

Thus the equivalent circuit for Fig. 3.29 is as shown in Fig. 3.30 whose input admittance is
Fig. 3.30 Equivalent circuit for Fig. 3.29

\[ Y_1 = Y_{11} - \frac{Y_{21} Y_{12}}{Y_{22} + Y_L} \]

\[ = g_{11} + \frac{y^2 (1-j\theta)}{g_{22} + g_{L2} + \frac{1}{j\omega L_2}} \]

After normalizing the denominator,

\[ Y_1 = g_{11} + \frac{y^2 \omega L_2 \left[ \omega L_2 (g_{22}+g_{L2}) \right]}{1 + \omega^2 L_2^2 (g_{22}+g_{L2})} + \frac{y^2 \omega L_2 \theta}{1 + \omega^2 L_2^2 (g_{22}+g_{L2})} \]

\[ + \frac{j\omega y^2 L_2 \left[ 1 - \omega L_2 \theta (g_{22}+g_{L2}) \right]}{1 + \omega^2 L_2^2 (g_{22}+g_{L2})} \] \quad \cdots (3.20)

The third term on the R.H.S. of eq. 3.20 is the conductance due to the phase delay \( \theta = \omega t_d \) and the last term is the gyrated conductance.

Eq. 3.20 can be written as

\[ Y_1 = Y_{eq} + j\omega C_{eq} \] \quad \cdots (3.21)
where

\[
Y_{eq} = g_{11} + \frac{y^2 \omega I_2 \left[ \omega I_2 (g_{22} + g_{L2}) + \theta \right]}{1 + \omega^2 I_2^2 (g_{22} + g_{L2})^2}
\]

and

\[
C_{eq} = \frac{y^2 I_2 \left[ 1 - \omega I_2 \theta (g_{22} + g_{L2}) \right]}{1 + \omega^2 I_2^2 (g_{22} + g_{L2})^2}
\]

\\........................................ (3.22)

Thus Fig. 3.30 can be further reduced to Fig. 3.31, where the total conductance

Fig. 3.31 Final equivalent circuit for Fig. 3.29

\[
\varepsilon_F = \varepsilon_{L1} + \varepsilon_{11} + \frac{y^2 \omega I_2 \left[ \omega I_2 (g_{22} + g_{L2}) + \theta \right]}{1 + \omega^2 I_2^2 (g_{22} + g_{L2})^2}
\]

\......... (3.23)

as \( \varepsilon_F \) is positive for all \( \omega \), the circuit is stable.

The overall Q of the circuit is

\[
Q = \frac{\omega C_{eq}}{\varepsilon_F}
\]

......................................................... (3.24)

as the gyrated capacitance \( C_{eq} \) decreases as \( \omega \) increases, due to \( \varepsilon_{11} \), \( g_{22} \) and \( \theta \) (see eq. 3.21), the overall Q of the circuit
is expected to fall as $\omega$ increases. When the frequency
increases to such a value that $C_{eq}$ vanishes and thereafter
becomes negative, the device no longer functions as a gyrator.
CHAPTER 4

RESULTS AND CONCLUSION

4.1 Introduction

The purpose of this chapter is to explore the range of practical results that might be expected when tuning systems using the immittance converters discussed in the previous chapter are realized as integrated circuits. The first section deals with the results that have been obtained from practical realization of the basic building blocks of the immittance converters. The second section shows how the overall performance of the tuning system using immittance converters to tune a ferrite rod antenna is governed by the performance of the building blocks. Finally, some conclusions are drawn about the most suitable form of immittance converter for tuning broadcast band receivers.

4.1.1 Circuit Parameters

The circuit parameters of several practical realization of the building blocks have been measured. The input resistance, output resistance and time delay, where applicable, of the unity gain voltage amplifier, current amplifier, cascode form current attenuator and constant current source are tabulated in Table 4.1. Note that the input resistance $R_i$ of
<table>
<thead>
<tr>
<th>Item</th>
<th>Parameters</th>
<th>Measured Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>input resistance of the unity gain voltage amplifier (Fig. 3.5)</td>
<td>3M Ω</td>
<td>measured at 1 KHz</td>
</tr>
<tr>
<td>2</td>
<td>input resistance of the unity gain current amplifier (Fig. 3.11); the output resistance of the voltage amplifier (Fig. 3.5)</td>
<td>0.25 Ω</td>
<td>dc value, for frequency characteristic see Fig. 4.1</td>
</tr>
<tr>
<td>3</td>
<td>output resistance of the cascode form constant attenuator (Fig. 3.15)</td>
<td>≈10M Ω</td>
<td>measured at low frequency</td>
</tr>
<tr>
<td>4</td>
<td>output resistance of the cascode form constant current source (Fig. 3.10 c)</td>
<td>≈10M Ω</td>
<td>measured at low frequency</td>
</tr>
<tr>
<td>5</td>
<td>unloaded Q of the ferrite rod antenna</td>
<td>≈150</td>
<td>measured at 1 MHz, for frequency characteristic see Fig. 4.2</td>
</tr>
<tr>
<td>6</td>
<td>time delay of the unity gain voltage amplifier (Fig. 3.5)</td>
<td>3 nS ± 25%</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>time delay of the unity gain current amplifier (Fig. 3.11)</td>
<td>2 nS ± 25%</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>time delay of the current attenuator (Fig. 3.15)</td>
<td>2 nS ± 25%</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>time delay of the antenna tuning system using a two amplifier immittance converter (Fig. 3.1)</td>
<td>6 nS ± 25%</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>time delay of the antenna tuning system using one amplifier negative immittance converter (Fig. 3.24)</td>
<td>4 nS ± 25%</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>time delay of the antenna tuning system using one amplifier positive immittance converter (Fig. 3.26)</td>
<td>4 nS</td>
<td></td>
</tr>
</tbody>
</table>
the current amplifier \((I_{C1} \approx 1 \text{ mA} \text{ Fig. 3.11})\) is approximately 
0.26 \( \Omega \) from zero \( H_z \) to 40 \( \text{KH}_z \) and then rises to 4\( \Omega \) at 
400 \( \text{KH}_z \) and 28\( \Omega \) at 1.6 \( \text{MH}_z \). At low frequency from 0-40 \( \text{KH}_z \), 
the measured results agree closely with the calculated value 
(sect. 3.1.4), but above 40 \( \text{KH}_z \) they do not. 
Assuming \( r_1 \propto \frac{1}{I_{C1}} \), then \( r_1 \) between 1\( \Omega \) and 40\( \Omega \) at 400 \( \text{KH}_z \) 
and between 7\( \Omega \) and 280\( \Omega \) at 1.6 \( \text{MH}_z \) can be obtained by 
varying \( I_C \) from 0.10 mA to 4 mA. The time delay of the 
voltage amplifier, current amplifier and current attenuator 
are respectively 3 nS, 2 nS & 2 nS. They are subject to variations 
from about 0.2 nS upwards depending on the \( \beta \) cut-off frequency 
and wiring (the integrated circuit will reduce the wiring 
delay drastically). Thus it is expected that the time delay 
for an antenna tuning system using a one amplifier immittance 
converter can be reduced to less than \( \frac{1}{3} \) nS.

4.1.2 Performance Curves for One Amplifier Immittance 
Converters

It has been shown that it is possible to achieve in 
wide range input impedance, output impedance and time delay 
for practical immittance converters. e.g. the input impedance 
may be in the order of 30\( \Omega \) if no special precautions are 
taken to reduce it. If special precautions are taken input 
impedances considerably lower than 1\( \Omega \) can be achieved. The 
parameters of the final circuit may thus be chosen on the 
basis of the design compromises and the degree of complication 
acceptable.
This section will study the effect of the important parameters of the immittance converter on the final circuit Q and its stability.

(I) One Amplifier Negative Immittance Converter (Fig. 3.24)

Fig. 4.3 shows the effect of time delay $t_d$, input resistance $r_1$ of the current amplifier and the antenna loss (see Fig. 4.2) on the overall Q of the circuit. As $t_d$ changes from $\frac{1}{2}$ nS to 1 nS and 2nS, it has a predominant effect on the circuit Q. Because a capacitance range of 10:1 is required to cover the frequency range from 0.4 MHz to 1.6 MHz, the feedback factor $A$ increases from a small fraction to close unity. As shown by the vector diagram of Fig. 3.22, the circuit Q is very sensitive to time delay when $A$ is close to unity. The circuit Q increases as time delay increases and it runs into oscillations when OR crosses the 90° axis. e.g., for $t_d = 2$ nS, $Q \approx 1000$ at 1.2 MHz and the circuit tends to oscillate.

Fig. 4.4 and Fig. 4.5 indicate that for a one amplifier negative immittance converter to have the required circuit Q shown in the figures, the input resistance $r_1$ must have the characteristic shown, i.e. increasing from 17 $\Omega$ to 69 $\Omega$ (Fig. 4.4) and from 45 $\Omega$ to 615 $\Omega$ (Fig. 4.5) as the frequency in increased from 400 KHz to 1.6 MHz. The ripple of $r_1$ is due to the combined effect of time delay and antenna loss.
(II) **One Amplifier Positive Immittance Converter (Fig. 3.26)**

Fig. 4.6 shows the effect of time delay $t_d$, the input resistance $r_1$ of the current amplifier and the antenna loss (Fig. 4.2) on the overall circuit $Q$ of the one amplifier positive immittance converter used to tune the antenna. As time delay introduces a loss factor, the maximum $Q$ is always less than the $Q$ of the antenna loaded by $r_1$, which is shown by the dotted curve in the Figure. The sag in the middle of the curve is due to the effect of time delay (see Fig. 3.28).

As the feedback factor $A$ decreases from 14.6 at 400 KHz to zero at 1.6 MHz (i.e. the time delay has no effect on the circuit $Q$ at 1.6 MHz and all curves meet at one point at 1.6 MHz.)

4.2 **Concluding Remarks**

From the foregoing sections, it is noted that there are commonalities between the two new forms of immittance converter, the current amplifier negative immittance converter and the current amplifier positive immittance converter, when used to tune an antenna, as follows:

1. Both use amplifiers whose port characteristics are similar to those of a common base bipolar transistor.

2. It is possible to obtain the overall circuit $Q$ required, with normal value of input resistance of the amplifier and in many cases no special precautions are needed to reduce it to a very low value.
3. Since the antenna signal is circulated by the amplifier system, no other amplifiers need be connected to the antenna. The signal can be taken directly from the immittance converter amplifier. This applies to all immittance converters treated in this thesis.

In addition, the current amplifier negative immittance converter has the following attraction. The inductance \( L \) provides a path for the direct current of \( Q_2 \) (see Fig. 3.24) and \( C \) blocks the dc supply voltage from reaching \( Q_2 \) emitter, in addition of being resonating elements. As a result, the integrated form of it becomes a simple and elegant circuit.

However, it has the following major disadvantage. Only a limited capacitance range can be obtained depending on the operating frequency and the circuit parameters. Because a large capacitance range needs a feedback factor \( A \) close to unity, the circuit \( Q \) becomes sensitive to the time delay (see Fig. 3.22 and Sect. 4.1.2) and other circuit parameters. Thus, as \( A \) approaches unity, \( Q \) may rise to infinity (depending on circuit parameters) and the circuit may oscillate. The useful capacitance range is limited by the circuit stability and sensitivity.

The above disadvantage of the negative immittance converter does not apply to the current amplifier positive immittance converter which has the following advantages:

1. It is a stable circuit because time delay introduces only a \( Q \) loss and it can have a larger stable capacitance
range than that of the negative immittance converter.

2. The normal input resistance of the current amplifier without impedance reducing tricks can be used.

However, it has the following problems associated with it, although they are not serious, they must be overcome to obtain satisfactory system performance:

1. The current amplifier must have a fixed stable gain of approximately 10 to provide the required capacitance range. e.g., in the circuit of Fig. 3.26, any changes in $R_1$, $R_2$ or $r_e$ of $Q_2$ will change the fixed gain and thus its resonanting frequency. Any change in gain will interfere with the tracking (see sect. 2.1.4).

2. Since the amplifier gain is higher than in the previous case, the time delay through the circuit is also greater.

The thesis has shown that the current forms of immittance converter appear to meet the requirements of a tuning system for fully integrated circuit broadcast receivers. However, the detailed design of the amplifiers and the noise problems the system may introduce have not been studied and further work in this direction is required before these immittance converters can be applied to practical integrated broadcast receivers.
Fig. 4.1 Input resistance of the current amplifier and output resistance of the voltage amplifier against frequency

\[ I_C = 1 \, mA \]
Fig. 4.3 - Q-factor of the one current amplifier negative immittance converter used to tune a ferrite rod antenna.

C=260 pF, L=0.7 mH, r1 = 64 Ω,

unload Q of antenna (Fig. 4.2)

(1) \( t_d = \frac{1}{2} \) nS
(2) \( t_d = 1 \) nS
(3) \( t_d = 2 \) nS
Fig. 4.4. Input resistance $r_1$ of the current amplifier against frequency for the required $Q$, $C=470$ pF, $L=0.7$ mH, $t_d=1$ nS, unloaded $Q$ of the antenna (Fig. 4.2)
Fig. 4.5 Input resistance $r_1$ of the current amplifier for the required $Q$.
$C=470 \, \text{pF}$, $L=0.7 \, \text{mH}$, $t_d=4 \, \text{nS}$.
Unloaded $Q$ of antenna (Fig. 4.2).
Fig. 4.6  Q-factor of the one current amplifier positive immittance converter used to tune a ferrite rod antenna. $C=14.5 \, \text{pF}$, $L=0.7 \, \text{mH}$, $r_1 = 37 \, \Omega$.

Unloaded Q of antenna (Fig. 4.2) (1) $t_d=1 \, \text{nS}$
(2) $t_d=2 \, \text{nS}$ (3) $t_d=4 \, \text{nS}$
REFERENCES


0.2 Grebene, A. B., "A Monolithic Phase-Locked Filter/Demodulator", a technical report of signetics, California. (Signetic Part No. E-5021)


Chapter 1

1.1 Merrill, J. L., "Theory of the Negative Impedance Converters", The Bell System Journal, pp. 89-109, January 1951

1.2 Linvill, J. G., "Transistor Negative-Impedance Converters", Proceedings of IRE, pp. 725-730, June 1953


1.4 Lundy, W. R., "Negative Impedance Circuits - Some Basic Relations and Limitations", IRE Trans. on Circuit Theory, pp. 132-139, September 1957

1.5 Yanagisawa, T., "RC Active Networks Using Current Inversion Type Negative Impedance Converters", IRE Trans. on Circuit Theory, pp. 140-144, September 1957


1.10 Larky, A. I., "Negative-Impedance Converters", IRE Trans. on Circuit Theory, pp. 124-131, September 1957


1.16 Tellegen, B. D. H., "The Gyrator, a New Electric Network Element", Phillips Research Reports, 3, 81, 1948


1.18 Haykin, S. S., "Active Network Theory", Addison-Wesley, 1970, pp. 176-190


Chapter 2

2.1 Thompson, P. M., Yap, C. S., Peil, W., "Impedance Converters for Tuning Ferrite Rod Antenna", IEEE International Solid-State Circuits Conference, Pennsylvania, 1970


Chapter 3


3.3 "RCA Linear Integrated Circuit", Circuits Technical Series IC-41, pp. 135-142

VITA

NAME: Cho-Sing Yap

BORN: Bahau, N.S., Malaysia
August 3, 1937

EDUCATION: Primary - Chi Wen Public Primary School
Bahau, N.S., Malaysia

Secondary - The Singapore Chinese High School,
Singapore

University - Graduate of the Institution of
Electronic and Radio Engineers,
England, 1966

University of Ottawa, Ontario,
Canada

Course - Electrical Engineering
Degree - B.A.Sc., 1968

PUBLICATION:

P.M. Thompson; C.S. Yap; W. Peil, "Impedance
Converters for Tuning Ferrite Rod Antenna",
I.E.E.E. International Solid-State Circuits